

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 7,279,708

Inter Partes Review No. IPR2025-01557

DECLARATION OF DR. JERZY KANICKI

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Exhibit List

Exhibit Description	Exhibit #
U.S. Patent No. 7,279,708 to Kwak et al.	1001
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Prosecution History of U.S. Patent No. 7,279,708	1003
U.S. Pub. No. 2004/0115989 to Matsueda et al.	1004
U.S. Pub. No. 2003/0194484 to Yamazaki	1005
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U.S. Pub. No. 2002/0153611 to Nakanishi	1007
U.S. Patent No. 6,815,903 to Nakanishi	1008
U.S. Patent No. 7,330,168 to Anzai	1009
U.S. Patent No. 6,949,883 to Matsueda	1010
U.S. Patent No. 6,106,923 to Takahashi	1011
Japanese Pub. No. 1992/017393	1012
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Declaration of Eric Vance	1014

I, Jerzy Kanicki, make this declaration in connection with the proceeding identified above.

I. INTRODUCTION

1. I have been retained as an expert witness on behalf of BOE Technology Group Co., Ltd. (“Petitioner” or “BOE”) to provide expert opinions on the patentability of United States Patent No. 7,279,708 (“the ’708 patent”).

2. I am being compensated at my normal rate, plus reimbursement for expenses, for my analysis. My compensation does not depend on the content of my opinions or the outcome of this proceeding.

II. QUALIFICATIONS

3. In formulating my opinions, I have relied upon my knowledge, training, and experience in the relevant art. My qualifications are stated more fully in my curriculum vitae, which has been provided as Appendix A. Here, I provide a brief summary of my qualifications.

4. I am currently a Professor in the Department of Electrical Engineering and Computer Science (EECS) at the University of Michigan, Ann Arbor, Michigan. I have studied, taught, and practiced in flat panel displays (FPDs) and integrated circuits (ICs) fabrication for over 25 years, including design, thin film depositions, processing, fabrication, and photolithography of devices and circuits used in both applications. The flat panel displays include, for example, active-

matrix liquid crystal displays, (AM-LCDs), active-matrix organic light emitting displays (AM-OLEDs) and other light transmissive, reflective, and emitting display technologies. I received my Doctorate of Science (D.Sc.) from the Free University of Brussels, Belgium in 1982. My educational background also includes a B.S. (1976) and M.S. (1978) in Chemistry from the Free University of Brussels, Belgium.

5. Since 1995, I have been a member of the faculty at the University Of Michigan College Of Engineering, Ann Arbor, Michigan. During that period, I have held the position of Professor in the Department of Electrical Engineering and Computer Science (EECS). Between 1995 and 1999, I was group team leader within the University of Michigan Center of Display Technology and Manufacturing. For a number of years, I also held the position of Professor in the Program of Macromolecular Science and Engineering (2000-2011), and Applied Physics. During my tenure at the University of Michigan, I have conducted leading work on various flat panel displays, device and circuit fabrication technologies, including, for example, design for various devices and integrated circuits to be used with flat-panel displays (active-matrix arrays including pixel circuits for AM-LCDs and AM-OLEDs, data and gate drivers chips, and associated electronics), x-ray and optical imagers (pixel circuits, driving and readout chips, and associated electronics), chemical sensors (readout chips), solar cells (DC/AC

converters), and fingerprint sensors (driving circuits and readout chips). As a faculty member, over the years I have graduated several PhD dissertations in the field of flat panel displays, semiconductor devices, and circuits. Upon graduation, my PhD graduate students have moved either into industrial positions in the displays and electronics industries or into academic positions in the U.S. or abroad.

6. I have taught several different courses at the undergraduate and graduate levels, including Solid-State Technology Laboratory and Digital Integrated Circuit Technologies, within the EECS department at the University of Michigan. These courses generally covered the physics, technology, design, and fabrication of solid-state devices and integrated circuits. I have also introduced two new courses, including “Flat Panel Displays” and “Thin Film Devices Technology” in 1997, which are still being offered annually. These courses have generally covered the thin-film devices and circuits technologies used in different applications including AM-OLEDs. As a faculty member, I direct at any given time the research of several graduate and undergraduate students in Solid-State Devices and Nanotechnology, including semiconductors, electronic materials, devices, and circuits for various applications including FPDs. As part of my group research, I utilize the University of Michigan Lurie Nanofabrication Facility (LNF), <https://lnf.umich.edu/>, that among others has the capability to fabricate and test devices and circuits used in the FPDs and IC industries. Moreover, over the

years I have also supervised the research of several post-doctoral fellows and visiting scientists from industry or/and other universities within my group doing research in the area of the solid-state devices and circuits. More information about my professional activities can be found on my research group web page:

www.eecs.umich.edu/omelab/.

7. From 1983 to 1995, I was a Research Staff Member at the IBM T.J. Watson Research Center in Yorktown Heights, New York, involved in the research and development of flat panel display materials, devices, circuits, driving electronics, and manufacturing methods. During that period, I was a member of a team that developed the first IBM active-matrix liquid-crystal displays (AM-LCDs) manufacturing technology, leading to the introduction of the first color laptop computer (CL57-SX) on March 24, 1992. I, among others, was also responsible at IBM for the initial fundamental understanding of device physics and pixel design approaches used for, and manufacturing methods of, certain AM-LCDs for IBM's ThinkPad laptop computers.

8. From 2002 to 2003, I was on sabbatical at the University of California Santa Barbara (UCSB) within the Center for Polymers and Organic Solids. My research was related to organic polymer thin-film transistors, organic light-emitting devices, and electrically injected lasers. My host was Professor Alan J. Heeger from Physics Department. He won the Nobel Prize for Chemistry in 2000 along

with *Alan* G. MacDiarmid and Hideki Shirakawa “for their discovery and development of conductive polymers.”

9. From 2009 to 2010, I was on sabbatical at the University of California Sand Diego (UCSD) within the California Institute for Telecommunications and Information Technology. My research was related to organic polymer thin-film transistor chemical sensors, amorphous InGaZnO thin-film transistors, image sensors and solar cells. My host was Professor Andrew C. Kummel from the Department of Chemistry and Biochemistry.

10. From 2018 to 2019, I was on sabbatical at the Massachusetts Institute of Technology within Microsystems Technology Laboratories. My research was related to hydrogenated diamond devices and circuits, and Perovskites materials based on opto-electronic devices. My host was Professor Jesus del Alamo from Department of Electrical Engineering and Computer Science.

11. From 2024 to 2025, I was on sabbatical at the Massachusetts Institute of Technology within Research Laboratory of Electronics (RTL). My research was related to pixel driving circuits for micro-LEDs and micro-LEDs fabrication and integration with the backplane electronics based on CMOS, low temperature polycrystalline silicon thin film transistors (poly-Si TFTs) or amorphous InGaZnO (a-IGZO) TFTs. My host was Professor Jeehwan Kim of the

Department Materials Science and Engineering and Mechanical Engineering, respectively.

12. I am a member of several professional organizations including the Society for Information Display (SID) and the Institute of Electrical and Electronics Engineers (IEEE). My areas of expertise include chemistry, solid-state physics, material sciences, device physics, circuits, solid-state device and circuit fabrication / manufacturing methods, and nanotechnology. I have edited or co-edited several books, authored over 300 technical papers, and given over 350 presentations (among which over 70 were invited presentations) relating to thin film semiconductor devices, circuits, and associated FPD technologies. My papers have received over 12,000 citations, and I have an H-index of 60, i10-index of 204, RG score of 42.30 and D-index of 51. I was included in World Best Scientist 2025 and ranked 886 in the US and 2316 in the world, respectively. To be ranked you have to meet the D-index inclusive threshold typically between 30 – 70 depending on discipline. I have also been the chair or co-chair at numerous national and international FPD conferences and symposia. I was an editor for IEEE Transactions on Electron Devices for eight years, and I am a reviewer for several prestigious international archival journals. I am also a reviewer of proposals for several federal agencies, such as the National Science Foundation (NSF), Department of Defense (DoD), and Defense Advanced Research Program Agency

(DARPA). Among other distinctions, I was awarded the IBM External Honors, which recognizes the technical leadership of staff members in IBM's Research Division, three times. My research work at the University of Michigan has been supported by grants from the state of Michigan, federal agencies, and several international industries.

III. MATERIALS CONSIDERED

13. In preparing this declaration, I have reviewed, among other things, the '708 patent and file history. I have also considered each of the documents cited in this Declaration and the documents specifically identified in the Exhibit List. In formulating my opinions, I have further relied upon my extensive experience in the relevant fields.

IV. SUMMARY OF THE '708 PATENT

A. Filing And Priority Dates

14. The '708 patent was filed on May 29, 2005, published on March 23, 2006, and issued on October 9, 2007. The '708 patent claims priority to Korean patent application 10-2004-0038735, which was filed on May 29, 2004.

B. Specification And Claims

15. The '708 patent is titled "Electroluminescence Display Device and Method of Manufacturing the Same." The '708 patent discloses "[a]n electroluminescence (EL) display device." (EX1001, Abstract.)

16. The '708 specification explains that “[a]s resolution of images displayed on the display device increases and the display device becomes larger, there is a need to reduce power consumption and improve aspects of image quality such as brightness. One of the methods is to reduce resistances of various wires through which power is supplied to the display area. Examples of such wires include the driving power supply line and the electrode power supply line.” (EX1001, 1:66-2:6.)

17. The '708 specification states that “having an electrode that is electrically contacted to a cathode through a wide contacting portion between a terminal and a cathode” can reduce the contact resistance, and “the image quality can be improved.” (EX1001, 2:7-13.) However, “most of an insulating layer on an upper portion of the terminal is removed and the terminal is excessively exposed. Thus, the layer constituting the terminal may be peeled or damaged seriously in a subsequent process. In addition, an over coat layer that is made of an acryl-based resin is disposed on a lower portion of the electrode formed of the same oxide material as the anode, and the discharge path of gas generated from the over coat layer is blocked or lengthened by the electrode. Thus, the gas cannot discharge well, defects may occur, and time for processing may increase.” (EX1001, 2:14-24.)

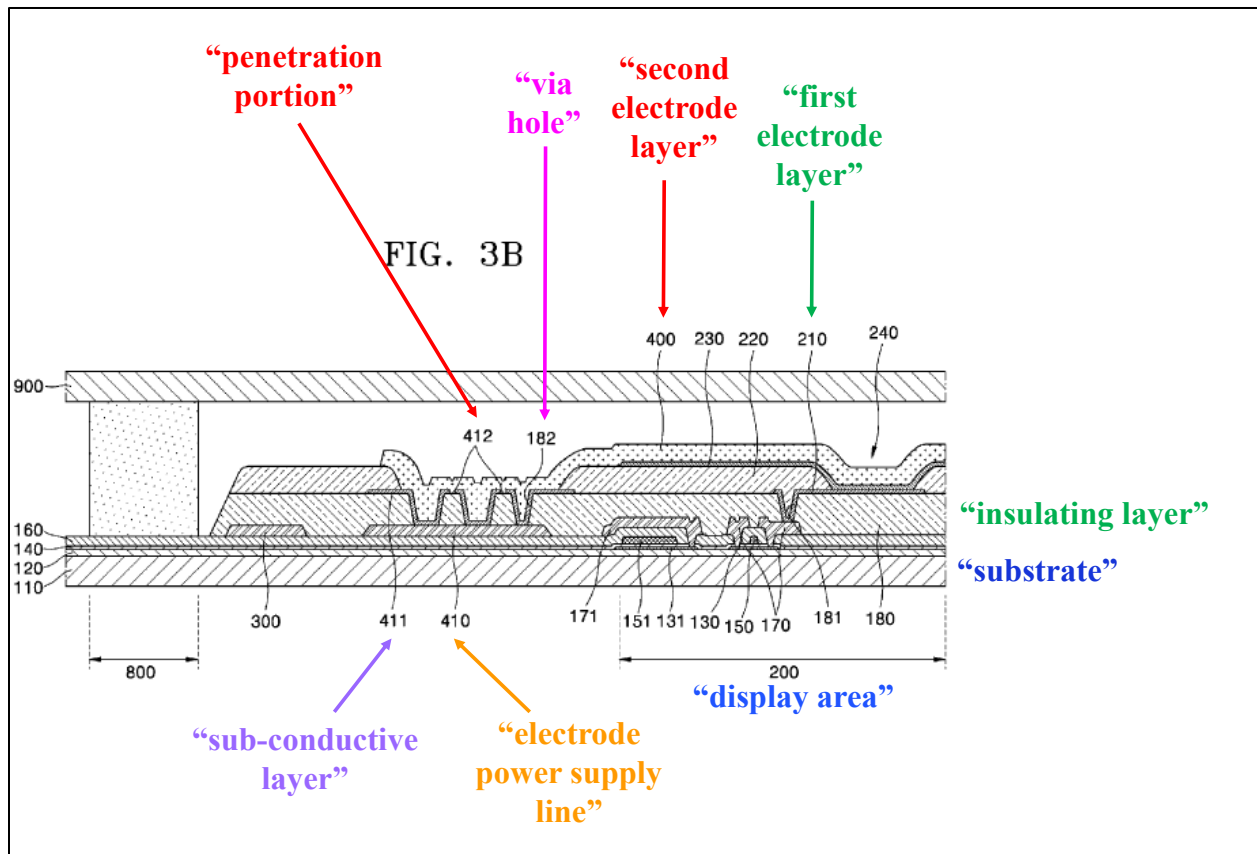
18. This is explained in other parts of the specification: “the sub-conductive layer 411 may be formed on the surface of the insulating layer 180 including the via hole 182. . . . Since the insulating layer 180 extends between the electrode power supply line 410 and the sub-conductive layer 411 (except for the via hole 182), peeling of the electrode power supply line 410 can be prevented.” (EX1001, 6:27-36.) “One or more penetration portions 412 may be formed on the sub-conductive layer 411 that is on the insulating layer 180. As shown in FIG. 2D, after forming the penetration portion 412 on the sub-conductive layer 411, the stacked portions on the substrate undergo an annealing process under a vacuum environment for a predetermined period. This annealing can serve to discharge the gas such as benzaldehyde, benzyl alcohol, benzene-based compounds that can be generated from the insulating layer 180 containing an organic layer. Thus, the insulation can be saved from being damaged by the gas.” (EX1001, 6:57-67.)

19. Figure 3B (annotated below) shows a cross-sectional view of the EL display device. The '708 patent claims are directed to an EL display device and manufacturing thereof. Independent claim 1 is directed to the EL device, which comprises:

- a *display area 200* with pixels that have a *first electrode layer 210* and a *second electrode layer 400* on a *substrate 110* and an

electroluminescence unit formed between the first electrode layer and the second electrode layer;

- an *electrode power supply line 410* to supply electrode power to the display area;
- an *insulating layer 180* disposed on the electrode power supply line, including a *via hole 182* and containing an organic material; and
- a *sub-conductive layer 411* formed on the insulating layer including the via hole along the electrode power supply line,
- wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and the sub-conductive layer on the insulating layer includes a *penetration portion 412*.



20. Independent claim 9 is also directed to an electroluminescence display device. It has limitations like claim 1 and further requires the sub-conductive layer comprise a plurality of unit sub-conductive layers.

21. Independent claim 11 is directed to a method of manufacturing an electroluminescence display device and includes forming the limitations recited in independent claim 1. Independent claim 15 is like independent claim 1 but does not require forming a penetration portion.

22. Dependent claims 2-4, 12, and 14 are directed to the sub-conductive layer comprising the same layer as the first electrode layer and comprising two penetration portions and associated forming steps. Dependent claims 5 and 6 are

require the penetration portion comprise a penetration hole and a line type penetration portion. Dependent claims 7 and 8 are directed to a thin film transistor layer. Dependent claims 10 and 14 relate to distances. And dependent claim 13 is directed to via holes.

C. Prosecution History

23. I understand that during prosecution of the '708 patent, the Examiner issued a Non-Final Office Action on January 29, 2007 that objected to the drawings for not showing the limitations of claim 10. (EX1003, 222.) The Examiner also rejected claim 10 for being indefinite and claims 11-15 for being incomplete. (EX1003, 223.) Claims 1-9 were indicated as allowed. Claim 10 was indicated as allowable but objected to for being dependent upon a rejected base claim. (EX1003, 223.)

24. On April 17, 2007, Applicant responded by submitting a replacement figure sheet for Figure 6B, and amending claims 11 and 15 by amending “forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole” and adding two limitations:

- “forming an organic EL unit on the first electrode layer; and”
- “forming a second electrode layer on the organic EL unit.”

25. On May 30, 2007, the Examiner issued a Notice of Allowance stating that the primary reason for the allowance is because of the “sub-conductive layer

formed on an insulating layer including a via hole along an electrode power supply line” and the “sub-conductive layer on the insulating layer includes a penetration portion” limitations. (EX1003, 195-196.)

V. RELEVANT LEGAL STANDARDS AND DEFINITIONS

A. Anticipation

26. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in a single prior art reference or system. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily or implicitly present in the allegedly anticipating reference and that it would have been so recognized by a POSITA. In addition, I understand that an enabling disclosure is a disclosure that allows a POSITA to make the invention without undue experimentation. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the primary reference has enabling disclosure, to explain the meaning of a term used in the primary reference, and/or to show that a characteristic is inherent in the primary reference.

B. Obviousness

27. I understand that a claim is unpatentable if the differences between the claimed subject matter and the prior art are such that the subject matter as a whole would have been obvious at the time the claimed subject matter was made to a

POSITA to which the subject matter pertains. I understand that a patent claim may be obvious to a POSITA in view of the prior art teachings of a single reference or a combination of references.

28. To assess obviousness, I understand that I am to consider the scope and content of the prior art, the differences between the prior art and the claim, the level of ordinary skill in the art, and any secondary considerations to the extent they exist.

29. It is also my understanding that there are principles that may be used as further guidance in an obviousness analysis (especially when considering combinations of references), which include considering whether:

- the claimed subject matter is simply a combination of prior art elements according to known methods to yield predictable results;
- the claimed subject matter is a simple substitution of one known element for another to obtain predictable results;
- the claimed subject matter uses known techniques to improve similar devices or methods in the same way;
- the claimed subject matter applies a known technique to a known device or method that is ready for improvement to yield predictable results;

- the claimed subject matter would have been “obvious to try” choosing from a finite number of identified, predictable solutions, with a reasonable expectation of success;
- there is known work in one field of endeavor that may prompt variations of it for use in either the same field or a different one based on design incentives or other market forces if the variations would have been predictable to a POSITA;
- there existed at the time of conception and reduction to practice a known problem for which there was an obvious solution encompassed by the patent’s claims; and
- there is some teaching, suggestion, or motivation in the prior art that would have led a POSITA to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed subject matter.

30. I understand that there are secondary considerations that may tend to show that a claimed invention would not have been obvious to a POSITA. These include, for example, commercial success, long-felt but unsolved needs, failure of others, and unexpected results. I further understand that there must be a relationship, or nexus, between any secondary considerations and the novelty of the claimed invention.

VI. LEVEL OF ORDINARY SKILL IN THE ART FOR THE '708 PATENT

31. I am informed and understand that various factors can be considered in determining a person of ordinary skill in the art (POSITA). I am informed and understand that those factors include: (1) the educational level of the inventors; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the field.

32. A person of ordinary skill in the art (POSITA) in the field of the '708 patent would have a bachelor's degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable about OLED materials, and display pixel design, layout, and operation.

33. I agree with this level of ordinary skill for the '708 patent. Based on my experience, I understand and know of the capabilities of a person of this skill level as of the time the '708 priority application was filed in 2004. I am familiar with how a POSITA would have understood and used the terminology found in the '708 patent at the time of the filing of the priority application, and with the state of the art at that time.

VII. CLAIM CONSTRUCTION

34. I have been informed that claim construction requires consideration of the words of the claims themselves, the specification, the prosecution history, and extrinsic evidence concerning relevant scientific principles, the meaning of technical terms, and the state of the art. I have also been informed that the specification is usually definitive, as it is the single best guide to the meaning of a disputed term.

35. I have been informed that, in the context of this proceeding, Petitioner did not propose any terms for construction. Instead, Petitioner believes each of the terms of the '708 patent carries its ordinary and customary meaning, which is the meaning that the term would have to a POSITA. I agree with Petitioner and apply the ordinary and customary meaning of the terms in my analysis below.

VIII. PRIOR ART

36. I understand that each of the references discussed herein qualifies as prior art against the '708 patent:

37. U.S. Publication No. 2004/0115989 A1 ("Matsueda," EX1004) was filed on August 11, 2003, claims priority to Japanese patent applications filed on September 25, 2002 and August 4, 2003, and published on June 17, 2004.

38. U.S. Publication No. 2003/0194484 A1 ("Yamazaki," EX1005) was filed on April 9, 2003 and published on October 16, 2003.

39. U.S. Publication No. 2002/0021266 A1 (“Koyama,” EX1006) was filed on April 17, 2001 and published on February 21, 2002.

40. U.S. Publication No. 2002/0153611 A1 (“Nakanishi,” EX1007) was filed on April 22, 2002, claims priority to a Japanese patent application filed on April 24, 2001, and published on October 24, 2002.

IX. ANALYSIS AND OPINION

A. Claims 1-5, 7, And 9-15 Are Obvious Over Matsueda

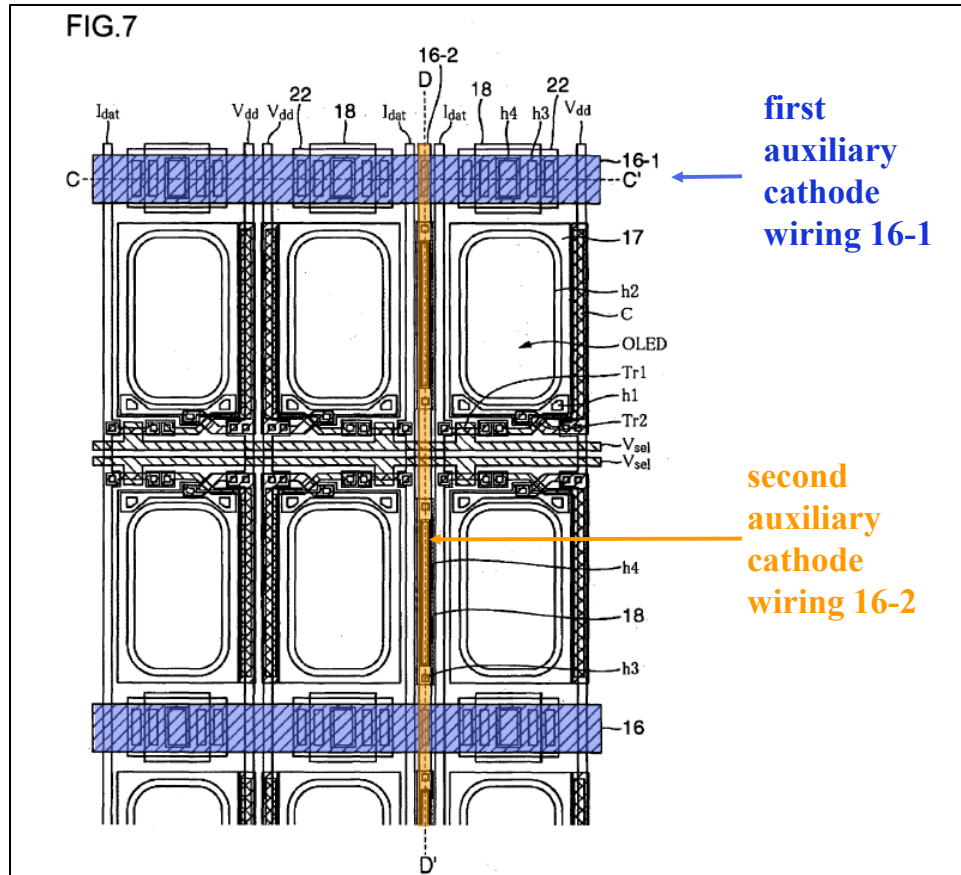
1. Summary of Matsueda

41. Matsueda is titled “Electro-Optical Apparatus, Matrix Substrate and Electronic Equipment.” (EX1004, Title.) It discloses an “electro-optical apparatus” including an organic EL display panel 100. (EX1004, Abstract, [0048].)

42. Matsueda explains that “[t]he wiring resistance of the common electrode is an issue in realizing a display panel using the electro-optical devices. Specifically, a higher wiring resistance of the common electrode leads to an increased voltage drop in pixels in the center of the screen, thereby failing to supply sufficient current to the central part of the screen.” In AMOLED displays, the common electrode may be a shared continuous electrode layer that spans the display and serves as the carrier contact injection for the organic light emitting diodes (OLEDs) in the panel. Consequently, “a gray-scale is not displayed accurately and display performance decreases. This matter may become a serious

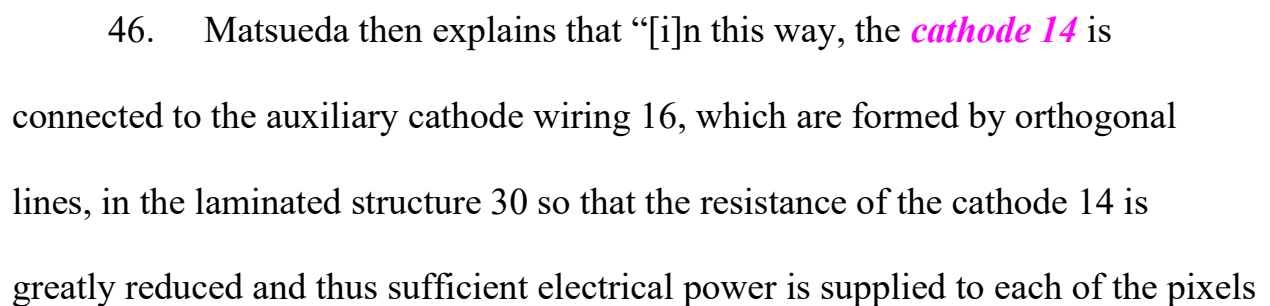
problem in a larger display panel because the wiring resistance of the common electrode becomes higher.” (EX1004, [0005].)

43. Matsueda thus discloses “the present invention provides an electro-optical apparatus and a matrix substrate having a structure for power-supply wiring that is capable of providing a sufficient power to a common electrode of electrooptical devices.” (EX1004, [0006].) The power-supply wiring is referred to as the auxiliary cathode wiring 16, shown in Figure 7 (below). “[T]he auxiliary cathode wiring 16 disposed along the row direction are called *first auxiliary cathode wiring 16-1*, while the auxiliary cathode wiring 16 disposed along the column direction are called *second auxiliary cathode wiring 16-2*.” (EX1004, [0064].) The auxiliary cathode wiring (also called auxiliary metal) may address a challenge related to voltage drop (IR drop) across the OLED cathode layer. The cathode is typically a thin transparent conductive layer having a high resistance. Current flows horizontally through the cathode from each pixel to the edge mounted cathode contact pads. In large displays, this causes a voltage gradient resulting in display brightness non uniformity. To address this issue, auxiliary cathode wiring was introduced. One example of possible solution is described in Matsueda.



44. A POSITA would have known that auxiliary cathode wiring (sometimes referred to as the cathode auxiliary metal) may be used to address issues related to voltage drop (IR drop) across the OLED cathode layer. The cathode may be a thin transparent conductive layer having a high resistance. Current may flow horizontally through the cathode from each pixel to the edge mounted cathode contact pads. In a large display, this may cause a voltage gradient resulting in display brightness non uniformity. To address this issue, auxiliary cathode wiring may be used.

45. Figures 8 and 9 (annotated below) show cross-sectional views of the power-supply wiring for the electro-optical apparatus. The “laminated structure 30 in which the first auxiliary cathode wiring 16-1, insulating interlayer film 21, a planarizing film 20, source metal layers 22, ITO layers 18, and a bank layer 19 are sequentially laminated, is formed on the display area 11 and on the substrate 15. The upper surface of the laminated structure 30 is covered with the film of a cathode 14.” (EX1004, [0067].) “On the *planarizing films 20*, the *islanded ITO layers 18* are disposed in a direction in which the *first auxiliary cathode wiring 16-1* extend at multiple positions and are connected to the source metal layers 22 through contact holes h3. The bank layer 19, which is made of a photosensitive organic material or the like is formed on the planarizing films 20. . . . In the surface of the bank layers 19, contact holes h4, which are aligned precisely at multiple positions communicating to the ITO layers 18, are disposed in the direction in which the *second auxiliary cathode wiring 16-2* extend.” (EX1004, [0069].)



10. Therefore, the luminance non-uniformity resulting from non-uniformity of the currents supplied to the pixels 10 is reduced, achieving enhanced or excellent display performance.” (EX1004, [0070].)

2. Claim 1

a. Preamble: “An electroluminescence display device, comprising:”

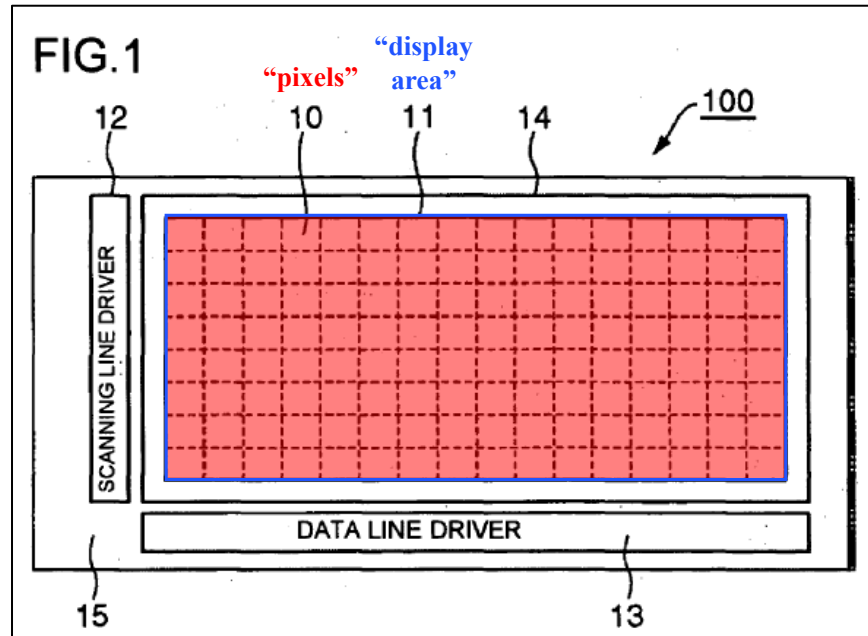
47. Matsueda teaches “[a]n electroluminescence display device.” For example, Matsueda discloses “FIG. 1 is a schematic of an active-matrix-type organic EL display panel 100 of the exemplary embodiment.” (EX1004, [0047].) Matsueda also discloses “FIG. 7 shows the layout of wiring in an organic EL display panel 100 according to a third exemplary embodiment of the present invention.” (EX1004, [0064].)

b. 1[a]: “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

48. Matsueda teaches “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer.” For example, Matsueda discloses “[a]s illustrated in FIG. 1, a plurality of pixels 10, a scanning line driver 12, and a data line driver 13 are disposed on or above a substrate 15. *The plurality of pixels 10 have laminated*

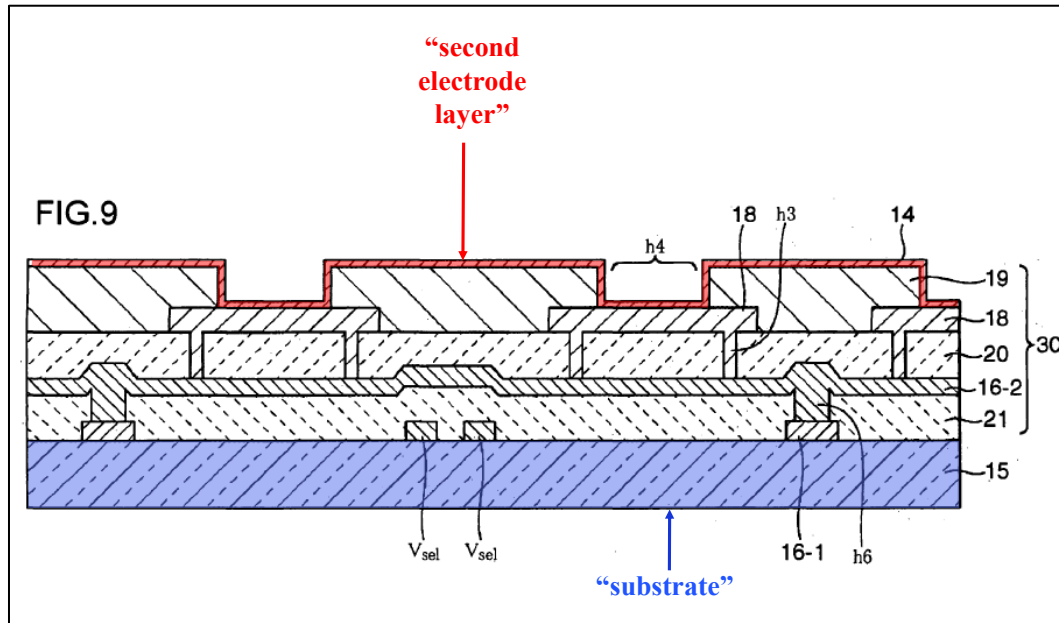
structures disposed on a display area 11.” (EX1004, [0047] (emphasis added).)

Figure 1 (annotated below) show the *display area 11* with *pixels 10*.



49. Matsueda explains that “[r]elated art active-matrix-addressing-type organic EL display panels use such a structure, that is, a pixel electrode, as the anode [(“first electrode layer”)], is disposed for each pixel in a pixel area and a common electrode [(“second electrode layer”)], as the cathode, covers the entire pixel area.” (EX1004, [0004].) Matsueda also discloses “[t]he entire surface of the laminated structure disposed on the display area 11 is covered with a film of a cathode 14 which serves as a common electrode.” (EX1004, [0047].) As Matsueda explains, the EL display panels using a pixel electrode/anode in the pixel area and a common electrode/cathode, which is on the substrate 15, means the display area 11 with pixels 10 have an anode 17 and a cathode 14 on a substrate

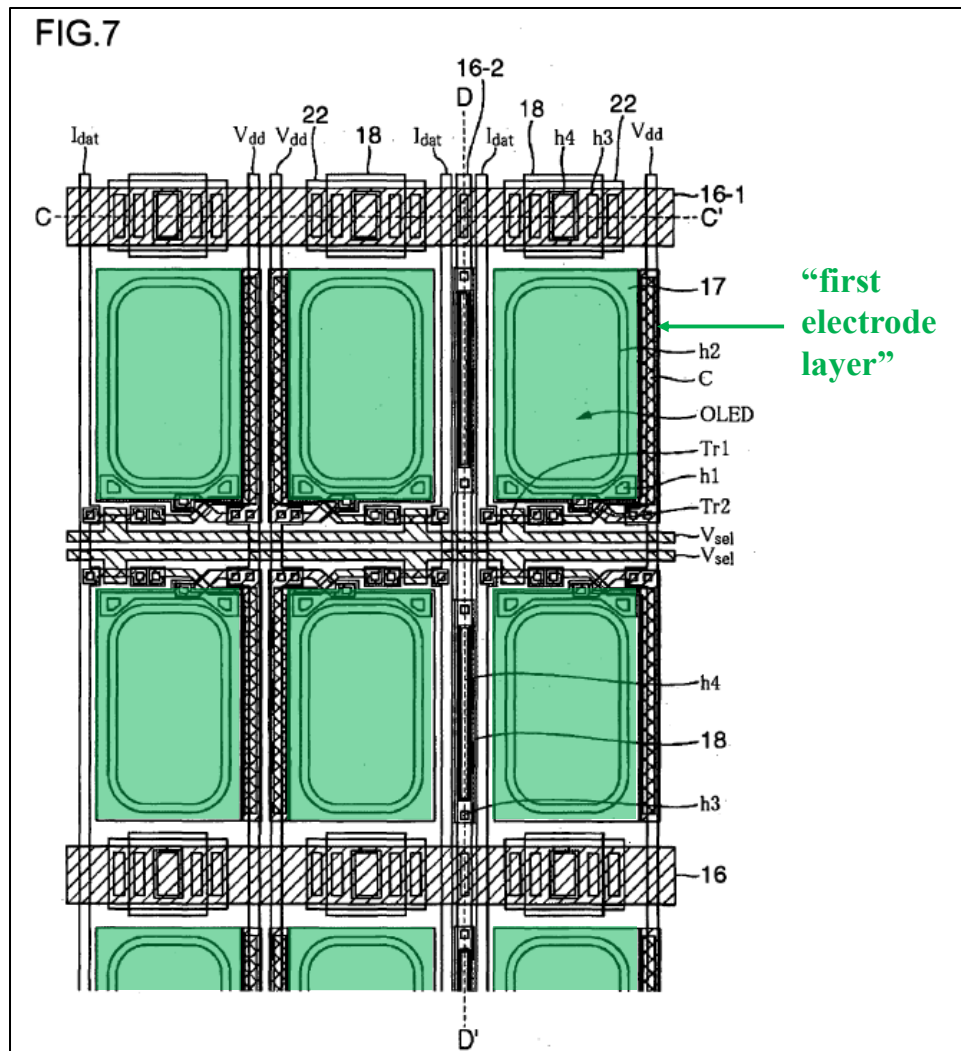
15. Figure 9 (annotated below) shows the **cathode 14** (“second electrode layer”) on the **substrate 15**.



50. Matsueda refers to the cathode 14 as the “second electrode layer” and anode 17 (which may be ITO) as the “first electrode layer.” This is like the ’708 patent. A POSITA would have understood that the cathode 14 being on the substrate 15 and the “a second electrode layer 14 [being] formed on or above the first electrode layers” (EX1004, Abstract) means the **anode 17** (Figure 7 (annotated below)) is on the substrate 15. Notably, Matsueda explains that: “[t]he organic EL display panel 100 has a bottom-emission structure that emits light through the substrate 15. However, the present invention is not limited to this structure. The organic EL display panel 100 may have a so-called top-emission structure that emits light through the cathode 14 if the cathode 14 is a light-

transmitting conductive film. In the organic EL display panel 100 having the top-emission structure, the cathode 14 may be formed of a semitransparent conductive metal layer obtained by processing a thin metal film such as a calcium, lithium, or aluminum film to be thin so as to be able to transmit a light, in addition to a light-transmitting conductive material such as an indium tin oxide (ITO). Such a semitransparent conductive metal layer allows the cathode 14 to have low resistance.” (EX1004, [0048].)

51. Figure 7 (annotated below) shows the *anode / pixel element 17*.



52. Matsueda discloses “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent material is interposed between an anode and a cathode.” (EX1004, [0004].) Thus, Matsueda teaches the EL unit is formed between the anode 17 and the cathode 14.

c. 1[b]: “an electrode power supply line to supply electrode power to the display area;”

53. As shown for element 1[a], Matsueda teaches a display area 11 (“display area”).

54. Matsueda teaches “an electrode power supply line to supply electrode power to the display area.” For example, Matsueda discloses “FIG. 7 [(below)] shows the layout of wiring in an organic EL display panel 100 according to a third exemplary embodiment of the present invention. This exemplary embodiment differs from the first and second exemplary embodiments on the point of that auxiliary cathode wiring 16 are disposed in both the row and the column directions. For the sake of distinguishing between the auxiliary cathode wiring 16 which are disposed in both the row and the column directions, the auxiliary cathode wiring 16 disposed along the row direction are called *first auxiliary cathode wiring 16-1*, while the auxiliary cathode wiring 16 disposed along the column direction are called *second auxiliary cathode wiring 16-2*. When the ‘auxiliary cathode wiring 16’ is simply used, it includes both.” (EX1004, [0064].)

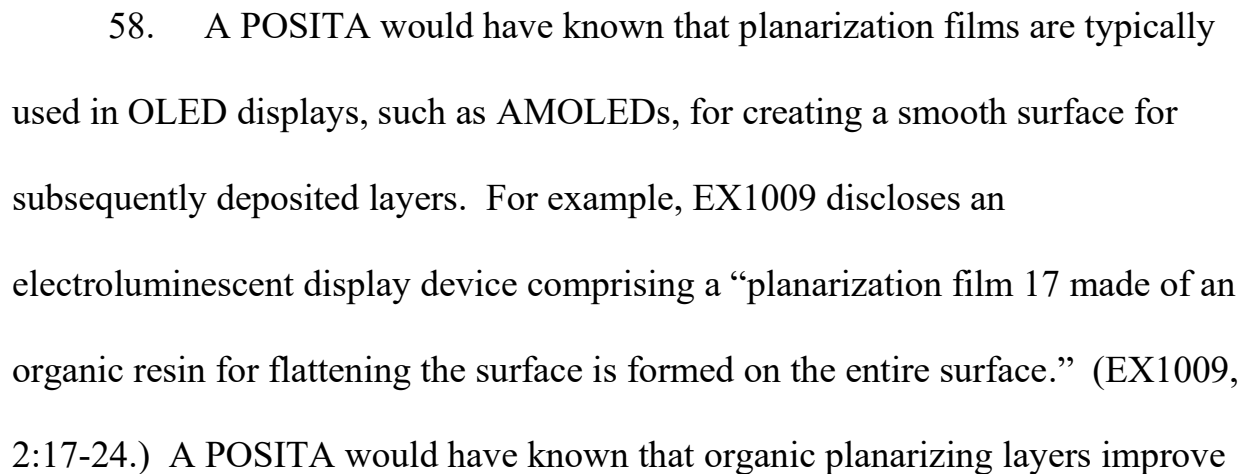


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- d. **1[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”**

56. As shown for element 1[b], Matsueda teaches an auxiliary cathode wiring 16 (“electrode power supply line”).

57. Matsueda teaches “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material.” For example, Matsueda discloses “[r]eferring to FIG. 8, a laminated structure 30 in which the *first auxiliary cathode wiring 16-1*, insulating interlayer film 21, a *planarizing film 20*, source metal layers 22, ITO layers 18, and a bank layer 19 are sequentially laminated, is formed on the display area 11 and on the substrate 15.” (EX1004, [0067] (emphasis added).) Matsueda also discloses “[o]n the *planarizing films 20*, the islanded ITO layers 18 are disposed in a direction in which the first auxiliary cathode wiring 16-1 extend at multiple positions and are connected to the source metal layers 22 through *contact holes h3*.” (EX1004, [0069] (emphasis added).) Figures 8 and 9 (annotated below) show planarizing film 20 disposed on auxiliary cathode wiring 16-2 and 16-1, respectively. These figures also show *planarizing film 20* disposed on *auxiliary cathode wiring 16-1 and 16-2*, including *contact hole h3*.

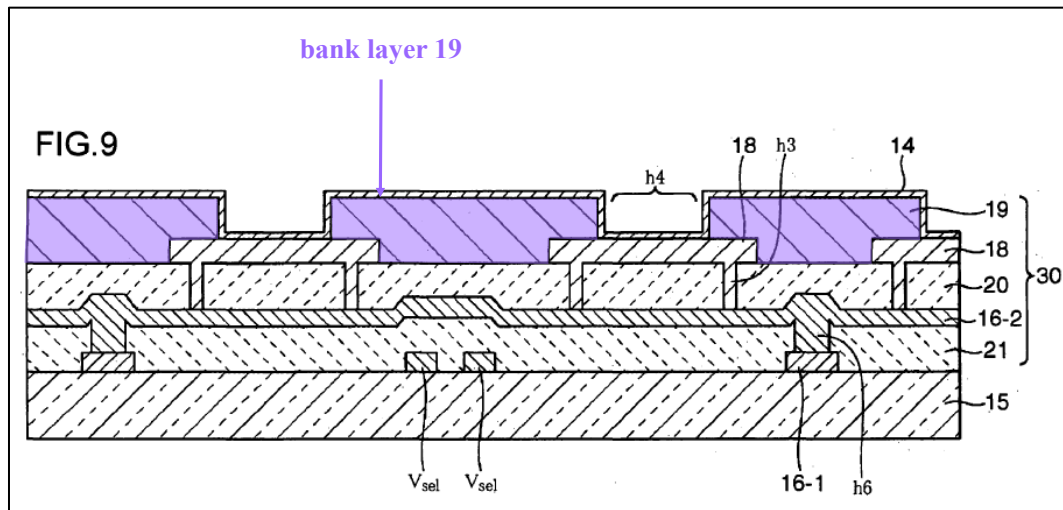
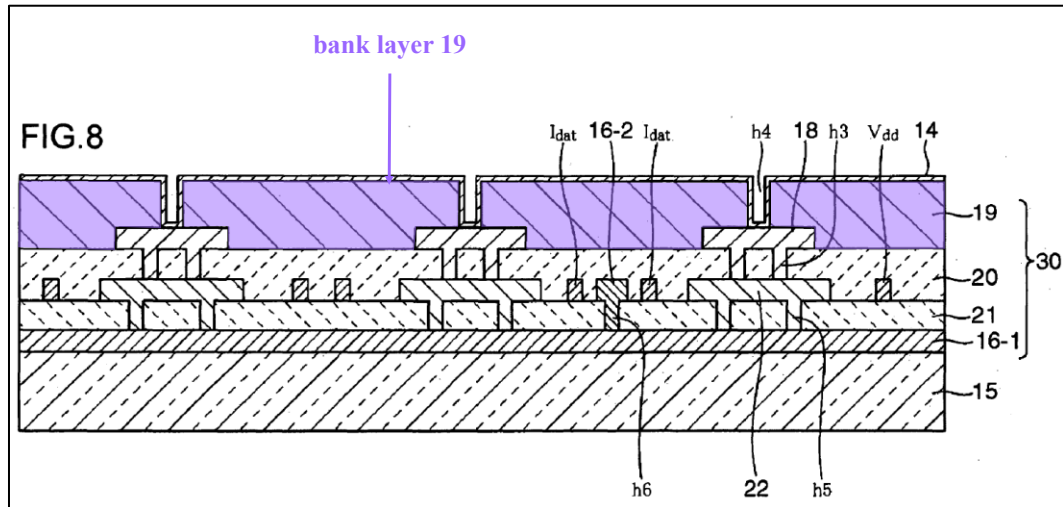


performance and manufacturability of the displays, acting as a mechanical and chemical buffer layer, typically applied after fabrication of the transistors and before deposition of the organic layer. It would have been obvious for the planarizing film 20 to contain an organic material because planarizing films for EL devices at the time of the '708 patent comprised organic materials. This is because the purpose of the planarizing film in organic displays is to provide a smooth and uniform (planar) surface for layers (such as ITO, EL layer) that are subsequently formed, and organic materials are well suited for this purpose. They also prevent electrical shorts, improves optical uniformity, and enables high-resolution pixels. One example material used for a planarization film is an organic polymer (e.g., photosensitive polyimide (PSPI) or acrylic resin).

59. Additionally, Matsueda discloses “[t]he bank layer 19, which is made of a photosensitive organic material or the like is formed on the planarizing films 20.” (EX1004, [0069].) Figures 8 and 9 (annotated below) show *bank layer 19*. A POSITA would have understood that a photosensitive material may be needed to define / etch the vias. Thus, Matsueda teaches an organic material located between the cathode and the auxiliary cathode wiring (“electrode power supply line”). Configuring the planarizing film 20 to contain an organic material is an obvious design choice. As Matsueda explains, “the upper surface of the planarizing film 20 is covered with the bank layer 19, which is made of a photosensitive organic

material or the like. The bank layer 19 is a component to partition the pixels 10.”

(EX1004, [0053].) Thus, Matsueda teaches element 1[c].

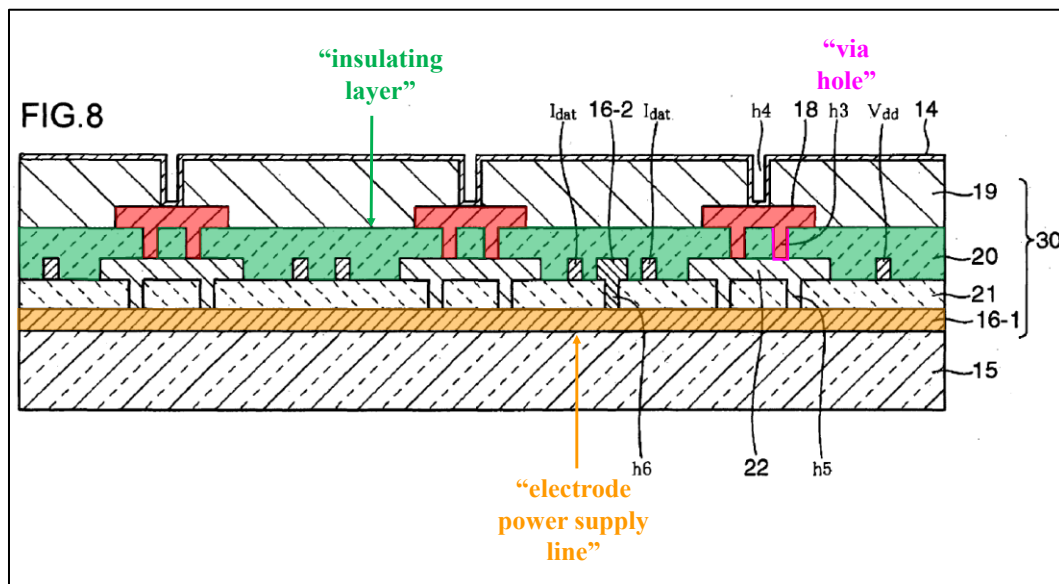


- e. **1[d]: “a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”**

60. As shown for element 1[c], Matsueda teaches a planarizing film 20 (“insulating layer”) including the contact hole h3 (“via hole”). As shown for

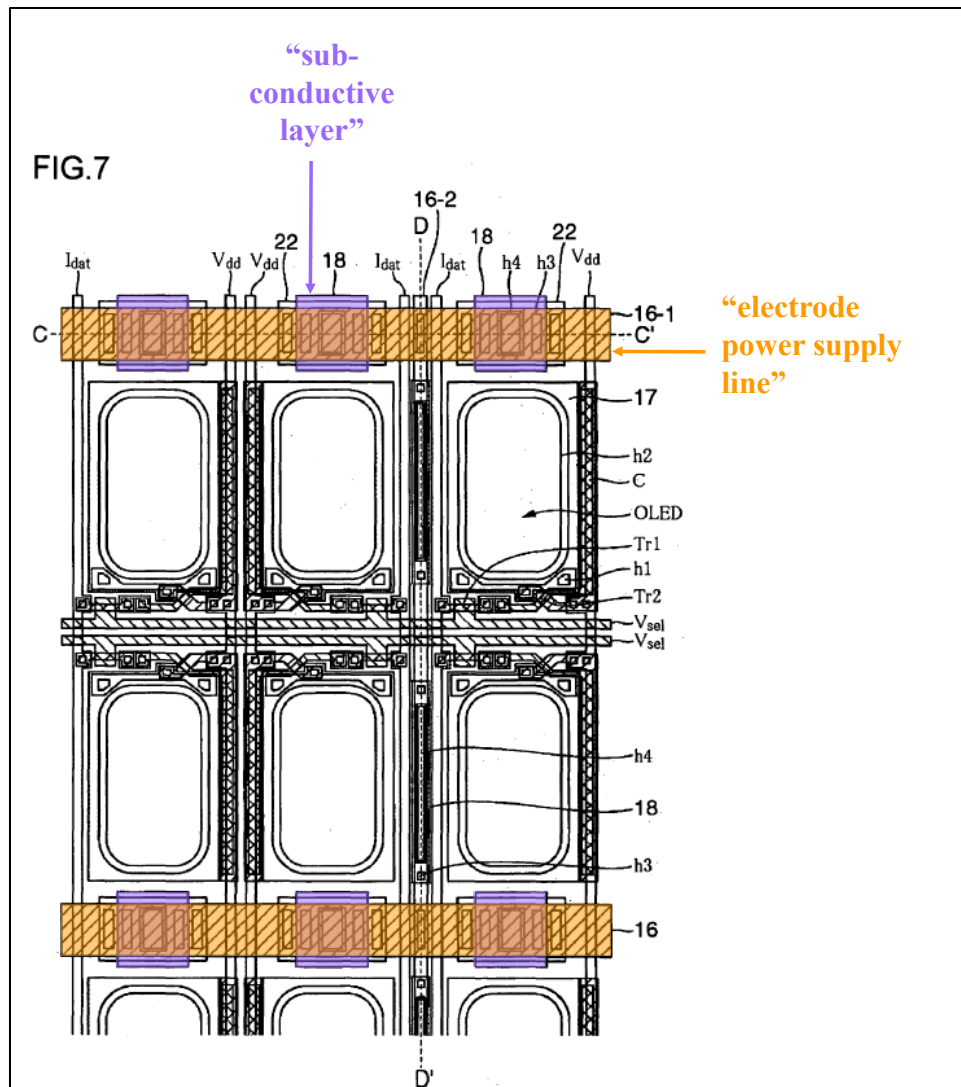
element 1[a], Matsueda teaches an auxiliary cathode wiring 16 (“electrode power supply line”).

61. Matsueda teaches “a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line.” For example, Matsueda discloses “[o]n the planarizing films 20, the islanded ITO layers 18 are disposed in a direction in which the first auxiliary cathode wiring 16-1 extend at multiple positions and are connected to the source metal layers 22 through contact holes h3.” (EX1004, [0069].) Figures 8 and 9 (annotated below) shows *ITO layer 18* formed on *planarizing film 20* including *contact hole h3*.





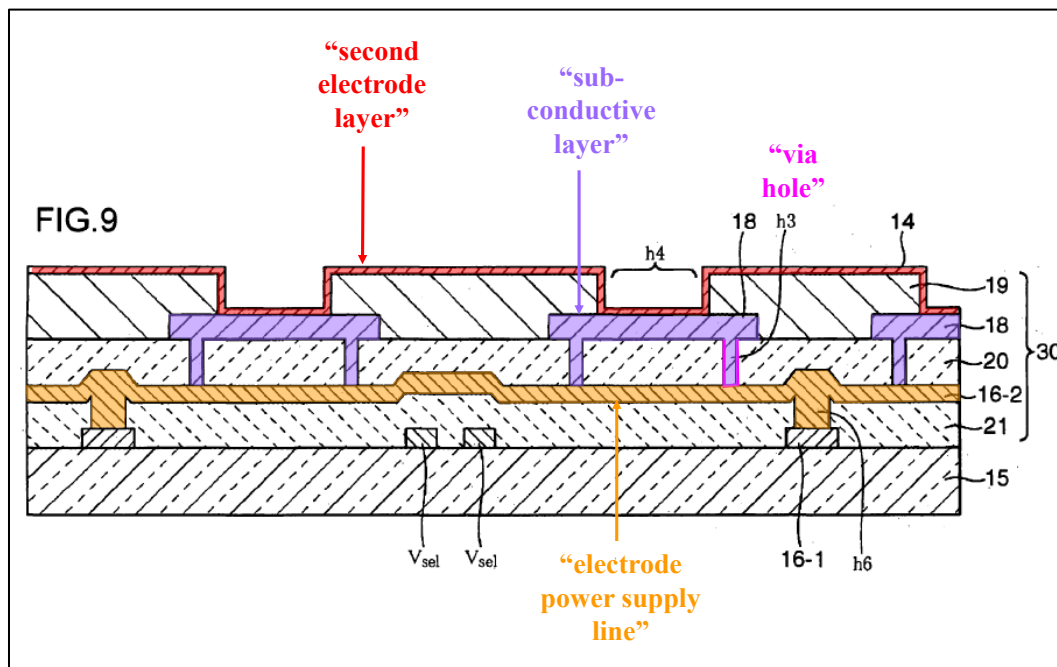
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f. 1[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

63. As shown for element 1[b], Matsueda teaches an auxiliary cathode wiring 16 (“electrode power supply line”). As shown for element 1[a], Matsueda teaches a cathode 14 (“second electrode layer”). As shown for element 1[c], Matsueda teaches a contact hole h3 (“via hole”). As shown for element 1[d], Matsueda teaches an ITO layer 18 (“sub-conductive layer”).

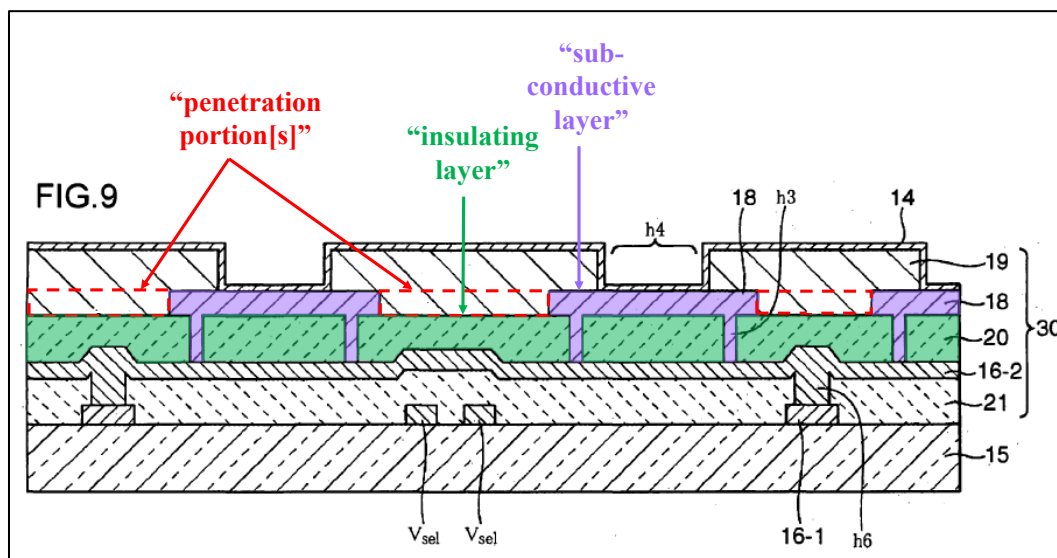
64. Matsueda teaches “the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer.” For example, Matsueda discloses “[t]he cathode 14 formed on the bank layers 19 is connected to the auxiliary cathode wiring 16 in the laminated structure 30 so that the electrical resistance decreases and thus sufficient current is supplied to each of the pixels 10.” (EX1004, [0069] (emphasis added).) Matsueda also discloses “[t]he ITO layers 18 are connected to the second auxiliary cathode wiring 16-2 through the contact holes h3 formed in the planarizing films 20.” (Ex1004, [0070].) Figure 9 shows auxiliary cathode wiring 16 and cathode 14 coupled to each other at the contact hole h3 through the ITO layer 18.

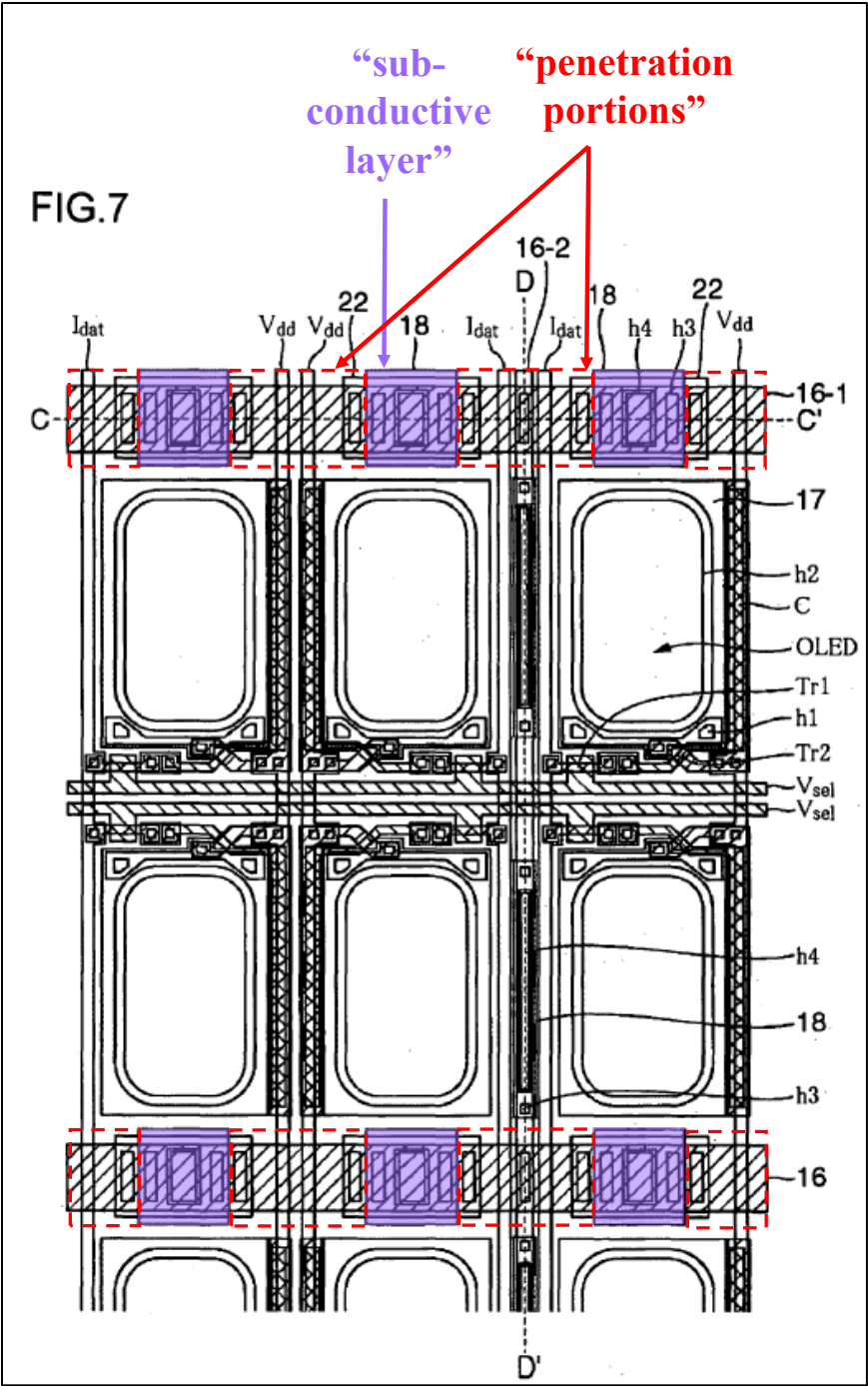


g. 1[f]: “the sub-conductive layer on the insulating layer includes a penetration portion.”

65. As shown for element 1[d], Matsueda teaches an ITO layer 18 (“sub-conductive layer”) on the planarizing film 20 (“insulating layer”).

66. Matsueda teaches “the sub-conductive layer on the insulating layer includes a penetration portion.” For example, Matsueda discloses “[o]n the planarizing films 20, the *islanded ITO layers 18* are disposed in a direction in which the first auxiliary cathode wiring 16-1 extend at multiple positions and are connected to the source metal layers 22 through contact holes h3.” (EX1004, [0069] (emphasis added).) A POSITA would have understood the ITO layers 18 being “islanded” means they are separated from each other, by a penetration portion. Figure 9 (annotated below) shows the ITO layer 18 on the *planarizing film 20*, and Figures 7 and 9 (annotated below) show the *ITO layer 18* including a *penetration portion*.

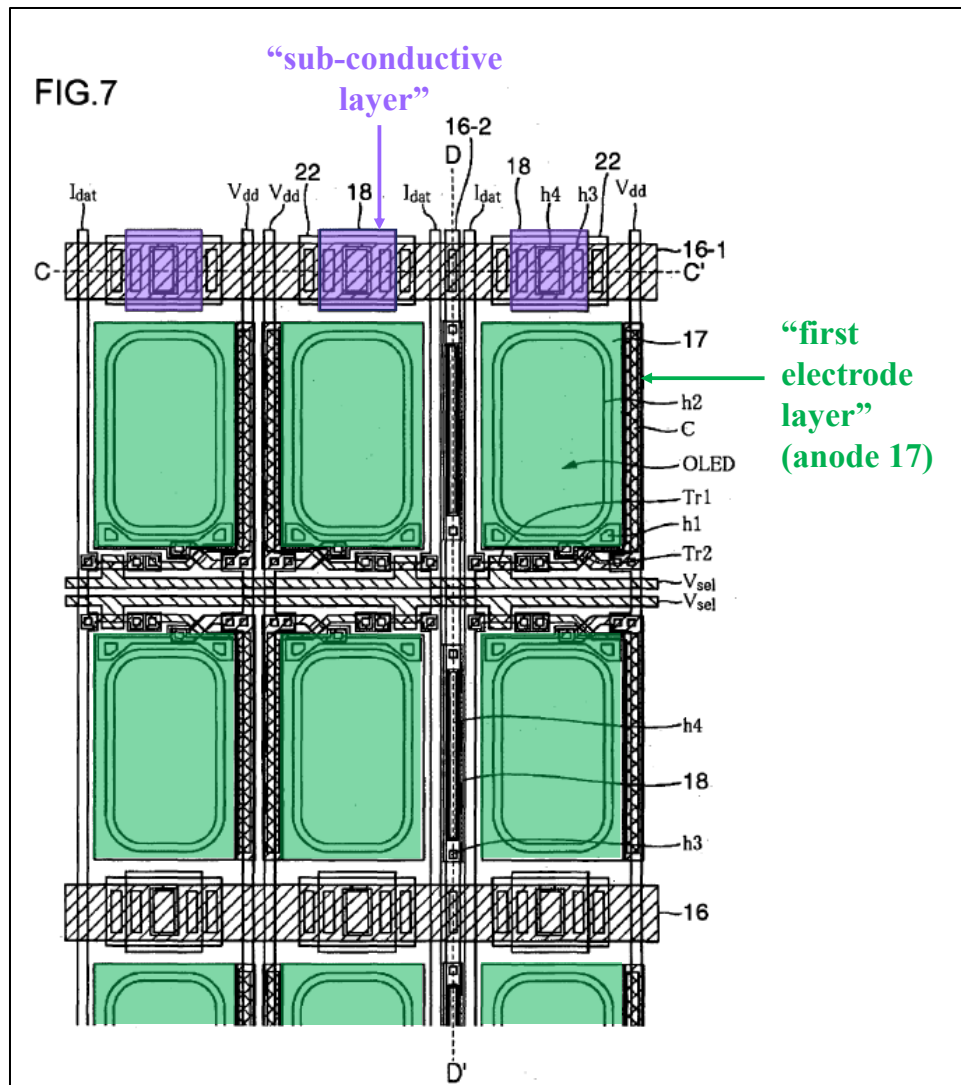




3. Claim 2: “The device of claim 1, wherein the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.”

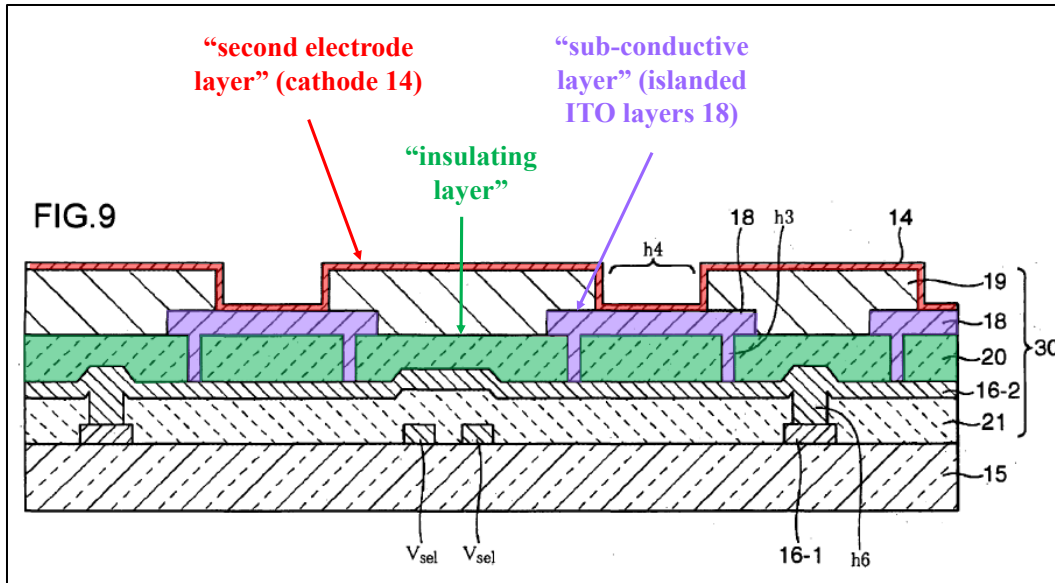
67. As shown for element 1[d], Matsueda teaches an ITO layer 18 (“sub-conductive layer”). As shown for element 1[a], Matsueda teaches an anode / pixel element 17 (“first electrode layer”).

68. Matsueda teaches “the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.” For example, Figure 7 (annotated below) shows the *islanded ITO layers 18* located in areas different from the *anode / pixel electrode 17*.



69. Figure 9 (annotated below) shows a cross-sectional view of the wiring area, with the **cathode 14** deposited on the **ITO layers 18**, which is deposited on the **planarizing film 20**. Matsueda discloses that “[t]he organic EL display panel 100 has a bottom-emission structure that emits light through the substrate 15.” (EX1004, [0048].) Matsueda explains that “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent material is interposed between an anode and a cathode.” (EX1004, [0004].) Thus, it is

obvious that in the display area, where the pixels are located, the anode / pixel element 17 would be deposited on the planarizing film 20, which would mean the ITO layers 18 (“sub-conductive layer”) are deposited on the same layer as the anode / pixel element 17 (“first electrode layer”). For example, Matsueda discloses in another one of its patents (EX1010) that “[t]he ITO layer 59 is patterned so as to form a pixel electrode layer (an anode) 59.” (EX1010, 5:21-23, Figs. 2, 3.) As another example, EX1008 discloses “anode (pixel electrode) 23” at 5:57, and describes a pixel electrode made of ITO at 7:10. The ITO layers 18 and anode / pixel element 17 are disposed on the planarizing film 20. Figure 4 shows the ITO layer 18 is also disposed on the source metal layer 22, which is a source electrode layer of the transistor. (EX1004, [0052].) The anode / pixel element 17 is on or above the transistor. (*See, e.g.*, EX1010, Fig. 3 (showing anode 59 on the wiring (source metal layer) 57).) As a result, the ITO layer 18 and anode / pixel element 17 both being disposed on the source metal layer 22 means the ITO layer 18 and anode / pixel element 17 are deposited on the same layer.

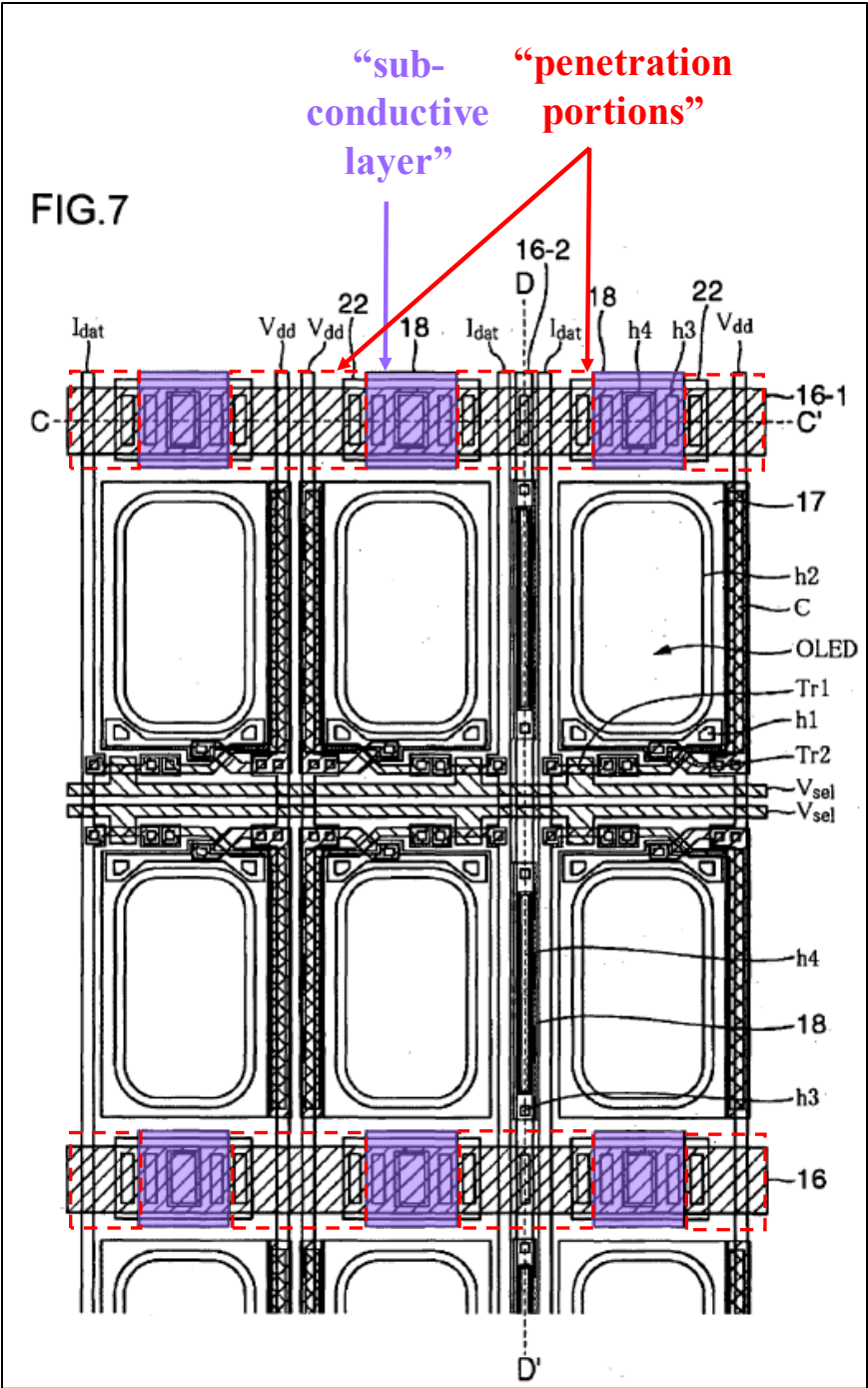


4. Claim 3

- a. 3[a]: “The device of claim 1, wherein the sub-conductive layer comprises two penetration portions, and”

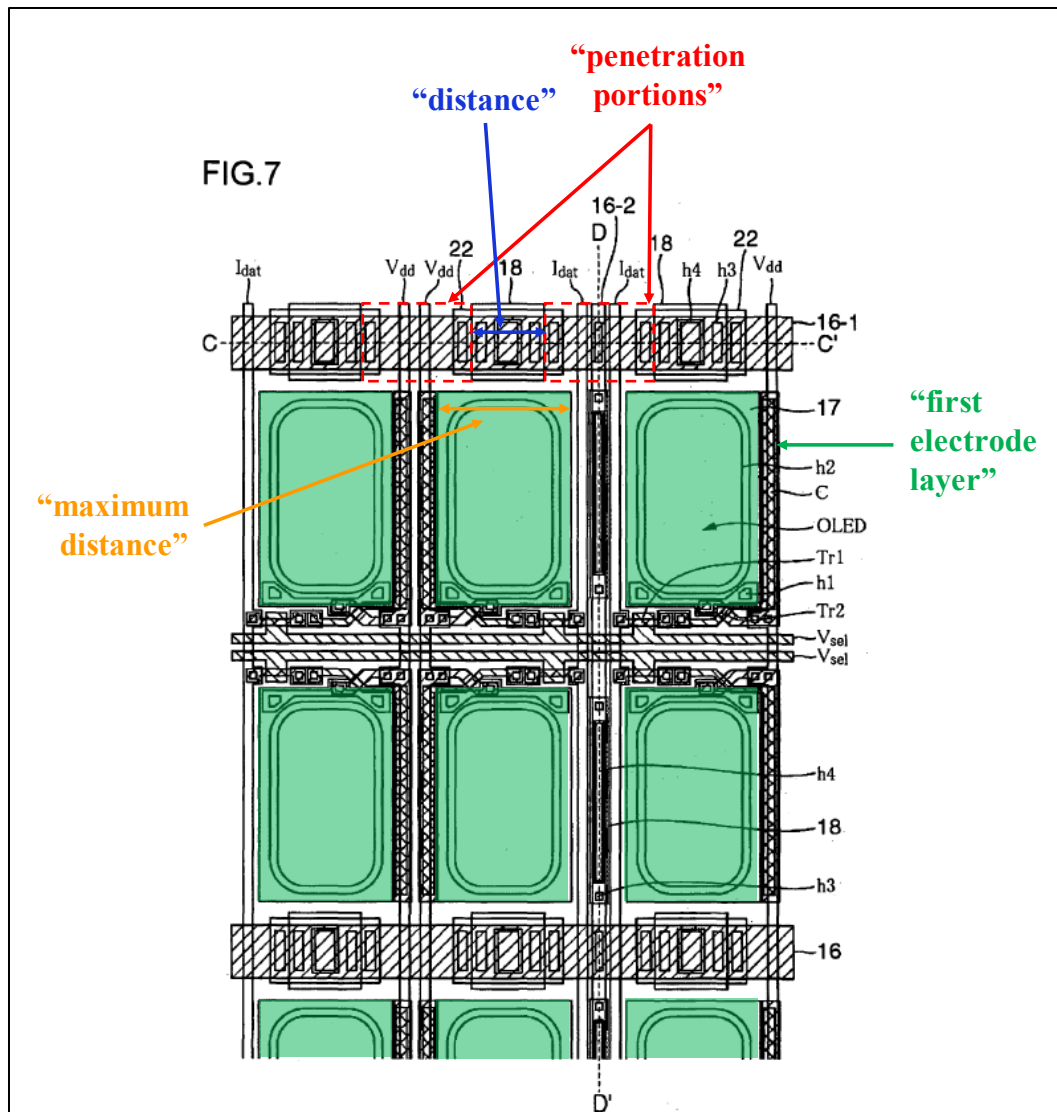
70. As shown for element 3[a], Matsueda teaches ITO layer 18 (“sub-conductive layer”).

71. Matsueda teaches “the sub-conductive layer comprises two penetration portions.” For example, Figures 7 and 9 (annotated below) show that ITO layer 18 comprises two penetration portions.



72. As shown element 1[a], Matsueda discloses a layer of pixel elements 17 (“first electrode layer”).

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74. A POSITA would have understood that the relative sizes of the objects and spacings between the objects in the figures in Matsueda are representative. For example, Figures 3 and 4 show the ITO layer 18 is smaller than the pixel electrode 17. The source metal layer 22 is on the same layer as and disposed between the data line I_{dat} and V_{dd} line. The source metal layer 22 cannot be connected to the data line I_{dat} and V_{dd} line, otherwise they would short and the device would not work. The pixel electrode 17 is disposed between the data line

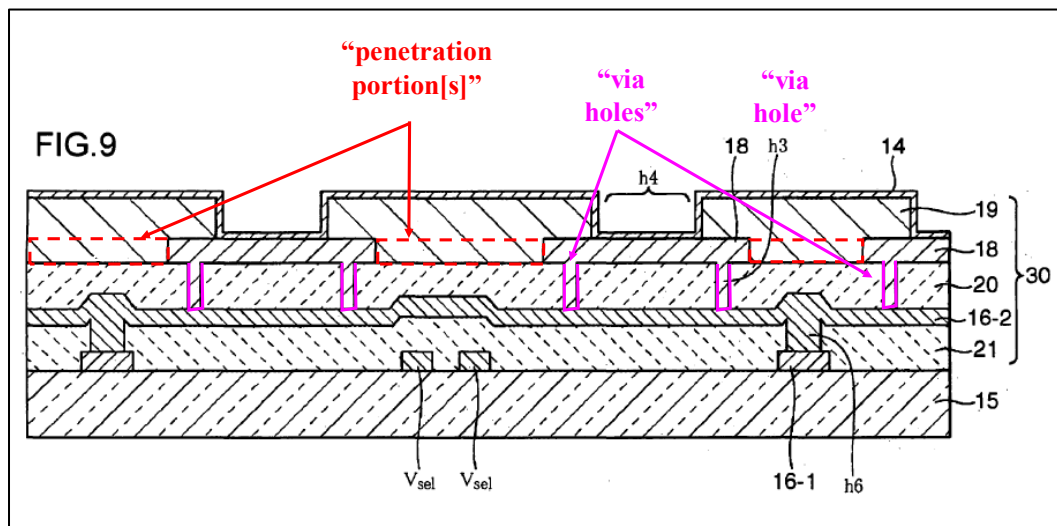
I_{dat} and V_{dd} line. The width of the ITO layer 18 (equal to the “distance”) is less than the width of the pixel element 17 (equal to the “maximum distance”).

(EX1004, [0035], [0051], [0053], [0055], [0059], [0064], [0065].)

5. Claim 4: “The device of claim 3, wherein at least one of the two penetration portions is disposed on at least a part of an outer portion of the via hole.”

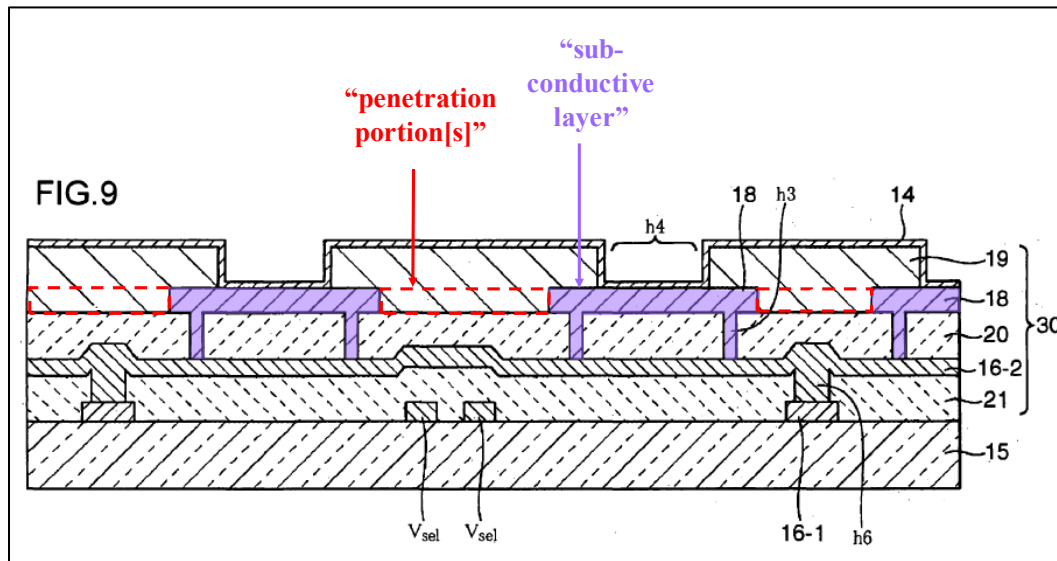
75. As shown for element 1[c], Matsueda teaches a contact hole h3 (“via hole”).

76. Matsueda teaches “at least one of the two penetration portions is disposed on at least a part of an outer portion of the via hole.” For example, Figure 9 (annotated below) shows at least one of the two penetration portions is disposed on at least a part of an outer portion of the *contact hole h3*.



6. Claim 5: “The device of claim 1, wherein the penetration portion comprises a penetration hole.”

77. Matsueda teaches “the penetration portion comprises a penetration hole.” For example, Figure 9 (annotated below) shows the *penetration portion* goes through the *sub-conductive layer*, thereby comprising a penetration hole.



7. Claim 7

a. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

78. As shown for element 1[a], Matsueda discloses an anode / pixel electrode 17 (“first electrode layer”).

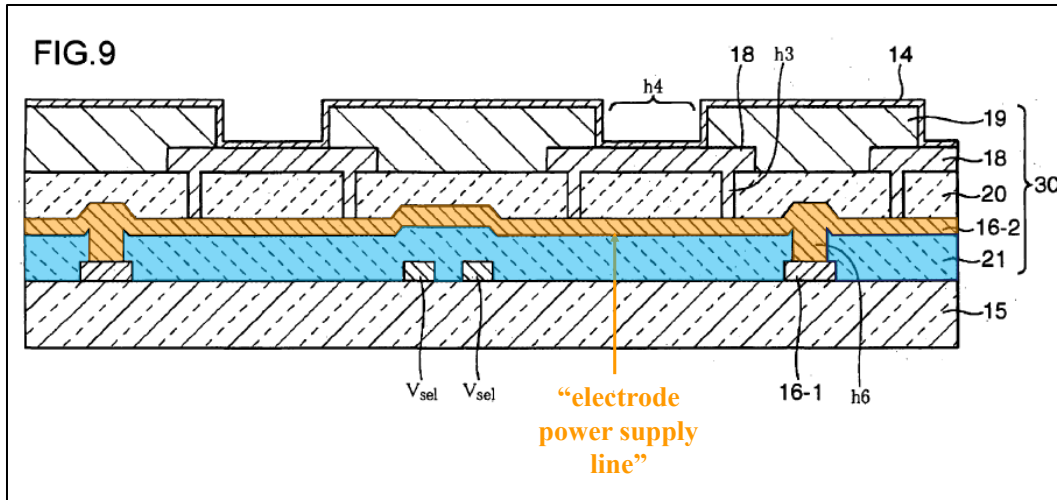
79. Matsueda discloses “which the auxiliary cathode wiring 16, an insulating interlayer film 21, *source metal layers 22*, a planarizing film 20, *ITO layers 18*, and a bank layer 19 are sequentially laminated is formed in the display area 11 on the substrate 15.” (EX1004, [0052] (emphasis added); *also* [0067].)

Figures 4 and 8 of Matsueda shows that its ITO layer 18 disposed is on the source metal layer 22. A source metal refers to the source electrode of a thin film transistor, and thus, the source metal layer 22 is a source electrode layer of a thin film transistor layer. Matsueda teaches the anode / pixel electrode 17 is on or above the transistor. (See claim 2.) Thus, Matsueda's thin film transistor layer is disposed under the anode / pixel electrode 17.

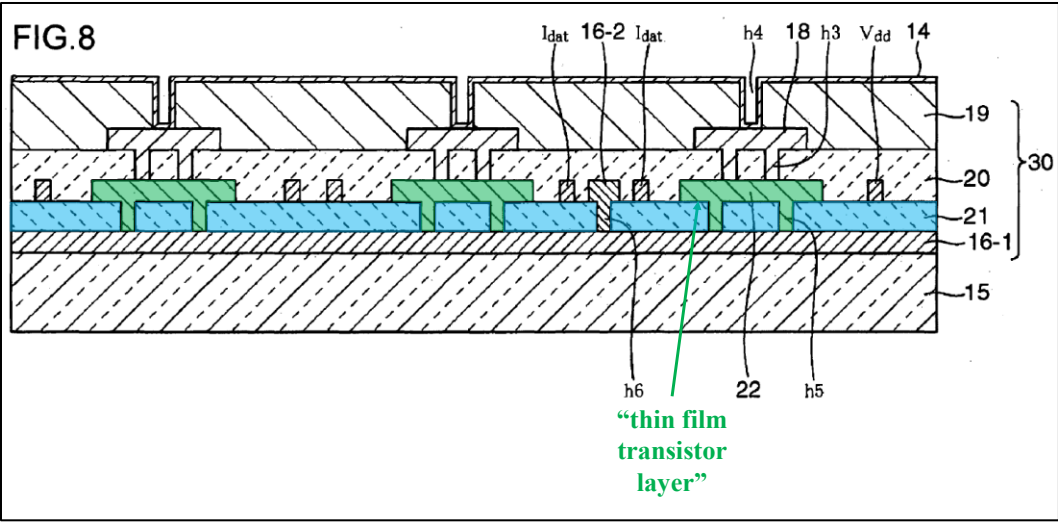
b. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”

80. As shown for element 1[b], Matsueda teaches an auxiliary cathode wiring 16-2 (part of “electrode power supply line”).

81. Matsueda discloses “[r]eferring to FIG. 9, the laminated structure 30 in which the *first auxiliary cathode wiring 16-1*, the scanning lines V_{sel} , the *insulating interlayer film 21*, the second auxiliary cathode wiring 16-2, the planarizing film 20, the ITO layers 18, and the bank layers 19 are sequentially laminated, is formed on the substrate 15.” (EX1004, [0070] (emphasis added).) Figure 9 (below) of Matsueda shows that *auxiliary cathode wiring 16-2* is located on the *insulating interlayer film 21*.



82. Matsueda discloses “[r]eferring to FIG. 8, a laminated structure 30 in which the first auxiliary cathode wiring 16-1, *insulating interlayer film 21*, a planarizing film 20, *source metal layers 22*, ITO layers 18, and a bank layer 19 are sequentially laminated, is formed on the display area 11 and on the substrate 15.” (EX1004, [0067] (emphasis added).) Figure 8 (below) shows that the source metal layers 22 (source electrode of the “thin film transistor layer” (see 7[a])) is located on the *insulating interlayer film 21*. As a result, the electrode power supply line comprises a layer (auxiliary cathode wiring 16-2) that is the same layer as the source metal layers.



8. Claim 9

a. Preamble: “An electroluminescence display device, comprising:”

83. The preamble of claim 9 is similar to the preamble of claim 1, which Matsueda teaches. The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 9
“An electroluminescence display device, comprising:”	“An electroluminescence display device, comprising:”

b. 9[a]: “a display area with pixels that have a first electrode layer and a second electrode layer and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

84. Element 9[a] is similar to element 1[a], which Matsueda teaches. The table below shows the similarities.

Element 1[a]	Element 9[a]
“a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an	“a display area with pixels that have a first electrode layer and a second electrode layer and an

electroluminescence unit formed between the first electrode layer and the second electrode layer;”	electroluminescence unit formed between the first electrode layer and the second electrode layer;”
--	--

c. 9[b]: “an electrode power supply line to supply electrode power to the display area;”

85. Element 9[b] is similar to element 1[b], which Matsueda teaches. The table below shows the similarities.

Element 1[b]	Element 9[b]
“an electrode power supply line to supply electrode power to the display area;”	“an electrode power supply line to supply electrode power to the display area;”

d. 9[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”

86. Element 9[c] is similar to element 1[c], which Matsueda teaches. The table below shows the similarities.

Element 1[c]	Element 9[c]
“an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”	“an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material;”

e. 9[d]: “a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”

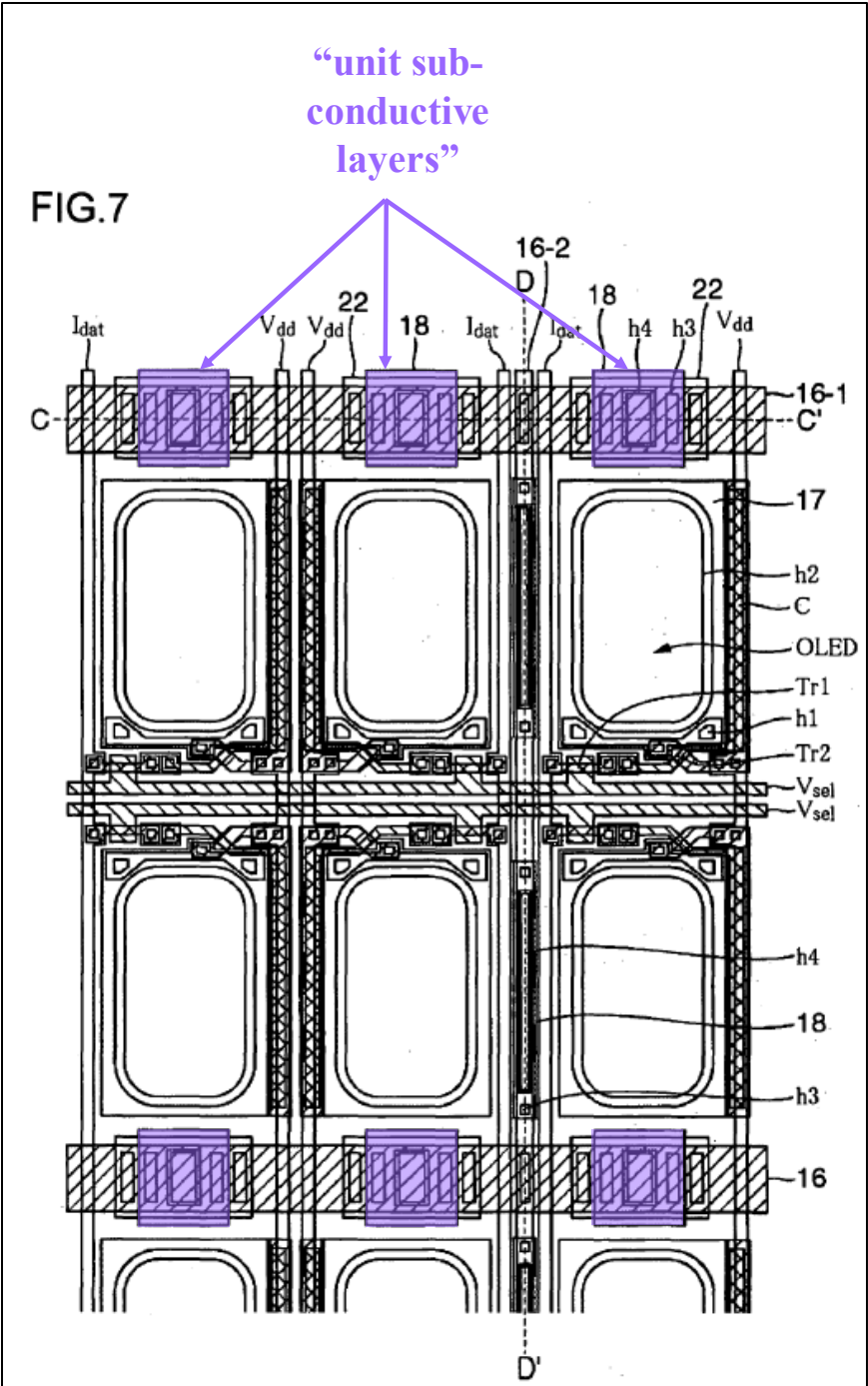
87. Element 9[d] is similar to element 1[d], except element 9[d] additionally requires the sub-conductive layer “comprising a plurality of unit sub-

conductive layers.” Matsueda teaches element 1[d]. The table below shows the similarities.

Element 1[d]	Element 9[d]
“a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”	“a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”

88. As shown for element 1[d], Matsueda teaches ITO layer 18 (“sub-conductive layer”).

89. Matsueda teaches “a sub-conductive layer comprising a plurality of unit sub-conductive layers.” For example, Matsueda discloses “[o]n the planarizing films 20, *the islanded ITO layers 18* are disposed in a direction in which the first auxiliary cathode wiring 16-1 extend at multiple positions and are connected to the source metal layers 22 through contact holes h3.” (EX1004, [0069] (emphasis added).) A POSITA would have understood the ITO layers being islanded means there are a plurality of unit sub-conductive layers. Figure 7 (annotated below) shows the *islanded ITO layers 18*.



- f. **9[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”**

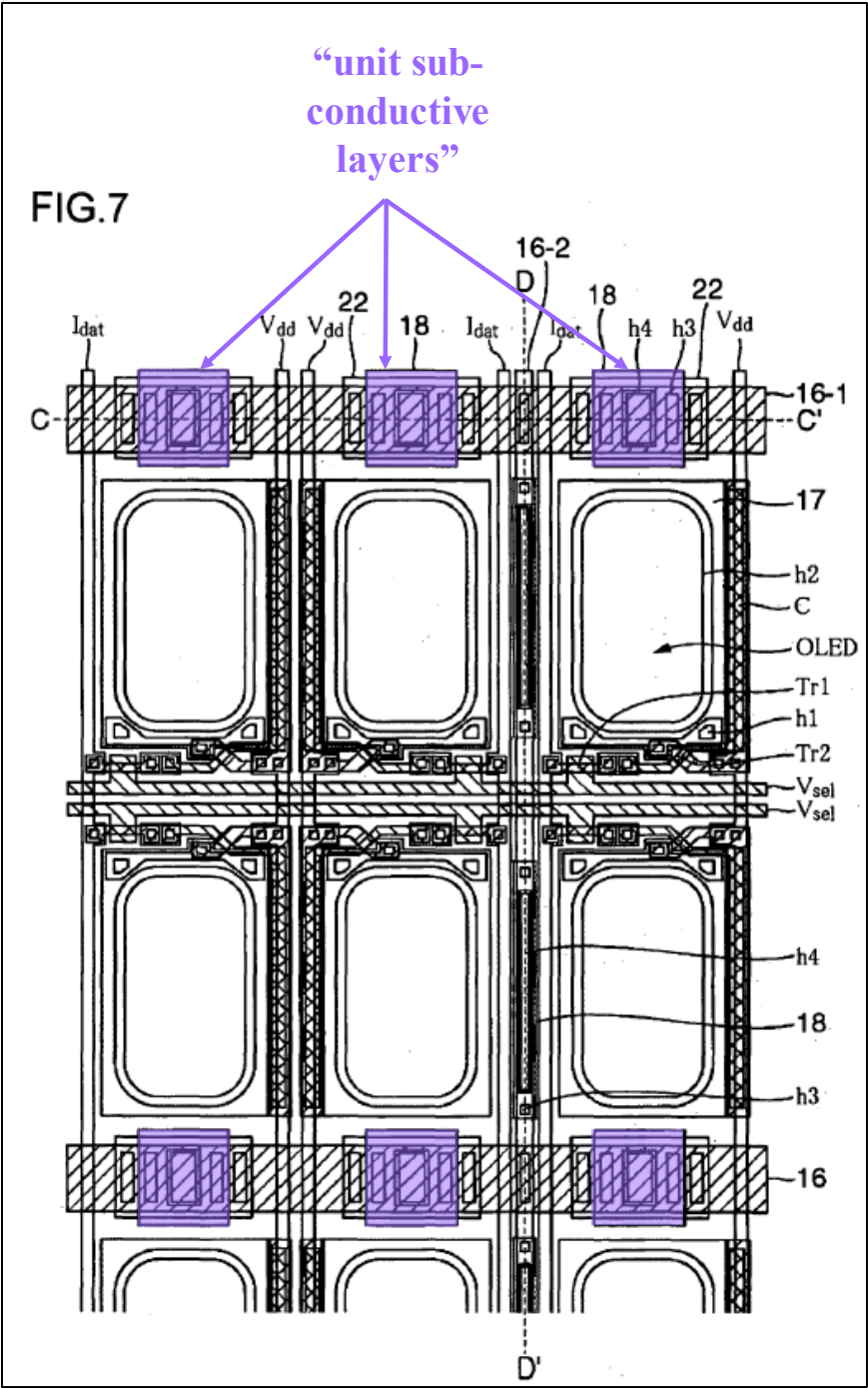
90. Element 9[e] is similar to element 1[e], which Matsueda teaches. The table below shows the similarities.

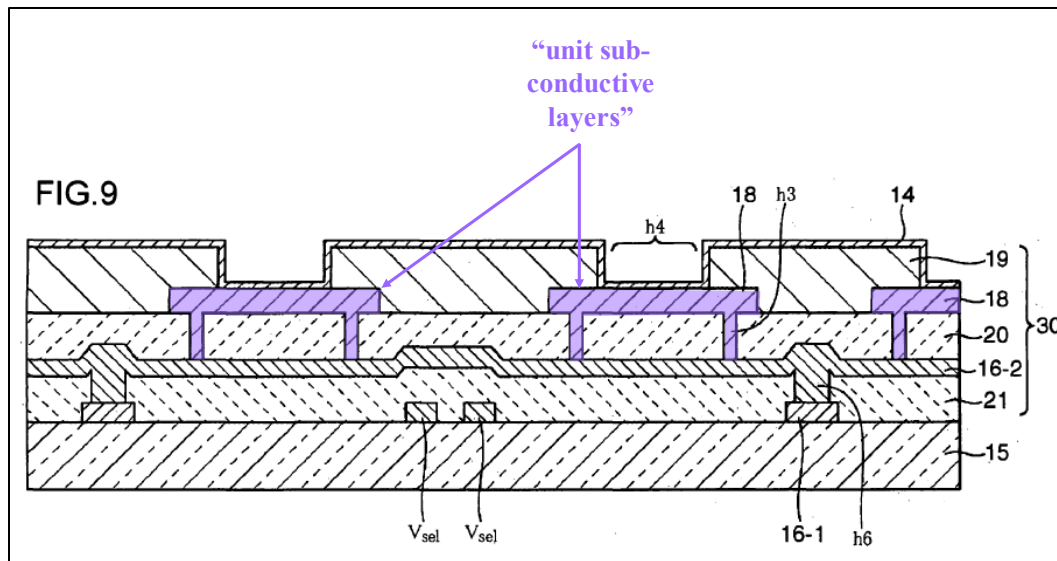
Element 1[e]	Element 9[e]
“wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer,”	“wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

- g. **9[f]: “the unit sub-conductive layers on the insulating layer are separated from each other.”**

91. As shown for element 9[f], Matsueda teaches islanded ITO layers 18 (“unit sub-conductive layers”). As shown for element 1[d], Matsueda teaches the ITO layer 18 on the planarizing film 20 (“insulating layer”).

92. Matsueda teaches “the unit sub-conductive layers on the insulating layer are separated from each other.” For example, Figures 7 and 9 (annotated below) show the *islanded ITO layers 18* are separated from each other.

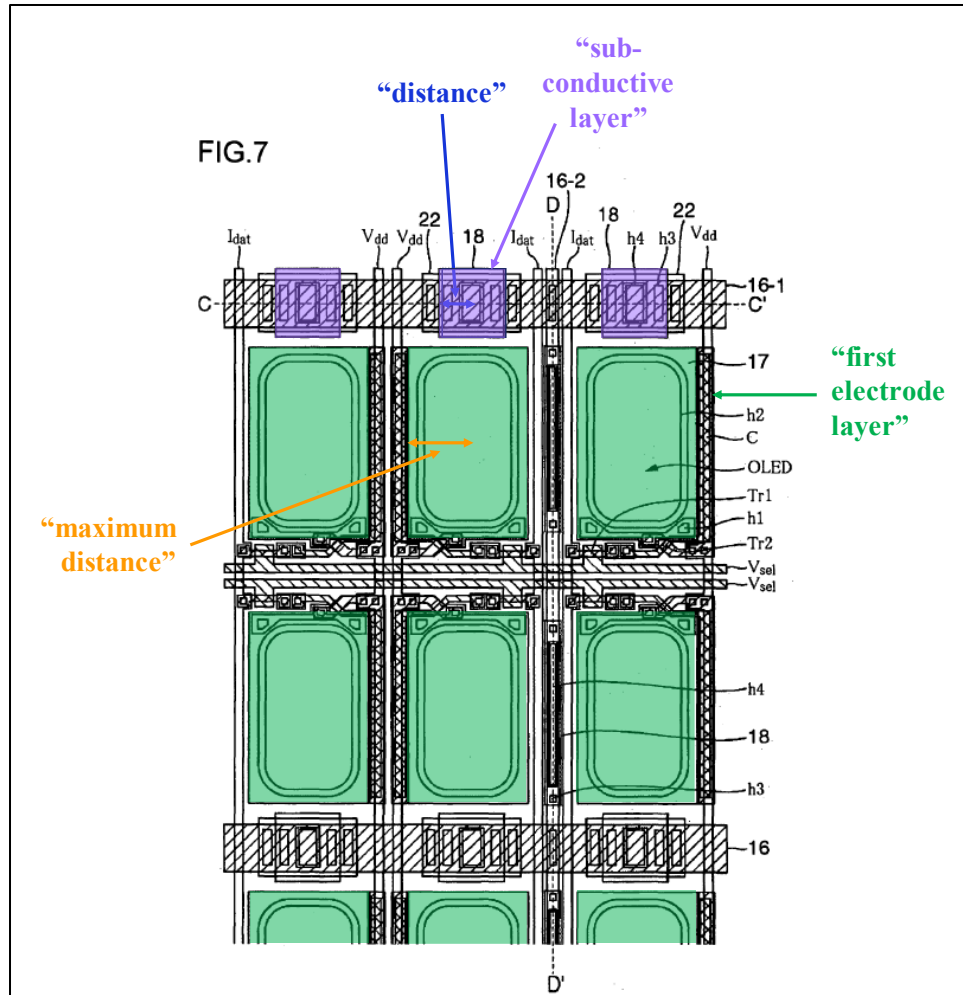




9. **Claim 10: “The device of claim 9, wherein a distance between a point of the unit sub-conductive layer and a neighboring outer point is less than or equal to a maximum distance between a point of the first electrode layer and a neighboring outer point.”**

93. As shown for element 9[f], Matsueda teaches islanded ITO layers 18 (“unit sub-conductive layers”). As shown element 1[a], Matsueda discloses a layer of pixel elements 17 (“first electrode layer”).

94. Matsueda teaches “a distance between a point of the unit sub-conductive layer and a neighboring outer point is less than or equal to a maximum distance between a point of the first electrode layer and a neighboring outer point.” For example, Figure 7 (annotated below) shows a *distance* between a point of the *ITO layers 18* and a neighboring outer point is less than or equal to a *maximum distance* between a point of *pixel element 17* and a neighboring outer point.



95. A POSITA would have understood that the relative sizes of the objects and spacings between the objects in the figures in Matsueda are representative. For example, Figures 3 and 4 show the ITO layer 18 is smaller than the pixel electrode 17. The source metal layer 22 is on the same layer as and disposed between the data line I_{dat} and Vdd line. The source metal layer 22 cannot be connected to the data line I_{dat} and Vdd line, otherwise they would short and the device would not work. The pixel electrode 17 is disposed between the data line I_{dat} and Vdd line. The width of the ITO layer 18 (equal to the “distance”) is less

than the width of the pixel element 17 (equal to the “maximum distance”).

(EX1004, [0035], [0051], [0053], [0055], [0059], [0064], [0065].)

10. Claim 11

a. Preamble: “A method of manufacturing an electroluminescence display device, comprising:”

96. As shown for the preamble of claim 1, Matsueda teaches an organic EL display panel 100 (“electroluminescence display display”).

97. Matsueda teaches “[a] method of manufacturing an electroluminescence display device.” For example, Matsueda describes the manufacturing process including steps for forming several layers of the organic EL display panel 100:

- “The first power lines and the second power lines may be formed in the same layer for the sake of convenience in the manufacturing process or may be formed in different layers.” (EX1004, [0009].)
- “The second power lines and the second electrode layer are formed in different layers of the laminated structure so that manufacturing processes thereof are separated.” (EX1004, [0017].)
- “In the matrix substrate according to the present invention, preferably, the first power lines and the second power lines are disposed in the same layer at least partially, thus simplifying the manufacturing

process.” (EX1004, [0024].)

- “The second power lines and the second electrode layer are formed in different layers of the laminated structure so that manufacturing processes thereof are separated.” (EX1004, [0033].)

98. It would have been obvious that Matsueda’s manufacturing process to form the EL display panel 100 includes forming all of the layers of the EL display panel 100. Thus, Matsueda teaches the preamble of claim 11.

b. 11[a]: “forming an insulating layer including an organic material on an electrode power supply line;”

99. As shown for element 1[b], Matsueda teaches auxiliary cathode wiring 16 (“electrode power supply line”). As shown for element 1[c], Matsueda teaches a planarizing film 20 (“insulating layer”) including an organic material on the auxiliary cathode wiring. Thus, Matsueda teaches “an insulating layer including an organic material on an electrode power supply line.”

100. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process includes all steps for forming the organic EL display panel 100 including forming the planarizing film 20 on the auxiliary cathode wiring 16. Thus, Matsueda teaches element 11[a].

c. 11[b]: “forming a via hole on the insulating layer;”

101. As shown for element 1[c], Matsueda teaches a planarizing film 20 (“insulating layer”) including a contact hole h3 (“via hole”). Thus, Matsueda teaches “a via hole on the insulating layer.”

102. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process includes all steps for forming the organic EL display panel 100 including forming the contact hole h3 on the planarizing film 20. Thus, Matsueda teaches element 11[b].

d. 11[c]: “forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”

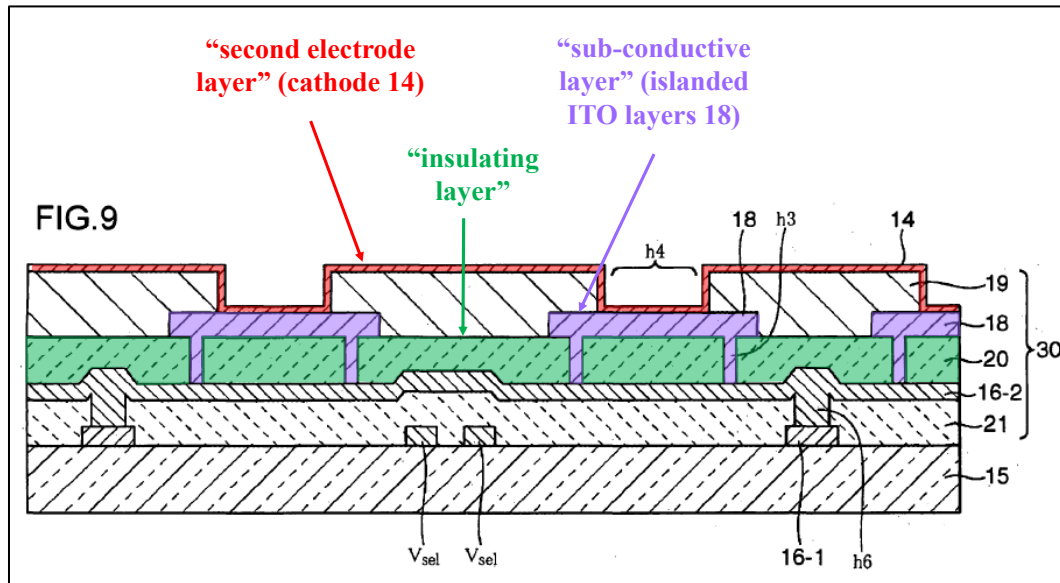
103. As shown for element 1[d], Matsueda teaches ITO layer 18 (“sub-conductive layer”). As shown for element 1[a], Matsueda teaches a pixel element 17 (“first electrode layer”). As shown for element 1[c], Matsueda teaches a planarizing film 20 (“insulating layer”) including a contact hole h3 (“via hole”). Thus, Matsueda teaches “a sub-conductive layer . . . on the insulating layer including the via hole.”

104. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL

display panel 100. It would have been obvious that the manufacturing process includes all steps for forming the organic EL display panel 100 including forming ITO layer 18 on planarizing film 20 including the contact hole h3. Matsueda also teaches “a first electrode layer on the insulating layer.” For example, Figure 9 (annotated below) shows the *cathode 14* disposed on the *islanded ITO layers 18*, which is disposed on the *planarizing film 20*. Matsueda’s “organic EL display panel 100 has a bottom-emission structure that emits light through the substrate 15.” (EX1004, [0048].) It also discloses “[t]he organic EL display panel 100 may have a so-called top-emission structure that emits light through the cathode 14 if the cathode 14 is a light-transmitting conductive film.” (EX1004, [0048].) Matsueda explains that “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent material is interposed between an anode and a cathode.” (EX1004, [0004]; *see also* [0054].)

105. Matsueda discloses “a second electrode layer 14 formed on or above the first electrode layers.” (EX1004, Abstract.) A POSITA would have understood Matsueda’s “first electrode layer” refers to the anode / pixel element 17 because they are “formed on or above a viewing area 11.” (EX1004, Abstract.) Further, the EL device includes first and second electrode layers. Because the “second electrode layer functions as a cathode,” the first electrode layer would function as an anode. (EX1004, Claim 3.) The anode (first electrode layer) is on

the cathode, and the cathode is on the planarizing film 20. This means that in the display area (not shown in Figure 9), where the pixels are located, the anode / pixel element 17 is on the planarizing film 20 (“insulating layer”). Thus, Matsueda teaches element 11[c].



e. 11[d]: “forming a penetration portion on the sub-conductive layer;”

106. As shown for element 1[f], Matsueda teaches the ITO layer 18 (“sub-conductive layer”) including a penetration portion. Thus, Matsueda teaches “a penetration portion on the sub-conductive layer.”

107. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process

includes all steps for forming the organic EL display panel 100 including forming a penetration portion on ITO layer 18. Thus, Matsueda teaches element 11[d].

f. 11[e]: “forming an organic EL unit on the first electrode layer; and”

108. As shown for element 1[a], Matsueda teaches an organic EL unit on the anode / pixel element 17 (“first electrode layer”). Thus, Matsueda teaches “an organic EL unit on the first electrode layer.”

109. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process includes all steps for forming the organic EL display panel 100 including forming an organic EL unit on the anode / pixel element 17. Thus, Matsueda teaches element 11[e].

g. 11[f]: “forming a second electrode layer on the organic EL unit.”

110. As shown for element 1[a], Matsueda teaches forming a cathode 14 (“second electrode layer”) on the organic EL unit. Thus, Matsueda teaches “a second electrode layer on the organic EL unit.”

111. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process

includes all steps for forming the organic EL display panel 100 including forming the cathode 14 on the organic EL unit. Thus, Matsueda teaches element 11[f].

11. Claim 12: “The method of claim 11, wherein forming of the sub-conductive layer is simultaneous with forming the first electrode layer.”

112. As shown for element 1[d], Matsueda teaches an ITO layer 18 (“sub-conductive layer”). As shown for element 1[a], Matsueda teaches an anode / pixel element 17 (“first electrode layer”).

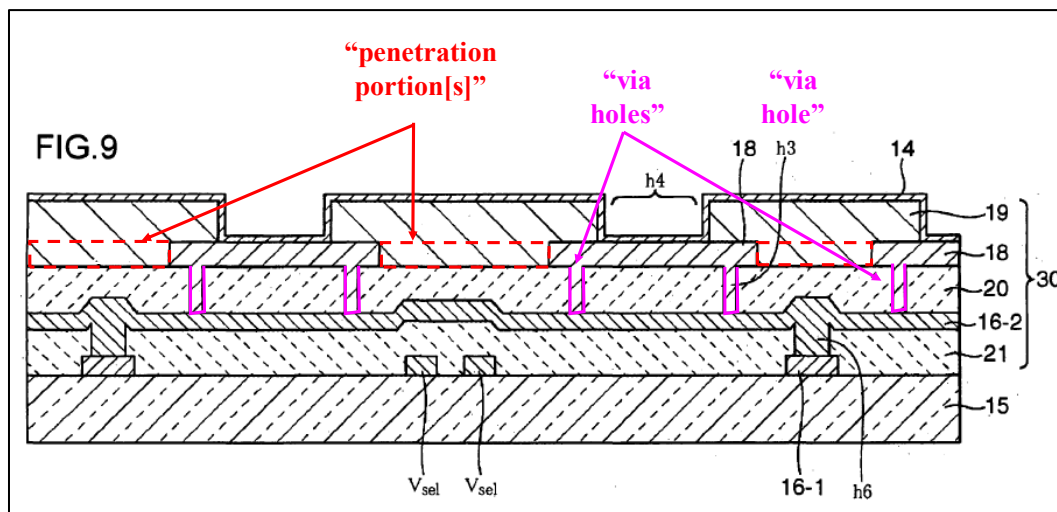
113. As shown for claim 2, Matsueda teaches the ITO layer 18 comprising the same layer as at least a part of the anode / pixel element 17. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. A POSITA would have understood that forming the ITO layer 18 to be the same layer as at least part of the anode / pixel element 17 means forming the ITO layer 18 simultaneous with forming the anode / pixel element 17. This is because display devices are fabricated by sequentially depositing layers on top of one another, where two or more parts, such as Matsueda’s ITO layer 18 and anode / pixel element 17, of the same layer are formed at the same time. It would have also been obvious to a POSITA to form the anode / pixel element 17 using ITO because doing so was known in the art. For example, Matsueda discloses in another one of his patents (EX1010) that “[t]he ITO layer 59 is patterned so as to form a pixel electrode layer

(an anode) 59.” (EX1010, 5:21-22.) As another example, EX1008 describes an anode, referred to as pixel electrode 23, made of ITO. (EX1008, 5:57, 7:10.)

12. Claim 13: “The method of claim 11, wherein two or more via holes are formed when the via hole is formed, and the penetration portion is formed between the via holes when the penetration portion is formed.”

114. As shown for element 1[c], Matsueda discloses contact hole h3 (“via hole”). As shown for element 1[f], Matsueda discloses a penetration portion.

115. Matsueda teaches “two or more via holes are formed when the via hole is formed.” For example, Matsueda discloses “[t]he contact holes h3 are formed at multiple positions along the direction in which the auxiliary cathode wiring 16 extends.” (EX1004, [0052].) Figure 9 (annotated below) shows two or more *contact holes h3* that are formed on the same layer. Because two or more other contact holes h3 are formed on the same layer as the contact hole h3, the two or more other contact holes are formed when the contact hole h3 is formed.



116. Matsueda also teaches “the penetration portion is formed between the via holes when the penetration portion is formed.” For example, Figure 9 (annotated above) shows the *penetration portion* is formed between the *contact holes h3* when the penetration portion is formed.

13. Claim 14

- a. **14[a]: “The method of claim 11, wherein forming the penetration portion comprises forming two or more penetration portions, and”**

117. As shown for element 3[a], Matsueda teaches two or more penetration portions.

118. As shown for the preamble of claim 11, Matsueda teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. It would have been obvious that the manufacturing process includes all steps for forming the organic EL display panel 100 including forming the penetration portion comprising forming two or more penetration portions. Thus, Matsueda teaches element 14[a].

- b. **14[b]: “a distance between the penetration portions is less than or equal to a maximum distance between two ends of the first electrode layer.”**

119. Element 14[b] is similar to element 3[b], which Matsueda teaches. The table below shows the similarities.

Element 3[b]	Element 14[b]
“a distance between the two penetration portions is less than or equal to a maximum distance between both ends of the first electrode layer.”	“a distance between the penetration portions is less than or equal to a maximum distance between two ends of the first electrode layer.”

14. Claim 15

- a. Preamble: “A method of manufacturing an electroluminescence display device, comprising:”**

120. The preamble of claim 15 is similar to the preamble of claim 11, which Matsueda teaches. The table below shows the similarities.

Preamble of Claim 11	Preamble of Claim 15
“A method of manufacturing an electroluminescence display device, comprising:”	“A method of manufacturing an electroluminescence display device, comprising:”

- b. 15[a]: “forming an insulating layer including an organic material on an electrode power supply line;”**

121. Element 15[a] is similar to element 11[a], which Matsueda teaches. The table below shows the similarities.

Element 11[a]	Element 15[a]
“forming an insulating layer including an organic material on an electrode power supply line;”	“forming an insulating layer including an organic material on an electrode power supply line;”

- c. 15[b]: “forming a via hole on the insulating layer;”**

122. Element 15[b] is similar to element 11[b], which Matsueda teaches. The table below shows the similarities.

Element 11[b]	Element 15[b]
“forming a via hole on the insulating layer;”	“forming a via hole on the insulating layer;”

- d. **15[c]: “forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”**

123. Element 15[c] is similar to element 11[c], except that element 15[c] additionally requires the “sub-conductive layer comprising a plurality of unit sub-conductive layers.” Matsueda teaches element 11[c]. Additionally, Matsueda teaches the “sub-conductive layer comprising a plurality of unit sub-conductive layers.” The table below shows the similarities.

Element 11[c]	Element 15[c]
“forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”	“forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”

- e. **15[d]: “forming an organic EL unit on the first electrode layer; and”**

124. Element 15[d] is similar to element 11[e], which Matsueda teaches. The table below shows the similarities.

Element 11[e]	Element 15[d]
“forming an organic EL unit on the first electrode layer; and”	“forming an organic EL unit on the first electrode layer; and

f. 15[e]: “forming a second electrode layer on the organic EL unit.”

125. Element 15[e] is similar to element 11[f], which Matsueda teaches.

The table below shows the similarities.

Element 11[f]	Element 15[e]
“forming a second electrode layer on the organic EL unit.”	“forming a second electrode layer on the organic EL unit.”

B. Claim 7 Is Obvious Over Matsueda And Yamazaki

1. Summary of Yamazaki

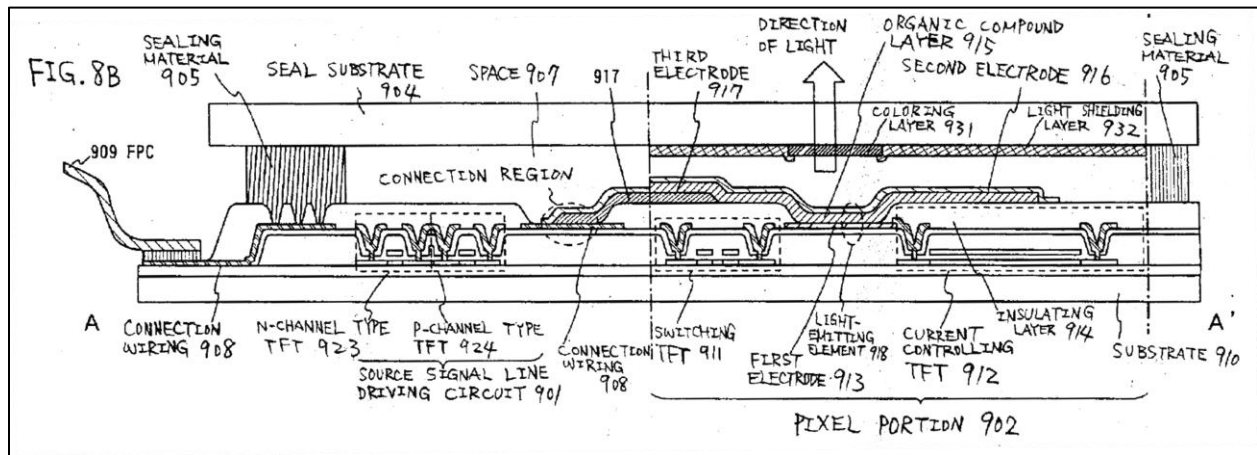
126. Yamazaki is titled “Method of Fabricating Light-Emitting Device and Apparatus for Manufacturing Light-Emitting Device.” It discloses the structure of a “light-emitting device which is typified by EL element.” (EX1005, [0002].)

“This light-emitting device is also referred to as an organic EL display (OELD: Organic EL Display) or organic light-emitting diode (OLED: Organic Light Emitting Diode).” (EX1005, [0004].)

127. Yamazaki’s OLED display device comprises “pixel portion 902 is formed by a plurality of pixels each including a switching TFT 911, a current controlling TFT 912, and a first electrode (anode) 913 electrically connected to a drain of the current controlling TFT 912.” (EX1005, [0109].) It also comprises a “second electrode (cathode) 916 [that] functions also as a wiring common to all the

pixels and electrically connected to FPC 909 via the connection wiring 908.”

(EX1005, [0111].) Figure 8B (below) shows a cross-sectional view of the structure of Yamazaki’s OLED display device.



2. Claim 7

- a. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

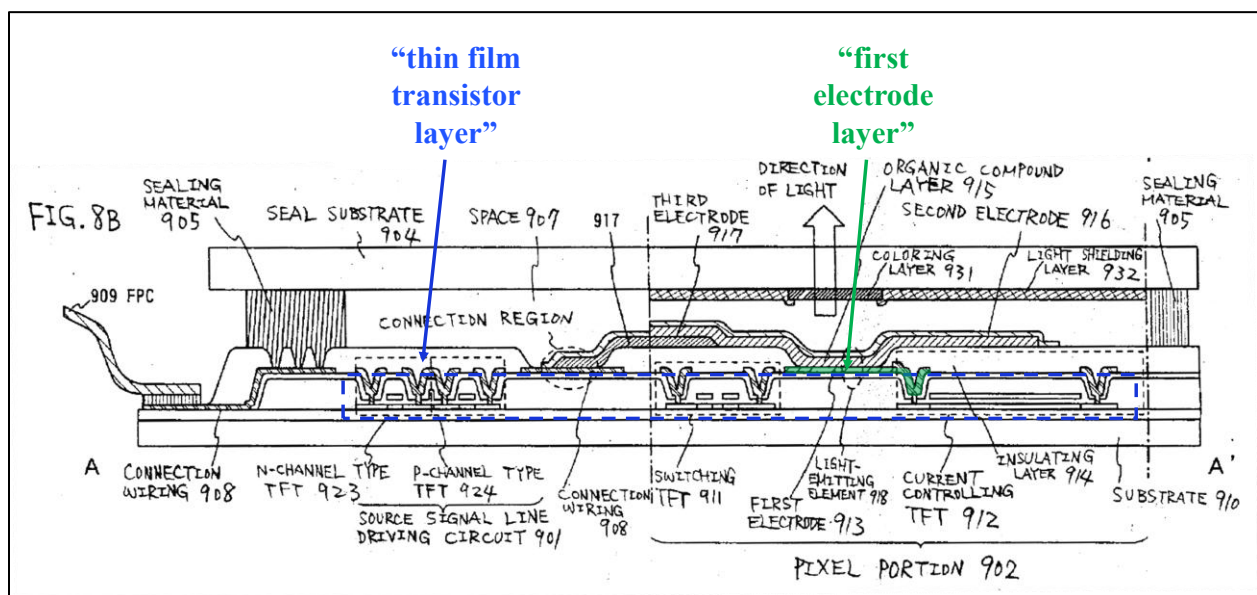
128. As shown above, Matsueda teaches claim 7. If, for some reason, Matsueda does not teach some of the limitations of claim 7, Yamazaki does. As shown for element 1[a], Matsueda teaches an anode 17 (“first electrode layer”).

129. If, for some reason, Matsueda does not teach “a thin film transistor layer [] disposed under the first electrode layer,” Yamazaki teaches “a thin film transistor layer is disposed under the first electrode layer.” For example, Yamazaki discloses “the pixel portion 902 is formed by a plurality of pixels each including a switching TFT 911, a current controlling TFT 912, and a first electrode (anode) 913 electrically connected to a drain of the current controlling TFT 912.”

(EX1005, [0109].) “Further, an insulating layer 914 is formed at both ends of the first electrode (anode) 913 and an organic compound layer 915 is formed on the first electrode (anode) 913.” (EX1005, [0110].)

130. Figure 8B (below) shows that the *layer of the switching TFT 911, current controlling TFT 912, and other TFTs* is disposed under the *anode 913*.

Thus, Yamazaki teaches element 7[a].

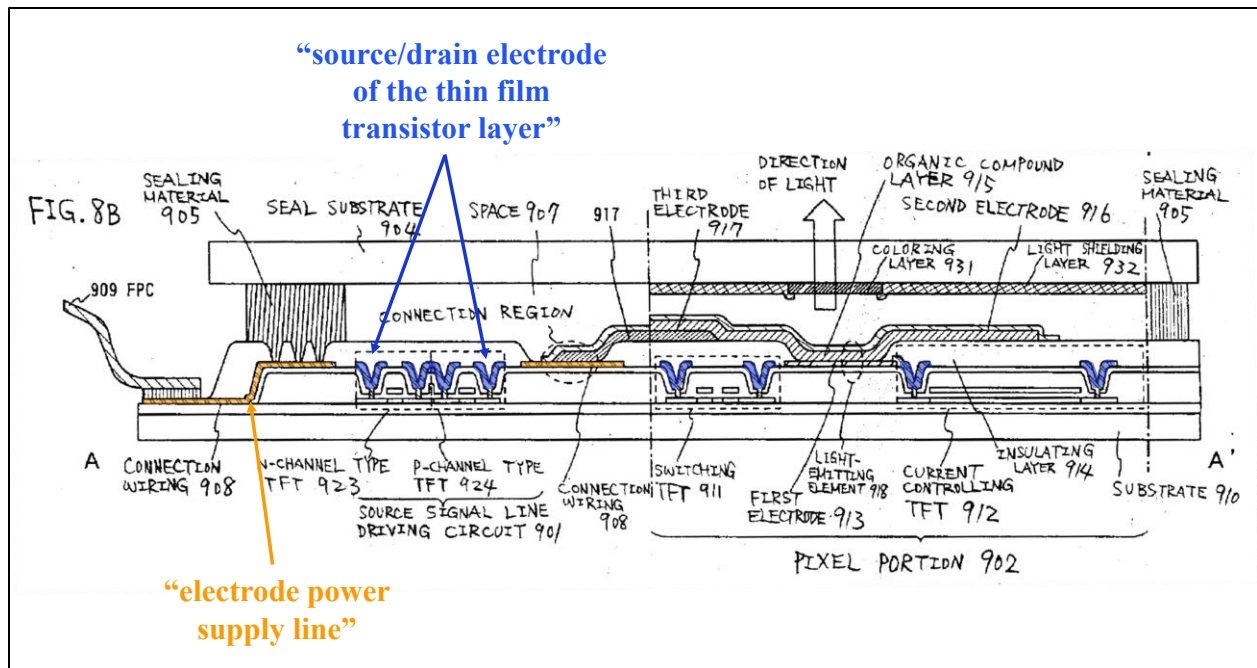


- b. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”

131. As shown for element 1[b], Matsueda teaches an auxiliary cathode wiring 16 (“electrode power supply line”). The auxiliary cathode wiring 16 is electrically connected to the cathode 14 and configured to supply electrical power to the cathode. (EX1004, [0061], [0064].)

132. As shown for element 7[a], Yamazaki teaches a layer of the switching TFT 911, current controlling TFT 912, and other TFTs (“thin film transistor layer”).

133. Yamazaki teaches “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.” For example, Yamazaki discloses “[t]he second electrode (cathode) 916 functions also as a wiring common to all the pixels and electrically connected to FPC 909 via the connection wiring 908.” (EX1005, [0111].) Thus, connection wiring 908 is electrically connected to the cathode 916. It would have been obvious that the connection wiring 908 is an electrode power supply line configured to supply electrical power to the cathode because it transmits signals from the driving circuits and is common to all pixels. Figure 8B (annotated below) shows the *connection wiring 908* comprises a layer that is the same layer as the *source/drain electrode of the thin film transistor layer*.



134. It would have been obvious to a POSITA at the time of the '708 patent to combine Matsueda and Yamazaki. Matsueda and Yamazaki both relate to OLED devices having auxiliary wiring and TFTs. Matsueda teaches an OLED display panel 100 that includes auxiliary cathode wiring 16 to reduce the “wiring resistance of the common electrode [that] leads to an increased voltage drop in pixels in the center of the screen.” (EX1004, [0005].) The increased voltage drop causes issues with “a gray-scale [] not [being] displayed accurately and display performance decreas[ing].” (EX1004, [0005].) Similarly, Yamazaki teaches “a light-emitting device having EL element” such as an organic OLED or OLED display device. (EX1005, [0004].) Yamazaki’s OLED display comprises an auxiliary electrode used “[f]or attaining a low-resistance cathode.” (EX1005, [0100], [0111].) Thus, Matsueda and Yamazaki are from the same field of

endeavor and reasonably pertinent to the same technical problems of lowering the resistance of the cathode to enhance the display performance.

135. Matsueda describes that its OLED display device includes a pixel circuit comprising “a switching transistor Tr1, a driving transistor Tr2, a storage capacitor C, and a light-emitting section OLED.” (EX1004, [0049].). Matsueda also explains that “[e]lectronic devices, such as a transistor, may lie between the first electrode layers and the first power lines in the invention.” (EX1004, [0009].) The ITO layer 18 is also disposed on the source metal layer 22, as shown in Figure 4, which is a source electrode layer of the transistor. (EX1004, [0052].) Thus, a POSITA would have been motivated to look to another reference, such as Yamazaki, for disclosures of such details.

136. There would have been a reasonable expectation of success because the structure of Matsueda’s OLED display device is similar to the structure of Yamazaki’s OLED display device. Both OLED display devices include auxiliary wiring connected to the cathode and transistors such as switching transistors and current controlling / driving transistors. Both apply to top-emission structures. (EX1004, [0048]; EX1005, [0095]-[0096], Fig. 8B.) Because of the amount of overlap between Matsueda and Yamazaki and given that the art has already demonstrated success, it would have been obvious to combine the teachings of Matsueda and Yamazaki.

C. Claims 1, 2, 5, 7, 9, 11, 12, And 15 Are Obvious Over Koyama And Nakanishi

1. Summary of Koyama

137. Koyama is titled “Self-Luminous Device and Electric Machine Using the Same.” (EX1006, Title.) It discloses “a self-luminous device (or an EL display device) manufactured by forming a light emitting element (such as an EL (Electro Luminescence) element) on a substrate.” (EX1006, [0002].) “The light emitting element here is also called an OLED (Organic Light Emitting Device).” (EX1006, [0002].)

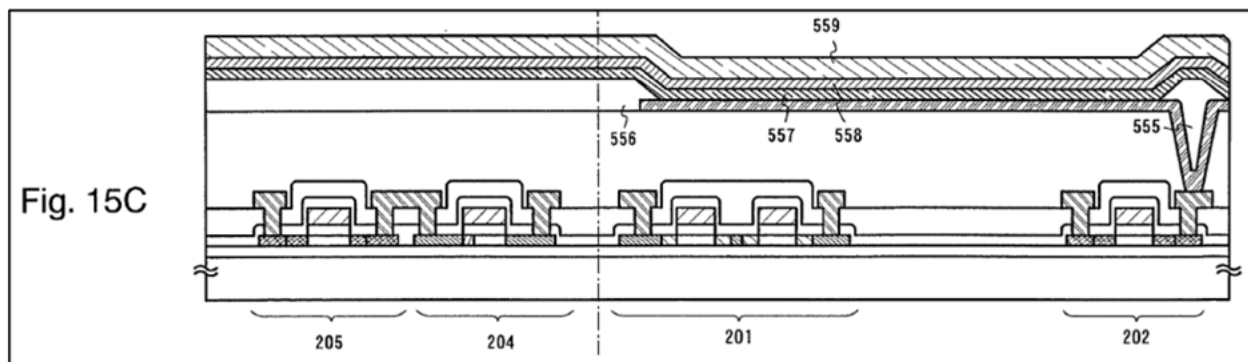
138. Koyama’s display device comprises a pixel portion 101/1201 having a plurality of pixels 104. (EX1006, [0110].) Each pixel has “an independent EL element. All pixels have a protective electrode 1207 as an electrode common to the pixels.” (EX1006, [0220].) Each pixel comprises a pixel electrode 554, an EL layer 558, and a cathode 559. (EX1006, [0202]-[0206], Fig. 15C.)

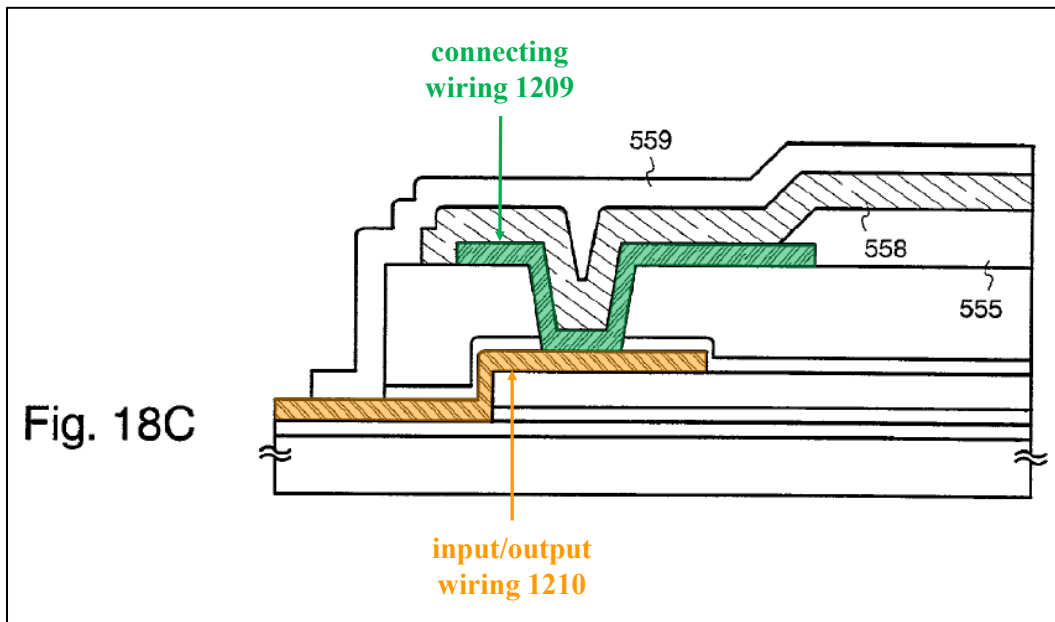
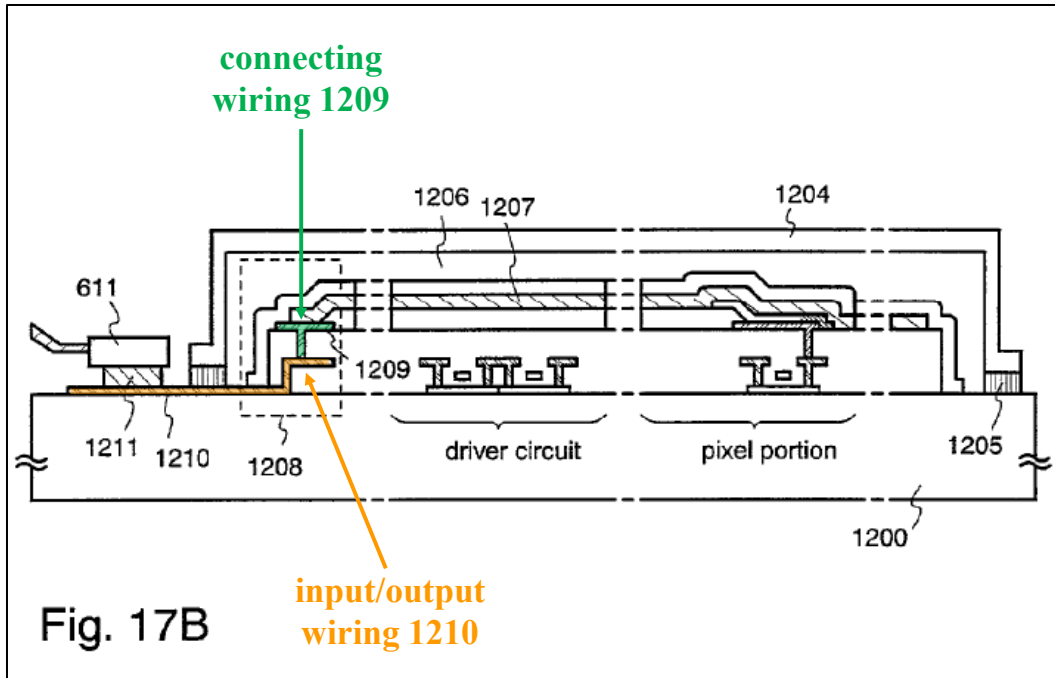
139. The pixels receive a voltage via connecting wiring 1209, which is connected to input/output wiring 1210. (EX1006, [0222].) “The *input/output wiring 1210* is a power supply line for applying a given voltage (ground potential in this embodiment, specifically, 0V) to the protective electrode 1207.” (EX1006, [0222].) And circuits are used to operate the display device, including “a TFT functioning as a switching element (hereinafter referred to as switching TFT), 302, a TFT functioning as an element for controlling current supplied to an EL element

303 (current controlling element) (hereinafter referred to as current controlling TFT), and 304, a capacitor (storage capacitor).” (EX1006, [0006].)

140. Koyama also discloses the manufacturing of the display device, including forming the TFTs on a substrate in the pixel portion, forming an interlayer insulating film 553 on the layer of TFTs to level the surface, and then subsequently forming the pixel electrode 554, EL layer 558, cathode 559, and protective electrode 1207. (EX1006, [0194], [0201], [0203]-[0206], [0220].) The protective electrode 1207 is connected to the input/output wiring 1210 through a connecting wiring 1209. (EX1006, [0222].)

141. Figures 15C, 17B, and 18C (below) show Koyama’s display device including *connection wiring 1209* and *input/output wiring 1210*.





2. Summary of Nakanishi

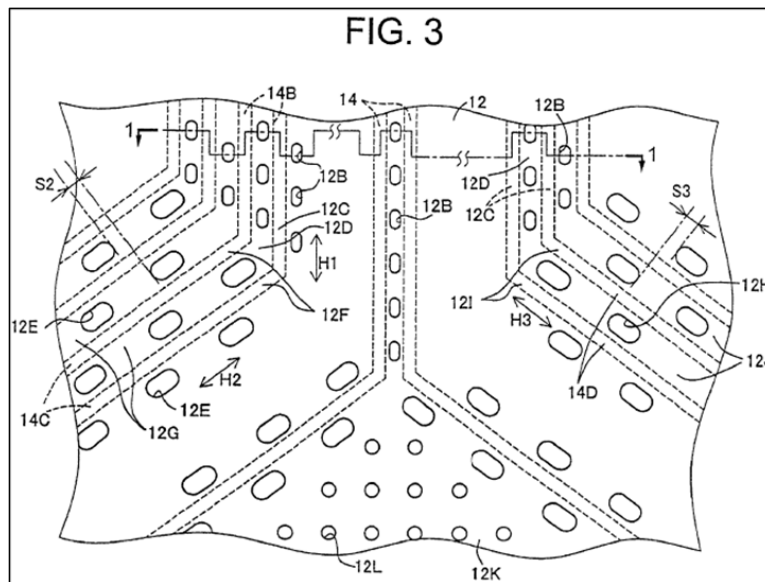
142. Nakanishi is titled “Wiring Substrate.” (EX1007, Title.) It discloses a wiring substrate comprising a conductive layer 12 having wiring correspondence

regions separated by wiring noncorrespondence regions. (EX1007, Abstract.) The conductive layer 12 is on a core substrate 11, which is “formed from a glass-epoxy-resin composite material.” (EX1007, [0043].)

143. Nakanishi explains that “a conductor layer has poorer gas release properties than a dielectric layer, which is especially important during firing, curing, thermal treatment, and other processes performed during manufacture of the wiring substrate. Therefore, during the course of such treatments or processes, a conductor layer having a large area is likely to hinder diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer, which reduces the bonding strength between the layers of the wiring substrate.” (EX1007, [0006].)

144. Nakanishi’s solution is to follow “conventional wisdom [] to provide a conductor layer . . . , with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].)

145. Figures 1 and 3 (below) show the conductive layer 12 comprising through holes 12B, 12E, 12H, and 12L.



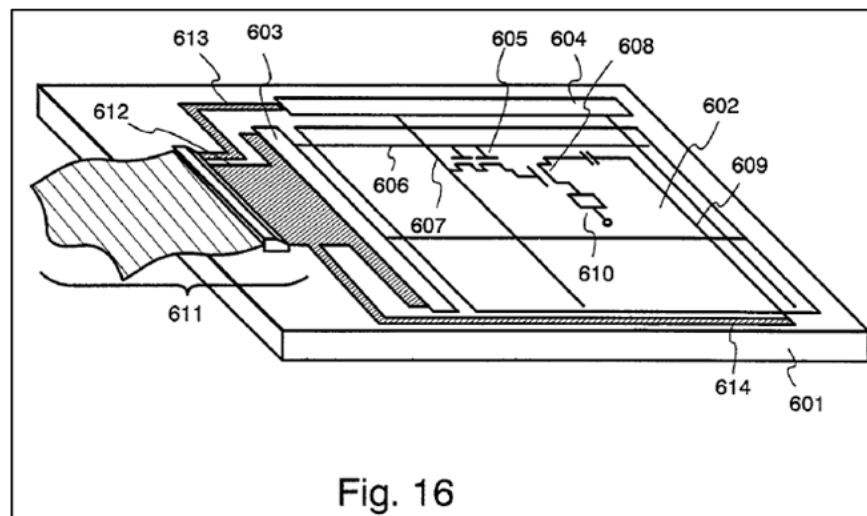
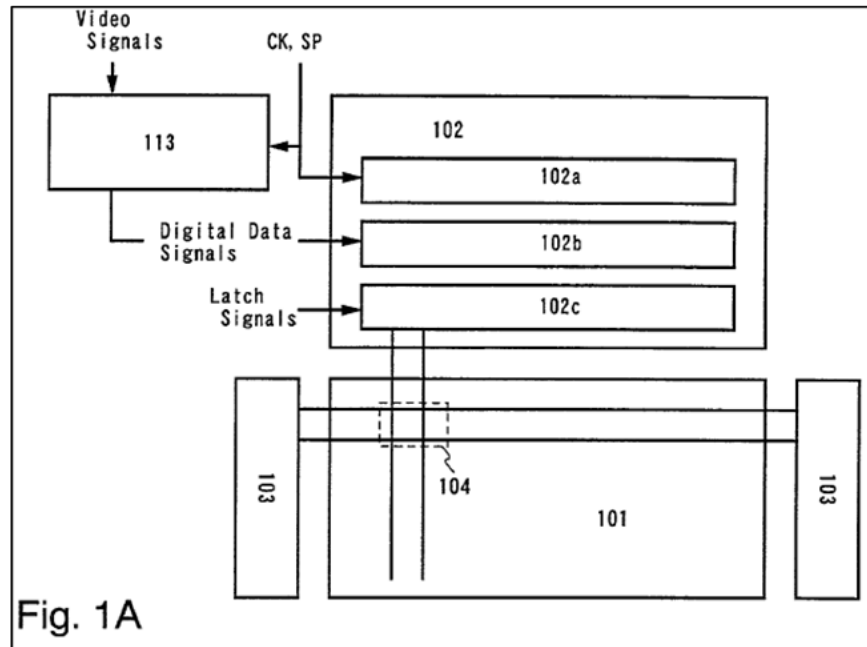
a. Preamble: “An electroluminescence display device, comprising:”

80

(such as an EL (Electro Luminescence) element) on a substrate, and an electric machine having the self-luminous device as a display (display unit). ***The light emitting element here is also called an OLED (Organic Light Emitting Device).***” (EX1006, [0002] (emphases added).)

147. Koyama also discloses “[t]he light emitting element has a layer containing an EL material that can provide EL (Electro Luminescence: the luminescence generated by applying an electric field) (hereinafter referred to as EL layer), in addition to an anode and a cathode. The luminescence generated from an EL material includes light emission (fluorescence) upon returning from the singlet excitation to the ground state and light emission (phosphorescence) upon returning from the triplet excitation to the ground state. ***The self-luminous device of the present invention can use both types of light emitting elements with one type containing fluorescent EL materials and the other type containing phosphorescent EL materials.***” (EX1006, [0003] (emphasis added).)

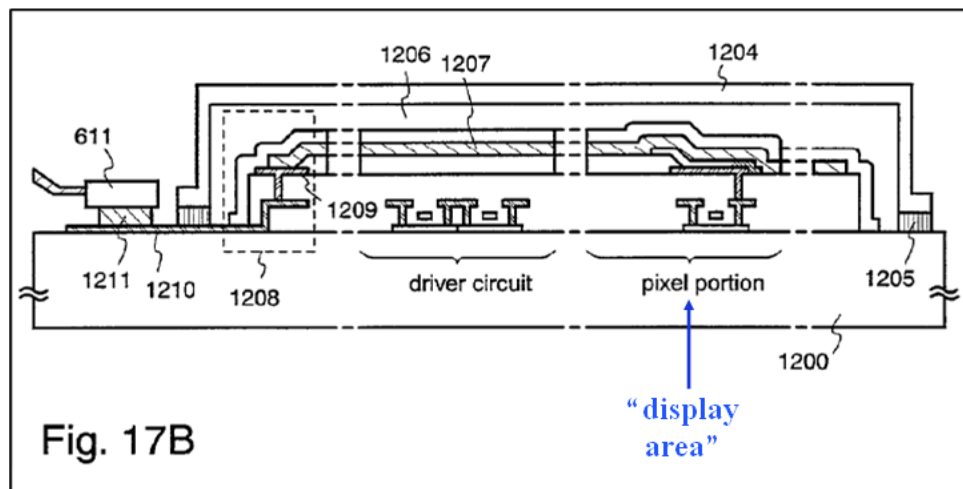
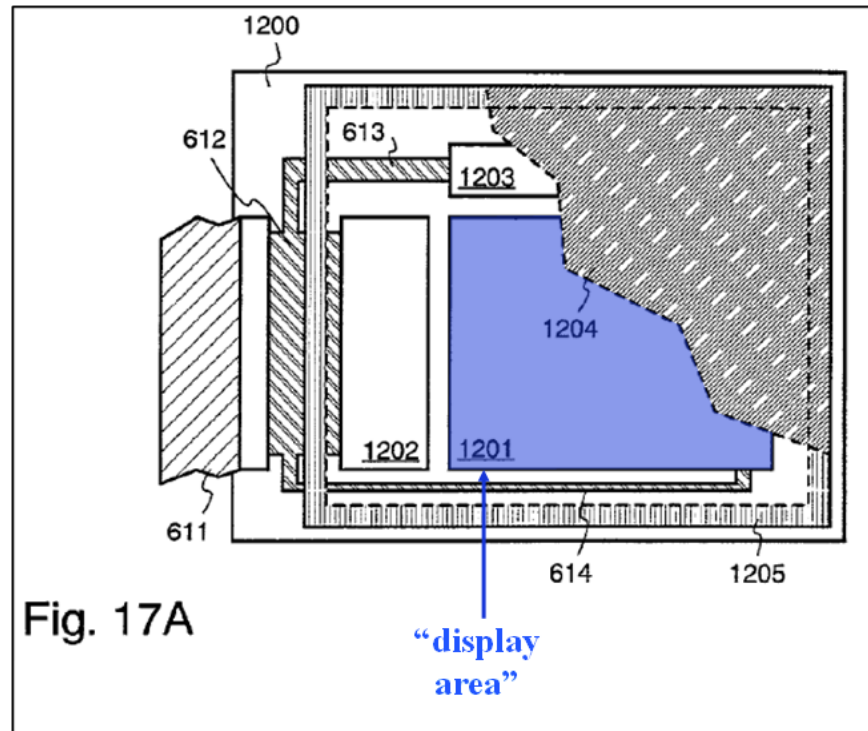
148. Figures 1A and 16 (below) show Koyama’s EL display device.



- b. 1[a]: “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

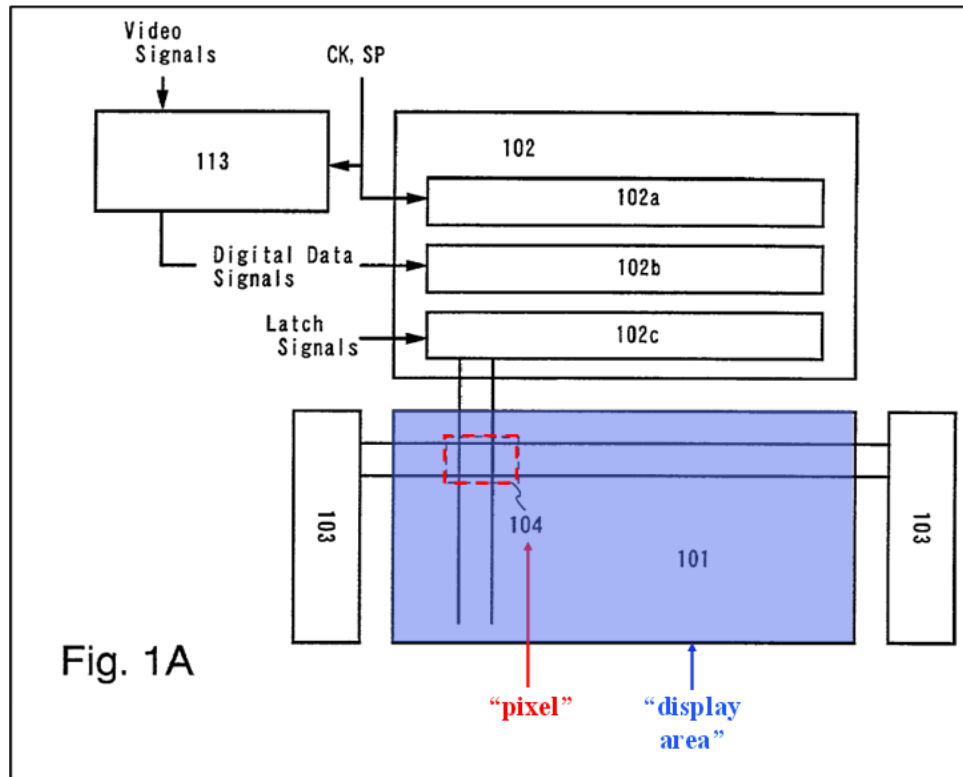
149. Koyama teaches “a display area with pixels.” For example, Koyama discloses “[a]s shown in FIG. 17B, the pixel portion is provided with a plurality of

pixels each having an independent EL element.” (EX1006, [0220].) Figures 17A and 17B (annotated below) show the pixel portion 1201 with a plurality of pixels.



150. Koyama also discloses “[t]he pixel portion 101 has a plurality of pixels 104 arranged in a matrix-like manner. FIG. 1B shows an enlarged view of

the pixels 104.” (EX1006, [0100].) Figure 1A (annotated below) shows the *pixel portion 101* with a *plurality of pixels 104*.



151. Koyama provides additional disclosures to show that it teaches a “display area with pixels”:

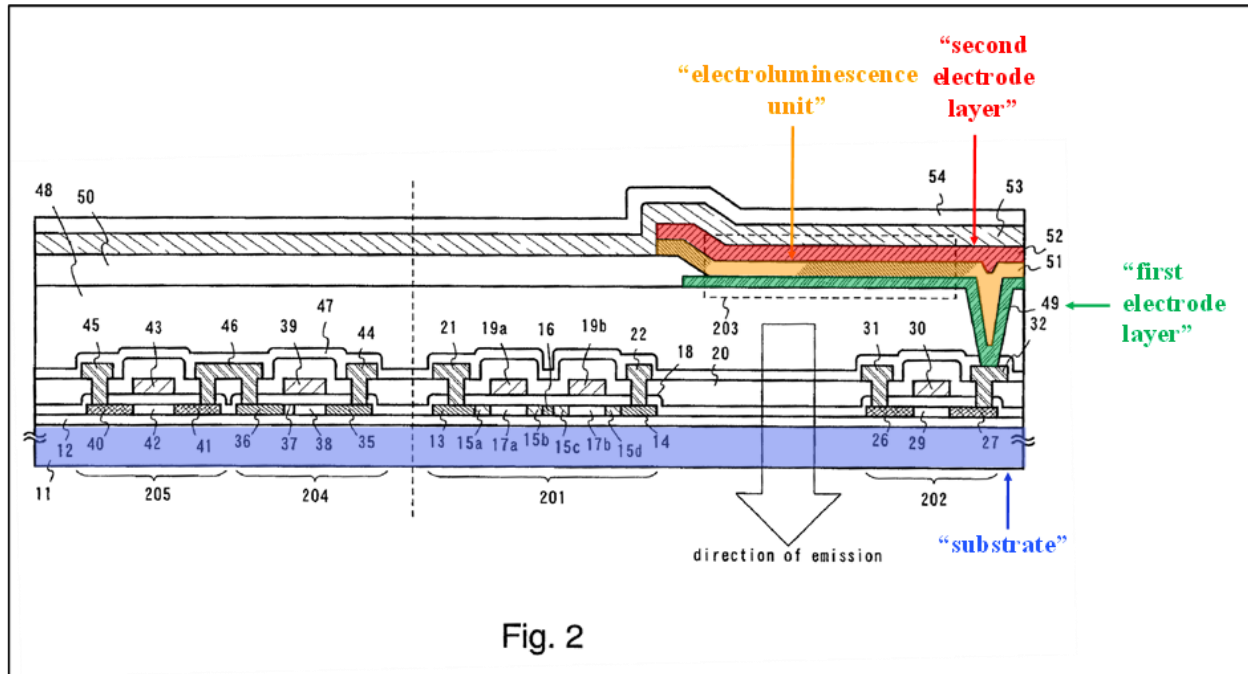
- “The TFTs constitute a pixel portion 101 and a data signal side driver circuit 102 and gate signal side driver circuits 103 with the three of them arranged on the periphery of the pixel portion.” (EX1006, [0083].)
- “The pixel portion 101 has 640x480 (width×length) pixels.” (EX1006, [0087].)

- “The active matrix self-luminous device according to this embodiment is composed of a pixel portion 602, a gate side driver circuit 603, and a source side driver circuit 604, which are formed on a glass substrate 601.” (EX1006, [0210].)
- “A pixel portion 1201, a data signal side driver circuit 1202, and a gate signal side driver circuit 1203 are formed on a substrate 1200.” (EX1006, [0214].)

152. Koyama also teaches “a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer.” For example, Koyama discloses “[t]he substrate 11 is a transparent substrate, and typical examples of a transparent substrate usable as the substrate 11 include a glass substrate, a quartz substrate, a glass ceramic substrate and a crystalline glass substrate.” (EX1006, [109].)

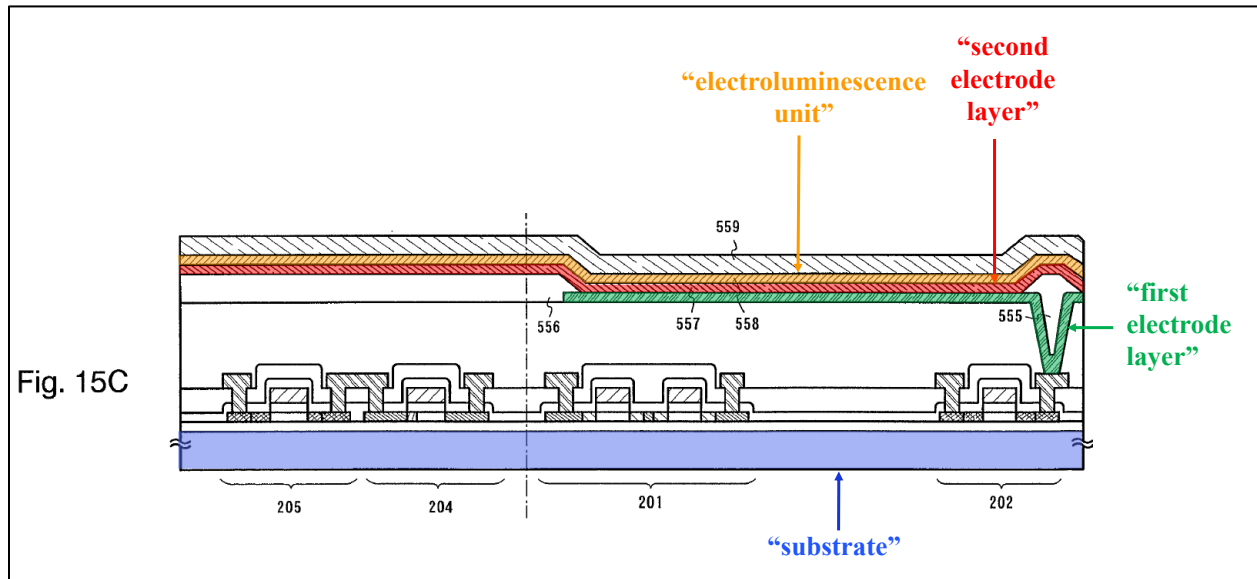
“Reference symbol 49 denotes a pixel electrode (an anode of the EL element) formed of a conductive oxide film.” (EX1006, [0129].) “An EL layer 51 is formed on the insulating film 50.” (EX1006, [0130].) “A cathode 52 of the EL element is formed on the EL layer 51.” (EX1006, [0133].) “The EL element herein refers to a light emitting element composed of a pixel electrode (anode), an EL layer, and a cathode.” (EX1006, [0134].)

153. Figure 2 (annotated below) shows the *pixel electrode 49* (“first electrode layer”) and *cathode 52* (“second electrode layer”) on a *substrate 11*. The figure also shows the *EL layer 51* formed between the pixel electrode 49 and the cathode 52.



154. Koyama also discloses “a base film 501 is formed to a thickness of 300 nm on a glass substrate 500.” (EX1006, [0173], Fig. 13A.) “A contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.” (EX1006, [0202].) “After that, a hole injection layer 557 and a light emitting layer 558 are formed by spin coating.” (EX1006, [0204].) “Next, a cathode 559 is formed to a thickness of 400 nm from a conductive film having low work function.” (EX1006, [0206].)

155. Figure 15C (annotated below) shows the *pixel electrode 554* and *cathode 557* on a *substrate 500*. The figure also shows the *light emitting layer 558* formed between the pixel electrode 49 and the cathode 42.



156. Koyama provides additional disclosures about an anode / pixel electrode (“first electrode layer”), cathode (“second electrode layer”), substrate, and an EL unit:

- “The light emitting element has a layer containing an EL material that can provide EL (Electro Luminescence: the luminescence generated by applying an electric field) (hereinafter referred to as EL layer), in addition to an anode and a cathode.” (EX1006, [0003].)
- “The EL element 109 is composed of an EL layer, an anode (pixel electrode) connected to the current controlling TFT 108, and a

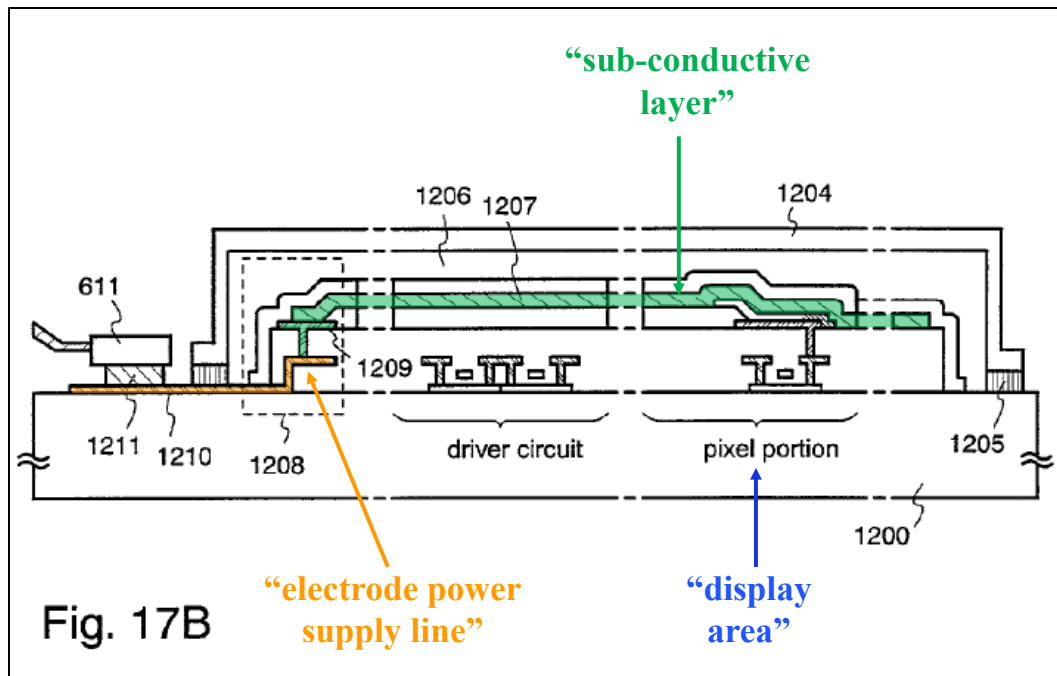
cathode (opposite electrode) provided so as to oppose the anode across the EL layer sandwiched therebetween.” (EX1006, [0101].)

c. 1[b]: “an electrode power supply line to supply electrode power to the display area;”

157. As shown for element 1[a], Koyama teaches a pixel portion 101/1201 (“display area”).

158. Koyama teaches “an electrode power supply line to supply electrode power to the display area.” For example, Koyama discloses “[i]n a region denoted by 1208, *the protective electrode 1207 is connected to an input/output wiring 1210 through a connecting wiring 1209* that is formed of the same material as the pixel electrode. *The input/output wiring 1210 is a power supply line for applying a given voltage (ground potential in this embodiment, specifically, 0V) to the protective electrode 1207.* The input/output wiring 1210 is connected to the FPC 611 through a conductive paste material 1211.” (EX1006, [0222], Fig. 17A.) Koyama’s pixels have a protective electrode 1207 as an electrode common to the pixels. (EX1006, [0220].)

159. Figure 17B (annotated below) shows *input/output wiring 1210* supplying electrode power to the *protective electrode 1207 via connecting wiring 1209*, which as shown in the figure, is in the *pixel portion*. The protective electrode 1207 is a common electrode to the display area.



160. Koyama provides additional disclosures that show that it teaches “an electrode power supply line to supply electrode power to the display area”:

- “An FPC 611 serving as an external input/output terminal is provided with input/output wirings (connecting wirings) 612 and 613 for transmitting signals to the driver circuits, and an input/output wiring 614 connected to the power supply line 609.” (EX1006, [0212].)
- “In the structure according to this embodiment, ground potential (earth potential) is given to the power supply line 609. The current controlling TFT 608 has a drain region connected to an EL element 610. A given voltage (10 to 12 V, in this embodiment) is applied to a cathode of the EL element 610.” (EX1006, [0211], Fig. 16.)

- “A pixel portion 1201, a data signal side driver circuit 1202, and a gate signal side driver circuit 1203 are formed on a substrate 1200. The wirings from the respective driver circuits are connected through the input/output wirings 612 to 614 to the FPC 611 and to external equipment.” (EX1006, [0214].)
- “The protective electrode 558 is thus electrically connected to the input/output wiring 1210 through the connection wiring 1209.” (EX1006, [0226].)

d. 1[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”

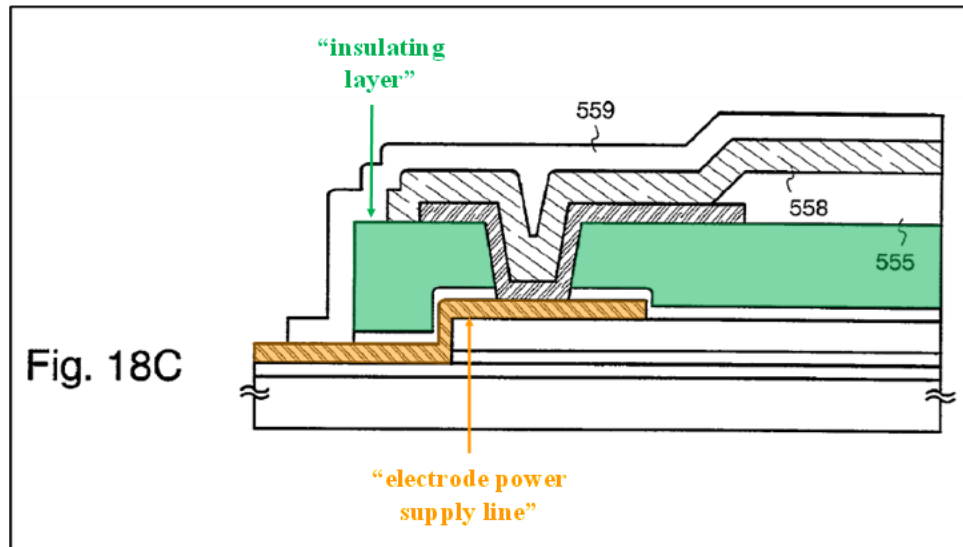
161. As shown for element 1[b], Koyama teaches input/output wiring 1210 (“electrode power supply line”), which is connected to connecting wire 1209, protective electrode 1207, cathode 557, and pixel electrode 554. (EX1006, Figs. 15A-15C.)

162. Koyama teaches “an insulating layer . . . containing an organic material.” For example, “*a second interlayer insulating film 553 is formed from an organic resin* as shown in FIG. 15B. Usable organic resins include polyimide, polyamide, acrylic resin, and BCB (benzocyclobutene).” (EX1006, [0201], Fig. 15B (emphasis added).)

163. Koyama explains that “[t]he major role of the second interlayer insulating film 553 is leveling, and hence acrylic resin having a superior leveling effect is particularly preferable.” (EX1006, [0201], Fig. 15B (emphasis added).) Koyama also discloses “[r]eference symbol 48 denotes a second interlayer insulating film, which has a function of a leveling film for leveling a level difference caused by the TFTs. ***A preferred material for the second interlayer insulating film 48 is an organic resin film***, such as a polyimide film, a polyamide film, an acrylic film, or a BCB (benzocyclobutene) film. These organic resin films are advantageous in that they are easy to form a very flat surface and relative dielectric constant thereof is low. An EL layer is extremely sensitive to unevenness, and the level difference caused by the TFTs is desired to be absorbed almost completely by the second interlayer insulating film.” (EX1006, [0128] (emphasis added).)

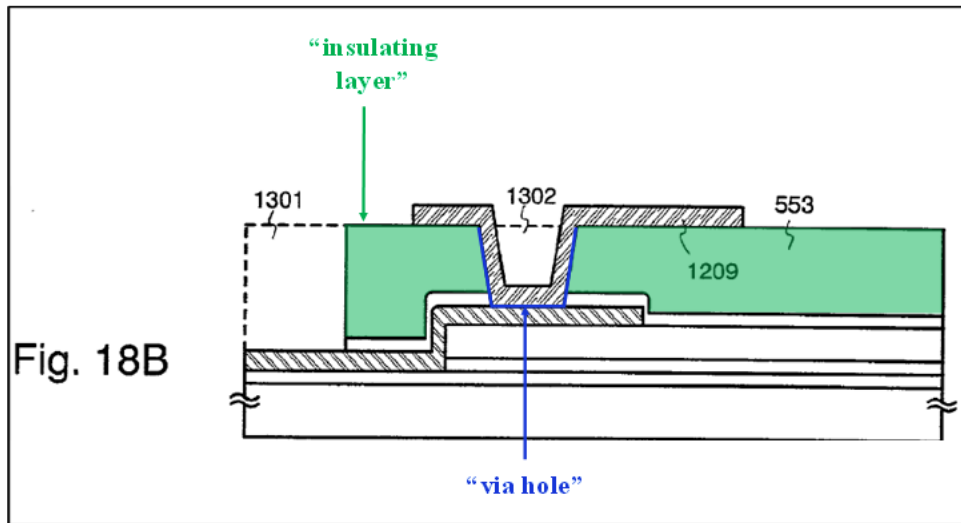
164. Koyama teaches the “insulating layer disposed on the electrode power supply line.” For example, Koyama discloses “[a]t this point, an end of the substrate (the region denoted by 1208 in FIG. 17B) is rid of the first interlayer insulating film 544 and the gate insulating film 514 thereof, and the ***input/output wiring 1210 is formed thereon***.” (EX1006, [0224] (emphasis added).)

165. Figure 18C (annotated below) shows the *interlayer insulating film 553* disposed on the *input/output wiring 1210*.



166. Koyama also teaches the “insulating layer . . . including a via hole.” For example, Koyama discloses “[a] contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.” (EX1006, [0202], Fig. 15B.) Koyama also discloses “the second interlayer insulating film 553 in FIG. 15B is partially etched. The connection wiring 1209 is formed on an opening 1302 to obtain the structure shown in FIG. 18B.” (EX1006, [0225].)

167. Figure 18B (annotated below) shows the *interlayer insulating film 553* including a *via hole*. The via hole is an opening that allows the connection wiring 1209 to electrically connect to input/output wiring 1210 (see Figure 18C above).

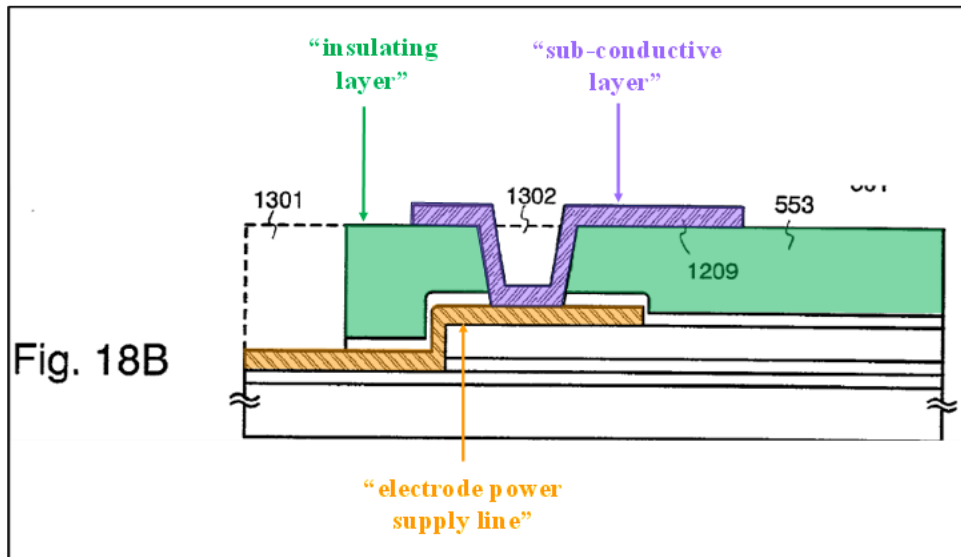


- e. 1[d]: “a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”

168. As shown for element 1[c], Koyama teaches an interlayer insulating film 553 (“insulating layer”) including a via hole. As shown for element 1[a], Koyama teaches input/output wiring 1210 (“electrode power supply line”).

169. Koyama teaches “a sub-conductive layer formed on the insulating layer . . . along the electrode power supply line.” For example, Koyama discloses “the second interlayer insulating film 553 in FIG. 15B is partially etched. The connection wiring 1209 is formed on an opening 1302 to obtain the structure shown in FIG. 18B.” (EX1006, [0225].)

170. Figure 18B (annotated below) shows the *connection wiring 1209* formed on the *interlayer insulating film 553*. The figure also shows the connection wiring 1209 formed along the *input/output wiring 1210*.

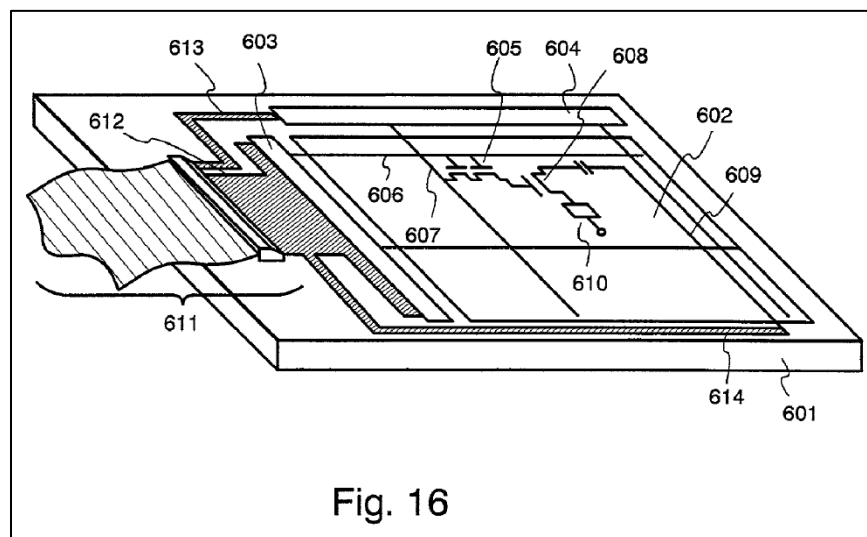


171. It would have been obvious that the connection wiring 1209 is formed along the input/output wiring 1210. This is because Koyama’s power supply line 609 is similar to connecting wiring 1209. Koyama explains that “an input/output wiring 614 connected to the power supply line 609.” (EX1006, [0212].) Similarly, “the protective electrode 1207 is *connected to an input/output wiring 1210 through a connecting wiring 1209* that is formed of the same material as the pixel electrode.” (EX1006, [0222] (emphasis added).) The power supply line 609 receives ground (“ground potential (earth potential) is given to the power supply line 609”) (*id.*, [0211])), and connection wiring 1209 does too via the input/output wiring 1210 (“[t]he input/output wiring 1210 is a power supply line for applying a given voltage (ground potential in this embodiment, specifically, 0V) to the protective electrode 1207”) (*id.*, [0222]).

172. Input/output wiring 614 is similar to input/output wiring 1210.

Input/output wiring 614 is connected to an FPC (FPC 111) ([0214]), and input/output wiring 1210 is connected to an FPC (FPC 611) ([0222]).

173. Figure 16 (below) shows the power supply line 609 extending along the input/output wiring 614. Given the similarities between power supply line 609 and connecting wiring 1209, and the similarities between input/output wiring 614 and input/output wiring 1210, it would have been obvious that the connection wiring 1209 is formed along the input/output wiring 1210.



- f. 1[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

174. As shown for element 1[b], Koyama teaches input/output wiring 1210 (“electrode power supply line”). As shown for element 1[a], Koyama teaches a

cathode 229/559 (“second electrode layer”). As shown for element 1[d], Koyama teaches connection wiring 1209 (“sub-conductive layer”).

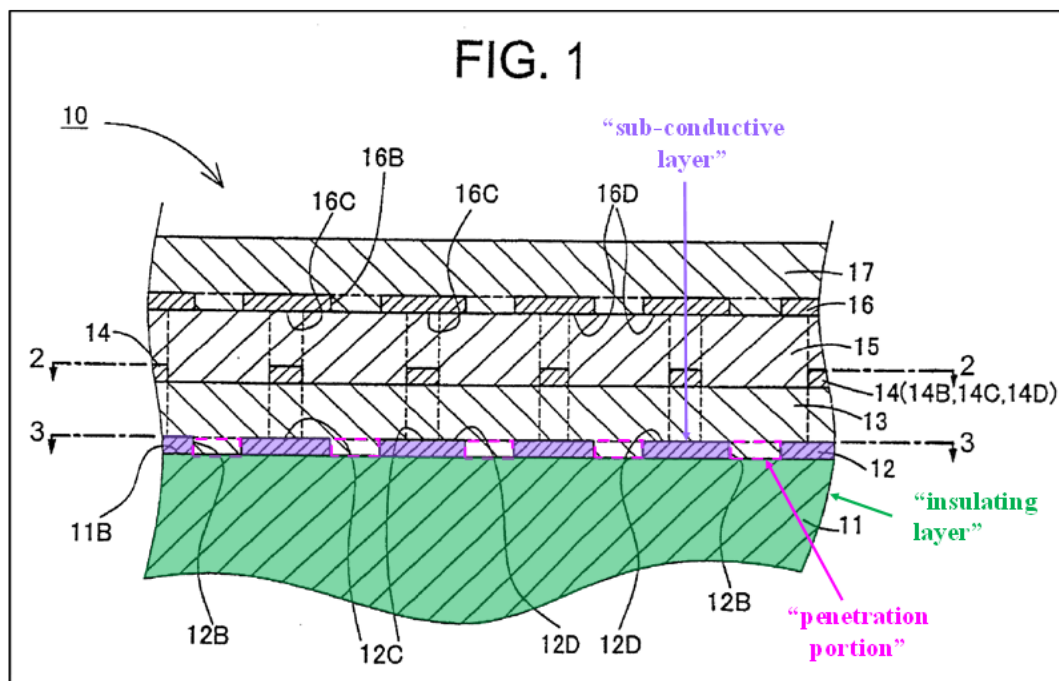
175. Koyama teaches “the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer.” For example, Koyama discloses “[i]n a region denoted by 1208, the protective electrode 1207 is connected to an input/output wiring 1210 through a connecting wiring 1209 that is formed of the same material as the pixel electrode.” (EX1006, [0222].) “The protective electrode 558 is thus electrically connected to the input/output wiring 1210 through the connection wiring 1209.” (EX1006, [0226].)

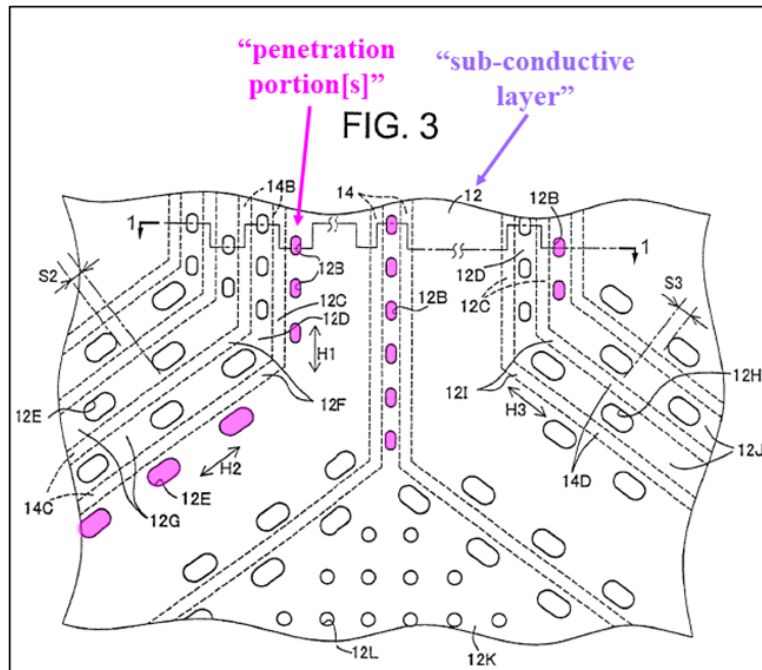
g. 1[f]: “the sub-conductive layer on the insulating layer includes a penetration portion.”

176. As shown for element 1[d], Koyama teaches a connection wiring 1209 (“sub-conductive layer”) on the interlayer insulating film 553 (“insulating layer”).

177. If, for some reason, Koyama does not teach the “sub-conductive layer . . . includes a penetration portion,” Nakanishi does. For example, Nakanishi discloses “[t]he first conductor layer 12 is a solid conductor layer and has a number of through holes 12B, 12E, 12H, and 12L formed therein. The through holes 12B are formed to directly connect the core substrate 11 and the first dielectric layer 13 therethrough, thereby enhancing the strength of the wiring substrate 10.” (EX1007, [0049].) “The core substrate is formed from a glass-epoxy-resin

composite material and has a thickness of about 600 um.” (EX1007, [0043].) A POSITA would have understood that glass-epoxy-resin is an insulating layer that contains an organic material due to the inclusion of resin. Figure 1 (annotated below) shows the *conductor layer 12* on the *core substrate 11*. Figure 1, along with Figure 3, (annotated below) also show the conductor layer 12 includes *through holes 12B, 12E, 12H, and 12L*. Thus, Nakanishi teaches element 1[f].





178. It would have been obvious to a POSITA at the time of the '708 patent to combine Koyama and Nakanishi. Koyama and Nakanishi both relate to conductor layers on insulating layers containing an organic material. Koyama teaches an organic display device comprising a connection wiring 1209 on an interlayer insulating film 553 containing an organic material (organic resin). (EX1006, [0201], [0225], Fig. 18B.) Nakanishi similarly teaches a wiring substrate comprising a conductor layer 12 on a core substrate 11 also containing an organic material (glass-epoxy-resin). (EX1007, [0043], [0049], Fig. 1.) Both of the devices of Koyama and Nakanishi are subjected to heat during the manufacturing process. A POSITA would have known that the heat treatment may lead to issues such as “a conductor layer . . . hinder[ing] diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release

phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer.” (EX1007, [0006].)

179. It was known in the art to release gas from an organic layer located below a metal layer. For example, Takahashi explains that “Difficulty has been encountered in incorporating these AC grounding planes into metal/polyimide structures. The difficulty results from the fact that the polyimide layers readily absorb water at room temperature, and readily release the water as steam when the structure is heated, which may occur during operation of the Substrate in the field from the power dissipation of integrated circuit components which are attached to the Substrate.” (EX1011, 2:7-14.) “The above delamination process may also occur when an upper polyimide layer is being cured by a heat treatment, or by other heat treatments which may be needed in the manufacturing of the multilayer substrate. In addition to releasing steam, polyimide layers which may not have been fully cured may release gases that are generated as part of the imidization process.” (EX1011, 2:31-37.) Takahashi teaches a “venting structure 10 [] formed within a metal layer 12, which may serve as an AC grounding plane or power distribution plane, or the like. . . . Venting structure 10 comprises an aperture 14 formed in metal layer 12. Aperture 14 may have any shape, and has a perimeter which encompasses its shape.” (EX1011, 3:34-46.) As another example, Ushio discloses “[c]onventionally used polyimide films have a saturated moisture

absorption of approximately 3% and contain approximately 1% moisture even at normal temperature and normal humidity (25°C, 50% RH). For this reason, when a polyimide-insulated multilayer board is exposed to high temperatures (250 to 300°C), such as during soldering, absorbed moisture contained in the polyimide rapidly vaporizes and expands, easily causing voids and large swelling at the interface between the polyimide and the conductor layer, and in some cases causing peeling or cracks at the interface between the metal conductor thin film layer and the polyimide insulating layer where stress is likely to concentrate.” (EX1012, EX1013, 490.) Ushio’s solution is “the polyimide insulating multilayer substrate of the present invention is a polyimide insulating multilayer substrate having a metal thin film conductor layer and a polyimide insulating layer constituting a power plane and a ground plane, wherein a plurality of dehumidifying pores is provided through the metal thin film conductor layer, and the plurality of dehumidifying pores has an opening area of 0.001 to 0.04 square millimeters, may have any shape, and are filled and sealed with polyimide.” (EX1012, EX1013, 490-491.)

180. Nakanishi explains that “a conductor layer has poorer gas release properties than a dielectric layer, which is especially important during firing, curing, thermal treatment, and other processes performed during manufacture of the wiring substrate. Therefore, during the course of such treatments or processes,

a conductor layer having a large area is likely to hinder diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer, which reduces the bonding strength between the layers of the wiring substrate.” (EX1007, [0006].) Nakanishi teaches that “the conventional wisdom is to provide a conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) Nakanishi teaches including through holes in the conductor layer maintains the bonding strength of the conductor layer with the dielectric layer and prevents the generation of blisters caused by the conductor layer having poor gas release properties. A POSITA would have been motivated to combine Nakanishi’s technical features with the teachings of Koyama to generate an OLED device with better reliability and performance.

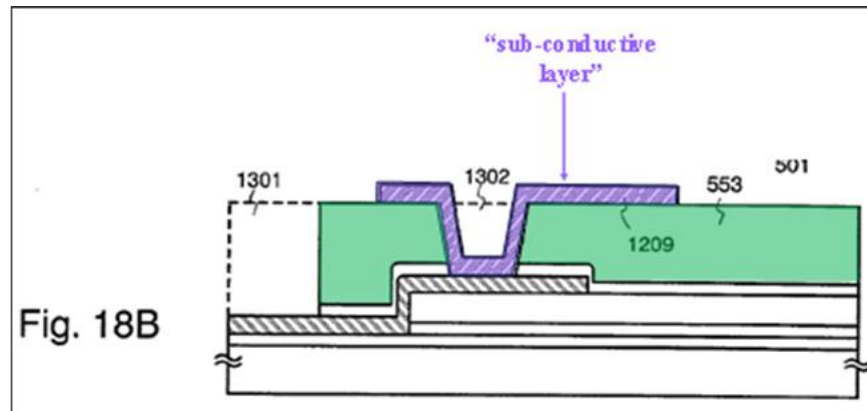
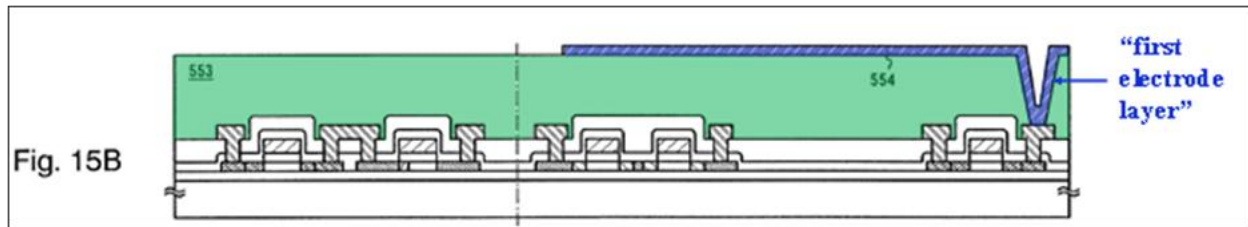
181. Further, there would have been a reasonable expectation of success because Nakanishi’s techniques were known (“conventional wisdom”) in the prior art and have been successfully demonstrated. A POSITA would have been motivated to use the techniques disclosed in Nakanishi to improve the similar device of Koyama in the same way. Thus, it would have been obvious to a POSITA to combine the teachings of Koyama and Nakanishi.

4. Claim 2: “The device of claim 1, wherein the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.”

182. As shown for element 1[d], Koyama teaches connection wiring 1209 (“sub-conductive layer”). As shown for element 1[a], Koyama teaches an anode / pixel electrode 49/554 (“first electrode layer”).

183. Koyama teaches “the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.” For example, Koyama discloses “[t]he connection wiring 1209 and the pixel electrode 554 in FIG. 15B are simultaneously formed. (FIG. 18B).” (EX1006, [0225].) A POSITA would have understood the connection wiring 1209 and pixel electrode 554 being simultaneously formed means they are defined over, and thus, on the same layer, as shown in Figures 15B and 18B.

184. Figure 15B (annotated below) shows that *pixel electrode 554* is formed on top of the *interlayer insulating film 553*. Figure 18B (annotated below) shows that *connection wiring 1209* is also formed on top of the *interlayer insulating film 553*. Because both the pixel electrode 554 and the connection wiring 1209 are on the interlayer insulating film 553, the connection wiring 1209 comprises the same layer as at least a part of the pixel electrode 554.



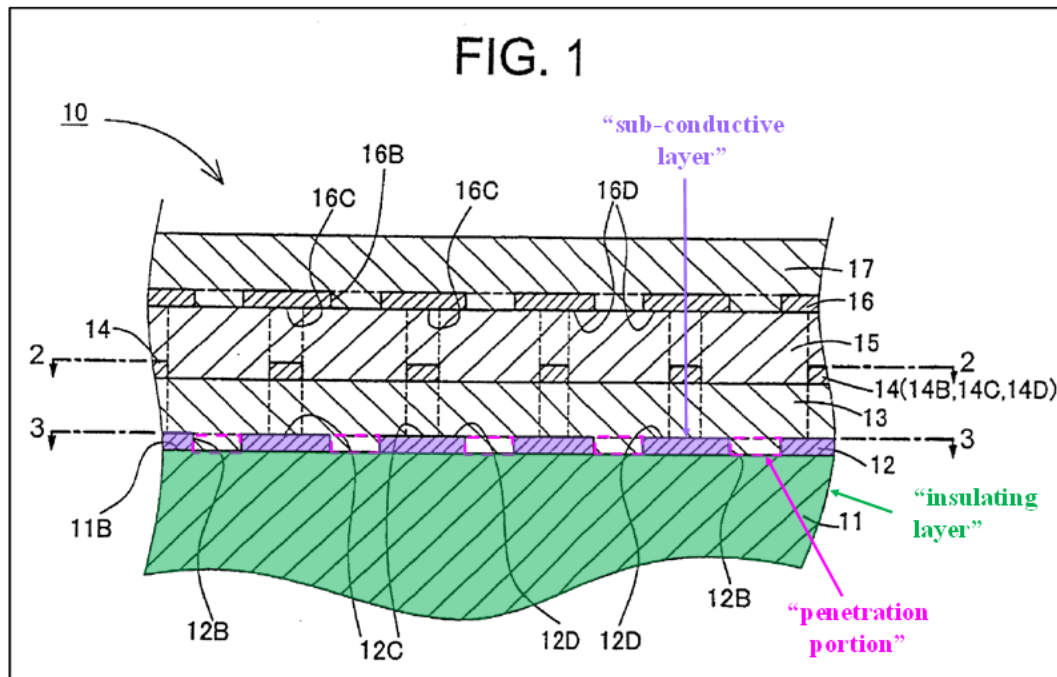
5. Claim 5: “The device of claim 1, wherein the penetration portion comprises a penetration hole.”

185. As shown for element 1[f], Nakanishi discloses through holes 12B, 12E, 12H, and 12L (“penetration portion”).

186. Nakanishi teaches “the penetration portion comprises a penetration hole.” For example, Nakanishi discloses “[t]he through holes 12B are formed to directly connect the core substrate 11 and the first dielectric layer 13 therethrough, thereby enhancing the strength of the wiring substrate 10.” (EX1007, [0049].) Nakanishi explains that “[o]n a front surface 11B of the *core substrate 11*, a *first conductor layer 12* (which is to be grounded, thereby forming a ground plane), a *first dielectric layer 13*, a plurality of signal wiring layers 14, a second dielectric layer 15, a second conductor layer 16 (which is to be supplied with a positive

supply potential, thereby forming a power plane), and a third dielectric layer 17 *are arranged in layers in this order.*” (EX1007, [0044] (emphases added).) A POSITA would have understood that the through hole allowing a direct connection from the first dielectric layer 13 to the core substrate 11 means the through hole is a penetration hole that penetrates through the conductor layer 12.

187. Figure 1 (annotated below) shows the through holes 12B comprise a penetration hole.



6. Claim 7

- a. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

188. As shown for element 1[a], Koyama teaches an anode / pixel electrode 49/554 (“first electrode layer”).

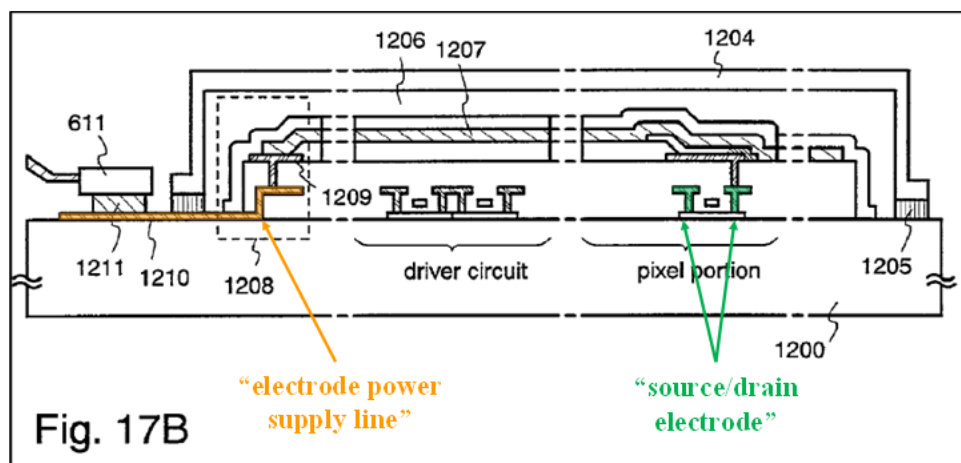
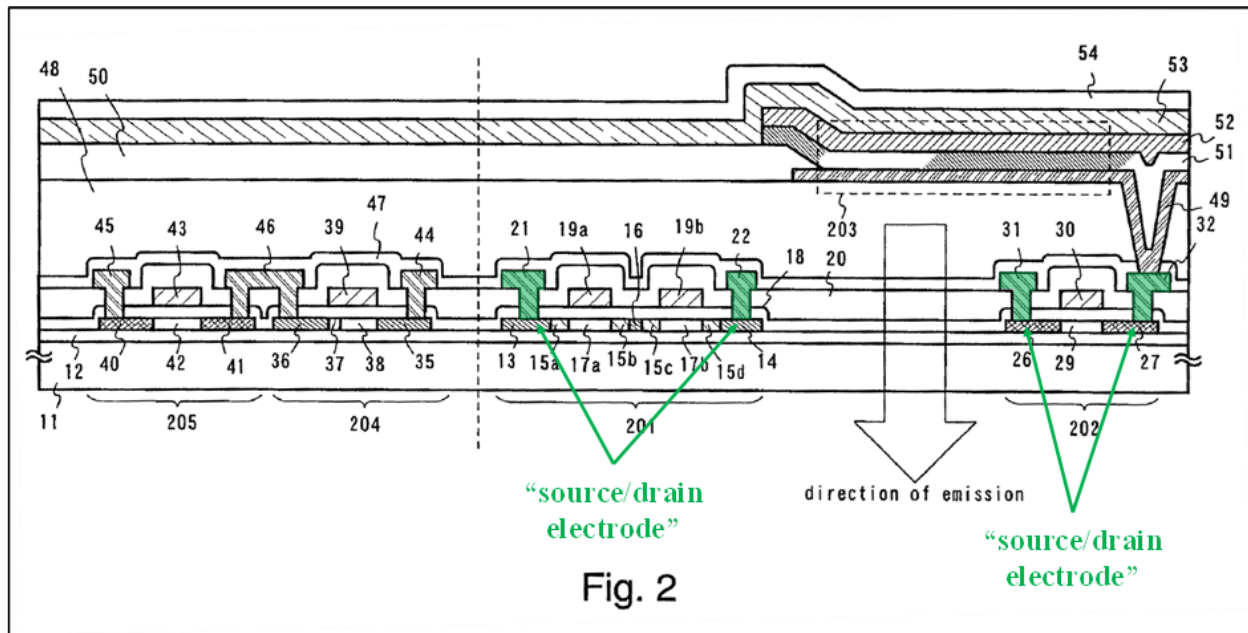
- b. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”**

192. As shown for element 1[b], Koyama teaches input/output wiring 1210 (“electrode power supply line”). As shown for element 7[b], Koyama teaches a layer (including the source / drain electrodes) of the switching TFT 201 and the current controlling TFT 202 (“thin film transistor layer”).

193. Koyama teaches “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.” For example, Koyama discloses “the input/output wiring 1210, and the source wiring and the drain wiring of FIG. 15A are formed simultaneously. (FIG. 18A).” (EX1006, [0224].) The input/output wiring 1210 is formed at the same time as the source / drain wiring, as shown in Figures 15A and 18A. Hence, the input/output wiring 1210 (“electrode power supply line”) comprises a layer that is the same layer as a source / drain electrode of the thin film transistor layer. A POSITA would have understood the input/output wiring 1210 and source / drain wiring of the TFT being formed simultaneously means they are on the same layer.

194. Referring to Figure 2, Koyama discloses “[t]he switching TFT 201 is formed to have: an active layer including a source region 13, a drain region 14, . . . a source wiring 21; and a drain wiring 22.” (EX1006, [0114].) Koyama also discloses “[t]he current controlling TFT 202 is formed to have a source region 26,

a drain region 27, . . . a source wiring 31, and a drain wiring 32.” (EX1006, [0119].) Figures 2 and 17B (annotated below) show that Koyama’s *source wiring 21 and drain wiring 22* (switching TFT 201) and *source wiring 31 and drain wiring 32* (current controlling TFT 202) are located on the same level as input/output wiring 1210, as shown in Figure 17B.



7. Claim 9

a. Preamble: “An electroluminescence display device, comprising:”

195. The preamble of claim 9 is similar to the preamble of claim 1, which Koyama teaches. The table below shows the similarities.

Preamble of Claim 1	Preamble of Claim 9
“An electroluminescence display device, comprising:”	“An electroluminescence display device, comprising:”

b. 9[a]: “a display area with pixels that have a first electrode layer and a second electrode layer and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

196. Element 9[a] is similar to element 1[a], which Koyama teaches. The table below shows the similarities.

Element 1[a]	Element 9[a]
“a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”	“a display area with pixels that have a first electrode layer and a second electrode layer and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

c. 9[b]: “an electrode power supply line to supply electrode power to the display area;”

197. Element 9[b] is similar to element 1[b], which Koyama teaches. The table below shows the similarities.

Element 1[b]	Element 9[b]
“an electrode power supply line to supply electrode power to the display area;”	“an electrode power supply line to supply electrode power to the display area;”

- d. **9[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”**

198. Element 9[c] is similar to element 1[c], which Koyama teaches. The table below shows the similarities.

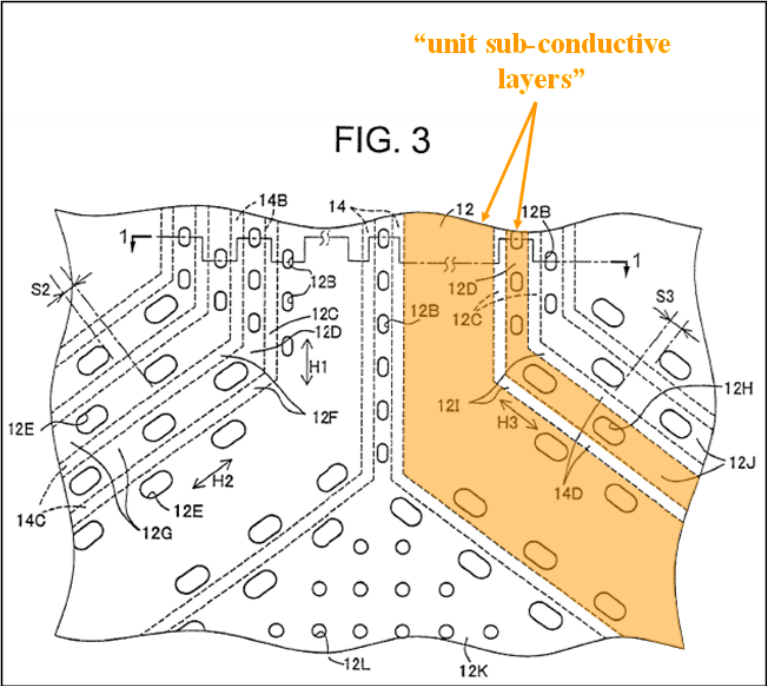
Element 1[c]	Element 9[c]
“an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”	“an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material;”

- e. **9[d]: “a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”**

199. Element 9[d] is similar to element 1[d], except element 9[d] additionally requires the sub-conductive layer “comprising a plurality of unit sub-conductive layers.” Koyama teaches element 1[d]. The table below shows the similarities.

Element 1[d]	Element 9[d]
“a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”	“a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”

200. Nakanishi teaches “a plurality of unit sub-conductive layers.” For example, as shown for element 1[f], Nakanishi teaches a conductor layer 12 (“sub-conductive layer”). Nakanishi discloses “the first conductor layer 12 is divided into (1) a wiring correspondence region, which corresponds to the signal wiring layers 14 as projected thereon along the thickness direction (i.e., perpendicular to the drawing sheet), and (2) *a remaining wiring noncorrespondence region.*” (EX1007, [0051] (emphasis added).) Nakanishi discloses the “conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) The “wiring noncorrespondence region [] is the remaining portion of the conductor layer after removal of the wiring correspondence regions.” (EX1007, [0019], [0053].) Figure 3 (annotated below) shows the wiring noncorrespondence regions comprising a plurality of *parallel-wiring-gap noncorrespondence portions 12D, 12G, and 12J.*



201. It would have been obvious to combine Koyama and Nakanishi. (See 1[f].)

f. 9[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

202. Element 9[e] is similar to element 1[e], which Koyama teaches. The table below shows the similarities.

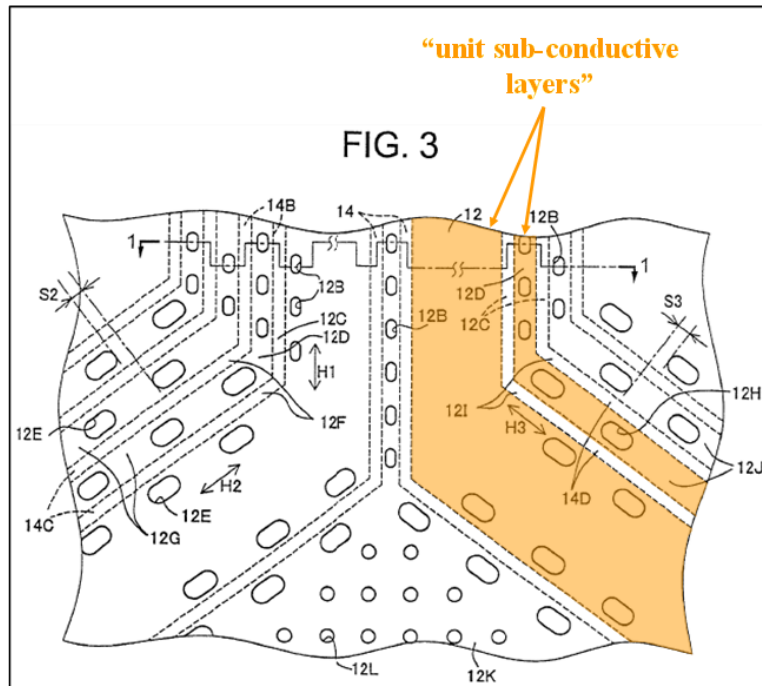
Element 1[e]	Element 9[e]
“wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer,”	“wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

g. 9[f]: “the unit sub-conductive layers on the insulating layer are separated from each other.”

203. As shown for element 9[f], Nakanishi teaches a conductive layer 12 comprising wiring correspondence regions (“unit sub-conductive layers”). As shown for element 1[f], Nakanishi teaches the conductive layer 12 on the core substrate 11 (“insulating layer”). A POSITA would have understood that the conductive layer 12 comprising wiring correspondence regions and being on the core substrate 11 would mean the wiring correspondence regions are on the core substrate 11.

204. Nakanishi teaches “the unit sub-conductive layers on the insulating layer are separated from each other.” For example, Nakanishi discloses “[t]he conductor layer includes (1) a plurality of wiring correspondence regions corresponding to the plurality of signal wiring layers as projected onto the conductor layer in the thickness direction of the conductor layer, and (2) a wiring noncorrespondence region, which is the remaining portion of the conductor layer after removal of the wiring correspondence regions.” (EX1007, [0019].) A POSITA would have understood that the wiring correspondence regions being separated from the wiring noncorrespondence regions means the wiring correspondence regions (“unit sub-conductive layers”) are separated from each other.

205. Figure 3 (annotated below) shows the *wiring correspondence regions* are separated from each other.



8. Claim 11

- a. **Preamble: “A method of manufacturing an electroluminescence display device, comprising:”**

206. As shown for the preamble of claim 1, Koyama teaches an organic EL display panel 100 (“electroluminescent display”).

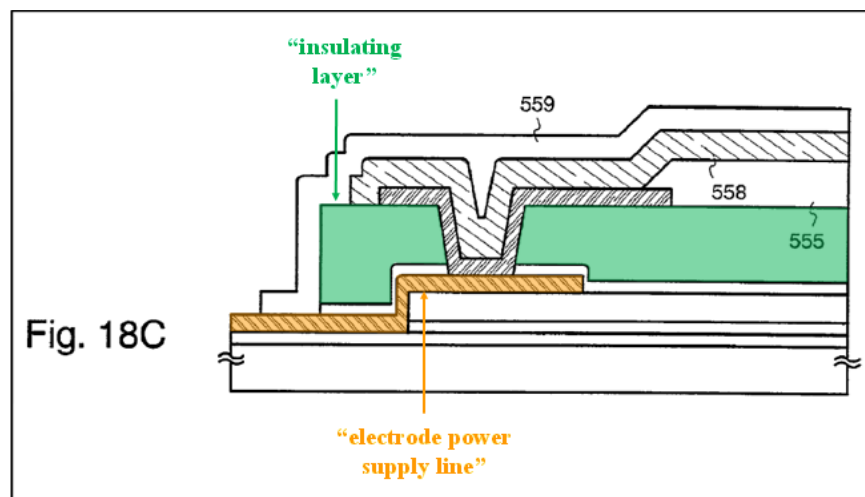
207. Koyama teaches “[a] method of manufacturing an electroluminescence display device.” For example, Koyama discloses “[t]he present invention relates to a self-luminous device (or an EL display device) manufactured by forming a light emitting element (such as an EL (Electro Luminescence) element) on a substrate.” (EX1006, [0002].) Koyama describes

the manufacturing process including steps for forming the layers of the EL display device, including Figures 15A-15C and Figures 18A-18C.

b. 11[a]: “forming an insulating layer including an organic material on an electrode power supply line;”

208. As shown for element 1[b], Koyama teaches input/output wiring 1210 (“electrode power supply line”). As shown for element 1[c], Koyama teaches an interlayer insulating film 553 (“insulating layer”) including an organic material on input/output wiring 1210. Thus, Koyama teaches “an insulating layer including an organic material on an electrode power supply line.”

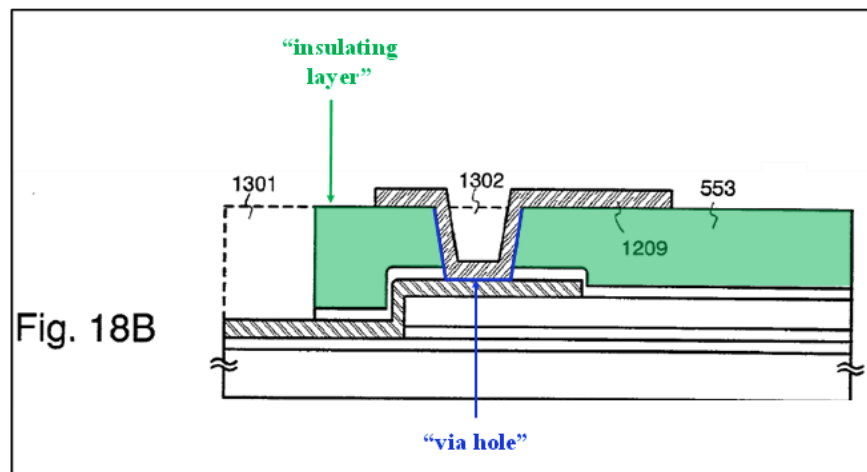
209. As shown for the preamble of claim 11, Koyama teaches the manufacturing process including steps for forming the layers of the organic EL display panel. Figure 18C (annotated below) shows forming *interlayer insulating film 553* on the *input/output wiring 1210*.



c. 11[b]: “forming a via hole on the insulating layer;”

210. As shown for element 1[c], Koyama teaches interlayer insulating film 553 (“insulating layer”) including a via hole. Thus, Koyama teaches “a via hole on the insulating layer.”

211. As shown for the preamble of claim 11, Koyama teaches the manufacturing process including steps for forming the layers of the organic EL display panel. Figure 18B (annotated below) shows forming a *via hole* on the *interlayer insulating film 553*.

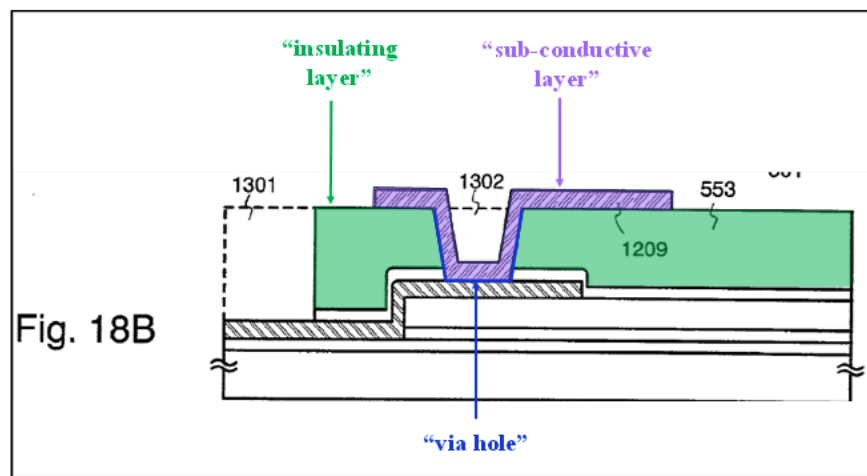


d. 11[c]: “forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”

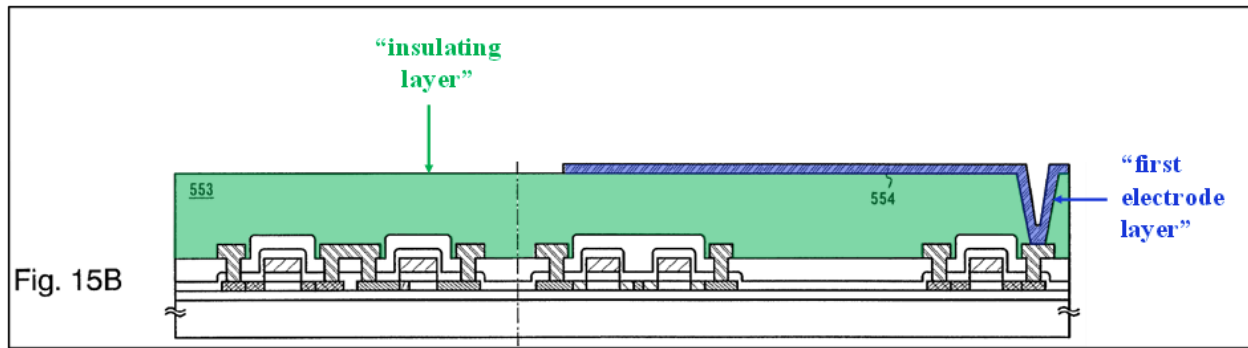
212. As shown for element 1[d], Koyama teaches connection wiring 1209 (“sub-conductive layer”). As shown for element 1[a], Koyama teaches an anode / pixel electrode 49/554 (“first electrode layer”). As shown for element 1[c], Koyama teaches interlayer insulating film 553 (“insulating layer”) including a via

hole. Thus, Koyama teaches “a sub-conductive layer . . . on the insulating layer including the via hole.”

213. As shown for the preamble of claim 11, Koyama teaches the manufacturing process including steps for forming the layers of the organic EL display panel. Figure 18B (annotated below) shows forming *connection wiring 1209* on the *interlayer insulating film 553* including the *via hole*.



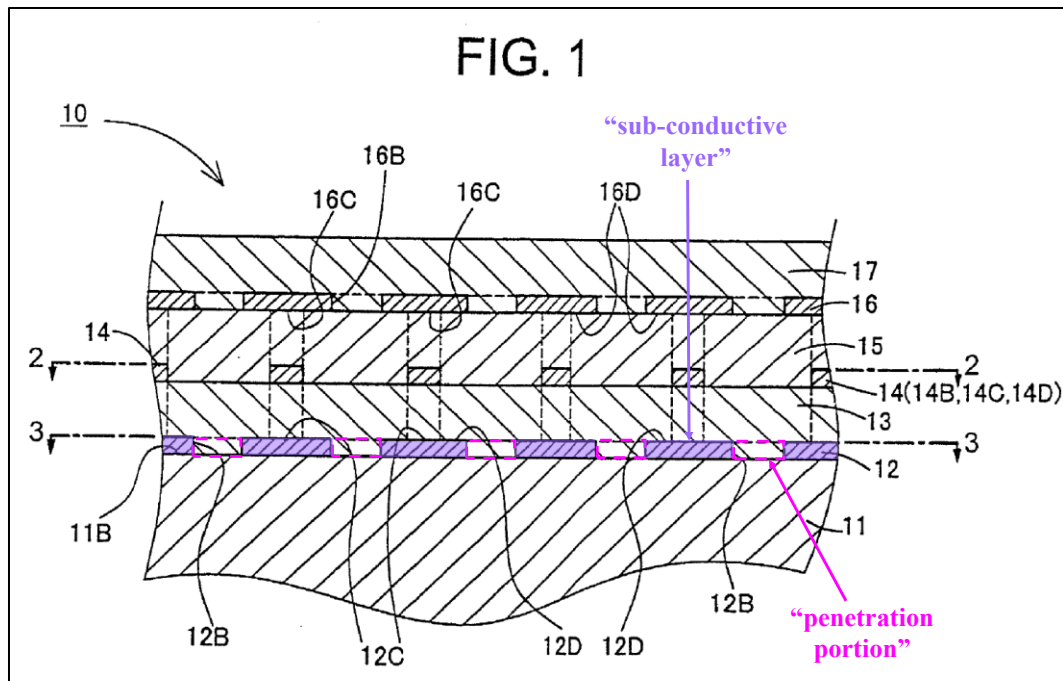
214. Koyama also teaches “a first electrode layer on the insulating layer.” For example, Koyama discloses a “contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.” (EX1006, [0202].) Figure 15B (annotated below) shows forming the *pixel electrode 554* on the *interlayer insulating film 553*.



e. **11[d]: “forming a penetration portion on the sub-conductive layer;”**

215. As shown for element 1[f], Nakanishi teaches a conductor layer 12 (“sub-conductive layer”) including through holes 12B, 12E, 12H, and 12L (“penetration portion[s]”). Thus, Nakanishi teaches “a penetration portion on the sub-conductive layer.”

216. Nakanishi teaches “forming a penetration portion on the sub-conductive layer.” For example, Nakanishi teaches “[t]he through holes are also intended to allow release of gas therethrough,” and then discusses “fabricating the wiring substrate 10” including fabricating the through holes. (EX1007, [0049].) Figure 11 (annotated below) shows forming *through holes 12B, 12E, 12H, and 12L* on the *conductor layer 12*. Thus, Nakanishi teaches element 11[d].

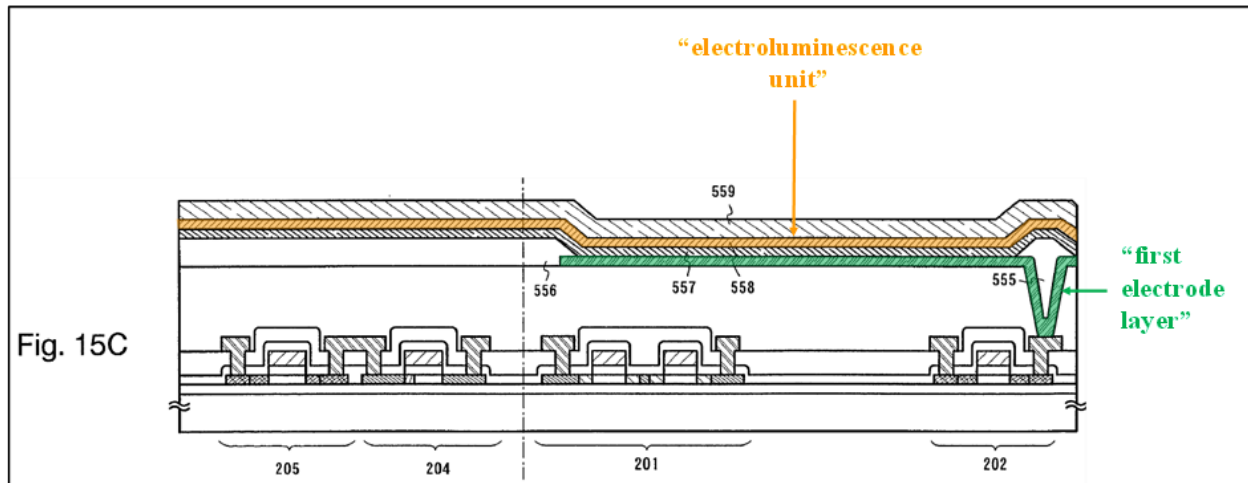


f. 11[e]: “forming an organic EL unit on the first electrode layer; and”

217. As shown for element 1[a], Koyama teaches a light emitting layer 558 on the pixel electrode 554 (“first electrode layer”). Thus, Koyama teaches “an organic EL unit on the first electrode layer.”

218. As shown for the preamble of claim 11, Koyama teaches the manufacturing process including steps for forming the layers of the organic EL display panel. Koyama discloses “[t]he surface of the pixel electrode 554 is next subjected to ozone treatment. The ozone treatment in this embodiment is provided through UV light irradiation while the pixel electrode is exposed to oxygen gas. After that, a hole injection layer 557 and a light emitting layer 558 are formed by

spin coating.” (EX1006, [0204].) Figure 15C (annotated below) shows forming *light emitting layer 558* on the *pixel electrode 554*.



g. 11[f]: “forming a second electrode layer on the organic EL unit.”

219. As shown for element 1[a], Koyama teaches forming a cathode 229/559 (“second electrode layer”) on the light emitting layer 558 (“organic EL unit”). Thus, Koyama teaches “a second electrode layer on the organic EL unit.”

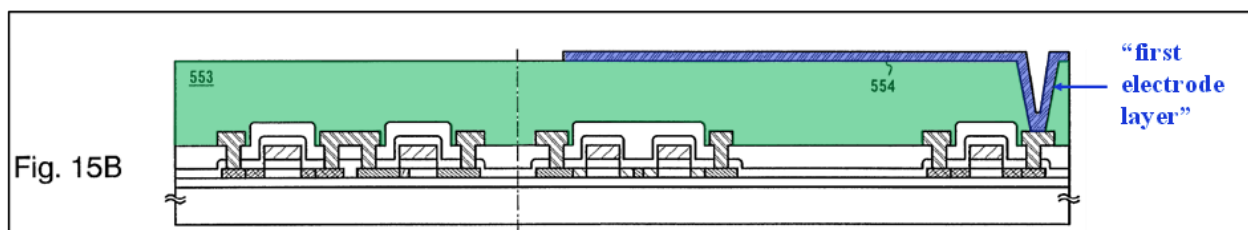
220. As shown for the preamble of claim 11, Koyama teaches the manufacturing process including steps for forming the layers of the organic EL display panel. Koyama discloses “[a]fter that, a hole injection layer 557 and a light emitting layer 558 are formed by spin coating.” (EX1006, [0204].) Koyama then discloses “[n]ext, a cathode 559 is formed to a thickness of 400 nm from a conductive film having low work function.” (EX1006, [0206].)

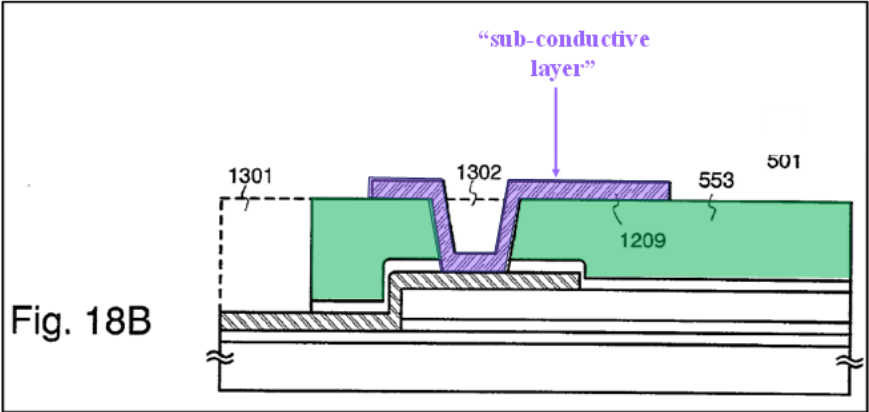
9. Claim 12: “The method of claim 11, wherein forming of the sub-conductive layer is simultaneous with forming the first electrode layer.”

221. As shown for element 1[d], Koyama teaches connection wiring 1209 (“sub-conductive layer”). As shown for element 1[a], Koyama teaches a light emitting layer 558 on the pixel electrode 554 (“first electrode layer”).

222. Koyama teaches “forming of the sub-conductive layer is simultaneous with forming the first electrode layer.” For example, Koyama discloses “[t]he connection wiring 1209 and the pixel electrode 554 in FIG. 15B are simultaneously formed. (FIG. 18B).” (EX1006, [0225].)

223. Figure 15B (annotated below) shows forming the *pixel electrode 554* on top of the *interlayer insulating film 553*. Figure 18B (annotated below) shows forming the *connection wiring 1209* on top of the *interlayer insulating film 553*. The display devices are fabricated by sequentially depositing layers, and as a result, the connection wiring 1209 and pixel electrode 554 both formed directly on the interlayer insulating film 553 means forming the connection wiring 1209 is simultaneous with forming the pixel electrode 554.





10. Claim 15

- a. Preamble: “A method of manufacturing an electroluminescence display device, comprising:”

224. The preamble of claim 15 is similar to the preamble of claim 11, which Koyama teaches. The table below shows the similarities.

Preamble of Claim 11	Preamble of Claim 15
“A method of manufacturing an electroluminescence display device, comprising:”	“A method of manufacturing an electroluminescence display device, comprising:”

- b. 15[a]: “forming an insulating layer including an organic material on an electrode power supply line;”

225. Element 15[a] is similar to element 11[a], which Koyama teaches. The table below shows the similarities.

Element 11[a]	Element 15[a]
“forming an insulating layer including an organic material on an electrode power supply line;”	“forming an insulating layer including an organic material on an electrode power supply line;”

c. 15[b]: “forming a via hole on the insulating layer;”

226. Element 15[b] is similar to element 11[b], which Koyama teaches.

The table below shows the similarities.

Element 11[b]	Element 15[b]
“forming a via hole on the insulating layer;”	“forming a via hole on the insulating layer;”

d. 15[c]: “forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”

227. Element 15[c] is similar to element 11[c], except that element 15[c] additionally requires the “sub-conductive layer comprising a plurality of unit sub-conductive layers.” Koyama teaches element 11[c]. Additionally, Nakanishi teaches the “sub-conductive layer comprising a plurality of unit sub-conductive layers.” The table below shows the similarities.

Element 11[c]	Element 15[c]
“forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”	“forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”

e. 15[d]: “forming an organic EL unit on the first electrode layer; and”

228. Element 15[d] is similar to element 11[e], which Koyama teaches.

The table below shows the similarities.

Element 11[e]	Element 15[d]
“forming an organic EL unit on the first electrode layer; and”	“forming an organic EL unit on the first electrode layer; and

f. 15[e]: “forming a second electrode layer on the organic EL unit.”

229. Element 15[e] is similar to element 11[f], which Koyama teaches.

The table below shows the similarities.

Element 11[f]	Element 15[e]
“forming a second electrode layer on the organic EL unit.”	“forming a second electrode layer on the organic EL unit.”

D. Claims 1-5, 7, And 9-15 Are Obvious Over Matsueda And Nakanishi

1. Claim 1

a. Preamble: “An electroluminescence display device, comprising:”

230. As shown above, Matsueda teaches the preamble of claim 1.

b. 1[a]: “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

231. As shown above, Matsueda teaches element 1[a].

- c. **1[b]: “an electrode power supply line to supply electrode power to the display area;”**

232. As shown above, Matsueda teaches element 1[b].

- d. **1[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”**

233. As shown above, Matsueda teaches element 1[c].

- e. **1[d]: “a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”**

234. As shown above, Matsueda teaches element 1[d].

- f. **1[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”**

235. As shown above, Matsueda teaches element 1[e].

- g. **1[f]: “the sub-conductive layer on the insulating layer includes a penetration portion.”**

236. As shown above, Matsueda teaches element 1[f].

237. If, for some reason, Matsueda does not teach a “penetration portion,”

Nakanishi teaches a “penetration portion.” (*See* element 1[f].)

238. It would have been obvious to a POSITA at the time of the '708 patent to combine Matsueda and Nakanishi. Matsueda and Nakanishi both relate to conductor layers on insulating layers containing an organic material. Matsueda teaches a device including auxiliary cathode wiring 16 on a planarizing film 20 and

bank layer 19 containing an organic resin. (EX1004, [0053], [0067], [0069], Figs. 8, 9.) Nakanishi similarly discloses a device including a conductor layer 12 on a core substrate 11 that also contains an organic resin. (EX1007, [0043], [0049], Fig. 1.) Matsueda and Nakanishi both disclose conductor layers on insulating layers containing an organic material. They both disclose transmitting signals via a conductor layer on top of an organic insulating layer. Matsueda and Nakanishi also both disclose using heat during the manufacturing process. In Matsueda, “the bank layer . . . is made of the organic material, has low resistance to heat and chemicals, [and thus,] it is difficult to form the auxiliary cathode wiring 16 on the bank layer, but it is easy to form metal wiring such as the auxiliary cathode wiring 16 on the substrate 15 provided with the FET or the like.” (EX1004, [0056].) In Nakanishi, the “conductor layer . . . hinder[s] diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer.” (EX1007, [0006].) Thus, Matsueda and Nakanishi are from the same field of endeavor and reasonably pertinent to the same technical problems of improving the manufacturing and quality of devices that have conductor layers on organic insulating layers, which are subjected to heat during the manufacturing process.

239. Nakanishi explains that it is “conventional wisdom [to] . . . provid[e] a conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) Nakanishi’s technical features of using through holes in the conductive layer (to allow the diffusion of gas released from the underlying dielectric layer) may be combined with the teachings of Matsueda to generate an improved OLED device with better reliability and performance.

240. Further, there would have been a reasonable expectation of success because Nakanishi’s techniques were known (“conventional wisdom”) in the prior art and have been successfully demonstrated. Matsueda and Nakanishi both relate to conductive layers on organic insulating layers and devices that are subject to heat treatment, thereby susceptible to issues of impaired bonding strength and generation of blisters. As a result, a POSITA would have been motivated to use the technique disclosed in Nakanishi to improve the similar devices. The prior art had already known and demonstrated that such techniques were success. Thus, it would have been obvious to a POSITA to combine the teachings of Matsueda and Nakanishi.

2. Claim 2: “The device of claim 1, wherein the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.”

241. As shown above, Matsueda teaches claim 2.

3. Claim 3

a. 3[a]: “The device of claim 1, wherein the sub-conductive layer comprises two penetration portions, and”

242. As shown above, Matsueda teaches element 3[a].

243. If, for some reason, Matsueda does not teach “two penetration portions,” Nakanishi teaches “two penetration portions.” (*See* claim 3.)

244. It would have been obvious to combine Matsueda and Nakanishi.
(*See* 1[f].)

b. 3[b]: “a distance between the two penetration portions is less than or equal to a maximum distance between both ends of the first electrode layer.”

245. As shown above, Matsueda teaches element 3[b].

4. Claim 4: “The device of claim 3, wherein at least one of the two penetration portions is disposed on at least a part of an outer portion of the via hole.”

246. As shown above, Matsueda teaches claim 4.

247. If, for some reason, Matsueda does not teach “two penetration portions,” Nakanishi teaches “two penetration portions.” (*See* claim 4.)

248. It would have been obvious to combine Matsueda and Nakanishi.

(See 1[f].)

5. Claim 5: “The device of claim 1, wherein the penetration portion comprises a penetration hole.”

249. As shown above, Matsueda teaches claim 5.

250. If, for some reason, Matsueda does not teach a “penetration portion,” Nakanishi teaches a “penetration portion.” (See claim 5.)

251. It would have been obvious to combine Matsueda and Nakanishi.

(See 1[f].)

6. Claim 7

a. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

252. As shown above, Matsueda teaches element 7[a].

253. If, for some reason, Matsueda does not teach a “penetration portion,” Nakanishi teaches a “penetration portion.” (See claim 7[a].)

254. It would have been obvious to combine Matsueda and Nakanishi.

(See 1[f].)

b. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”

255. As shown above, Matsueda teaches element 7[b].

256. If, for some reason, Matsueda does not teach a “penetration portion,” Nakanishi teaches a “penetration portion.” (*See* claim 7[b].)

257. It would have been obvious to combine Matsueda and Nakanishi. (*See* 1[f].)

7. Claim 9

a. Preamble: “An electroluminescence display device, comprising:”

258. As shown above, Matsueda teaches the preamble of claim 9.

b. 9[a]: “a display area with pixels that have a first electrode layer and a second electrode layer and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

259. As shown above, Matsueda teaches element 9[a].

c. 9[b]: “an electrode power supply line to supply electrode power to the display area;”

260. As shown above, Matsueda teaches element 9[b].

d. 9[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”

261. As shown above, Matsueda teaches element 9[c].

e. 9[d]: “a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”

262. As shown above, Matsueda teaches element 9[d].

- f. **9[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”**

263. As shown above, Matsueda teaches element 9[e].

- g. **9[f]: “the unit sub-conductive layers on the insulating layer are separated from each other.”**

264. As shown above, Matsueda teaches element 9[f].

- 8. **Claim 10: “The device of claim 9, wherein a distance between a point of the unit sub-conductive layer and a neighboring outer point is less than or equal to a maximum distance between a point of the first electrode layer and a neighboring outer point.”**

265. As shown above, Matsueda teaches claim 10.

9. Claim 11

- a. **Preamble: “A method of manufacturing an electroluminescence display device, comprising:”**

266. As shown above, Matsueda teaches the preamble of claim 11.

- b. **11[a]: “forming an insulating layer including an organic material on an electrode power supply line;”**

267. As shown above, Matsueda teaches element 11[a].

- c. **11[b]: “forming a via hole on the insulating layer;”**

268. As shown above, Matsueda teaches element 11[b].

- d. **11[c]: “forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”**

269. As shown above, Matsueda teaches element 11[c].

e. 11[d]: “forming a penetration portion on the sub-conductive layer;”

270. As shown above, Matsueda teaches element 11[d].

271. If, for some reason, Matsueda does not teach a “penetration portion,” Nakanishi teaches a “penetration portion.” (See 11[d].)

272. It would have been obvious to combine Matsueda and Nakanishi.
(See 1[f].)

f. 11[e]: “forming an organic EL unit on the first electrode layer; and”

273. As shown above, Matsueda teaches element 11[e].

g. 11[f]: “forming a second electrode layer on the organic EL unit.”

274. As shown above, Matsueda teaches element 11[f].

10. Claim 12: “The method of claim 11, wherein forming of the sub-conductive layer is simultaneous with forming the first electrode layer.”

275. As shown above, Matsueda teaches claim 12.

11. Claim 13: “The method of claim 11, wherein two or more via holes are formed when the via hole is formed, and the penetration portion is formed between the via holes when the penetration portion is formed.”

276. As shown above, Matsueda teaches claim 13.

277. If, for some reason, Matsueda does not teach a “penetration portion,” Nakanishi teaches a “penetration portion.” (*See* claim 13.)

278. It would have been obvious to combine Matsueda and Nakanishi.
(*See* 1[f].)

12. Claim 14

- a. **14[a]: “The method of claim 11, wherein forming the penetration portion comprises forming two or more penetration portions, and”**

279. As shown above, Matsueda teaches element 14[a].

280. If, for some reason, Matsueda does not teach “two or more penetration portions,” Nakanishi teaches “two or more penetration portions.” (*See* 14[a].)

281. It would have been obvious to combine Matsueda and Nakanishi.
(*See* 1[f].)

- b. **14[b]: “a distance between the penetration portions is less than or equal to a maximum distance between two ends of the first electrode layer.”**

282. As shown above, Matsueda teaches element 14[b].

13. Claim 15

- a. **Preamble: “A method of manufacturing an electroluminescence display device, comprising:”**

283. As shown above, Matsueda teaches the preamble of claim 15.

- b. 15[a]: “forming an insulating layer including an organic material on an electrode power supply line;”**

284. As shown above, Matsueda teaches element 15[a].

- c. 15[b]: “forming a via hole on the insulating layer;”**

285. As shown above, Matsueda teaches element 15[b].

- d. 15[c]: “forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”**

286. As shown above, Matsueda teaches element 15[c].

- e. 15[d]: “forming an organic EL unit on the first electrode layer; and”**

287. As shown above, Matsueda teaches element 15[d].

- f. 15[e]: “forming a second electrode layer on the organic EL unit.”**

288. As shown above, Matsueda teaches element 15[e].

* * *

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Dated: 9/19/2025



Jerzy Kanicki

Jerzy Kanicki, D.Sc.

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Education

Universite Libre de Bruxelles, Bruxelles, Belgium

(Free University of Brussels, Brussels, Belgium)

- 1/20/1982 **Docteur en Sciences** (*Doctor es Science, D.Sc.*), D.Sc. Thesis: “*Optical Electrical and Photo-electronic Properties of trans-Poly-acetylene.*” Graduated with “Highest Distinction” (“La Plus Grande Distinction”)
- 7/20/1978 **Master of Science** (*M.Sc.*), section Chemical Sciences, M.Sc. Thesis: “*Photo-electronic Properties of the SnO₂-(poly-2-Vinylpyridine-I₂) structures.*” Graduated with “High Distinction” (“Grand Distinction”)
- 7/20/1976 **Bachelor of Science** (*B.Sc.*), section Chemical Sciences

Employment History

- 9/11/1994 - present **University of Michigan, College of Engineering, Ann Arbor, MI**
Position: Professor of Electrical Engineering and Computer Sciences
Research Interest: Amorphous and polycrystalline semiconductors (inorganic and organic) thin-film devices and circuits; Flat panel displays and detectors; X-ray imagers; Organic opto-electronic devices; Flexible substrates; Inorganic and organic solar cell devices and manufacturing technologies.
- 2000 - 2011 **University of Michigan, College of Engineering, Ann Arbor, MI**
Position: Professor of Macromolecular Science and Engineering
Research Interest: Organic materials, devices, and electronics
- 6/1/2024-
6/31/2025 **Massachusetts Institute of Technology (MIT), Cambridge, MA**
Position: Visiting Scholar within Research Laboratory of Electronics (RLE) - sabbatical
Research Interest: Pixel and driving circuits for micro-LEDs and micro-LEDs fabrication and integration with the backplane electronics
Host: Prof. Jeehwan Kim
- 1/1/2018- **Massachusetts Institute of Technology (MIT), Cambridge, MA**

- 8/31/2018 **Position:** Visiting Scholar within Microsystems Technology Laboratories (MTL)
- sabbatical
Research Interest: Hydrogenated diamond devices and circuits, and Perovskites materials based opto-electronic devices
Host: Prof. Jesus del Alamo
- 7/11/2009-
6/30/2010 **University of California San Diego (UCSD), San Diego, CA**
Position: Visiting Scholar with California Institute for Telecommunications and Information Technology - sabbatical
Research Interest: Organic thin – film transistor chemical sensors, amorphous InGaZnO thin – film transistors, image sensors and Cu(In,Ga)Se solar cells
Host: Prof. Andrew C. Kummel, Department of Chemistry and Biochemistry
- 7/31/2003-
8/11/2002 **University of California Sanat Barbara (UCSB), Santa Barbara, CA**
Position: Visiting Professor with Center for Polymers and Organic Solids
Research Interest: Organic polymer thin – film transistors, organic light – emitting devices and electrically injected lasers
Host: Prof. Alan J. Heeger, Department of Physics
- 8/30/1994-
1/31/1983 **IBM Thomas J. Watson Research Center, Yorktown Heights, NY**
Position: Research Staff Member
Duties: Member of the team that developed hydrogenated amorphous silicon (a-Si:H) thin film transistors (TFTs) and active-matrix arrays technology for active-matrix (AM) liquid crystal displays (LCDs). This development resulted in introduction by IBM of the first color laptop computer (CL57-SX) on March 24, 1992
- 1982 **Belgium Army, Belgium**
Position: Sergeant Major in Belgium Army
Duties: Responsible for a unit of about 30 soldiers, and training of new soldiers

Teaching: Undergraduate and Graduate Courses

EECS 215 – Introduction to Circuits
EECS 314 – Electrical Circuits, Systems and Applications
EECS 421 – Properties of Transition
EECS 423 – Solid State Device Laboratory
EECS 512 – Amorphous and Microcrystalline Thin Film Devices
EECS 513 – Flat Panel Displays
EECS 498 & 598 – Organic and Molecular Electronics
EECS 523 – Digital Integrated Circuit Technology
EECS 528 – Principles of Microelectronics Process Technology

Consulting & Expert Witness

Past consulting has been in fields of study generally related to:

- ❖ Hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFT) technology

- ❖ Active-matrix liquid-crystal displays (AM-LCDs) technology
- ❖ A-Si:H TFT processing, properties and electrical characterization methods
- ❖ Thin-film plasma-enhanced chemical vapor deposition (PECVD) technology for integrated circuits and other technologies
- ❖ AM-LCD and AM-OLEDs pixel electrodes circuits and related driving schemes
- ❖ Electrical instability of the a-Si:H TFTs
- ❖ Device physics of the a-Si:H and a-InGaZnO TFTs
- ❖ Electrostatic discharge protection (ESD) circuits for AM-LCDs
- ❖ Organic light emitting devices for active-matrix organic light emitting displays (AM-OLEDs)
- ❖ Amorphous InGaZnO thin-film transitions for next generation flat panel displays
- ❖ Integrated circuits technology including processing technology
- ❖ Crystalline silicon solar cells and associated manufacturing technologies

Has expertise in the following topics:

- ❖ Patent infringements
- ❖ Expert witness
- ❖ Expert testimony
- ❖ Litigation support consultant

Able to provide patents background research and testimonials in support of the attorneys and their clients during patents infringement litigations. Past projects have been with several multinational organizations, both large and medium size.

Honors and Awards

2013	Certificate of Commendation for Outstanding Service by Society for Information Display for his organization of the first I-Zone at the 2012 SID International Symposium
2011	The IEEE Electron Devices Society Certificate in Recognition and Appreciation of valued services and contributions as IEEE Transactions on Electron Device Editor, Molecular and Organic Devices 2004-2011
2008, 2010, 2011, 2012, and 2014	Certificate of Appreciation Award for contributing to the success of the annual “Symposium on Vehicular Displays” by Society for Information Display
2008	The Minister of Education, Science and Technology of Republic of Korea, Excellence Award in Fundamental and Original Technology section of the 8 th International Meeting on Information Display (IMID) (2 nd place) for “Photofield-Effect in Amorphous InGaZnO TFTs” paper
2001	RSNA Certificate of Merit in recognition of the excellence of your education exhibit presented at the 87 th Scientific Assembly and Annual Meeting of the Radiological Society of North America (RSNA)
1999	Recognized by Materials Research Society (MRS) for serving as a tutorial instructor during Spring Meeting

1992 & 1996	Recognized by MRS for contributions in serving the society as symposia organizer
1992	IBM Appreciation and Recognition Award for a first plateau invention achievement
1990	IBM Invention Achievement Award for a first patent application
1989, 1990 & 1993	IBM External Honors for technical leadership
1982	Stas Prize for outstanding D.Sc. thesis research work

Professional Service and Associations

Officer:

- ❖ Director for Metropolitan Detroit, Society for Information Display (SID): 2005 - present
- ❖ Board of Directors, SID, 2005-present

Editor:

- ❖ IEEE Transaction on Electron Devices: 1989, 2005 – 2011
- ❖ Materials Research Society Proceedings: 1993, 1995 - 1997
- ❖ Journal of Non - Crystalline Solids: 1995
- ❖ Artech House, Inc., “*Amorphous & Microcrystalline Semiconductor Devices*,” book- two volumes, 1991 and 1992
- ❖ Journal of Korean Display Society, foreign member

Conference Organizer:

- ❖ Display Week I-Zone- 2012, 2013, and 2014 during SID International Symposium and Exhibit
- ❖ Symposium on “*Flat Panel Displays Materials II*,” 1996 Materials Research Society Spring Meeting, April 8-12, 1996, San Francisco, CA
- ❖ Symposium on “*Amorphous and Crystalline Insulating Thin Films III*,” 1995 International Conference on Solid State Devices and Materials, August 21-24, 1995, Osaka, Japan
- ❖ Symposium on “*Amorphous Insulating Thin Films II*,” 1994 European Materials Research Society Spring Conference, May 24-27, 1994, Strasbourg, France
- ❖ Symposium on “*Amorphous Insulating Thin Films*,” 1992 Materials Research Society Fall Meeting, December 1-4, 1992, Boston, MA
- ❖ International Topical Conference on “*Hydrogenated Amorphous Silicon Devices and Technology*,” November 21-23, 1988, Yorktown Heights, NY

Technical Program Committee:

- ❖ IEEE – The Electron Devices Society; IEDM and DRC – program committee member and chair
- ❖ IEEE “*Standard Test Methods for the Characterization of Organic Transistors*”- standard development committee member
- ❖ IEEE Standard development for “*Organic Electronics*” - technical committee member
- ❖ Society for Information Display; SID International Symposium – program- Committee member
- ❖ Society for Information Display; SID Vehicle Displays and Interfaces- program committee chair and member

- ❖ Society for Information Display; International Meeting on Information Display (IMID)- program committee member
- ❖ Society for Information Display; Display Week I-Zone- program committee chair and member
- ❖ Materials Research Society; MRS Meetings – program committee member
- ❖ The Japan Society of Applied Physics; AM-FPDs Workshops – program committee member

Professional Journal Referee:

- ❖ IEEE Trans. Elec. Dev., IEEE Elec. Dev. Letters, Appl. Phys. Letters, J. Appl. Phys., Thin Solid Films, Solid-State Electronics, and many others

Panelist and proposal review:

- ❖ National Science Foundation, Department of Energy (DoE) and Department of Defense (DoD)
- ❖ Panelist at various national and international meetings

Professional Society Member:

- ❖ Institute of Electrical and Electronics Engineers (IEEE)-elected to grade of Senior Member since 2000
- ❖ Society for Information Display (SID)- member

Service to University of Michigan, College of Engineering and EECS Department

- ❖ College of Engineering (CoE) Freshmen advisor
- ❖ EECS Casebook committee – chair
- ❖ College representative for EECS department
- ❖ ECE faculty search committee - member
- ❖ Senate Assembly and SACU - alternate
- ❖ Electrical engineering graduate program committee - member
- ❖ ECE student projects laboratory - coordinator
- ❖ Industrial Programs Committee - member
- ❖ CoE Faculty committee on discipline - member
- ❖ CoE Library Advisory Committee - member

Research Record, Headlights

1983 - present Details can be provided upon request

Publications

1983 - present Over 400 publications, 5 book chapters, and 3 books

Google Scholar, ResearchGate (R^G) Citations and Ranking of Best Scientists in the World – Electronics and Electrical Engineering

<https://scholar.google.com/citations?user=gGSiW3YAAAAJ&hl=en>
<https://research.com/u/jerzy-kanicki>

- ❖ Citations: 12,082
- ❖ Reads: 75,587

- ❖ h-index: 60
- ❖ i10-index: 204
- ❖ R^G score: 42.30
- ❖ D-index 51
- ❖ Ranked #886 in United States and #2316 in the world

Presentations

1985 - present Over 100 invited and 250 contributed presentations at the national and international meetings.

Areas of Expertise

- ❖ Hydrogenated amorphous and polycrystalline silicon and alloys, devices, circuits and technology
- ❖ Flat panel displays (transmissive, reflective, emissive, and electrochromic) technology including systems and manufacturing
- ❖ Integrated circuits processing and technology
- ❖ Thin film processing and technology for different applications including displays, imagers, solar cells and integrated circuits
- ❖ Organic semiconductors, devices and circuits physics, opto-electronic properties and technology
- ❖ Metal oxide semiconductors, devices, and circuits physics, opto-electronic properties and technology
- ❖ Organic and inorganic solar cells fundamentals and fabrication technology
- ❖ Detectors physics, electronics and technology
- ❖ X-ray imagers physics, technology and systems
- ❖ Chemical sensors physics
- ❖ DNA-based membranes and flexible substrates

Interests and Others

- ❖ Enjoy working with others in team-oriented projects
- ❖ Love spending time with his family
- ❖ Love sports and outdoors
- ❖ Married, three grown children
- ❖ Fluent in French and Polish; and limited knowledge of Italian and Russian
- ❖ Citizen of the World (Familiar with different cultures)

References

- ❖ Can be provided upon request