

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

BOE TECHNOLOGY GROUP CO., LTD.
Petitioner,

v.

SAMSUNG DISPLAY CO., LTD.
Patent Owner.

Patent No. 7,279,708

Inter Partes Review No. IPR2025-01557

**PETITION FOR *INTER PARTES* REVIEW
UNDER 35 U.S.C. §§ 311-319 AND 37 C.F.R. § 42.100 *et seq.***

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Exhibit List

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Petitioner BOE Technology Group Co., Ltd., (“Petitioner” or “BOE”) respectfully petitions for *inter partes* review of claims 1-5, 7, and 9-15 of U.S. Patent No. 7,279,708 (“the ’708 patent” (EX1001)) in accordance with 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.100 *et seq.*

I. INTRODUCTION

The ’708 patent is directed to a sub-conductive layer that electrically connects an electrode (*e.g.*, cathode) in an electroluminescence (EL) display to the wires/lines that provide power to the display area to reduce the resistance of these power lines. (EX1001, 1:66-2:13.) The sub-conductive layer comprises penetration portion(s) to allow the gas generated from an underlying organic insulating layer to discharge, thereby preventing trapped gas from causing damage. (EX1001, 6:57-67.)

The idea of a sub-conductive layer that electrically contacts an electrode in an EL display and includes penetration portions was known before the ’708 patent. Discussed in more detail below, Matsueda discloses an EL display comprising ITO layers that electrically connect the cathode to auxiliary cathode wiring (power lines). Like the ’708 patent, Matsueda aims to reduce the wiring resistance via its ITO layers and makes them “islanded” with openings in between, thereby allowing the gas to release from the underlying planarizing layer. And then there is Koyama and Nakanishi. Komaya discloses an OLED display comprising connecting wiring

(a conductor layer) that electrically connects the cathode to input/output wiring. An organic interlayer insulating layer is located under the connecting wiring and, as Nakanishi explains, it may release gas when subjected to heat during the manufacturing process. Nakanishi teaches adding through holes in the conductor layer to allow the gas to release. Thus, the '708 patent's claimed sub-conductive layer and penetration portion were not new.

Petitioner submits that the challenged claims are unpatentable for the reasons set forth in this Petition, as supported by Dr. Jerzy Kanicki (EX1002).

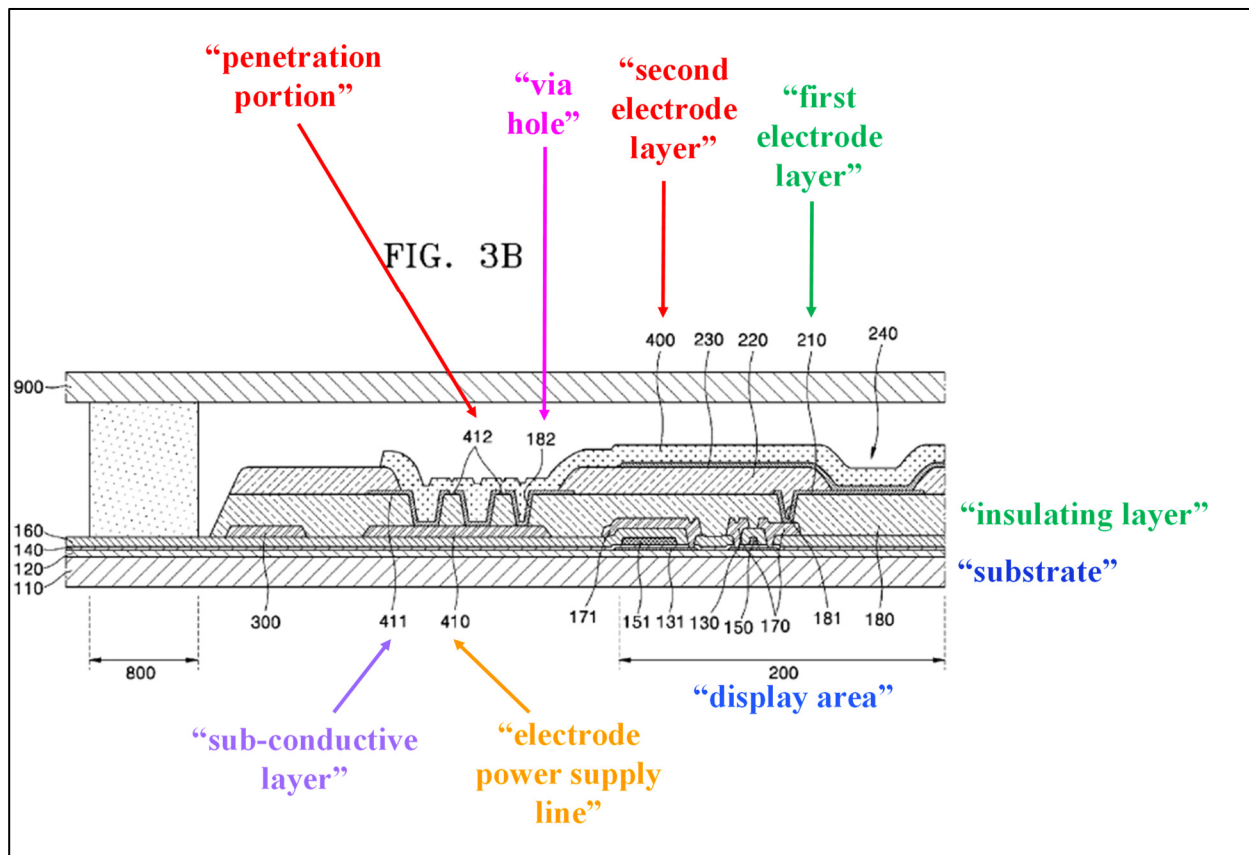
II. SUMMARY OF THE '708 PATENT

The '708 patent discloses “[a]n electroluminescence (EL) display device” comprising a sub-conductive layer. (EX1001, Abstract.) The '708 specification explains that “[a]s resolution of images displayed on the display device increases and the display device becomes larger, there is a need to reduce power consumption and improve aspects of image quality such as brightness.” (EX1001, 1:66-2:2.) The EL display device improves the image quality by “having an electrode that is electrically contacted to a cathode” to reduce contact resistance. (EX1001, 2:7-13; EX1002, ¶¶15-17.)

“[T]he sub-conductive layer 411 may be formed on the surface of the insulating layer 180” to prevent “peeling of the electrode power supply line 410.” (EX1001, 6:27-36.) Additionally, “[o]ne or more penetration portions 412 may be

formed on the sub-conductive layer 411” such that “the insulation [layer 180] can be saved from being damaged by the gas” that is discharged during the annealing process. (EX1001, 6:57-67.) Figure 3B¹ (below) shows a cross-sectional view of an organic EL display comprising a *display area 200* with pixels having an EL unit formed between a *first electrode layer 210* and a *second electrode layer 400* on a *substrate 110*. The organic EL display also comprises a *sub-conductive layer 411* formed on the *insulating layer 180* including a *via hole 182* along the *electrode power supply line 410*. The figure also shows the sub-conductive layer 411 including *penetration portions 412*. (EX1002, ¶¶18-22.)

¹ All emphasis and annotations added, unless otherwise noted.



A. Effective Filing Date

The '708 patent was filed on May 27, 2005, published on March 23, 2006, issued on October 9, 2007, and claims priority to a Korean application filed on May 29, 2004. For purposes of this Petition only, Petitioner relies on May 29, 2004 as the earliest effective filing date. (EX1002, ¶14.)

B. Prosecution History

During prosecution, the Examiner did not reject the claims based on any prior art, only based on § 112. (EX1003, 222-223.) Applicant made amendments to address the § 112 rejections, then the Examiner issued a Notice of Allowance, stating the distinguishing limitations were the sub-conductive layer: (1) “formed on

an insulating layer including a via hole along an electrode power supply line,” and (2) “on the insulating layer includes a penetration portion.” (EX1003, 195-196; EX1002, ¶¶23-25.)

C. Level Of Ordinary Skill In The Art

A person of ordinary skill in the art (POSITA) in the field of the ’708 patent would have a bachelor’s degree in electrical engineering or materials science, including OLED displays, or an equivalent level of skill, knowledge, and experience. This POSITA would have been aware of and generally knowledgeable about OLED materials, and display pixel design, layout, and operation. (EX1002, ¶¶31-33.)

III. CLAIM CONSTRUCTION

For purposes of this Petition only, Petitioner does not believe any terms require a form construction. Each term carries its “ordinary and customary meaning” (“the meaning that the term would have to a person of ordinary skill in the art in question” at the time of the invention). *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007) (citation omitted); (EX1002, ¶¶34-35.)

IV. PRECISE REASONS FOR RELIEF REQUESTED

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests cancellation of the challenged claims based on the following references (EX1002, ¶¶36-40):

Prior Art	Abbreviation	Date	Prior Art At Least Under §
U.S. 2004/0115989	Matsueda (EX1004)	August 11, 2003 (filed)	102(e)
U.S. 2003/0194484	Yamazaki (EX1005)	April 9, 2003 (filed)	102(e)
U.S. 2002/0021266	Koyama (EX1006)	February 21, 2002 (published)	102(b)
U.S. 2002/0153611	Nakanishi (EX1007)	October 24, 2002 (published)	102(b)

The statutory grounds (pre-AIA) for the challenge of each claim are:

Ground	35 U.S.C. §	Claim(s)	Prior Art Reference(s)
1	103	1-5, 7, 9-15	Matsueda
2	103	7	Matsueda, Yamazaki
3	103	1, 2, 5, 7, 9, 11, 12, 15	Koyama, Nakanishi
4	103	1-5, 7, 9-15	Matsueda, Nakanishi

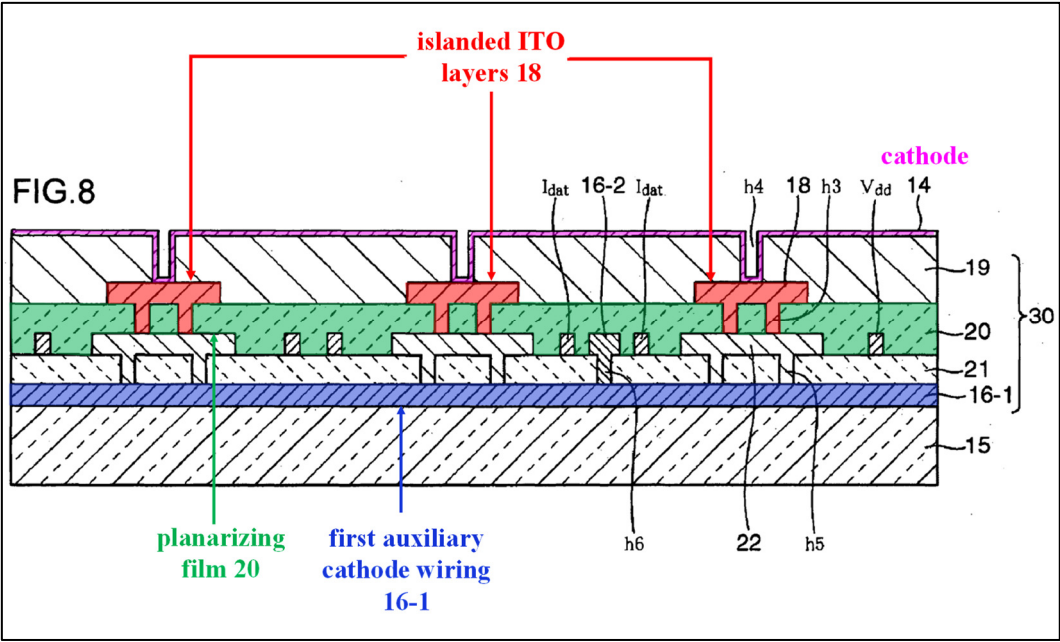
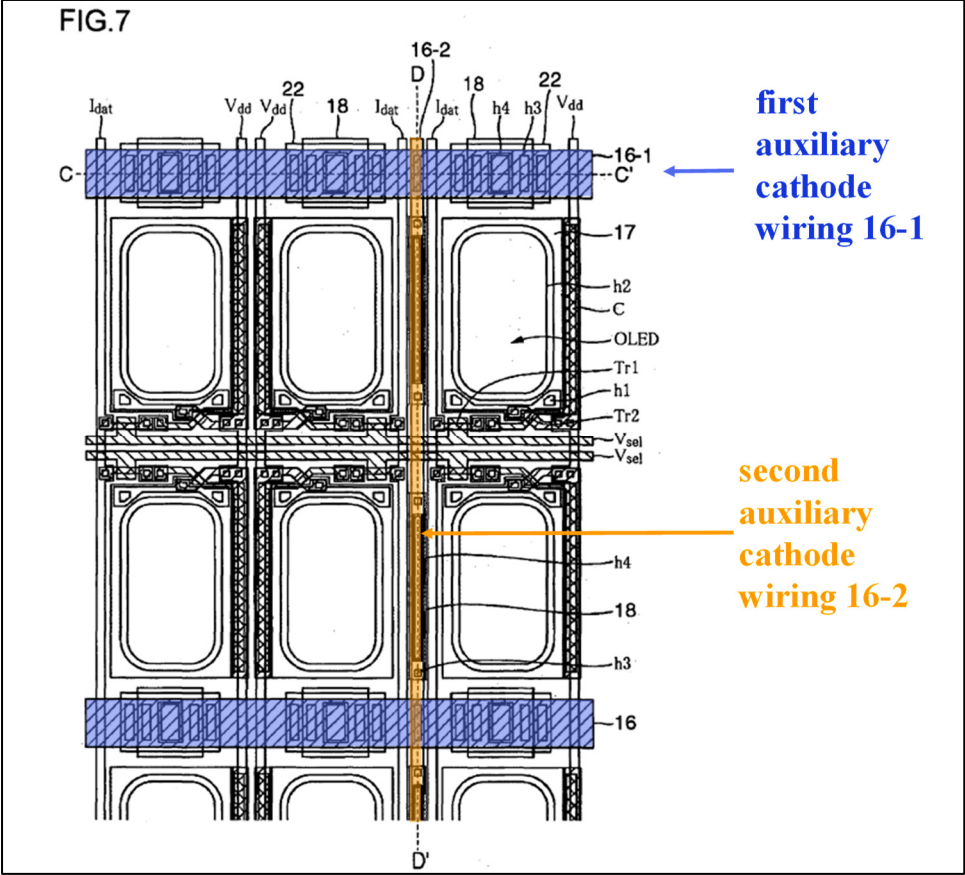
Below, Petitioner discusses why the challenged claims are unpatentable under the statutory grounds raised, including how and where the prior art satisfies each limitation of each challenged claim, as required by 37 C.F.R. § 42.104(b)(4). Petitioner's showing establishes a reasonable likelihood that it will prevail on each ground of unpatentability to each challenged claim.

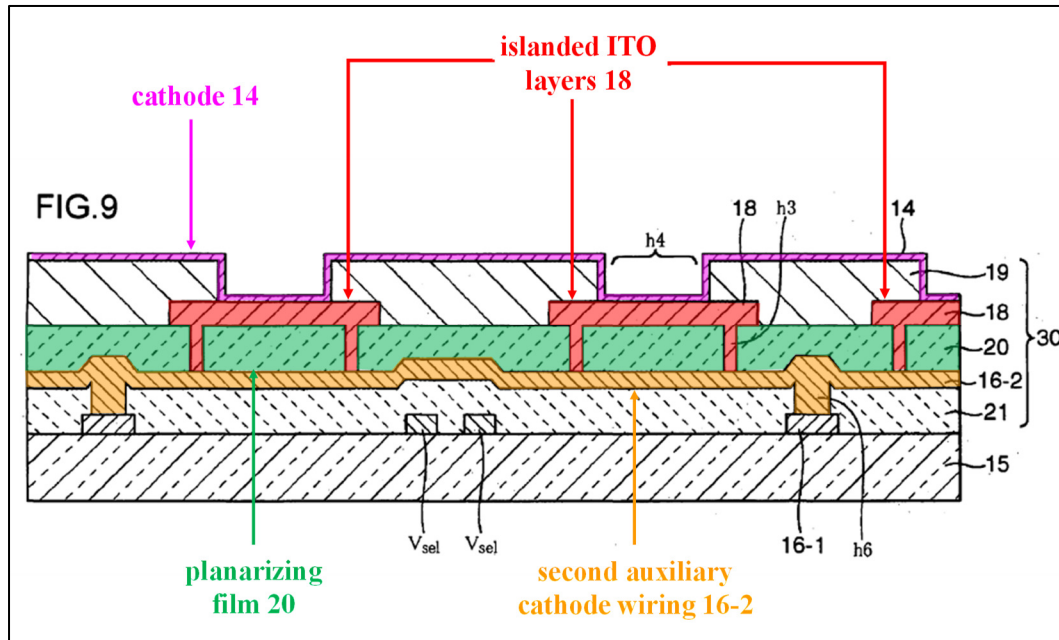
V. GROUND 1: MATSUEDA RENDERS OBVIOUS CLAIMS 1-5, 7, AND 9-15

A. Summary Of Matsueda

Matsueda discloses an electro-optical device “having a structure for power-supply wiring that is capable of providing a sufficient power to a common electrode of electrooptical devices.” (EX1004, [0006], [0048].) The Examiner never found, and the Applicant never cited Matsueda during prosecution.

Matsueda explains that the high resistance of the common electrode may be a problem that leads to “increased voltage drop in pixels in the center of the screen.” (EX1004, [0005].) It discloses “an electro-optical apparatus and a matrix substrate having a structure for power-supply wiring that is capable of providing a sufficient power to a common electrode of electrooptical devices.” (EX1004, [0006].) The power-supply wiring structure comprises auxiliary cathode wiring 16 disposed along the row and column directions (*first auxiliary cathode wiring 16-1* and *second auxiliary cathode 16-2*, respectively) (Figure 7 (below)). (EX1004, [0064].) Figures 8 and 9 (below) show that the electro-optical device also comprises *islanded ITO layers 18* on the *planarizing film 20* that is “disposed in a direction in which the first auxiliary cathode wiring 16-1 extend at multiple positions and are connected to the source metal layers 22 through contact holes h3.” (EX1004, [0069]; EX1002, ¶¶41-46.)



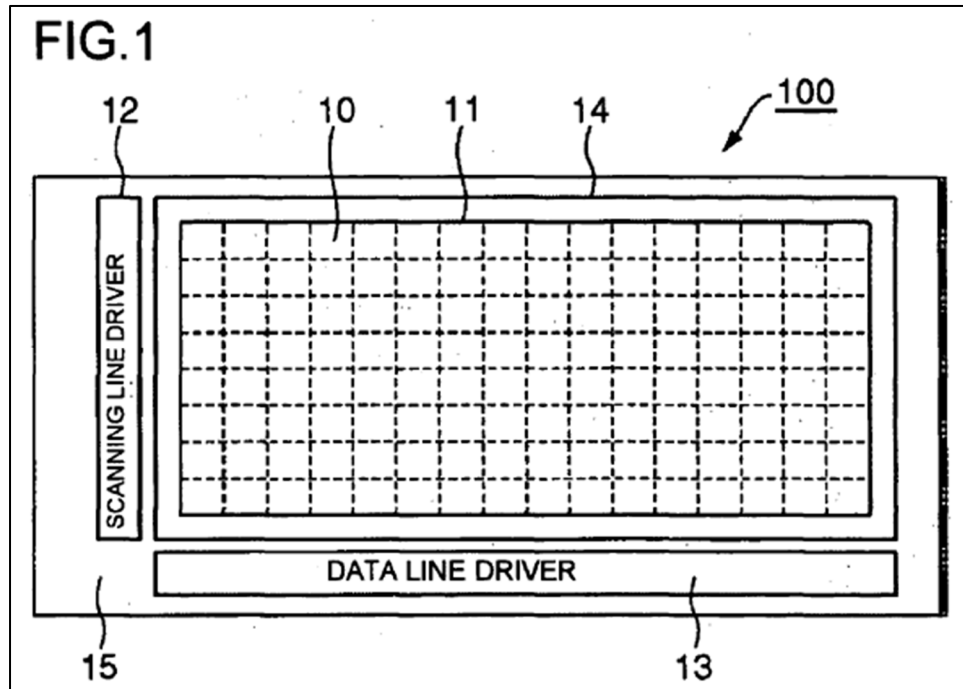


B. Claim 1

1. Preamble: “An electroluminescence display device, comprising:”

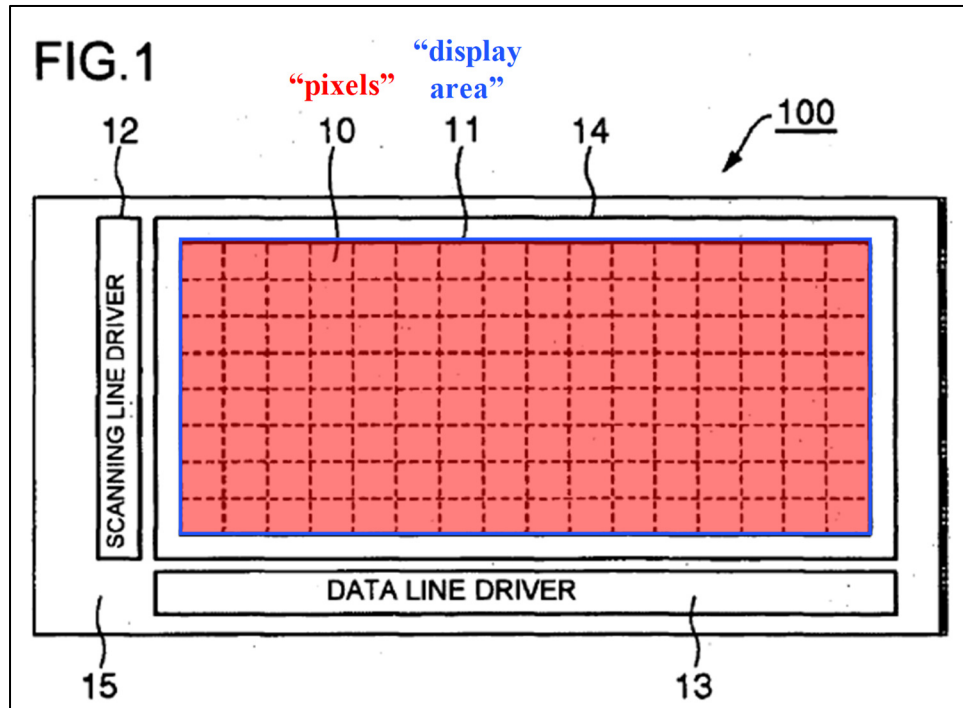
To the extent the preamble is limiting (which Petitioner does not concede for this claim or any other claim), Matsueda discloses the preamble.

Matsueda discloses “FIG. 1 [(below)] is a schematic of an active-matrix-type organic EL display panel 100 of the exemplary embodiment.” (EX1004, [0047]; *also* [0064] (“FIG. 7 shows the layout of wiring in an organic EL display panel 100”). (EX1002, ¶47.)

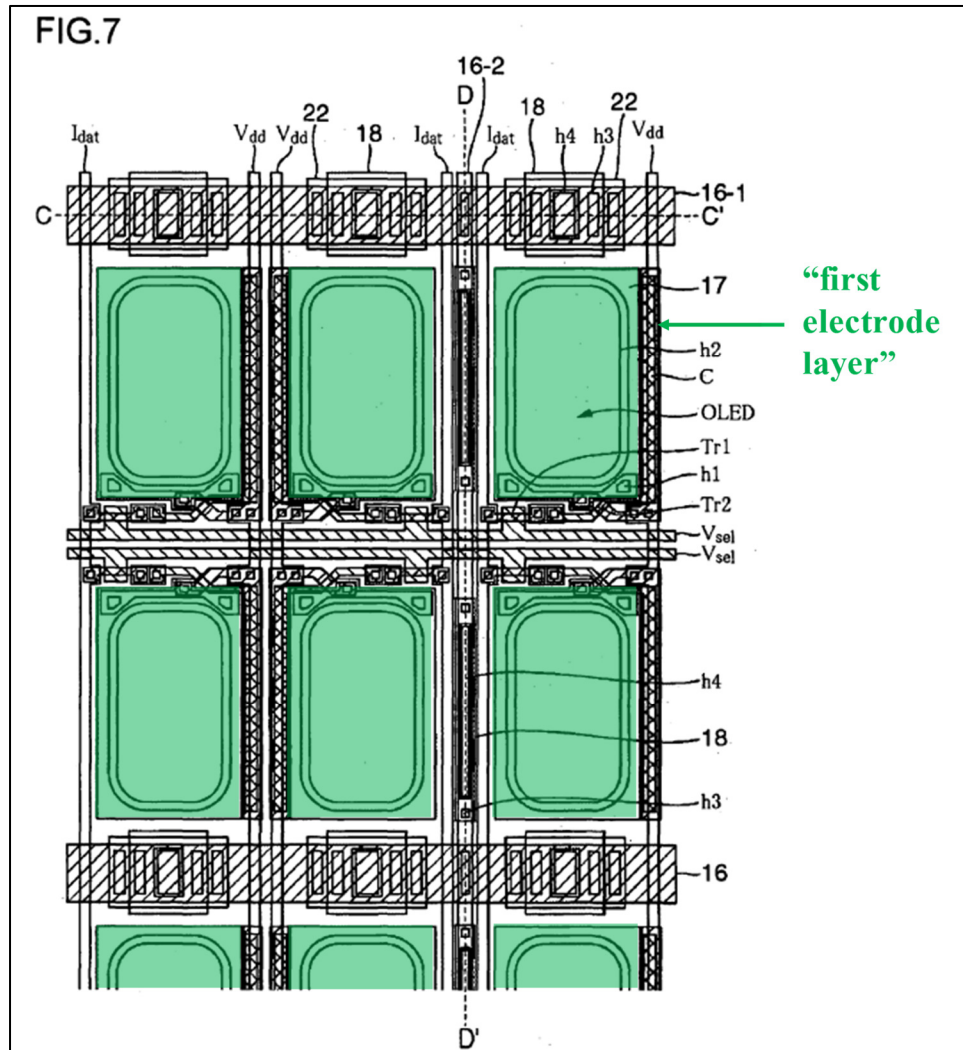


2. 1[a]: “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

Matsueda discloses an organic EL display panel 100 (Figure 1 (below)) comprising a “plurality of *pixels 10* hav[ing] laminated structures disposed on a *display area 11*.” (EX1004, [0047]; EX1002, ¶48.)



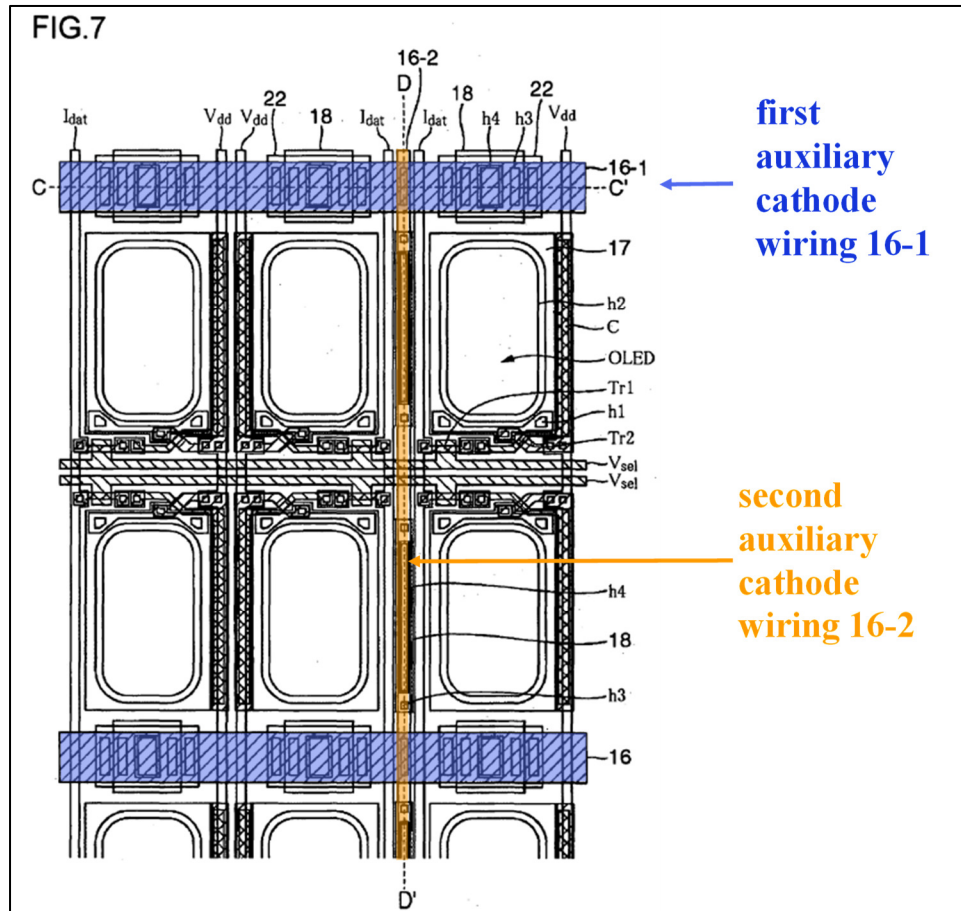
Matsueda discloses an “active-matrix-addressing-type organic EL display panels use . . . a pixel electrode, as the anode, is disposed for each pixel in a pixel area and a common electrode, as the cathode, covers the entire pixel area.” (EX1004, [0004].) “The entire surface of the laminated structure disposed on the display area 11 is covered with a film of a cathode 14 which serves as a common electrode.” (EX1004, [0047].) Figure 9 (below) shows the *cathode 14* on *substrate 15*. Like the ’708 claims, Matsueda refers to the cathode 14 as the “second electrode layer” and anode 17 as the “first electrode layer.” A POSITA would have understood that the cathode 14 being on the substrate 15 and the second electrode layer 14 being formed on or above the first electrode layers



Matsueda discloses that its “electro-optical devices hav[e] a laminated structure including first electrode layers . . . and a second electrode layer formed on or above the first electrode layers.” (EX1004, [0007].) It explains that “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent material is interposed between an anode and a cathode.” (EX1004, [0004].) Thus, Matsueda teaches an EL unit formed between the anode 17 and the cathode 14. (EX1002, ¶52.)

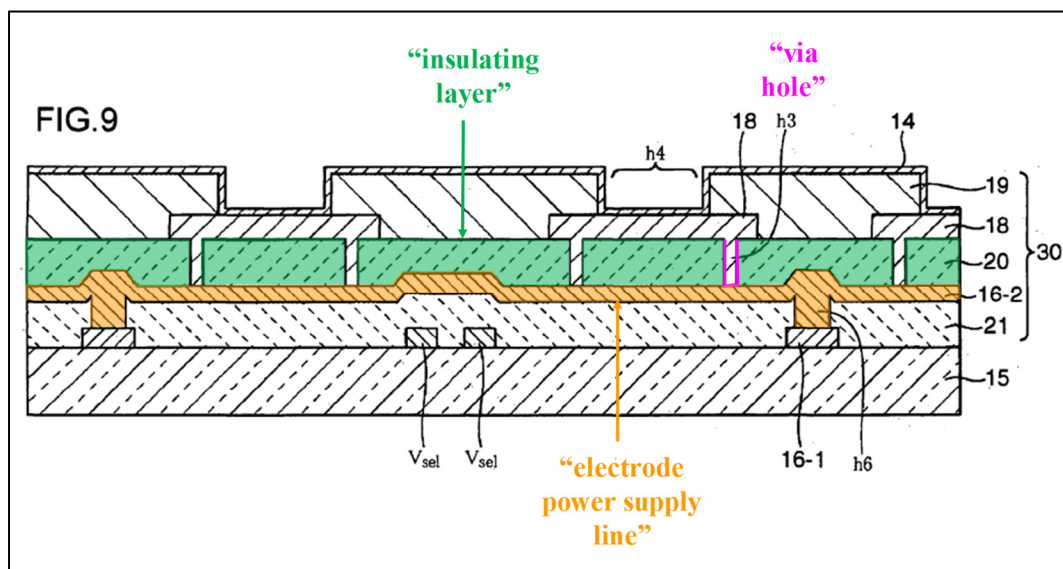
3. 1[b]: “an electrode power supply line to supply electrode power to the display area;”

Matsueda discloses “[t]he laminated structure further includes first power lines to supply a voltage to the first electrode layers, and second power lines electrically connected to the second electrode layer.” (EX1004, [0007], [0064].) Matsueda also discloses “the second power lines function as auxiliary cathode wiring, thereby supplying sufficient electrical power to the cathode of the electro-optical devices.” (EX1004, [0026].) Matsueda explains that “[t]he entire surface of the laminated structure disposed on the display area 11 is covered with a film of a cathode 14 which serves as a common electrode.” (EX1004, [0047].) By supplying electrical power to the cathode, which covers the display area 11, Matsueda teaches auxiliary cathode wiring 16 (Figure 7 (below)) supplying electrode power to the display area 11. (EX1002, ¶¶53-55.)



4. 1[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”

Matsueda discloses “[r]eferring to FIG. 8, a laminated structure 30 in which the *first auxiliary cathode wiring 16-1*, insulating interlayer film 21, a *planarizing film 20*, . . . are sequentially laminated, is formed on the display area 11 and on the substrate 15.” (EX1004, [0067], [0069].) Thus, Matsueda teaches a planarizing film 20 (“insulating layer”) disposed on auxiliary cathode wiring 16 (“electrode power supply line” (see 1[b])). Figures 8 and 9 (below) show *planarizing film 20*



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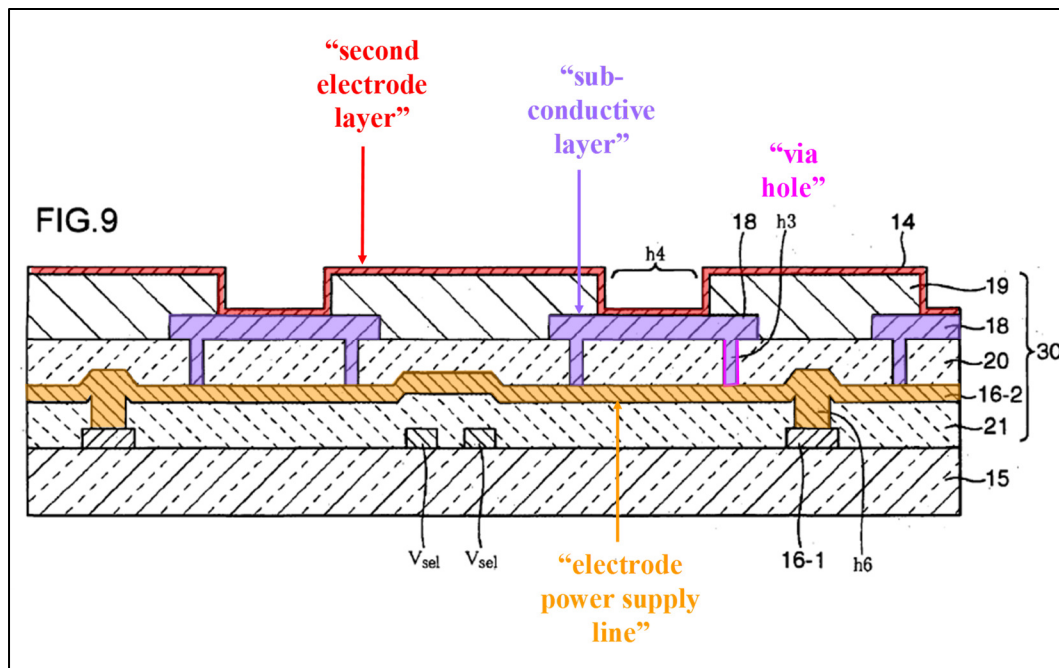
through contact holes h3.” (EX1004, [0069].) Thus, Matsueda teaches the planarizing film 20 including a contact hole h3 (“via hole”). Figures 8 and 9 (above) show *planarizing film 20* including *contact hole h3*. (EX1002, ¶57.)

It would have been obvious to a POSITA that Matsueda’s planarizing film 20 contains an organic material because planarizing films for EL devices at the time of the ‘708 patent comprised organic materials. The purpose of the planarizing film in organic displays is to provide a smooth and uniform (planar) surface for layers that are subsequently formed, and organic materials are well suited for this purpose. (*See, e.g.*, EX1009, 2:17-24 (“planarization film 17 made of an organic resin for flattening the surface is formed on the entire surface” of an electroluminescent display device); EX1002, ¶58.)

Additionally, it would have been obvious for Matsueda’s planarizing film to contain an organic material. Matsueda teaches an organic material located between the cathode and the auxiliary cathode wiring (“electrode power supply line”). One example organic material is the bank layer 19: “[t]he bank layer 19, which is made of a photosensitive organic material or the like is formed on the planarizing films 20.” (EX1004, [0069], [0053].) Configuring the planarizing film 20 to contain an organic material would have been an obvious design choice. (EX1002, ¶59.)

auxiliary cathode wiring 16 (“electrode power supply line” (*see* 1[b])) and cathode 14 (“second electrode layer” (*see* 1[a])) coupled to each other. (EX1002, ¶¶63-64.)

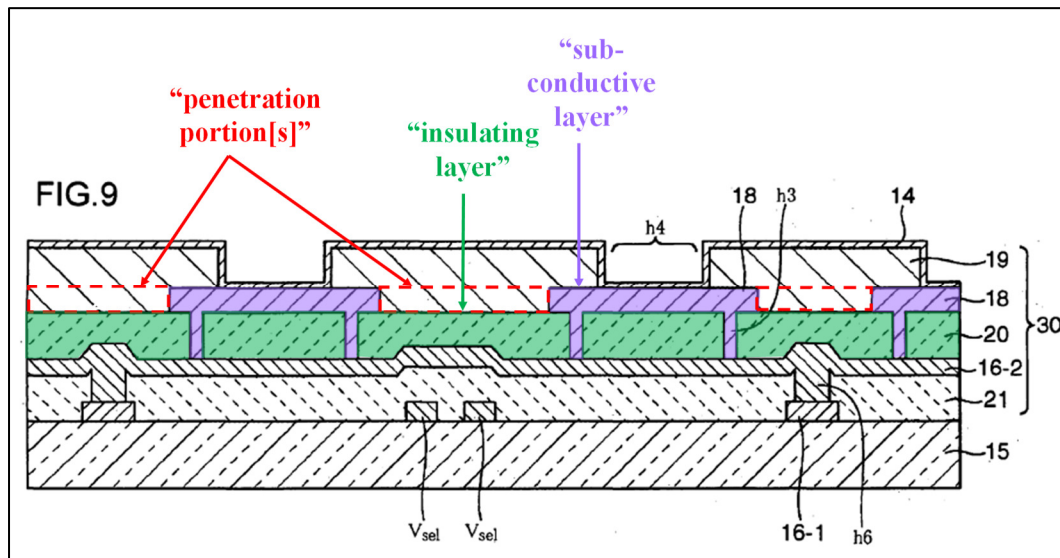
Matsueda also discloses “[t]he ITO layers 18 are connected to the second auxiliary cathode wiring 16-2 through the contact holes h3 formed in the planarizing films 20.” (EX1004, [0070].) Figure 9 shows *auxiliary cathode wiring 16* and *cathode 14* coupled to each other at the *contact hole h3* (“via hole” (*see* 1[c])) through the *ITO layer 18* (“sub-conductive layer” (*see* 1[d])). (EX1002, ¶¶64.)

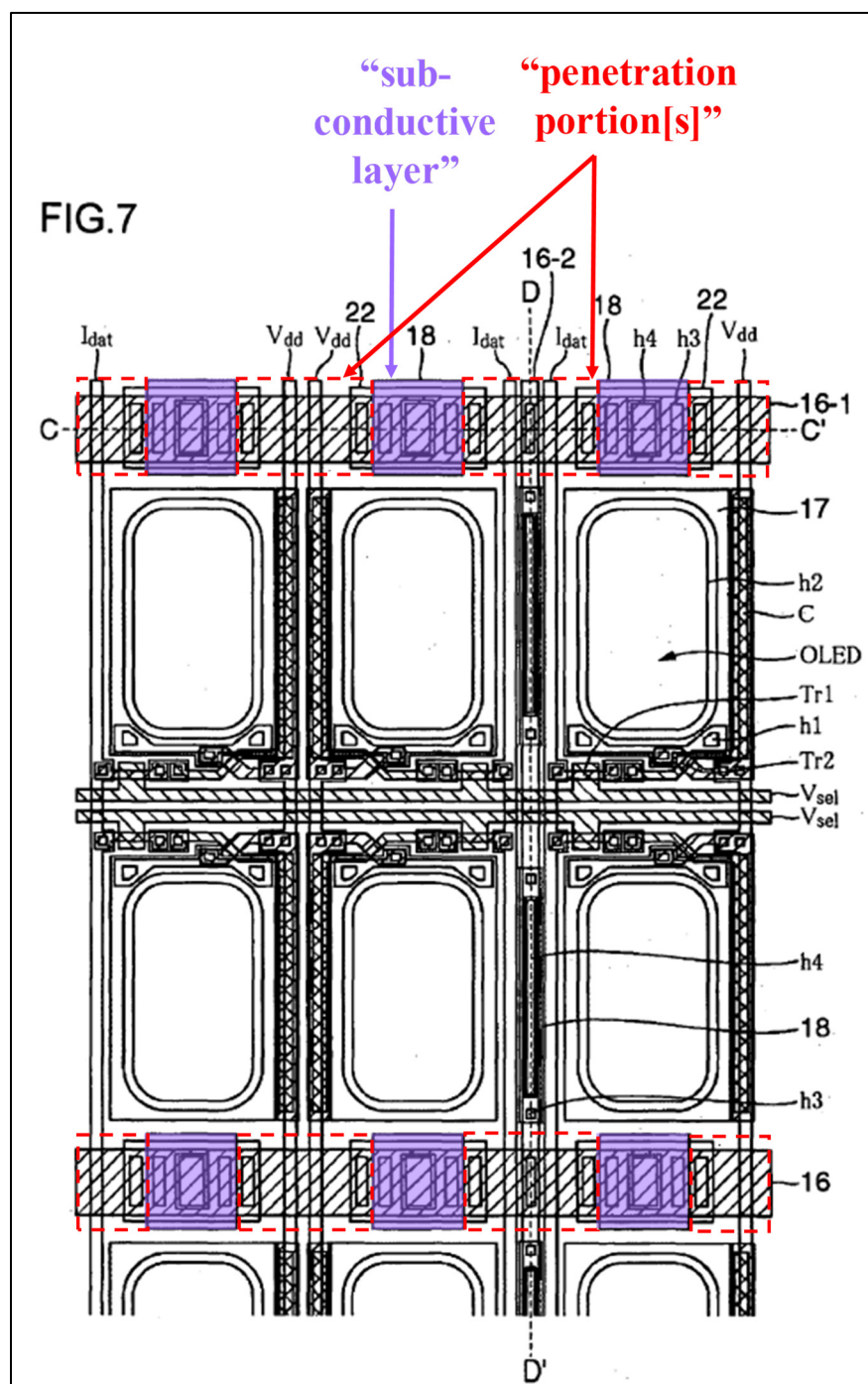


7. 1[f]: “the sub-conductive layer on the insulating layer includes a penetration portion.”

Matsueda discloses “[o]n the planarizing films 20, the islanded ITO layers 18 are disposed in a direction in which the first auxiliary cathode wiring 16-1

extend at multiple positions and are connected to the source metal layers 22 through contact holes h3.” (EX1004, [0069].) A POSITA would have understood the ITO layers 18 being “islanded” means they are separated by a penetration portion. Figure 9 (below) shows the ITO layer 18 on the *planarizing film 20*, and Figures 7 and 9 (below) show the *ITO layer 18* including a *penetration portion*. (EX1002, ¶¶65-66.)





C. Claim 2: “The device of claim 1, wherein the sub-conductive layer comprises the same layer as at least a part of the first electrode layer.”

Matsueda teaches *islanded ITO layers 18* (“sub-conductive layer” (*see* 1[d])) located in the wiring area, and the *anode / pixel electrode 17* (“first electrode layer” (*see* 1[a])) located in the display area, as shown in Figure 7 (below). (EX1002, ¶¶67-68.)

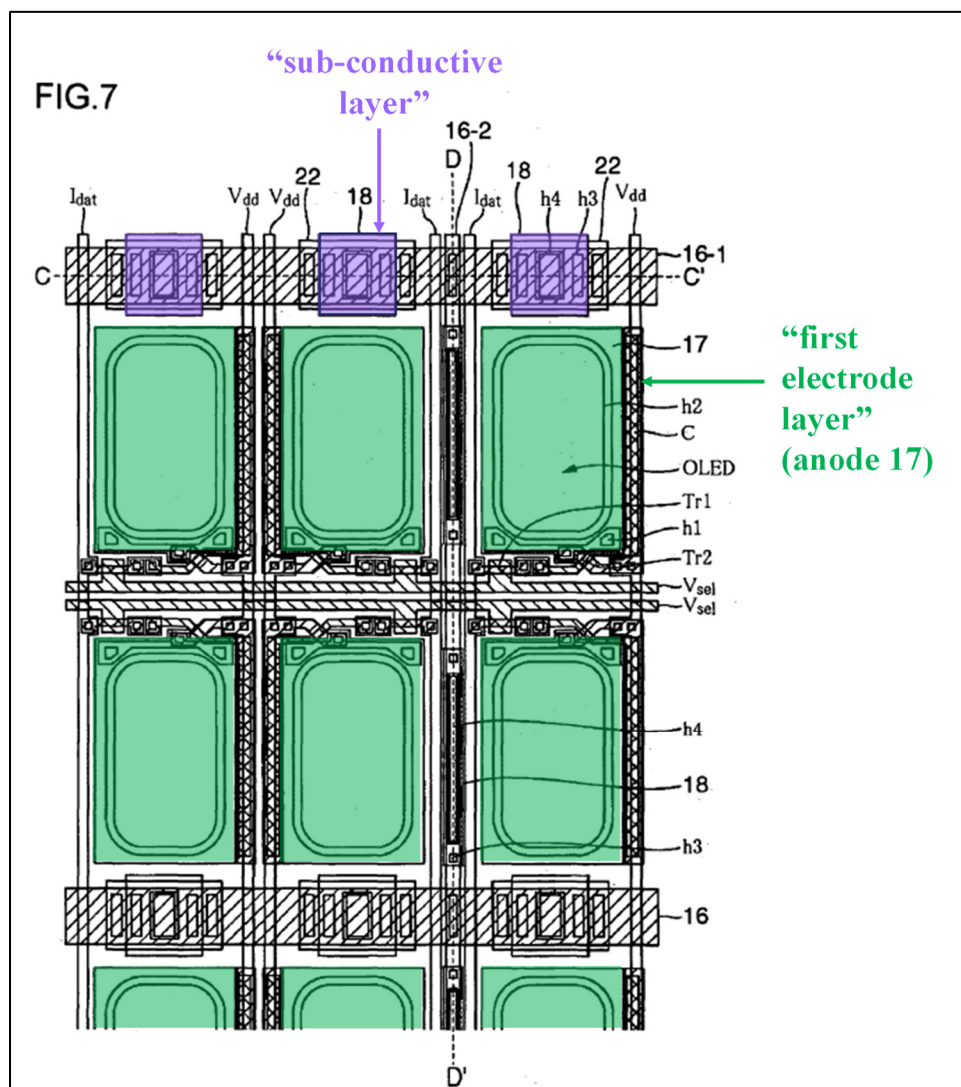
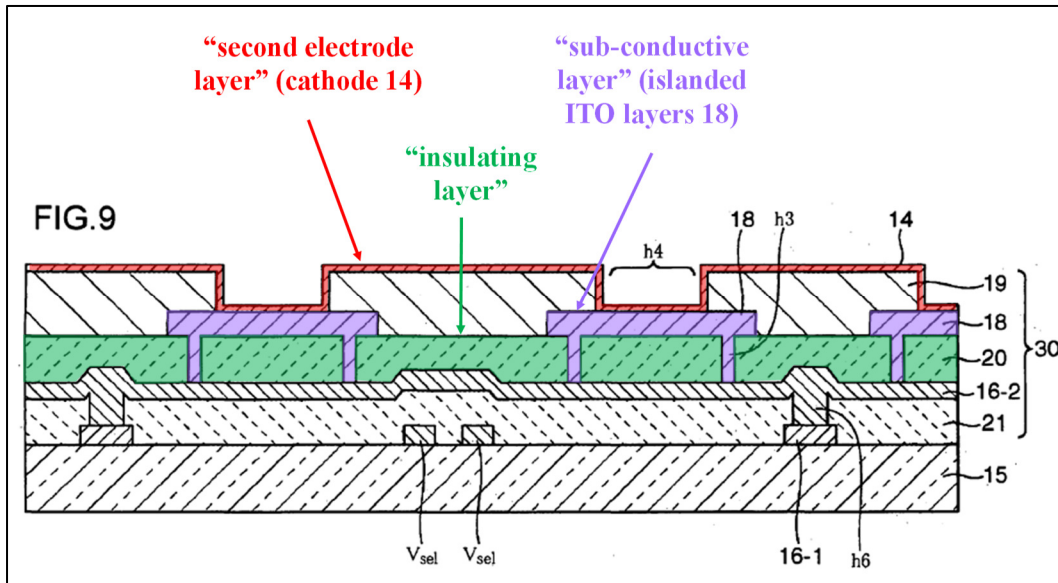


Figure 9 (below) shows a cross-sectional view of the wiring area, with the **cathode 14** disposed on the **islanded ITO layers 18**, and the islanded ITO layers 18 disposed on the **planarizing film 20**. Matsueda discloses that “[t]he organic EL display panel 100 has a bottom-emission structure that emits light through the substrate 15.” (EX1004, [0048].) Matsueda explains that “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent

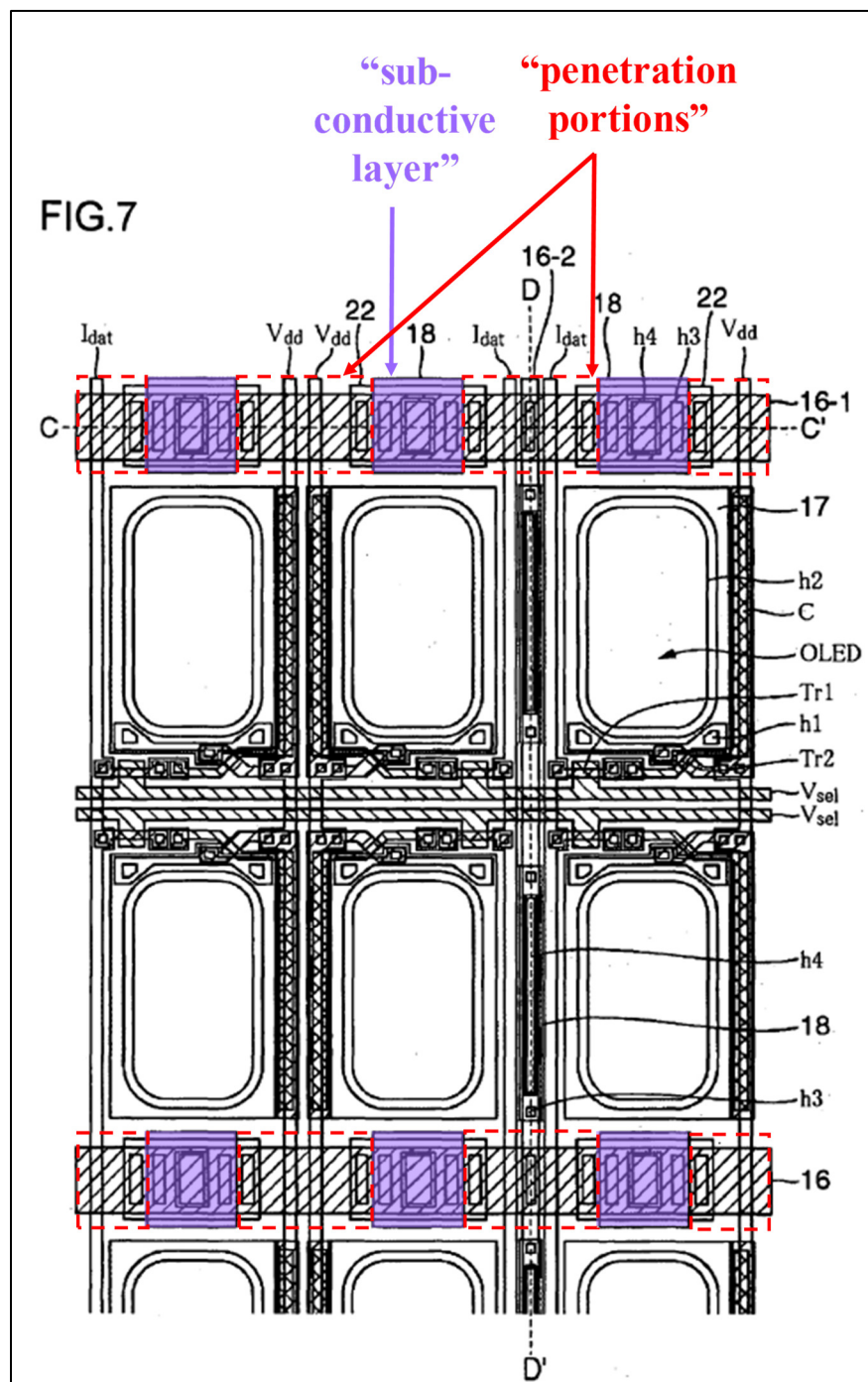
material is interposed between an anode and a cathode.” (EX1004, [0004].) Thus, it would have been obvious that in the display area (not shown in Figure 9), where the pixels are located, the anode / pixel element 17 would be disposed on the planarizing film 20. Matsueda discloses such teachings in another one of his patents, for example, EX1010 at 5:21-23 (“The ITO layer 59 is patterned so as to form a pixel electrode layer (an anode) 59.”), Figs. 2, 3). As another example, EX1008 discloses “anode (pixel electrode) 23” at 5:57, and describes a pixel electrode made of ITO at 7:10. The ITO layers 18 and anode / pixel element 17 are disposed on the planarizing film 20. The ITO layer 18 is also disposed on the source metal layer 22, as shown in Figure 4, which is a source electrode layer of the transistor. (EX1004, [0052].) The anode / pixel element 17 is on or above the transistor. (*See, e.g.*, EX1010, Fig. 3 (showing anode 59 on the wiring (source metal layer) 57).) Thus, it would have been obvious that the ITO layers 18 are deposited on the same layer as the anode / pixel element 17. (EX1002, ¶69.)

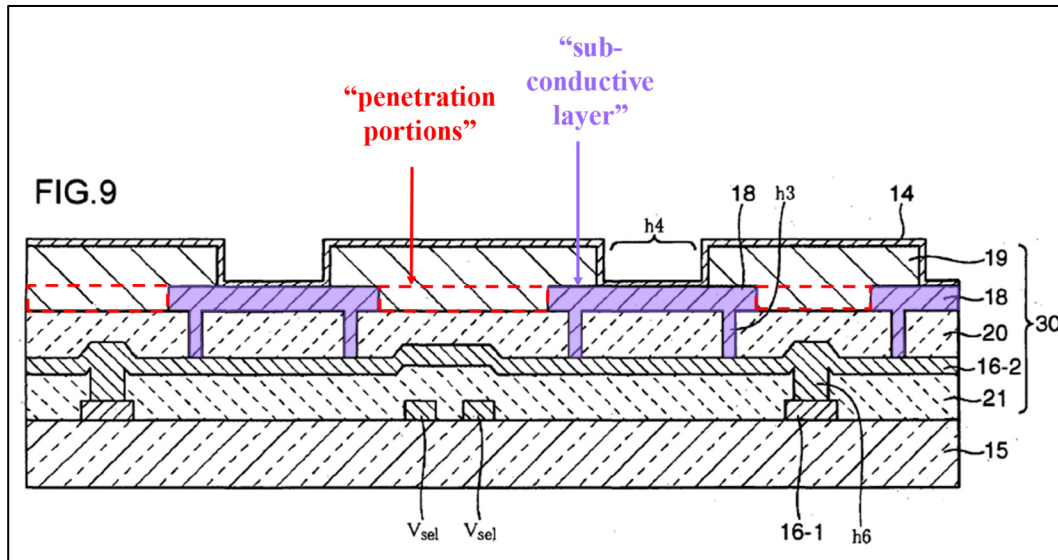


D. Claim 3

1. 3[a]: “The device of claim 1, wherein the sub-conductive layer comprises two penetration portions, and”

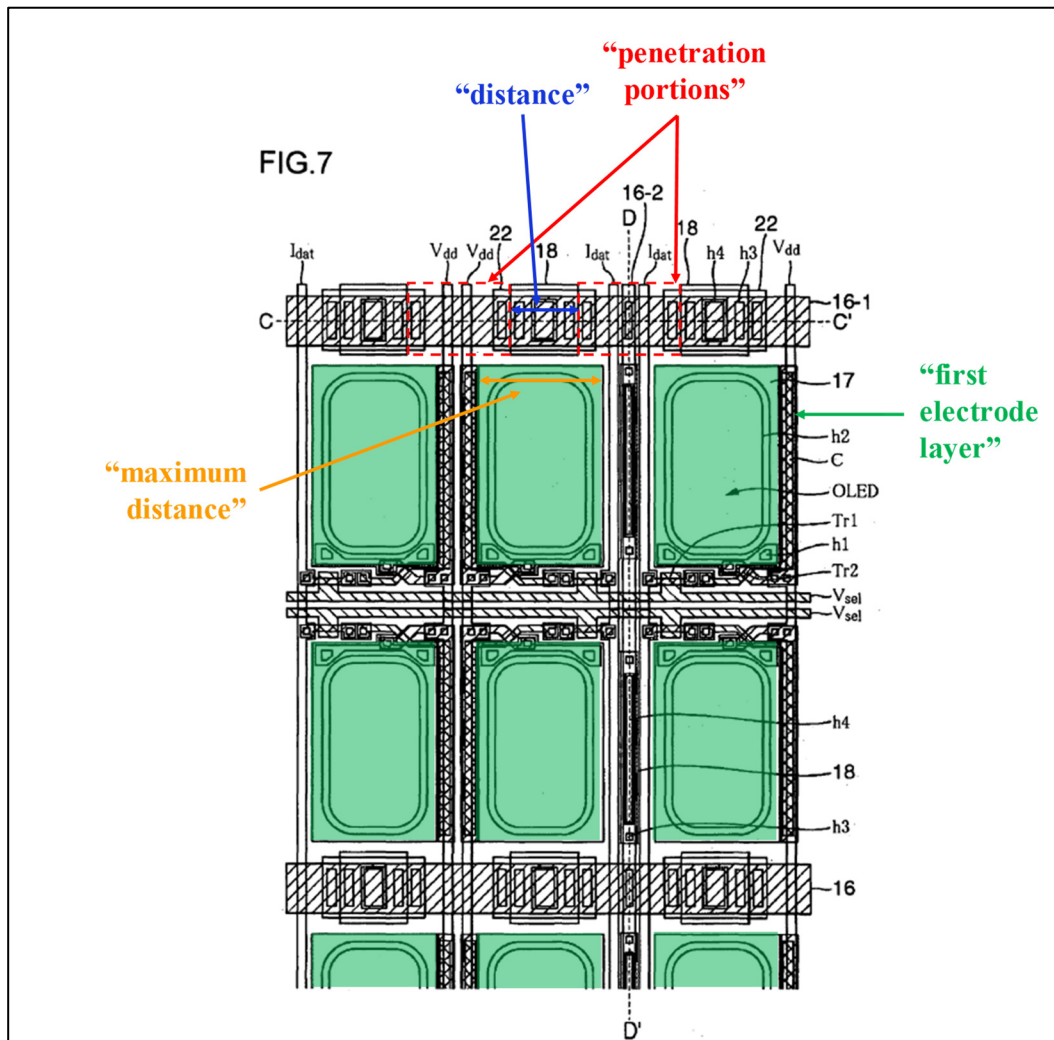
Figures 7 and 9 (below) show that Matsueda’s *islanded ITO layers 18* (“sub-conductive layer” (*see* 1[d])) comprises two *penetration portions*. (EX1002, ¶¶70-71.)





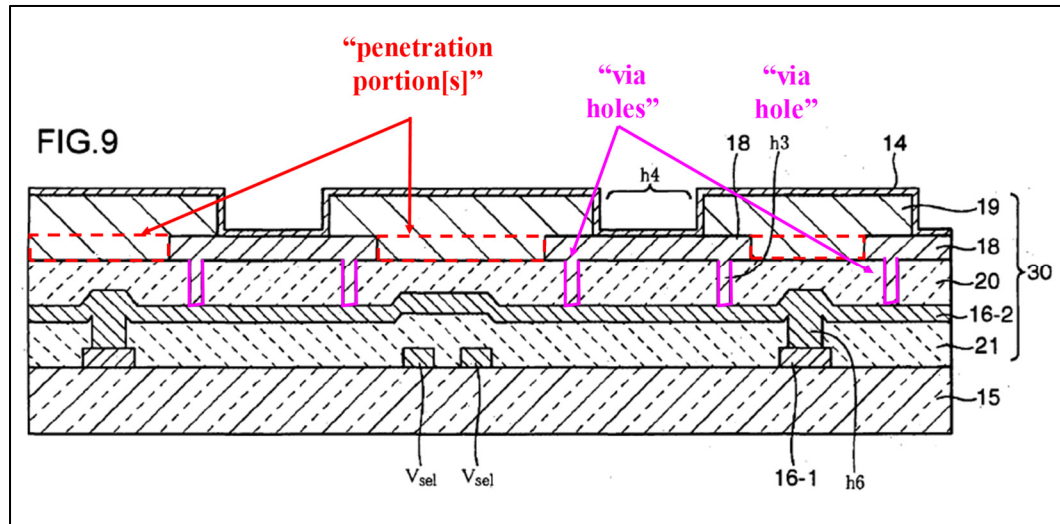
2. 3[b]: “a distance between the two penetration portions is less than or equal to a maximum distance between both ends of the first electrode layer.”

Figure 7 (below) shows the *distance* between two *penetration portions* is less than a *maximum distance* between both ends of the *pixel element 17* (“first electrode layer” (see 1[a])). A POSITA would have understood that the relative sizes of the objects and spacings between the objects in the figures in Matsueda are representative. For example, Figures 3 and 4 show the ITO layer 18 is smaller than the pixel electrode 17. The source metal layer 22 is on the same layer as and disposed between the data line I_{dat} and Vdd line, which means the source metal layer 22 cannot be connected to the data line I_{dat} and Vdd line. The pixel electrode 17 is disposed between the data line I_{dat} and Vdd line, and as a result, the width of the ITO layer 18 is less than the width of the pixel element 17. (EX1004, [0035], [0051], [0053], [0055], [0059], [0064], [0065]; EX1002, ¶¶72-74.)



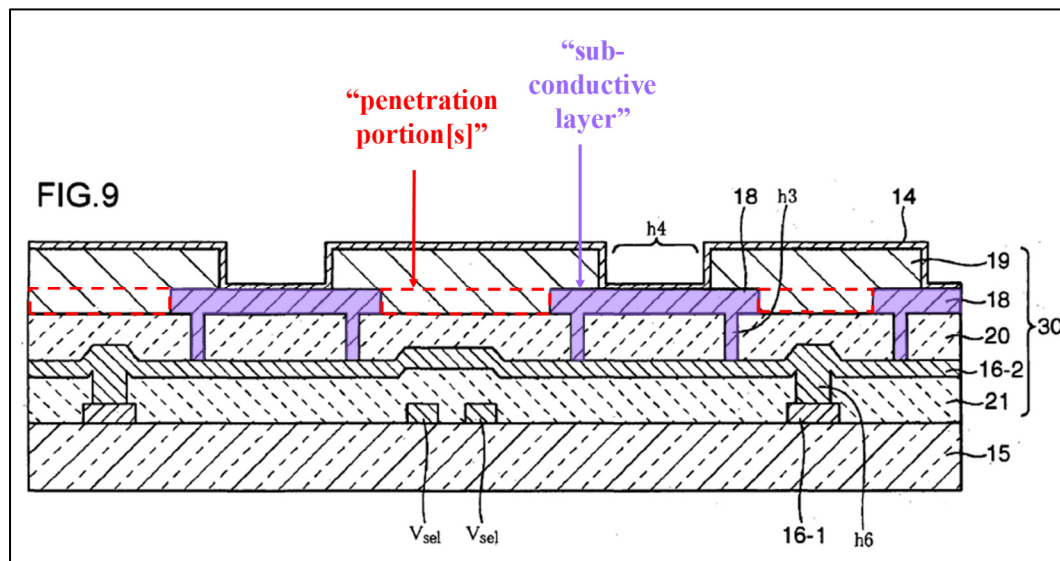
E. Claim 4: “The device of claim 3, wherein at least one of the two penetration portions is disposed on at least a part of an outer portion of the via hole.”

Figure 9 (below) shows at least one of the two *penetration portions* is disposed on at least a part of an outer portion of the *contact hole h3* (“via hole” (see 1[c])). (EX1002, ¶¶75-76.)



F. Claim 5: "The device of claim 1, wherein the penetration portion comprises a penetration hole."

Figure 9 (below) shows the *penetration portion* goes through the *ITO layers* 18. Thus, the penetration portion comprises a penetration hole. (EX1002, ¶77.)



G. Claim 7

1. **7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”**

As shown in Figures 4 and 8, Matsueda discloses an ITO layer 18 disposed on the source metal layer 22. (EX1004, [0052], [0067].) A POSITA would have understood the source metal layer 22 is a source electrode layer of a transistor (“thin film transistor layer”). Matsueda also discloses the anode / pixel electrode 17 (“first electrode layer” (*see* 1[a])) on or above the transistor. (*See* claim 2.) As a result, Matsueda’s thin film transistor layer is disposed under the anode / pixel electrode 17. (EX1002, ¶¶78-79.)

2. **7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”**

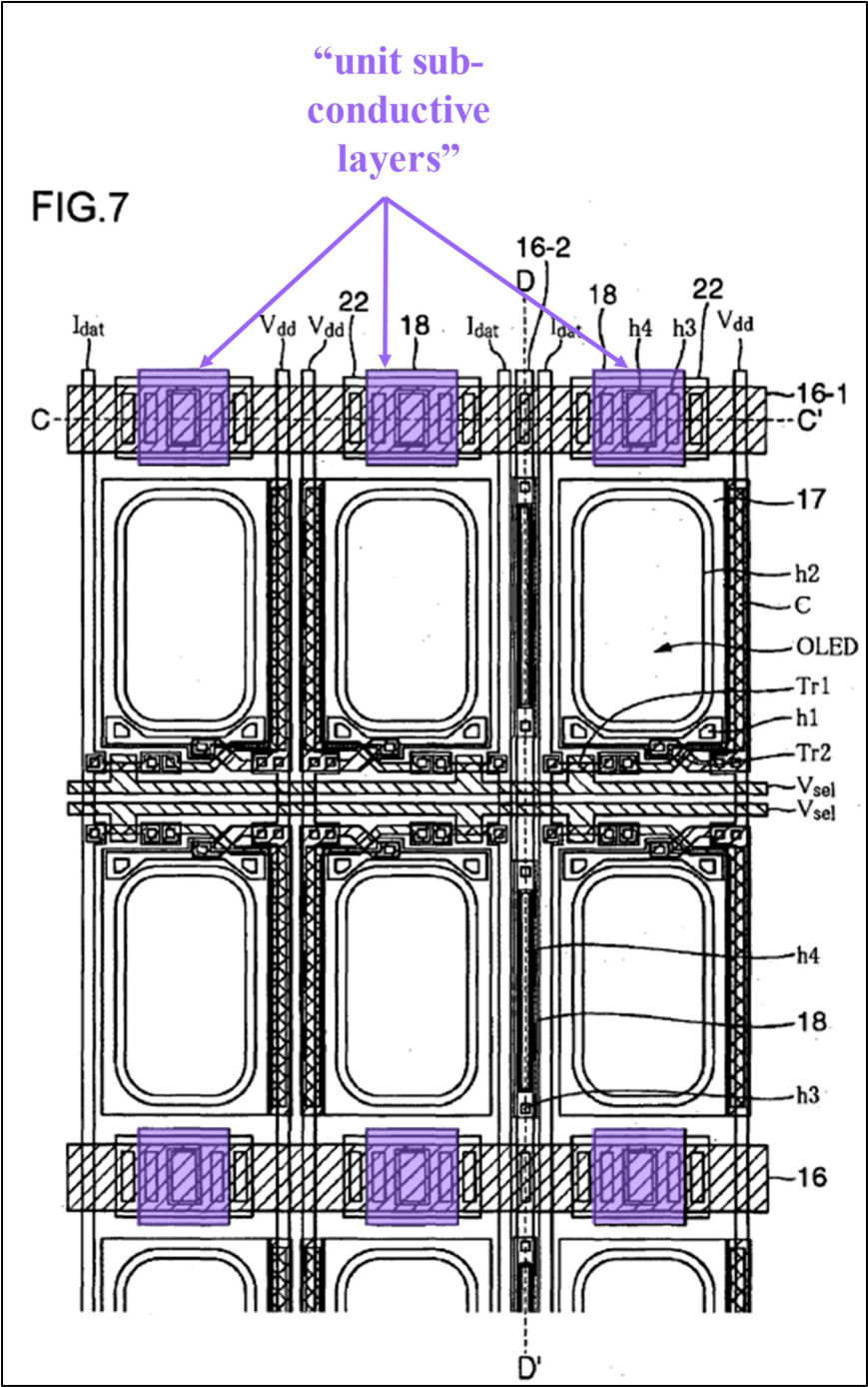
Figure 9 (below) of Matsueda shows that *auxiliary cathode wiring 16-2* (part of “electrode power supply line” (*see* 1[b])) is located on the *insulating interlayer film 21*. Figure 8 (below) shows that the *source metal layers 22* (source electrode of the “thin film transistor layer” (*see* 7[a])) is located on the *insulating interlayer film 21*. As a result, the electrode power supply line comprises a layer (auxiliary cathode wiring 16-2) that is the same layer as the source metal layers. (EX1002, ¶¶80-82.)

2. **9[d]: “a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”**

Element 9[d] is similar to element 1[d], but element 9[d] also requires the sub-conductive layer “comprising a plurality of unit sub-conductive layers.”

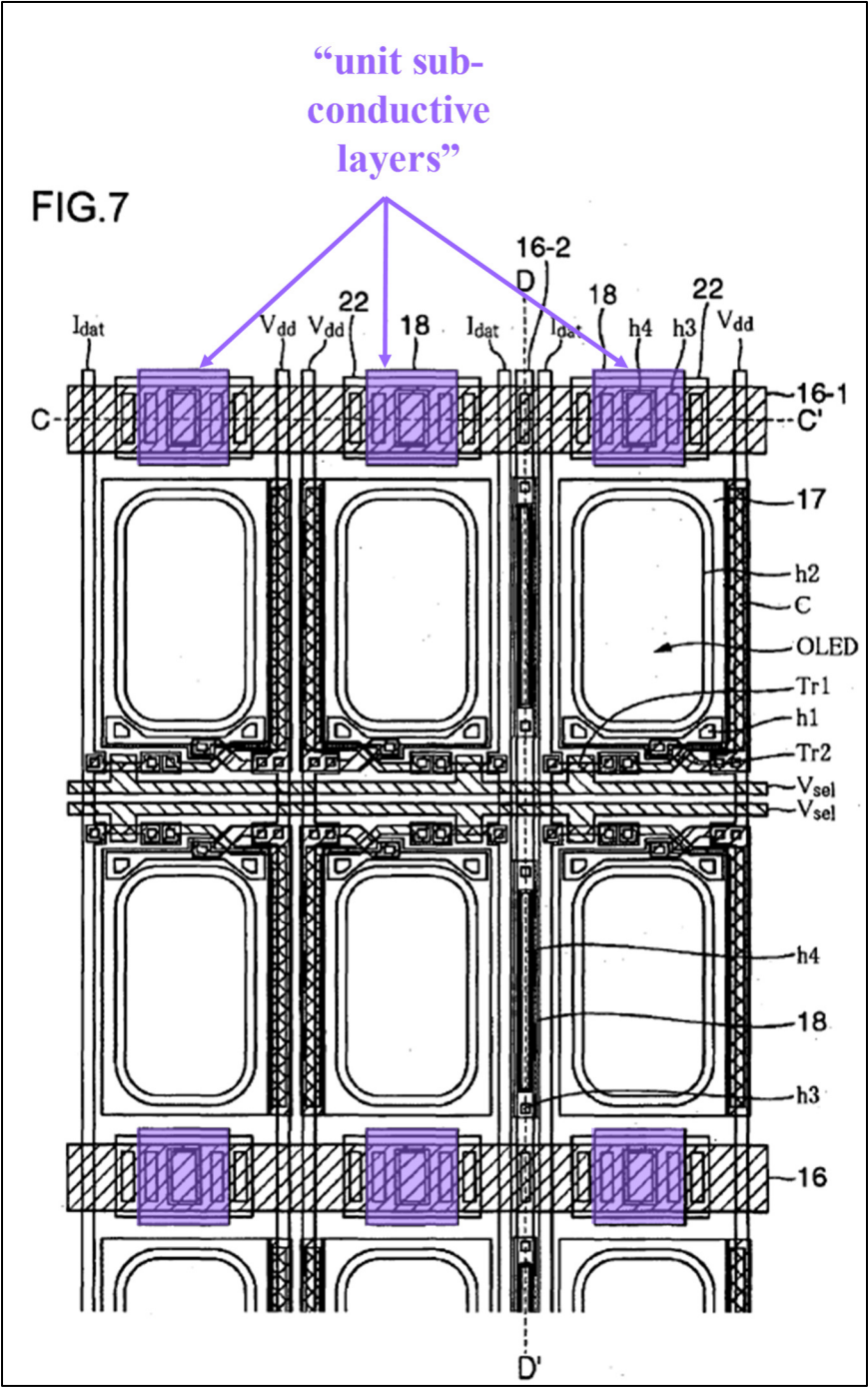
Matsueda teaches element 1[d]. (*See* 1[d]; EX1002, ¶¶87-88.)

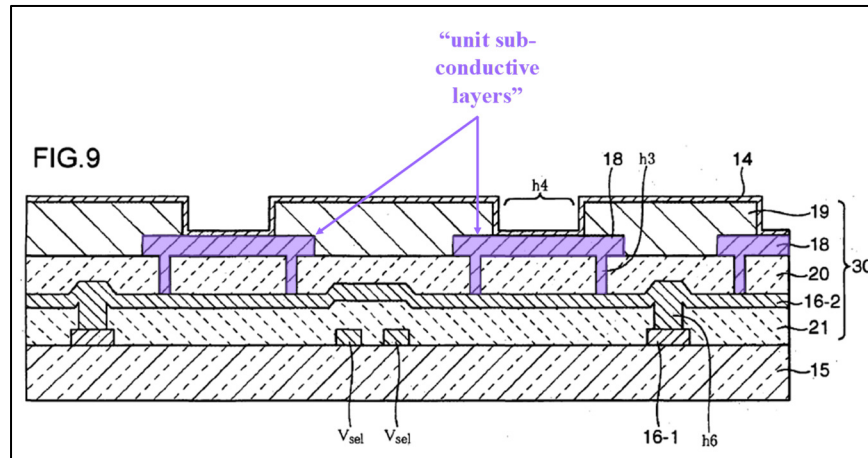
Matsueda discloses “[o]n the planarizing films 20, the *islanded ITO layers 18* are disposed” (EX1004, [0069].) A POSITA would have understood the ITO layers 18 being “islanded” means there are a plurality of unit sub-conductive layers separated from each other. Figure 9 (below) shows the *islanded ITO layers 18*. (EX1002, ¶89.)



3. 9[f]: “the unit sub-conductive layers on the insulating layer are separated from each other.”

Matsueda’s ITO layer 18 is on the planarizing film (“insulating layer”). (*See* 1[d].) Figures 7 and 9 (below) show the *islanded ITO layers 18* (“unit sub-conductive layers (*see* 9[d])) are separated from each other. (EX1002, ¶¶91-92.)

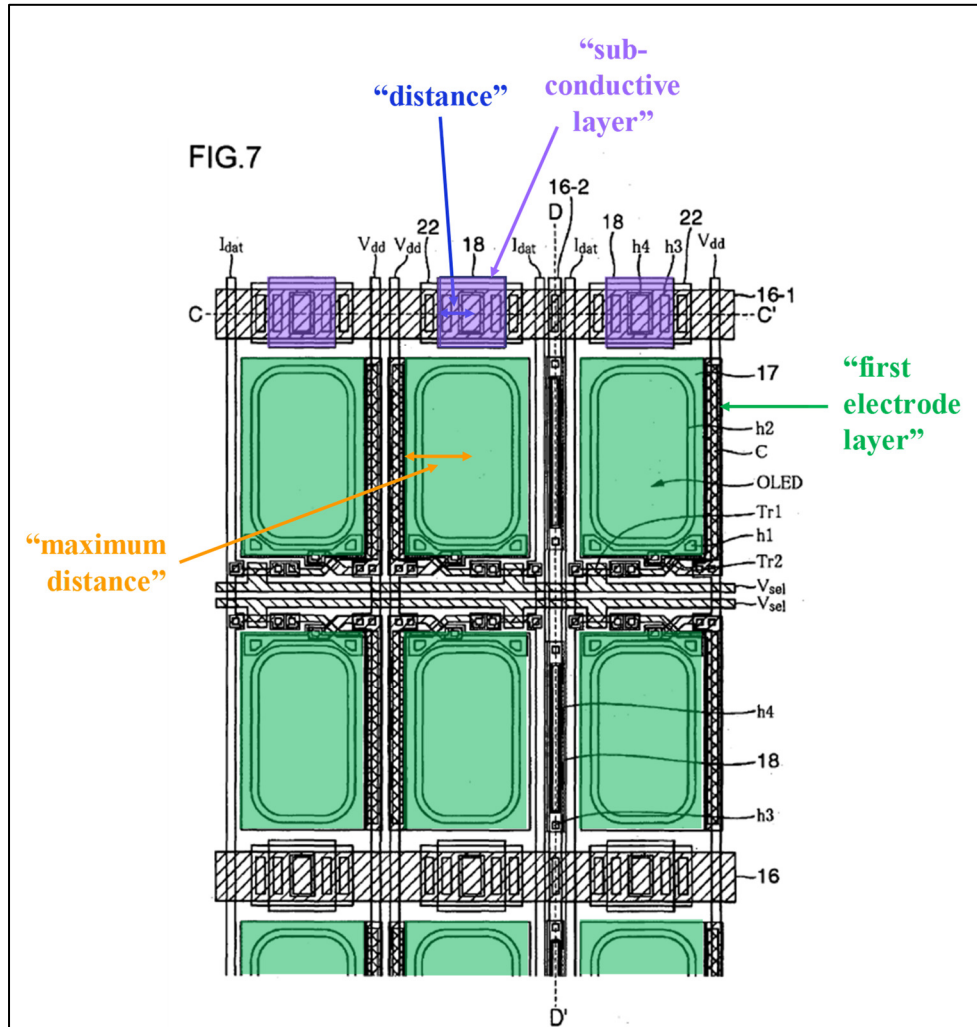




- I. Claim 10: “The device of claim 9, wherein a distance between a point of the unit sub-conductive layer and a neighboring outer point is less than or equal to a maximum distance between a point of the first electrode layer and a neighboring outer point.”**

Figure 7 (below) shows a *distance* between a point of the *ITO layers 18* (“unit sub-conductive layer” (*see* 9[f])) and a neighboring outer point is less than or equal to a *maximum distance* between a point of *pixel element 17* (“first electrode layer” (*see* 1[a])) and a neighboring outer point. A POSITA would have understood that the relative sizes of the objects and spacings between the objects in the figures in Matsueda are representative. For example, Figures 3 and 4 show the ITO layer 18 is smaller than the pixel electrode 17. The source metal layer 22 is on the same layer as and disposed between the data line I_{dat} and Vdd line, which means the source metal layer 22 cannot be connected to the data line I_{dat} and Vdd line. The pixel electrode 17 disposed between the data line I_{dat} and Vdd line, and as a result, the width of the ITO layer 18 is less than the width of the pixel element

17. (EX1004, [0035], [0051], [0053], [0055], [0059], [0064], [0065]; EX1002, ¶¶93-95.)



J. Claim 11

1. Preamble: “A method of manufacturing an electroluminescence display device, comprising:”

To the extent the preamble is limiting (which Petitioner does not concede for this claim or any other claim), Matsueda discloses the preamble.

Matsueda teaches an organic EL display panel 100 (“electroluminescence display device”). (*See* 1[pre]; EX1002, ¶¶96.)

Matsueda describes the manufacturing process including steps for forming several layers of the organic EL display panel 100, such as “[t]he first power lines and the second power lines may be formed . . . in the manufacturing process or may be formed in different layers.” (EX1004, [0009]; *also* [0017], [0024], [0033]; EX1002, ¶¶97.)

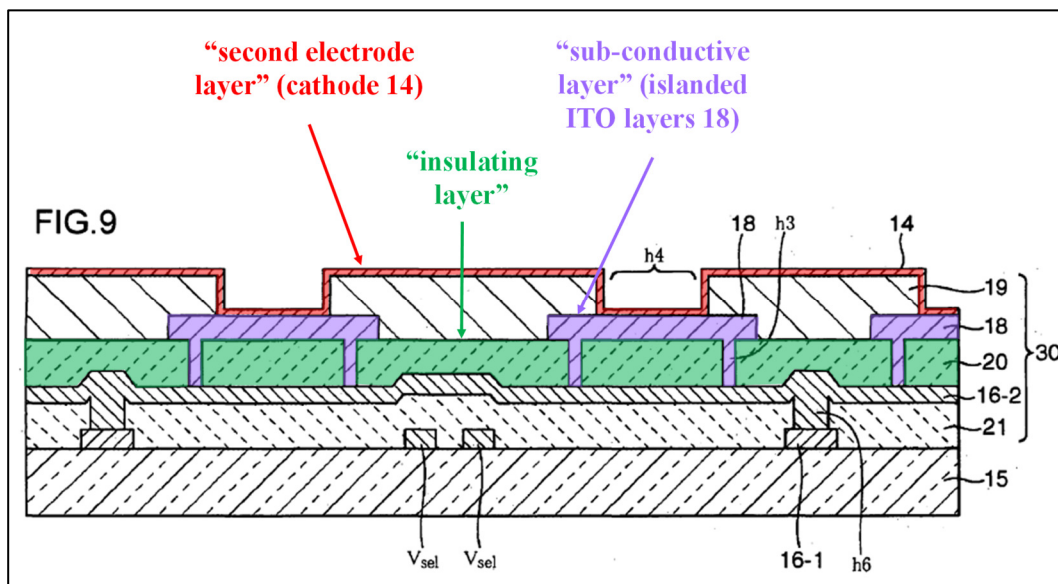
Because forming the EL display panel 100 includes forming each layer of the EL display panel, it would have been obvious that Matsueda’s manufacturing process forming the EL display panel 100 includes forming all of the layers of the EL display panel 100. Thus, Matsueda teaches the preamble of claim 11. (EX1002, ¶¶98.)

2. Elements 11[a]-11[f]

Elements 11[a]-11[f] recite steps for “forming” the structures recited in elements 1[a], 1[c], 1[d], and 1[f], which Matsueda teaches. (*See* claim 1.)

Matsueda teaches a manufacturing process, including all the steps, for forming the structure of the organic EL display panel 100. (*See* 11[pre].) It would have been obvious that this manufacturing process and these steps including forming the structures recited in elements 1[a], 1[c], 1[d], and 1[f]. (EX1002, ¶¶99-111.)

Matsueda also teaches “a first electrode layer on the insulating layer.” For example, Figure 9 (below) shows a cross-sectional view of the wiring area, with the **cathode 14** disposed on the **islanded ITO layers 18**, which is disposed on the **planarizing film 20**. Matsueda discloses that “[t]he organic EL display panel 100 has a bottom-emission structure that emits light through the substrate 15.” (EX1004, [0048].) Matsueda explains that “[o]rganic EL devices are electro-optical devices in which a light-emitting layer having a fluorescent material is interposed between an anode and a cathode.” (EX1004, [0004].) Thus, it would have been obvious that in the display area (not shown in Figure 9), where the pixels are located, the anode / pixel element 17 (“first electrode layer” (see claim 2)) is on the planarizing film 20 (“insulating layer” (see 1[c])). (EX1002, ¶¶104-105.)

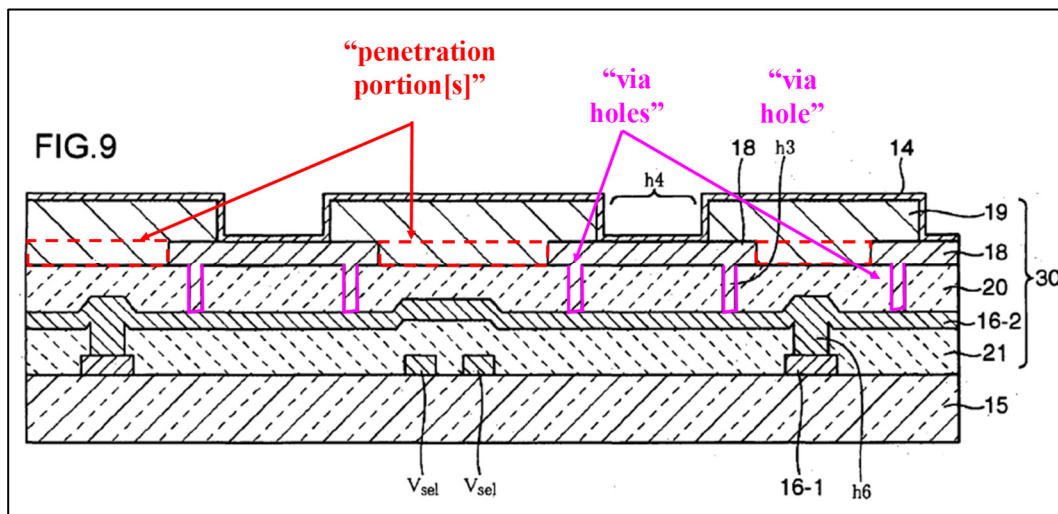


K. Claim 12: “The method of claim 11, wherein forming of the sub-conductive layer is simultaneous with forming the first electrode layer.”

Matsueda teaches the ITO layer 18 (“sub-conductive layer” (*see* 1[d])) comprising the same layer as at least a part of the anode / pixel element 17 (“first electrode layer.” (*See* claim 2). Matsueda also teaches the manufacturing process including steps for forming several layers of the organic EL display panel 100. (*See* 11[pre].) These layers include the ITO layer 18 and the anode / pixel element 17. Thus, Matsueda teaches forming the ITO layer 18 on the same layer as the anode / pixel element 17. Because the ITO layer 18 is formed on the same layer as the anode / pixel element 17, it would have been obvious that Matsueda teaches forming the ITO layer 18 simultaneous with forming the anode / pixel element 17. Further, it would have been obvious to a POSITA to form the anode / pixel element 17 using ITO. Matsueda discloses such teachings in another one of his patents, for example, EX1010 at 5:21-22 discloses “[t]he ITO layer 59 is patterned so as to form a pixel electrode layer (an anode) 59.” As another example, EX1008 discloses “anode (pixel electrode) 23” at 5:57, and describes a pixel electrode made of ITO at 7:10. (EX1002, ¶¶112-113.)

- L. Claim 13: “The method of claim 11, wherein two or more via holes are formed when the via hole is formed, and the penetration portion is formed between the via holes when the penetration portion is formed.”**

Matsueda discloses “[t]he contact holes h3 are formed at multiple positions along the direction in which the auxiliary cathode wiring 16 extends.” (EX1004, [0052].) Figure 9 (below) shows two or more *contact holes h3* (“via hole” (see 1[c])) that are formed on the same layer, which means they are formed at the same time as the other contact hole h3. The *penetration portion* is formed between the *contact holes h3* when the penetration portion is formed, as shown in the figure. (EX1002, ¶¶114-116.)



M. Claim 14

- 1. 14[a]: “The method of claim 11, wherein forming the penetration portion comprises forming two or more penetration portions, and”**

Matsueda teaches a manufacturing process, including all the steps, for forming the structure of the organic EL display panel 100. (*See* 11[pre].) It would have been obvious that this manufacturing process and these steps include forming the structure recited in element 3[a]. (EX1002, ¶¶117-118.)

- 2. 14[b]: “a distance between the penetration portions is less than or equal to a maximum distance between two ends of the first electrode layer.”**

Element 14[b] is similar to element 3[b], which Matsueda teaches. (EX1002, ¶119.)

N. Claim 15

- 1. Elements 15[pre]-15[b], 15[d], and 15[e]**

Elements 15[pre]-15[b], 15[d], and 15[e] are similar to elements 11[pre]-11[b], 11[e], and 11[f], respectively, which Matsueda teaches. (EX1002, ¶¶120-122, 124, 125.)

- 2. 15[c]: “forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”**

Element 15[c] is similar to element 11[c], but element 15[c] also requires the “sub-conductive layer comprising a plurality of unit sub-conductive layers.”

Matsueda teaches element 11[c]. (*See* 11[c].) Additionally, Matsueda teaches the

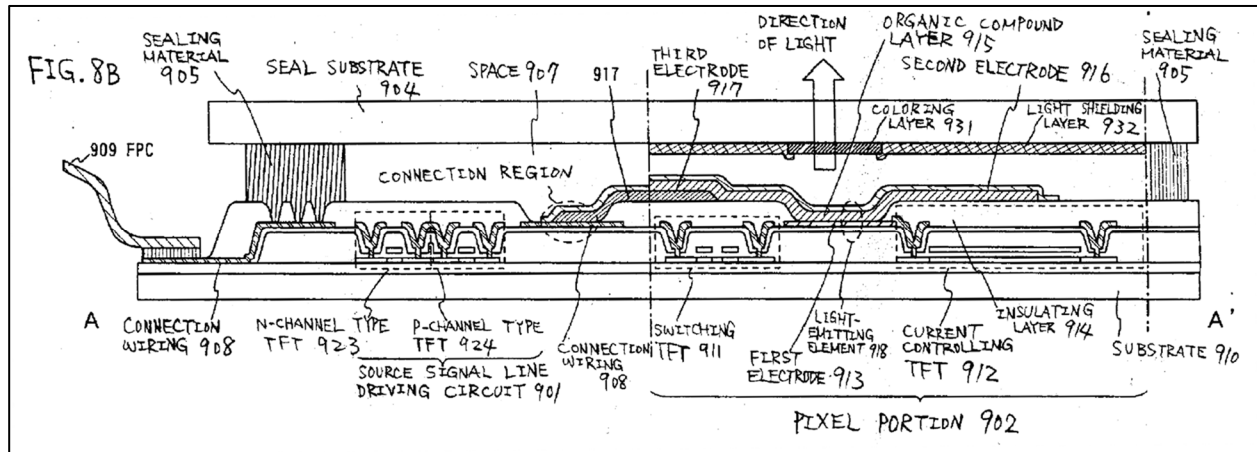
“sub-conductive layer comprising a plurality of unit sub-conductive layers.” (*See* 9[d]; EX1002, ¶123.)

VI. GROUND 2: MATSUEDA AND YAMAZAKI RENDER OBVIOUS CLAIM 7

A. Summary Of Yamazaki

Yamazaki discloses a “light-emitting device [] also referred to as an organic EL display (OELD: Organic EL Display) or organic light-emitting diode (OLED: Organic Light Emitting Diode),” as shown in Figure 8B (below). (EX1005, [0002], [0004].) The Examiner never found, and the Applicant never cited Yamazaki during prosecution.

Yamazaki’s OLED display device comprises “pixel portion 902 is formed by a plurality of pixels each including a switching TFT 911, a current controlling TFT 912, and a first electrode (anode) 913 electrically connected to a drain of the current controlling TFT 912.” (EX1005, [0109].) It also comprises a “second electrode (cathode) 916 [that] functions also as a wiring common to all the pixels and electrically connected to FPC 909 via the connection wiring 908.” (EX1005, [0111]; EX1002, ¶¶126-127.)



B. Claim 7

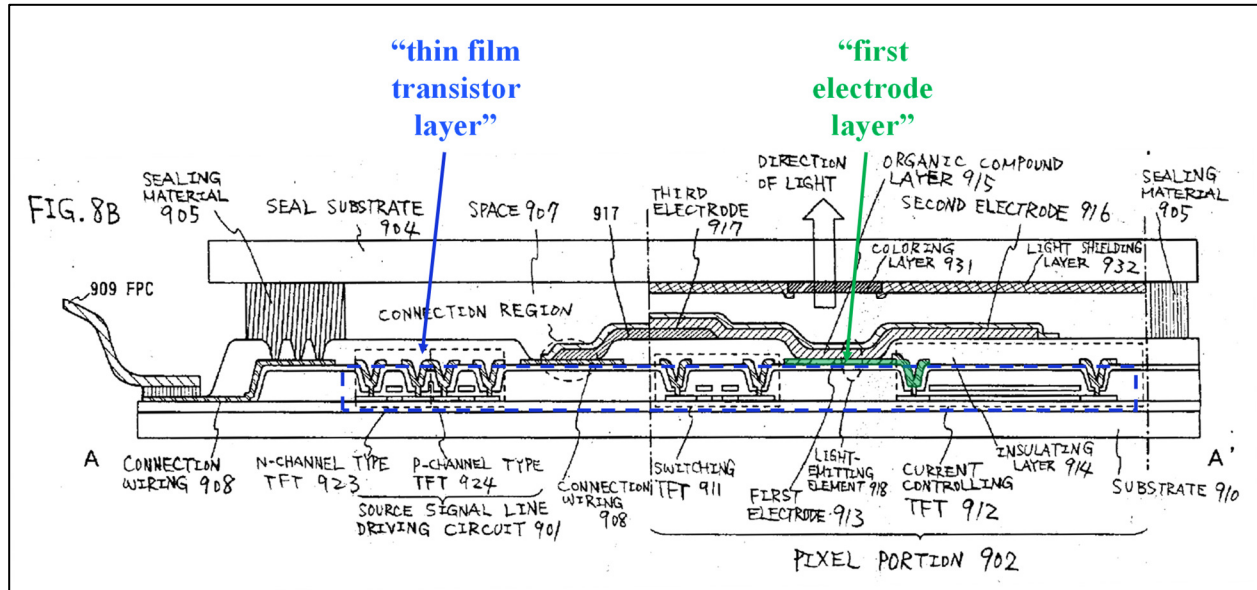
As shown for Ground 1, Matsueda teaches claim 7. To the extent that Matsueda does not teach claim 7, Yamazaki does, and it would have been obvious to combine Matsueda and Yamazaki, as discussed below.

1. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

Yamazaki discloses “the pixel portion 902 is formed by a plurality of pixels each including a switching TFT 911, a current controlling TFT 912, and a first electrode (anode) 913 electrically connected to a drain of the current controlling TFT 912.” (EX1005, [0109].) Figure 8B (below) shows the *layer of the switching TFT 911, current controlling TFT 912, and other TFTs*. Yamazaki also discloses an “insulating layer 914 is formed at both ends of the first electrode (anode) 913 and an organic compound layer 915 is formed on the first electrode (anode) 913.” (EX1005, [0110].) As shown in the figure, the layer of the switching TFT 911,

current controlling TFT 912, and other TFTs are disposed under the **anode 913**.

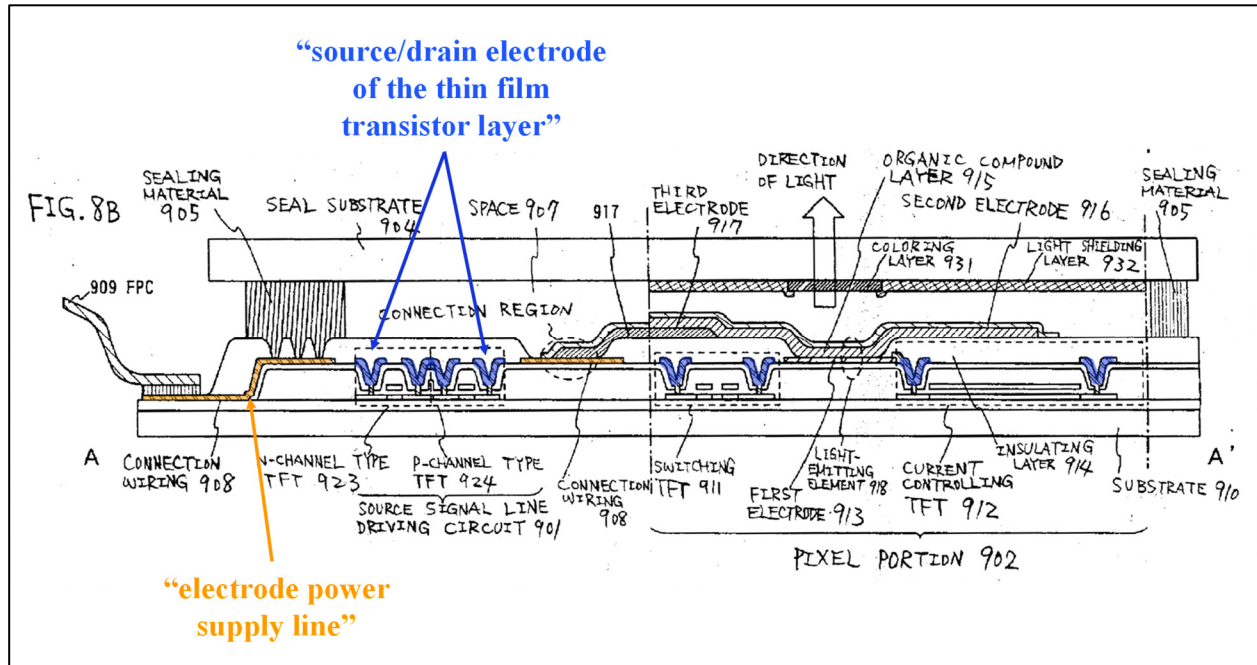
The anode is a “first electrode layer.” (See 1[a]; EX1002, ¶¶128-130.)



2. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”

Yamazaki discloses “reference numeral 908 designates a wiring for transmitting signals inputted to the source signal line driving circuit 901 and the gate signal line driving circuit 903 for receiving a video signal or a clock signal from FPC (flexible printed circuit) 909 for constituting an external input terminal.” (EX1005, [0106].) Thus, connection wiring 908 is an electrode power supply line configured to supply electrical power by transmitting signals from the driving circuits. It supplies electrical power to the cathode 916: “[t]he second electrode (cathode) 916 functions also as a wiring common to all the pixels and electrically connected to FPC 909 via the connection wiring 908.” (EX1005, [0111].) Figure

8B (below) shows the **connection wiring 908** comprises a layer that is the same layer as the **source/drain electrode of the switching TFT 911, current controlling TFT 912, and other TFTs** (“thin film transistor layer”) (see 7[a]). (EX1002, ¶¶131-133.)



It would have been obvious to combine the teachings of Matsueda and Yamazaki. Matsueda and Yamazaki are from the same field of endeavor. They both disclose OLED devices having auxiliary wiring and TFTs. Matsueda discloses reducing the “wiring resistance of the common electrode [that] leads to an increased voltage drop in pixels in the center of the screen” in an OLED display panel 100 by including auxiliary cathode wiring. (EX1004, [0005].) Matsueda explains that the increased voltage drop causes issues with “a gray-scale [that] is not displayed accurately and display performance decreases.” (EX1004, [0005].)

Similarly, Yamazaki discloses “attaining a low-resistance cathode” in an OLED display by including an auxiliary electrode. (EX1005, [0100], [0111].) Thus, Matsueda and Yamazaki are also reasonably pertinent to the same technical problems of lowering the resistance of the cathode to improve the performance of an OLED display. (EX1002, ¶134.)

Matsueda’s OLED display device includes a pixel circuit comprising “a switching transistor Tr1, a driving transistor Tr2, a storage capacitor C, and a light-emitting section OLED.” (EX1004, [0049].) Matsueda also explains that “[e]lectronic devices, such as a transistor, may lie between the first electrode layers and the first power lines in the invention.” (EX1004, [0009].) The ITO layer 18 is also disposed on the source metal layer 22, as shown in Figure 4, which is a source electrode layer of the transistor. (EX1004, [0052].) A POSITA would have been motivated to look to another reference, such as Yamazaki, for such details. Like Yamazaki, Matsueda teaches an auxiliary cathode wiring 16 (“electrode power supply line” (*see* 1[b])) electrically connected to the cathode 14 and configured to supply electrical power to the cathode. (EX1004, [0061], [0064]; EX1002, ¶135.)

Because Matsueda and Yamazaki are both OLED display devices with structures that are similar and both relate to lowering the resistance of the cathode, there would have been a reasonable expectation of success in combining Matsueda and Yamazaki. Both Matsueda and Yamazaki disclose OLED display devices that

include auxiliary wiring connected to the cathode and transistors such as switching transistors and current controlling / driving transistors. Both references apply to top-emission structures. (EX1004, [0048]; EX1005, [0095]-[0096], Fig. 8B.) The prior art successfully demonstrated an OLED structure auxiliary wiring on the same layer as the transistors, and thus, it would have been obvious to combine the teachings of Matsueda and Yamazaki. (EX1002, ¶136.)

VII. GROUND 3: KOYAMA AND NAKANISHI RENDER OBVIOUS CLAIMS 1, 2, 5, 7, 9, 11, 12, AND 15

A. Summary Of Koyama

Koyama discloses “an OLED (Organic Light Emitting Device).” (EX1006, [0002], Title.) The Examiner never found, and the Applicant never cited Koyama during prosecution.

Koyama’s OLED display comprises a pixel portion 101/1201 having a plurality of pixels 104. (EX1006, [0110].) Each pixel has “an independent EL element” comprising a pixel electrode 554, an EL layer 558, and a cathode 559. (EX1006, [0220], [0202]-[0206], Fig. 15C.) Further, “[a]ll pixels have a protective electrode 1207 as an electrode common to the pixels.” (EX1006, [0220]; EX1002, ¶¶137-138.)

“The input/output wiring 1210 is a power supply line for applying a given voltage (ground potential in this embodiment, specifically, 0V) to the protective electrode 1207.” (EX1006, [0222].) “[T]he protective electrode 1207 is connected

to an input/output wiring 1210 through a connecting wiring 1209.” (EX1006, [0222].) Thus, the pixels receive a voltage via connecting wiring 1209 and input/output wiring 1210. (EX1002, ¶139.)

Koyama’s pixel circuit for operating the display device includes “a TFT functioning as a switching element (hereinafter referred to as switching TFT), 302, a TFT functioning as an element for controlling current supplied to an EL element 303 (current controlling element) (hereinafter referred to as current controlling TFT), and 304, a capacitor (storage capacitor).” (EX1006, [0006]; EX1002, ¶139.)

The process of manufacturing the display device includes forming the TFTs on a substrate in the pixel portion, forming an interlayer insulating film 553 on the layer of TFTs to level the surface, forming the pixel electrode 554, forming the EL layer 558, forming the cathode 559, and forming the protective electrode 1207. (EX1006, [0194], [0201], [0203]-[0206], [0220]; EX1002, ¶140.)

Figures 15C, 17B, and 18C (below) show Koyama’s display device, including showing the protective electrode 1207 is connected to the *input/output wiring 1210* through a *connecting wiring 1209*. (EX1002, ¶141.)

Fig. 15C

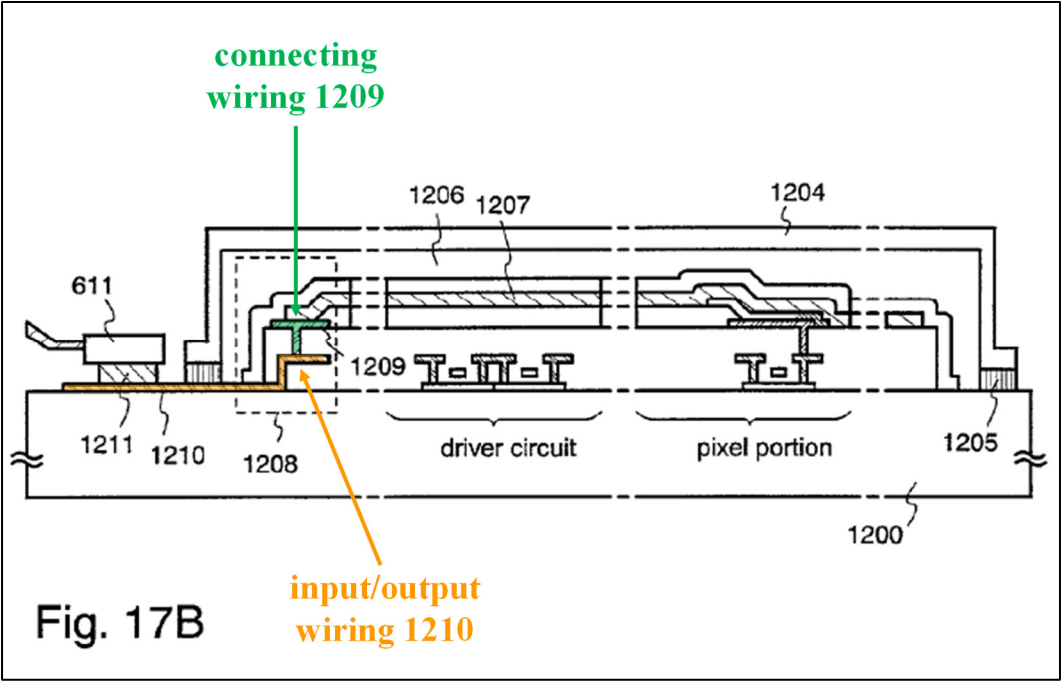
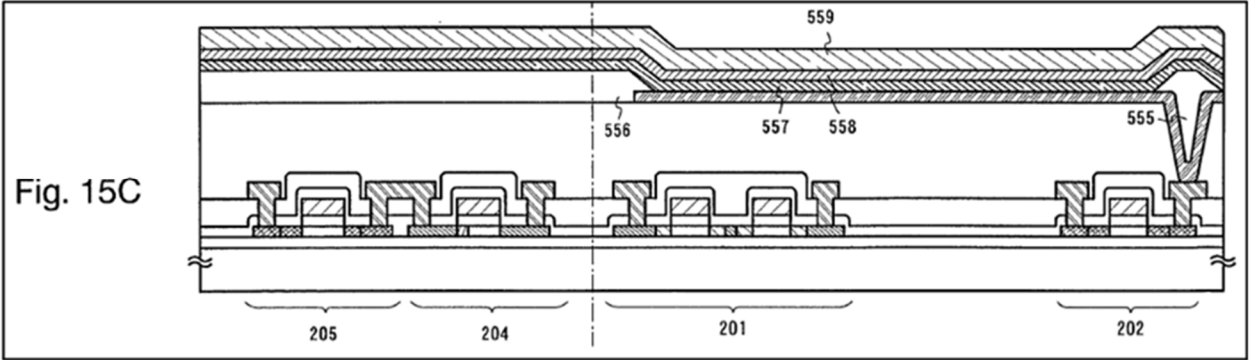
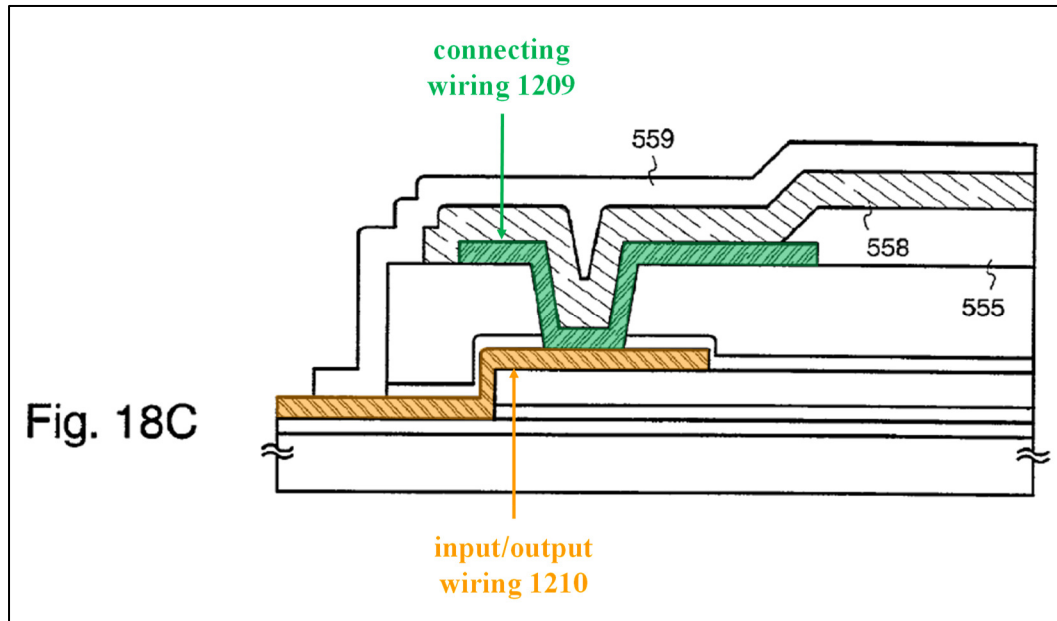


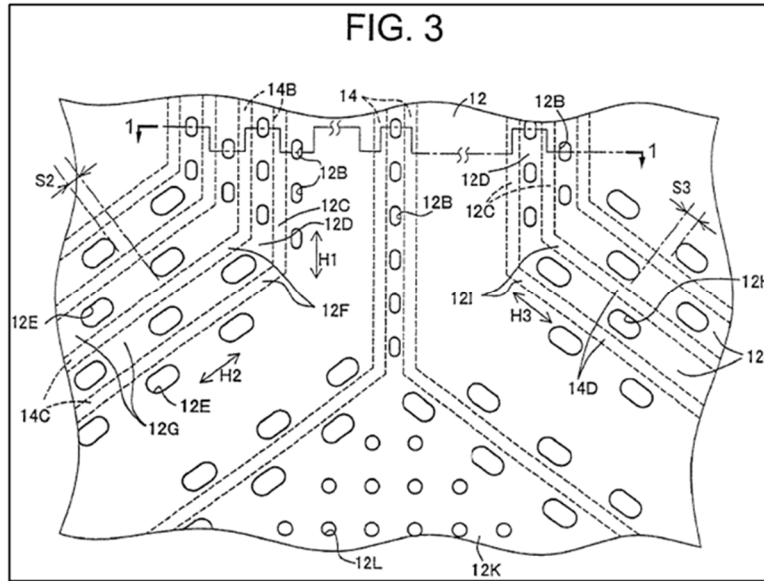
Fig. 17B



B. Summary Of Nakanishi

Nakanishi discloses a wiring substrate comprising a conductive layer 12 on a core substrate 11 “formed from a glass-epoxy-resin composite material.” (EX1007, [0043], Abstract; EX1002, ¶142.) The Examiner never found, and the Applicant never cited Nakanishi during prosecution.

Nakanishi explains that there are applications where a conductor layer is disposed on another layer, such as a dielectric layer or a conductor layer, that release gas. It states that a “conductor layer has poorer gas release properties than a dielectric layer, which is especially important during firing, curing, thermal treatment, and other processes performed during manufacture of the wiring substrate. Therefore, during the course of such treatments or processes, a conductor layer having a large area is likely to hinder diffusion of gas released

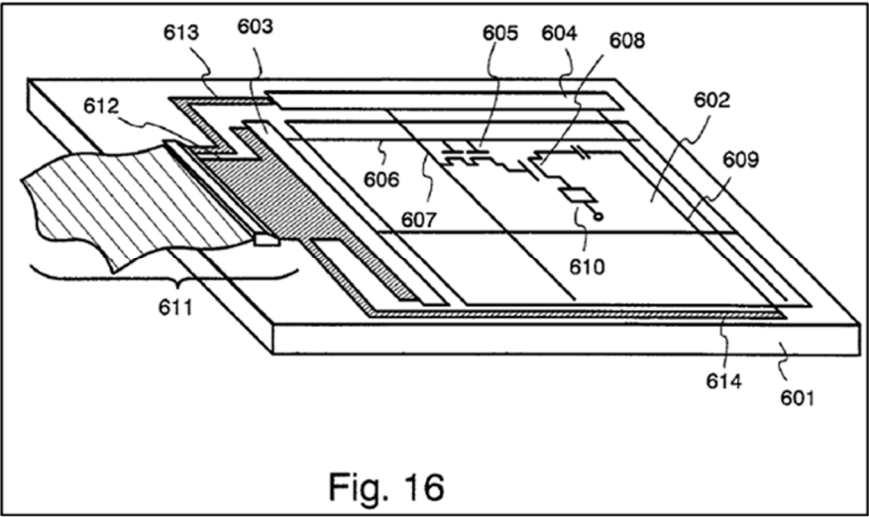
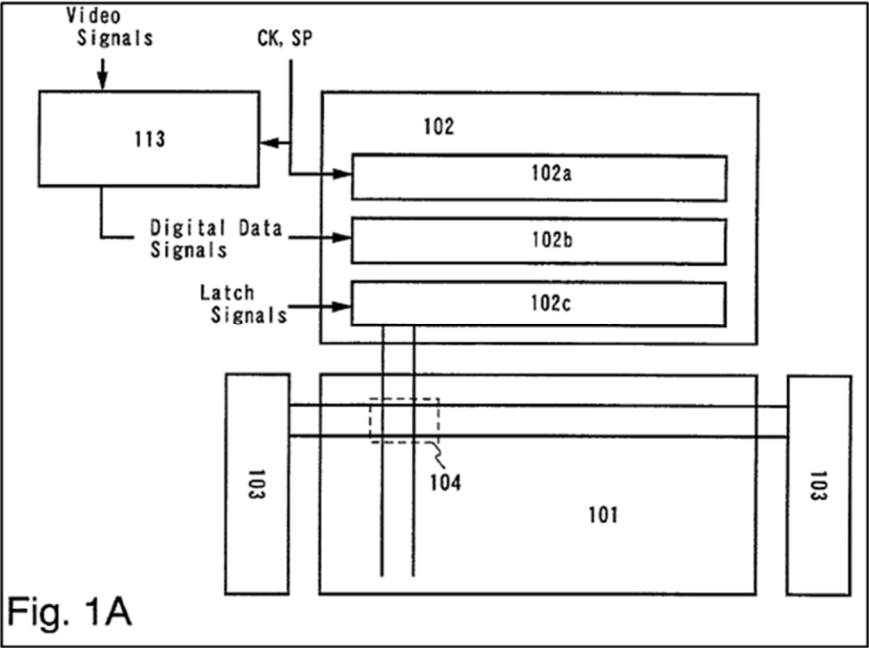


C. Claim 1

1. Preamble: “An electroluminescence display device, comprising:”

To the extent the preamble is limiting (which Petitioner does not concede for this claim or any other claim), Koyama discloses the preamble.

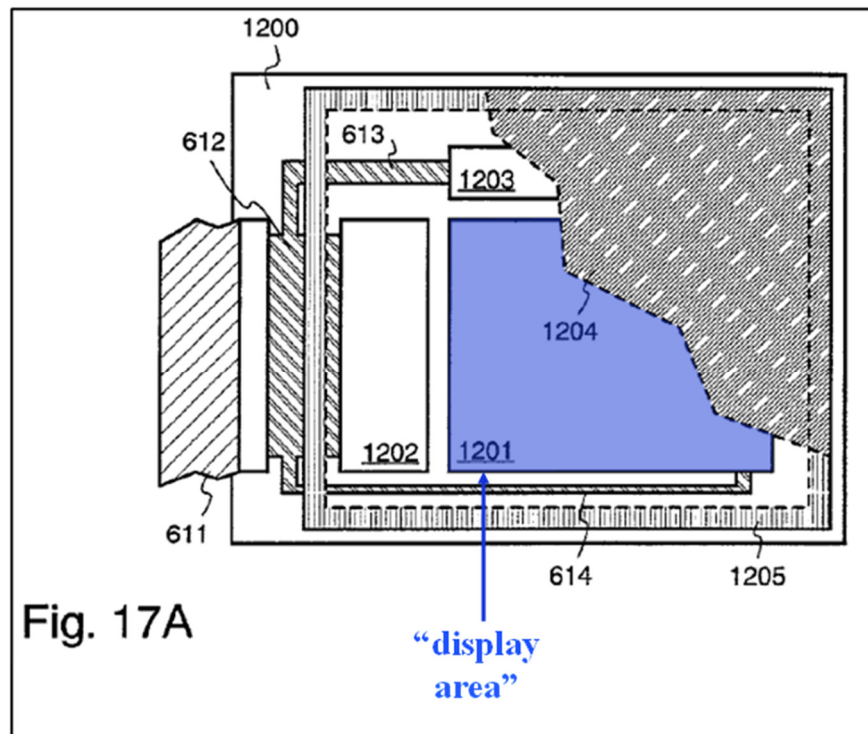
Koyama discloses “a self-luminous device (or *an EL display device*) manufactured by forming a light emitting element (such as an EL (Electro Luminescence) element) on a substrate, and an electric machine having the self-luminous device as a display (display unit). *The light emitting element here is also called an OLED (Organic Light Emitting Device).*” (EX1006, [0002], [0003] (emphasis added).) Figures 1A and 16 (below) show Koyama’s EL display device. (EX1002, ¶¶146-148.)

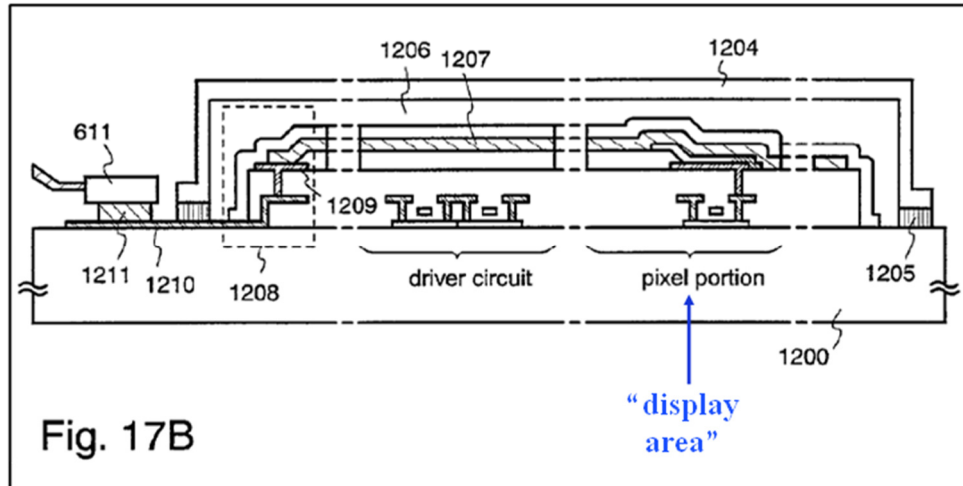


2. 1[a]: “a display area with pixels that have a first electrode layer and a second electrode layer on a substrate and an electroluminescence unit formed between the first electrode layer and the second electrode layer;”

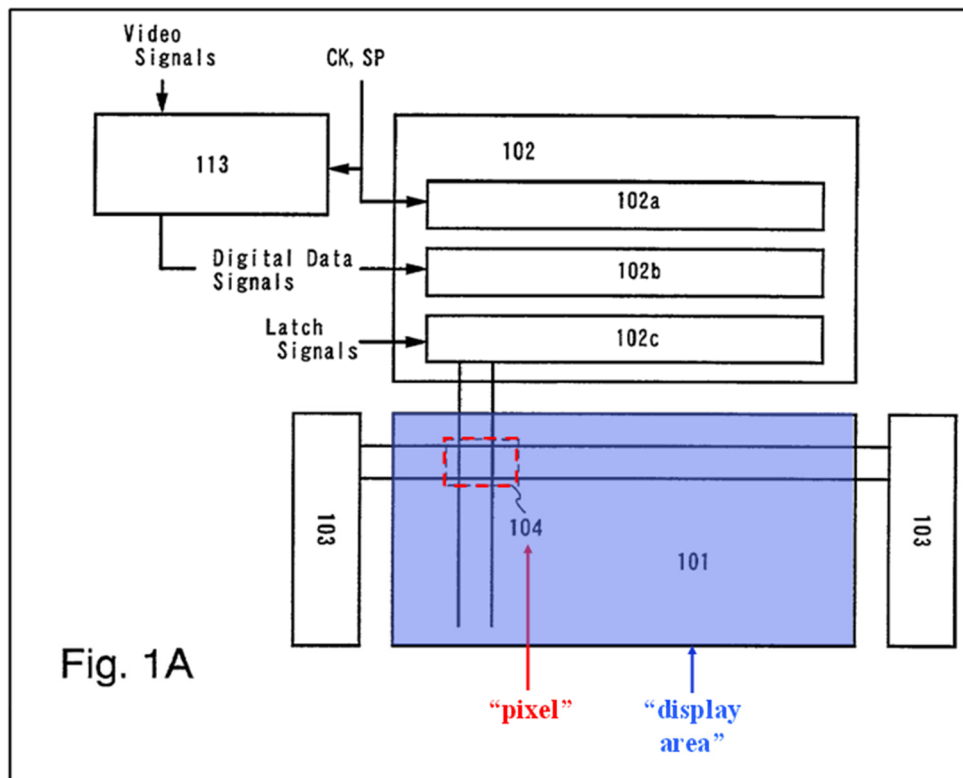
Koyama discloses “[a]s shown in FIG. 17B, the *pixel portion [1201]* is provided with a plurality of pixels each having an independent EL element.”

(EX1006, [0220], Fig. 17A; EX1002, ¶149.)





Koyama also discloses “[t]he pixel portion 101 has a plurality of pixels 104 arranged in a matrix-like manner.” (EX1006, [0100], [0083], [0087], [0210], [0214].) Figure 1A (below) shows the *pixel portion 101* with a *plurality of pixels 104*. (EX1002, ¶150.)



Koyama also discloses an “EL element herein refers to a light emitting element composed of a pixel electrode (anode), an EL layer, and a cathode.” (EX1006, [0134].) It describes the pixel electrode 49 (“first electrode layer”), a cathode 52 (“second electrode layer”), and a “pixel electrode (an anode of the EL element) [49] formed of a conductive oxide film.” (EX1006, [0129].) “An EL layer 51 is formed on the insulating film 50.” (EX1006, [0130].) “A cathode 52 of the EL element is formed on the EL layer 51.” (EX1006, [0133].) Further, “[t]he substrate 11 is a transparent substrate, and typical examples of a transparent substrate usable as the substrate 11 include a glass substrate, a quartz substrate, a glass ceramic substrate and a crystalline glass substrate.” (EX1006, [0109]; EX1002, ¶¶151-152.)

Figure 2 (below) shows the *pixel electrode 49* and *cathode 52* on a *substrate 11*, and the *EL layer 51* formed between the pixel electrode 49 and the cathode 52. (EX1002, ¶153.)

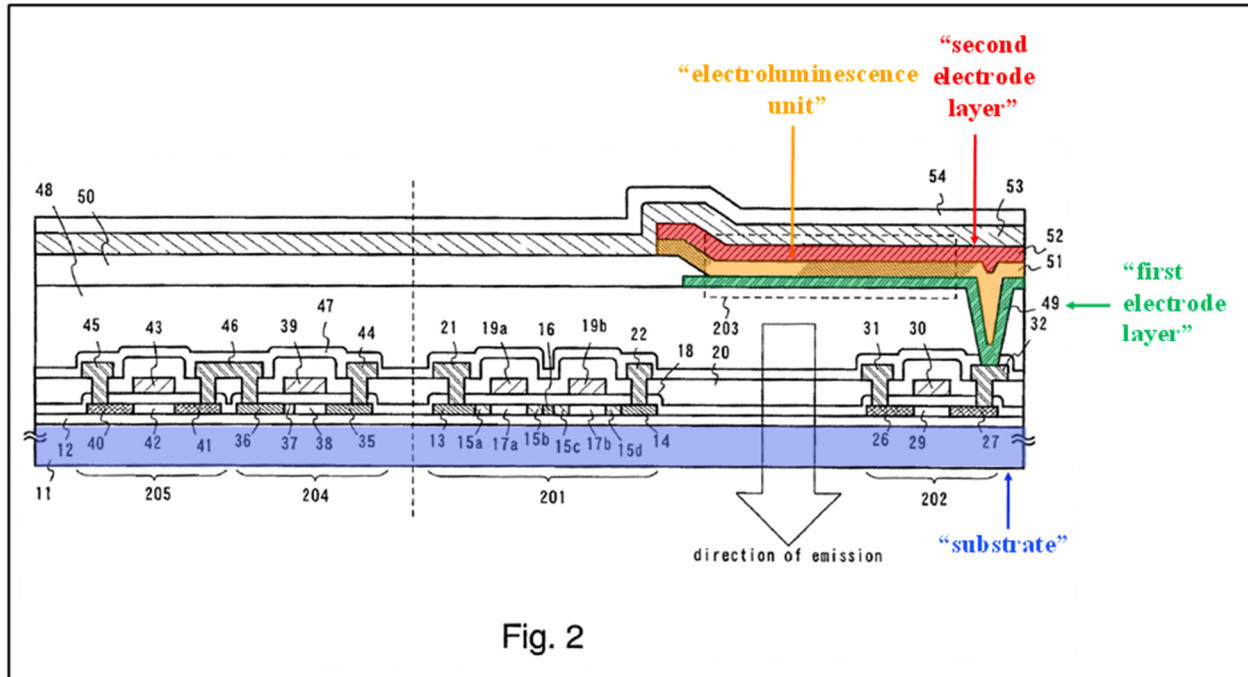
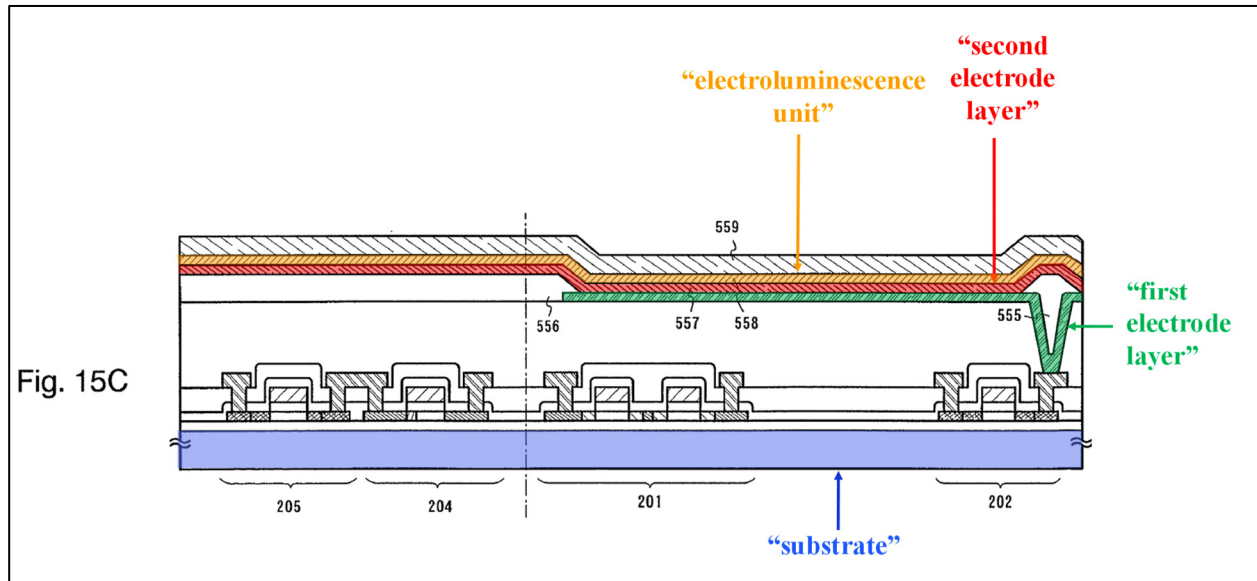


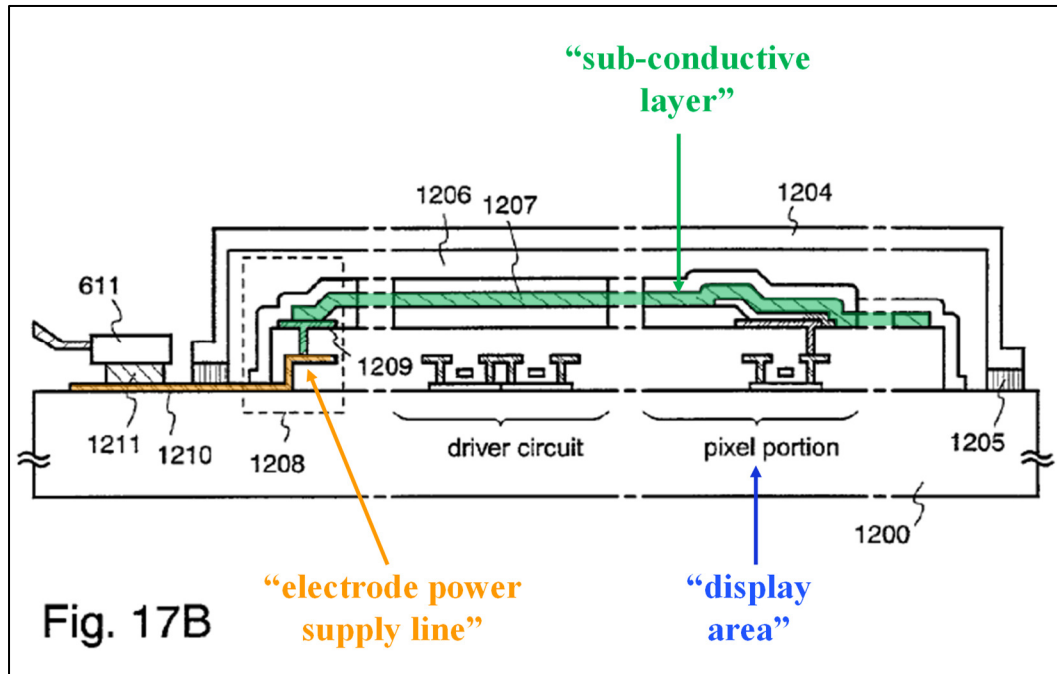
Figure 15C (below) and other passages of Koyama show and describe the *pixel electrode 554* and *cathode 557* on a *substrate 500*, and a *light emitting layer 558* formed between the pixel electrode 554 and the cathode 559. (EX1006, [0173] (“a base film 501 is formed to a thickness of 300 nm on a glass substrate 500”), Fig. 13A, [0202] (“A contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.”), [0204] (“After that, a hole injection layer 557 and a light emitting layer 558 are formed by spin coating.”), [0206] (“Next, a cathode 559 is formed to a thickness of 400 nm from a conductive film having low work function.”); *see also* [0003], [0101]; EX1002, ¶¶154-156.)



3. 1[b]: “an electrode power supply line to supply electrode power to the display area;”

Koyama discloses “input/output wiring 1210 is a power supply line for applying a given voltage (ground potential in this embodiment, specifically, 0V) to the protective electrode 1207.” (EX1006, [0222].) All of the pixels have a protective electrode 1207 as an electrode common to the pixels (EX1006, [0220].) The input/output wiring 1210 is connected to the FPC 611 and also connected to the connecting wiring 1209 and protective electrode 1207, which is in the pixel portion (“display area” (see 1[a])). (EX1006, [0222], Fig. 17A; EX1002, ¶¶157-158.)

Figure 17B (below) shows *input/output wiring 1210* supplying electrode power to the *protective electrode 1207* in the *pixel portion* via *connecting wiring 1209*. (EX1006, [0211], [0212], [0214], [0226], Fig. 16; EX1002, ¶¶159-160.)



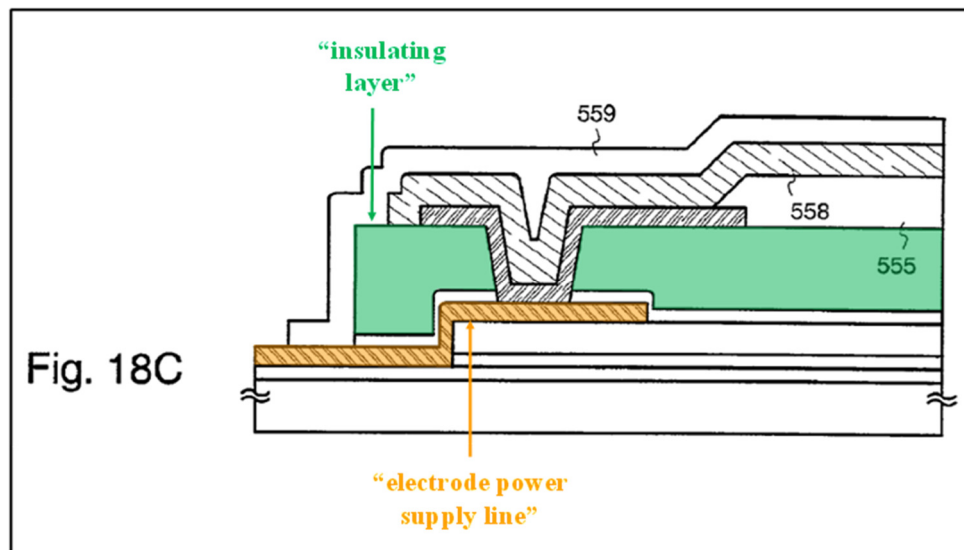
4. 1[c]: “an insulating layer disposed on the electrode power supply line, including a via hole and containing an organic material; and”

Koyama discloses “a second interlayer insulating film 553 is formed from an organic resin as shown in FIG. 15B. Usable organic resins include polyimide, polyamide, acrylic resin, and BCB (benzocyclobutene).” (EX1006, [0201].)

Koyama explains that “[t]he major role of the second interlayer insulating film 553 is leveling, and hence acrylic resin having a superior leveling effect is particularly preferable.” (EX1006, [0201], Fig. 15B.) Koyama also uses reference number 48 to refer to the second interlayer insulating film, and explains that it “has a function of a leveling film for leveling a level difference caused by the TFTs,” “is an organic resin film, such as a polyimide film, a polyamide film, an acrylic film, or a BCB (benzocyclobutene) film,” and further explains that “these organic resin films

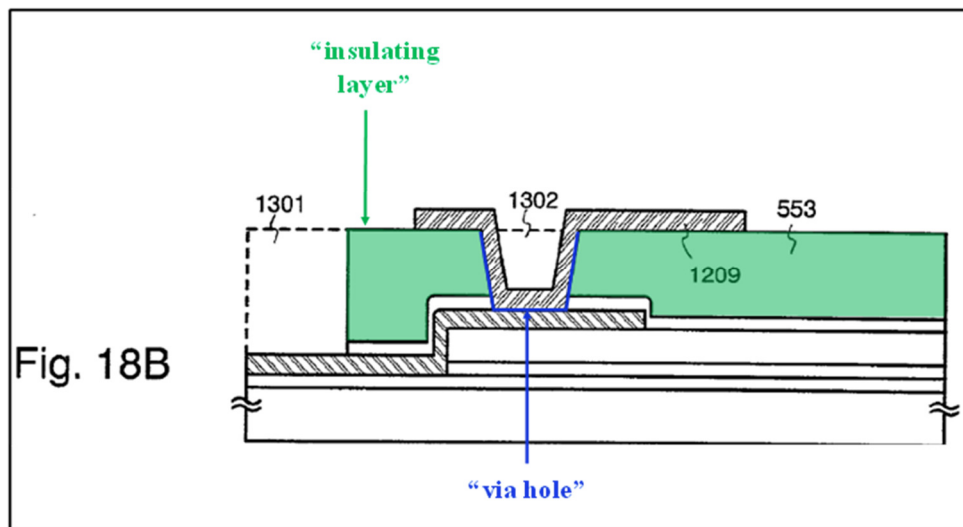
are advantageous in that they are easy to form a very flat surface and relative dielectric constant thereof is low. An EL layer is extremely sensitive to unevenness, and the level difference caused by the TFTs is desired to be absorbed almost completely by the second interlayer insulating film.” (EX1006, [0128].) Thus, Koyama teaches interlayer insulating film 553/48 (“insulating layer”) containing an organic material. (EX1002, ¶¶161-164.)

The *interlayer insulating film 553* is disposed on the *input/output wiring 1210* (“electrode power supply line” (*see* 1[b])) as explained in [0224] and shown in Figure 18C (below). (EX1002, ¶¶164-165.)



Koyama also discloses “[a] contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.” (EX1006, [0202], Fig. 15B.) “[T]he second interlayer insulating film 553 in FIG. 15B is partially etched. The connection

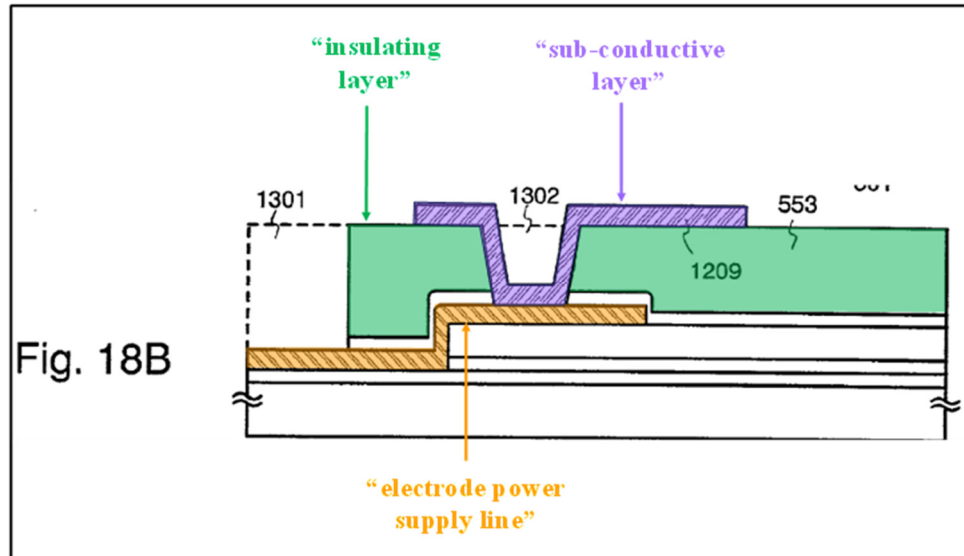
wiring 1209 is formed on an opening 1302 to obtain the structure shown in FIG. 18B.” (EX1006, [0225].) The via hole is an opening that allows the connecting wiring 1209 to electrically connect to input/output wiring 1210 (shown in Figure 18C above). Thus, the *interlayer insulating film 553* includes a *via hole*, as shown in Figure 18B (below). (EX1002, ¶¶167-168.)



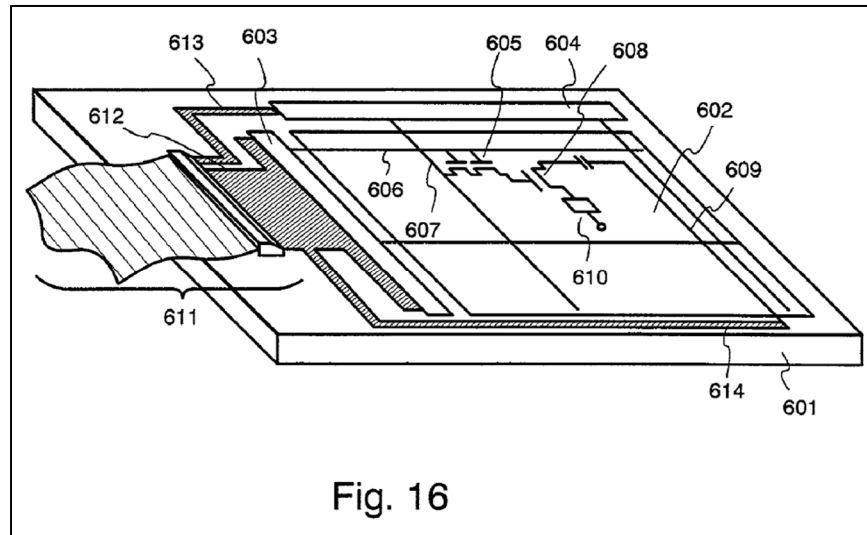
5. 1[d]: “a sub-conductive layer formed on the insulating layer including the via hole along the electrode power supply line,”

Koyama discloses a connecting wiring 1209. Figure 18B (below) shows the *connecting wiring 1209* formed on the *interlayer insulating film 553* (“insulating layer” (see 1[c])) and along the *input/output wiring 1210* (“electrode power supply line” (see 1[a])). Koyama also discloses “the second interlayer insulating film 553 in FIG. 15B is partially etched. The connecting wiring 1209 is formed on an

opening 1302 to obtain the structure shown in FIG. 18B.” (EX1006, [0225]; EX1002, ¶¶168-170.)



Koyama explains that “FPC 611 serving as an external input/output terminal is provided with input/output wirings (connection wirings) 612 and 613 for transmitting signals to the driver circuits, and *an input/output wiring 614 connected to the power supply line 609.*” (EX1006, [0212].) A POSITA would have understood power supply line 609 is similar to connecting wiring 1209, and input/output wiring 614 is similar to input/output wiring 1210. Figure 16 (below) shows the power supply line 609 extending along the input/output wiring 614. It would have been obvious that the connecting wiring 1209 is formed along the input/output wiring 1210. (EX1002, ¶¶171-173.)

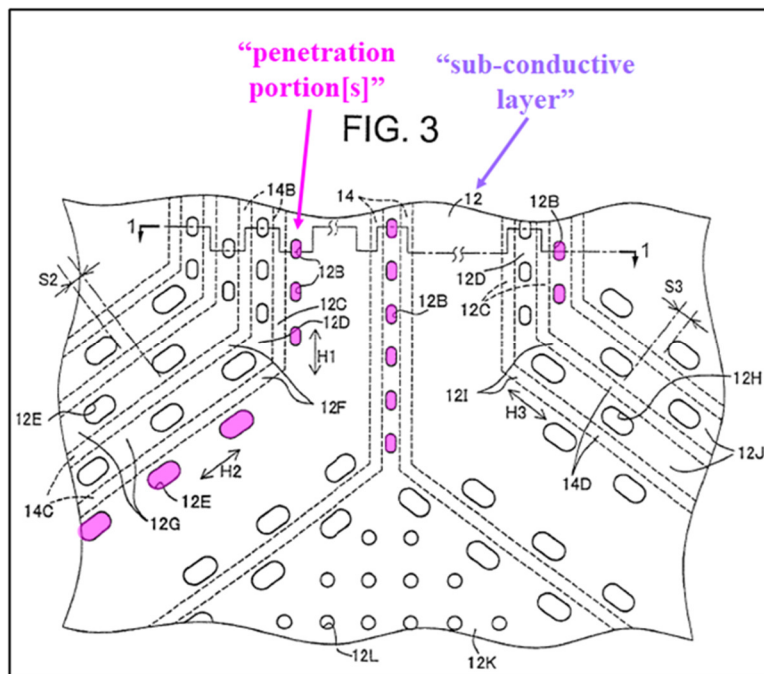
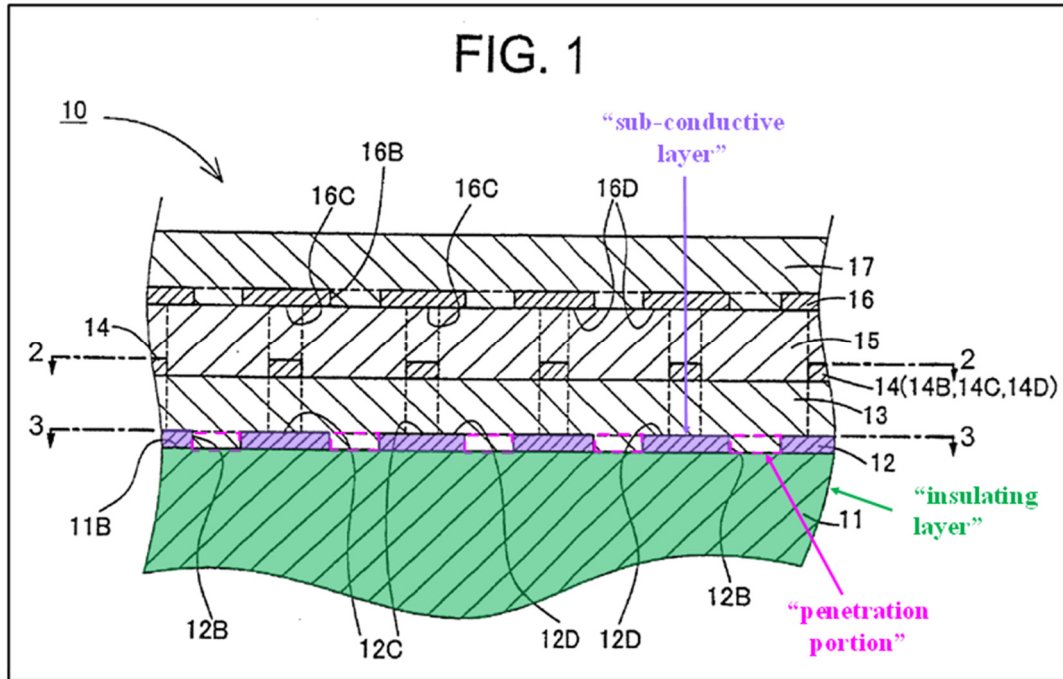


6. 1[e]: “wherein the electrode power supply line and the second electrode layer are coupled to each other at the via hole through the sub-conductive layer, and”

Koyama discloses input/output wiring 1210 (“electrode power supply line” (*see* 1[b])) and a cathode 52/559 (“second electrode layer” (*see* 1[a])) coupled to each other: “[i]n a region denoted by 1208, the protective electrode 1207 is connected to an input/output wiring 1210 through a connecting wiring 1209 that is formed of the same material as the pixel electrode.” (EX1006, [0222].) And they are coupled to each other through connecting wiring 1209 (“sub-conductive layer” (*see* 1[d])). “The protective electrode 558 is thus electrically connected to the input/output wiring 1210 through the connection wiring 1209.” (EX1006, [0226]; EX1002, ¶¶174-175.)

7. 1[f]: “the sub-conductive layer on the insulating layer includes a penetration portion.”

Nakanishi discloses a first conductor layer 12 on a “core substrate [11] formed from a glass-epoxy-resin composite material and has a thickness of about 600 um.” (EX1007, [0043].) Epoxy-resin is an insulating layer that contains an organic material, and thus, the core substrate 11 is also an insulating layer that contains an organic material. Nakanishi also discloses “first conductor layer 12 is a solid conductor layer and has a number of through holes 12B, 12E, 12H, and 12L formed therein. The through holes 12B are formed to directly connect the core substrate 11 and the first dielectric layer 13 therethrough, thereby enhancing the strength of the wiring substrate 10.” (EX1007, [0049].) Figures 1 and 3 (below) show the *conductor layer 12* on the *core substrate 11* and including *through holes 12B, 12E, 12H, and 12L* (“penetration portion”). (EX1002, ¶¶177-178.)



It would have been obvious to combine the teachings of Koyama and Nakanishi. Koyama and Nakanishi are from the same field of endeavor. They both disclose conductor layers on insulating layers containing an organic material.

Koyama discloses a connecting wiring 1209 on an interlayer insulating film 553 containing an organic resin. (EX1006, [0201], [0225], Fig. 18B.) Nakanishi similarly discloses a conductor layer 12 on a core substrate 11 that also contains an organic resin. (EX1007, [0043], [0049], Fig. 1.) Thus, they both have the same structure (conductor layers on insulating layers containing an organic material) and same function (transmitting signals via a conductor layer on top of an organic insulating layer). Both of the devices of Koyama and Nakanishi are subjected to heat during the manufacturing process. Koyama describes “[h]eat treatment is then given to the film in atmosphere containing 3% of hydrogen at 300 to 450° C. for one to four hours to hydrogenate the film. This step is for hydrogen termination of dangling bonds of the semiconductor using hydrogen that is thermally excited. Other hydrogenation measures include plasma hydrogenation (using plasma-excited hydrogen).” (EX1006, [0198].) A POSITA would have known that the heat treatment may lead to issues such as “a conductor layer . . . hinder[ing] diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer.” (EX1007, [0006].) Koyama describes a “protective electrode 53 expectedly provides a heat releasing effect to alleviate heat generated from the EL layer.” (EX1006, [0137].) Koyama and Nakanishi are reasonably pertinent to the same technical problems of improving

the manufacturing and quality of devices that have conductor layers on organic insulating layers, which are subjected to heat during the manufacturing process. (EX1002, ¶¶179-181.)

Nakanishi solves the problem by using “conventional wisdom [of] . . . provid[ing] a conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) Thus, Nakanishi teaches adding through holes in the conductor layer to maintain the bonding strength of the conductor layer with the dielectric layer and preventing the generation of blisters caused by the conductor layer having poor gas release properties. These technical features may be combined with the teachings of Koyama to generate an OLED device with better reliability and performance. Nakanishi thus improves upon Koyama. Like Nakanishi, Koyama teaches a connecting wiring 1209 (sub-conductive layer) on the interlayer insulating film 553 (insulating layer). Given that the prior art has already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. (EX1002, ¶¶181-182.)

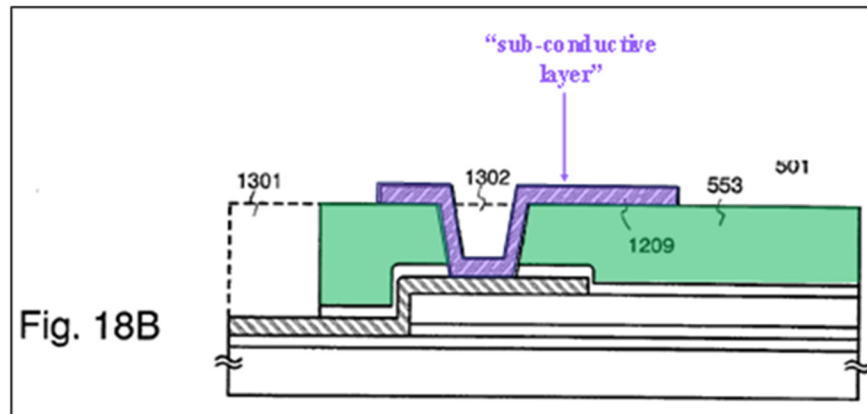
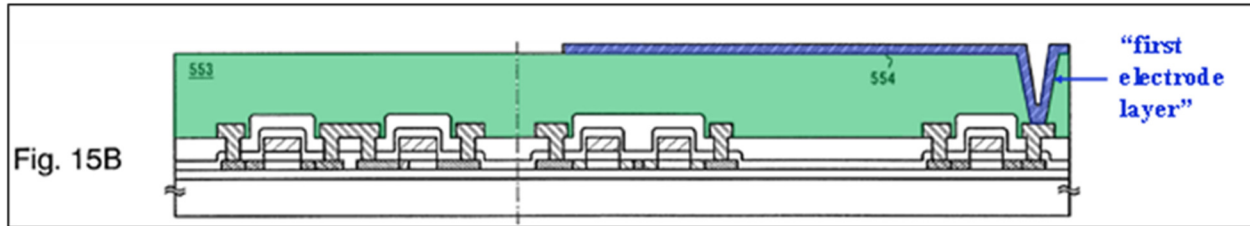
Because Koyama and Nakanishi both relate to conductive layers on organic insulating layers and devices that are subjected to heat treatment during the manufacturing process, a POSITA would be motivated to use the techniques taught

by Nakanishi to improve the similar device of Koyama in the same way. The result would be Koyama's OLED device with improved reliability due to the inclusion of through holes that allow the diffusion of gas released from the underlying dielectric layer. As Nakanishi stated, such techniques were known and part of "conventional wisdom." Thus, it would have been obvious to a POSITA to combine the teachings of Koyama and Nakanishi. (EX1002, ¶¶181-182.)

D. Claim 2: "The device of claim 1, wherein the sub-conductive layer comprises the same layer as at least a part of the first electrode layer."

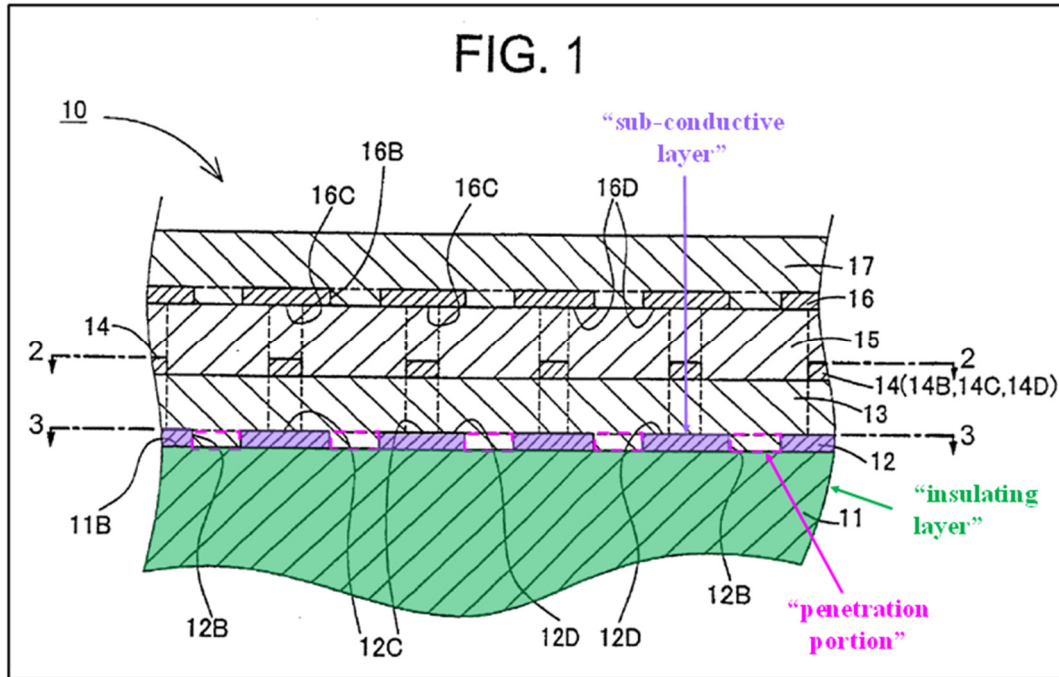
Koyama teaches connecting wiring 1209 ("sub-conductive layer" (*see* 1[d])) and anode / pixel electrode 49/554 ("first electrode layer" (*see* 1[a])) and discloses "[t]he connection wiring 1209 and the pixel electrode 554 in FIG. 15B are simultaneously formed. (FIG. 18B)." (EX1006, [0225].) A POSITA would have understood the connecting wiring 1209 and pixel electrode 554 being simultaneously formed means they are on the same layer. (EX1006, Figs. 17B, 18B; EX1002, ¶¶183-184.)

Figures 15B and 18B (below) show that *pixel electrode 554* is formed on top of the *interlayer insulating film 553*, and *connecting wiring 1209* is also formed on top of the *interlayer insulating film 553*. Thus, the connecting wiring 1209 comprises the same layer as at least a part of the pixel electrode 554. (EX1002, ¶185.)



E. Claim 5: “The device of claim 1, wherein the penetration portion comprises a penetration hole.”

Nakanishi discloses through holes 12B, 12E, 12H, and 12L (“penetration portion” (*see* 1[f])). It discloses “[t]he through holes 12B are formed to directly connect the core substrate 11 and the first dielectric layer 13 therethrough, thereby enhancing the strength of the wiring substrate 10.” (EX1007, [0049], [0044].) A POSITA would have understood that the through hole formed to directly connect the *core substrate 11* and first dielectric layer 13 means the *through hole* is a penetration hole that penetrates through the *conductor layer 12* (“sub conductive layer” (*see* 1[d])), as shown in Figure 1 (below). (EX1002, ¶¶186-188.)



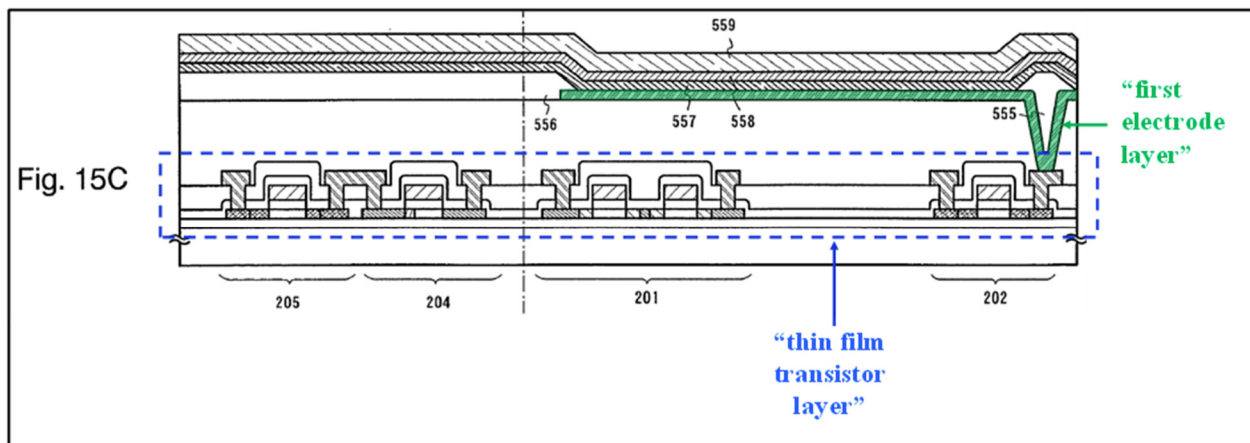
F. Claim 7

1. 7[a]: “The device of claim 1, wherein a thin film transistor layer is disposed under the first electrode layer, and”

Koyama discloses a thin film transistor layer comprising a switching TFT 201 and a current controlling TFT 202. Koyama explains that “[t]he switching TFT 201 is formed to have: an active layer including a source region 13, a drain region 14, LDD regions 15a to 15d, a separate region 16, and channel forming regions 17a and 17b; gate insulating films 18; gate electrodes 19a and 19b, a first interlayer insulating film 20; a source wiring 21; and a drain wiring 22.” (EX1006, [0114], [0230].) “The current controlling TFT 202 is formed to have a source region 26, a drain region 27, a channel forming region 29, a gate insulating film 18,

a gate electrode 30, the first interlayer insulating film 20, a source wiring 31, and a drain wiring 32.” (EX1006, [0119]; EX1002, ¶¶189-191.)

Figure 15C (below) shows the *layer of the switching TFT 201 and current controlling TFT 202* is disposed under the *pixel electrode 554* (“first electrode layer” (see 1[a])). (EX1002, ¶192.)

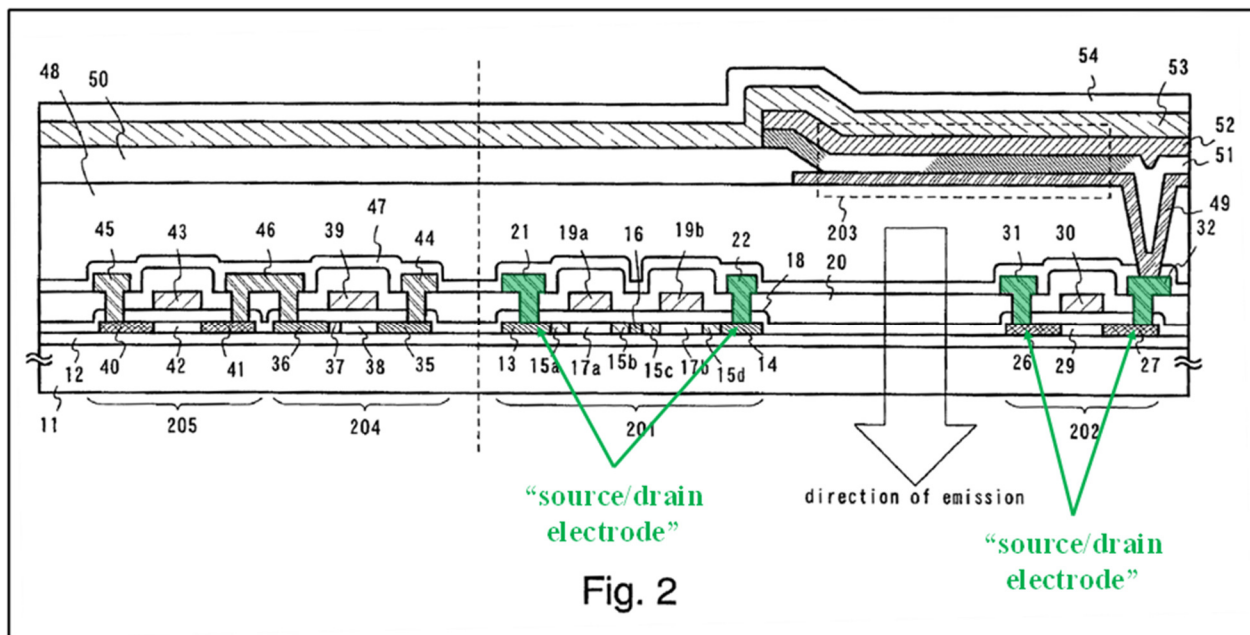


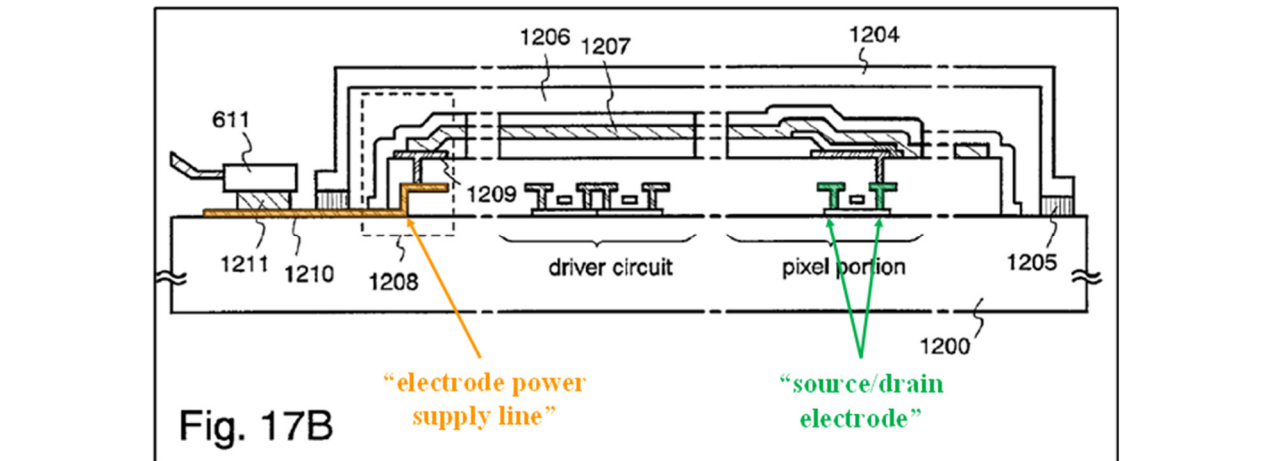
2. 7[b]: “the electrode power supply line comprises a layer that is the same layer as a source/drain electrode of the thin film transistor layer.”

Koyama teaches input/output wiring 1210 (“electrode power supply line” (see 1[b])), and a layer (including the source / drain electrodes) of the switching TFT 201 and the current controlling TFT 202 (“thin film transistor layer” (see 7[b])). Koyama discloses “the input/output wiring 1210, and the source wiring and the drain wiring of FIG. 15A [(below)] are formed simultaneously. (FIG. 18A [(below)]).” (EX1006, [0224].) A POSITA would have understood that the source wiring and the drain wiring include source and drain electrodes. Because the

input/output wiring 1210 is formed at the same time as the source wiring and drain wiring, the input/output wiring 1210 comprises a layer that is the same layer as a source / drain electrode of the thin film transistor layer. (EX1002, ¶¶193-194.)

Figures 2 and 17B (below) show the *source wiring 21 and drain wiring 22* (switching TFT 201) and *source wiring 31 and drain wiring 32* (current controlling TFT 202) are located on the same level as *input/output wiring 1210*. Koyama explains that “[t]he switching TFT 201 is formed to have: an active layer including a source region 13, a drain region 14, . . . a source wiring 21; and a drain wiring 22.” (EX1006, [0114].) Further, “[t]he current controlling TFT 202 is formed to have a source region 26, a drain region 27, . . . a source wiring 31, and a drain wiring 32.” (EX1006, [0119]; EX1002, ¶195.)





G. Claim 9

1. Elements 9[pre]-9[c] and 9[e]

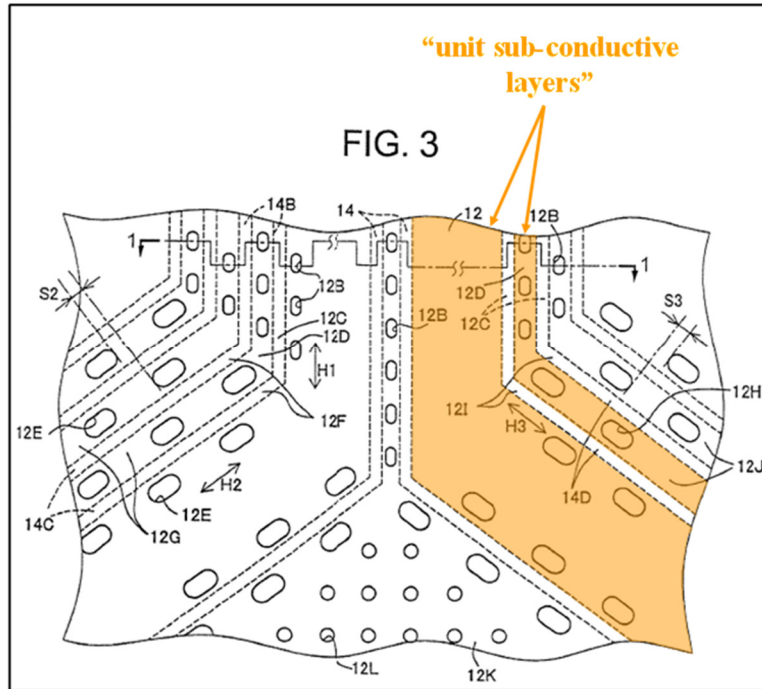
Elements 9[pre]-9[c] and 9[e] are similar to elements 1[pre]-1[c] and 1[e], respectively, which Koyama and Nakanishi teach. (EX1002, ¶¶196-199, 203.)

2. **9[d]: “a sub-conductive layer comprising a plurality of unit sub-conductive layers formed on the insulating layer including the via hole along the electrode power supply line,”**

Nakanishi discloses “the first conductor layer 12 is divided into (1) a wiring correspondence region, which corresponds to the signal wiring layers 14 as projected thereon along the thickness direction (i.e., perpendicular to the drawing sheet), and (2) a remaining wiring noncorrespondence region.” (EX1007, [0051].) Nakanishi explains the “conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) The “wiring noncorrespondence region [] is the remaining portion of the

9[d])). The conductive layer 12 is on the core substrate 11 (“insulating layer” (*see* 1[f])). A POSITA would have understood that the conductive layer 12 comprising parallel-wiring-gap noncorrespondence regions and being on the core substrate 11 would mean the parallel-wiring-gap correspondence regions are on the core substrate 11. (EX1002, ¶204.)

Nakanishi discloses “[t]he conductor layer includes (1) a plurality of wiring correspondence regions corresponding to the plurality of signal wiring layers as projected onto the conductor layer in the thickness direction of the conductor layer, and (2) a wiring noncorrespondence region, which is the remaining portion of the conductor layer after removal of the wiring correspondence regions.” (EX1007, [0019].) A POSITA would have understood that the wiring noncorrespondence regions being separated from the wiring noncorrespondence regions means the *wiring noncorrespondence regions* (“unit sub-conductive layers”) are separated from each other, as shown in Figure 3 (below). (EX1002, ¶¶205-206.)



H. Claim 11

1. Preamble: “A method of manufacturing an electroluminescence display device, comprising:”

To the extent the preamble is limiting (which Petitioner does not concede for this claim or any other claim), Koyama discloses the preamble.

Koyama discloses “a self-luminous device (or *an EL display device*) manufactured by forming a light emitting element (such as an EL (Electro Luminescence) element) on a substrate, and an electric machine having the self-luminous device as a display (display unit). *The light emitting element here is also called an OLED (Organic Light Emitting Device).*” (EX1006, [0002], [0003] (emphasis added); *see* claim 1.) Koyama also describes the “process of manufacturing the self-luminous device” including the steps for forming the layers

of the EL display device, as shown in Figures 15A-15C and Figures 18A-18C, for example. (EX1006, [0224]-[0227]; EX1002, ¶¶207-208.)

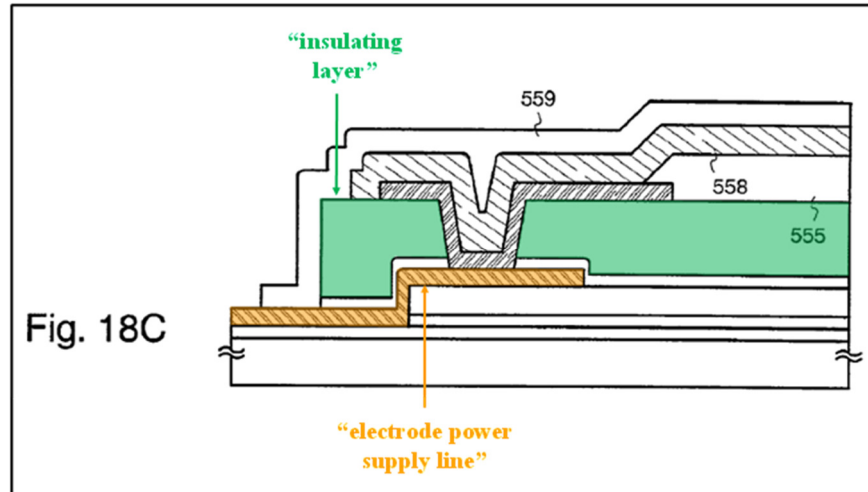
2. Elements 11[a]-11[f]

Elements 11[a]-11[f] recite steps for “forming” the structures recited in elements 1[a], 1[c], 1[d], and 1[f], which Koyama and Nakanishi teach. (See claim 1.) Because the presence of the structures requires “forming” them, Koyama and Nakanishi teach elements 11[a]-11[f]. (EX1002, ¶¶209-221.)

Koyama also teaches the “process of manufacturing the self-luminous device” including steps for forming the layers of the organic EL display panel. (See 11[pre].) Koyama’s figures show that it teaches elements 11[a]-11[f].

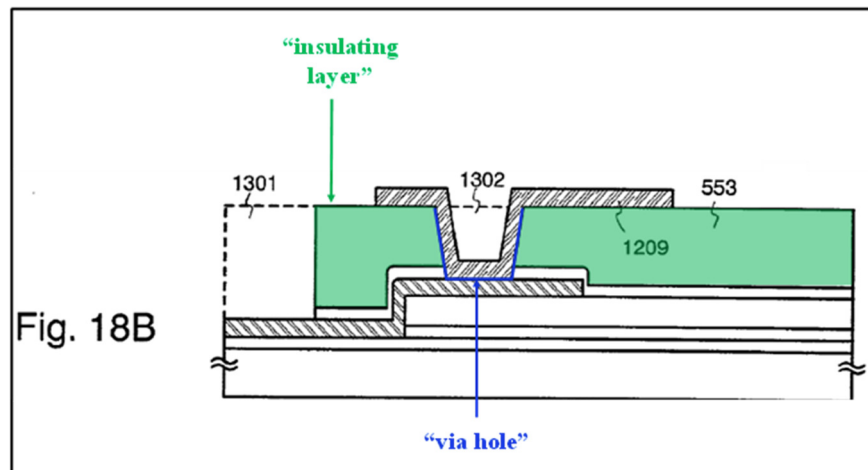
- **11[a]: “forming an insulating layer including an organic material on an electrode power supply line;”**

Figure 18C (below) shows forming *interlayer insulating film 553* (“insulating layer” (see 1[c])) on the *input/output wiring 1210* (“electrode power supply line” (see 1[b])). (EX1002, ¶¶209-210.)



- 11[b]: “forming a via hole on the insulating layer;”

Figure 18B (below) shows forming a *via hole* on the *interlayer insulating film 553* (“insulating layer” (see 1[c])). (EX1002, ¶¶211-212.)



- 11[c]: “forming a sub-conductive layer and a first electrode layer on the insulating layer including the via hole;”

Figure 18B (below) shows forming *connecting wiring 1209* (“sub-conductive layer” (see 1[d])) on the *interlayer insulating film 553* (“insulating layer” (see 1[c])) including the *via hole*. (EX1002, ¶¶213-214.)

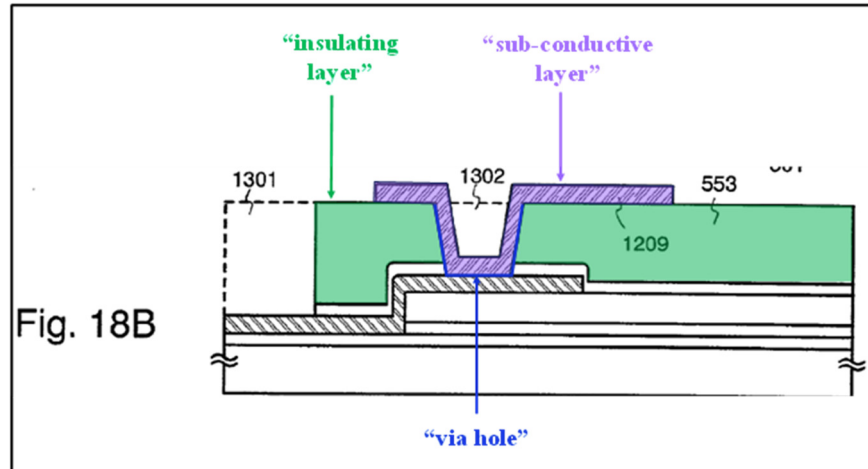
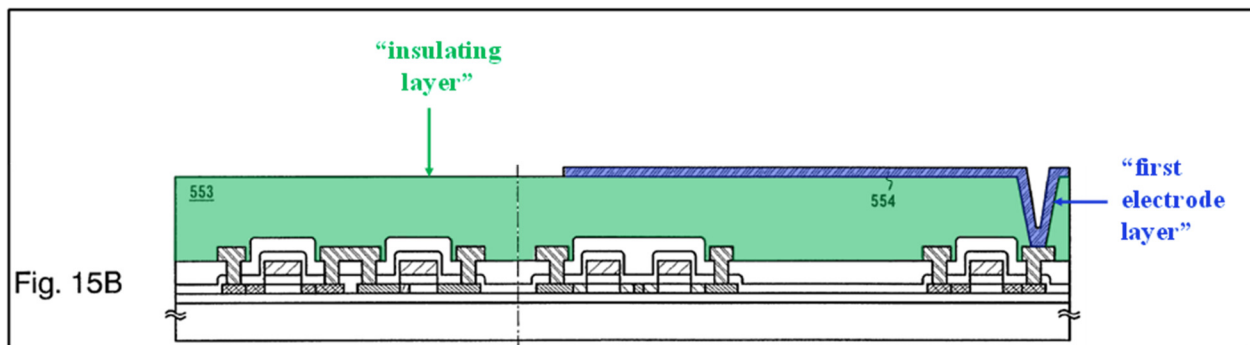


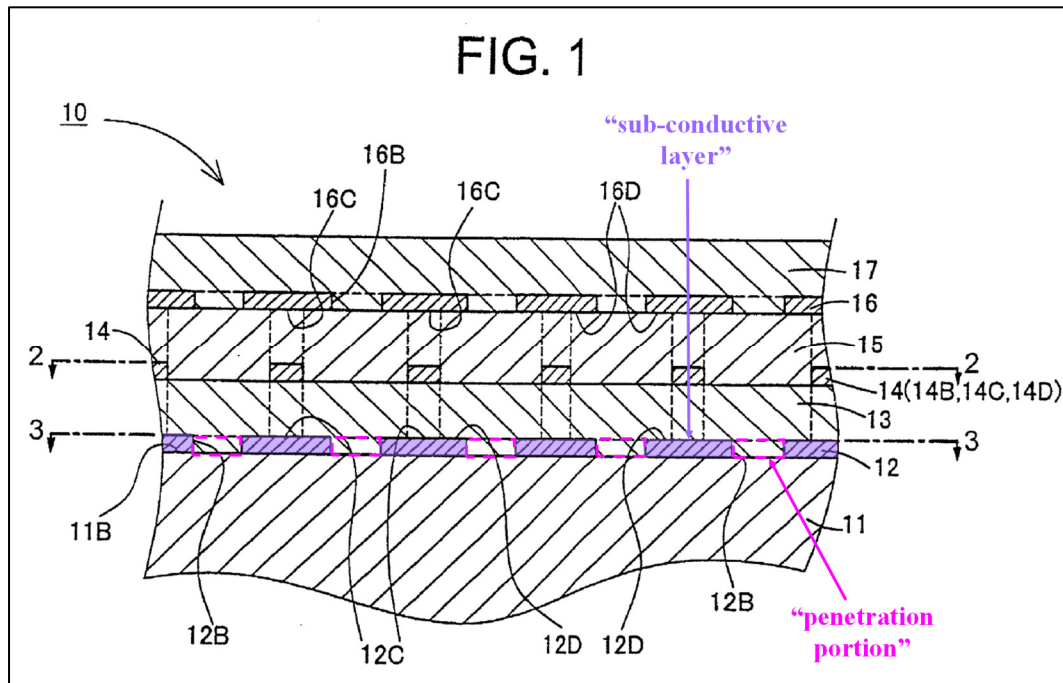
Figure 15B (below) shows forming the *pixel electrode 554* (“first electrode layer” (see 1[a])) on the *interlayer insulating film 553*. Koyama also discloses “[a] contact hole reaching the drain wiring 552 is then formed in the second interlayer insulating film 553 to form a pixel electrode 554 from a conductive oxide film.” (EX1006, [0202]; EX1002, ¶215.)



- 11[d]: “forming a penetration portion on the sub-conductive layer;”

Figure 1 of Nakanishi (below) shows forming *through holes 12B, 12E, 12H, and 12L* (“penetration portion[s]” (see 1[f])) on the *conductor layer 12*

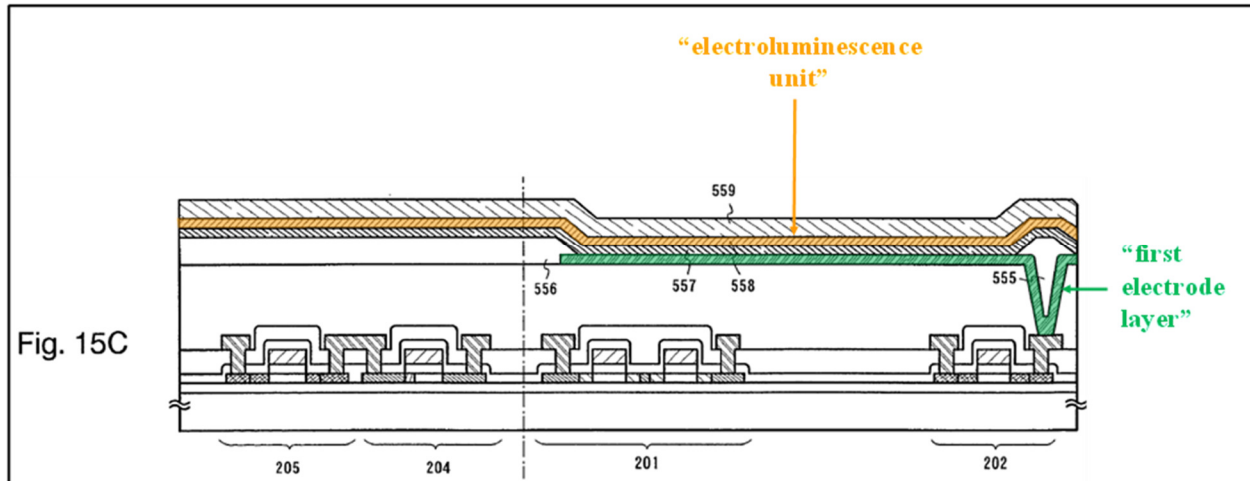
(“sub-conductive layer” (*see* (1[f])). Nakanishi also discloses “[t]he through holes are also intended to allow release of gas therethrough,” and then discusses “fabricating the wiring substrate 10” including fabricating the through holes. (EX1007, [0049]; EX1002, ¶¶216-217.)



- 11[e]: “forming an organic EL unit on the first electrode layer;”

Figure 15C (annotated below) shows forming *light emitting layer 558* (“organic EL unit” (*see* 1[a])) on the *pixel electrode 554* (“first electrode layer” (*see* 1[a])). Koyama discloses “[t]he surface of the pixel electrode 554 is next subjected to ozone treatment. The ozone treatment in this embodiment is provided through UV light irradiation while the pixel electrode is exposed to oxygen gas.

After that, a hole injection layer 557 and a light emitting layer 558 are formed by spin coating.” (EX1006, [0204]; EX1002, ¶¶218-219.)



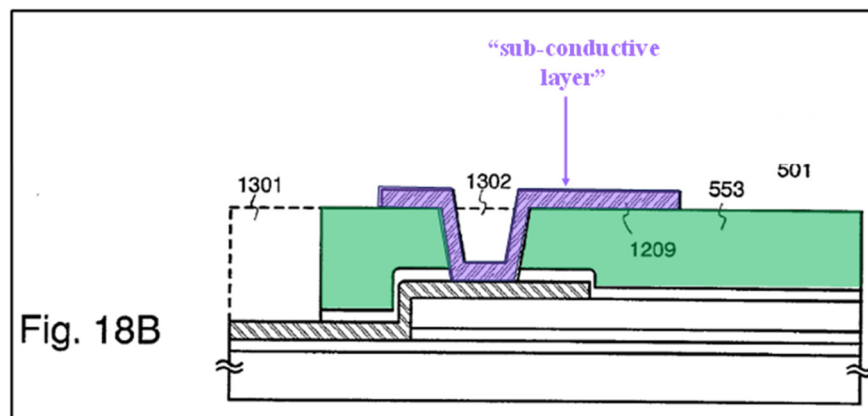
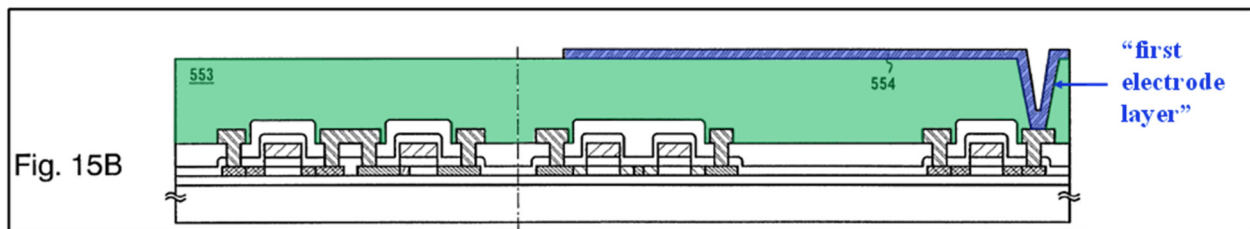
- 11[f]: “forming a second electrode layer on the organic EL unit.”

Koyama discloses “a hole injection layer 557 and a light emitting layer 558 are formed by spin coating.” (EX1006, [0204].) Koyama then discloses “[n]ext, a cathode 559 is formed to a thickness of 400 nm from a conductive film having low work function.” (EX1006, [0206].) The cathode 559 discussed in [0204] is a “second electrode layer” (*see* 1[a]), and light emitting layer 558 is an “organic EL unit” (*see* 1[a]). (EX1002, ¶¶220-221.)

I. Claim 12: “The method of claim 11, wherein forming of the sub-conductive layer is simultaneous with forming the first electrode layer.”

Koyama teaches connecting wiring 1209 (“sub-conductive layer” (*see* 1[d])) and a light emitting layer 558 on the pixel electrode 554 (“first electrode layer” (*see* 1[a])). Koyama discloses “[t]he connection wiring 1209 and the pixel

electrode 554 in FIG. 15B are simultaneously formed. (FIG. 18B).” (EX1006, [0225].) Figures 15B and 18B (below) show forming the *pixel electrode 554* on top of the *interlayer insulating film 553* and forming the *connecting wiring 1209* on top of the *interlayer insulating film 553*. Because the connecting wiring 1209 and pixel electrode 554 are both formed on the interlayer insulating film 553, forming of the connecting wiring 1209 is simultaneous with forming the pixel electrode 554. (EX1002, ¶¶222-224.)



J. Claim 15

1. Elements 15[pre]-15[b], 15[d], and 15[e]

Elements 15[pre]-15[b], 15[d], and 15[e] are similar to elements 11[pre]-11[b], 11[e], and 11[f], respectively, which Koyama and Nakanishi teach. (EX1002, ¶¶225-227, 229, 230.)

2. 15[c]: “forming a sub-conductive layer comprising a plurality of unit sub-conductive layers and a first electrode layer on the insulating layer;”

Element 15[c] is similar to element 11[c], but element 15[c] also requires the “sub-conductive layer comprising a plurality of unit sub-conductive layers.”

Koyama teaches element 11[c]. Additionally, Nakanishi teaches the “sub-conductive layer comprising a plurality of unit sub-conductive layers.” (*See* 15[c]; EX1002, ¶228.)

VIII. GROUND 4: MATSUEDA AND NAKANISHI RENDER OBVIOUS CLAIMS 1-5, 7, AND 9-15

A. Elements 1[pre]-1[e], 11[pre]-11[c], 11[e], 11[f], and 15[pre]-15[e], Claims 2, 7, 9, 10, And 12

Matsueda teaches elements 1[pre]-1[e], 11[pre]-11[c], 11[e], 11[f], 15[pre]-15[e], and claims 2, 7, 9, 10, and 12. (*See* Ground 1; EX1002, ¶¶231-236, 242, 253-270, 274-276, 284-289.)

A. Elements 1[f], 11[d], Claims 3-5, 13, And 14

Matsueda teaches elements 1[f] and 11[d], and claims 3-5, 13, and 14. (*See* Ground 1.) To the extent that Matsueda does not a “penetration portion” or “two or more penetration portions,” Nakanishi teaches a “penetration portion” and “two or more penetration portions.” (*See* Ground 3, elements 1[f], 11[d], claims 3-5, 13, 14; EX1002, ¶¶237-238, 243-252, 271-273, 277-283.)

It would have been obvious to combine the teachings of Matsueda and Nakanishi. Matsueda and Nakanishi are from the same field of endeavor. They both disclose conductor layers on insulating layers containing an organic material. Matsueda discloses auxiliary cathode wiring 16 on a planarizing film 20 and bank layer 19 containing an organic resin. (EX1004, [0053], [0067], [0069], Figs. 8, 9.) Nakanishi similarly discloses a conductor layer 12 on a core substrate 11 that also contains an organic resin. (EX1007, [0043], [0049], Fig. 1.) Thus, they both have the same structure (conductor layers on insulating layers containing an organic material) and the same function (transmitting signals via a conductor layer on top of an organic insulating layer). Both of the devices of Matsueda and Nakanishi are subjected to heat during the manufacturing process. Matsueda explains that “[s]ince the bank layer, which is made of the organic material, has low resistance to heat and chemicals, it is difficult to form the auxiliary cathode wiring 16 on the bank layer, but it is easy to form metal wiring such as the auxiliary cathode wiring 16 on the substrate 15 provided with the FET or the like.” (EX1004, [0056].) A POSITA would have known that the heat treatment may lead to issues such as “a conductor layer . . . hinder[ing] diffusion of gas released from an underlying dielectric layer or conductor layer. This gas release phenomenon may generate blisters between a dielectric layer and a conductor layer in contact with the dielectric layer.” (EX1007, [0006].) Matsueda and Nakanishi are reasonably

pertinent to the same technical problems of improving the manufacturing and quality of devices that have conductor layers on organic insulating layers, which are subjected to heat during the manufacturing process. (EX1002, ¶¶239.)

Nakanishi solves the problem by using “conventional wisdom [of] . . . provid[ing] a conductor layer, which is electromagnetically coupled with a signal wiring layer, with a number of through holes to maintain the bonding strength with a dielectric layer and to prevent the generation of blisters.” (EX1007, [0007].) Thus, Nakanishi teaches adding through holes in the conductor layer to maintain the bonding strength of the conductor layer with the dielectric layer and preventing the generation of blisters caused by the conductor layer having poor gas release properties. These technical features may be combined with the teachings of Matsueda to generate an OLED device with better reliability and performance. Nakanishi thus improves upon Matsueda. Like Nakanishi, Matsueda teaches an ITO layer 18 (sub-conductive layer) on the planarizing film 20 (insulating layer). Given that the prior art has already known and demonstrated such techniques with success, there would have been a reasonable expectation of success. (EX1002, ¶240.)

Because Matsueda and Nakanishi both relate to conductive layers on organic insulating layers and devices that are subjected to heat treatment during the manufacturing process, a POSITA would have been motivated to use the

techniques disclosed in Nakanishi to improve the similar device of Matsueda in the same way. The result would have been Matsueda's OLED device with improved reliability due to the inclusion of through holes that allow the diffusion of gas released from the underlying dielectric layer. As Nakanishi stated, such techniques were known and part of "conventional wisdom." Thus, it would have been obvious to a POSITA to combine the teachings of Matsueda and Nakanishi. (EX1002, ¶241.)

IX. THE BOARD SHOULD NOT DENY INSTITUTION UNDER *FINTIV*²

A. A Final Written Decision Will Issue Before Any Trial

A schedule has not yet been issued and no trial date has been set in the corresponding district court litigation. A Final Written Decision is expected to issue around March 2027, whereas the trial date for the district court case (which has not been set) will likely be after.

² Petitioner is not addressing in full discretionary issues in the Petition per USPTO guidance. See *FAQs for Interim Processes for PTAB Workload Management*, USPTO, <https://www.uspto.gov/patents/ptab/faqs/interim-processes-workload-management> (last visited Aug. 28, 2025).

B. Merits Of The Petition Support Institution

As discussed above, the prior art teaches every element of the challenged claims, and the claims are unpatentable. Thus, the merits of the Petition weigh strongly in favor of institution. *See* 3/26/25 Stewart Memorandum, 2 (“The strength of the unpatentability challenge” is a relevant consideration), available at https://ptacts.uspto.gov/ptacts/public-informations/petitions/1557276/download-documents?artifactId=UqSSfECO18_URcCJvOtOEi9yjB-dRaL4VDQtAXRyo29b-QU48RPCg0M (last visited Sep. 16, 2025).

X. THE BOARD SHOULD NOT DENY INSTITUTION UNDER § 35 U.S.C. 325(D)

The Petition does not raise the same or substantially the same art previously presented to the Office, nor does the Petition raise the same or substantially the same arguments previously presented to the Office in the examination of the ’708 patent. *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (PTAB Feb. 13, 2020).

Examination of the ’708 patent was short and not particularly robust. The Examiner’s sole Office Action contained objections to the drawings and § 112 rejections. (EX1003, 222-223.) Only five prior art references were identified during prosecution—none are the prior art of this Petition. (EX1001, 1.) And the prior art of this Petition teaches a sub-conductive layer having the limitations that

the prior art of record did not have, and thus is materially different and not cumulative of the art applied during examination.

Even if the Board were to conclude otherwise, the Office erred in a material manner. The Examiner allowed the claims without even identifying the prior art of this Petition. Where the examination record is not well developed, as here, it may indicate that the Examiner erred by “overlook[ing] something persuasive.”

Advanced Bionics, IPR2019-01469, Paper 6 at 10.

For all the foregoing reasons, the Board should decline to deny the Petition under § 325(d).

XI. NOTICES AND STATEMENTS

Pursuant to 37 C.F.R. § 42.8(b)(1), BOE Technology Group Co., Ltd., is the real party-in-interest for Petitioner.

Pursuant to 37 C.F.R. § 42.8(b)(2), Petitioner identifies the following related matters:

- *Samsung Display Co. Ltd. v. BOE Technology Group Co., Ltd. et al.*, 2:25-cv-00430-JRG-RSP (E.D. Tex.).

Pursuant to 37 C.F.R. § 42.8(b)(3), Petitioner identifies the following counsel (and a power of attorney accompanies this Petition).

Lead Counsel	First Backup Counsel	
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	<th data-bbox="812 613 1425 657">Second Backup Counsel</th> Jean Nguyen Registration No. 71,051 MORRISON & FOERSTER LLP 707 Wilshire Boulevard, Suite 6000 Los Angeles, CA 90017-3543 Email: JNguyen@mofo.com Tel: (213) 892-5200 Fax: (213) 892-5454	Second Backup Counsel

Pursuant to 37 C.F.R. § 42.8(b)(4), service information for lead and back-up counsel is provided above. Petitioner consents to electronic service by email to BOE-Samsung-IPR@mofo.com.

Pursuant to 37 C.F.R. § 42.104(a), Petitioner certifies that the '708 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

The USPTO is authorized to charge any required fees, including the fee as set forth in 37 C.F.R. § 42.15(a) and any excess claim fees, to Deposit Account No. **03-1952** referencing Docket No. **37294-00000.02**.

Dated: September 19, 2025

Respectfully submitted,

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Certification of Word Count (37 C.F.R. § 42.24)

I hereby certify that this Petition for *Inter Partes* Review has 11,121 words (as counted by the “Word Count” feature of the Microsoft Word™ word-processing system), exclusive of “a table of contents, a table of authorities, mandatory notices under § 42.8, a certificate of service or word count, or appendix of exhibits or claim listing.”

Dated: September 19, 2025

By /Mehran Arjomand/
Mehran Arjomand

Certificate of Service (37 C.F.R. § 42.6(e)(4) and 42.205(a))

I hereby certify that the attached Petition for *Inter Partes* Review and supporting materials were served as of the below date by Priority Mail Express on the Patent Owner at the correspondence address indicated for U.S. Patent No. 7,279,708.

Lewis Roca Rothgerber Christie LLP
PO BOX 29001
Glendale, CA

A copy of the attached Petition for *Inter Partes* Review and supporting materials were also served via e-mail on the following litigation counsel:

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Dated: September 19, 2025

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