

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR PRODUCTS, INC.,

Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01559
U.S. Patent No. 9,524,974

**DECLARATION OF DAVID KUAN-YU LIU, PH.D., IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,524,974**

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LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 9,524,974 (“the ’974 Patent”)
Ex-1002	Declaration of Dr. David Kuan-Yu Liu
Ex-1003	Curriculum Vitae of Dr. David Kuan-Yu Liu
Ex-1004	Prosecution History of U.S. Patent No. 9,524,974 (App. No. 14/806,111)
Ex-1005	U.S. Patent No. 8,592,978 (“Matsuno”)
Ex-1006	U.S. Patent App. Pub. No. 2015/0162277 (“Zhang”)
Ex-1007	U.S. Patent No. 6,500,765 (“Kao”)
Ex-1008	U.S. Patent App. Pub. No. 2011/0032763 (“Kwak”)
Ex-1009	[Intentionally left blank]
Ex-1010	[Intentionally left blank]
Ex-1011	[Intentionally left blank]
Ex-1012	[Intentionally left blank]
Ex-1013	[Intentionally left blank]
Ex-1014	[Intentionally left blank]
Ex-1015	[Intentionally left blank]
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Ex-1017	[Intentionally left blank]
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Ex-1020	Claim Mapping Table
Ex-1021	Rino Micheloni et al., Inside NAND Flash Memories (2010)
Ex-1022	Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Oct. 16, 2024)
Ex-1023	First Amended Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Dec. 19, 2024)
Ex-1024	Second Amended Complaint (Redacted Version), <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Jul. 28, 2025)
Ex-1025	Paul Zimmerman, <i>Double patterning lithography: double the trouble</i>

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

	<i>or double the fun?</i> , SPIE Newsroom, (July 20, 2009)
Ex-1026	U.S. Patent No. 6,204,200
Ex-1027	Christopher Bencher, et al., <i>22nm Half-Pitch Patterning by CVD Spacer Self Alignment Double Patterning (SADP)</i> , Optical Microlithography XXI (2008)
Ex-1028	Seiichi Aritome, NAND Flash Memory Technologies (2016)
Ex-1029	U.S. Patent No. 9,123,776
Ex-1030	U.S. Patent No. 9,595,477
Ex-1031	U.S. Patent App. Pub. No. 2008/0014760 (“Murata”)
Ex-1032	Mincheol Park et al., <i>Effect of low-k dielectric material on 63nm MLC (multi-level cell) NAND flash cell arrays</i> , IEEE VLSI-TSA International Symposium on VLSI Technology 37 (2005)
Ex-1033	Daewoong Kang et al., <i>The Air Spacer Technology for Improving the Cell Distribution in 1 Giga Bit NAND Flash Memory</i> , 21st IEEE Non-Volatile Semiconductor Memory Workshop (2006)
Ex-1034	Jiyoung Kim, et al., <i>A stacked memory device on logic 3D technology for ultra-high-density data storage</i> , Nanotechnology 22 (2011)
Ex-1035	T. Kundu, et al., <i>Electrical Techniques for the Characterization of Dielectric Films</i> , The Electrochemical Society Interface 14 (Sept. 2005)
Ex-1036	U.S. Patent No. 5,707,901
Ex-1037	David Abercrombie, <i>Self-Aligned Double Patterning, Part One</i> , Siemens Digital Industries Software Blog (Jan. 27, 2015)
Ex-1038	LayWai Kong, et al., <i>3D-interconnect: Visualization of extrusion and voids induced in copper-filled through-silicon vias (TSVs) at various temperatures using X-ray microscopy</i> , Microelectric Engineering 24 (2012)
Ex-1039	Sean King, <i>Dielectric Barrier, Etch Stop, and Metal Capping Materials for State of the Art and beyond Metal Interconnects</i> , ECS J. Solid State Sci. & Tech. N3029 (2015)
Ex-1040	Claim Construction Order, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Oct. 3, 2025)

I. INTRODUCTION

1. Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Petitioner”) request *inter partes* review (“IPR”) of Claims 1-2, 4, 6, and 11-18 of U.S. Patent No. 9,524,974 (“the ’974 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“PO”).

2. I have been retained by Micron Technology, Inc. and Micron Semiconductor Products, Inc. (collectively, “Petitioner”), as an independent expert in this proceeding before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand that Petitioner is requesting that the Board institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 9,524,974 (“the ’974 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“Patent Owner” or “PO”).

3. I am not and have never been an employee of Petitioner. I am being compensated at my usual and customary hourly rate of \$600 for time testifying and \$550 for all other time. No part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

4. I have been asked to provide my independent analysis of Claims 1-2, 4, 6, and 11-18 of the ’974 Patent in light of the prior art publications cited below. I have also been asked to consider the state of the art and prior art available as of July 22, 2015. Based on the prior art discussed in this declaration, it is my opinion that

Claims 1-2, 4, 6, and 11-18 of the '974 Patent are unpatentable for the reasons provided below.

II. BACKGROUND AND QUALIFICATIONS

5. My curriculum vitae ("CV") is filed concurrently as Ex-1003 and provides an accurate identification of my background and experience. Among other things, my CV includes a list of my issued patents and publications for at least the last 30 years. My CV also includes information about my expert witness experience, with case numbers where available.

6. I received a Bachelor of Science in Electrical Engineering from the University of California, Berkeley, in 1983. I received a Master of Science and Ph.D. in Electrical Engineering from Stanford University in 1985 and 1989, respectively.

7. I worked on a novel Conductivity Modulated Power MOSFET for my Ph.D. thesis. The novel device uses a trench injector to facilitate an optimal tradeoff between the breakdown voltage and ON-Resistance of a Power MOSFET (Vertical DMOS) through the use of a minority carrier injector.

8. From 1989 to 1992, I was a member of technical staff at Texas Instruments, Inc. ("TI"). At TI, my job responsibilities included process integration, device modeling, high-voltage complementary metal oxide semiconductor (CMOS) process integration, and investigating novel source-side injection mechanisms for Flash EPROM channel hot-electron programming.

9. From 1992 to 1995, I was a member of the technical staff at Advanced Micro Devices, Inc. (“AMD”) where I was a key contributor in optimizing Flash cell and periphery devices in AMD’s CMOS-based 0.5 μ m and 0.35 μ m Flash EPROM technology. My job responsibilities at AMD also included process integration, device modeling, and development of triple-well process technology to accommodate x-decoder transistors and high-voltage transistors for negative gate erase operations. While at AMD, I was awarded a Spotlight Award for developing a method of manufacturing a self-aligned source (SAS) etch for a NOR flash memory.

10. I spent the next five years of my career in managerial and director roles at several California-based semiconductor companies. I was responsible for increasing yield and for leading teams of engineers working to develop next-generation memory devices.

11. In 2000, I co-founded Progressant Technologies in Fremont, California. Progressant Technologies developed IP for negative differential resistance transistor technology and was eventually acquired by Synopsys, Inc.

12. From 2000 to 2004, I was a Senior Manager at Xilinx, Incorporated, where I was responsible for developing nonvolatile memory process technology for flash and CPLD product applications, as well as advanced CMOS process technology (specifically 75nm CMOS technology node, a half node version between 90nm and 65nm).

13. From 2004 to 2007, I was a Senior Scientist at Maxim Integrated Products where I was responsible for developing Embedded Non-volatile Memory process technology for Power Management product applications.

14. Since 2007, I have served as a technical consultant where I have provided expert advice regarding Flash memory technology, CMOS process technology, and semiconductor device physics. As part of this, I have considered, assessed, and assisted with the design of various different memory devices, including NAND flash and monolithic 3D memory structures.

15. I hold over 99 U.S. patents, a vast majority of which are directly related to Nonvolatile memory device technology. For example, U.S. Patent No. 5,250,464 relates to use of sidewall layers of silicone dioxide and silicon nitride to form a sidewall anti-fuse structure.

16. I am not now and have never been an employee of the Petitioner.

III. INFORMATION CONSIDERED

17. In preparation for this declaration, I have considered the materials discussed in this declaration, including, for example, the '974 Patent, the references cited by the '974 Patent, the prosecution history of the '974 Patent and applications from which it derives (including the references cited therein), various background articles and materials referenced in this declaration, and the prior art references identified in this declaration.

18. In forming the opinions expressed below, I have considered: the documents listed above, any additional documents discussed below, and my education, training, experience, and knowledge in the relevant field of multimedia processing or communications networks.

IV. RELEVANT LEGAL STANDARDS

19. In forming my opinions and considering the subject matter of the '974 Patent and its claim in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

A. Claim Interpretation

20. I have been informed and understand that in an IPR proceeding, claims are to be interpreted according to the *Phillips* claim construction standard. I have been informed and understand that claim construction is a matter of law and that the final claim constructions for this proceeding will be determined by the PTAB.

B. Perspective of One of Ordinary Skill in the Art

21. I have been informed and understand that a patent is to be understood from the perspective of a hypothetical “person of ordinary skill in the art” (“POSITA”). Such an individual is considered to possess normal skills and knowledge in a particular technical field (as opposed to being a genius). I understand that in considering what the claims of a patent require, what was known prior to that

patent, what a prior art reference discloses, and whether an invention is obvious or not, one must use the perspective of such a POSITA.

22. A POSITA at the relevant time would have had a bachelor's degree in electrical engineering, computer engineering, or a related field, and at least two years of experience in the research, design, or development of semiconductor memory device structures, or the equivalent, with additional education substituting for experience and vice versa. I believe that I possessed and exceeded such experience and knowledge before and at the priority date and that I am qualified to opine on the '974 Patent.

C. Obviousness

23. I have been informed and understand that a patent claim is obvious under 35 U.S.C. §103, and therefore invalid, if the claimed subject matter, as a whole, would have been obvious to a POSITA as of the priority date of the patent based on one or more prior art references and/or the knowledge of a POSITA.

24. I understand that an obviousness analysis must consider (1) the scope and content of the prior art, (2) the differences between the claims and the prior art, (3) the level of ordinary skill in the pertinent art, and (4) secondary considerations, if any, of non-obviousness (such as unexpected results, commercial success, long felt but unmet need, failure of others, copying by others, and skepticism of experts).

25. I understand that a prior art reference may be combined with other references to disclose each element of the invention under 35 U.S.C. §103. I understand that a reference may also be combined with the knowledge of a POSITA, and that this knowledge may be used to combine multiple references. I further understand that a POSITA is presumed to know the relevant prior art. I understand that the obviousness analysis may take into account the inferences and creative steps that a POSITA would employ.

26. In determining whether a prior art reference would have been combined with other prior art or other information known to a POSITA, I understand that the following principles may be considered:

- whether the references to be combined involve non-analogous art;
- whether the references to be combined are in different fields of endeavor than the alleged invention in the Patent;
- whether the references to be combined are reasonably pertinent to the problems to which the inventions of the Patent are directed;
- whether the combination is of familiar elements according to known methods that yields predictable results;
- whether a combination involves the substitution of one known element for another that yields predictable results;
- whether the combination involves the use of a known technique to

improve similar items or methods in the same way that yields predictable results;

- whether the combination involves the application of a known technique to a prior art reference that is ready for improvement, to yield predictable results;
- whether the combination is “obvious to try”;
- whether the combination involves the known work in one field of endeavor prompting variations of it for use in either the same field or a different one based on design incentives or other market forces, where the variations are predictable to a POSITA;
- whether there is some teaching, suggestion, or motivation in the prior art that would have led one of ordinary skill in the art to modify the prior art reference or to combine prior art reference teachings to arrive at the claimed invention;
- whether the combination requires modifications that render the prior art unsatisfactory for its intended use;
- whether the combination requires modifications that change the principle of operation of the reference;
- whether the combination is reasonably expected to be a success; and
- whether the combination possesses the requisite degree of predictability

at the time the invention was made.

27. I understand that in determining whether a combination of prior art references renders a claim obvious, it is helpful to consider whether there is some teaching, suggestion, or motivation to combine the references and a reasonable expectation of success in doing so. I understand, however, that a teaching, suggestion, or motivation to combine is not required.

V. RELIEF REQUESTED

28. I understand that Petitioner challenges the validity of Claims 1-4, 6-7, and 11-18 of the '974 Patent. In particular, I understand that Petitioner asserts the following grounds for challenging the claims of the '974 Patent:

Ground	Summary
1	Claims 1-4, 12, and 15 is obvious over Matsuno (Ex-1005).
2	Claims 6, 11, and 16 are obvious over Matsuno in view of Zhang (Ex-1006).
3	Claims 13-14 and 17-18 are obvious over Matsuno in view of Kao (Ex-1007).
4	Claims 1-4, 11-12, and 15 are obvious over Kwak (Ex-1008).

Ground	Summary
5	Claims 6-7 and 16 are obvious over Kwak in view of Zhang.
6	Claims 13-14 and 17-18 are obvious over Kwak in view of Kao.

VI. THE CHALLENGED PATENT

A. Priority Date

29. The earliest possible priority date for the '974 Patent is July 22, 2015. Ex-1024 ¶22; Ex-1023 ¶22; Ex-1022 ¶23. Petitioner takes no position on the proper priority date for each claim of the '974 Patent. I take no position on the proper priority date for each claim of the '974 Patent.

B. The '974 Patent

30. The '974 Patent “relates generally to non-volatile semiconductor memories of the flash memory type, their formation, structure and use.” Ex-1001, 1:6-8. In describing general “EEPROM architecture” that “utilizes a NAND array,” the '974 Patent acknowledges that “NAND strings are generally connected by conductive lines in order to form arrays that may contain many NAND strings.” *Id.*, 1:18-19, 1:47-48. “At either end of a NAND string a contact area may be formed. This allows connection of the NAND string as part of the array. Metal contact plugs (or ‘vias’) may be formed over contact areas to connect the contact areas (and

thereby connect NAND strings) to conductive metal lines that extend over the memory array (e.g. bit lines).” *Id.*, 1:49-54.

31. “Contacts to contact areas may be formed by etching contact holes through a dielectric layer and then filling the holes with metal to form vias. Metal lines, such as bit lines, extend over the memory array and in peripheral areas in order to connect the memory array and various peripheral circuits.” *Id.*, 1:56-61.

32. The specification states that due to the close proximity of bit lines, processing is difficult and the risk of capacitive coupling increases. *Id.*, 1:63-67. The specification further states “a need for an integrated circuit manufacturing process that forms conductive lines, such as bit lines, in close proximity in an efficient manner.” *Id.*, 2:3-5.

33. By the time the ’974 Patent was filed, a process called “self-aligned double patterning” or “sidewall-assisted double patterning” was a known process to manufacture integrated circuits. Ex-1001, Abstract; Ex-1037, 2. With sidewall-assisted double patterning, mandrels made of a resist material are formed in a pattern on a dielectric layer and a substrate; the mandrels, including their sidewalls, are then covered with another layer; that layer is etched to form spacers; the mandrels are then removed, leaving a gap between the spacers; a second mask is used to prevent the etch of areas that do not need a trench; the dielectric layer is etched around the second mask, leaving trenches of a certain pattern in the dielectric layer; and finally

the top portion of the spacers and second mask are polished. Ex-1037, 2-3, Fig. 4; Ex-1025, 2, Fig. 2.

34. The '974 Patent describes using a “sidewall assisted process” to form trenches for bit lines “so that trenches alternate between two different profiles.” Ex-1001, 2:9-11.

35. The '974 Patent's Figure 2C illustrates “bit lines formed in a dielectric layer.” *Id.*, 7:44-45; *see id.*, 7:28-32. The '974 Patent acknowledges that alternating bit lines was known in the art. *Id.*, 7:37-38. Due to the decrease in spacing between conductive lines as memory devices became smaller, the chance of capacitive coupling between bit lines increased. *Id.*, 7:41-44. To make a “bit line” using sidewall-assisted double patterning, elongated openings called “trenches” are formed in a dielectric layer; the trenches are filled with a conductive material; and then the excess conductive material is removed. The remaining conductive material makes up the “bit line.” *Id.*, 7:44-50.

36. The '974 Patent explains that “sidewall assisted patterning (SAP) may be used to enable patterning of features that are smaller than the smallest features that can be patterned by direct patterning using a given photolithographic process.” *Id.*, 7:54-57, Figs. 3A-C.

37. The '974 Patent describes “an alternative sidewall assisted process for forming trenches,” with trenches that “alternate between two different types of

trench with two different profiles.” *Id.*, 8:16-20. As shown in Figure 4A below, mandrels 411 are covered by liner layer 415. *Id.*, 8:20-28. Then sidewall spacer liner 417 is deposited over liner layer 415. *Id.*, 8:28-39.

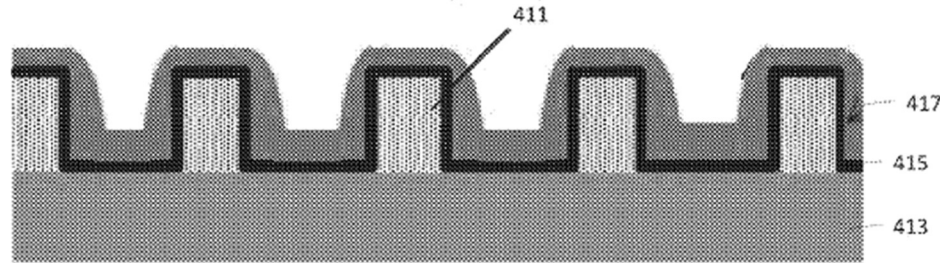


FIG. 4A

Id., Fig. 4A.

38. Figure 4B shows the remaining structure after sidewall spacer layer 417 and liner layer 415 were etched, leaving sidewall spacer 417a-c along the sides of mandrel 411 and liner layer portions 415a-c. *Id.*, 40-45.

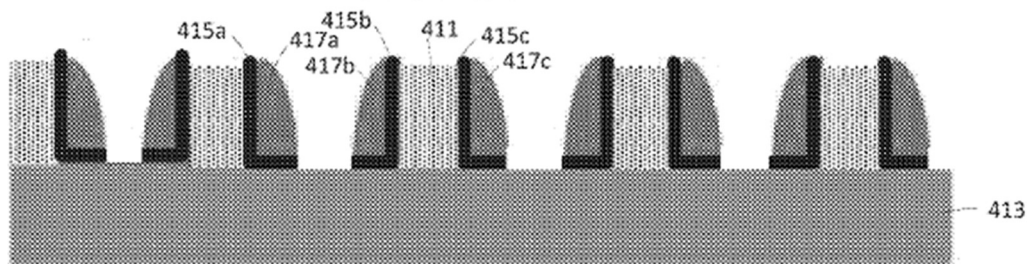


FIG. 4B

Id., Fig. 4B.

39. The '974 Patent states “sidewall spacers, liner layer portions, and dielectric layer 413 are substantially unaffected by removal of mandrels,” as illustrated in Figure 4C below. *Id.*, 8:53-57. The '974 Patent explains that masking

portion 419 consists of sidewall spacer 417a and liner layer portion 415a. *Id.*, 8:57-60.

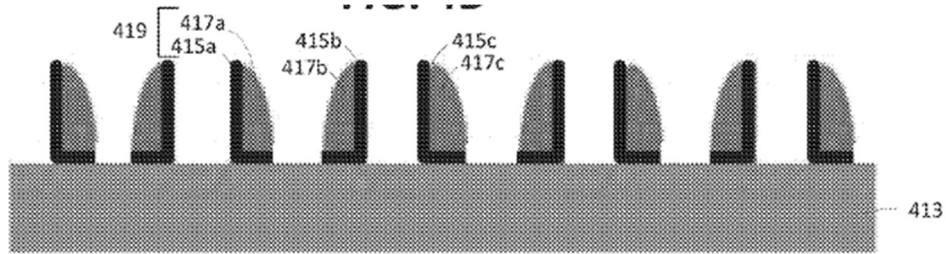


FIG. 4C

Id., Fig. 4C.

40. Figure 4D below illustrates “the result of anisotropic etching” using the pattern of Figure 4C as an etch mask to etch dielectric layer 413. *Id.*, 8:61-63.

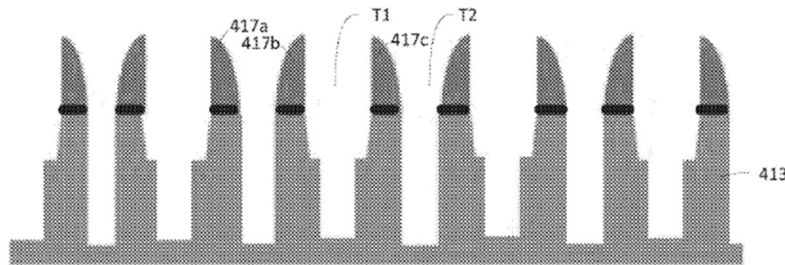


FIG. 4D

Id., Fig. 4D.

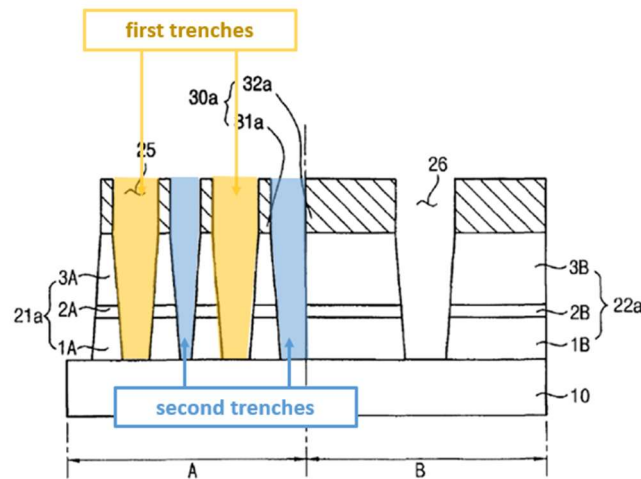
41. The '974 Patent states that alternating trenches may be used “in forming integrated circuits including, but not limited to, NAND flash memories,” such as for forming bit lines. *Id.*, 9:44-47. The '974 Patent states that mandrels “may be formed by direct patterning, or may be formed by one of the SAP [(sidewall assisted)] processes.” *Id.*, 10:10-32.

C. Prosecution History of the '974 Patent

42. The '974 file history is submitted as Ex-1004. During prosecution, the Examiner rejected certain claims over the prior art reference U.S. Patent No. 8,247,291 (“Min”). Ex. 1004, 65-70. The Examiner mapped first and second trenches to elements 25 and 26 of Min’s Figures 1F-1G respectively to show trenches arranged in an alternating pattern. *See id.*, 66. To overcome this rejection, the Applicant argued that Min’s trenches 25 and 26 “have the same shape and are not in an alternating pattern as recited in claim 1.” *Id.*, 97. The Examiner then allowed the claims based on arguments made by the applicant. *Id.*, 110.

43. But the Examiner appears to have overlooked the first and second trenches (yellow and blue) formed between first spacers 71 in area A that are differently shaped and arranged in an alternating pattern.

FIG. 1G



VII. CLAIM CONSTRUCTION

44. I do not believe that any term requires explicit construction to resolve the issues presented in the Petition. I ascribe the plain meaning to each claim term, as that plain meaning would have been understood by a POSITA. *See* Ex-1040, 49-62.

45. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

VIII. TECHNOLOGICAL BACKGROUND

46. This section provides technology background to the '974 Patent.

47. The '974 Patent and the prior art discussed in the Petition relate generally to manufacturing MOSFET semiconductor devices. Ex-1027, 1:24-26. And NAND flash memory is implemented using CMOS technology. *See, e.g.*, Ex-1028, 276.

48. NAND flash has been known and in use for quite some time, having been first developed in 1987. *See* Ex-1028, 22, 329. Like all semiconductor memory, NAND flash includes memory “cells,” with a number of memory cells arranged in series to form a string. In NAND flash, data is stored in a “cell” formed from a single transistor that is connected with many other memory cell transistors in series. Given that the string of memory cells can only conduct and pass current when each and every memory cell transistor in the string is turned on, this results in the logical equivalent of what a POSITA would have understood to be a “NOT AND” circuit. Ex-1028, 38-39. This is why this type of memory is referred to as “NAND.”

49. The strings of memory cells are configured into a memory array with each bit line connecting to many strings running in a vertical direction (in a 2-dimensional array). Figure 2.2 of Micheloni illustrates how a NAND string (shown on the left side) is connected to other strings sharing the same bit line, with two strings sharing a bit line contact. Bit lines are arranged in the horizontal direction with alternating bit lines being designated either as even bit line or odd bit line; respectively. *See* Ex-1021, 21.

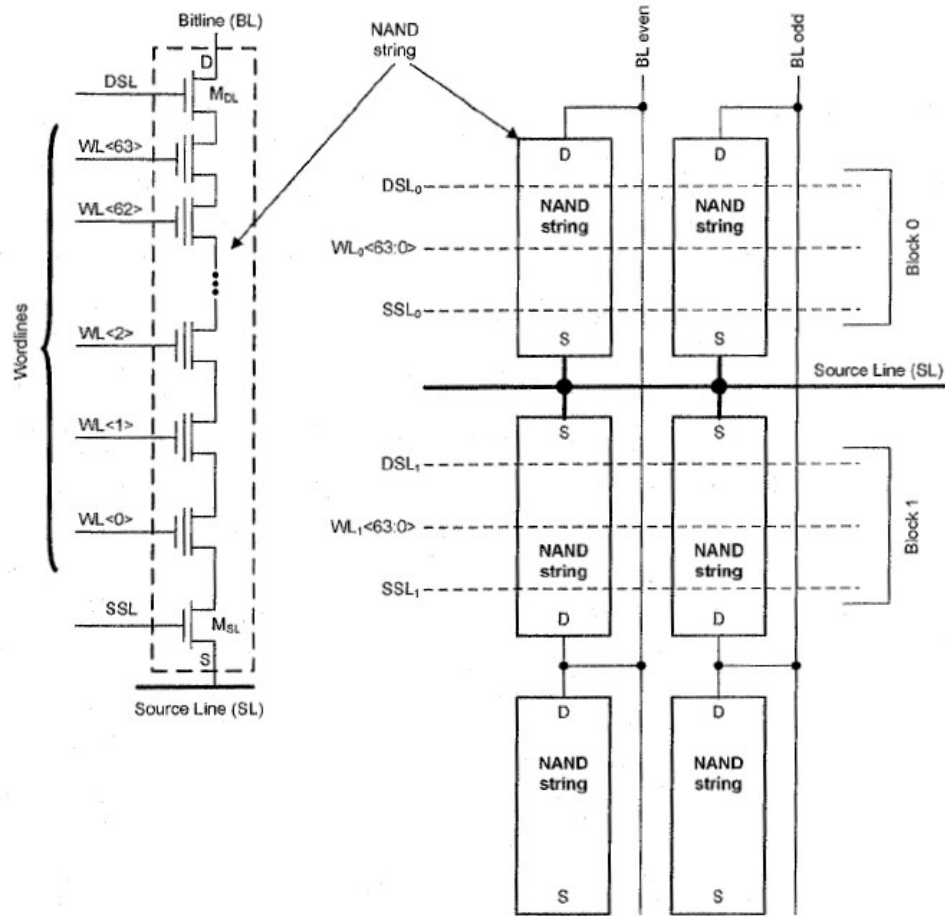


Fig. 2.2. NAND string (left) and NAND array (right)

A. It was well known to etch trenches of a particular profile (etch selectivity)

50. A POSITA would have known how to form trenches and bit lines of different depths, sizes, shapes, and profiles using various etching techniques.

51. A POSITA would have considered the type of materials and number of layers to use to etch a certain shape or profile. Some materials are more resistant than others to a given etchant. It was well known in the 1990s that a stop etch layer or layer, for instance, is used to prevent over-etching. *See, e.g., Ex-1036* (U.S. Patent

No. 5,707,901). Over-etching occurs when unintended removal of materials occurs to an underlying layer, resulting in poor electrical characteristics of the MOS device. *Id.*, 1:15-23, 2:40-48.

52. Masks were well-known in the art to assist with creating a specific pattern in a layer.

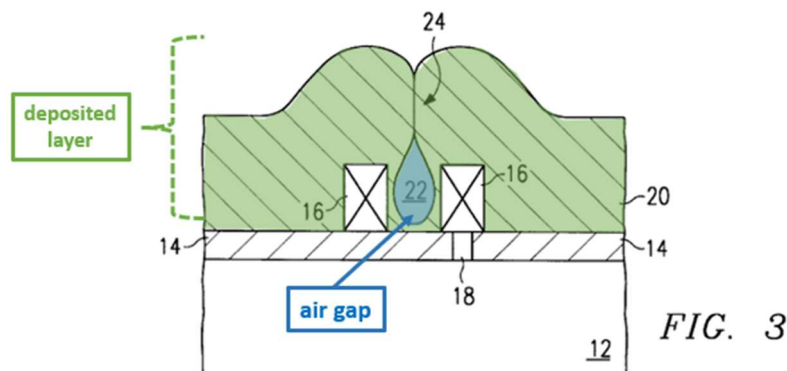
53. Etch selectivity is the ratio between two etch rates, usually between a material being etched and a mask (or different layer). Etch selectivity allows a POSITA to have more flexibility or control over the etching process. A POSITA would have understood that one can tailor the conditions and chemistry of an etch such that a specific layer is etched at a higher rate than that of another layer. *See* Ex-1039, N3033-N3034. The use of multiple layers of different materials and chemistries allows for better flexibility of the etching process and tailoring of trench profile. *See id.* A higher selectivity generally means it will be easier to etch a vertical profile since a faster removal of the targeted layer can be achieved without any significant etching of the masking layer. The selectivity can be adjusted by adjusting the processes or mask material, which affects etch rates. Like the etch stop layer discussed above, by switching chemistries, a POSITA would have more flexibility over the etch process that results in a wider range of available trench profiles.

B. It was well known to use air gaps in trenches or interconnects.

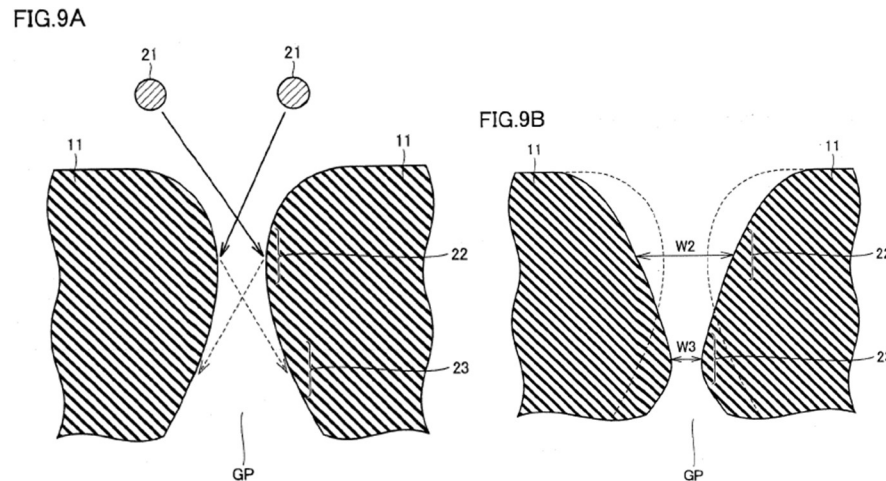
54. A POSITA would have known how to encapsulate or enclose an air gap within a trench. *See, e.g.*, Ex-1038, 26, Figs. 3-6. Conductive lines, such as bit lines, are subject to significant capacitance when they are close to one another. And this capacitance impacts memory performance. For example, an increase in capacitance causes the bit line sensing margin and refresh ability to degrade.

55. As early as 2006, the industry was addressing this “problem of increased parasitic capacitance between” NAND flash memory cells using air spacers. Ex-1033; *see also* Ex-1006, ¶¶9-10.

56. There are many ways to enclose an air gap within a trench, such as sputtering or deposition of a capping material. *See, e.g.*, Ex-1039, N3029. For example, depositing a metal layer with a high deposition rate or with a thick enough material results in “bread-loafing,” which causes the material to “pinch off” in a region between sidewalls and form an air gap, as annotated below in Figure 3 of U.S. Patent No. 6,204,200. *See* Ex-1026, Fig. 3.



57. For a pinch-off region below the surface, a POSITA would have known how to use a sputtering deposition method to facilitate a pinch-off region below the surface of a dielectric layer. *See* Ex-1031, ¶¶99, Figs. 9A-9B. For example, using a sputtering deposition like that in Figure 9B allows for the pinch-off region to be at a lower region 23, such that W3 would be zero. Thus, a subsequent planarization or polishing to region 22 allows for the pinch-off at region 23 to remain intact.



IX. BRIEF DESCRIPTION OF THE APPLIED PRIOR ART REFERENCES

58. This petition presents four references, none of which were of record during prosecution. *See* Ex-1004.

A. Matsuno (Ex-1005)

59. U.S. Patent No. 8,592,978 (“Matsuno”) was filed March 23, 2010, and issued November 26, 2013. Ex-1005. Matsuno qualifies as prior art under at least §102(a)(1) and §102(a)(2).

60. Matsuno discloses “[t]he present invention relates to a method of fabricating a semiconductor device provided with a microscopic wiring pattern and the semiconductor device.” Ex-1005, 1:16-18. Matsuno discloses first and second trenches having different shapes, with first buried wiring 10a having a rectangular cross section while “second buried wiring 10b has a trapezoidal [cross-]section with both side surfaces being tapered.” Ex-1005, 4:8-24. As shown in Figure 11 below, Matsuno discloses first and second trenches having different shapes.

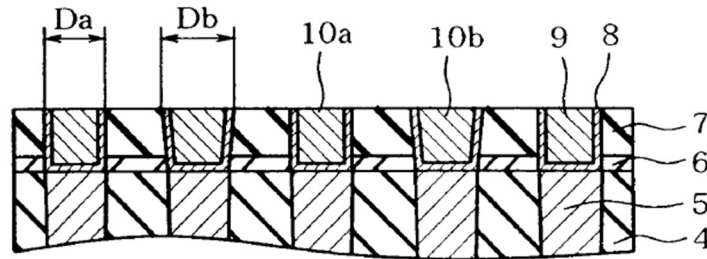


FIG. 11

Id., Fig. 11.

61. Matsuno discloses an embodiment “directed to a NAND flash memory.” Ex-1005, 2:43-45; *see id.*, Fig. 1 (NAND flash memory cell array). Matsuno specifically describes “sequential steps of the fabrication process,” *id.*, 2:36-37, including the depositing numerous films on a semiconductor substrate; forming a resist pattern; etching silicon nitride film using the resist pattern as a mask to create core patterns; depositing an amorphous silicon film to form a liner layer

over core patterns; etching the amorphous silicon film to create spacers or mask patterns; removing core patterns; etching the films using the mask pattern; depositing a barrier metal layer and copper layer; and planarizing the layers until a predetermined height is reached. *Id.*, 4:41-6:28.

B. Zhang (Ex-1006)

62. U.S. Patent Application Publication No. 2015/0162277 (“Zhang”) was filed December 5, 2013 and published June 11, 2015. Ex-1006. Zhang qualifies as prior art under at least §102(a)(1) and §102(a)(2).

63. Zhang discloses a “damascene interconnect process [that] incorporates air gaps into a high modulus dielectric material.” Ex-1006, Abstract. Zhang’s Figures 5C-5D disclose etching two types of trenches based on a hard mask layer, first trenches 133 having a width of D1 and second trenches 137 with width D2. *See* Ex-1006, ¶¶49-50.

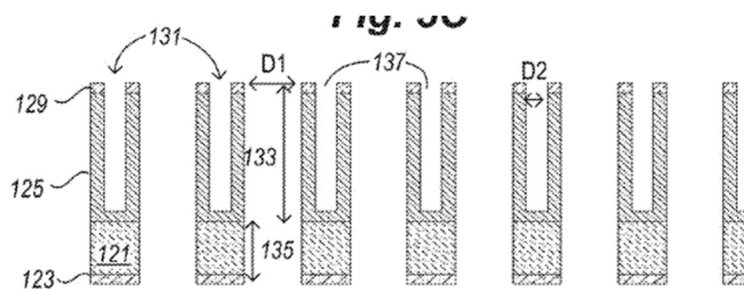


Fig. 5D

Ex-1006, Fig. 5D.

64. Zhang also discloses steps to “form air gaps and encapsulated trenches and vias.” Ex-1006, ¶53. Zhang discloses “recesses 137 of the U-shaped structures 131”—*i.e.*, second trenches—“are capped with a layer 139. The capping layer 139 will cap each U-shaped structure so as to include an air gap 141, thus forming a plurality of air gaps 141 that extend vertically within the recesses 137.” *Id.*, ¶55.

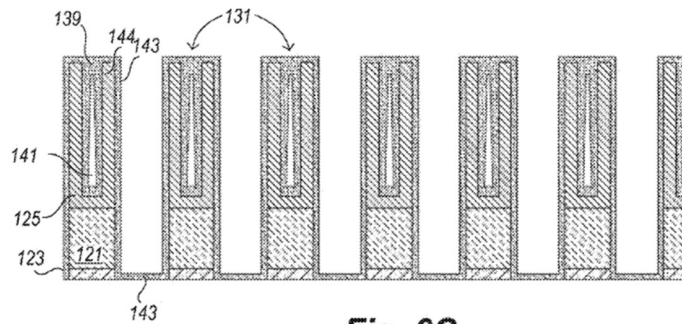


Fig. 6C

Id., Fig. 6C.

C. Kao (Ex-1007)

65. U.S. Patent No. 6,500,765 (“Kao”) was filed March 23, 2001, and issued December 31, 2002. Ex-1007. Kao qualifies as prior art under §102(a)(1) and §102(a)(2).

66. Kao discloses “[a] method of manufacturing a field effect transistor with a dual-spacer structure.” Ex-1007, Abstract. Kao describes deposition of a dielectric layer 114 on the sidewall of gate 106a and gate dielectric layer 104, which is then covered by a dielectric layer 116. *See id.*, 2:39-52. In Kao, dielectric layers 114 and 116 are then etched to form 117 spacer, formed from 116b and 114a, as shown in Figures 3-5 below. *Id.*, 2:39-3:2.

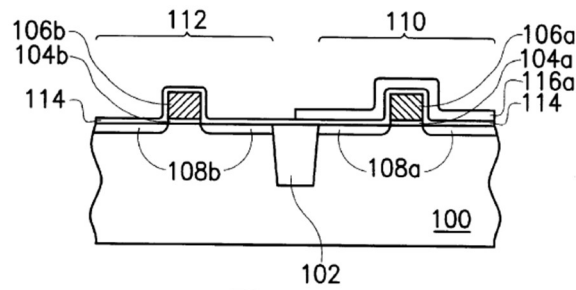


FIG. 3

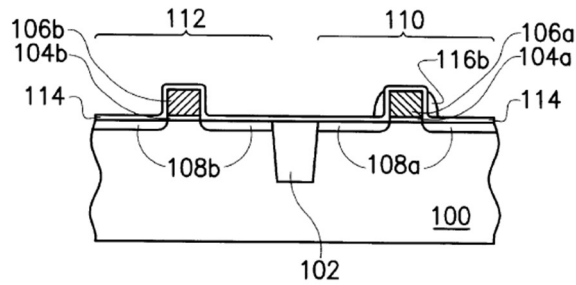


FIG. 4

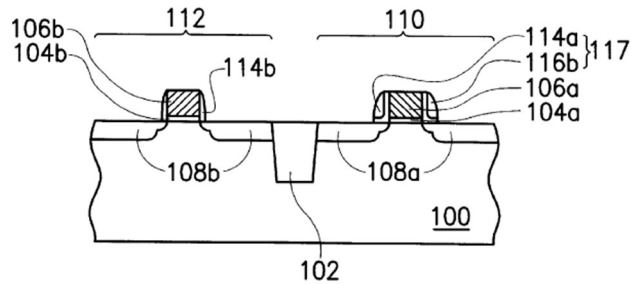


FIG. 5

Id., Figs. 3-5.

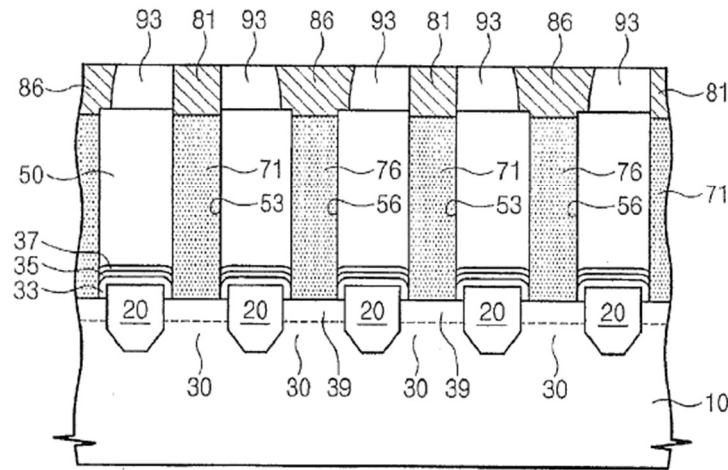
D. Kwak (Ex-1008)

67. U.S. Patent Application No. 2011/0032763 (“Kwak”) was filed October 21, 2010, and published February 10, 2011. Ex-1008. Kwak qualifies as prior art under §102(a)(1) and §102(a)(2).

68. Kwak discloses “a semiconductor device” with first and second bit lines. Ex-1008, Abstract. Kwak describes forming bit lines using masks and spacers.

See, e.g., id., ¶¶6, 63-64. Kwak states even bit lines and odd bit lines “may have different structures,” as illustrated in Figure 14 below. *Id.*, ¶45.

Fig. 14



Id., Fig. 14.

X. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS

69. The '974 Patent contains 20 claims. This Petition challenges independent Claims 1, 12, and 17 and dependent Claims 2, 4, 6-7, 9, 11, 13-15, and 18. *See* Ex. 1020. Independent Claim 1 is a “system” claim and Claim 12 is a “method” claim that adapts recitations from system Claim 1. Independent Claim 17 is also a “method” of manufacturing 3D NAND memory, but recites different steps than those recited in independent Claim 12. The subject matter of the challenged claims is disclosed by the prior art as shown below.

A. Ground 1: Claims 1-2, 4, 12, and 15 Are Obvious Over Matsuno

1. Independent Claim 1

a. Element 1[preamble]: A NAND flash memory comprising:

70. If Claim 1's preamble is limiting, Matsuno discloses the preamble. Matsuno discloses an "embodiment [that] is directed to a NAND flash memory." Ex-1005, 2:44-45; *see id.*, 2:50-54 (providing a NAND flash memory configuration with "a part of memory cell array formed in a memory cell region of the NAND flash memory. The memory cell array is comprised of NAND cell units (memory units) Su arranged in a matrix").

b. Element 1[a]: a semiconductor substrate;

71. Matsuno discloses a semiconductor substrate. Ex-1005, 5:1-6:14. Matsuno discloses "a method of fabricating a semiconductor device comprising forming an insulating film and a core-forming film above *a semiconductor substrate.*" *Id.*, 1:56-58; 2:15-17 (providing "a semiconductor device comprising a semiconductor substrate"). The semiconductor substrate 1 is red in Matsuno's Figure 3 below.

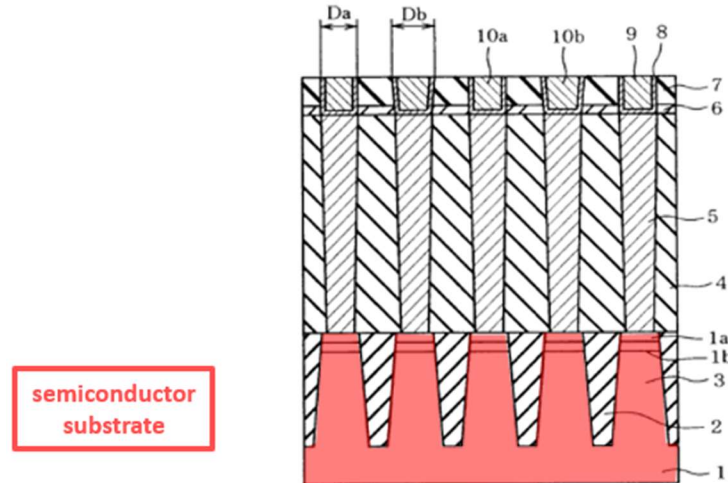


FIG. 3

Id., Fig. 3 (annotated).

c. **Element 1[b]: a dielectric layer extending over the semiconductor substrate;**

72. The '974 Patent states “memory elements are arranged in a plane (e.g., in an X-Z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements.” Ex-1001, 4:64-5:3, 5:15-35. It further states “[t]ypically, in a monolithic three dimensional memory array, *one or more memory device levels are formed above* a single substrate.” *Id.*, 5:49-51. It also states “layers of adjacent memory device levels of a monolithic three dimensional memory array *may be shared or have intervening layers* between memory device levels.” *Id.*, 5:58-61. The '974 Patent does not describe any embodiment where a dielectric layer that is etched to form trenches is deposited

directly onto, or in direct contact with a semiconductor substrate. *See, e.g., id.*, Figs. 2C, 3A-3C, 4A-4D. Therefore, a POSITA would have understood that, as recited in the claims and used in the context of the specification, the recited dielectric layers being placed “over” the semiconductor substrate encompasses layers that are above an underlying semiconductor substrate, even if there are “intervening layers” between them.

73. Consistent with the '974 Patent's description, Matsuno teaches a dielectric layer extending over the semiconductor substrate. Specifically, Matsuno includes several films layered over the semiconductor substrate. Ex-1005, 1:55-58, 3:11-14. For example, Matsuno describes silicon oxide film 4 formed on the upper surface of silicon substrate 1; silicon nitride film 6 formed on silicon oxide film 4; silicon oxide film 7 formed on the upper surface of silicon nitride film 6; and silicon nitride film 11 formed on the upper surface of silicon oxide film 7. *Id.*, 3:49-67, 4:49-59, Fig. 3. Figure 3 below shows silicon oxide film 7 (purple), after trenches have been formed, extending over semiconductor substrate 1 (red). *Id.*, 4:1-6. Matsuno also states its Figures 4-11 show “part of the structure in which the first and second buried wirings 10a and 10b are formed,” while “another part related to the silicon substrate 1 is eliminated.” *Id.*, 4:41-48. Figure 4 annotated below discloses silicon oxide film 7 (purple) without the trenches formed. Although silicon substrate 1 is

not shown, a POSITA would have understood silicon oxide film 7 extends over silicon (semiconductor) substrate 1.

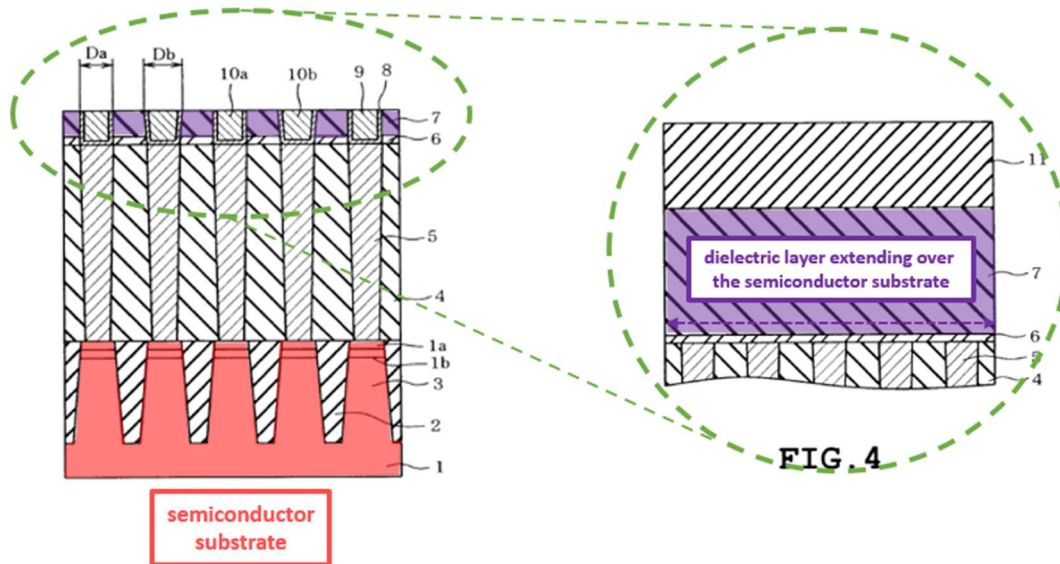


FIG. 3

Ex-1005, Figs. 3 and 4 (annotated and modified).

74. A POSITA would have known that silicon oxide is a dielectric material.

Ex-1035, 17. Indeed, silicon oxide is a more “favorable” dielectric material than silicon nitride for spacers because it allows for a more uniform voltage distribution across cell arrays. Ex-1032, 37. Because the trenches are etched in silicon oxide film 7, silicon oxide film 7 corresponds to the claimed dielectric layer extending over semiconductor substrate. Thus, Matsuno discloses a dielectric layer extending over the semiconductor substrate.

- d. **Element 1[c]: a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;**

75. Matsuno discloses first trenches etched in the dielectric layer. Specifically, Matsuno discloses trenches etched in silicon oxide film 7 between tapered wiring groove patterns 7a (purple). As shown by Figure 10 annotated below, first trenches (yellow) are formed between tapered wiring groove patterns 7a that make up the facing pair Aj are elongated along a first direction.

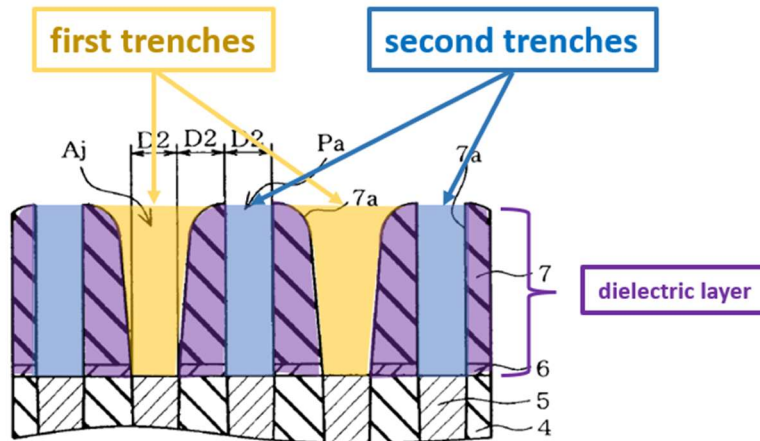


FIG. 10

Ex-1005, Fig. 10 (annotated).

76. Matsuno states “silicon oxide film 7 is etched at each adjacent pair Aj so as to have tapered surfaces reaching the lower ends, whereupon the wiring groove patterns 7a are formed.” *Id.*, 6:6-9. Thus, the first trenches (yellow) are of a shape in

cross section along a plane that is perpendicular to the first direction that is wider at the top because of the tapered surfaces than their lower portions.

- e. **Element 1[d][i]: a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane,**

77. Matsuno describes another set of trenches etched between the facing pair Pa of wiring groove patterns 7a. Specifically, Matsuno discloses “silicon oxide film 7 is etched at each facing pair Pa so as to have substantially vertical surfaces.” Ex-1005, 6:5-6. Thus, trenches formed between wiring groove patterns 7a (purple) that make up the facing pair Pa are elongated along a second direction are second trenches in the dielectric layer. This is illustrated in annotated Figure 10 below.

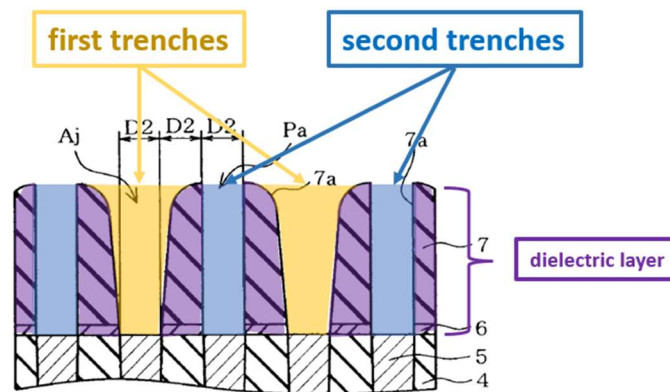


FIG. 10

Ex-1005, Fig. 10 (annotated).

78. Because “[e]ach facing pair Pa with the vertical side surfaces ha[s] the same inter-pattern dimension that is substantially the same as D2 throughout elongation thereof,” these trenches are of a second shape that is rectangular in cross section to the first direction. Ex-1005, 5:50-52.

f. Element 1[d][ii]: the second shape being different from the first shape,

79. Matsuno explains that the trenches etched between each adjacent pair Aj are tapered with “upper ends which are further spread” than the lower end of the trench, whereas the trenches etched between each facing pair Pa are generally the same width throughout the elongation. Ex-1005, 6:5-17.

80. Matsuno’s Figure 10 shows that the first trenches (yellow) and second trenches (blue). Because the first trenches reduce in width from the upper region to the lower region (i.e., trapezoidal) and the second trenches are the same width (e.g., rectangular), the shape of the second trenches (i.e., second shape) is different from the shape of the first trenches (i.e., first shape).

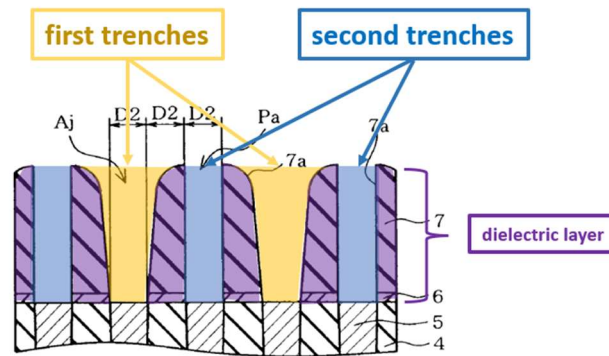


FIG. 10

Id., Fig. 10 (annotated).

81. After metal layers are deposited into the trenches, the planarization process polishes the dielectric layer and metal layers to a predetermined height. Ex-1005, 6:18-31. As shown by Figure 11 below, after planarization, first trenches (yellow) are trapezoidal and second trenches (blue) are rectangular.

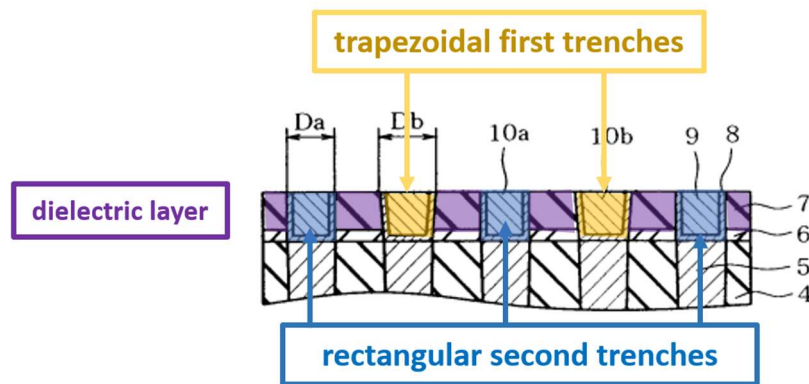


FIG. 11

Ex-1005, Fig. 11 (annotated).

- g. **Element 1[d][iii]: the first and second trenches arranged in an alternating pattern that alternates from first trench to second trench along a second direction that is perpendicular to the first direction; and**

82. Matsuno discloses “a plurality of first buried wirings and a plurality of second buried wirings provided in the insulating film at predetermined intervals *alternately* in a direction parallel to a surface of the semiconductor substrate.” Ex-1005, 2:18-21. Matsuno explains that “first buried wirings 10a are formed in the respective facing pairs Pa, and the second buried wirings 10b are formed in the respective adjacent pairs Aj.” *Id.*, 6:29-31. Second buried wirings 10b are formed in first trenches, whereas first buried wirings 10a are formed in second trenches. As shown by annotated Figure 11 below, first trenches (yellow) and second trenches (blue) are in an alternating pattern. *See* Ex-1005, 4:8-11 (“The first and second wirings 10a and 10b are formed so as to correspond to the bit lines BL1 and BL2 which are disposed cyclically and *alternatively*, respectively.”).

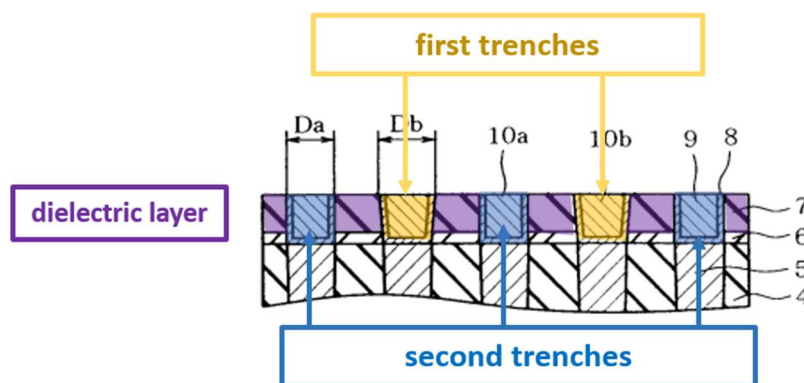


FIG. 11

Ex-1005, Fig. 11 (annotated).

83. Relative to Matsuno's Figure 11, the first direction is the direction going into the page. The alternating pattern alternates in a second direction (left-to-right) which is perpendicular to the first direction.

h. Element 1[e]: a plurality of bit lines located in the first trenches.

84. Matsuno discloses “[c]onductor films comprising a barrier metal layer 8 and a copper (Cu) layer 9 are buried in the pattern thereby to be formed into first and second buried wirings 10a and 10b...*The first and second wirings 10a and 10b are formed so as to correspond to the bit lines BL1 and BL2 which are disposed cyclically and alternately, respectively.*” Ex-1005, 4:3-11, 6:18-24. Annotated Figures 2 and 3 show Matsuno’s bit lines BL2 (10b) in yellow in the first trenches.

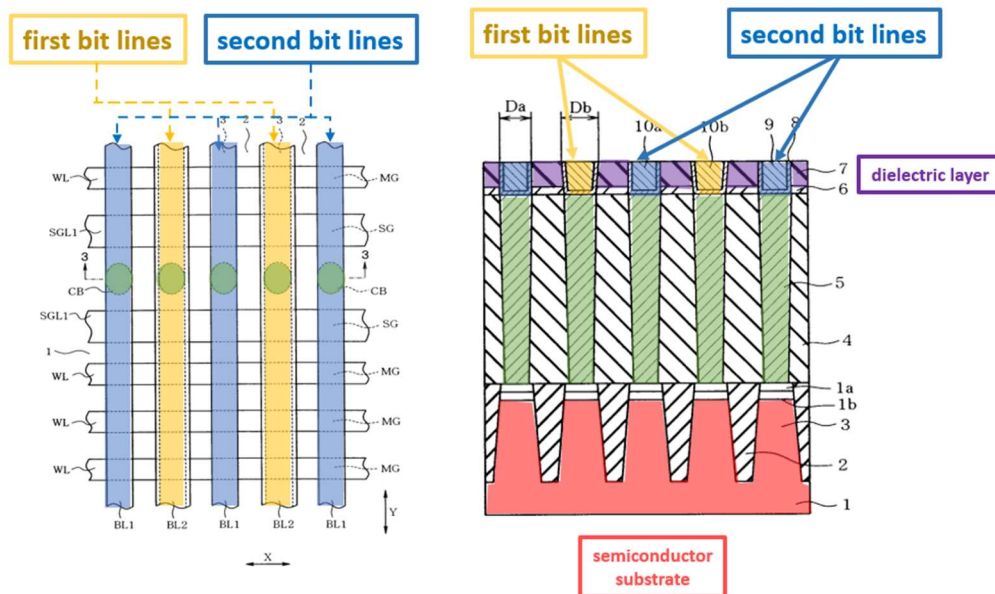


FIG. 2

FIG. 3

Id., Figs. 2-3 (annotated).

- 2. Dependent Claim 2: The NAND flash memory of claim 1 further comprising**
[a] a plurality of additional bit lines located in the second trenches,
[b] each of the plurality of bit lines having the first shape in cross section along the plane and each of the plurality of additional bit lines having the second shape in cross section along the plane.

85. Matsuno discloses additional bit lines located in the second trenches. Matsuno states “the first buried wirings 10a are formed in the respective facing pairs Pa.” Ex-1005, 6:31-32; *see id.*, 4:3-6 (barrier metal layer 8 and copper layer 9 form “first and second buried wirings 10a and 10b”). A POSITA would have understood that the metal layers making up second buried wiring 10a are bit lines. Thus, second buried wirings 10a are located in second trenches Pa. Annotated Figures 2-3 show Matsuno’s bit lines BL1 or 10a in blue.

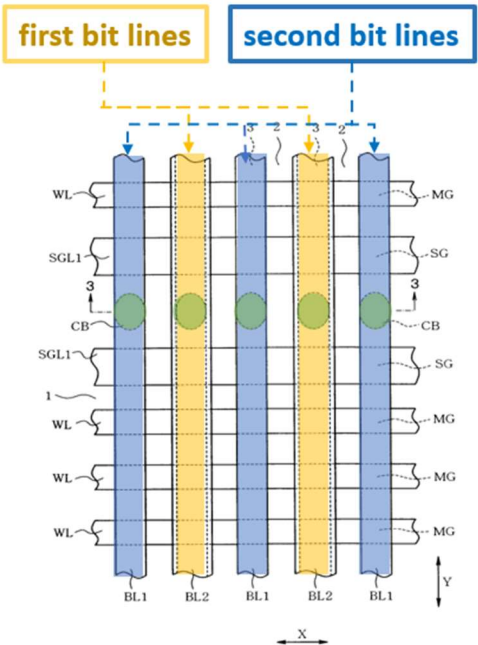


FIG. 2

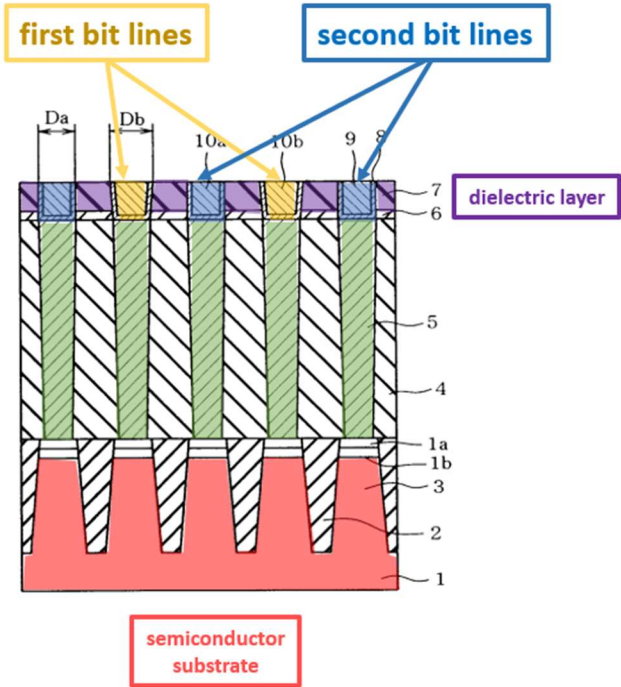


FIG. 3

Id., Figs. 2-3 (annotated).

86. Matsuno also discloses the bit lines having the first shape in cross section along the plane and the additional bit lines having the second shape in cross section along the plane. Because “buried wirings 10b are formed in the respective adjacent pairs Aj and the wiring groove patterns 7a have the tapered surfaces,” the bit lines (i.e., buried wirings 10b) have the first shape of the first trenches. Ex-1005, 6:35-40. Because “the first buried wirings 10a are formed in the respective facing pairs Pa,” the additional bit lines (i.e., buried wirings 10a) have the same shape as the second shape (i.e., the shape of the second trenches). *Id.*, 6:31-35.

3. **Dependent Claim 4: wherein the first shape has a first width at a level of an upper surface of the dielectric layer, the second shape has a second width at the level of the upper surface of the dielectric layer, and the second width is less than the first width.**

87. Matsuno states “the second buried wiring 10b is formed so that *the upper portion thereof has a larger wiring width* than the first buried wiring 10a and the lower portion thereof has substantially the same wiring width as the first buried wiring 10a.” Ex-1005, 4:25-29. Because of the planarization process, the upper portions of the buried wirings are flush with the upper surface of the dielectric layer. See Ex-1005, 6:18-28. As explained in Sections X.A.1.d-e, the buried wiring 10b takes on the first shape of the first trench and the buried wiring 10a takes on the second shape of the second trench. Matsuno discloses “the width of each wiring 10b is *wider at the upper surface* thereof as shown by reference symbol ‘Db’ and is substantially the same as dimension Da at the lower end,” whereas second trenches 10a have a width of Da from the upper surface to the lower end, as illustrated by Figure 11 below. Ex-1005, 6:38-40.

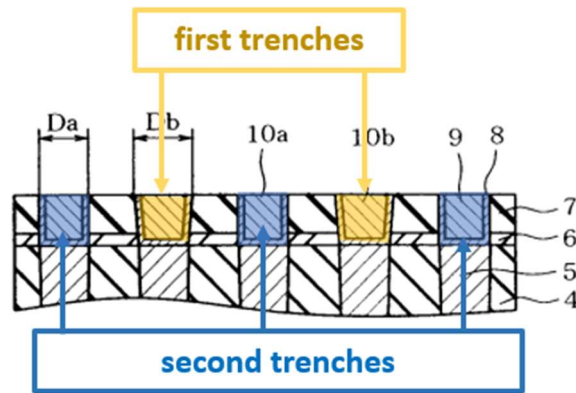


FIG. 11

Id., Fig. 11 (annotated).

4. Independent Claim 12

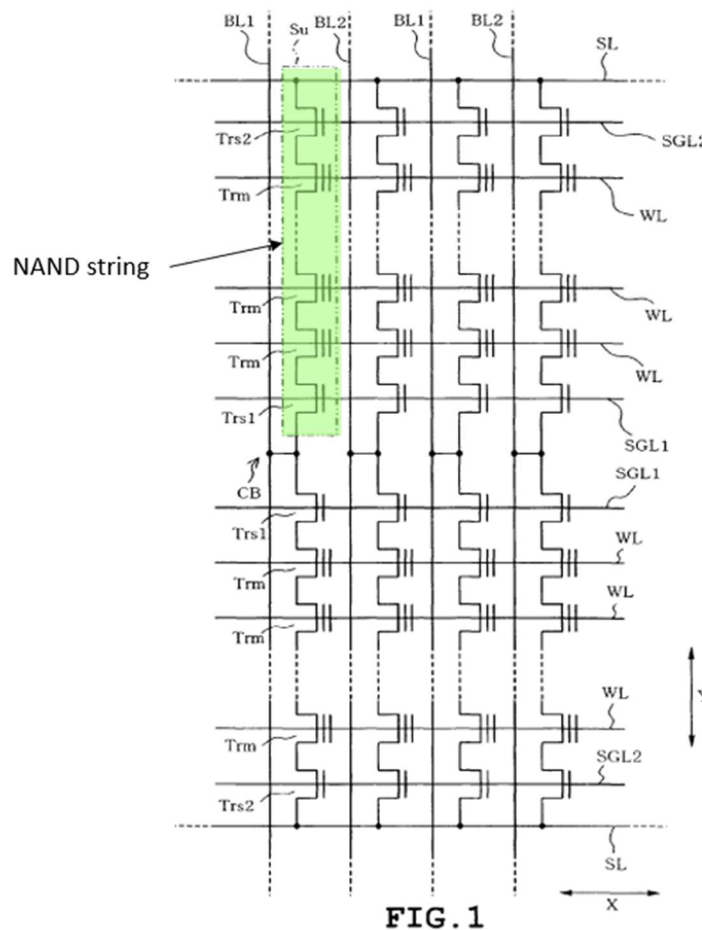
a. Element 12[preamble]: A method of forming a NAND flash memory comprising:

88. If Claim 12's preamble is limiting, Matsuno discloses the preamble. Matsuno discloses its "present invention relates to a method of fabricating a semiconductor device provided with a microscopic wiring pattern." Ex-1005, 1:16-18. Matsuno also teaches an "embodiment [that] is directed to a NAND flash memory." *Id.*, 2:44-45.

b. Element 12[a]: forming a plurality of NAND strings disposed on a surface of a substrate;

89. Matsuno discloses a "memory cell array is composed of NAND cell units (memory units) Su arranged in a matrix. Each NAND cell unit includes two selective gate transistors Trs1 and Trs2 and a plurality of memory cell transistors Trm (2^n where n is a positive number, 8, for example) series connected between the

selective gate transistors Trs1 and Trs2. In the NAND cell units Su, the memory cell transistors Trm adjacent to each other are arranged to share a single source/drain region.” Ex-1005, 2:53-61. A POSITA would have understood Matsuno’s NAND memory cells connected in series with the shared source and drain region as outlined by Su and annotated in green below constitute a NAND string.



Ex-1005, Fig. 1 (annotated).

90. A POSITA would have known that NAND memory architecture is implemented using CMOS process technology, which uses conductive paths on a

substrate to connect NAND strings and arrays. Therefore, Matsuno's memory cell array is disposed on a surface of a substrate. *See* Ex-1005, 3:16-19 (substrate's surface "divided into a plurality of a active regions 3 (element formation regions)"); 3:26-28 ("Gate electrodes MG of the memory cell transistors...formed on the portions of the action region 3...."); 2:15-17 (providing "a semiconductor device comprising a semiconductor substrate").

c. Element 12[b]: depositing a dielectric layer over the plurality of NAND strings;

91. Matsuno discloses films "formed on the upper surface of the silicon substrate 1 so as to cover gate electrodes of the memory cell transistors Trm and selective gate transistors Trs1 and Trs2 or peripheral circuit transistors (not shown) etc." Ex-1005, 3:38-53. These transistors make up a NAND string. *See supra* Section X.A.4.b. As explained above, silicon oxide film 7 is a dielectric layer that extends over silicon oxide film 4 and semiconductor substrate 1. *See supra* Section X.A.1.c.

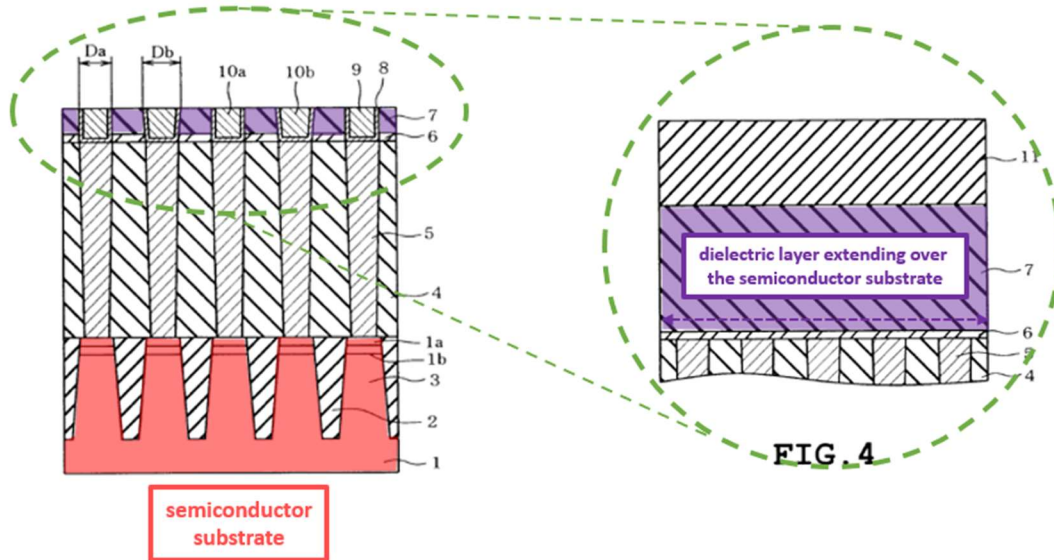


FIG. 3

See Ex-1005, Figs. 3-4 (annotated).

92. Thus, Matsuno teaches depositing a dielectric layer over the plurality of NAND strings.

- d. **Element 12[c]: etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;**

93. For the reasons set forth in Section X.A.1.d, Matsuno teaches “a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction.” Ex-1020. Matsuno further discloses “silicon oxide film 7 is *etched* at each adjacent pair A_j so as to have tapered surfaces reaching the lower ends,” as shown in Figure 10 below. Ex-1005, 6:6-7.

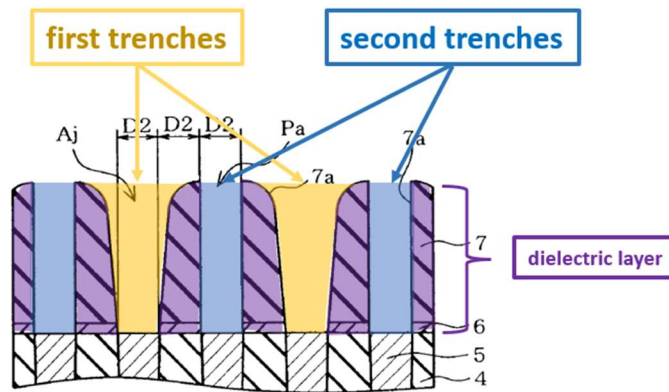


FIG. 10

Ex-1005, Fig. 10 (annotated).

- f. **Element 12[e]: the second shape being different to the first shape,**
Element 12[f]: the first and second trenches arranged in an odd-even alternating pattern along a direction that is perpendicular to the first direction such that two first trenches are separated by a second trench; and
Element 12[g]: depositing metal in the plurality of first trenches to form a plurality of bit lines located in the first trenches.

95. Matsuno teaches Elements 12[e]-[g] for the reasons set forth in Sections X.A.1.f-h. *See* Ex-1020.

5. Dependent Claim 15: The method of claim 12 further comprising depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches.

96. Matsuno teaches “depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches” for the same reasons it teaches Claim 2. *See supra* Section X.A.2.

B. Ground 2: Claims 6, 11, and 16 Are Obvious Over Matsuno in view of Zhang

97. As shown below, the subject matter of Claims 6, 11, and 16 are taught by Matsuno in view of Zhang.

1. A POSITA would have been motivated to combine Matsuno with Zhang

98. A POSITA would have been motivated to combine the teachings of Matsuno and Zhang and would have had a reasonable expectation of success in doing so at least because they relate to the same field and address the same well-known issues. Matsuno and Zhang provide complementary solutions for fabricating interconnects with certain structural and electrical configurations in semiconductor devices. *See, e.g.*, Ex-1005, 1:16-2:26, 2:44-51; Ex-1006, ¶¶4, 6, 31-35, 40-46. A POSITA seeking flexibility or precision in the patterning process would have known of and consulted these proposed solutions. Ex-1005, 1:40-51; *see* Ex-1006, ¶¶2, 9.

99. Matsuno discloses fabricating a “NAND flash memory” configured to have “first buried wirings 10a...formed in the respective facing pairs Pa, and the

second buried wirings 10b...formed in the respective adjacent pairs Aj.” Ex-1005, 6:29-31. This results in two trench shapes: a substantially vertical trench (e.g., 10a) and a tapered trench (e.g., 10b). Matsuno states this configuration is advantageous because, “even when an overhang is formed on the rounded portion or the like during the forming of the barrier metal layer 8 by a sputter method, the above-described configuration can suppress adverse effect on the subsequent forming of the copper layer 9...In this respect, when the width of the wiring groove pattern in each adjacent pair Aj is small so that the aforesaid overhang occurs during the forming of a barrier metal layer, an effective width is reduced such that there is a possibility of malfunction in burying such as occurrence of void in the adjacent pair Aj during the plating of copper layer. However, the above-described configuration can suppress the occurrence of malfunction as much as possible.” *Id.*, 6:41-60. Matsuno further discloses another advantage in its configuration: the “contact areas of the first and second buried wirings 10a and 10b with the respective contact plug 5 are substantially equal to each other...Consequently, the variations in the contact resistance can be suppressed.” *Id.*, 6:61-7:3.

100. A POSITA would have known that as memory technology and integration density advanced, the distance between the bit lines would continue to decrease. As the distance between the bit lines decreased, the inter bit line capacitance would increase proportionally, which would result in negative effects

on memory performance because the current consumption and accuracy of sense current are dependent on the overall bit line capacitance, and that for a given bit line, the inter bit line capacitance is a significant component to the overall bit line capacitance. Consequently, an increase in inter bit line capacitance causes the bit line sensing margin and refresh ability to degrade, in addition to increasing the current consumption of the NAND memory. *See, e.g.*, Ex-1039, N3029. Figure 18.5 of Micheloni illustrates that a major contributor of bit line capacitance is the inter bit line capacitance, especially as NAND memory cells scale down. Ex-1021, 518.

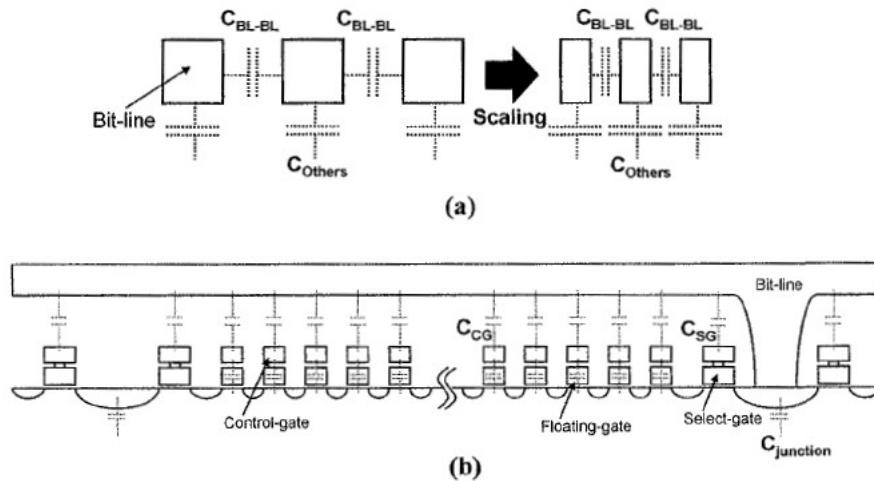


Fig. 18.5. Cross sectional view of (a) a bit-line and (b) a NAND Flash memory cell

101. Zhang discloses forming air gaps within dielectric materials above a semiconductor substrate so as to achieve “low capacitance between metal lines.” Ex-1006, ¶¶40-46, 64. Accordingly, a POSITA would have been motivated to implement Matsuno’s NAND memory configuration using Zhang’s air gaps because a POSITA would have recognized that—as stated in Zhang—“incorporation of an

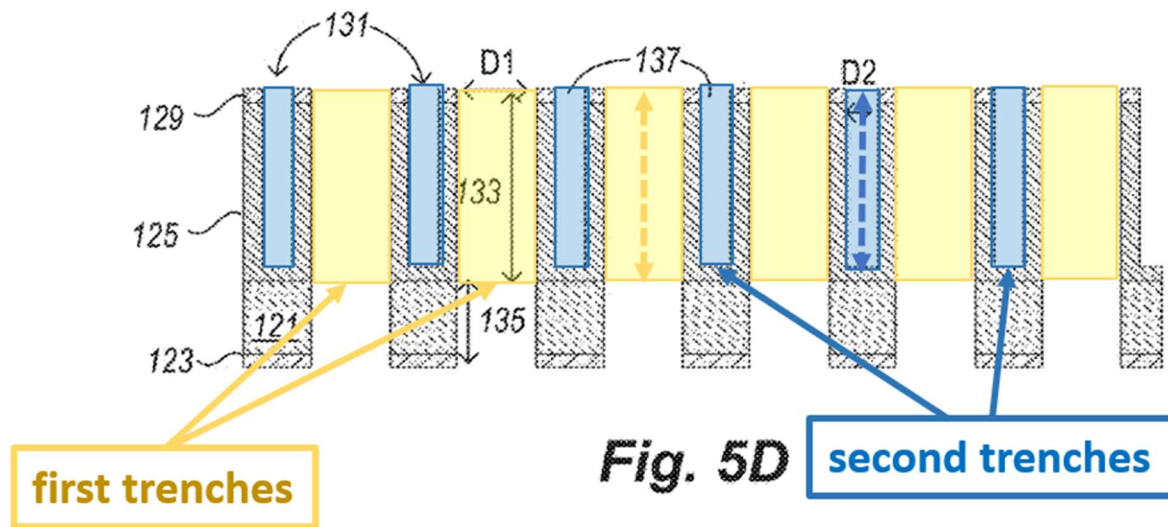
air gap in a layer” “reduce[s] capacitance between adjacent” conductive lines and mitigates the effects of the reduction in the inter bit line spacing. Ex-1006, ¶¶9-10, 55, 64. A dielectric constant of an insulating material is the measurement of the insulator’s ability to store electric energy. Zhang explains that “the dielectric constant of the air is 1.0 and it is substantially smaller than that of any other material.” *Id.*, ¶55. A dielectric material with a higher dielectric constant will increase the capacitance. Therefore “it is desired to have the air gap as large as practical within the constraints of the materials used and to provide sufficient structural integrity ... after the metal is deposited.” *Id.* A POSITA would have known that air gaps are therefore meant to be placed between adjacent metal lines that are spaced tightly apart, rather than be incorporated into working metal bit lines due to reliability issues. Zhang discloses that the disclosed air gap structure provides an “effective dielectric constant is less than 2.0,” but the structure “still provid[es] advantageous structural properties. Thus, holes essentially have been incorporated into the dielectric material in an organized fashion so as not to weaken the overall interconnect structure. ***Such a low dielectric constant achieves a low capacitance between the metal lines.***” *Id.*, ¶64 (emphasis added). A POSITA would have recognized the proposed combination of Matsuno in view of Zhang benefits from Matsuno’s more tailored profile for its first trenches (e.g., wider mouth allows for

fewer voids/more reliable bitlines), while also benefiting from reduction in capacitance between the first bitlines as taught by Zhang.

102. With this combination, a POSITA would have had a reasonable expectation of success in achieving the objective of decreasing the capacitance between bit lines by combining the teachings of Matsuno and Zhang without change in their respective functions because both references use “conventional thin film deposition[,], photolithography[, and] etching techniques” to fabricate semiconductor devices. Ex-1006, ¶¶32-35, 40-46; *see generally* Ex-1005 (using deposition, photolithography and etching techniques); *see infra* Sections X.B.2-4.

2. Dependent Claim 6: The NAND flash memory of claim 1 further comprising a plurality of air gaps located in the second trenches.

103. Zhang discloses air gaps located in second trenches. Zhang discloses incorporating air gaps into dielectric material to lower the “effective dielectric constant” of “interconnect structure[s].” Ex-1006, ¶10. Zhang’s Figure 5D annotated below illustrates first trenches (yellow) between U-shaped structures and second trenches (blue) within the U-shaped structures.

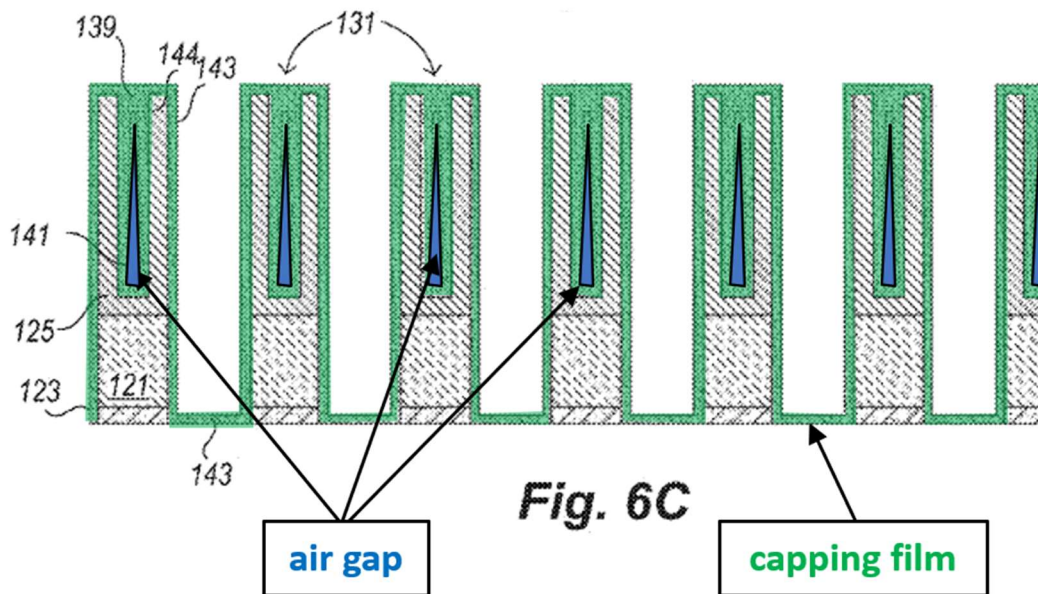


Id., Fig. 5D (annotated).

104. Zhang discloses at step “134, the recesses 137 of the U-shaped structures 131 are capped with a layer 139. The capping layer 139 will cap each U-shaped structure so as to include an air gap 141, thus forming a plurality of air gaps 141 that extend vertically within the recesses 137.” Ex-1006, ¶55. Zhang therefore discloses incorporating air gaps into second trenches.

105. Zhang explains that the width of the second trench “D2 is selected to ensure that adjacent capping layers 139 will touch each other at the top opening of the U-shaped structures 131 to seal off the top and form a sealing cap before the central portion of the region is fully formed to ensure that the air gap 141 remains.” Ex-1006, ¶55. Zhang describes a capping layer that “result[s] in the cap being formed almost immediately upon the deposition starting so that little to no material from the capping layer 139 enters the U-shaped structure 131. Therefore, the top of

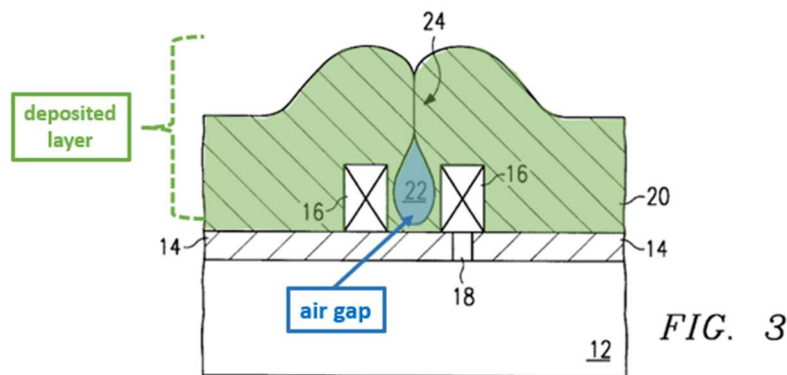
the U-shaped structure 131 will be essentially capped and maintain nearly the same open area as when it was originally etched.” *Id.* Figure 6C of Zhang below illustrates the capping layer 139 lining both the first and second trenches, resulting in air gaps formed in second trenches.



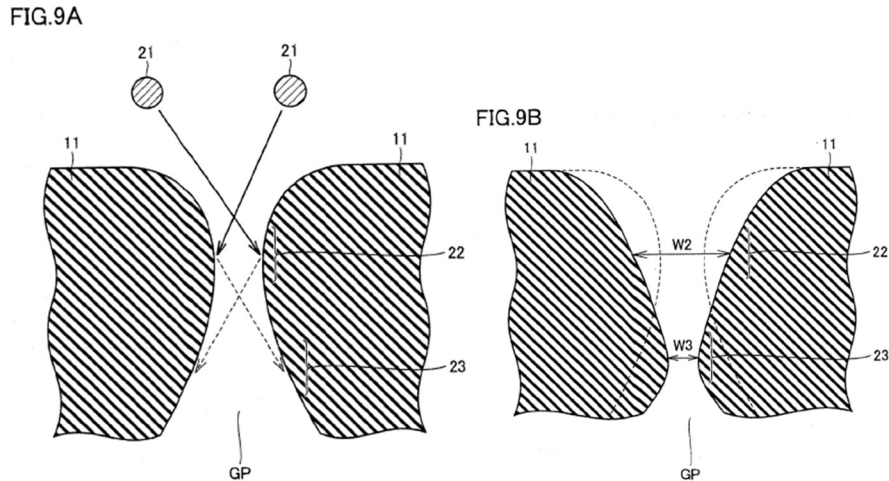
Id., Fig. 6C (annotated).

106. A POSITA would have found it obvious to incorporate air gaps into the second trenches of Matsuno in view of Zhang’s teachings. A POSITA would have known that air gaps replace dielectric material, and are not meant to exist inside bitlines or metal lines. Matsuno discloses “barrier metal layer 8 is formed in the wiring groove patterns 7a by sputtering as shown in FIG. 11.” Ex-1005, 6:18-19. A POSITA implementing air gaps between bit lines in the first trenches would have understood that depositing the barrier metal layer 8 that is thick enough to

encapsulate the tops of the second trenches results in air gaps formed in the second trenches, like Zhang's teachings. A POSITA would know that the barrier metal layer inside the second trenches would not be used to carry any electrical signals. *See* Ex-1006, ¶55. A POSITA would have further understood that a high deposition rate or deposition of a thick enough material results in "breadloafing," which causes the material to "pinch off" in a region between sidewalls and form an air gap, as illustrated below. Ex-1026, Fig. 3 (annotated).



107. For a pinch-off region below the surface, a POSITA would have known how to use a sputtering deposition method to facilitate a pinch-off region below the surface of a dielectric layer. *See* Ex-1031, ¶99, Figs. 9A-9B.



Ex-1031, Figs. 9A-9B.

108. A POSITA would know, similar to the technique described by Murata in Ex-1026, the sputtering deposition process can be tailored, illustrated in Figs. 9A-9B above, such that the accelerated charge particle 21 can collide with sputtering region 22. This would etch the regions close to the surface of the opening, and deposition and redeposition would occur at the region 23, which is lower than the surface of opening, thereby allowing the pinched off region to be formed around region 23, i.e., closing the opening at W3.

109. Thus, a POSITA would have known how to deposit a layer to create an air gap. Modified Figure 10' of Matsuno shown below illustrates a pinch-off region toward the top of the second trenches, resulting in air gaps in the second trenches (blue). Ex-1026, Fig. 3.

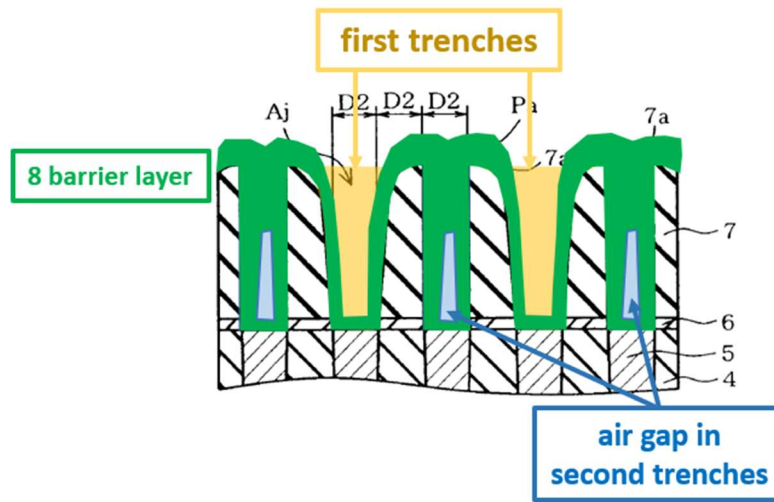


FIG. 10'

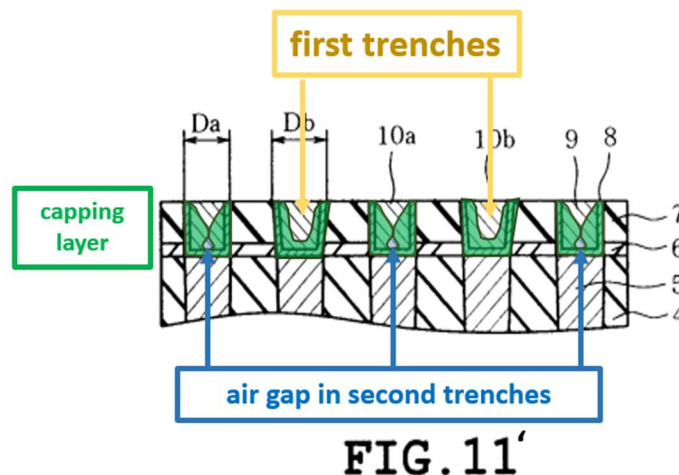
Ex-1005, Fig. 10' (modified).

110. A POSITA would have known how to adjust the thickness of the capping metal layer to enclose an air gap. For this modification, deposition of a metal layer would be with a tailored profile and thick enough to seal off second trenches to form an air gap while the first trenches are not filled up at the top, like the profiles in Figure 6C of Zhang. A POSITA would have known to continue the rest of Matsuno's process—which is deposition of copper layer 9—resulting in bit lines formed in the first trenches, but not in the second trenches.

111. Although the deposition of a thick capping metal layer results in an uneven top layer, Matsuno's subsequent planarization would level and polish "the copper layer 9 and barrier metal layer 8" to their "respective predetermined heights." Ex-1005, 6:18-28. A POSITA would have known how to determine a height or where to position a pinch-off region to preserve the air gaps in the second trenches

after planarization. *See* Ex-1031, ¶¶99, Figs. 9A-9B. Again as described above, a POSITA would have known that a sputtering deposition technique can be used where the region below the top surface would be closed off (pinched off) due to the retrograded nature of the sputtering-redeposition method in the metal deposition process. Subsequent planarization with this retrograde profile prevents shorting the bit lines.

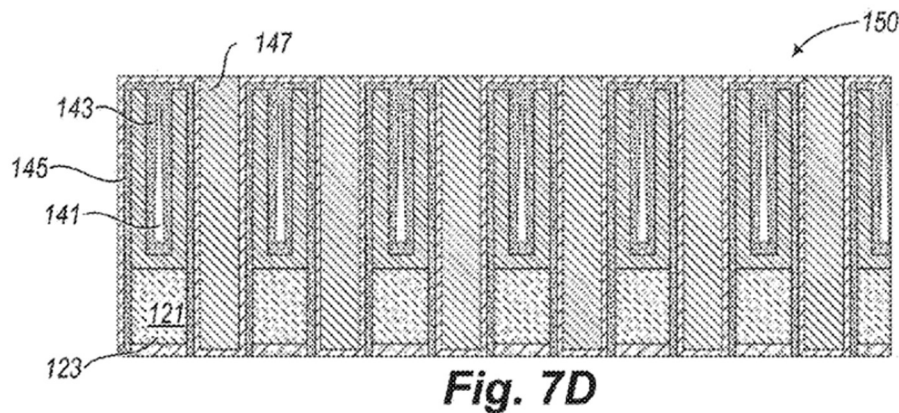
112. Because air gaps were incorporated into the second trenches, the resulting configuration leaves a portion of the metal barrier layer forming the cap in the second trenches that maintain the air gaps, while the bit lines formed in the first trenches from the barrier metal layer and copper layer remains. Modified Figure 11' of Matsuno below illustrates the resulting configuration of bit lines in the first trenches (yellow) with air gaps in the second trenches (blue).



Ex-1005, Fig. 11' (modified).

113. A POSITA would have recognized implementation details depend on desired benefits and having to make tradeoffs. For example, a POSITA seeking to implement Matsuno in view of Zhang using minimum spacing rules would have known how to design the memory array beneath the bitlines such that the cells 5 beneath the active bitlines in the first trenches are connected to the active area, whereas the cells 5 beneath the air gaps in the second trenches are not connected to the active area.

114. In another example, a POSITA willing to use more space would have known how to align air gaps to underlying dielectric material and bitlines to underlying metal connects. Figure 7D of Zhang illustrates this understanding, with its air gaps 141 in trenches 143 above a dielectric material 123, while its bitlines 147 may connect to underlying metal contacts. Ex-1006, 7:63-8:3, 10:44-60, 11:20-24.



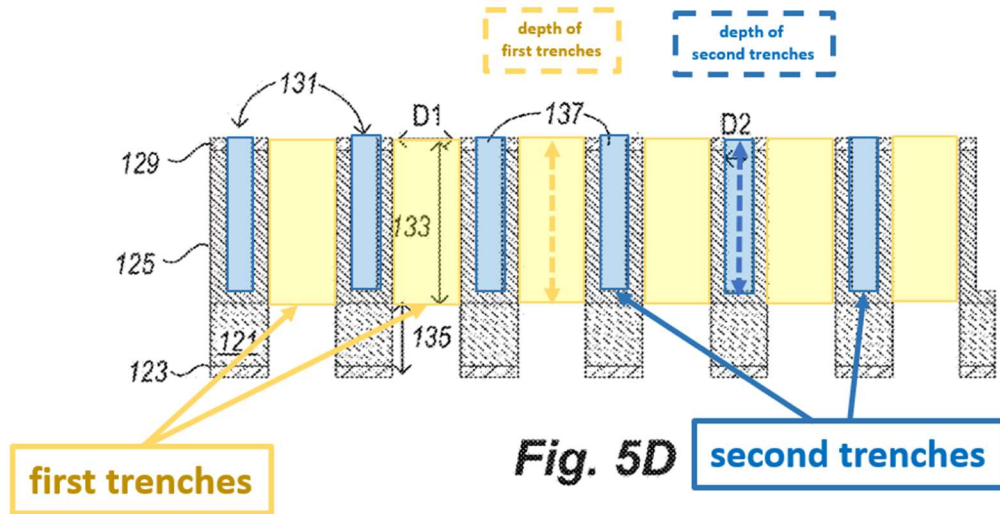
Ex-1006, Fig. 7D.

115. Under either implementation, a POSITA would have been motivated to put air gaps between the bit lines of the first trenches to reduce overall k-value, reduce capacitance, and improve RC relay. *See, e.g.,* Ex-1006, ¶5 (“reduce capacitance between adjacent nanowires”). A POSITA would have had a reasonable likelihood of success because methods of creating air gaps with sealing caps was one of many known tools available to improve the capacitive properties of conductive interconnects, such as bit lines. Therefore, Matsuno in view of Zhang teaches Claim 6.

3. Dependent Claim 11: The NAND flash memory of claim 1 wherein the plurality of first trenches have a first depth and the plurality of second trenches have a second depth that is different to the first depth.

116. Zhang describes two sets of trenches: a first set of the trenches 133 and a second set of trenches etched from “the high modulus insulator 125 between the [first] trenches...to form the U-shaped structures 131, with the etched recesses having a width D2.” Ex-1006, ¶50. Zhang discloses that vias 135 are formed directly under first trenches 133. *Id.* Zhang discloses while recesses 137 (or second trenches) has a depth that “will usually stop before reaching the ULK dielectric layer 121,...etching of the [first trenches 133 and vias 135 between the U-shaped structures 131 continues through the entire ULK dielectric layer 121, into the substrate 123.” *Id.* Annotated Figure 5D below shows that the depth of the first

trenches (blue dashed line) is deeper than the depth of the second trenches (yellow dashed line).



Ex-1006, Fig. 5D (annotated).

117. A POSITA, in view of Zhang, would have found it obvious to make the Matsuno's first trenches have a different depth than the depth of Matsuno's second trenches. For example, a POSITA wanting (1) first trenches to be electrically connected to the active areas of the substrate would have a depth that reaches the active areas themselves, and (2) second trenches to reduce capacitance between first trenches would have implemented a shallower depth than that of first trenches. A POSITA would have known different methods of etching trenches of different depths, like the methods taught in Zhang.

118. As an example of trenches electrically connecting to a substrate's active area, Figure 2.1 of Micheloni illustrates a case where different trench depths would

be required to implement contacts to the control gate and the source/drain of a flash memory cell. Ex-1021, 20.

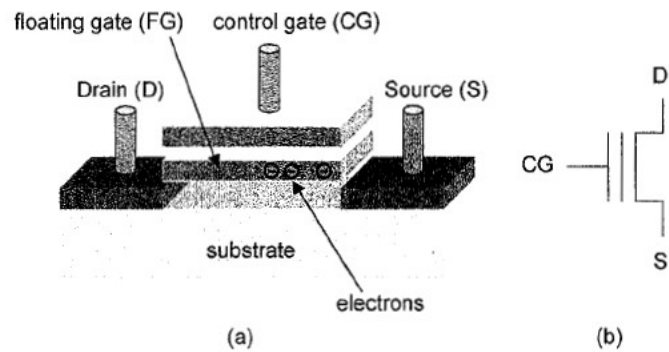


Fig. 2.1. (a) Floating gate memory cell and (b) its schematic symbol

119. As an example of shallower depths to reduce capacitance, especially applicable to Matsuno, a POSITA would know that by staggering the bit line contacts, that is by having the alternate bit line contact at a different location, would serve to reduce the capacitance between two adjacent bit lines with contacts. See Ex-1005, Fig. 2 (modified) below. Thus, the cross-section 3-3' of Fig. 2 would have alternating trench at different depth, since the even trench would not have the bit line contact at the cross-section location.

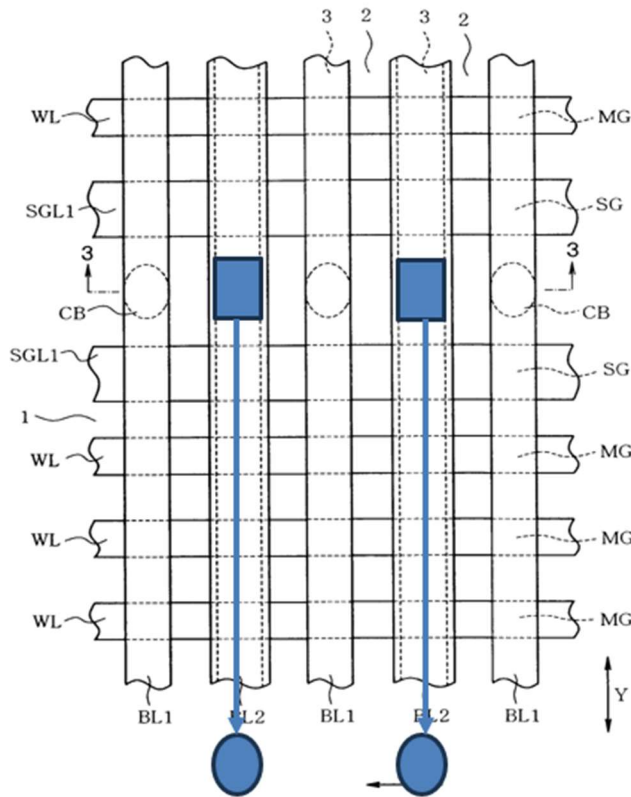


FIG. 2

120. A POSITA would have known different methods of etching trenches of different depths, like the methods taught in Zhang. Zhang achieves different depth through the use of (1) different material that have different etch rates (i.e., layer 121 etches faster than layer 125 due to the difference in dielectric constants), and (2) the width of the D2 is narrower than D1, resulting in a slower etch rate for the second trenches.

121. A POSITA would know that other methods can be used to achieve different depths between first trenches and second trenches. One example would be

the addition of the following steps: (1) depositing an etch stop layer between layer 125 and layer 121 prior to the trench etch, (2) depositing a liner material after the initial etching of layer 125, such that the liner layer would fill the width of D1 and only serving as a liner covering D2, (3) performing an additional etch to remove the etch stop layer in D2, and (4) removing liner layer and performing subsequent etching of layer 121 in D2.

122. A POSITA would have been motivated to have different depths for the first and second trenches in Matsuno's configuration because a trench's capacitance is directly proportionate to the trench's surface area. In another example, different depths for Matsuno's configuration may accommodate an array layout where the bit line contacts are not aligned on the same horizontal direction. A POSITA would have known how to adjust trench depths and spacing to optimize or obtain a specific capacitance or resistance.

4. Dependent Claim 16: The method of claim 12 further comprising depositing the metal in the plurality of second trenches to cap air gaps in the plurality of second trenches.

123. As explained in Section X.B.2, Matsuno-Zhang teaches deposition of a metal layer that results in air gaps in second trenches. *See* Ex-1020. A POSITA would have understood that after planarization, caps are formed from the metal layer that preserve the air gaps.

C. Ground 3: Claims 13-14 and 17-18 Are Obvious Over Matsuno in view of Kao

1. A POSITA would have been motivated to combine Matsuno with Kao

124. A POSITA would have been motivated to combine Matsuno with Kao and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Matsuno and Kao both provide solutions for manufacturing semiconductor devices with tight tolerances due to ever increasing integration density. *Compare* Ex-1005, 1:15-18, 2:44-45, *with* Ex-1007, 1:6-9, 1:27-32. A POSITA seeking to fabricate NAND memory devices, which uses MOSFET technology, would have known of and consulted these proposed solutions.

125. A POSITA would have found it obvious to use a dual-layer spacer like that taught in Kao to manufacture Matsuno's semiconductor device. Matsuno discloses techniques for manufacturing a semiconductor device using a sidewall transfer process using layer 13 formed over mandrels to construct its sidewall spacers. *See, e.g.*, Ex-1005, 1:16-18, 1:55-2:26, 2:43-49. Kao similarly discloses "a method of manufacturing a field effect transistor," using sidewalls of gates to form spacers. Ex-1007, 1:35-36, 1:45-51.

126. Kao specifically discloses forming sidewall spacers using portions of two dielectric layers that were formed together over a substrate. *See* Ex-1007, 1:39-

67. Kao describes “the problem caused by different diffusion rate of the different-type implanted ions can be solved by adjusting the thickness of the spacer. Therefore, the dopants with different diffusion rate can evenly diffuse in the substrate and the shape of the source/drain region can be well controlled.” Ex-1007, 3:25-31. Similarly, Matsuno explains that its disclosed configurations for wiring groove patterns address the “problem of a difference in the shape of the processed film.” Ex-1005, 1:46-51, 6:41-60. Both Matsuno and Kao show a POSITA’s desire to have more precise control in creating a custom sidewall profile. For example, Figures 7-9 of Matsuno disclose sidewall spacers. Kao describes forming multiple dielectric layers to form a sidewall spacer. *See* Ex-1007, 2:45-60, Figs. 3, 4. A POSITA would have found it obvious to implement bit lines, like those in Matsuno, with a custom sidewall profile to achieve certain processing or performance requirements. Sidewall spacers with tailored thickness, materials, or density can enhance etch and implantation process windows, which provide greater flexibility and reliability in advanced process nodes, through the ability of obtaining better physical profiles of the process features. More precise or customized sidewall spacers can also increase yield and process repeatability by accommodating tighter tolerances. For example, customized sidewall spacers can reduce capacitance, resulting in improved performance, such as switching speeds or lower power consumption. Spacer customization also allows POSITAs to fine-tune the distance and dielectric

environment between the gate and drain, further suppressing unwanted capacitance and minimizing potential signal delays or leakage. *See* Ex-1005, Fig. 7.

127. A POSITA would have had a reasonable expectation of success in achieving their objectives, e.g., manufacturing a semiconductor device using sidewall spacers, by combining the teachings of Matsuno and Kao with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of manufacturing semiconductor memory using mask and etching techniques. *See* Ex-1030, Fig. 9; *see infra* Sections X.C.2-5.

2. Dependent Claim 13: The method of claim 12 further comprising, prior to etching the plurality of first trenches and the plurality of second trenches, forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.

128. Matsuno discloses an etch mask comprising a sidewall spacer. Specifically, Matsuno discloses “forming a plurality of mask patterns by anisotropically etching the mask-forming film until the upper surfaces of the core patterns are exposed.” Ex-1005, 1:59-65, 4:65-5:24. Figures 7 and 8 show mask patterns 13a etched from amorphous silicon film 13, with mask patterns 13a right against the sides of core patterns 11a.

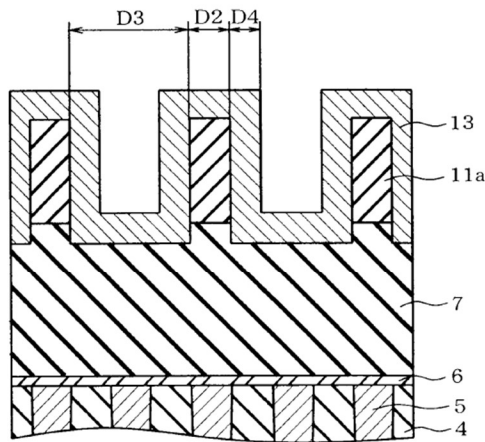


FIG. 7

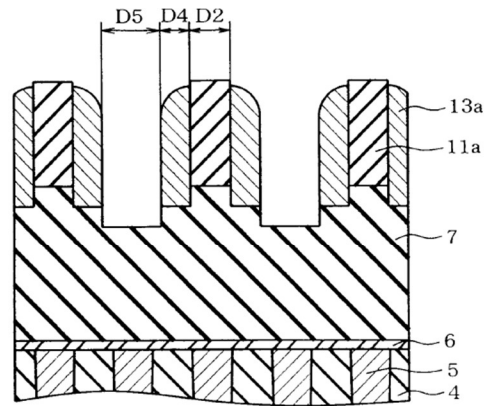


FIG. 8

Id., Figs. 7-8.

129. Kao discloses a mask portion formed with both “a first material and a liner part that is formed of a second material.”

130. Kao discloses “dielectric layer 114 is formed over the substrate 100” and made from silicon oxide. Ex-1007, 2:39-41. Kao then discloses “dielectric layer 116, which is made of silicon nitride, “is formed on the dielectric layer 114,” which is made of silicon nitride. *Id.*, 2:39-43. Kao further describes subsequently etching dielectric layers 116 and 114 to form “first spacer 116b...located at the sidewall of the gate 106a” and “remaining dielectric layer 114a,” respectively. *Id.*, 2:44-66. Dielectric layer parts 114a and 116b “together form a third spacer 117.” *Id.*, 2:66-67. Kao’s Figures 2 and 5 annotated below show a mask portion comprising sidewall spacer material 116b (pink) and liner 114a (cyan) made of different materials that corresponds to claimed mask portion.

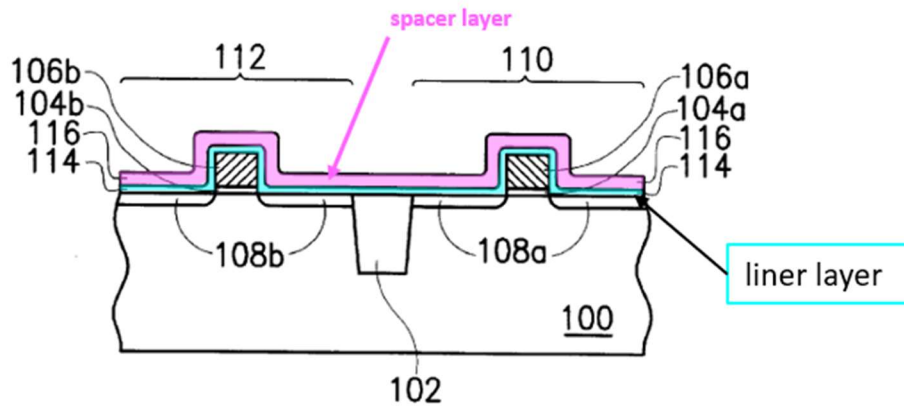


FIG. 2

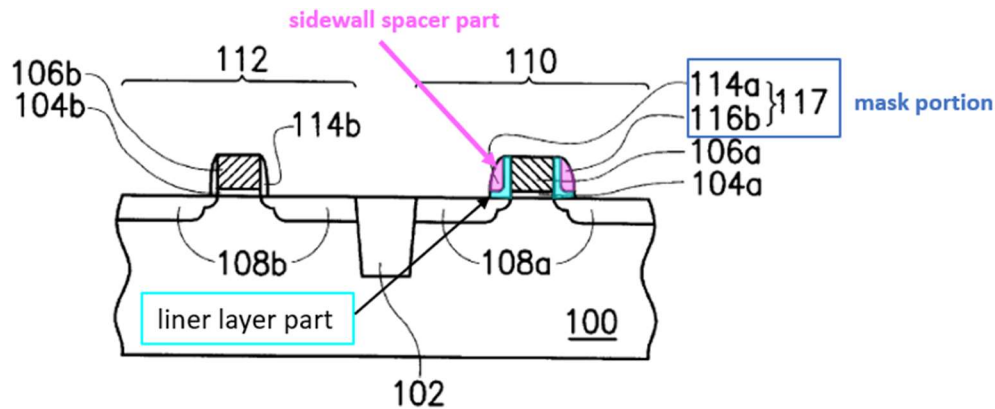


FIG. 5

Ex-1007, Figs. 2, 5 (annotated).

131. A POSITA would have found it obvious to do combine Matsuno and Kao. A POSITA would have motivated to combine Matsuno with Kao because a liner layer under a sidewall spacer layer can act as an etch stop for subsequent etching. Using a liner layer under a subsequent spacer layer was known in the art, specifically where the liner layer acts as an etch stop. *See* Ex-1034, 4:58-5:13. Modified Figure 6' below illustrates a liner layer (cyan), as taught by Kao, formed

along side surfaces of core patterns 11a and over the exposed parts of silicon film 7 in Matsuno.

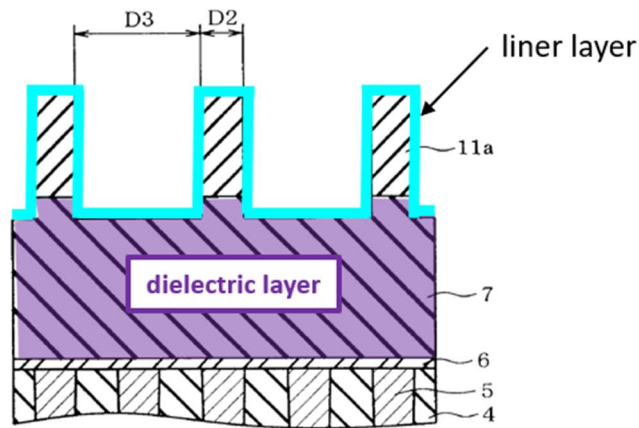


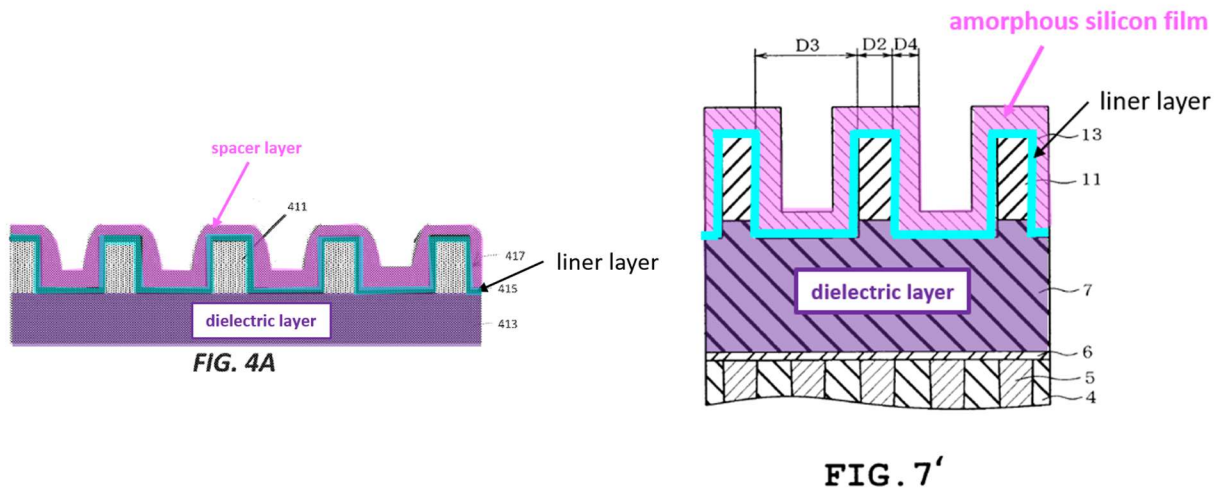
FIG. 6'

Ex-1005, Fig. 6' (modified).

132. A POSITA would have known that by modifying Matsuno's steps to deposit an additional liner layer over core patterns 11a and exposed parts of silicon oxide film 7 *before* amorphous silicon film was deposited would improve the subsequent etching of silicon oxide film 7. A POSITA wanting to have better flexibility in the etching process or to tailor the trench's profile would have known how to use etch selectivity to select different materials with different chemistries and etch rates to accomplish specific goals. Etch selectivity is the ratio between two etch rates, usually between a material being etched and a mask. A higher selectivity generally means it will be easier to etch a vertical profile. The selectivity can be adjusted by adjusting the processes or mask material, which affects etch rates. For

example, a POSITA not wanting to over-etch silicon oxide film 7 would have known that a liner layer made of a different material than the amorphous silicon film and the silicon oxide film would have a different etch rate and therefore would act as an etch stop to prevent unintended etching of silicon oxide film 7. By switching chemistries, a POSITA would have more flexibility in the types of trench profiles available. As applied to Matsuno, which has a silicon oxide layer 7, a POSITA would have found it obvious to select a different material for the next layer, such as a silicon nitride. *See, e.g.*, Ex-1036. A POSITA would have also found it obvious to switch materials for the subsequent layer, such as back to a silicon oxide, to benefit from etch selectivity. By switching chemistries, a POSITA would have more control over the etch process that results in a more precisely etched trench.

133. A POSITA would have also found it obvious to continue with the rest of Matsuno's steps after adding the liner layer to form the rest of the NAND flash memory. For example, amorphous silicon film 13 would then extend over the liner layer. *See* Ex-1005, 5:2-22. Below are the '974 Patent's Figure 4A and Matsuno's modified Figure 7', showing a spacer layer (pink) formed over a liner layer (cyan), along side surfaces of mandrels.



Ex-1001, Fig. 4A (annotated); Ex-1005, Fig. 7' (modified and annotated).

134. Matsuno discloses that after the etching of amorphous silicon film 13, “a pair of mask patterns 13a are formed on both side surfaces of the core patterns 11a respectively.” Ex-1005, 5:23-27. A POSITA would have known that portions of liner layer (cyan) on top of the mandrel (i.e., core patterns 11a) would also be etched away so that the core pattern could be removed. As explained above, a POSITA would have known to use different materials for the sidewall spacer and the liner layer. Below are Figure 4B of the '974 Patent and modified Figure 8' of Matsuno, showing that mask patterns 13a (pink) and liner layer portions (cyan) together correspond to “a plurality of mask portions [(blue bracket)], each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.”

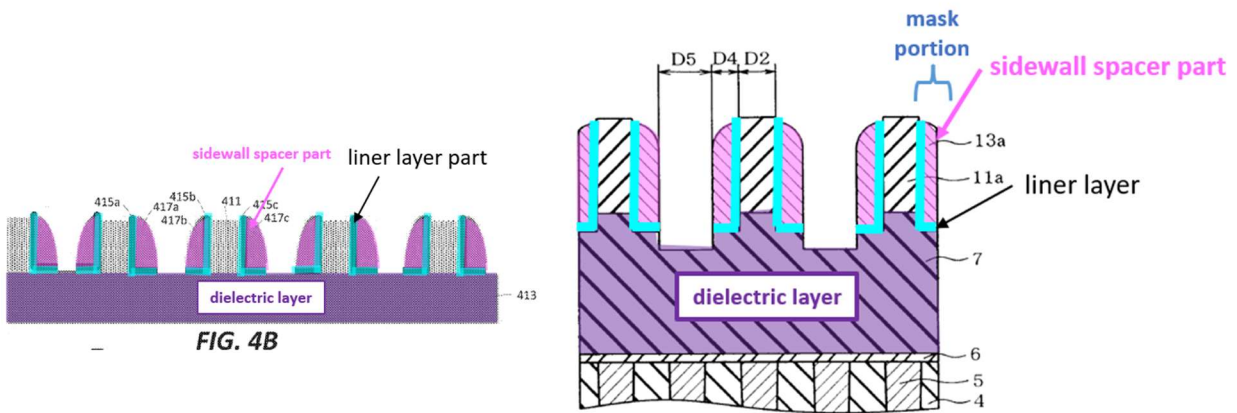


FIG. 8'

Ex-1001, Fig. 4B (annotated); Ex-1005, Fig. 8' (modified and annotated).

135. Matsuno's mask portions are formed on the core patterns 11a, which are removed prior to etching the trenches. *See* Ex-1005, 5:15-58. Together, the mask portions form an etch mask to be used for the subsequent etch of the trenches. *See* Ex-1005, 5:56-6:17, Figs. 9-10.

136. Thus, Matsuno-Kao teaches Claim 13.

3. **Dependent Claim 14: The method of claim 13 wherein the second material has a higher etch rate than the first material and wherein first trenches are formed at locations corresponding to locations of liner parts of neighboring mask portions.**

137. The '974 Patent explains that an etch selective to the liner layer material is used to remove dielectric layer and liner layer portions along sidewall spacers to form T1 trenches "between pairs of sidewall spacers 417b-c." Ex-1001, 8:61-9:6. As

a result, T1 trenches are “wider at the top than at the bottom,” compared to T2 trenches which “remain substantially uniform.” Ex-1001, 9:6-19.

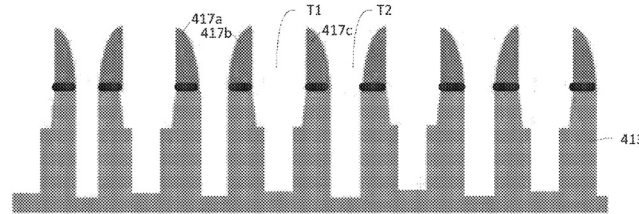


FIG. 4D

Id., Fig. 4D.

138. Kao discloses dielectric layer 116 formed over another dielectric layer 114, each made of a different material. Ex-1007, 2:39-43. Kao then discloses “a portion of the dielectric layer 114 is removed to form a second spacer 114b on the sidewall of the gate 106b and the gate dielectric layer 104b and to expose a portion of the substrate 100. A remaining dielectric layer 114a is left between the first spacer 116b and the first gate 106a.” *Id.*, 2:61-66. Kao states “[t]he method for removing the portion of the dielectric layer 114 is anisotropic etching.” *Id.*, 2:67-3:2.

139. Using the same modification to Kwak described for Claim 13, a POSITA would have known to use a liner layer material (i.e., second material) that has a higher etch rate than the sidewall spacer part material (i.e., first material). *See supra* Section X.C.2.

140. Kwak discloses selecting materials “having an etching selectivity” with respect to surrounding layers. *See, e.g.*, Ex-1008, ¶¶73-75.

141. As shown in Figures 4 and 5 of Kao, layer 114 is etched while spacer 116b remains generally the same.

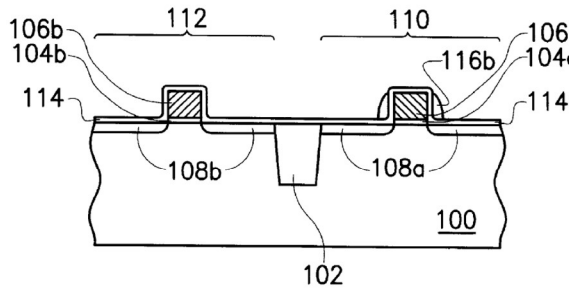


FIG. 4

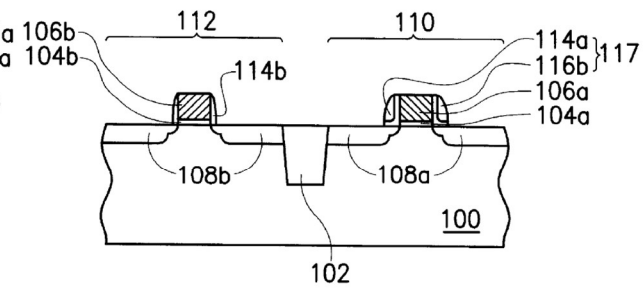


FIG. 5

Ex-1007, Figs. 4-5.

142. This step illustrates an etch selectivity for layer 114, compared to spacer 116b. A POSITA would have understood that one can tailor the conditions and chemistry of an etch such that layer 114 is etched at a higher rate than that of layer 116 because this selectivity in etch rate would allow for more flexibility and control of the etching process.

143. In addition, a POSITA would have known to use a liner layer material (i.e., second material) that has a higher etch rate than the sidewall spacer part material (i.e., first material). *See* Ex-1030. A material's etch rate depends on the material's chemistry. A POSITA would have been motivated to select a liner layer material with a higher etch rate than the sidewall spacer part material because this etch rate would allow for the etching tool to etch through the more resistant liner layer, while also creating a more concave shape trench in the less-resistant sidewall

spacer material. A trench shape that is more concave decreases the likelihood of voids forming during in the trench when the trench is subsequently filled. A simple way to visualize this effect is simply realizing that a wider opening at the top of the trench in a concave shaped trench would allow the trench filling material to easily entering into the bottom of the trench and filling the trench without void. A non-concave, or even a substantially straight, trench would not have the benefit of fully ensuring all the filling material entering and filling the bottom of the trench without being stuck around the sides of the top of the trench opening. If the trenching filling material is stuck at the top of the trench opening, it will further impede the subsequent filling material from entering the bottom of the trench, and thus increases the likelihood of void forming inside the trench.

4. Independent Claim 17

- a. Element 17[preamble]: A method of forming a NAND flash memory comprising:
Element 17[a]: forming a plurality of NAND strings disposed on a surface of a substrate;
Element 17[b]: depositing a dielectric layer over the plurality of NAND strings;**

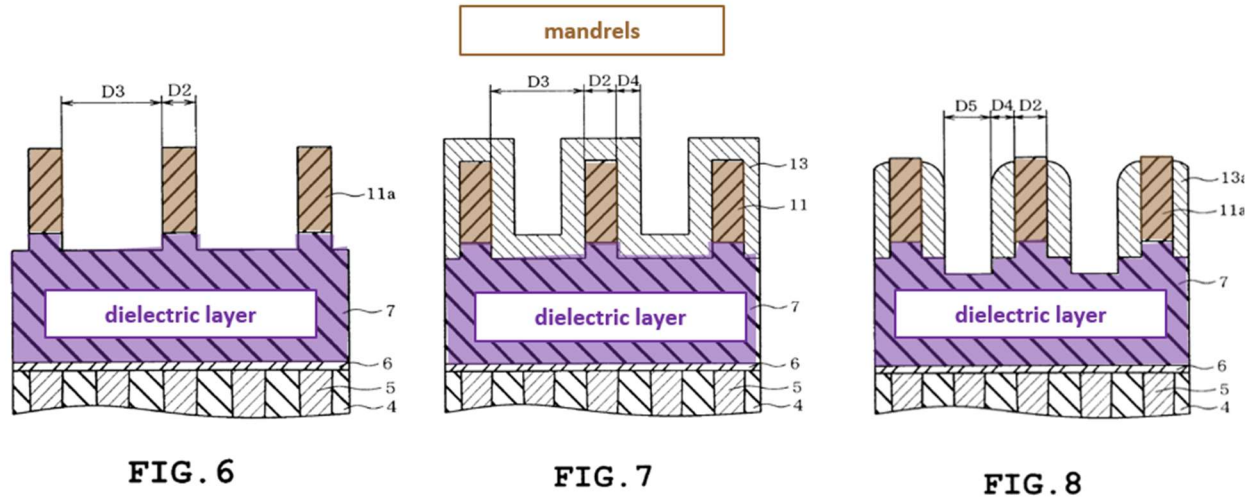
144. Matsuno-Kao discloses Elements 17[preamble]-[b] for the same reasons Matsuno discloses Elements 12[preamble]-[b]. *See supra* Sections X.A.4.a-c; Ex-1020.

b. Element 17[c]: forming a plurality of mandrels on the dielectric layer;

145. The '974 Patent uses “mandrels...formed on the surface of a dielectric layer” to form sidewall spacers. *See* Ex-1001, 7:61-65, 8:8:21-24, Figs. 3A, 4A. It states “mandrels may be formed first by an appropriate process” and when removed “leave[] masking portions.” *Id.*, 8:25, 8:53-60, Fig. 4C. Matsuno teaches “forming a plurality of mandrels on the dielectric layer” the same way that '974 Patent does.

146. Although Matsuno does not use the term “mandrel,” it discloses “resist pattern 12 is formed by a photolithography technique so as to have a line-and-space (L/S) pattern.” Ex-1005, 4:60-62. Resist pattern 12 is formed on a silicon nitride film 11. *See id.*, 4:55-56, Fig. 5.

147. Matsuno states that “silicon nitride film 11 is etched by a dry etching process with the resist pattern 12 serving as a mask.” Ex-1005, 4:65-67. After the dry etching and slimming processes are carried out, core patterns 11a are formed. *See id.*, 4:65-5:14, Fig. 6. Matsuno then describes depositing liner layer 13—on core patterns 11a (brown)—which will then be etched to become sidewall spacers 13a. *See id.*, 5:15-49.



Id., Figs. 6-8 (annotated).

148. A POSITA would have understood Matsuno's core patterns 11a are mandrels because they serve as a pattern for subsequent sidewall spacers, just as explained in the '974 Patent.

- c. **Element 17[d]: forming a liner layer along side surfaces of the plurality of mandrels;**
Element 17[e]: forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels;
Element 17[f]: removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material;

149. Matsuno-Kao teaches Elements 17[d]-[f] for the same reasons it teaches Claim 13. Ex-1020; *see supra* Section X.C.2.

- d. **Element 17[g]: subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel;**

150. Matsuno-Kao teaches Element 17[g] for the same reasons Matsuno teaches Element 12[c]. Ex-1020; *see supra* Section X.A.4.d.

- e. **Element 17[h]: etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and**

151. Matsuno-Kao teaches etching second trenches in the dielectric layer for the same reasons it teaches Element 12[d]. *See supra* Section X.A.4.e. And, as discussed in Section X.C.4.d, Matsuno-Kao teaches trenches etched into the dielectric layer between sidewall spacers that were formed on mandrels. As shown in Figure 8, Matsuno's sidewall spacers 13a (pink) are formed on neighboring mandrels 11a (brown). *See also* Ex-1005, 1:59-65, 4:65-5:24, 5:40-49.

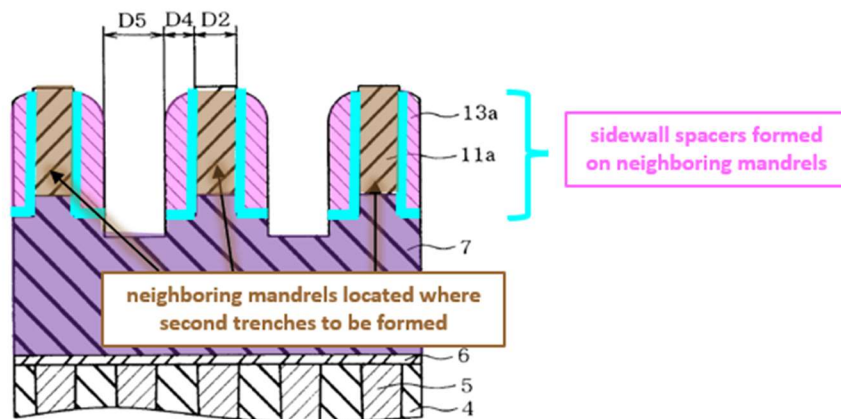


FIG. 8'

Id., Fig. 8 (annotated).

152. Matsuno states after mandrels are removed, trenches “are formed in the silicon oxide film 7 and the silicon nitride film 6 by the dry etching process” using the side wall spacers (mask patterns) 13a. Ex-1005, 5:50-6:17. As a result, second trenches (yellow) are etched in dielectric layer 7 where facing pairs Pa—which are between sidewall spacers—are located.

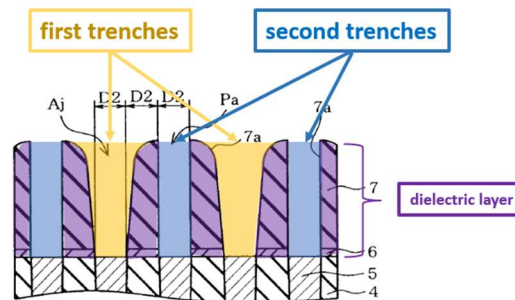


FIG. 10

Ex-1005, Fig. 10 (annotated).

- f. Element 17[i]: depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches.**

153. Matsuno discloses “[c]onductor films comprising a barrier metal layer 8 and a copper (Cu) layer 9 are buried in the pattern thereby to be formed into first and second buried wirings 10a and 10b.” Ex-1005, 4:3-6. Specifically, copper layer 9 is plated into the trenches. *Id.*, 6:20-22. Matsuno discloses “[t]he first and second wirings 10a and 10b are formed so as to correspond to the bit lines BL1 and BL2 which are disposed cyclically and alternately, respectively.” *Id.*, 4:8-11. Thus,

Matsuno-Kao teaches “depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches.”

5. Dependent Claim 18: The method of claim 17 further comprising depositing the copper in the plurality of second trenches to form a plurality of additional bit lines.

154. Matsuno-Kao teaches Claim 18. Matsuno discloses the first and second buried wirings 10a and 10b that correspond to the bit lines and additional bit lines comprise a barrier metal layer 8 and copper layer 9. *See* Ex-1005, 4:3-11. Thus, Matsuno-Kao discloses the plurality of bit lines and the plurality of additional bit lines are formed of copper.

D. Ground 4: Claims 1-2, 4, 11-12, and 15 Are Obvious Over Kwak

1. Independent Claim 1

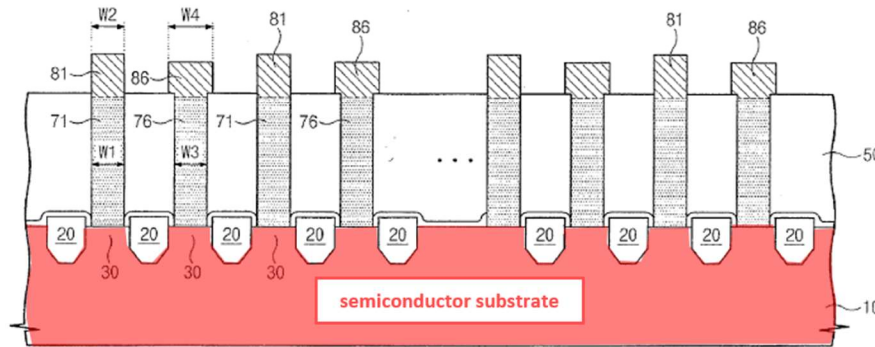
a. Element 1[preamble]: A NAND flash memory comprising:

155. Kwak discloses “a non-volatile memory device such as a *NAND flash memory* device.” Ex-1008, ¶36; *see also id.*, ¶42 (“the NAND flash memory device of Fig. 1”).

b. Element 1[a]: a semiconductor substrate;

156. Kwak discloses “a method for forming a conductive line that includes forming an insulation layer on a *substrate*.” Ex-1008, ¶5. Kwak uses “semiconductor substrate” and “substrate” interchangeably. *See id.*, ¶33. Annotated Figure 4 shows semiconductor substrate 10 in red. *See id.*, ¶49.

Fig. 4

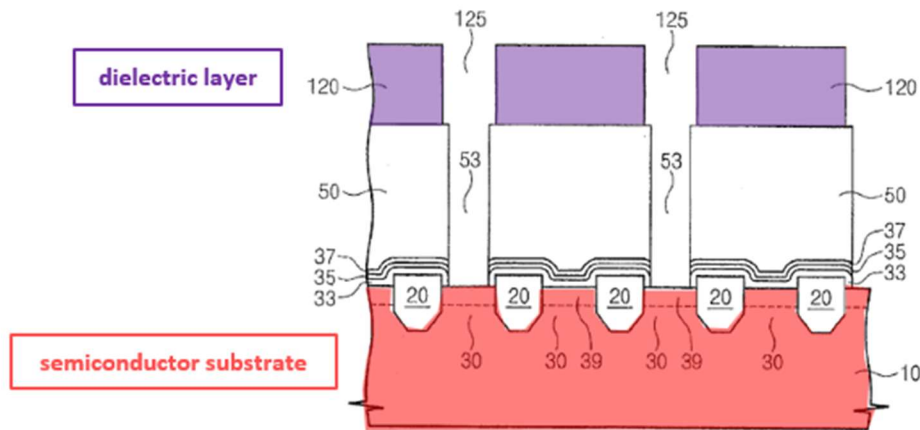


Id., Fig. 4 (annotated).

c. Element 1[b]: a dielectric layer extending over the semiconductor substrate;

157. Kwak discloses “insulation layer 50 may be formed” on substrate 10, and “mold layer 120 may be formed on the insulation layer 50.” Ex-1008, ¶68. A POSITA would have known that mold layer 120 is made of a dielectric material to isolate conducting features from one another. In fact, Kwak discloses that “the mold layer 120 may include a material such as a nitride.” Ex-1008, ¶68. Annotated Figure 16 below shows dielectric layer 120 (purple) after “a patterning process is performed” to form trenches. Ex-1008, ¶68. As explained above in Section X.A.1.c, Kwak’s dielectric layer “extend[s] over” the semiconductor substrate the same way as described in the ’974 Patent.

Fig. 16



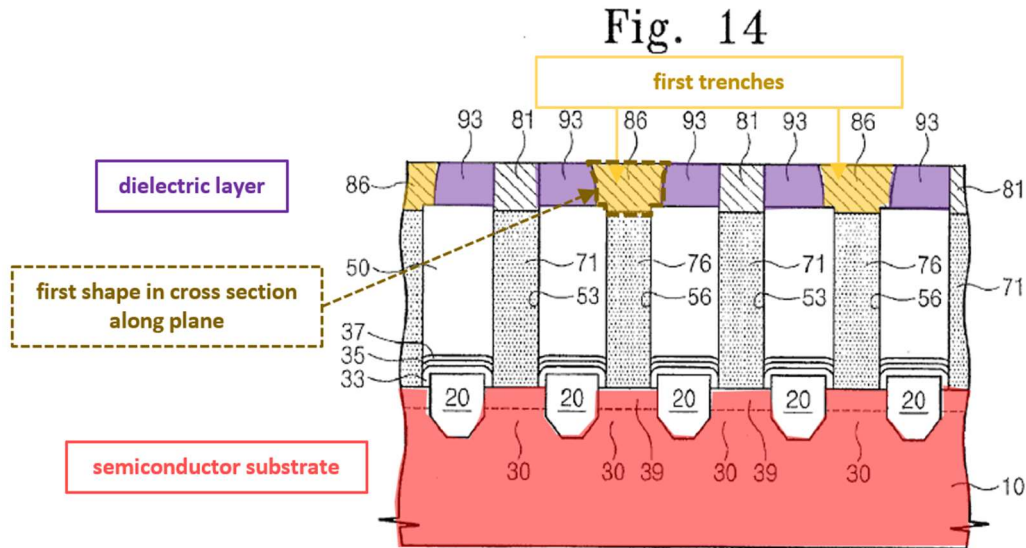
Id., Fig. 16 (annotated).

- d. **Element 1[c]: a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;**

158. Kwak discloses “even contacts 76 and even bit lines 86 can be formed according to any of various exemplary methods.” Ex-1008, ¶62. Kwak’s Figure 14 specifically describes “even bit lines 86 are formed in a self-aligned manner between spacers 93.” *Id.*, ¶62. A POSITA would have known that bit lines are formed in a trench. Ex-1008, ¶61 (“a portion of a spacer 93 is etched”).

159. Kwak discloses “spacers 93 may include a nitride (e.g., silicon nitride), an oxide (e.g., aluminum oxide) or a nitride oxide (e.g., silicon oxynitride).” Ex-1008, ¶59. Because silicon nitride is a dielectric material, Kwak discloses spacers 93 made of a dielectric material. A POSITA would have known that spacers may be

formed from mold layer 120, like that of Figure 16, resulting in first trenches (yellow) between spacers that run in a first direction (into the page) and that are in a shape in cross section along a plane perpendicular to the first direction, as illustrated in Figure 14 below. *See supra* Section X.D.1.c.



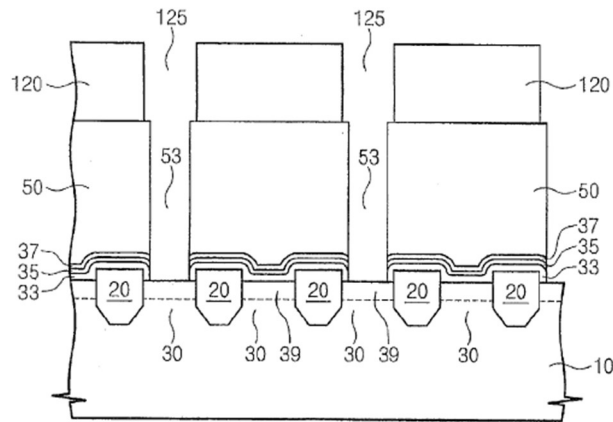
Ex-1008, Fig. 14 (annotated).

- e. **Element 1[d][i]: a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane,**

160. Kwak discloses “when one bit line is called an ‘even bit line’, a bit line adjacent to the one bit line is called an ‘odd bit line.’” Ex-1008, ¶34, Figs. 3-4. Kwak also discloses, referring to Figure 16: “a patterning process is performed on the mold layer 120 to form odd line-type openings 125 and odd contact holes 53. Each odd line-type opening 125 defines an odd bit line while each odd contact hole 53 is self-

¶68.

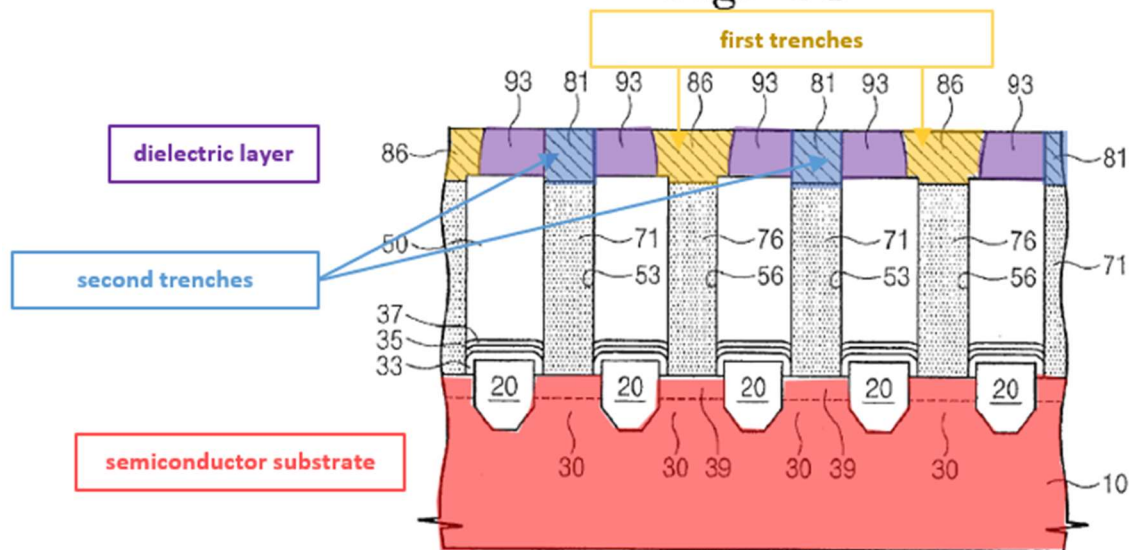
Fig. 16



Id., Fig. 16.

are located inside second trenches (blue) between spacers 93. *Id.*, ¶¶60, 63, 66-67.

Fig. 14



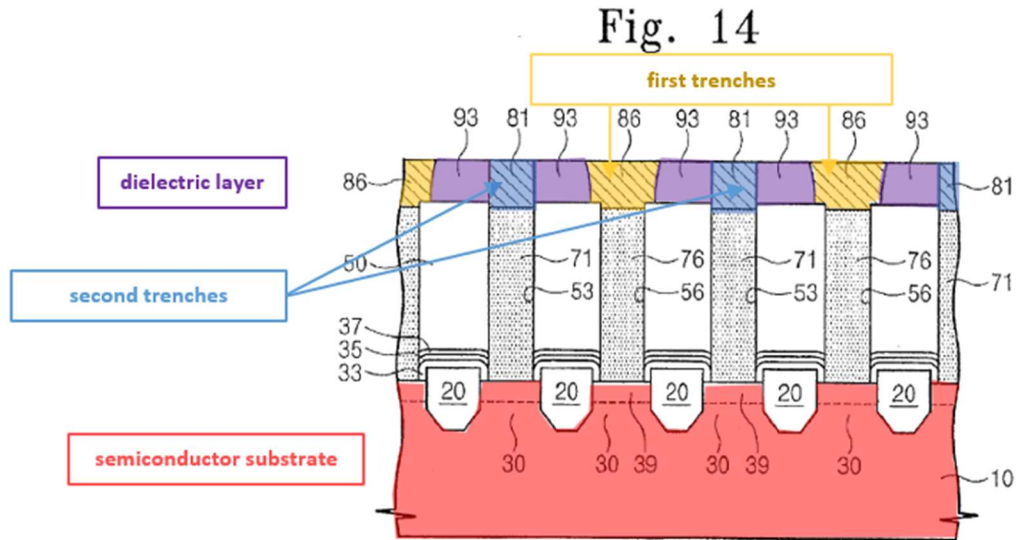
Id., Fig. 14 (annotated).

f. Element 1[d][ii]: the second shape being different from the first shape,

162. Kwak discloses “even contacts 76 and even bit lines 86 can be formed according to any of various exemplary methods. For example, and with reference to FIG. 14, even bit line contacts 76 may be formed by filling the even contact holes 56 and the line-type groove 100 between spacers 93 with a conductive material and subsequently performing an etch-back process...A conductive material for bit lines 86 may then be formed on the even bit line contacts 76 to fill the line-type groove 100 between the spacers 93.” Ex-1008, ¶62; *see also id.*, ¶59.

163. A POSITA would have understood even bit lines 86 to be positioned in first trenches (yellow), which are shaped by the curved sides of spacers 93.

164. Kwak discloses odd bit lines 81 formed using a mask or formed between the sidewalls of the spacers. *See* Ex-1008, ¶¶54, 59 (“adjacent...even and odd bit lines can be insulated from each other by a spacer 93”). Kwak also discloses, with reference to Figure 16: “the width of the odd line-type opening 125 may be...substantially equal to the width of the odd contact hole 53.” *Id.*, ¶69. A POSITA would have known that odd line-type opening 125 results in second trenches having a rectangular shape in cross section along the plane. Figure 14 annotated below shows the resulting structure with odd bit lines 81 positioned in second trenches (blue) which are substantially equal in width from the upper portion to the lower portion of the trench.



Ex-1008, Fig. 14 (annotated).

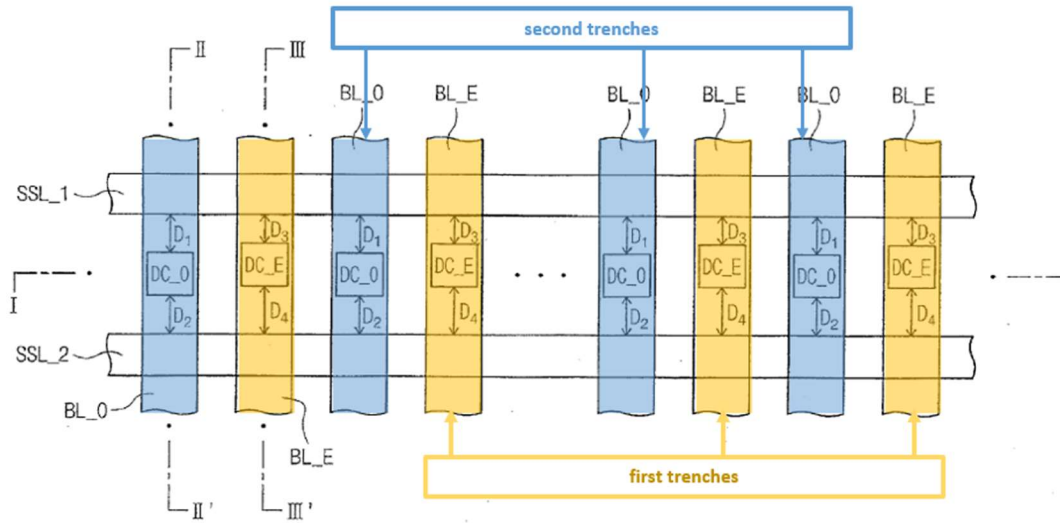
165. Therefore, the first and second shapes are different.

g. Element 1[d][iii]: the first and second trenches arranged in an alternating pattern that alternates from first trench to second trench along a second direction that is perpendicular to the first direction; and

166. Kwak discloses “odd bit lines BL_O and even bit lines BL_E” in an alternating patterning. Ex-1008, ¶44; *see also id.*, ¶34 (“[W]hen considering adjacent two bit lines, when one bit line is an ‘odd bit line’, the other one is an ‘even bit line’, and vice versa.”). The first direction, relative to Figure 14, goes into the page. *See supra* Section XD.1.d.

167. A POSITA would have known that bit lines are located within a trench. Figure 3, annotated below, illustrates first trenches and second trenches alternating—from first trench (yellow) to second trench (blue) along a second direction perpendicular to the first direction.

Fig. 3



Ex-1008, Fig. 3 (annotated).

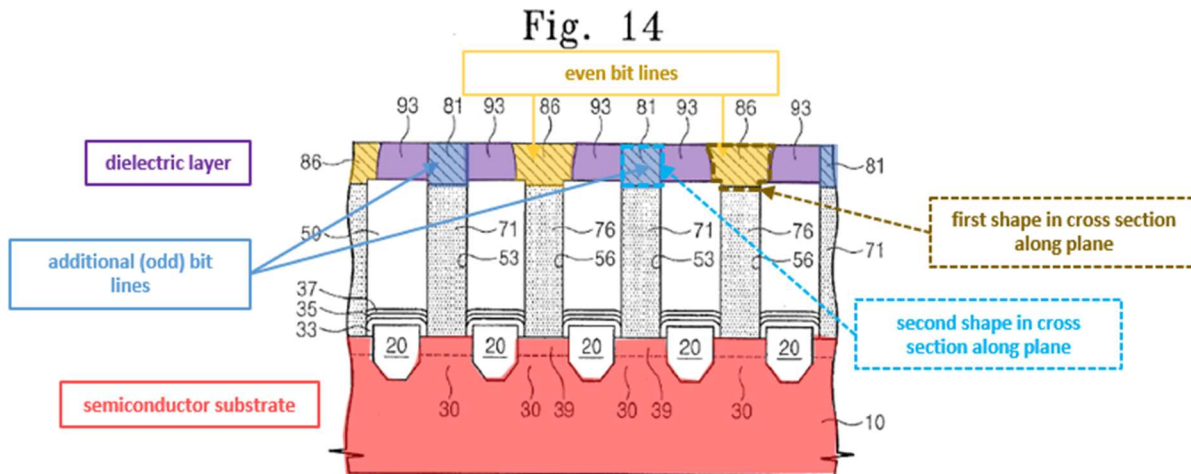
h. Element 1[e]: a plurality of bit lines located in the first trenches.

168. Kwak discloses “bit lines 86 are...subsequently formed” after even bit line contacts 76 are confined with respect to line-type grooves 100. Ex-1008, ¶60. Kwak also discloses “[r]eferring to Fig. 14, *even bit lines 86 are formed in a self-aligned manner between spacers 93* and are electrically connected to respective ones of even bit line contacts 76 by etching the conductive material for the bit lines 86.” *Id.*, ¶¶63-64.

2. **Dependent Claim 2: The NAND flash memory of claim 1 further comprising**
[a] **a plurality of additional bit lines located in the second trenches,**
[b] **each of the plurality of bit lines having the first shape in cross section along the plane and each of the plurality of additional bit lines having the second shape in cross section along the plane.**

169. Kwak discloses “bit lines may be provided as either a first bit line or a second bit line, wherein second bit lines can be disposed between adjacent first bit lines.” Ex-1008, ¶43. Kwak discloses, referencing Figure 16: “*[e]ach odd line-type opening 125 defines an odd bit line* while each odd contact hole 53 is self-aligned with the odd line-type opening 125 and defines an odd bit line contact.” *Id.*, ¶68; *see id.*, ¶69 (“odd bit line contacts 71 and odd bit lines 81 are formed by filling each odd contact hole 53 and each odd line-type opening 125 with conductive material”).

170. Annotated Figure 14 illustrates the resulting structure with even bit lines (yellow) having the first shape in cross section along the plane and odd bit lines (blue) having the second shape in cross section along the plane.



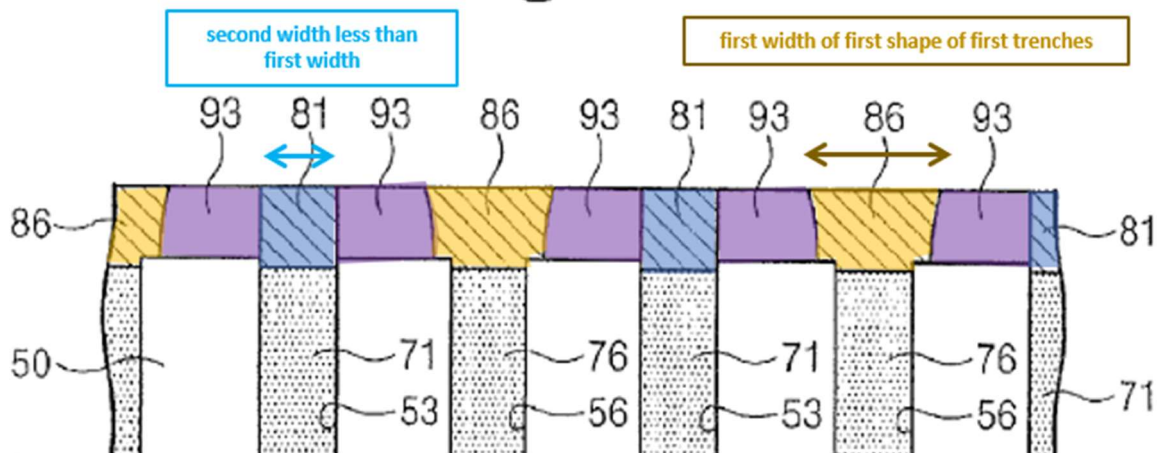
Ex-1008, Fig. 14 (annotated).

3. **Dependent Claim 4:** wherein the first shape has a first width at a level of an upper surface of the dielectric layer, the second shape has a second width at the level of the upper surface of the dielectric layer, and the second width is less than the first width.

171. Kwak discloses “[d]uring the etching process, when a portion of a spacer 93 is etched, the width of a subsequently formed even bit line 86 may be greater than the width of the odd bit line 81.” Ex-1008, ¶61, Fig. 4. Kwak also states “an odd bit line and an even bit line can have...different structures (e.g., different widths, different heights, or different widths and heights).” *Id.*, ¶¶49, 43. Kwak states “the width of the line-type groove 100 can be adjusted by varying the width of the spacers 93. Thus the width of subsequently formed even bit lines 86 can be appropriately adjusted, as well as the ratio between the widths of the even and odd bit lines 71 and 76, by controlling the width of the spacers 93.” *Id.*, ¶61.

172. Kwak's Figure 14, annotated below, illustrates the first shape of first trenches (yellow) having a first width at a level of an upper surface of dielectric layer 93 (purple) and the second shape of second trenches (blue) having a second width at the level of the upper surface of dielectric layer that is less than the first width.

Fig. 14



Ex-1008, Fig. 14 (magnified and annotated).

- 4. Dependent Claim 11: wherein the plurality of first trenches have a first depth and the plurality of second trenches have a second depth that is different to the first depth.**

173. Kwak teaches second trenches having a depth different than the depth of first trenches.

174. Kwak’s Figure 34 shows grooves 267 and contact hole 258 formed in dielectric layer 250. Ex-1008, ¶¶91-92. Kwak states “insulation layer 250 may be patterned to form a contact hole 258” and that bit lines and bit line contacts are

formed after conductive material is deposited into the grooves and contact hole. *Id.*, ¶¶92-93, Fig. 35.

Fig. 34

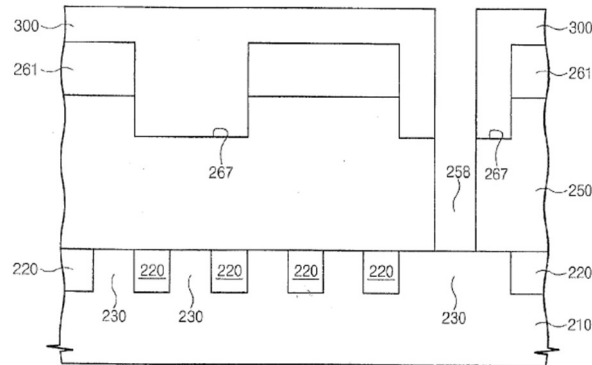
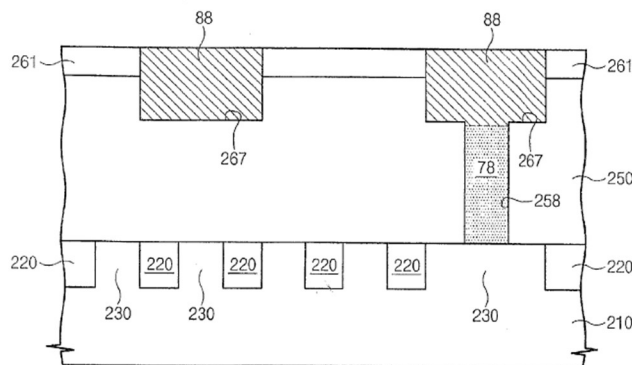


Fig. 35



Id., Figs. 34-35.

175. Contact hole 258 extends to active region 230 with bit line contact 78 filling in contact hole 258. *See* Ex-1008, ¶73. As shown in Figures 34 and 35, the trench that contains bit line 88 is of a different depth than the trench that contains bit line 88 and bit line contact 78. A POSITA would have been motivated to have first

and second trenches with different depths because one set of trenches (e.g., first trenches) touches a bit line contact to electrically connect to an active region, while the other set of trenches (e.g., second trenches) could be shallower and have no electrical connection to an active region, as to reduce capacitance between the bit lines of the first trenches. Moreover, Kwak discloses “*a height of one of the first bit lines is different from a height of the second bit line.*” Ex-1008, cl. 3; *see also id.*, ¶49 (“In one embodiment, an odd bit line and an even bit line can have...*different heights....*”). Because even/odd bit lines are formed in first/second trenches respectively in a dielectric layer, a POSITA would have understood that first and second trenches having different heights are of different depths. For example, a POSITA would have known that one common occurrence of bit line with different heights is in a cross-section where one bit line has the bit line contact directly underneath the bit line, whereas another bit line would not have the bit line contact beneath the bit line. A POSITA would also know that the another bit line would have its own bit line contact underneath the another bit line elsewhere, away from the cross-section, at another horizontal plane of cross section.

5. Independent Claim 12

a. Element 12[preamble]: A method of forming a NAND flash memory comprising:

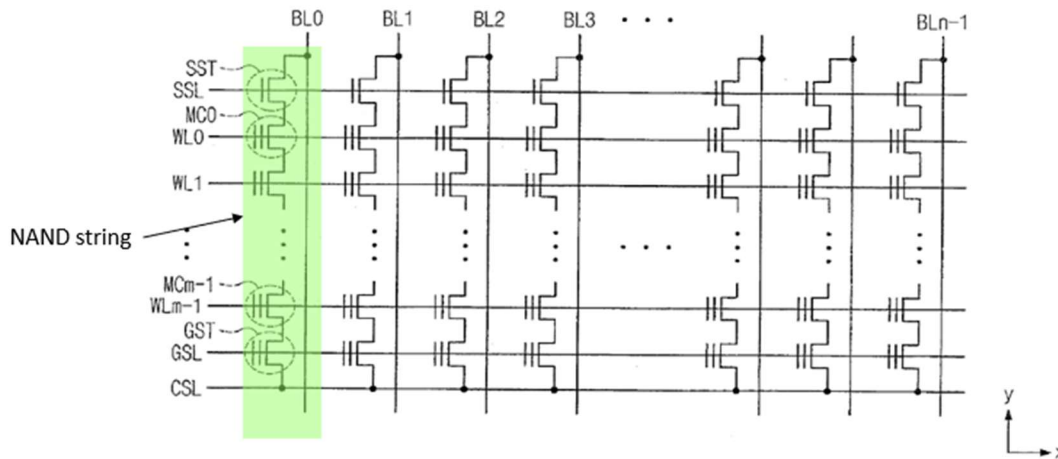
176. Kwak discloses “a method for forming...bit lines in a semiconductor device such as a non-volatile memory.” Ex-1008, ¶2. Kwak states “one embodiment of a non-volatile memory device” is “*NAND flash memory.*” *Id.*, ¶36.

b. Element 12[a]: forming a plurality of NAND strings disposed on a surface of a substrate;

177. Kwak discloses “[a] plurality of memory cells are coupled to each of the word lines WL0 to WLM-1 such that a plurality of memory cells MC0 to MCm-1 arranged in the column direction are connected in series to *form a unit NAND string.*” Ex-1008, ¶38. Kwak further discloses “*memory cells* can include a tunneling insulation layer, a memory layer..., and a control insulation layer (or an inter-gate dielectric layer) which are sequentially *stacked on a semiconductor substrate.*” *Id.*, ¶41 (emphases added); *see id.*, ¶68 (isolation region, active region, string select line, word line, ground select line formed on substrate 10).

178. An example of a NAND string is annotated in lime green in Kwak’s Figure 1. *See* Ex-1008, ¶37.

Fig. 1



Id., Fig. 1 (annotated).

c. Element 12[b]: depositing a dielectric layer over the plurality of NAND strings;

179. Kwak discloses “a device isolation region 20, an active region 30, a string select line SSL, a word line, and ground select line GSL may be formed on the substrate 10.” Ex-1008, ¶68; *see id.*, ¶¶6, 10, 53-54. A POSITA would have understood the SSL, word line, and GSL formed on substrate 10 corresponds to NAND strings on a semiconductor substrate.

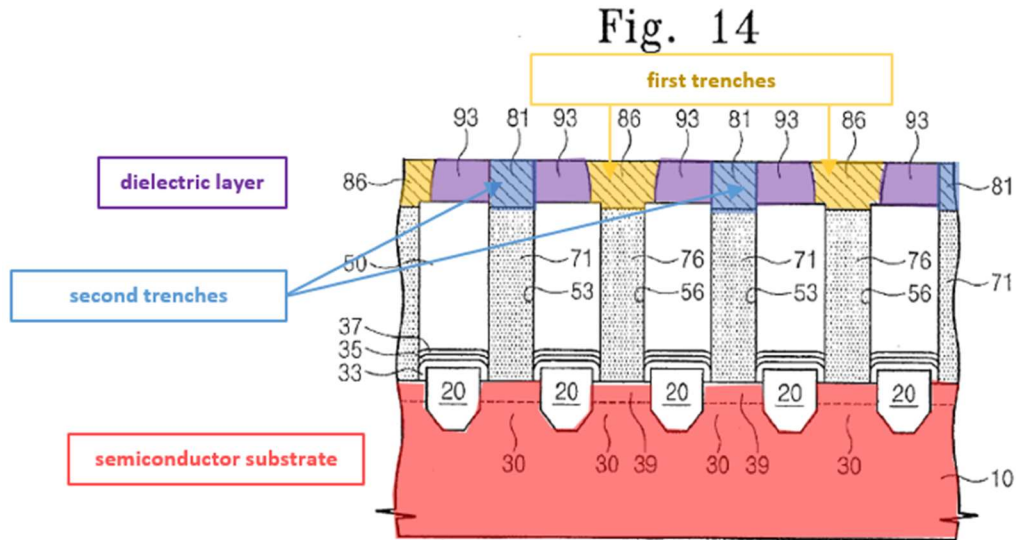
180. Kwak also discloses depositing a mold layer on substrate 10. *See* Ex-1008, ¶68; *supra* Section X.D.1.c.

- d. **Element 12[c]: etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;**
Element 12[d]: etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane,
Element 12[e]: the second shape being different to the first shape,
Element 12[f]: the first and second trenches arranged in an odd-even alternating pattern along a direction that is perpendicular to the first direction such that two first trenches are separated by a second trench; and

181. Kwak discloses etching dielectric layers and conductive material. *See, e.g.,* Ex-1008, ¶¶55, 59, 61-62, 66, 68. Kwak teaches the trench configurations recited in Elements 12[c]-[f] for the reasons it teaches Elements 1[c]-[d]. *See* Ex-1020; *supra* Sections X.D.1.d-g.

- e. **Element 12[g]: depositing metal in the plurality of first trenches to form a plurality of bit lines located in the first trenches.**

182. Kwak discloses bit lines 86 in first trenches for the reasons set forth in Section X.D.1.h. Ex-1020.



Ex-1008, Fig. 14 (annotated).

183. Kwak discloses “a conductive material may be formed to fill the even contact holes 56 and the line-type grooves 100 between spacers 93 and a planarization process may then be performed to form the even bit lines 86 and respective even bit line contacts 76.” Ex-1008, ¶63. Kwak specifically discloses “[t]he conductive material from which the bit lines 86 are formed may include a material such as a *metal*, a metal alloy, a silicide, a conductive metal nitride, a conductive metal oxide, silicon, or the like or combinations thereof.” *Id.*

6. Dependent Claim 15: The method of claim 12 further comprising depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches.

184. Kwak discloses additional bit lines in second trenches for the reasons set forth in Section X.D.2. Kwak discloses “a conductive material is formed on the mold layer 120 to fill the odd contact holes 53 and the odd line-type openings 125,”

which then “form[s] odd bit lines 81 and odd bit line contacts 71.” Ex-1008, ¶69. Kwak discloses conductive material that forms bit lines “may include a material such as a metal.” *Id.*, ¶63.

E. Ground 5: Claims 6 and 16 Are Obvious Over Kwak in View of Zhang

185. As shown below, the subject matter of Claims 6 and 16 are taught by Kwak in view of Zhang.

1. A POSITA would have been motivated to combine Kwak with Zhang

186. A POSITA would have been motivated to combine the teachings of Kwak and Zhang and would have had a reasonable expectation of success in doing so at least because they relate to the same field and address the same well-known issues. Kwak and Zhang provide complementary solutions for fabricating interconnects with certain structural and electrical configurations in semiconductor devices. *See, e.g.*, Ex-1008, ¶¶2-15; Ex-1006, ¶¶4, 6, 31-35, 44. Both Kwak and Zhang use capping layers to encapsulate recesses. *See* Ex-1008, ¶66; Ex-1006, ¶¶55-57.

187. A POSITA seeking a more precise and accurate photolithography process would have known of and consulted these proposed solutions. Ex-1008, ¶¶2-3; *see* Ex-1006, ¶¶2, 9.

188. Kwak discloses forming a “NAND flash memory” with first bit lines and second bit lines disposed between adjacent spacers. *See* Ex-1008, ¶8. This results in two trench shapes: a curved, trapezoidal bit line (e.g., 86) and a rectangular bit line (e.g., 81). *See id.*, Fig. 14. Kwak states this configuration is advantageous because the risk of misalignment between bit line and bit line contact is reduced. *See id.*, ¶¶61, 65. This is because for the even bit lines, which have a larger width at the surface of the insulating layer with a smaller width at the lower portion, subsequent layers have a larger area to make an electrical contact.

189. A POSITA would have known that as memory technology and integration density advanced, the distance between bit lines continues to decrease. As this distance decreased, the inter bit line capacitance would increase proportionally, which results in negative effects on memory performance, given that the current consumption and accuracy of sense current are dependent on the overall bit line capacitance, and that for a given bit line, the inter bit line capacitance is a significant component to the overall bit line capacitance. Consequently, an increase in inter bit line capacitance causes the bit line sensing margin and refresh ability to degrade, in addition to increasing the current consumption of the NAND memory. For example, an increase in capacitance causes the bit line sensing margin and refresh ability to degrade. Figure 18.5 of Micheloni illustrates that a major

contributor of bit line capacitance is the inter bit line capacitance, especially as the NAND memory cell is scaled down. Ex-1021, 518.

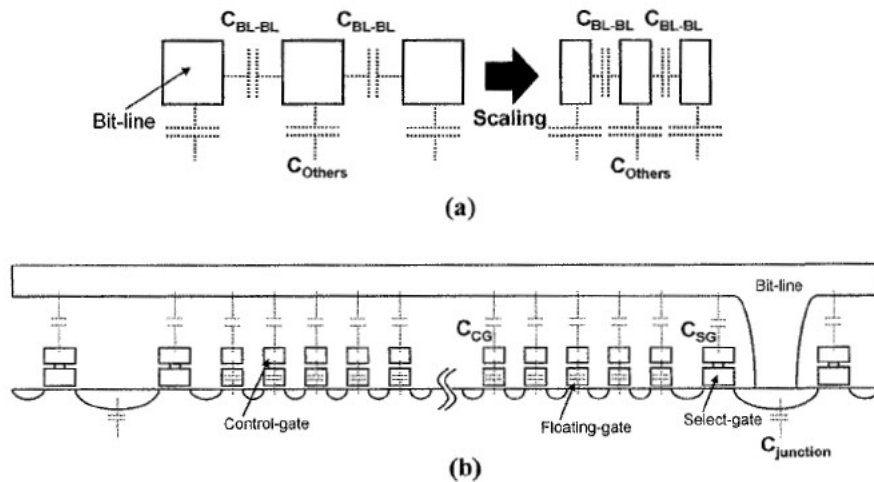


Fig. 18.5. Cross sectional view of (a) a bit-line and (b) a NAND Flash memory cell

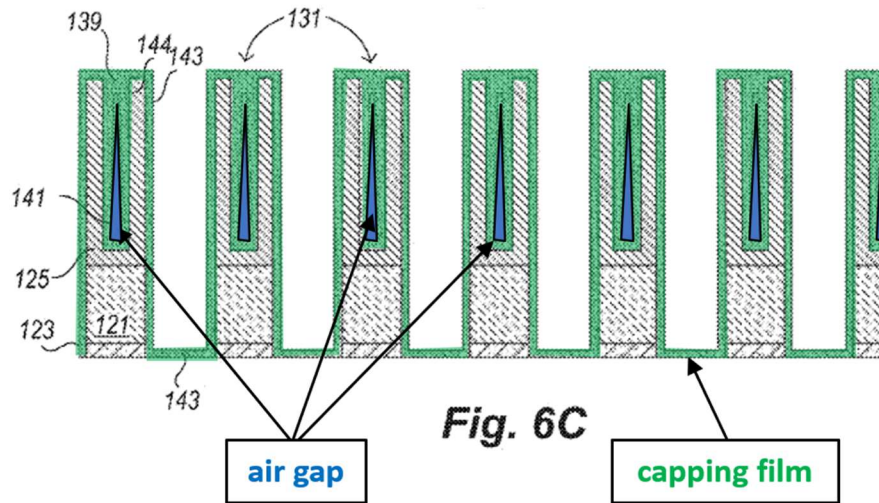
190. Accordingly, a POSITA would have been motivated to implement Kwak's NAND memory configuration using Zhang's air gaps because a POSITA would have recognized that—as stated in Zhang—“incorporation of an air gap in a layer” “reduce[s] capacitance between adjacent” bit lines and mitigates the effects of the reduction in the inter bit line spacing. Ex-1006, ¶¶9-10, 55, 64. As explained above, air gaps provide a low dielectric constant to achieve low capacitance between bit lines. *See supra* ¶¶100-101 (citing Ex-1006, ¶¶9-10, 55, 64). With this combination, a POSITA would have recognized that Kwak's bit lines are interconnects to the drain of the memory array. A POSITA would have known how to implement an appropriate memory array for bit lines or air gaps. For example, a POSITA seeking to implement air gaps could fill holes 53 with dielectric material

or design holes 53 to be a shorter depth to avoid contact with the active areas. The appropriate implementation would depend on several design factors.

191. A POSITA would have had a reasonable expectation of success in achieving the objective of decreasing the capacitance between bit lines by combining the teachings of Kwak and Zhang without change in their respective functions because both references use “conventional thin film deposition[, photolithography[, and] etching techniques” to fabricate semiconductor devices. Ex-1006, ¶¶32-35; *see, e.g.*, Ex-1008, ¶¶66-83 (using photolithography and etching techniques); *infra* Sections X.E.2-3.

2. Dependent Claim 6: The NAND flash memory of claim 1 further comprising a plurality of air gaps located in the second trenches.

192. Zhang discloses air gaps in second trenches. As explained in Section X.B.2, Zhang describes a capping layer that “result[s] in the cap being formed almost immediately upon the deposition starting so that little to no material from the capping layer 139 enters the U-shaped structure 131. Therefore, the top of the U-shaped structure 131 will be essentially capped and maintain nearly the same open area as when it was originally etched.” Ex-1006 ¶55. Figure 6C of Zhang below illustrates the capping layer 139 (green) lining both the first and second trenches, resulting in air gaps (dark blue) formed in second trenches.



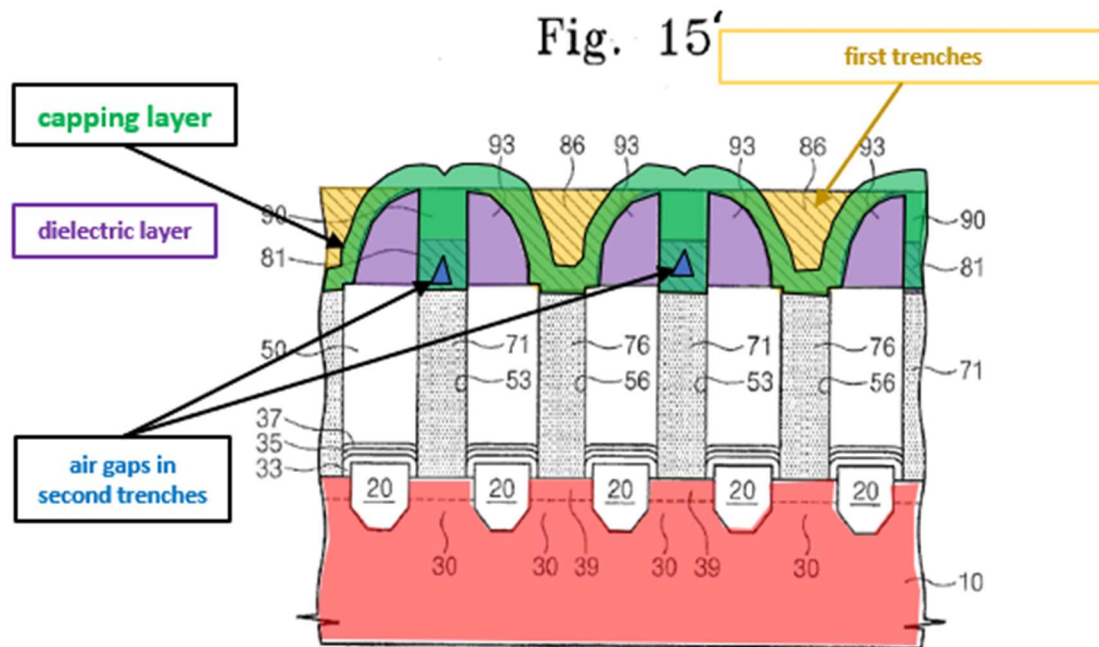
Id., Fig. 6C (annotated).

193. Kwak discloses “a capping layer 90...can be formed on the odd bit lines 81.” Ex-1008, ¶57. A POSITA would have found it obvious to use another capping layer in Kwak, like Zhang’s capping layer, to incorporate air gaps into second trenches. Ex-1008, Fig 15. By depositing a capping layer thick enough or at a deposition rate to result in portions of capping layer at the top of Kwak’s second trenches (e.g., odd trenches), like Zhang’s U-shaped structures, a sealing cap is formed at the tops of the second trenches with air gaps remaining. Ex-1006, ¶55. A POSITA would have known how to adjust the thickness of the capping metal layer to allow for the enclosure of an air gap for the reasons explained in Section X.B.2.

194. For this modification, an initial deposit of metal will form at the top of the first trenches but it would be thick enough to seal off second trenches so that an air gap is formed while the first trenches are not filled up at the top, like the profiles

in Figure 6C of Zhang. Moreover, a POSITA would have known how to use a sputtering deposition method to facilitate a lower pinch-off region for the reasons explained in Section X.B.2. *See* Ex-1031, ¶99, Figs. 9A-9B.

195. Below, Modified Figure 15' of Kwak illustrates capping layer (green) formed on the sidewalls of spacers (purple) and on contacts 76 under first trenches (yellow).

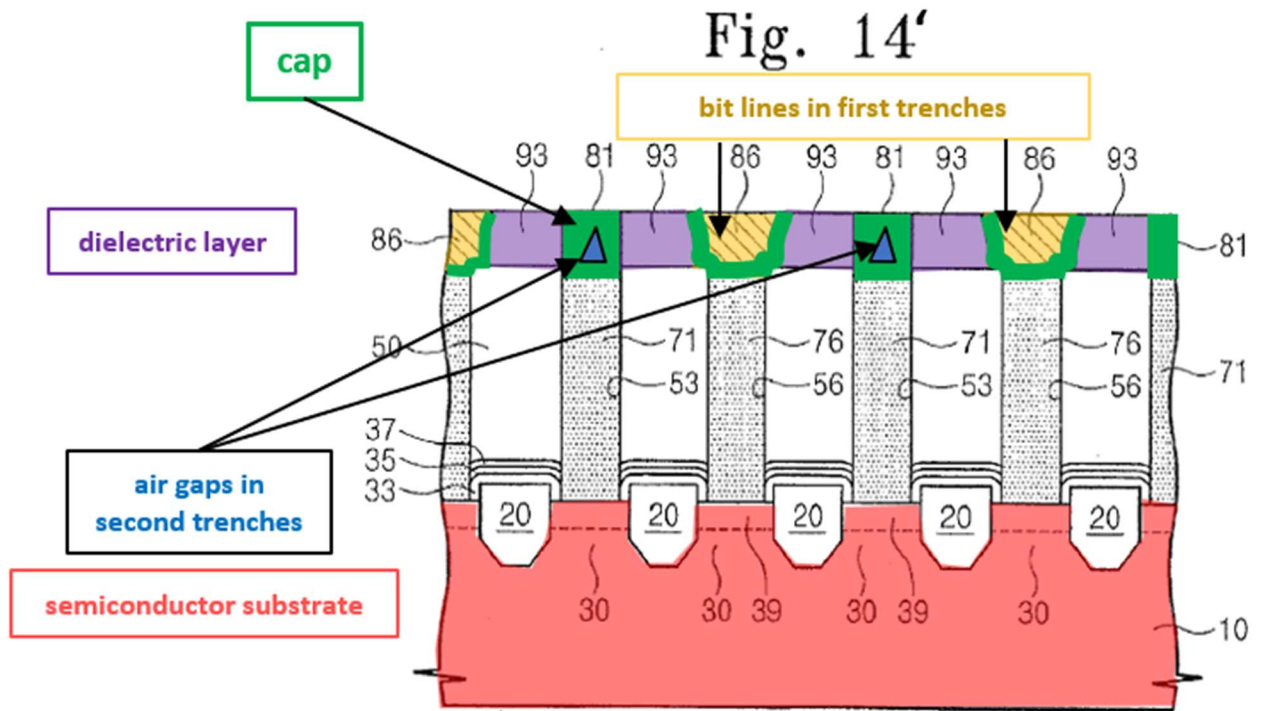


Ex-1008, Fig. 15' (modified).

196. The deposition of a thick capping layer results in an uneven top layer, A subsequent planarization would level these layers. *See, e.g.,* Ex-1008 ¶64 (“a planarization process may then be performed to form the even bit lines 86”). A POSITA would have known how to determine where to position a pinch-off region

to preserve the air gaps in the second trenches after planarization. A POSITA would have also known to planarize the layers and caps as to prevent shorting the bit lines.

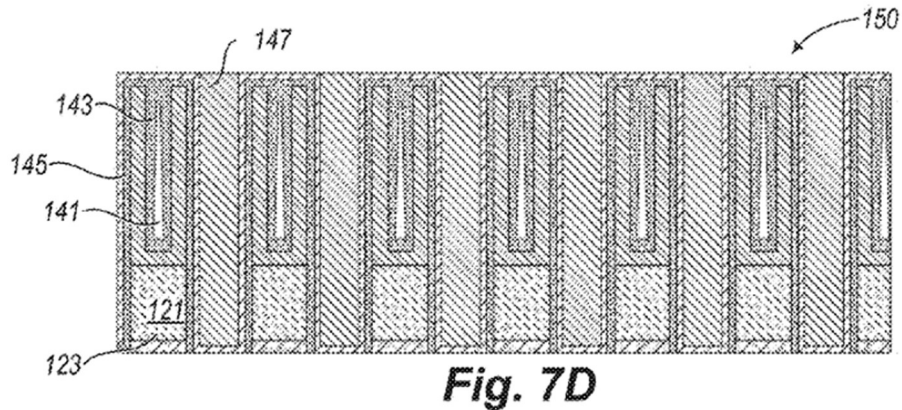
197. Because air gaps were incorporated into the second trenches, the resulting configuration leaves a portion of the metal barrier layer forming the cap in the second trenches that maintain the air gaps, while the bit lines formed in the first trenches from the barrier metal layer and copper layer remains. Modified Figure 14' of Kwak below illustrates the resulting configuration of bit lines in the first trenches (yellow) with air gaps in the second trenches (blue).



Ex-1008, Fig. 14' (modified).

198. A POSITA would have known how to adapt the contents of holes 53 for air gaps. For example, Figure 7D of Zhang illustrates air gaps 141 in trenches

143 above a dielectric material 123, while its bitlines 147 may connect to underlying metal contacts. *See* Ex-1006, 7:63-8:3, 10:44-60, 11:20-24. A POSITA would have known how to similarly fill the contents of Kwak's holes 53 with a dielectric material. Ex-1006, Fig. 7D; *see supra* Sections X.B.2, X.E.1.



199. A POSITA would have been motivated to put air gaps between the bit lines of the first trenches to reduce overall k-value, reduce capacitance, and improve RC relay. Ex-1006, ¶5 (“reduce capacitance between adjacent nanowires”). A POSITA would have had a reasonable likelihood of success because methods of creating air gaps with sealing caps was one of many known tools available to improve the capacitive properties of conductive interconnects, such as bit lines.

3. Dependent Claim 16: The method of claim 12 further comprising depositing the metal in the plurality of second trenches to cap air gaps in the plurality of second trenches.

200. Kwak in view of Zhang teaches capping air gaps in the second trenches with a metal capping layer for the reasons explained in Section X.E.2.

F. Ground 6: Claims 13-14 and 17 Are Obvious Over Kwak in view of Kao

1. A POSITA would have been motivated to combine Kwak with Kao

201. A POSITA would have been motivated to combine Kwak with Kao and would have a reasonable expectation of success in doing so, because they are both from the same field and relate to the same well-known issues. Kwak and Kao provide complementary solutions for manufacturing semiconductor devices using a sidewall transfer process. *Compare* Ex-1008, 1:20-23, 6:42-46, *with* Ex-1007, Abstract. For example, a POSITA wanting to have more flexibility or better control in etching a trench profile would have known of and consulted these proposed solutions.

202. Kwak discloses techniques for manufacturing a semiconductor device using a sidewall transfer process. *See, e.g.*, Ex-1008, Abstract, ¶¶5-6, 9-10, 59. Kwak describes forming sidewall spacers formed along the sidewalls of bit lines or of mask patterns. *See id.*, ¶¶59, 83.

203. Kao similarly discloses “a method of manufacturing a field effect transistor,” using sidewalls of gates to form spacers. Ex-1007, 1:35-36, 1:45-51. Kao specifically discloses forming sidewall spacers using portions of two dielectric layers that were formed together over a substrate. *See* Ex-1007, 1:6-10, 1:39-67.

204. A POSITA would have had a reasonable expectation of success in achieving their objectives, e.g., manufacturing a semiconductor device using

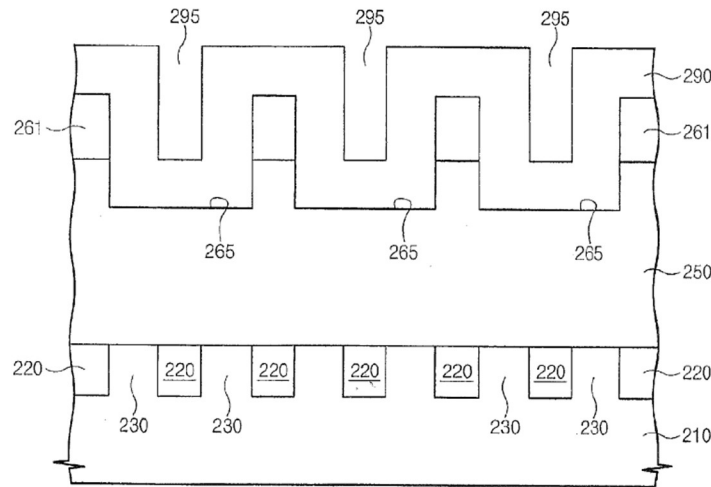
sidewall spacers, by combining the teachings of Kwak and Kao with no change in their respective functions because both references purport to solve these problems in similar and predictable ways, such as using the well-known teachings of manufacturing semiconductor memory using mask and etching techniques. *See infra* Sections X.F.2-4.

2. **Dependent Claim 13: The method of claim 12 further comprising, prior to etching the plurality of first trenches and the plurality of second trenches, forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.**

205. Kwak discloses using a second mask 110 and spacers 93 as an “etch mask.” Ex-1008, ¶60, Figs. 12-13. Although Kwak does not explicitly disclose a mask portion formed with both “a first material and a liner part that is formed of a second material,” it would have been obvious for a POSITA to modify Kwak to do so.

206. Kwak discloses a first mask pattern 261 that acts as a mandrel on a dielectric layer. Ex-1008, ¶ 73. Kwak states “[r]eferring to FIG. 21, a second insulation layer 290 having an *etching selectivity* with respect to the first mask pattern 261 is formed...In one embodiment, the second insulation layer 290 may...be formed on the side and top surfaces of the first mask pattern 261 and within the plurality of first grooves 265 defined within the first insulation layer 250.” Ex-1008, ¶74.

Fig. 21



Ex-1008, Fig. 21.

207. Thus, Kwak teaches adding a spacer layer over mask pattern 261 and first insulation layer 250.

208. Kao discloses a liner layer deposited before insulation layer 290 is added. Kao's mask including a liner layer is discussed above.

209. Kao discloses "dielectric layer 114 is formed over the substrate 100" and made from silicon oxide. Ex-1007, 2:39-41. Kao then discloses "dielectric layer 116 is formed on the dielectric layer 114," which is made of silicon nitride. Ex-1007, 2:39-43. Kao further describes subsequently etching dielectric layers 116 and 114 to form "first spacer 116b...located at the sidewall of the gate 106a" and "remaining dielectric layer 114a," respectively. Ex-1007, 2:44-66. Dielectric layer parts 114a and 116b "together form a third spacer 117." Ex-1007, 2:66-67. Kao's Figures 2 and

5 annotated below show a mask portion comprising sidewall spacer material 116b (pink) and liner 114a (cyan) made of different materials that corresponds to claimed mask portion.

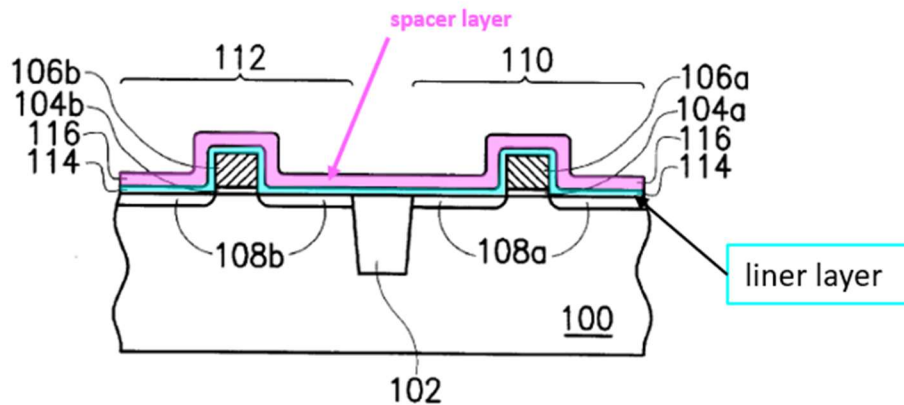


FIG. 2

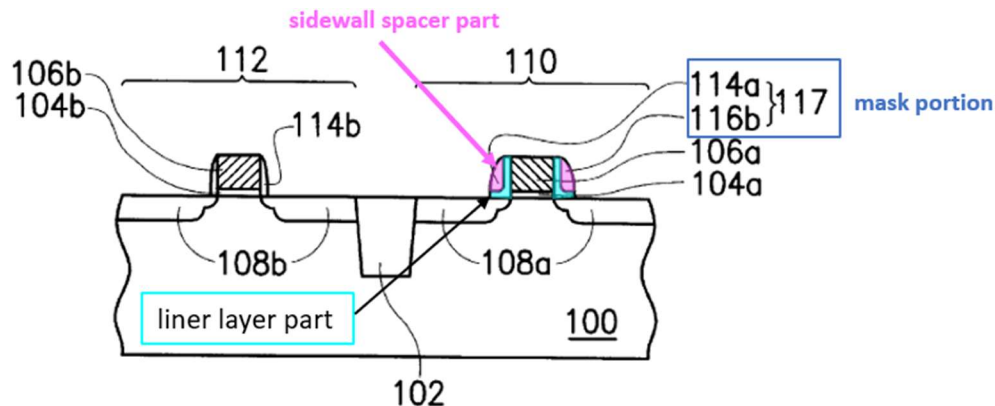


FIG. 5

Ex-1007, Figs. 2, 5 (annotated).

210. A POSITA would have found it obvious to use a dual-layer spacer like that taught in Kao, instead of single layer 417, because doing so provides better flexibility for the type of profile for even bit lines. Ex-1034, 4:58-5:13. In contrast, a single layer constrains a POSITA to a limited range of trench profiles because there

is less contrast in etch selectivity. A POSITA would have known that by modifying Kwak's steps to deposit an additional liner layer over mask pattern 261 and exposed parts of first insulation layer 250 *before* second insulation layer 290 was deposited would improve the subsequent etching of first insulation layer 250. A POSITA wanting to have better flexibility for the etching process or to tailor the trench's profile would have known how to use etch selectivity to select different materials with different chemistries and etch rates to accomplish specific goals. Etch selectivity is the ratio between two etch rates, usually between a material being etched and a mask. A higher selectivity generally means it will be easier to etch a vertical profile. The selectivity can be adjusted by adjusting the processes or mask material, which affects etch rates. For example, a POSITA not wanting to over-etch first insulation layer 250 would have known that a liner layer made of a different material than second insulation layer and first insulation layer would have a different etch rate and therefore would act as an etch stop to prevent unintended etching of first insulation layer. *See* Ex-1039, N3033-N3034. By switching chemistries, a POSITA would have more control over the etch process that results in a more precisely etched trench.

211. A POSITA would have also found it obvious to continue with the rest of Kwak's steps after adding the liner layer to form the rest of the NAND flash memory. For example, second insulation layer 290 would then extend over the liner

layer. *See* Ex-1005, 5:2-22. As shown below, Kwak's Modified Figure 21' second insulation layer 290 (pink) formed on liner layer (cyan) along side surfaces of mask pattern 261 is similar to Figure 4A of the '974 Patent.

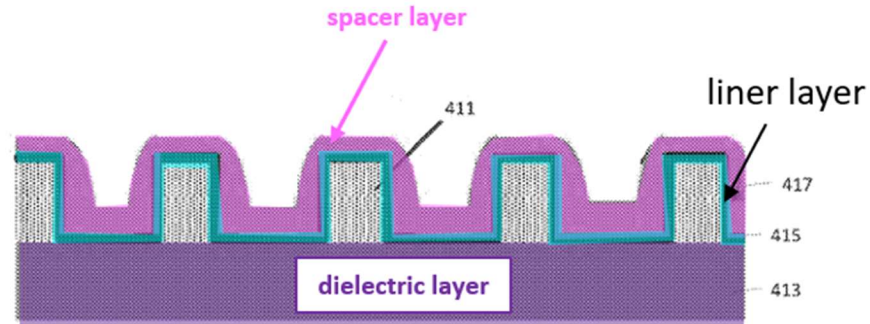
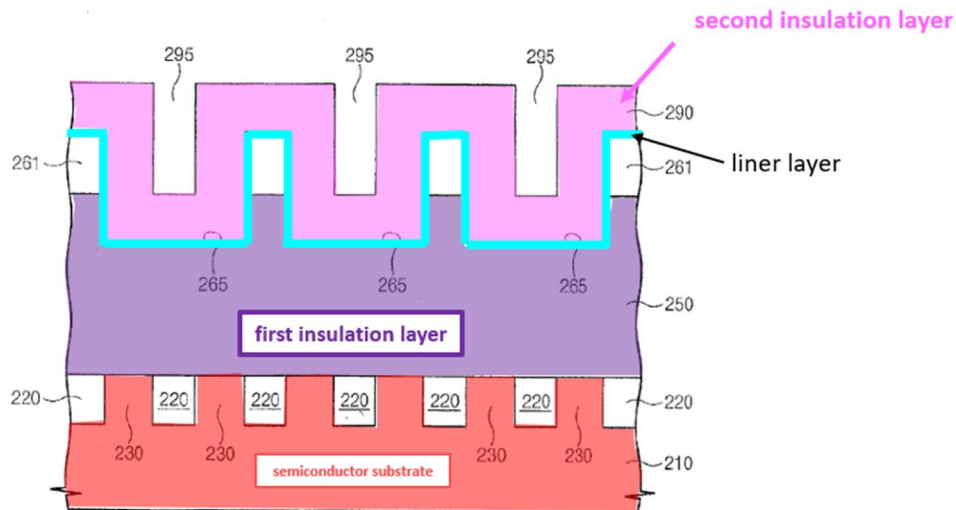


Fig. 21'



'974 Patent, Fig. 4A (annotated); Ex-1008, Fig. 21' (modified and modified).

212. Kwak teaches second insulation layer 290 can “be formed on the sidewall of the mask pattern 261...as a spacer 297 instead of being formed by filling the first groove,” as shown in Figure 27. Ex-1008, ¶83. A POSITA would have

known that portions of liner layer (cyan) on top of mask pattern 261 would also be etched away so that mask pattern 261 could be removed. A POSITA would have known to use different materials for the sidewall spacer and the liner layer. As demonstrated in a comparison with Figure 4B of the '974 Patent, Kwak's Modified Figure 27' spacers 297 (pink) and liner layer portions (cyan) together correspond to the claimed "a plurality of mask portions [(blue bracket)], each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material."

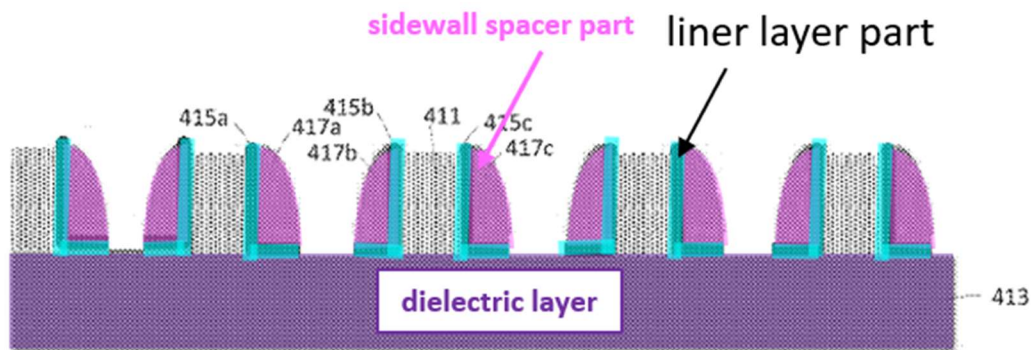
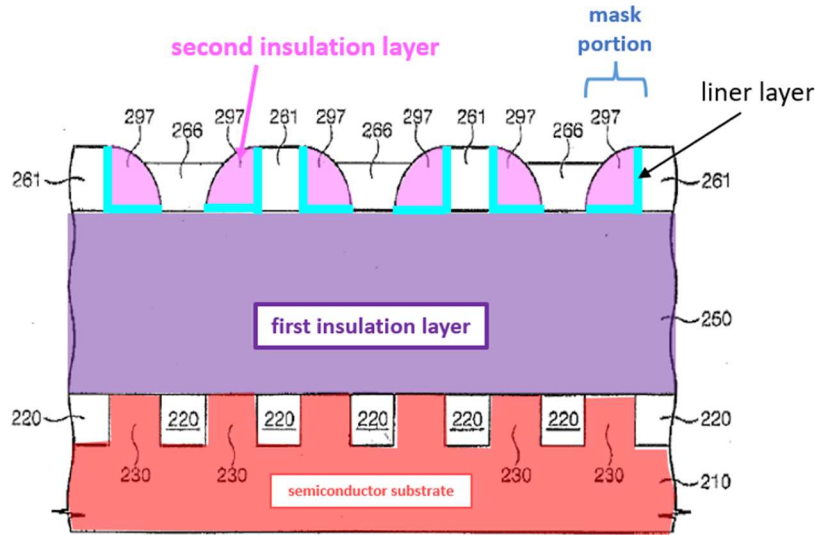


FIG. 4B

Fig. 27'



'974 Patent, Fig. 4B (annotated); Ex-1008, Fig. 27' (modified and annotated).

213. Kwak states that after spacers 297 are formed, “[t]he process for forming the bit line contacts and bit lines may then proceed.” Ex-1008, ¶83. Thus, Kwak’s mask portions are formed “prior to etching the plurality of first trenches and the plurality of second trenches.” Accordingly, Kwak in view of Kao teaches Claim 13.

3. Dependent Claim 14: The method of claim 13 wherein the second material has a higher etch rate than the first material and wherein first trenches are formed at locations corresponding to locations of liner parts of neighboring mask portions.

214. The '974 Patent explains that an etch selective to the liner layer material is used to remove dielectric layer and liner layer portions along sidewall spacers to form T1 trenches “between pairs of sidewall spacers 417b-c.” Ex-1001, 8:61-9:6. As

a result, T1 trenches are “wider at the top than at the bottom,” compared to T2 trenches which “remain substantially uniform.” Ex-1001, 9:6-19.

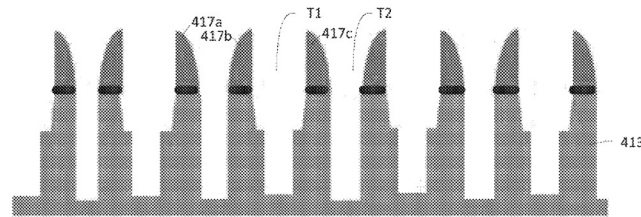


FIG. 4D

Id., Fig. 4D.

215. Using the same modification to Kwak described for Claim 13, a POSITA would have known to use a liner layer material (i.e., second material) that has a higher etch rate than the sidewall spacer part material (i.e., first material). *See supra* Section X.F.2.

216. Kwak discloses selecting materials “having an etching selectivity” with respect to surrounding layers. *See, e.g.*, Ex-1008, ¶¶73-75.

217. Kao discloses an etch selectivity for a liner layer compared to a spacer layer for the reasons explained in Section X.C.3. A POSITA would have understood that one can tailor the conditions and chemistry of an etch such that layer 114 is etched at a higher rate than that of layer 116.

218. Applying Kao’s teaching to Kwak, a POSITA would have been motivated to select a liner layer material with a higher etch rate than the sidewall spacer part material because doing so would allow for the etching tool to etch

through the more resistant liner layer, while also creating a more concave shape trench in the less-resistant sidewall spacer material. A trench shape that is more concave decreases the likelihood of voids forming during in the trench when the trench is subsequently filled.

219. In addition, a POSITA would have known to use a liner layer material (i.e., second material) that has a higher etch rate than the sidewall spacer part material (i.e., first material). Ex-1030; *see supra* Section X.F.2.

4. Independent Claim 17

- a. Element 17[preamble]: A method of forming a NAND flash memory comprising:
Element 17[a]: forming a plurality of NAND strings disposed on a surface of a substrate;
Element 17[b]: depositing a dielectric layer over the plurality of NAND strings;**

220. Kwak-Kao discloses Elements 17[preamble]-[b] for the same reasons Kwak discloses Elements 12[preamble]-[b]. *See supra* Sections X.D.5.a-c; Ex-1020.

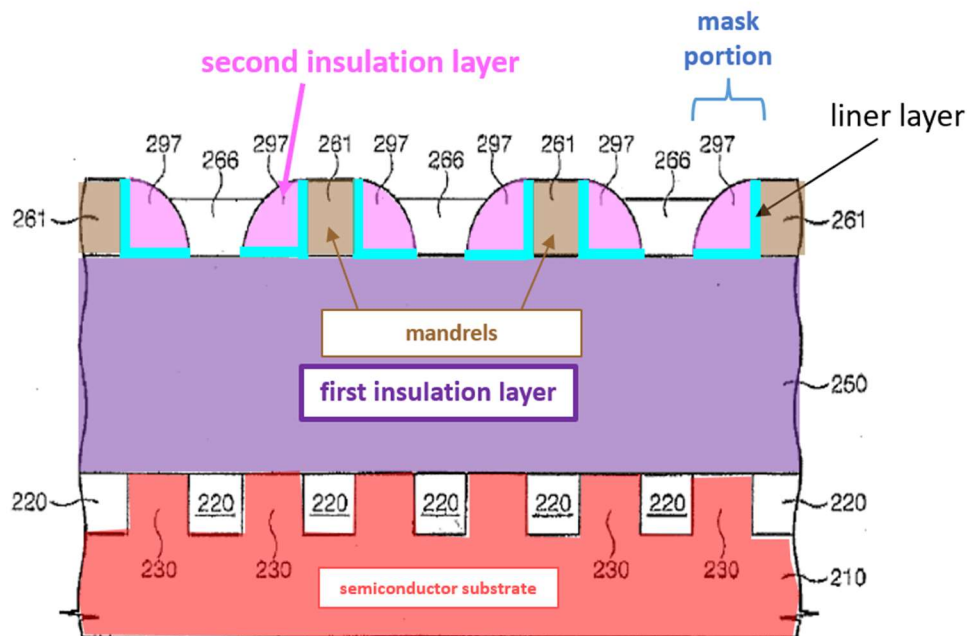
- b. Element 17[c]: forming a plurality of mandrels on the dielectric layer;**

221. The '974 Patent uses “mandrels...formed on the surface of a dielectric layer” to form sidewall spacers. *See* Ex-1001, 7:61-65, 8:8:21-24, Figs. 3A, 4A. It states “mandrels may be formed first by an appropriate process” and when removed “leave[] masking portions.” *Id.*, 8:25, 8:53-60, Fig. 4C.

222. Kwak discloses “[a] first mask pattern 261 is formed to cover odd device isolation regions” and “second insulation layer 290...can be formed on the sidewall of the first mask pattern 261 (e.g., within grooves of the first mask pattern 261) as a spacer 297.” Ex-1008, ¶¶ 73-74, 83.

223. A POSITA would have understood first mask pattern 261 are mandrels because it serves as a pattern for subsequent sidewall spacers, as illustrated below in modified Figure 27’.

Fig. 27’



Ex-1008, Fig. 27’ (modified and annotated).

- c. **Element 17[d]: forming a liner layer along side surfaces of the plurality of mandrels; Element 17[e]: forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels; Element 17[f]: removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material;**

224. Kwak-Kao teaches Elements 17[d]-[f] for the same reasons it teaches Claim 13. Ex-1020; *see supra* Section X.F.2.

- d. **Element 17[g]: subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel;**

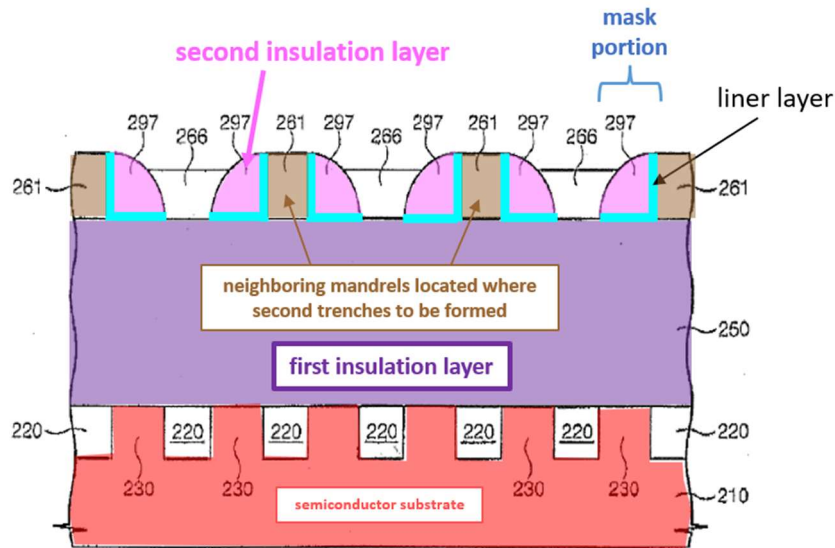
225. Kwak-Kao teaches Element 17[g] for the same reasons Kwak teaches Element 12[c]. Ex-1020; *see supra* Section X.D.5.d.

- e. **Element 17[h]: etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and**

226. Kwak-Kao teaches etching second trenches in the dielectric layer for the same reasons Kwak teaches Element 12[d]. *Supra* Section X.D.5.d. And, Kwak-Kao teaches trenches etched into the dielectric layer between sidewall spacers that were formed on mandrels. *See supra* Section X.F.2.

227. As shown in Kwak's modified Figure 27' below, sidewall spacers 297 (pink) are formed on neighboring mandrels 261 (brown). *See* Ex-1008 ¶¶73, 83; *supra* Section X.F.4.b.

Fig. 27'



Ex-1008, Fig. 27' (modified and annotated).

228. A POSITA would have known to etch second trenches between the sidewall spacers 261 (pink and cyan) after neighboring mandrels (brown) are removed.

- f. **Element 17[i]: depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches.**

229. Kwak discloses bit lines made of metal. Ex-1008, ¶63. A POSITA would have found it obvious to use copper as a bit line material. *See, e.g., supra* Section X.C.4.f (Matsuno's copper deposition); Ex-1039, N3029. Thus, Kwak in view of Kao teaches "depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches."

XI. CONCLUSION

230. The unpatentability grounds presented above are reasonably likely to prevail, and IPR should be instituted for Claims 1-2, 4, 6, and 11-18 of the '974 Patent based on each of the grounds specified in this Petition.

Dated: October 14, 2025

Respectfully submitted,



Dr. David Kuan-Yu Liu