

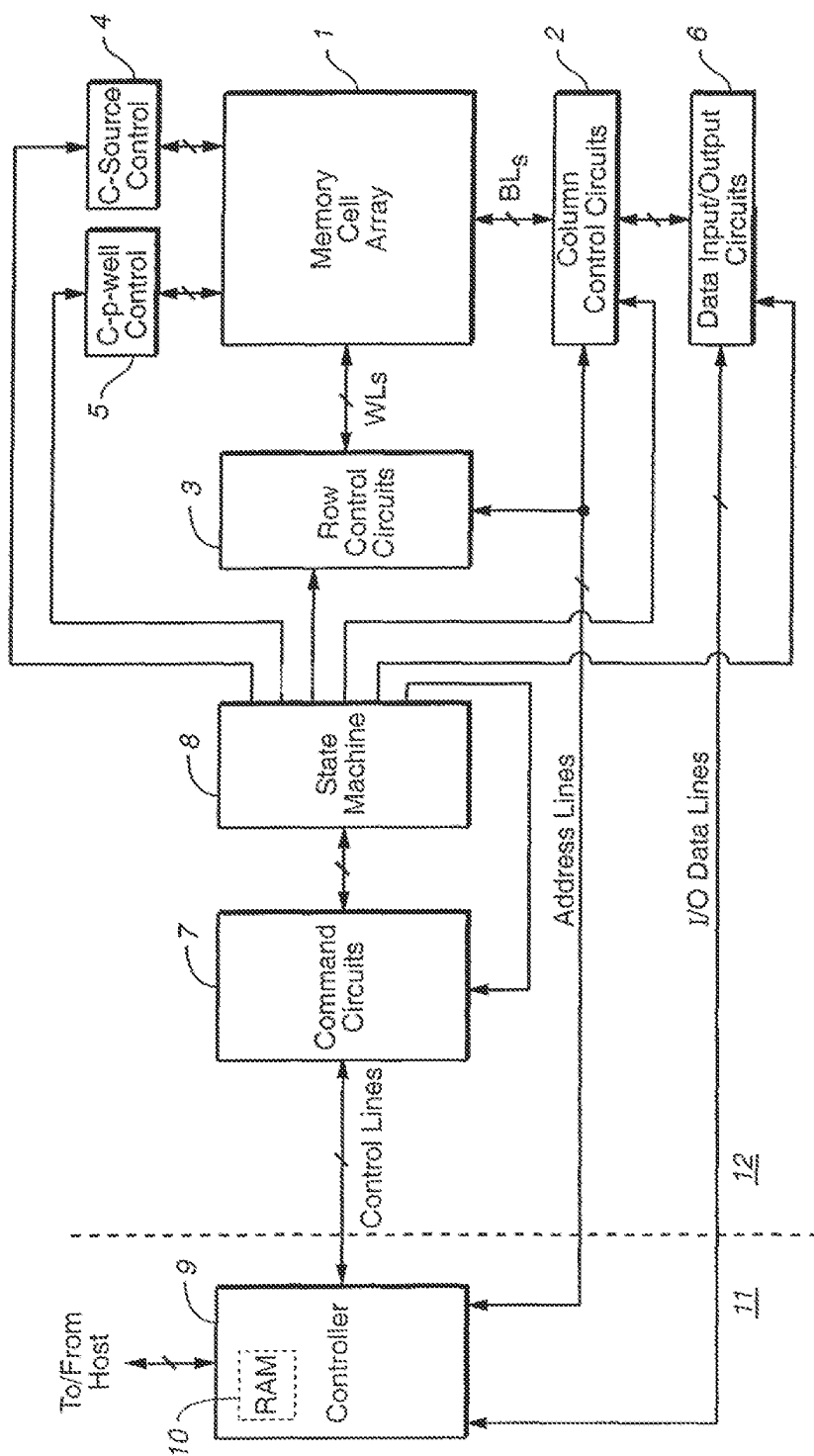


FIG. 1
(Prior Art)

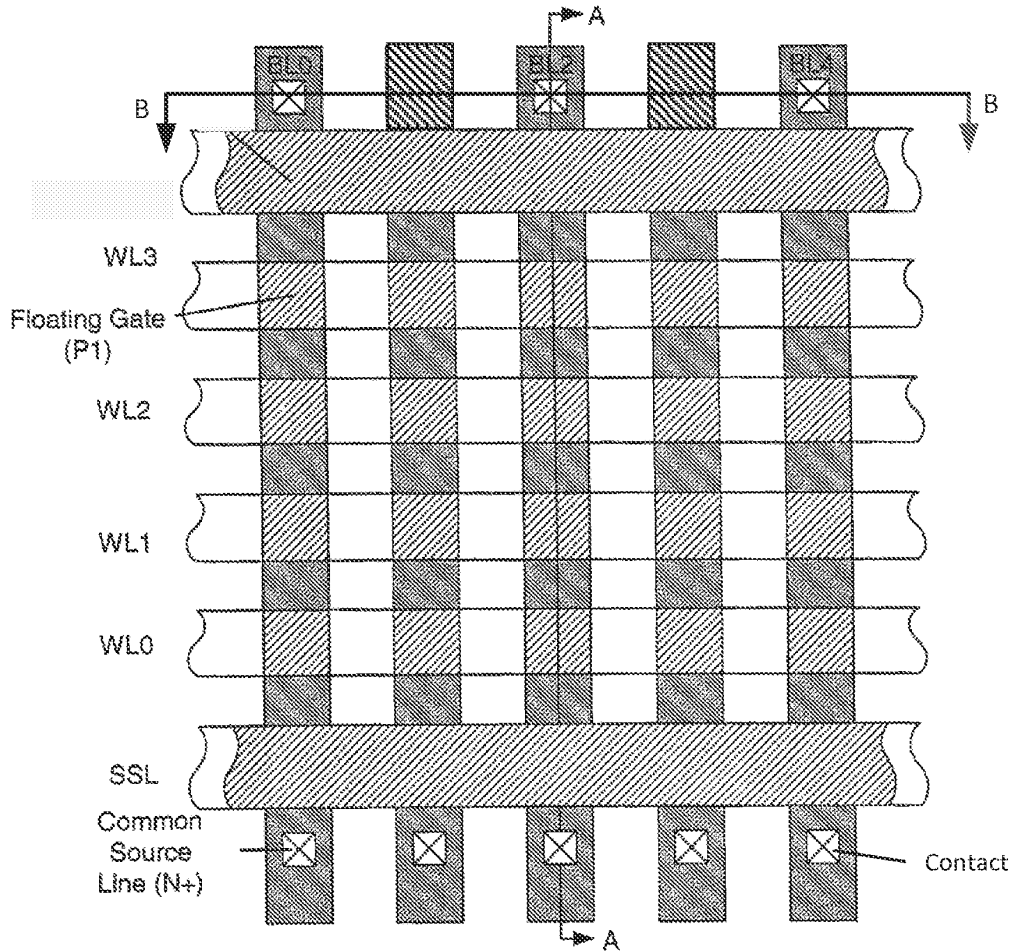


FIG. 2A (PRIOR ART)

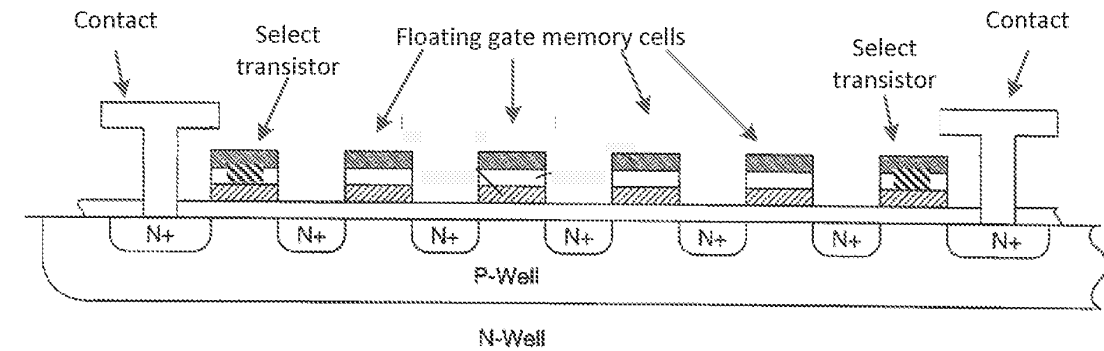


FIG. 2B (PRIOR ART)
(Section A-A)

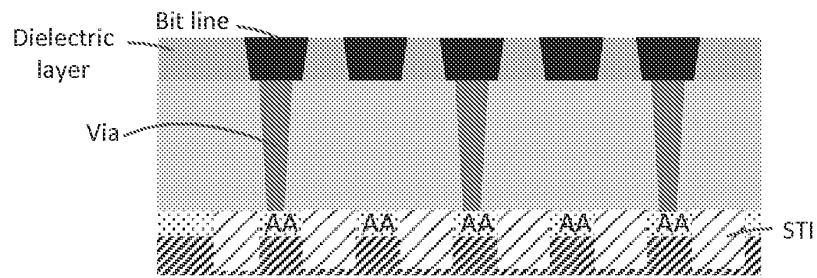


FIG. 2C (Prior Art)
(Section B-B)

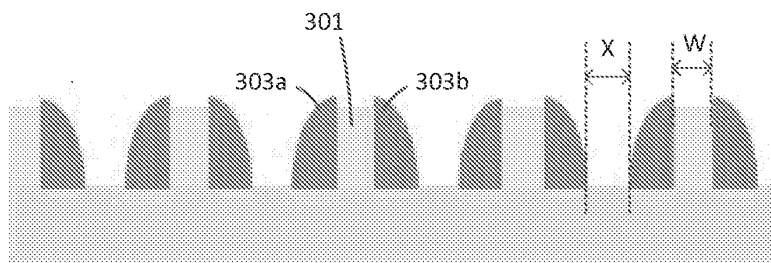


FIG. 3A

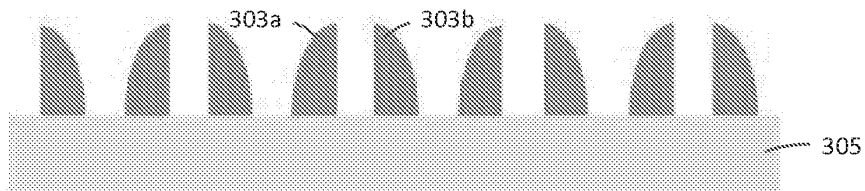


FIG. 3B

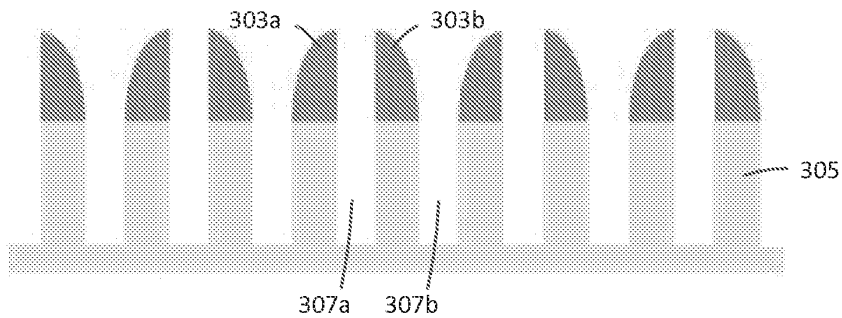


FIG. 3C

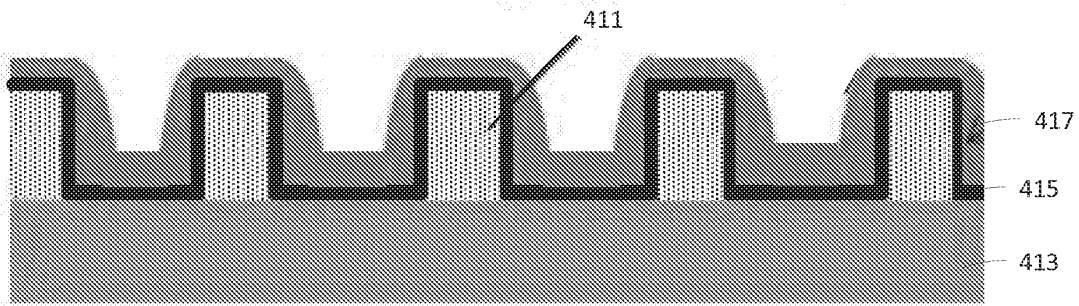


FIG. 4A

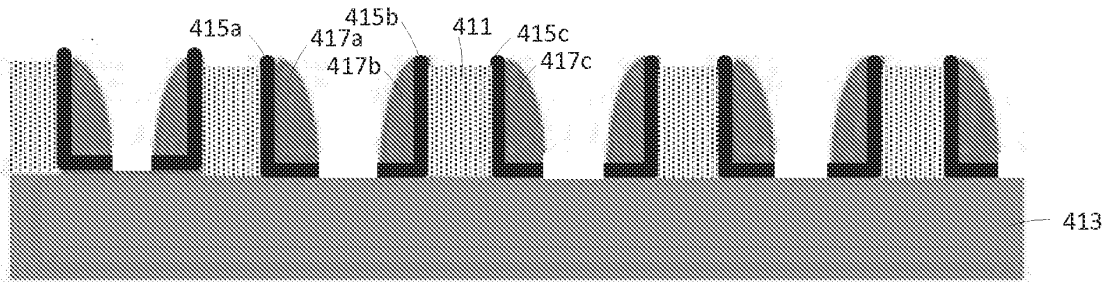


FIG. 4B

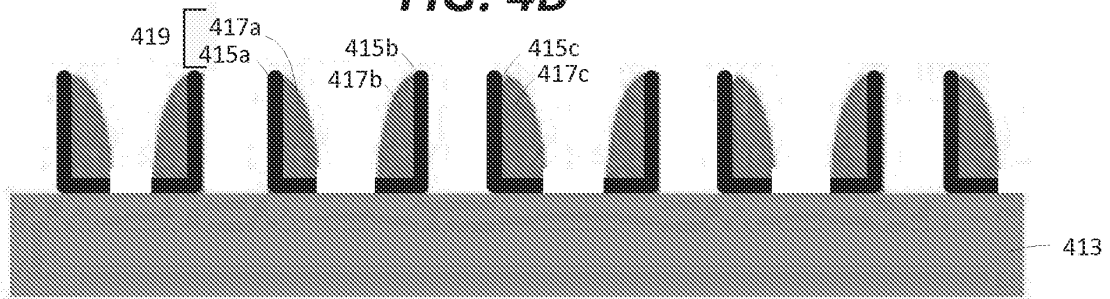


FIG. 4C

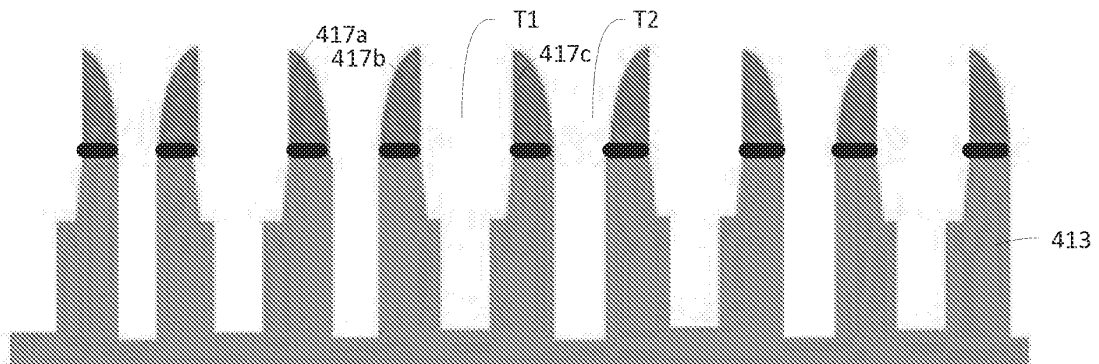


FIG. 4D

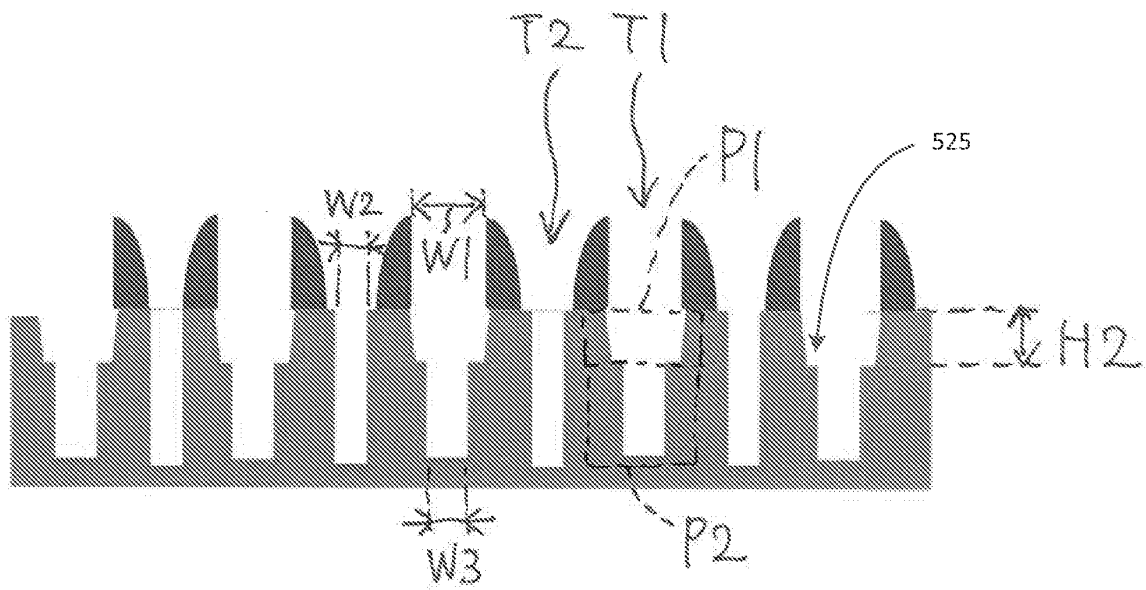


FIG. 5

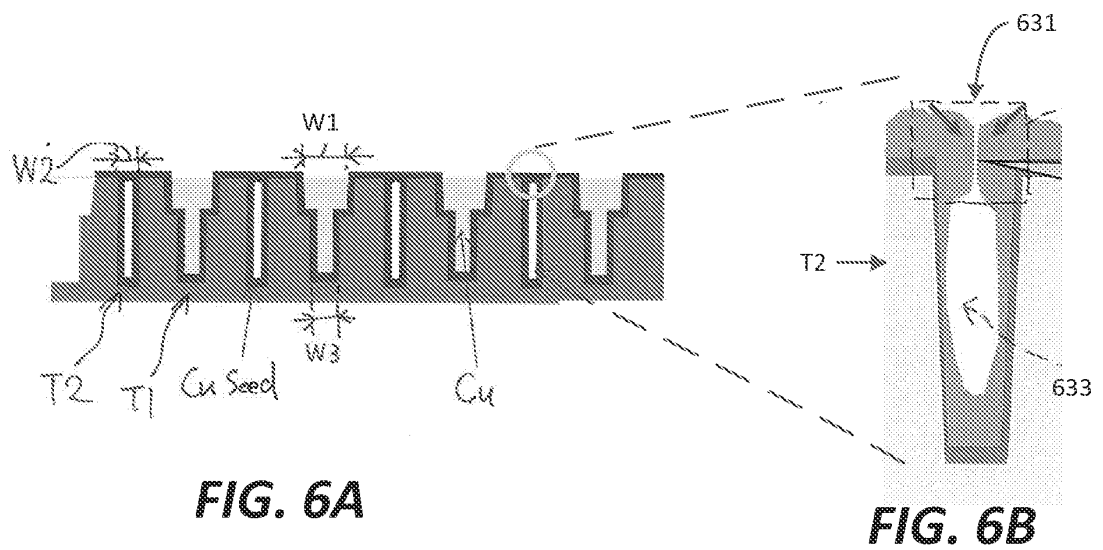


FIG. 6A

FIG. 6B

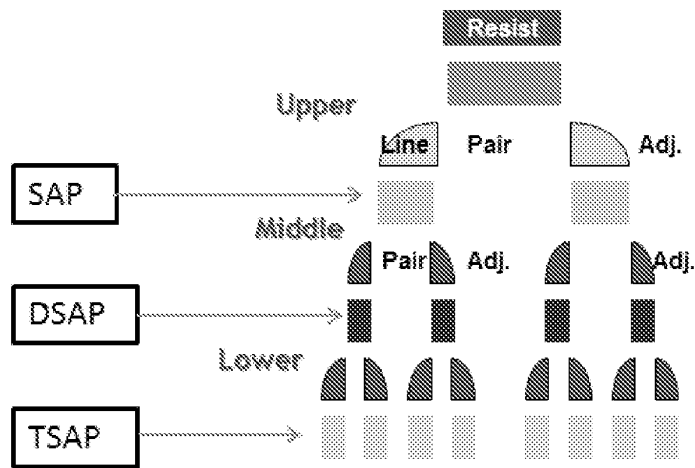


FIG. 7

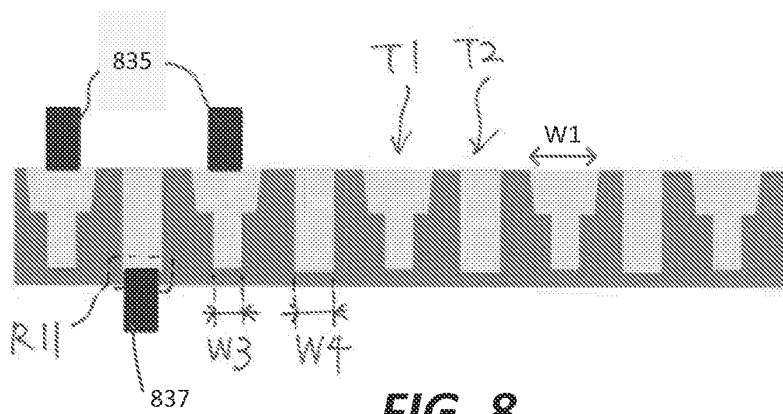


FIG. 8

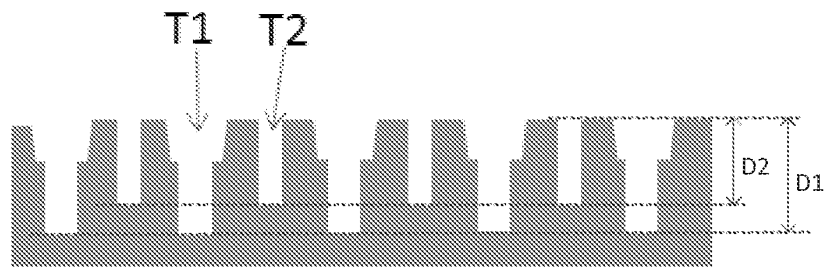


FIG. 9A

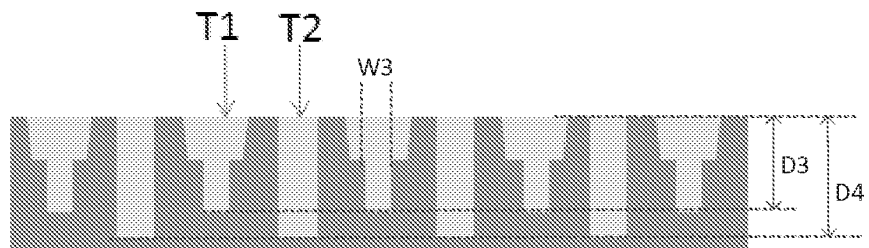


FIG. 9B

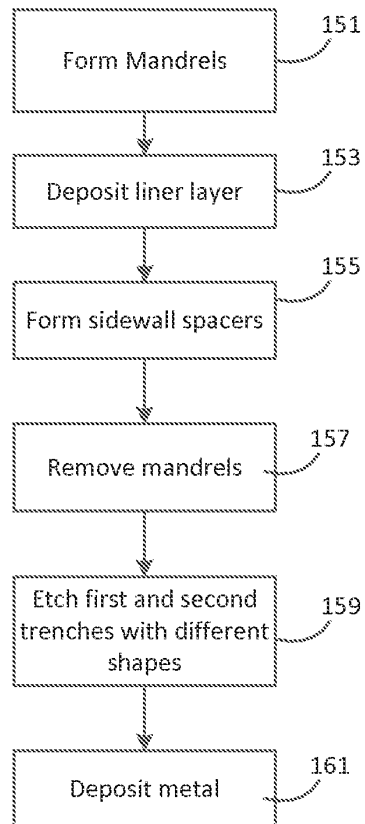


FIG. 10

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0084567-986US0
		Application Number	
Title of Invention	Alternating Sidewall Assisted Patterning		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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Postal Code	95035	Country¹	US		
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Legal Name					
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Title of Invention	Alternating Sidewall Assisted Patterning		

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Inventor 4

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Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
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Title of Invention	Alternating Sidewall Assisted Patterning		

Application Information:

Title of the Invention	Alternating Sidewall Assisted Patterning		
Attorney Docket Number	0084567-986US0	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	5

Filing By Reference :

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0084567-986US0
		Application Number	
Title of Invention	Alternating Sidewall Assisted Patterning		

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Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
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Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0084567-986US0
		Application Number	
Title of Invention	Alternating Sidewall Assisted Patterning		

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☐ Person to whom the inventor is obligated to assign.	☐ Person who shows sufficient proprietary interest	
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Name of the Deceased or Legally Incapacitated Inventor :		
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Organization Name	SanDisk Technologies, Inc.	

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		Application Number	
Title of Invention	Alternating Sidewall Assisted Patterning		

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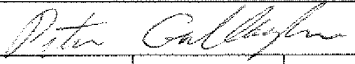
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		Application Number	
Title of Invention	Alternating Sidewall Assisted Patterning		

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NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
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First Name	Peter A.	Last Name	Gallagher	Registration Number	47584
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ALTERNATING SIDEWALL ASSISTED PATTERNING

Inventors: Erika Kanezaki
Ryo Nakamura
Kotaro Jinnouchi
Satoshi Kamata

BACKGROUND

[0001] This application relates generally to non-volatile semiconductor memories of the flash memory type, their formation, structure and use.

[0002] There are many commercially successful non-volatile memory products being used today, particularly in the form of small form factor cards, USB drives, embedded memory, and Solid State Drives (SSDs) which use an array of flash EEPROM cells. An example of a flash memory system is shown in FIG. 1, in which a memory cell array 1 is formed on a memory chip 12, along with various peripheral circuits such as column control circuits 2, row control circuits 3, data input/output circuits 6, etc.

[0003] One popular flash EEPROM architecture utilizes a NAND array, wherein a large number of strings of memory cells are connected through one or more select transistors between individual bit lines and a reference potential. A portion of such an array is shown in plan view in Figure 2A. Although four floating gate memory cells are shown in each string, the individual strings typically include 16, 32 or more memory cell charge storage elements, such as floating gates, in a column. Control gate (word) lines labeled WL0 – WL3 and string selection lines, Drain Select Line, “DSL” and Source Select Line “SSL” extend across multiple strings over rows of floating gates. An individual cell within a column is read and verified during programming by causing the remaining cells in the string to be turned on hard by placing a relatively high voltage on their respective word lines and by placing a relatively lower voltage on the one selected word line so that the current flowing through each string is primarily dependent only upon the level of charge stored in the addressed cell below the selected word line. That current typically is sensed for a large number of strings in parallel, thereby to read charge level

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states along a row of floating gates in parallel.

[0004] The top and bottom of the string connect to the bit line and a common source line respectively through select transistors (source select transistor and drain select transistor). Select transistors do not contain floating gates and are used to connect NAND strings to control circuits when they are to be accessed, and to isolate them when they are not being accessed.

[0005] NAND strings are generally connected by conductive lines in order to form arrays that may contain many NAND strings. At either end of a NAND string a contact area may be formed. This allows connection of the NAND string as part of the array. Metal contact plugs (or “vias”) may be formed over contact areas to connect the contact areas (and thereby connect NAND strings) to conductive metal lines that extend over the memory array (e.g. bit lines). FIG. 2A shows bit line contacts BL0-BL4 and common source line contacts at either end of NAND strings. Contacts to contact areas may be formed by etching contact holes through a dielectric layer and then filling the holes with metal to form vias. Metal lines, such as bit lines, extend over the memory array and in peripheral areas in order to connect the memory array and various peripheral circuits. Electrical contact between metal lines and vias occurs where horizontal metal lines intersect vertical contact plugs. These metal lines may be close together (particularly in the memory array area where bit lines may be very close) which tends to make processing difficult and provides a risk of capacitive coupling. The characteristics of such lines (e.g. resistance and coupling) and the quality of connections with vias may be significant factors for good memory operation.

[0006] Thus, there is a need for an integrated circuit manufacturing process that forms conductive lines, such as bit lines, in close proximity in an efficient manner.

SUMMARY

[0007] A sidewall assisted process may be used to form trenches, e.g. for bit lines, or other conductive lines, so that trenches alternate between two different profiles. For example, a first trench profile may have an upper portion that is significantly wider than a lower portion, while a second trench profile may be substantially rectangular, having the same width from top to bottom. In one example, metal (e.g. copper) is deposited so that air gaps are formed in second trenches while metal is deposited substantially void-free in first trenches. In another example, substantially void-free metal is deposited in both first and second trenches so that alternating conductive lines are formed. Lines formed in first trenches may have wider upper surfaces that facilitate connection of contact plugs from above (e.g. greater tolerance for misalignment). Lines formed in second trenches may have wider lower surfaces that facilitate connection with underlying contact plugs. First and second trenches may be formed so that they have different depths.

[0008] An example of a NAND flash memory includes: a semiconductor substrate; a dielectric layer extending over the semiconductor substrate; a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction; a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the first and second trenches arranged in an alternating pattern; and a plurality of bit lines located in the first trenches.

[0009] A plurality of additional bit lines may be located in the second trenches. The plurality of bit lines and the plurality of additional bit lines may be formed of copper. The first shape may have a first width at a level of an upper surface of the dielectric layer, the second shape may have a second width at the level of the upper surface of the dielectric layer, and the second width may be less than the first width. The first shape may have a third width at a bottom surface of the first shape, the third width being substantially less than the second width, and the second shape may have substantially the second width from top to bottom. A plurality of air gaps may be located in the second trenches. The plurality of first trenches may be filled with copper that forms the

plurality of bit lines and the plurality of second trenches may be capped by copper that seals the plurality of air gaps in the second trenches. An individual first trench may have a cross sectional area along the plane that is equal to a cross sectional area of an individual second trench along the plane. The first shape may have an upper portion that extends from a level of an upper surface of the dielectric layer down to an intermediate level with tapering sidewalls, and may have a lower portion that extends from the intermediate level to a bottom surface of the first shape, the lower portion having substantially parallel sidewalls. The second shape may be substantially rectangular. The plurality of first trenches may have a first depth and the plurality of second trenches may have a second depth.

[0010] An example of a method of forming a NAND flash memory includes: forming a plurality of NAND strings disposed on a surface of a substrate; depositing a dielectric layer over the plurality of NAND strings; etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction; etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the first and second trenches arranged in an alternating pattern; and depositing metal in the plurality of first trenches to form a plurality of bit lines located in the first trenches.

[0011] Prior to etching the plurality of first trenches and the plurality of second trenches, an etch mask may be formed that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material. The second material may have a higher etch rate than the first material and first trenches may be formed at locations corresponding to locations of liner parts of neighboring mask portions. The metal may be deposited in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches. The metal may be deposited in the plurality of second trenches to cap air gaps in the plurality of second trenches.

[0012] An example of a method of forming a NAND flash memory includes: forming a plurality of NAND strings disposed on a surface of a substrate; depositing a dielectric layer over the

plurality of NAND strings; forming a plurality of mandrels on the dielectric layer; forming a liner layer along side surfaces of the plurality of mandrels; forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels; removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material; subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel; etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches.

[0013] Copper may be deposited in the plurality of second trenches to form a plurality of additional bit lines. Depositing copper may include electroplating with conditions that provide substantially void-free filling of the plurality of first trenches and provide significant air-gaps in the plurality of second trenches. The dielectric layer may be formed of silicon oxide, the liner layer may be formed of silicon oxide, the sidewall spacers may be formed of silicon nitride, and the etching may use anisotropic etching that has a significantly higher etch rate for silicon oxide than for silicon nitride.

[0014] Various aspects, advantages, features and embodiments are included in the following description of examples, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] FIG. 1 is a block diagram of a prior art memory system.

[0016] FIG. 2A is a plan view of a prior art NAND array.

[0017] FIG. 2B shows a cross section of the NAND array of FIG. 2A.

[0018] FIG. 2C shows another cross section of the NAND array of FIG. 2A.

[0019] FIGs. 3A-C illustrate an example of sidewall assisted patterning.

[0020] FIGs. 4A-D illustrate another example of sidewall assisted patterning.

[0021] FIG. 5 shows different trench patterns formed by the process of FIGs. 4A-D.

[0022] FIGs. 6A-B illustrate formation of conductive lines in first trenches and air gaps in second trenches.

[0023] FIG. 7 illustrates different sidewall assisted processes.

[0024] FIG. 8 shows different uses for first and second conductive lines with different profiles.

[0025] FIGs. 9A-B show first and second trenches with different depths.

[0026] FIG. 10 shows an example of steps used to form a pattern of alternating first and second trenches.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

Memory System

[0027] Semiconductor memory devices include volatile memory devices, such as dynamic random access memory (“DRAM”) or static random access memory (“SRAM”) devices, non-volatile memory devices, such as resistive random access memory (“ReRAM”), electrically erasable programmable read only memory (“EEPROM”), flash memory (which can also be considered a subset of EEPROM), ferroelectric random access memory (“FRAM”), and magnetoresistive random access memory (“MRAM”), and other semiconductor elements capable of storing information. Each type of memory device may have different configurations. For example, flash memory devices may be configured in a NAND or a NOR configuration.

[0028] The memory devices can be formed from passive and/or active elements, in any combinations. By way of non-limiting example, passive semiconductor memory elements include ReRAM device elements, which in some embodiments include a resistivity switching storage element, such as an anti-fuse, phase change material, etc., and optionally a steering element, such as a diode, *etc.* Further by way of non-limiting example, active semiconductor memory elements include EEPROM and flash memory device elements, which in some embodiments include elements containing a charge storage region, such as a floating gate, conductive nanoparticles, or a charge storage dielectric material.

[0029] Multiple memory elements may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory devices in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a string is composed of multiple memory elements sharing a single bit line and accessed as a group. Alternatively, memory elements may be configured so that each element is individually accessible, *e.g.*, a NOR memory array. NAND and NOR memory configurations are exemplary, and memory elements may be otherwise configured.

[0030] The semiconductor memory elements located within and/or over a substrate may be

arranged in two or three dimensions, such as a two dimensional memory structure or a three dimensional memory structure.

[0031] In a two dimensional memory structure, the semiconductor memory elements are arranged in a single plane or a single memory device level. Typically, in a two dimensional memory structure, memory elements are arranged in a plane (*e.g.*, in an x-z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements. The substrate may be a wafer over or in which the layer of the memory elements are formed or it may be a carrier substrate which is attached to the memory elements after they are formed. As a non-limiting example, the substrate may include a semiconductor such as silicon.

[0032] The memory elements may be arranged in the single memory device level in an ordered array, such as in a plurality of rows and/or columns. However, the memory elements may be arrayed in non-regular or non-orthogonal configurations. The memory elements may each have two or more electrodes or contact lines, such as bit lines and word lines.

[0033] A three dimensional memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three dimensions (*i.e.*, in the x, y and z directions, where the y direction is substantially perpendicular and the x and z directions are substantially parallel to the major surface of the substrate).

[0034] As a non-limiting example, a three dimensional memory structure may be vertically arranged as a stack of multiple two dimensional memory device levels. As another non-limiting example, a three dimensional memory array may be arranged as multiple vertical columns (*e.g.*, columns extending substantially perpendicular to the major surface of the substrate, *i.e.*, in the y direction) with each column having multiple memory elements in each column. The columns may be arranged in a two dimensional configuration, *e.g.*, in an x-z plane, resulting in a three dimensional arrangement of memory elements with elements on multiple vertically stacked memory planes. Other configurations of memory elements in three dimensions can also constitute a three dimensional memory array.

[0035] By way of non-limiting example, in a three dimensional NAND memory array, the

memory elements may be coupled together to form a NAND string within a single horizontal (e.g., x-z) memory device levels. Alternatively, the memory elements may be coupled together to form a vertical NAND string that traverses across multiple horizontal memory device levels. Other three dimensional configurations can be envisioned wherein some NAND strings contain memory elements in a single memory level while other strings contain memory elements which span through multiple memory levels. Three dimensional memory arrays may also be designed in a NOR configuration and in a ReRAM configuration.

[0036] Typically, in a monolithic three dimensional memory array, one or more memory device levels are formed above a *single* substrate. Optionally, the monolithic three dimensional memory array may also have one or more memory layers at least partially within the single substrate. As a non-limiting example, the substrate may include a semiconductor such as silicon. In a monolithic three dimensional array, the layers constituting each memory device level of the array are typically formed on the layers of the underlying memory device levels of the array. However, layers of adjacent memory device levels of a monolithic three dimensional memory array may be shared or have intervening layers between memory device levels.

[0037] Then again, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device having multiple layers of memory. For example, non-monolithic stacked memories can be constructed by forming memory levels on separate substrates and then stacking the memory levels atop each other. The substrates may be thinned or removed from the memory device levels before stacking, but as the memory device levels are initially formed over separate substrates, the resulting memory arrays are not monolithic three dimensional memory arrays. Further, multiple two dimensional memory arrays or three dimensional memory arrays (monolithic or non-monolithic) may be formed on separate chips and then packaged together to form a stacked-chip memory device.

[0038] Associated circuitry is typically required for operation of the memory elements and for communication with the memory elements. As non-limiting examples, memory devices may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. This associated circuitry may be on the same substrate as the

memory elements and/or on a separate substrate. For example, a controller for memory read-write operations may be located on a separate controller chip and/or on the same substrate as the memory elements.

[0039] In other embodiments, types of memory other than the two dimensional and three dimensional exemplary structures described here may be used.

[0040] An example of a prior art memory system, which may be modified to include various structures described here, is illustrated by the block diagram of FIG. 1. A planar memory cell array 1 including a plurality of memory cells is controlled by a column control circuit 2, a row control circuit 3, a c-source control circuit 4 and a c-p-well control circuit 5. The memory cell array 1 is, in this example, of the NAND type similar to that described above in the Background. A control circuit 2 is connected to bit lines (BL) of the memory cell array 1 for reading data stored in the memory cells, for determining a state of the memory cells during a program operation, and for controlling potential levels of the bit lines (BL) to promote the programming or to inhibit the programming. The row control circuit 3 is connected to word lines (WL) to select one of the word lines (WL), to apply read voltages, to apply program voltages combined with the bit line potential levels controlled by the column control circuit 2, and to apply an erase voltage coupled with a voltage of a p-type region on which the memory cells are formed. The c-source control circuit 4 controls a common source line (labeled as "c-source" in Figure 1) connected to the memory cells (M). The c-p-well control circuit 5 controls the c-p-well voltage.

[0041] The data stored in the memory cells are read out by the column control circuit 2 and are output to external I/O lines via an I/O line and a data input/output buffer 6. Program data to be stored in the memory cells are input to the data input/output buffer 6 via the external I/O lines, and transferred to the column control circuit 2. The external I/O lines are connected to a controller 9. The controller 9 includes various types of registers and other memory including a volatile random-access-memory (RAM) 10.

[0042] The memory system of Figure 1 may be embedded as part of the host system, or may be included in a memory card, USB drive, or similar unit that is removably insertible into a mating socket of a host system. Such a card may include the entire memory system, or the controller

and memory array, with associated peripheral circuits, may be provided in separate cards. The memory system of FIG. 1 may also be used in a Solid State Drive (SSD) or similar unit that provides mass data storage in a tablet, laptop computer, or similar device. Memory systems may be used with a variety of hosts in a variety of different environments. For example, a host may be a mobile device such as a cell phone, laptop, music player (e.g. MP3 player), Global Positioning System (GPS) device, tablet computer, or the like. Such memory systems may be inactive, without power, for long periods during which they may be subject to various conditions including high temperatures, vibration, electromagnetic fields, etc. Memory systems for such hosts, whether removable or embedded, may be selected for low power consumption, high data retention, and reliability in a wide range of environmental conditions (e.g. a wide temperature range). Other hosts may be stationary. For example, servers used for internet applications may use nonvolatile memory systems for storage of data that is sent and received over the internet. Such systems may remain powered up without interruption for extended periods (e.g. a year or more) and may be frequently accessed throughout such periods. Individual blocks may be frequently written and erased so that endurance may be a major concern.

[0043] FIGs. 2A-2C show different views of a prior art NAND flash memory. In particular, FIG. 2A shows a plan view of a portion of such a memory array including bit lines and word lines (this is a simplified structure with a small number of word lines and bit lines). FIG. 2B shows a cross section along A-A (along a NAND string) showing individual memory cells that are connected in series. Contact plugs, or vias, are formed at either end to connect the NAND strings in the memory array to conductive lines (e.g. connecting to bit lines at one end and to a common source line at the other end). Such a via may be formed of metal that is deposited into a contact hole that is formed in a dielectric layer. FIG. 2C shows a cross section along B-B of FIG. 2A. This view shows metal contact plugs extending down through contact holes in a dielectric layer to make contact with active areas ("AA") in the substrate (i.e. with N+ areas of FIG. 2B). STI regions are located between active areas of different strings to electrically isolate an individual NAND string from its neighbors. Bit lines extend over the memory array in a direction perpendicular to the plane of the cross section shown. Alternating bit lines are connected to vias in the cross section shown. (It will be understood that other vias, that are not visible in the cross section shown, may connect the remaining bit lines to other active areas)..

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[0044] As memories become smaller, the spacing between conductive lines such as bit lines tends to diminish. Accordingly, capacitive coupling between bit lines tends to increase as technology progresses to ever-smaller dimensions. FIG. 2C shows an example of bit lines formed in a dielectric layer. For example, copper bit lines may be formed by a damascene process in which elongated openings, or trenches, are formed in the dielectric layer and then copper is deposited to fill the trenches. When excess copper is removed (e.g. by Chemical Mechanical Polishing, CMP) copper lines remain. A suitable dielectric may be chosen to keep bit line-to-bit line capacitance low. In some cases air gaps may be formed between bit lines to keep bit line-to-bit line coupling low.

[0045] In order to make small features sidewall assisted patterning (SAP) may be used to enable patterning of features that are smaller than the smallest features that can be patterned by direct patterning using a given photolithographic process. FIGs. 3A-C illustrate how a pattern (e.g. word line pattern, or bit line pattern in a NAND flash memory) may be formed by sidewall assisted processing.

[0046] FIG. 3A shows mandrels (e.g. mandrel 301) with sidewall spacers (e.g. sidewall spacers 303a-b) formed along sides of the mandrels so that the width, X, of a gap between sidewall spacers formed on sides of neighboring mandrels is approximately equal to the width, W, of a mandrel.

[0047] FIG. 3B shows subsequent removal of mandrels. Mandrels may be removed using a selective etch so that sidewall spacers remain substantially unetched by this step. Underlying layer 305 may also be substantially unetched. This etch leaves alternating portions of an upper surface of underlying layer 305 exposed and covered by sidewall spacers. These portions may have approximately the same dimensions.

[0048] FIG. 3C shows subsequent etching of underlying layer 305 using sidewall spacers as an etch mask. It can be seen that trenches (e.g. trenches 307a-b) are formed where underlying layer 305 is exposed. Thus, a set of substantially identical trenches are formed. These trenches may be used to form bit lines, or other conductive lines, by filling the trenches with copper and then removing excess copper in a damascene process. Alternatively, a layer that is patterned in this

way (patterned like layer 305) may be used to pattern underlying layers (i.e. may be used as an etch mask).

[0049] FIGs. 4A-C illustrate an alternative sidewall assisted process for forming trenches. In this example however, trenches are not substantially identical. Instead, trenches are formed so that they alternate between two different types of trench with two different profiles.

[0050] FIG. 4A shows a cross section of a portion of an integrated circuit at an intermediate stage of fabrication after mandrels (e.g. mandrel 411) are formed on the surface of a dielectric layer 413. Overlying the mandrels is a liner layer 415. The mandrels may be formed first by an appropriate process. Then, liner layer 415 may be deposited so that it covers all exposed surfaces including sides of mandrels and areas between mandrels. Then, sidewall spacer layer 417 is deposited over the liner layer. Both liner layer 415 and the dielectric layer 413 may be formed of the same material, which is silicon oxide in this example. In other examples, different materials with similar etch properties may be used. Mandrels may be formed of amorphous silicon. The sidewall spacer layer may be formed of a material that is different to the material (or materials) of the liner layer and underlying dielectric so that it has different etch characteristics allowing selective etching of the liner layer and underlying dielectric without substantial etching of sidewall spacer material. An example of a sidewall spacer layer material is silicon nitride.

[0051] FIG. 4B shows the structure of FIG. 4A after etching through sidewall spacer layer 417 to leave sidewall spacers (e.g. sidewall spacer 417a-c) lying along sides of mandrels. Liner layer 415 is etched through to form separate portions (e.g. liner layer portions 415a-c) lying between the sidewall spacers and mandrel sides (and under sidewall spacers). Liner layer 415 is etched through over mandrels, thereby exposing upper surfaces of mandrels (e.g. mandrel 411) and is etched through between sidewall spacers thereby exposing the upper surface of dielectric layer 413. Etching may be performed in separate steps, first etching sidewall spacer layer 417, then liner layer 415 using different process conditions.

[0052] FIG. 4C shows the structure of FIG. 4B after removal of mandrels. Removal of mandrels may use a selective etch so that sidewall spacers, liner layer portions, and dielectric layer 413 are substantially unaffected by removal of mandrels. This leaves masking portions as shown with

each masking portion including a sidewall spacer and a portion of liner layer (e.g. masking portion 419 includes sidewall spacer 417a and liner layer portion 415a).

[0053] FIG. 4D shows the result of anisotropic etching (e.g. reactive ion etching, RIE) using the pattern of FIG. 4C as an etch mask to etch dielectric layer 413. Etching is not uniform because each mask portion includes a portions of liner layer and a sidewall spacer that are formed of different materials (silicon oxide and silicon nitride respectively in this example) which have different etch characteristics. In particular, the etch used to form trenches is selective to silicon oxide (has a significantly higher etch rate for silicon oxide than for silicon nitride) so that as etching progresses downwards into dielectric layer 413, etching also removes liner layer portions (e.g. liner layer portion 415a) along sides of sidewall spacers. This causes first trenches (T1) between pairs of sidewall spacers that were formed on opposing sides of the same mandrel (e.g. between sidewall spacers 417b-c) to have a profile that is wider at the top than at the bottom. A step is shown that corresponds to the etch breaking through the liner layer portion at an intermediate stage during etching. In contrast to first trenches (T1), second trenches (T2) between sidewall spacers of neighboring mandrels (e.g. between sidewall spacers 417a-b) are substantially uniform. Masking portions have liner layer portions along inner sides but have no such liner layer portions along outer sides so that T2 trenches defined by outer sides of sidewall spacers of neighboring mandrels, remain substantially uniform from top to bottom.

[0054] FIG. 5 illustrates the different profiles of first and second types of trenches formed. A first type of trench, T1, is formed where a mandrel was removed and is defined by inner sides of sidewall spacers (where liner layer portions were located). An upper portion, P1, has a width W1 that is approximately equal to the distance between sidewall spacers that define it and a height H2 that is approximately the height of a liner layer portion. The upper portion may taper somewhat down to a step 525. The lower portion, P2, below the step, has a substantially uniform width, W3, which is significantly narrower than the width of the upper portion ($W3 < W1$). W3 is less than W1 by approximately two times the liner layer thickness ($W1 - W3 = 2 * T_{\text{liner}}$). Thus, first trenches have a T-shaped profile in cross section as shown.

[0055] In contrast, a second type of trench, T2, has a substantially uniform width, W2, from top

to bottom. Trenches alternate between first and second types, T1 and T2, in an odd-even arrangement, i.e. T1 trenches may be considered odd numbered and T2 trenches may be considered even numbered where trenches are numbered sequentially by physical location. It will be understood that the dimensions and spacing of T1 and T2 trenches may be configured by choosing appropriate dimensions for mandrels, liner layer, sidewall spacers, and by choosing appropriate etch conditions.

[0056] Alternating trenches may be used for any suitable purpose, for example, in forming integrated circuits including, but not limited to, NAND flash memories. One example of their use is in a damascene process for forming bit lines. FIG. 6A shows an example where a copper deposition process is used to deposit and remove copper to leave the structure shown. Odd trenches (T1 trenches) are filled with copper in a substantially void-free manner so that conductive lines are formed. A copper seed layer may be deposited first (e.g. by CVD) followed by trench filling (e.g. by electrochemical deposition (ECD)). In contrast, even trenches (T2 trenches) are not filled with copper. Instead, copper seals the top openings of even trenches (T2 trenches) so that air gaps are enclosed by this process. The dimensions of T1 and T2 trenches, and a copper deposition process, may be selected so that T1 trenches, having openings that are W1 wide, are substantially void free, while T2 trenches, having openings that are W2 wide, form voids (or air gaps).

[0057] FIG. 6B illustrates how copper deposition may close off a T2 trench opening and thus form a void, or air gap, in the trench. Deposition of copper may occur at a high rate at the opening of a trench in area 631. For example, CVD and/or electrochemical deposition (ECD) of copper may occur at a high rate where a strong electric field occurs at the edges of trench T2. Such high rate growth causes deposition from either side to reduce deposition rates lower down within trench T2. Copper deposited along edges eventually meets and seals off the trench to form air gap 633 as shown. In contrast, wider openings of T1 trenches are not significantly affected by any increased deposition around openings so that deposition within T1 trenches continues and fills the trenches in a substantially void-free manner. Air gaps enclosed in second trenches may reduce coupling between conductive lines formed in first trenches.

[0058] Various sidewall assisted processes may be used according to different examples. FIG. 7 illustrates a single SAP process (“SAP”) in which two mask portions are defined by two sidewall spacers formed along sides of a mandrel that was patterned directly by photolithography (by a portion of photoresist “Resist”). These mask portions may be used as mandrels (or to define mandrels) on which secondary sidewall spacers are formed (four sidewall spacers, two on each such mandrel) in what may be referred to as a double sidewall assisted process (“DSAP”). Secondary sidewall spacers may define mandrels on which tertiary sidewall spacers are formed (eight sidewall spacers, two on each mandrel) in what may be referred to as a triple sidewall assisted process (“TSAP”). Mandrels of FIG. 4A may be formed by direct patterning, or may be formed by one of the SAP processes illustrated. Thus, even though alternating trenches may be used to form air gaps, conductive line density may be maintained by increasing trench density (e.g. if half of the trenches are used for air gaps as in FIG. 6A then the number of trenches may be doubled by replacing single SAP with DSAP).

[0059] FIG. 8 shows an example where both first and second trenches (T1 and T2) are filled with metal (e.g. copper) in a substantially void-free manner (i.e. no air gaps are formed in either T1 or T2 trenches). Dimensions of first and second trenches, and metal deposition parameters, may be selected to provide good filling in both trench profiles. Thus conductive metal lines are formed in both first and second trenches. The cross sectional areas of the two profiles may be equal so that the resistances of conductive lines formed in the trenches are equal. Alternatively, cross sectional areas may be configured so that they are different and provide different line resistances. It can be seen that the relatively wide (W1) top surfaces of conductive lines formed in first trenches (T1) facilitate alignment of later-formed overlying contact plugs 835. Overlying contact plugs may have large contact areas and wide margins for misalignment (increased overlay margin). Thus, conductive lines formed in T1 trenches may be suitable for connecting overlying structures. In contrast, relatively wide (W4) lower surfaces of conductive lines formed in second trenches (wide compared with W3) may make second trenches more suitable for connecting with underlying contact plugs and thereby connecting underlying structures, for example, underlying contact plug 837 in region R11. Thus, two different sets of conductive lines may be formed in the same metal layer, by the same process steps, with different characteristics. These different characteristics may make each set of conductive lines suitable for a different

purpose so that a single metal layer can form different components that are adapted for different functions.

[0060] While previous examples have shown first and second trenches having the same depth, in other examples, trenches are formed with different depths. Microloading effects generally result in higher etching rates in wider openings than in narrower openings. Thus, by choosing suitable etch conditions and trench dimensions, microloading effects may cause one set of trenches to be deeper or shallower than the other.

[0061] FIG. 9A shows an example in which first trenches (T1) have a depth D1 that is deeper than the depth D2 of second trenches (T2). In this example, first trenches are significantly wider than second trenches so that etching progresses faster in first trenches causing them to become deeper.

[0062] FIG. 9B shows an example in which second trenches (T2) have a depth D4 that is deeper than the depth (D3) of first trenches (T1). Second trenches are wider than the initial width (W3) of first trenches (the width before liner layer portions are etched through) leading to a faster initial etch rate in second trenches. Even though first trenches may subsequently widen, thus reducing microloading effects in first trenches, the result is the shallower first trenches shown.

[0063] FIG. 10 illustrates an example of steps used in a sidewall assisted process to form a pattern of alternating trenches. Mandrels are formed 151 on a dielectric layer. Formation of mandrels may be by direct patterning (single SAP), or from a sidewall formed by a previous sidewall assisted process (e.g. in a DSAP, or TSAP process). A liner layer is deposited 153 over the mandrels so that sidewalls of mandrels are covered by the liner layer. The liner layer may be the same material as an underlying dielectric layer, or may at least have similar etch characteristics. Then sidewall spacers are formed 155 by depositing a sidewall spacer layer and etching back. This also etches back the liner layer thereby exposing upper surfaces of mandrels. Mandrels are then removed 157 (e.g. by selective etching) to leave a pattern of mask portions, each portion including a sidewall spacer and a portion of the liner layer along one side of the sidewall spacer. First and second trenches are then etched 159 using the pattern of mask portions as an etch mask. The etch is selective to the liner layer and underlying dielectric layer so that

etching proceeds down into the liner layer to form trenches and also etches through liner layer portions in alternate gaps. When liner layer portions are etched through, wider gaps are formed by their removal and thus first trenches are formed with a narrower lower portion and a wider upper portion. Subsequently, metal is deposited 161 (e.g. by electroplating). Metal may fill both trenches to form conductive lines (e.g. bit lines of a NAND flash memory), or may fill first trenches and may cap the second trenches to form air gaps in second trenches.

Conclusion

[0064] Although the various aspects have been described with respect to examples, it will be understood that protection within the full scope of the appended claims is appropriate.

IT IS CLAIMED:

1. A NAND flash memory comprising:
 - a semiconductor substrate;
 - a dielectric layer extending over the semiconductor substrate;
 - a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;
 - a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the first and second trenches arranged in an alternating pattern; and
 - a plurality of bit lines located in the first trenches.
2. The NAND flash memory of claim 1 further comprising a plurality of additional bit lines located in the second trenches.
3. The NAND flash memory of claim 2 wherein the plurality of bit lines and the plurality of additional bit lines are formed of copper.
4. The NAND flash memory of claim 1 wherein the first shape has a first width at a level of an upper surface of the dielectric layer, the second shape has a second width at the level of the upper surface of the dielectric layer, and the second width is less than the first width.
5. The NAND flash memory of claim 4 wherein the first shape has a third width at a bottom surface of the first shape, the third width being substantially less than the second width, and the second shape has substantially the second width from top to bottom.

6. The NAND flash memory of claim 1 further comprising a plurality of air gaps located in the second trenches.

7. The NAND flash memory of claim 6 wherein the plurality of first trenches are filled with copper that forms the plurality of bit lines and the plurality of second trenches are capped by copper that seals the plurality of air gaps in the second trenches.

8. The NAND flash memory of claim 1 wherein an individual first trench has a cross sectional area along the plane that is equal to a cross sectional area of an individual second trench along the plane.

9. The NAND flash memory of claim 1 wherein the first shape has an upper portion that extends from a level of an upper surface of the dielectric layer down to an intermediate level with tapering sidewalls, and has a lower portion that extends from the intermediate level to a bottom surface of the first shape, the lower portion having substantially parallel sidewalls.

10. The NAND flash memory of claim 9 wherein the second shape is substantially rectangular.

11. The NAND flash memory of claim 1 wherein the plurality of first trenches have a first depth and the plurality of second trenches have a second depth.

12. A method of forming a NAND flash memory comprising:
forming a plurality of NAND strings disposed on a surface of a substrate;
depositing a dielectric layer over the plurality of NAND strings;
etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;

etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the first and second trenches arranged in an alternating pattern; and

depositing metal in the plurality of first trenches to form a plurality of bit lines located in in the first trenches.

13. The method of claim 12 further comprising, prior to etching the plurality of first trenches and the plurality of second trenches, forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.

14. The method of claim 13 wherein the second material has a higher etch rate than the first material and wherein first trenches are formed at locations corresponding to locations of liner parts of neighboring mask portions.

15. The method of claim 12 further comprising depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches.

16. The method of claim 12 further comprising depositing the metal in the plurality of second trenches to cap air gaps in the plurality of second trenches.

17. A method of forming a NAND flash memory comprising:
forming a plurality of NAND strings disposed on a surface of a substrate;
depositing a dielectric layer over the plurality of NAND strings;
forming a plurality of mandrels on the dielectric layer;
forming a liner layer along side surfaces of the plurality of mandrels;
forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels;

removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material;

subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel;

etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and

depositing copper in the plurality of first trenches to form a plurality of bit lines located in in the first trenches.

18. The method of claim 17 further comprising depositing the copper in the plurality of second trenches to form a plurality of additional bit lines.

19. The method of claim 17 wherein depositing copper comprises electroplating with conditions that provide substantially void-free filling of the plurality of first trenches and provide significant air-gaps in the plurality of second trenches.

20. The method of claim 17 wherein the dielectric layer is formed of silicon oxide, the liner layer is formed of silicon oxide, the sidewall spacers are formed of silicon nitride, and wherein the etching uses anisotropic etching that has a significantly higher etch rate for silicon oxide than for silicon nitride.

ALTERNATING SIDEWALL ASSISTED PATTERNING

ABSTRACT OF THE DISCLOSURE

A dielectric layer extending over a substrate has alternating first and second trenches extending in a first direction. The first trenches have a first shape in cross section along a plane that is perpendicular to the first direction and the second trenches have a second shape in cross section along the plane. Bit lines are located in at least the first trenches.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Alternating Sidewall Assisted Patterning
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT International application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.	
LEGAL NAME OF INVENTOR Inventor: <u>Erika Kanezaki</u> Date (Optional): <u>7/22/2015</u> Signature: <u>Erika Kanezaki</u>	
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**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Alternating Sidewall Assisted Patterning
As the below named inventor, I hereby declare that: This declaration is directed to: ☒ The attached application, or ☐ United States application or PCT international application number _____ filed on _____. The above-identified application was made or authorized to be made by me. I believe that I am the original inventor or an original joint inventor of a claimed invention in the application. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both. WARNING: Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available. LEGAL NAME OF INVENTOR Inventor: <u>Ryo Nakamura</u> Date (Optional): <u>7/22/2015</u> Signature: <u>Ryo Nakamura</u> Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.	

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of
Invention

Alternating Sidewall Assisted Patterning

As the below named inventor, I hereby declare that:

This declaration
is directed to:



The attached application, or



United States application or PCT international application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001
by fine or imprisonment of not more than five (5) years, or both.

WARNING:

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LEGAL NAME OF INVENTOR

Inventor:

Kotaro Shinouchi

Date (Optional):

17/22/2015

Signature:

Kotaro Shinouchi

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form.
Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN
APPLICATION DATA SHEET (37 CFR 1.76)**

Title of Invention	Alternating Sidewall Assisted Patterning
-------------------------------	--

As the below named inventor, I hereby declare that:

This declaration is directed to: ☒ The attached application, or
☐ United States application or PCT International application number _____
filed on _____

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Satoshi Kamata Date (Optional): 7/22/2015
Signature: Satoshi Kamata

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form. Use an additional PTO/SB/AIA01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450, DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Alternating Sidewall Assisted Patterning		
First Named Inventor/Applicant Name:		Erika Kanezaki		
Filer:		Peter Ailbe Gallagher		
Attorney Docket Number:		0084567-986US0		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1600

Electronic Acknowledgement Receipt	
EFS ID:	22987918
Application Number:	14806111
International Application Number:	
Confirmation Number:	1674
Title of Invention:	Alternating Sidewall Assisted Patterning
First Named Inventor/Applicant Name:	Erika Kanezaki
Customer Number:	66785
Filer:	Peter Ailbe Gallagher
Filer Authorized By:	
Attorney Docket Number:	0084567-986US0
Receipt Date:	22-JUL-2015
Filing Date:	
Time Stamp:	16:02:31
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$1600
RAM confirmation Number	2469
Deposit Account	040258
Authorized User	GALLAGHER, PETER A
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:	
Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Drawings-only black and white line drawings	0084567-986US0_Drawings.pdf	1062919	no	8
			4e8a47910809194fb2f47fbc091e08b76c46d60d		
Warnings:					
Information:					
2		0084567-986US0_Application.pdf	1122902	yes	30
			1af609459a6821793f4c257633b9bfd3dbfabb4f		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Application Data Sheet		1	7	
	Specification		8	25	
	Claims		26	29	
	Abstract		30	30	
Warnings:					
Information:					
3	Oath or Declaration filed	0084567-986US0_Decls.pdf	184091	no	4
			02f58dfa02e6635c9e7a6769806c6ff874ce9ad8		
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	34718	no	2
			0d2b934587f126b305e8b56fae4420ecb0b9e865		
Warnings:					
Information:					
Total Files Size (in bytes):			2404630		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

SCORE Placeholder Sheet for IFW Content

Application Number: 14806111

Document Date: 07/22/2015

The presence of this form in the IFW record indicates that the following document type was received in electronic format on the date identified above. This content is stored in the SCORE database.

- Drawings – Other than Black and White Line Drawings

Since this was an electronic submission, there is no physical artifact folder, no artifact folder is recorded in PALM, and no paper documents or physical media exist. The TIFF images in the IFW record were created from the original documents that are stored in SCORE.

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- Examiners may access SCORE content via the eDAN interface.
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14806111
	Filing Date		2015-07-22
	First Named Inventor	Erika Kanazaki	
	Art Unit	2812	
	Examiner Name	Not Yet Assigned	
	Attorney Docket Number	0084567-986US0	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7737015	B2	2010-06-15	Kohli et al.	
	2	7795080	B2	2010-09-14	Orimoto et al.	
	3	7800155	B2	2010-09-21	Matsuno	
	4	7863190	B1	2011-01-04	Papasoulitis	
	5	7884415	B2	2011-02-08	Nagano	
	6	7905959	B2	2011-03-15	Tzu et al.	
	7	8053347	B2	2011-11-08	Kang et al.	
	8	8129264	B2	2012-03-06	Kim et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14806111	
	Filing Date		2015-07-22	
	First Named Inventor	Erika Kanezaki		
	Art Unit	2812		
	Examiner Name	Not Yet Assigned		
	Attorney Docket Number	0084567-986US0		

	9	8362542	B2	2013-01-29	Kang et al.	
	10	8383479	B2	2013-02-26	Purayath	
	11	8492224	B2	2013-07-23	Purayath et al.	
	12	8546239	B2	2013-10-01	Harari et al.	
	13	8603890	B2	2013-12-10	Purayath et al.	

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U.S.PATENT APPLICATION PUBLICATIONS

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20060194390	A1	2006-08-31	Imai et al.	
	2	20070184615	A1	2007-08-09	Brazzelli et al.	
	3	20070257305	A1	2007-11-08	Sasago et al.	
	4	20080003743	A1	2008-01-03	Lee	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14806111	
	Filing Date		2015-07-22	
	First Named Inventor	Erika Kanezaki		
	Art Unit	2812		
	Examiner Name	Not Yet Assigned		
	Attorney Docket Number	0084567-986US0		

	5	20080283898	A1	2008-11-20	Kuniya	
	6	20090212352	A1	2009-08-27	Aoyama et al.	
	7	20090267131	A1	2009-10-29	Nitta	
	8	20100019311	A1	2010-01-28	Sato et al.	
	9	20100127320	A1	2010-05-27	Nishihara et al.	
	10	20100230741	A1	2010-09-16	Choi et al.	
	11	20110057250	A1	2011-03-10	Higashi et al.	
	12	20110303967	A1	2011-12-15	Harari et al.	
	13	20110309430	A1	2011-12-22	Purayath et al.	

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14806111	
	Filing Date		2015-07-22	
	First Named Inventor	Erika Kanezaki		
	Art Unit	2812		
	Examiner Name	Not Yet Assigned		
	Attorney Docket Number	0084567-986US0		

	1							☐
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14806111
	Filing Date		2015-07-22
	First Named Inventor	Erika Kanezaki	
	Art Unit	2812	
	Examiner Name	Not Yet Assigned	
	Attorney Docket Number	0084567-986US0	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print		Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Erika Kanezaki et al.		
Title:	Alternating Sidewall Assisted Patterning		
Application No.:	14/806,111	Filing Date:	July 22, 2015
Examiner:	Not Yet Assigned	Group Art Unit:	
Docket No.:	0084567-986US0	Conf. No.:	1674

Mail Stop
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Dear Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) call(s) the documents listed on the enclosed Form PTO-SB08 to the Examiner's attention in this patent application.

According to 37 C.F.R. 1.98(a)(2)(ii), copies of the U.S. Patents and U.S. Published Patent Applications documents are not required and are therefore not enclosed.

Citation of these documents shall not be construed as (1) an admission that the documents are prior art with respect to the invention or inventions claimed in this application, (2) a representation that a search has been made (other than as indicated by any cited document), or (3) an admission that the cited information is, or is considered to be, material to patentability as defined in § 1.56(b).

This information disclosure statement is submitted under 37 C.F.R. § 1.97(b) and consequently no fee should be required. The Commissioner is authorized, however, to charge

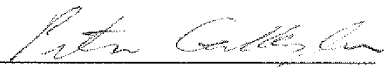
Attorney Docket No.: 0084567-986US0
FILED VIA EFS

Application No.: 14/806,111

any fee that may be required, or to credit any overpayment, against Deposit Account No. 04-0258.

FILED VIA EFS

Respectfully submitted,

 7/23/15
Peter A. Gallagher Date
Reg. No. 47584

DAVIS WRIGHT TREMAINE LLP
505 Montgomery Street, Suite 800
San Francisco, California 94111-6533
Telephone: (415) 276-6500
Facsimile: (415) 276-6599
Email: PeterGallagher@dwt.com

Electronic Acknowledgement Receipt	
EFS ID:	23013658
Application Number:	14806111
International Application Number:	
Confirmation Number:	1674
Title of Invention:	Alternating Sidewall Assisted Patterning
First Named Inventor/Applicant Name:	Erika Kanezaki
Customer Number:	66785
Filer:	Peter Ailbe Gallagher/Sara Eaton
Filer Authorized By:	Peter Ailbe Gallagher
Attorney Docket Number:	0084567-986US0
Receipt Date:	24-JUL-2015
Filing Date:	
Time Stamp:	11:36:26
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	20150724_IDS-SB08_986US0.pdf	613118 ea925d395b1eb41715be4858548653eba247fe24	no	6

Warnings:

Information:

2	Transmittal Letter	20150724_IDS- Transmittal_986US0.pdf	40965 113a945dcf58732f0b469c7c7ab13cd7c78d17ea	no	2
Warnings:					
Information:					
Total Files Size (in bytes):				654083	
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/806,111	07/22/2015	2812	1600	0084567-986US0	20	3

CONFIRMATION NO. 1674

FILING RECEIPT



66785
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

Date Mailed: 08/07/2015

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Erika Kanezaki, Yokkaichi, JAPAN;
Ryo Nakamura, Yokkaichi, JAPAN;
Kotaro Jinnouchi, Yokkaichi, JAPAN;
Satoshi Kamata, Yokkaichi, JAPAN;

Applicant(s)

SanDisk Technologies, Inc., Plano, TX;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 08/05/2015

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/806,111**

Projected Publication Date: 01/26/2017

Non-Publication Request: No

Early Publication Request: No
Title

Alternating Sidewall Assisted Patterning

Preliminary Class

438

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/806,111				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	280			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	600			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	720			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 80 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *			OR	x 420 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL		TOTAL	1600			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
TOTAL ADD'L FEE								OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanazaki	0084567-986US0	1674
66785 7590 05/26/2016 DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION IP Docketing Dept. Davis Wright Tremaine LLP 1201 Third Avenue, Suite 2200 Seattle, WA 98101			EXAMINER THAI, LUAN C	
			ART UNIT 2891	PAPER NUMBER
			NOTIFICATION DATE 05/26/2016	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@dwt.com

Office Action Summary	Application No. 14/806,111	Applicant(s) KANEZAKI ET AL.	
	Examiner LUAN C. THAI	Art Unit 2891	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-20 is/are rejected.
- 8) ☐ Claim(s) _____ is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 07/22/15 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 3) ☐ Interview Summary (PTO-413) |
| 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) | Paper No(s)/Mail Date. _____ |
| Paper No(s)/Mail Date _____ | 4) ☐ Other: _____ |

DETAILED ACTION

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

Information Disclosure Statement

1. The Information disclosure Statement filed on 07/24/15 has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale or otherwise available to the public before the effective filing date of the claimed invention.

(a)(2) the claimed invention was described in a patent issued under section 151, or in an application for patent published or deemed published under section 122(b), in which the patent or application, as the case may be, names another inventor and was effectively filed before the effective filing date of the claimed invention.

3. Claims 1-2, 4-5, 8-12, and 15, are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Min et al. (8,247,291).

Regarding claims 1-2, 11-12, and 15, Min et al. (See specifically Figs. 1A-1H and the associated description) discloses a method of forming a NAND flash memory (Col. 2, lines 60+, Col. 3, lines 3+) comprising: forming a plurality of NAND strings (See Fig. 3) disposed on a surface of a substrate (10); depositing a dielectric layer (20) over the plurality of NAND strings

(See Figs. 1A-1B); etching a plurality of first trenches (25) having a first depth in the dielectric layer (20/22a), each first trench (25) being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction (See Figs. 1F-1G); etching a plurality of second trenches (26) having a second depth in the dielectric layer (20/22a), each second trench (26) being elongated along the first direction and having a second shape in cross section along the plane, the first and second trenches arranged in an alternating pattern (See Figs. 1F-1G); and depositing metal (81a/82a) in the plurality of first trenches and second trenches (25/26) to form a plurality of bit lines located in the first trenches and second trenches (25/26) (See Fig. 1H). Min et al. further discloses prior to etching the plurality of first trenches (25) and the plurality of second trenches (26), forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.

Regarding claims 4-5, Min et al. further discloses the first shape of the first trenches (25) having a first width at a level of an upper surface of the dielectric layer (22a), the second shape of the second trenches having a second width at the level of the upper surface of the dielectric layer (22a), wherein the second width is less than the first width (See Fig 1G). Min et al. also discloses the first shape having a third width at a bottom surface of the first shape, the third width being substantially less than the second width, and the second shape has substantially the second width from top to bottom (See Fig. 1G).

Regarding claims 8-10, Min et al. further discloses the first shape having an upper portion that extends from a level of an upper surface of the dielectric layer (3B) down to an intermediate level (2B) with tapering sidewalls, and has a lower portion that extends from the intermediate

level (2B) to a bottom surface of the first shape, the lower portion having substantially parallel sidewalls, and wherein the second shape is substantially rectangular (See Fig. 1G).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102 of this title, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims the examiner presumes that the subject matter of the various claims was commonly owned as of the effective filing date of the claimed invention(s) absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and effective filing dates of each claim that was not commonly owned as of the effective filing date of the later invention in order for the examiner to consider the applicability of 35 U.S.C. 102(b)(2)(C) for any potential 35 U.S.C. 102(a)(2) prior art against the later invention.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

- a. Determining the scope and contents of the prior art.
 - b. Ascertaining the differences between the prior art and the claims at issue.
 - c. Resolving the level of ordinary skill in the pertinent art.
 - d. Considering objective evidence present in the application indicating obviousness or nonobviousness.
5. Claim 3 is rejected under 35 U.S.C. 103 as being unpatentable over Min et al. (8,247,291).

Regarding claim 3, Min et al. discloses all the limitations of the claimed invention except for specifying the bit lines being formed of copper.

However, copper is a known material that is routinely used in the art to form bit lines.

Therefore, forming the bit lines of copper would have been obvious modification.

6. Claims 13-14, 17-18, and 20, are rejected under 35 U.S.C. 103 as being unpatentable over Min et al. (8,247,291) in view of Juengling (7,442,976).

Regarding claims 13-14, 17-18, and 20, the proposed method of Min et al. further discloses prior to etching the plurality of first and second trenches, forming an etch mask that includes a plurality of mask portions or mandrels (41a/42a) on the dielectric layer (20); forming sidewall spacers (71/72) alongside surfaces of the plurality of mandrels (41a/42a) (See Figs. 1C-1D); removing the plurality of mandrels (41a/42a) to leave a pattern of sidewall spacers (Fig. 1E); subsequently etching a plurality of first trenches in the dielectric layer (20), an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel (41a) (Figs. 1F-1G); etching a plurality of second trenches in the dielectric layer (20), an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels (See Figs. 1F-1G); and depositing copper in the plurality of first and second trenches to form a plurality of bit lines located in in the first and second trenches (See Fig. 1H). The proposed method of Min et al., thus, disclosed all the limitations of the claimed invention except for a liner layer formed alongside surface of the plurality of mandrels before the forming the sidewall spacers thereon.

Juengling, while related to a similar method of forming a NAND flash memory, teaches (See specifically Figs. 17-20 and the associated descriptions) a liner layer (1902) being formed

alongside surface of the plurality of mandrels (1802) before the forming the sidewall spacers (200) on the liner layer (1902) (See Figs. 19-20).

Although Min et al. lacks an inclusion of the use of a liner layer, selecting a specific type of known available liner layer, in semiconductor art, as disclosed by Juengling, for providing a desired sidewall spacers would have been obvious to one of ordinary skill in the art. It would have been obvious to modify Min et al. by applying the liner layer, as disclosed by Juengling, in order to provide a suitable sidewall spacers for the intended NAND flash memory. The further citation in claim 20, regarding the dielectric layer being formed of silicon oxide, the liner layer being formed of silicon oxide, the sidewall spacers being formed of silicon nitride, and the etching being used of anisotropic etching process, would have also been obvious for similar reasons (e.g., known available materials and process) set forth above.

7. Claims 6-7 and 16 are rejected under 35 U.S.C. 103 as being unpatentable over Min et al. (8,247,291) in view of Purayath et al. (8,946,048).

Regarding claims 6-7 and 16, the proposed method of Min et al. disclosed all the limitations of the claimed invention as described above except for a plurality of air gaps located in the second trenches.

Purayath et al., while related to a similar method of forming a NAND flash memory, teaches (See specifically Figs. 7O, 8A-8L, and the associated descriptions) air gaps being introduced in the bit lines to form isolation between closely spaced components in the memory structure, in order to decrease parasitic interferences between neighboring floating gates, neighboring control gates (Col. 5, lines 62+).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Min et al. by forming the air gaps, as being taught by Purayath et al., in the second trenches of Min et al. structure. The purpose of doing so would help to decrease parasitic interferences between neighboring floating gates, neighboring control gates, and the person skilled in the art would regard it as a simple modification without any inventive skills.

8. Claim 19 is rejected under 35 U.S.C. 103 as being unpatentable over Min et al. (8,247,291) and Juengling (7,442,976), as applied to claim 17, and further in view of Purayath et al. (8,946,048).

Regarding claim 19, the proposed method of Min et al. and Juengling disclosed all the limitations of the claimed invention as described above except for a plurality of air gaps located in the second trenches.

Purayath et al., while related to a similar method of forming a NAND flash memory, teaches (See specifically Figs. 7O, 8A-8L, and the associated descriptions) air gaps being introduced in the bit lines to form isolation between closely spaced components in the memory structure, in order to decrease parasitic interferences between neighboring floating gates, neighboring control gates (Col. 5, lines 62+).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the proposed method of Min et al. and Juengling by forming the air gaps, as being taught by Purayath et al., in the second trenches of the proposed method of Min et al. and Purayath et al. structure. The purpose of doing so would help to decrease parasitic interferences between neighboring floating gates, neighboring control gates, and the person skilled in the art would regard it as a simple modification without any inventive skills.

Conclusion

9. The rejections above rely on the references for all the teachings expressed in the text of the references and/or one of ordinary skill in the art would have reasonably understood from the texts. Only specific portions of the texts have been pointed out to emphasize certain aspects of the prior art, however, each reference as a whole should be reviewed in responding to the rejection, since other sections of the same reference and/or various combinations of the cited references may be relied on in future rejections in view of amendments.

10. Applicant is reminded to specifically point out the support for any amendments made to the disclosure. See 37 C.F.R. 1.121; 37 C.F.R. Part 41.37; and MPEP 714.02.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Landau can be reached on 571-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

Application/Control Number: 14/806,111

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Art Unit: 2891

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/Luan C. Thai/

Primary Examiner

Art Unit 2891

May 23, 2016

Notice of References Cited	Application/Control No. 14/806,111	Applicant(s)/Patent Under Reexamination KANEZAKI ET AL.	
	Examiner LUAN C. THAI	Art Unit 2891	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8,247,291 B2	08-2012	Min; Jae-Ho	H01L21/0337	257/E21.538
*	B	US-7,442,976 B2	10-2008	Juengling; Werner	H01L27/10823	257/296
*	C	US-8,946,048 B2	02-2015	Purayath; Vinod Robert	H01L21/28273	257/319
*	D	US-7,842,558 B2	11-2010	Juengling; Werner	H01L21/0337	257/216
	E	US-				
	F	US-				
	G	US-				
	H	US-				
	I	US-				
	J	US-				
	K	US-				
	L	US-				
	M	US-				

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	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 14806111	Applicant(s)/Patent Under Reexamination KANEZAKI ET AL.
	Examiner LUAN C THAI	Art Unit 2891

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
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EAST Search History

EAST Search History (Prior Art)

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5/ 23/ 2016 11:57:29 AM

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	Examiner LUAN C THAI	Art Unit 2891

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	05/23/16	LT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

	/LUAN C THAI/ Primary Examiner.Art Unit 2891
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EAST Search History

EAST Search History (Prior Art)

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EAST Search History

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5/ 23/ 2016 7:12:57 AM

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Receipt date: 07/24/2015

14806111 -- GAU: 2891

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0851-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14806111
	Filing Date	2015-07-22
	First Named Inventor	Erika Kanazaki
	Art Unit	2812
	Examiner Name	Not Yet Assigned
	Attorney Docket Number	0084567-986US0

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	7737015	B2	2010-06-15	Kohli et al.	
	2	7795080	B2	2010-09-14	Orimoto et al.	
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Receipt date: 07/24/2015

14806111 - GAU: 2891

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14806111
Filing Date	2015-07-22
First Named Inventor	Erika Kanezaki
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	0084567-986US0

9	8362542	B2	2013-01-29	Kang et al.	
10	8383479	B2	2013-02-26	Purayath	
11	8492224	B2	2013-07-23	Purayath et al.	
12	8546239	B2	2013-10-01	Harari et al.	
13	8603890	B2	2013-12-10	Purayath et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20060194390	A1	2006-08-31	Imai et al.	
	2	20070184615	A1	2007-08-09	Brazzelli et al.	
	3	20070257305	A1	2007-11-08	Sasago et al.	
	4	20080003743	A1	2008-01-03	Lee	

Receipt date: 07/24/2015

14806111 - GAU: 2891

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14806111
Filing Date	2015-07-22
First Named Inventor	Erika Kanezaki
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	0084567-986US0

5	20080283898	A1	2008-11-20	Kuniya	
6	20090212352	A1	2009-08-27	Aoyama et al.	
7	20090267131	A1	2009-10-29	Nitta	
8	20100019311	A1	2010-01-28	Sato et al.	
9	20100127320	A1	2010-05-27	Nishihara et al.	
10	20100230741	A1	2010-09-16	Choi et al.	
11	20110057250	A1	2011-03-10	Higashi et al.	
12	20110303967	A1	2011-12-15	Harari et al.	
13	20110309430	A1	2011-12-22	Purayath et al.	

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Receipt date: 07/24/2015

14806111 - GAU: 2891

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14806111
Filing Date	2015-07-22
First Named Inventor	Erika Kanezaki
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	0084567-986US0

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EXAMINER SIGNATURE

Examiner Signature	/LUAN C THAI/	Date Considered	05/20/2016
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

Receipt date: 07/24/2015

14806111 - GAU: 2891

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14806111
Filing Date	2015-07-22
First Named Inventor	Erika Kanazaki
Art Unit	2812
Examiner Name	Not Yet Assigned
Attorney Docket Number	0084567-986US0

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature		Date (YYYY-MM-DD)	
Name/Print		Registration Number	

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Kanezaki		
Title:	Alternating Sidewall Assisted Patterning		
Application No.:	14/806,111	Filing Date:	July 22, 2015
Examiner:	Luan C. Thai	Group Art Unit:	2891
Docket No.:	0084567-986US0	Conf. No.:	1674

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO OFFICE ACTION AND AMENDMENT

Sir:

This is in response to the non-final Office Action dated May 26, 2016, setting a shortened statutory period for response to expire August 26, 2016.

Claim Amendments are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks begin on page 7 of this paper.

Reconsideration is kindly requested in light of the following remarks or amendments.

Attorney Docket No.: 0084567-986US0

Application No.: 14/806,111

- 1 -

DWT 29909487v1 0084567-986US0

CLAIM AMENDMENTS

Please amend the claims by amending claims 1, 2, 3, 11, and 12, all without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1. (Currently amended) A NAND flash memory comprising:
a semiconductor substrate;
a dielectric layer extending over the semiconductor substrate;
a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;
a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the second shape being different from the first shape, the first and second trenches arranged in an alternating pattern that alternates from first trench to second trench along a second direction that is perpendicular to the first direction; and
a plurality of bit lines located in the first trenches.

2. (Currently amended) The NAND flash memory of claim 1 further comprising a plurality of additional bit lines located in the second trenches, each of the plurality of bit lines having the first shape in cross section along the plane and each of the plurality of additional bit lines having the second shape in cross section along the plane.

3. (Currently amended) The NAND flash memory of claim 2 wherein the plurality of bit lines and the plurality of additional bit lines are formed of copper and wherein the cross sectional area of copper of an individual bit line of the plurality of bit lines is substantially equal to the cross sectional area of copper of an individual bit line of the plurality of additional bit lines.

4. (Original) The NAND flash memory of claim 1 wherein the first shape has a first width at a level of an upper surface of the dielectric layer, the second shape has a second width at the level of the upper surface of the dielectric layer, and the second width is less than the first width.

5. (Original) The NAND flash memory of claim 4 wherein the first shape has a third width at a bottom surface of the first shape, the third width being substantially less than the second width, and the second shape has substantially the second width from top to bottom.

6. (Original) The NAND flash memory of claim 1 further comprising a plurality of air gaps located in the second trenches.

7. (Original) The NAND flash memory of claim 6 wherein the plurality of first trenches are filled with copper that forms the plurality of bit lines and the plurality of second trenches are capped by copper that seals the plurality of air gaps in the second trenches.

8. (Original) The NAND flash memory of claim 1 wherein an individual first trench has a cross sectional area along the plane that is equal to a cross sectional area of an individual second trench along the plane.

9. (Original) The NAND flash memory of claim 1 wherein the first shape has an upper portion that extends from a level of an upper surface of the dielectric layer down to an intermediate level with tapering sidewalls, and has a lower portion that extends from the intermediate level to a bottom surface of the first shape, the lower portion having substantially parallel sidewalls.

10. (Original) The NAND flash memory of claim 9 wherein the second shape is substantially rectangular.

11. (Currently amended) The NAND flash memory of claim 1 wherein the plurality of first trenches have a first depth and the plurality of second trenches have a second depth that is different to the first depth.

12. (Currently amended) A method of forming a NAND flash memory comprising:

forming a plurality of NAND strings disposed on a surface of a substrate;

depositing a dielectric layer over the plurality of NAND strings;

etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;

etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the second shape being different to the first shape, the first and second trenches arranged in an odd-even alternating pattern along a direction that is perpendicular to the first direction such that two first trenches are separated by a second trench; and

depositing metal in the plurality of first trenches to form a plurality of bit lines located in in the first trenches.

13. (Original) The method of claim 12 further comprising, prior to etching the plurality of first trenches and the plurality of second trenches, forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.

14. (Original) The method of claim 13 wherein the second material has a higher etch rate than the first material and wherein first trenches are formed at locations corresponding to locations of liner parts of neighboring mask portions.

15. (Original) The method of claim 12 further comprising depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches.

16. (Original) The method of claim 12 further comprising depositing the metal in the plurality of second trenches to cap air gaps in the plurality of second trenches.

17. (Original) A method of forming a NAND flash memory comprising:
 forming a plurality of NAND strings disposed on a surface of a substrate;
 depositing a dielectric layer over the plurality of NAND strings;
 forming a plurality of mandrels on the dielectric layer;
 forming a liner layer along side surfaces of the plurality of mandrels;
 forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels;
 removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material;
 subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel;
 etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and
 depositing copper in the plurality of first trenches to form a plurality of bit lines located in in the first trenches.

18. (Original) The method of claim 17 further comprising depositing the copper in the plurality of second trenches to form a plurality of additional bit lines.

19. (Original) The method of claim 17 wherein depositing copper comprises electroplating with conditions that provide substantially void-free filling of the plurality of first trenches and provide significant air-gaps in the plurality of second trenches.

20. (Original) The method of claim 17 wherein the dielectric layer is formed of silicon oxide, the liner layer is formed of silicon oxide, the sidewall spacers are formed of silicon nitride, and wherein the etching uses anisotropic etching that has a significantly higher etch rate for silicon oxide than for silicon nitride.

REMARKS

Claims 1-20 are pending. Reconsideration of all rejected claims is requested.

Claim Rejections Under 35 U.S.C. §102

Claims 1-2, 4-5, 8-12, and 15 were rejected under 35 U.S.C. §102(a)(1) as being anticipated by U.S. Patent No. 8,247,291 to Min et al. ("Min").

Claim 1, as amended for clarification, recites:

"a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the second shape being different from the first shape, the first and second trenches arranged in an alternating pattern that alternates from first trench to second trench along a second direction that is perpendicular to the first direction"

Support for this amendment may be found throughout the specification, for example, in Fig. 9A (reproduced here), which shows an alternating pattern that alternates from trench T1 to differently shaped trench T2 along the cross section shown.

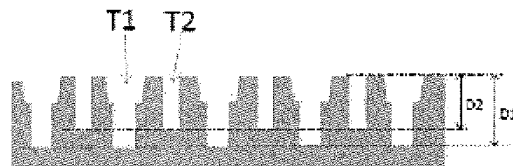
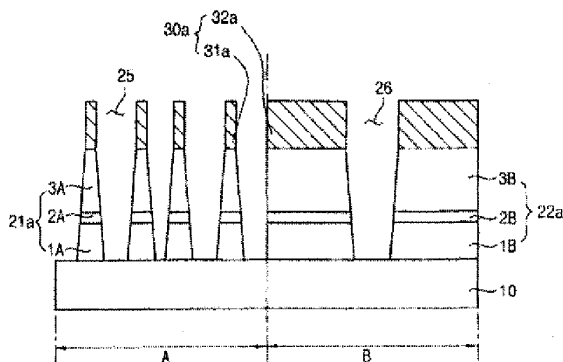


FIG. 9A

The Office Action ("OA") cited trenches 25 and 26 of Min (Fig. 1G, reproduced below) as corresponding to first and second trenches of claim 1. However, trenches 25 and 26 appear to have the same shape and are not in an alternating pattern as recited in claim 1.

In particular, Fig. 1G does not show a pattern that alternates between trenches 25 and 26 along the cross section shown. Trenches 25 are located in area A (to the left) while trench 26 is located in area B (to the right). Because Min does not teach or suggest such an alternating arrangement, the rejection should be withdrawn.



Claims 2-11 are submitted to be allowable at least for depending from claim 1 and further for reciting additional features that are not disclosed by the cited references. For example, claim 2, as amended for clarification recites:

“a plurality of additional bit lines located in the second trenches, each of the plurality of bit lines having the first shape in cross section along the plane and each of the plurality of additional bit lines having the second shape in cross section along the plane”

In contrast, no such bit lines appear to be formed in trenches 26 of Min, which are disclosed as containing a peripheral wiring circuit: “[A] second conductive pattern 82a in the second trench 26 at the second area B, which may be referred to as second wiring structure, may include a peripheral wiring circuit arranged in the peripheral/core area of the flash memory device...” col. 12, lines 51-55. All elements formed in trenches 25 appear to be uniformly shaped.

Claim 8 recites:

“an individual first trench has a cross sectional area along the plane that is equal to a cross sectional area of an individual second trench along the plane.”

In contrast, trenches 25 and 26 appear to have different cross sectional areas because they are used to produce wiring with different sizes. “[T]he mask pattern 60a on the dummy mask layer 50 may have different line widths in the first area A and the second area B according to line widths of the wiring structures in the respective first and second areas A and B.” Col. 7, lines 29-32. “The present embodiment exemplarily discloses the cell and the peripheral/core areas as the first and second areas, respectively, in which two kinds of the wiring structures having different pattern sizes are positioned at each areas and contrasted with each other.” Col. 12, lines 9-13.

Claim 12 is amended for clarification similarly to claim 1. Claim 12 recites:

“etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, the second shape being different to the first shape, the first and second trenches arranged in an odd-even alternating pattern along a direction that is perpendicular to the first direction such that two first trenches are separated by a second trench”

Support for this amendment may be found throughout the specification, for example, in Fig. 9A (above) and paragraph 0055. No such odd-even alternating pattern is disclosed by Min.

Therefore, claim 12 is submitted to be allowable.

Claims 13-16 are submitted to be allowable at least for depending from claim 12 and further for reciting additional features that are not disclosed by the cited references.

Claim Rejections Under 35 U.S.C. §103

Claim 3 was rejected under 35 U.S.C. §103 as being unpatentable over Min. Claim 3 is amended to recite:

“wherein the cross sectional area of copper of an individual bit line of the plurality of bit lines is substantially equal to the cross sectional area of copper of an individual bit line of the plurality of additional bit lines”

Support for this amendment may be found throughout the specification, for example, in Fig. 8 and paragraph 0059. Even if Min was modified to fill trenches 25 and 26 with copper as the OA indicates, the resulting lines would not have substantially equal cross sectional area because trenches 25 and 26 are used to form lines of different line widths. “[T]he mask pattern 60a on the dummy mask layer 50 may have different line widths in the first area A and the second area B according to line widths of the wiring structures in the respective first and second areas A and B.” Col. 7, lines 29-32.

Claims 13-14, 17-18, and 20 were rejected under 35 U.S.C. §103 as being unpatentable over Min in view of U.S. Patent No. 7,442,976 to Juengling.

Claim 17 recites:

“forming a liner layer along side surfaces of the plurality of mandrels;

forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels;

removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material”

The OA acknowledged that Min failed to disclose forming a liner layer along side surfaces of a plurality of mandrels. The OA cited layer 1902 formed on pillar 1802 of Juengling. However, Juengling is directed to processes for forming “DRAM cells with vertical transistors” (title). Layer 1902 is a gate oxide of such a device (“the gate oxide 1902” col. 12, ln 67) and pillar 1802 is not a mandrel that is removed, but remains to form part of the vertical transistor

(“[E]ach pillar 1802 of the pair of pillars 1802 forms a source or a drain region of the transistor” col. 14, lns 57-58). Thus, Juengling does not teach or suggest modifying the process of Min to include portions of liner layer material in spacers 71/72 as the OA indicates because Juengling’s teaching is unrelated to such spacers.

The cited rationale for modifying Min “in order to provide a suitable sidewall spacers for the intended NAND flash memory” (OA, page 6) is not understood. Min does not indicate that spacers 71/72 are unsuitable for their purpose as etching masks (“using first spacer 71 as an etching mask... using the second spacer 72 as an etching mask” col. 11, lns. 18-22). Because Juengling’s cited teaching is directed to formation of gate oxide on a silicon pillar to form a vertical transistor, this teaching does not provide a rationale for modifying etch masking spacers 71/72. Should the rejection be maintained, it is requested that some explanation be provided as to why one of ordinary skill would modify spacers 71/72 and how this would make spacers 71/72 more suitable for their purpose.

Claims 18-20 are submitted to be allowable at least for depending from claim 17 and further for reciting additional features that are not disclosed by the cited references.

Claims 6-7 and 16 were rejected under 35 U.S.C. §103 as being unpatentable over Min in view of U.S. Patent No. 8,946,048 to Purayath et al. (“Purayath”). The OA acknowledged that Min fails to disclose a plurality of air gaps located in the second trenches and indicated that it would be obvious to modify Min to include such air gaps based on Purayath’s teaching of “air gaps being introduced in the bit lines...” (OA, page 6, lines 18-19, emphasis added). However, the cited portion of Purayath does not disclose air gaps in bit lines, but instead teaches: “air gaps are introduced in the column (bit line) and/or row (word line) direction to form isolation...” (col. 5, lns. 62-64, emphasis added). Thus, this disclosure appears to refer to air gap orientation, not location.

Furthermore, it is submitted that would not be obvious to modify Min as the OA indicates. It is submitted that air gaps in trenches 26 of Min would make Min unsatisfactory for its intended purpose (see MPEP 2143.01V) because such air gaps would replace peripheral circuit wiring that Min forms in trenches 26, which applies “driving signals to peripheral circuits for driving transistors in the cell areas of the flash memory device,” col. 12, lines 54-57. Furthermore, it is not seen how air gaps in trenches 26 of Min would “decrease parasitic

interferences between neighboring floating gates, neighboring control gates” as the OA indicates because they are located in area B, which appears to be a peripheral area that does not include floating gates or control gates. Thus, there appears to be no rationale for the proposed modification.

Claim 7 recites:

“the plurality of second trenches are capped by copper that seals the plurality of air gaps in the second trenches”

No such capping of trenches by copper that seals air gaps was identified in either Min or Purayath. See also claims 16 and 19.

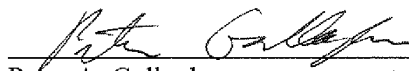
Claim 19 was rejected under 35 U.S.C. §103 as being unpatentable over Min, Juengling, and further in view of Purayath. However, this rejection, like the rejection of claims 6 above appears to be based on a misunderstanding of Purayath, lacks a rationale for the proposed modification, and would render Min unsatisfactory for its intended purpose (see MPEP 2143.01V).

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters that need to be resolved, a telephone call to the undersigned at 415-276-4812 would be appreciated.

FILED VIA EFS

Respectfully submitted,



Peter A. Gallagher
Reg. No. 47,584

8/22/16
Date

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Electronic Acknowledgement Receipt	
EFS ID:	26710809
Application Number:	14806111
International Application Number:	
Confirmation Number:	1674
Title of Invention:	Alternating Sidewall Assisted Patterning
First Named Inventor/Applicant Name:	Erika Kanezaki
Customer Number:	66785
Filer:	Peter Ailbe Gallagher/Eileen Bowen (PAG)
Filer Authorized By:	Peter Ailbe Gallagher
Attorney Docket Number:	0084567-986US0
Receipt Date:	22-AUG-2016
Filing Date:	22-JUL-2015
Time Stamp:	16:19:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		0084567-986US0_Response.pdf	358177	yes	11
			e04e76ba06e20e553cb9436bc08e72e492bb1abb		

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(Column 1)		(Column 2)							
FOR		NUMBER FILED	NUMBER EXTRA			RATE (\$)		FEE (\$)	
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A			N/A			
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A			N/A			
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A			N/A			
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 =	*			X \$ =			
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 =	*			X \$ =			
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL			
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	08/22/2016	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$420 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE						0			
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
TOTAL ADD'L FEE									
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

66785 7590 09/29/2016
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

EXAMINER

THAI, LUAN C

ART UNIT

PAPER NUMBER

2891

DATE MAILED: 09/29/2016

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanazaki	0084567-986US0	1674

TITLE OF INVENTION: Alternating Sidewall Assisted Patterning

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/29/2016

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

66785 7590 09/29/2016

DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanezaki	0084567-986USO	1674

TITLE OF INVENTION: Alternating Sidewall Assisted Patterning

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/29/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
THAI, LUAN C	2891	257-296000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanezaki	0084567-986US0	1674

EXAMINER
THAI, LUAN C

ART UNIT	PAPER NUMBER
2891	

66785 7590 09/29/2016
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

DATE MAILED: 09/29/2016

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/806,111	Applicant(s) KANEZAKI ET AL.	
	Examiner LUAN C. THAI	Art Unit 2891	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the amendment filed on 08/22/16.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|--|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☐ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☒ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

/LUAN C. THAI/
Primary Examiner, Art Unit 2891

DETAILED ACTION

This Office action is responsive to the amendment filed on 08/22/16.

1. Claims 1-20 are allowed.
2. The following is an examiner's statement of reasons for allowance: regarding independent claims 1, 12, and 17, the primary reason for the allowance of the claims is based on the arguments presented by the applicant at pages 7-11 of the Remarks of the amendment filed on 08/22/16.

Since claims 2-11, 13-15 and 18-20, depend either on claims 1, 12, or 17, they are also allowed.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 8:00 AM - 4:30 PM, Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew C. Landau can be reached on 571-272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

Art Unit: 2891

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/LUAN C. THAI/

Primary Examiner

Art Unit 2891

September 5, 2016

Search Notes 	Application/Control No. 14806111	Applicant(s)/Patent Under Reexamination KANEZAKI ET AL.
	Examiner LUAN C THAI	Art Unit 2891

CPC- SEARCHED		
Symbol	Date	Examiner
H01L27/11524,21/76816,21/76863,21/76877,27/0207	09/05/16	LT

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
257	296	09/05/16	LT
438	386	09/05/16	LT

SEARCH NOTES		
Search Notes	Date	Examiner
EAST search attached	05/23/16	LT
EAST search updated	09/05/16	LT

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
257	296	09/05/16	LT
438	386	09/05/16	LT
H01L	27/11524,21/76816,21/76863,21/76877,27/0207	09/05/16	LT

	/ LUAN C THAI/ Primary Examiner.Art Unit 2891
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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office
 Address: COMMISSIONER FOR PATENTS
 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1674

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/806,111	07/22/2015	257	2891	0084567-986US0		
APPLICANTS SanDisk Technologies, Inc., Plano, TX; INVENTORS Erika Kanazaki, Yokkaichi, JAPAN; Ryo Nakamura, Yokkaichi, JAPAN; Kotaro Jinnouchi, Yokkaichi, JAPAN; Satoshi Kamata, Yokkaichi, JAPAN; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 08/05/2015						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/LUAN C THAI/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY JAPAN	SHEETS DRAWINGS 8	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION IP Docketing Dept. Davis Wright Tremaine LLP 1201 Third Avenue, Suite 2200 Seattle, WA 98101 UNITED STATES						
TITLE Alternating Sidewall Assisted Patterning						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	((nand near1 flash near1 memory) with (substrate carrier) with (dielectric insulat\$3) with ((bit near line) with ((first second) with trench\$2)) with (((first second) near direction) with perpendicular)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:17
L2	0	((nand near1 flash near1 memory) same (substrate carrier) same (dielectric insulat\$3) same ((bit near line) with ((first second) with trench\$2)) same (((first second) near direction) with perpendicular)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:18
L3	0	((nand near1 flash near1 memory) and (substrate carrier) same (dielectric insulat\$3) and ((bit near line) with ((first second) with trench\$2)) and (((first second) near direction) with perpendicular)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:18
L4	0	((nand near1 flash near1 memory) with ((nand near string) with (substrate carrier)) with (dielectric insulat\$3) with ((bit near line) with ((first second) near1 trench\$2)) with ((sidewall near1 spacer) with liner with mandrel)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:24
L5	0	((nand near1 flash near1 memory) same ((nand near string) with (substrate carrier)) same (dielectric insulat\$3) same ((bit near line) with ((first second) near1 trench\$2)) same ((sidewall near1 spacer) with liner with mandrel)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:25
L6	0	((nand near1 flash near1 memory) and ((nand near string) with (substrate carrier)) and (dielectric insulat\$3) and ((bit near line) with ((first second) near1 trench\$2)) and ((sidewall near1 spacer) with liner with mandrel)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:25
L7	0	(nand and (flash near1 memory) and ((nand near string) with (substrate carrier)) and (dielectric insulat\$3) and ((bit near line) with ((first second) near1 trench\$2)) and ((sidewall near1 spacer) with liner with mandrel)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:26
L8	0	((flash near1 memory) and ((nand near	US-PGPUB;	OR	ON	2016/09/05

		string) with (substrate carrier)) and (dielectric insulat\$3) and ((bit near line) with ((first second) near1 trench\$2)) and ((sidewall near1 spacer) with liner with mandrel)).clm.	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			14:26
L9	0	(flash near1 memory) and ((nand near string) with (substrate carrier)) and (dielectric insulat\$3) and ((bit near line) with ((first second) near1 trench\$2)) and ((sidewall near1 spacer) with liner with mandrel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:26
L10	0	(flash near1 memory) and ((nand near string) with (substrate carrier)) and (dielectric insulat\$3) and ((bit near line) with ((first second) near1 trench\$2)) and (sidewall with spacer with liner with mandrel)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:27
L11	27	(nand near1 flash near1 memory) and (substrate carrier) same (dielectric insulat\$3) and ((bit near line) with ((first second) with trench\$2)) and (((first second) near direction) with perpendicular)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:27
L12	16	11 AND ((H01L27/11524 OR H01L21/76816 OR H01L21/76865 OR H01L21/76877 OR H01L27/0207).CPC.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:35
L13	16	KANEZAKI-E	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:37
L14	135	NAKAMURA-RYO	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:38
L15	0	14 and nand and trench\$2	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:38
L16	0	14 and nand	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2016/09/05 14:39

EAST Search History

			IBM_TDB			
L17	27	14 and memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:39
L18	2	JINNOUCHI-KOTARO	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2016/09/05 14:41

9/ 5/ 2016 2:42:15 PM**C:\ Users\ lthai\ Documents\ EAST\ Workspaces\ NAND-Flash-Memory.wsp**

Issue Classification 	Application/Control No. 14806111	Applicant(s)/Patent Under Reexamination KANEZAKI ET AL.
	Examiner LUAN C THAI	Art Unit 2891

CPC						
Symbol					Type	Version
H01L		27		11524	F	2013-01-01
H01L		21		76865	I	2013-01-01
H01L		21		76877	I	2013-01-01
H01L		21		76816	I	2013-01-01
H01L		27		0207	I	2013-01-01

CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
(Assistant Examiner)		20	
(Date)			
/LUAN C THAI/	09/05/16	O.G. Print Claim(s)	O.G. Print Figure
Primary Examiner.Art Unit 2891		1	4D, 9A, 9B
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 14806111	Applicant(s)/Patent Under Reexamination KANEZAKI ET AL.
	Examiner LUAN C THAI	Art Unit 2891

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION													
CLASS		SUBCLASS				CLAIMED					NON-CLAIMED								
257		296				H	0	1	L	27 / 108 (2006.0)									
CROSS REFERENCE(S)						H	0	1	L	21 / 20 (2006.0)									
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																		
438	386																		

NONE		Total Claims Allowed:	
		20	
(Assistant Examiner)	(Date)		
/LUAN C THAI/ Primary Examiner.Art Unit 2891	09/05/16	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4D, 9A, 9B

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Kanezaki et al.		
Title:	Alternating Sidewall Assisted Patterning		
Application No.:	14/806,111	Filing Date:	July 22, 2015
Examiner:	Luan C. Thai	Group Art Unit:	2891
Docket No.:	0084567-986US0	Conf. No.:	1674

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS – NOTICE
OF ALLOWANCE MAILED**

Dear Sir:

In response to the “Notice to File Corrected Application Papers – Notice of Allowance Mailed” mailed by the United States Patent and Trademark Office on October 19, 2016, Replacement Figure 2A is enclosed.

No new matter has been added.

Please telephone the undersigned at (415) 276-6500, if there are any questions.

Attorney Docket No.: 0084567-986US0

Application No.: 14/806,111

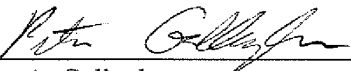
- 1 -

DWT 30570227v1 0084567-986US0

The Commissioner is hereby authorized to charge any additional fees, which may be required, or credit any overpayment to Deposit Account No. 04-0258.

FILED VIA EFS

Respectfully submitted,


Peter A. Gallagher
Reg. No. 47,584

10/19/16
Date

DAVIS WRIGHT TREMAINE LLP
505 Montgomery Street, Suite 800
San Francisco, California 94111-6533
Telephone: (415) 276-6500
Facsimile: (415) 276-6599

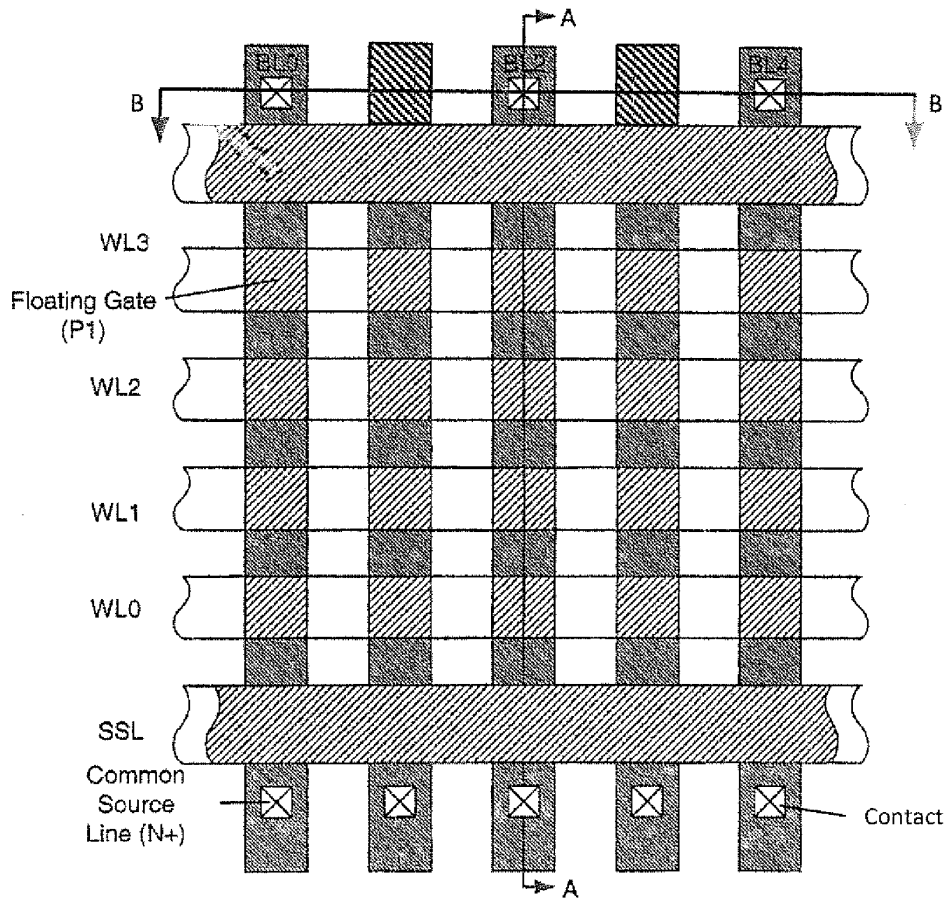


FIG. 2A (PRIOR ART)

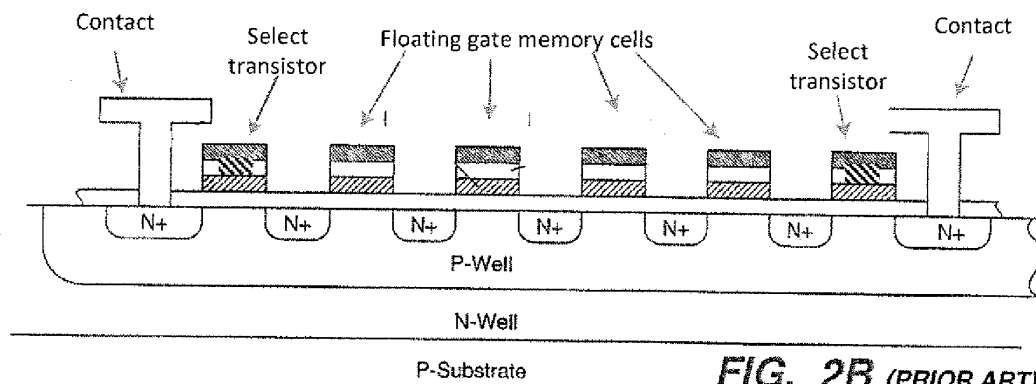


FIG. 2B (PRIOR ART)
(Section A-A)

Electronic Acknowledgement Receipt	
EFS ID:	27260010
Application Number:	14806111
International Application Number:	
Confirmation Number:	1674
Title of Invention:	Alternating Sidewall Assisted Patterning
First Named Inventor/Applicant Name:	Erika Kanezaki
Customer Number:	66785
Filer:	Peter Ailbe Gallagher/Eileen Bowen (PAG)
Filer Authorized By:	Peter Ailbe Gallagher
Attorney Docket Number:	0084567-986US0
Receipt Date:	19-OCT-2016
Filing Date:	22-JUL-2015
Time Stamp:	13:48:15
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	0084567-986US0_Response_MP.pdf	33688	no	2
			c728deaf58ad6a0ba5b2d58d7d0a2e1e7b1779c7		

Warnings:

Information:					
2	Drawings-only black and white line drawings	0084567-986US0_Replacement_Fig2A.pdf	106722	no	1
			c8abe282939d9625b0d0b87d9f3919b3db55cb36		
Warnings:					
Information:					
Total Files Size (in bytes):			140410		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. New Applications Under 35 U.S.C. 111 If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. National Stage of an International Application under 35 U.S.C. 371 If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. New International Application Filed with the USPTO as a Receiving Office If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanazaki	0084567-986US0	1674
66785 7590 10/19/2016 DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION IP Docketing Dept. Davis Wright Tremaine LLP 1201 Third Avenue, Suite 2200 Seattle, WA 98101			EXAMINER THAI, LUAN C	
			ART UNIT 2891	PAPER NUMBER
			NOTIFICATION DATE 10/19/2016	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentdocket@dwt.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 14806111
Applicant : Kanezaki
Filing Date : 07/22/2015
Date Mailed : 10/19/2016

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The informalities requiring correction are indicated in the attachment(s). If the informality pertains to the abstract, specification (including claims) or drawings, the informality must be corrected with an amendment in compliance with 37 CFR 1.121 (or, if the application is a reissue application, 37 CFR 1.173). Such an amendment may be filed after payment of the issue fee if limited to correction of informalities noted herein. See Waiver of 37 CFR 1.312 for Documents Required by the Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004). In addition, if the informality is not corrected until after payment of the issue fee, for purposes of 35 U.S.C. 154(b)(1)(iv), "all outstanding requirements" will be considered to have been satisfied when the informality has been corrected. A failure to respond within the above-identified time period will result in the application being ABANDONED.

See attachment(s).

*A copy of this notice **MUST** be returned with the reply. Please address response to
"Mail Stop Issue Fee, Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450".*

/Chris Harmon/
Publication Branch
Office of Data Management
(571) 272-4200

IDENTIFICATION OF DRAWING DEFICIENCIES

- ☐ There is a hole or the image thereof within the illustration. FIG(s)
- ☐ The illustration is penetrated or traversed by a solid or broken line that is not intended to be part of the drawing, such as a dark line caused by a flaw in the copying process. FIG(s)
- ☐ An ink stamp or the image thereof obscures part of the illustration. FIG(s)
- ☐ The drawing is marred by black smudges, obliterations, or fax/copier marks (for example, speckles or dots in a substantial portion of the drawing). FIG(s)
- ☐ Figure numbers are duplicated or missing. FIG(s)
- ☐ Drawing sheet or figure is missing. FIG(s)
- ☐ Numbers, letters, or reference characters in the drawing have been crossed out or are illegibly handwritten. FIG(s)
- ☐ The character of the lines, numbers, and letters is poor. FIG(s)
- ☐ The drawing's background shows that the original drawing was made on graph paper or other paper with a pattern or decoration. FIG(s)
- ☐ The FIG. number label is placed in a location that causes the drawing to be read upside down. FIG(s)
- ☒ Data, a reference number, or part of the drawing is truncated or missing, or a lead line has no reference number. FIG(s) 2A
- ☐ The drawing and/or the FIG. label contain(s) foreign language. FIG(s)
- ☐ This utility application contains a photograph of a view that is capable of being illustrated as a line drawing. FIG(s)
- ☐ A petition under 37 CFR 1.84(a)(2) to accept color drawings has been granted, but the brief description of the drawings in the specification does not contain (or has not been amended to contain) the paragraph required by 37 CFR 1.84(a)(2)(iii).
- ☐ This reissue application contains added and/or amended drawings that are not labeled as "New" or "Amended" or "Canceled" as required by 37 CFR 1.173(b)(3). FIG(s)
- ☐ This Design reissue application contains a drawing that is labeled as "Canceled" but is not surrounded by brackets, or a drawing that is surrounded by brackets but is not labeled as "Canceled." See 37 CFR 1.173(b)(3). FIG(s)
- ☐ OTHER:
- ☐ COMMENTS:

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

66785 7590 09/29/2016
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

Eileen Bowen	(Depositor's name)
EFS Filing	(Signature)
11-9-16	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	07/22/2015	Erika Kanezaki	0084567-986US0	1674

TITLE OF INVENTION: Alternating Sidewall Assisted Patterning

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	12/29/2016

EXAMINER	ART UNIT	CLASS-SUBCLASS
THAI, LUAN C	2891	257-296000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Davis Wright Tremaine
LLP
2. _____
3. _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

SanDisk Technologies LLC

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Plano, TX

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 040258 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature

Peter Gallagher

Date

11/9/16

Typed or printed name

Peter Gallagher

Registration No.

47,584

Electronic Patent Application Fee Transmittal				
Application Number:		14806111		
Filing Date:		22-Jul-2015		
Title of Invention:		Alternating Sidewall Assisted Patterning		
First Named Inventor/Applicant Name:		Erika Kanezaki		
Filer:		Peter Ailbe Gallagher/Eileen Bowen (PAG)		
Attorney Docket Number:		0084567-986US0		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt	
EFS ID:	27465313
Application Number:	14806111
International Application Number:	
Confirmation Number:	1674
Title of Invention:	Alternating Sidewall Assisted Patterning
First Named Inventor/Applicant Name:	Erika Kanezaki
Customer Number:	66785
Filer:	Peter Ailbe Gallagher/Eileen Bowen (PAG)
Filer Authorized By:	Peter Ailbe Gallagher
Attorney Docket Number:	0084567-986US0
Receipt Date:	09-NOV-2016
Filing Date:	22-JUL-2015
Time Stamp:	17:14:38
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$960
RAM confirmation Number	111016INTEFSW00003772040258
Deposit Account	040258
Authorized User	Eileen Bowen
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	0084567-986US0_Issue_Fee_Pa yment.pdf	71938	no	1
			fdf878c6c6b62b3c149adc6ac9f8d35504c25711		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30270	no	2
			965a448e171c8022b549f5ee14e918fc81e7b383		
Warnings:					
Information:					
Total Files Size (in bytes):			102208		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/806,111	12/20/2016	9524974	0084567-986US0	1674

66785 7590 11/30/2016
DAVIS WRIGHT TREMAINE LLP - SANDISK CORPORATION
IP Docketing Dept.
Davis Wright Tremaine LLP
1201 Third Avenue, Suite 2200
Seattle, WA 98101

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Erika Kanezaki, Yokkaichi, JAPAN;
SanDisk Technologies, Inc., Plano, TX;
Ryo Nakamura, Yokkaichi, JAPAN;
Kotaro Jinnouchi, Yokkaichi, JAPAN;
Satoshi Kamata, Yokkaichi, JAPAN;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
 Stylesheet Version v1.2

Assignment ID: PATI432478

SUBMISSION TYPE:	NEW ASSIGNMENT	
NATURE OF CONVEYANCE:	ASSIGNMENT	
CONVEYING PARTY DATA		
Name		Execution Date
SanDisk Technologies LLC		08/12/2024
RECEIVING PARTY DATA		
Company Name:	Palisade Technologies, LLP	
Street Address:	1468 James Rd.	
City:	Gardnerville	
State/Country:	NEVADA	
Postal Code:	89460	
PROPERTY NUMBERS Total: 14		
Property Type	Number	
Patent Number:	9530716	
Patent Number:	8148962	
Patent Number:	9501398	
Patent Number:	9448876	
Patent Number:	9454448	
Patent Number:	8327051	
Patent Number:	9466383	
Patent Number:	9281314	
Patent Number:	8996838	
Patent Number:	9373408	
Patent Number:	9524974	
Patent Number:	9349458	
Patent Number:	7743258	
Patent Number:	8135961	
CORRESPONDENCE DATA		
Fax Number:		
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>		
Phone:	3129194254	
Email:	dave@gerasimowlaw.com	

Correspondent Name:	David Gerasimow
Address Line 1:	FL3 PMB1717
Address Line 2:	211 W Wacker Dr
Address Line 4:	Chicago, ILLINOIS 60606
NAME OF SUBMITTER:	David Gerasimow
SIGNATURE:	David Gerasimow
DATE SIGNED:	08/15/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 2 source=SDTL Palisade Assignment#page1.tiff source=SDTL Palisade Assignment#page2.tiff	

SDTL PALISADE ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, **SanDisk Technologies LLC**, with a registered address at 7501 N Capital of Texas Hwy, Building A, Suite #100, Austin, TX 78731, ("Assignor"), does hereby assign, transfer and convey unto **Palisade Technologies, LLP**, with an office at 1468 James Rd., Gardnerville, NV 89460, USA, ("Assignee"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Schedule A (collectively "Patent Rights").

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

This assignment is made effective as of: August 7, 2024.

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at Sandy, UT, USA
on 8/12/24.

ASSIGNOR SanDisk Technologies LLC,

By:

Name: David Dutcher

Title: VP, Chief IP and Licensing Counsel

STATE OF Utah)
COUNTY OF South Lake) ss.

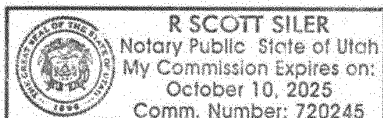
On 08-12-2024 before me,

R. Scott Siler Notary Public

Personally appeared David Dutcher, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that she executed the same in her authorized capacity, and that by her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of Utah that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.



R. Scott Siler
Notary Public

SCHEDULE TO ASSIGNMENT

Country	Patent/Publication Number	Application Number
US	9,530,716	13/452,767
KR	10-1774059	2011-7028490
US	8,148,962	12/464,301
CN	ZL201380072287.2	201380072287.2
US	9,501,398	13/831,218
US	9,448,876	14/454,667
US	9,454,448	14/454,672
US	8,327,051	11/986,389
US	9,466,383	14/144,056
US	9,281,314	14/511,834
US	8,996,838	14/273,031
TW	TW201606496	104112604
CN	ZL201510626779.2	201510626779.2
DE	102015116905	102015116905.3
US	9,373,408	14/508,274
US	9,524,974	14/806,111
US	9,349,458	14/515,762
US	7,743,258	11/511,766
US	8,135,961	12/760,359

PTO/AIA/81A (02-15)

Approved for use through 03/31/2021. OMB 0651-0035

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	9524974
	Issue Date	12/20/2016
	First Named Inventor	Erika KANEZAKI
	Title	Alternating sidewall assisted patterning
	Attorney Docket No.	9062-0024

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

174899

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name

Address

City

State

Zip

Country

Telephone

Email

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 1.33(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

Signature	<i>Peter Hardigan</i>	SIGNATURE of Applicant or Patent Owner	Date	8/29/2024
Name	Peter Hardigan	Telephone	(917) 622-0926	
Title and Company	Manager, Palisade Technologies, LLP			

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: PALISADE TECHNOLOGIES, LLP

Application No./Patent No.: 9524974 Filed/Issue Date: 12/20/2016

Titled: ALTERNATING SIDEWALL ASSISTED PATTERNING

PALISADE TECHNOLOGIES, LLP, a LIMITED LIABILITY PARTNERSHIP

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is ____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: ERIKA KANEZAKI, ET AL. To: SANDISK TECHNOLOGIES INC.

The document was recorded in the United States Patent and Trademark Office at
Reel 036407, Frame 0563, or for which a copy thereof is attached.

2. From: SANDISK TECHNOLOGIES INC To: SANDISK TECHNOLOGIES LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 038812, Frame 0954, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: SANDISK TECHNOLOGIES LLC To: PALISADE TECHNOLOGIES, LLP

The document was recorded in the United States Patent and Trademark Office at
Reel 068301, Frame 0100, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David Gerasimow/

Signature

David Gerasimow

Printed or Typed Name

08-29-2024

Date

57,512

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION # 14/806,111	RECEIPT DATE / TIME 08/29/2024 04:45:16 PM Z ET	ATTORNEY DOCKET # 0084567-986USO
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Title of Invention

Alternating Sidewall Assisted Patterning

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	9524974
CONFIRMATION #	1674	FILED BY	David Gerasimow
PATENT CENTER #	66982867	FILING DATE	07/22/2015
CUSTOMER #	66785	FIRST NAMED INVENTOR	Erika Kanazaki
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA9524974.pdf	2	Power of Attorney	265 KB
Warning: The PDF file has been signed with a digital signature and the legal effect of the document will be based on the contents of the file not the digital signature.			
POA9524974 3.73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	119 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA9524974.pdf	FA6C05571035D211B8AFD7C5346462FA26439F9681DC9F535 0C030F6EDB0BD5245D22411C15499E6597BC877CF2192716C B802A290238DBED4DEEACA437F727C

POA9524974 3.73c.pdf

37626606C00131BA054B12D123FB4D8BBF8DE17BC6FD97C44
154B5644677E9016D97273F0952EEB90554C4B8664CE4DC8D
EDB6C69C58845C63D2D0C36022A7E3

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/806,111	07/22/2015	Erika Kanazaki	9062-0024

CONFIRMATION NO. 1674

174899

The Law Offices of David A. Gerasimow, P.C.
211 W. Wacker Dr.
Ste. 1717
Chicago, IL 60606

POA ACCEPTANCE LETTER



OC000000077829941

Date Mailed: 09/13/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/dtdinh/