

1[preamble] A NAND flash memory comprising:	12[preamble] A method of forming a NAND flash memory comprising:	17[preamble] A method of forming a NAND flash memory comprising:
1[a] a semiconductor substrate;		
1[b] a dielectric layer extending over the semiconductor substrate;		
	12[a] forming a plurality of NAND strings disposed on a surface of a substrate;	17[a] forming a plurality of NAND strings disposed on a surface of a substrate;
	12[b] depositing a dielectric layer over the plurality of NAND strings;	17[b] depositing a dielectric layer over the plurality of NAND strings;
1[c] a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;	12[c] etching a plurality of first trenches in the dielectric layer, each first trench being elongated along a first direction and having a first shape in cross section along a plane that is perpendicular to the first direction;	17[g] subsequently etching a plurality of first trenches in the dielectric layer, an individual first trench formed at a location between sidewall spacers that were formed on a common mandrel;
1[d][i] a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane, [ii] the second shape being different from the first shape, [iii] the first and second trenches arranged in an alternating pattern that alternates from a first trench to second trench along a second direction that is perpendicular to the first direction; and	12[d] etching a plurality of second trenches in the dielectric layer, each second trench being elongated along the first direction and having a second shape in cross section along the plane,	
	12[e] the second shape being different to the first shape,	
	12[f] the first and second trenches arranged in an odd-even alternating pattern along a direction that is perpendicular to the first direction such that two first trenches are separated by a second trench; and	
1[e] a plurality of bit lines located in the first trenches.	12[g] depositing metal in the plurality of first trenches to form a plurality of bit lines located in the first trenches.	
	13. The method of claim 12 further comprising, prior to etching the plurality	17[c] forming a plurality of mandrels on the dielectric layer;

	of first trenches and the plurality of second trenches, forming an etch mask that includes a plurality of mask portions, each mask portion comprising a sidewall spacer part that is formed of a first material and a liner part that is formed of a second material.	17[d] forming a liner layer along side surfaces of the plurality of mandrels; 17[e] forming sidewall spacers on the liner layer along side surfaces of the plurality of mandrels; 17[f] removing the plurality of mandrels to leave a pattern of sidewall spacers with portions of liner layer material;
		17[h] etching a plurality of second trenches in the dielectric layer, an individual second trench formed at a location between sidewall spacers that were formed on neighboring mandrels; and
		17[i] depositing copper in the plurality of first trenches to form a plurality of bit lines located in the first trenches.
	14. The method of claim 13 wherein the second material has a higher etch rate than the first material and wherein first trenches are formed at locations corresponding to locations of liner parts of neighboring mask portions.	
2[a] The NAND flash memory of claim 1 further comprising a plurality of additional bit lines located in the second trenches,	15. The method of claim 12 further comprising depositing the metal in the plurality of second trenches to form a plurality of additional bit lines located in the second trenches.	18. The method of claim 17 further comprising depositing the copper in the plurality of second trenches to form a plurality of additional bit lines.
2[b] each of the plurality of bit lines having the first shape in cross section along the plane and each of the plurality of additional bit lines having the second shape in cross section along the plane.		

4. The NAND flash memory of claim 1 wherein the first shape has a first width at a level of an upper surface of the dielectric layer, the second shape has a second width at the level of the upper surface of the dielectric layer, and the second width is less than the first width.		
6. The NAND flash memory of claim 1 further comprising a plurality of air gaps located in the second trenches.	16. The method of claim 12 further comprising depositing the metal in the plurality of second trenches to cap air gaps in the plurality of second trenches.	
9. The NAND flash memory of claim 1 wherein the first shape has an upper portion that extends from a level of an upper surface of the dielectric layer down to an intermediate level with tapering sidewalls, and has a lower portion that extends from the intermediate level to a bottom surface of the first shape, the lower portion having Substantially parallel sidewalls.		
11. The NAND flash memory of claim 1 wherein the plurality of first trenches have a first depth and the plurality of second trenches have a second depth that is different to the first depth.		