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Micro/Nano Lithography

Double patterning lithography: double the trouble or double the fun?

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The immaturity of next generation technologies means that existing techniques need to be extended in order to solve the 32nm and 22nm half-pitch nodes.

20 July 2009, SPIE Newsroom. DOI: 10.1117/2.1200906.1691

Delays in readiness of next generation lithography (NGL) suggest the use of existing methods to enable the production of key technologies at the 32 and 22nm half-pitch nodes. In order to achieve this, some version of double patterning (DP) technology will need to be combined with established techniques. The most obvious of these is 193nm immersion (193i) lithography. Although the cost of ownership of a combined method is an issue, the huge opportunity costs of any NGL in its current state make DP lithography (DPL) the clear choice for the foreseeable future.

What is unclear is the exact approach or combination of approaches that will provide the best resolution and the best economics for the 22nm node and beyond. Despite the lack of an obvious choice of methodology, DPL has already shown that it is lithography's bridge to the 22nm node,¹ producing a six-transistor static random access memory (SRAM) cell under 0.1 μm^2 nearly six months before a similarly scaled SRAM was produced using extreme ultraviolet lithography.² Still, DP is a relative newcomer to lithography, brought on by necessity rather than any desire to embrace the methodology. For the lithography community, DP is double the trouble because there is no new breakthrough technology behind it. An alternative wavelength for photolithography is perhaps a decade away from being introduced into manufacturing, and no other lithography-based disruptive technologies are on the horizon. For process engineers around the world, however, DP is double the fun because of the new opportunities the technology offers. It comes in so many novel varieties (each with its own processing-related challenges) that process engineers everywhere are celebrating resulting in a new found popularity for DP within the lithography community.

Each of the major DPL techniques comes with its own pros and cons (see Table 1). One of the initial efforts was a litho-etch, litho-etch (LELE) approach that requires, as the name suggests, two etch steps.³ Developed subsequently, the litho-freeze process requires only one etch step and uses a track process to 'freeze' the resist before undergoing a second resist coat and exposure step (see Figure 1).⁴ Because the freeze uses a chemical modification of the first exposed/developed resist, it is not adversely affected by subsequent lithography processing. The cost of ownership of this approach should be less than LELE, since fewer processing steps are needed. However, overlay remains a concern at 22nm.

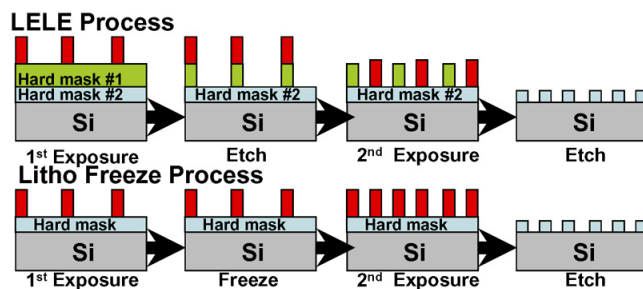


Figure 1. Schematic of two approaches to double patterning lithography. The litho-freeze process was developed subsequently to the litho-etch, litho-etch (LELE) approach. Si: silicon substrate.

Another promising contender for DPL is dual-tone development (DTD), in which a conventional exposure is followed by two development steps.⁵ In positive-tone development, all material that has been exposed to some threshold dose is removed, while in negative-tone development, all material that has a threshold lower than a specific dose is removed. DTD may be a path to lowering cost of ownership. However, many materials issues must still be overcome.⁵ Additionally, line edge roughness (LER) is an issue in the development process,⁶ and the combination of two development steps may result in unacceptable LER.

The self-aligned double patterning (SADP) process (see Figure 2) is another variation of DPL.⁷ With SADP, the resist is exposed, followed by development. A masking material is then deposited and etched to form sidewall spacers. The resist material from the exposure step is then removed and the substrate etched using the remaining spacers as a mask. Lastly, the residual spacers are removed leaving the final pattern.

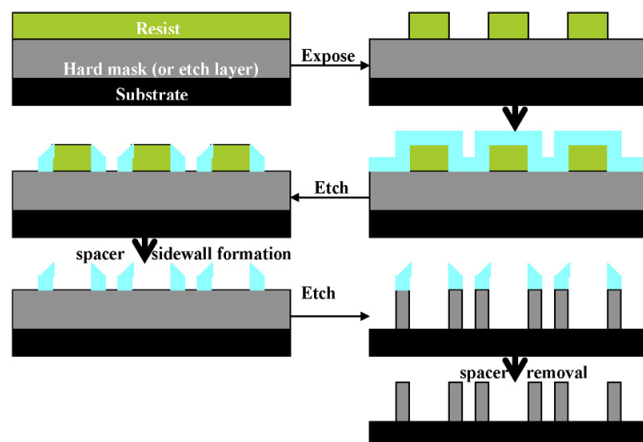


Figure 2. Schematic of the general process flow for the self-aligned double patterning (SADP) process. A masking material is deposited on top of a processed resist material to form sidewall spacers.

Table 1. Summary of DPL advantages and disadvantages

DP approach	Advantages	Disadvantages
Litho-etch, litho-etch (LELE)	No fundamental limitations ≥ 22 nm	Costly extra processing Challenging overlay for ≤ 22 nm
Litho-freeze	No fundamental limitations ≥ 22 nm Intermediate processing possible on track	Costly extra processing Challenging overlay for ≤ 22 nm
Self-aligned double patterning (SADP)	Single critical exposure, other processing steps are done offline on less expensive tools More cost effective than LELE or Litho-freeze	Need to modify design for 2D applications Significant extra processing required

	No overlay issues→Better scalability Currently applicable to memory patterning Best line-edge/linewidth roughness and critical dimension uniformities	
Dual tone development (DTD)	Improved cost effectiveness	New materials development required Negative-tone materials historically difficult Does not currently meet 32nm requirements Challenging overlay for ≤ 22 nm Line-edge/linewidth roughness may be a show stopper
Double exposure (DE)	Best overall cost No overlay issues	Materials not currently available Material integration may be difficult No intrinsic improvement for Line-edge/linewidth roughness may limit applicability below 22nm

The advantages of the SADP process are that only one critical exposure is needed and overlay poses no issue. In addition, both critical dimension uniformities (CDUs) and LER are shown to be improved over any conventional lithography process, meeting the International Technology Roadmap for Semiconductors requirements for the 22nm node.⁷

The main limiting factor for a broad implementation of this technique is that it is not well suited to non-uniform designs. Recently, however, a proposed gridded design scheme with SADP has suggested a path to 16nm on a 44nm pitch for logic chips.⁸ A method of contact formation using SADP has been proposed,⁹ indicating that further development may enable this technique to have broader applicability than memory applications. Further, SADP processing done externally to the exposure tool uses equipment that is far less costly than adding additional exposure tools.

An alternative is to use double exposure (DE) materials. This approach would have the lowest cost of ownership of all DPL technologies and would eliminate the overlay concerns as the wafer does not leave the exposure tools between the two exposures. However, this approach has several clear drawbacks. First, the necessary materials do not yet exist. Second, even if these materials are developed, their integration into a working resist system in a timeframe useful for integration into 22nm processing will be challenging. Since this process still uses diffusion, LER may limit the utility of this approach beyond the 22nm node.

With no NGL available for the foreseeable future, arguments about the cost of ownership of DPL are not currently relevant. Double the trouble or double the fun, the bottom line is that some form of DPL will be used for the 32nm and 22nm nodes and likely beyond because it poses no fundamental show stoppers to implementation.

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Paul Zimmerman received his PhD in chemistry from the University of Pittsburgh and completed an MBA in 2000. He has worked for Intel Corporation since 1994, researching and solving complex material problems related to device performance, metrology, and lithography. Paul is currently on assignment in the Lithography Division at SEMATECH.

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