

22nm Half-Pitch Patterning by CVD Spacer Self Alignment Double Patterning (SADP)

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ABSTRACT

Self-aligned double patterning (SADP) is a patterning technique that uses CVD spacers formed adjacent to a core (template) pattern that is defined by conventional lithography. After stripping the core (template) material, the spacers serve as a hardmask with double the line density of the original lithographically defined template. This integration scheme is an alternative to conventional double patterning for extending the half-pitch resolution beyond the current lithography tool's half-pitch limit. Using a positive tone (spacer as mask) approach, we show capability to create 22nm line and space arrays, on 300mm wafers, with full wafer critical dimension uniformity (CDU) < 2nm (3 sigma) and line edge roughness (LER) < 2nm. These 22nm line and space results stem from template lithography using 1.2NA 193nm water immersion lithography. In this paper, we also demonstrate lot to lot manufacturability, the patterning of two substrate types (STI and silicon oxide trench), as well as demonstrate the formation of gridded design rule (GDR) building blocks for circuit design.

Keywords: self-aligned double patterning, APF®, spacer mask, frequency doubling, SADP, SaDPT,

1. INTRODUCTION

Current state-of-the-art photo lithography scanners using 193nm wavelength lasers and numerical apertures of 1.35 have reached fundamental printing limits of 40-45nm (half-pitch). Yet, consumer demands and device trends continue to drive smaller feature sizes, and most flash memory manufacturers have already navigated beyond the lithographic printing limits by turning to double patterning techniques. One new process flow that is gaining recognition and acceptance in the world of NAND flash is “self-aligned double patterning” also known as “spacer mask patterning”, “frequency doubling”, or “pitch-halving”. This process flow involves using sidewall spacers to create hard masks as a means of doubling the printed line density [1]. The NAND flash masking layers that are currently experimenting with the sidewall spacer patterning schemes include active area, gate, wordline, and bitline.

Generic SADP Process Flow:

The strength of spacer mask patterning is in its ability to create high density arrays of parallel lines. For any given line that is lithographically defined, spacers can be applied on each side that effectively doubles the line density after stripping the original template material. Depending on the process flow, one can either create positive tone (lines) or negative tone (trenches) hard masks.

A positive spacer tone example of this process flow includes (a) lithography, (b) resist trim, (c) template etch, (d) spacer formation (deposition and etch), (e) strip of the sacrificial template, (f) device etching using the spacers as a hardmask, and hardmask strip (Figure 1). In this case, “positive spacer tone” means that spacers are used as hardmask.

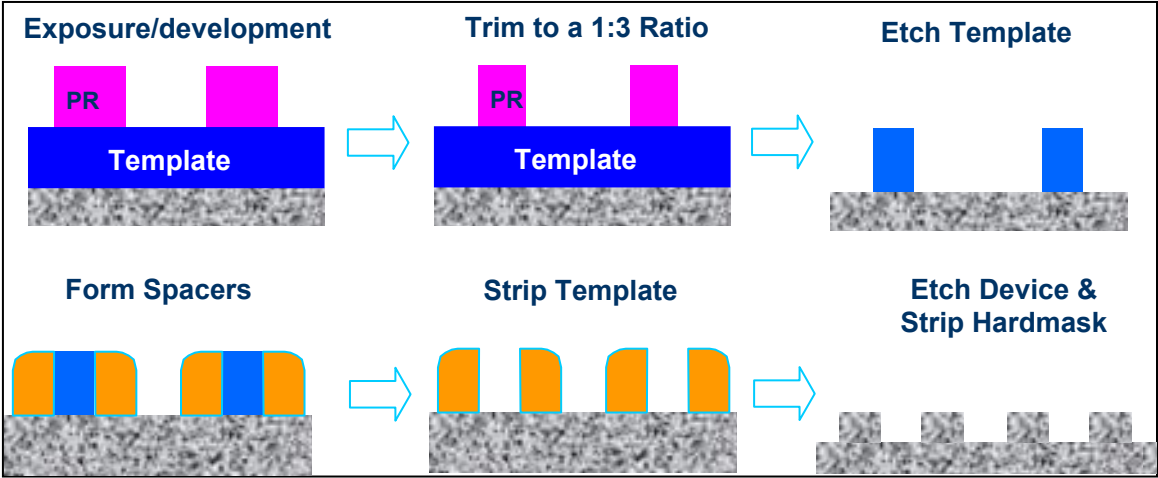


Figure 1. Generic process flow for positive tone spacer mask double patterning.

A negative spacer tone example of this process flow includes (a) lithograph, (b) resist trim, (c) template etch, (d) spacer formation (deposition and etch), (e) gap fill, (f) CMP, (g) spacer strip, and (h) device etching and hardmask strip (Figure 2). In this case, “negative spacer tone” means that spacers are ultimately removed effectively reversing the tone.

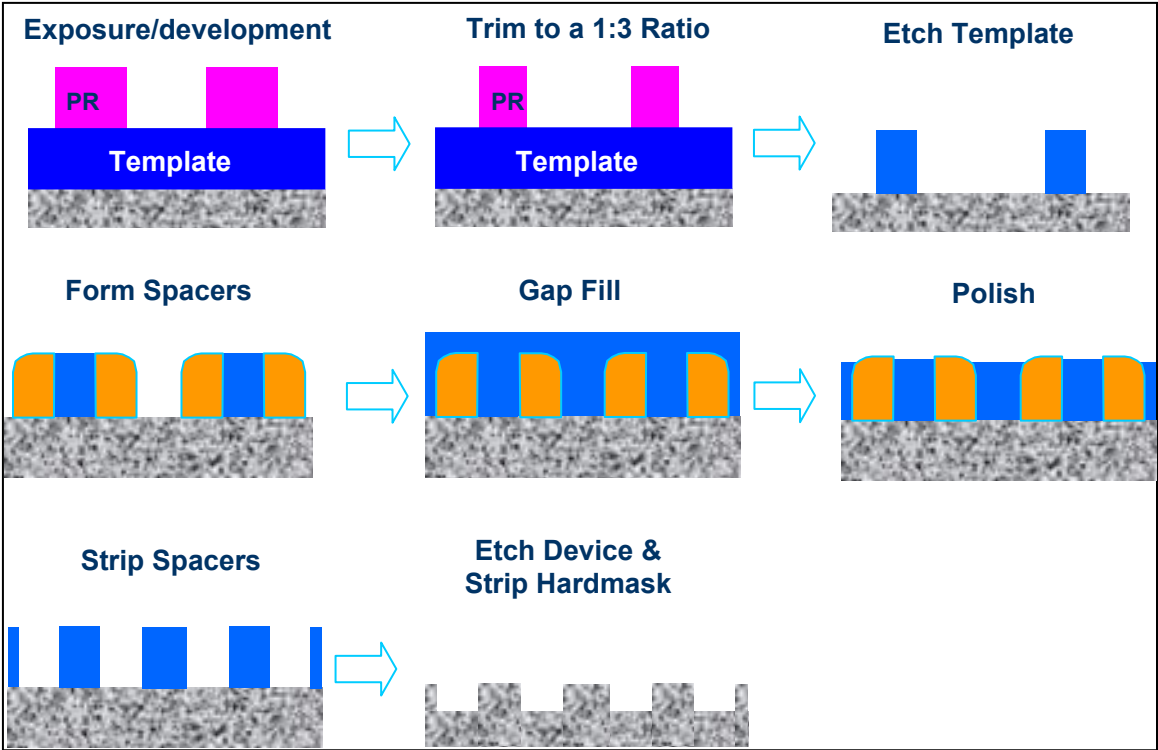


Figure 2. Generic process flow for negative tone spacer double patterning.

In both cases, the chip designers and mask designers need to work closely together because the lines (or trenches) do not lie where the original lithographically generated lines (or trenches) were printed. In addition, for each single line in the template, two lines are formed that ultimately form a closed loop. One such example is shown in Figure 3.

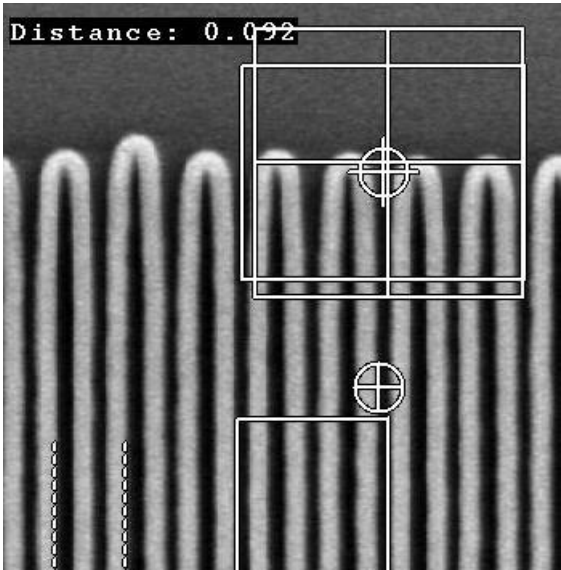


Figure 3. SEM image of spacer mask applied to template of parallel lines, after stripping template.

The pattern formed by the spacer is itself does not build a usable circuit; therefore, additional mask and etch steps are performed to “re-work” the closed loop, parallel lines into real device circuits. An easy two-mask sequence of rework to visualize is the positive spacer tone example for NAND-flash floating gate formation. These two masks typically involve cropping away areas of the spacer and adding larger periphery features such as wide lines or pads. In Figure 4, we show a hypothetical mask set.

Mask A defines the template (or sacrificial core) pattern that is used for the spacer mask double patterning. Mask B illustrates a hypothetical cropping mask that would trim the closed-loop patterns into individual lines. Mask C illustrates a hypothetical periphery mask, which would define larger features such as contact pads.

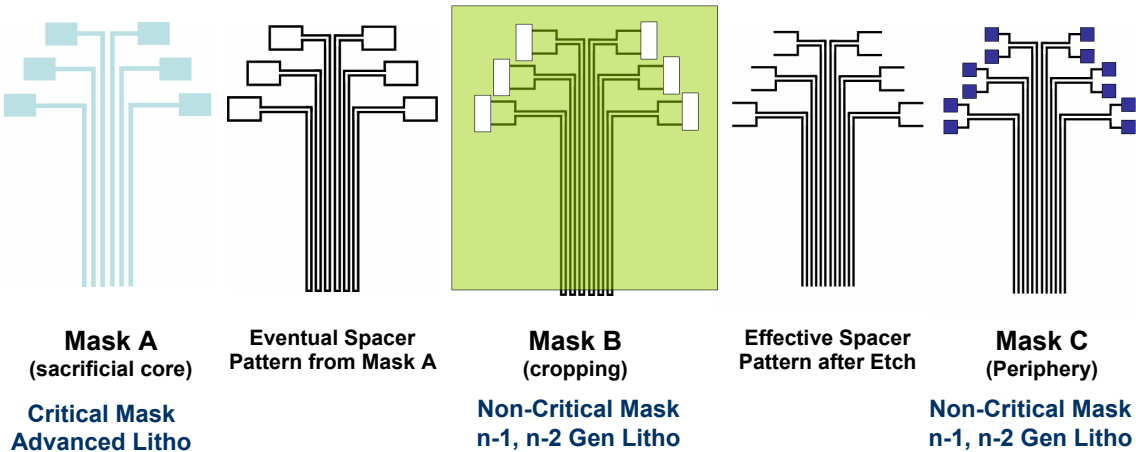


Figure 4. Hypothetical mask set for spacer mask patterning including (A) template, (B) cropping ,and (C) periphery.

2. DEMONSTRATING 22NM HALF-PITCH SADP

To demonstrate the implementation of SADP for building a 22nm line and space array, we designed a patterning film stack: Producer® APF® (CVD carbon hardmask material), CVD nitride (or silicon) cap, followed by another layer of APF to serve as a sacrificial template, and finally, another dielectric cap (Figure 5.1). Photolithography was performed using an ASML 1700i water immersion tool, printing 45nm line and space, which was subsequently trimmed to 23nm line (67nm space) before etching the APF template. Following this, a CVD dielectric spacer was deposited targeting a 22nm sidewall width, leaving a 23nm gap between spacers (Figure 5.3). After spacer etch, the APF template was cleanly removed using a conventional oxygen ash process requiring no wet-clean. Finally, the spacers were used as a hardmask to transfer the pattern into the bottom layer of APF (Figure 5.5), which was then used to drive the final pattern into silicon (Figure 5.6). Since APF is a widely adopted hardmask for most dielectrics and conductors used in the semiconductor industry, this scheme could be applied universally to any desired substrate material. SEM images of the process flow are shown in Figure 6.

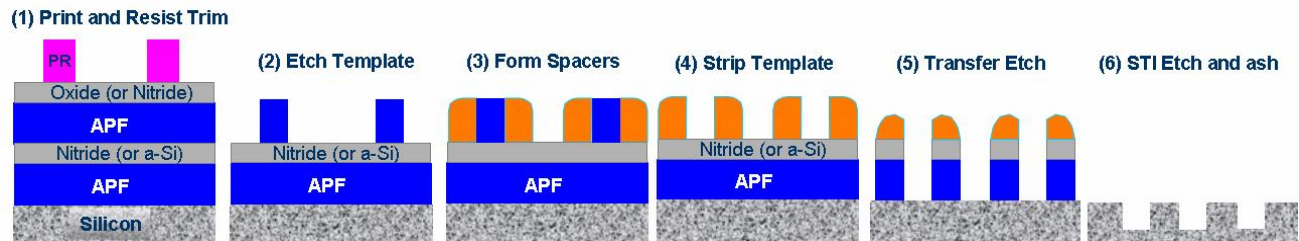


Figure 5: Illustration of process flow for generating 22nm STI array.

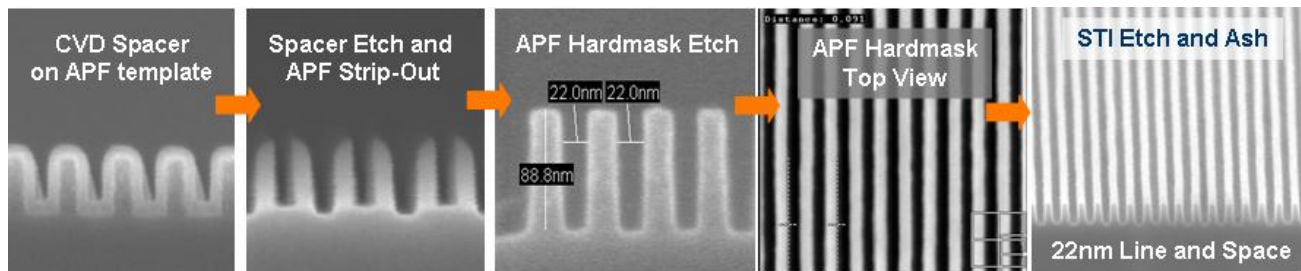


Figure 6: SEM images of process flow.

CD SEM characterization was performed after formation of the Producer APF hardmask. Five key dimensions were measured including line width, template space, gap space, line edge roughness (LER) on the line edge adjacent to the template space and LER on the line edge adjacent to the gap space (Figure 7). For these measurements, we report mean and 3 sigma values in nanometers (Table 1) taken from a 20 die spiral map.

The terms “template space” and “gap space” are new to the industry, so we will define their meaning. Within the line and space array, each line is defined primarily by the sidewall spacer. Therefore, all lines originate from the same processing step and therefore maintain the same CD mean and distribution. However, in the case of the spaces, adjacent spaces originate from different physical structures. The space which originates from the template (Mask A) is termed the “template space”. The space which originates from the gap between spacers (Figure 5.3) is termed the “gap space”.

It is possible that the template space and the gap space do not have the same CD mean and distribution; however, the bias between these two dimensions is easily controlled by the photoresist trim step. If the template space and gap space are not equal, one can simply feed-back the correction needed to the photo-resist trim etch to make them matched. Additionally, if the line width is not on target, a bias can easily be applied by increasing or decreasing the deposition time during the spacer deposition process. It is therefore very easy to perform CD bias corrections and achieve equal line and space arrays using one or two iterations through the process sequence.

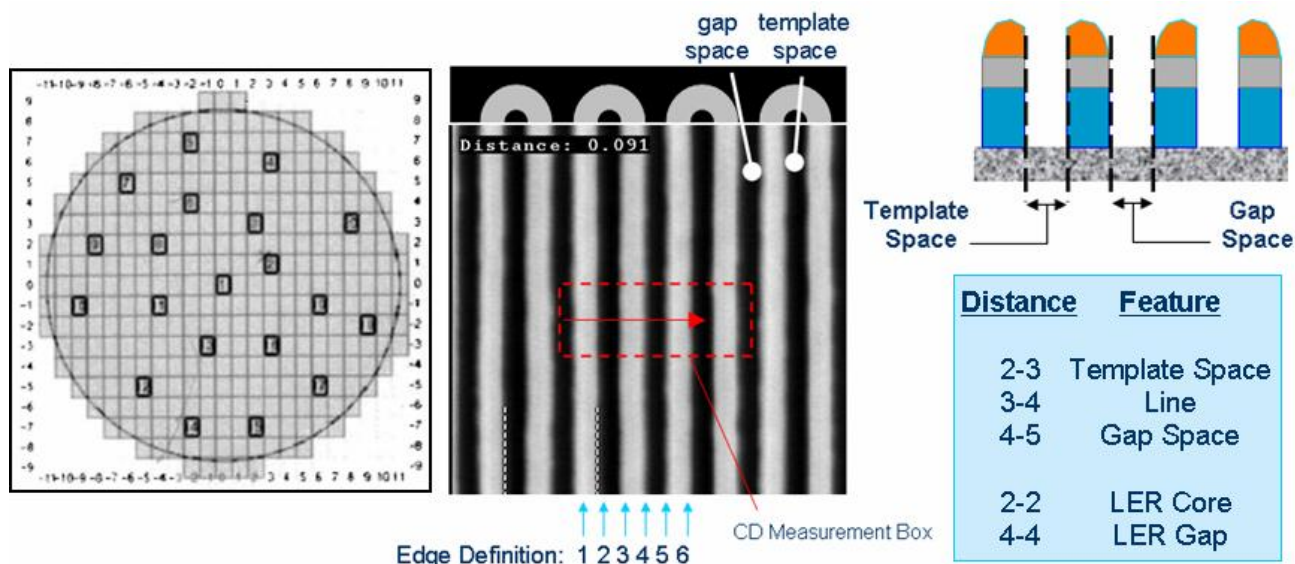


Figure 7. CD SEM measurement map, set-up, and definition of key dimensions.

		Immersion Litho	Template Space	Line	Gap Space	LER Template	LER Gap
Mean (nm)	Slot 16	47.6	24.1	22.8	22.9	1.6 nm	1.7 nm
	Slot 25	47.5	24.7	22.5	22.7	1.6 nm	1.5 nm
3 Sigma (nm)	Slot 16	1.8	1.7	1.8	2.2		
	Slot 25	1.8	2.0	1.1	2.5		

Table 1: CD SEM summary data (in nanometers) for 22nm SADP demonstration. Measurement of APF hardmask.

The results from our 300mm wafer demonstrations are shown above (Table 1). The target CD was 22.5nm, which was defined by the 90nm immersion lithography pitch divided by 4. After a few iterations of bias corrections we were able to achieve all CDs were within 2nm of the target. Within wafer CD uniformity of the lines were <2nm (3 σ) and LER on both interfaces was <2nm. In addition to using the APF hardmask to form STI trenches (Figure 6, far right), we also demonstrated the formation of 22nm half-pitch trenches in oxide [2] (Figure 8). Samples from these demonstrations were sent to customers for 3rd party verification; which confirmed similar CD performance finding all 3-sigma values less than 2.0nm and core-space / template-space matching of less than 0.5nm.

To study the lot-to-lot manufacturability, we replicated the process flow across three separate wafer runs spanning a time period of three months. A summary of this lot-to-lot repeatability is shown in Table 2, where the small wafer runs demonstrate the capability to control CDs within 2nm of the 22.5nm target CD.

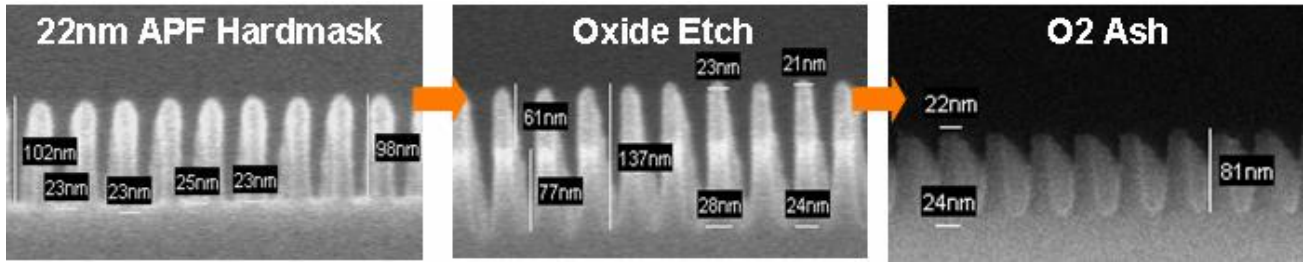


Figure 8. Snapshots of SADP process flow for etching 22nm half-pitch trenches in silicon oxide.

	Wafer CD Mean (nm)			3 sigma CDU (nm)		
	Lot 1	Lot 2	Lot 3	Lot 1	Lot 2	Lot 3
Space (Template)	24.1	23.7	23.5	1.7	1.8	2.1
Line Width	22.8	23.8	24.1	1.9	1.2	1.1
Space (Gap)	22.9	22.3	22.3	2.2	3.3	3.5

Table 2: CD SEM measurements for 3 separate spacer mask patterning runs, demonstrating stable process flow. CD measurement is on APF Hardmask.

3. MANIPULATION OF SADP ARRAY INTO USABLE CIRCUIT

To illustrate how one might go about manipulating the 22nm array into a usable circuit, we applied a cutting mask to the 22nm STI trenches and built examples of gridded design rule structures. After silicon etch was performed to cut the once continuous array of STI, we obtained 22nm active areas comprised of both long lines and small islands mixed densely together (Figure 9). For further details related to the designing of logic circuits using this method of manufacturing, please refer to the accompanying conference paper (6925-48) entitled “APF Pitch-Halving for 22nm Logic Cells using Gridded Design Rules” authored with Michael Smayling of Tela Innovations.

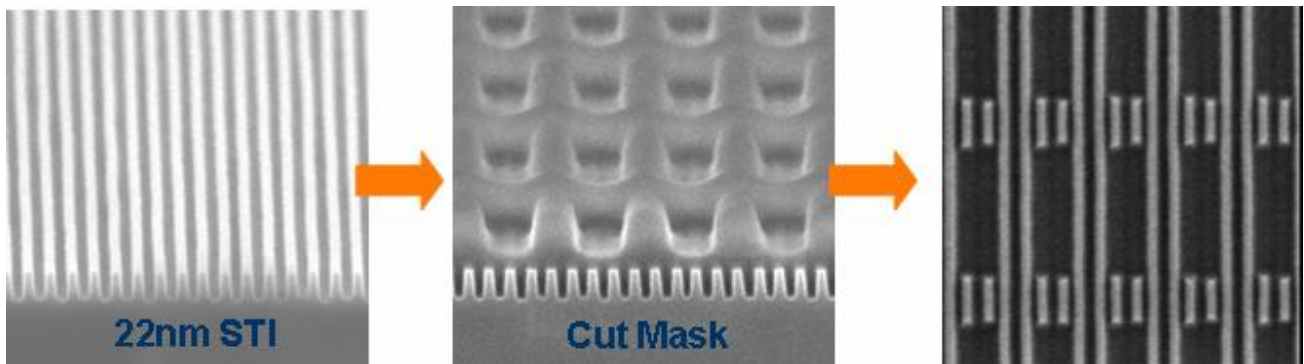


Figure 9: Examples of 22nm half-pitch GDR (gridded design rule) structures patterned into silicon. The structures were manufactured using an SADP (self-aligned double patterning) spacer hardmask scheme in conjunction with a cut mask.

4. CONCLUSIONS

With the physical limits of photolithography reached, and double patterning a certain path for device manufacturing in years to come, the spacer mask double patterning scheme clearly demonstrates the technical capabilities to meet

roadmap requirements down to at least 22nm half-pitch. The demonstrations discussed, stemming from a dual layer APF patterning stack, show world leading half-pitch, CD uniformity, LER, overlay and profile simultaneously with full 300mm manufacturability. The performance of this scheme and ease of execution highlights why spacer mask patterning schemes are the best option for NAND flash.

The authors would like to thank the Maydan Technology Center Group at Applied Materials and all the members of the double patterning team, including numerous engineers from spacer deposition and etch product groups. Special thanks also for the great collaborative effort from Chris Borst and the rest of the lithography teams at the State University of New York at Albany College of Nanoscale Science and Engineering.

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