The Chalkboard

Electrical Techniques for the Characterization of Dielectric Films

by T. Kundu, R. Garg, N. A. Chowdhury, and D. Misra

The science and technology of dielectric materials—a strong topic in physics, chemistry, and electrical engineering—has been pursued for well over 100 years. At present, dielectric materials have wide applications throughout the electronics, microwave, communication, and aerospace industries. Silicon dioxide has been the most significant and ubiquitous dielectric for several decades. This material is used as the gate dielectric in complementary metal oxide semiconductor (CMOS) technology, which dominates the modern electronics industry. Silicon dioxide is currently being replaced by higher dielectric constant (high-*k*) materials to reduce power consumption in microchips. The understanding of this dielectric film electrically still remains a challenge. Metal/insulator/semiconductor (MIS) structures are widely used for the characterization of dielectric materials as shown in this tutorial.

A dielectric material is deposited as a thin film, on p- or n-type semiconductor surfaces (*e.g.*, Si, Ge) by various techniques including thermal oxidation, sputtering, and chemical vapor deposition. On top of that, gate metals like Al and Pt are deposited to complete the MIS structure (Fig. 1). Inside the dielectric, there are four different types of charges that contribute to the capacitance: (*i*) fixed oxide charge, primarily due to the structural defects in the dielectric; (*ii*) oxide trapped charge, whose origin is due to trapped electrons or holes in the bulk of the dielectric; (*iii*) mobile ionic charge, if ionic impurities are present in the dielectric; and (*iv*) interface charge, formed due to oxidation-induced structural defects and by broken bonds at the interface.[1] These charges can be measured by measuring the capacitance as a function of voltage. During the measurement a dc voltage is swept from the negative to positive direction and is superimposed by an ac signal with a small amplitude of 10-15 mV. The dc voltage determines the bias condition while the ac voltage is necessary to measure the capacitance.

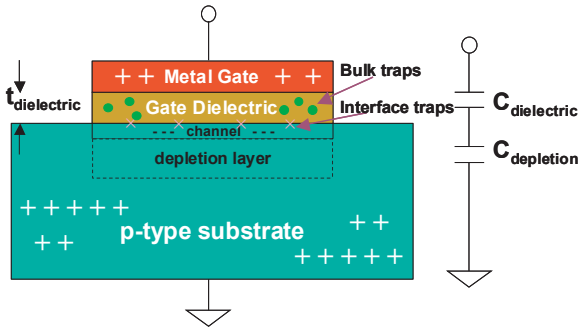


FIG. 1. A metal/insulator/semiconductor (p-type) (MIS) structure is shown that is used extensively to characterize dielectric films. Dielectric/semiconductor interface traps and bulk traps are shown. For positive gate bias, semiconductor and metal gate act as cathode and anode, respectively, whereas for negative gate bias, the opposite holds. The equivalent circuit of the series capacitance of dielectric and depletion capacitances is also provided.

When the voltage is swept across the MIS device, the semiconductor surface goes through an accumulation of majority carriers (electrons for n-type and holes for p-type), depletion of majority carriers, or inversion with minority carriers. For example, if we consider a p-type semiconductor for our MIS device and apply a negative potential at the metal electrode (gate), mobile positive holes, the majority carriers accumulate at the dielectric-semiconductor interface during accumulation. These carriers form a thin layer, which acts much like a parallel plate capacitor equal in area to the gate. Once the voltage is raised to a small positive value, the holes are repelled, causing depletion. Raising the voltage further attracts electrons to the interface. The electrical equivalent circuit of a MIS capacitor is, therefore, a series combination of a fixed voltage-independent gate oxide (insulator) capacitance and a voltage-dependent semiconductor capacitance due to depletion (Fig. 1).

Figure 2 shows the C-V characteristics of MIS structures with a dielectric deposited on a p-type semiconductor. Both the cases of dielectric with and without traps (ideal case) are considered. The capacitance in the accumulation region is defined by the gate area (A) and the dielectric thickness ($t_{dielectric}$) and is designated as $C_{dielectric}$ (the accumulation capacitance). The dielectric constant (k) can be obtained from the following equation

$$K = \frac{C_{dielectric}\ t_{dielectric}}{A} \qquad [1]$$

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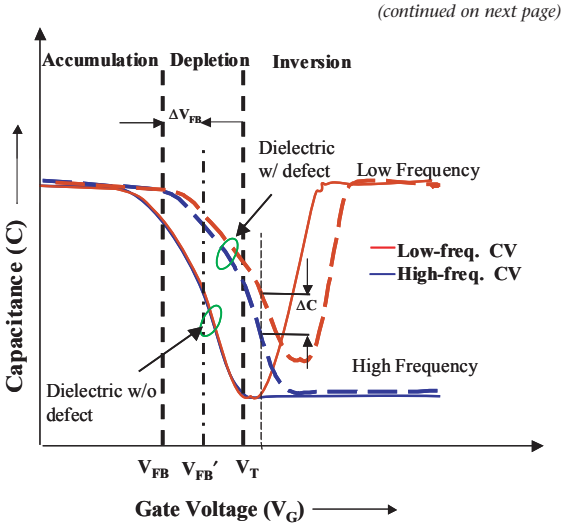


FIG. 2. High-frequency (hf) and low-frequency (lf) capacitance-voltage (C-V) characteristics of MIS structure for dielectric films with and without (ideal) defects are shown. Flatband voltage shift of hf C-V, $\Delta V_{FB} = (V_{FB}' - V_{FB}) > 0$ indicates negative charge trapping. For a film with defects, stretch-out of hf C-V, and offset in capacitance, ΔC, in between hf and lf C-V indicate the presence of interface traps.

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The central region of the C-V curve, where the capacitance changes rapidly with the gate voltage, is the depletion region that contributes to a depletion capacitance, $C_{depletion}$, further separating the effective capacitor plates and decreasing the device capacitance (as two capacitances in series reduce the overall capacitance). The depletion region starts at a voltage defined by the flatband voltage (V_{FB}). The effective value of capacitance is now given by Eq. 2. The capacitance decreases till the depletion width reaches a maximum and inversion sets in

$$C_{total} = \frac{C_{dielectric}\ C_{depletion}}{C_{dielectric} + C_{depletion}} \quad \text{(farads) [2]}$$

Inversion forms a layer of minority carriers (electrons in this case)—the so-called inversion layer. In the inversion region, the value of the capacitance depends on whether the measurement is conducted at low-frequency (0.01 to ~1 Hz) or at high-frequency (~1 MHz). When measured at high frequency, the charges are not able to follow the signal and the capacitance is clipped to the capacitance at maximum depletion width. The low-frequency capacitance includes the contribution from the minority carriers also and hence the capacitance increases. At strong inversion, the minority carriers become more significant and hence the capacitance is only due to the inversion capacitance.[2]

As shown in Fig. 2, the presence of negatively charged traps in the bulk dielectric and interface traps cause the high-frequency C-V plot to shift in parallel to the right of the ideal curve, and to stretch out along the bias axis, respectively. The shift in flatband voltage, $\Delta V_{FB} = V_{FB}' - V_{FB}$ is used in Eq. 3 to calculate the total trapped charge in the dielectric, Q_{tot}. Due to capacitance across the dielectric film, negative charge trapping in film translates to $\Delta V_{FB} > 0$, whereas for positive charge trapping, it is $\Delta V_{FB} < 0$

$$Q_{total} = C_{dielectric}\ \Delta V_{FB} \text{ (coulombs) [3]}$$

Interface traps also cause an offset in between low-frequency and high-frequency C-V plots (ΔC) as shown in Fig. 2. This offset can be utilized to calculate interface trap level density (D_{it}) from the measured high-frequency capacitance (C_{hf}) and low-frequency capacitance (C_{lf}) at a certain gate bias

$$D_{it} = \frac{C_{dielectric}}{q}\left(\frac{C_{lf}/C_{dielectric}}{1 - C_{lf}/C_{dielectric}} - \frac{C_{hf}/C_{dielectric}}{1 - C_{hf}/C_{dielectric}}\right)$$

(cm^{-2} eV^{-1}) [4]

Here, q is charge of an electron. D_{it} can be measured for different gate biases in the depletion regime.

The measurement of surface conductance also enables computation of the interface state density, D_{it}, especially for devices with low interface trap density. Difficulty arises in capacitance measurements because the interface-trap capacitance must be extracted from the measured capacitance that consists of oxide capacitance, depletion-layer capacitance, and interface-trap capacitance. While the capacitance and conductance as functions of voltage and frequency contain identical information about the interface, greater inaccuracies arise in extracting this information from the measured capacitance, because difference between two capacitances must be used. In the conductance method this difficulty does not apply as the measured conductance is directly related to the interface traps.[3-5]

Interface traps maintain electrical communication with the semiconductor substrate by capturing and emitting carriers (electrons/holes) depending on the gate bias, which induces a change of occupancy in them. If we keep a constant dc bias and simultaneously apply the ac test signal, a change of occupancy causes an energy loss, which depends on test signal frequency for the given dc bias. If frequency is too low, traps respond immediately; if too high, they do not respond at all. Energy loss, which is due to capture/emission of carriers by interface traps, and is represented by an equivalent conductance, G_p, of the MIS structure, is minimal in both the cases. However, in the low frequency range, for a given bias if frequency is increased gradually, energy loss increases as more interface traps respond with a time lag. If the frequency is increased further, it starts to decrease as fewer traps respond. Maximum energy loss occurs when most of the interface traps respond. So, G_p, measured over a wide range of frequencies and gate voltages, is a measure of D_{it} with respect to gate bias.

An equivalent circuit as shown in Fig. 3a represents a MIS structure with interface traps. Here, R_{it} represents the energy loss due to interface traps, while C_{it} represents the capacitance due to charge stored in those traps. Formation of a depletion region, whose capacitance is represented by C_D, takes place along with interaction of semiconductor carriers with interface traps. Hence, C_D is shown in parallel with the series combination of C_{it} and R_{it}. Storage of charge across the dielectric material occurs in addition to that in the depletion region and at the interface traps. Thus $C_{dielectric}$ remains in series with the network mentioned above. A simplified circuit (Fig. 3b) contains the parallel combination of equivalent conductance, G_p, and capacitance, C_p, which can be derived from the parallel network of Fig. 3a. The measured parallel conductance, G_m, and capacitance, C_m, are also indicated (Fig. 3c) across the two-terminal MIS structure using conventional measurement instruments (*e.g.*, a LCR meter). To find G_p from the measured data, the following equation is used

$$G_p/\omega = \frac{\omega G_m C_{dielectric}^2}{G_m^2 + \omega^2 (C_{dielectric} - C_m)^2}$$

(F/cm^2) [5]

where $\omega = 2\pi f$ is the radian frequency. G_p is estimated as a function of both gate bias and frequency, especially in the depletion regime, and G_p/ω *vs.* log(f) is plotted for each gate bias (Fig. 4). D_{it} can be calculated from the highest peak of G_p/ω *vs.* log(f) plots using Eq. 6

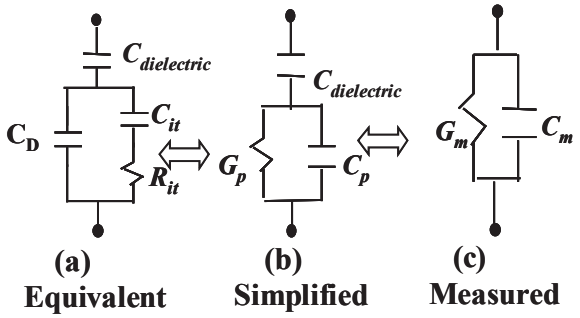


*FIG. 3. (a) Equivalent circuit for MIS structures with interface traps. R_{it} and C_{it} represent interface traps induced energy loss and charge storage respectively. (b) Simplified circuit, derived from (a), for analysis. Equivalent conductance, G_p, is computed from measured data as a function of both test (ac) signal frequency and gate bias (dc). (c) Circuit representing parallel capacitance (C_m) and conductance (G_m), which is measured across two-terminal MIS structures for different frequencies and biases using conventional instruments (*e.g., *LCR meter).*

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$$D_{it} = \frac{2.5}{q}\left(\frac{G_p}{\omega}\right)_{max} \quad (cm^{-2}\ eV^{-1})\ [6]$$

The leakage current through the dielectric material can be measured by varying the gate bias. For ultrathin films significant leakage current occurs via quantum mechanical tunneling of electrons from cathode to anode under the electric field across the dielectric, $E_{dielectric} = (V_G - V_{FB})/t_{dielectric}$, where $t_{dielectric}$ is film thickness. Defects in the films may also assist in tunneling, which is more pronounced for low gate bias values. Thus leakage current flow at low bias is a good indication of presence of defects in dielectric films.

In summary, the MIS device structure seems to be ideal for electrical characterization of dielectric films. Parameters like the dielectric constant can be measured and pre-existing defects can be quantified in the dielectric bulk and at the semiconductor/dielectric interface. The measurement techniques described above are quite versatile for the characterization of a wide range of dielectric materials used not only in the electronics industry but also in other disciplines. ■

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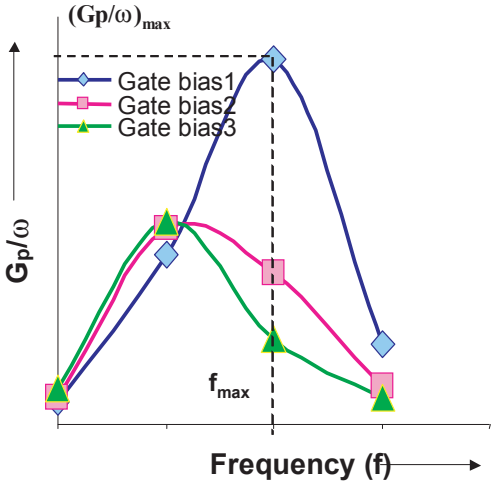


FIG. 4. G_p/ω vs. log(f) plots for different gate biases in the depletion regime. D_{it} is computed from the highest peak of the plots.

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