

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC. and
MICRON SEMICONDUCTOR PRODUCTS, INC.,

Petitioner

v.

PALISADE TECHNOLOGIES, LLP,
Patent Owner.

Case No. IPR2025-01559
U.S. Patent No. 9,524,974

PETITIONER'S UPDATED LIST OF EXHIBITS

LIST OF EXHIBITS¹

Ex-1001	U.S. Patent No. 9,524,974 (“the ’974 Patent”)
Ex-1002	Declaration of Dr. David Kuan-Yu Liu
Ex-1003	Curriculum Vitae of Dr. David Kuan-Yu Liu
Ex-1004	Prosecution History of U.S. Patent No. 9,524,974 (App. No. 14/806,111)
Ex-1005	U.S. Patent No. 8,592,978 (“Matsuno”)
Ex-1006	U.S. Patent App. Pub. No. 2015/0162277 (“Zhang”)
Ex-1007	U.S. Patent No. U.S. Patent No. 6,500,765 (“Kao”)
Ex-1008	U.S. Patent App. Pub. No. 2011/0032763 (“Kwak”)
Ex-1009	[Intentionally left blank]
Ex-1010	[Intentionally left blank]
Ex-1011	[Intentionally left blank]
Ex-1012	[Intentionally left blank]
Ex-1013	[Intentionally left blank]
Ex-1014	[Intentionally left blank]
Ex-1015	[Intentionally left blank]
Ex-1016	[Intentionally left blank]
Ex-1017	[Intentionally left blank]
Ex-1018	[Intentionally left blank]
Ex-1019	[Intentionally left blank]
Ex-1020	Claim Mapping Table
Ex-1021	Rino Micheloni et al., Inside NAND Flash Memories (2010)
Ex-1022	Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Oct. 16, 2024)
Ex-1023	First Amended Complaint, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Dec. 19, 2024)
Ex-1024	Second Amended Complaint (Redacted Version), <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Jul. 28, 2025)
Ex-1025	Paul Zimmerman, <i>Double patterning lithography: double the trouble</i>

¹ Four-digit pin citations that begin with 0 are the page stamps added by Micron in the bottom right corner of the exhibits. All other pin citations are to original page, column, paragraph, or line numbers.

	<i>or double the fun?</i> , SPIE Newsroom (July 20, 2009)
Ex-1026	U.S. Patent No. 6,204,200
Ex-1027	Christopher Bencher, et al., <i>22nm Half-Pitch Patterning by CVD Spacer Self Alignment Double Patterning (SADP)</i> , Optical Microlithography XXI (2008)
Ex-1028	Seiichi Aritome, NAND Flash Memory Technologies (2016)
Ex-1029	U.S. Patent No. 9,123,776
Ex-1030	U.S. Patent No. 9,595,477
Ex-1031	U.S. Patent App. Pub. No. 2008/0014760 (“Murata”)
Ex-1032	Mincheol Park et al., <i>Effect of low-k dielectric material on 63nm MLC (multi-level cell) NAND flash cell arrays</i> , IEEE VLSI-TSA International Symposium on VLSI Technology 37 (2005)
Ex-1033	Daewoong Kang et al., <i>The Air Spacer Technology for Improving the Cell Distribution in 1 Giga Bit NAND Flash Memory</i> , 21st IEEE Non-Volatile Semiconductor Memory Workshop (2006)
Ex-1034	Jiyoung Kim, et al., <i>A stacked memory device on logic 3D technology for ultra-high-density data storage</i> , Nanotechnology 22 (2011)
Ex-1035	T. Kundu, et al., <i>Electrical Techniques for the Characterization of Dielectric Films</i> , The Electrochemical Society Interface 14 (Sept. 2005)
Ex-1036	U.S. Patent No. 5,707,901
Ex-1037	David Abercrombie, <i>Self-Aligned Double Patterning, Part One</i> , Siemens Digital Industries Software Blog (Jan. 27, 2015)
Ex-1038	LayWai Kong, et al., <i>3D-interconnect: Visualization of extrusion and voids induced in copper-filled through-silicon vias (TSVs) at various temperatures using X-ray microscopy</i> , Microelectric Engineering 24 (2012)
Ex-1039	Sean King, <i>Dielectric Barrier, Etch Stop, and Metal Capping Materials for State of the Art and beyond Metal Interconnects</i> , ECS J. Solid State Sci. & Tech. N3029 (2015)
Ex-1040	Claim Construction Order, <i>Palisade Techs, LLP v. Micron Tech., Inc. and Micron Semiconductor Prods., Inc.</i> , No. 7:24-cv-00262 (W.D. Tex. Oct. 3, 2025)
Ex-1041	Proposed Protective Order
Ex-1042	Search Disclosure Declaration

Respectfully submitted,

/s/ John Kappos

John Kappos (Reg. No. 37,861)
O'Melveny & Myers LLP
2801 North Harwood Street, Suite 1600
Dallas, TX 75201
Telephone: (972) 360-1900
Fax: (972) 360-1901
E-Mail: jkappos@omm.com
Attorney for Petitioner

CERTIFICATE OF SERVICE

I hereby certify that on November 26, 2025, I caused a true and correct copy of the foregoing PETITIONER'S UPDATED LIST OF EXHIBIT was served in its entirety by filing these documents through the PTAB P-TACTS System, as well as by email, on the counsel of record for the Patent Owner:

David T. DeZern
Registration No. 60,117
NELSON BUMGARDNER CONROY
P.C.
2727 N. Harwood Street, Suite 250
Dallas, Texas 75201
Telephone: 214.446-4950
Email: david@nelbum.com
Email: Palisade@nelbum.com

Justin B. Kimble
Registration No. 58,591
NELSON BUMGARDNER CONROY
P.C.
2727 N. Harwood Street, Suite 250
Dallas, Texas 75201
Telephone: 214.446-4950
Email: justin@nelbum.com

Dated: November 26, 2025

Respectfully submitted,

/s/ John Kappos

John Kappos (Reg. No. 37,861)
O'Melveny & Myers LLP
2801 North Harwood Street, Suite 1600
Dallas, TX 75201
Telephone: (972) 360-1900
Fax: (972) 360-1901
E-Mail: jkappos@omm.com
Attorney for Petitioner