

ABSTRACT OF THE DISCLOSURE

A data storage device includes a memory having a three-dimensional (3D) memory configuration. The memory includes a structure that extends through multiple layers of the memory. A method includes storing information at the data storage device. The information identifies a location associated with a variation of the structure. The method further includes accessing the information.

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STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

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CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is related to U.S. Patent Application No. _____, filed concurrently herewith and entitled “ERROR CORRECTING CODE TECHNIQUES FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION” (Attorney Docket No. SDA-2116-US), and is further related to U.S. Patent Application No. _____, filed concurrently herewith and entitled “MEMORY ACCESS TECHNIQUES FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION” (Attorney Docket No. SDA-2118-US), each disclosure of which is incorporated herein by reference in its entirety.

FIELD OF THE DISCLOSURE

[0002] The present disclosure is generally related to memories and more particularly to memories having a three-dimensional memory configuration.

BACKGROUND

[0003] Non-volatile data storage devices have enabled increased portability of data and software applications. For example, multi-level cell (MLC) storage elements of a flash memory device may each store multiple bits of data, enhancing data storage density as compared to single-level cell (SLC) flash memory devices. Consequently, flash memory devices enable users to store and access a large amount of data. As a number of bits stored per cell increases, bit errors in stored data typically increase. A data storage device may encode and decode data using an error correcting code (ECC) technique to correct certain bit errors in data. The ECC technique may utilize parity information that decreases data storage capacity for other information, such as user data.

[0004] To further increase data storage capacity, a memory may have a three-dimensional memory configuration. A three-dimensional memory may include multiple layers of storage elements that are “stacked” relative to a semiconductor substrate.

Depending on the particular implementation, each layer of a three-dimensional memory may operate similarly to a two-dimensional (or “planar”) memory. A three-dimensional memory fabrication process typically includes different fabrication steps than a two-dimensional memory fabrication process. For example, a three-dimensional memory fabrication process may connect layers of storage elements to form a column of storage elements.

SUMMARY

[0005] A data storage device may include a memory having a three-dimensional (3D) memory configuration. To fabricate the memory, multiple layers of storage elements may be formed on a substrate, and a region (e.g., a “memory hole”) may be etched through the multiple layers. The region may be filled (e.g., with a charge trap material and a channel material) to form a structure that connects layers of storage elements of the memory. Depending on the particular etch process and the number of layers formed on the substrate, the region may have a “tapered” profile. To illustrate, if the etch process begins at a “top” layer and etches down to reach a “bottom” layer, then the top layer may be subject to the etch process for a greater time duration than the bottom layer. Because more etching is performed to reach “down” to the bottom layer relative to the top layer, the region may have a variation, such as a “tapered” profile. As a result, a first portion of the structure that is nearer to the substrate may have a narrower width relative to a second portion of the structure that is farther from the substrate than the first portion. Such tapering can affect device performance, such as performance characteristics of storage elements connected to the structure.

[0006] The data storage device may include a controller that is configured to determine a location of the variation of the structure. The location may correspond to a portion of the structure where “tapering” of the structure begins. To illustrate, within a particular distance above the substrate of the memory, the structure may be approximately uniform in width. At a greater distance from the substrate, the structure may begin to “taper.” The controller may measure a first parameter associated with a first layer of storage elements and a second parameter associated with a second layer of storage elements. Based on a difference between the first parameter and the second

parameter, the controller may detect a variation between the first layer and the second layer (or that a “taper” effect occurs approximately at the location).

[0007] An error correcting code (ECC) parameter table may be determined based on the location of the variation. The ECC parameter table may indicate a first parameter associated with a first set of physical pages of storage elements formed below the location within the memory and may further indicate a second parameter associated with a second set of physical pages of storage elements formed above the location within the memory. The first parameter may indicate a first ECC technique associated with the first set of physical pages, and the second parameter may indicate a second ECC technique associated with the second set of physical pages. In an illustrative example, data stored at the first set of physical pages is encoded using a polynomial-based encoding technique, such as a Bose-Chaudhuri-Hocquenghem (BCH) encoding technique. Data stored at the second set of physical pages may be encoded using a probabilistic-based encoding technique, such as a low-density parity check (LDPC) encoding technique or a turbo encoding technique.

[0008] Alternatively or in addition to the ECC parameter table, a memory access parameter table may be determined based on the location of the variation. The memory access parameter table may specify write parameters and/or read parameters for accessing the memory. To illustrate, the memory access parameter table may indicate a first parameter associated with a first set of physical pages of storage elements formed below the location within the memory and may further indicate a second parameter associated with a second set of physical pages of storage elements formed above the location within the memory. In an illustrative example, data stored at the first set of physical pages is programmed using a first programming voltage indicated by the first parameter. Data stored at the second set of physical pages may be programmed using a second programming voltage indicated by the second parameter. Alternatively or in addition, the first parameter and the second parameter may indicate a number of programming pulses, a duration of the programming pulses, another write parameter, a read parameter (e.g., a read voltage), or a combination thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] FIG. 1 is a block diagram of a particular illustrative embodiment of a system including a data storage device that includes a memory having a three-dimensional memory configuration;

[0010] FIGs. 2-5 illustrate example structures that can be implemented within the memory of the data storage device of FIG. 1;

[0011] FIG. 6 illustrates a particular illustrative example of a table indicating locations of variations of a structure of the memory of the data storage device of FIG. 1;

[0012] FIGs. 7-15 are flow diagrams that illustrate particular illustrative embodiments of methods of operation of the data storage device of FIG. 1; and

[0013] FIGs. 16 and 17 are block diagrams of particular embodiments of the memory of the data storage device of FIG. 1.

DETAILED DESCRIPTION

[0014] Referring to FIG. 1, a particular illustrative embodiment of a system is depicted and generally designated 100. The system 100 includes a data storage device 102 and a host device 172. The data storage device 102 and the host device 172 may be coupled via a connection, such as a wireless connection or a bus. The data storage device 102 may be embedded within the host device 172, such as in accordance with a Joint Electron Devices Engineering Council (JEDEC) Solid State Technology Association Universal Flash Storage (UFS) configuration. Alternatively, the data storage device 102 may be removable from the host device 172 (i.e., “removably” coupled to the host device 172). As an example, the data storage device 102 may be removably coupled to the host device 172 in accordance with a removable universal serial bus (USB) configuration. In an illustrative implementation, the data storage device 102 corresponds to a solid-state drive (SSD) that is integrated within an electronic device, such as the host device 172.

[0015] The data storage device 102 may include a memory 104. The memory 104 may be a non-volatile memory, such as a NAND flash memory, as an illustrative

example. The memory 104 may have a multi-layer memory configuration, such as a three-dimensional (3D) memory configuration. As an illustrative example, the memory 104 may include one or more layers having a first orientation and may further include one or more elements, such as vertical columns, having a second orientation perpendicular to (or approximately perpendicular to) the first orientation to enable cross-layer coupling of storage elements of the one or more layers. In a particular implementation, the memory 104 is a non-volatile memory having a three-dimensional (3D) memory configuration that is monolithically formed in physical levels of arrays of memory cells having an active area disposed above a silicon substrate.

[0016] The memory 104 may include read/write circuitry 106, a physical page 108, and a physical page 118. The data storage device 102 includes circuitry that is associated with operation of memory cells of the memory 104. The circuitry may correspond to the read/write circuitry 106, as an illustrative, non-limiting example.

[0017] The physical pages 108, 118 may be included in a block (e.g., an erase group) of the memory 104. The memory 104 may include multiple blocks of physical pages, and each block may include multiple physical pages. Although FIG. 1 depicts that the memory 104 includes two physical pages (i.e., the physical pages 108, 118), it should be appreciated that the memory 104 may have another configuration. For example, the memory 104 may include another number of physical pages (e.g., more than two physical pages).

[0018] The physical pages 108, 118 may each be configured to store threshold voltages indicating one or more pages of data. To illustrate, one or more of the physical pages 108, 118 may correspond to a physical page of single-level cell (SLC) storage elements that can be programmed to store threshold voltages indicating bit values of a page, such as in connection with a one-bit-per-cell (“X1”) configuration. One or more of the physical pages 108, 118 may correspond to a physical page of multi-level cell (MLC) storage elements that can be programmed to store threshold voltages indicating bit values of multiple pages, such as in connection with a two-bit-per-cell (“X2”) configuration or a three-bit-per-cell (“X3”) configuration, as illustrative examples.

[0019] The data storage device 102 may further include a controller 130 that is operationally coupled to the memory 104. The memory 104 and the controller 130 may be operationally coupled via a connection, such as a bus. The memory 104 may be included on a memory die that is separate from the controller 130 and that is coupled to the controller 130. In one or more other implementations, the memory 104 and the controller 130 may be included on a common die. FIG. 1 illustrates that the controller 130 may include an error correcting code (ECC) engine 132, a location identifier 134, a random access memory (RAM) 144, a wear distributor 168, and a host interface 170.

[0020] The ECC engine 132 is configured to generate one or more ECC codewords using one or more ECC encoding techniques. The ECC engine 132 may include one or more encoders, such as a Reed-Solomon (RS) encoder, a Bose-Chaudhuri-Hocquenghem (BCH) encoder, a low-density parity check (LDPC) encoder, a turbo encoder, an encoder configured to encode data according to one or more other ECC techniques, or a combination thereof. The ECC engine 132 may include one or more decoders configured to decode data read from the memory 104 to detect and correct, up to an error correction capability of the ECC scheme, one or more bit errors that may be present in the data.

[0021] The location identifier 134 may include a power-up indicator 136. The location identifier 134 may determine one or more measurements, such as measurements 142. The measurements 142 may be stored at the controller 130, at the memory 104, at another location, or a combination thereof.

[0022] The controller 130 is configured to send data and commands to the memory 104 and to receive data from the memory 104. For example, the controller 130 is configured to send data and a write command to cause the memory 104 to store the data to a specified address of the memory 104. The controller 130 is configured to send a read command to read data from a specified address of the memory 104.

[0023] The data storage device 102 is configured to receive data and instructions from the host device 172 and to send data to the host device 172. For example, the controller 130 may send data to the host device 172 via the host interface 170 and may receive data from the host device 172 via the host interface 170.

[0024] The host device 172 may correspond to a mobile telephone, a computer (e.g., a laptop, a tablet, or a notebook computer), a music player, a video player, a gaming device or console, an electronic book reader, a personal digital assistant (PDA), a portable navigation device, another electronic device, or a combination thereof. The host device 172 may communicate via a host controller, which may enable the host device 172 to communicate with the data storage device 102. The host device 172 may operate in compliance with a JEDEC Solid State Technology Association industry specification, such as an embedded MultiMedia Card (eMMC) specification or a Universal Flash Storage (UFS) Host Controller Interface specification. The host device 172 may operate in compliance with one or more other specifications, such as a Secure Digital (SD) Host Controller specification, as an illustrative example. Alternatively, the host device 172 may communicate with the data storage device 102 using another communication protocol.

[0025] During a first mode of operation of the data storage device 102, the controller 130 may be configured to determine a location associated with a variation of a structure that extends through multiple layers of the memory 104. The structure may include a channel region and a charge trap region that are formed within an etched region (e.g., a “memory hole”). The structure may extend through multiple layers of the memory 104 to connect physical pages of the memory 104, such as the physical pages 108, 118. The variation may correspond to a “tapering” of the structure, as described further with reference to FIGs. 2-5. In the example of FIG. 1, a location 116 is associated with a variation of a structure that extends through multiple layers of the memory 104. The location 116 may correspond to a distance within the memory 104 from a surface of a substrate of the memory 104 (i.e., the distance may define the location 116 because the location 116 is separated from the surface of the substrate by the distance).

[0026] The location identifier 134 may determine the location 116 by measuring a first parameter at the physical page 118 and by measuring a second parameter at the physical page 108. To illustrate, the location identifier 134 may send one or more control signals to the read/write circuitry 106 to cause the read/write circuitry 106 to program a first storage element of the physical page 118 to a particular state and to

cause the read/write circuitry 106 to program a second storage element of the physical page 108 to the particular state, such as a particular threshold voltage. The particular state may correspond to an “A” state (e.g., a threshold voltage indicating one or more bit values, such as a “0” bit value), as an illustrative example. The particular state may correspond to a “B” state or a “C” state (e.g., a first threshold voltage indicating a first bit sequence or a second threshold voltage indicating a second bit sequence) in connection with an illustrative MLC implementation, as additional illustrative examples.

[0027] The location identifier 134 may be responsive to the read/write circuitry 106 to determine the first parameter and the second parameter. For example, the location identifier 134 may be configured to determine a first number of programming pulses used by the read/write circuitry 106 to program the first storage element to the particular state and further to determine a second number of programming pulses used by the read/write circuitry 106 to program the second storage element to the particular state. In this example, the first parameter indicates the first number of programming pulses, and the second parameter indicates the second number of programming pulses. Alternatively or in addition, the first parameter and the second parameter may indicate one or more other parameters (e.g., a programming voltage of the programming pulses, a pulse duration (or “width”) of the programming pulses, another parameter, or a combination thereof).

[0028] The location identifier 134 may compare the first parameter and the second parameter. For example, the location identifier 134 may determine a difference between the first parameter and the second parameter, such as by subtracting the first parameter from the second parameter. If the difference between the first parameter and the second parameter exceeds a threshold, the location identifier 134 may detect a variation of a structure that connects physical pages. In the example of FIG. 1, the variation is between the physical pages 108, 118 (i.e., at the location 116). The location identifier 134 may detect the variation during testing of the memory 104 (e.g., “at the factory”), as an illustrative example.

[0029] To further illustrate, in a particular embodiment, the location identifier 134 identifies the location 116 in response to an initial power-up of the data storage device.

As an illustrative example, the controller 130 may access the power-up indicator 136 in response to each power-up of the data storage device 102. In a particular embodiment, the data storage device 102 includes a power-up detector (not shown in FIG. 1) that is configured to detect that power is being received at the data storage device 102 (e.g., from the host device 172).

[0030] A first value of the power-up indicator 136 may indicate that the data storage device 102 has not been previously powered up (i.e., the current power-up is an initial power-up of the data storage device 102). In this case, the controller 130 may perform operations to determine (or attempt to determine) one or more locations of variations of structures extending through multiple layers of the memory 104. After performing the operations (e.g., after determining the location 116), the controller 130 may adjust the power-up indicator 136 from the first value to a second value to indicate that the data storage device has been powered up. Although the example of FIG. 1 illustrates that the power-up indicator 136 is stored at the location identifier 134, it should be appreciated that the power-up indicator 136 may be stored at another location, such as at the memory 104.

[0031] In response to determining the location 116, the controller 130 may generate information 146 that indicates the location 116. The information 146 may be stored (e.g., cached) at the RAM 144, as illustrated in FIG. 1. Alternatively or in addition, the information 146 may be stored at the memory 104. As described further with reference to FIG. 6, the information 146 may correspond to a table. In a particular illustrative embodiment, the controller 130 is configured to utilize the information 146 to determine one or more operating parameters for the memory 104. For example, the controller 130 may assign one or more sets of parameters to the physical page 108 and may assign one or more sets of parameters to the physical page 118.

[0032] To further illustrate, the controller 130 may generate an ECC parameter table 148 in response to determining the location 116. The ECC parameter table 148 may assign a parameter 150 to one or more physical pages, such as the physical page 118, of the memory 104 that are located below the location 116 relative to a substrate of the memory 104. As another example, the controller 130 may assign a parameter 152 to one or more physical pages, such as the physical page 108, of the memory 104 that are

disposed above the location 116 relative to the substrate. The ECC engine 132 may operate in accordance with the parameters 150, 152. For example, the parameter 150 may specify a first encoding technique for encoding data to be stored at the physical page 118, and the parameter 152 may specify a second encoding technique for data to be stored at the physical page 108. In an illustrative embodiment, the controller 130 is configured to generate the ECC parameter table 148 in response to an initial power-up of the data storage device 102.

[0033] As another example, the controller 130 may generate a memory access parameter table 154 in response to determining the location 116. The memory access parameter table 154 may indicate one or more memory access parameters. For example, the memory access parameter table 154 may indicate one or more parameters for writing data to the memory 104 by the read/write circuitry 106, one or more parameters for sensing data from the memory 104 by the read/write circuitry 106, or a combination thereof.

[0034] To illustrate, the memory access parameter table 154 may include a write parameter table that specifies a parameter 156 for writing data to physical pages of the memory 104 that are disposed below the location 116 relative to the substrate of the memory 104. The write parameter table may further indicate a parameter 158 associated with physical pages of the memory 104 that are disposed above the location 116 relative to the substrate. For example, the parameter 156 may be associated with the physical page 118, and the parameter 158 may be associated with the physical page 108. In a particular embodiment, the parameter 156 indicates a write voltage for writing data to physical pages of the memory 104 that are disposed below the location 116, and the parameter 158 indicates a second write voltage for writing data to physical pages located above the location 116. In an illustrative embodiment, the controller 130 is configured to generate the write parameter table in response to an initial power-up of the data storage device 102.

[0035] Alternatively or in addition, the memory access parameter table 154 may indicate a read parameter table. In this case, the parameter 156 (or another parameter) may indicate a read parameter associated with physical pages of the memory 104 that are disposed below the location 116 relative to the substrate of the memory 104. For

example, the parameter 156 may be associated with the physical page 118. The parameter 158 (or another parameter) may indicate a read parameter associated with physical pages of the memory 104 that are disposed above the location 116 relative to the substrate of the memory 104. For example, the parameter 158 may be associated with the physical page 108. In an illustrative embodiment, the controller 130 is configured to generate the read parameter table in response to an initial power-up of the data storage device 102.

[0036] During a second mode of operation of the data storage device 102, data may be written to and accessed from the memory 104 using the information 146, the ECC parameter table 148, the memory access parameter table 154, or a combination thereof. The controller 130 may receive data from the host device 172 to be stored at the memory 104. For example, the controller 130 may receive a first request for write access to the memory 104 from the host device 172. The first request may include first data to be stored at the memory 104. After receiving the first request from the host device 172, the controller 130 may receive a second request for write access to the memory 104 from the host device 172. The second request may include second data to be stored at the memory 104. In this case, the first data may correspond to a first file (e.g., an audio file, an image file, a video file, or another file), and the second data may correspond to a second file. In another example, the first data and the second data may be included in a single request received from the host device 172, and the first data and the second data may correspond to a single file to be stored at the memory 104.

[0037] In response to receiving data from the host device 172, the controller 130 may access a logical-to-physical address mapping table 166 to determine physical pages of the memory 104 at which to store the data. As a particular example, the controller 130 may access the logical-to-physical address mapping table 166 to determine a first physical address of the memory 104 associated with the first data received from the host device 172. The controller 130 may access the logical-to-physical address mapping table 166 to determine a second physical address of the memory 104 associated with the second data received from the host device 172. In an illustrative example, the first physical address corresponds to the physical page 118, and the second physical address corresponds to the physical page 108.

[0038] After accessing the logical-to-physical address mapping table 166, the controller 130 may access the ECC parameter table 148 to determine one or more encoding techniques to encode the first data and the second data. For example, if the controller 130 receives first data that is to be stored at the physical page 118, the controller 130 may access the ECC parameter table 148 to determine that the parameter 150 indicates that the first data is to be encoded using a first encoding technique. As another example, the controller 130 may access the ECC parameter table 148 to determine that second data to be stored at the physical page 108 is to be encoded using a second encoding technique that is different than the first encoding technique. In an illustrative embodiment, the first encoding technique is associated with a lower complexity and/or a higher code rate than the second encoding technique. To illustrate, the first encoding technique may be a polynomial-based encoding technique, such as a BCH encoding technique. The second encoding technique may be a probabilistic-based encoding technique, such as an LDPC encoding technique or a turbo code encoding technique, as illustrative examples. A BCH technique may have lower decoding complexity and faster decoding operation compared to an LDPC technique and a turbo code technique and may be advantageous for data with lower error rates. An LDPC technique or turbo code technique may have higher error correction capability relative to a BCH technique and may be advantageous for data with higher error rates. It should be appreciated that the particular ECC schemes (e.g., BCH, LDPC, turbo code, etc.) are provided for illustration and that the particular ECC scheme may be selected based on the application.

[0039] The controller 130 may selectively adjust the ECC engine 132 to encode the first data using the first encoding technique and may selectively adjust the ECC engine 132 to encode the second data using the second encoding technique. To illustrate, in some implementations, the ECC engine 132 includes multiple encoders including a first encoder and a second encoder. The first encoder may be configured to encode data using a polynomial-based encoding technique, and the second encoder may be configured to encode data using a probabilistic-based encoding technique. The first encoder may be configured to encode data using a BCH encoding technique, and the second encoder may be configured to encode data using an LDPC encoding technique or a turbo code encoding technique, as illustrative examples.

[0040] The controller 130 may selectively input the first data to the first encoder and the second data to the second encoder. In this example, the controller 130 may selectively activate and deactivate the first encoder and the second encoder. For example, the second encoder may be deactivated (e.g., powered down) while the first encoder encodes the first data, and the first encoder may be deactivated (e.g., powered down) while the second encoder encodes the second data.

[0041] In one or more other implementations, the ECC engine 132 may include a common encoder configured to selectively encode data using the first encoding technique or the second encoding technique. To illustrate, the controller 130 may send an encoder enable signal to the ECC engine 132 to adjust a mode of operation of the common encoder from the first encoding technique to the second encoding technique (or vice versa). A first value of the encoder enable signal may select the first encoding technique, and a second value of the encoder enable signal may select the second encoding technique.

[0042] The controller 130 may input the first data to the ECC engine 132. The ECC engine 132 may encode the first data using the first encoding technique to generate an ECC codeword 120. The controller 130 may further input the second data to the ECC engine 132. The ECC engine 132 may encode the second data using the second encoding technique to generate an ECC codeword 110.

[0043] The ECC codeword 120 may include data 122 (e.g., the first data), ECC bits 124, and a portion 126. The ECC codeword 110 may include data 112 (e.g., the second data) and ECC bits 114. The ECC codeword 120 may be stored at the physical page 118, and the ECC codeword 110 may be stored at the physical page 108. The ECC bits 114, 124 may include parity bits to enable the ECC engine 132 to correct one or more bit errors in the data 112, 122. Although the example of FIG. 1 illustrates that the ECC codewords 110, 120 include separate groups of data and ECC bits for purposes of illustration, it should be appreciated that a particular ECC scheme may generate an ECC codeword that does not include separate groups of data and ECC bits.

[0044] In a particular embodiment, “short” ECC codewords having a first number of ECC bits are stored to physical pages of the memory 104 that are below the location

116, and “extended” ECC codewords having a second number of ECC bits are stored to physical pages of the memory 104 that are above the location 116. In this example, the second number of ECC bits is greater than the first number of ECC bits, such as to compensate for reduced data reliability caused by a “taper” effect associated with physical pages above the location 116. As a non-limiting, illustrative example, the first number may correspond to 100 bytes, and the second number may correspond to 200 bytes. In the example of FIG. 1, the portion 126 may include a “padded” portion (e.g., zero-padded portion) that accounts for the “unused” ECC portion of the ECC codeword 120. To further illustrate using the foregoing example, the ECC bits 114 may include 200 bytes, the ECC bits 124 may include 100 bytes, and the portion 126 may include 100 bytes of non-ECC bits (e.g., a sequence of zero bits). Alternatively, the portion 126 may store other information. For example, the portion 126 may store measurements generated by the location identifier 134 (e.g., the measurements 142), other information, or a combination thereof.

[0045] Alternatively or in addition to using the ECC parameter table 148, the data storage device 102 may write data to the memory 104 based on a write parameter table indicated by the memory access parameter table 154. For example, the read/write circuitry 106 may write the ECC codeword 120 to the physical page 118 based on the parameter 156, and the read/write circuitry 106 may write the ECC codeword 110 to the physical page 108 based on the parameter 158. Depending on the particular implementation, one or both of the parameters 156, 158 may indicate a number of programming pulses, a pulse duration (or “width”) of the programming pulses, a programming voltage of the programming pulses, or a combination thereof. To illustrate, the second number of programming pulses may be greater than the first number of programming pulses to compensate for a variation of a structure occurring at the location 116 that causes threshold voltages programmed above the location 116 using a certain number of programming pulses to be less than threshold voltages programmed below the location 116 using the number of programming pulses.

[0046] Alternatively or in addition, the data storage device 102 may be configured to sense data using the memory access parameter table 154, such as in response to receiving one or more requests for read access from the host device 172 for data stored

at the memory 104. To further illustrate, the controller 130 may receive a first request for read access to the memory 104 from the host device 172. The first request may indicate that the data 122 is to be accessed from the memory 104. The first request may indicate a first logical address associated with the data 122. After receiving the first request from the host device 172, the controller 130 may receive a second request for read access to the memory 104 from the host device 172. The second request may indicate that the data 112 is to be accessed from the memory 104. The second request may indicate a second logical address associated with the data 112. Alternatively, the host device 172 may send a single request to the controller 130 requesting read access to the data 112, 122.

[0047] The controller 130 may access the logical-to-physical address mapping table 166 to determine physical addresses associated with the data 112, 122. For example, the controller 130 may access the logical-to-physical address mapping table 166 to identify a first physical address of the physical page 108 based on the first logical address and to further identify a second physical address of the physical page 118 based on the second logical address.

[0048] The data storage device 102 may be configured to access the ECC codewords 110, 120 from the physical pages 108, 118 based on one or more read parameters indicated by the memory access parameter table 154. For example, the read/write circuitry 106 may be responsive to the controller 130 to sense the physical page 118 using a first read voltage indicated by the parameter 156. As another example, the read/write circuitry 106 may be responsive to the controller 130 to access the physical page 108 using a second read voltage indicated by the parameter 158. In a particular embodiment, the parameter 156 indicates a first set of threshold voltages for sensing data from physical pages below the location 116 (e.g., the physical page 108). The parameter 158 may indicate a second set of threshold voltages for sensing data from physical pages above the location 116 (e.g., the physical page 118). To illustrate, the second set of threshold voltages may be different than the first set of threshold voltages to compensate for a variation of a structure occurring at the location 116 that causes threshold voltages programmed above the location 116 using a particular number of programming pulses to be less than threshold voltages programmed below the location

116 using the number of programming pulses. In this example, distributions of threshold voltages stored at the physical page 108 may be different than (e.g., less than) distributions of threshold voltages stored at the physical page 118, resulting in read levels that do not “align” with distributions of threshold voltages actually stored at the physical page 108 (and potentially resulting in a high error rate of read data). By adjusting read voltages of the read/write circuitry 106 based on the location 116, read performance is improved by sensing storage elements of the physical page 108 using read levels that are more closely based on (e.g., “matched” to) threshold voltages stored at the physical page 108.

[0049] The controller 130 may access the ECC parameter table 148 to determine one or more encoding techniques to decode the data 112, 122. For example, the controller 130 may access the parameter 150 to determine that the ECC codeword 120 is encoded using a first encoding technique and/or that the ECC codeword 120 is to be decoded using a first decoding technique that corresponds to the first encoding technique. As another example, the controller 130 may access the parameter 152 to determine that the ECC codeword 110 is encoded using a second encoding technique and/or that the ECC codeword 110 is to be decoded using a second decoding technique that corresponds to the second encoding technique. The first decoding technique may be a polynomial-based decoding technique, such as a BCH-based decoding technique. The second decoding technique may be a probabilistic-based decoding technique, such as an LDPC-based decoding technique or a turbo code-based decoding technique, as illustrative examples. The second decoding technique may be an iterative decoding technique. For example, an LDPC-based decoding technique may include iteratively updating check nodes and variable nodes at the ECC engine 132.

[0050] The controller 130 may selectively adjust the ECC engine 132 to decode the ECC codeword 120 using the first decoding technique to decode the ECC codeword 110 using the second decoding technique. To illustrate, in some implementations, the ECC engine 132 includes multiple decoders including a first decoder and a second decoder. The first decoder may be configured to decode data using a polynomial-based decoding technique, and the second decoder may be configured to decode data using a probabilistic-based decoding technique. The first decoder may be configured to decode

data using a BCH-based decoding technique, and the second decoder may be configured to decode data using an LDPC-based decoding technique or a turbo code-based decoding technique, as illustrative examples.

[0051] The controller 130 may selectively input the ECC codeword 120 to the first decoder and the ECC codeword 110 to the second decoder. In this example, the controller 130 may selectively activate and deactivate the first decoder and the second decoder. For example, the second decoder may be deactivated (e.g., powered down) while the first decoder decodes the ECC codeword 120, and the first decoder may be deactivated (e.g., powered down) while the second decoder decodes the ECC codeword 110.

[0052] In one or more other implementations, the ECC engine 132 may include a common decoder configured to selectively decode an ECC codeword using the first decoding technique or the second decoding technique. To illustrate, the controller 130 may send a decoder enable signal to the ECC engine 132 to change a mode of operation of the common decoder from the first decoding technique to the second decoding technique (or vice versa). A first value of the decoder enable signal may select the first decoding technique, and a second value of the decoder enable signal may select the second decoding technique.

[0053] The ECC engine 132 may decode the ECC codewords 110, 120 using the ECC bits 114, 124 to detect and correct, up to an error correction capability of the one or more decoding techniques, one or more bit errors that may be present in the data 112, 122. The controller 130 may send the data 112, 122 to the host device 172 via the host interface 170.

[0054] The example techniques described with respect to FIG. 1 enable improved accuracy of ECC operations (e.g., encoding and decoding operations) and/or memory access operations (e.g., read and write operations) at the data storage device 102. For example, by selectively performing encoding operations, write operations, read operations, and/or decoding operations at the data storage device 102 based on the location 116, the data storage device 102 may compensate for one or more effects of a

variation of a structure that is connected to the physical pages 108, 118. FIG. 2 describes an example variation of a structure.

[0055] Referring to FIG. 2, a particular illustrative embodiment of a column is depicted and generally designated 200. The column 200 may be integrated within a memory having a three-dimensional (3D) memory configuration. For example, the column 200 may be integrated within the memory 104 of FIG. 1.

[0056] The column 200 includes storage elements formed within multiple layers of materials that are formed on a substrate 208 (e.g., a silicon substrate). To illustrate, FIG. 2 depicts a layer 210, a layer 212, and a layer 214. The layer 210 may be formed adjacent to the substrate 208 (i.e., the layer 210 may be a “bottom” layer). The layer 212 may be adjacent to the layer 210. The layer 214 may be farther from the substrate than other layers of the column 200 (i.e., the layer 214 may be a “top” layer). The layers 210, 212, and 214 may include a conductive (or semiconductive) material, such as doped polysilicon, as an illustrative, non-limiting example. The column 200 may include other layers, such as an oxide layer interposed between the layers 210, 212, as an illustrative example.

[0057] The column 200 may further include a structure 202. To form the structure 202, an etch process may be performed to etch through layers of the column 200 to form an etched region (e.g., a cavity, such as a “memory hole”). After etching through layers of the column 200 to form the etched region, the etched region may be filled with one or more materials to form the structure 202. The structure 202 may have a circular or substantially circular shape (e.g., a cross section of the structure 202 that is perpendicular to a surface of the substrate 208 may be circular).

[0058] The column 200 may further include multiple storage elements, such as a storage element 204 and a storage element 206. The storage element 204 may be included in the physical page 108 of FIG. 1, and the storage element 206 may be included in the physical page 118 of FIG. 1. The storage elements 204, 206 are connected to the structure 202.

[0059] The structure 202 may have a variation. For example, as illustrated in the example of FIG. 2, the structure 202 may have a “conical” or “tapered” profile. The

location 116 may indicate a region of the structure 202 associated with tapering of the structure 202. For example, in the example of FIG. 2, the structure 202 is not tapered below the location 116 (i.e., nearer to the substrate 208 than the location 116) and the structure 202 is tapered above the location 116 (i.e., farther from the substrate than the location 116). In the example of FIG. 2, the location 116 is between the storage elements 204, 206 because the structure 202 begins “tapering” approximately between the storage elements 204, 206.

[0060] By identifying the location 116, accuracy of operations at the data storage device 102 can be improved. For example, by identifying the location 116, the storage elements 204, 206 may be associated with different ECC parameters and/or different memory access parameters to compensate for differences in physical characteristics of the storage elements 204, 206 due to tapering of the structure 202. Differences in physical characteristics of storage elements are described further with reference to FIG. 3.

[0061] Referring to FIG. 3, a particular illustrative embodiment of a portion of the column 200 is depicted and generally designated 300. The portion 300 illustrates that a charge trap structure 304 and a conductive channel 306 may be formed within the structure 202. A control gate 302 and a control gate 310 may be connected to the charge trap structure 304. The control gate 302 may be included in the storage element 204 of FIG. 2, and the control gate 310 may be included in the storage element 206 of FIG. 2. The control gates 302, 310 may be separated by a material, such as an oxide region 308.

[0062] The control gates 302, 310 and the oxide region 308 may be formed within multiple layers of the memory 104. For example, the control gate 302 may be formed within a layer that includes polysilicon, the oxide region 308 may be formed within a layer that includes oxide, and the control gate 310 may be formed within another layer that includes polysilicon. The control gates 302, 310 and the oxide region 308 may be formed within one or more “physical layers” of the memory 104. For example, a physical layer may include the control gate 302 and the oxide region 308.

[0063] It should be appreciated that one or more additional materials may be formed within the structure 202. To illustrate, the charge trap structure 304 may be separated from the control gate 302 and the conductive channel 306 by a gate dielectric, such as a silicon oxide, as an illustrative example. The charge trap structure 304 may include an insulating material, such as silicon nitride, as an illustrative example. The channel may include a conductive material, such as a metal (e.g., copper), as an illustrative example.

[0064] The portion 300 may be biased to write a value to the storage element 204 and to sense a value stored at the storage element 204. The portion 300 may be biased to write a value to the storage element 206 and to sense a value stored at the storage element 206. To illustrate, charge may be injected into or drained from the charge trap structure 304 by biasing the control gate 302 relative to the conductive channel 306. In this example, an amount of charge in the charge trap structure 304 affects an amount of current through the conductive channel 306 during a read operation of the storage element 204 and indicates one or more bit values that may be stored in the storage element 204. As another example, charge may be injected into or drained from the charge trap structure 304 by biasing the control gate 310 relative to the conductive channel 306. In this example, an amount of charge in the charge trap structure 304 affects an amount of current through the conductive channel 306 during a read operation of the storage element 206 and indicates a state of the storage element 206. The state of the storage element 206 may correspond to one or more bit values that are stored by the storage element 206.

[0065] FIG. 3 illustrates a variation (or “tapering”) associated with the structure 202. The variation may correspond to a difference between a first width of the structure at a first distance from the substrate 208 and a second width of the structure at a second distance from the substrate 208, where the second distance is greater than the first distance. To further illustrate, FIG. 3 illustrates that a variation associated with the structure 202 may affect a channel width 312 (e.g., radius) that is associated with the control gate 302. FIG. 3 further indicates that a channel width 314 (e.g., radius) associated with the control gate 310 may be less than the channel width 312 due to tapering of the structure 202. Because the channel width 314 is greater than the channel width 312, operation of the storage element 204 of FIG. 2 may differ from operation of

the storage element 206 of FIG. 2. For example, because the width of the conductive channel 306 affects an amount of current conducted by the structure 202, the difference between the channel widths 312, 314 may affect operation of a memory that includes the portion 300. Accordingly, biasing the control gate 302 with a voltage may cause the conductive channel 306 to conduct less current as compared to applying the voltage to the control gate 310. In this case, programming the storage elements 204, 206 using a common programming voltage may cause the storage elements 204, 206 to store different threshold voltages (because a greater programming voltage may be needed to activate the control gate 302 relative to the control gate 310), which may result in an “incorrect” state being programmed to the storage element 204. During a sense operation that senses a state of the storage element 204, a greater voltage (relative to the storage element 206) may be applied to the control gate 302 to cause conduction to occur from the control gate 302 to the conductive channel 306 (or for the storage element 204 to “turn on”). Therefore, a variation of the structure 202 may cause read operations of the storage element 204 to differ relative to the storage element 206. In this case, sensing the storage elements 204, 206 using a common read voltage may result in different states being sensed from the storage elements 204, 206 (because a greater read voltage may be needed to activate the control gate 302 relative to the control gate 310), which may result in an “incorrect” state being sensed from the storage element 204.

[0066] Alternatively or in addition, and depending on the particular implementation, a variation of the structure 202 may cause a gate-to-channel distance 316 associated with the storage element 204 to be greater than a gate-to-channel distance 318 associated with the storage element 206. In this case, the charge trap structure 304 may have a greater taper effect than the conductive channel 306. During a write operation that programs a state to the storage element 204, a greater voltage (relative to the storage element 206) may be applied to the control gate 302 to accumulate charge within the charge trap structure 304 (e.g., by drawing electrons from the conductive channel 306 to within the charge trap structure 304). Therefore, tapering of the structure 202 may cause programming operations of the storage element 204 to differ relative to the storage element 206, which may result in an “incorrect” state being programmed to and/or sensed from the storage element 204.

[0067] FIG. 3 illustrates that a variation (e.g., tapering) of a structure (e.g., the structure 202) extending through multiple layers of a memory (e.g., the memory 104) may affect read and write operations of the memory. Performance of a memory that includes the portion 300 may be improved by using different ECC techniques and/or memory access techniques for the storage elements 204, 206. For example, because a variation of the structure 202 occurs at the location 116, a first ECC technique and/or a first memory access technique may be associated with the storage element 206, and a second ECC technique and/or a second memory access technique may be associated with the storage element 204 to improve operation of the memory 104. The second ECC technique may compensate for a greater number of errors that may occur at the storage element 204 as compared to the storage element 206 due to “tapering” of the structure 202. For example, the second ECC technique may have a higher error correction capability than the first ECC technique, which may improve error correction. The second memory access technique may compensate for a greater number of write errors and/or read errors that may occur at the storage element 204 as compared to the storage element 206 due to “tapering” of the structure 202. For example, the second memory access technique may program the storage element 204 using a different programming voltage (as compared to the first memory access technique) in order to program the storage element 204 to the “correct” state. As another example, the second memory access technique may sense the storage element 204 using a different read voltage (as compared to the first memory access technique) in order to read the storage element 204 at the “correct” threshold voltage (e.g., to compensate for reduced effectiveness of programming operations at the storage element 204 caused by tapering of the structure 202). As described further with reference to FIG. 4, ECC techniques and/or memory access techniques can be selectively applied to physical pages of a block based on a location of a variation of a structure.

[0068] Referring to FIG. 4, a particular illustrative embodiment of a block (e.g., an erase group of storage elements) is depicted and generally designated 400. The block 400 may be included in the memory 104 of FIG. 1. The example of FIG. 4 illustrates that the block 400 may include the physical pages 108, 118 and may further include the column 200.

[0069] The block 400 may further include a column 404 and a column 406. The columns may be formed upon the substrate 208. The columns 200, 404, and 406 may include multiple physical pages (e.g., word lines of storage elements) formed within layers of the memory 104. For example, the physical pages 108, 118 may be formed within multiple layers of the block 400. Each physical page of the block 400 may include multiple storage elements. As an example, the storage element 204 of FIG. 2 may be formed within the physical page 108, and the storage element 206 of FIG. 2 may be formed within the physical page 118.

[0070] In the example of FIG. 4, a variation (e.g., tapering) occurs in a structure of each of the columns 200, 404, and 406. It should be appreciated that, depending on the particular fabrication process, a block may include one or more columns with structures that do not include (or that do not substantially include) a variation. FIG. 4 further depicts that the variation within each of the columns 200, 404, and 406 occurs at (or approximately at) the location 116. It should be appreciated that variations within the columns 200, 404, and 406 may occur at different locations (e.g., at different heights above the substrate 208).

[0071] FIG. 4 illustrates that a location (e.g., the location 116) of a variation of a structure may occur between (or approximately between) physical pages of a block, such as the block 400. The data storage device 102 may apply techniques for encoding, writing, reading, and decoding data from a physical page of the block 400 based on a location of the physical page relative to the location 116. As described further with reference to FIG. 5, the location 116 may define multiple levels of a three-dimensional (3D) memory.

[0072] Referring to FIG. 5, a particular illustrative embodiment of a three dimensional (3D) memory is depicted and generally designated 500. The 3D memory 500 may be included in the memory 104 of FIG. 1. The 3D memory 500 may include the block 400 of FIG. 4. The 3D memory 500 may further include a block 504 and a block 506. Each of the blocks 400, 504, and 506 may be formed upon the substrate 208.

[0073] In FIG. 5, the location 116 defines a level 502. The level 502 may “partition” the 3D memory 500 into multiple levels (e.g., a “bottom” level that is

adjacent to the substrate 208 and a “top” level that is non-adjacent to the substrate 208). For example, the level 502 may define a plane that intersects each of the blocks 400, 504, and 506 at a level k , where k is a positive integer indicating a distance between the substrate 208 and the location 116. The level k may indicate a number of physical pages of the 3D memory 500 between the substrate 208 and the location 116.

[0074] In a particular embodiment, the wear distributor 168 of FIG. 1 is configured to perform “intra-level” wear leveling of the 3D memory 500. The wear distributor 168 may confine a first wear leveling process to storage elements within a first set of physical pages located below the level 502 and may further confine a second wear leveling process to storage elements within a second set of physical pages located above the level 502. As an illustrative example, the wear distributor 168 may distribute wear within the first set by moving the ECC codeword 120 among physical pages of the 3D memory 500 below the level 502 and may distribute wear within the second set by moving the ECC codeword 110 among physical pages of the 3D memory 500 above the level 502.

[0075] An intra-level wear leveling technique may advantageously enable the controller 130 to maintain a first set of ECC codewords associated with a first encoding technique (e.g., having a first number of ECC bits) within the first set of physical pages and a second set of ECC codewords associated with a second encoding technique (e.g., having a second number of ECC bits) within the second set of physical pages. The intra-level wear leveling process may improve operation of the data storage device 102 by avoiding programming of a “short” ECC codeword (e.g., the ECC codeword 120) to a physical page located above the level 502 (which may result in a bit error rate of data exceeding an error correction capability of the ECC engine 132) and/or by avoiding programming of an “extended” ECC codeword (e.g., the ECC codeword 110) to a physical page located below the level 502 (for which a “short” ECC codeword may suffice).

[0076] The level 502 may intersect each of the blocks 400, 504, and 506 at a common level k . Alternatively, depending on the particular fabrication process used to fabricate the 3D memory 500, the level 502 may intersect two or more of the blocks 400, 504, and 506 at different locations. To illustrate, the level 502 may intersect the

block 400 at a first distance from the substrate 208, the level 502 may intersect the block 504 at a second distance from the substrate 208, and the level 502 may intersect the block 506 at a third distance from the substrate 208. In this example, the level 502 may correspond to a “non-uniform” plane, such as an inclined plane. An illustrative example of an inclined plane is described further with reference to FIG. 6.

[0077] Referring to FIG. 6, a particular illustrative example of a table is depicted and generally designated 600. In a particular embodiment, the table 600 is included in the information 146 of FIG. 1. The table 600 may represent characteristics of a memory having a three-dimensional (3D) memory configuration. The memory may correspond to the memory 104 and/or the 3D memory 500.

[0078] FIG. 6 illustrates that the table 600 may include a block column and a location column. The block column may include block entries 602, 606, and 610. The location column may include location entries 604, 608, and 612. In a particular embodiment, the table 600 indicates an inclined plane that is defined by the level 502 of FIG. 5. For example, the block entry 602 and the location entry 604 indicate that the level 502 intersects a 0th block of the 3D memory 500 at a k th physical page of the 0th block. The block entry 606 and the location entry 608 indicate that the level 502 intersects a 5th block of the 3D memory 500 at a $(k+1)$ th physical page of the 5th block. Further, the block entry 610 and the location entry 612 indicate that the level 502 intersects an N th block of the 3D memory 500 at a $(k+2)$ th physical page of the N th block, where N indicates a positive integer number of blocks of the 3D memory 500 (e.g., 512 blocks, or another number of blocks). In this example, the level 502 may correspond to an inclined plane that intersects two or more blocks at different locations (e.g., at physical pages corresponding to k , $k+1$, and $k+2$).

[0079] The controller 130 may maintain the table 600 to track locations of variations of structures of the 3D memory 500. The locations of variations of structures may be inhomogeneous (e.g., may not define a plane that is parallel to a surface of the substrate 208). To illustrate, the example of FIG. 6 indicates that the level 502 may have an “inclined” shape. Enabling the controller 130 to define an inhomogeneous level (e.g., an inclined plane as indicated by the table 600) may improve performance of the data storage device 102 by enabling the controller 130 to selectively encode, write, read,

and/or decode data for a particular block of the memory 104 based on the level 502. It should be appreciated that the example of FIG. 6 is illustrative and that the level 502 may have another shape, such as a uniform shape that intersects each block of the 3D memory 500 at a common distance from the substrate 208, a declined shape, a “lumped” or “jagged” shape, or another shape.

[0080] Referring to FIG. 7, a particular illustrative embodiment of a method is depicted and generally designated 700. The method 700 may be performed by the data storage device 102 of FIG. 1, such as by the controller 130.

[0081] The method 700 includes determining a location associated with a variation of a structure that extends through multiple layers of a memory of a data storage device, at 704. The memory has a three dimensional (3D) memory configuration. The location may correspond to the location 116, and the structure may correspond to the structure 202. The multiple layers may include the layers 210, 212, and 214, the memory may correspond to the memory 104, and the data storage device may correspond to the data storage device 102.

[0082] The method 700 may further include generating information indicating the location, at 708. For example, the information may correspond to the information 146. In a particular embodiment, the information 146 corresponds to the table 600. Alternatively, the information 146 may indicate another table, other information, or a combination thereof.

[0083] The method 700 further includes storing the information at the data storage device, at 712. In a particular embodiment, the controller 130 stores the information 146 at the memory 104. In one or more other implementations, the information 146 may be stored at the controller 130, such as at a non-volatile memory portion that may be included in the controller 130 in certain implementations (not shown in FIG. 1). The controller 130 may store (e.g., cache) the information 146 at the RAM 144, as illustrated in FIG. 1.

[0084] The method 700 further includes accessing the information, at 716. For example, the controller 130 may access the information to generate the ECC parameter table 148, the memory access parameter table 154, or a combination thereof.

[0085] The method 700 may improve performance of the data storage device 102 by enabling the controller 130 to track at least one location of a variation of a structure extending through layers of the memory 104. For example, the method 700 may enable the data storage device 102 to perform a “recalibration” procedure to re-determine at least one location of a variation of a structure that extends through layers of the memory 104. Certain example aspects of a recalibration procedure are described further with reference to FIGs. 8 and 9.

[0086] Referring to FIG. 8, a particular illustrative embodiment of a method is depicted and generally designated 800. The method 800 may be performed by the data storage device 102, such as by the controller 130. In an illustrative embodiment, one or more operations of the method 800 are performed by the location identifier 134 of FIG. 1.

[0087] The method 800 may include detecting a power-up operation at a data storage device that includes a memory having a three dimensional (3D) memory configuration, at 804. The data storage device may correspond to the data storage device 102, and the memory may correspond to the memory 104. In a particular embodiment, the data storage device 102 includes a power-up detector configured to detect that power is being received at the data storage device 102 (e.g., from the host device 172).

[0088] The method 800 may further include determining whether a level determination procedure is to be performed, at 808. For example, the controller 130 may access the power-up indicator 136 to determine whether to perform the level determination procedure. A first value of the power-up indicator 136 may indicate that the level determination procedure has been previously performed (e.g., in response to an initial power-up of the data storage device 102), and a second value of the power-up indicator 136 may indicate that the level determination procedure has not been previously performed (e.g., that the current power-up is an initial power-up of the data storage device 102).

[0089] If a determination is made, at 812, that the level determination procedure is not to be performed, the method 800 may further include determining, at 816, whether

to perform a level re-determination procedure (or “recalibration” procedure). For example, the controller 130 may periodically or occasionally perform the level re-determination procedure to determine whether the location 116 has shifted (e.g., due to physical wear of the memory 104). In a particular embodiment, the controller 130 is configured to track a number of power-ups of the data storage device 102, and the level re-determination procedure is initiated in response to a threshold number of power-ups of the data storage device 102. As an illustrative example, the controller 130 may initiate the level re-determination procedure in response to a first number (such as an intermediate number) of power-ups of the data storage device 102, which may occur during a middle-of-life (MOL) stage of operation of the data storage device 102. As another illustrative example, the controller 130 may initiate the level re-determination procedure in response to a second number of power-ups of the data storage device 102, such as at an end-of-life (EOL) stage of operation of the data storage device 102.

[0090] If a determination is made, at 816, not to perform the level re-determination procedure, the method 800 may further include initiating an operating mode of the data storage device, at 820. If a determination is made, at 812, to perform the level determination procedure, or if a determination is made, at 816, to perform the level re-determination procedure, then operation may continue as described with reference to FIG. 9.

[0091] Referring to FIG. 9, a particular illustrative embodiment of a method of determining a location of a variation of a structure is depicted and generally designated 900. The method 900 may be performed by the data storage device 102, such as by the controller 130. In an illustrative embodiment, one or more operations of the method 900 are performed by the location identifier 134 of FIG. 1.

[0092] The method 900 may include initiating a procedure to determine or to re-determine a location of a variation of a structure of a memory having a three-dimensional memory configuration, at 904. The memory may correspond to the memory 104, the location may correspond to the location 116, and the structure may correspond to the structure 202. In a particular embodiment, initiating the procedure includes selecting a block of the memory (e.g., one of the blocks 400, 504, and 506), selecting a structure of the block (e.g., a structure of a column, such as the structure 202

of the column 200), and/or initializing a value of an index x to zero, where the index x has an integer value indicating a physical page of the memory.

[0093] To illustrate, if a physical page of the memory adjacent to the substrate 208 (or a “bottom” physical page) is indicated by an index value of zero, then the value of the index x may be initialized to zero. In this example, the method 900 may correspond to a “bottom-up” search for a taper effect of a structure, such as the structure 202. In one or more other implementations, a physical page of the memory farthest from the substrate 208 (or a “top” physical page) may be indicated by the index value of zero, and the method 900 may correspond to a “top-down” search for a taper effect of the structure. Alternatively or in addition, the value of the index x may be selected using one or more other techniques (e.g., by randomly or pseudo-randomly selecting the value of the index x).

[0094] The method 900 may further include selecting an x th storage element associated with a first layer that is connected to a structure that extends through multiple layers of the memory and further selecting an $(x+1)$ th storage element associated with a second layer that is connected to the structure, at 908. To illustrate, for $x = 0$, the x th storage element may correspond to a storage element of the layer 210, and the $(x+1)$ th storage element may correspond to a storage element of the layer 212. In this example, the first layer may correspond to the layer 210, and the second layer may correspond to the layer 212.

[0095] The method 900 may further include measuring a first parameter of the x th storage element, at 912, and measuring a second parameter of the $(x+1)$ th storage element, at 916. As an example, the measurements 142 of FIG. 1 may indicate the first parameter and the second parameter. The first parameter may correspond to a first number of programming pulses applied to the first storage element to program the first storage element to a particular threshold voltage, and the second parameter may correspond to a second number of programming pulses applied to the second storage element to program the second storage element to the particular threshold voltage, as an illustrative example.

[0096] The method 900 may further include determining a difference between the first parameter and the second parameter, at 920. For example, the location identifier 134 may subtract the first parameter from the second parameter to determine the difference.

[0097] If a determination is made, at 924, that the difference satisfies a threshold, the method 900 may further include determining that a location of a variation of a structure is between the first layer and the second layer, at 932. For example, the location may correspond to the location 116, and the structure may correspond to the structure 202. The variation may correspond to a “tapering” of the structure 202 that occurs between (or approximately between) the first layer and the second layer.

[0098] The threshold may be selected based on particular device parameters. For example, expected values of the channel widths 312, 314 and/ or expected values of the gate-to-channel distances 316, 318 may be determined based on a fabrication process used to fabricate the memory 104. Expected values of channel widths and/ or expected values of gate-to-channel distances may be used to determine expected operating characteristics of storage elements of the memory 104. The threshold of FIG. 9 may be selected based on the expected operating characteristics. For example, a “tolerance” range may be defined for operating characteristics of storage elements of the memory 104. The threshold of FIG. 9 may correspond to such a tolerance range, and an indication of the threshold may be stored at the data storage device 102 (e.g., at the memory 104) to be accessed by the controller 130.

[0099] If a determination is made, at 924, that the difference fails to satisfy the threshold, the method 900 may further include determining that the location of the variation (if any) is above or below the first layer and the second layer, at 928. For example, in a “bottom-up” search, the location identifier 134 may determine that the location of the variation (if any) is above the first layer and the second layer. In a “top-down” search, the location identifier 134 may determine that the location of the variation (if any) is below the first layer and the second layer.

[00100] The method 900 may further include determining whether the procedure is complete, at 936. For example, the procedure may be performed to determine (or

attempt to determine) at least one location of a variation in each block of the memory. If the procedure is complete (e.g., has been performed for each block of the memory), the method 900 may further include storing information indicating the location of the variation, at 940. The information may correspond to the information 146 and/or may represent the table 600.

[00101] The method 900 may further include adjusting a power-up indicator from a first value to a second value in response to performing the procedure, at 944. The power-up indicator may correspond to the power-up indicator 136. In a particular embodiment, the power-up indicator 136 is changed from the first value to the second value in response to performing a first iteration of the procedure and in response to an initial power-up of the data storage device 102. After the initial power-up of the data storage device 102, the method 900 may be re-performed, such as at a middle-of-life (MOL) operating stage of the data storage device 102 (e.g., after a first number of power-ups of the data storage device 102) and/or at an end-of-life (EOL) operating stage of the data storage device 102 (e.g., after a second number of power-ups of the data storage device 102). In a particular embodiment, the controller 130 is configured to maintain an indication of a number of power-ups of the data storage device 102, such as at a state machine that may be included in the controller 130.

[00102] The method 948 may further include initiating an operating mode of the data storage device, at 948. For example, the data storage device 102 may enter a mode of operation in which data is stored to and accessed from the memory 104.

[00103] If a determination is made, at 936, that the procedure is not complete, the method 900 may include selecting another block of the memory, selecting another structure of a block of the memory, and/or adjusting the value of the index x , at 952. For example, after measuring parameters for a first storage element associated with a first layer of the memory 104 and a second storage element associated with a second layer of the memory 104, a third parameter may be measured for a third storage element associated with a third layer of the memory 104 that is connected to a structure that extends through multiple layers of the memory. The third parameter may be compared to the second parameter to determine a difference (e.g., to detect a variation between the

third layer and the second layer). In this example, the method 900 may continue, at 908, after incrementing the value of the index x .

[00104] Alternatively or in addition, the location identifier 134 may determine locations of multiple variations for a single block of the memory 104. To illustrate, if the location 116 is determined for the column 200 of the block 400 of FIG. 4, the location identifier 134 may determine a location of a variation of another structure of the memory 104, such as a structure of the column 404 and/or a variation of a structure of the column 406. The location identifier 134 may determine an average location of variations of the block 400, such as when tapering effects associated with the columns 200, 404, and 406 are non-uniform (e.g., have different profiles). Accordingly, the location 116 may correspond to an average location of variations of the columns 200, 404, and 406. In this case, if a location of a variation has been determined for one column of the block (e.g., the column 200), another column of the block may be selected (e.g., by selecting the column 404 or the column 406), and the method 900 may continue, at 908.

[00105] Alternatively or in addition, the location identifier 134 may determine locations of variations for multiple blocks of the memory 104. In this example, if a location of a variation has been determined for a particular block (e.g., the block 400), another block (e.g., the block 504 or the block 506) may be selected, and the method 900 may continue, at 908.

[00106] The method 900 enables determination of locations of one or more variations of structures that extend through layers of a memory having a 3D memory configuration. For example, the method 900 may enable the controller 130 to identify a “taper” effect that occurs at the location 116 of the structure 202 of FIG. 2. In a particular embodiment, the controller 130 uses the location 116 to determine one or more ECC techniques and/or one or more memory access techniques, as described further with reference to FIGs. 10-15.

[00107] Referring to FIG. 10, a particular illustrative embodiment of a method is depicted and generally designated 1000. The method 1000 may be performed by the data storage device 102, such as by the controller 130. In an illustrative embodiment,

one or more operations of the method 1000 are performed by the location identifier 134 of FIG. 1.

[00108] The method 1000 may include generating an error correcting code (ECC) parameter table that indicates a first ECC parameter for a first set of one or more physical pages of a memory that are disposed below a location and that further indicates a second ECC parameter for a second set of one or more physical pages of the memory that are disposed above the location, at 1004. The ECC parameter table is generated based on a location of a variation in a structure of the memory that extends through multiple layers of the memory. The memory may correspond to the memory 104, the location may correspond to the location 116, and the structure may correspond to the structure 202. The first set may include the physical page 118, and the second set may include the physical page 108. The ECC parameter table may correspond to the ECC parameter table 148, the first parameter may correspond to the parameter 150, and the second parameter may correspond to the parameter 152. The parameters 150, 152 may indicate encoding techniques and/or decoding techniques that are usable by the ECC engine 132, as illustrative examples.

[00109] The method 1000 may further include storing the ECC parameter table at a data storage device that includes the memory, at 1008. The data storage device may correspond to the data storage device 102. The ECC parameter table may be stored (e.g., cached) at the RAM 144, as illustrated in FIG. 1. Alternatively or in addition, the ECC parameter table may be stored at the memory 104.

[00110] The method 1000 illustrates that an ECC parameter table may be generated based on a location of a variation of a structure of a memory, such as the memory 104. The ECC parameter table may be used to adjust encoding techniques and/or decoding techniques based on a physical location of the data (e.g., based on whether data is to be written to or read from the physical page 108 versus the physical page 118).

[00111] Referring to FIG. 11, a particular illustrative embodiment of a method is depicted and generally designated 1100. The method 1100 may be performed by the data storage device 102, such as by the controller 130. In an illustrative embodiment,

one or more operations of the method 1100 are performed by the location identifier 134 of FIG. 1.

[00112] The method 1100 may include generating a memory access parameter table that indicates a first memory access parameter for a first set of one or more physical pages of a memory that are disposed below a location and that further indicates a second memory access parameter for a second set of one or more physical pages of the memory that are disposed above the location, at 1104. The memory access parameter table is generated based on a location of a variation in a structure of the memory that extends through multiple layers of the memory. The memory may correspond to the memory 104, the location may correspond to the location 116, and the structure may correspond to the structure 202. The first set may include the physical page 118, and the second set may include the physical page 118. The memory access parameter table may correspond to the memory access parameter table 154, the first parameter may correspond to the parameter 156, and the second parameter may correspond to the parameter 158. The parameters 156, 158 may indicate read techniques and/or write techniques that are usable by the read/write circuitry 106, as illustrative examples.

[00113] The method 1100 may further include storing the memory access parameter table at a data storage device that includes the memory, at 1108. The data storage device may correspond to the data storage device 102. The memory access parameter table may be stored (e.g., cached) at the RAM 144, as illustrated in FIG. 1. Alternatively or in addition, the memory access parameter table may be stored at the memory 104.

[00114] The method 1100 illustrates that a memory access parameter table may be generated based on a location of a variation of a structure of a memory, such as the memory 104. The memory access parameter table may be used to adjust write techniques and/or read techniques based on a physical location of the data (e.g., based on whether data is to be written to or read from the physical page 108 versus the physical page 118).

[00115] Referring to FIG. 12, a particular illustrative embodiment of a method is depicted and generally designated 1200. The method 1200 may be performed by the

data storage device 102. For example, certain operations of the method 1200 may be performed by the controller 130, the read/write circuitry 106, or a combination thereof.

[00116] The method 1200 may include receiving a first request for write access from a host device to write first data to a memory having a three-dimensional memory configuration and including multiple layers formed upon a substrate, at 1204. The memory may correspond to the memory 104, and the host device may correspond to the host device 172. The first data may correspond to the data 122, and the substrate may correspond to the substrate 208. The multiple layers may include the layers 210, 212, and 214.

[00117] The method 1200 may further include accessing a logical-to-physical address mapping table to determine that the first data is to be stored at a first physical page of the memory, at 1208. The first physical page is disposed within the memory at a first distance from the substrate. The logical-to-physical address mapping table may correspond to the logical-to-physical address mapping table 166, and the first physical page may correspond to the physical page 118.

[00118] The method 1200 may further include accessing an error correcting code (ECC) parameter table to determine that the first physical page is included in a first set of one or more physical pages associated with a first ECC parameter, at 1212. The ECC parameter table may correspond to the ECC parameter table 148, and the first parameter may correspond to the parameter 150. In an illustrative embodiment, the parameter 150 indicates a first encoding technique.

[00119] The method 1200 may further include changing a mode of operation of an ECC engine based on the first ECC parameter, at 1216. The ECC engine may correspond to the ECC engine 132. The mode of operation of the ECC engine 132 may be changed by the controller 130 by causing the ECC engine 132 to encode data using the first encoding technique, such as by activating a first encoder of the ECC engine 132 and/or by deactivating a second encoder of the ECC engine 132.

[00120] The method 1200 may further include encoding the first data at the ECC engine using the first encoding technique to generate a first ECC codeword, at 1220. The first ECC codeword may correspond to the ECC codeword 120.

[00121] The method 1200 may further include storing the first ECC codeword to the physical page, at 1224. For example, the controller 130 may instruct the read/write circuitry 106 to store the ECC codeword 120 at the physical page 118.

[00122] The method 1200 may further include receiving a second request for write access from the host device to write second data to the memory, at 1228. The second data may correspond to the data 112.

[00123] The method 1200 may further include accessing the logical-to-physical address mapping table to determine that the second data is to be stored at a second physical page of the memory, at 1232. The second physical page is disposed within the memory at a second distance from the substrate, and the second distance is greater than the first distance. The second physical page may correspond to the physical page 108.

[00124] The method 1200 may further include accessing the ECC parameter table to determine that the second physical page is included in a second set of one or more physical pages associated with a second ECC parameter, at 1236. The second ECC parameter may specify a second encoding technique that is different than the first encoding technique. The second ECC parameter may correspond to the parameter 152.

[00125] The method 1200 may further include changing the mode of operation of the ECC engine based on the second ECC parameter, at 1240. To illustrate, the controller 130 may deactivate a first encoder of the ECC engine 132 associated with the first encoding technique and may activate a second encoder of the ECC engine 132 associated with the second encoding technique.

[00126] The method 1200 may further include encoding the second data at the ECC engine using the second encoding technique to generate a second ECC codeword, 1244. The second ECC codeword may correspond to the ECC codeword 110.

[00127] The method 1200 may further include storing the second ECC codeword to the second physical page, at 1248. To illustrate, the controller 130 may instruct the read/write circuitry 106 to store the ECC codeword 110 at the physical page 108.

[00128] The method 1200 may improve accuracy of encoding operations at the data storage device 102. For example, because a variation of the structure 202 may increase

a bit error rate of data stored at the physical page 108 relative to data stored at the physical page 118, data to be stored at the physical pages 108, 118 may be encoded using different techniques.

[00129] Referring to FIG. 13, a particular illustrative embodiment of a method is depicted and generally designated 1300. The method 1300 may be performed by the data storage device 102. For example, certain operations of the method 1300 may be performed by the controller 130, the read/write circuitry 106, or a combination thereof.

[00130] The method 1300 may include receiving a first request for read access from a host device to read first data from a memory having a three-dimensional memory configuration and including multiple layers formed upon a substrate, at 1304. The memory may correspond to the memory 104, and the host device may correspond to the host device 172. The substrate may correspond to the substrate 208, and the multiple layers may include the layers 210, 212, and 214. The first data may correspond to the data 122.

[00131] The method 1300 may further include accessing a logical-to-physical address mapping table to determine that the first data is stored at a first physical page of the memory, at 1308. The first physical page is disposed within the memory at a first distance from the substrate. The logical-to-physical address mapping table may correspond to the logical-to-physical address mapping table 166, and the first physical page may correspond to the physical page 118.

[00132] The method 1300 may further include accessing an error correcting code (ECC) parameter table to determine that the first physical page is included in a first set of one or more physical pages associated with a first ECC parameter, at 1312. The ECC parameter table may correspond to the ECC parameter table 148, and the first ECC parameter may correspond to the parameter 150. In a particular embodiment, the parameter 150 specifies a first decoding technique.

[00133] The method 1300 may further include sensing a first ECC codeword from the first physical page, at 1316. The first ECC codeword may correspond to the ECC codeword 120.

[00134] The method 1300 may further include changing a mode of operation of an ECC engine based on the first ECC parameter, at 1320. The ECC engine may correspond to the ECC engine 132. In a particular embodiment, the ECC engine 132 includes a first decoder configured to decode ECC codewords using the first ECC decoding technique, and the controller 130 changes the mode of operation of the ECC engine 132 by enabling the first decoder.

[00135] The method 1300 may further include decoding the first ECC codeword at the ECC engine using the first decoding technique to generate the first data, at 1324. For example, the controller 130 may input the ECC codeword 120 to the first decoder, and the first decoder may output the data 122.

[00136] The method 1300 may further include sending the first data to the host device, at 1328. For example, the controller 130 may send the data 122 to the host device 172 via the host interface 170.

[00137] The method 1300 may further include receiving a second request for read access from the host device to read second data from the memory, at 1332. The second data may correspond to the data 112.

[00138] The method 1300 may further include accessing the logical-to-physical address mapping table to determine that the second data is stored at a physical page of the memory, at 1336. The second physical page is disposed within the memory at a second distance from the substrate, and the second distance is greater than the first distance. The second physical page may correspond to the physical page 108.

[00139] The method 1300 may further include accessing the ECC parameter table to determine that the second physical page is included in a second set of one or more physical pages associated with a second ECC parameter, at 1340. The second ECC parameter may specify a second decoding technique that is different than the first decoding technique. In a particular embodiment, the second parameter corresponds to the parameter 152.

[00140] The method 1300 may further include changing the mode of operation of the ECC engine based on the second ECC parameter, at 1344. For example, in a particular

embodiment, the controller 130 deactivates the first decoder of the ECC engine 132 and activates a second decoder of the ECC engine 132.

[00141] The method 1300 may further include decoding the second ECC codeword at the ECC engine using the second decoding technique to generate the second data, at 1348. For example, the controller 130 may input the ECC codeword 110 at the second decoder of the ECC engine 132, and the second decoder may output the data 112.

[00142] The method 1300 may further include sending the second data to the host device, at 1352. To illustrate, the controller 130 may send the data 112 to the host device 172 via the host interface 170.

[00143] The method 1300 may improve accuracy of decoding operations at the data storage device 102. For example, because a variation of the structure 202 may increase a bit error rate of data stored at the physical page 108 relative to data stored at the physical page 118, data read from the physical pages 108, 118 may be decoded using different techniques.

[00144] Referring to FIG. 14, a particular illustrative embodiment of a method is depicted and generally designated 1400. The method 1400 may be performed by the data storage device 102. For example, certain operations of the method 1400 may be performed by the controller 130, the read/write circuitry 106, or a combination thereof.

[00145] The method 1400 may include receiving a first request for write access from a host device to write first data to a memory having a three-dimensional memory configuration and including multiple layers formed upon a substrate, at 1404. The memory may correspond to the memory 104, and the host device may correspond to the host device 172. The substrate may correspond to the substrate 208, and the multiple layers may include the layers 210, 212, and 214. The first request may correspond to the first request described with reference to FIG. 12, or to another request.

[00146] The method 1400 may further include accessing a logical-to-physical address mapping table to determine that the first data is to be stored at a first physical page of the memory, at 1408. The first physical page is disposed within the memory at a first

distance from the substrate. The first physical page may correspond to the physical page 118.

[00147] The method 1400 may further include accessing a memory access parameter table to determine that the first physical page is included in a first set of one or more physical pages associated with a first write parameter, at 1412. The memory access parameter table may correspond to the memory access parameter table 154, and the first write parameter may correspond to the parameter 156. In a particular embodiment, the parameter 156 indicates a programming voltage to be applied to the physical page 118.

[00148] The method 1400 may further include adjusting write circuitry based on the first write parameter, at 1416. To illustrate, the controller 130 may send one or more control signals to the read/write circuitry 106 to cause the read/write circuitry 106 to write data using a first programming voltage indicated by the parameter 156.

[00149] The method 1400 may further include writing the first data to the first physical page using the first write technique, at 1420. For example, the data 122 may be written to the physical page 118 within the ECC codeword 120.

[00150] The method 1400 may further include receiving a second request for write access from the host device to write second data to the memory, at 1424. The second data may correspond to the data 112. The second request may correspond to the second request described with reference to FIG. 12, or to another request.

[00151] The method 1400 may further include accessing the logical-to-physical address mapping table to determine that the second data is to be stored at a second physical page of the memory, at 1428. The second physical page is disposed within the memory at a second distance from the substrate, and the second distance is greater than the first distance. The second physical page may correspond to the physical page 108.

[00152] The method 1400 may further include accessing the memory access parameter table to determine that the second physical page is included in a second set of one or more physical pages associated with a second write parameter, at 1432. The second write parameter may correspond to the parameter 158. In a particular

embodiment, the parameter 158 specifies a second programming voltage that is different than the first programming voltage.

[00153] The method 1400 may further include adjusting the write circuitry based on the second write parameter, at 1436. For example, the controller 130 may assert one or more control signals that cause the read/write circuitry 106 to write data using the second programming voltage.

[00154] The method 1400 may further include writing the second data to the second physical page, at 1440. To illustrate, the data 112 may be written within the ECC codeword 110 to the physical page 108.

[00155] The method 1400 may improve accuracy of write operations at the data storage device 102. For example, because a variation of the structure 202 may increase a bit error rate of data stored at the physical page 108 relative to the physical page 118, data may be written to the physical pages 108, 118 using different techniques.

[00156] Referring to FIG. 15, a particular illustrative embodiment of a method is depicted and generally designated 1500. The method 1500 may be performed by the data storage device 102. For example, certain operations of the method 1500 may be performed by the controller 130, the read/write circuitry 106, or a combination thereof.

[00157] The method 1500 may include receiving a first request for read access from a host device to read first data from a memory having a three-dimensional memory configuration and including multiple layers formed upon a substrate, at 1504. The memory may correspond to the memory 104, and the host device may correspond to the host device 172. The substrate may correspond to the substrate 208, and the multiple layers may include the layers 210, 212, and 214. The first data may correspond to the data 122. The first request may correspond to the first request described with reference to FIG. 13, or to another request.

[00158] The method 1500 may further include accessing a logical-to-physical address mapping table to determine that the first data is stored at a first physical page of the memory, at 1508. The first physical page is disposed within the memory at a first distance from the substrate. The logical-to-physical address mapping table may

correspond to the logical-to-physical address mapping table 166, and the first physical page may correspond to the physical page 118.

[00159] The method 1500 may further include accessing a memory access parameter table to determine that the first physical page is included in a first set of one or more physical pages associated with a first read parameter, at 1512. The memory access parameter table may correspond to the memory access parameter table 154, and the first read parameter may correspond to the parameter 156. In a particular embodiment, the parameter 156 specifies a first read voltage.

[00160] The method 1500 may further include adjusting read circuitry based on the first parameter, at 1516. For example, the controller 130 may assert one or more control signals that cause the read/write circuitry 106 to read data using the first read voltage.

[00161] The method 1500 may further include reading the first data from the first physical page, at 1520. To illustrate, the read/write circuitry 106 may sense the ECC codeword 120 from the physical page 118. In a particular embodiment, the ECC engine 132 decodes the ECC codeword 120 to generate the data 122.

[00162] The method 1500 may further include sending the first data to the host device, at 1524. To illustrate, the controller 130 may send the data 122 to the host device 172 via the host interface 170.

[00163] The method 1500 may further include receiving a second request for read access from the host device to read second data from the memory, at 1528. The second data may correspond to the data 112. The second request may correspond to the second request described with reference to FIG. 13, or to another request.

[00164] The method 1500 may further include accessing the logical-to-physical address mapping table to determine that the second data is stored at a second physical page of the memory, at 1532. The second physical page is disposed within the memory at a second distance from the substrate, and the second distance is greater than the first distance. The second physical page may correspond to the physical page 108.

[00165] The method 1500 may further include accessing the memory access parameter table to determine that the second physical page is included in a second set of

one or more physical pages associated with a second read parameter, at 1536. The second read parameter may correspond to the parameter 158. In a particular embodiment, the parameter 158 specifies a second read voltage that is different than the first read voltage.

[00166] The method 1500 may further include adjusting the read circuitry based on the second read parameter, at 1540. For example, the controller 130 may assert one or more control signals that cause the read/write circuitry 106 to read data using the second read voltage.

[00167] The method 1500 may further include reading the data from the second physical page, at 1544. To illustrate, the read/write circuitry 106 may sense the ECC codeword 110 from the physical page 108. The ECC engine 132 may decode the ECC codeword 110 to generate the data 112.

[00168] The method 1500 may further include sending the second data to the host device, at 1548. For example, the controller 130 may send the data 112 to the host device 172 via the host interface 170.

[00169] The method 1500 may improve accuracy of read operations at the data storage device 102. For example, because a variation of the structure 202 may increase a bit error rate of data stored at the physical page 108 relative to the physical page 118, data may be read from the physical pages 108, 118 using different techniques.

[00170] FIG. 16 illustrates an embodiment of a 3D memory 1600 in a NAND flash configuration. The 3D memory 1600 may correspond to the memory 104 of FIG. 1. The memory 1600 includes multiple physical layers 1602 that are monolithically formed above a substrate 1604, such as a silicon substrate. Storage elements (e.g., memory cells), such as a representative storage element 1610, are arranged in arrays in the physical layers 1602.

[00171] The representative memory cell 1610 includes a charge trap structure 1614 between a word line/control gate (WL4) 1628 and a conductive channel 1612. Charge may be injected into or drained from the charge trap structure 1614 via biasing of the conductive channel 1612 relative to the word line 1628. For example, the charge trap

structure 1614 may include silicon nitride and may be separated from the word line 1628 and the conductive channel 1612 by a gate dielectric, such as a silicon oxide. An amount of charge in the charge trap structure 1614 affects an amount of current through the conductive channel 1612 during a read operation of the memory cell 1610 and indicates one or more bit values that are stored in the memory cell 1610.

[00172] The 3D memory 1600 includes multiple erase blocks, including a first block (block 0) 1650, a second block (block 1) 1652, and a third block (block 2) 1654. Each block 1650-1654 includes a “vertical slice” of the physical layers 1602 that includes a stack of word lines, illustrated as a first word line (WL0) 1620, a second word line (WL1) 1622, a third word line (WL2) 1624, a fourth word line (WL3) 1626, and the fifth word line (WL4) 1628. Multiple conductive channels (having a substantially vertical orientation (i.e., having an up and down orientation in FIG. 16) that is substantially perpendicular to an upper surface of the substrate 1604) extend through the stack of word lines. Each conductive channel is coupled to a storage element in each word line 1620-1628, forming a NAND string of storage elements. FIG. 16 illustrates three blocks 1650-1654, five word lines 1620-1628 in each block, and three conductive channels in each block for clarity of illustration. However, the 3D memory 1600 may have more than three blocks, more than five word lines per block, and more than three conductive channels per block.

[00173] The 3D memory further includes read/write circuitry 1660 and data latches 1662. The read/write circuitry 1660 may correspond to the read/write circuitry 106 of FIG. 1. The read/write circuitry 1660 is coupled to the conductive channels via multiple conductive lines, illustrated as a first bit line (BL0) 1630, a second bit line (BL1) 1632, and a third bit line (BL2) 1634 at a “top” end of the conductive channels (e.g., farther from the substrate 1604) and a first source line (SL0) 1640, a second source line (SL1) 1642, and a third source line (SL2) 1644 at a “bottom” end of the conductive channels (e.g., nearer to or within the substrate 1604). The read/write circuitry 1660 is illustrated as coupled to the bit lines 1630-1634 via “P” control lines, coupled to the source lines 1640-1644 via “M” control lines, and coupled to the word lines 1620-1628 via “N” control lines. Each of P, M, and N has a positive integer value based on the specific

configuration of the 3D memory 1600. In the illustrative example of FIG. 16, $P=3$, $M=3$, and $N=5$.

[00174] In operation, data (e.g., an ECC codeword) may be latched into the data latches 1662 (e.g., by the controller 130 of FIG. 1) for writing to one of the word lines 1620-1628. To write data to one or more of the word lines 1620-1628, the read/write circuitry 1660 may read bits from the data latches 1662 and apply selection signals to control lines coupled to the word lines 1620-1628, the bit lines 1630-1634, and the source lines 1640-1642 to cause a programming voltage (e.g., a voltage pulse or series of voltage pulses) to be applied across selected storage element(s) of the selected word line (e.g., the fourth word line 1628).

[00175] The read/write circuitry 1660 may be responsive to a control signal 1665 (e.g., from the controller 130 of FIG. 1) to select between read/write voltages 1661 and read/write voltages 1663. The read/write voltages 1663 may include programming voltages for word lines of the 3D memory 1600 that are below the location 116. The read/write voltages 1661 may further include programming voltages for word lines of the 3D memory 1600 that are above the location 116. In the example of FIG. 16, the word lines 1620-1624 are below the location 116, and the word lines 1626, 1628 are above the location 116. Accordingly, based on the control signal 1665, the read/write circuitry 1660 may write data from the data latches 1662 to any of the word lines 1620-1624 using one or more programming voltages included in the read/write voltages 1663 or to any of the word lines 1626, 1628 using one or more programming voltages included in the read/write voltages 1661.

[00176] During a read operation, the controller 130 of FIG. 1 may receive a request from a host device, such as the host device 172 of FIG. 1. The controller 130 may cause the read/write circuitry 1660 to read bits from particular storage elements of the 3D memory 1600 by applying appropriate signals to the control lines to cause storage elements of a selected word line to be sensed. The logical values read from the storage elements of the selected word line may be saved at the data latches 1662 and provided to the controller 130.

[00177] The read/write circuitry 1660 may be responsive to the control signal 1665 to select a particular read voltage (or set of read voltages) of the read/write voltages 1661, 1663. The read/write voltages 1663 may include read voltages for word lines of the 3D memory 1600 that are below the location 116. The read/write voltages 1661 may further include read voltages for word lines of the 3D memory 1600 that are above the location 116. In the example of FIG. 16, the word lines 1620-1624 are below the location 116, and the word lines 1626, 1628 are above the location 116. Accordingly, based on the control signal 1665, the read/write circuitry 1660 may read data from any of the word lines 1620-1624 using read voltages included in the read/write voltages 1663 or from any of the word lines 1626, 1628 using read voltages included in the read/write voltages 1661. The data may be saved to the data latches 1662 to be accessed by the controller 130.

[00178] FIG. 17 is a diagram of a particular embodiment of a memory 1700. The memory may correspond to the memory 104 of FIG. 1. FIG. 17 illustrates a portion of a three-dimensional architecture of the memory 104 according to a particular embodiment. In the embodiment illustrated in FIG. 17, the memory 1700 is a vertical bit line Resistive Random Access Memory (ReRAM) with a plurality of conductive lines in physical layers over a substrate (e.g., substantially parallel to a surface of the substrate), such as representative wordlines 1720, 1721, 1722, and wordline 1723 (only a portion of which is shown in FIG. 17) and a plurality of vertical conductive lines through the physical layers, such as representative bit lines 1710, 1711, 1712, and 1713. The memory 1700 also includes a plurality of resistance-based storage elements (e.g., memory cells), such as representative storage elements 1730, 1731, 1732, 1740, 1741, and 1742, each of which is coupled to a bit line and a wordline in arrays of memory cells in multiple physical layers over the substrate (e.g., a silicon substrate).

[00179] The memory 1700 also includes data latches 1702 and read/write circuitry 1704. In a particular embodiment, the data latches 1702 correspond to the data latches 1662 of FIG. 16 and the read/write circuitry 1704 corresponds to the read/write circuitry 106 of FIG. 1 and/or the read/write circuitry 1660 of FIG. 16. The read/write circuitry 1704 is coupled to wordline drivers 1708 and bit line drivers 1706.

[00180] In the embodiment illustrated in FIG. 17, each of the wordlines includes a plurality of fingers (e.g., a first wordline 1720 includes fingers 1724, 1725, 1726, and 1727). Each finger may be coupled to more than one bit line. To illustrate, a first finger 1724 of the first wordline 1720 is coupled to a first bit line 1710 via a first storage element 1730 at a first end of the first finger 1724 and is coupled to a second bit line 1711 via a second storage element 1740 at a second end of the first finger 1724.

[00181] In the embodiment illustrated in FIG. 17, each bit line may be coupled to more than one wordline. To illustrate, the first bit line 1710 is coupled to the first wordline 1720 via the first storage element 1730 and is coupled to a third wordline 1722 via a third storage element 1732.

[00182] During a write operation, the controller 130 may receive data from a host device, such as the host device 172 of FIG. 1. The controller 130 may send the data (or a representation of the data) to the memory 1700 to be stored in the data latches 1702. The controller 130 may encode the data (e.g., at the ECC engine 132) prior to sending the encoded data to the data latches 1702.

[00183] The read/write circuitry 1704 may read bits from the data latches 1702 and apply selection signals to selection control lines coupled to the wordline drivers 1708 and the bit line drivers 1706 to cause a write voltage to be applied across a selected storage element. For example, to select the first storage element 1730, the read/write circuitry 1704 may activate the wordline drivers 1708 and the bit line drivers 1706 to drive a programming current (also referred to as a write current) through the first storage element 1730. To illustrate, a first write current may be used to write a first logical value (e.g., a value corresponding to a high-resistance state) to the first storage element 1730, and a second write current may be used to write a second logical value (e.g., a value corresponding to a low-resistance state) to the first storage element 1730. The programming current may be applied by generating a programming voltage across the first storage element 1730 by applying a first voltage to the first bit line 1710 and to wordlines other than the first wordline 1720 and applying a second voltage to the first wordline 1720. In a particular embodiment, the first voltage is applied to other bit lines (e.g., the bit lines 1714, 1715) to reduce leakage current in the memory 104.

[00184] During a read operation, the controller 130 may receive a request from a host device, such as the host device 130 of FIG. 1. The controller 130 may cause the read/write circuitry 1704 to read bits from particular storage elements of the memory 104 by applying selection signals to selection control lines coupled to the wordline drivers 1708 and the bit line drivers 1706 to cause a read voltage to be applied across a selected storage element. For example, to select the first storage element 1730, the read/write circuitry 1704 may activate the wordline drivers 1708 and the bit line drivers 1706 to apply a first voltage (e.g., 0.7 volts (V)) to the first bit line 1710 and to wordlines other than the first wordline 1720. A lower voltage (e.g., 0 V) may be applied to the first wordline 1720. Thus, a read voltage is applied across the first storage element 1730, and a read current corresponding to the read voltage may be detected at a sense amplifier of the read/write circuitry 1704. The read current corresponds (via Ohm's law) to a resistance state of the first storage element 1730, which corresponds to a logical value stored at the first storage element 1730. The logical value read from the first storage element 1730 and other elements read during the read operation may be saved at the data latches 1702 and provided to the controller 130.

[00185] The example of FIG. 17 illustrates that the read/write circuitry may selectively apply read/write voltages 1707 for word lines 1721, 1722 and read/write voltages 1705 for word lines 1720, 1723. The read/write circuitry 1704 may selectively apply the read/write voltages 1705, 1707 based on a control signal 1709, which may be received from the controller 130 of FIG. 1. The controller 130 may selectively assert the control signal 1709 to adjust the read/write circuitry 1704. For example, the controller 130 may selectively assert the control signal 1709 to cause data to be programmed to and read from the word lines 1721, 1722 at different programming voltages and read voltages as compared to the word lines 1720, 1723.

[00186] As used herein, a variation of a structure may occur "approximately" at a location if the variation causes a performance difference between a first storage element on one side of the location (e.g., below the location) and a second storage element on another side of the location (e.g., above the location). To illustrate, a location of a variation of a structure (e.g., the location 116) may be approximately between the

storage elements 204, 206 if the variation causes a performance difference between the storage elements 204, 206. The performance difference may correspond to a difference in a number of programming pulses used to program the storage element 204 to a particular state relative to the storage element 206, as an illustrative example. It is noted that the location of the variation need not be exactly located between the storage elements 204, 206 to cause a performance difference between the storage elements 204, 206. As used herein, a location may be “associated with” a variation of a structure if the variation occurs approximately at the location.

[00187] It is noted that the particular examples herein are provided for illustrative purposes and that certain modifications of the examples are within the scope of the disclosure. For example, although FIG. 5 illustrates that the 3D memory 500 includes a single level (the level 502), the 3D memory 500 may include multiple levels. For example, depending on the particular fabrication process, the 3D memory 500 may include multiple different variations (e.g., “taper” effects) of one or more structures extending through layers of the 3D memory 500. In this case, the 3D memory 500 may include multiple levels associated with multiple subsets of physical pages. Each of the subsets may be associated with a particular encoding technique, writing technique, reading technique, and/or decoding technique.

[00188] Depending on the particular fabrication process, a variation of a structure may have one or more of a variety of shapes. The structure 202 is illustrated as having a “conical” or “tapered” shape for illustration. However, a structure may have another shape. For example, depending on the particular fabrication process, a structure of a memory may increase in uniformity (e.g., tapering may decrease) with increased distance from a surface of a substrate of the memory. In this case, reliability of first data stored at a first set of one or more physical pages of the memory nearer the substrate may be less than reliability of second data stored at a second set of one or more physical pages of the memory that are farther from the substrate. The data storage device 102 may be configured to compensate for reduced reliability of the first data. For example, the data storage device 102 may apply the second encoding technique of FIG. 12, the second decoding technique of FIG. 13, the second write technique of FIG. 14, and/or the second read technique of FIG. 15 to the first data to compensate for

reduced reliability of the first data. In this example, the data storage device 102 may apply the first encoding technique of FIG. 12, the first decoding technique of FIG. 13, the first write technique of FIG. 14, and/or the first read technique of FIG. 15 to the second data.

[00189] It is further noted that levels of a memory may be defined separately for different parameters of the memory. To illustrate, the level 502 of the 3D memory 500 may define a first encoding technique for a first set of one or more physical pages of the 3D memory 500 above the location 116 and may further define a second encoding technique for a second set of one or more physical pages of the 3D memory 500 below the location 116. A second level of the 3D memory 500 may define a first write technique for a third set of one or more physical pages of the 3D memory 500 that are below the second level and may further define a second write technique for a fourth set of one or more physical pages of the 3D memory 500 that are above the second level. A third level of the 3D memory 500 may define a first read technique for a fifth set of one or more physical pages of the 3D memory 500 that are below the third level and may further define a second read technique for a sixth set of one or more physical pages of the 3D memory 500 that are above the third level. A fourth level of the 3D memory 500 may define a first decoding technique for a seventh set of one or more physical pages of the 3D memory 500 that are above the fourth level and may further define a second write technique for an eighth set of one or more physical pages of the 3D memory 500 that are above the fourth level.

[00190] In a particular illustrative embodiment, the location identifier 134 stores indications of storage elements (e.g., the first storage element and the second storage element described with reference to FIG. 1) and measured parameters associated with the storage elements (e.g., the first parameter and the second parameter described with reference to FIG. 1) within the measurements 142. In this case, the location identifier 134 may “track” one or more locations of variations associated with the memory 104. For example, due to physical wear and/or other effects, physical characteristics of the memory 104 may change over an operating life of the data storage device 102, which may add or change locations of variations to the memory 104. Alternatively or in addition, the location identifier 134 may randomly or pseudo-randomly select storage

elements of the memory 104 for measurements. Alternatively or in addition, the location identifier 134 may initially measure parameters for a set of storage elements that includes the first storage element and the second storage element. During one or more subsequent measurement (or “calibration”) operations, the location identifier 134 may “add” additional storage elements of the memory 104 to the set of storage elements and may measure parameters of the additional storage elements (e.g., to increase accuracy of measurement operations as physical wear accrues at the data storage device 102 due to operation of the data storage device 102).

[00191] It should be appreciated that in some cases operations described herein as being performed by the data storage device 102 can be performed by another device, such as a design computer, fabrication equipment, etc. To illustrate, although FIG. 1 describes that the controller 130 may generate the information 146, it should be appreciated that the information 146 may be generated externally to the data storage device 102 and loaded to the data storage device 102 (e.g., via the host interface 170). As an example, the information 146 may be loaded to the data storage device 102 via a firmware update. Alternatively or in addition, the information 146 may be “hard coded” into the data storage device 102, such as by fabricating the data storage device 102 with hardware and/or instructions based on the information 146.

[00192] Although certain structures and operations have been described in combination for convenience of illustration, certain structures and operations may be implemented separately. For example, depending on the particular implementation, the information 146 may be loaded to the controller 130 from an external device, and the location identifier 134 may be omitted from the data storage device 102. Alternatively or in addition, one or more of the ECC parameter table 148 or the memory access parameter table 154 may be omitted from the data storage device 102.

[00193] Although one or more components described herein are illustrated as block components and described in general terms, such components may include one or more microprocessors, state machines, and/or other circuits configured to enable the data storage device 102 (or one or more components thereof) to perform operations described herein. One or more components described herein may be coupled using one or more nodes, one or more buses (e.g., data buses and/or control buses), one or more

other structures, or a combination thereof. One or more components described herein may include one or more physical components, such as hardware controllers, state machines, logic circuits, one or more other structures, or a combination thereof, to enable the data storage device 102 to perform one or more operations described herein. As an illustrative example, the power-up indicator 136 may include a state machine configured to store a value that is adjustable by the controller 130 in response to a power-up event at the data storage device 102.

[00194] Alternatively or in addition, or more aspects of the data storage device 102 may be implemented using a microprocessor or microcontroller programmed (e.g., by executing instructions) to perform operations described herein, such as one or more operations of the methods 700-1500. In a particular embodiment, the data storage device 102 includes a processor executing instructions (e.g., firmware) retrieved from the memory 104. Alternatively or in addition, instructions that are executed by the processor may be retrieved from a separate memory location that is not part of the memory 104, such as at a read-only memory (ROM). One or more operations described herein as being performed by the controller 130 may be performed at the memory 104 (e.g., “in-memory” ECC decoding, as an illustrative example) alternatively or in addition to performing such operations at the controller 130.

[00195] To further illustrate, the controller 130 may include a processor that is configured to execute instructions to perform certain operations (e.g., an algorithm) described herein. The instructions may include general purpose instructions, and the processor may include a general purpose execution unit operable to execute general purpose instructions. The processor may access the instructions from the memory 104, the RAM 144, another memory location, or a combination thereof. The processor may execute the instructions to access information that is stored at the data storage device 102, where the information identifies a location associated with a variation of the structure. As an illustrative example, the processor may execute the instructions to access the information 146 from the memory 104 by sending a read command to the memory 104. The information may be saved at data latches of the memory 104 (e.g., the data latches 1662 and/or the data latches 1702) and then loaded to the RAM 144.

Alternatively or in addition, the processor may execute the instructions to perform one or more other operations described herein.

[00196] The data storage device 102 may be attached to or embedded within one or more host devices, such as within a housing of a host communication device (e.g., the host device 172). For example, the data storage device 102 may be integrated within a packaged apparatus such as a mobile telephone, a computer (e.g., a laptop, a tablet, or a notebook computer), a music player, a video player, a gaming device or console, an electronic book reader, a personal digital assistant (PDA), a portable navigation device, or other device that uses internal non-volatile memory. However, in other embodiments, the data storage device 102 may be implemented in a portable device configured to be selectively coupled to one or more external devices, such as the host device 172.

[00197] To further illustrate, the data storage device 102 may be configured to be coupled to the host device 172 as embedded memory, such as in connection with an embedded MultiMedia Card (eMMC®) (trademark of JEDEC Solid State Technology Association, Arlington, Virginia) configuration, as an illustrative example. The data storage device 102 may correspond to an eMMC device. As another example, the data storage device 102 may correspond to a memory card, such as a Secure Digital (SD®) card, a microSD® card, a miniSD™ card (trademarks of SD-3C LLC, Wilmington, Delaware), a MultiMediaCard™ (MMC™) card (trademark of JEDEC Solid State Technology Association, Arlington, Virginia), or a CompactFlash® (CF) card (trademark of SanDisk Corporation, Milpitas, California). The data storage device 102 may operate in compliance with a JEDEC industry specification. For example, the data storage device 102 may operate in compliance with a JEDEC eMMC specification, a JEDEC Universal Flash Storage (UFS) specification, one or more other specifications, or a combination thereof.

[00198] The memory 104 may include a three-dimensional (3D) memory, a flash memory (e.g., a NAND memory, a NOR memory, a single-level cell (SLC) flash memory, a multi-level cell (MLC) flash memory, a divided bit-line NOR (DINOR) memory, an AND memory, a high capacitive coupling ratio (HiCR) device, an asymmetrical contactless transistor (ACT) device, or another flash memory), an erasable

programmable read-only memory (EPROM), an electrically-erasable programmable read-only memory (EEPROM), a read-only memory (ROM), a one-time programmable memory (OTP), a resistive random access memory (ReRAM), or a combination thereof. Alternatively or in addition, the memory 104 may include another type of memory. The memory 104 may include a semiconductor memory device.

[00199] Semiconductor memory devices include volatile memory devices, such as dynamic random access memory (“DRAM”) or static random access memory (“SRAM”) devices, non-volatile memory devices, such as resistive random access memory (“ReRAM”), electrically erasable programmable read only memory (“EEPROM”), flash memory (which can also be considered a subset of EEPROM), ferroelectric random access memory (“FRAM”), and other semiconductor elements capable of storing information. Each type of memory device may have different configurations. For example, flash memory devices may be configured in a NAND or a NOR configuration.

[00200] The memory devices can be formed from passive and/or active elements, in any combinations. By way of non-limiting example, passive semiconductor memory elements include ReRAM device elements, which in some embodiments include a resistivity switching storage element, such as an anti-fuse, phase change material, etc., and optionally a steering element, such as a diode, etc. Further by way of non-limiting example, active semiconductor memory elements include EEPROM and flash memory device elements, which in some embodiments include elements containing a charge storage region, such as a floating gate, conductive nanoparticles, or a charge storage dielectric material.

[00201] Multiple memory elements may be configured so that they are connected in series or so that each element is individually accessible. By way of non-limiting example, flash memory devices in a NAND configuration (NAND memory) typically contain memory elements connected in series. A NAND memory array may be configured so that the array is composed of multiple strings of memory in which a string is composed of multiple memory elements sharing a single bit line and accessed as a group. Alternatively, memory elements may be configured so that each element is

individually accessible, e.g., a NOR memory array. NAND and NOR memory configurations are exemplary, and memory elements may be otherwise configured.

[00202] The semiconductor memory elements located within and/or over a substrate may be arranged in two or three dimensions, such as a two dimensional memory structure or a three dimensional memory structure. In a two dimensional memory structure, the semiconductor memory elements are arranged in a single plane or a single memory device level. Typically, in a two dimensional memory structure, memory elements are arranged in a plane (e.g., in an x-z direction plane) which extends substantially parallel to a major surface of a substrate that supports the memory elements. The substrate may be a wafer over or in which the layer of the memory elements are formed or it may be a carrier substrate which is attached to the memory elements after they are formed. As a non-limiting example, the substrate may include a semiconductor such as silicon.

[00203] The memory elements may be arranged in the single memory device level in an ordered array, such as in a plurality of rows and/or columns. However, the memory elements may be arrayed in non-regular or non-orthogonal configurations. The memory elements may each have two or more electrodes or contact lines, such as bit lines and word lines.

[00204] A three dimensional memory array is arranged so that memory elements occupy multiple planes or multiple memory device levels, thereby forming a structure in three dimensions (i.e., in the x, y and z directions, where the y direction is substantially perpendicular and the x and z directions are substantially parallel to the major surface of the substrate). As a non-limiting example, a three dimensional memory structure may be vertically arranged as a stack of multiple two dimensional memory device levels. As another non-limiting example, a three dimensional memory array may be arranged as multiple vertical columns (e.g., columns extending substantially perpendicular to the major surface of the substrate, i.e., in the y direction) with each column having multiple memory elements in each column. The columns may be arranged in a two dimensional configuration, e.g., in an x-z plane, resulting in a three dimensional arrangement of memory elements with elements on multiple vertically stacked memory planes. Other

configurations of memory elements in three dimensions can also constitute a three dimensional memory array.

[00205] By way of non-limiting example, in a three dimensional NAND memory array, the memory elements may be coupled together to form a NAND string within a single horizontal (e.g., x-z) memory device levels. Alternatively, the memory elements may be coupled together to form a vertical NAND string that traverses across multiple horizontal memory device levels. Other three dimensional configurations can be envisioned wherein some NAND strings contain memory elements in a single memory level while other strings contain memory elements which span through multiple memory levels. Three dimensional memory arrays may also be designed in a NOR configuration and in a ReRAM configuration.

[00206] Typically, in a monolithic three dimensional memory array, one or more memory device levels are formed above a single substrate. Optionally, the monolithic three dimensional memory array may also have one or more memory layers at least partially within the single substrate. As a non-limiting example, the substrate may include a semiconductor such as silicon. In a monolithic three dimensional array, the layers constituting each memory device level of the array are typically formed on the layers of the underlying memory device levels of the array. However, layers of adjacent memory device levels of a monolithic three dimensional memory array may be shared or have intervening layers between memory device levels.

[00207] Alternatively, two dimensional arrays may be formed separately and then packaged together to form a non-monolithic memory device having multiple layers of memory. For example, non-monolithic stacked memories can be constructed by forming memory levels on separate substrates and then stacking the memory levels atop each other. The substrates may be thinned or removed from the memory device levels before stacking, but as the memory device levels are initially formed over separate substrates, the resulting memory arrays are not monolithic three dimensional memory arrays. Further, multiple two dimensional memory arrays or three dimensional memory arrays (monolithic or non-monolithic) may be formed on separate chips and then packaged together to form a stacked-chip memory device.

[00208] Associated circuitry is typically required for operation of the memory elements and for communication with the memory elements. As non-limiting examples, memory devices may have circuitry used for controlling and driving memory elements to accomplish functions such as programming and reading. This associated circuitry may be on the same substrate as the memory elements and/or on a separate substrate. For example, a controller for memory read-write operations may be located on a separate controller chip and/or on the same substrate as the memory elements.

[00209] One of skill in the art will recognize that this invention is not limited to the two dimensional and three dimensional exemplary structures described but cover all relevant memory structures within the spirit and scope of the invention as described herein and as understood by one of skill in the art. The illustrations of the embodiments described herein are intended to provide a general understanding of the various embodiments. Other embodiments may be utilized and derived from the disclosure, such that structural and logical substitutions and changes may be made without departing from the scope of the disclosure. This disclosure is intended to cover any and all subsequent adaptations or variations of various embodiments. Those of skill in the art will recognize that such modifications are within the scope of the present disclosure.

[00210] The above-disclosed subject matter is to be considered illustrative, and not restrictive, and the appended claims are intended to cover all such modifications, enhancements, and other embodiments, that fall within the scope of the present disclosure. Thus, to the maximum extent allowed by law, the scope of the present invention is to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing detailed description.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
		Application Number	
Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
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Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

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Title of the Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		
Attorney Docket Number	SDA-2117-T1-US	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
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Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
		Application Number	
Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

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Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
		Application Number	
Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

Authorization to Permit Access:☒ Authorization to Permit Access to the Instant Application by the Participating Offices

If checked, the undersigned hereby grants the USPTO authority to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the World Intellectual Property Office (WIPO), and any other intellectual property offices in which a foreign application claiming priority to the instant patent application is filed access to the instant patent application. See 37 CFR 1.14(c) and (h). This box should not be checked if the applicant does not wish the EPO, JPO, KIPO, WIPO, or other intellectual property office in which a foreign application claiming priority to the instant patent application is filed to have access to the instant patent application.

In accordance with 37 CFR 1.14(h)(3), access will be provided to a copy of the instant patent application with respect to: 1) the instant patent application-as-filed; 2) any foreign application to which the instant patent application claims priority under 35 U.S.C. 119(a)-(d) if a copy of the foreign application that satisfies the certified copy requirement of 37 CFR 1.55 has been filed in the instant patent application; and 3) any U.S. application-as-filed from which benefit is sought in the instant patent application.

In accordance with 37 CFR 1.14(c), access may be provided to information concerning the date of filing this Authorization.

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

☒ Assignee☐ Legal Representative under 35 U.S.C. 117☐ Joint Inventor☐ Person to whom the inventor is obligated to assign.☐ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor: If the Applicant is an Organization check here. ☒

Organization Name

SANDISK TECHNOLOGIES INC.

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
		Application Number	
Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

Mailing Address Information For Applicant:			
Address 1		TWO LEGACY TOWN CENTER	
Address 2		6900 NORTH DALLAS PARKWAY	
City		PLANO	State/Province TX
Country	US	Postal Code	75024
Phone Number		Fax Number	
Email Address			
Additional Applicant Data may be generated within this form by selecting the Add button.			

Assignee Information including Non-Applicant Assignee Information:

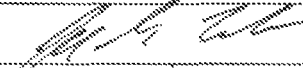
Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City			State/Province	
Country		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.				

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	SDA-2117-T1-US
		Application Number	
Title of Invention	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

Signature:

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications.					
Signature				Date (YYYY-MM-DD)	2014-05-08
First Name	JEFFREY G	Last Name	TOLER	Registration Number	36342
Additional Signature may be generated within this form by selecting the Add button.					

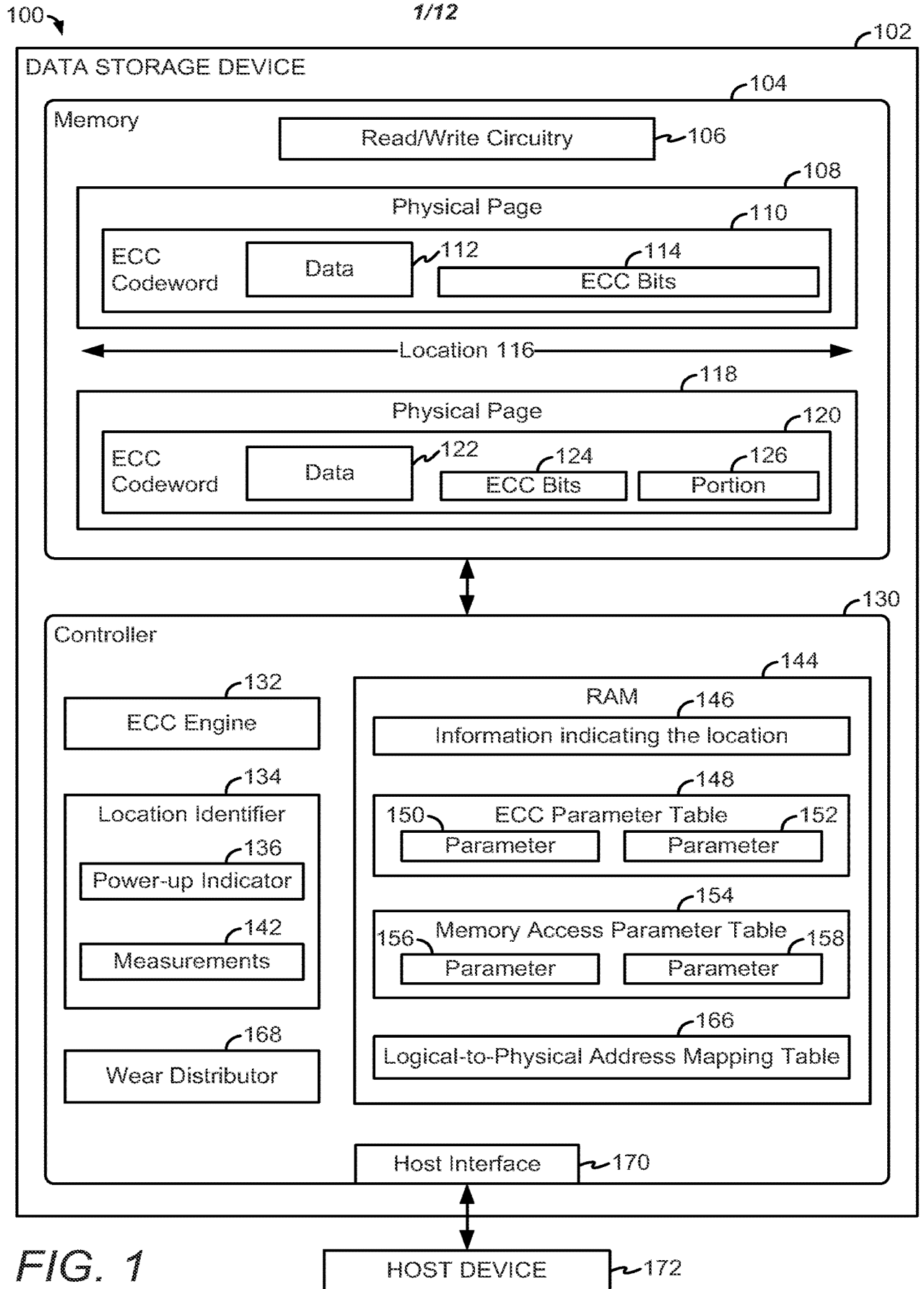
This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



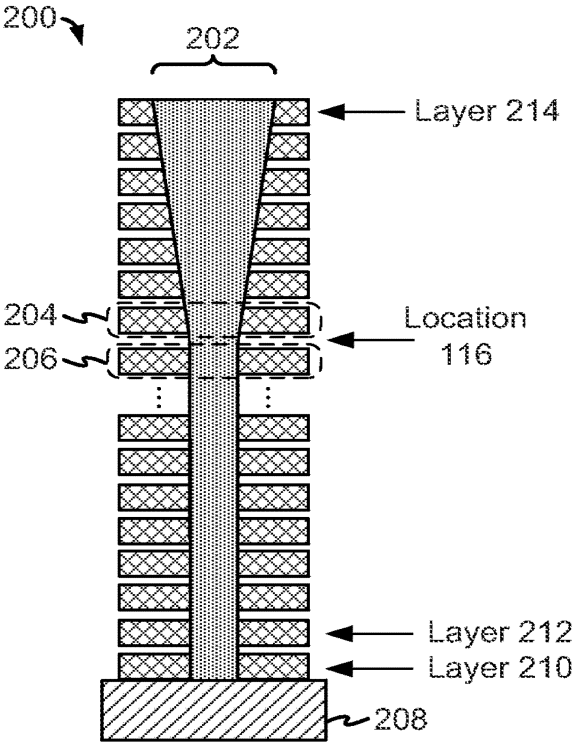


FIG. 2

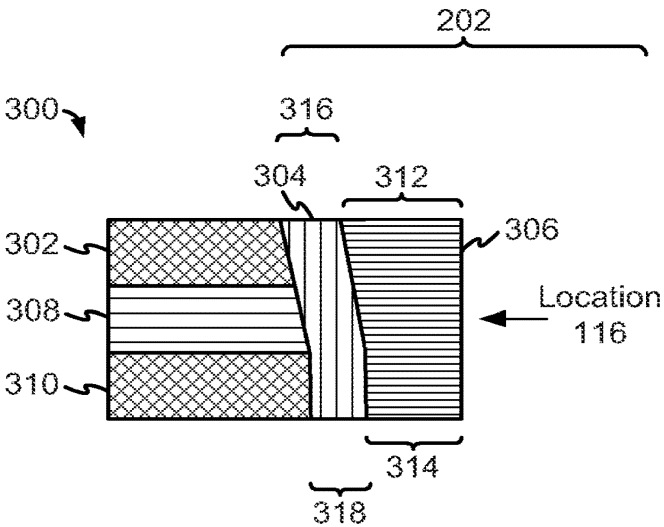


FIG. 3

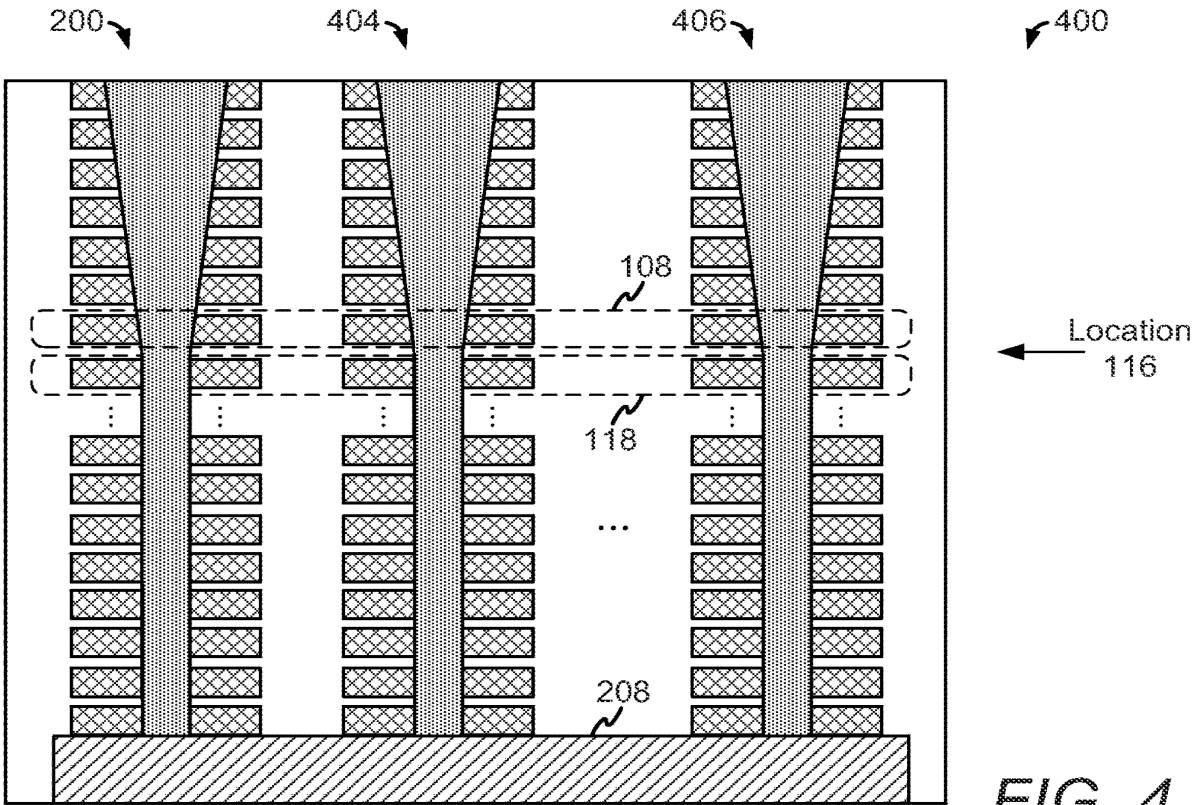


FIG. 4

3/12

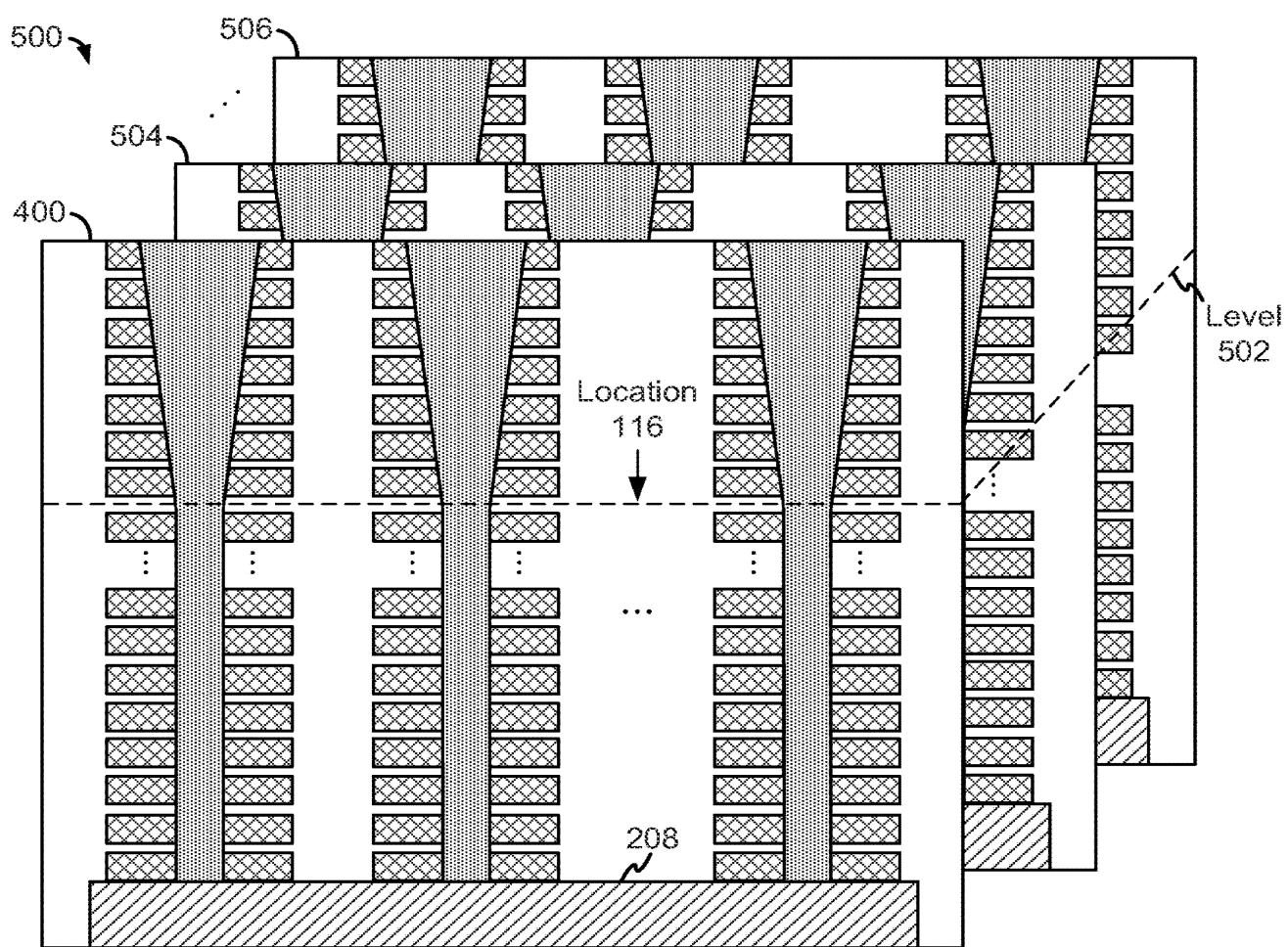


FIG. 5

600

Table	
Block	Location of Variation
602 0	WL _k 604
606 5	WL _{_(k+1)} 608
⋮	⋮
610 N	WL _{_(k+2)} 612

FIG. 6

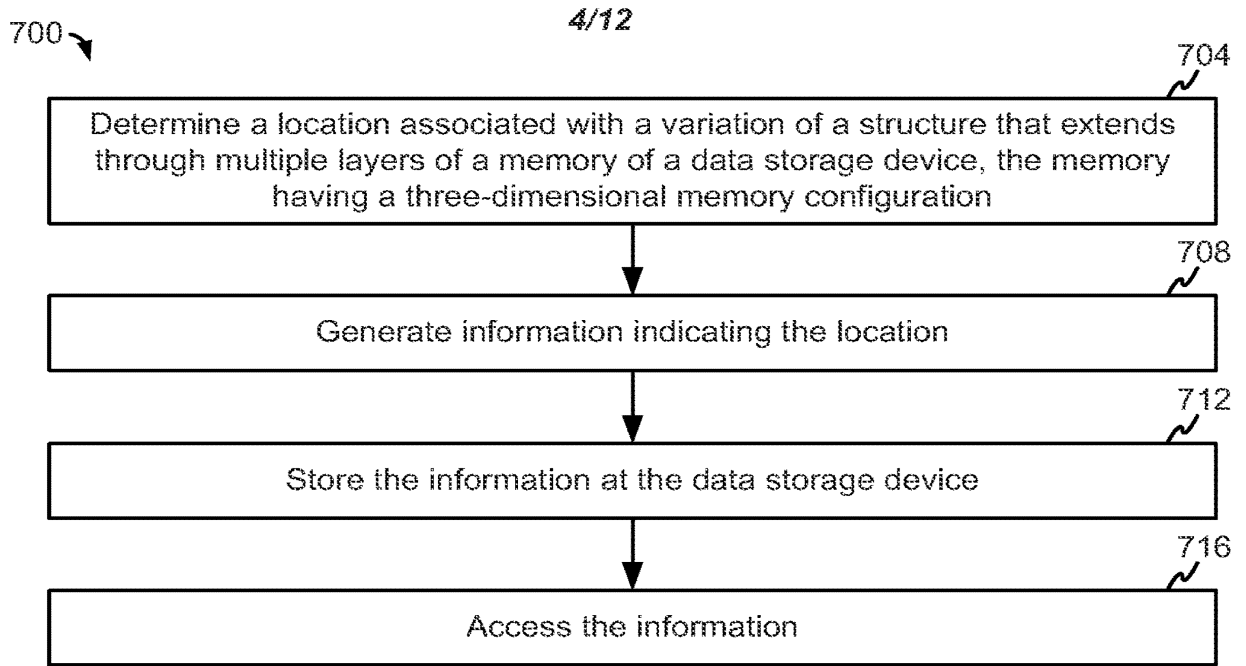


FIG. 7

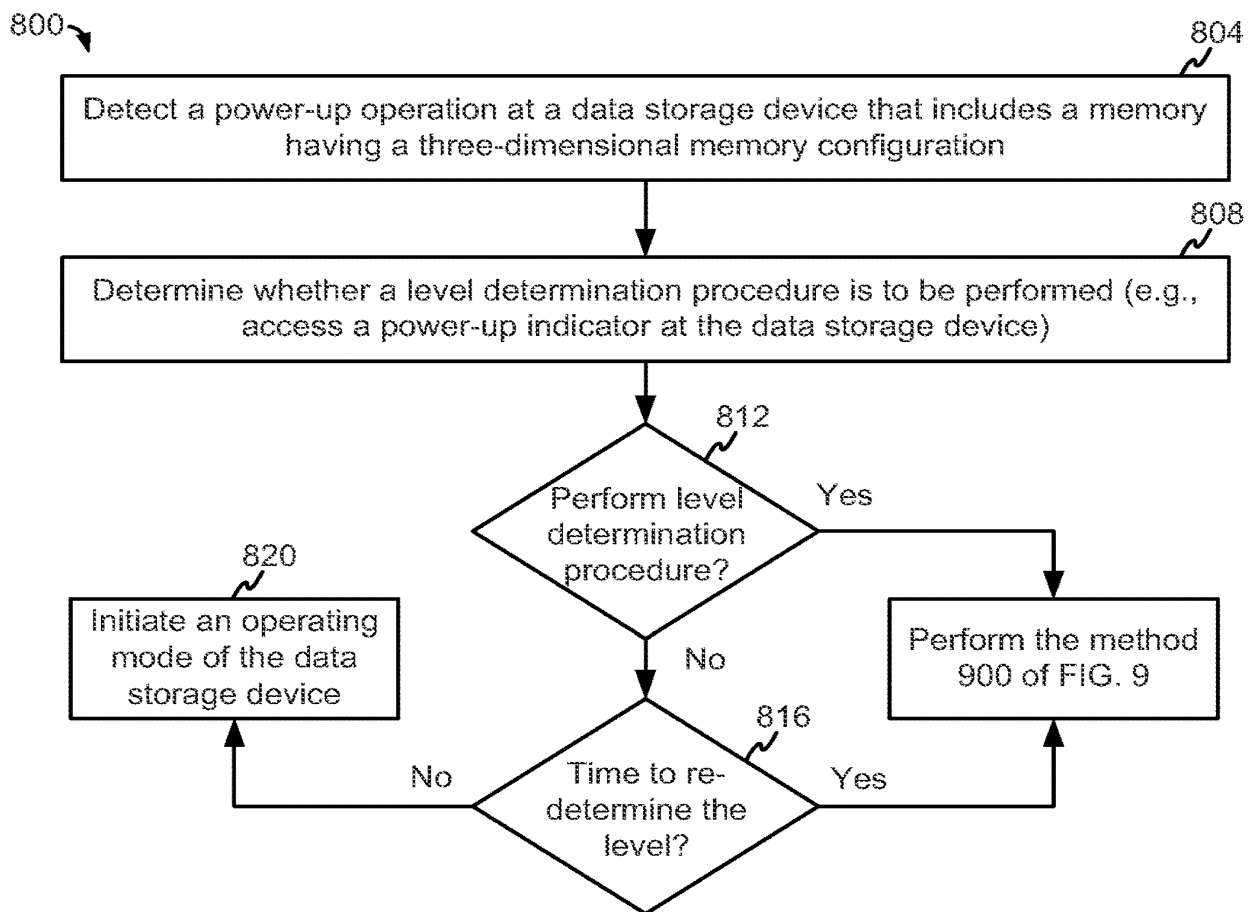


FIG. 8

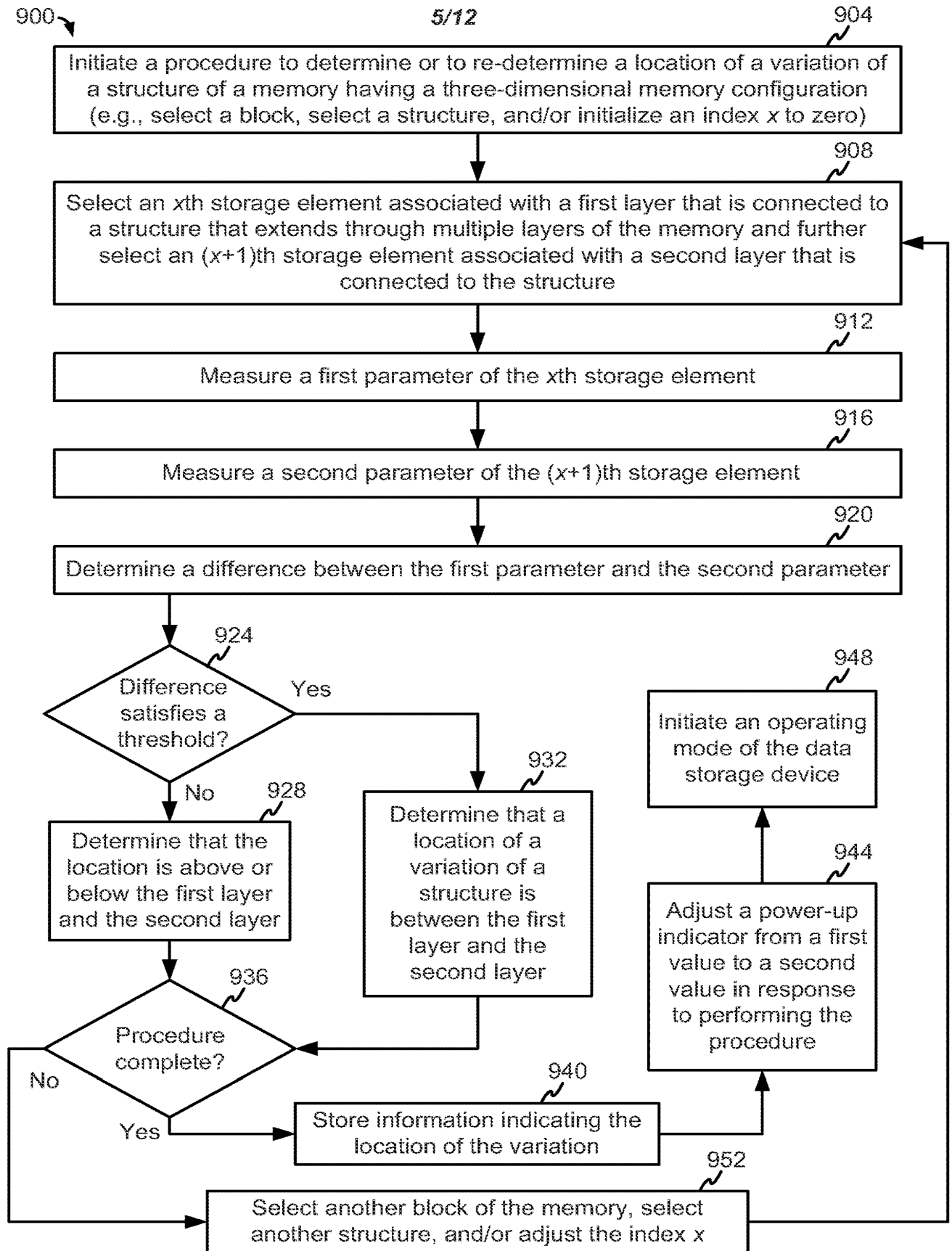


FIG. 9

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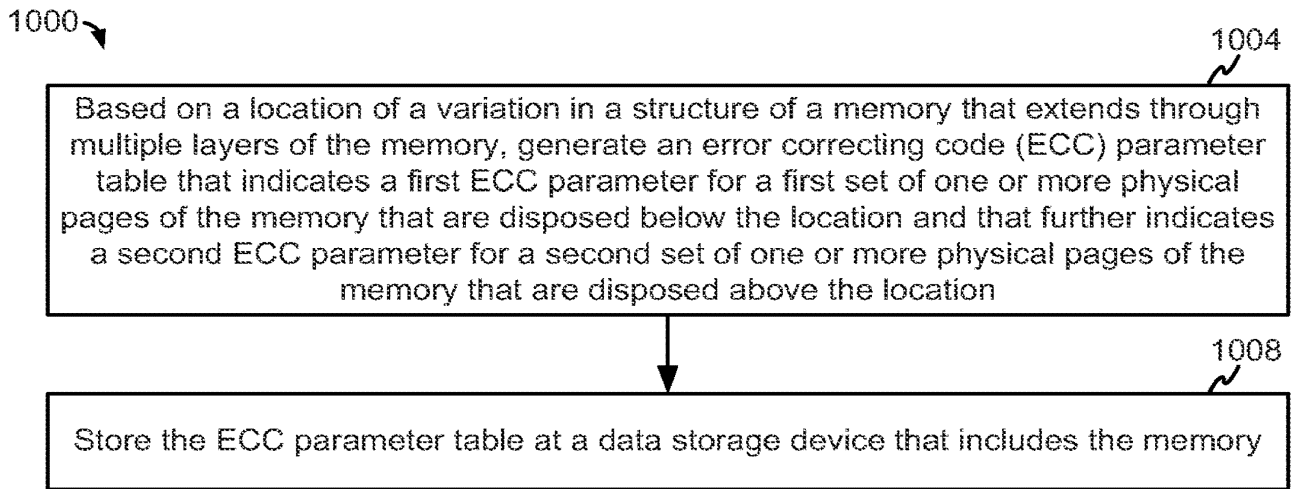


FIG. 10

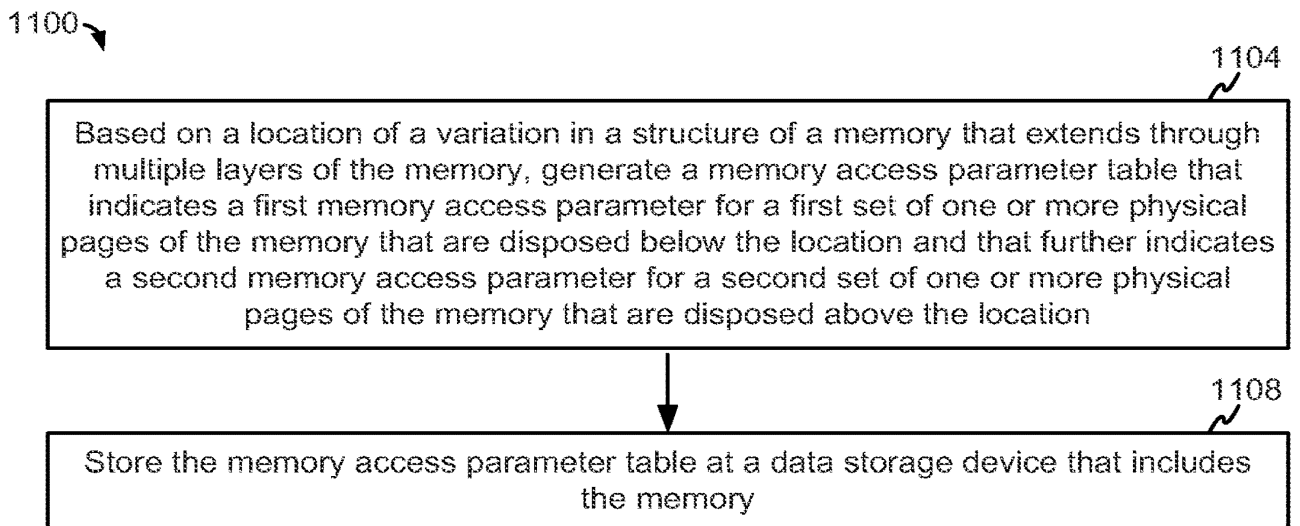


FIG. 11

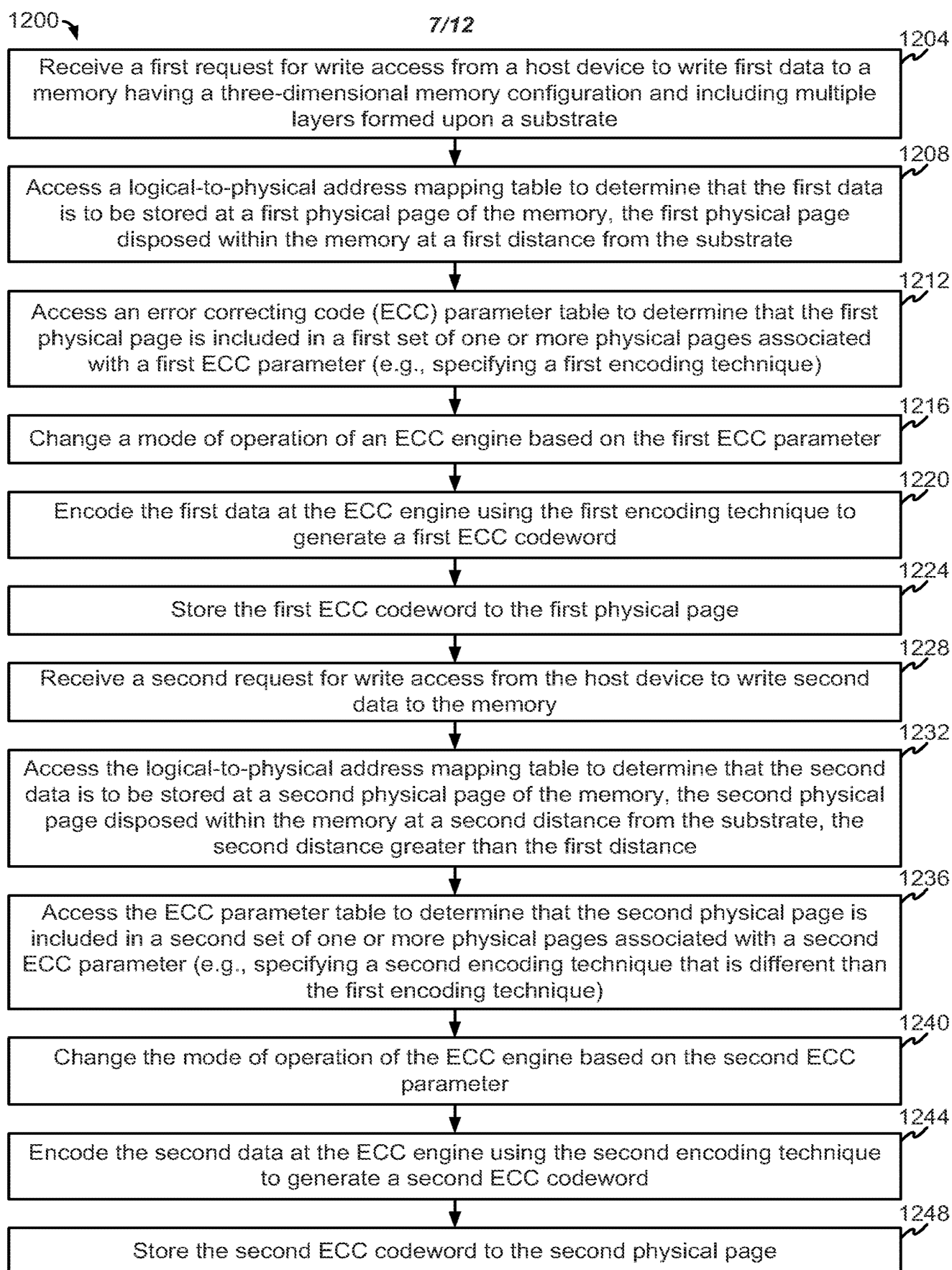


FIG. 12

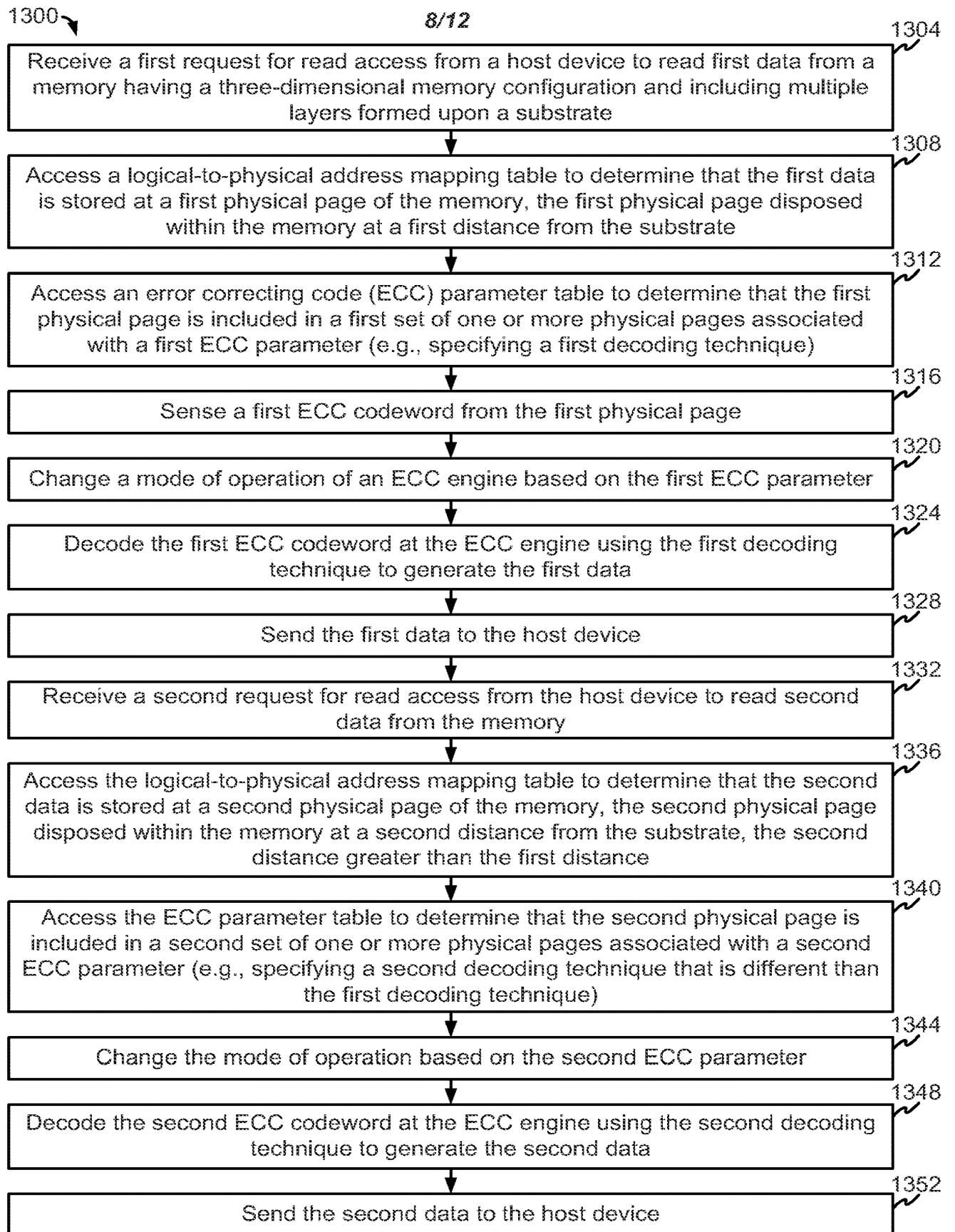


FIG. 13

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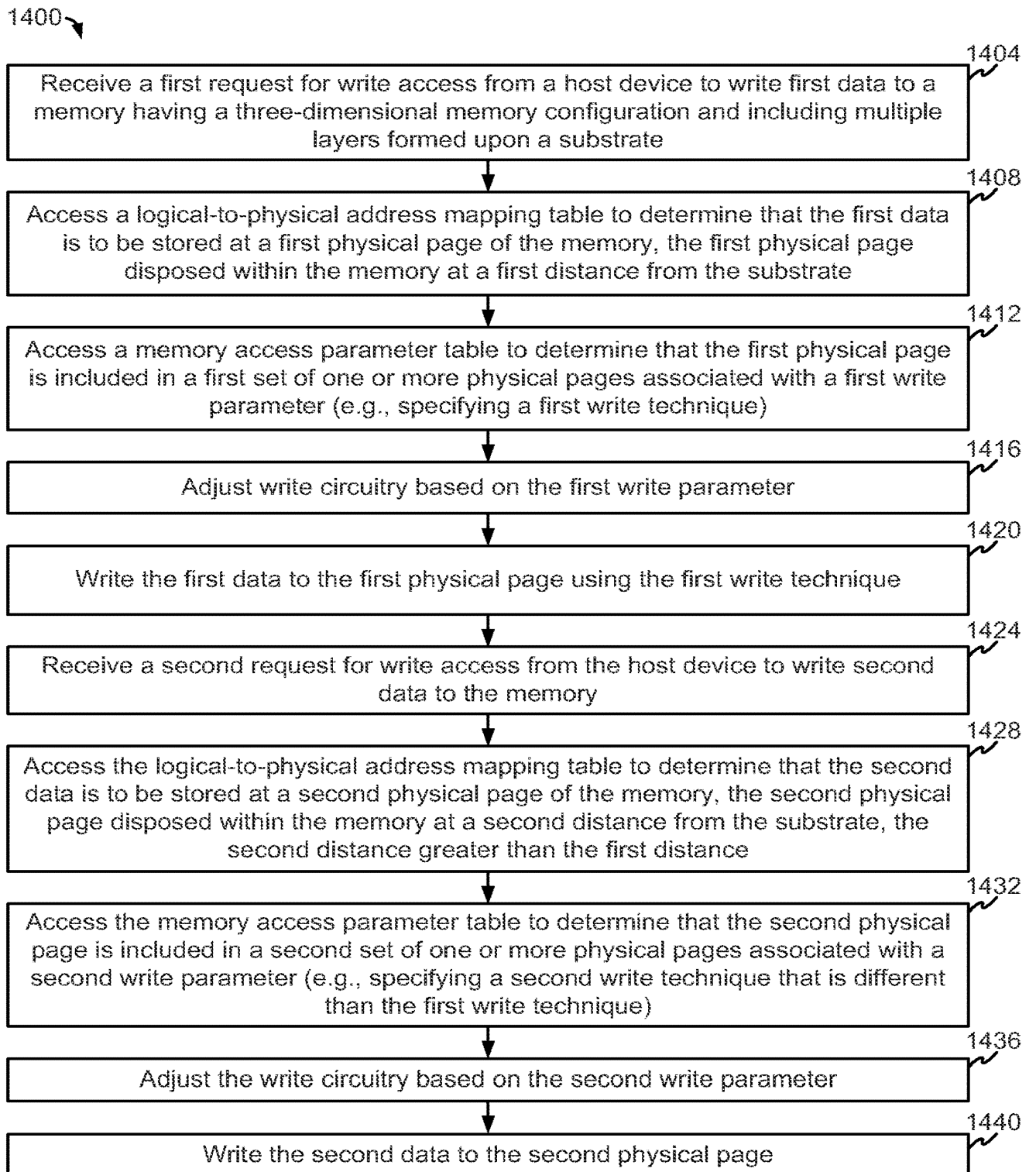
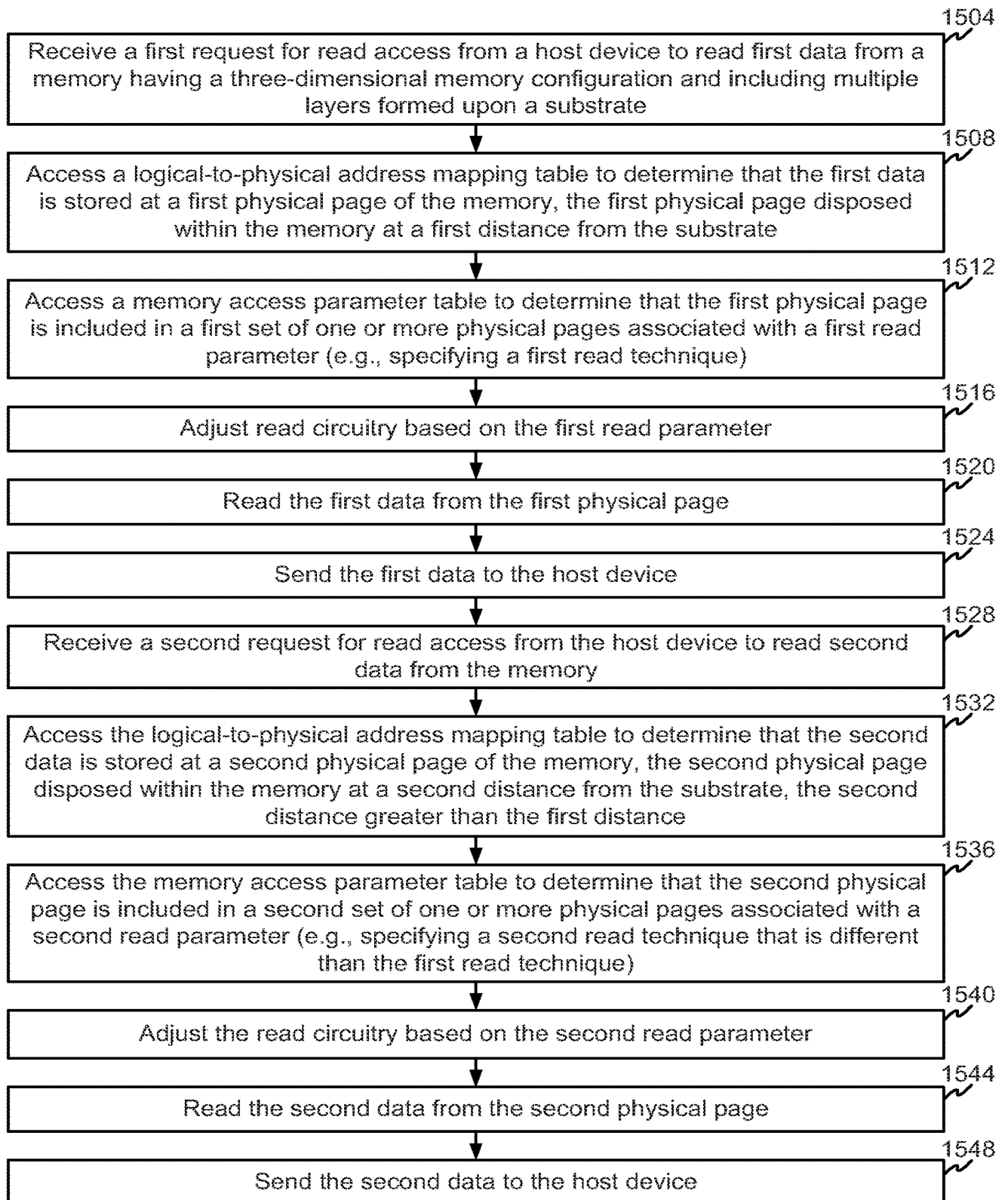


FIG. 14

1500 ↗

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**FIG. 15**

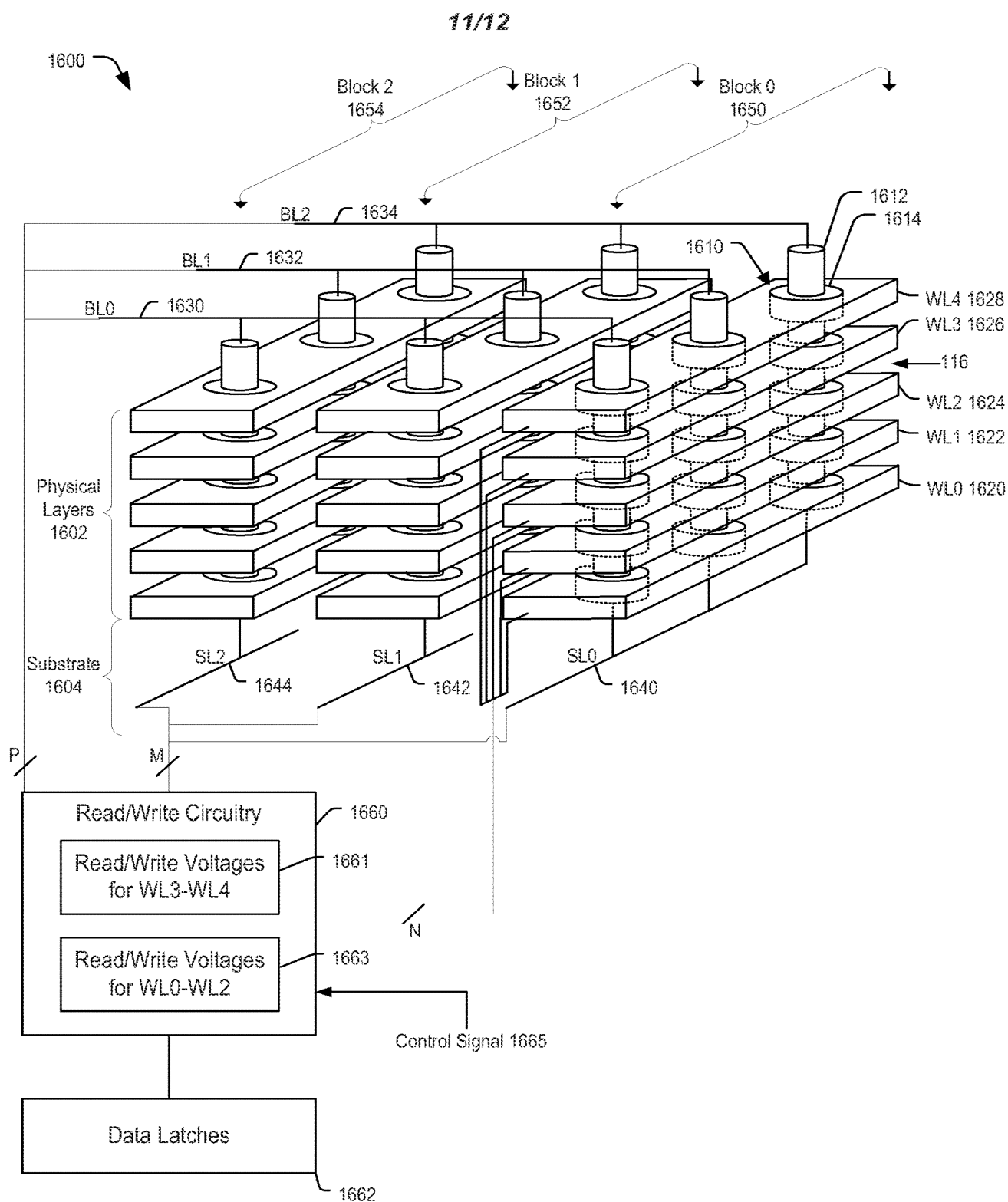


FIG. 16

12/12

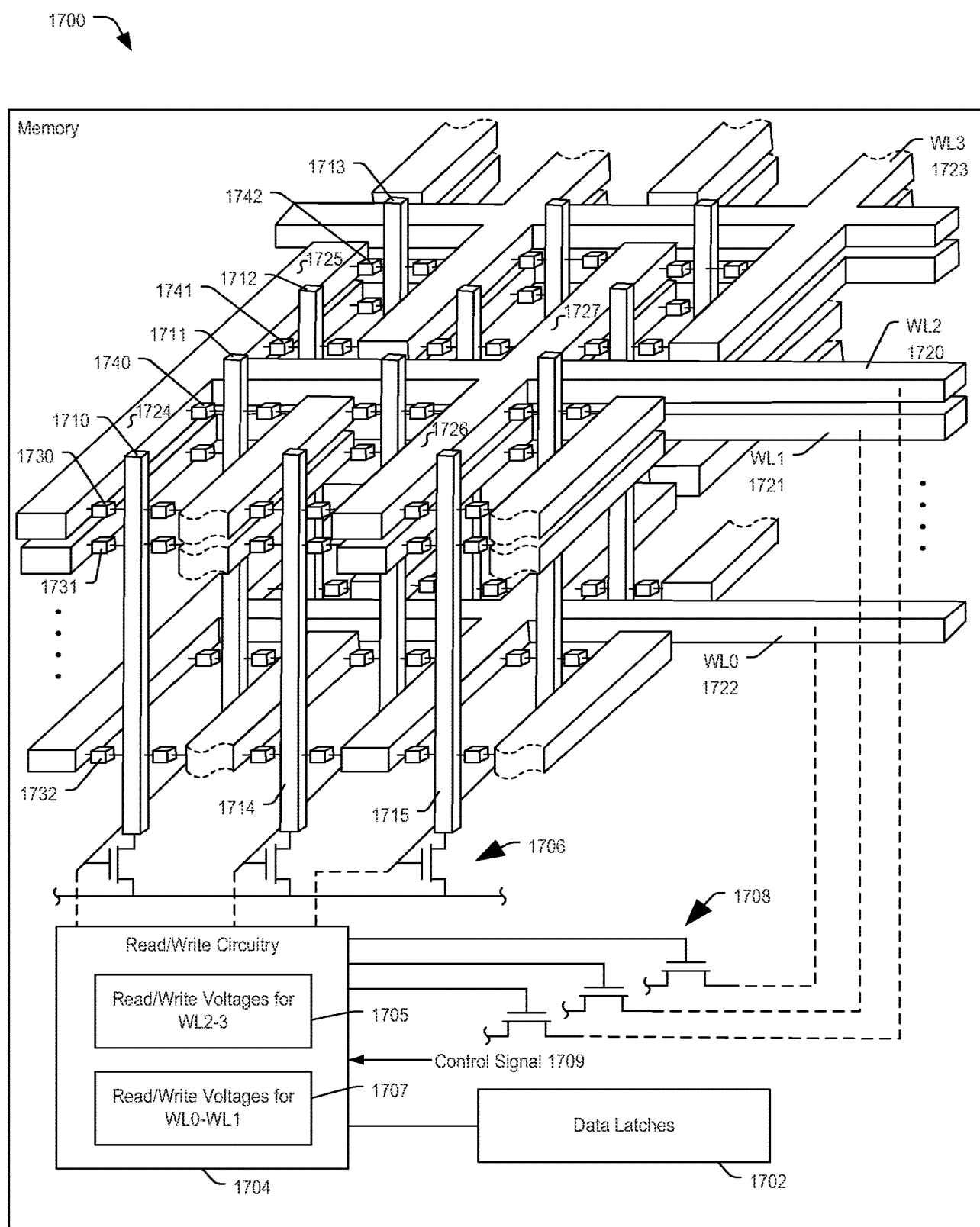


FIG. 17

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original and sole inventor (if only one name is listed below) or an original and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

which (check) ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____
☐ and was amended on _____ (if applicable).

I hereby state that the above-identified application was made or was authorized to be made by me.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

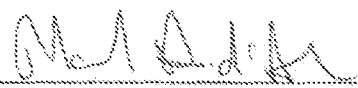
I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose

information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

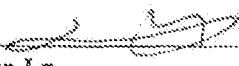
Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom. I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

Full name of sole (or joint) inventor: **Manuel Antonio D'ABREU**

Inventor's Signature:  Date: 5/8/2014
 Residence: **2166 Huntington Circle**
El Dorado Hills, CA 95762
 Post Office Address: same Citizenship: US

Full name of sole (or joint) inventor: **Xinde HU**

Inventor's Signature:  Date: 05/08/2014
 Residence: **12292 Blanton Ln.**
San Diego, CA 92128
 Post Office Address: same Citizenship: CN

WHAT IS CLAIMED IS:

1. A method comprising:
in a data storage device that includes a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory, performing:
storing information at the data storage device, the information identifying a location associated with a variation of the structure; and
accessing the information.
2. The method of claim 1, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation corresponds to a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.
3. The method of claim 1, further comprising:
measuring a first parameter of a first storage element associated with a first layer of the memory;
measuring a second parameter of a second storage element associated with a second layer of the memory; and
determining whether a difference between the first parameter and the second parameter satisfies a threshold.
4. The method of claim 3, wherein the first parameter corresponds to a first number of programming pulses applied to the first storage element to program the first storage element to a particular threshold voltage, and wherein the second parameter corresponds to a second number of programming pulses applied to the second storage element to program the second storage element to the particular threshold voltage.
5. The method of claim 3, further comprising determining that the location is above the first layer and the second layer in response to determining that the difference fails to satisfy the threshold.

6. The method of claim 3, wherein the difference satisfies the threshold, and further comprising determining that the location is between the first layer and the second layer in response to determining that the difference satisfies the threshold.

7. The method of claim 1, wherein the information is generated in response to an initial power-up of the data storage device.

8. The method of claim 1, further comprising adjusting a power-up indicator stored at the data storage device from a first value to a second value after determining the location.

9. The method of claim 6, further comprising
in response to determining the location, generating the information; and
storing the information at the data storage device.

10. The method of claim 9, wherein the data storage device further includes a controller that is operationally coupled to the memory, wherein the information is stored at the memory, and wherein the controller accesses the information from the memory.

11. The method of claim 1, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and wherein the data storage device further includes circuitry associated with operation of the memory cells.

12. A data storage device comprising:
a memory having a three-dimensional (3D) memory configuration and including
a structure extending through multiple layers of the memory; and
a controller coupled to the memory, wherein the controller is configured to
access information that is stored at the memory, the information
identifying a location associated with a variation of the structure.

13. The data storage device of claim 12, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation is a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

14. The data storage device of claim 12, wherein the controller is further configured to measure a first parameter of a first storage element associated with a first layer of the memory, to measure a second parameter of a second storage element associated with a second layer of the memory, and to determine whether a difference between the first parameter and the second parameter satisfies a threshold.

15. The data storage device of claim 14, wherein the first parameter corresponds to a first number of programming pulses applied to the first storage element to program the first storage element to a particular threshold voltage, and wherein the second parameter corresponds to a second number of programming pulses applied to the second storage element to program the second storage element to the particular threshold voltage.

16. The data storage device of claim 14, wherein the difference fails to satisfy the threshold, and wherein the controller is further configured to determine that the location is above the first layer and the second layer in response to determining that the difference fails to satisfy the threshold.

17. The data storage device of claim 14, wherein the difference satisfies the threshold, and wherein the controller is further configured to determine that the location is between the first layer and the second layer in response to determining that the difference satisfies the threshold.

18. The data storage device of claim 17, wherein the controller is further configured to generate the information in response to an initial power-up of the data storage device.

19. The data storage device of claim 12, wherein the controller is further configured to generate the information in response to determining the location and to store the information at the memory.

20. The data storage device of claim 12, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and further comprising circuitry associated with operation of the memory cells.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		
First Named Inventor/Applicant Name:		MANUEL ANTONIO D'ABREU		
Filer:		Jeffrey G. Toler/Katherine Meals		
Attorney Docket Number:		SDA-2117-T1-US		
Filed as Large Entity				
Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	280	280
Utility Search Fee	1111	1	600	600
Utility Examination Fee	1311	1	720	720
Request for Prioritized Examination	1817	1	4000	4000
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				5740

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

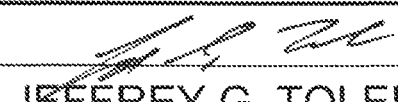
1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

**CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION
UNDER 37 CFR 1.102(e) (Page 1 of 1)**

First Named Inventor:	Manuel Antonio d'Abreu	Nonprovisional Application Number (if known):	
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1), the prioritized examination fee set forth in 37 CFR 1.17(c), and if not already paid, the publication fee set forth in 37 CFR 1.18(d) have been filed with the request. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.
2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims.
3. The applicable box is checked below:
 - I. ☒ **Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)**
 - i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.
---OR---
(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.
 - ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, or the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.
 - II. ☐ **Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)**
 - i. A request for continued examination has been filed with, or prior to, this form.
 - ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
 - iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
 - iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
 - v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature 	Date <u>5-8-2014</u>
Name (Print/Typed) JEFFREY G. TOLER	Practitioner Registration Number 38342
<i>Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.*</i>	
☒ *Total of <u>1</u> forms are submitted.	

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 14/273,031	
APPLICATION AS FILED - PART I							
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA		RATE(\$)	FEE(\$)		RATE(\$)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A			N/A
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A			N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A			N/A
TOTAL CLAIMS (37 CFR 1.16(i))	20	minus 20 =	*				x 80 =
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2	minus 3 =	*				x 420 =
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL			TOTAL 1600
APPLICATION AS AMENDED - PART II							
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY	
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		OR OTHER THAN SMALL ENTITY	
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	MINUS	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=
	Application Size Fee (37 CFR 1.16(s))						
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.							



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
14/273,031	05/08/2014	2189	1600	SDA-2117-T1-US	20	2

CONFIRMATION NO. 1165

71591
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

FILING RECEIPT



Date Mailed: 05/23/2014

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

MANUEL ANTONIO D'ABREU, EL DORADO HILLS, CA;
XINDE HU, SAN DIEGO, CA;

Applicant(s)

SANDISK TECHNOLOGIES INC., PLANO, TX

Assignment For Published Patent Application

SANDISK TECHNOLOGIES INC., PLANO, TX

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access - A proper **Authorization to Permit Access to Application by Participating Offices** (PTO/SB/39 or its equivalent) has been received by the USPTO.

If Required, Foreign Filing License Granted: 05/22/2014

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 14/273,031**

Projected Publication Date: 11/12/2015

Non-Publication Request: No

Early Publication Request: No

Title

STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL
MEMORY CONFIGURATION

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

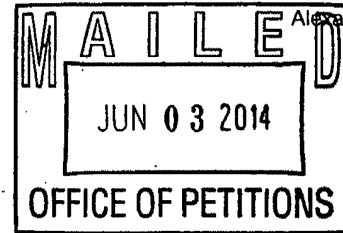
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Doc Code: TRACK1.GRANT

Decision Granting Request for Prioritized Examination (Track I or After RCE)	Application No.: 14/273,031
1. THE REQUEST FILED <u>May 8, 2014</u> IS GRANTED. The above-identified application has met the requirements for prioritized examination A. ☒ for an original nonprovisional application (Track I). B. ☐ for an application undergoing continued examination (RCE). 2. The above-identified application will undergo prioritized examination. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs: A. filing a <u>petition for extension of time</u> to extend the time period for filing a reply; B. filing an <u>amendment to amend the application to contain more than four independent claims, more than thirty total claims</u>, or a multiple dependent claim; C. filing a <u>request for continued examination</u>; D. filing a notice of appeal; E. filing a request for suspension of action; F. mailing of a notice of allowance; G. mailing of a final Office action; H. completion of examination as defined in 37 CFR 41.102; or I. abandonment of the application. Telephone inquiries with regard to this decision should be directed to Irvin Dingle at (571)272-3210, Office of Petitions. Irvin Dingle <u>/Irvin Dingle/</u> [Signature] <u>Paralegal Specialist</u> (Title)	

Issue Classification 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

CPC						
Symbol					Type	Version
G06F		11	/	1072	F	2013-01-01
G11C		29	/	04	I	2013-01-01
G11C		16	/	0466	I	2013-01-01
H01L		27	/	11578	I	2013-01-01
H01L		27	/	11568	I	2013-01-01
H01L		29	/	7923	I	2013-01-01
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			/			
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CPC Combination Sets					
Symbol		Type	Set	Ranking	Version

NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/JOHN LANE/ Primary Examiner.Art Unit 2189	08/11/2014	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 1 and 7

Issue Classification 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

☐ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
5	5														
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7	9														
8	10														
11	11														
12	12														
13	13														
14	14														
15	15														
16	16														

NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/JOHN LANE/ Primary Examiner.Art Unit 2189	08/11/2014	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 1 and 7



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BIB DATA SHEET

CONFIRMATION NO. 1165

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/273,031	05/08/2014	711	2189	SDA-2117-T1-US		
APPLICANTS SANDISK TECHNOLOGIES INC., PLANO, TX, Assignee (with 37 CFR 1.172 Interest); INVENTORS MANUEL ANTONIO D'ABREU, EL DORADO HILLS, CA; XINDE HU, SAN DIEGO, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/22/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JOHN A LANE/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 12	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS TOLER LAW GROUP 8500 BLUFFSTONE COVE, SUITE A201 AUSTIN, TX 78759 UNITED STATES						
TITLE STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Search Notes 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	103,154, 170	08/11/2014	JAL
365	185.12, 189.09		
714	773		

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text search with and w/o limited classified search of class/sub in "SEARCHED" section	08/11/2014	JAL

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	103,154, 170	08/11/2014	JAL
365	185.12, 189.09		
714	773		

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Notice of References Cited	Application/Control No. 14/273,031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.	
	Examiner JOHN LANE	Art Unit 2189	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2012/0284589	11-2012	Kim et al.	714/785
*	B	US-2011/0238884	09-2011	Sutardja, Pantas	711/1
*	C	US-8,737,130	05-2014	D'Abreu et al.	365/185.18
*	D	US-2010/0332923	12-2010	D'ABREU et al.	714/708
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	5091	((variation or taper\$5 or etch\$5 or trap\$5 or layer\$5) with (location or spot or point or area) with (structur\$5 or physical\$5 or substrate or material) with (stor\$5 or record\$5 or maintain\$5)).ab.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:32
L2	5569	((variation or taper\$5 or etch\$5 or trap\$5 or layer\$5) with (location or spot or point or area) with (structur\$5 or physical\$5 or substrate or material) with (stor\$5 or record\$5 or maintain\$5)).clm.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:32
L3	86157	"711"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:33
L4	121091	"365"/\$.ccls.	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:34
L5	201974	3 or 4	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:34
L6	814	1 and 2	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:34
L7	43	5 and 6	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 10:34
L8	5	7 AND ((H01L29/7887).CPC.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 11:34
L9	7	7 AND ((H01L29/7923).CPC.)	US-PGPUB; USPAT; EPO; JPO; IBM_TDB	OR	ON	2014/07/31 11:35

7/31/2014 11:36:49 AM



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NOTICE OF ALLOWANCE AND FEE(S) DUE

71591 7590 08/22/2014
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

EXAMINER

LANE, JOHN A

ART UNIT

PAPER NUMBER

2189

DATE MAILED: 08/22/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/273,031

05/08/2014

MANUEL ANTONIO D'ABREU

SDA-2117-T1-US

1165

TITLE OF INVENTION: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional

UNDISCOUNTED

\$960

\$0

\$0

\$960

11/24/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or **Fax** (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

71591 7590 08/22/2014
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165

TITLE OF INVENTION: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	11/24/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
LANE, JOHN A	2189	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165

71591	7590	08/22/2014
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TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

EXAMINER	
LANE, JOHN A	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 08/22/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/273,031	Applicant(s) D'ABREU ET AL.	
	Examiner JOHN LANE	Art Unit 2189	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the application filed 05/08/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)	5. ☒ Examiner's Amendment/Comment
2. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/JOHN LANE/ Primary Examiner, Art Unit 2189	
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EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The present application, filed on or after March 16, 2013, has been examined under the first inventor to file provisions of the AIA.

The application has been amended as follows:

In the Specification:

In paragraph [0001]:

On line 1, after "No." insert ---14/273,005---.

On line 4, delete "(Attorney Docket No. SDA-2116-US)".

On line 5, after "No." insert ---14/272,951---.

On lines 7-8, delete "(Attorney Docket No. SDA-2118-US)".

Statement of Reason for Allowance

2. The following is an examiner's statement of reasons for allowance:

The art of record neither teaches nor fairly suggests the method and device of independent claims 1 and 12 respectively, including the following **combination of** limitations defining the main invention/embodiment:

In a data storage device that includes a memory...and...a structure extending through multiple layers...

Storing information at the data storage device, the information identifying a location associated with a variation of the structure.

Accessing the information.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Claims 1-20 are allowable over the prior art of record.

Any response to this action should be mailed to:

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for Official communications intended for entry)

Or:

(571) 273-4208, (for Non-Official or draft communications, please label "Non-Official" or "DRAFT")

Or:

Via e-mail at Jack.Lane@uspto.gov (for Non-Official or Draft communications, please label "Non-Official" or "DRAFT")

Art Unit: 2189

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reg Bragdon can be reached on 571 272-4204.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100.

**/Jack A Lane/
Primary Examiner, Art Unit 2189**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Manuel Antonio d'Abreu et al.

Title: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A
THREE-DIMENSIONAL MEMORY CONFIGURATION

App. No.: 14/273,031

Filed: May 8, 2014

Examiner: Unknown

Group Art Unit: 2189

Atty. Dkt. No.: SDA-2117-T1-US

Confirmation No: 1165

Customer No.: 71591

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

POWER OF ATTORNEY

I hereby appoint the practitioners at Customer Number **71591** to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

CHANGE OF CORRESPONDENCE ADDRESS

Please change the correspondence address for the above-identified application to the address associated with Customer Number 71591.

STATEMENT UNDER 37 CFR 3.73(b)

SanDisk Technologies Inc., a Texas Corporation, states that it is the Assignee of the entire right, title and interest in the patent application/patent identified above by virtue of an assignment from the inventors of the patent application identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 032851, Frame 0941, or for which a copy thereof is attached. The undersigned, whose title is supplied below, is authorized to act on behalf of the Assignee.

September 4, 2014
Date


E. Earle Thompson
Managing Director

Electronic Acknowledgement Receipt

EFS ID:	20200146
Application Number:	14273031
International Application Number:	
Confirmation Number:	1165
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU
Customer Number:	71591
Filer:	Jeffrey G. Toler/Suzanne Schultz
Filer Authorized By:	Jeffrey G. Toler
Attorney Docket Number:	SDA-2117-T1-US
Receipt Date:	22-SEP-2014
Filing Date:	08-MAY-2014
Time Stamp:	11:18:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	SDA-2117-T1-US_POA.pdf	55161 3823907418e708082e5db0dabaa08d71ffa85627	no	1

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US

71591
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

CONFIRMATION NO. 1165
POA ACCEPTANCE LETTER



Date Mailed: 09/26/2014

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 09/22/2014.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/hgray/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Electronic Patent Application Fee Transmittal				
Application Number:		14273031		
Filing Date:		08-May-2014		
Title of Invention:		STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION		
First Named Inventor/Applicant Name:		MANUEL ANTONIO D'ABREU		
Filer:		Jeffrey G. Toler/Suzanne Nobert		
Attorney Docket Number:		SDA-2117-T1-US		
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Request for Continued Examination	1801	1	1200	1200
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	20734651
Application Number:	14273031
International Application Number:	
Confirmation Number:	1165
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU
Customer Number:	71591
Filer:	Jeffrey G. Toler/Suzanne Nobert
Filer Authorized By:	Jeffrey G. Toler
Attorney Docket Number:	SDA-2117-T1-US
Receipt Date:	18-NOV-2014
Filing Date:	08-MAY-2014
Time Stamp:	18:52:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	5133
Deposit Account	502469
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	SDA-2117-T1-US_RCE.pdf	697280	no	3
			627adaf14021b3dea639b4f221ddf545ccd5299c		
Warnings:					
Information:					
2		SDA-2117-T1-US_Amendment.pdf	224282	yes	7
			b40556fa1d9822324b263e240a06f3aa5eca5347		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Specification		2	2	
	Claims		3	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SDA-2117-T1-US_IDS.pdf	612504	no	4
			c5ab6e9882c0242bf620696cb39687dcfdb0e303		
Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	13272951_NFOA_8-1-14.pdf	291553	no	7
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Information:					
5	Other Reference-Patent/App/Search documents	14273005_NFOA_10-10-14.pdf	227685	no	6
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Warnings:					
Information:					

6	Non Patent Literature	Arya.pdf	1776949	no	11
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8	Other Reference-Patent/App/Search documents	14272951_App_5-8-14.pdf	2790728	no	75
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Warnings:					
Information:					
9	Non Patent Literature	Jang.pdf	1652810	no	2
			a7f921d996cc3f756a7c4f1ad914a75aad8f75bf		
Warnings:					
Information:					
10	Non Patent Literature	Nowak.pdf	421765	no	2
			f1b25aa9a64cb9edde4b1c5c97ce861165148688		
Warnings:					
Information:					
11	Non Patent Literature	Walker.pdf	2175244	no	7
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Warnings:					
Information:					
12	Fee Worksheet (SB06)	fee-info.pdf	30282	no	2
			20ad8452be0fe8b042ba9fcb164ed2efb86c0181		
Warnings:					
Information:					
Total Files Size (in bytes):			13031301		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	20734651
Application Number:	14273031
International Application Number:	
Confirmation Number:	1165
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU
Customer Number:	71591
Filer:	Jeffrey G. Toler/Suzanne Nobert
Filer Authorized By:	Jeffrey G. Toler
Attorney Docket Number:	SDA-2117-T1-US
Receipt Date:	18-NOV-2014
Filing Date:	08-MAY-2014
Time Stamp:	18:52:44
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	5133
Deposit Account	502469
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	SDA-2117-T1-US_RCE.pdf	697280	no	3
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Warnings:					
Information:					
2		SDA-2117-T1-US_Amendment.pdf	224282	yes	7
			b40556fa1d9822324b263e240a06f3aa5eca5347		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment Submitted/Entered with Filing of CPA/RCE		1	1	
	Specification		2	2	
	Claims		3	6	
	Applicant Arguments/Remarks Made in an Amendment		7	7	
Warnings:					
Information:					
3	Information Disclosure Statement (IDS) Form (SB08)	SDA-2117-T1-US_IDS.pdf	612504	no	4
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Warnings:					
Information:					
4	Other Reference-Patent/App/Search documents	13272951_NFOA_8-1-14.pdf	291553	no	7
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Warnings:					
Information:					
5	Other Reference-Patent/App/Search documents	14273005_NFOA_10-10-14.pdf	227685	no	6
			8af68fdd37b507c11de0f14633323e7dad2e83f0		
Warnings:					
Information:					

6	Non Patent Literature	Arya.pdf	1776949	no	11
			a5de6e439a4d567f0bb6900f8e24f9886cf1aa8f		
Warnings:					
Information:					
7	Other Reference-Patent/App/Search documents	14273005_App_5-8-14.pdf	2130219	no	75
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Information:					
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9	Non Patent Literature	Jang.pdf	1652810	no	2
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Warnings:					
Information:					
10	Non Patent Literature	Nowak.pdf	421765	no	2
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Warnings:					
Information:					
11	Non Patent Literature	Walker.pdf	2175244	no	7
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Warnings:					
Information:					
12	Fee Worksheet (SB06)	fee-info.pdf	30282	no	2
			20ad8452be0fe8b042ba9fcb164ed2efb86c0181		
Warnings:					
Information:					
Total Files Size (in bytes):			13031301		

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National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14273031
	Filing Date		2014-05-08
	First Named Inventor	Manuel Antonio d'Abreu	
	Art Unit	2189	
	Examiner Name	John A. Lane	
Attorney Docket Number		SDA-2117-T1-US	

U.S. PATENTS						Remove		
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Patent citation information please click the Add button.						Add		
U.S. PATENT APPLICATION PUBLICATIONS						Remove		
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	20140059406	A1	2014-02-27	HYUN et al.			
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add		
FOREIGN PATENT DOCUMENTS						Remove		
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add
NON-PATENT LITERATURE DOCUMENTS								Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14273031
	Filing Date		2014-05-08
	First Named Inventor	Manuel Antonio d'Abreu	
	Art Unit	2189	
	Examiner Name	John A. Lane	
	Attorney Docket Number	SDA-2117-T1-US	

1	Non-Final Office Action mailed August 1, 2014 in U.S. Application No. 14/272,951 (Attorney Docket No. SDA-2118-T1-US), 7 pages.	☐
2	Non-Final Office Action mailed October 10, 2014 in U.S. Application No. 14/273,005 (Attorney Docket No. SDA-2116-T1-US), 6 pages.	☐
3	ARYA, "A Survey of 3D NAND Flash Memory", http://lpsoc.eic.nctu.edu.tw/courses/MS2012Autumn/term/Report/3D%20Nand%20Flash%20Memory%20-%20PranavArya(0160814).pdf , March 19, 2013, 11 pages.	☐
4	D'ABREU et al., "Error Correcting Code Techniques for a Memory Having a Three-Dimensional Memory Configuration," U.S. Application No. 14/273,005 filed May 8, 2014 (Attorney Docket No. SDA-2116-T1-US), 75 pages.	☐
5	D'ABREU et al., "Memory Access Techniques for a Memory Having a Three-Dimensional Memory Configuration," U.S. Application No. 14/272,951 filed May 8, 2014 (Attorney Docket No. SDA-2118-T1-US), 75 pages.	☐
6	JANG et al., "Vertical Cell Array Using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory," IEEE, 2009 Symposium on VLSI Technology Digest of Technical Papers, Honolulu, HI, June 16-18, 2009, pp. 192-193.	☐
7	NOWAK et al., "Intrinsic Fluctuations in Vertical NAND Flash Memories," IEEE, 2012 Symposium on VLSI Technology Digest of Technical Papers, Honolulu, HI, June 12-14, 2012, pp. 21-22.	☐
8	WALKER, "A Rigorous 3-D NAND Flash Cost Analysis," IEEE Transactions on Semiconductor Manufacturing, Vol. 26, No. 4, November 2013, pp. 619-625.	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14273031
Filing Date	2014-05-08
First Named Inventor	Manuel Antonio d'Abreu
Art Unit	2189
Examiner Name	John A. Lane
Attorney Docket Number	SDA-2117-T1-US

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey G. Toler/	Date (YYYY-MM-DD)	2014-11-18
Name/Print	Jeffrey G. Toler	Registration Number	38,342

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Manuel Antonio d'Abreu et al.

Title: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A
THREE-DIMENSIONAL MEMORY CONFIGURATION

App. No.: 14/273,031

Filed: May 8, 2014

Examiner: Lane, John A.

Group Art Unit: 2189

Atty. Dkt. No.: SDA-2117-T1-US

Confirmation No: 1165

Customer No.: 71591

Mail Stop: RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**SUBMISSION ACCOMPANYING REQUEST FOR CONTINUED
EXAMINATION PURSUANT TO 37 C.F.R. § 1.114**

Dear Sir:

This Amendment is being submitted following the Notice of Allowance mailed on August 22, 2014. Applicant is filing a Request for Continued Examination (RCE) in order to have the present response considered.

REMARKS

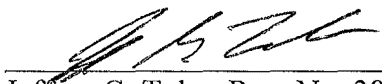
Applicant thanks the Examiner for the Notice of Allowance mailed August 22, 2014. The specification and claims 9 and 10 have been amended. No new matter has been added. Applicant respectfully submits that the application remains in condition for allowance.

CONCLUSION

The Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-2469.

Respectfully submitted,

10-18-2014
Date



Jeffrey G. Toler, Reg. No. 38,342
Toler Law Group, PC
8500 Bluffstone Cove, Suite A201
Austin, TX 78759
Telephone: (512) 327-5515
Facsimile: (512) 327-5575

SPECIFICATION AMENDMENTS

Please amend the specification as indicated:

Please replace paragraph [0001] with the following amended paragraph:

[0001] This application is related to U.S. Patent Application No. _____, No. 14/273,005, filed concurrently herewith and entitled “ERROR CORRECTING CODE TECHNIQUES FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION,” (~~Attorney Docket No. SDA-2116-US~~), and is further related to U.S. Patent Application No. _____, No. 14/272,951, filed concurrently herewith and entitled “MEMORY ACCESS TECHNIQUES FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION,” (~~Attorney Docket No. SDA-2118-US~~), each disclosure of which is incorporated herein by reference in its entirety.

**REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)**

Application Number	14273031	Filing Date	2014-05-08	Docket Number (if applicable)	SDA-2117-T1-US	Art Unit	2189
First Named Inventor	Manuel Antonio d'Abreu			Examiner Name	LANE, John A.		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 502469

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Doc code: RCEX

Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (07-09)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Jeffrey G. Toler/	Date (YYYY-MM-DD)	2014-11-18
Name	Jeffrey G. Toler	Registration Number	38342

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

CLAIM AMENDMENTS

1. (Original) A method comprising:
in a data storage device that includes a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory, performing:
storing information at the data storage device, the information identifying a location associated with a variation of the structure; and
accessing the information.
2. (Original) The method of claim 1, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation corresponds to a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.
3. (Original) The method of claim 1, further comprising:
measuring a first parameter of a first storage element associated with a first layer of the memory;
measuring a second parameter of a second storage element associated with a second layer of the memory; and
determining whether a difference between the first parameter and the second parameter satisfies a threshold.
4. (Original) The method of claim 3, wherein the first parameter corresponds to a first number of programming pulses applied to the first storage element to program the first storage element to a particular threshold voltage, and wherein the second parameter corresponds to a second number of programming pulses applied to the second storage element to program the second storage element to the particular threshold voltage.

5. (Original) The method of claim 3, further comprising determining that the location is above the first layer and the second layer in response to determining that the difference fails to satisfy the threshold.

6. (Original) The method of claim 3, wherein the difference satisfies the threshold, and further comprising determining that the location is between the first layer and the second layer in response to determining that the difference satisfies the threshold.

7. (Original) The method of claim 1, wherein the information is generated in response to an initial power-up of the data storage device.

8. (Original) The method of claim 1, further comprising adjusting a power-up indicator stored at the data storage device from a first value to a second value after determining the location.

9. (Currently amended) The method of claim 6, further comprising:
in response to determining the location, generating the information; and
storing the information at the data storage device.

10. (Currently amended) The method of claim [[9,]] 1, wherein the data storage device further includes a controller that is operationally coupled to the memory, wherein the information is stored at the memory, and wherein the controller accesses the information from the memory.

11. (Original) The method of claim 1, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and wherein the data storage device further includes circuitry associated with operation of the memory cells.

12. (Original) A data storage device comprising:
a memory having a three-dimensional (3D) memory configuration and including a structure extending through multiple layers of the memory; and
a controller coupled to the memory, wherein the controller is configured to access information that is stored at the memory, the information identifying a location associated with a variation of the structure.

13. (Original) The data storage device of claim 12, wherein the structure includes a conductive channel and a charge trap structure, and wherein the variation is a difference between a first width of the structure at a first distance from a substrate of the memory and a second width of the structure at a second distance from the substrate, the second distance greater than the first distance.

14. (Original) The data storage device of claim 12, wherein the controller is further configured to measure a first parameter of a first storage element associated with a first layer of the memory, to measure a second parameter of a second storage element associated with a second layer of the memory, and to determine whether a difference between the first parameter and the second parameter satisfies a threshold.

15. (Original) The data storage device of claim 14, wherein the first parameter corresponds to a first number of programming pulses applied to the first storage element to program the first storage element to a particular threshold voltage, and wherein the second parameter corresponds to a second number of programming pulses applied to the second storage element to program the second storage element to the particular threshold voltage.

16. (Original) The data storage device of claim 14, wherein the difference fails to satisfy the threshold, and wherein the controller is further configured to determine that the location is above the first layer and the second layer in response to determining that the difference fails to satisfy the threshold.

17. (Original) The data storage device of claim 14, wherein the difference satisfies the threshold, and wherein the controller is further configured to determine that the location is between the first layer and the second layer in response to determining that the difference satisfies the threshold.

18. (Original) The data storage device of claim 17, wherein the controller is further configured to generate the information in response to an initial power-up of the data storage device.

19. (Original) The data storage device of claim 12, wherein the controller is further configured to generate the information in response to determining the location and to store the information at the memory.

20. (Original) The data storage device of claim 12, wherein the memory is a non-volatile memory that is monolithically formed in one or more physical levels of arrays of memory cells having an active area disposed above a silicon substrate, and further comprising circuitry associated with operation of the memory cells.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 14/273,031		Filing Date 05/08/2014		☐ To be Mailed	
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (j), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$	=
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$	=
☐ APPLICATION SIZE FEE (37 CFR 1.16(s)) If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
11/18/2014	CLAIMS REMAINING AFTER AMENDMENT							
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X \$80 =	0	
	Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X \$420 =	0	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE						0		

AMENDMENT	(Column 1)	(Column 2)	(Column 3)	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	
	CLAIMS REMAINING AFTER AMENDMENT							
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$	=	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$	=	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
TOTAL ADD'L FEE								

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

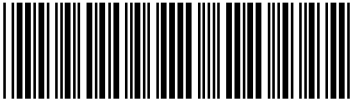
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

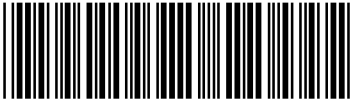
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Issue Classification 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

CPC						
Symbol					Type	Version
G06F		11	/	1072	F	2013-01-01
G11C		29	/	04	I	2013-01-01
G11C		16	/	0466	I	2013-01-01
H01L		27	/	11578	I	2013-01-01
H01L		27	/	11568	I	2013-01-01
H01L		29	/	7923	I	2013-01-01
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CPC Combination Sets						
Symbol			Type	Set	Ranking	Version

NONE	Total Claims Allowed: 20		
(Assistant Examiner)	(Date)		
/JOHN LANE/ Primary Examiner.Art Unit 2189	12/02/2014	O.G. Print Claim(s) 1	O.G. Print Figure 1 and 7
(Primary Examiner)	(Date)		

Issue Classification 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

☐ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
3	3	19	19												
4	4	20	20												
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15	15														
16	16														

NONE	Total Claims Allowed: 20	
(Assistant Examiner)	(Date)	
/JOHN LANE/ Primary Examiner.Art Unit 2189	12/02/2014	O.G. Print Claim(s) 1
(Primary Examiner)	(Date)	O.G. Print Figure 1 and 7

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14273031	
	Filing Date		2014-05-08	
	First Named Inventor	Manuel Antonio d'Abreu		
	Art Unit	2189		
	Examiner Name	John A. Lane		
	Attorney Docket Number	SDA-2117-T1-US		

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	1	20140059406	A1	2014-02-27	HYUN et al.			
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14273031	14273031 - GAU: 2139
	Filing Date		2014-05-08	
	First Named Inventor	Manuel Antonio d'Abreu		
	Art Unit	2189		
	Examiner Name	John A. Lane		
	Attorney Docket Number	SDA-2117-T1-US		

1	Non-Final Office Action mailed August 1, 2014 in U.S. Application No. 14/272,951 (Attorney Docket No. SDA-2118-T1-US), 7 pages.	☐
2	Non-Final Office Action mailed October 10, 2014 in U.S. Application No. 14/273,005 (Attorney Docket No. SDA-2116-T1-US), 6 pages.	☐
3	ARYA, "A Survey of 3D NAND Flash Memory", http://lpsoc.eic.nctu.edu.tw/courses/MS2012Autumn/term/Report/3D%20Nand%20Flash%20Memory%20-%20PranavArya(0160814).pdf , March 19, 2013, 11 pages.	☐
4	D'ABREU et al., "Error Correcting Code Techniques for a Memory Having a Three-Dimensional Memory Configuration," U.S. Application No. 14/273,005 filed May 8, 2014 (Attorney Docket No. SDA-2116-T1-US), 75 pages.	☐
5	D'ABREU et al., "Memory Access Techniques for a Memory Having a Three-Dimensional Memory Configuration," U.S. Application No. 14/272,951 filed May 8, 2014 (Attorney Docket No. SDA-2118-T1-US), 75 pages.	☐
6	JANG et al., "Vertical Cell Array Using TCAT (Terabit Cell Array Transistor) Technology for Ultra High Density NAND Flash Memory," IEEE, 2009 Symposium on VLSI Technology Digest of Technical Papers, Honolulu, HI, June 16-18, 2009, pp. 192-193.	☐
7	NOWAK et al., "Intrinsic Fluctuations in Vertical NAND Flash Memories," IEEE, 2012 Symposium on VLSI Technology Digest of Technical Papers, Honolulu, HI, June 12-14, 2012, pp. 21-22.	☐
8	WALKER, "A Rigorous 3-D NAND Flash Cost Analysis," IEEE Transactions on Semiconductor Manufacturing, Vol. 26, No. 4, November 2013, pp. 619-625.	☐

If you wish to add additional non-patent literature document citation information please click the Add button **Add**

EXAMINER SIGNATURE

Examiner Signature	/John Lane/	Date Considered	12/02/2014
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.



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CONFIRMATION NO. 1165

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/273,031	05/08/2014	711	2139	SDA-2117-T1-US		
APPLICANTS SANDISK TECHNOLOGIES INC., PLANO, TX, Assignee (with 37 CFR 1.172 Interest); INVENTORS MANUEL ANTONIO D'ABREU, EL DORADO HILLS, CA; XINDE HU, SAN DIEGO, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/22/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/JOHN A LANE/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 12	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 2
ADDRESS TOLER LAW GROUP 8500 BLUFFSTONE COVE, SUITE A201 AUSTIN, TX 78759 UNITED STATES						
TITLE STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION						
FILING FEE RECEIVED 1600	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		



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NOTICE OF ALLOWANCE AND FEE(S) DUE

71591 7590 12/09/2014
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

EXAMINER

LANE, JOHN A

ART UNIT

PAPER NUMBER

2139

DATE MAILED: 12/09/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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14/273,031

05/08/2014

MANUEL ANTONIO D'ABREU

SDA-2117-TI-US

1165

TITLE OF INVENTION: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
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nonprovisional

UNDISCOUNTED

\$960

\$0

\$0

\$960

03/09/2015

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
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INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

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(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165

TITLE OF INVENTION: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	03/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
LANE, JOHN A	2139	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
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2 _____
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3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

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Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

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- ☐ Publication Fee (No small entity discount permitted)
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5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165

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EXAMINER	
LANE, JOHN A	

ART UNIT	PAPER NUMBER
2139	

DATE MAILED: 12/09/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/273,031	Applicant(s) D'ABREU ET AL.	
	Examiner JOHN LANE	Art Unit 2139	AIA (First Inventor to File) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to the RCE and amendment filed 11/18/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 1-20. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some *c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)	5. ☐ Examiner's Amendment/Comment
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>11/18/14(2 pages)</u>	6. ☒ Examiner's Statement of Reasons for Allowance
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material	7. ☐ Other _____.
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	

/JOHN LANE/ Primary Examiner, Art Unit 2139	
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Statement of Reason for Allowance

1. The following is an examiner's statement of reasons for allowance:

The art of record neither teaches nor fairly suggests the method and device of independent claims 1 and 12 respectively, including the following **combination of** limitations defining the main invention/embodiment:

In a data storage device that includes a memory...and...a structure extending through multiple layers...

Storing information at the data storage device, the information identifying a location associated with a variation of the structure.

Accessing the information.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

2. Claims 1-20 are allowable over the prior art of record.

Any response to this action should be mailed to:

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

or faxed to:

(571) 273-8300, (for Official communications intended for entry)

Or:

(571) 273-4208, (for Non-Official or draft communications, please label

Art Unit: 2139

"Non-Official" or "DRAFT")

Or:

Via e-mail at Jack.Lane@uspto.gov (for Non-Official or Draft communications, please label "Non-Official or "DRAFT")

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reg Bragdon can be reached on 571 272-4204.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100.

**/Jack A Lane/
Primary Examiner, Art Unit 2189**

Search Notes 	Application/Control No. 14273031	Applicant(s)/Patent Under Reexamination D'ABREU ET AL.
	Examiner JOHN LANE	Art Unit 2189

CPC- SEARCHED		
Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
711	103,154, 170	08/11/2014	JAL
365	185.12, 189.09		
714	773		

SEARCH NOTES		
Search Notes	Date	Examiner
EAST text search with and w/o limited classified search of class/sub in "SEARCHED" section	08/11/2014	JAL
EAST to date.	12/02/2014	JAL

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	103,154, 170	08/11/2014	JAL
365	185.12, 189.09		
714	773		

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Electronic Acknowledgement Receipt

EFS ID:	21545460
Application Number:	14273031
International Application Number:	
Confirmation Number:	1165
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU
Customer Number:	71591
Filer:	Jeffrey G. Toler/Suzanne Nobert
Filer Authorized By:	Jeffrey G. Toler
Attorney Docket Number:	SDA-2117-T1-US
Receipt Date:	19-FEB-2015
Filing Date:	08-MAY-2014
Time Stamp:	16:32:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 960
RAM confirmation Number	3352
Deposit Account	502469
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)
Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	SDA-2117-T1-US_Issue_Fee.pdf	124503	no	1
			c98fb44930ea42b4ba8871774fd787dc836a3d9		

Warnings:

Information:

2	Fee Worksheet (SB06)	fee-info.pdf	30826	no	2
			a6b2961ee3234d29fa3fae238902cf5e3cdb1c74		

Warnings:

Information:

Total Files Size (in bytes):	155329
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

71591 7590 12/09/2014
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165

TITLE OF INVENTION: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$960	\$0	\$0	\$960	03/09/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
LANE, JOHN A	2139	711-170000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 TOLER LAW GROUP, PC

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

SANDISK TECHNOLOGIES INC.

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PLANO, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 502469 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

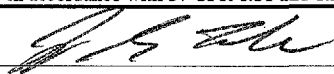
NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature



Date

2-19-2015

Typed or printed name JEFFREY G. TOLER

Registration No. 38342

Electronic Patent Application Fee Transmittal

Application Number:	14273031			
Filing Date:	08-May-2014			
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION			
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU			
Filer:	Jeffrey G. Toler/Suzanne Nobert			
Attorney Docket Number:	SDA-2117-T1-US			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	1501	1	960	960

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	03/31/2015	8996838	SDA-2117-T1-US	1165

71591 7590 03/11/2015
TOLER LAW GROUP
8500 BLUFFSTONE COVE, SUITE A201
AUSTIN, TX 78759

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

MANUEL ANTONIO D'ABREU, EL DORADO HILLS, CA;
SANDISK TECHNOLOGIES INC., PLANO, TX, Assignee (with 37 CFR 1.172 Interest);
XINDE HU, SAN DIEGO, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

Electronic Acknowledgement Receipt

EFS ID:	24741645
Application Number:	14273031
International Application Number:	
Confirmation Number:	1165
Title of Invention:	STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATION
First Named Inventor/Applicant Name:	MANUEL ANTONIO D'ABREU
Customer Number:	71591
Filer:	Jeffrey G. Toler/Tina Hall
Filer Authorized By:	Jeffrey G. Toler
Attorney Docket Number:	SDA-2117-T1-US
Receipt Date:	27-JAN-2016
Filing Date:	08-MAY-2014
Time Stamp:	16:32:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	SDA-2117-T1-US_RequestforCOC_COC.pdf	161502 b5a4c876f20769ffac059b97f419f14f4013ec85	no	4

Warnings:

Information:

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Manuel Antonio D'Abreu et al.
Assignee: SanDisk Technologies Inc.
Title: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A
THREE-DIMENSIONAL MEMORY CONFIGURATION
Patent No.: 8,996,838 B1 Issued: March 31, 2015
Atty. Docket No.: SDA-2117-T1-US Confirmation No. : 1165
Customer No.: 71591

Certificate of Correction Branch
Office of Patent Publication
COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT—
USPTO ERROR (37 C.F.R. § 1.322(a))**

Dear Sir:

In accordance with the provisions of 35 U.S.C. § 254 and 37 C.F.R. § 1.322(a), it is respectfully requested that a Certificate of Correction be issued to correct the following error:

In the Claims

In the Claims section, Claim 8 (Column 36, Line 63) "The method of claim 7, wherein the data storage device" should be --The method of claim 1, wherein the data storage device--.

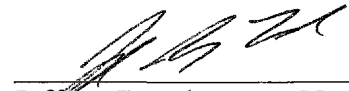
Claim 8 appears correctly in the Request for Continued Examination Pursuant (37 C.F.R. § 1.114) filed on November 18, 2014 in the U.S. Patent and Trademark Office, on page 4, line 20 (previously numbered as claim 10).

Attached hereto, in duplicate, is Form PTO/SB/44, with at least one copy suitable for printing.

Applicant notes that the error was the result of a mistake on the part of the U.S. Patent and Trademark Office. Thus, Applicant believes that no further fees are due. However, the Commissioner is hereby authorized to charge any fees, which may be required, to Deposit Account Number 50-2469.

Respectfully submitted,

1-22-2016
Date



Jeffrey G. Toler, Reg. No. 38,342
Toler Law Group, PC
8500 Bluffstone Cove, Suite A201
Austin, Texas 78759
(512) 327-5515 (phone)
(512) 327-5575 (fax)

UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

Page 1 of 1

PATENT NO. : 8,996,838 B1
APPLICATION NO.: 14/273,031
ISSUE DATE : March 31, 2015
INVENTOR(S) : Manuel Antonio D'Abreu et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims section, Claim 8 (Column 36, Line 63) "The method of claim 7, wherein the data storage device" should be --The method of claim 1, wherein the data storage device--.

MAILING ADDRESS OF SENDER (Please do not use customer number below):

Toler Law Group, PC
8500 Bluffstone Cove, Suite A201
Austin, Texas 78759

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**

Page 1 of 1

PATENT NO. : 8,996,838 B1

APPLICATION NO.: 14/273,031

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INVENTOR(S) : Manuel Antonio D'Abreu et al.

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US	1165
71591	7590	03/15/2016		
TOLER LAW GROUP 8500 BLUFFSTONE COVE, SUITE A201 AUSTIN, TX 78759			EXAMINER LANE, JOHN A	
			ART UNIT	PAPER NUMBER
			2139	
			NOTIFICATION DATE	DELIVERY MODE
			03/15/2016	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

snobert@tlgiplaw.com
docketinggroup@tlgiplaw.com
thall@tlgiplaw.com



UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Patent No. 8996838
Issued Date: 31 March, 2015
Appl. No: 14/273,031
Filed.: 08 May 2014

PART (A) RESPONSE FOR CERTIFICATES OF CORRECTION

This is a decision on the Certificate of Correction request filed 27 January 2016.

The request for issuance of Certificate of Correction for the above-identified correction(s) under the provisions of 37 CFR 1.322 and/or 1.323 is hereby:

(Check one)

☒ Approved ☐ Approved in Part ☐ Denied

Comments:

PART (B) PETITION UNDER 37 CFR 1.324 OR 37 CFR 1.48

This is a decision on the petition filed to correct inventorship under 37 CFR 1.324.

This is a decision on the request under 37 CFR 1.48, petition filed . In view of the fact that the patent has already issued, the request under 37 CFR 1.48 has been treated as a petition to correct inventorship under 37 CFR 1.324.

The petition is hereby: ☐ Granted ☐ Dismissed

The patented filed is being forwarded to Certificate of Corrections Branch for issuance of a certificate naming only the actual inventor or inventors.

/Reginald Bragdon/
Technology Center 2100
Phone: (571)272-4204

Certificates of Correction Branch email: CustomerServiceCoC@uspto.gov CoC Central Phone Number: (703) 756-1814

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

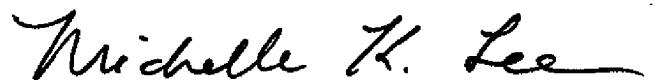
PATENT NO. : 8,996,838 B1
APPLICATION NO. : 14/273031
DATED : March 31, 2015
INVENTOR(S) : Manuel Antonio D'Abreu et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims section, Claim 8 (Column 36, Line 63) "The method of claim 7, wherein the data storage device" should be --The method of claim 1, wherein the data storage device--.

Signed and Sealed this
Fifth Day of April, 2016



Michelle K. Lee
Director of the United States Patent and Trademark Office

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI432478

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT
CONVEYING PARTY DATA	
Name	Execution Date
SanDisk Technologies LLC	08/12/2024
RECEIVING PARTY DATA	
Company Name:	Palisade Technologies, LLP
Street Address:	1468 James Rd.
City:	Gardnerville
State/Country:	NEVADA
Postal Code:	89460
PROPERTY NUMBERS Total: 14	
Property Type	Number
Patent Number:	9530716
Patent Number:	8148962
Patent Number:	9501398
Patent Number:	9448876
Patent Number:	9454448
Patent Number:	8327051
Patent Number:	9466383
Patent Number:	9281314
Patent Number:	8996838
Patent Number:	9373408
Patent Number:	9524974
Patent Number:	9349458
Patent Number:	7743258
Patent Number:	8135961
CORRESPONDENCE DATA	
Fax Number:	
<i>Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.</i>	
Phone:	3129194254
Email:	dave@gerasimowlaw.com

Correspondent Name:	David Gerasimow
Address Line 1:	FL3 PMB1717
Address Line 2:	211 W Wacker Dr
Address Line 4:	Chicago, ILLINOIS 60606
NAME OF SUBMITTER:	David Gerasimow
SIGNATURE:	David Gerasimow
DATE SIGNED:	08/15/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).
Total Attachments: 2 source=SDTL Palisade Assignment#page1.tiff source=SDTL Palisade Assignment#page2.tiff	

SDTL PALISADE ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, **SanDisk Technologies LLC**, with a registered address at 7501 N Capital of Texas Hwy, Building A, Suite #100, Austin, TX 78731, ("Assignor"), does hereby assign, transfer and convey unto **Palisade Technologies, LLP**, with an office at 1468 James Rd., Gardnerville, NV 89460, USA, ("Assignee"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Schedule A (collectively "Patent Rights").

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

This assignment is made effective as of: August 7, 2024.

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at Sandy, UT, USA
on 8/12/24.

ASSIGNOR SanDisk Technologies LLC,

By:

Name: David Dutcher

Title: VP, Chief IP and Licensing Counsel

STATE OF Utah)
COUNTY OF Salt Lake) ss.

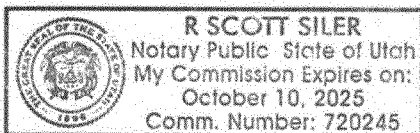
On 08-12-2024 before me,

R. Scott Siler Notary Public

Personally appeared David Dutcher, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that she executed the same in her authorized capacity, and that by her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of Utah that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.



R. Scott Siler
Notary Public

SCHEDULE TO ASSIGNMENT

Country	Patent/Publication Number	Application Number
US	9,530,716	13/452,767
KR	10-1774059	2011-7028490
US	8,148,962	12/464,301
CN	ZL201380072287.2	201380072287.2
US	9,501,398	13/831,218
US	9,448,876	14/454,667
US	9,454,448	14/454,672
US	8,327,051	11/986,389
US	9,466,383	14/144,056
US	9,281,314	14/511,834
US	8,996,838	14/273,031
TW	TW201606496	104112604
CN	ZL201510626779.2	201510626779.2
DE	102015116905	102015116905.3
US	9,373,408	14/508,274
US	9,524,974	14/806,111
US	9,349,458	14/515,762
US	7,743,258	11/511,766
US	8,135,961	12/760,359

Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS	Patent Number	8996838
	Issue Date	03/31/2015
	First Named Inventor	Manuel Antonio D'ABREU
	Title	Structure variation detection for a memory having a three-dimensional
	Attorney Docket No.	9062-0010

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

174899

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or
Individual Name

Address

City

Country

Telephone

State

Zip

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 1.33(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

Signature	<i>Peter Hardigan</i>	SIGNATURE of Applicant or Patent Owner		Date	8/29/2024
Name	Peter Hardigan			Telephone	(917) 622-0926
Title and Company	Manager, Palisade Technologies, LLP				

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

STATEMENT UNDER 37 CFR 3.73(c)Applicant/Patent Owner: PALISADE TECHNOLOGIES, LLPApplication No./Patent No.: 8996838Filed/Issue Date: 3/31/2015Titled: STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL MEMORY CONFIGURATIONPALISADE TECHNOLOGIES, LLP, a LIMITED LIABILITY PARTNERSHIP

(Name of Assignee)

(Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose one of options 1, 2, 3 or 4 below):

1. ☒ The assignee of the entire right, title, and interest.
2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):
- ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.
- ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (e.g., bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose one of options A or B below):

- A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.
- B. ☒ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: MANUEL ANTONIO D'ABREU, ET AL. To: SANDISK TECHNOLOGIES INC.The document was recorded in the United States Patent and Trademark Office at
Reel 032851, Frame 0941, or for which a copy thereof is attached.2. From: SANDISK TECHNOLOGIES INC To: SANDISK TECHNOLOGIES LLCThe document was recorded in the United States Patent and Trademark Office at
Reel 038807, Frame 0948, or for which a copy thereof is attached.

[Page 1 of 2]

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

STATEMENT UNDER 37 CFR 3.73(c)3. From: SANDISK TECHNOLOGIES LLC To: PALISADE TECHNOLOGIES, LLP

The document was recorded in the United States Patent and Trademark Office at
 Reel 068301, Frame 0100, or for which a copy thereof is attached.

4. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
 Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☒ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David Gerasimow/

Signature

David Gerasimow

Printed or Typed Name

08-29-2024

Date

57,512

Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES
PATENT AND TRADEMARK OFFICEP.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov**ELECTRONIC ACKNOWLEDGEMENT RECEIPT**APPLICATION #
14/273,031RECEIPT DATE / TIME
08/29/2024 04:24:49 PM Z ETATTORNEY DOCKET #
SDA-2117-T1-US**Title of Invention**STRUCTURE VARIATION DETECTION FOR A MEMORY HAVING A THREE-DIMENSIONAL
MEMORY CONFIGURATION**Application Information**APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # 8996838

CONFIRMATION # 1165

FILED BY David Gerasimow

PATENT CENTER # 66982319

FILING DATE 05/08/2014

CUSTOMER # 71591

FIRST NAMED
INVENTOR MANUEL ANTONIO D'ABREUCORRESPONDENCE
ADDRESS -

AUTHORIZED BY -

Documents**TOTAL DOCUMENTS: 2**

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA8996838.pdf	2	Power of Attorney	265 KB
Warning: The PDF file has been signed with a digital signature and the legal effect of the document will be based on the contents of the file not the digital signature.			
POA8996838 3.73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	119 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA8996838.pdf	FEE7D1B4989197A5A2684A57B8D3842706CA21545453A442D 43D25891C74C0C559B08520B5E931C08A47350F07296E13591

2007AD26FB2183435A8ABD3478A58

POA8996838 3.73c.pdf

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8CBDEA8209D37FFAE5012AA9D9650E4E95FEC2AC3D4617D
C23B279E462C5DF9442A43451F3808915

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	SDA-2117-T1-US

71591
WD_TOLER LAW GROUP
5601 Great Oaks Parkway
San Jose, CA 95119

CONFIRMATION NO. 1165
POWER OF ATTORNEY NOTICE



OC00000077832387

Date Mailed: 09/13/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mtekle michael/



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Alexandria, Virginia 22313-1450
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
14/273,031	05/08/2014	MANUEL ANTONIO D'ABREU	6062-0010

174899
The Law Offices of David A. Gerasimow, P.C.
211 W. Wacker Dr.
Ste. 1717
Chicago, IL 60606

CONFIRMATION NO. 1165
POA ACCEPTANCE LETTER



Date Mailed: 09/13/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/mtekle michael/