



The Memory Guy Blog

Jim Handy, Objective Analysis, on Semiconductor Memories

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Why Do We Need 3D NAND?

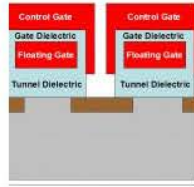


Jim Handy

August 14, 2024

NAND Flash, Process Geometries & Die Sizes, Vertical Structures

3D NAND, 3DNAND, AMAT, Applied Materials, BICS, Samsung, TCAT, Toshiba, trench, V-NAND, vertical, VNAND



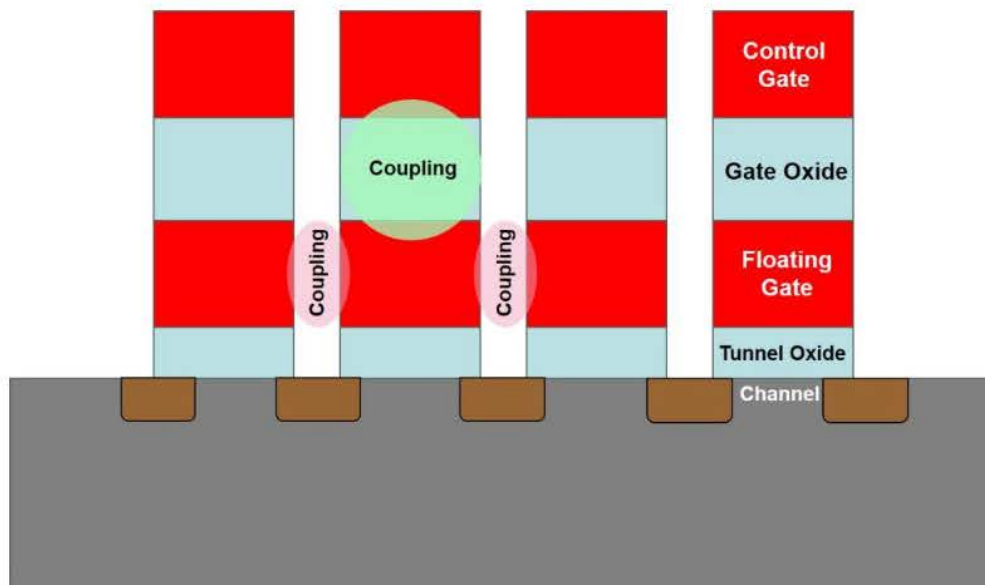
(The following is an update of a post that originally ran 18 October 2013. It was republished in 2024 as a part of a series to honor the [3D NAND inventors who have received the 2024 FMS Lifetime Achievement Award.](#))

A memory chip of a certain area costs about the same amount to produce, no matter how many bits it holds. Naturally, the more bits you can cram onto this chip, the cheaper the price per bit will be. Low cost is of the utmost importance in the world of memory.

Memory chip makers have shrunk the cost of a bit some ten orders of magnitude since the 1960s largely by shrinking the lithographic process, or “scaling” to increasingly tighter process geometries.

Planar flash was always expected to reach a [scaling limit](#). As flash approached the 15nm process node in 2010, technologists developed new processes and harnessed innovative materials to push scaling farther than it was expected to go. In the end, though, everyone in the industry knew that there would come a point at which planar NAND could simply no longer be shrunk.

This had to do with the fact that the cells were squeezed so close to each other that the capacitive coupling between the two adjacent floating gates in the diagram below (pink orbs) became greater than the coupling from a cell’s own control gate to its floating gate (green circle).



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CONTACT

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Jun Fang

July 14, 2014 at 7:18 pm

Hi JimHandy,

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Jun Fang

July 14, 2014 at 7:18 pm

Hi JimHandy,

The materials in your blog are really valuable to people who working in semi area, and I learned a lot from your blog in the case of flash knowledge.

And I would like to consult you a question, in the case of planar NAND flash, there is source and drain for each unit cell, so how about 3D NAND flash, it looks like no any source and drain any more for each unit cell, is it right?

Thanks,

Jun



Jim Handy

July 14, 2014 at 8:02 pm

Jun Fang,

Thanks for the compliment!

I will double-check with people who understand this better than I do, but I believe that there is no source or drain for most of the transistors in a planar NAND string. You might think of it more as a single transistor with 64 gates, all in a row.

I'll double-check, though, in case I am wrong.

Jim



Jim Handy

July 15, 2014 at 8:50 pm

OK, I was wrong about that!

Planar NAND has source and drain implants, but 3D NAND does not.

I don't really understand why, but I am told that undoped thin film transistors don't need the implant because they are based upon a different kind of MOSFET.

You're going to have to talk to someone smarter than me to find out more, I'm afraid!

Jim

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