



The Memory Guy Blog

Jim Handy, Objective Analysis, on Semiconductor Memories

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What is a 3D NAND?

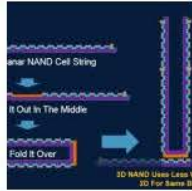


Jim Handy

August 23, 2024

NAND Flash, Process Geometries & Die Sizes, Vertical Structures

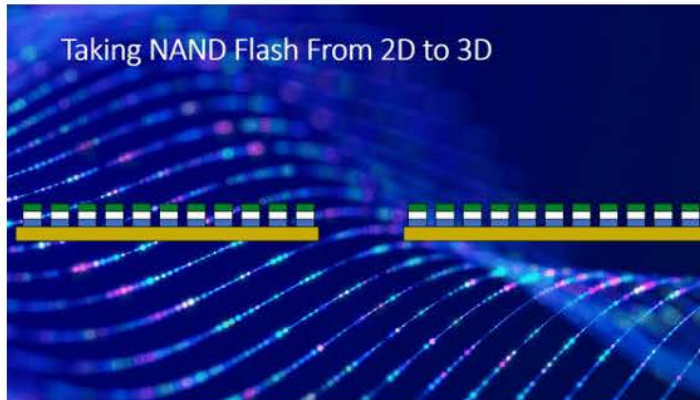
3D NAND, 3DNAND, AMAT, Applied Materials, BICS, Samsung, TCAT, Toshiba, trench, V-NAND, vertical, VNAND



(The following is an update of a post that originally ran 25 October 2013. It was republished in 2024 as a part of a series to honor the [3D NAND inventors who have received the 2024 FMS Lifetime Achievement Award.](#))

In the prior post we discussed the need to go vertically into the body of the die, since NAND flash can not be scaled much farther in length and width on the die's surface. Toshiba invented a 3D NAND which has been adopted and refined by all flash makers. The idea is simple: Rather than shrink the cell's length and width, why not turn the NAND string so that it's standing on its end?

This concept is illustrated by this post's first graphic, which was provided by Applied Materials. In 2024 we animated this for the presentation of the Lifetime Achievement Award to 3D NAND's inventors.



Both the diagram and the GIF present the idea of a standard NAND string, that would normally run longitudinally across the surface of the die, being split and turned on its end to become a vertical string. It makes things easier if the string is split into two sections and formed into a "U" shape rather than a single column.

Naturally a fab can't make 3D NAND chips by manufacturing NAND strings and folding them. Instead the string is formed vertically using a completely different manufacturing process than is used for standard NAND flash. In fact, this is a technique that is new to all of semiconductors.

If you can lay down a horizontal series of control gates, then run a vertical series of floating gates and a channel that responds to those gates, then you can build strings that may be several cells long in the same area as a single planar cell.

How much space does this save? If your 3D NAND flash

16 GB Cells in a Planar 30nm Chip

16 GB Cells in a 3D NAND Chip

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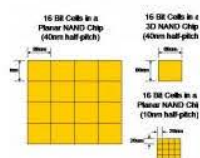
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If you can lay down a horizontal series of control gates, then run a vertical series of floating gates and a channel that responds to those gates, then you can build strings that may be several cells long in the same area as a single planar cell.



How much space does this save? If your 3D NAND flash string is sixteen-cells deep, then it effectively shrinks the production process to $\frac{1}{4}$ its size, as is shown in a top-down view in the illustration on the left. (Click on it to enlarge.) This is a very abstract representation of sixteen NAND flash cells which are not necessarily in the same string.

Here's what the diagram represents: At a half pitch of 40nm (making the cell 80nm on a side) a block of sixteen planar memory cells would consume a certain amount of space. When these 16 cells are manufactured vertically they would consume as much area as a single one of those 16 planar cells.

What would it take to fit 16 cells into the same area using a planar process? The third part of the diagram shows us this – the process would have to shrink to a half pitch of 10nm, or $\frac{1}{4}$ that of the first block. That's a significant jump equivalent to about four process generations!

For vertical strings of different lengths this ratio would be different, in fact it is the square root of the number of cells in the string, so a trench 4-cells deep would provide as many cells in a given die area as a planar process with half the pitch, and a 64-deep trench would rival a process with one eighth the pitch of the 3D approach.

Another way to put this is that if you were to draw a diagram like the second graphic that had 64 boxes representing planar cells (in an 8x8 grid) then each box would have to be 10x10nm in order for the whole set of 64 boxes to have same 80x80nm size as the 40nm trench box.

So here's how these different numbers of trenches compare against their planar counterparts:

- 16-cell trenches at 40nm compete against 10nm planar cells
- 32-cell trenches at 40nm compete against 7nm planar cells
- 64-cell trenches at 40nm compete against 5nm planar cells
- 128-cell trenches at 40nm compete against 3.5nm planar cells

By shifting from planar 2D NAND to a 3D technology the pressure is instantly removed from lithographic scaling. Cost reduction is no longer solely determined by shrinking the horizontal patterns on the surface of the chip. Instead it becomes a factor of how many transistors you can make in a single vertical string.

The next post will get into the mechanics of how such vertical strings can be manufactured.

Above I mention a sixteen-bit string, but that's just something that [The Memory Guy](#) chose for convenience's sake. NAND producers are already making vertical strings 128 cells high, which, with the "U" shape in the diagram yields a 256-cell string. Some are already talking about going to 1,000 layers. It is fathomable that they could go well beyond this level, but nobody's publicly disclosing their research efforts in this

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How many levels can be used by this kind of approach? When I originally wrote this post in 2013 memory makers argued that it takes twice as many layers to double the chip's capacity in the same die area, and that going from 128 layers to 256 might be impossible, yet they achieved that milestone within a decade. At that time I said that I would not be surprised to see them abandon binary string lengths moving to other peculiar numbers to optimize the cost per gigabyte, and that has indeed happened.

Let's be perfectly clear, though: 3D NAND is not stacks of chips. A lot of people mistakenly think this is the case. The cost of a semiconductors is roughly proportional to its die area. A stack of eight chips is over eight times as expensive as an individual chip of the same area as the stack. Stacking chips doesn't save money.

Of course, I wrote the above paragraph in 2013, before anyone was even thinking about bonded NAND flash, which YMTC currently produces and WDC and Kioxia are sampling. A future post will discuss this approach, where today two wafers are used to produce the equivalent of one 3D NAND wafer at a lower overall cost. Before I write that post, though, I will need to understand how two wafers can cost less than one. Nobody has been willing to share that with me yet.

But it's important to remember that Moore's Law is about continually increasing the number of transistors on a chip so that the cost per transistor will decline. This is the economic foundation of the semiconductor industry, and it would fall apart if prices stopped declining.

By going vertical, NAND flash makers are finding a way to get more bits onto a chip of a given size than they can through simple lithographic shrinks, increasing the number of bits per chip, even if they aren't able to shrink the length and width of a cell on that chip.

This post is a part of a series called [What is 3D NAND? Why do we need it? How do they make it?](#) that was published in weekly segments during the fourth quarter of 2013 on [The Memory Guy](#) blog, and was updated in 2024. The different sections are listed below, with a hot link to each section.

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Jacob Ofek

March 19, 2015 at 8:03 am

Usually in the 2D flash memory we see NPN junction near each one of the memory cells done by doping. How can doping possible in a vertical channel ? are they doing this NPN at all ?



Jim Handy 

March 19, 2015 at 5:58 pm

Jacob, I had the same question, so I asked the books' author, Betty Prince.

She says that none of the vertical junctions are doped. It would be very difficult.

Junctionless channels are possible because, for a Gate-All-Around nanowire memory device, the side fringing field from the gate induces an inversion in the source/drain region which makes the device work without doping.

There has been further work in this area for even smaller nanowires which involves a bulk effect pinch-off effect under the gate which turns the device on and off. Much work is ongoing in this area.



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This is covered in Chapter 3 Section 4 of her book. In particular see figure 3.26.

Jim

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