



The Memory Guy Blog

Jim Handy, Objective Analysis, on Semiconductor Memories

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3D NAND: Making a Vertical String

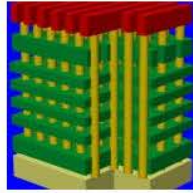


Jim Handy

August 30, 2024

Charge Trapping, NAND Flash, Vertical Structures

3D NAND, 3DNAND, Applied Materials, BiCS, Bit Cost Scaling, bit lines, cake, Charge Trap, charge trapping, CTF, gate-all-around, hole, International Electron Device Meeting, kioxia, layer cake, ONO, silicon dioxide, silicon nitride, Toshiba, V-NAND, VNAND



(The following is an update of a post that originally ran on 1 November 2013. It was republished in 2024 as a part of a series to honor the [3D NAND inventors who have received the 2024 FMS Lifetime Achievement Award.](#))

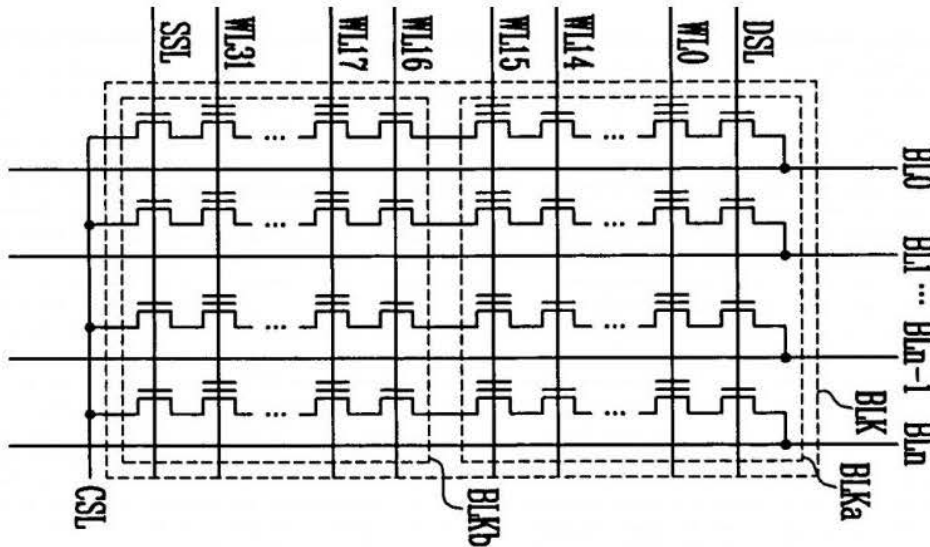
Let's look at how one form of 3D NAND is manufactured.

For this post we will explore the original design proposed by Toshiba, now Kioxia, at the IEEE's VLSI Symposium in 2007. It's shown in the first graphic of this post. (Click on any of the graphics for a better view.)

Kioxia calls this technology "BiCS FLASH" for "Bit Cost Scaling." The technique doesn't scale the process geometry the way the world of semiconductors always had done before – it scales the cost without shrinking the length and width of the memory cell. It accomplishes this by going vertically, as is shown in this post's first graphic.

This takes a special effort. This is where the real genius comes in.

Here's a schematic of a small part of a NAND flash array:



In planar NAND parallel strips of polysilicon running across the surface of the chip are used for the wordlines that connect the control gates of the memory cells (the lines labeled WL0 through WL31 in the diagram above). In 3D NAND these parallel strips are replaced with horizontal sheets of polysilicon.

How are these sheets manufactured? First a layer of CMOS logic is built on the chip to serve as the peripheral logic and conductive paths are produced on the substrate to

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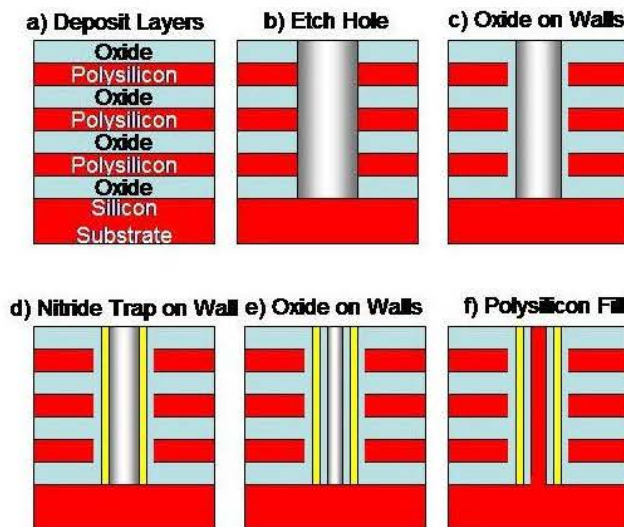
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used for the wordlines that connect the control gates of the memory cells (the lines labeled WL0 through WL31 in the diagram above). In 3D NAND these parallel strips are replaced with horizontal sheets of polysilicon.

How are these sheets manufactured? First a layer of CMOS logic is built on the chip to serve as the peripheral logic and conductive paths are produced on the substrate to connect pairs of adjacent columns to form the “U” shaped structure shown as the first graphic in the prior post: [“What is a 3D NAND?”](#) This logic is then insulated with a layer of silicon dioxide. A conductive polysilicon layer is deposited on top of this to form the first wordline and control gate, and a silicon dioxide layer is grown on top of the polysilicon to insulate it from the polysilicon layer that will be deposited above it. This is repeated a number of times with pairs of polysilicon and silicon dioxide layers laid one above another as sheets across the entire wafer. It’s something like a layer cake with alternating layers of cake and frosting. This is shown as “a” in the graphic below.



Once the desired number of these layers has been deposited upon the wafer, an array of circular holes is patterned onto it and these holes are then etched through all of the layers to the substrate. A single hole is shown in “b” in the figure. This type of etching is a technique borrowed from the DRAM trench cell that was used by IBM, Toshiba, Siemens, and their licensees.

Only a single mask step is needed to form the holes for all the layers in the device. Even though the string may have 16, 32, 64, or more transistors, it’s still just a single mask step. This creates very economical lithography compared to today’s NAND fabrication processes.

The next step is to make the floating gate and the channel. The inside walls of the holes are first coated with a silicon dioxide layer (“c” in the graphic) to create the gate dielectric (the dielectric between the control gate and the floating gate). Think of this as a tube lining the hole. Then a charge trap, which replaces the planar NAND cell’s floating gate, is made by depositing a silicon nitride layer onto the silicon dioxide, forming a tube within the tube – “d” in the graphic. Another oxide layer is deposited on the silicon nitride to form the tunnel dielectric (“e” in the graphic) – the third of three concentric tubes lining the walls of the hole. Finally the entire hole (or what’s left of it after these concentric tubes have been layered on the sidewalls) is filled by depositing polysilicon into it (“f” in the graphic). In the end this produces a NAND string that behaves similar to the schematic in the second graphic.

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forming a tube within the tube – “d” in the graphic. Another oxide layer is deposited on the silicon nitride to form the tunnel dielectric (“e” in the graphic) – the third of three concentric tubes lining the walls of the hole. Finally the entire hole (or what’s left of it after these concentric tubes have been layered on the sidewalls) is filled by depositing polysilicon into it (“f” in the graphic). In the end this produces a NAND string that behaves similar to the schematic in the second graphic.

After the holes are processed, another lithography/etch cycle is used to carve long slits for the length of the array between the adjacent connected columns to isolate the control gates of the “Up” column from those of the “Down” column of the “U” shaped structure.

From a lithographic viewpoint, the width of the NAND flash string is limited by the thickness of the walls of the tubes lining the hole, and the thickness of the polysilicon channel. Once these features have reached a certain thickness they will no longer be able to shrink any further, limiting the number of columns that can be packed into an area of a chip. 3D NAND abandons lithographical shrinks to pursue layer count increases.

When this post was originally published in 2013, it said: “3D NAND could stay around much longer than the 3 generations that are currently projected.” That certainly came true. Toshiba, now Kioxia, is today beginning to launch its eighth generation of BiCS FLASH, and they openly speak of future generations. Flash with over 300 layers has been sampled; compare that to the 3 generations that were first considered: 24, 32, and 48 layers!

NAND flash lithography actually moved backwards with the adoption of 3D and has remained at the same 40nm node for its history, after having reached 15nm in planar form. This is why Toshiba coined the term: “Bit Cost Scaling”. The objective of 3D NAND has been to continue to reduce costs to follow Moore’s Law without using lithographic shrinks. This is a completely different approach than had ever been tried in semiconductors.

Astute readers will note that I didn’t say anything about patterning the floating gate. That’s because it’s very difficult to pattern anything vertically – you can’t do it using lithography since you can’t make the light go sideways. This is where some real magic comes into play.

The original BiCS design used a silicon nitride [charge trap](#) as a substitute for the floating gate – the same technique that Spansion (now Infineon) has used since the 2002 introduction of its MirrorBit NOR flash. This technology is highly manufacturable and now accounts for the vast majority of Infineon’s NOR flash production. A charge trap is an insulating layer, so two adjacent charge traps will not interfere with each other even though there is no distinction between each cell’s charge trap. This layer doesn’t need to be patterned at all.

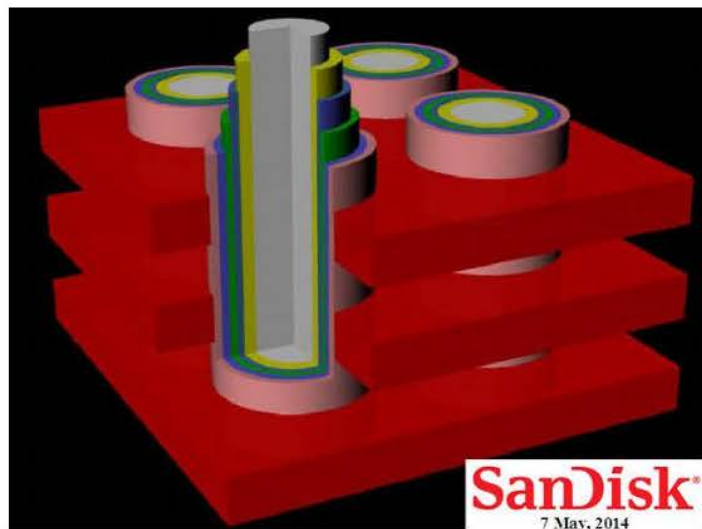
Charge traps have been used for nearly all 3D NAND for this reason. The only 3D floating gate NAND is produced by SK hynix’ Solidigm subsidiary and was developed by an Intel-Micron joint venture. The floating gate is patterned through a very elaborate addition to the process described in this post. Micron abandoned the floating gate 3D NAND approach in 2020, leaving Intel’s Solidigm spin-out as the sole user.

The charge trap posed a special problem during 3D NAND’s introduction: Before 2013,

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The charge trap posed a special problem during 3D NAND's introduction: Before 2013, nobody but Spansion had successfully produced charge trap flash in volume, although many had tried. Before it was acquired by Spansion in 2008 a company named Saifun licensed charge trap technology to a number of firms, including Macronix, NEC, Qimonda, SMIC, Sony, and Tower, but none of these licensees were able to move beyond prototypes and into production. [Samsung announced a charge trap flash](#) for its 40nm node in 2006, but never released the part to production. When this post was originally published, [Objective Analysis](#) said that it anticipated that the cause of these difficulties, whatever it may be, could delay the introduction of 3D NAND. That indeed happened: Although the first production 3D NAND chips shipped in 2013, it took another three years for the industry to ramp the product into high volume.



SanDisk (acquired by Western Digital in 2016) presented a very clear illustration of a BiCS vertical structure in its [May 2014 Investor Day presentations](#), and allowed me to include a copy of it here. The company didn't call out the different layers of the structure. My guess is that (working out from the center) the gray center is a SiO₂ fill, the yellow is the polysilicon channel, the blue is the tunnel dielectric, the green is a charge trapping layer, the next blue is the gate dielectric, but I don't know what the pink layer would be. The control gates are the red horizontal layers, and the insulator between bits, a horizontal SiO₂ layer, is not shown in order to add clarity.

You might think that manufacturing a vertical NAND string looks extraordinarily difficult, and you are right. It's tough to etch a hole sufficiently deep and narrow, and sufficiently consistent from top to bottom. It's also very tough to keep the width of the hole consistent while going through layers of very different materials. A lot of research has been devoted to managing this. Applied Materials, who took a lot of time to bring me up to speed on the process, has an excellent tool for this kind of process, as does Lam Research. Both companies' tools have seen strong adoption for true mass production of 3D technology.

Coventor, which has been acquired by Lam Research, shared a video of the process of making BiCS NAND that can be accessed from [another post on The Memory Guy](#).

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Coventor, which has been acquired by Lam Research, shared a video of the process of making BiCS NAND that can be accessed from [another post on The Memory Guy](#). Have a look and you will be amazed at its complexity!

In the next post we will explore how other companies chose a different approach to manufacturing a vertical NAND string.

This post is a part of a series called [What is 3D NAND? Why do we need it? How do they make it?](#) that was originally published in weekly segments during the fourth quarter of 2013 on [The Memory Guy](#) blog, and was updated in 2024. The different sections are listed below, with a hot link to each section.

- [Why Do We Need 3D NAND?](#)
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Click on any of the above links to learn more about 3D NAND technology.



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