



The Memory Guy Blog

Jim Handy, Objective Analysis, on Semiconductor Memories

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An Alternative Kind of Vertical 3D NAND String

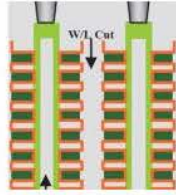


Jim Handy

September 9, 2024

NAND Flash, Vertical Structures

3D NAND, 3DNAND, BiCS, Bit Cost Scaling, Charge Trap, charge trapping, CTF, floating gate, gate-all-around, TANOS, V-NAND, Vertical Structures, VNAND, word lines, wordlines

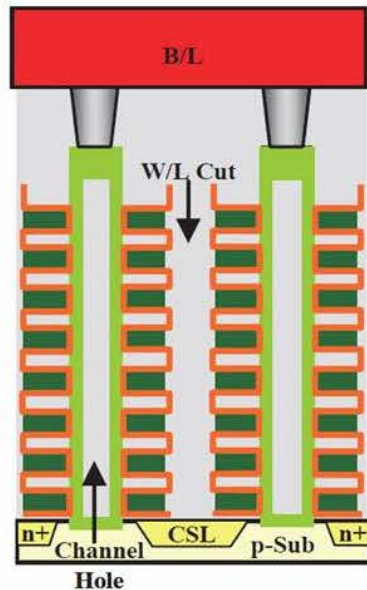


(The following is an update of a post that originally ran on 8 November 2013. It was republished in 2024 as a part of a series to honor the [3D NAND inventors who have received the 2024 FMS Lifetime Achievement Award](#).)

My [prior 3D NAND post](#) explained how Toshiba's BiCS

cell works, using a silicon nitride charge trap to substitute for a floating gate. This post will look at an alternative technology first introduced by Samsung and now used by all 3D NAND makers except for Solidigm (now owned by SK hynix) who uses a floating gate design that this series did not detail.

Samsung's approach is illustrated in the graphic below, a diagram Samsung presented at a technical conference. This cell also uses a charge trap.



Let [The Memory Guy](#) warn you, if the process in my prior post seemed tricky, this one promises to put that one to shame!

Part of this stems from the use of a different kind of NAND bit cell. You can shrink flash cells smaller if you use a high-k gate dielectric (one with a high dielectric constant "k") since it provides a very high capacitance (higher coupling) between the charge trap and the control gate. Capacitance decreases with process shrinks since a shrink reduces the plate dimensions of a cell's capacitors; if you change the dielectric from silicon dioxide to a high-k material

that will help to offset this decrease.

High-k dielectrics perform better with a metal control gate than with the polysilicon gate used in conventional flash cells, so some high-k designs deposit a tantalum control gate on top of the high-k dielectric.

Samsung has chosen a cell type called TANOS, which stands for Tantalum-Alumina-Nitride-Oxide-Silicon. Even this is a shortened term, since the "Tantalum" is really tantalum nitride, "Alumina" is short for an aluminum-based high-k gate dielectric (usually Al_2O_3). "Nitride" is short for silicon nitride, and "Oxide" is an abbreviation

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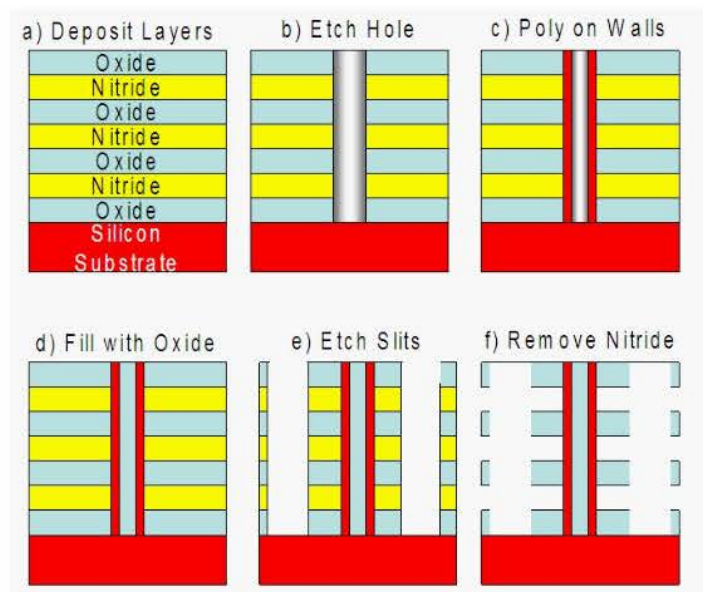
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The TANOS structure combines a silicon nitride charge trap with a high-k gate dielectric and a tantalum control gate. According to Samsung this cell provides certain advantages over the BiCS cell, including faster erase speed, wider threshold voltage margins, and better data retention characteristics.

An added benefit of using tantalum instead of polysilicon is that tantalum lowers the resistance of the gates and the interconnect between them. Since these layers are really thin, that resistance is important, and one way that 3D NAND makers have been able to add layers is by making each layer as thin as possible.

The TCAT (Terabit Cell Array Transistor) structure described in this post was first presented by Samsung at the IEEE’s VLSI Technology Forum (VLSIT) in 2009. Samsung introduced a product based on this technology last August that the company calls V-NAND for “Vertical NAND.”

The series of sketches in the next two graphics illustrate the process steps involved in manufacturing a TCAT string. It’s more extensive than the BiCS series, so I will ask for the reader’s patience.



Similar to the BiCS design, the process starts by depositing multiple layers onto the surface of a CMOS wafer, (Step a in the graphic) but rather than alternating conductive polysilicon and insulating silicon dioxide layers the TCAT process begins with alternating layers of silicon nitride and silicon dioxide. That may surprise you, since both of these materials are insulators, but we will see that the silicon nitride layer is sacrificial – it serves as a placeholder and will be removed so that the space it consumes

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Samsung calls this a “gate replacement process.” (When Micron moved away from a floating gate process to a similar approach, they called theirs “Replacement Gate.”)

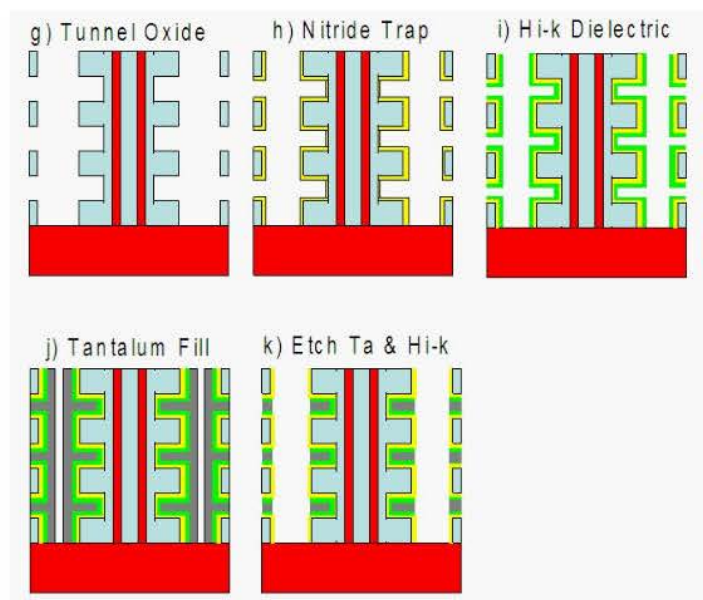
As with the BiCS process, a hole is etched through all the deposited layers to the substrate. This is shown as Step b) in the second graphic.

The hole is next lined with polysilicon for the channel, skipping the deposition of all the ONO layers used in the BiCS approach. This is shown as Step c) in the graphic. In Step d) the center of the hole is filled with silicon dioxide, which (I am told) gives better sub-threshold characteristics and threshold voltage distributions than a solid polysilicon channel would. This has been dubbed a “Macaroni Channel” and was also introduced in BiCS.

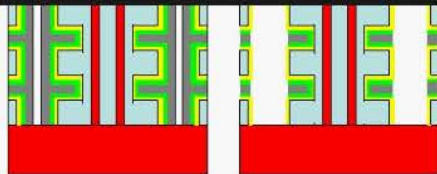
So how do they make the gate, now that the hole has been plugged? This is the mind-bending part! In Step e) slits are etched – the same as in BiCS (although I didn’t show these in the prior post’s graphic) to separate the columns from each other. All of the processing from here on is performed through these slits. (Note that the layers of oxide and nitride on either side of the drawing are actually attached to adjacent pillars that are not fully shown.)

In Step f) the sacrificial silicon nitride layers are selectively etched away from the sides, leaving a structure that resembles a very narrow tower with fins.

The entire tower is then coated with a silicon dioxide tunnel dielectric layer (Step g below), followed by a silicon nitride charge trap (Step h) and then the alumina high-k gate dielectric (Step i).



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Finally most of the slit and all the remaining gaps in the finned pillar are filled with the tantalum nitride control gate material (Step j) which is subsequently etched out of the center of the slit along with the high-k dielectric on the walls (Step k).

What remains is a vertical NAND string of TANOS transistors: The tantalum nitride plug (gray), an alumina high-k gate dielectric (green), a silicon nitride charge trap (yellow), the silicon dioxide tunnel dielectric (pale blue), and the polysilicon channel (red).

To go back to the layer cake analogy I used in the prior post, we have just built a layer cake, removed all of the frosting, and replaced it with a different and more complex frosting.

The BiCS approach described in the prior post made the transistors from the walls of the hole and worked toward the center, starting with the control gate and ending with the channel. The TCAT design starts with the channel at the center and builds the transistors from the middle out, ending with the control gate. That's why TCAT's process is sometimes referred to as "Gate Last" and the BiCS approach is called "Gate First."

Either way, since the gate surrounds the channel both BiCS and TCAT are called "Gate All Around" structures. Since one of the problems presented by planar scaling is the fact that the coupling capacitance between the control gate and the rest of the transistor diminishes with shrinking processes, a big benefit of the Gate All-Around approach is that it provides a large surface area to couple the control gate to the charge trap.

I am told that one strength of the TCAT approach is that it is less constrained in the horizontal plane than is the BiCS approach so the holes may be made smaller, resulting in a smaller die size. This is because of the number of layers deposited into the hole: The hole in BiCS is filled with three concentric tubes to form the oxide-nitride-oxide layers and then is plugged with a polysilicon cylinder. The TCAT hole is filled with a single polysilicon tube and an oxide cylinder. This was expected to allow TCAT to scaled to tighter horizontal lithographies than BiCS. The Memory Guy has not investigated this to see if it really came out that way, but 3D NAND does not undergo a lot of horizontal scaling for this basic reason. See the post: [Why 3D NAND is Stuck at 40nm.](#)

Coventor, which has been acquired by Lam Research, shared a video of the process of making BiCS NAND that can be accessed from [another post on The Memory Guy](#). Have a look and you will be amazed at its complexity, and then consider what a TCAT video would be like!

The next post will show how the control gates on all those internal layers are connected to the support logic, a simple job in a planar NAND that becomes a daunting challenge in 3D.

This post is a part of a series called [What is 3D NAND? Why do we need it? How do](#)

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This post is a part of a series called [What is 3D NAND? Why do we need it? How do they make it?](#) that was originally published in weekly segments during the fourth quarter of 2013 on [The Memory Guy](#) blog, and was updated in 2024. The different sections are listed below, with a hot link to each section.

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Dennis Debord

November 12, 2013 at 5:40 am

Great information and look forward to the next article.



JimHandy 

November 12, 2013 at 9:30 am

Thanks, Dennis!



Don Banach

November 13, 2013 at 11:56 am

Thanks, Dennis!



Don Banach

November 13, 2013 at 11:56 am

Excellent series of articles Jim, with just the right amount of detail. I have recommended it to many of my colleagues.
Thanks for publishing!



JimHandy

November 13, 2013 at 2:31 pm

Thank YOU, Don, for the compliment!

I only hoped to make this really unusual technology understandable.

My volunteer proofreaders deserve a lot of the credit for clarity. They hold me to that task!

Jim



Mark Liu

November 19, 2013 at 1:32 am

Thank you very much! Very helpful!

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Albert Lin

April 3, 2015 at 2:43 pm



Albert Lin

April 1, 2015 at 2:41 pm

Hi,

I have a question pertaining to the 2nd and 3rd graphs in this post. In the 2nd graph, step f leaves with an empty space outside the poly (the place was originally occupied by nitride). But step g in the 3rd graph, it appears to me that a layer of oxide is grown outside the poly. Is there any process to deposit oxide from step f to step g. There is not mentioning in the text.

Best regards,

Albert



Jim Handy 

April 1, 2015 at 3:12 pm

Albert, The addition of oxide is in the paragraph right beside the top of the third graphic in the post: "The entire tower is then coated with a silicon dioxide tunnel dielectric layer (Step g in the third graphic)"

My graphic skills aren't all that good, so you may not have noticed that the existing oxide got a little bigger when the oxide was grown on the poly.

Thanks for the comment,

Jim

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