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Monolithic 3D

By Ron Wilson 08.31.2011 0

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Two assumptions have become accepted truths in SoC planning: first, that the way forward involves 3DICs; and second, that 3DICs require through-silicon vias (TSVs.) One result has been a tremendous focus on the challenges of TSVs, and a growing realization of just how formidable those problems really will be in production. But what if the first assumption is true and the second one is false? One of the hottest water-cooler topics at Semicon West this year was a PowerPoint pitch from a new venture called Monolithic 3D. In it, the company argued exactly this point.

“Logically, there are only two ways to make 3DICs,” explained Monolithic 3D founder Zvi Or-Bach. “You can use TSVs to stack up prefabricated dice, or you can do monolithic 3D—successive layers of transistors and interconnect on one substrate. But everyone knows you can’t really do monolithic 3D in practice, because the temperatures you need to form the second layer of transistors destroy the interconnect stack on the first layer.”

Or-Bach’s claim is that there is a third alternative—a middle path, if you will. Essentially, Monolithic 3D proposes to use SmartCut technology—the ion cutting process that Soitec uses to make SoI wafers for AMD and IBM—to stack up consecutive layers of active silicon, the way a deli manager stacks up salami on a sandwich. How to do this without damaging the underlying layers is Monolithic 3D’s special—not secret, but heavily patented—sauce.

First, ion cutting may require some explanation. The key idea is that if you implant a thin layer of H⁺ ions into a single crystal of silicon, the ions will weaken the bonds between the silicon atoms in their area, creating a fracture plane (figures 1 & 2.) Judicious force will then precisely break the wafer at the plane of the H⁺ implant, allowing you to in effect peel off an arbitrarily thin layer. Monolithic 3D proposes this



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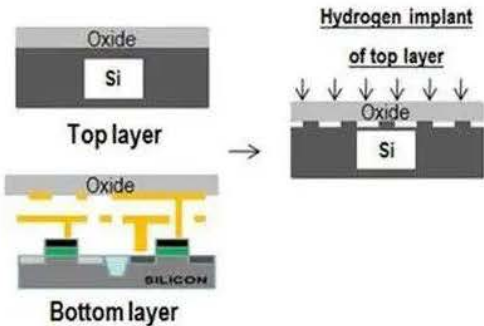
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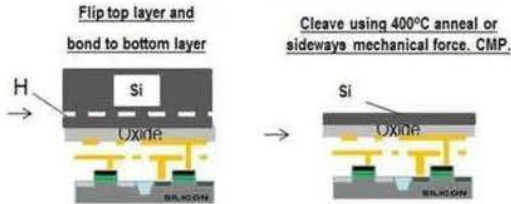


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SmartCut technology starts with implanting a layer of hydrogen ions into the silicon.



The process ends with bonding the wafers together and cleaving off the donor wafer.

But a stack of thin wafer slices is a long way from a 3DIC. Monolithic 3D has proposed a number of ways of doing the rest of the job without cooking or mechanically damaging the bottom layers.

All the approaches start by fabricating a conventional wafer, up through the completed top interconnect layer and passivation, to serve as the bottom wafer of the 3D stack. This first wafer can employ pretty much any silicon technology, including HKMG transistors and ultra-low-k dielectric materials. The only thing non-standard about this first wafer is that the top metal layer will include landing pads for vias coming down from subsequent layers.

The next step can vary enormously, depending on what you want to build. One of the simplest possibilities, perhaps more useful for illustration than for production, is the following. On a second wafer, diffuse in a buried N⁺ layer, above it leaving a P- surface layer. Grow an oxide on the surface, and activate the dopants with a high-temperature cycle. Now do the SmartCut: implant hydrogen ions into a thin plane part-way through the N⁺ buried layer. Then turn this prepared donor wafer over and do an oxide-oxide bond to the completed base wafer. Cleave the top wafer at the plane defined by the H⁺ implant. You now have a layer-cake: a completed wafer on the bottom, a thick layer of oxide where the two wafers bonded together, a thin layer of P- silicon, and on top a thin layer of N⁺ silicon.



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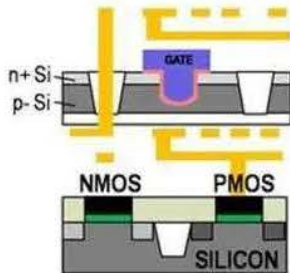
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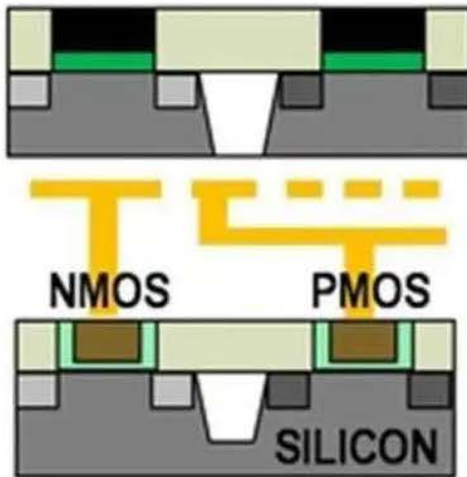
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At this point you can polish the surface, and using only low-temperature processes, fabricate recessed-channel transistors similar to the array transistors used in DRAM cells (RCATs.) Above the transistors you fabricate a second conventional interconnect stack, and you are done (figure 3.) You can repeat as desired to form additional active layers.



This is just one example. Or-Bach and chief scientist Deepak Sekar described a similar sequence—but forming transistor sites on the donor wafer and using a carrier to transfer the slice right-side up—that allows a gate-last, HKMG process on both the donor slice and the base wafer (figure 4.) The two have outlined other ideas as well, including 3D DRAM, 3D FPGAs, monolithic displays and image sensors, and fully-redundant logic circuits.



There are three common factors in all these ideas. First, there are no new materials or unusual process steps required. Second, you do all the high-temperature processing for the donor wafer before bonding the wafers and cleaving, so the base wafer is never driven outside its thermal budget. And third, you keep the added layer of silicon so thin that vias all the way through to the base wafer's top interconnect layer need be no deeper than a typical isolation trench. This allows you to form the vias with conventional moderate-aspect-ratio etch technology, allowing nearly arbitrary placement and potentially—depending on how you handle wafer alignment—very high density.

To be sure there are unresolved questions. Monolithic 3D is showing PowerPoints, not finished 3DICs. Sekar points to the stability of modern ultra-low-k interconnect stacks during wafer bonding, cleaving, and polishing operations as one such question. Others might include transistor variations induced by

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To be sure there are unresolved questions. Monolithic 3D is showing PowerPoints, not finished 3DICs. Sekar points to the stability of modern ultra-low-k interconnect stacks during wafer bonding, cleaving, and polishing operations as one such question. Others might include transistor variations induced by internal stresses in the silicon slices, and temperature management in the microscopically-thin silicon slices sandwiched between two thermally-insulating interconnect stacks.

The only way to answer such questions, Or-Bach and Sekar said, is to make devices. To that end Monolithic 3D is seeking licensee-partners to take PowerPoint to reality.

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Formerly the editorial director of ESD magazine, Embedded.com, and Embedded Systems Conferences, Ron Wilson now works for Altera. *He has over 38 years of experience in the electronics industry. He held a variety of editorial positions within EE Times from 1991 to 2006. Wilson also served as a writer and the publisher of ESD Magazine and has written and edited for EDN

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Formerly the editorial director of ESD magazine, Embedded.com, and Embedded Systems Conferences, Ron Wilson now works for Altera. *He has over 38 years of experience in the electronics industry. He held a variety of editorial positions within EE Times from 1991 to 2006. Wilson also served as a writer and the publisher of ISD Magazine and has written and edited for EDN Magazine and Computer Design. Wilson also has experience in design engineering, evaluation, customer training, market research, product marketing and marketing management. In addition, Wilson's work has been published in a variety of media, including newspaper and magazine articles, portions of two books on electronics and a long-running Blog on SoC design for EDN. Additionally, Wilson is a pioneer in the electronics marketplace. He created the first virtual event in 2002 entitled "SOC-Online" and created the EETimes Industry Challenge series addressing key issues in electronics which incorporated research, print online and live events. *per EETimes press release date July 1, 2010.

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