

UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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MICRON TECHNOLOGY, INC., and  
MICRON SEMICONDUCTOR PRODUCTS, INC.,  
Petitioner

v.

PALISADE TECHNOLOGIES, LLP,  
Patent Owner.

**DECLARATION OF R. JACOB BAKER PH.D., P.E.  
IN SUPPORT OF PETITION FOR INTER PARTES REVIEW  
OF U.S. PATENT NO. 8,148,962**

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## **I. INTRODUCTION**

1. I have been retained by Micron Technology, Inc. (“Petitioner” or “Micron”) as an independent expert consultant in this proceeding before the Patent Trial and Appeal Board (“PTAB” or “Board”). I understand that Micron is requesting that the Board institute an *inter partes* review (“IPR”) proceeding of U.S. Patent No. 8,148,962 (“the ’962 Patent”) (Ex-1001), currently assigned to Palisade Technologies, LLP (“Patent Owner” or “PO”).

2. I am being compensated at my usual and customary rate of \$765 per hour. No part of my compensation depends on the outcome of this proceeding, and I have no other interest in this proceeding.

3. I have been asked to provide my independent analysis of the ’962 Patent in light of the prior art publications cited below. I have also been asked to consider the state of the art and prior art available as of May 12, 2009. Based on the prior art discussed in this declaration, it is my opinion that Claims 1, 7-11, 14, and 16-20 of the ’962 Patent are unpatentable for the reasons provided below.

### **A. Qualifications**

4. My qualifications generally are set forth in my *curriculum vitae*, which is submitted as Ex-1003.

5. I started working as an Engineer in 1985 and I started teaching Electrical and Computer Engineering courses in 1991. I am currently a Professor

Emeritus of Electrical and Computer Engineering at the University of Nevada, Las Vegas (“UNLV”). I am the named inventor on over 150 U.S. patents resulting from my industry work.

6. I received B.S. and M.S. degrees in Electrical Engineering from UNLV in 1986 and 1988, respectively. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno, in 1993.

7. My doctoral research, culminating in the award of a Ph.D., investigated the use of power MOSFETs in the design of very high peak power, and high-speed, instrumentation. I developed techniques to reliably stack power MOSFETs to switch higher voltages, that is, greater than 1,000 V and 100 Amps of current with nanosecond switching times. This work was reported in the paper entitled “Transformerless Capacitive Coupling of Gate Signals for Series Operation of Power MOSFET Devices,” published in the IEEE Transactions on Power Electronics. The paper received the Best Paper Award in 2000.

### **Industry Experience**

8. I have done technical and expert witness consulting for over 200 companies since I started working as an engineer in 1985. From 1985 to 1993 I worked for EG&G Energy Measurements and the Lawrence Livermore National Laboratory designing nuclear diagnostic instrumentation for underground nuclear weapon tests at the Nevada test site. During this time, I designed, and oversaw the

fabrication of, over 30 electronic and electro-optic instruments including high-speed cable and fiber-optic receiver/transmitters, PLLs, frame and bit-syncs, data converters, streak-camera sweep circuits, Pockel's cell drivers, micro-channel plate gating circuits, charging circuits for battery backup of equipment for recording test data, and analog oscilloscope electronics.

9. My work during this time, as one example, had a direct impact on my doctoral research work using power MOSFETs, subsequent publishing efforts, and industry designs. In addition to the 2000 Best Paper Award from the IEEE Power Electronics Society, I published several other papers in related areas while working in industry. I hold a patent, Patent No. 5,874,830, in the area of power supply design, titled, "Adaptively biased voltage regulator and operating method," which was issued on February 23, 1999. I have designed dozens of linear and switching power supplies for commercial products and scientific instrumentation.

10. I am a licensed Professional Engineer and have extensive industry experience in circuit design, fabrication, and manufacture of Dynamic Random Access Memory (DRAM) semiconductor integrated circuit chips, Phase-Change Random Access Memory (PCRAM) chips, and CMOS Image Sensors (CISs) at Micron Technology, Inc. ("MTI") in Boise, Idaho. I spent considerable time working on the development of flash memory chips while at MTI. My efforts resulted in more than a dozen patents relating to flash memory. One of my projects at MTI included

the development, design, and testing of circuit design techniques for a multi-level cell (MLC) flash memory using signal processing. This effort resulted in higher-density memories for use in solid-state drives and flash memory cards having an ATA interface that are ubiquitous in consumer electronics including cameras and data storage systems. Further, the use of higher-density memory can result in fewer changes in the flash translation layer for logical to physical addressing, less need for garbage collection, and larger data segments that can improve a computing system's performance. Another project I worked on at MTI focused on the design of buffers for high-speed double-data rate DRAM which resulted in around 10 U.S. patents in buffer design. Among many other experiences, I led the development of the delay locked loop (DLL) in the late 1990s so that MTI DRAM products could transition to the DDR memory protocol, used in mobile and non-mobile (server, desktop, cell phones, tablets, etc.) computing systems as main computer memory, for addressing and controlling accesses to memory via interprocess communications (IPC) with the memory controller (MC). I provided technical assistance with MTI acquisition of Photobit during 2001 and 2002, including transitioning the manufacture of CIS products into MTI's process technology. Further, I did consulting work at Sun Microsystems and then Oracle on the design of memory modules during 2009 and 2010. This work entailed the design of low-power, high-speed, and wide

interconnection methods with the goal of transmitting data to/from the memory module and the MC at higher speeds.

11. I have extensive experience in the development of instrumentation and commercial products in a multitude of areas including: integrated electrical/biological circuits and systems, array (memory, imagers, and displays) circuit design, CMOS analog and digital circuit design, diagnostic electrical and electro-optic instrumentation for scientific research, CAD tool development and online tutorials, low-power interconnect and packaging techniques, design of communication/interface circuits (to meet commercial standards such as USB, firewire, DDR, PCIe, SPI, etc.), circuit design for the use and storage of renewable energy, and power electronics. For example, a part of my research at Boise State, for many years, focused on the use of Thru-Silicon-Vias (TSVs), aka Thru-Wafer Vias (TWVs), for high-density packaging. These packaging techniques were utilized in the memory module development work I did with Sun Microsystems and Oracle. As another example, I've designed circuitry for use in implementing Universal Serial Bus (USB) interface circuits while I did consulting at Tower Semiconductor. I designed PCI communication circuits for IPC between a Graphics Processor Unit (GPU) and memory while consulting for Rendition, Inc.

12. My current research work is focused in part on the design of integrated circuits for wireless sensing using LIDAR (LIght Detection And Ranging). I have

worked with several companies in the development of these circuits and systems including Freedom Photonics, Aerius Photonics and FLIR. In the early 1990s, I worked on wireless systems for wideband impulse radar while at Lawrence Livermore Laboratory. Further, part of my research for several years focused on the digitization of IQ channels using delta-sigma modulation. The knowledge and experience gained from this effort are reflected in my textbook *CMOS Mixed-Signal Circuit Design* and a presentation, which I have presented at several universities and companies, [http://cmosedu.com/jbaker/papers/talks/BP\\_DSM\\_talk.pdf](http://cmosedu.com/jbaker/papers/talks/BP_DSM_talk.pdf).

### **Academic Experience**

13. I was an adjunct faculty member in the Electrical Engineering department of the University of Nevada, Las Vegas in 1991 and 1992. From 1993 to 2000, I served on the faculty at the University of Idaho as an Assistant Professor and then as a tenured Associate Professor of Electrical Engineering. In 2000, I joined a new Electrical and Computer Engineering program at Boise State University (“BSU”) where I served as department chair from 2004 to 2007. At BSU, I helped establish graduate programs in Electrical and Computer Engineering including, in 2006, the university’s second Ph.D. degree. In 2012, I re-joined the faculty at UNLV. Over the course of my career as a professor, I have advised over 100 masters and doctoral students.

14. I have been recognized for my contributions as an educator in the field. While at Boise State University, I received the President's Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001). In 2007, I received the Frederick Emmons Terman Award (the "Father of Silicon Valley"). The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator's contributions to the profession. In 2011 I received the IEEE Circuits and Systems Education Award. I received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor Award every year it was awarded while I have been back at UNLV.

15. I have authored several books and papers in the electrical and computer engineering area. My published books include *CMOS Circuit Design, Layout, and Simulation* (Baker, R.J., *Wiley-IEEE*, ISBN: 9781119481515 (4th ed., 2019)) and *CMOS Mixed-Signal Circuit Design* (Baker, R.J., *Wiley-IEEE*, ISBN: 9780470290262 (2nd ed., 2009) and ISBN: 9780471227540 (1st ed., 2002)). I co-authored *DRAM Circuit Design: Fundamental and High-Speed Topics* (Keeth, B., Baker, R.J., Johnson, B., and Lin, F., *Wiley-IEEE*, ISBN: 9780470184752 (2008)), *DRAM Circuit Design: A Tutorial* (Keeth, B. and Baker, R.J., *Wiley-IEEE*, ISBN: 0-7803-6014-1 (2001)), and *CMOS Circuit Design, Layout and Simulation* (Baker, R.J., Li, H.W., and Boyce, D.E., *Wiley-IEEE*, ISBN: 9780780334168 (1998)). I

contributed as an editor and co-author on several other electrical and computer engineering books.

**Other Relevant Experience**

16. I have given more than 50 invited talks at conferences, companies, and universities. Further, I am the author or co-author of more than 100 papers and presentations in the areas of electrical and computer engineering design, fabrication and packaging.

17. I currently serve, or have served, as a volunteer on: the IEEE Press Editorial Board (1999-2004); as editor for the Wiley-IEEE Press Book Series on Microelectronic Systems (2010-2018); as the Technical Program Chair of the 2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS 2015); on the IEEE Solid-State Circuits Society (SSCS) Administrative Committee (2011-2016); as a Distinguished Lecturer for the SSCS (2012-2015); and as the Technology Editor (2012-2014) and Editor-in-Chief (2015-2020) for *IEEE Solid-State Circuits Magazine*. These meetings, groups, and publications are intended to allow researchers to share and coordinate research. My active participation in these meetings, groups, and publications allowed me to see what other researchers in the field have been doing.

18. In addition to the above, I am an IEEE Fellow for contributions to semiconductor memory design and a member of the honor societies Eta Kappa Nu and Tau Beta Pi.

**B. Materials Considered**

19. In forming my opinions, I reviewed the following documents, in addition to others I have cited in my declaration.

| Ex. No. | Description                                                                                                                                                                   |
|---------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ex-1001 | U.S. Patent No. 8,148,962 (“the ’962 Patent”)                                                                                                                                 |
| Ex-1004 | Prosecution History of U.S. Patent No. 8,148,962 (App. No. 12/464,301)                                                                                                        |
| Ex-1005 | U.S. Patent No. 7,151,363 (“Scott”)                                                                                                                                           |
| Ex-1006 | U.S. Patent No. 7,026,802 (“Gradinariu”)                                                                                                                                      |
| Ex-1007 | Def.’s Opening Claim Construction Br., <i>Palisade Technologies, LLP. v. Micron Tech., Inc.</i> , ECF No. 58, No. 7:24-cv-00262 (W.D. Tex. July 30, 2025)                     |
| Ex-1008 | Joint Claim Construction Statement, <i>Palisade Technologies, LLP. v. Micron Tech., Inc.</i> , ECF No. 90, No. 7:24-cv-00262 (W.D. Tex. Sept. 22, 2025)                       |
| Ex-1009 | Claim Construction Order and Memorandum in Support Thereof, <i>Palisade Technologies, LLP. v. Micron Tech., Inc.</i> , ECF No. 93, No. 7:24-cv-00262 (W.D. Tex. Oct. 3, 2025) |
| Ex-1010 | John Watson, <i>Mastering Electronics</i> (3d ed. 1990)                                                                                                                       |
| Ex-1011 | Yuan Taur & Tak H. Ning, <i>Fundamentals of Modern VLSI Devices</i> (1998)                                                                                                    |

| Ex. No. | Description                                                                                            |
|---------|--------------------------------------------------------------------------------------------------------|
| Ex-1012 | Paul R. Gray & Robert G. Meyer, <i>Analysis and Design of Analog Integrated Circuits</i> (2d ed. 1984) |

## II. LEGAL STANDARDS

20. In forming my opinions and considering the subject matter of the '962 Patent and its claims in light of the prior art, I am relying on certain legal principles that counsel in this case explained to me. My understanding of these concepts is summarized below.

21. I understand that earlier publications and patents may act to render a patent unpatentable for one of two reasons: (1) anticipation and (2) obviousness.

### A. Anticipation

22. It is my understanding that the claims of a patent are anticipated by a prior art reference if each and every element of the claim is found either explicitly or inherently in the reference. I understand that inherency requires a showing that the missing descriptive matter in the claim is necessarily present in the allegedly anticipating reference, and that it would have been so recognized by a person of ordinary skill in the art ("POSITA").

23. I understand that when a challenged claim covers several structures, either generically or as alternatives, the claim is deemed anticipated if any of the structures within the scope of the claim is found in the prior art reference.

24. Although anticipation typically involves the analysis of a single prior art reference, I understand that additional references may be used to show that the prior art reference has enabling disclosure (i.e., allows a POSITA to make the invention without undue experimentation), to explain the meaning of a term used in the prior art reference, and/or to show that a characteristic is inherent in the prior art reference.

**B. Obviousness**

25. I understand that a claim is invalid as obvious if it would have been obvious to a person of ordinary skill in the art at the time the alleged invention was made. This means that even if all of the elements of the claim cannot be found in a single prior art reference that would anticipate the claim, a person of ordinary skill in the art who was aware of the prior art would have been able to come up with the claimed invention. This may be the case, for example, where the missing element represents only an insubstantial difference over the prior art or a reconfiguration of a known system. I understand that in an obviousness determination, the person of ordinary skill in the art is presumed to have knowledge of all material prior art.

26. I understand that an obviousness analysis requires an understanding of the scope and content of the prior art, any differences between the alleged invention and the prior art, and the level of ordinary skill in evaluating the pertinent art.

27. I understand that when a product is available, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill in the art can implement a predictable variation, obviousness likely bars its patentability. For the same reason, if a technique has been used to improve one device and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique would have been obvious.

28. I understand that whether a prior art reference renders a patent claim unpatentable as obvious is determined from the perspective of a person of ordinary skill in the art at the time of the alleged invention. I have been told that there is no requirement that the prior art contain an express suggestion to combine known elements to achieve the claimed invention, but a suggestion to combine known elements to achieve the claimed invention may come from the prior art, as filtered through the knowledge of one skilled in the art. In addition, I have been told that the inferences and creative steps a person of ordinary skill in the art would employ are relevant to the determination of obviousness.

29. I understand that one may consider, e.g., whether (1) the change was merely the predictable result of using prior art elements according to their known functions, or whether it was the result of true inventiveness; (2) there is some teaching or suggestion in the prior art to make the modification or combination of

elements claimed in the patent; (3) the claimed innovation applies a known technique that had been used to improve a similar device or method in a similar way; (4) the claimed invention would have been obvious to try, meaning that the claimed innovation was one of a relatively small number of possible approaches to the problem with a reasonable expectation of success by those skilled in the art; (5) the invention merely substituted one known element for another known element in order to obtain predictable results; (6) the invention merely applies a known technique to a known device, method, or product to yield predictable results; or (7) known work in one field of endeavor may have prompted variations of it for use in either the same field or a different one based on design incentives or other market forces that would have been predictable to a person of ordinary skill in the art.

30. I further understand that certain factors may support or rebut the obviousness of a claim. I understand that such secondary considerations include, among other things, commercial success of the patented invention, skepticism of those having ordinary skill in the art at the time of the invention, unexpected results of the invention, any long-felt but unsolved need in the art that was satisfied by the alleged invention, the failure of others to make the alleged invention, praise of the alleged invention by those having ordinary skill in the art, and copying of the alleged invention by others in the field. I understand that there must be a nexus—that is, a connection—between any such secondary considerations and the alleged invention.

I also understand that contemporaneous and independent invention by others is a secondary consideration tending to show obviousness.

31. I am not aware of any allegations by the named inventor of the '962 Patent or any assignee of the '962 Patent that any secondary considerations tend to rebut the obviousness of the '962 Patent.

32. Additionally, I understand that in considering obviousness, it is important not to use the benefit of hindsight derived from the patent under consideration.

**C. Level of Ordinary Skill in the Art**

33. When interpreting a patent, I understand that it is important to identify the relevant art pertaining to that patent, as well as the level of ordinary skill in that art at the time of the claimed invention. The “art” is the field of technology to which the patent is related.

34. I am informed and understand that a POSITA is a hypothetical person who is presumed to know the relevant prior art. I understand that the actual inventor’s skill is not determinative of the level of ordinary skill. I further understand that factors that may be considered in determining level of skill include: (i) the types of problems encountered in the art; (ii) prior art solutions to those problems; (iii) the rapidity with which innovations are made; (iv) the sophistication of the technology; and (v) the educational level of active workers in the field. I understand that not all

such factors may be present in every case, and one or more of them may predominate.

35. I understand that a POSITA is one who is presumed to be aware of all pertinent art, thinks along conventional wisdom in the art, and is a person of ordinary creativity.

36. A person of ordinary skill in the art at the relevant time, which I have been told to consider as around May 12, 2009 (“POSITA”) would have had a bachelor’s degree in computer engineering, electrical engineering or a closely related field, along with at least two years of experience in the research, design, development, implementation, or management of semiconductor devices or integrated circuits. An individual with an advanced degree in a relevant field, such as computer or electrical engineering, would require less experience in the development and use of memory devices and systems (e.g., 1-2 years).

37. Based on my education and experience, I would have, at least, met the criteria for a POSITA on May 12, 2009, and I still exceed it today.

**D. Claim Construction**

38. I understand that the United States Patent and Trademark Office interprets claim terms in an *inter partes* review proceeding under the same claim construction standard that is used in a United States federal court. I understand that

under this standard, the meaning of claim terms is considered from the viewpoint of a POSITA at the time of the alleged invention.

39. I have been informed that claim terms are generally given their ordinary and customary meaning as understood by one of ordinary skill in the art in light of the specification and the prosecution history pertaining to the patent. I understand, however, that claims terms are generally not limited by the embodiments described in the specification.

40. I understand that in addition to the claims, specification, and prosecution history, other evidence may be considered to ascertain the meaning of claim terms, including textbooks, encyclopedias, articles, and dictionaries. I have been informed that this other evidence is often less significant and less reliable than the claims, specification, and prosecution history.

41. I understand that a patent claim may be expressed using functional language, and that terms reciting “means” are presumptively subject to certain statutory requirements for so-called “means-plus-function” claiming. I understand that construing a means-plus-function limitation involves multiple steps. The first step is a determination of the function. The next step is to determine the corresponding structure, which can be disclosed anywhere in the specification. I understand that the corresponding structure must be clearly linked with the associated function.

### III. SUMMARY OF GROUNDS

42. I understand that Petitioner challenges the validity of Claims 1, 7-11, 14, and 16-20 of the '962 Patent. It is my opinion that the following grounds demonstrate that the claims of the '962 Patent are invalid:

| Ground | Summary                                                                                                                      |
|--------|------------------------------------------------------------------------------------------------------------------------------|
| 1      | Claims 1, 7-11, 14, and 16-20 are obvious over U.S. Patent No. 7,151,363 ("Scott") (Ex-1005)                                 |
| 2      | Claims 1, 7-11, 14, and 16-20 are obvious over Scott (Ex-1005) in view of U.S. Patent No. 7,026,802 ("Gradinariu") (Ex-1006) |

### IV. THE '962 Patent

#### A. Overview of the '962 Patent

43. The '962 Patent generally relates to systems and methods for improved voltage regulation. Ex-1001, Abstract. Voltage regulation refers to the process of "stabiliz[ing] a source voltage in light of a varying output load." *Id.*, 1:5-7.

44. Loads that are coupled to a power supply can selectively operate circuitry to preserve battery resources. Ex-1001, 1:11-18. For example, a mobile phone may deactivate its camera circuitry when the camera is not in use. *Id.*, 1:11-18, 4:52-66. However, this selective activation and deactivation of circuitry causes variations in the supply voltage. *Id.*, 1:19-24. Most electrical circuits require a stable

supply voltage to function properly. *Id.*, 1:19-24, 4:66-5:2. To address this issue, circuits may include a voltage regulator, which receives a voltage from the power supply and delivers a stable voltage to the load, even when load conditions vary. *Id.*, 1:25-27, 5:2-6.

45. Figure 2 of the '962 Patent (annotated below) illustrates a circuit diagram of a prior art voltage regulator, which the patentee refers to as a “source follower.” Ex-1001, 5:7-8, *see also* 1:25-34. This prior art voltage regulator includes a differential amplifier (orange box) and a pass transistor (blue box). *Id.*, 5:8-10, Fig. 2. One end (132) of the pass transistor is connected to a load (green box) to supply power to the load (green arrow). *Id.*, 1:31-32, 5:7-18, Fig. 2. The output voltage is fed back (orange arrow) to the differential amplifier (orange box), where it is compared to a reference voltage. *Id.*, 5:7-18, Fig. 2. The output of the differential amplifier is a “control voltage” (blue arrow) that drives the gate of the pass transistor (blue box). *Id.*, 1:32-34, 5:7-18, Fig. 2. This feedback arrangement enables the pass device to maintain a substantially constant output to the load by responding to variations in output voltage. *Id.*, 5:15-22.

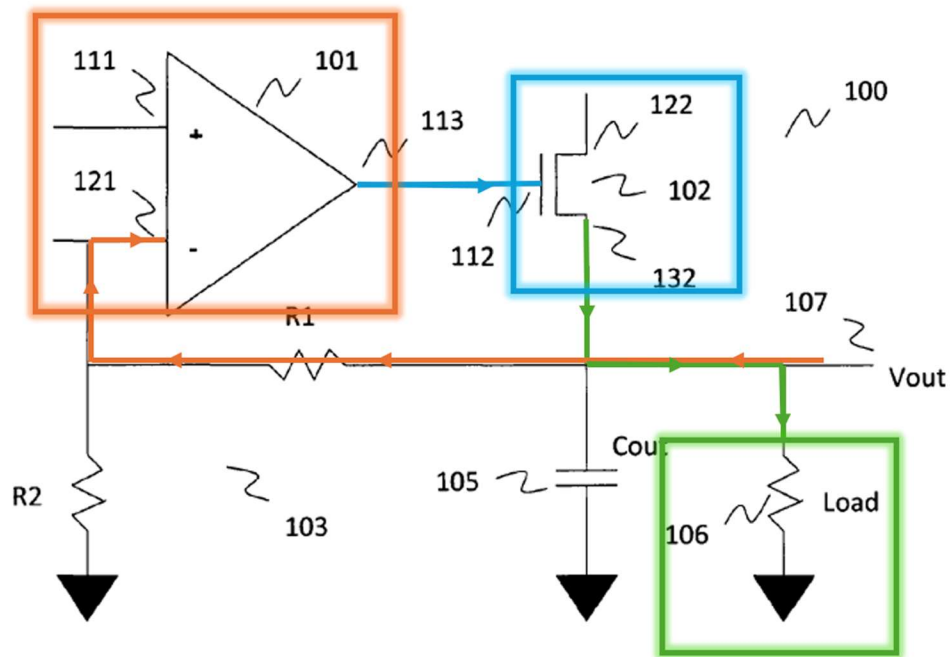


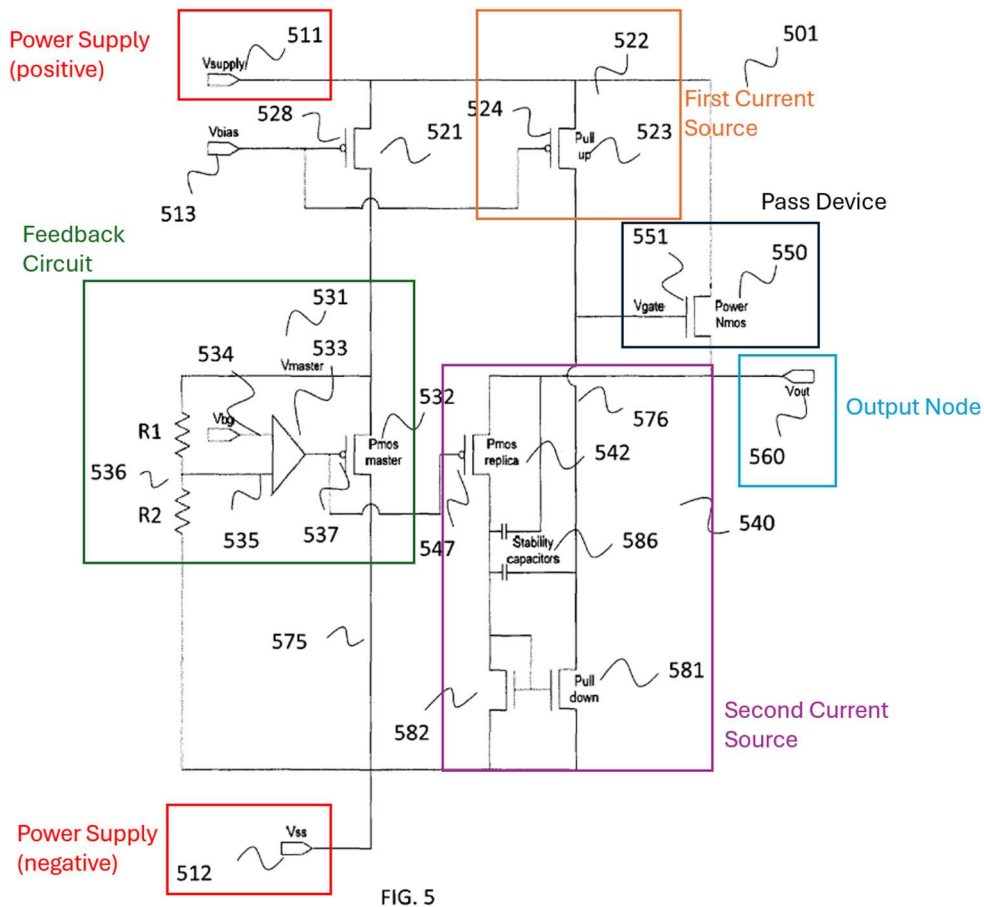
FIG. 2  
Prior Art

'962 Patent, Fig. 2 (annotated).

46. The '962 Patent criticizes the source follower of Figure 2, asserting that it relies on a large capacitor (105), which increases the size and complexity of the circuit. Ex-1001, 1:42-47, 5:22-32. The '962 Patent further contends that the source follower of Figure 2 “is ineffective at regulating voltage for circuits operating at certain frequencies, such as below 100 kHz.” *Id.*, 5:32-35, *see also id.*, 1:35-41. In view of these alleged deficiencies, the '962 Patent purports to disclose an “improved voltage regulator.” *Id.*, Abstract. According to the patentee, embodiments of the alleged invention provide a voltage regulator that does not rely on a large capacitor

and is effective for circuits operating at both low and high frequencies. *Id.*, 3:62-4:8, 5:36-44.

47. According to the patentee, the voltage regulators of the '962 Patent “are advantageous because they supply a load source current via a single current path... thus reducing power consumption compared to other known regulators.” Ex-1001, 8:41-45. An exemplary embodiment is illustrated in Figure 5, annotated below.



*Id.*, Fig. 5 (annotated).

48. The voltage regulator of Figure 5 receives input from a power supply that includes a positive terminal and a negative terminal (red boxes). Ex-1001, 5:45-51, Fig. 5. It supplies a regulated voltage to a load at the output node (blue box). *Id.*

49. The voltage regulator includes four main components that collectively perform the described voltage regulation: (1) a “feedback circuit” (green box); (2) a first current source (orange box); (3) a second current source (purple box); and (4) a pass device (black box). Ex-1001, 2:25-53, 8:46-9:63, Fig. 5. The details of each of these components is described below.

50. *First*, the regulator includes a “feedback circuit” (green box) coupled to the first current path (575). Ex-1001, 2:25-27, Fig. 5. The feedback circuit “maintain[s] a voltage at a gate of feedback transistor 532 substantially constant.” *Id.*, 8:48-50. To do so, it includes a differential amplifier (534) that compares two inputs: (1) a “voltage proportional to a voltage across the drain and source terminals of feedback transistor” (535); and (2) a reference voltage (534), such as the bandgap voltage. *Id.*, 8:50-57, Fig. 5. The output of this comparison is the “substantially constant” voltage, which is supplied to the gate (537) of the feedback transistor and supplied as an input to the second current source (purple box). *Id.*, 8:46-60, 9:13-15, Fig. 5.

51. *Second*, the regulator includes a first current source (orange box) that supplies a substantially constant current to the second current path (576). Ex-1001,

2:30-32, 8:61-9:8, Fig. 5. In the embodiment of Figure 5, the first current source is a slave transistor (523) because its gate is electrically coupled to the gate of a master transistor (521). *Id.*, 8:63-66, Fig. 5. The magnitude of the constant current supplied by the first current source is determined by the bias voltage (513). *Id.*, 2:30-32, 8:67-9:8, Fig. 5.

52. *Third*, the regulator includes a second current source (purple box). The second current source supplies a variable current to the second current path (576) that is inverse to the voltage at the output node (560). When the voltage at the output node increases, the second current source causes the current in the second current path to decrease. Conversely, when the voltage at the output node decreases, the second current source causes the current in the second current path to increase.

53. To do so, the second current source includes a replica transistor (542) with a gate coupled to the gate of the “feedback transistor.” *Id.* The drain of the replica transistor is coupled to the output of the voltage regulator (560). *Id.*, 9:13-17. Because of this arrangement, the current through the replica transistor increases when the regulator’s output voltage increases, and decreases when the output voltage decreases. *Id.*, 9:17-20. The current through the replica transistor drives the gate of the “pull down” transistor 581. *Id.*, 9:40-44. When the current at this gate increases, the transistor pulls down more current through the second current path, reducing the overall current. *Id.*, 9:64-10:9. Conversely, when the current at the gate of the pull

down transistor decreases, the transistor pulls down less current, causing the current of the second current path to increase. *Id.*

54. *Fourth*, the regulator includes a pass device (black box). *Id.*, 2:40-50, 9:55-63, Fig. 5. The pass device is a transistor with its gate coupled to the second current path. *Id.* The pass device provides load current to the output of the voltage regulator based on the current of the second current path. *Id.*

#### **B. Prosecution History of the '962 Patent**

55. The '962 file history is submitted as Ex-1004. The application was originally filed on May 12, 2009. A Notice to File Corrected Application Papers was issued on May 28, 2009 due to issues with erasures and overwriting in at least Figures 1-5. The applicant filed a Preliminary Amendment on July 28, 2009, replacing Figure 2 and updating Figures 1 and 3-7.

56. A Non-Final Rejection was issued on August 16, 2011 rejecting claims 1-12 and 18-20 as indefinite. The applicant was instructed that “[t]he entire disclosure, i.e. specification, abstracts, and claims should be revised carefully” to “facilitate finding support for the recited limitations, as well as to provide proper antecedence for all claimed limitations.” The applicant submitted an Amendment/Request for Reconsideration on November 16, 2011, making modest amendments to just the claims. The examiner issued a Notice of Allowance on November 29, 2011. *See generally* Ex-1004.

## **V. TECHNOLOGY BACKGROUND**

57. The '962 Patent relies on some fundamental concepts of electronics and integrated circuits. Prior to the priority date, these components were widely used and understood. The following sections summarize well-understood electronics and integrated circuits concepts that a POSITA would have understood at that time. Each of these concepts would have been implemented in integrated circuits, and POSITAs would have reliably and predictably known how to do so.

### **A. Electronic Circuits and Basic Components**

58. It was well known to a person of ordinary skill in the art prior to the alleged invention date that matter is made up of atoms, which include electrons orbiting a nucleus. *See* Ex-1010, 7. Free electrons, which are electrons that are not bound to any nucleus, are contained in large numbers in materials called conductors (e.g., metals such as copper), which conduct the flow of electrons in a uniform direction. *Id.*, 8-10. This flow of electrons is called current and is expressed in units of amperes. *Id.* On the other hand, “[m]aterials that are classed as insulators contain only a very few free electrons” and do not conduct current well. *Id.*, 8. It was well known in electrical engineering that current is at the heart of virtually all electrical principles and technologies.

59. A person of ordinary skill would have known that, whereas current may flow continuously in one direction through a circuit (direct current), “[c]urrent that

flows first one way and then the other is called alternating current, and a voltage source supplying such a current is called an alternating voltage.” Ex-1010, 12. It was known that “[a]lternating current is used for all mains power supplies because a.c. [i.e., alternating current] permits the user of transformers to increase and decrease the voltage, so that the power can be transmitted from place to place using efficient high-voltage transmission lines.” *Id.* It was known that alternating current and alternating voltage are periodic, and “[t]he rate at which the voltage reverses is the frequency of the alternation.” *Id.*

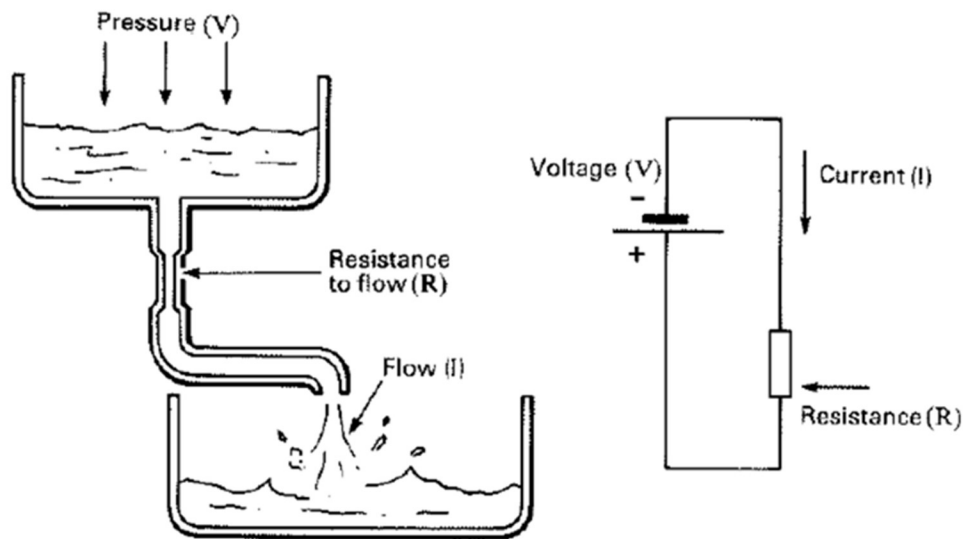
60. A person of ordinary skill would have known that “[i]n addition to measuring the current flow, we also need to measure another factor, the potential difference between two points,” which “is the energy difference between” the two points. Ex-1010, 10. The potential difference is also called voltage and is expressed in units of volts. *Id.*

61. Additionally, a person of ordinary skill would have known that resistance is another fundamental concept involved in the flow of electrons. Ex-1010, 10. “Resistance is a property of all materials that reduces the flow of electricity through them,” so that “[t]he higher the resistance, the more difficult it is for current to flow.” *Id.* Resistance is expressed in units of ohms. *Id.*, 11.

62. The relationship between current (denoted by the letter  $I$ ), voltage (denoted by the letter  $V$ ), and resistance (denoted by the letter  $R$ ) is given by Ohm's Law,  $V = I * R$  (i.e., voltage is current multiplied by resistance). Ex-1010, 10-11.

63. Figure 2.5 of John Watson's *Mastering Electronics* (an introductory electronics text), shows how the electrical principles of current, voltage, and resistance are analogous to principles relating to the flow of water.

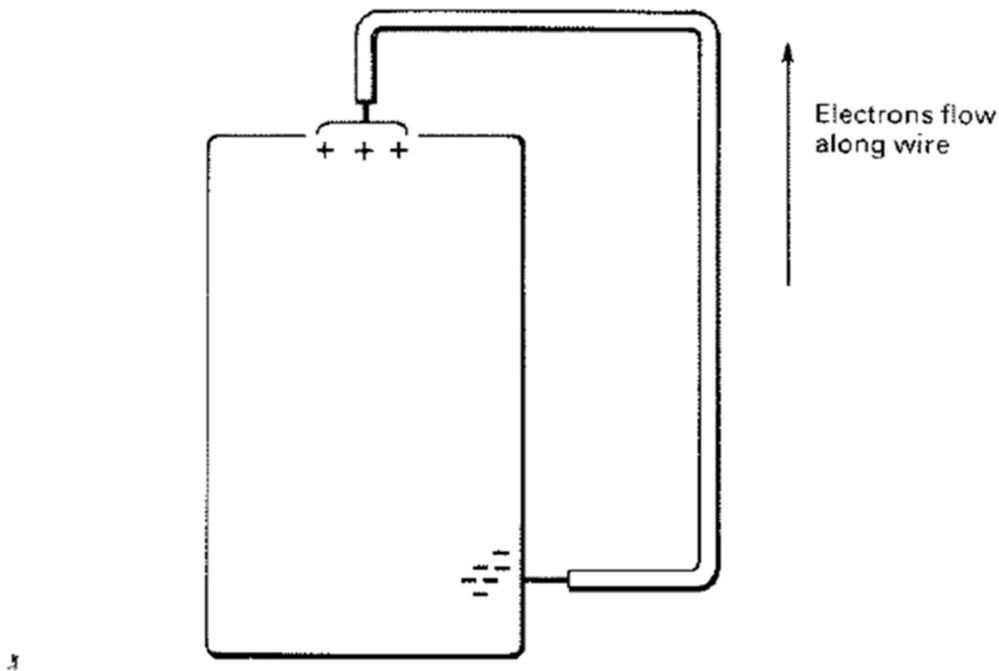
fig 2.5 a plumbing analogy: voltage, current and resistance all have their equivalents in the water system



*Id.*, Fig. 2.5.

64. A person of ordinary skill would have known that electrons (and thus current) flow in a circuit, as shown in Figure 2.3 below.

fig 2.3 *electrons flowing in a circuit*

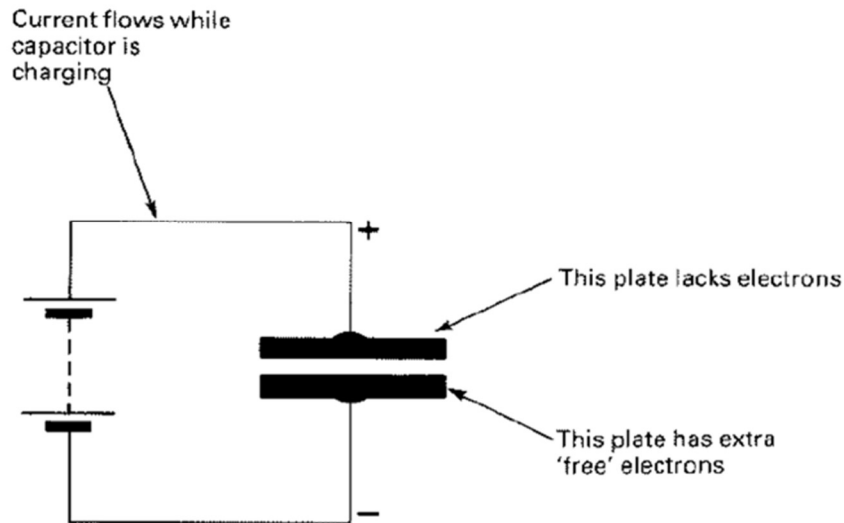


*Id.*, Fig. 2.3. A person of ordinary skill would have known that without a closed path (e.g., as shown above in Figure 2.3, above), current cannot flow. *Id.*, 8-11, FIGS. 2.3-2.5.

65. A person of ordinary skill would have also known that capacitors are common electronics components. Ex-1010, 25. “A capacitor is a component that can store electric charge,” and “[i]n essence, it consists of two flat parallel plates, very close to each other, but separated by an insulator.” *Id.* A person of ordinary skill would have known that “[w]hen the capacitor is connected to a voltage supply, a current will flow through the circuit” as shown below, and “[e]lectrons are stored in

one of the plates of the capacitor” and “in the other there is a shortage of electrons.”  
*Id.*, 25-27.

fig 3.8 *a capacitor connected to a power supply; current will flow until the capacitor is charged*



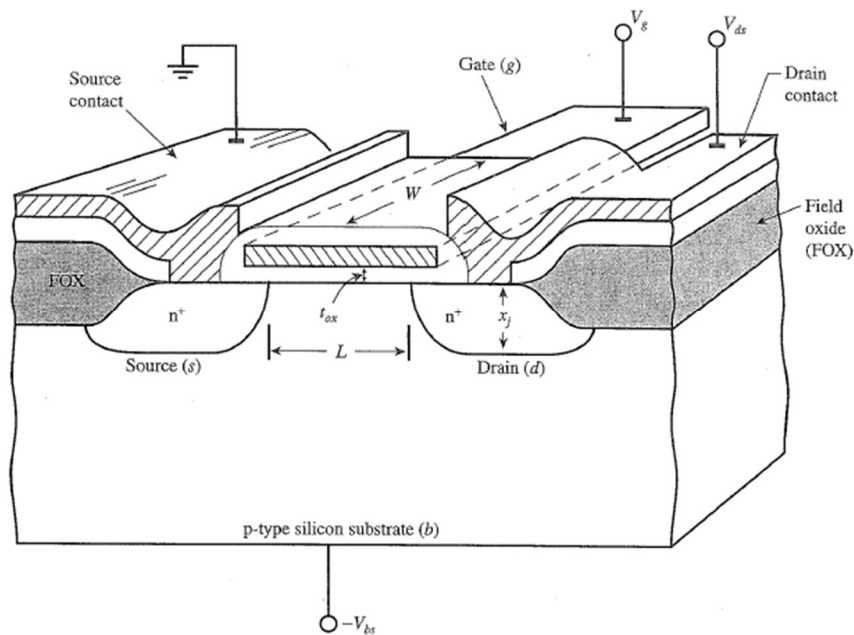
*Id.*, Fig. 3.8. A person of ordinary skill would have known that “[i]n this state the capacitor is said to be charged,” and “[i]f the charged capacitor is connected in a circuit, it will, for a short time, act as a voltage source, just like a battery.” *Id.*, 27.

#### **B. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)**

66. A metal oxide semiconductor field effect transistor (MOSFET) was known by those skilled in the art as the building block of circuits in various applications, including voltage regulators. *See* Ex-1011, 112. MOSFETs have been known since at least as early as 1960. *Id.*, at 2.

67. The MOSFET was known to be a four-terminal device with the terminals designated as gate, source, drain, and substrate (substrate is sometimes

referred to as a body). *Id.*, 112. The substrate was typically a silicon substrate. Although pure silicon is a poor conductor, the electrical conductivity of silicon was known to be increased by introducing impurity atoms, or dopants, into the silicon. Silicon material doped with p-type dopants is called p-type silicon, and silicon material doped with n-type dopants is called n-type silicon. An example MOSFET that includes a p-type silicon substrate and n-type source and drain regions that are each heavily doped compared to the substrate is shown below. *Id.*



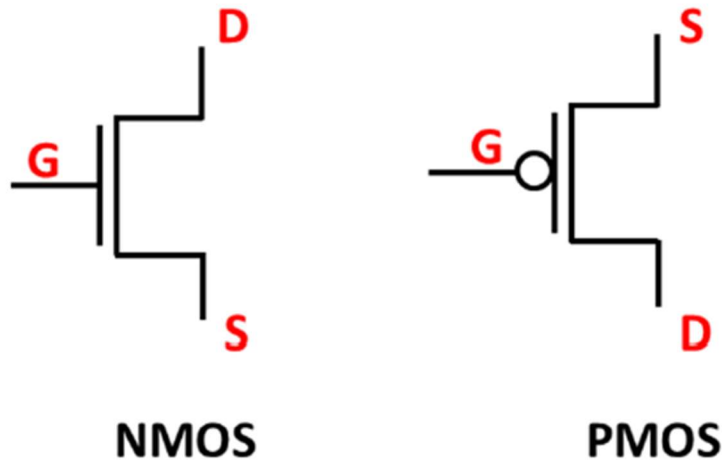
*Id.*, Fig. 3.1.

68. In configurations where the source and drain regions are heavily n-doped, similar to the configuration shown in Figure 3.1 above, the MOSFET was typically known as an n-channel MOSFET (or NMOSFET, NMOS transistor, or simply NMOS). Another type of MOSFET that was known is a p-channel MOSFET

(or PMOSFET, PMOS transistor, or simply PMOS), in which the dopant types are reversed compared to those of an n-channel MOSFET as I described above (and exemplary shown in Figure 3.1.) *See also* Ex-1011, 112.

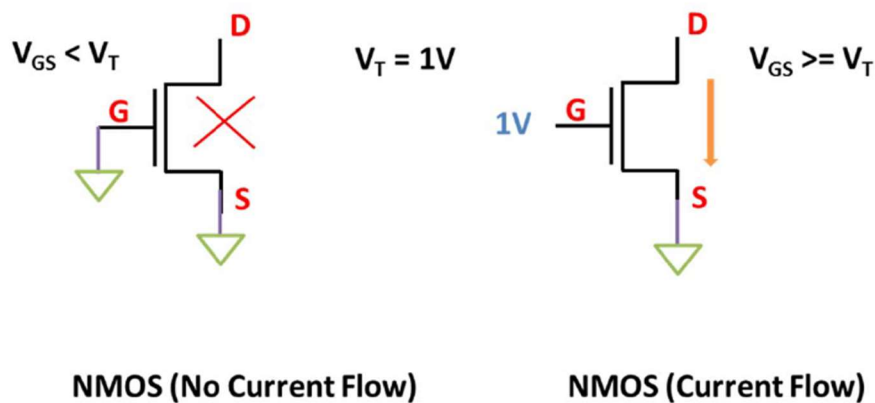
69. In the simplified model for a MOSFET, there is no current flow between the source and drain unless the voltage between gate and source terminals exceeds a threshold voltage. Ex-1011, 112. When a sufficiently large voltage (called the threshold voltage of the transistor or  $V_T$ ) is applied between the gate and the source, the silicon surface between the source and drain is inverted to n-type, which forms a conductive n-channel between the source and drain. *Id.* If there is a voltage difference between the source and drain, current will then flow between those terminals. *Id.* Thus, the MOSFET operates like a switch and conducts current depending on the  $|V_{GS}|$  (voltage between gate and source terminals). *Id.* For a PMOS, the current flows from source to drain when the gate voltage is below the source voltage by the threshold voltage. On the contrary, for an NMOS, the current flows from drain to source when the gate voltage is greater than the source voltage by the threshold voltage.

70. The following demonstratives illustrate the above basic concepts. Demonstrative A illustrates the symbols that were commonly attributed to an NMOS and a PMOS in circuit designs. The gate, drain, and source are respectively labeled G, D, and S in these demonstratives.



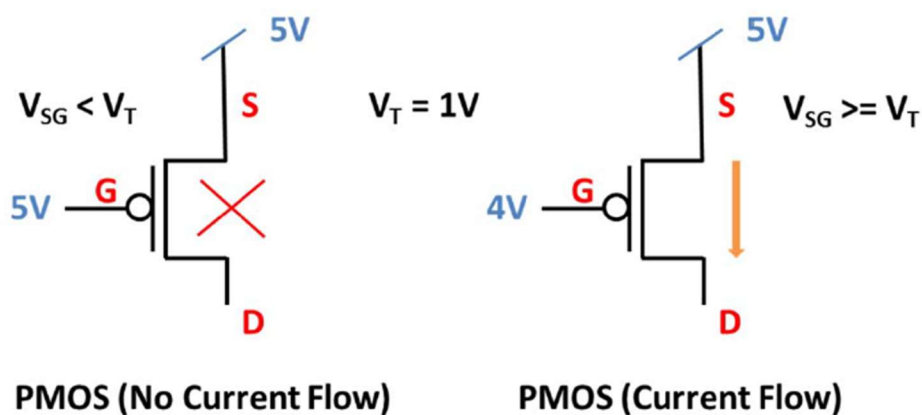
### DEMONSTRATIVE A

Demonstrative B illustrates an NMOS with a threshold voltage of 1V and describes that when the gate to source voltage ( $V_{GS}$ ) is less than 1V (e.g., both gate and source are at ground (shown by the green triangles), no current flows through the NMOS (represented by the red “X”), but when the gate to source voltage is greater than or equal to the threshold voltage, current flows from drain to source (shown by the orange arrow).



### DEMONSTRATIVE B

71. Demonstrative C similarly illustrates the operation of a PMOS with the difference being that for the PMOS, the gate voltage has to be lower than the source voltage for the PMOS to conduct current. That is, instead of  $V_{GS}$  being greater than  $V_T$ , the  $V_{SG}$  must be greater than  $V_T$ .



### DEMONSTRATIVE C

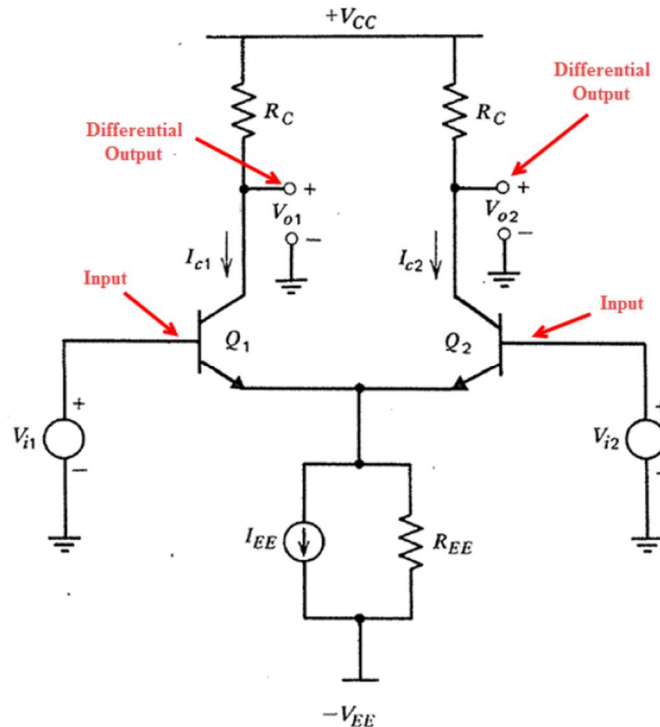
72. One of ordinary skill would have understood that the current-conducting capability of the MOSFET depends on the dimensions of the transistor, i.e., width (W) and length (L). When the MOSFET operates in the above-threshold region (i.e.,  $|V_{GS}|^1$  is greater than threshold), for a given  $V_{DS}$ , the MOSFET current (i.e., the drain-source or source-drain current) is proportional to  $|V_{GS}|$ , i.e., a higher  $|V_{GS}|$  results in a higher current through the MOSFET.

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<sup>1</sup> I use the absolute value sign with  $V_{GS}$  because for a PMOS, the  $V_{SG}$  has to be greater than threshold for the PMOS to conduct.

### C. Differential Amplifiers

73. A differential amplifier is a circuit component that accepts two inputs and amplifies the voltage difference between the two inputs. An example of a basic prior art differential amplifier is shown below:



Ex. 1012, Fig. 3.26.

74. In the above differential amplifier, bipolar transistors  $Q_1$  and  $Q_2$  form a transistor pair that amplifies the difference between the input voltages  $V_{i1}$  and  $V_{i2}$ . When  $V_{i1}$  is applied to transistor  $Q_1$ , the voltage drops across resistor  $R_C$  that is connected to  $Q_1$ , causing an output to appear at output terminal  $V_{o1}$ . At the same time, the current flow through transistor  $Q_1$  causes a voltage drop across resistor  $R_{EE}$ . Because both transistors  $Q_1$  and  $Q_2$  are connected to resistor  $R_{EE}$ , this voltage drop

causes the current flow through transistor  $Q_2$  to decrease, which in turn causes an output to appear at output terminal  $V_{o2}$ . The differential outputs  $V_{o1}$  and  $V_{o2}$  are inverted with respect to one another (i.e., equal and opposite), and can be used as differential inputs for subsequent circuit components or, if only a single output is needed, the other can be discarded.

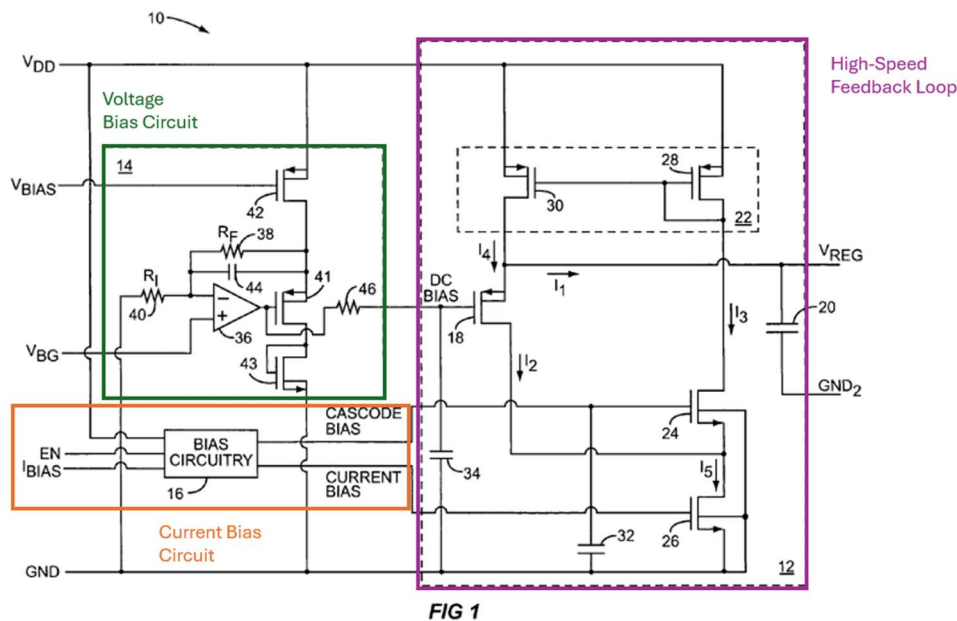
## **VI. THE PRIOR ART IN THE APPLIED INVALIDITY GROUNDS**

### **A. Scott (U.S. Patent No. 7,151,363) (Ex-1005)**

75. Scott is a U.S. patent that was issued on Dec. 19, 2006. Ex-1005, Cover. It issued from a patent application originally filed on Jun. 8, 2004. *Id.*

76. I understand Scott is prior art under at least pre-AIA §§ 102(a)-(b).

77. Scott is directed to a voltage regulator including a “high-speed feedback loop.” Ex-1005, Abstract, 1:6-10. Figure 1 (annotated below) illustrates that in addition to a high speed feedback loop (purple box), Scott’s voltage regulator includes voltage bias circuitry (green box) and current bias circuitry (orange box). *Id.*, 3:24-28.



*Id.*, Fig. 1 (annotated).

78. The high-speed feedback loop includes a reservoir capacitor (20). Ex-1005, 3:28-32. The capacitor stores a charge that corresponds to the regulated voltage ( $V_{\text{REG}}$ ). *Id.*, 3:47-51. When there is a dip in the regulated voltage, charge is drawn from the reservoir capacitor to maintain a consistent output voltage. *Id.*, 3:35-38, 3:62-63.

79. The reservoir capacitor is also coupled to the output of an output transistor (18). Ex-1005, 3:28-32. The output transistor provides a regulated voltage to charge the reservoir capacitor. *Id.*, 3:32-33. When no charge is drawn from the reservoir capacitor, the output transistor draws a current  $I_2$  which is based on a DC bias and the regulated voltage stored in the reservoir capacitor. *Id.*, 3:47-51. The

current I4 is essentially equal to I2, such that the current I1 is zero and the charge stored in the reservoir capacitor remains constant. *Id.*, 3:58-61.

80. When there is a dip in  $V_{REG}$ , charge is drawn from the reservoir capacitor, which leads to a reduction in the current I2 by reducing the gate-source voltage of the output transistor (18). *Id.*, 3:62-66. The current source (26) is biased by the current bias circuit to produce a constant current I5. *Id.*, 3:66-4:1. The high-speed feedback loop is arranged such that the sum of currents I2 and I3 is the constant current I5. *Id.*, 4:1-4. Thus, the reduction in the current I2 causes an immediate increase in the current I3. *Id.*

81. The high-speed feedback loop also includes a current mirror (22), which includes transistor 28 and transistor 30. *Id.*, 3:38-40, Fig. 1. Transistor 28 in the current mirror sinks the current I3, and transistor 30 provides a current I4, which is defined as the current I3 multiplied by a current mirror ratio gain (M). *Id.*, 3:52-55. Thus, the current mirror operates to increase the current I4 in response to the increase in the current I3. *Id.*, 4:4-8. When the current I4 becomes larger than the current I2, the current I1 increases, because the current I1 is essentially equal to the current I4 minus I2. *Id.*, 4:8-10. The increased current I1 charges the reservoir capacitor. *Id.*, 4:10-11.

82. As the charge in the reservoir capacitor increases, the current I2 increases, which causes currents I3, I4, and I1 to decrease. *Id.*, 4:11-13. When I2 has

increased to be equal to  $I_4$ , the reservoir capacitor has been charged to a point where  $V_{REG}$  is back to its desired value. *Id.*, 4:14-17.

83. Scott's voltage regulator also includes voltage bias circuitry (green box). Ex-1005, 4:66-67, Fig. 1. The voltage bias circuitry generates the DC bias from a bandgap voltage, and provides the DC bias to the output transistor (18). *Id.*, 4:67-5:2. To do so, it includes an operational amplifier (36) that compares the bandgap voltage and a voltage determined by the resistors  $R_F$  and  $R_I$ . *Id.*, 5:2-8. The values of  $R_F$  and  $R_I$  can be selected so the operational amplifier amplifies the bandgap voltage to provide the desired voltage. *Id.*, 5:8-11. The output of the operational amplifier is provided at the gate of transistor 41 and mirrored at the gate of output transistor 18, where the voltage is called the DC bias. *Id.*, 5:18-21, Fig. 1. The gate-source voltage of the output transistor adds to the DC bias to replicate the desired regulator output voltage. *Id.*

84. Scott's voltage regulator also includes the current bias circuitry (orange box). Ex-1005, 5:39-40, Fig. 1. The current bias circuitry operates to maintain the current source transistor 26 and cascade transistor 24 in saturation. *Id.*, 5:39-52. The particular implementation of the current bias circuitry is not the subject of the invention of Scott. *Id.*

**B. Gradinariu (U.S. Patent No. 7,026,802) (Ex-1006)**

85. Gradinariu is a U.S. patent that was issued on Apr. 11, 2006. Ex-1006, Cover. It issued from a patent application originally filed on Oct. 14, 2004. *Id.*

86. I understand Gradinariu is prior art under at least pre-AIA §§ 102(a)-(b).

87. Gradinariu is directed to a “replica biased voltage regulator circuit” that provides “continuous and proportional load regulation.” Ex-1006, Abstract, 1:8-10, 3:36-38. To do so, Gradinariu includes a supply section that supplies current to two current legs—an output leg and a replica leg. *Id.*, 3:55-58. The output leg provides an output voltage, and the replica leg provides a replica voltage. *Id.*, 4:1-3. Moreover, the current legs are arranged as “voltage mirrors,” such that the replica voltage is forced to track the output voltage. *Id.*, 4:3-6. The current legs are ideally arranged such that the voltages supplied by each of them are the same. *Id.*, 4:19-23.

88. Gradinariu’s voltage regulator supplies the replica voltage to an amplifier, where it is compared to a reference voltage. Ex-1006, 3:50-54, 4:24-28. Through this comparison, the amplifier provides negative feedback: it increases output when the replica voltage falls below the reference voltage and vice versa. *Id.*, 4:38-47. Because the output voltage and replica voltage are connected, variations in the output voltage are reflected in the replica voltage. *Id.*, 5:14-23. These variations

to the replica voltage are corrected by the amplifier, which are then reflected in the output voltage. *Id.*, 5:23-25.

## VII. CLAIM CONSTRUCTION

89. I understand that in a related district court proceeding, the parties have agreed that several terms in Claim 14 are so-called “means-plus-function” terms. I understand that for one term, the parties agreed on the identification of structure and function. That agreed construction is provided below.

| Term                                                                                                                                                                                                                                                                                                     | Agreed Construction:                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal” | <p>35 U.S.C. § 112, ¶6 applies.</p> <p><b>Function:</b> supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal</p> <p><b>Structure:</b> pass transistor 350 of Fig. 3, pass transistor 450 of Fig. 4, pass transistor 550 of Fig. 5, pass transistor 650 of Fig. 6, and equivalents, as described and shown at 5:58-67; 6:15-24; 7:27-51; 9:55-63; 10:54-62, Figs. 3, 4, 5, 6.</p> |

I apply this agreed construction for this claim term herein.

90. I understand that for three other terms in Claim 14 that the parties agreed are so-called “means-plus-function” terms, the parties agreed on the function, but not the structure. I understand that the parties presented arguments on the

appropriate structure for these terms, and the District Court construed these terms, as shown below.

| Term                                                                                                                                                          | District Court's Construction                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <p>“feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant” (Claim 14)</p>                                        | <p>35 U.S.C. § 112, ¶6 applies.</p> <p><b>Function:</b> maintaining a voltage at a gate of a feedback transistor substantially constant</p> <p><b>Structure:</b> Feedback circuit arranged as shown in Figure 3, element 331 including differential amplifier 333, voltage divider 336, and feedback transistor 332. Feedback circuit arranged as shown in Figure 4, including differential amplifier 433, voltage divider 436, and feedback transistor 432. Feedback circuit arranged as shown in Figure 5, element 531 including differential amplifier 533, voltage divider 536, and feedback transistor 532. Feedback circuit arranged as shown in Figure 6, element 631 including differential amplifier 633, voltage divider 636, and feedback transistor 632, and equivalents.</p> |
| <p>“first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant” (Claim 14)</p> | <p>35 U.S.C. § 112, ¶6 applies.</p> <p><b>Function:</b> supplying to a second current path referenced to said input a first current that is substantially constant</p> <p><b>Structure:</b> first current source 322 of Fig. 3, first current source 422 of Fig. 4, first current source 522 of Fig. 5, first current source 622 of Fig. 6, and equivalents, as described and shown at 6:25-41; 7:52-61; 8:61-9:8; 10:63-11:3, Figs. 3, 4, 5, 6.</p>                                                                                                                                                                                                                                                                                                                                      |
| <p>“second current supply means... for receiving a first voltage reference and a second voltage reference and for supplying a second current to said</p>      | <p>35 U.S.C. § 112, ¶6 applies.</p> <p><b>Function:</b> receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

|                                                                                                                          |                                                                                                                                                                                                                                                                                                    |
|--------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| second current path with a magnitude based on said first voltage reference and said second voltage reference” (Claim 14) | voltage reference<br><br><b>Structure:</b> second current source 340 of Fig. 3, second current source 440 of Fig. 4, second current source 540 of Fig. 5, second current source 640 of Fig. 6, and equivalents, as described and shown at 6:42-62; 7:62-8:17; 9:40-54; 10:40-53, Figs. 3, 4, 5, 6. |
|--------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

I apply these District Court constructions throughout this declaration.

91. For the remaining claim terms, I believe that the grounds below invalidate the challenged claims in a manner consistent with the '962 Patent and under any construction. It is my understanding that when interpreting the meaning of a claim, the PTAB only needs to construe the terms that are in controversy, and only to the extent necessary to resolve the controversy. Therefore, I do not think it is necessary for the Board to construe any other term to resolve whether the prior art invalidates the challenged claims of the '962 Patent.

92. I apply the plain and ordinary meaning to the claim terms, as that plain and ordinary meaning would have been understood by a POSITA. I understand that the parties disputed two other terms—“feedback circuit... including a feedback transistor” and “substantially constant”—in the underlying district court case. The court has adopted “plain and ordinary meaning” as the proper construction of both terms, and I have applied that construction herein.

93. I reserve the right to offer opinions on any claim constructions proposed in this proceeding or to offer opinions on additional constructions in the district court.

## **VIII. DETAILED EXPLANATION OF THE UNPATENTABILITY GROUNDS**

94. The subject matter of Claims 1, 7-11, 14, and 16-20 is disclosed by the prior art as shown below.

### **A. Ground 1: Claims 1, 7-11, 14, and 16-20 Are Obvious Over Scott**

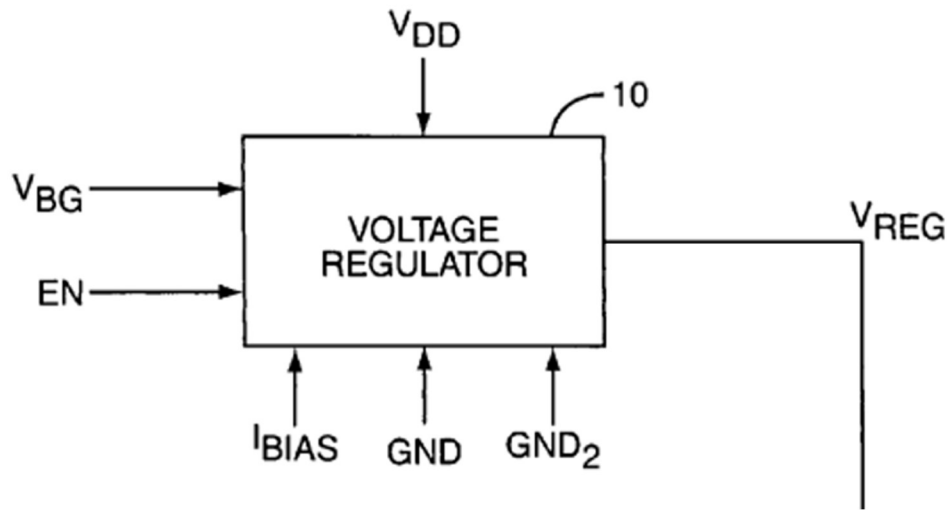
#### **1. Claim 1**

- a. Element 1[pre]: A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:**

95. To the extent the preamble is limiting, Scott discloses or teaches the preamble. The preamble has two requirements: (1) “[a] voltage regulator circuit integrated in an integrated circuit”; and (2) the voltage regulator circuit is “adapted to provide a voltage from a power supply to a load under varying load conditions.”

96. *First*, Scott discloses a voltage regulator circuit. Voltage regulator is in the title—“High PSRR, Fast Settle Time Voltage Regulator.” Figure 1 illustrates the voltage regulator circuit that is central to the invention. Ex-1005, Cover, 1:6-10, 3:24-26, Fig. 1. The specification confirms that the “present invention relates to a voltage regulator.” *Id.*, 1:6-8.

97. Further, Scott's voltage regulator circuit is "integrated in an integrated circuit." A POSITA would have understood that an integrated circuit is a circuit fabricated on a single semiconductor "chip," such as a silicon chip, rather than being built as separate parts and wired together. Indeed, the schematics seen in Scott show circuit blocks, such as current mirrors, that only function in an integrated circuit where the transistors are fabricated exactly the same, that is, matched. Scott emphasizes that all of the components of its voltage regulator form a circuit integrated on "a single semiconductor die." Ex-1005, 1:43-45; *see also* Cl. 12 ("[T]he reservoir capacitance, first circuitry, second circuitry, and the current mirror are fabricated on a single semiconductor die."). The patent figures further confirm that Scott's voltage regulator is integrated in an integrated circuit. A POSITA would have understood that integrated circuits can be represented in circuit diagrams as a rectangle with multiple pins representing inputs and outputs. This is because a designer integrating the circuit into a broader design can utilize the circuit by connecting to the integrated circuit's inputs and outputs, without concern for the exact details of the circuitry within the integrated circuit. Scott Figure 2 (below) represents its voltage regulator as a rectangle with several input pins and an output pin, indicating that it is an integrated circuit.



Ex-1005, Fig. 2 (excerpt). Moreover, a POSITA would have understood that voltage regulators are generally implemented as an integrated circuit, because voltage regulators require tightly coupled components, such as current mirrors which can only function in an integrated circuit as discussed above, and fast reaction times, making them ideal candidates for integration. Voltage regulators have been produced as ICs for decades to minimize cost and increase reliability.

98. *Second*, Scott discloses a voltage regulator circuit “adapted to provide a voltage from a power supply to a load under varying load conditions.” Figure 2 (excerpted above) illustrates that Scott’s voltage regulator receives power from a power supply  $V_{DD}$  (the claimed “power supply”) and supplies a regulated voltage  $V_{REG}$ . *Id.*, Fig. 2. The regulated voltage  $V_{REG}$  is supplied to the claimed load. *Id.*, 4:38-41 (disclosing “a load... connected to the regulated voltage  $V_{REG}$ ”). Moreover, Scott discloses that its load is under varying load conditions, because “the regulated

voltage ( $V_{REG}$ ) remains substantially constant as the load is varied.” *Id.*, 3:35-38.

Thus, Scott discloses the claimed varying load conditions.

99. Thus, Scott discloses or teaches Element 1[pre].

**b. Element 1[a]: an input adapted to receive a voltage from said power supply;**

100. As discussed in relation to Element 1[pre] (§ VIII.A.1.a, *supra*), Scott discloses a voltage regulator that receives a voltage  $V_{DD}$  from a power supply. Ex-1005, Figs. 1, 2. As illustrated in Figure 1 (annotated below), at least current source transistor 42 is an input adapted to receive a voltage  $V_{DD}$  from the power supply.

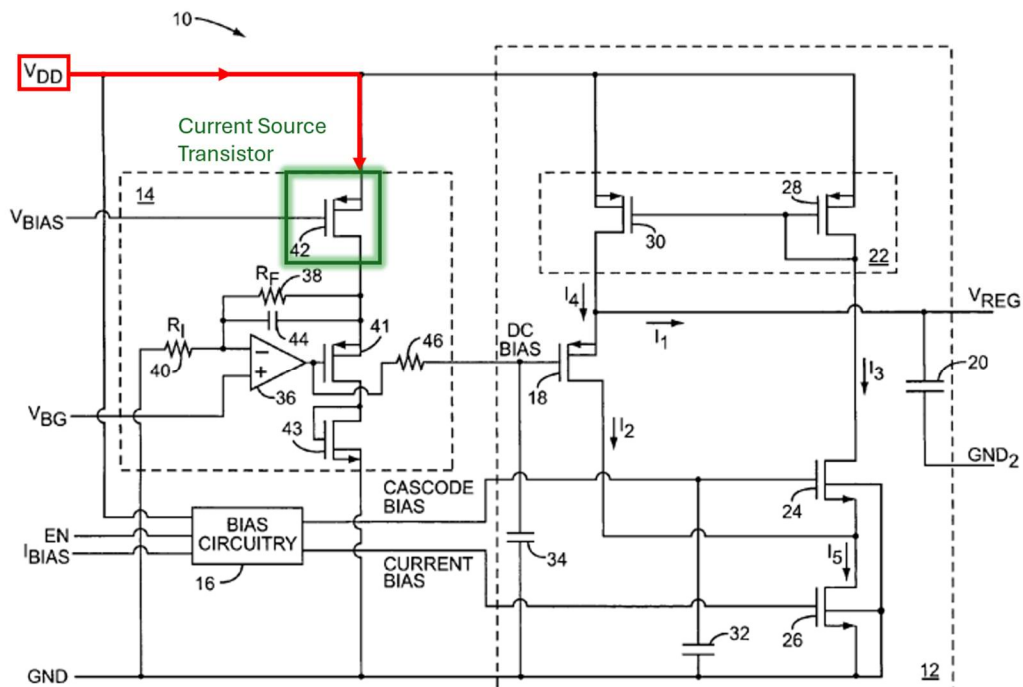


FIG 1

*Id.*, Fig. 1 (annotated); *see also* 5:2-7 (labeling transistor 42 as the “current source transistor”). Thus, at least current source transistor 42 is the claimed “input adapted to receive a voltage from said power supply.”

101. Thus, Scott discloses or teaches Element 1[a].

**c. Element 1[b]: an output adapted to be coupled to said load;**

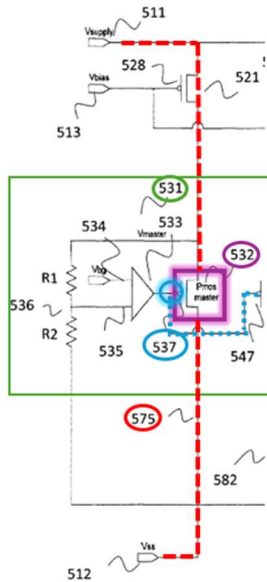
102. As discussed in relation to Element 1[pre] (§ VIII.A.1.a, *supra*), Scott discloses an output coupled to the load. For example, Scott discloses that “charge is drawn... by a load (not shown) connected to the regulated voltage ( $V_{\text{REG}}$ ).” Ex-1005, 4:39-41. The regulated voltage  $V_{\text{REG}}$  is the voltage regulator’s output, which Scott discloses is coupled to a load. *Id.*

103. Thus, Scott discloses or teaches Element 1[b].

**d. Element 1[c]: a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;**

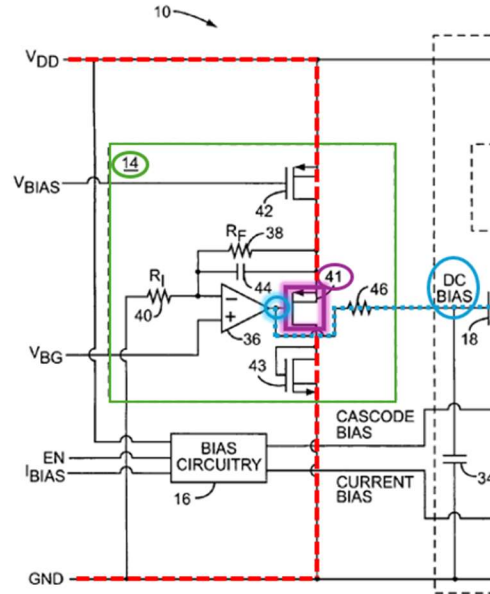
104. Element 1[c] requires a “feedback circuit” that (1) must be coupled to a first current path; (2) must include a “feedback transistor,” and (3) must maintain a substantially constant voltage at the gate of the “feedback transistor.” Scott’s voltage regulator includes voltage bias circuitry (14) (Ex-1005, 4:66-67), which matches the claimed “feedback circuit.” A comparison of the ’962 Patent’s Figure 5 and Scott’s Figure 1 (both annotated below) shows this. Scott’s voltage bias circuitry

discloses every element of the claimed feedback circuit in the same way as the '962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)

- Feedback Circuit:**
- 1) Coupled to **First Current Path**
  - 2) Includes **Feedback Transistor**
  - 3) Maintains **Substantially Constant Gate Voltage**



Scott, Fig. 1  
(annotated excerpt)

105. First, Scott's voltage bias circuitry is coupled to a first current path. In Figure 5 of the '962 Patent (annotated above), the first current path is labeled element 575 (red). Ex-1001, 9:4-7, Fig. 5. Figure 5 shows that the coupling to the feedback circuit comes between the first current path's connection to a power supply ( $V_{\text{supply}}$ ) and ground ( $V_{\text{ss}}$ ). *Id.* Scott's voltage bias circuitry (green) is similarly coupled to a first current path; the current path labeled in red connects a power supply ( $V_{\text{DD}}$ ) and ground (GND), just like the '962 Patent's first current path. Ex-1005, Fig. 1. Moreover, the first current path of both patents includes a current source transistor. Ex-1001, Fig. 5 (element 521); Ex-1005, Fig. 1 (element 42). The amount of current supplied to the feedback circuit in both patents is determined by a bias voltage at the

gate of the current source transistor. *Compare* Ex-1001, 8:65-9:4, Fig. 5; *with* Ex-1005, 5:2-21, Fig. 1. Thus, Scott discloses a feedback circuit coupled to a first current path.

106. *Second*, Scott's voltage bias circuitry includes a "feedback transistor." Scott calls its "feedback transistor" an "output matching transistor" (purple). Ex-1005, 5:2-7. In Figure 5 of the '962 Patent (annotated above), the feedback transistor (purple) is element 532. Ex-1001, 8:47-50, Fig. 5. The source of the '962 Patent's feedback transistor is connected to the power supply through the current source transistor 521, and its drain is connected to ground. *Id.*, Fig. 5, 9:1-4. Scott's "output matching transistor" (purple) is the claimed "feedback transistor," because it is also connected to the power supply through the current source transistor 42, and its drain is also connected to ground. Ex-1005, Fig. 1, 5:14-18. Moreover, the gate of both patents' "feedback transistors" is driven by the output of an amplifier that compares a bandgap voltage with a proportion of the supply voltage. *Compare* Ex-1001, 8:46-60, Fig. 5; *with* Ex-1005, 5:2-21, Fig. 1. Even though Scott does not use the same terminology as the '962 Patent, Scott's "output matching transistor" is connected in exactly the same way as the '962 Patent's "feedback transistor."

107. *Third*, Scott's voltage bias circuitry maintains a voltage at the gate of its feedback transistor "substantially constant" in the same manner as the '962 Patent. Scott's Figure 1 (annotated above) shows that the voltage at the gate (blue)

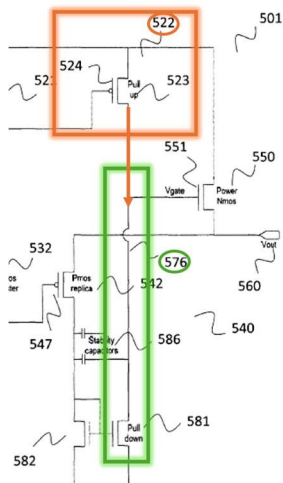
of the “feedback transistor” (purple) is maintained by an “operational amplifier 36” comparing a bandgap voltage  $V_{BG}$  and a resistor-divided voltage proportional to the transistor’s source-drain voltage, which is the same as how the ’962 Patent maintains the “substantially constant” voltage. *Compare* Ex-1005, 5:2-11, Fig. 1; *with* Ex-1001, 8:46-60, Fig. 5. Moreover, Scott labels the voltage provided to the gate of transistor 18 (blue line showing connection) as “DC BIAS.” Ex-1005, 4:66-5:2, 5:31-35, Fig. 1. DC BIAS is a substantially constant voltage, because the inputs of the amplifier (36) that supplies the voltage are selected to “provide the desired regulator output voltage ( $V_{REG}$ ),” which is designed to “remain[] substantially constant” *Id.*, 5:7-14, 3:37-38.

108. In summary, Scott’s voltage bias circuitry (green) is coupled to a first current path (red), includes a feedback transistor (purple), and maintains a voltage at the gate of the transistor substantially constant (blue). Thus, Scott discloses or teaches each limitation of Element 1[c].

**e. Element 1[d]: a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;**

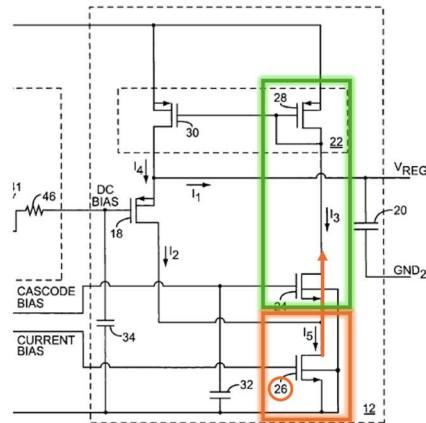
109. Element 1[d] requires a “first current supply circuit” that supplies a “substantially constant” current to a second current path. Scott’s voltage regulator includes a current source (26) (Ex-1005, 3:38-40), which matches the claimed first current supply circuit. A comparison of the ’962 Patent’s Figure 5 with Scott’s

Figure 1 (both annotated below) shows this. As further explained below, Scott's supply circuit discloses every element of the first current supply circuit in the same way as the '962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)

- First Current Supply Circuit:**
- 1) Supplies a **Substantially Constant Current**
  - 2) Current Supplied to **Second Current Path**



Scott, Fig. 1  
(annotated excerpt)

110. First, Scott's current source (orange) supplies a substantially constant current. Ex-1005, Fig. 1. For example, Scott discloses that "[t]he current source[] 26 is biased to produce a current  $I_5$ , where the current  $I_5$  is a **constant current**." *Id.*, 3:66-4:1 (emphasis added). In context, a POSITA would have understood that the constant current  $I_5$  is "substantially constant" in the sense meant by the '962 Patent. In a live circuit, a current designed to be constant will vary slightly due to temperature fluctuations, manufacturing imperfections, or other real-world complications. A POSITA would have understood that a "constant" current, in

practice, is designed to be constant, but may fluctuate slightly. Thus “constant” and “substantially constant” mean the same thing in a real-world circuit in this context.

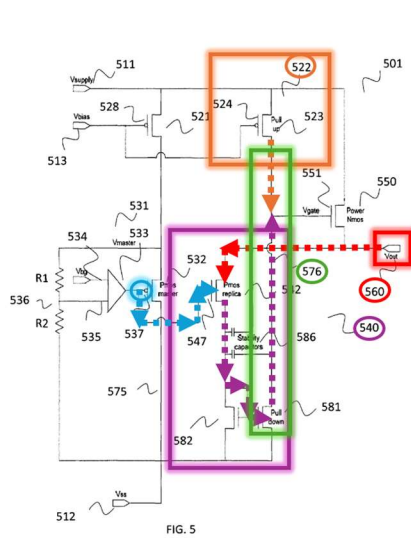
111. *Second*, Scott’s current source (orange) supplies its substantially constant current (orange arrow) to a second current path (green). Ex-1005, Fig. 1. Scott discloses that “the sum of the currents I2 and I3 is essentially equal to the constant current I5.” *Id.*, 4:1-4. Therefore, changes in the current I2 result in inverse changes in I3, such that the sum continues to equal I5. *Id.* In this way, Scott’s current source supplies a current to the second current path, because the magnitude of I2 directly impacts the magnitude of I3, which is in the second current path. *Id.*, 4:1-4, Fig. 1.

112. Moreover, the green box identified in Figure 1 (annotated above) is the claimed second current path. The ’962 Patent explains that the second current path is coupled to at least two elements: the first current supply circuit and the pass device. Ex-1001, 2:30-45. In addition to being coupled to a first current supply circuit, as explained above, the green box identified in Scott’s Fig. 1 (annotated above) is coupled to a pass device. *See infra*, § VIII.A.1.f. Thus, the identified element is the claimed second current path.

113. In summary, Scott’s current source (orange) supplies a substantially constant current (orange arrow) to a second current path (green). Thus, Scott discloses or teaches every limitation of Element 1[d].

- f. **Element 1[e]: a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit;**

114. Element 1[e] requires a “second current supply circuit” coupled to three components: (a) the first current supply circuit; (b) the gate of the feedback transistor; and (c) the output of the voltage regulator. Additionally, the “second current supply circuit” must supply a current to the second current path, where the magnitude of the current is based on two quantities: (a) the voltage at the gate of the feedback transistor; and (b) the voltage at the output of the voltage regulator. Scott’s voltage regulator includes an “output transistor” (18) (Ex-1005, 3:28-32, Fig. 1), which is the claimed “second current supply circuit.” A comparison of the ’962 Patent’s Figure 5, and Scott’s Figure 1 (both annotated below) shows this. As further explained below, Scott’s “output transistor” discloses every element of the second current supply circuit in the same way as the ’962 Patent.



'962 Patent, Fig. 5  
(annotated)

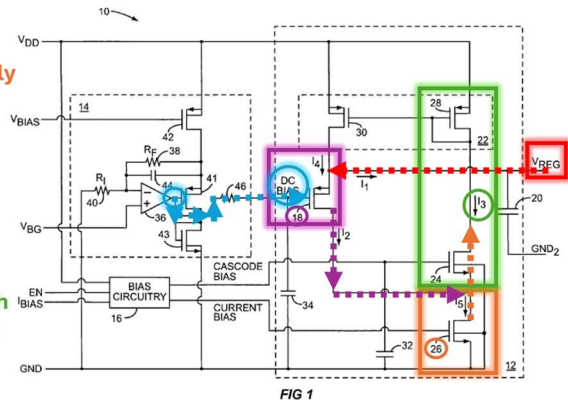
**Second Current Supply Circuit:**

1) Coupled to three elements:

- a) **First Current Supply Circuit**
- b) **Gate of Feedback Transistor**
- c) **Output of Voltage Regulator**

2) Supplies a **Current** to the **Second Current Path** based on two quantities:

- a) **Voltage at Gate of Feedback Transistor**
- b) **Voltage at Output of Voltage Regulator**



Scott, Fig. 1  
(annotated)

(1) **The output transistor is coupled to the three required elements.**

115. Scott's output transistor (second current supply circuit, purple) is coupled to the three required elements: (1) the first current supply circuit; (2) the gate of the feedback transistor; and (3) the output of the voltage regulator. Ex-1005, Fig. 1.

116. *First*, the output transistor's coupling to the first current supply circuit (orange) is illustrated by the current  $I_2$  (purple arrow). *Id.* "[T]he output transistor 18 draws a current  $I_2$  based on a DC bias [annotated in blue] and the charge stored across the reservoir capacitor 20, which corresponds to the regulated voltage ( $V_{REG}$ ) [annotated in red]." *Id.*, 3:47-51. The current  $I_2$  (purple arrow) connects the output transistor (purple) to the current source (orange). *Id.*, Fig. 1. They are connected in such a way that "the sum of the currents  $I_2$  and  $I_3$  is essentially equal to the constant

current  $I_5$ ,” which is the current produced by the current source. *Id.*, 3:66-4:4. The current source connected to the output transistor is the claimed “first current supply circuit.” *Supra*, § VIII.A.1.e.

117. *Second*, the output transistor’s coupling to the gate of the feedback transistor (blue) is illustrated in Figure 1 by the DC BIAS (blue arrow). Ex-1005, Fig. 1. Scott’s detailed description discloses that the output transistor is coupled to the DC BIAS. *See Id.*, 3:49-50 (“[T]he output transistor 18 draws a current  $I_2$  **based on a DC bias.**”); 4:67-5:2 (“The voltage bias circuitry 14 operates to generate the DC bias... and to **provide DC bias for the output transistor 18.**”); 5:33-35 (“[T]he matching transistor 41 in conjunction with the operational amplifier 36 **generates the DC bias voltage for the output transistor 18.**”) (all emphases added). Figure 1 illustrates that the output transistor receives the DC BIAS from the gate of the matching transistor (41). *Id.*, Fig. 1; *see also id.*, 5:33-35 (“[T]he matching transistor 41 in conjunction with the operational amplifier 36 generates the DC bias voltage for the output transistor 18.”). The matching transistor (41) is the claimed “feedback transistor.” *Supra*, § VIII.A.1.d. Thus, Scott’s output transistor is coupled to the claimed “feedback transistor.”

118. *Third*, the output transistor’s coupling to the output of the voltage regulator (red) is illustrated in Figure 1 by the current  $I_1$  (red arrow). Ex-1005, Fig. 1. Scott’s detailed description discloses that the output transistor is coupled to  $V_{REG}$ .

*See Id.*, 3:49-51 (“[T]he output transistor 18 draws a current  $I_2$  based on a DC bias and **the charge stored across the reservoir capacitor 20, which corresponds to the regulated voltage ( $V_{REG}$ ).**”); 4:41-44 (“The dip in the regulated voltage ( $V_{REG}$ ) causes an **instantaneous reduction in the current  $I_2$  proportional to the transconductance ( $g_m$ ) of the output transistor 18.**”).  $V_{REG}$  is the output of the voltage regulator, because the “load (not shown) [is] connected to the regulated voltage  $V_{REG}$ .” *Id.*, 4: 38-41; *see also supra*, § VIII.A.1.c.

119. Thus, Scott’s output transistor is coupled to the three elements required of the second current supply circuit.

**(2) The output transistor supplies a current to the second current path based on the required voltages.**

120. Scott’s output transistor (purple) supplies a current (purple arrow) based on the two required quantities: (1) the voltage at the gate of the feedback transistor (blue arrow); and (2) the voltage at the output of the voltage regulator (red arrow). Ex-1005, Fig. 1.

121. *First*, the DC BIAS voltage is provided to the output transistor from the gate of the matching transistor. *Id.*, Fig. 1, 5:33-35 (“[T]he matching transistor 41 in conjunction with the operational amplifier 36 generates the DC bias voltage for the output transistor 18.”). The matching transistor (41) is the claimed “feedback transistor.” *Supra*, § VIII.A.1.d. “The matching of the transistor 41 to the output

transistor 18 produces a DC bias output such that the  $V_{GS}$  of the output transistor 18 will add to the DC bias voltage to replicate the desired regulator output voltage ( $V_{REG}$ ).” Ex-1005, 5:18-21. Thus, the current provided by the output transistor is based in part on the DC BIAS, which is supplied by the voltage at the gate of the feedback transistor.

122. *Second*, the voltage at the output of the voltage regulator ( $V_{REG}$ ) is coupled to the output transistor (red arrow showing coupling). Ex-1005, Fig. 1; *see also supra*, § VIII.A.1.f.(1). Scott’s detailed description discloses that changes in  $V_{REG}$  impact the current I2 (purple arrow) provided by the output transistor. *Id.*, Fig. 1, 4:41-44 (“The dip in the regulated voltage ( $V_{REG}$ ) causes an instantaneous reduction in the current I2 proportional to the transconductance (gm) of the output transistor 18.”). Thus, the current provided by the output transistor is based in part on the output of the voltage regulator.

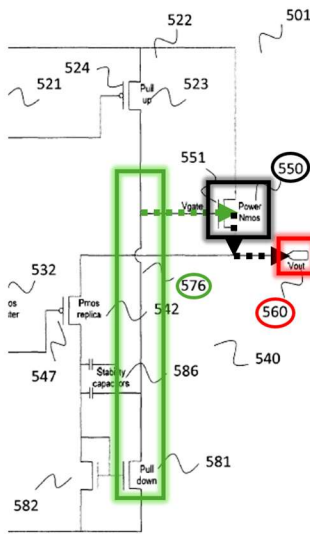
123. The current I2 (purple arrow) supplied by the output transistor is supplied to the second current path (green). Ex-1005, Fig. 1. The current I3 is in the second current path. *Id.* The currents I2 and I3 are connected “such that the sum of the currents I2 and I3 is essentially equal to the constant current I5.” *Id.*, 4:2-4. In other words, a reduction in the current I2 causes an increase in the current I3, and vice versa. *Id.*, 4:1-13. Thus, the output transistor supplies a current to the second current path. Note that the inverse arrangement—where a decrease in the voltage

supplied by the second current supply circuit causes an increase in the current of the second current path—is the same as the one disclosed in the '962 Patent. *See* Ex-1001, 9:64-10:9.

124. In summary, Scott's output transistor is the disclosed "second current supply circuit," because it is coupled to the three required elements, and supplies a current to the second current path based on the two required voltages. Thus, Scott discloses or teaches every limitation of Element 1[e].

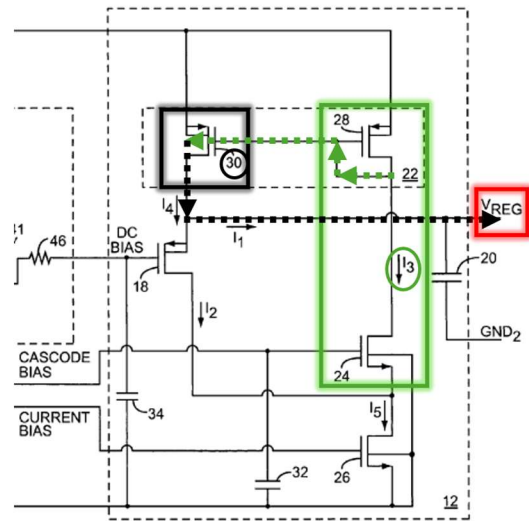
- g. Element 1[f]: a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;**

125. Element 1[f] requires a pass device with a gate coupled to the second current path, that receives a signal based on the current of the second current path. Additionally, the pass device must provide a load current to the load via the output of the voltage regulator based on the signal it receives from the second current path. Scott's voltage regulator includes a transistor (30) that provides a current I<sub>4</sub> (Ex-1005, Fig. 1, 3:52-55), which is the claimed pass device. A comparison of the '962 Patent's Figure 5 and Scott's Figure 1 (both annotated below) shows this. Scott's transistor (30) discloses every limitation of the claimed "pass device" in the same way as the '962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)

- Pass Device :**
- 1) Includes a **Gate** that receives a signal from **Second Current Path**
  - 2) Supplies a **Load Current** to the load via the **Voltage Regulator Output**



Scott, Fig. 1  
(annotated excerpt)

126. Scott's Figure 1 (annotated above) illustrates that the transistor 30 (black) is coupled to the second current path (green arrow showing coupling). Ex-1005, Fig. 1. Moreover, Scott's description discloses that the transistor 30 receives a signal based on the current of  $I_3$  in the second current path. *Id.*, 3:52-58. Specifically, Scott discloses that the transistor 28 "sinks a current  $I_3$ " from the second current path, enabling the transistor 30 to provide a current  $I_4$ , "where the current  $I_4$  is defined as the current  $I_3$  multiplied by a current mirror gain ratio." Thus, Scott's transistor 30 includes a gate coupled to the second current path, and receives a signal based on the current of the second current path.

127. Scott's transistor 30 also supplies a load current  $I_4$  (black arrow) to the load via the output of the voltage regulator circuit ( $V_{REG}$ , red) based on the signal it receives. The current  $I_4$  is based on the signal the transistor 30 receives from the

second current source I3 because “[i]n response to the increase in the current I3, the current mirror 22 operates to increase the current I4.” *Id.*, 4:4-5; *see also* 4:11-13 (decreases in I3 cause decreases in I4). The current I4 is also supplied to the load via the output of the voltage regulator  $V_{REG}$  via that current’s impact on the current I1. *See id.*, 4:8-11 (“By increasing the current I4, the current I4 becomes larger than the current I2. Accordingly, the current I1 increases and is essentially equal to  $I4 - I2$ .”). The current I1 directly provides charge to the reservoir capacitor. *Id.*, 4:10-11. The output of the voltage regulator circuit draws its charge from the reservoir capacitor. *See id.*, 3:62-63 (“When charge is drawn from the reservoir capacitor 20, there is a dip in the regulated voltage ( $V_{REG}$ ).”); *see also id.*, 3:28-32 (“The output transistor 18 provides a regulated voltage ( $V_{REG}$ ) across the reservoir capacitor 20.”). Thus, Scott’s transistor 30 supplies a load current to the load via the output of the voltage regulator with a magnitude based on the signal it receives from the second current path.

128. To the extent Patent Owner argues that the load current must be provided directly to the load from the pass device, the claim language does not require that. Ex-1001, Cl. 1 (“a pass device... adapted to... supply a load current to said load.”). Moreover, the annotated comparison above shows that the ’962 Patent’s pass device provides a load current (black arrow) indirectly in a way similar to Scott. *Compare* Ex-1001, Fig. 5; *with* Ex-1005, Fig. 1.

129. In summary, Scott's transistor 30 is the claimed pass device, because its gate is coupled to the second current path and receives a signal based on the current of that path, and supplies a load current to the load via the output of the voltage regulator based on the signal the transistor 30 receives at its gate. Therefore, Scott discloses or teaches every limitation of Element 1[f].

- h. Element 1[g]: wherein said second current supply circuit is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases; and**

130. Element 1[g] requires the second current supply circuit to be adapted to, via the pass device, cause an increase in the magnitude of the load current supplied to the output when the output voltage decreases, and vice versa. Scott's voltage regulator does this in essentially the same way as the '962 Patent. As discussed above, Scott's output transistor is the claimed second current supply circuit, and operates in conjunction with the pass device to perform the claimed voltage regulation. *Supra*, §§ VIII.A.1.f-g. Specifically, Scott discloses that when "a dip occurs in the regulated output voltage... the high-speed feedback loop operates to rapidly increase the charging current." Ex-1005, 1:55-63. To do so, the output transistor (the claimed "second current supply circuit") reduces the current I<sub>2</sub>, causing an increase in the current I<sub>3</sub>, which causes the pass device to increase the

output currents I4 and I1. *Id.*, 3:62-4:11. Similarly, when the regulated output voltage increases, the output transistor increases the current I2, causing the pass device to decrease the output currents I4 and I1. *Id.*, 4:11-13.

131. Therefore, Scott discloses or teaches every limitation of Element 1[g].

- i. **Element 1[h]: wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit.**

132. Element 1[h] requires the feedback circuit, first current supply circuit, second current supply circuit, and pass device to be integrated in an integrated circuit. As discussed above, these elements of Scott are integrated in an integrated circuit. *Supra*, § VIII.A.1.a; *see also* Figs. 1, 2. Additionally, Element 1[h] requires the elements to be referenced to the input of the voltage regulator circuit. As discussed above, the elements are referenced to  $V_{DD}$ , the input of the voltage regulator circuit. *Supra*, § VIII.A.1.b; *see also* Figs. 1, 2.

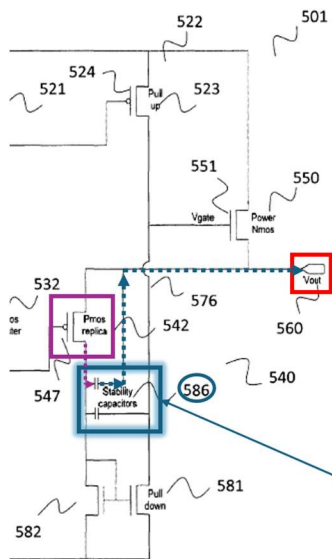
133. Therefore, Scott discloses or teaches every limitation of Element 1[h].

134. Thus, Scott renders Claim 1 obvious.

- 2. **Claim 7: The voltage regulator circuit of claim 1, wherein said second current supply circuit further comprises at least one stability capacitor arrangement.**

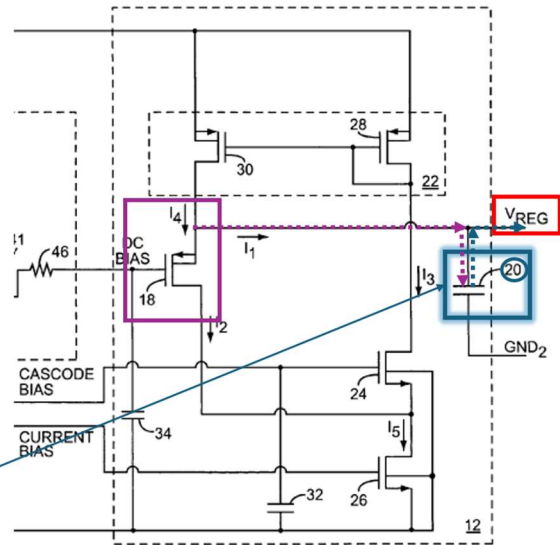
135. Scott's voltage regulator includes a reservoir capacitor (Ex-1005, 3:28-32) which is the claimed "stability capacitor arrangement." A comparison of the '962

Patent's Figure 5 and Scott's Figure 1 (both annotated below) shows this. As further explained below, Scott's reservoir capacitor is a stability capacitor arrangement that is connected to the same elements and operates in the same way as at least one of the '962 Patent's stability capacitor arrangements.



'962 Patent, Fig. 5  
(annotated excerpt)

**Stability Capacitor  
Arrangement**



Scott, Fig. 1  
(annotated excerpt)

136. Scott's reservoir capacitor (blue) is at least one "stability capacitor arrangement." Ex-1005, 3:28-38. For example, Scott discloses that "charge is stored in the reservoir capacitor 20... such that the regulated voltage ( $V_{REG}$ ) remains substantially constant as the load is varied." *Id.*, 3:36-38. Because the reservoir capacitor ensures the regulated voltage remains substantially constant, it is a "stability capacitor arrangement." *Id.*; see also *id.*, 1:53-55 ("The charge stored by the reservoir capacitor corresponds to a regulated voltage provided by the voltage

regulator.”) The ’962 Patent explains the operation of its “stability capacitor arrangement” in the same way—the stability capacitor arrangement stores charge so as to ensure quick responses to changes in output voltage levels. Ex-1001, 9:44-49.

137. Scott’s “stability capacitor arrangement” is also arranged in the same way as at least one of the ’962 Patent’s, as the annotated figures above show. *Compare* Ex-1001, Fig. 5; *with* Ex-1005, Fig. 1. In both patents, the stability capacitor is coupled to a replica transistor that comprises the second current supply circuit. *Id.* And both are connected to the output of the voltage regulator to provide current quickly based on changes in the output voltage. *Compare* Ex-1001, 9:44-49, Fig. 1; *with* Ex-1005, 3:35-38, Fig. 5.

138. To the extent Patent Owner argues that the “stability capacitor arrangement” requires multiple capacitors, with one placed in the circuit before and one after the pass device, the claim does not expressly require that. *See* Ex-1001, Cl. 7. The placement of the stability capacitor is immaterial. A POSITA would have understood that the stability capacitor arrangement could perform its function whether placed after or before and after the pass device. The fact that the stability capacitors of both Scott and the ’962 Patent perform the same function underscores this fact. *Compare* Ex-1001, 9:44-49 (“stability capacitor arrangement... is constructed to store charge so as to ensure... response to changes in output voltage

levels”); *with* Ex-1005, 3:35-38 (“charge is stored in the reservoir capacitor... such that the regulated voltage ( $V_{\text{REG}}$ ) remains substantially constant”).

139. Thus, Scott renders Claim 7 obvious.

**3. Claim 8: The voltage regulator circuit of claim 7, wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads.**

140. Scott’s reservoir capacitor (20) is the claimed stability capacitor arrangement. *Supra*, § VIII.A.2. Scott discloses that “in one embodiment, the **reservoir capacitor 20 is a 10 pF capacitor.**” Ex-1005, 4:31-32 (emphasis added). The size of the reservoir capacitor is important to the invention of Scott, because it enables the voltage regulator to restore the desired regulated voltage quickly. *Id.*, 4:27-33. Since 10 pico-farads is less than 30 pico-farads, Scott’s reservoir capacitor has the required capacitance.

141. Therefore, Scott renders Claim 8 obvious.

**4. Claim 9: The voltage regulator of claim 1, wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path.**

142. Claim 9 requires the magnitude of the load current to be at least one order magnitude greater than the second current path. Scott discloses or teaches this limitation through its current mirror gain ratio (M). Ex-1005, 3:52-58.

143. As discussed above, the current  $I_3$  is the current of Scott’s second current path, and the current  $I_4$  is Scott’s load current. *Supra*, §§ VIII.A.1.d-f. Scott

discloses a current mirror, where one transistor sinks the current  $I_3$  and another provides a current  $I_4$ . Ex-1005, 3:52-54. “[T]he current  $I_4$  is defined as the current  $I_3$  multiplied by a current mirror gain ratio (M).” *Id.*, 3:54-55. *Id.*, 3:55-58. Scott provides an example in which the current of  $I_3$  is 300  $\mu\text{A}$ , and M is 1.5, the current  $I_4$  is equal 450  $\mu\text{A}$  ( $300 \mu\text{A} \times 1.5 = 450 \mu\text{A}$ ). *Id.*, 4:45-48.

144. Scott states that the “current mirror gain ratio (M) may be any number greater than zero.” *Id.*, 3:55-58. Thus, if the current mirror gain ratio is 10 or greater, then  $I_4$  is at least one order of magnitude greater than  $I_3$ . For example, if  $I_3$  is 100  $\mu\text{A}$ , and M is 10, then  $I_4$  is 1000  $\mu\text{A}$ , or 1 mA ( $100 \mu\text{A} \times 10 = 1000 \mu\text{A} = 1 \text{ mA}$ ). 1000  $\mu\text{A}$ , or 1 mA, is an order of magnitude greater than 100  $\mu\text{A}$ . Therefore, Scott discloses or renders obvious that  $I_4$  (Scott’s “load current”) is at least one order of magnitude greater than the magnitude of the current of  $I_3$  (in Scott’s “second current path”).

145. Thus, Scott discloses or teaches Claim 9.

**5. Claim 10: The voltage regulator of claim 1, wherein said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp.**

146. Claim 10 requires the load current to have a magnitude of less than one amp, and the current of the second current path to have a magnitude of less than one

milli-amp. Scott expressly discloses an example that meets these requirements. Ex-1005, 4:34-56.

147. As discussed above, the current I3 is the current of Scott's second current path, and the current I4 is Scott's load current. *Supra*, §§ VIII.A.1.d-f. Scott discloses one example wherein the current I3 (the claimed "second current path" current) ranges from 200  $\mu$ A (0.2 milli-amps) to 300  $\mu$ A (0.3 milli-amps), so it is less than one milli-amp. Ex-1005, 4:34-56. In the same example, the current I4 (the claimed "load current") ranges from 300  $\mu$ A (0.00030 amps) to 450  $\mu$ A (0.00045 amps), so it is less than one amp. *Id.* Thus, Scott discloses this limitation.

148. Thus, Scott renders claim 10 obvious.

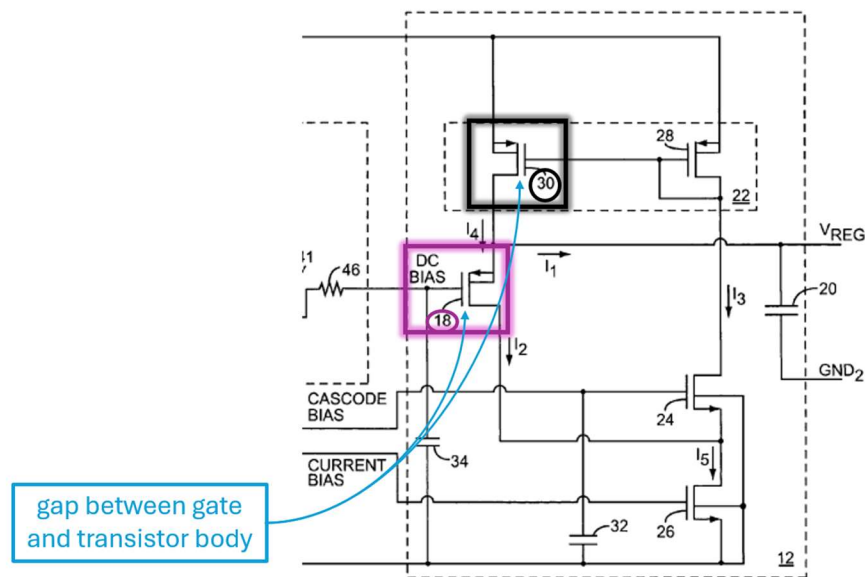
**6. Claim 11: The voltage regulator of claim 1, wherein said signal received at said pass device gate is a voltage.**

149. Claim 11 requires the signal received at the pass device to be a voltage. As discussed above, Scott's transistor 30 is the claimed pass device. *Supra*, § VIII.A.1.g. Scott's transistor 30 receives a voltage at its gate, so it meets the requirement of Claim 11. Ex-1005, Fig. 1.

150. There are two main types of transistors used in integrated circuit design—MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors) and BJTs (Bipolar Junction Transistors). MOSFETs are voltage controlled, meaning they receive a voltage at their gate, while BJTs are current controlled. The three

terminals of a MOSFET are referred to as the gate, source, and drain. The three terminals of a BJT are referred to as the emitter, base, and collector. In circuit diagrams, the gate of the MOSFET is separated from the body by a small gap, while in a BJT the gate is shown as directly connected to the main body of the transistor.

151. Scott's transistor 30 is a MOSFET. Ex-1005, Fig. 1. Figure 1 (annotated below) shows that transistor 30 (black) has a gate physically separated from the body.



Scott, Fig. 1  
(annotated excerpt)

This physical separation means the transistor is a MOSFET. Moreover, the “output transistor” (purple) also has a gap between its gate and body. Ex-1005, Fig. 1. Scott expressly calls two of the terminals of the output transistor a “gate” and a “source.” Ex-1005, 3:63-65 (“The instantaneous effect of this voltage dip is to reduce a voltage

from the **gate** to the **source** of the output transistor 18.”) (emphasis added). This further shows that the transistor 30 is a MOSFET, because only MOSFETs have terminals called a “gate” and “source,” and the output transistor 18 is drawn to be the same as transistor 30. *Id.*, Fig. 1.

152. Because MOSFETs receive a voltage at their gates, and the transistor 30 is a MOSFET, the transistor 30 receives a voltage at its gate. Ex-1001, Fig. 1. Thus, Scott renders Claim 11 obvious.

## 7. Claim 14

- a. **Element 14[pre]: A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions, comprising:**

153. To the extent the preamble is limiting, Scott discloses most of the preamble for the same reasons as Element 1[pre]. *Supra*, § VIII.A.1.a.

154. Scott also discloses the remainder of the preamble, which requires that the load is “integrated in the IC” and operates under “selectively variable load conditions.” Scott discloses a load, transistor 30, connected to  $V_{REG}$  that is integrated in the IC and connected to the external load of the voltage regulator. Scott discloses selectively variable load conditions because it discloses that a voltage regulator provides a regulated voltage “as **load current** and supply voltage change.” *Id.*, 1:14-16 (emphasis added). A POSITA would have understood that one reason a load

current varies is because the load circuitry connected to the output of the voltage regulator,  $V_{\text{REG}}$ , varies.

155. Thus, Scott discloses or teaches Element 14[pre].

**b. Element 14[a]: an input adapted to receive a voltage from said power supply;**

156. Scott discloses Element 14[a] for the same reasons as Element 1[a], which is identical. *Supra*, § VIII.A.1.b.

**c. Element 14[b]: an output adapted to be coupled to said load;**

157. Scott discloses Element 14[b] for the same reasons as Element 1[b], which is identical. *Supra*, § VIII.A.1.c.

**d. Element 14[c]: a first current path referenced to said input;**

158. Scott discloses Element 14[c] for the same reasons as Element 1[c], which explains how the “first current path” is coupled to the input. *Supra*, § VIII.A.1.d.

**e. Element 14[d]: feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;**

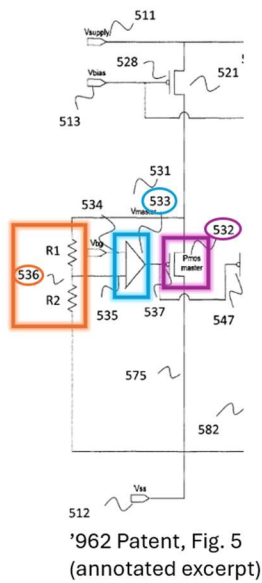
159. In the related district court litigation, the parties agreed that 35 U.S.C. § 112, ¶6 applies to Element 14[d], and agreed on the function. *See* Ex-1008 (Joint Claim Construction Statement), 4. The Court has construed the term’s structure in its claim construction order. *See* Ex-1009 (Claim Construction Order), 64. The

Court's construction including a representative structure disclosed by the prior art, applied herein, is provided below.

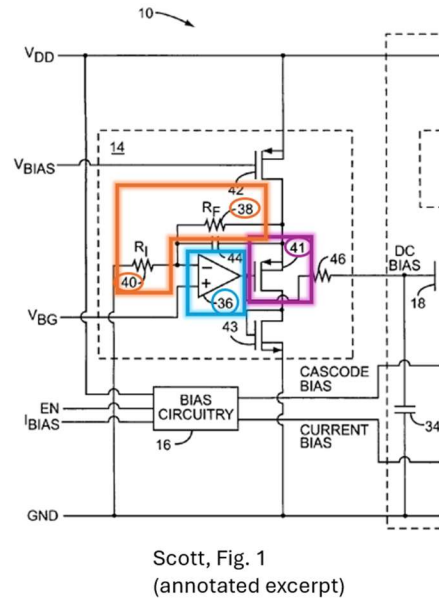
| Term                                                                                                                       | District Court's Construction                                                                                                                                                                                                                                                                                                   |
|----------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| "feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant" '962 Patent, Claim 14 | 35 U.S.C. § 112, ¶6 applies.<br><br><b>Function:</b> maintaining a voltage at a gate of a feedback transistor substantially constant<br><br><b>Representative Structure:</b> feedback circuit arranged as shown in Figure 5, element 531 including differential amplifier 533, voltage divider 536, and feedback transistor 532 |

160. Scott discloses the identified function for the reasons discussed in Element 1[c], which shows how Scott discloses "a feedback circuit... constructed to maintain a voltage at a gate of a feedback transistor substantially constant." *Supra*, § VIII.A.1.d.

161. The structure requires a feedback circuit including three elements: (1) a differential amplifier; (2) a voltage divider; and (3) a "feedback transistor." Scott's "voltage bias circuitry" has each of these elements arranged in the same way as in the '962 Patent, as shown by the comparison of the '962 Patent's Figure 5 and Scott's Figure 1, both annotated below.



- Feedback Circuit including:**
- 1) **Differential Amplifier**
  - 2) **Voltage Divider**
  - 3) **Feedback Transistor**



See also Ex-1005, 5:2-5 (“The illustrated embodiment of the voltage bias circuitry 14 includes an operational amplifier 36, a feedback resistor 38, an input resistor 40, [and] an output matching transistor 41.”)

162. First, Scott discloses the required differential amplifier. Scott’s voltage bias circuitry includes an operational amplifier (blue). Ex-1005, 5:2-5, Fig. 1. A POSITA would have understood that an operational amplifier is a component that includes a differential amplifier, in addition to other internal components. An operational amplifier includes a differential amplifier as its input stage to compare the voltages at the two input terminals. The “+” and “-” on the input of the op-amp symbol 36 in Scott are used to denote that the input is connected to a differential amplifier that takes the difference of the voltages on these two inputs. It further includes other components that may amplify and/or buffer the result of the

comparison before output such as an amplifier and buffer for driving heavy loads that follows the differential amplifier. Moreover, Scott's operational amplifier is arranged in the same way as the '962 Patent's differential amplifier. *Compare* Ex-1001, Fig. 5; *with* Ex-1005, Fig. 1. Both Scott and the '962 include two identical inputs—a bandgap voltage and a “feedback” voltage—and output a substantially constant voltage at a gate of a transistor. *Compare* Ex-1001, 8:48-56, Fig.5; *with* Ex-1005, 5:2-21, Fig. 1.

163. *Second*, Scott discloses the required voltage divider. Scott discloses a “feedback resistor” and an “input resistor” (orange), that operate in conjunction to provide one of the inputs to the operational amplifier (blue). Ex-1005, 5:2-14, Fig. 1. A POSITA would have understood that these resistors act together as a voltage divider, because a voltage divider consists of two resistors in series that are connected across a voltage source. A voltage divider produces an output that is a fraction of its input voltage. The '962 Patent's voltage divider has the same arrangement as Scott's. Ex-1001, 8:50-56, Fig. 5.

164. *Third*, Scott discloses the required “feedback transistor.” Scott discloses a “matching output transistor” (purple) which is the required “feedback transistor.” Ex-1005, 5:2-5, Fig. 1. The output of the operational amplifier (blue) is coupled to the gate of the matching output transistor (purple), and that gate voltage is also coupled to an “output transistor.” Ex-1005, 5:14-18, Fig. 1. The '962 Patent's

“feedback transistor” is arranged in the same way. Ex-1001, 8:57-60, 9:13-15, Fig.

5.

165. Thus, Scott discloses the same structure as the '962 Patent, or equivalents thereof, and therefore discloses or teaches Element 14[d].

**f. Element 14[e]: first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;**

166. In the related district court litigation, the parties agreed that 35 U.S.C. § 112, ¶6 applies to Element 14[e], and agreed on the function. *See* Ex-1008 (Joint Claim Construction Statement), 5-6. The District Court’s construction identified the relevant structure, as shown below. Ex-1009, 65.

| Term                                                                                                                                                              | District Court’s Construction                                                                                                                                                                                                                                                                             |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant” ’962 Patent, Claim 14 | 35 U.S.C. § 112, ¶6 applies.<br><br><b>Function:</b> supplying to a second current path referenced to said input a first current that is substantially constant<br><br><b>Representative Structure:</b> first current source 622 of Fig. 6, and equivalents, as described and shown at 10:63-11:3, Fig. 6 |

167. Scott discloses the identified function for the reasons discussed in Element 1[d], which shows how Scott discloses “a first current supply circuit constructed to supply to a second current path a first current that is substantially constant.” *Supra*, § VIII.A.1.e.

168. The representative structure is the first current source 622, which is a transistor that (1) has a bias voltage applied at its gate; and (2) supplies a constant current to the second current path. *See* Ex-1001, 10:63-67 (“[F]irst current source 622 operates to supply a consistent level of pull down current to second current path 676. In the embodiment shown, a bias voltage is applied to gate 671 of transistor 672, which functions to supply a constant current dependent on the bias voltage.”). Scott’s current source (26) is the claimed first current supply means. The current source is a transistor with a bias voltage applied at its gate, and it supplies a constant current to the second current path. *See* Ex-1005, 3:66-4:1 (“The current sources [sic] 26 is biased to produce a current  $I_5$ , where the current  $I_5$  is a constant current.”); *see also* Fig. 1.

169. Thus, Scott discloses the same structure as the ’962 Patent, or equivalents thereof, and therefore discloses or teaches Element 14[e].

- g. Element 14[f]: second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;**

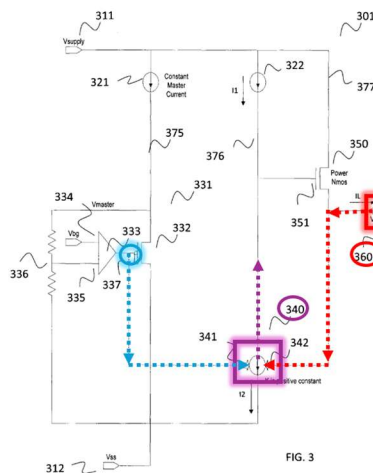
170. In the related district court litigation, the parties agreed that 35 U.S.C. § 112, ¶6 applies to Element 14[f], and agreed on the function. *See* Ex-1008 (Joint

Claim Construction Statement), 6. The District Court’s construction identified the relevant structure, as shown below. Ex-1009, 66.

| Term                                                                                                                                                                                                                                                                                  | District Court’s Construction                                                                                                                                                                                                                                                                                                                                                                                                  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| “second current supply means... for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference” ’962 Patent, Claim 14 | <p>35 U.S.C. § 112, ¶6 applies.</p> <p><b>Function:</b> receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference</p> <p><b>Representative Structure:</b> second current source 340 of Fig. 3, and equivalents, as described and shown at 6:42-62, Fig. 3</p> |

171. Scott discloses the identified function and the required couplings for the reasons discussed in Element 1[e], which explains how Scott discloses “a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit.” *Supra*, § VIII.A.1.f. The required voltage references in the agreed function are supplied by the gate of the feedback transistor and the output of the voltage regulator. *Id.*

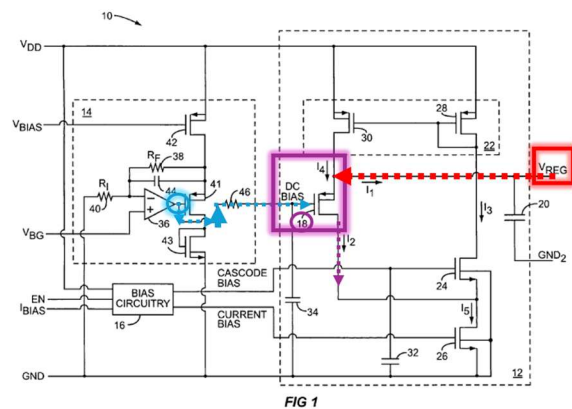
172. The representative structure is the second current source 340, which is “a variable current source adapted to supply a current to second current path” based on two reference signals. Ex-1001, 6:42-48. The first reference signal is based on a voltage at the gate of the feedback transistor, and the second is based on the voltage at the output node. *Id.* A comparison of the '962 Patent's Figure 3 and Scott's Figure 1 (both annotated below) shows that Scott's voltage regulator has all of these elements, arranged in the same way as the '962 Patent.



'962 Patent, Fig. 3  
(annotated)

Variable Current  
Source with 2  
reference signals:

- 1) Gate of the feedback transistor
- 2) Output of voltage regulator



Scott, Fig. 1  
(annotated)

173. As illustrated above, Scott's output transistor (purple) is the claimed second current source. Ex-1005, 3:47-51, 5:18-21, Fig. 1. It is a variable current source because it “draws a current  $I_2$ .” *Id.*, 3:49-51. As discussed with reference to Element 1[e], the current  $I_2$  is a variable current that is supplied to the second current path. *Supra*, § VIII.A.1.f. Moreover, the current supplied by Scott's output transistor

is based on the two required reference signals. Ex-1005, 3:47-51 (“[T]he output transistor 18 draws a current  $I_2$  based on a DC bias and the charge stored across the reservoir capacitor 20, which corresponds to the regulated voltage ( $V_{REG}$ ).”). First, the DC BIAS voltage is based on the voltage at the gate of the “feedback transistor” (blue), to which it is coupled. Ex-1005, 5:18-21 (“The matching of the transistor 41 to the output transistor 18 produces a DC bias output.”), Fig. 1. Second, the output transistor is also coupled to the output of the voltage regulator (red), and its current is based on that voltage as well. *Id.*, 3:47-51, Fig. 1. The ’962 Patent’s “second current supply means” is arranged in the same way. *See* Ex-1001, 9:13-17, Fig. 5.

174. Thus, Scott discloses or teaches Element 14[f].

- h. Element 14[g]: means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;**

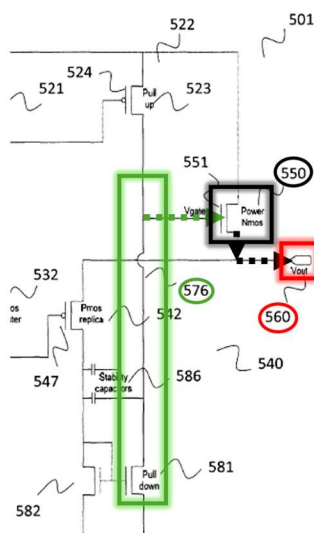
175. The parties agree that 35 U.S.C. § 112, ¶6 applies to Element 14[g], and further agree on the function and structure for the claim term. *See* Ex-1008 (Joint Claim Construction Statement), 2-3. The agreed function and a representative identification of the agreed structure is provided below.

| Term                                                                      | Agreed Construction                                                                 |
|---------------------------------------------------------------------------|-------------------------------------------------------------------------------------|
| “means for supplying current to said load for receiving a signal based on | 35 U.S.C. § 112, ¶6 applies.<br><b>Function:</b> supplying current to said load for |

|                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                    |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal” ’962 Patent, Claim 14 | receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal<br><br><b>Representative Structure:</b> pass transistor 550 of Fig. 5, as described and shown at 7:27-51 |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

176. Scott discloses the agreed function for the same reasons as Element 1[f], which shows how Scott discloses “a pass device... adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal.” *Supra*, § VIII.A.1.g.

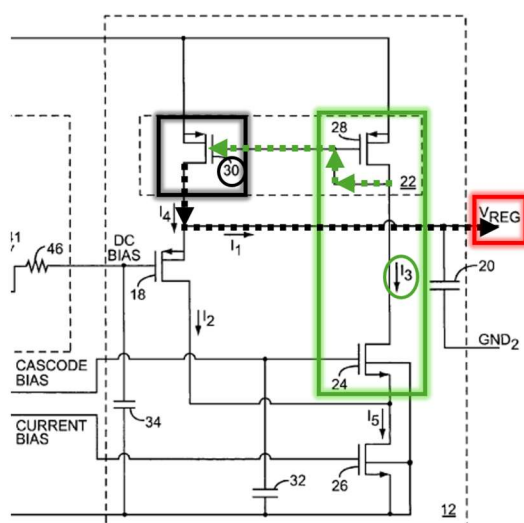
177. The agreed structure requires a “pass transistor” that receives a signal at its gate based on the magnitude of the second current path. *See* Ex-1001, 7:27-30. Further, the transistor “may be adapted to supply, to a load coupled to output 460, a load current with a magnitude based on the signal received at pass transistor gate.” *Id.*, 7:32-35. A comparison of the ’962 Patent’s Figure 5 and Scott’s Figure 1 (both annotated below) shows that Scott discloses these elements with the same arrangement as the ’962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)

**Pass Device :**

- 1) Includes a **Gate** that receives a signal from **Second Current Path**
- 2) Supplies a **Load Current** to the load via the **Voltage Regulator Output**



Scott, Fig. 1  
(annotated excerpt)

178. Scott discloses a transistor (black) that receives a signal at its gate from the current I3 (green), which is part of Scott's "second current path." Ex-1005, 3:52-58, Fig. 1. The transistor (black) supplies a current I4 (black arrow), which is derived from the current I3 (green) received at the transistor's gate. *Id.* Thus, the transistor receives a signal at its gate based on the magnitude of the second current path. *Id.* Further, increases in the current I4 supplied by Scott's transistor (black) are reflected in the current I1 (black arrow), which is supplied to the regulated voltage output via the reservoir capacitor. *Id.*, 4:8-11. Thus, Scott's transistor supplies a load current with a magnitude based on the signal received at its gate. *Id.* The structure of the '962 Patent's supply means is arranged in the same way. *See* Ex-1001, 7:27-35, Fig. 5. To the extent that Scott's disclosed structure is not exactly the same as that disclosed in the '962 Patent, Scott performs the same function in substantially the

same way to achieve substantially the same result. A POSITA would have understood that, while there are many ways to physically arrange the components of an integrated circuit, many are functionally the same and result in virtually the same circuit. To the extent these structures are not identical, they are virtually the same and result in virtually the same circuit.

179. Thus, Scott discloses or teaches Element 14[g].

- i. **Element 14[h]: wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage said load increases, a magnitude of said load current is decreased; and**

180. Scott discloses Element 14[h] for the same reasons as Element 1[g].

*Supra*, § VIII.A.1.h.

- j. **Element 14[i]: wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit.**

181. Scott discloses Element 14[i] for the same reasons as Elements 1[pre] and 1[h]. *Supra*, §§ VIII.A.1.a, i.

182. Thus, Scott renders Claim 14 obvious.

**8. Claim 16**

- a. Element 16[pre]: A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:**

183. To the extent the preamble is limiting, Scott discloses the preamble. Scott discloses an integrated circuit for the same reasons discussed above. *Supra*, §§ VIII.A.1.a, h.

184. Scott also discloses the remainder of the preamble, which requires a method of regulating a supply voltage for selectively operable circuitry. Scott discloses a method of regulating a supply voltage because it claims, in part “[a] method for regulating an output voltage of a voltage regulator.” Ex-1005, Cl. 16. Scott discloses selectively operable load circuitry because it discloses that a voltage regulator provides a regulated voltage “as **load current** and supply voltage change.” *Id.*, 1:14-16 (emphasis added). A POSITA would have understood that one reason a load current varies is because the load circuitry is selectively operable. For example, a load consisting of a battery and charging circuitry shut off the charging current to the battery when the battery is charged which reduces the amount of current supplied by the regulator.

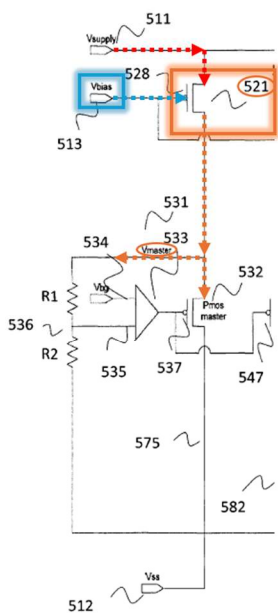
185. Thus, Scott discloses or teaches every limitation of Element 16[pre].

**b. Element 16[a]: receiving, from a power supply, a power supply voltage;**

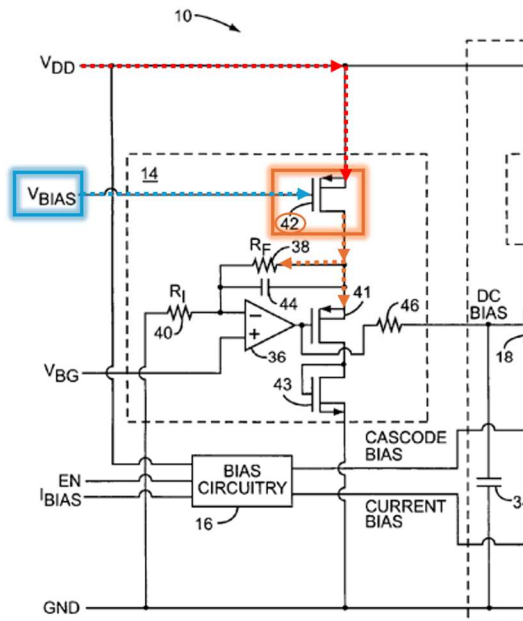
186. Scott discloses Element 16[a] for the same reasons as Element 1[a], which explains how Scott discloses the structure for receiving a power supply from a power supply voltage. *Supra*, § VIII.A.1.b. A POSITA would have understood that the structure disclosed in Scott needs a power supply voltage to power Scott's regulator. For example, when Scott discloses a structure for receiving a power supply voltage, a POSITA would have understood that the described circuit is meant to be used to regulate an output voltage from a power supply voltage that powers the regulator. *See* Cl. 16 (claiming "**a method** for regulating an output voltage of a voltage regulator") (emphasis added).

**c. Element 16[b]: supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current;**

187. Element 16[b] requires supplying a master current to a first current path integrated in the integrated circuit and referenced to the power supply voltage. A comparison of the '962 Patent's Figure 5 and Scott's Figure 1 (both annotated below) shows that Scott's current source transistor (42) (Ex-1005, 5:2-7) discloses this requirement in the same way as the '962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)



Scott, Fig. 1  
(annotated excerpt)

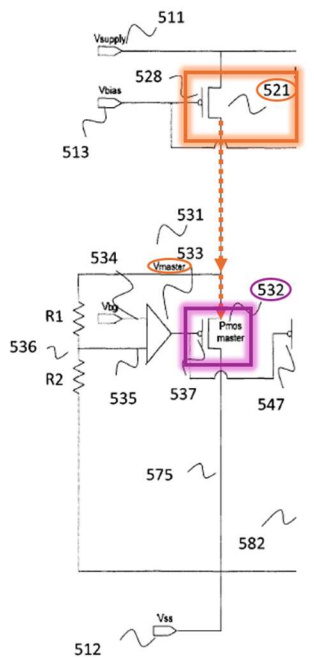
188. Scott's current source transistor (orange) supplies the claimed "master current" (orange arrow) from its drain. As discussed with reference to Element 1[b], the current path it is supplied to is part of the claimed "first current path." *Supra*, § VIII.A.1.c. The current source, also part of the claimed "first current path," is referenced to the power supply voltage (red arrow), as claimed. Ex-1005, Fig. 1. The master current supplied is based on a voltage bias (blue) supplied at its gate. *Id.* Moreover, every element of Scott's voltage regulator, including the first current path, is integrated in one integrated circuit. *Supra*, § VIII.A.1.a. A POSITA would have understood that current mirrors only function as current mirrors when implemented in an integrated circuit where the transistors are fabricated exactly the same.

189. The '962 Patent's "master transistor 521" (orange), described by this claim limitation, operates in the same way. Ex-1001, Fig. 5. It receives an input from the voltage supply (red arrow) at its source, and supplies a current (orange arrow) from its drain based on a bias voltage (blue) received at its gate. *Id.*, Fig. 5, 8:67-9:4.

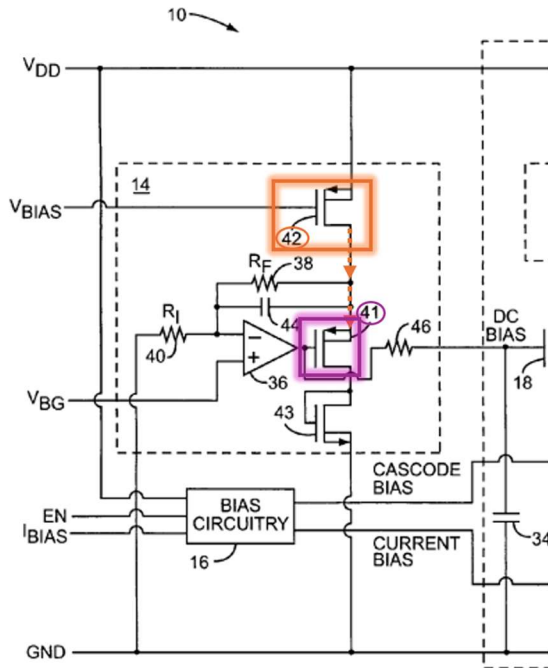
190. Thus, Scott discloses or teaches Element 16[b].

**d. Element 16[c]: receiving, at a feedback transistor integrated in said integrated circuit, said master current;**

191. Scott discloses receiving the master current at a feedback transistor. As described in reference to Element 1[c], Scott's output matching transistor (18) is the claimed "feedback transistor." *Supra*, §VIII.A.1.d. A comparison of the '962 Patent's Figure 5 and Scott's Figure 1 (both annotated below) shows that Scott discloses receiving the master current at its feedback transistor in the same way as the '962 Patent.



'962 Patent, Fig. 5  
(annotated excerpt)



Scott, Fig. 1  
(annotated excerpt)

192. As shown, Scott's current source (orange) supplies the master current (orange arrow) to its matching output transistor (purple), which is the claimed "feedback transistor." Ex-1005, Fig. 1; *see also id.*, 5:14-16 ("The matching output transistor 41... is biased by the current source 42."). Moreover, as the comparison above shows, the master current is supplied in the same way in the '962 Patent. Ex-1001, Fig. 1. Thus, Scott discloses the feedback transistor receiving the master current. Additionally, every element of Scott's voltage regulator, including the matching output transistor (the claimed "feedback transistor"), is integrated in one integrated circuit. *Supra*, § VIII.A.1.a.

193. Thus, Scott discloses or teaches Element 16[c].

- e. **Element 16[d]: maintaining, via a feedback circuit integrated in said integrated circuit and coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant;**

194. Scott discloses Element 16[d] for the same reasons as Element 1[c], which explains how Scott discloses how the structure of the feedback circuit is constructed to maintain a substantially constant voltage at the gate of the feedback transistor. *Supra*, § VIII.A.1.b. A POSITA would have understood that the specification and figures disclosed in Scott inherently determine how Scott's voltage regulator operates. For example, when Scott discloses structure designed to maintain a substantially constant voltage at the gate of the feedback transistor, a POSITA would have understood that the circuit is meant to be used in order to maintain a regulated, or fixed voltage as the amount of current supplied to a load changes. *See* Cl. 16 (claiming "**a method** for regulating an output voltage of a voltage regulator") (emphasis added). Moreover, every element of Scott's voltage regulator, including the voltage bias circuitry (the claimed "feedback circuit"), is integrated in one integrated circuit. *Supra*, § VIII.A.1.a.

195. Thus, Scott discloses or teaches Element 16[d].

- f. **Element 16[e]: supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude;**

196. Scott discloses most of Element 16[e] for the same reasons as Element 1[d], which explains how Scott discloses the “first current supply circuit” constructed to supply a constant current to a second current path. § VIII.A.1.e. A POSITA would have understood that the specification and figures disclosed in Scott teach how Scott’s voltage regulator operates. For example, when Scott discloses a supply circuit constructed to supply a constant current to a second current path, a POSITA would have understood that the circuit operates as described in Scott. *See* Cl. 16 (claiming “**a method** for regulating an output voltage of a voltage regulator”) (emphasis added).

197. Moreover, every element of Scott’s voltage regulator, including the identified “second current path,” is integrated in one integrated circuit. *Supra*, § VIII.A.1.a. The second current path is also coupled to a pass transistor, as described with reference to Element 1[f]. *Supra*, § VIII.A.1.g.

198. Thus, Scott discloses or teaches Element 16[e].

- g. Element 16[f]: supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load;**

199. Scott discloses Element 16[f] for the same reasons as Element 1[e], which explains how Scott discloses the “second current supply circuit” constructed to supply a variable current based on the voltage at the gate of the feedback transistor and the output of the voltage regulator to the second current path. *Supra*, § VIII.A.1.f. A POSITA would have understood that the specification and figures disclosed in Scott teach how Scott’s voltage regulator operates. For example, when Scott discloses a supply circuit that is designed to supply a variable current, a POSITA would have understood that the circuit is meant to be used to supply the current as described. *See* Cl. 16 (claiming “**a method** for regulating an output voltage of a voltage regulator”) (emphasis added).

200. Thus, Scott discloses or teaches Element 16[f].

- h. Element 16[g]: receiving, at a gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path; and**

201. Scott discloses Element 16[g] for the same reasons as Element 1[f], which explains how Scott discloses its “pass device” is constructed to receive a control signal based on the magnitude of a current of the second current path. *Supra*, § VIII.A.1.g. A POSITA would have understood that the specification and figures

disclosed in Scott teach how Scott's voltage regulator operates. For example, when Scott discloses a pass transistor designed to receive a control signal at its gate, a POSITA would have understood that the transistor is meant to be used to receive the control signal as described. *See* Cl. 16 (claiming “**a method** for regulating an output voltage of a voltage regulator”) (emphasis added). Moreover, every element of Scott's voltage regulator, including the transistor 30 (the claimed “pass device”) is integrated in one integrated circuit. *Supra*, § VIII.A.1.a.

202. Thus, Scott discloses or teaches Element 16[g].

- i. **Element 16[h]: supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.**

203. Scott discloses Element 16[h] for the same reasons as Elements 1[f]-[g]. *Supra*, §§ VIII.A.1.g-h. Element 1[f] explains how Scott discloses its “pass device” is constructed to supply a load current to the load based on the control signal received from the second current path. *Supra*, § VIII.A.1.g. Element 1[g] explains how Scott voltage regulator is constructed to increase the load current when a voltage at the load decreases and vice versa. *Supra*, § VIII.A.1.h. A POSITA would have understood that the specification and figures in Scott teach how Scott's voltage regulator operates. For example, when Scott describes a structure for supplying a

load current to a load, a POSITA would have understood that the circuit is meant to supply the load the current to the load as described. *See* Cl. 16 (claiming “**a method** for regulating an output voltage of a voltage regulator”) (emphasis added).

204. Thus, Scott discloses or teaches Element 16[h].

205. Therefore, Scott renders Claim 16 obvious.

## 9. Claim 17

- a. **Element 17[pre]: A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:**

206. To the extent the preamble is limiting, Scott discloses the preamble for the same reasons as Element 16[pre], which is identical. *Supra*, § VIII.A.8.a.

- b. **Element 17[a]: generating, at a first current path integrated in said integrated circuit, a substantially constant master current;**

207. Scott discloses Element 17[a] for the same reasons as Element 16[b]. *Supra*, § VIII.A.6.c. Element 16[b] requires “supplying” the master current to the first current path. *Id.* Scott’s current source transistor, which “supplies” the master current to the first current path, necessarily also “generates” the master current at the first current path, as described above. *Id.*

208. Thus, Scott discloses or teaches Element 17[a].

- c. Element 17[b]: supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current;**

209. Scott discloses Element 17[b] for the same reasons as Elements 1[d] and 16[e]. *Supra*, §§ VIII.A.1.e, VIII.A.8.f.

- d. Element 17[c]: supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load;**

210. Scott discloses most of Element 17[c] for the same reasons as Elements 1[e] and 16[g]. *Supra*, §§ VIII.A.1.f, VIII.A.8.g. Element 17[c] additionally requires that the second current source is integrated in the integrated circuit. Every element of Scott's voltage regulator, including the output transistor (the claimed "second current source") is integrated in one integrated circuit. *Supra*, § VIII.A.1.a.

211. Thus, Scott discloses or teaches Element 17[c].

- e. Element 17[d]: receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path;**

212. Scott discloses Element 17[d] for the same reasons as Elements 1[f] and 16[g]. *Supra*, §§ VIII.A.1.g, VIII.A.8.h.

- f. Element 17[e]: supplying, to said load circuitry via said pass transistor, a load current in response to said control signal; and**

213. Scott discloses Element 17[e] for the same reasons as Elements 1[f] and 16[h]. *Supra*, §§ VIII.A.1.g, VIII.A.8.i.

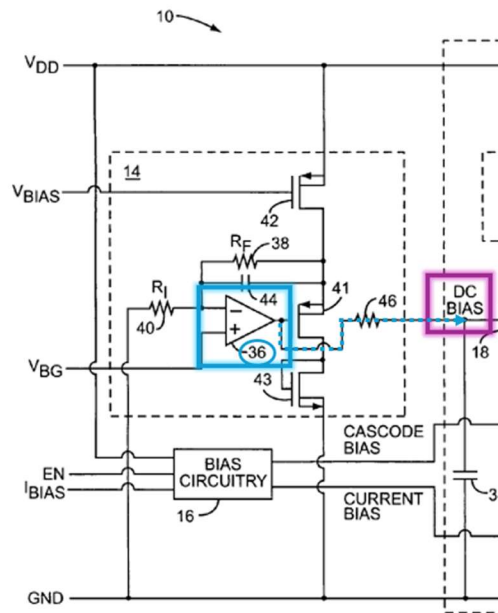
- g. Element 17[f]: wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current.**

214. Element 17[f] requires the magnitude of two currents, the first current and the second current, to be dependent “at least in part” on the magnitude of the claimed master current. As discussed with reference to Element 17[a], Scott’s voltage bias circuitry produces the claimed “master current” via its operational amplifier 36.

215. *First*, the magnitude of the first current is dependent on the magnitude of the master current. As discussed with reference to Element 1[d], the constant current I5 is the claimed first current. *Supra*, §§ VIII.A.1.e. The second current I2, which reflects changes in the regulated output voltage, is compared to the first current I5 to supply a current I3, which is a proportion of the current that is ultimately supplied to restore the regulated output voltage. *Supra*, §§ VIII.A.1.e-g; *see also* Ex-1005, 3:47-4:56. While the first current I5 does not directly take the master current as one of its inputs, it is “at least in part dependent” on the magnitude of that current because it must be set at a level where its comparison with I2 produces a voltage I3

that can restore the regulated output voltage  $V_{\text{REG}}$ . *See id.* The master current is set to reflect the same output voltage  $V_{\text{REG}}$ . Ex-1005, 5:8-11. If the first current were not “at least in part dependent” on the master current, the comparison of that current with  $I_2$  would not be meaningful, because it would not necessarily operate to cause the regulated output voltage to be restored. *See supra*, §§ VIII.A.1.e-g; *see also* Ex-1005, 3:47-4:56. To the extent Patent Owner argues that the first current must be directly set by the master current, that is not supported in the ’962 Patent. The first current source in the ’962 Patent supplies its current “based on a magnitude of the bias voltage at gate 528”—not the master current. Ex-1001, 8:61-9:8.

216. *Second*, the magnitude of the second current is based on the magnitude of the master current. As discussed with reference to Element 1[e], the magnitude of the second current is based in part on the magnitude of the DC BIAS voltage at the gate of the output transistor 18. *Supra*, § VIII.A.1.f.(2); *see also* Ex-1005, 3:62-66, 5:18-21. As shown in Figure 1 (annotated below), the master current (blue arrow) is supplied to where the DC BIAS (purple box) is generated.



Scott, Fig. 1  
(annotated excerpt)

Thus, the master current helps determine the magnitude of the DC BIAS voltage. Ex-1005, Fig. 1. Since the DC BIAS voltage helps determine the magnitude of the claimed “second current” (*Supra*, § VIII.A.1.f.(2)), the magnitude of the second current is based, in part, on the magnitude of the master current.

217. Both Scott's first and second current are dependent, at least in part, on the magnitude of the master current. Thus, Scott discloses or teaches Element 17[f].

218. Therefore, Scott renders Claim 17 obvious.

**10. Claim 18: The method of claim 17, wherein supplying said second current includes supplying a current based on a difference between a voltage at a gate of a feedback transistor of a feedback circuit and a voltage at said load circuitry.**

219. Claim 18 requires the second current to be based on a difference between the voltage at the gate of a feedback transistor and the voltage at the load

circuitry. As discussed with reference to Element 1[e], Scott's output transistor, which supplies the second current, has its source coupled to the load circuitry and its gate coupled to the gate of the feedback transistor. *Supra*, § VIII.A.1.f. The discussion of Element 1[e] also shows that the second current, supplied by the output transistor, is dependent on those voltages at its source and gate. *Id.*

220. The second current is further dependent on a *difference* between those voltages, as required by Claim 18. As discussed in reference to Claim 11, the output transistor is a MOSFET transistor, because it is drawn with a gap between the gate and body, and its terminals are labeled "gate" and "source." *Supra*, § VIII.A.6; *see also* Ex-1005, 3:63-65. A POSITA would have understood that in a MOSFET transistor, current flow is controlled in part the difference between the gate and source voltages. *See supra*, ¶¶ 66-72. Therefore, the second current supplied by the output transistor is based on the difference between its gate voltage (voltage at gate of feedback transistor) and source voltage (voltage at load circuitry).

221. Thus, Scott renders Claim 18 obvious.

**11. Claim 19: The method of claim 17, wherein supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases.**

222. Scott discloses Claim 19 for the same reasons as Elements 1[g] and 16[h]. *Supra*, §§ VIII.A.1.h, VIII.A.8.i. Thus, Scott renders Claim 19 obvious.

- 12. Claim 20: The method of claim 17, wherein supplying said load current includes supplying a current with a magnitude of less than one amp, and wherein supplying first current and supplying said second current includes supplying a current with a magnitude of less than one milli-amp.**

223. Claim 20 requires the load current to be less than one amp, and the first and second current to be less than one milli-amp. As discussed in reference to Claim 1, Scott's load current is I4, the first current is I5, and the second current is I2. *Supra*, §§ VIII.A.1.e-g. Scott's detailed description discloses an example where all the currents meet Claim 20's requirements. Ex-1005, 4:34-56. In this example, I4 (the claimed "load current") ranges from 300  $\mu$ A to 450  $\mu$ A, so it is always less than one amp. *Id.* I5 (the claimed "first current") is a constant 500  $\mu$ A, so it is less than one milli-amp. *Id.* And I2 (the claimed "second current") ranges from 200  $\mu$ A to 300  $\mu$ A, so it is also always less than one milli-amp. *Id.*

224. Thus, Scott renders Claim 20 obvious.

**B. Ground 2: Claims 1, 7-11, 14, and 16-20 Are Obvious Over Scott in view of Gradinariu**

225. Claims 1, 7-11, 14, and 16-20 are obvious in light of Scott alone. *Supra*, § VIII.A. Claims 1, 14, 16, and 19 are further obvious over Scott in view of Gradinariu.

**1. Motivation to Combine Scott and Gradinariu**

226. A POSITA would have been motivated to combine Scott and Gradinariu because both are directed to voltage regulators. *See* Ex-1005, 1:6 ("The

present invention relates to a voltage regulator); Ex-1006, 1:7-8 (“The present invention relates generally to voltage regulator circuits.”). Moreover, both inventions operate on the same principle—monitoring an output voltage and adjusting the load current accordingly to maintain a regulated output voltage. *See* Ex-1005, 1:57-60 (“The high-speed feedback loop operates to... restor[e] the regulated voltage to its desired value.”); Ex-1006, 2:49-53 (“The present invention... provides a regulated output voltage.”).

227. In particular, a POSITA would have been motivated to combine Scott with Gradinariu’s teaching that voltage regulators correct for output changes in either direction. It was known well before the application date here that voltage regulators correct for changes in output voltage in either direction. Because of this, a regulator that only provided one-way correction would not be commercially viable or practical. Gradinariu even discusses prior art references that describe corrections based on increases and decreases in output voltage. Ex-1006, 1:44-2:5. The alleged differences in these inventions relate to how that correction is achieved, not the type of correction applied. *Id.*, 2:6-36. While Scott’s disclosure focuses mainly on increasing a load current when the output voltage decreases (Ex-1005, 3:62-4:13), a POSITA would have understood that a voltage regulator needs to provide corrections in both directions in order to operate properly. *See* Ex-1006, 1:44-2:5. Thus, to the extent Scott does not disclose decreasing a load current when the output

voltage increases, a POSITA would have been motivated to combine Scott with Gradinariu's teaching of providing corrections in both directions. This would result in an improved voltage regulator circuit with bi-directional adjustment capability required in commercially viable voltage regulators, including those common in the prior art. *See* Ex-1006, 1:48-2:5.

228. A POSITA would have had an expectation of success when modifying Scott with Gradinariu's teaching about making voltage adjustments in both directions based on feedback from the output related to changes to the load. While Scott focuses on increasing load current when output voltage drops, it also discloses that it can respond to increases in output voltage by decreasing load current. *See* Ex-1005, 4:11-13 ("As the charge in the reservoir capacitor 20 increases, the current I<sub>2</sub> increases, thereby causing a decrease in the currents I<sub>3</sub>, I<sub>4</sub>, and I<sub>1</sub>."). In other words, Scott is already capable of reacting to output voltage changes in both directions. *Id.*, 3:62-4:13. Thus, a POSITA designing a voltage regulator according to Scott would have expected to be able to implement Gradinariu's teaching of reacting to changes in both directions with at most minor, easily implemented modifications.

## **2. Claim 1**

229. As discussed in section VIII.A.1, *supra*, all elements of Claim 1 are obvious over Scott alone.

- a. **Element 1[g]: wherein said second current supply circuit is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases; and**

230. To the extent Element 1[g] is not obvious over Scott alone, it is obvious over Scott in light of Gradinariu. Element 1[g] requires the second current supply circuit to operate via the pass device to cause an increase in the magnitude of the load current supplied to the output when the output voltage decreases, and vice versa. Scott in view of Gradinariu discloses or teaches these requirements.

231. As discussed with reference to Ground 1, Scott's output transistor is the claimed second current supply circuit, and operates in conjunction with the pass device to provide an output current to the load. *Supra*, §§ VIII.A.1.f-g. Gradinariu similarly includes what it calls a "output leg," which supplies an output current to a load through its terminal transistor N5. Ex-1006, 3:56-58, 4:29-33, Fig. 1.

232. As discussed with reference to Ground 1, Scott's output transistor causes an increase in magnitude of the load current when the output voltage decreases and vice versa. *Supra*, § VIII.A.1.h. To the extent the Board finds that Scott alone does not disclose this limitation, Scott in view of Gradinariu does. For example, Gradinariu discloses that its amplifier provides negative feedback with respect to the replica voltage. Ex-1006, 4:38-39. The replica voltage tracks the

output voltage, so output voltage changes are reflected in the replica voltage. *Id.*, 4:3-6. When the replica voltage drops below a reference voltage, the amplifier increases its output, and vice versa. *Id.*, 4:38-47. These changes in the amplifier's output are provided to the transistor N2, which provides current to the load through the output leg. *Id.*, 5:14-25. Thus, the output leg, in conjunction with the amplifier and the transistor N2, causes an increase in magnitude of the load current supplied to the output when the output voltage drops, and vice versa, as required by Element 1[g]. *Id.*

233. Thus, Scott in view of Gradinariu renders Claim 1 obvious.

### **3. Claim 14**

234. As discussed in section VIII.A.7, *supra*, all elements of Claim 14 are obvious over Scott alone.

- a. Element 14[h]: wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage said load increases, a magnitude of said load current is decreased; and**

235. To the extent Element 14[h] is not obvious over Scott alone, it is obvious over Scott in light of Gradinariu, for the same reasons as Element 1[g]. *Supra*, § VIII.B.2.a.

236. Thus, Scott in view of Gradinariu renders Claim 14 obvious.

**4. Claim 16**

237. As discussed in section VIII.A.6, all elements of Claim 16 are obvious over Scott alone.

- a. Element 16[h]: supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.**

238. To the extent Element 16[h] is not obvious over Scott alone, it is obvious over Scott in light of Gradinariu, for the same reasons as Element 1[g]. *Supra*, § VIII.B.2.a.

239. Thus, Scott in view of Gradinariu renders Claim 16 obvious.

- 5. Claim 19: The method of claim 17, wherein supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases.**

240. As discussed in section VIII.A.11, *supra*, Claim 19 is obvious over Scott alone. To the extent Claim 19 is not obvious over Scott alone, it is obvious over Scott in light of Gradinariu, for the same reasons as Element 1[g]. *Supra*, § VIII.B.2.a.

241. Thus, Scott in view of Gradinariu renders Claim 19 obvious.

**IX. CONCLUSION**

242. For the reasons set forth above, I believe that Claims 1, 7-11, 14, and 16-20 of the '962 Patent are unpatentable in view of the prior art.

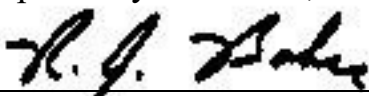
243. In signing this declaration, I recognize that it will be filed as evidence in a contested case before the Patent Trial and Appeal Board of the United States Patent and Trademark Office. I also recognize that I may be subject to cross-examination in the case and that cross-examination will take place in the United States. If cross-examination is required of me, I will appear for cross-examination within the United States during the time allotted for cross-examination.

244. I reserve the right to supplement my opinions in the future to respond to any arguments that the Patent Owner raises and to take into account new information as it becomes available to me.

245. I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Dated: October 16, 2025

Respectfully submitted,

  
\_\_\_\_\_  
R. Jacob Baker, Ph.D., P.E.