Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Filer:	Amy M. Salmela/Aubre Rabe
Attorney Docket Number:	4146.08US01

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	330	330
Utility Search Fee	1111	1	540	540
Utility Examination Fee	1311	1	220	220
Pages:				
Claims:				
Independent claims in excess of 3	1201	2	220	440
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1530**

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 :
H03F 3/45, G05F 3/16

A1

(11) International Publication Number: **WO 97/05696**

(43) International Publication Date: 13 February 1997 (13.02.97)

(21) International Application Number: PCT/US96/12238

(22) International Filing Date: 24 July 1996 (24.07.96)

(30) Priority Data:
08/509,982 1 August 1995 (01.08.95) US

(71) Applicant: INFORMATION STORAGE DEVICES, INC. [US/US]; 2045 Hamilton Avenue, San Jose, CA 95125 (US).

(72) Inventor: TRAN, Hieu, Van; 2741 Coltwood Drive, San Jose, CA 95148 (US).

(74) Agents: BLAKELY, Roger, W., Jr. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

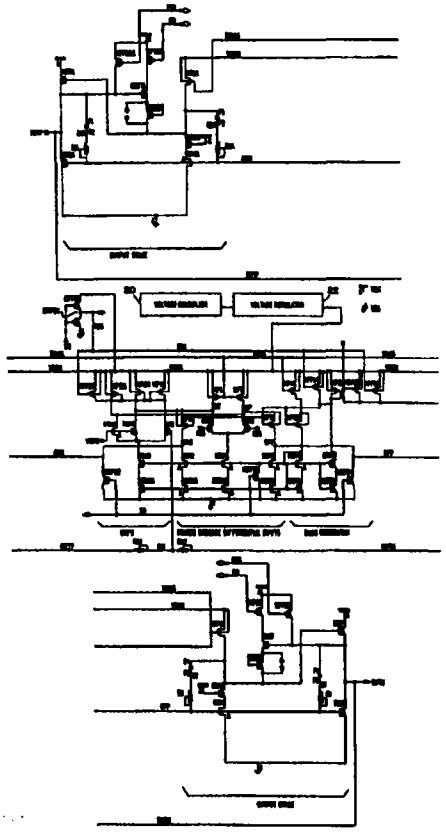
(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
With amended claims.

(54) Title: FULLY DIFFERENTIAL OUTPUT CMOS POWER AMPLIFIER

(57) Abstract

A fully differential output CMOS power amplifier suitable to be used in a non-volatile memory mixed mode chip for voice record and playback to drive a very low impedance load such as an 8-ohm speaker from a low voltage supply. This fully differential CMOS power amplifier utilizes a voltage multiplying technique for the input stage (MN2, MN3, MP6, MP7), a level shift/gain stage (MN/P12, MN/P13), and a common mode feedback network (MN1, MN10, MP10). It also utilizes native n-MOS having a threshold voltage VT = 0v for the folded cascode differential input and the source follower output stage (MN7), enhancement n-MOS (VT = 0.7v) for the common source output, and a voltage regulator (22) using p-MOS diode connected devices (M1-M5) for simulating a resistor divider to regulate the voltage multiplier output. The amplifier also includes a mechanism for crossover distortion reduction at the output driver stage, and a scheme to set the idle current in the output driver n-MOS transistors (MN7, MN9).



Petitioner Micron Ex-1004, 0003

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

Petitioner Micron Ex-1004, 0004

FULLY DIFFERENTIAL OUTPUT

CMOS POWER AMPLIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of analog CMOS integrated circuit design, and specifically to integrated operational amplifiers driving low impedance loads.

2. Prior Art

A fully differential output operational amplifier is normally superior to a single ended output operational amplifier in terms of power supply noise rejection and noise coupling rejection, since the power supply variation or any noise source couples equally to both output branches at the same time and thus appears as a common mode signal not effecting the differential output of the operational amplifier. This is especially important for a mixed mode chip (integrated circuit having both analog and digital circuits on the same substrate), where the noise is generated from the switching of the digital circuits.

In the prior art, fully differential output CMOS power amplifiers are implemented using typically a two (or sometimes more) stage operational amplifier which are powered from the normal system power supply VCC. The typical two stage operational amplifier consists of a mostly differential voltage amplifying input stage for

Petitioner Micron Ex-1004, 0005

noise and offset considerations, and a current gain and/or MOS output driver stage for driving a low impedance load. These two stages both get their power from VCC. Such CMOS operational amplifiers are difficult to operate from a low voltage power supply for driving low impedance loads, such as an 8 ohm speaker, since the gate driving ability of the MOS output stage is so limited. The limited gate drive could be made up in substantial part by increasing the size of the output devices, but this could make the MOS driver prohibitively large.

Conventional enhancement mode n-MOS input stages for low voltage operation also suffer from minimum input common mode range, since the input voltage has to be at least larger than the VT (threshold voltage) of the input n-MOS. Also, conventional enhancement mode n-MOS source follower output drivers suffer from a limited swing on the output voltage in the positive direction because of the VT drop from the gate to source.

BRIEF SUMMARY OF THE INVENTION

A fully differential output CMOS power amplifier utilizing a voltage multiplying technique to provide a regulated power supply higher than the system power supply to a folded differential input stage, the bias generator, the common mode feedback circuit, and the gain/level shift stage. This allows the analog gate voltages of the output transistors to go much higher than the normal power supply, resulting in significantly reduced required size of the output transistors. Since the pump is mainly to provide for the gate voltages which require little current, it is small. In a preferred embodiment, this CMOS power amplifier is used

Petitioner Micron Ex-1004, 0006

in a mixed mode chip which already has a voltage multiplier for the on-chip memory circuit, and therefore can readily use the on-chip pump without adding another pump circuit. This power amplifier also includes a voltage regulator to regulate the multiplied voltage to a fixed level to reduce power supply variation and noise from the oscillator of the voltage multiplier.

The voltage regulator is configured in a negative feedback operational amplifier loop with diode connected p-MOS devices serving as a resistor divider to reduce the current loading to the voltage multiplier. Each diode connected p-MOS has its own well tied to its source so the VGS (gate to source voltage) of each p-MOS is precisely mirrored across the diode chain by the negative feedback action. This gives a precise voltage at the output of the regulator, in the preferred embodiment of the invention, 5 times VREF.

This fully differential output CMOS power amplifier also includes a folded cascode differential input stage utilizing native n-MOS (VT ≈ Ov) to give a near rail to rail input common mode range, a native n-MOS (VT ≈ Ov) source follower on the output stage to give a high swing voltage output, an enhancement mode n-MOS common source output stage, a mechanism for reducing crossover distortion of the output driver stage, and a scheme to set the idle current in the output drivers when the input signal is zero.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram for the preferred embodiment of the fully differential CMOS power amplifier of the present invention, comprising Figures

Petitioner Micron Ex-1004, 0007

1A and 1C, each showing one of the differential output stages, and Figure 1B showing among other things the folded cascode differential input stage and the bias generator.

Figure 2 is a circuit diagram for the voltage regulator used in the circuit of Figure 1.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a circuit diagram for the preferred embodiment of the fully differential CMOS power amplifier of the present invention, using a folded cascode input stage and n-MOS transistors for the output drivers.

The preferred embodiment of the present invention is intended to be used as the output power amplifier on an integrated circuit analog signal recording and playback system such as disclosed in U.S. Patents 4,890,259, 4,989,179, 5,220,531, 5,126,967, 5,241494 and 5,164,915. Such integrated circuits already include a MOS charge pump voltage multiplier (the voltage multiplier 20 of Figure 1) for other purposes, namely to provide the required high voltages for the erase and program functions for the on-chip floating gate storage cells from a single, relatively low voltage power supply to the chip, such a low voltage battery power supply providing VCC, and VSS, shown also as ground potential. MOS charge pump voltage multipliers are well known in the art, and need not be further described herein.

Also shown in Figure 1 is a voltage regulator 22, used to regulate the multiplied voltage to reduce the voltage variation and noise coupled to the power amplifier from the charge pump, which typically has a

Petitioner Micron Ex-1004, 0008

ripple voltage on its output. The ripple period depends on the period of the pump clock generator. The ripple magnitude depends on the pumping capacitors, the magnitude of the pumping clock waveform (typically equal to VCC), the output loading current and the output loading capacitance. Even though this ripple is reduced by the power supply rejection capability of the power amplifier, it is still significant, so the voltage regulator 22 is used to reduce the ripple seen by the power amplifier. This is especially important in the idle state (when the input signal is zero), as the ripple will appear on the output as an idle noise which limits the signal to noise ratio of the power amplifier.

The fully differential output CMOS power amplifier includes a differential stage, a gain stage, common mode feedback and a bias generator, all of which get their power from the output of the voltage regulator, VCCM, a voltage significantly higher than VCC. The output stage, the only stage requiring substantial power, gets its power from the normal system power supply VCC.

The preferred embodiment of the present invention shown in Figure 1 is intended to operate as part of an integrated circuit responsive to a power down signal to power down the circuit whenever the PD (power down) signal goes high. As the subsequent description will illustrate, the following notation is used in Figures 1 and 2 herein:

p-channel devices are so indicated by the circle in the gate contact, and further by the P appearing as the second letter of the device designation

n-channel devices are so indicated by the absence of a circle in the gate contact, and

Petitioner Micron Ex-1004, 0009

further by the N appearing as the second letter of the device designation

native devices are indicated by the thickened line parallel to the gate and by the letter A adjacent thereto

most devices associated with the power down function are so indicated by "PD" appearing as the third and fourth letter designations of the respective devices

In the circuit of Figure 1, n-channel device MNPD1 and p-channel device MPPD1 are used to invert the PD (power down) signal to provide the signal PDB (PD bar or $\overline{PD}$). Device MPPD1 is connected to VCCM instead of VCC so that PDB is VCCM when PD is zero. Thus when the circuit is enabled (PD = Ov), PDB will be equal to VCCM, completely shutting off p-channel devices MPPD2/3/4/5/5A. At the same time, PD = Ov (PD = VSS) will also completely shut off n-channel devices MNPD2/3/4. As shall subsequently be described in further detail, devices MPPD2/3/4/5/5A and MNPD2/3/4 will be turned on when PD goes high to cut off all current paths in the circuit.

Current IBIAS to the circuit is a controlled current source (actually a current sink, though the phrase current source may be used generically hereafter for source or sink, as will be obvious to one skilled in the art) mirrored from a bias current generator elsewhere in the integrated circuit, as is well known in the art. This sets the gate-source voltage of transistor MBIAS1, the input bias reference p-MOS device, to provide the basic current mirror for biases of other p-channel devices, namely devices

Petitioner Micron Ex-1004, 0010

MP6/7/8/8A/14, each therefore acting as a bias current source for various other parts of the circuit.

The bias current through p-channel device MP14 also flows through p-channel device MP13B and n-channel devices MN14, MN14A to provide biases for n-MOS current mirrors formed by n-channel devices MN11/MN11A, MN12/MN12A, MN13/MN13A of the folded cascode differential input stage, and also to provide biases for n-channel devices MN10/MN10A of the common mode feedback network. It also provides a bias for n-channel devices MN15/MN15A connected in series with diode connected p-channel device MP15 to generate a p-MOS bias for the gates of p-channel devices MP12, MP13 of the folded cascode differential input stage. p-channel device MP13B is used to force the drain-source voltage of p-channel device MP14 to be close to the drain-source voltage of p-channel devices MP7 and MP6 for more precise current matching between p-channel device MP7 and n-channel devices MN13/MN13A and between p-channel device MP6 and n-channel devices MN12/MN12A (since n-channel devices MN13/MN13A and MN12/MN12A are mirrored from n-channel device MN14, which is sinking the bias current from p-channel devices MP14).

The n-MOS cascode current mirror formed by n-channel devices MN14/MN14A uses a native (VT $\approx$ Ov) n-MOS device MN14 in series with enhancement mode n-MOS device MN14A to minimize the headroom voltage, since the bias voltage is only one gate-source voltage of the enhancement mode n-MOS device MN14A (this is in comparison with the normal two diode connected n-MOS transistors in series, which requires the sum of 2 gate-source voltages of headroom voltage). n-channel device MN14A is in saturation, since its drain voltage is close to its gate voltage. n-channel device MN14 is also in

Petitioner Micron Ex-1004, 0011

saturation since its threshold voltage is a few hundred millivolts because of the body effect. Hence, the cascoding effect is achieved with lower headroom voltage by using a native device connected in series with an enhancement n-MOS device. The native n-MOS device has its drain and gate tied together. The other n-MOS device mirrors the current to n-channel devices MN10/MN10A, MN11/MN11A, MN12/MN12A, MN13/MN13A, and MN15/MN15A, which use the same scheme.

n-channel devices MN15/MN15A mirror the current from n-channel devices MN14/MN14A to p-channel device MP15 to generate the bias for the common gate connection of p-channel devices MP12 and MP13. p-channel device MP15 is sized such that the source voltages of p-channel devices MP12 and MP13 sit close to VCCM (only one drain-source saturation voltage of p-channel devices MP6 and MP7 away from VCCM) for maximum swing on the nodes OP, ON and hence on nodes OPP, ONN to optimize the size of n-channel device MN9 and MN9A.

n-channel devices MN2/MN3, p-channel devices MP6/MP7 and MP12/MP13, and n-channel devices MN12/MN12A, MN11/MN11A and MN13/MN13A constitute a folded differential native n-MOS input stage. The native n-MOS devices MN2 and MN3 are chosen for the input n-MOS pair to increase the minimum input voltage range by one enhancement mode threshold voltage and thus lower the minimum voltage input close to ground. The outputs of the folded cascode input stage on nodes OPP and ONN are differential, and are each applied to a respective single ended n-MOS output stage. In particular, when the differential inputs POS and NEG are applied to the differential input n-channel pair MN2 and MN3, the differential outputs of nodes ON and OP respond in opposite directions, in turn causing nodes ONN and OPP

Petitioner Micron Ex-1004, 0012

to follow the voltage variations of nodes ON and OP, respectively, through the common gate connected p-MOS devices MP12 and MP13. The voltages on nodes ONN and OPP are thus applied differentially to the two identical n-MOS output stages.

n-channel devices MN4, MN16, p-channel device MP8, n-channel devices MN7, MN9, p-channel device MP20, n-channel devices MN17, MN18, p-channel device MPPD5, resistor R2, capacitor C2, resistor R1 and capacitor C1 constitute an n-MOS output stage. The second identical n-MOS output stage is formed by corresponding devices having the same designations followed by the letter "A", and accordingly the description to follow is also directly applicable, though being responsive to the opposite node ONN, the opposite voltage of the differential voltages on nodes ONN, OPP. In each output stage, the capacitor is realized on-chip in integrated circuit form using techniques well known in MOS integrated circuits and MOS integrated circuit formation.

p-channel device MPPD5 is part of the shutdown circuit, and is held off (PDB high) when the circuit is not powered down (PD low). p-channel device MP20 is also related to the power down function, and is held on by PD when the circuit is not powered down. n-channel device MN7 is used in a source follower mode, and is a native n-MOS to increase the high swing by one enhancement mode threshold voltage to make the high end output OUTN swing of the output stage close to the power supply voltage VCC. n-channel devices MN4, MN16, p-channel device MP8, resistor R2, and capacitor C2 provide gain/level shift for the source follower MN7, with resistor R2 and capacitor C2 providing a compensation network for the gain/level network.

Petitioner Micron Ex-1004, 0013

Resistor R1 and capacitor C1 provide a compensation network for the final gain output stage comprising n-channel device MN9.

The output stage described above operates as follows: Assuming the signal on node OPP goes lower, n-channel device MN9 is gradually turned off, and n-channel device MN4 is also gradually turned off. p-channel device MP8 pulls the gate of n-channel device MN7 toward VCCM, and device MN7 in turn pulls the output OUTN toward VCC. Conversely, as the voltage on node OPP goes higher, n-channel device MN9 is gradually turned on, pulling the output OUTN lower. n-channel device MN4 is also gradually turned on harder, pulling the gate of n-channel device MN7 toward ground, tending to turn off device MN7 to release OUTN from the pull up effects of device MN7. Thus the output stage acts as an inverting stage.

n-channel devices MN17 and MN18 are to reduce the crossover distortion. At the mid point (analog ground, e.g. 1.5V, or zero differential input to the system), as the voltage on node OPP goes from low to high, n-channel device MN4 is turned on, pulling the gate of n-channel device MN7 too quickly toward ground, shutting n-channel device MN7 off completely. In the meantime, n-channel device MN9 is not yet turned on, so the output OUTN is floating for a short period until n-channel device MN9 is turned on. This causes distortion. To prevent this, the voltage on the gate of n-channel device MN7 is lowered slowly to turn off device MN7 slowly by a local feedback path from the output OUTN to the gate of n-channel device MN17, which does not allow the gate of n-channel device MN7 to fall too rapidly. n-channel device MN16 acts as a resistive path to further slow down the falling of the gate of n-channel device MN7.

Petitioner Micron Ex-1004, 0014

By not allowing the gate of device MN7 to fall before device MN9 is turned on, a direct current path is created between VCC and VSS through devices MN7 and MN9 for a short period. This is the familiar tradeoff between reducing crossover distortion and increasing the direct current consumption. In that regard, n-channel device MN18, as an option, may be shorted for reducing further the crossover distortion at the expense of increasing the direct current consumption.

The idle current in the output stage (when there is no differential signal) is precisely set by the size ratio of n-channel devices MN9 to MN4 (and the bias current in n-channel device MN4, which is set by the current mirrored to p-channel device MP8). Note that the gate voltages of n-channel devices MN9 and MN4 are the same and the drain voltage of n-channel device MN9 is almost the same as the drain voltage of n-channel device MN4 by the action of source follower native n-MOS device MN7. Also because the gate of the n-channel device is allowed to swing higher than the normal power supply voltage VCC, allowing the use of a much smaller device for n-channel device MN9 (better matching between devices MN9 and MN4 because they are closer together physically), this allows the idle current to be controlled much better.

As stated before, n-channel devices MN4A, MN16A, p-channel device MP8A, n-channel device MN7A, MN9A, p-channel device MP20A, n-channel devices MN17A, MN18A, p-channel device MPPD5A, resistor R2A, capacitor C2A, resistor R1A and capacitor C1A constitute another exact replica of the above n-MOS output stage. This output branch receives its input from the ONN signal, which is differentially is always in the opposite direction to the OPP signal by the action of the input stage. Thus

the output OUTP always swings in the opposite direction of the output OUTN.

The outputs OUTP and OUTN are normally connected across a speaker for driving differentially to increase the power output by four times (since the voltage swing across the speaker is doubled) as compared to a single ended power amplifier. Normally the power amplifier is used in a unity gain mode, in which case OUTP of the respective output stage is also connected to NEG input of the differential input stage.

Resistors RX1 and RX2 are common mode feedback resistors connected between the differential outputs. Their resistances are high to prevent excessive loading. The resistor network is used to sense the common mode voltage on the inputs of the power amplifier and to feed back the common mode voltage to a common mode feedback amplifier for common mode voltage correction.

n-channel devices MN1/MN1A/MN1B, p-channel devices MP10/MP10A/MP10B and n-channel devices MN10/MN10A constitute the common mode feedback amplifier. It is a conventional MOS differential amplifier with the native n-MOS transistors as the input n-MOS pair. The native n-MOS is used to increase the input voltage range as in the folded cascode input pair. The common mode input VCMD is the analog ground level (the mid point, e.g. 1.5V in the preferred embodiment). Assuming the average of the differential outputs OUTN and OUTP is somehow higher than normal, the voltage of node CM at the resistive network junction will be higher than VCMD, causing n-channel device MN1 to turn on harder, pulling the gate of p-channel device MP10 lower, which turns p-channel devices MP10A and MP10B on harder and pulls the node OP and ON higher respectively, in turn pulling both nodes ONN and OPP higher by the common gate connected p-

Petitioner Micron Ex-1004, 0016

channel devices MP12, MP13. With the voltages of nodes ONN and OPP higher, the voltages of both nodes OUTN and OUTP go lower (the output stages of the amplifier are inverting stages), restoring the common mode voltage in the output nodes OUTN and OUTP. As the differential output OUTN and OUTP swing in the opposite direction, opposite action happens.

The folded differential input stage obtains its power from the regulated pumped output VCCM, which allows nodes ON and OP to be biased one saturation drain-source voltage VDS_{sat} from VCCM (VCCM - $VDS_{MP6/7sat}$). This also means the voltages of nodes OPP and ONN can swing to two saturation VDSs from VCCM (VCCM - $VDS_{MP6/7sat}$ - $VDS_{MP12/13sat}$), which allows the size of n-channel devices MN9/MN9A to be small devices, even though n-channel devices MN9/MN9A have to sink a relatively huge current from the low impedance load. The level shift/gain stages (n-channel devices MN4, MN16, p-channel device MP8, resistor R2 and capacitor C2, and n-channel devices MN4A, MN16A, p-channel device MP8A, resistor R2A and capacitor C2A) get their power supply from VCCM, which allows the gate of n-channel devices MN7/MN7A to swing close to VCCM. This allows n-channel devices MN7/MN7A to be also to be small, even though n-channel devices MN7/MN7A have to source a relatively huge current to the low impedance load. The common mode feedback circuit and the bias generator also get their power supply from VCCM for proper operation.

As stated before, when the circuit is enabled (PD = Ov), PDB will be equal to VCCM, completely shutting off p-channel devices MPPD2/3/4/5/5A. At the same time, PD = Ov (PD = VSS) will also completely shut off n-channel devices MNPD2/3/4. However when PD goes high for power down, n-channel devices MNPD2/3/4 PDB will be turned on,

Petitioner Micron Ex-1004, 0017

and PDB will go low, turning on p-channel devices MPPD2/3/4/5/5A. This shuts down the various bias current sources in the amplifier and cuts off all current paths in the circuit. The turning on of p-channel devices MPPD5/5A on power down clamps the voltage of output nodes OUTN and OUTP at VCC, thereby holding the differential output at zero. Also on power down, p-channel devices MP20/20A are turned off to cut off the current path from VCC to VCCM through n-channel devices MN17/17A, MN18/18A and p-channel devices MP8/8A.

Figure 2 is a circuit diagram for the voltage regulator 22 used in the circuit of Figure 1. As shown in Figure 2, an operational amplifier I1 is configured in a negative feedback loop to regulate the multiplied voltage VCCMP to a fixed level VCCM based on an input reference voltage VREF to reduce the coupling of power supply variations and noise to the power amplifier. The operational amplifier I1 used in the preferred embodiment is a conventional two stage operational amplifier. p-channel devices M1/M2/M3/M4/M5, when p-channel device M5 is on, are a series of diode connected devices, and each have their sources connected to their own well to eliminate body effect) to simulate a resistor divider of larger value resistors to reduce current loading to the voltage multiplier. In this way, p-channel devices M1/M2/M3/M4/M5 are small as compared to the large area that would be needed to realize large value resistors on-chip. In this Figure, n-channel devices MPD2 and M8 are used for power down purposes. In normal operation (PD low), n-channel device MPD2 and M8 will be off. This will hold P-channel device M5 on, activating the simulated resistor divider to feed back one fifth of the regulated voltage VCCM to the negative input of the operational amplifier. On power down when PD goes high, n-channel devices MPD2 and M8 will be

Petitioner Micron Ex-1004, 0018

turned on. n-channel devices M7/M8 are used to keep VCCM close to VCC during power down. This holds the negative input to the operational amplifier I1 high, and N-channel device MPD2 being on pull the voltage on node VCCMR to ground, turning off N-channel device M6 to decouple the output VCCM and the resistor divider from the voltage multiplier.

Thus the regulator output VCCM is regulated precisely by the negative feedback action of the operational amplifier at 5 times the reference voltage VREF, which is also 5 times the gate-source voltage of each of the p-channel devices M1/M2/M3/M4/M5 for the current flowing there through at the regulated voltage. As can be seen from the Figure, n-channel devices M6, M8 are native n-MOS devices. n-channel device M8 is to precharge the output node VCCM close to VCC, and n-channel device M7 is to keep VCCM within one threshold voltage of VCC on startup until the charge pump output VCCMP is high enough.

There has been described herein a fully differential output CMOS power amplifier that uses small output transistors for driving a low impedance load such as an 8 ohm speaker at low power supply voltages such as 2.5 volts by utilizing a stepped up voltage for a folded cascode differential input with native n-MOS devices, for the level shift/gain stage, for the common feedback network, and for the bias generator. The fully differential output CMOS power amplifier has a folded cascode differential input stage that uses native n-MOS for near rail-to-rail common mode input range, an output stage that uses native n-MOS devices in a source follower configuration for high swing efficiency, and a local feedback mechanism for reducing crossover distortion for the n-MOS output stage. A voltage

Petitioner Micron Ex-1004, 0019

regulator is provided for the stepped up voltage that uses very little current without requiring large value resistors by utilizing diode connected p-MOS transistors as a resistor divider. The n-MOS device output stage includes circuitry that accurately sets the idle current by utilizing a source follower native n-MOS to force the drain voltage of the output driver n-MOS to be almost the same as the drain voltage of a reference n-MOS device. However while a preferred embodiment of the present invention have been disclosed and described herein, it will be obvious to those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Petitioner Micron Ex-1004, 0020

What is claimed is:

1. A differential output CMOS power amplifier for low voltage operation comprising:

a folded cascode differential input stage having native n-MOS devices forming the differential input;

a level shift and gain stage coupled to the differential input stage;

a pair of power output stages coupled to the level shift and gain stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier;

a bias generator for providing bias currents to the folded cascode differential input stage, the level shift and gain stage, and the pair of power output stages;

the pair of power output stages having input power terminals for coupling to a low voltage power supply;

the bias generator, the folded cascode differential input stage and the level shift and gain stage having terminals for coupling to a voltage substantially higher than the low voltage power supply.

2. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have a n-MOS device connected as a source follower.

Petitioner Micron Ex-1004, 0021

3. The differential output CMOS power amplifier of claim 2 wherein the pair of power output stages each have local feedback for reducing crossover distortion.

4. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have as an output driver a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

5. The differential output CMOS power amplifier of claim 4 wherein the pair of power output stages each have a reference source follower native n-MOS device coupled to set the idle current for the output stage by forcing the drain voltage of the output driver to approximately equal the drain voltage of the reference source follower native n-MOS device.

6. The differential output CMOS power amplifier of claim 1 further comprised of a common mode voltage feedback circuit coupled to the output terminals for feeding the common mode output voltage back to the differential input stage.

7. The differential output CMOS power amplifier of claim 6 wherein the common mode voltage feedback circuit is for coupling to a voltage substantially higher than the low voltage power supply.

Petitioner Micron Ex-1004, 0022

8. The differential output CMOS power amplifier of any one of claims 1, 6 or 7 further comprised of a voltage multiplier for coupling to a low voltage power supply and for providing the voltage substantially higher than the low voltage power supply.

9. The differential output CMOS power amplifier of claim 8 further comprised of a voltage regulator coupled to the voltage multiplier to regulate the voltage substantially higher than the low voltage power supply irrespective of variations in the output voltage of the voltage multiplier.

10. The differential output CMOS power amplifier of claim 9 wherein the voltage regulator comprises:

a plurality of diode connected p-MOS devices connected in series;

a first power supply connection connected to one end of the series connected p-MOS devices;

a regulator output connection connected to the second end of the series connected p-MOS devices;

a second power supply connection;

a transistor coupled between the second power supply connection and the output connection; and,

an amplifier coupled to the transistor for controlling the current flow from the second power supply connection through the transistor responsive to the difference between the voltage across one on the series connected p-MOS devices and a reference voltage.

Petitioner Micron Ex-1004, 0023

11. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage with native n-MOS devices forming the differential input; and,

a pair of power output stages coupled to the folded cascode differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier, the output stages each having a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

12. The differential output CMOS power amplifier of claim 11 wherein the pair of power output stages are for coupling to a low voltage power supply, and the differential input stage is for coupling to a voltage substantially higher than the low voltage power supply.

13. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage having native n-MOS devices as the input devices for near rail-to-rail common mode input range;

a level shift and gain stage coupled to the differential input stage; and,

a pair of power output stages coupled to the differential input stage, each power output stage having

Petitioner Micron Ex-1004, 0024

an output terminal forming one of the differential outputs of the CMOS power amplifier.

14. The differential output CMOS power amplifier of claim 13 wherein the differential input stage is a folded cascode differential input stage with native n-MOS devices forming the differential input.

15. The differential output CMOS power amplifier of either claim 13 or claim 14 wherein the pair of power output stages are for coupling to a low voltage power supply, and the differential input stage is for coupling to a voltage substantially higher than the low voltage power supply.

16. A voltage regulator comprising:

a plurality of diode connected p-MOS devices connected in series;

a first power supply connection connected to one end of the series connected p-MOS devices;

a regulator output connection connected to the second end of the series connected p-MOS devices;

a second power supply connection;

a transistor coupled between the second power supply connection and the output connection; and,

an amplifier coupled to the transistor for controlling the current flow from the second power supply connection through the transistor responsive to

Petitioner Micron Ex-1004, 0025

the difference between the voltage across one on the series connected p-MOS devices and a reference voltage.

Petitioner Micron Ex-1004, 0026

AMENDED CLAIMS

[received by the International Bureau on 12 December 1996 (12.12.96); original claims 1-16 replaced by amended claims 1-12 (4 pages)]

1. A differential output CMOS power amplifier for low voltage operation comprising:

a folded cascode differential input stage having native n-MOS devices forming the differential input;

a level shift and gain stage coupled to the differential input stage;

a pair of power output stages coupled to the level shift and gain stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier;

a bias generator for providing bias currents to the folded cascode differential input stage, the level shift and gain stage, and the pair of power output stages;

the pair of power output stages having input power terminals for coupling to a low voltage power supply;

the bias generator, the folded cascode differential input stage and the level shift and gain stage having terminals for coupling to a voltage substantially higher than the low voltage power supply.

2. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have a n-MOS device connected as a source follower.

Petitioner Micron Ex-1004, 0027

3. The differential output CMOS power amplifier of claim 2 wherein the pair of power output stages each have local feedback for reducing crossover distortion.

4. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have as an output driver a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

5. The differential output CMOS power amplifier of claim 4 wherein the pair of power output stages each have a reference source follower native n-MOS device coupled to set the idle current for the output stage by forcing the drain voltage of the output driver to approximately equal the drain voltage of the reference source follower native n-MOS device.

6. The differential output CMOS power amplifier of claim 1 further comprised of a common mode voltage feedback circuit coupled to the output terminals for feeding the common mode output voltage back to the differential input stage.

7. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage with native n-MOS devices forming the differential input; and,

Petitioner Micron Ex-1004, 0028

a pair of power output stages coupled to the folded cascode differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier, the output stages each having a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

8. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage having native n-MOS devices as the input devices for near rail-to-rail common mode input range;

a level shift and gain stage coupled to the differential input stage; and,

a pair of power output stages coupled to the differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier.

9. The differential output CMOS power amplifier of claim 8 wherein the differential input stage is a folded cascode differential input stage with native n-MOS devices forming the differential input.

10. The differential output CMOS power amplifier of claim 9 wherein the pair of power output stages each have a native n-MOS device connected as a source follower.

AMENDED SHEET (ARTICLE 19)

Petitioner Micron Ex-1004, 0029

11. A voltage regulator for receiving a voltage input and providing a regulated voltage output comprising:

a plurality of transistors connected in series, the first of the series of transistors being diode coupled when active, the rest of the series of transistors being diode coupled, the series of transistors having a first end thereof coupled to a circuit ground and a second end thereof coupled to the regulator output;

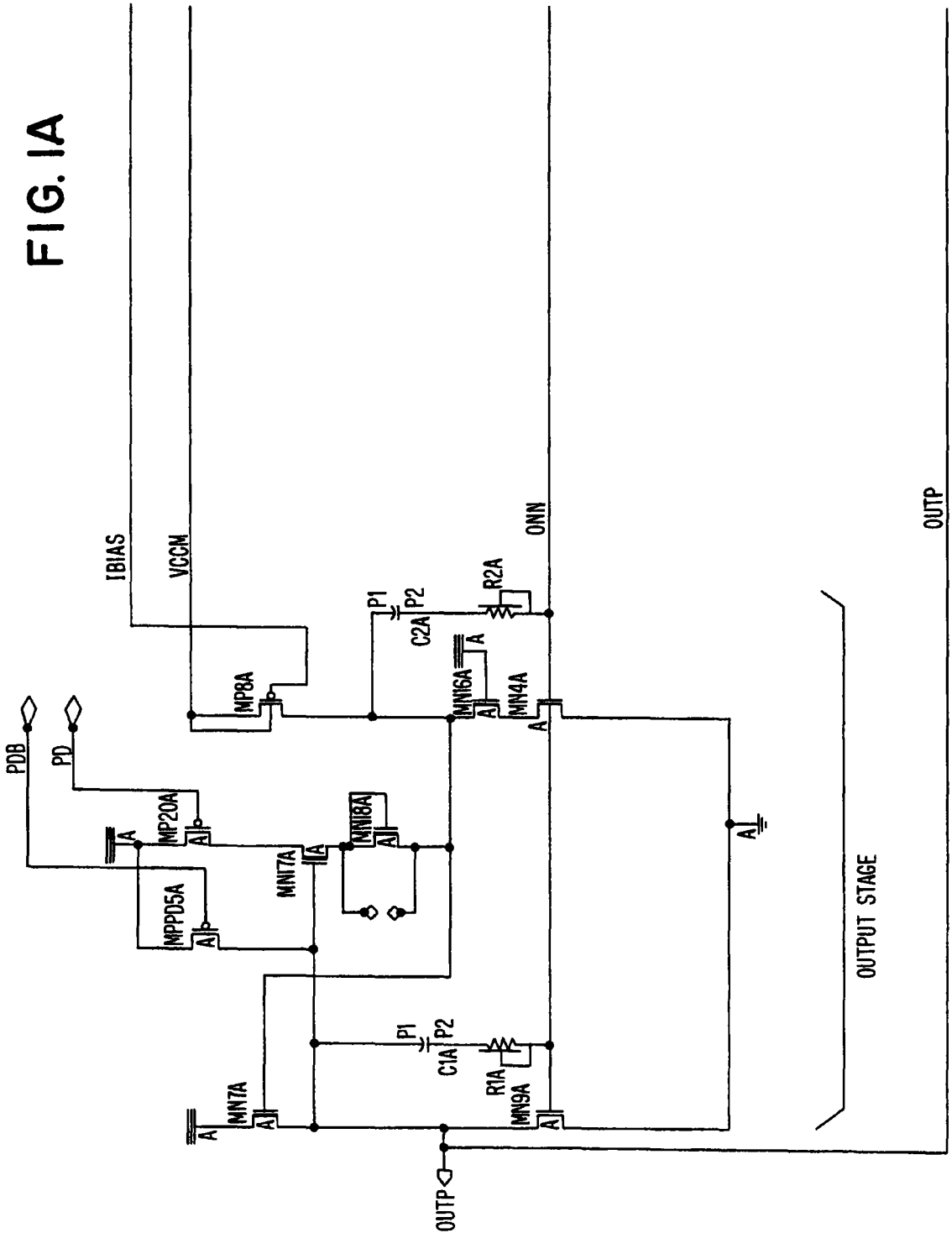
a differential amplifier having an amplifier output, a first input coupled to the connection between two of the series of diode connected transistors, and a second input coupled to a reference voltage; and,

a regulating transistor coupled between the voltage input and the first end of the series of diode connected transistors and controlled by the amplifier output to provide a current through the series of diode connected transistors to maintain the voltage between the inputs of the differential amplifier substantially equal.

12. The voltage regulator of claim 11 wherein the transistors are MOS transistors, each having a source, a gate, and a drain.

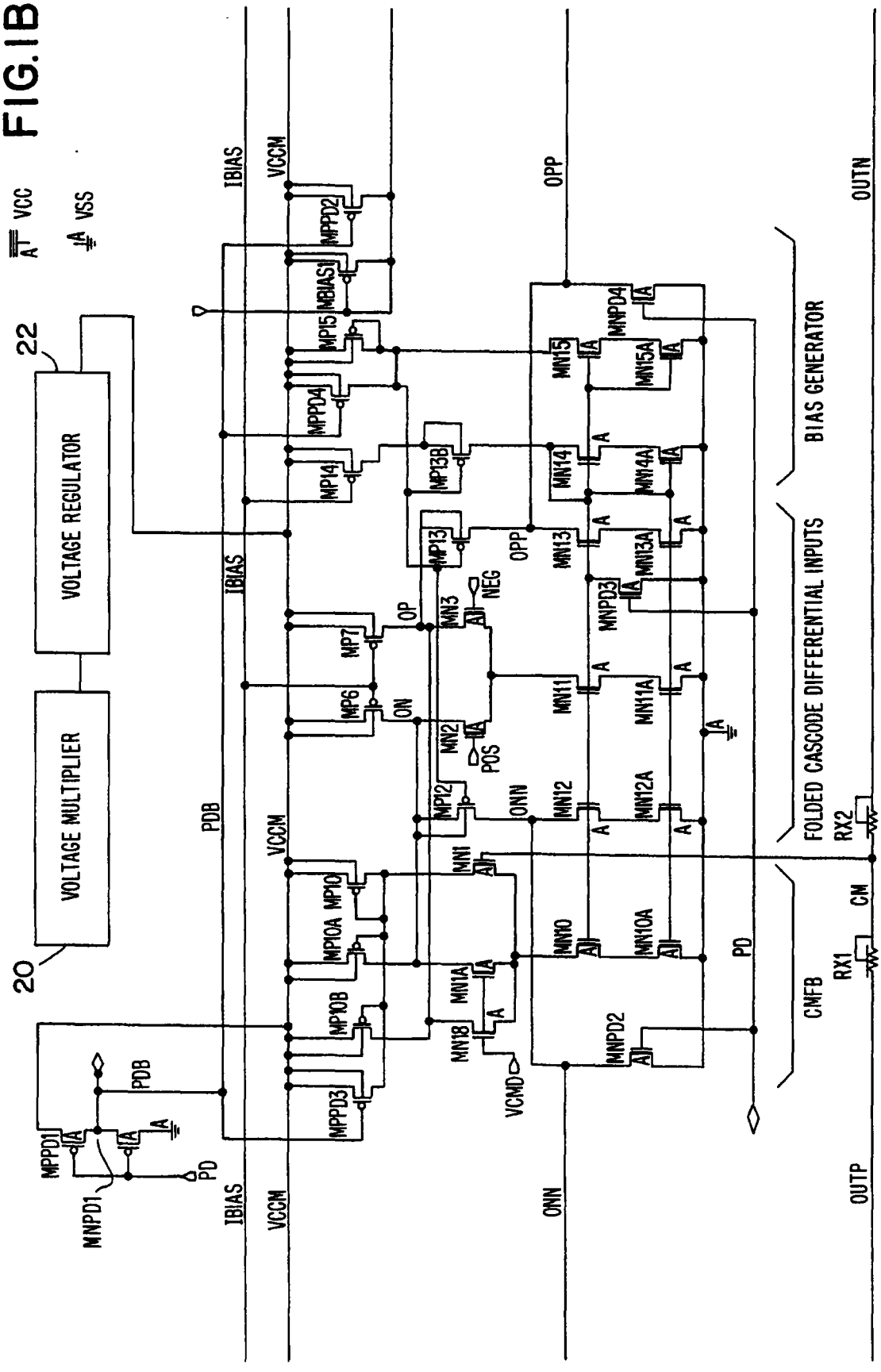
Petitioner Micron Ex-1004, 0030

FIG. IA



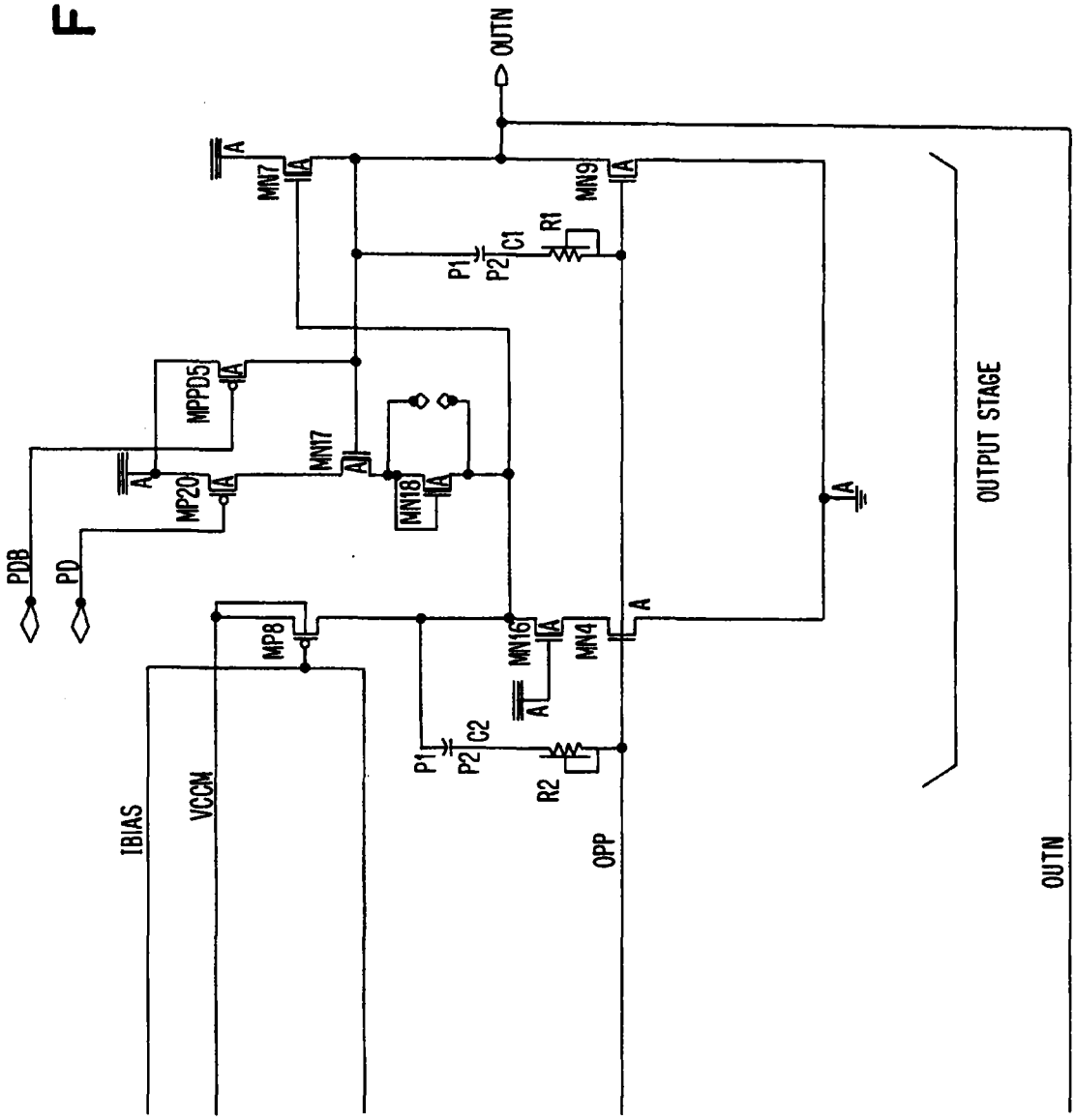
Petitioner Micron Ex-1004, 0031

FIG.1B



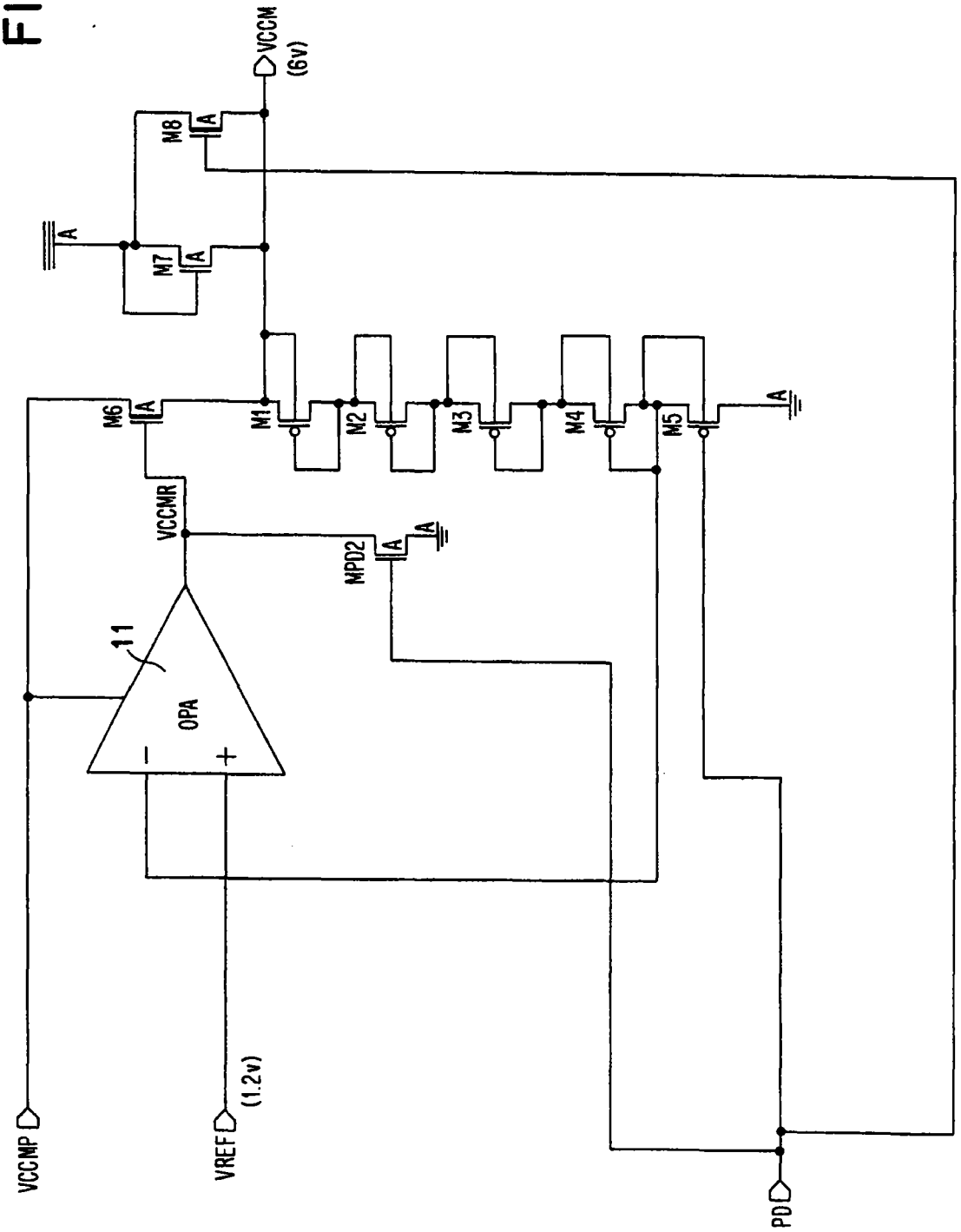
Petitioner Micron Ex-1004, 0032

FIG. IC



Petitioner Micron Ex-1004, 0033

FIG. 2



Petitioner Micron Ex-1004, 0034

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO3F 3/45; G05F 3/16
US CL :330/253, 255; 323/313
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 330/253, 255,258,261; 323/313

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,797,631 (HSU et al.) 10 January 1989, see the figure and col. 2,lines 5-7.	13-15
Y	US,A, 5,212,455 (Pernici et al.) 18 May 1993, see fig. 1.	13-15
X	US, A, 5,434,498 (Cordoba et al.) 18 July 1995, see fig. 1.	16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
03 OCTOBER 1996	16 OCT 1996

Name and mailing address of the ISA/US	Authorized officer
Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231	Steven Mottola
Facsimile No. (703) 305-3230	Telephone No. (703) 308-4914

Form PCT/ISA/210 (second sheet)(July 1992)★

Petitioner Micron Ex-1004, 0035

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

Petitioner Micron Ex-1004, 0036

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS
search terms: folded cascode, level shift, bias, differential, push pull, source follower

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claim(s)1-15, drawn to a differential amplifier, classified in class 330, subclass 253.
Group II, claim(s) 16, drawn to a voltage regulator, classified in class 323, subclass 313.
The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the differential amplifier of Group I does not require a power supply incorporating the particular voltage regulator of Group II.

Petitioner Micron Ex-1004, 0037

What is claimed is:

1. A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;

a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;

a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit;

a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;

wherein said second current source is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases; and

Petitioner Micron Ex-1004, 0038

wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit.

2. The voltage regulator circuit of claim 1, wherein said second current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current source is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor.

3. The voltage regulator circuit of claim 2, wherein said replica transistor is an nmos transistor.

4. The voltage regulator of claim 2, wherein said second current source is constructed to supply said second current based on $K(Vgate - Vout - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

5. The voltage regulator circuit of claim 2, wherein said replica transistor is a pmos transistor.

Petitioner Micron Ex-1004, 0039

6. The voltage regulator of claim 2, wherein said second current source is constructed to supply said second current based on $K(Vout - Vgate - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

7. The voltage regulator circuit of claim 1, wherein said second current source further comprises at least one stability capacitor arrangement.

8. The voltage regulator circuit of claim 8, wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads.

9. The voltage regulator of claim 1, wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path.

10. The voltage regulator of claim 1, wherein said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp.

11. The voltage regulator of claim 1, wherein said signal received at said pass device gate is a voltage.

12. A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

Petitioner Micron Ex-1004, 0040

an input adapted to receive a voltage from said power supply, wherein said input includes a positive node and a negative node;

an output adapted to be coupled to said load;

a current mirror that includes

a first transistor coupled to a first current path that includes a gate constructed to receive a bias voltage and a first end coupled to said positive node;

a second transistor coupled to a second current path that includes a gate coupled to said gate of said first transistor; and

wherein said current mirror is operable to mirror a current of said first current path at said second current path;

a feedback circuit coupled to said first current path that includes:

a differential amplifier that includes a first input, a second input, and an output, wherein said differential amplifier is adapted to provide, at said output, an output voltage based on a difference between a voltage at said first input and a voltage at said second input, and wherein said first input is constructed to receive a reference voltage;

a feedback transistor that includes a gate, a first end, and a second end, wherein said first end is coupled to a second end of said first transistor of said current mirror, and wherein said second end is coupled to said negative node;

a voltage divider that includes a first end coupled to said second end of said first transistor of said current mirror and a second end coupled to said negative node;

wherein said second input of said differential amplifier is coupled to said voltage divider such that a voltage at said second input is based on a voltage across said first end

Petitioner Micron Ex-1004, 0041

and said second end of said feedback transistor, wherein said gate of said feedback transistor is coupled to said output of said differential amplifier; and

wherein said differential amplifier, said feedback transistor, and said voltage divider are constructed and arranged such that a voltage at said gate of said feedback transistor is maintained at a substantially constant magnitude;

a current source that includes a first end coupled to a second end of said second transistor of said current mirror and a second end coupled to said negative node, and wherein said current source is constructed to receive a first voltage reference based on a voltage at said gate of said feedback transistor and a second voltage reference based on a voltage at said output of said voltage regulator circuit and supply a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;

a pass device that includes a first end coupled to said positive node, a second end constructed to be coupled to said load at said output of said voltage regulator circuit, and a gate coupled to said second end of said second transistor of said current mirror and said first end of said current source, wherein said gate is adapted to receive a signal based on a magnitude of a current of said second current path;

wherein said current source is constructed to, if said second voltage reference increases in magnitude, cause a decrease said signal received at said gate of said pass device, and if said second voltage reference decreases in magnitude, cause an increase in a magnitude of said signal received at said gate of said pass device;

wherein said pass device is constructed to supply a load current to a load coupled to said output of said voltage regulator circuit with a magnitude based on said signal received at said gate of said pass device; and

Petitioner Micron Ex-1004, 0042

wherein said current mirror, said feedback circuit, said current source, and said pass device are integrated in an integrated circuit.

13. The voltage regulator circuit of claim 16, wherein said current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and said output of said voltage regulator circuit, and wherein said current source is adapted to supply a current with a magnitude based on said signal received at said gate of said replica transistor.

14. A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions, comprising:

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a first current path referenced to said input;

feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;

first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;

second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second

Petitioner Micron Ex-1004, 0043

current path with a magnitude based on said first voltage reference and said second voltage reference;

means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;

wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage at said load increases, a magnitude of said load current is decreased; and

wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit.

15. The voltage regulator circuit of claim 14, wherein said second current supply means includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current supply means are for supplying said second current with a magnitude based on said voltage at said gate of said replica transistor.

16. A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

receiving, from a power supply, a power supply voltage;

Petitioner Micron Ex-1004, 0044

supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current;

receiving, at a feedback transistor integrated in said integrated circuit, said master current;

maintaining, via a feedback circuit integrated in said integrated circuit and coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant;

supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude;

supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load;

receiving, at a gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path; and

supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.

17. A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

generating, at a first current path integrated in said integrated circuit, a substantially constant master current;

Petitioner Micron Ex-1004, 0045

supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current;

supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load;

receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path;

supplying, to said load circuitry via said pass transistor, a load current in response to said control signal; and

wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current.

18. The method of claim 8, wherein supplying said second current includes supplying a current based on a difference between a voltage at a gate of a feedback transistor of a feedback circuit and a voltage at said load circuitry.

19. The method of claim 1, wherein supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases.

Petitioner Micron Ex-1004, 0046

20. The method of claim 11, wherein supplying said load current includes supplying a current with a magnitude of less than one amp, and wherein supplying first current and supplying said second current includes supplying a current with a magnitude of less than one milli-amp.

5

Petitioner Micron Ex-1004, 0047

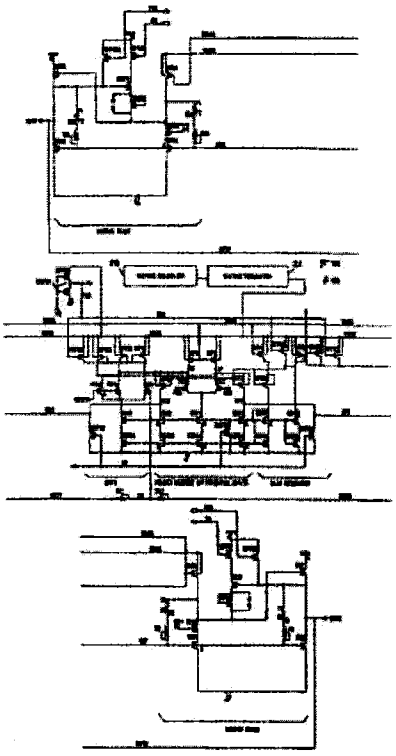
FULLY DIFFERENTIAL OUTPUT CMOS POWER AMPLIFIER

Publication number: EP0783796 (A1)
Publication date: 1997-07-16
Inventor(s): TRAN HIEU VAN [US]
Applicant(s): INFORMATION STORAGE DEVICES [US]
Classification:
- international: ***G05F3/24; H03F3/30; H03F3/45;*** **G05F3/08; H03F3/30; H03F3/45;** (IPC1-7): H03F3/45; G05F3/16
- European: G05F3/24C; H03F3/30B7B; H03F3/45S1B1B; H03F3/45S3B1A3
Application number: EP19960925488 19960724
Priority number(s): WO1996US12238 19960724; US19950509982 19950801

Also published as:
WO9705696 (A1)
US5631606 (A)
JP10507334 (T)
AU6598596 (A)
CA2201367 (A1)

Abstract not available for EP 0783796 (A1)
Abstract of corresponding document: **WO 9705696 (A1)**

A fully differential output CMOS power amplifier suitable to be used in a non-volatile memory mixed mode chip for voice record and playback to drive a very low impedance load such as an 8-ohm speaker from a low voltage supply. This fully differential CMOS power amplifier utilizes a voltage multiplying technique for the input stage (MN2, MN3, MP6, MP7), a level shift/gain stage (MN/P12, MN/P13), and a common mode feedback network (MN1, MN10, MP10). It also utilizes native n-MOS having a threshold voltage VT = 0v for the folded cascode differential input and the source follower output stage (MN7), enhancement n-MOS (VT = 0.7v) for the common source output, and a voltage regulator (22) using p-MOS diode connected devices (M1-M5) for simulating a resistor divider to regulate the voltage multiplier output.; The amplifier also includes a mechanism for crossover distortion reduction at the output driver stage, and a scheme to set the idle current in the output driver n-MOS transistors (MN7, MN9).



Data supplied from the ***esp@cenet*** database — Worldwide

Petitioner Micron Ex-1004, 0048

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03F 3/45, G05F 3/16 — A1

(11) International Publication Number: **WO 97/05696**

(43) International Publication Date: 13 February 1997 (13.02.97)

(21) International Application Number: PCT/US96/12238

(22) International Filing Date: 24 July 1996 (24.07.96)

(30) Priority Data:
08/509,982 1 August 1995 (01.08.95) US

(71) Applicant: INFORMATION STORAGE DEVICES, INC. [US/US]; 2045 Hamilton Avenue, San Jose, CA 95125 (US).

(72) Inventor: TRAN, Hieu, Van; 2741 Coltwood Drive, San Jose, CA 95148 (US).

(74) Agents: BLAKELY, Roger, W., Jr. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

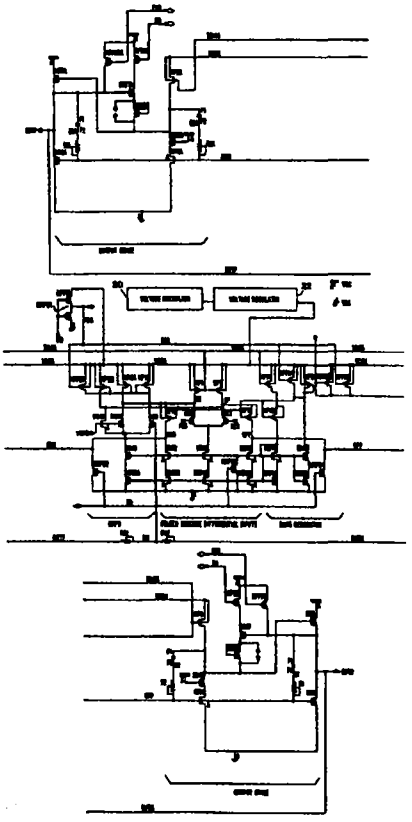
(81) Designated States: AL, AM, AT, AT (Utility model), AU, AZ, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IL, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TR, TT, UA, UG, UZ, VN, ARIPO patent (KE, LS, MW, SD, SZ, UG), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG).

Published
With international search report.
With amended claims.

(54) Title: FULLY DIFFERENTIAL OUTPUT CMOS POWER AMPLIFIER

(57) Abstract

A fully differential output CMOS power amplifier suitable to be used in a non-volatile memory mixed mode chip for voice record and playback to drive a very low impedance load such as an 8-ohm speaker from a low voltage supply. This fully differential CMOS power amplifier utilizes a voltage multiplying technique for the input stage (MN2, MN3, MP6, MP7), a level shift/gain stage (MN/P12, MN/P13), and a common mode feedback network (MN1, MN10, MP10). It also utilizes native n-MOS having a threshold voltage VT = 0v for the folded cascode differential input and the source follower output stage (MN7), enhancement n-MOS (VT = 0.7v) for the common source output, and a voltage regulator (22) using p-MOS diode connected devices (M1-M5) for simulating a resistor divider to regulate the voltage multiplier output. The amplifier also includes a mechanism for crossover distortion reduction at the output driver stage, and a scheme to set the idle current in the output driver n-MOS transistors (MN7, MN9).



Petitioner Micron Ex-1004, 0049

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AM	Armenia	**GB**	United Kingdom	**MW**	Malawi
AT	Austria	**GE**	Georgia	**MX**	Mexico
AU	Australia	**GN**	Guinea	**NE**	Niger
BB	Barbados	**GR**	Greece	**NL**	Netherlands
BE	Belgium	**HU**	Hungary	**NO**	Norway
BF	Burkina Faso	**IE**	Ireland	**NZ**	New Zealand
BG	Bulgaria	**IT**	Italy	**PL**	Poland
BJ	Benin	**JP**	Japan	**PT**	Portugal
BR	Brazil	**KE**	Kenya	**RO**	Romania
BY	Belarus	**KG**	Kyrgystan	**RU**	Russian Federation
CA	Canada	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CF	Central African Republic			**SE**	Sweden
CG	Congo	**KR**	Republic of Korea	**SG**	Singapore
CH	Switzerland	**KZ**	Kazakhstan	**SI**	Slovenia
CI	Côte d'Ivoire	**LI**	Liechtenstein	**SK**	Slovakia
CM	Cameroon	**LK**	Sri Lanka	**SN**	Senegal
CN	China	**LR**	Liberia	**SZ**	Swaziland
CS	Czechoslovakia	**LT**	Lithuania	**TD**	Chad
CZ	Czech Republic	**LU**	Luxembourg	**TG**	Togo
DE	Germany	**LV**	Latvia	**TJ**	Tajikistan
DK	Denmark	**MC**	Monaco	**TT**	Trinidad and Tobago
EE	Estonia	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**UG**	Uganda
FI	Finland	**ML**	Mali	**US**	United States of America
FR	France	**MN**	Mongolia	**UZ**	Uzbekistan
GA	Gabon	**MR**	Mauritania	**VN**	Viet Nam

Petitioner Micron Ex-1004, 0050

FULLY DIFFERENTIAL OUTPUT CMOS POWER AMPLIFIER

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to the field of analog CMOS integrated circuit design, and specifically to integrated operational amplifiers driving low impedance loads.

2. Prior Art

A fully differential output operational amplifier is normally superior to a single ended output operational amplifier in terms of power supply noise rejection and noise coupling rejection, since the power supply variation or any noise source couples equally to both output branches at the same time and thus appears as a common mode signal not effecting the differential output of the operational amplifier. This is especially important for a mixed mode chip (integrated circuit having both analog and digital circuits on the same substrate), where the noise is generated from the switching of the digital circuits.

In the prior art, fully differential output CMOS power amplifiers are implemented using typically a two (or sometimes more) stage operational amplifier which are powered from the normal system power supply VCC. The typical two stage operational amplifier consists of a mostly differential voltage amplifying input stage for

Petitioner Micron Ex-1004, 0051

noise and offset considerations, and a current gain and/or MOS output driver stage for driving a low impedance load. These two stages both get their power from VCC. Such CMOS operational amplifiers are difficult to operate from a low voltage power supply for driving low impedance loads, such as an 8 ohm speaker, since the gate driving ability of the MOS output stage is so limited. The limited gate drive could be made up in substantial part by increasing the size of the output devices, but this could make the MOS driver prohibitively large.

Conventional enhancement mode n-MOS input stages for low voltage operation also suffer from minimum input common mode range, since the input voltage has to be at least larger than the VT (threshold voltage) of the input n-MOS. Also, conventional enhancement mode n-MOS source follower output drivers suffer from a limited swing on the output voltage in the positive direction because of the VT drop from the gate to source.

BRIEF SUMMARY OF THE INVENTION

A fully differential output CMOS power amplifier utilizing a voltage multiplying technique to provide a regulated power supply higher than the system power supply to a folded differential input stage, the bias generator, the common mode feedback circuit, and the gain/level shift stage. This allows the analog gate voltages of the output transistors to go much higher than the normal power supply, resulting in significantly reduced required size of the output transistors. Since the pump is mainly to provide for the gate voltages which require little current, it is small. In a preferred embodiment, this CMOS power amplifier is used

Petitioner Micron Ex-1004, 0052

in a mixed mode chip which already has a voltage multiplier for the on-chip memory circuit, and therefore can readily use the on-chip pump without adding another pump circuit. This power amplifier also includes a voltage regulator to regulate the multiplied voltage to a fixed level to reduce power supply variation and noise from the oscillator of the voltage multiplier.

The voltage regulator is configured in a negative feedback operational amplifier loop with diode connected p-MOS devices serving as a resistor divider to reduce the current loading to the voltage multiplier. Each diode connected p-MOS has its own well tied to its source so the VGS (gate to source voltage) of each p-MOS is precisely mirrored across the diode chain by the negative feedback action. This gives a precise voltage at the output of the regulator, in the preferred embodiment of the invention, 5 times VREF.

This fully differential output CMOS power amplifier also includes a folded cascode differential input stage utilizing native n-MOS (VT ≈ Ov) to give a near rail to rail input common mode range, a native n-MOS (VT ≈ Ov) source follower on the output stage to give a high swing voltage output, an enhancement mode n-MOS common source output stage, a mechanism for reducing crossover distortion of the output driver stage, and a scheme to set the idle current in the output drivers when the input signal is zero.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a circuit diagram for the preferred embodiment of the fully differential CMOS power amplifier of the present invention, comprising Figures

Petitioner Micron Ex-1004, 0053

1A and 1C, each showing one of the differential output stages, and Figure 1B showing among other things the folded cascode differential input stage and the bias generator.

Figure 2 is a circuit diagram for the voltage regulator used in the circuit of Figure 1.

DETAILED DESCRIPTION OF THE INVENTION

Figure 1 is a circuit diagram for the preferred embodiment of the fully differential CMOS power amplifier of the present invention, using a folded cascode input stage and n-MOS transistors for the output drivers.

The preferred embodiment of the present invention is intended to be used as the output power amplifier on an integrated circuit analog signal recording and playback system such as disclosed in U.S. Patents 4,890,259, 4,989,179, 5,220,531, 5,126,967, 5,241494 and 5,164,915. Such integrated circuits already include a MOS charge pump voltage multiplier (the voltage multiplier 20 of Figure 1) for other purposes, namely to provide the required high voltages for the erase and program functions for the on-chip floating gate storage cells from a single, relatively low voltage power supply to the chip, such a low voltage battery power supply providing VCC, and VSS, shown also as ground potential. MOS charge pump voltage multipliers are well known in the art, and need not be further described herein.

Also shown in Figure 1 is a voltage regulator 22, used to regulate the multiplied voltage to reduce the voltage variation and noise coupled to the power amplifier from the charge pump, which typically has a

Petitioner Micron Ex-1004, 0054

ripple voltage on its output. The ripple period depends on the period of the pump clock generator. The ripple magnitude depends on the pumping capacitors, the magnitude of the pumping clock waveform (typically equal to VCC), the output loading current and the output loading capacitance. Even though this ripple is reduced by the power supply rejection capability of the power amplifier, it is still significant, so the voltage regulator 22 is used to reduce the ripple seen by the power amplifier. This is especially important in the idle state (when the input signal is zero), as the ripple will appear on the output as an idle noise which limits the signal to noise ratio of the power amplifier.

The fully differential output CMOS power amplifier includes a differential stage, a gain stage, common mode feedback and a bias generator, all of which get their power from the output of the voltage regulator, VCCM, a voltage significantly higher than VCC. The output stage, the only stage requiring substantial power, gets its power from the normal system power supply VCC.

The preferred embodiment of the present invention shown in Figure 1 is intended to operate as part of an integrated circuit responsive to a power down signal to power down the circuit whenever the PD (power down) signal goes high. As the subsequent description will illustrate, the following notation is used in Figures 1 and 2 herein:

p-channel devices are so indicated by the circle in the gate contact, and further by the P appearing as the second letter of the device designation

n-channel devices are so indicated by the absence of a circle in the gate contact, and

Petitioner Micron Ex-1004, 0055

further by the N appearing as the second letter of the device designation

native devices are indicated by the thickened line parallel to the gate and by the letter A adjacent thereto

most devices associated with the power down function are so indicated by "PD" appearing as the third and fourth letter designations of the respective devices

In the circuit of Figure 1, n-channel device MNPD1 and p-channel device MPPD1 are used to invert the PD (power down) signal to provide the signal PDB (PD bar or $\overline{PD}$). Device MPPD1 is connected to VCCM instead of VCC so that PDB is VCCM when PD is zero. Thus when the circuit is enabled (PD = Ov), PDB will be equal to VCCM, completely shutting off p-channel devices MPPD2/3/4/5/5A. At the same time, PD = Ov (PD = VSS) will also completely shut off n-channel devices MNPD2/3/4. As shall subsequently be described in further detail, devices MPPD2/3/4/5/5A and MNPD2/3/4 will be turned on when PD goes high to cut off all current paths in the circuit.

Current IBIAS to the circuit is a controlled current source (actually a current sink, though the phrase current source may be used generically hereafter for source or sink, as will be obvious to one skilled in the art) mirrored from a bias current generator elsewhere in the integrated circuit, as is well known in the art. This sets the gate-source voltage of transistor MBIAS1, the input bias reference p-MOS device, to provide the basic current mirror for biases of other p-channel devices, namely devices

Petitioner Micron Ex-1004, 0056

MP6/7/8/8A/14, each therefore acting as a bias current source for various other parts of the circuit.

The bias current through p-channel device MP14 also flows through p-channel device MP13B and n-channel devices MN14, MN14A to provide biases for n-MOS current mirrors formed by n-channel devices MN11/MN11A, MN12/MN12A, MN13/MN13A of the folded cascode differential input stage, and also to provide biases for n-channel devices MN10/MN10A of the common mode feedback network. It also provides a bias for n-channel devices MN15/MN15A connected in series with diode connected p-channel device MP15 to generate a p-MOS bias for the gates of p-channel devices MP12, MP13 of the folded cascode differential input stage. p-channel device MP13B is used to force the drain-source voltage of p-channel device MP14 to be close to the drain-source voltage of p-channel devices MP7 and MP6 for more precise current matching between p-channel device MP7 and n-channel devices MN13/MN13A and between p-channel device MP6 and n-channel devices MN12/MN12A (since n-channel devices MN13/MN13A and MN12/MN12A are mirrored from n-channel device MN14, which is sinking the bias current from p-channel devices MP14).

The n-MOS cascode current mirror formed by n-channel devices MN14/MN14A uses a native (VT ≈ Ov) n-MOS device MN14 in series with enhancement mode n-MOS device MN14A to minimize the headroom voltage, since the bias voltage is only one gate-source voltage of the enhancement mode n-MOS device MN14A (this is in comparison with the normal two diode connected n-MOS transistors in series, which requires the sum of 2 gate-source voltages of headroom voltage). n-channel device MN14A is in saturation, since its drain voltage is close to its gate voltage. n-channel device MN14 is also in

Petitioner Micron Ex-1004, 0057

saturation since its threshold voltage is a few hundred millivolts because of the body effect. Hence, the cascoding effect is achieved with lower headroom voltage by using a native device connected in series with an enhancement n-MOS device. The native n-MOS device has its drain and gate tied together. The other n-MOS device mirrors the current to n-channel devices MN10/MN10A, MN11/MN11A, MN12/MN12A, MN13/MN13A, and MN15/MN15A, which use the same scheme.

n-channel devices MN15/MN15A mirror the current from n-channel devices MN14/MN14A to p-channel device MP15 to generate the bias for the common gate connection of p-channel devices MP12 and MP13. p-channel device MP15 is sized such that the source voltages of p-channel devices MP12 and MP13 sit close to VCCM (only one drain-source saturation voltage of p-channel devices MP6 and MP7 away from VCCM) for maximum swing on the nodes OP, ON and hence on nodes OPP, ONN to optimize the size of n-channel device MN9 and MN9A.

n-channel devices MN2/MN3, p-channel devices MP6/MP7 and MP12/MP13, and n-channel devices MN12/MN12A, MN11/MN11A and MN13/MN13A constitute a folded differential native n-MOS input stage. The native n-MOS devices MN2 and MN3 are chosen for the input n-MOS pair to increase the minimum input voltage range by one enhancement mode threshold voltage and thus lower the minimum voltage input close to ground. The outputs of the folded cascode input stage on nodes OPP and ONN are differential, and are each applied to a respective single ended n-MOS output stage. In particular, when the differential inputs POS and NEG are applied to the differential input n-channel pair MN2 and MN3, the differential outputs of nodes ON and OP respond in opposite directions, in turn causing nodes ONN and OPP

Petitioner Micron Ex-1004, 0058

to follow the voltage variations of nodes ON and OP, respectively, through the common gate connected p-MOS devices MP12 and MP13. The voltages on nodes ONN and OPP are thus applied differentially to the two identical n-MOS output stages.

n-channel devices MN4, MN16, p-channel device MP8, n-channel devices MN7, MN9, p-channel device MP20, n-channel devices MN17, MN18, p-channel device MPPD5, resistor R2, capacitor C2, resistor R1 and capacitor C1 constitute an n-MOS output stage. The second identical n-MOS output stage is formed by corresponding devices having the same designations followed by the letter "A", and accordingly the description to follow is also directly applicable, though being responsive to the opposite node ONN, the opposite voltage of the differential voltages on nodes ONN, OPP. In each output stage, the capacitor is realized on-chip in integrated circuit form using techniques well known in MOS integrated circuits and MOS integrated circuit formation.

p-channel device MPPD5 is part of the shutdown circuit, and is held off (PDB high) when the circuit is not powered down (PD low). p-channel device MP20 is also related to the power down function, and is held on by PD when the circuit is not powered down. n-channel device MN7 is used in a source follower mode, and is a native n-MOS to increase the high swing by one enhancement mode threshold voltage to make the high end output OUTN swing of the output stage close to the power supply voltage VCC. n-channel devices MN4, MN16, p-channel device MP8, resistor R2, and capacitor C2 provide gain/level shift for the source follower MN7, with resistor R2 and capacitor C2 providing a compensation network for the gain/level network.

Petitioner Micron Ex-1004, 0059

Resistor R1 and capacitor C1 provide a compensation network for the final gain output stage comprising n-channel device MN9.

The output stage described above operates as follows: Assuming the signal on node OPP goes lower, n-channel device MN9 is gradually turned off, and n-channel device MN4 is also gradually turned off. p-channel device MP8 pulls the gate of n-channel device MN7 toward VCCM, and device MN7 in turn pulls the output OUTN toward VCC. Conversely, as the voltage on node OPP goes higher, n-channel device MN9 is gradually turned on, pulling the output OUTN lower. n-channel device MN4 is also gradually turned on harder, pulling the gate of n-channel device MN7 toward ground, tending to turn off device MN7 to release OUTN from the pull up effects of device MN7. Thus the output stage acts as an inverting stage.

n-channel devices MN17 and MN18 are to reduce the crossover distortion. At the mid point (analog ground, e.g. 1.5V, or zero differential input to the system), as the voltage on node OPP goes from low to high, n-channel device MN4 is turned on, pulling the gate of n-channel device MN7 too quickly toward ground, shutting n-channel device MN7 off completely. In the meantime, n-channel device MN9 is not yet turned on, so the output OUTN is floating for a short period until n-channel device MN9 is turned on. This causes distortion. To prevent this, the voltage on the gate of n-channel device MN7 is lowered slowly to turn off device MN7 slowly by a local feedback path from the output OUTN to the gate of n-channel device MN17, which does not allow the gate of n-channel device MN7 to fall too rapidly. n-channel device MN16 acts as a resistive path to further slow down the falling of the gate of n-channel device MN7.

Petitioner Micron Ex-1004, 0060

By not allowing the gate of device MN7 to fall before device MN9 is turned on, a direct current path is created between VCC and VSS through devices MN7 and MN9 for a short period. This is the familiar tradeoff between reducing crossover distortion and increasing the direct current consumption. In that regard, n-channel device MN18, as an option, may be shorted for reducing further the crossover distortion at the expense of increasing the direct current consumption.

The idle current in the output stage (when there is no differential signal) is precisely set by the size ratio of n-channel devices MN9 to MN4 (and the bias current in n-channel device MN4, which is set by the current mirrored to p-channel device MP8). Note that the gate voltages of n-channel devices MN9 and MN4 are the same and the drain voltage of n-channel device MN9 is almost the same as the drain voltage of n-channel device MN4 by the action of source follower native n-MOS device MN7. Also because the gate of the n-channel device is allowed to swing higher than the normal power supply voltage VCC, allowing the use of a much smaller device for n-channel device MN9 (better matching between devices MN9 and MN4 because they are closer together physically), this allows the idle current to be controlled much better.

As stated before, n-channel devices MN4A, MN16A, p-channel device MP8A, n-channel device MN7A, MN9A, p-channel device MP20A, n-channel devices MN17A, MN18A, p-channel device MPPD5A, resistor R2A, capacitor C2A, resistor R1A and capacitor C1A constitute another exact replica of the above n-MOS output stage. This output branch receives its input from the ONN signal, which is differentially is always in the opposite direction to the OPP signal by the action of the input stage. Thus

Petitioner Micron Ex-1004, 0061

the output OUTP always swings in the opposite direction of the output OUTN.

The outputs OUTP and OUTN are normally connected across a speaker for driving differentially to increase the power output by four times (since the voltage swing across the speaker is doubled) as compared to a single ended power amplifier. Normally the power amplifier is used in a unity gain mode, in which case OUTP of the respective output stage is also connected to NEG input of the differential input stage.

Resistors RX1 and RX2 are common mode feedback resistors connected between the differential outputs. Their resistances are high to prevent excessive loading. The resistor network is used to sense the common mode voltage on the inputs of the power amplifier and to feed back the common mode voltage to a common mode feedback amplifier for common mode voltage correction.

n-channel devices MN1/MN1A/MN1B, p-channel devices MP10/MP10A/MP10B and n-channel devices MN10/MN10A constitute the common mode feedback amplifier. It is a conventional MOS differential amplifier with the native n-MOS transistors as the input n-MOS pair. The native n-MOS is used to increase the input voltage range as in the folded cascode input pair. The common mode input VCMD is the analog ground level (the mid point, e.g. 1.5V in the preferred embodiment). Assuming the average of the differential outputs OUTN and OUTP is somehow higher than normal, the voltage of node CM at the resistive network junction will be higher than VCMD, causing n-channel device MN1 to turn on harder, pulling the gate of p-channel device MP10 lower, which turns p-channel devices MP10A and MP10B on harder and pulls the node OP and ON higher respectively, in turn pulling both nodes ONN and OPP higher by the common gate connected p-

Petitioner Micron Ex-1004, 0062

channel devices MP12, MP13. With the voltages of nodes ONN and OPP higher, the voltages of both nodes OUTN and OUTP go lower (the output stages of the amplifier are inverting stages), restoring the common mode voltage in the output nodes OUTN and OUTP. As the differential output OUTN and OUTP swing in the opposite direction, opposite action happens.

The folded differential input stage obtains its power from the regulated pumped output VCCM, which allows nodes ON and OP to be biased one saturation drain-source voltage VDS_{sat} from VCCM (VCCM - $VDS_{MP6/7sat}$). This also means the voltages of nodes OPP and ONN can swing to two saturation VDSs from VCCM (VCCM - $VDS_{MP6/7sat}$ - $VDS_{MP12/13sat}$), which allows the size of n-channel devices MN9/MN9A to be small devices, even though n-channel devices MN9/MN9A have to sink a relatively huge current from the low impedance load. The level shift/gain stages (n-channel devices MN4, MN16, p-channel device MP8, resistor R2 and capacitor C2, and n-channel devices MN4A, MN16A, p-channel device MP8A, resistor R2A and capacitor C2A) get their power supply from VCCM, which allows the gate of n-channel devices MN7/MN7A to swing close to VCCM. This allows n-channel devices MN7/MN7A to be also to be small, even though n-channel devices MN7/MN7A have to source a relatively huge current to the low impedance load. The common mode feedback circuit and the bias generator also get their power supply from VCCM for proper operation.

As stated before, when the circuit is enabled (PD = Ov), PDB will be equal to VCCM, completely shutting off p-channel devices MPPD2/3/4/5/5A. At the same time, PD = Ov (PD = VSS) will also completely shut off n-channel devices MNPD2/3/4. However when PD goes high for power down, n-channel devices MNPD2/3/4 PDB will be turned on,

Petitioner Micron Ex-1004, 0063

and PDB will go low, turning on p-channel devices MPPD2/3/4/5/5A. This shuts down the various bias current sources in the amplifier and cuts off all current paths in the circuit. The turning on of p-channel devices MPPD5/5A on power down clamps the voltage of output nodes OUTN and OUTP at VCC, thereby holding the differential output at zero. Also on power down, p-channel devices MP20/20A are turned off to cut off the current path from VCC to VCCM through n-channel devices MN17/17A, MN18/18A and p-channel devices MP8/8A.

Figure 2 is a circuit diagram for the voltage regulator 22 used in the circuit of Figure 1. As shown in Figure 2, an operational amplifier I1 is configured in a negative feedback loop to regulate the multiplied voltage VCCMP to a fixed level VCCM based on an input reference voltage VREF to reduce the coupling of power supply variations and noise to the power amplifier. The operational amplifier I1 used in the preferred embodiment is a conventional two stage operational amplifier. p-channel devices M1/M2/M3/M4/M5, when p-channel device M5 is on, are a series of diode connected devices, and each have their sources connected to their own well to eliminate body effect) to simulate a resistor divider of larger value resistors to reduce current loading to the voltage multiplier. In this way, p-channel devices M1/M2/M3/M4/M5 are small as compared to the large area that would be needed to realize large value resistors on-chip. In this Figure, n-channel devices MPD2 and M8 are used for power down purposes. In normal operation (PD low), n-channel device MPD2 and M8 will be off. This will hold P-channel device M5 on, activating the simulated resistor divider to feed back one fifth of the regulated voltage VCCM to the negative input of the operational amplifier. On power down when PD goes high, n-channel devices MPD2 and M8 will be

Petitioner Micron Ex-1004, 0064

turned on. n-channel devices M7/M8 are used to keep VCCM close to VCC during power down. This holds the negative input to the operational amplifier I1 high, and N-channel device MPD2 being on pull the voltage on node VCCMR to ground, turning off N-channel device M6 to decouple the output VCCM and the resistor divider from the voltage multiplier.

Thus the regulator output VCCM is regulated precisely by the negative feedback action of the operational amplifier at 5 times the reference voltage VREF, which is also 5 times the gate-source voltage of each of the p-channel devices M1/M2/M3/M4/M5 for the current flowing there through at the regulated voltage. As can be seen from the Figure, n-channel devices M6, M8 are native n-MOS devices. n-channel device M8 is to precharge the output node VCCM close to VCC, and n-channel device M7 is to keep VCCM within one threshold voltage of VCC on startup until the charge pump output VCCMP is high enough.

There has been described herein a fully differential output CMOS power amplifier that uses small output transistors for driving a low impedance load such as an 8 ohm speaker at low power supply voltages such as 2.5 volts by utilizing a stepped up voltage for a folded cascode differential input with native n-MOS devices, for the level shift/gain stage, for the common feedback network, and for the bias generator. The fully differential output CMOS power amplifier has a folded cascode differential input stage that uses native n-MOS for near rail-to-rail common mode input range, an output stage that uses native n-MOS devices in a source follower configuration for high swing efficiency, and a local feedback mechanism for reducing crossover distortion for the n-MOS output stage. A voltage

Petitioner Micron Ex-1004, 0065

regulator is provided for the stepped up voltage that uses very little current without requiring large value resistors by utilizing diode connected p-MOS transistors as a resistor divider. The n-MOS device output stage includes circuitry that accurately sets the idle current by utilizing a source follower native n-MOS to force the drain voltage of the output driver n-MOS to be almost the same as the drain voltage of a reference n-MOS device. However while a preferred embodiment of the present invention have been disclosed and described herein, it will be obvious to those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.

Petitioner Micron Ex-1004, 0066

What is claimed is:

1. A differential output CMOS power amplifier for low voltage operation comprising:

a folded cascode differential input stage having native n-MOS devices forming the differential input;

a level shift and gain stage coupled to the differential input stage;

a pair of power output stages coupled to the level shift and gain stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier;

a bias generator for providing bias currents to the folded cascode differential input stage, the level shift and gain stage, and the pair of power output stages;

the pair of power output stages having input power terminals for coupling to a low voltage power supply;

the bias generator, the folded cascode differential input stage and the level shift and gain stage having terminals for coupling to a voltage substantially higher than the low voltage power supply.

2. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have a n-MOS device connected as a source follower.

Petitioner Micron Ex-1004, 0067

3. The differential output CMOS power amplifier of claim 2 wherein the pair of power output stages each have local feedback for reducing crossover distortion.

4. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have as an output driver a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

5. The differential output CMOS power amplifier of claim 4 wherein the pair of power output stages each have a reference source follower native n-MOS device coupled to set the idle current for the output stage by forcing the drain voltage of the output driver to approximately equal the drain voltage of the reference source follower native n-MOS device.

6. The differential output CMOS power amplifier of claim 1 further comprised of a common mode voltage feedback circuit coupled to the output terminals for feeding the common mode output voltage back to the differential input stage.

7. The differential output CMOS power amplifier of claim 6 wherein the common mode voltage feedback circuit is for coupling to a voltage substantially higher than the low voltage power supply.

Petitioner Micron Ex-1004, 0068

8. The differential output CMOS power amplifier of any one of claims 1, 6 or 7 further comprised of a voltage multiplier for coupling to a low voltage power supply and for providing the voltage substantially higher than the low voltage power supply.

9. The differential output CMOS power amplifier of claim 8 further comprised of a voltage regulator coupled to the voltage multiplier to regulate the voltage substantially higher than the low voltage power supply irrespective of variations in the output voltage of the voltage multiplier.

10. The differential output CMOS power amplifier of claim 9 wherein the voltage regulator comprises:

a plurality of diode connected p-MOS devices connected in series;

a first power supply connection connected to one end of the series connected p-MOS devices;

a regulator output connection connected to the second end of the series connected p-MOS devices;

a second power supply connection;

a transistor coupled between the second power supply connection and the output connection; and,

an amplifier coupled to the transistor for controlling the current flow from the second power supply connection through the transistor responsive to the difference between the voltage across one on the series connected p-MOS devices and a reference voltage.

Petitioner Micron Ex-1004, 0069

11. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage with native n-MOS devices forming the differential input; and,

a pair of power output stages coupled to the folded cascode differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier, the output stages each having a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

12. The differential output CMOS power amplifier of claim 11 wherein the pair of power output stages are for coupling to a low voltage power supply, and the differential input stage is for coupling to a voltage substantially higher than the low voltage power supply.

13. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage having native n-MOS devices as the input devices for near rail-to-rail common mode input range;

a level shift and gain stage coupled to the differential input stage; and,

a pair of power output stages coupled to the differential input stage, each power output stage having

Petitioner Micron Ex-1004, 0070

an output terminal forming one of the differential outputs of the CMOS power amplifier.

14. The differential output CMOS power amplifier of claim 13 wherein the differential input stage is a folded cascode differential input stage with native n-MOS devices forming the differential input.

15. The differential output CMOS power amplifier of either claim 13 or claim 14 wherein the pair of power output stages are for coupling to a low voltage power supply, and the differential input stage is for coupling to a voltage substantially higher than the low voltage power supply.

16. A voltage regulator comprising:

a plurality of diode connected p-MOS devices connected in series;

a first power supply connection connected to one end of the series connected p-MOS devices;

a regulator output connection connected to the second end of the series connected p-MOS devices;

a second power supply connection;

a transistor coupled between the second power supply connection and the output connection; and,

an amplifier coupled to the transistor for controlling the current flow from the second power supply connection through the transistor responsive to

Petitioner Micron Ex-1004, 0071

the difference between the voltage across one on the series connected p-MOS devices and a reference voltage.

Petitioner Micron Ex-1004, 0072

AMENDED CLAIMS

[received by the International Bureau on 12 December 1996 (12.12.96); original claims 1-16 replaced by amended claims 1-12 (4 pages)]

1. A differential output CMOS power amplifier for low voltage operation comprising:

a folded cascode differential input stage having native n-MOS devices forming the differential input;

a level shift and gain stage coupled to the differential input stage;

a pair of power output stages coupled to the level shift and gain stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier;

a bias generator for providing bias currents to the folded cascode differential input stage, the level shift and gain stage, and the pair of power output stages;

the pair of power output stages having input power terminals for coupling to a low voltage power supply;

the bias generator, the folded cascode differential input stage and the level shift and gain stage having terminals for coupling to a voltage substantially higher than the low voltage power supply.

2. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have a n-MOS device connected as a source follower.

Petitioner Micron Ex-1004, 0073

3. The differential output CMOS power amplifier of claim 2 wherein the pair of power output stages each have local feedback for reducing crossover distortion.

4. The differential output CMOS power amplifier of claim 1 wherein the pair of power output stages each have as an output driver a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

5. The differential output CMOS power amplifier of claim 4 wherein the pair of power output stages each have a reference source follower native n-MOS device coupled to set the idle current for the output stage by forcing the drain voltage of the output driver to approximately equal the drain voltage of the reference source follower native n-MOS device.

6. The differential output CMOS power amplifier of claim 1 further comprised of a common mode voltage feedback circuit coupled to the output terminals for feeding the common mode output voltage back to the differential input stage.

7. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage with native n-MOS devices forming the differential input; and,

Petitioner Micron Ex-1004, 0074

a pair of power output stages coupled to the folded cascode differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier, the output stages each having a native n-MOS device connected as a source follower to provide a high output voltage swing efficiency.

8. A differential output CMOS power amplifier comprising:

a folded cascode differential input stage having native n-MOS devices as the input devices for near rail-to-rail common mode input range;

a level shift and gain stage coupled to the differential input stage; and,

a pair of power output stages coupled to the differential input stage, each power output stage having an output terminal forming one of the differential outputs of the CMOS power amplifier.

9. The differential output CMOS power amplifier of claim 8 wherein the differential input stage is a folded cascode differential input stage with native n-MOS devices forming the differential input.

10. The differential output CMOS power amplifier of claim 9 wherein the pair of power output stages each have a native n-MOS device connected as a source follower.

AMENDED SHEET (ARTICLE 19)

Petitioner Micron Ex-1004, 0075

11. A voltage regulator for receiving a voltage input and providing a regulated voltage output comprising:

a plurality of transistors connected in series, the first of the series of transistors being diode coupled when active, the rest of the series of transistors being diode coupled, the series of transistors having a first end thereof coupled to a circuit ground and a second end thereof coupled to the regulator output;

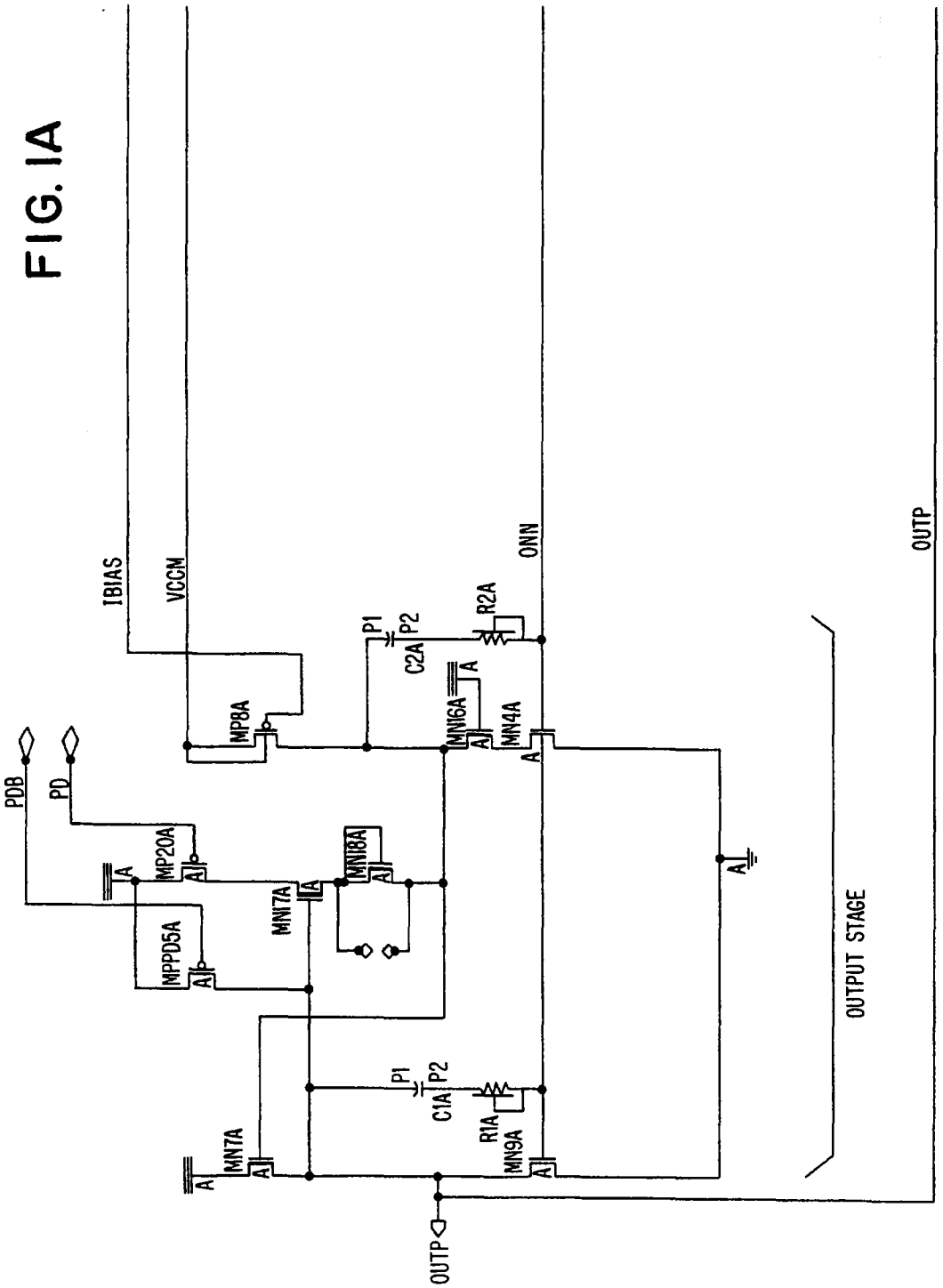
a differential amplifier having an amplifier output, a first input coupled to the connection between two of the series of diode connected transistors, and a second input coupled to a reference voltage; and,

a regulating transistor coupled between the voltage input and the first end of the series of diode connected transistors and controlled by the amplifier output to provide a current through the series of diode connected transistors to maintain the voltage between the inputs of the differential amplifier substantially equal.

12. The voltage regulator of claim 11 wherein the transistors are MOS transistors, each having a source, a gate, and a drain.

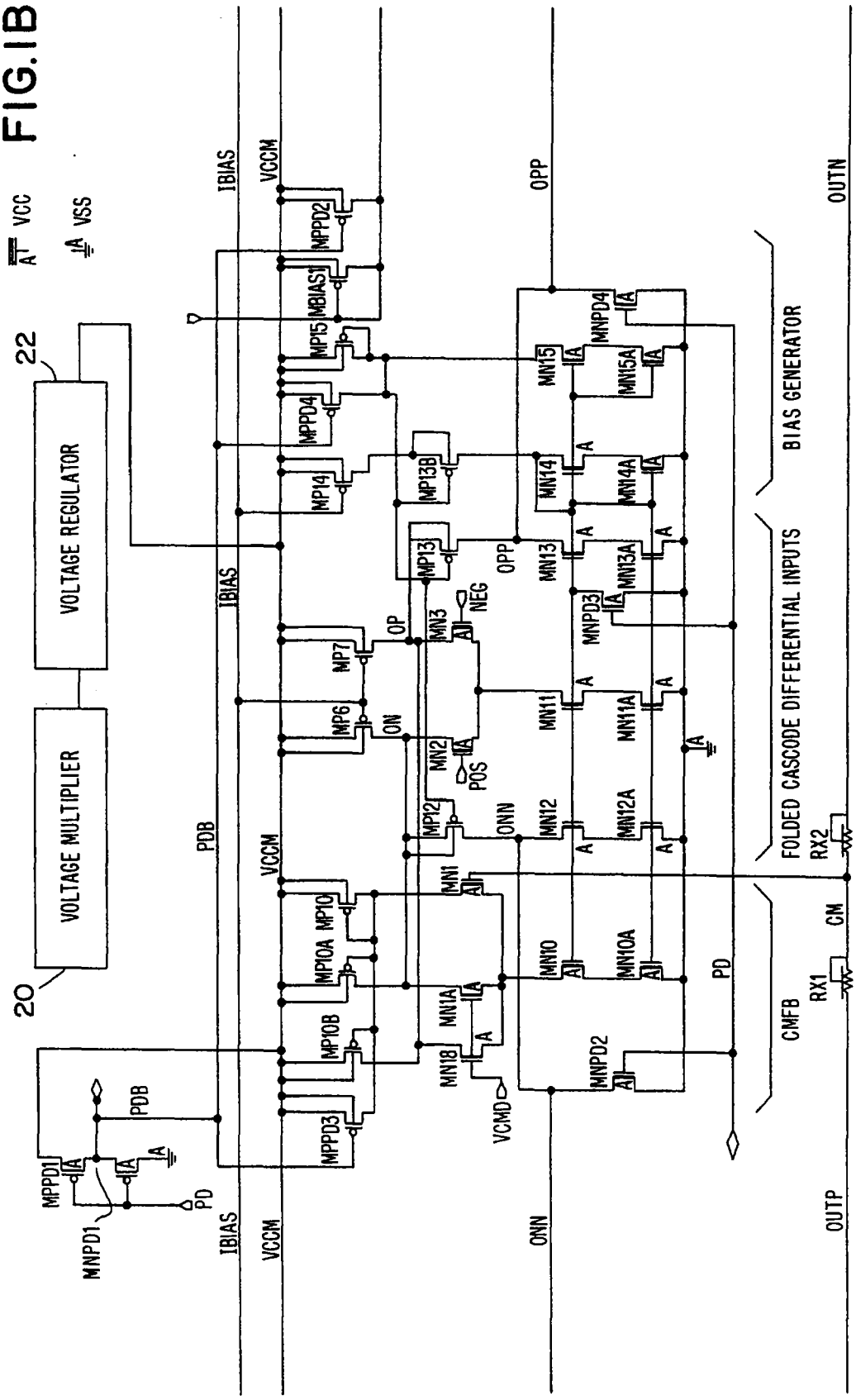
Petitioner Micron Ex-1004, 0076

FIG. IA



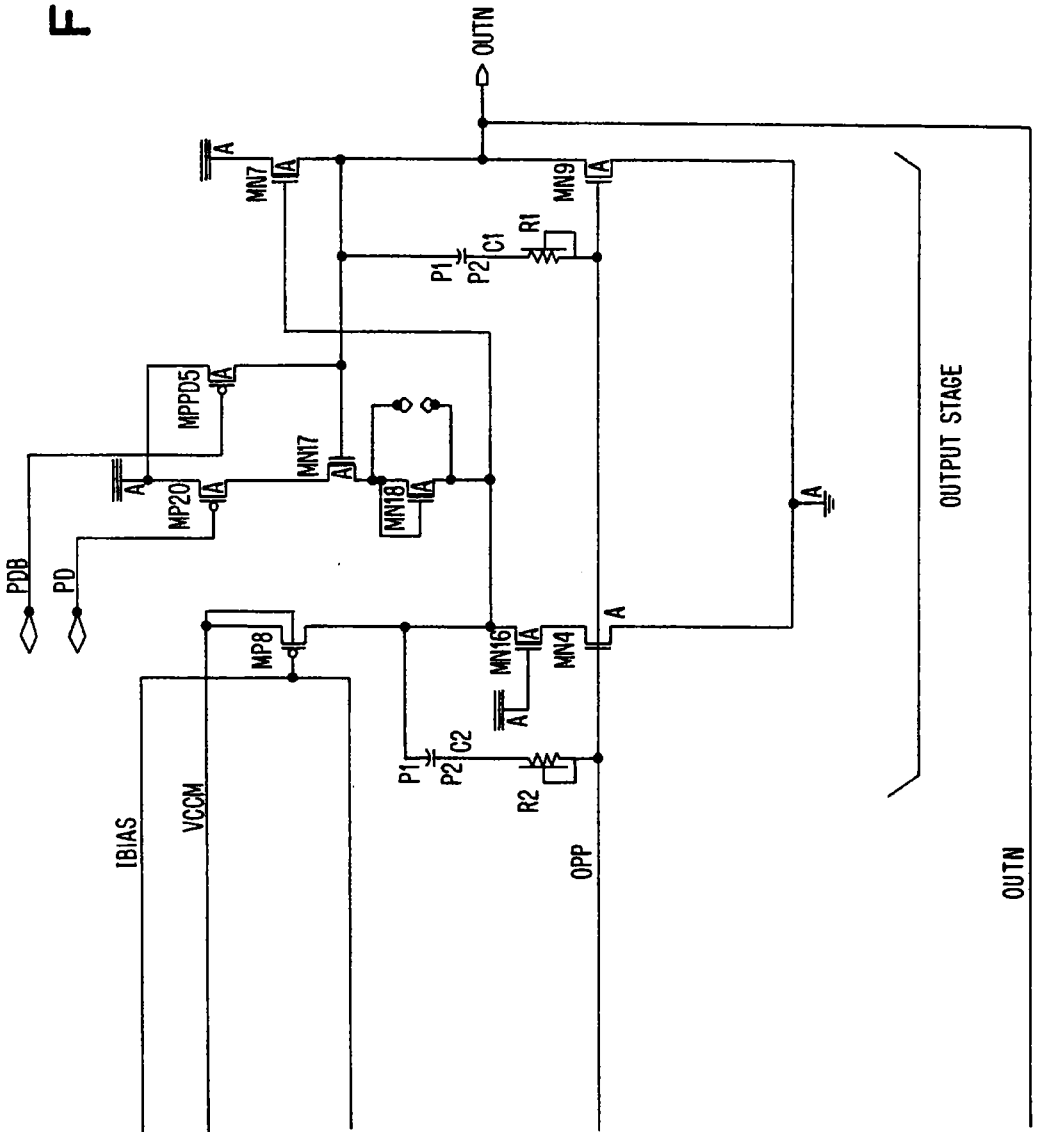
Petitioner Micron Ex-1004, 0077

FIG.1B



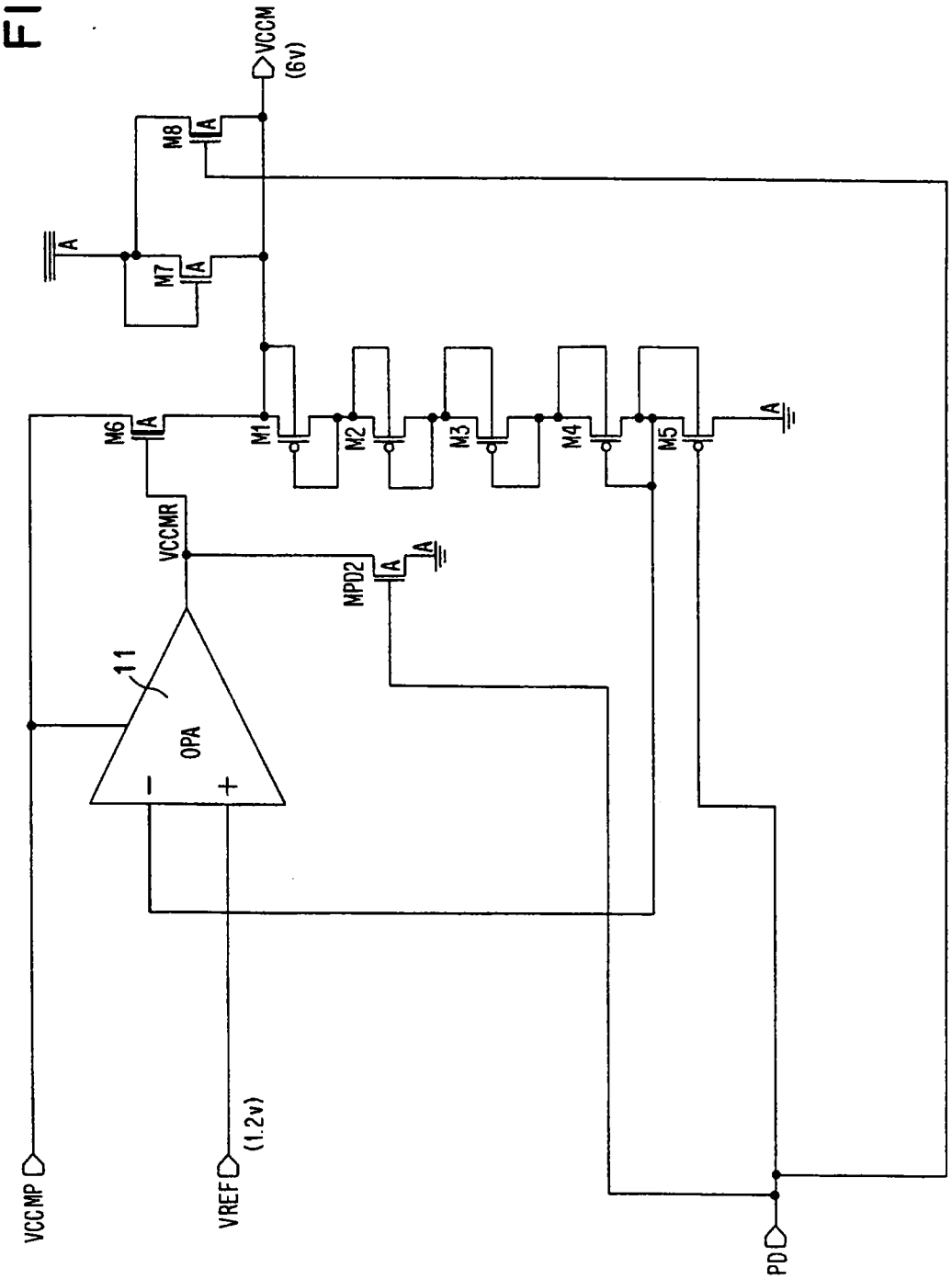
Petitioner Micron Ex-1004, 0078

FIG. IC



Petitioner Micron Ex-1004, 0079

FIG. 2



Petitioner Micron Ex-1004, 0080

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :HO3F 3/45; G05F 3/16
US CL :330/253, 255; 323/313
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 330/253, 255,258,261; 323/313

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,797,631 (HSU et al.) 10 January 1989, see the figure and col. 2,lines 5-7.	13-15
Y	US,A, 5,212,455 (Pernici et al.) 18 May 1993, see fig. 1.	13-15
X	US, A, 5,434,498 (Cordoba et al.) 18 July 1995, see fig. 1.	16

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

*	Special categories of cited documents:	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"A"	document defining the general state of the art which is not considered to be of particular relevance	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"E"	earlier document published on or after the international filing date	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"&"	document member of the same patent family
"O"	document referring to an oral disclosure, use, exhibition or other means		
"P"	document published prior to the international filing date but later than the priority date claimed		

Date of the actual completion of the international search 03 OCTOBER 1996	Date of mailing of the international search report 16 OCT 1996
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703) 305-3230	Authorized officer Steven Mottola Telephone No. (703) 308-4914

Form PCT/ISA/210 (second sheet)(July 1992)*

Petitioner Micron Ex-1004, 0081

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

Please See Extra Sheet.

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

Petitioner Micron Ex-1004, 0082

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12238

B. FIELDS SEARCHED
Electronic data bases consulted (Name of data base and where practicable terms used):

APS
search terms: folded cascode, level shift, bias, differential, push pull, source follower

BOX II. OBSERVATIONS WHERE UNITY OF INVENTION WAS LACKING
This ISA found multiple inventions as follows:

This application contains the following inventions or groups of inventions which are not so linked as to form a single inventive concept under PCT Rule 13.1. In order for all inventions to be examined, the appropriate additional examination fees must be paid.

Group I, claim(s)1-15, drawn to a differential amplifier, classified in class 330, subclass 253.
Group II, claim(s) 16, drawn to a voltage regulator, classified in class 323, subclass 313.
The inventions listed as Groups I and II do not relate to a single inventive concept under PCT Rule 13.1 because, under PCT Rule 13.2, they lack the same or corresponding special technical features for the following reasons: the differential amplifier of Group I does not require a power supply incorporating the particular voltage regulator of Group II.

Petitioner Micron Ex-1004, 0083

ABSTRACT

Systems and methods providing for improved voltage regulation of a supply voltage for an integrated circuit are described herein. The voltage regulator circuit includes a feedback circuit coupled to a first current path and adapted to maintain a gate voltage of a feedback transistor substantially constant. A pass device is coupled to a second current path and adapted to receive a signal with a magnitude based on first and second currents supplied by first and second current sources to the second current path. In an embodiment, the first current is a substantially constant current and the second current has a magnitude based on a magnitude of the voltage at the feedback transistor gate and a magnitude of a voltage at an output of the voltage regulator circuit coupled to the pass device.

Petitioner Micron Ex-1004, 0084

Electronic Acknowledgement Receipt

EFS ID:	5318329
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Amy M. Salmela/Aubre Rabe
Filer Authorized By:	Amy M. Salmela
Attorney Docket Number:	4146.08US01
Receipt Date:	12-MAY-2009
Filing Date:	
Time Stamp:	14:02:59
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$1530
RAM confirmation Number	259
Deposit Account	160631
Authorized User	SALMELA,AMY M.

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		4146_08US01_IDS.PDF	354239 2e6652ebdcb2d58c0675d9e6491a569fbc546aef	yes	7
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Transmittal Letter		1	2	
	Information Disclosure Statement (IDS) Filed (SB/08)		3	7	
Warnings:					
Information:					
2	Foreign Reference	EP1622067.PDF	801722 eccf6e8658310a5e7a73ce419121298240 8f7353	no	16
Warnings:					
Information:					
3	Foreign Reference	EP0851332.PDF	291329 43fc12ebd08dcfd8634a5696081d26d1150ca9eb	no	6
Warnings:					
Information:					
4	Foreign Reference	EP0957421.PDF	1096385 0dae40ea81016cfd3cb1e3f8c40b113ff1b09cc1	no	17
Warnings:					
Information:					
5	Foreign Reference	EP0783796.PDF	1201798 cb72a456d997f507616bcb3d24054d2793ab4850	no	36
Warnings:					
Information:					
6	Foreign Reference	WO9705696.PDF	1209259 abf58f3e1cb18d85909626ef15ad1dbc3ca4c01c	no	35
Warnings:					
Information:					

7	Foreign Reference	WO9305572.PDF	912499 8c9ff4bd5b7e9344f9f4ad644f223a232f3eb02d	no	27
Warnings:					
Information:					
8	Foreign Reference	WO2004027995.PDF	175649 75da2c14ca92edad96ccf4f75f30c5fededc65a2	no	5
Warnings:					
Information:					
9	Foreign Reference	EP1229419.PDF	97595 19e2129e17951f557d473772b368cec4f2994ae3	no	3
Warnings:					
Information:					
10	Foreign Reference	EP0661717.PDF	540832 3628963bc565caeffddd5261203b45643d75fce9	no	10
Warnings:					
Information:					
11	Foreign Reference	EP0602163.PDF	762792 af86260e32f26977fb31d050d724e2b55749e853	no	14
Warnings:					
Information:					
12	NPL Documents	AREA_efficient1.PDF	1319461 2b54cc81ffa81df4883b6f31e55c082a99e466ff	no	20
Warnings:					
Information:					
13	NPL Documents	AREA_efficient2.PDF	691675 5aca0413b6f2822f4c87110c7e505c0791004ce4	no	8
Warnings:					
Information:					
14	Application Data Sheet	4146_08US01_ADS.pdf	1016693 d2fe7df1063b7de5cc099863cf688b39f5ffca9e	no	4
Warnings:					
Information:					
15		4146_08US01_APP.PDF	1948623 e6ef9a7acb00e462a5f68c321a2ffab7655f8284	yes	43

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	22
	Claims	23	32
	Abstract	33	33
	Drawings-only black and white line drawings	34	41
	Oath or Declaration filed	42	43

Warnings:					
Information:					
16	Foreign Reference	EP0497591.PDF	437951 dd68e839669f9f19f23edb239447964c0e98429d	no	9
Warnings:					
Information:					
17	Fee Worksheet (PTO-875)	fee-info.pdf	36180 5e8007321332b51606d41d905e9ae496ade511c1	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	12894682		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 957 421 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
03.09.2003 Bulletin 2003/36

(51) Int Cl.[7]: **G05F 3/26**, G05F 3/24

(21) Application number: **99201460.5**

(22) Date of filing: **12.05.1999**

(54) **Current-efficient low-drop-out voltage regulator with improved load regulation and frequency response**

Stromeffiziente Regelungseinrichtung mit kleiner Verlustspannung, verbesserter Lastregelung und Frequenzgang

Régulateur de tension, efficace en courant, à faible tension de déchet avec une régulation de la charge et une réponse en fréquence améliorée

(84) Designated Contracting States:
DE FR GB IT NL

(30) Priority: **13.05.1998 US 85356 P**

(43) Date of publication of application:
17.11.1999 Bulletin 1999/46

(73) Proprietor: **Texas Instruments Incorporated**
Dallas, Texas 75251 (US)

(72) Inventors:
- **Rincon-Mora, Gabriel Alfonso**
  Collin County, Texas 75002 (US)
- **Corsi, Marco**
  Collin County, Texas 75025 (US)

(74) Representative: **Holt, Michael**
Texas Instruments Limited,
P.O. Box 5069
Northampton NN4 7ZE (GB)

(56) References cited:
EP-A- 0 745 923
EP-A- 0 851 332
US-A- 4 954 769
US-A- 5 168 209
US-A- 5 672 959
US-A- 5 751 639

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Jouve, 75001 PARIS (FR)

EP 0 957 421 B1

Petitioner Micron Ex-1004, 0089

Description

BACKGROUND OF THE INVENTION

[0001] This invention is in the field of integrated circuits, and is more specifically directed to voltage regulator circuits of the low drop-out type.

[0002] As is fundamental in the art, voltage regulator circuits are commonly used circuits for generating a stable voltage from an input voltage supply that may vary over time, and over varying load conditions. Especially in automotive applications and in battery-powered systems, the demand is high for voltage regulators that can generate a low-noise stable output voltage with a minimum difference in potential between the input voltage and the regulated output voltage (the minimum potential difference is referred to as the "drop-out" voltage). Typical modern low drop-out (LDO) voltage regulators have drop-out voltages that are on the order of 200 mV.

[0003] Modern portable electronic systems, such as wireless telephones, portable computers, pagers, and the like also present additional requirements upon voltage regulator circuits. As known in the art, many modern integrated circuits are operating at increasingly lower power supply voltages, with 3.3 V power supply voltages now common in these systems, and with sub-1-V power supply voltages expected within the near future. These low power supply voltages are greatly desirable in portable electronic systems, because of their improved reliability, power efficiency, and battery longevity. Additionally, because voltage regulator circuits must remain operable at all times, the quiescent current drawn by these circuits is an important characteristic, as any reduction in this quiescent current translates directly into longer battery life. Finally, the fast switching times and high frequencies at which modern integrated circuits operate in turn require excellent frequency response on the part of the voltage regulator circuitry.

[0004] An example of a modern LDO voltage regulator is described in Rincon-Mora, et al., "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator", *Journal of Solid-State Circuits*, Vol. 33, No. 1 (IEEE, January, 1998), pp. 36-44. As described therein, a current mirror circuit generates a significant boost current to assist an emitter follower at the output of the error amplifier, improving the slew-rate performance of the regulator while maintaining stability throughout the load-current range. In effect, the current mirror pushes the parasitic pole at the emitter of the emitter follower to a higher frequency during high load-current conditions, matching the increase in frequency of the required placement of this pole with increasing load current. Absent the current mirror and the resulting movement of the parasitic pole, more quiescent current flow than is necessary at low load-current conditions would be required to ensure stability at high load currents. The current mirror ratio is preferably maintained relatively high to minimize power consumption.

[0005] By way of further background, copending European application No. 97310344, filed 19.12.97 (Publ. 0 851 332), entitled "A Voltage Regulator", commonly assigned herewith, describes another LDO voltage regulator. In this regulator, a positive feedback path is provided from the current mirror to a source follower that is controlled by the output of the error amplifier; the positive feedback modulates the gate-to-source voltage of the source follower proportionally with the output device, to compensate the source follower for changes in the output impedance of the regulator. In this circuit described in this copending application, the positive feedback path includes an RC network to slow the response of the positive feedback relative to negative feedback provided to the error amplifier, in order to prevent oscillation of the circuit. Of course, this RC network reduces the bandwidth of the frequency response of the positive feedback.

BRIEF SUMMARY OF THE INVENTION

[0006] It is therefore an object of the present invention to provide a voltage regulator circuit in which load regulation, transient response, and power efficiency may be optimized.

[0007] It is a further object of the present invention to provide such a voltage regulator circuit in which the improved performance is obtained with minimal quiescent current flow, especially in low load-current conditions.

[0008] It is a further object of the present invention to provide such a voltage regulator circuit which operates at a low drop-out voltage.

[0009] It is a further object of the present invention to provide such a voltage regulator circuit which is suitable for use in low power supply voltage applications, such as in battery-powered systems.

[0010] These objectives are achieved by the voltage regulator as defined in claim 1, the method of generating a regulated output voltage as defined in claim 9 and the electronic system as defined in claim 10.

[0011] Other objects and advantages of the present invention will be apparent to those of ordinary skill in the art having reference to the following specification together with its drawings.

[0012] The present invention may be implemented in a low drop-out (LDO) voltage regulator circuit having an error amplifier for comparing an output-derived voltage against a reference voltage, and which drives a series pass switch device by way of a source follower. A current mirror is provided, in which a mirror leg conducts a fraction of the current conducted by the series pass switch device. A first positive feedback path, coupled between the current mirror and the source follower, includes an RC delay that stabilizes the feedback loop. A second positive feedback path, also coupled between the current mirror and the source follower but having reduced RC characteristics, discharges parasitic capacitance of the output transistor which appears at the source follow-

Petitioner Micron Ex-1004, 0090

er, thus improving the transient response of the voltage regulator.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING

[0013]

Figure 1 is an electrical diagram, in schematic form, of a voltage regulator circuit according to the preferred embodiment of the invention.

Figures 2a and 2b are timing diagrams illustrating the operation of the circuit of Figure 1.

Figure 3 is a frequency response plot illustrating the relative gain, over frequency, of the positive feedback paths in the voltage regulator circuit according to the preferred embodiment of the invention.

Figure 4 is an electrical diagram, in block form, illustrating an example of an electronic system, namely a wireless telephone, including the voltage regulator circuit of Figure 1 according to the preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0014] Referring now to Figure 1, the construction of low drop-out (LDO) voltage regulator 10 according to the preferred embodiment of the invention will now be described in detail. The construction of voltage regulator 10 of Figure 1 is suitable for implementation as part of an overall larger integrated circuit or, alternatively, may be realized as a separate stand-alone integrated circuit. It is contemplated that variations in the construction of voltage regulator 10 will become apparent to those of ordinary skill in the art having reference to this specification, and it is further contemplated that such variations are within the scope of the present invention as claimed hereinbelow.

[0015] The overall function of voltage regulator 10, as is typical for voltage regulator circuits in the art, is to drive a stable voltage at its output on line V_{OUT}, where the output voltage is derived from an input power supply voltage on line V_{IN}. Load 11 is connected to line V_{OUT}, and is indicative, in this example, of other circuitry in the electronic system (or, in some cases, on the same integrated circuit) which operates based upon the stable regulated voltage on line V_{OUT}. As is typical in the art, an external capacitor C_0 (with an associated equivalent series resistance represented by resistor ESR) is connected externally to voltage regulator 10, for defining the frequency response of the circuit. As is typical in the art, a reference voltage is provided to voltage regulator 10 on line V_{REF}, typically from a reference voltage generator circuit such as a bandgap reference voltage circuit, for use in maintaining a stable output voltage on line V_{OUT}.

[0016] In the exemplary embodiment of Figure 1, error amplifier 38 receives the reference voltage on line V_{REF} at a first input. A second input of error amplifier 38 receives, on line V_{FB}, a feedback voltage generated from the output of voltage regulator 10. In this example, line V_{REF} is received by the inverting input of error amplifier 38, while the non-inverting input of error amplifier 38 receives the feedback voltage on line V_{FB}. Of course, the specific polarity of the inputs receiving the feedback and reference voltages is not essential, so long as error amplifier 38 operates to generate an output signal based on the difference between these two voltages, and so long as the remainder of voltage regulator 10 comprehends the polarity of the differential signal. In other words, the overall loop through voltage regulator 10 has negative feedback.

[0017] According to the preferred embodiment of the present invention, error amplifier 38 may be implemented as a conventional differential amplifier, preferably with a current mirror load that permits the desired low voltage operation. Examples of suitable realizations for error amplifier 38 are described in Rincon-Mora, et al., "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator", *Journal of Solid-State Circuits,* Vol. 33, No. 1 (IEEE, January, 1998), pp. 36-44. Error amplifier 38 will typically have a relatively low gain to ensure stability and to minimize quiescent current.

[0018] The output of error amplifier is applied to the gate of n-channel metal-oxide-semiconductor (NMOS) transistor 24, which has its drain receiving the input voltage on line V_{IN} and which has its source connected to, among other elements, the gates of p-channel metal-oxide-semiconductor (PMOS) transistors 12, 14, which are connected together in a current mirror arrangement. NMOS transistor 24 thus serves as a source follower stage at the output of error amplifier 38. PMOS transistor 12 is a relatively large device, for driving the regulated output voltage V_{OUT} at its output. According to the preferred embodiment of the present invention shown in Figure 1, the source follower connection of transistor 24 essentially isolates the relatively large gate capacitance of large PMOS output transistor 12 from the output of error amplifier 38 (which has a relatively large resistive component in its output impedance), and presents a low input capacitance to the output of error amplifier 38 and a relatively low output impedance to transistor 12. Furthermore, transistor 24 serves as a class "A" source follower stage, which provides a sufficiently large voltage swing at its source (up to a threshold voltage drop from line V_{IN}) as to be capable of turning off PMOS output transistor 12, at least deep into its subthreshold region. As such, NMOS transistor 24 is preferably a "natural n-channel transistor" (i.e., without a threshold adjust implant , so as to have a relatively low threshold voltage, permitting its source voltage to rise very close to the voltage on line V_{IN}.

[0019] In the output leg of voltage regulator 10, PMOS

Petitioner Micron Ex-1004, 0091

transistor 12 has its source receiving input voltage V_{IN}, and its in driving the output voltage on line V_{OUT}. As mentioned above, the gate of transistor 12 is driven from the source of NMOS transistor 24, responsive to the output of error amplifier 38. Negative feedback to error amplifier 38 is generated on line V_{FB} by a resistor divider of resistors 40, 42, which are preferably of relatively high resistance values to minimize quiescent current therethrough; line V_{FB} is taken from the node between resistors 40, 42, and applied to the non-inverting input of error amplifier 38.

[0020] As noted above, PMOS transistor 14 is provided in voltage regulator 10 to mirror the output current through PMOS output transistor 12, and as such has its source receiving the input voltage on line V_{IN} and its gate driven by the source follower stage of transistor 24. In order to minimize quiescent current, mirror PMOS transistor 14 is preferably much smaller, in drive capability, than output PMOS transistor 12, for example on the order of 1000 times smaller. As such, while the current through transistors 12, 14 mirror one another, the current through mirror transistor 14 is much smaller than that through output transistor 12.

[0021] Bipolar p-n-p transistors 16, 18 have their emitters connected to the drains of PMOS transistors 12, 14, respectively. The bases of transistors 16, 18 are connected in common, and to the collector of transistor 16; the collectors of transistors 16, 18 are further connected to the drains of NMOS transistors 20, 22, respectively, which have their sources at ground. The gates of transistors 20, 22 are connected together, and to the drain of transistor 22. The circuit of transistors 16, 18, 20, 22 is provided to equalize the drain-to-source voltages of transistors 12, 14 relative to one another, and thus maintain proper current mirroring, given the extremely large (e.g., 1000:1) ratio of drive between these transistors. Also, because voltage regulator 10 is preferably of the low drop-out (LDO) type, the circuit including bipolar transistors 16, 18 also serves to maintain the drain-to-source voltages of transistors 12, 14 equal to one another even in a "drop-out" condition (e.g., when $V_{IN} \approx V_{OUT}$ at startup, or due to a drained battery), to minimize the current that may otherwise be required to be conducted through small mirror PMOS transistor 14.

[0022] As illustrated in Figure 1, the source of NMOS source follower transistor 24 is connected to current source 34, which sinks current from the source of transistor 24 to ground. Current source 34 is implemented in the conventional manner, for example by way of an NMOS transistor with its gate biased by a reference voltage. Current source 34 is preferably a very small device, or is biased so as to conduct very little current, in order to minimize quiescent current through the path of NMOS transistor 24 and current source 34, while still conducting sufficient current to stabilize voltage regulator 10 in low load-current conditions.

[0023] Similarly as the circuit described in copending application S.N. 08/992,706, voltage regulator 10 includes a first positive feedback network which includes NMOS transistor 28 having its source-drain path connected in parallel with current source 34, and having its gate controlled by the node at the drain of transistor 22 (and gates of transistors 20, 22), via series resistor 32 and shunt capacitor 30. The drive of NMOS transistor 28 is preferably larger than that of NMOS transistors 20 and 22, so that in the event of increased current through PMOS output transistor 12 (mirrored through transistors 14, 18, 22), transistor 28 turns on and changes the gate-to-source voltage of NMOS transistor 24 by an amount that is approximately equal to or greater than the change in the gate-to-source voltage of PMOS transistor 12. This operation tends to cancel the load regulation effect, as will be described in further detail hereinbelow. The rate at which transistor 28 turns on to accomplish this function is controlled according to the values of resistor 32 and capacitor 30, to prevent oscillation.

[0024] According to the preferred embodiment of the present invention, voltage regulator 10 further includes a second feedback path of NMOS transistor 35, which has its source-drain path also in parallel with current source 34. In this embodiment of the invention, the RC delay at the gate of transistor 35 is much lower than that presented by resistor 32 and capacitor 30. In this example, the gate of transistor 35 is connected directly to the drain of NMOS transistor 22, and thus in common with the gates of transistors 20, 22. As such, only the parasitic gate capacitance of transistor 35 itself, and the series resistance of the interconnection to the gate of transistor 35, will affect the switching time of transistor 35, and as such the response of transistor 35 to variations in voltage at its gate is relatively fast.

[0025] According to the preferred embodiment of the invention, the size of transistor 35 is typically relatively small, somewhat smaller than that of transistor 28, depending upon the desired transient response of voltage regulator 10. Referring now to Figure 3, the relative frequency response of transistors 28, 35 over frequency, according to the preferred embodiment of the invention, is illustrated. In Figure 3, curves G_{28}, G_{35} illustrate the gain versus frequency (both on a log scale) of transistors 28, 35, respectively. At low frequencies, transistor 28 has a higher gain than transistor 35, but at higher frequencies transistor 35 has a higher gain than does transistor 28, because of the fall-off of the frequency response of transistor 28 due to capacitor 30 and resistor 32. Accordingly, transistor 35 has a smaller gain but a higher bandwidth, in the amplifier sense, than does transistor 28. In general, transistor 35 is included in voltage regulator 10 according to the preferred embodiment of the present invention, to provide a "boost" current path (i.e., positive feedback), at the source of NMOS transistor 24, that is able to rapidly respond to transient events, thus improving the overall transient response of voltage regulator 10. Transistors 28 and 35 cumulatively provide steady-state conduction from the source of transistor 24 during high load-current conditions, to maintain stability.

Petitioner Micron Ex-1004, 0092

The relatively low gain of transistor 35 at low frequencies prevents oscillation as voltage regulator 10 reaches a steady state (or at least until transistor 28 responds to the load variation, as controlled by the RC network of resistor 32 and capacitor 30).

[0026] Of course, while two positive feedback transistors 28, 35 with varying frequency response are provided in voltage regulator 10 according to the preferred embodiment of the invention, it is contemplated that further optimization of voltage regulator 10 may be accomplished by providing still additional positive feedback devices with different frequency response characteristics. It is expected that those of ordinary skill in the art having reference to this specification will be readily able to optimize circuit operation with two or more positive feedback devices, through design of the frequency response and associated RC delays.

[0027] As described in copending application S.N. 08/992,706, the positive feedback provided by transistor 28 improves load regulation by modulating the gate-to-source voltage of source follower NMOS transistor 24 proportionately with the gate-to-source voltage of output PMOS transistor 12. As is known in the art, load regulation refers to the magnitude of variation in the regulated output voltage on line V_{OUT} over the possible range of load conditions, and thus over the possible range of output current sourced by PMOS output transistor 12. Load regulation, in this example, is a function of the loop gain of voltage regulator 10, of the output resistance of PMOS output transistor 12, and of the systematic offset voltage performance of the feedback loop of resistors 40, 42, and error amplifier 38. In particular, in this embodiment of the invention, systematic offset voltage in the feedback loop significantly affects load regulation, considering that the loop gain is maintained low in order to meet the desired frequency response, and because the gate voltage of PMOS output transistor 12 swings over a relatively large range (on the order of 0.5 volts), depending upon its aspect ratio and upon the range of load currents therethrough.

[0028] On the other hand, because of the presence of resistor 32 and capacitor 30 to prevent oscillation, transistor 28 will not turn on quickly enough to provide suitable transient response, for example in the event of rapid changes in load current through load 11, or in the input voltage on line V_{IN}. Transistor 35, although of relatively low gain, is able to respond quickly to such transient events, so that the output voltage on line V_{OUT} settles quickly after such events.

[0029] Referring now to Figures 2a and 2b, the operation of voltage regulator 10 according to the preferred embodiment of the present invention will now be described in detail. Figure 2a illustrates the behavior of output voltage V_{OUT} in response to changes in the load current I_{load} drawn by load 11 in the example of Figure 1, as illustrated in Figure 2b. In the example of Figures 2a and 2b, a sudden increase in load current I_{load} occurs at time t_1, and a sudden decrease in load current I_{load} occurs at time t_2.

[0030] Prior to time t_1 of Figures 2a, and 2b, a relatively low level load current I_0 is being sourced by PMOS output transistor 12 through load 11; at this time, the output voltage on line V_{OUT} is at a level V_0, which will be near the reference voltage V_{REF} in the steady state. At this time prior to the transition, the gate-to-source voltage at PMOS output transistor 12 is relatively small as required to produce the relatively low load current I_0; the gate voltage of transistor 12 is, of course, under the control of error amplifier 38 via source follower 24.

[0031] At time t_1 in this example, the condition of load 11 changes so as to require additional current, up to current I_1 as shown in Figure 2b. The additional current ($I_1 - I_0$) must, of course, be sourced by PMOS output transistor 12. Since the gate of transistor 12 is controlled by way of error amplifier 38, conduction through transistor 12 does not change immediately. The additional load current demand is thus initially supplied from capacitor C_0, which causes the output voltage on line V_{OUT} to begin to fall toward ground, as illustrated in Figure 2a. This reduction in the output voltage causes a reduction in the feedback voltage on line V_{FB} generated by the resistor divider of resistors 40, 42. Error amplifier 38 responsively reduces the voltage at its output, reducing the voltage at the gate of NMOS source follower transistor 24, which permits the gate of transistor 12 to be discharged to ground through current source 34, and thus to conduct additional current.

[0032] However, the capacity of current source 34 is relatively limited, such as on the order of 1 μA, to minimize quiescent current. This limits the ability of source follower 24 to quickly turn on output PMOS transistor 12 from a low current condition to a high current condition, considering the relatively large gate capacitance of transistor 12 and the relatively small current conducted by current source 34. According to the preferred embodiment of the invention, however, the increased current that begins to be conducted through PMOS output transistor 12 is mirrored by PMOS mirror transistor 14, considering that the drain voltages of transistors 12, 14 are maintained relatively equal through the operation of the circuit of transistors 16, 18, 20, 22. The mirror current through transistor 14 is conducted by p-n-p transistor 18 and NMOS transistor 22 and, because this mirror current is increasing, the voltage at the gate of transistor 35 rises, turning on transistor 35 and opening another current path for the discharge of the gate of transistor 12 to ground, further increasing the magnitude of the gate-to-source voltage of transistor 12 and increasing its conduction. As such, transistor 35 provides positive feedback to the operation of voltage regulator 10 in response to this transient event, accelerating its response to the sudden load current demand increase. This positive feedback is especially important in the transition from low load current to a higher load current; conversely, for the transition from high load current to low load current, source follower transistor 24 is not limited in its

Petitioner Micron Ex-1004, 0093

current drive, and is therefore quite capable of switching the state of PMOS output transistor 12 without positive feedback.

[0033] As the gate capacitance of PMOS output transistor 12 is discharged toward ground through transistor 35 and current source 34, transistor 12 thus provides additional load current I_{load}, responsive to which the output voltage on line V_{OUT} rises (as capacitor C_0 charges) and is reflected by error amplifier 38. Due to the conduction through transistors 14, 18, and 22, transistor 35 remains on throughout this transient event, and also remains on into the steady-state high load-current condition. The negative transient voltage V_{tran}- measurement is the differential voltage between the starting voltage V_0 and the lowest peak voltage, as shown in Figure 2a. The presence of the second, low-gain, fast response feedback path comprised of transistor 35 reduces this negative transient voltage V_{tran}- from that which is attainable in conventional circuits that conduct similar quiescent current. The extent to which ripple remains in the voltage on line V_{OUT} is primarily due to the phase margin of voltage regulator 10.

[0034] The voltage level V_1 to which the output voltage on line V_{OUT} settles, in a high load current condition (load current I_{load} at level I_1) is determined by the load regulation capability of voltage regulator 10. In voltage regulator 10, the load regulation voltage differential V_{LAR} may be expressed as:

$$V_{LAR} = \frac{R_{12\text{-}on}}{1+AB} + \frac{\Delta V_{gs12} - \Delta V_{gs24}}{A_1}$$

where A corresponds to the open loop gain (to V_{OUT}), where A_1 corresponds to the open loop gain of error amplifier 38 (i.e., to the gate of transistor 24), where $R_{12\text{-}on}$ is the on-resistance of transistor 12, and where the gate-to-source voltage differentials ΔV_{gs12}, ΔV_{gs24} refer to the differentials as a result of the transient event. B refers to the feedback gain factor, which is defined in this example as the resistor divider ratio of resistors 40, 42 (i.e., by $\frac{R_{42}}{R_{40}+R_{42}}$. According to the preferred embodiment of the invention, the load regulation voltage differential V_{LAR} is minimized through the operation of transistor 28, under the control of resistor 32 and capacitor 30, which increases the differential gate-to-source voltage ΔV_{gs24} of transistor 24 in response to a transient event; indeed, the differential gate-to-source voltage ΔV_{gs24} is preferably increased beyond that of the differential gate-to-source voltage ΔV_{gs12} so as to partially cancel the first term of the differential load regulation voltage V_{LAR}.

[0035] This increase in the differential gate-to-source voltage ΔV_{gs24} occurs in voltage regulator 10 predominantly due to transistor 28 also turning on at some point after the initial transient after time t_1, and thus at some point after transistor 35 turns on. The delay time at which transistor 28 turns on is, of course, controlled by the network of resistor 32 and capacitor 30, according to the frequency response discussed above relative to Figure 3.

[0036] A transition from a high load-current condition to a low load-current condition occurs, in this example, at time t_2 of Figures 2a and 2b. At a point in time prior to time t_2 and after the output voltage on line V_{OUT} has settled, the condition of voltage regulator 10 of Figure 1 has output PMOS transistor 12 conducting a significant amount of current; this current is mirrored by transistor 14, with this mirror current conducted by transistors 18, 22. The relatively high current through transistor 22 causes transistors 28, 35 to remain on during the steady-state high load current condition, as noted above.

[0037] Upon load 11 reducing its load current demand at time t_2 in Figures 2a and 2b, the current that is then being conducted by PMOS output transistor 12 initially charges capacitor C_0, which raises the voltage on line V_{OUT}. This higher voltage is reflected in the feedback voltage on line V_{FB}, which in turn causes the output of error amplifier 38 to be driven high, toward input voltage V_{IN}. Because transistors 28 and 35 are initially on, however, the voltage at the source of transistor 24 is initially relatively low, which establishes a higher gate-to-source voltage for transistor 24 and thus results in a large gate drive for transistor 24. The current conducted by transistor 24 thus rapidly turns off p-channel transistors 12, 14, quickly reducing the load current sourced from the voltage at line V_{IN} through PMOS output transistor 12.

[0038] As the current through PMOS output transistor 12 is reduced, so too is the current through transistors 14, 18, 22; transistors 28, 35 are, in turn, turned off, which assists the voltage at the source of transistor 24 to rise toward the voltage on line V_{IN}, considering that the current sink of current source 34 is relatively small. As the load current through PMOS transistor 12 reduces, the voltage on line V_{OUT} will then eventually settle to its steady-state low load-current level at V_0, as shown in Figure 2a. The transient voltage V_{tran+} corresponds to the transient response of voltage regulator 10 in this transition.

[0039] A typical example of voltage regulator 10, according to the preferred embodiment of the invention, will have a gain for error amplifier 38 on the order of 40 to 60 dB, with a unity gain frequency (UGF) of about 1 MHz. Simulation has determined that, assuming an external capacitance of 10 μF (and assuming no equivalent series resistance ESR), with a connection resistance of 63 mΩ, a pulse in the load current I_{load} of from 10 mA to 100mA can be handled by voltage regulator 10 with a load regulation voltage differential of 1 mV. Also in this example, the negative transient voltage V_{tran}- on line V_{OUT} was 20 mV, and the positive transient voltage V_{tran}+ was 23 mV. Through simulation, this exemplary circuit achieved a quiescent current, at low load-current conditions, of about 20 μA.

[0040] According to the preferred embodiment of the

Petitioner Micron Ex-1004, 0094

invention, therefore, a voltage regulator circuit is provided which draws an extremely low quiescent current in steady-state, but which provides both excellent transient response and also excellent load regulation. Low drop-out (LDO) operation, such as on the order of 100 mV or lower, is readily obtained according to the preferred embodiment of the invention. The voltage regulator circuit according to this embodiment of the invention also provides these advantages in a circuit which may be efficiently implemented into an integrated circuit according to conventional technology, and is contemplated to be quite stable and robust in operation.

[0041] Referring now to Figure 4, an example of an electronic system incorporating voltage regulator 10 according to the preferred embodiment of the invention will now be described. The system illustrated in Figure 4 is wireless telephone handset 100, which is an electronic system which particularly benefits from voltage regulator 10, as conservation of battery power and low voltage operation is of particular concern in wireless telephones. The present invention will also be beneficial in other electronic systems, particularly those in which LDO voltage regulators are commonly used to provide clean power supply voltages generated from low voltage power sources, such as batteries. Examples of such systems include laptop or notebook computers, pagers, and automotive applications. Furthermore, the present invention may be implemented as a standalone voltage regulator for microprocessor or personal computer systems, particularly in providing clean power supply voltages to analog circuitry in such systems.

[0042] Handset 100 of Figure 4 includes microphone M for receiving audio input, and speaker S for outputting audible output, in the conventional manner. Microphone M and speaker S are connected to audio interface 112 which, in this example, converts received signals into digital form and vice versa, in the manner of a conventional voice coder/decoder ("codec"). In this example, audio input received at microphone M is applied to filter 114, the output of which is applied to the input of analog-to-digital converter (ADC) 116. On the output side, digital signals are received at an input of digital-to-analog converter (DAC) 122; the converted analog signals are then applied to filter 124, the output of which is applied to amplifier 125 for output at speaker S.

[0043] The output of audio interface 112 is in communication with digital interface 120, which in turn is connected to microcontroller 126 and to digital signal processor (DSP) 130, by way of separate buses. Microcontroller 126 controls the general operation of handset 100, and is connected to input/output devices 128, which include devices such a a keypad or keyboard, a user display, and any add-on cards. Microcontroller 126 handles user communication through input/output devices 128, and manages other functions such as connection, radio resources, power source monitoring, and the like. In this regard, circuitry used in general operation of handset 100, such as voltage regulators, power sources, operational amplifiers, clock and timing circuitry, switches and the like are not illustrated in Figure 1 for clarity; it is contemplated that those of ordinary skill in the art will readily understand the architecture of handset 100 from this description.

[0044] In handset 100 according to the preferred embodiment of the invention, DSP 130 is connected on one side to interface 120 for communication of signals to and from audio interface 112 (and thus microphone M and speaker S), and on another side to radio frequency (RF) circuitry 140, which transmits and receives radio signals via antenna A. DSP 30 is preferably a fixed point digital signal processor, for example the TMS320C54x DSP available from Texas Instruments Incorporated, programmed to perform signal processing necessary for telephony, including speech coding and decoding, error correction, channel coding and decoding, equalization, demodulation, encryption, and the like, under the control of instructions stored in program memory 131.

[0045] RF circuitry 140 bidirectionally communicates signals between antenna A and DSP 130. For transmission, RF circuitry 140 includes codec 132 which receives digital signals from DSP 130 that are representative of audio to be transmitted, and codes the digital signals into the appropriate form for application to modulator 134. Modulator 134, in combination with synthesizer circuitry (not shown), generates modulated signals corresponding to the coded digital audio signals; driver 136 amplifies the modulated signals and transmits the same via antenna A. Receipt of signals from antenna A is effected by receiver 138, which is a conventional RF receiver for receiving and demodulating received radio signals; the output of receiver 138 is connected to codec 132, which decodes the received signals into digital form, for application to DSP 130 and eventual communication, via audio interface 112, to speaker S.

[0046] Handset 100 is powered by battery 150, which is a rechargeable chemical cell of conventional type for wireless telephone handsets. The output of battery 150 is received by power management unit 160. Power management unit 160, in this example, is realized as a single integrated circuit; alternatively, the functions of power management unit 160 may be further integrated with other functions in handset 100, or may be realized as more than one integrated circuit. Power management unit 160 includes DC-DC converter circuit 162, constructed in the conventional manner for converting the voltage from battery 150 into one or more desired operating voltages for use in handset 100. The output of DC-DC converter 162 is illustrated in Figure 4 as line V_{IN}.

[0047] Conventional DC-DC converter circuitry typically produces power supply voltages that are somewhat noisy, and that fluctuate to some extent; as such, in handset 100, the voltage on line V_{IN} produced by DC-DC converter 162 will typically include some noise and fluctuation. Because digital circuitry is generally somewhat insensitive to noise and voltage fluctuations

Petitioner Micron Ex-1004, 0095

at their power supply, the voltage on line V_{IN} may, if desired, be applied directly to digital functions such as DSP 130 and the like within handset 100. Analog functions typically require a steady and noise-free power supply voltage to function accurately. Accordingly, in the example of Figure 4, power management unit 160 includes one or more LDO voltage regulators 10 (only one of which is illustrated in Figure 4, for clarity), for producing a stable output power supply voltage on line V_{OUT}. Power management unit 160 in this example also includes reference voltage circuitry 164 which produces a reference voltage on line V_{REF} for use by voltage regulator 10 (and also by DC-DC converter 162), generated from the battery voltage. Each of voltage regulators 10 are constructed in the manner described above relative to Figure 1, and generate a regulated output voltage on line V_{OUT}. In the example of Figure 4, line V_{OUT} is applied to receiver 138, modulator 134, and driver 136 in RF circuitry, and as such powers these sensitive analog circuits. Additionally, the integrated circuit of power management unit 160 may itself include power amplifier 125, which powers speaker S in handset 100, based upon the stable output voltage on line V_{OUT}; furthermore, analog filters 114, 124 may also be biased by the stable output voltage on line V_{OUT}, if desired.

[0048] With the incorporation of LDO voltage regulator 10 into power management unit 160, handset 100 thus benefits greatly from the provision of a stable power supply voltage for bias of its analog functions. These benefits are also available in any system according to the present invention utilizing the voltage regulation approach described hereinabove. This stable and regulated voltage is generated in a manner which requires little quiescent current, and which is capable of low voltage operation, thus conserving battery life. Additionally, the transient response and load regulation achieved according to the present invention is particularly beneficial in providing a stable output voltage, using circuitry which may be efficiently and readily implemented into integrated circuit realizations.

[0049] While the present invention has been described according to its preferred embodiments, it is of course contemplated that modifications of, and alternatives to, these embodiments, such modifications and alternatives obtaining the advantages and benefits of this invention, will be apparent to those of ordinary skill in the art having reference to this specification and its drawings. It is contemplated that such modifications and alternatives are within the scope of this invention as subsequently claimed herein.

Claims

1. A voltage regulator circuit, comprising:

   an error amplifier, having a first input receiving a reference voltage and having a second input, for generating a voltage at an output responsive to a difference in the voltages at its first and second inputs;

   a source follower transistor having a gate coupled to the output of the error amplifier, having a drain connected to an input voltage, and having a source;

   a current source, coupled between the source of the source follower transistor and a reference bias voltage;

   an output leg, comprising an output MOS transistor having a source-drain path coupled between the input voltage and an output node, and having a gate coupled to the source of the source follower transistor;

   a mirror leg, comprising a mirror MOS transistor having a source-drain path coupled on one side to the input voltage, and having a gate coupled to the source of the source follower transistor;

   a negative feedback circuit coupled to the output node and to the second input of the error amplifier, for providing feedback to the error amplifier based upon the voltage at the output node;

   a first positive feedback transistor having a conduction path connected in parallel with the current source, having a control electrode coupled to the mirror leg;

   a delay network, coupled to the control electrode of the first positive feedback transistor, for delaying the response of the control electrode of the first positive feedback transistor; and

   a second positive feedback transistor, having a conduction path connected in parallel with the current source, and having a control electrode coupled to the mirror leg, the second positive feedback transistor having a faster response than the first positive feedback transistor.

2. The voltage regulator of claim 1, wherein the delay network comprises:

   a resistor, connected on one side to the control electrode of the first positive feedback transistor, and connected on a second side to the mirror leg; and

   a capacitor, connected on one side to the control electrode of the first positive feedback transistor, and connected on a second side to a fixed voltage.

3. The voltage regulator of claim 1, wherein the output leg further comprises:

   a first bipolar transistor having a collector-emitter path connected on one end to the output node, and having a base connected to another end of the collector-emitter path; and

Petitioner Micron Ex-1004, 0096

a first MOS transistor having a source-drain path coupled between the collector-emitter path of the first bipolar transistor and the reference bias voltage, and having gate;

and wherein the mirror leg further comprises:

a second bipolar transistor having a collector-emitter path connected on one end to a second side of the source-drain path of the mirror MOS transistor, and having a base connected to the base of the first bipolar transistor; and
a second MOS transistor having a source-drain path coupled between the collector-emitter path of the second bipolar transistor and the reference bias voltage, and having a gate connected to the gate of the first MOS transistor and to the collector-emitter path of the second bipolar transistor.

4. The voltage regulator of claim 3, wherein the control electrode of the first positive feedback transistor and the control electrode of the second positive feedback transistor are coupled to the mirror leg at a node connecting the source-drain path of the second MOS transistor and the collector-emitter path of the second bipolar transistor.

5. The voltage regulator of claim 4, wherein the delay network comprises:

a resistor, connected on one side to the control electrode of the first positive feedback transistor, and connected on a second side to the node connecting the source-drain path of the second MOS transistor and the collector-emitter path of the second bipolar transistor; and
a capacitor, connected on one side to the control electrode of the first positive feedback transistor, and connected on a second side to a fixed voltage.

6. The voltage regulator of claim 1, wherein the source follower transistor, and the first and second positive feedback transistors, are each an n-channel MOS transistor.

7. The voltage regulator of claim 6, wherein the mirror MOS transistor and the output MOS transistor are each a p-channel MOS transistor.

8. The voltage regulator of claim 1, wherein the negative feedback circuit comprises a voltage divider.

9. A method of generating a regulated output voltage from an input voltage, comprising:

comparing a feedback voltage based upon the output voltage to a reference voltage;
responsive to the comparing step determining that the feedback voltage is lower than the reference voltage, controlling conduction through a source follower transistor having a drain coupled to the input voltage, and having a source coupled to the gate of an output transistor, so that the output transistor increases the current conducted through a source-drain path connected between the input voltage and an output node;
mirroring the current conducted by the output transistor with a mirror transistor;
responsive to an increase in the mirrored current, turning on a first transistor connected between the source of the source follower transistor and a reference bias voltage, to assist in discharge of the gate of the output transistor; and
after the turning on step, turning on a second transistor connected between the source of the source follower transistor and the reference bias voltage.

10. An electronic system, comprising:

a voltage source;
a reference voltage generator circuit;
a load; and
a voltage regulator, comprising:

an error amplifier, having a first input receiving a reference voltage from the reference voltage generator circuit and having a second input, for generating a voltage at an output responsive to a difference in the voltages at its first and second inputs;
a source follower transistor having a gate coupled to the output of the error amplifier, having a drain connected to an input voltage from the voltage source, and having a source;
a current source, coupled between the source of the source follower transistor and a reference bias voltage;
an output leg, comprising an output MOS transistor having a source-drain path coupled between the input voltage and an output node coupled to the load, and having a gate coupled to the source of the source follower transistor;
a mirror leg, comprising a mirror MOS transistor having a source-drain path coupled on one side to the input voltage, and having a gate coupled to the source of the source follower transistor;
a negative feedback circuit coupled to the output node and to the second input of the error amplifier, for providing feedback to

Petitioner Micron Ex-1004, 0097

the error amplifier based upon the voltage at the output node;
a first positive feedback transistor having a conduction path connected in parallel with the current source, having a control electrode coupled to the mirror leg;
a delay network, coupled to the control electrode of the first positive feedback transistor, for delaying the response of the control electrode of the first positive feedback transistor; and
a second positive feedback transistor, having a conduction path connected in parallel with the current source, and having a control electrode coupled to the mirror leg, the second positive feedback transistor having a faster response than the first positive feedback transistor.

Patentansprüche

1. Spannungsregelschaltung, welche aufweist:

einen Fehlerverstärker mit einem ersten Eingang, der eine Referenzspannung empfängt, und einem zweiten Eingang zum Erzeugen einer Spannung an einem Ausgang ansprechend auf eine Differenz der Spannungen an seinem ersten und zweiten Eingang,

einen Source-Folger-Transistor mit einem Gate-Anschluß, der mit dem Ausgang des Fehlerverstärkers gekoppelt ist, einem Drain-Anschluß, an den eine Eingangsspannung angelegt ist, und einem Source-Anschluß,

eine Stromquelle, die zwischen den Source-Anschluß des Source-Folger-Transistors und eine Referenzvorspannung geschaltet ist,

einen Ausgangszweig, der einen Ausgangs-MOS-Transistor aufweist, dessen Source-Drain-Pfad zwischen die Eingangsspannung und einen Ausgangsschaltungspunkt geschaltet ist und dessen Gate-Anschluß mit dem Source-Anschluß des Source-Folger-Transistors gekoppelt ist,

einen Spiegelzweig, der einen MOS-Spiegeltransistor aufweist, dessen Source-Drain-Pfad auf einer Seite auf die Eingangsspannung gelegt ist und dessen Gate-Anschluß mit dem Source-Anschluß des Source-Folger-Transistors gekoppelt ist,

einen Gegenkopplungskreis, der mit dem Ausgangsschaltungspunkt und dem zweiten Eingang des Fehlerverstärkers gekoppelt ist, um dem Fehlerverstärker auf der Grundlage der Spannung am Ausgangsschaltungspunkt eine Rückkopplung bereitzustellen,

einen ersten Transistor zur Mitkopplung, der einen Leitungspfad aufweist, der parallel zur Stromquelle geschaltet ist und der eine Steuerelektrode aufweist, die mit dem Spiegelzweig gekoppelt ist,

einen ersten Transistor zur Mitkopplung, der einen Leitungspfad aufweist, der parallel zur Stromquelle geschaltet ist und der eine Steuerelektrode aufweist, die mit dem Spiegelzweig gekoppelt ist,

ein Verzögerungsnetzwerk, das mit der Steuerelektrode des ersten Transistors zur Mitkopplung gekoppelt ist, um das Ansprechen der Steuerelektrode des ersten Transistors zur Mitkopplung zu verzögern, und

einen zweiten Transistor zur Mitkopplung, der einen Leitungspfad aufweist, der parallel zur Stromquelle geschaltet ist und der eine Steuerelektrode aufweist, die mit dem Spiegelzweig gekoppelt ist, wobei der zweite Transistor zur Mitkopplung ein schnelleres Ansprechen aufweist als der erste Transistor zur Mitkopplung.

2. Spannungsregler nach Anspruch 1, wobei das Verzögerungsnetzwerk aufweist:

einen Widerstand, der auf einer Seite an die Steuerelektrode des ersten Transistors zur Mitkopplung angeschlossen ist und der auf einer zwei en Seite an den Spiegelzweig angeschlossen ist, und

einen Kondensator, der auf einer Seite an die Steuerelektrode des ersten Transistors zur Mitkopplung angeschlossen ist und der auf einer zweiten Seite an eine feste Spannung gelegt ist.

3. Spannungsregler nach Anspruch 1, wobei der Ausgangszweig weiter aufweist:

einen ersten Bipolartransistor mit einem Kollektor-Emitter-Pfad, der an ein Ende des Ausgangsschaltungspunkts angeschlossen ist, und einer Basis, die an ein anderes Ende des Kollektor-Emitter-Pfads angeschlossen ist, und

einen ersten MOS-Transistor mit einem Source-Drain-Pfad, der zwischen den Kollektor-Emitter-Pfad des ersten Bipolartransistors und

Petitioner Micron Ex-1004, 0098

die Referenzvorspannung geschaltet ist, und einem Gate-Anschluß,

wobei der Spiegelzweig weiter aufweist:

einen zweiten Bipolartransistor mit einem Kollektor-Emitter-Pfad, der an einem Ende an eine zweite Seite des Source-Drain-Pfads des MOS-Spiegeltransistors angeschlossen ist, und einer Basis, die an die Basi des ersten Bipolartransistors angeschlossen ist, und

einen zweiten MOS-Transistor mit einem Source-Drain-Pfad, der zwischen den Kollektor-Emitter-Pfad des zweiten Bipolartransistors und die Referenzvorspannung geschaltet ist, und einem Gate-Anschluß, der an den Gate-Anschluß des ersten MOS-Transistors und den Kollektor-Emitter-Pfad des zweiten Bipolartransistors angeschlossen ist.

4. Spannungsregler nach Anspruch 3, wobei die Steuerelektrode des ersten Transistors zur Mitkopplung und die Steuerelektrode des zweiten Transistors zur Mitkopplung an einem Schaltungspunkt, der den Source-Drain-Pfad des zweiten MOS-Transistors und den Kollektor-Emitter-Pfad des zweiten Bipolartransistors verbindet, mit dem Spiegelzweig gekoppelt sind.

5. Spannungsregler nach Anspruch 4, wobei das Verzögerungsnetzwerk aufweist:

einen Widerstand, der auf einer Seite an die Steuerelektrode des ersten Transistors zur Mitkopplung angeschlossen ist und der auf einer zweiten Seite an den Schaltungspunkt angeschlossen ist, der den Source-Drain-Pfad des zweiten MOS-Transistors und den Kollektor-Emitter-Pfad des zweiten Bipolartransistors verbindet, und

einen Kondensator, der auf einer Seite an die Steuerelektrode des ersten Transistors zur Mitkopplung angeschlossen ist und der auf einer zweiten Seite an eine feste Spannung gelegt ist.

6. Spannungsregler nach Anspruch 1, wobei der Source-Folger-Transistor und der erste und der zweite Transistor zur Mitkopplung beide n-Kanal-MOS-Transistoren sind.

7. Spannungsregler nach Anspruch 6, wobei der MOS-Spiegeltransistor und der MOS-Ausgangstransistor jeweils p-Kanal-MOS-Transistoren sind.

8. Spannungsregler nach Anspruch 1, wobei der Gegenkopplungskreis einen Spannungsteiler aufweist.

9. Verfahren zum Erzeugen einer geregelten Ausgangsspannung anhand einer Eingangsspannung, welches aufweist:

Vergleichen einer Rückkopplungsspannung auf der Grundlage der Ausgangsspannung mit einer Referenzspannung,

ansprechend darauf, daß im Vergleichsschritt festgestellt wird, daß die Rückkopplungsspannung niedriger als die Referenzspannung ist, Steuern der Leitung durch einen Source-Folger-Transistor, dessen Drain-Anschluß auf die Eingangsspannung gelegt ist und dessen Source-Anschluß mit dem Gate-Anschluß eines Ausgangstransistors gekoppelt ist, so daß der Ausgangstransistor den Strom erhöht, der durch einen Source-Drain-Pfad geleitet wird, der zwischen die Eingangsspannung und einen Ausgangsschaltungspunkt geschaltet ist,

Spiegeln des vom Ausgangstransistor geleiteten Stroms mit einem Spiegeltransistor,

ansprechend auf eine Erhöhung des gespiegelten Stroms enfolgendes Durchschalten eines ersten Transistors, der zwischen den Source-Anschluß des Source-Folger-Transistors und eine Referenzvorspannung geschaltet ist, um das Entladen des Gate-Anschlusses des Ausgangstransistors zu unterstützen, und

nach dem Durchschaltschritt erfolgendes Durchschalten eines zweiten Transistors, der zwischen den Source-Anschluß des Source-Folger-Transistors und die Referenzvorspannung geschaltet ist.

10. Elektronisches System, welches aufweist:

eine Spannungsquelle,

eine Referenzspannungs-Generatorschaltung,

eine Last und

einen Spannungsregler, welcher aufweist:

einen Fehlerverstärker mit einem ersten Eingang, der eine Referenzspannung empfängt, und einem zweiten Eingang zum Erzeugen einer Spannung an einem Ausgang ansprechend auf eine Differenz der Spannungen an seinem ersten und zweiten Eingang,

Petitioner Micron Ex-1004, 0099

einen Source-Folger-Transistor mit einem Gate-Anschluß, der mit dem Ausgang des Fehlerverstärkers gekoppelt ist, einem Drain-Anschluß an den eine Eingangsspannung angelegt ist, und einem Source-Anschluß,

eine Stromquelle, die zwischen den Source-Anschluß des Source-Folger-Transistors und eine Referenzvorspannung geschaltet ist,

einen Ausgangszweig, der einen Ausgangs-MOS-Transistor aufweist, dessen Source-Drain-Pfad zwischen die Eingangsspannung und einen Ausgangsschaltungspunkt geschaltet ist und dessen Gate-Anschluß mit dem Source-Anschluß des Source-Folger-Transistors gekoppelt ist,

einen Spiegelzweig, der einen MOS-Spiegeltransistor aufweist, dessen Source-Drain-Pfad auf einer Seite auf die Eingangsspannung gelegt ist und dessen Gate-Anschluß mit dem Source-Anschluß des Source-Folger-Transistors gekoppelt ist,

einen Gegenkopplungskreis, die mit dem Ausgangsschaltungspunkt und dem zweiten Eingang des Fehlerverstärkers gekoppelt ist, um dem Fehlerverstärker auf der Grundlage der Spannung am Ausgangsschaltungspunkt eine Rückkopplung bereitzustellen,

einen ersten Transistor zur Mitkopplung, der einen Leitungspfad aufweist, der parallel zur Stromquelle geschaltet ist und der eine Steuerelektrode aufweist, die mit dem Spiegelzweig gekoppelt ist,

ein Verzögerungsnetzwerk, das mit der Steuerelektrode des ersten Transistors zur Mitkopplung gekoppelt ist, um das Ansprechen der Steuerelektrode des ersten Transistors zur Mitkopplung zu verzögern, und

einen zweiten Transistor zur Mitkopplung, der einen Leitungspfad aufweist, der parallel zur Stromquelle geschaltet ist und der eine Steuerelektrode aufweist, die mit dem Spiegelzweig gekoppelt ist, wobei der zweite Transistor zur Mitkopplung ein schnelleres Ansprechen aufweist als der erste Transistor zur Mitkopplung.

Revendications

1. Circuit régulateur de tension, comprenant :

un amplificateur d'erreurs, ayant une première entrée qui permet de recevoir une tension de référence et ayant une seconde entrée pour produire une tension une sortie en réponse à une différence entre les tensions à ses première et deuxième entrées ;
un transistor à source suiveuse ayant une grille couplée à la sortie de l'amplificateur d'erreurs, ayant un drain connecté à une tension d'entrée, et ayant une source ;
une source de courant, couplée entre la source du transistor à source suiveuse et une tension de polarisation de référence ;
une branche de sortie, qui comprend un transistor de sortie MOS ayant un chemin source - drain couplé entre la tension d'entrée et un noeud de sortie, et ayant une grille couplée à la source du transistor à source suiveuse ;
une branche de miroir, qui comprend un transistor MOS de miroir ayant un chemin source - drain couplé d'un côté à la tension d'entrée, et ayant une grille couplée à la source du transistor à source suiveuse ;
un circuit de réaction négative couplé au noeud de sortie et à la seconde entrée de l'amplificateur d'erreurs, qui permet de fournir une réaction à l'amplificateur d'erreurs sur la base de la tension au noeud de sortie ;
un premier transistor de réaction positive ayant un chemin de conduction connecté en parallèle à la source de courant, ayant une électrode de commande couplée à la branche de miroir ;
un réseau de retard, couplé à l'électrode de commande du premier transistor de réaction positive, qui permet de retarder la réponse de l'électrode de commande du premier transistor de réaction positive ; et
un second transistor de réaction positive ayant un chemin de conduction connecté en parallèle à la source de courant, ayant une électrode de commande couplée à la branche de miroir, le second transistor de réaction positive ayant une réponse plus rapide que le premier transistor de réaction positive.

2. Régulateur de tension selon la revendication 1, dans lequel le réseau de retard comprend :

une résistance, connectée d'un côté à l'électrode de command du premier transistor de réaction positive, et connectée de l'autre côté à la branche de miroir ; et
un condensateur, connecté d'un côté à l'électrode de commande du premier transistor de

Petitioner Micron Ex-1004, 0100

réaction positive, et connecté de l'autre côté à une tension fixe.

3. Régulateur de tension selon la revendication 1, dans lequel la branche de sortie comprend de plus :

un premier transistor bipolaire ayant un chemin collecteur - émetteur connecté à une extrémité au noeud de sortie, et ayant une base connectée à une autre extrémité du chemin collecteur - émetteur ; et
un premier transistor MOS ayant un chemin source - drain couplé entre le chemin collecteur - émetteur du premier transistor bipolaire et la tension de polarisation de référence, et ayant une grille ;

et dans lequel la branche de miroir comprend de plus :

un second transistor bipolaire ayant un chemin collecteur - émetteur connecté à une extrémité à un second côté du chemin source - drain du transistor MOS de miroir, et ayant une base connectée à la base du premier transistor bipolaire ; et
un second transistor MOS ayant un chemin source - drain couplé entre le chemin collecteur - émetteur du second transistor bipolaire et la tension de polarisation de référence, et ayant une grille connectée à la grille du premier transistor MOS et au chemin collecteur - émetteur du second transistor bipolaire.

4. Régulateur de tension selon la revendication 3, dans lequel l'électrode de commande du premier transistor de réaction positive et l'électrode de commande du second transistor de réaction positive sont couplées à la branche de miroir à un noeud qui connecte le chemin source - drain du second transistor MOS et le chemin collecteur - émetteur du second transistor bipolaire.

5. Régulateur de tension selon la revendication 4, dans lequel le réseau de retard comprend :

une résistance, connectée d'un côté à l'électrode de commande du premier transistor de réaction positive, et connectée à un second côté au noeud qui connecte le chemin source - drain du second transistor MOS et le chemin collecteur - émetteur du second transistor bipolaire ; et
un condensateur, connecté d'un côté à l'électrode de command du premier transistor de réaction positive, et connecté de l'autre côté à une tension fixe.

6. Régulateur de tension selon la revendication 1, dans lequel le transistor à source suiveuse, et les premier et second transistors de réaction positive, sont tous deux un transistor MOS à canal n.

7. Régulateur de tension selon la revendication 6, dans lequel le transistor MOS de miroir et le transistor MOS de sortie sont tous deux un transistor MOS à canal p.

8. Régulateur de tension selon la revendication 1, dans lequel le circuit de réaction négative comprend un diviseur de tension.

9. Procédé de production d'une tension de sortie régulée à partir d'une tension d'entrée, comprenant :

la comparaison d'une tension de réaction fondée sur la tension de sortie, à une tension de référence ;
en réponse à l'étape de comparaison, qui détermine que la tension de réaction est inférieure à la tension de référence, la commande de la conduction par un transistor à source suiveuse ayant un drain couplé à la tension d'entrée, et ayant une source couplée à la grille d'un transistor de sortie, de sorte que le transistor de sortie augmente le courant conduit à travers un chemin source - drain connecté entre la tension d'entrée et un noeud de sortie ;
générer le reflet du courant conduit par le transistor de sortie avec un transistor de miroir ;
en réponse à une augmentation du courant reflété, la mise en conduction d'un premier transistor connecté entre la source du transistor à source suiveuse et une tension de polarisation de référence, pour aider à décharger la grille du transistor de sortie ; et
après l'étape de mise en conduction, la mise en conduction d'un second transistor connecté entre la source du transistor à source suiveuse et la tension de polarisation de référence.

10. Système électronique, comprenant :

une source de tension ;
un circuit générateur de tension de référence ;
une charge ; et
un régulateur de tension, comprenant :

un amplificateur d'erreurs, ayant une première entrée qui permet de recevoir une tension de référence du circuit générateur de tension de référence et ayant une seconde entrée pour produire une tension à une sortie en réponse à une différence dans les tensions à ses première et seconde entrées ;
un transistor à source suiveuse ayant une

Petitioner Micron Ex-1004, 0101

grille couplée à la sortie de l'amplificateur d'erreurs, ayant un drain connecté à une tension d'entrée issue de la source de tension, et ayant une source ;

une source de courant, couplée entre la source du transistor à source suiveuse et une tension de polarisation de référence ;

une branche de sortie, qui comprend un transistor de sortie MOS ayant un chemin source - drain couplé entre la tension d'entrée et un noeud de sortie couplé à la charge, et ayant une grille couplée à la source du transistor à source suiveuse ;

une branche de miroir, qui comprend un transistor MOS de miroir ayant un chemin source - drain couplé d'un côté à la tension d'entrée, et ayant une grille couplée à la source du transistor à source suiveuse ;

un circuit de réaction négative couplé au noeud de sortie et à la seconde entrée de l'amplificateur d'erreurs, qui permet de fournir une réaction à l'amplificateur d'erreurs sur la base de la tension au noeud de sortie ;

un premier transistor de réaction positive ayant un chemin de conduction connecté en parallèle à la source de courant, ayant une électrode de commande couplée à la branche de miroir ;

un réseau de retard, couplé à l'électrode de commande du premier transistor de réaction positive, qui permet de retarder la réponse de l'électrode de commande du premier transistor de réaction positive ; et

un second transistor de réaction positive ayant un chemin de conduction connecté en parallèle à la source de courant, et ayant une électrode de commande couplée à la branche de miroir, le second transistor de réaction positive ayant une réponse plus rapide que le premier transistor de réaction positive.

Petitioner Micron Ex-1004, 0102

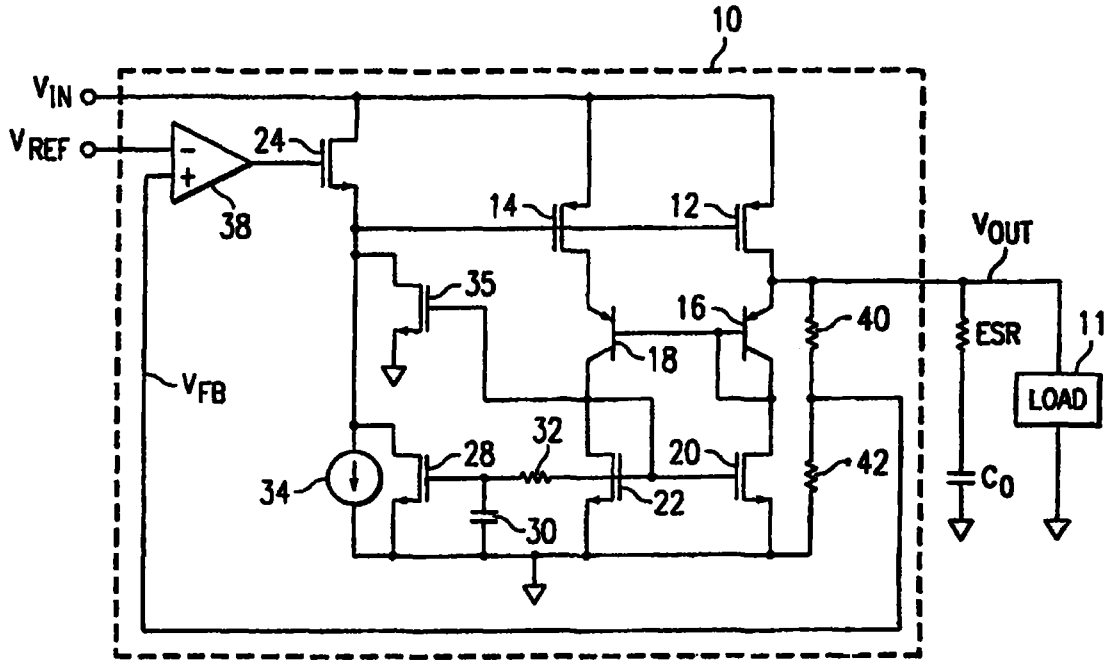


FIG. 1

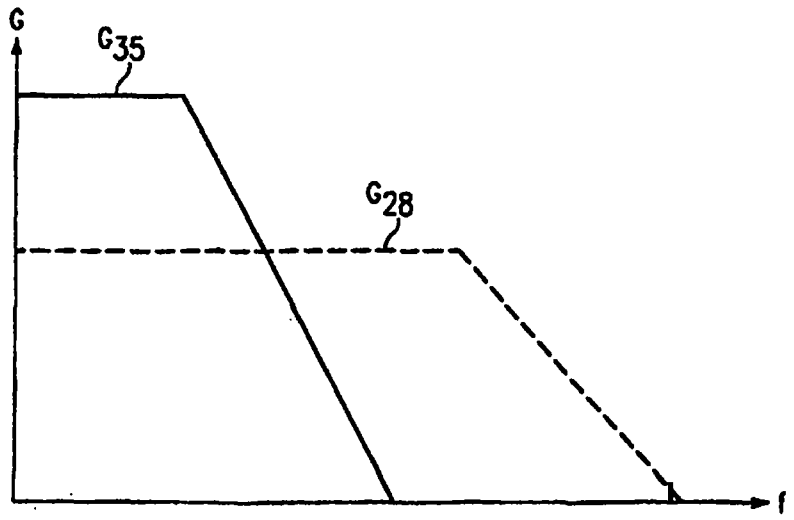


FIG. 3

Petitioner Micron Ex-1004, 0103

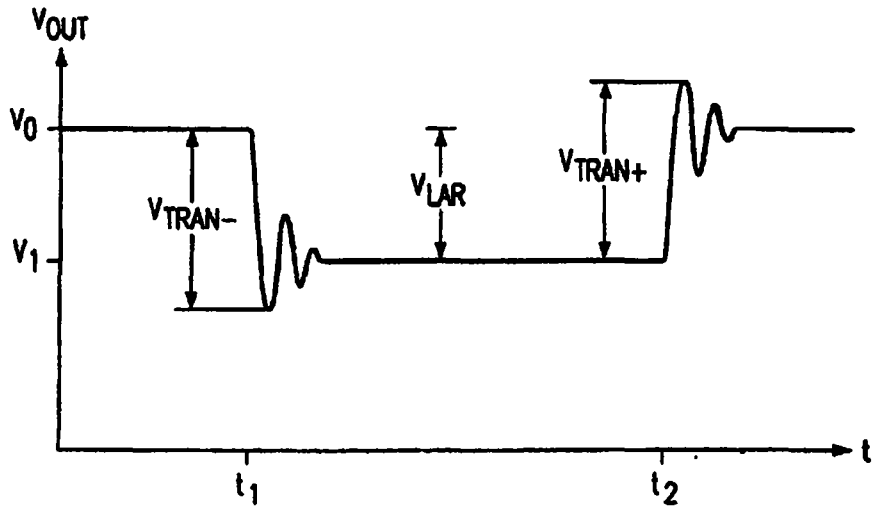


FIG. 2a

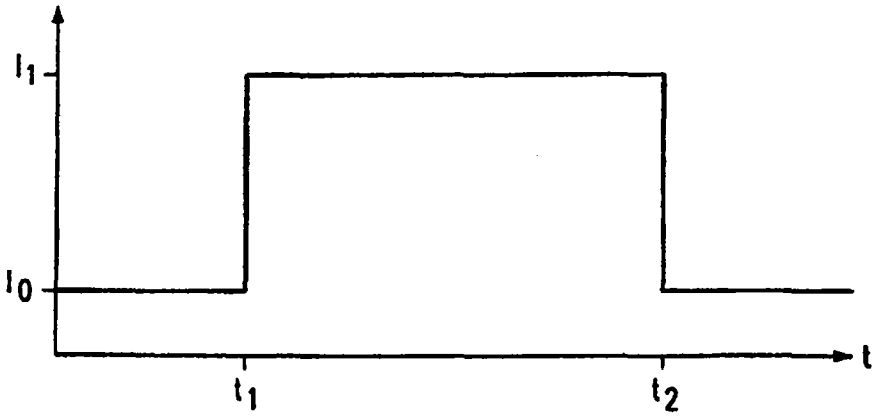


FIG. 2b

Petitioner Micron Ex-1004, 0104

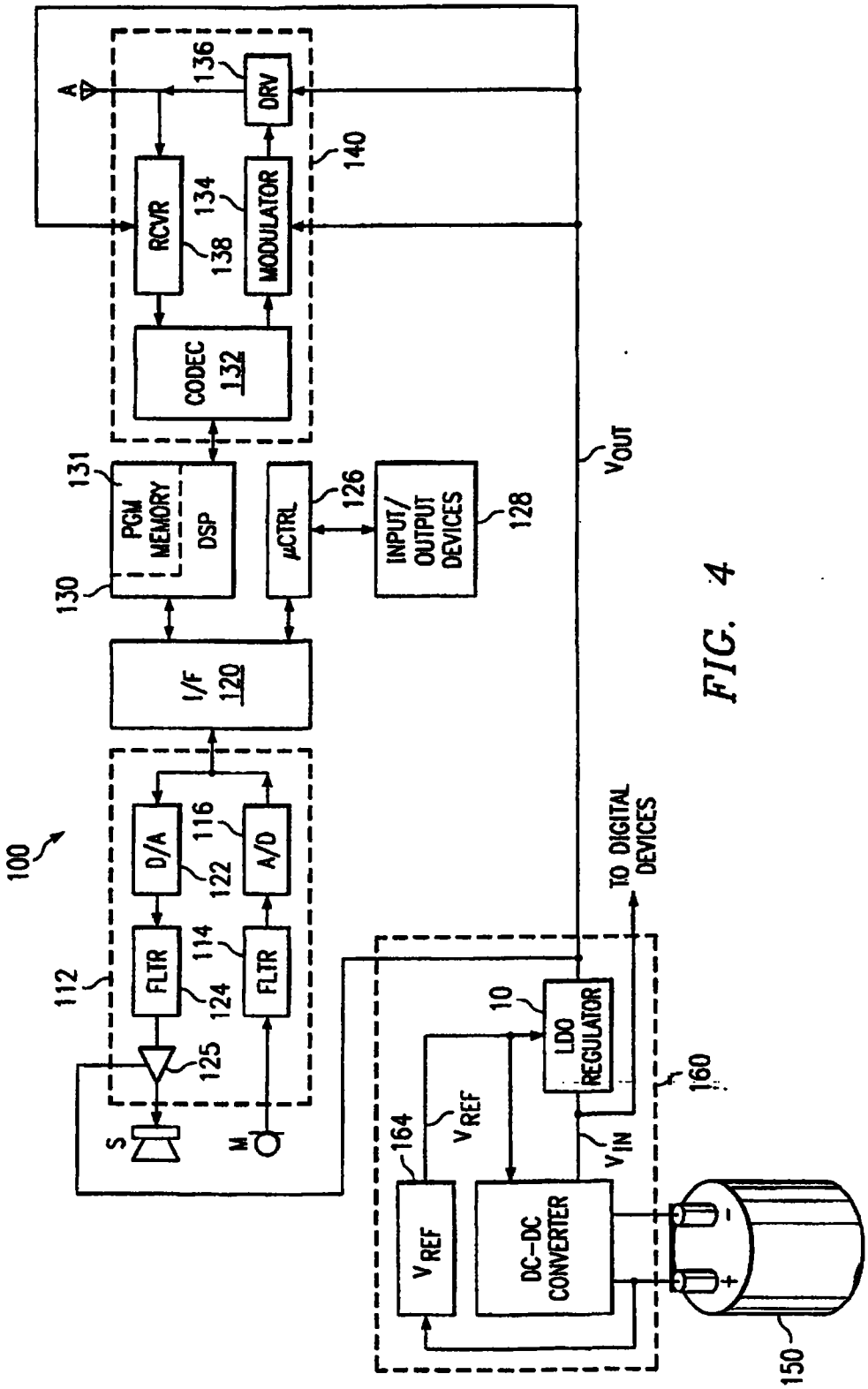


FIG. 4

Petitioner Micron Ex-1004, 0105

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 229 419 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
04.08.2004 Bulletin 2004/32

(51) Int Cl.[7]: **G05F 1/565**

(43) Date of publication A2:
07.08.2002 Bulletin 2002/32

(21) Application number: **02250520.0**

(22) Date of filing: **25.01.2002**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **02.02.2001 US 266077 P**
11.04.2001 US 833299

(71) Applicant: **Broadcom Corporation**
Irvine, California 92618 (US)

(72) Inventor: **Ingino, Joseph M.**
New York, New York 10016 (US)

(74) Representative:
Jehle, Volker Armin, Dipl.-Ing. et al
Patentanwälte
Bosch, Graf von Stosch, Jehle,
Flüggenstrasse 13
80639 München (DE)

(54) Low dropout voltage regulator with high bandwidth and high power supply rejection ratio

(57) A voltage regulator may include one or more features for generating high PSRR. For example, source follower devices may be included in the voltage regulator for providing current sources for the output voltage nodes. The source followers may be sensitive to power supply noise at the gate terminal. Filters are included on the gate terminals to filter the power supply noise, thus reducing the noise at the gate terminals. As another example, the voltage regulator may employ current sources on the output voltage nodes which produce current inversely proportional to the current drawn by the load. In one embodiment, the voltage regulator may include a power control circuit used to provide overvoltage protection during power up. The power control circuit provides a voltage during power up, and ceases providing the voltage after a time interval so that the circuit may operate.

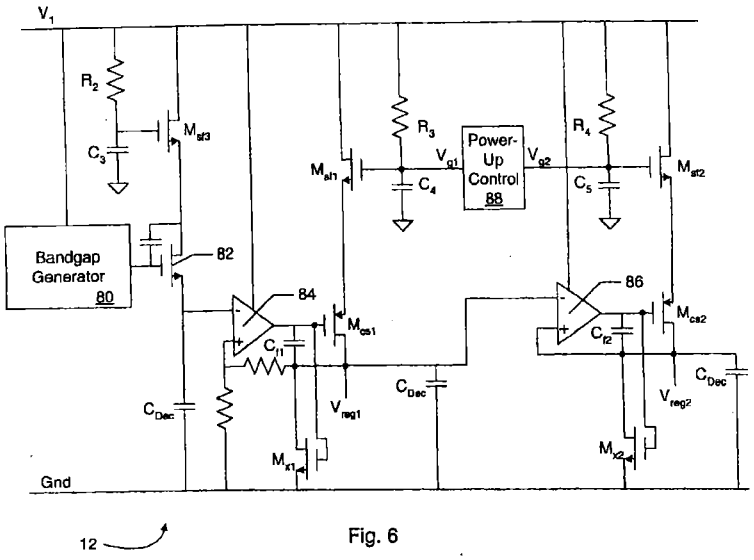


Fig. 6

Printed by Jouve, 75001 PARIS (FR)

EP 1 229 419 A3

Petitioner Micron Ex-1004, 0106

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 0520

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 6 018 265 A (KESHTBOD PARVIZ) 25 January 2000 (2000-01-25)	1-18	G05F1/565
A	* the whole document *	19-22	
X	EP 0 661 616 A (AT & T CORP) 5 July 1995 (1995-07-05)	1-9,16	
A	* the whole document *	10-15, 17-22	
X	US 5 191 278 A (CARPENTER BRIAN A) 2 March 1993 (1993-03-02)	1,9,16	
A	* the whole document *	2-8, 10-15, 17-22	
P,X	US 6 313 615 B1 (FAYNEH EYAL ET AL) 6 November 2001 (2001-11-06) * the whole document *	1-22	
P,X	US 6 278 320 B1 (VU LUAN) 21 August 2001 (2001-08-21) * the whole document *	1,9,16	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	14 June 2004	Schobert, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

Petitioner Micron Ex-1004, 0107

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 02 25 0520

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

14-06-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6018265 A	25-01-2000	AU 1816699 A	28-06-1999
		EP 1058870 A1	13-12-2000
		JP 3418175 B2	16-06-2003
		JP 2001526420 T	18-12-2001
		WO 9930216 A1	17-06-1999
EP 0661616 A	05-07-1995	US 5512817 A	30-04-1996
		EP 0661616 A2	05-07-1995
		JP 7249949 A	26-09-1995
US 5191278 A	02-03-1993	JP 2527888 B2	28-08-1996
		JP 5216548 A	27-08-1993
US 6313615 B1	06-11-2001	US 2002030471 A1	14-03-2002
US 6278320 B1	21-08-2001	NONE	

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Petitioner Micron Ex-1004, 0108

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 602 163 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
08.01.1997 Bulletin 1997/02

(21) Application number: **92919601.2**

(22) Date of filing: **03.09.1992**

(51) Int Cl.[6]: **H03F 3/45**

(86) International application number:
PCT/CA92/00381

(87) International publication number:
WO 93/05572 (18.03.1993 Gazette 1993/08)

(54) **POWER AMPLIFIER WITH QUIESCENT CURRENT CONTROL**

Leistungsverstärker mit signalabhängiger Ruhestromeinstellung

AMPLIFICATEUR DE PUISSANCE A REGULATION DU COURANT DE REPOS

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **06.09.1991 CA 2050878**

(43) Date of publication of application:
22.06.1994 Bulletin 1994/25

(73) Proprietor: **MITEL CORPORATION**
Kanata Ontario K2K 1X3 (CA)

(72) Inventor: **MOLNAR, Gerald**
Ottawa, Ontario K2C 1K8 (CA)

(74) Representative: **Harding, Richard Patrick et al**
A. R. Davies & Co.
27 Imperial Square
Cheltenham GL50 1RQ (GB)

(56) References cited:
EP-A- 0 138 261 **EP-A- 0 325 299**

- **IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 34, February 1991, NEW YORK US pages 278 - 279 G. NICOLLINI ET AL 'A-78db THD 100 OHM DIFFERENTIAL DRIVER FOR ISDN APPLICATIONS'**
- **NEUES AUS DER TECHNIK no. 1, 20 February 1987, WURZBURG DE page 1**
- **'OPERATIONSVERSTARKER'**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Jouve, 75001 PARIS (FR)

EP 0 602 163 B1

Petitioner Micron Ex-1004, 0109

Description

This invention relates to a power amplifier with a differential output and differential input, for example, suitable for use as a driver circuit for moving coil transducers, such as earpieces and speakers employed in telephone sets.

Modern telephone circuitry may be implemented in CMOS integrated circuits. Suitable drivers must be provided to interface with discrete moving coil transducer components, such as the earpieces and speakers employed in modern telephone sets. Generally, the drivers must be capable of supplying high power to the load at low D.C. bias voltages, and for this purpose fully differential amplifiers, which have a differential output and differential input, can be employed to advantage because of their ability to produce a high output power from the 5V CMOS voltage supply (No special power supply is required). The drivers must, however, have linear transfer characteristics, a very high input impedance in order to interface with the CMOS circuitry, a stable frequency response and be insensitive to process variations.

Two major problems must be addressed, namely the control of the common mode voltage associated with fully differential designs and the D.C. quiescent current associated CMOS amplifiers with large output transistors. The high load currents and large dimensions of the output transistors in the amplifier imply a high sensitivity of quiescent current to process variations and biasing. Small deviations in the gate voltages of the output transistors can lead to quiescent currents that greatly exceed desired requirements. Typical such cicuits are described in EP 0325 299, NEUES AUS DER TECHNIK, no. 1, 20 Feb. 1987, page 1, "OPERATIONSVERSTARKER", and IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE, Vol. 34, Feb 1991, New York, US, pages 278-279 G Nicollini et al. "A-78db THD 100 OHM DIFFERENTIAL DRIVER FOR ISDN APPLICATIONS".

The driver should also have high gain, inherent stability and simplicity of implementation. These features have proved difficult in the past to achieve.

According to the present invention there is provided a power amplifier comprising an input stage and an output state, the input stage having a fully differential amplifier with differential inputs and differential outputs, and a high input impedance closed loop common mode feedback control circuit deriving common mode feedback control signals from said differential outputs. Each said output stage comprises for each differential output of the input stage a class AB amplifier providing an output of the power amplifier and having N-channel and P-channel source followers interfacing with said fully differential amplifier and a quiescent current control input for maintaining a desired quiescent current, means for maintaining the common mode output voltage of the class AB amplifiers at a desired level, and a quiescent current regulator for supplying a common control signal to said quiescent current control inputs, said quiescent current regulator including transistor means configured to mimic the behavior of one of said source followers so as to generate said common control signal.

The quiescent current regulator preferably includes a pair of transistors that mimic the N-channel source follower of one of the class AB amplifiers. The gate of one of the mimic transistors is set to the quiescent state voltage of the input stage output. The drain voltage of the second mimic transistor corresponds to the drain voltage of one of a pair of transistors forming the N-channel follower connected to the gate of the N-channel driver transistor in the output stage and thus represents its gate voltage. The gate voltage of the second mimic transistor is used to bias the N-channel source follower of the output stage. A reference voltage generated at the input of the quiescent current regulator is effectively mirrored into the N-channel driver transistor of the output stage and can thus be used to determine the quiescent current of the output stage. This circuit results in an amplifier quiescent current that is insensitive to process variations.

The present invention is of two-stage design, in which the input stage is a preferably a folded cascode amplifier, which is characterized by high open loop gain and inherent stability.

In view of the poor output drive capability of the folded cascode amplifier, the common mode voltage control feedback circuit is required to have a very high input impedance (very much greater than 1 Megohm) to the folded cascode amplifier output to prevent the common mode feedback circuit from loading down the first stage and thus reducing its gain. The common mode feedback circuit should also operate in the linear fashion over a wide range of input voltage. Conventional designs are very difficult to realize in, for example, a two micron fabrication process. Thus, the common mode feedback control circuit preferably has a pair of transistors operating in the triode region as a pair of voltage dependent resistors connected to the differential outputs of the folded cascode. Summed current through these transistors is matched a control current used to determine the control signal to the folded cascode common mode control input.

The invention will now be described in more detail, by way of example only, with reference to the accompanying drawings, in which:-

Figure 1 is a block diagram of a power amplifier in accordance with the invention;

Figure 2 is a circuit diagram of a bias circuit for the amplifier;

Figure 3 shows the input stage of the circuit, represented by Stage I in Figure 1;

Figure 4 shows the common mode feedback control

Petitioner Micron Ex-1004, 0110

circuit;

Figure 5 shows a loop response of the common mode control circuit;

Figure 6 shows the first stage with common mode control compensation element;

Figure 7 is a circuit diagram of an output stage speaker driver;

Figure 8 is circuit diagram of a common mode feedback control circuit for the output stage; and

Figure 9 is a circuit diagram of the quiescent current regulator.

Referring now to Figure 1, the driver is broadly divided into two stages, Stage I and Stage II. Stage I includes an input stage 1 receiving a differential input, a common mode feedback control circuit 2, and a circuit 3 for generating bias voltages. The second stage, Stage II comprises an output stage 4, an output common mode feedback control circuit 5, a quiesdent current regulator 6, and a load 7, which may be a speaker or earpiece. The entire circuit, except of course the load, is implemented in two micron CMOS technology.

The bias circuit is shown in more detail in Figure 2. Its main purpose is to provide various reference voltages, Vb0, Vb1, Vb2, Vb3 that track changes due to process variations and external factors (temperature, voltage, etc.) and ensure that the circuits using the bias voltages can be made invariant to these influences.

The bias circuit 3, shown in more detail in Figure 2, includes field effect transistors 8, 9, and 10. A voltage reference V_{iref} is applied to the circuit and calibrated such that transistor 8 serves as a 20µa current source. This reference current is mirrored throughout the transistor chains of the bias network to create the precise reference voltages referred to above. Since each reference voltage Vb0, Vb1, Vb2, Vb3 is related to the 20µa current source, precision current sources can be realized within the amplifier design. Transistors 9 and 10 are made smaller than the transistors in the associated bias chains to ensure that these latter transistors operate in their respective saturation regions.

The input Pd is a power down input signal, which ensures that all currents in the bias chains are reduced to zero on power down. Subsequently, all other current sources within the driver circuit that utilize Vb0 to Vb3 are shut down.

Referring now to Figure 3, the input stage I provides most of the open loop gain for the amplifier circuit. The input stage I plays a major role in influencing PSRR, CMRR, noise and other amplifier characteristics. The input stage is therefore implemented as a fully differential folded cascode amplifier with a differential input and differential output. This approach affords high gain (greater than 60db), inherent stability, and simplicity of implementation.

The differential input has input transistors 11, 12 with respective series transistors 13, 14, having their gates connected together and providing a control input for the stage I output common mode voltage feedback control signal. The outputs of the transistors 11, 12 are connected to transistor chains 15, 16 to which are applied the bias voltage Vb1, Vb2 and Vb3. The outputs of the transistor chains 15, 16 provide the fully differential outputs of the folded cascode amplifier.

The folded cascode implementation has the advantage of providing high gain (greater than 60 dB), inherent stability (folded cascode designs are compensated by the load capacitance), and simplicity of implementation (a small number of transistors).

Transistor 17 provides a 100µa current source for the differential input path 11, 12. Transistors 11, 12 are misfits, which have a channel length of 3µm to promote better matching, i.e minimize output differential offset. The channel width (g_m) associated with these devices (300µm) has a major impact on the overall gain of the first stage. The sizes of transistors 13, 14, and 18, 19 and bias chains 15, 16, are all directly related to the size of the transistors in the reference current (20µa) of the bias chain.

The differential output signals of the first stage are biased at a DC common mode voltage equal to Vdd/2 (Vbias). The common mode output voltage is controlled by varying the gate voltage of transistors 13, 14.

Figure 4 shows the common mode feedback control circuit, which is implemented in a novel manner. The circuit provides common mode output voltage control of a 5V folded cascode operational amplifier, very high input impedance of the folded cascode output, and is capable of linear operation during high voltage swings.

The common mode feedback control circuit comprises a pair of transistors 20, 21 connected to the fully differential output of the input stage 1. Transistors 20, 21 are connected in a first path 22 with series transistors 23, 24. Current I_1 flows through this path into transistors 20, 21. This path is in parallel with the second path consisting of a series combination of transistors 25, 26 and the parallel combination of transistors 27, 28 receiving at their gate, bias voltage V_{bias}.

Transistors 27, 28 function as current sources with current I_0 being a function of the reference voltage Vbias. The gate voltage transistor 25 must be such that the drain current is equal to I_0. Once transistors 24 and 25 are matched and the gate voltage is common, I_0 must be equal to I_1 and hence the drain currents of transistors 20, 21 must sum to I_0. This is only be true if the common mode voltage at the output of the folded cascode is equal to V_{bias}.

The transistors 20, 21 thus act as voltage dependent resistors. In order to ensure linearity over wide swings of gate voltage, they are operated in the triode region, and this is accomplished by forcing the drains of

Petitioner Micron Ex-1004, 0111

transistors 27, 28, 20, 21 to a low voltage with transistors 23, 26. The absolute value of I_0 is determined by the size of transistors 27, 28 and the value of the voltage V_{bias}. These transistors have a high impedance (W=15μm, L=40μm) in order to keep the circuit current low.

Since the common mode control is a closed loop system, stability is important. To quantify the gain and phase response, the closed loop must be opened and the appropriate measurements taken (see Figure 5). Compensation elements can then be added to compensate for the frequency response. Figure 6 shows the input stage 1 and common mode feedback control circuit 2 with compensation elements 29.

Figure 7 shows an output stage for the amplifier. Two such output stages are provided, one for each differential output of the input Stage I. The main purpose of the circuit shown in Figure 7 is to buffer, i.e. provide current gain, for the outputs of the folded cascode input stage I.

The circuit shown in figure 7 comprises two output transistors, 30, 31 driven in a class AB manner. The size of transistors 30, 31 is determined by the output current (i.e. minimum load resistance or maximum load gm) that the amplifier must drive. N-channel and P-channel source followers, defined by transistors 32, 33 and 34, 35 respectively are provided. In the quiescent state, which is defined at V_0 equal to V_{bias} (nominally Vdd/2), the gate voltage of transistor 31 is barely over the threshold, and thus the drain current of transistor 31 defines the quiescent current of the output stage. If V_{iset} is assumed to be a bias voltage that ensures the quiescent drain current of transistor 31 is held at a predetermined level, the quiescent voltage value of the output is controlled by manipulating Vds of transistor 30 given the drain current defined by transistor 31. The gate voltage of transistor 30 is varied by altering the current in the P-channel source follower (transistors 34, 35) by changing the gate voltage of transistor 35. The signal CM_{CTL} is a control signal emanating from the output stage common mode feedback control circuit to be described in more detail below.

Consequently, in the quiescent state the output voltage is fixed at a predetermined value and the supply current drawn by the circuit is controlled. A positive deviation on Vo (the AC signal) results in an increased gate voltage at transistor 31 and a corresponding shut off of transistor 30. A negative deviation of Vo yields an increased turn on of transistor 30 and turn off of transistor 31, thus ensuring the Class AB operating conditions are maintained. Additional transistors 36, 37 ensure that no supply current is used in the power down state. These transistors have no effect on the circuit during normal operation.

The passive components shown in Figure 7 ensure AC compensation of the complete driver. In determining the values of these components, the following requirements must be taken into consideration:

- Reduction of the quiescent current in M1 and M2 reduces phase margin (increased impedance)
- M1 and M2 have large values of C_{GS}. The capacitance forms a pole with the output impedance of the source followers.

Referring now to figure 8, this shows the common mode feedback control circuit for the output stage. The outputs of each amplifier are resistively summed by resistors 38, 39 to extract the common mode voltage. A differential amplifier consisting of transistors 40, 41 is then used to compare this with the bias (nominally V_{DD}/2). The differential amplifier generates the control signal CM_{CTL} (shown in figure 7) to generate the output common mode voltage control signal.

Referring now to Figure 9, the quiescent current regulator is designed to regulate the output stage quiescent current over wide process and temperature variations. The quiescent current regulator meshes with the output stage to effectively control the quiescent current.

In Figure 9, transistor 42 forms a 10μa current source. Transistor 43, in series with transistor 42, is connected as a diode device and thus forms a voltage reference for the circuit. The magnitude of the current I_o and the size of the transistor M2 are both related to quiescent current in the output stage of the amplifier.

The current I_o flowing through transistor 42 is mirrored into transistor 44, which is connected in series with a matched transistor 45. Transistors 44 and 45 are in turn parallel with series combination of transistors 46, 47.

Output transistors 48, 49 have as their main function to mimic the N-channel voltage follower (33, 32) in the output stage (Figure 7). The gate of transistor 48 is set to V_{bias}, which is the desired quiescent state value of the folded cascode output. The drain voltage of transistor 49 is connected to the gate of transistor 46. Transistors 45 and 47 are matched and have a common gate voltage.

The current I_o is mirrored into transistor 44 as previously indicated. The drain current of transistor 44 is the same as the drain current of transistor 45, and due to the matching of transistors 45 and 47, as well as their common gate voltage, the drain current of transistor 47 must equal the drain current of transistor 45. This means that the gate voltage of transistor 46 must be the same as the gate voltage of transistor 44, and this will only occur is adequate loop gain exists from the gate of transistor 46 to the drain of transistor 49.

Since the main function of transistors 48, 49 is to mimic the N-channel voltage follower in the output stage of the amplifier, the drain voltage of transistor 49 represents the gate voltage of the N-channel driver transistor in the output stage (transistor 31, Figure 7). This means that the voltage at the drain of transistor 49 is related to the output stage quiescent current.

The gate voltage of transistor 49 (V_{iset}) can there-

Petitioner Micron Ex-1004, 0112

fore be used to bias the N-channel source followers (transistors 32, 33) of each amplifier in the output stage. The voltage generated at transistor 49 is effectively mirrored into the N-channel driver transistor of the output stage, and the sizing of transistor 43 and the magnitude of I_0 determine the quiescent current of the output stage in each amplifier. The above design results in an amplifier quiescent current which is insensitive to process variations.

The above described circuit provides a simple design for a power amplifier that can implemented in CMOS technology in a simple and effective manner, and which is relatively insensitive to variations in process parameters.

Claims

1. A power amplifier comprising an input stage (1) and an output state (4), the input stage (1) having a fully differential amplifier (M1 ... M5 in Fig. 3) with differential inputs and differential outputs, and a high input impedance closed loop common mode feedback control circuit (2) deriving common mode feedback control signals from said differential outputs, characterized in that said output stage (4) comprises for each differential output of the input stage a class AB amplifier (30, 31) providing an output of the power amplifier and having N-channel and P-channel source followers (32, 33, 34, 35) interfacing with said fully differential amplifier and a quiescent current control input for maintaining a desired quiescent current, means (5) for maintaining the common mode output voltage of the class AB amplifiers at a desired level, and a quiescent current regulator (6) for supplying a common control signal to said quiescent current control inputs, said quiescent current regulator (6) including transistor means (48, 49) configured to mimic the behavior of one (32, 33) of said source followers so as to generate said common control signal.

2. A power amplifier as claimed in claim 1, characterized in that said transistor means includes a pair of transistors (48, 49) that mimic one (32, 33) of the source followers of (32, 33) said one of the class AB amplifiers (30, 31), the gate of one of the mimic transistors (48) is set to the quiescent state voltage (V_{bias}) of the input stage output, the drain voltage of the second mimic transistor (49) corresponds to the drain voltage of one (32) of a pair of transistors (32, 33) forming said one follower which is connected to the gate of an associated driver (31) transistor in the input stage, and the gate voltage (V_{iset}) of the second mimic transistor (49) is used to bias said one source follower of the output stage, whereby a reference voltage generated at the input of the quiescent current regulator (6) is effectively mirrored into the associated driver transistor (31) of the output stage and determines the quiescent current of the output stage.

3. A power amplifier as claimed in claim 2, characterized in that said one source follower (32) is the N-channel source follower and said associated driver transistor is the N-channel driver transistor (31).

4. A power amplifier as claimed in claim 2, characterized in that for each class AB amplifier (30, 31), a first (32, 33) of said source followers maintains the gate voltage of one driver transistor (31) just over threshold value in the quiescent state so that the drain current of said driver transistor (31) determines the quiescent current of the ouptut stage and has a control input determining the level of said quiescent driver current, and a second (34, 35) of said followers determines the quiescent voltage output by determining the source - drain voltage of the other (30) of said class AB driver transistors in response to an output common mode feedback control signal (CM_{CTL}).

5. A power amplifier as claimed in claim 4, characterized in that it further comprises means (38, 39) for summing the separate outputs for each class AB driver amplifier (30, 31), and a differential amplifier (40, 41) for comparing the result of the summation to a reference voltage (V_{bias}) to produce said output common mode control signal.

6. A power amplifier as claimed in claim 5, characterized in that said quiescent current regulator (6) further comprises a current source transistor (42) supplying current to a diode-connected transistor (43) providing said reference voltage source, a first transistor (44) having its gate connected to said diode-connected transistor (43) so that the current generated by the current source transistor is mirrored thereinto, said first transistor (44) being in series with a second transistor (45), and said first and second transistors (44, 45) being in parallel with a series combination of third and fourth transistors (46, 47), the said second and fourth transistors (45, 47) being matched and their gates being connected together such that the driver current in the second and fourth transistors (45, 47) is the same, the drain of said mimicking transistor (49), being connected to the gate of the third transistor (46), and the gate of said one mimicking transistor (49) being connected to the drain of the first transistor.

7. A power amplifier as claimed in claim 1, characterized in that said differential amplifier (Fig. 3) of the input stage is folded cascode amplifier.

8. A power amplifier as claimed in claim 7, character-

Petitioner Micron Ex-1004, 0113

ized in that said common mode voltage feedback control circuit (2) comprises a pair of voltage-dependent resistor means (20, 21) connected to said differential outputs (15, 16) of the folded cascode amplifier, means (25, 26, 27, 28) for producing a reference current (I_o) dependent on a bias voltage equal to the desired common mode voltage of the folded cascode amplifier, and means (Fig. 4) for ensuring that the sum I_1 of the currents flowing through said pair of voltage-dependent resistor means (20, 21) is equal to said reference current, and means (Fig. 4) for deriving a common mode voltage signal from said reference current (I_o) to maintain the common mode output voltage of said cascode amplifier equal to said reference voltage.

9. A power amplifier as claimed in claim 8, characterized in that said voltage-dependent resistor means (20, 21) comprise transistors (20, 21) operating in the triode region.

10. A power amplifier as claimed in claim 8 or 9, characterized in that said common mode voltage feedback control circuit (2) comprises first and second parallel paths through which said respective currents I_o and I_1 flow, said first path including a pair of parallel-connected transistors (27, 28) with their gates tied to said reference voltage (V_{bias}) serving as a current sources and being in series with a further transistor (25), and said second path including said pair of voltage-dependent resistors (20, 21) in series with a further transistor (24), the further transistors (25, 24) of the respective paths being matched and having their gates connected together to ensure that the currents in the two paths remain the same, and the common mode feedback control signal being produced at said further transistor (25) in the first path.

11. A power amplifier as claimed in claim 10, comprising an additional transistor (26, 23) in each said path, said additional transistors (26, 23) having their gates connected together and tied to a second reference voltage source (Vb2).

Patentansprüche

1. Ein Leistungsverstärker mit einer Eingangsstufe (1) und einer Ausgangsstufe (4), wobei die Eingangsstufe (1) einen vollständigen Differenzverstärker (Fig. 3) mit Differenz-Eingängen und Differenz-Ausgängen aufweist, und mit einer Geschlossenschleifen-Gesamtbetriebsart-Rückkopplungs-Steuerschaltung (2) mit hoher Eingangsimpedanz, die von den Differenz-Ausgängen Gesamtbetriebsart-Rückkopplungs-Steuersignale ableitet,
dadurch gekennzeichnet,

daß die Ausgangsstufe (4) für jeden Differenz-Ausgang der Eingangsstufe einen AB-Typ-Verstärker (30, 31), der einen Ausgang des Leistungsverstärkers zur Verfügung stellt und N-Kanal- und P-Kanal-Source-Folger (32, 33, 34, 35) umfaßt, die mit dem vollständigen Differenzverstärker und einem Ruhestrom-Steuereingang zum Aufrechterhalten eines gewünschten Ruhestroms eine Schnittstelle aufweisen, Mittel (5) zum Aufrechterhalten der Gesamtbetriebsart-Ausgangsspannung des AB-Typ-Verstärkers auf einem gewünschten Pegel und einen Ruhestrom-Regler (6) zum Zuführen eines gemeinsamen Steuersignals an die Ruhestrom-Steuereingänge aufweist, wobei der Ruhestrom-Regler (6) Transistor-Mittel (48, 49) umfaßt, die so beschaffen sind, daß sie das Verhalten eines (32, 33) der Source-Folger nachbilden, um das gemeinsame Steuersignal zu erzeugen.

2. Ein Leistungsverstärker nach Anspruch 1,
dadurch gekennzeichnet,

daß die Transistor-Mittel ein Paar Transistoren (48, 49) aufweisen, die einen (32, 33) der Source-Folger (32, 33) des einen AB-Typ-Verstärkers (30, 31) nachbilden,
daß das Gate eines der nachbildenden Transistoren (48) auf die Ruhezustands-Spannung (V_{bias}) des Ausgangs der Eingangsstufe gesetzt ist,
daß die Drain-Spannung des zweiten nachbildenden Transistors (49) der Drain-Spannung eines (32) von zwei Transistoren (32, 33) entspricht, die den einen Folger bilden, der mit dem Gate eines zugehörigen Treiber-Transistors (31) in der Eingangsstufe verbunden ist, und
daß die Gate-Spannung (V_{iset}) des zweiten nachbildenden Transistors (49) zum Vorspannen des einen Source-Folgers der Ausgangsstufe benutzt wird, wobei eine Referenzspannung, die am Eingang des Ruhestrom-Reglers (6) erzeugt wird, in den zugehörigen Treiber-Transistor (31) der Ausgangsstufe wirksam gespiegelt wird und den Ruhestrom der Ausgangsstufe bestimmt.

3. Ein Leistungsverstärker nach Anspruch 2,
dadurch gekennzeichnet,
daß der eine Source-Folger (32) ein N-Kanal-Source-Folger ist und daß der zugehörige Treiber-Transistor der N-Kanal-Treiber-Transistor (31) ist.

4. Ein Leistungsverstärker nach Anspruch 2,
dadurch gekennzeichnet,
daß für jeden der AB-Typ-Verstärker (30, 31) ein erster (32, 33) der Source-Folger eine Gate-Spannung eines Treiber-Transistors (31) etwas über

Petitioner Micron Ex-1004, 0114

dem Schwellwert in dem Ruhezustand aufrechterhält, so daß der Drain-Strom des Treiber-Transistors (31) den Ruhestrom der Ausgangsstufe bestimmt, und dieser einen Steuereingang aufweist, der den Pegel des Ruhe-Treiberstromes bestimmt, und ein zweiter (34, 35) der Folger den Ruhespannungs-Ausgang durch Festlegen der Source-Drain-Spannung des anderen (30) der AB-Typ-Treiber-Transistoren in Abhängigkeit von einem Ausgangs-Gesamtbetriebsart-Rückkopplungs-Steuersignal (CM_{CTL}) bestimmt.

5. Ein Leistungsverstärker nach Anspruch 4, **dadurch gekennzeichnet,** daß dieser des weiteren Mittel (38, 39) zum Summieren der separaten Ausgänge jedes AB-Typ-Treiber-Verstärkers (30, 31) und einen Differenz-Verstärker (40, 41) zum Vergleichen des Ergebnisses der Summation mit einer Referenz-Spannung (V_{bias}) aufweist, um das Ausgangs-Gesamtbetriebsart-Steuersignal zu erzeugen.

6. Ein Leistungsverstärker nach Anspruch 5, **dadurch gekennzeichnet,**

daß der Ruhestrom-Regler (6) des weiteren einen Stromquellen-Transistor (42), der einem diodenverbundenen Transistor (43), der die Referenz-Spannungsquelle zur Verfügung stellt, Strom zuführt, und
einen ersten Transistor (44), dessen Gate mit dem diodenverbundenen Transistor (43) so verbunden ist, daß der von dem Stromquellen-Transistor erzeugte Strom dort hinein gespiegelt wird, aufweist,
wobei der erste Transistor (44) mit dem zweiten Transistor (45) in Serie geschaltet ist und der erste und zweite Transistor (44, 45) mit einer Serien-Kombination des dritten und vierten Transistors (46, 47) parallel geschaltet sind, wobei der zweite und vierte Transistor (45, 47) einander angepaßt sind und ihre Gates miteinander verbunden sind, so daß der Treiberstrom in dem zweiten und vierten Transistor übereinstimmt, wobei der Drain des nachbildenden Transistors (49) mit dem Gate des dritten Transistors (46) verbunden ist und wobei das Gate des einen nachbildenden Transistors (49) mit dem Drain des ersten Transistors verbunden ist.

7. Ein Leistungsverstärker nach Anspruch 1, **dadurch gekennzeichnet,** daß der Differenz-Verstärker (Fig. 3) der Eingangsstufe ein gefalteter Kaskoden-Verstärker ist.

8. Ein Leistungsverstärker nach Anspruch 7, **dadurch gekennzeichnet,**

daß die Gesamtbetriebsart-Spannungsrückkopplungs-Steuerschaltung (2) ein Paar spannungsabhängige Widerstandsmittel (20, 21), die mit den Differenz-Ausgängen (15, 16) des gefalteten Kaskoden-Verstärkers verbunden sind,
Mittel (25, 26, 27, 28) zum Erzeugen eines Referenzstroms (Io) abhängig von einer Vorspannung, die gleich der gewünschten Gesamtbetriebsart-Spannung des gefalteten Kaskoden-Verstärkers ist,
Mittel (Fig. 4) zum Sicherstellen, daß die Summe I_1 der durch das Paar der spannungsabhängigen Widerstandsmittel (20, 21) fließenden Ströme gleich dem Referenzstrom ist, und
Mittel (Fig. 4) zum Ableiten eines Gesamtbetriebsart-Spannungssignals von dem Referenzstrom (Io) zum Aufrechterhalten der Gesamtbetriebsart-Ausgangsspannung des Kaskoden-Verstärkers in Übereinstimmung mit der Referenzspannung, aufweist.

9. Ein Leistungsverstärker nach Anspruch 8, **dadurch gekennzeichnet,** daß die spannungsabhängigen Widerstandsmittel (20, 21) Transistoren (20, 21) umfassen, die im Trioden-Bereich arbeiten.

10. Ein Leistungsverstärker nach Anspruch 8 oder 9, **dadurch gekennzeichnet,** daß die Gesamtbetriebsart-Spannungsrückkopplung-Steuerschaltung (2) erste und zweite parallele Pfade aufweist, durch welche die entsprechenden Ströme I_0 und I_1 fließen, wobei der erste Pfad ein Paar parallel geschalteter Transistoren (27, 28) aufweist, deren Gates mit der Referenzspannung (V_{bias}), die als Stromquelle dient, verbunden sind und die mit einem weiteren Transistor (25) in Serie geschaltet sind, und wobei der zweite Pfad das Paar spannungsabhängiger Widerstände (20, 21) in Serie mit einem weiteren Transistor (24) aufweist, wobei die weiteren Transistoren (25, 24) der entsprechenden Pfade einander angepaßt sind und deren Gates miteinander verbunden sind, um sicherzustellen, daß die Ströme in den beiden Pfaden die gleichen bleiben, und wobei das Gesamtbetriebsart-Rückkopplungs-Steuersignal an dem weiteren Transistor (25) in dem ersten Pfad erzeugt wird.

11. Ein Leistungsverstärker nach Anspruch 10, mit einem zusätzlichen Transistor (26, 23) in jedem Pfad, wobei die Gates der zusätzlichen Transistoren (26, 23) miteinander und mit einer zweiten Referenz-Spannungsquelle (Vb2) verbunden sind.

Petitioner Micron Ex-1004, 0115

Revendications

1. Amplificateur de puissance comprenant un étage d'entrée (1) et un étage de sortie (4), l'étage d'entrée (1) comportant un amplificateur entièrement différentiel (Fig. 3) avec des entrées différentielles et des sorties différentielles, et un circuit de commande (2) à rétroaction de mode commun en boucle fermée et à entrée haute impédance, générant des signaux de commande à rétroaction de mode commun à partir desdites sorties différentielles, caractérisé en ce que ledit étage de sortie (4) comprend, pour chaque sortie différentielle de l'étage d'entrée, un amplificateur (30, 31) de classe AB constituant une sortie de l'amplificateur de puissance et doté de circuits suiveurs de source (32, 33, 34, 35) à canal N et à canal P assurant l'interface avec ledit amplificateur entièrement différentiel et une entrée de commande de courant de repos pour maintenir un courant de repos voulu, un moyen (5) pour maintenir la tension de sortie de mode commun des amplificateurs de classe AB à un niveau voulu et un régulateur de courant de repos (6) pour fournir un signal de commande commun auxdites entrées de commande de courant de repos, ledit régulateur de courant de repos (6) comportant un moyen à transistors (48, 49) configuré de façon à simuler le comportement de l'un (32, 33) desdits circuits suiveurs de source de façon à générer ledit signal commun de commande.

2. Amplificateur de puissance selon la revendication 1, caractérisé en ce que ledit moyen à transistors comporte une paire de transistors (48, 49) qui reproduisent l'un (32, 33) des circuits suiveurs de source (32, 33) de l'un susdit des amplificateurs (30, 31) de classe AB, la gâchette de l'un (48) des transistors de simulation étant mise au potentiel de repos (V_{pol}) de la sortie de l'étage d'entrée, le potentiel de drain du second transistor de simulation (49) correspondant au potentiel de drain de l'un (32) des transistors d'une paire de transistors (32, 33) formant le circuit suiveur susdit qui est relié à la gâchette d'un transistor préamplificateur (31) associé dans l'étage d'entrée, la tension de gâchette (V_{iset}) du second transistor de simulation (49) étant utilisée pour polariser ledit premier circuit suiveur de source de l'étage de sortie, une tension de référence générée à l'entrée du régulateur de courant de repos (6) étant effectivement reproduite dans le transistor préamplificateur associé (31) de l'étage de sortie et déterminant le courant de repos de l'étage de sortie.

3. Amplificateur de puissance selon la revendication 2, caractérisé en ce que le circuit suiveur de source (32) susdit est le circuit suiveur de source à canal N et ledit transistor préamplificateur associé est le transistor préamplificateur (31) à canal N.

4. Amplificateur de puissance selon la revendication 2, caractérisé en ce que pour chaque amplificateur (30, 31) de classe AB, un premier (32, 33) desdits circuits suiveurs de source maintient la tension de gâchette d'un transistor préamplificateur (31) juste au-dessus de la valeur de seuil à l'état de repos, de telle sorte que le courant de drain dudit transistor préamplificateur (31) détermine le courant de repos de l'étage de sortie, son entrée de commande déterminant le niveau dudit courant de repos du préamplificateur, et le second (34, 35) desdits circuits suiveurs détermine la sortie de tension de repos en fixant la tension source / drain de l'autre (30) desdits transistors préamplificateurs de classe AB en réponse à un signal de commande de sortie à rétroaction de mode commun (CM_{CTL}).

5. Amplificateur de puissance selon la revendication 4, caractérisé en ce qu'il comprend, en outre, un moyen (38, 39) pour effectuer la sommation des sorties séparées de chaque préamplificateur (30, 31) de classe AB et un amplificateur différentiel (40, 41) pour comparer le résultat de la sommation à la tension de référence (V_{pol}) afin de produire ledit signal de commande de sortie à rétroaction de mode commun.

6. Amplificateur de puissance selon la revendication 5, caractérisé en ce que ledit régulateur de courant de repos (6) comprend en outre un transistor de source de courant (42) alimentant en courant un transistor associé à une diode (43) qui constitue ladite source de tension de référence, un premier transistor (44) dont la gâchette est reliée audit transistor associé à une diode (43) de façon à ce que le courant produit par le transistor de source de courant soit reproduit dans celui-ci, ledit premier transistor (44) étant en série avec un deuxième transistor (45), lesdits premier et deuxième transistors (44, 45) étant en parallèle avec le montage série constitué par un troisième et un quatrième transistors (46, 47), lesdits deuxième et quatrième transistors (45, 47) étant appariés et leurs gâchettes étant reliées entre elles de telle sorte que le courant d'attaque des deuxième et quatrième transistors (45, 47) soit identique, le drain dudit transistor de simulation (49) étant relié à la gâchette du troisième transistor (46) et la gâchette dudit transistor de simulation (49) étant reliée au drain du premier transistor.

7. Amplificateur de puissance selon la revendication 1, caractérisé en ce que ledit amplificateur différentiel (Fig. 3) de l'étage d'entrée est un amplificateur cascode replié.

8. Amplificateur de puissance selon la revendication

Petitioner Micron Ex-1004, 0116

7, caractérisé en ce que ledit circuit de commande à rétroaction de mode commun (2) comprend une paire de moyens à résistance variable en fonction de la tension (20, 21) reliée auxdites sorties différentielles (15, 16) de l'amplificateur cascode replié, un moyen (25, 26, 27, 28) pour produire un courant de référence (I_0) dépendant d'une tension de polarisation égale à la tension de mode commun voulue de l'amplificateur cascode replié et un moyen (Fig. 4) permettant de s'assurer que la somme I_S des courants traversant ladite paire de moyens à résistance variable en fonction de la tension (20, 21) est bien égale audit courant de référence et un moyen (Fig. 4) pour générer un signal de tension de mode commun à partir dudit courant de référence (I_0) pour maintenir la tension de sortie de mode commun dudit amplificateur cascode égale à ladite tension de référence.

9. Amplificateur de puissance selon la revendication 8, caractérisé en ce que ladite paire de moyens à résistance variable en fonction de la tension (20, 21) comprend des transistors (20, 21) fonctionnant en zone triode.

10. Amplificateur de puissance selon l'une ou l'autre des revendications 8 et 9, caractérisé en ce que ledit circuit de commande à rétroaction de mode commun (2) comprend une première et une seconde branches de circuit parallèles dans lesquelles circulent les courants respectifs I_0 et I_1, ladite première branche de circuit comportant une paire de transistors (27, 28), reliés en parallèle et ayant leurs gâchettes reliées à ladite tension de référence (V_{pol}), qui servent de sources de courant et sont en série avec un autre transistor (25), ladite seconde branche de circuit comprenant ladite paire de résistances variables en fonction de la tension (20, 21) en série avec un autre transistor (24), les autres transistors (24, 25) des branches de circuit respectives étant appariés et ayant leurs gâchettes reliées entre elles pour s'assurer que les courants des deux branches de circuit soient identiques et le signal de commande à rétroaction de mode commun étant produit au niveau dudit autre transistor (25) de la première branche de circuit.

11. Amplificateur de puissance selon la revendication 10, comprenant un transistor additionnel (26, 23) dans chacune desdites branches de circuit, lesdits transistors additionnels (26, 23) ayant leurs gâchettes reliées entre elles et reliées à une seconde source de tension de référence (Vb2).

Petitioner Micron Ex-1004, 0117

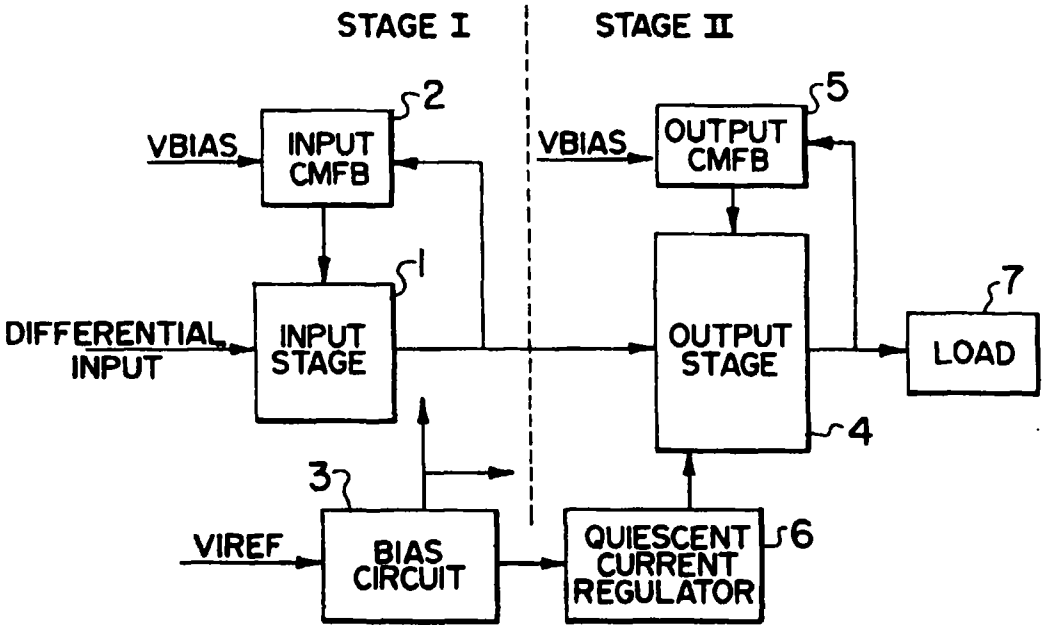


FIG. 1

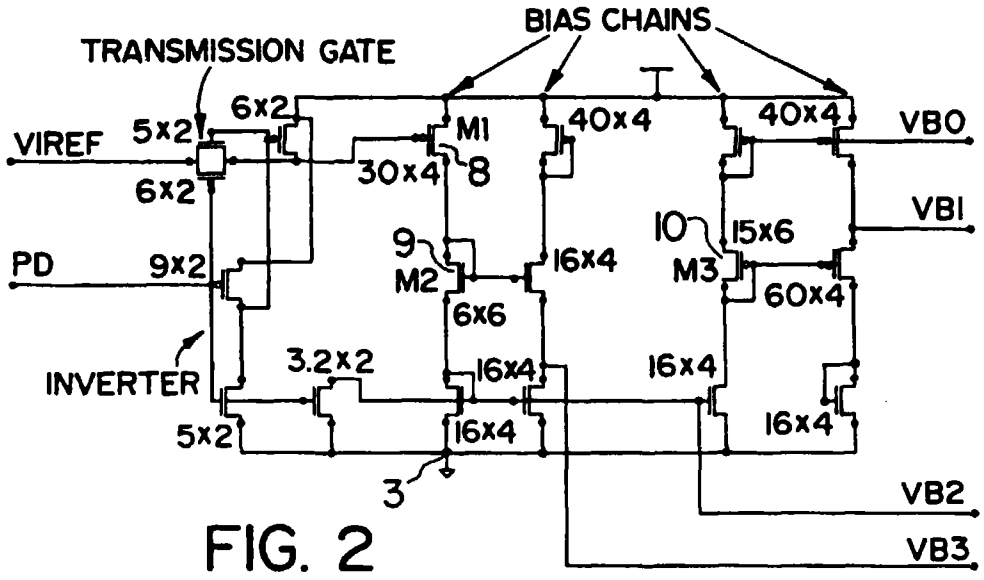


FIG. 2

Petitioner Micron Ex-1004, 0118

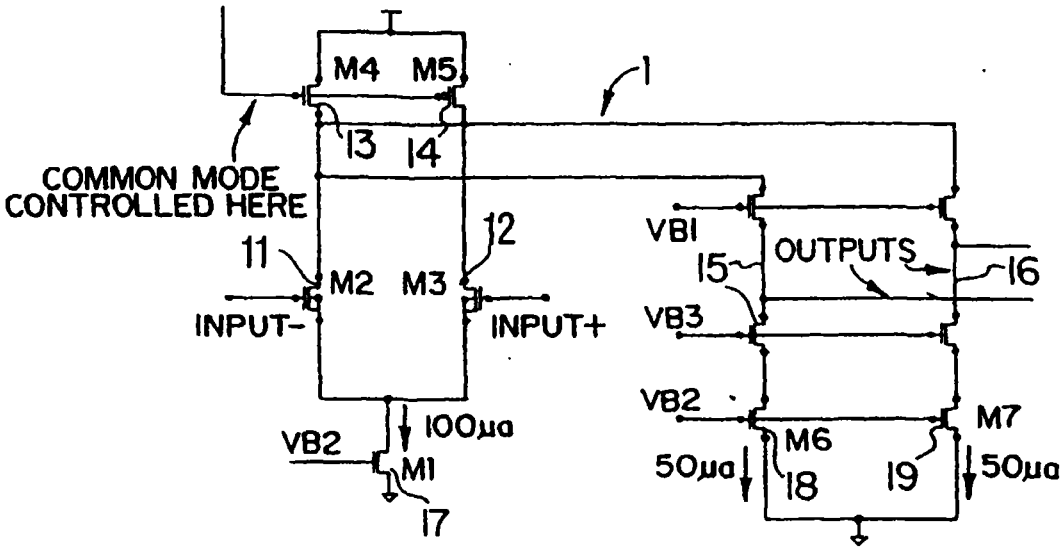


FIG. 3

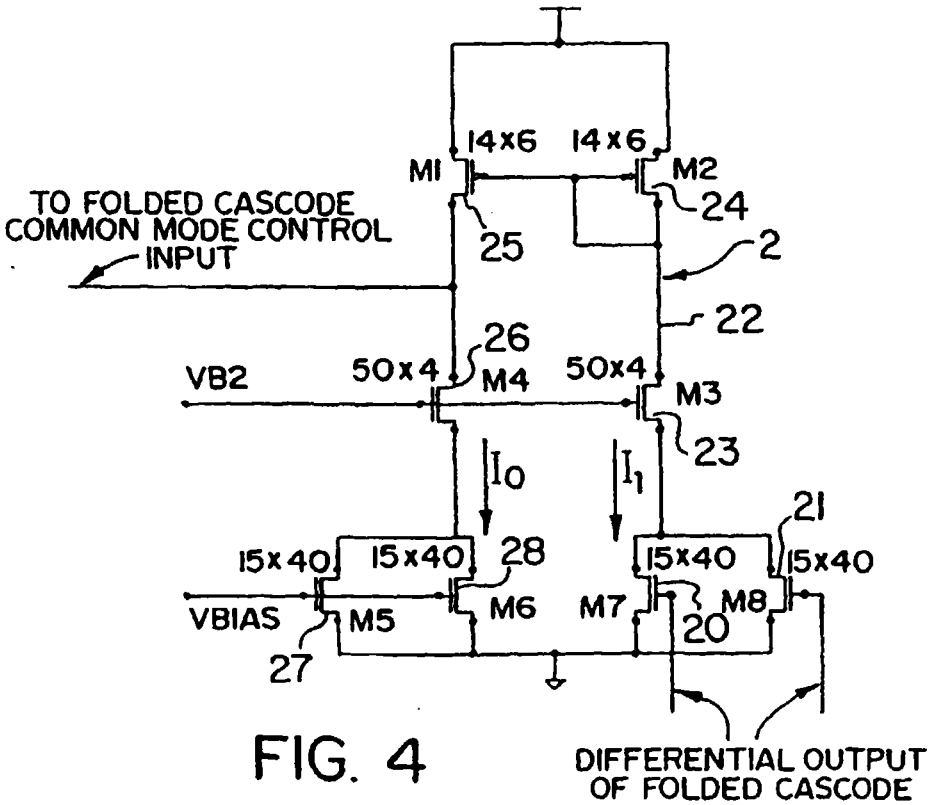


FIG. 4

Petitioner Micron Ex-1004, 0119

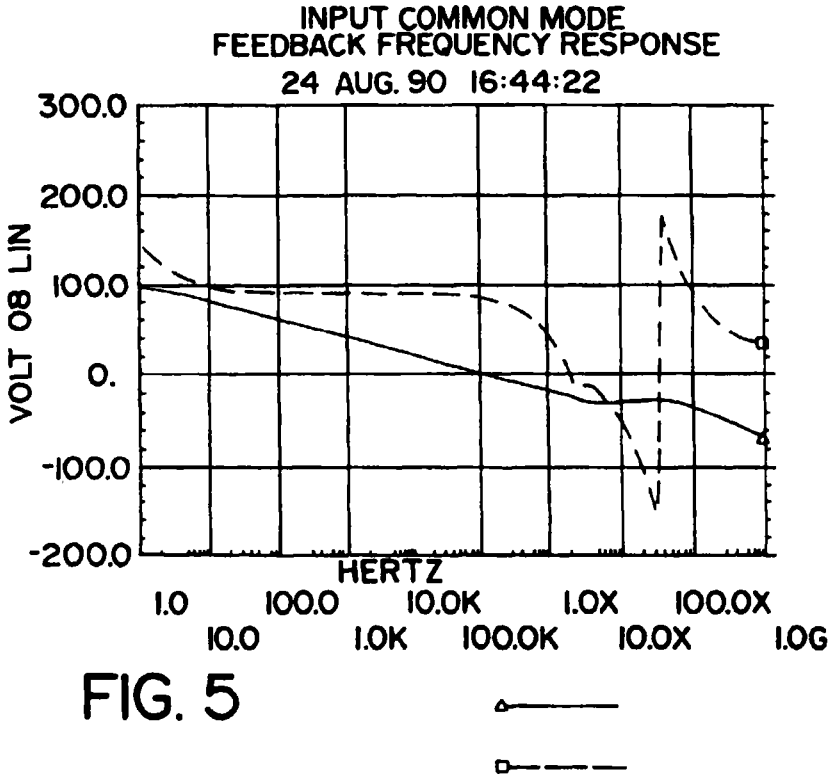


FIG. 5

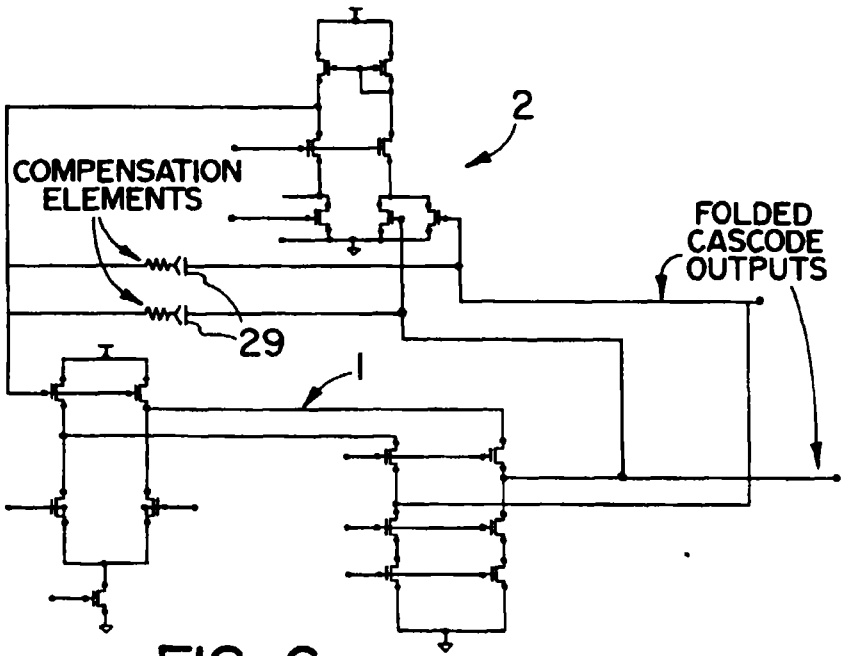


FIG. 6

Petitioner Micron Ex-1004, 0120

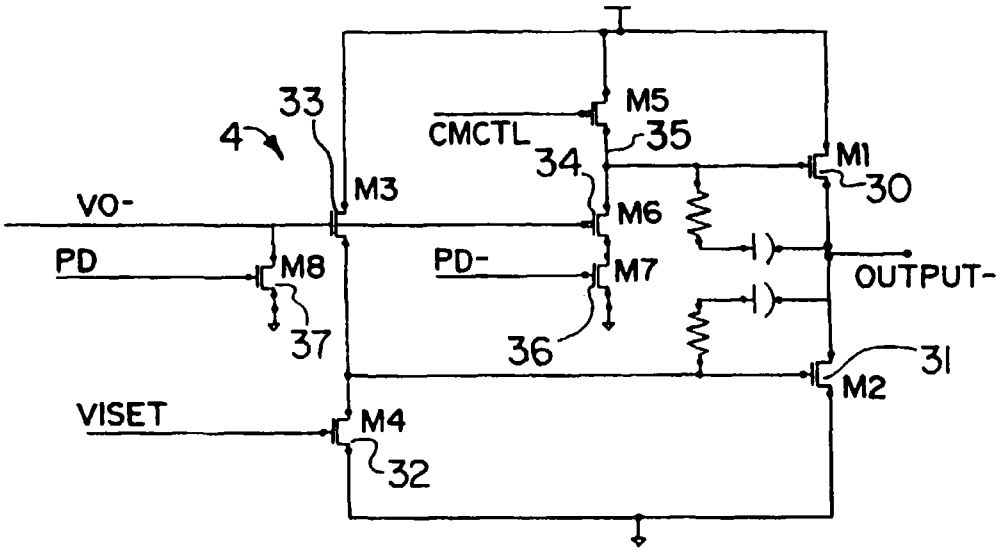


FIG. 7

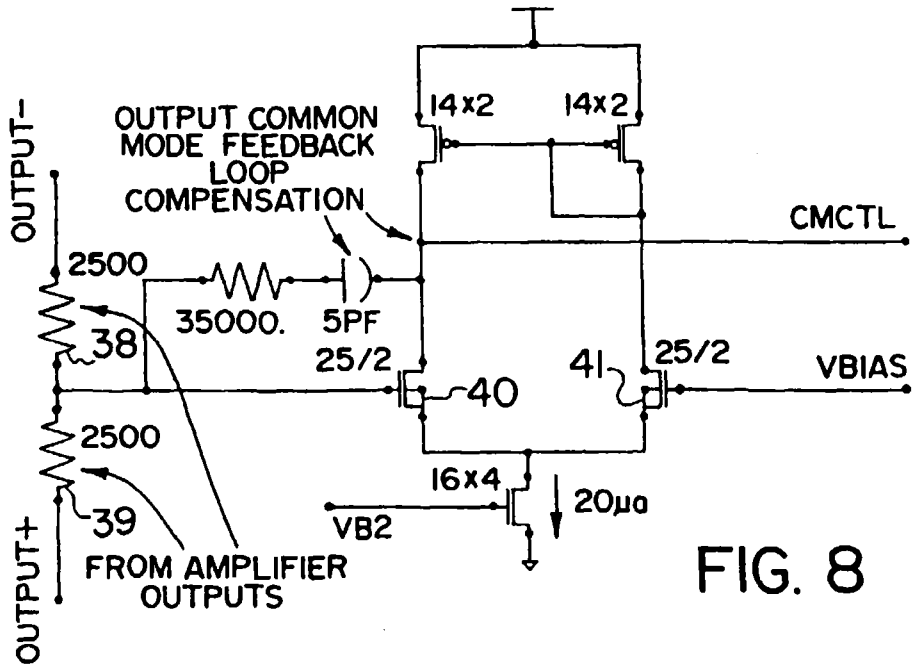


FIG. 8

Petitioner Micron Ex-1004, 0121

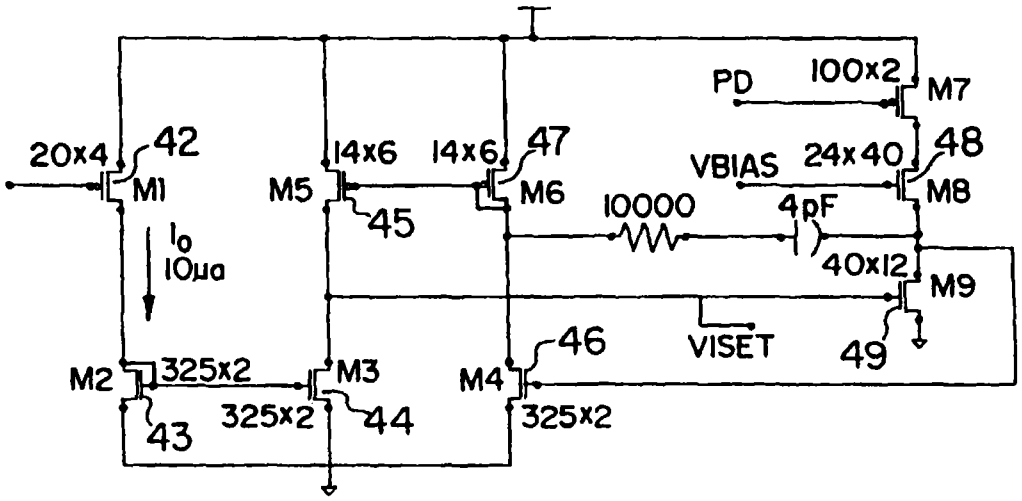


FIG. 9

Petitioner Micron Ex-1004, 0122

TRANSIENT LOAD VOLTAGE REGULATOR

FIELD OF THE INVENTION

The invention relates generally to integrated circuits and, more particularly, to electrical circuits adapted to stabilize a source voltage in light of a varying output load.

BACKGROUND OF THE INVENTION

Power usage is a primary concern for many consumer electronics devices. As a solution, many known devices are adapted to selectively operate certain circuitry so that battery resources are utilized as sparingly as possible. For example, a mobile phone may turn off camera circuitry while a user is on a call. To do so, the camera circuitry may be electrically isolated from the battery so it ceases to draw current from the battery.

This approach creates problems in the design of the integrated circuits (ICs) that operate electronic devices, because the selective turning on and off of circuits referenced to a power supply causes variations in a supply voltage. For most electrical circuits to operate properly, they must be referenced to a stable supply voltage.

Many solutions have been proposed for voltage regulators to stabilize a power supply voltage under varying load conditions. One known approach is a source follower (also known as a common-drain amplifier or voltage follower) such as an NMOS source follower. A classic NMOS source follower includes an N-Channel transistor (known as a pass transistor). A drain of the pass transistor is coupled to a load to supply power. The voltage across the load is fed back to a differential amplifier that supplies a control voltage at the gate of the pass transistor.

A source follower solution operates relatively well to stabilize a supply voltage for circuits that operate at frequencies such as 1Mhz and above. However, a source follower

typically operates poorly for circuits operating at lower frequencies such as below 100kHz. Because many integrated circuits require a regulated supply voltage at all frequency ranges, a source follower may be undesirable in many applications.

In addition, to effectively regulate a power supply, a source follower typically requires a relatively large output capacitor to ensure enough charge is available to compensate for changes in the load powered by the regulator. Such a capacitor often takes up a large amount of space on an integrate circuit or must be off-chip connected to a capacitor in an IC package.

Other approaches to power regulation, such as discussed in U.S. Pat. No. 6,653,891 to Hazucha et al., incorporate some form of additional feedback loop to improve upon an ability of a source follower voltage regulator to regulate voltage and current supplied to a load in light of varying load conditions. For example, U.S. Pat. No. 7,319,314 to Maheshwari et al. discloses the use of a dual difference amplifier stage feedback circuit and a voltage replicator to better stabilize a supply voltage. Similarly, U.S. Pat. No. 7,446,515 to Wang, U.S. Pat. No. 6,809,504 to Tang et al., U.S. Pat. No. 6,975,494 to Tang et al., U.S. Pat. No. 6,188,211 to Runcon-Mora et al., and U.S. Pat. No. 5,867,015 to Corsi et al. describe other various dual stage regulators. Still other approaches, such as U.S. Pat. Pub. No. 2009/0033298 to Kleveland, combine analog feedback circuitry with a digital controller and one or more sense circuits to provide additional feedback in light of varying load conditions.

A common drawback of the above-mentioned approaches is that each involves a relatively complex configuration of transistors and other circuit components, which not only requires significant space in an integrated circuit, but also increases design and IC implementation costs. And, for many known solutions, additional space on an IC, a circuit board, or in an IC package is required due to a need for a relatively large capacitor. Further,

Petitioner Micron Ex-1004, 0124

although the above-mentioned regulators may provide improved stability at a range of frequencies, they do so at the cost of relatively large current draw of the regulator itself, which is inefficient for purposes of preserving battery life.

Thus, a need exists in IC technology to provide an improved variable load voltage regulator for integrated circuits that has improved stability at both low and high frequencies of circuit operation. Also, a need exists to provide such a voltage regulator that does not require a large capacitor. Furthermore, a need exists for a simple, inexpensive, and easy to design voltage regulator for variable load integrated circuits.

SUMMARY OF THE INVENTION

In various embodiments, a voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions is described herein. The voltage regulator circuit includes an input adapted to receive a voltage from the power supply and an output adapted to be coupled to the load. The regulator further includes a feedback circuit coupled to a first current path. The feedback circuit includes a feedback transistor and is constructed to maintain a voltage at a gate of the feedback transistor substantially constant.

The voltage regulator circuit further includes a first current supply circuit constructed to supply to a second current path a first current that is substantially constant. The regulator further includes a second current supply circuit coupled to the first current supply circuit, the gate of the feedback transistor, and the output of the voltage regulator circuit. The second current supply circuit is constructed to supply a second current to the second current path with a magnitude

Petitioner Micron Ex-1004, 0125

based on the voltage at the gate of the feedback transistor and a voltage at the output of the voltage regulator circuit.

A pass device that includes a gate coupled to the second current path is adapted to receive a signal with a magnitude based on a magnitude of a current of the second current path and supply a load current to the load via the output of the voltage regulator circuit with a magnitude based on a magnitude of the signal. In an embodiment, the second current source is adapted to, via the pass device, cause an increase in a magnitude of the load current supplied to the output if a voltage at the output decreases and cause a decrease in magnitude of the load current supplied to the output if a voltage at the output increases. The feedback circuit, the first current supply circuit, the second current supply circuit, and the pass device are integrated in an integrated circuit and referenced to the input of the voltage regulator circuit.

In various embodiments, a voltage regulator circuit integrated in an integrated circuit (IC) adapted to provide a voltage from a power supply to a load under varying load conditions is described herein. The regulator includes an input adapted to receive a voltage from the power supply and an output adapted to be coupled to the load. The regulator further includes a first current path referenced to the input, and a feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant. The regulator also includes a first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant and a second current supply means coupled to the first current supply means, the gate of the feedback transistor, and the output of the voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to the second current path with a magnitude based on the first voltage reference and the second voltage reference.

Petitioner Micron Ex-1004, 0126

The regulator also includes means for supplying current to the load for receiving a signal with a magnitude based on a magnitude of the first current and the second current and for supplying a load current to the load via said output of the voltage regulator circuit with a magnitude based on a magnitude of the signal. In an embodiment, the first current supply means, the second current supply means and the means for supplying current to the load are arranged such that, if a voltage at the load decreases, a magnitude of said load current supplied to the load is increased and, if a voltage at the load increases, a magnitude of the load current supplied to the load is decreased. The feedback means, the first current supply means, the second current supply means, and the means for supplying current to the load are integrated in an integrated circuit.

In other embodiments according to various aspects of the invention described herein, methods of regulating a supply voltage for selectively operable load circuitry of an integrated circuit are described. In one embodiment, a method includes receiving, from a power supply, a power supply voltage and supplying, to a first current path referenced to the power supply voltage, a master current. The master current is received at a feedback circuit. A voltage at a gate of the feedback transistor is maintained substantially constant via the feedback circuit.

A first current with a substantially constant magnitude is supplied to a second current path coupled to a pass transistor. A second current is also supplied to the second current path. The second current has a magnitude based on the voltage at the gate of the feedback transistor and a voltage at the variable load. A control signal based on a magnitude of the second current and a magnitude of the first current is received at the gate of the pass transistor. A load current with a magnitude based on the control signal is supplied to the load via the pass transistor such that when a voltage across the variable load increases, a magnitude of the load current is reduced,

Petitioner Micron Ex-1004, 0127

and when a voltage across the variable load decreases, a magnitude of the load current is increased.

In other various embodiments, a method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit is described. The method includes generating, at a first current path integrated in the integrated circuit, a substantially constant master current. The method further includes supplying to a second current path via a first current source integrated in the integrated circuit, a first current and supplying, via a second current source integrated in the integrated circuit and coupled to the second current path, a second current with a magnitude based in part on a voltage at said variable load. The method also includes receiving, from the second current path, a control signal at a pass transistor integrated in the integrated circuit, wherein the control signal has a magnitude based on the first current and the second current. In addition, the method includes supplying, to the load circuitry via the pass transistor, a load current in response to the control current, wherein a magnitude of the first current and a magnitude of the second current are at least in part dependent on a magnitude of the master current.

Advantageously, embodiments of the invention described herein provide for improved regulation of a supply voltage for integrated circuits. The systems and methods for voltage regulation described herein provide for a simple, easy to design voltage regulator that utilizes a minimum of components and takes up a minimum amount of space on an IC while being capable of regulating a supply voltage for circuits operating at both low and high frequencies. The voltage regulator described herein is further capable of regulating a supply voltage while minimizing an amount of current drawn by the voltage regulator circuit, thus maximizing battery

Petitioner Micron Ex-1004, 0128

life. In addition, the voltage regulator described herein allows for effective power supply voltage regulation without a dependence on a larger output capacitor arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 illustrates generally a block diagram example of an integrated circuit (IC) layout.

FIG. 2 illustrates generally for exemplary purposes a schematic diagram of a known NMOS source follower circuit.

FIG. 3 illustrates generally a functional schematic diagram of one embodiment of a regulator according to various aspects of the invention described herein.

FIG. 4 illustrates generally a functional schematic diagram of an alternative embodiment of a regulator according to various aspects of the invention described herein.

FIG. 5 illustrates generally a schematic diagram of one embodiment of a regulator according to various aspects of the invention described herein.

FIG. 6 illustrates generally a schematic diagram of an alternative embodiment of a regulator according to various aspects of the invention described herein.

FIG. 7 illustrates generally one embodiment of a method of regulating a supply voltage under variable load conditions according to various aspects of the invention described herein.

FIG. 8 illustrates generally one embodiment of a method of regulating a supply voltage under variable load conditions according to various aspects of the invention described herein.

Petitioner Micron Ex-1004, 0129

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

FIG. 1 generally shows various aspects of a typical integrated circuit (IC) 195, which includes a variety of groups of circuits in IC portions that operate independently to perform functions of IC 195. For example, if IC 195 were adapted to operate a modern mobile telephone, IC portion 165 might interface with a memory device, IC portion 166 might operate a digital media player, IC portion 167 could operate a camera, and IC portion 168 may enable wireless connectivity such as Wi-Fi or Bluetooth.

Each of IC portions 165-168 will likely have unique power requirements. They may draw different levels of current (for example based on a number of transistors), require different voltage levels or operate at different frequencies. As previously mentioned, groups of circuits may frequently transition from a powered to a no or low power state and back. In order for circuits of IC 195 to operate properly, a stable power supply must be maintained in light of varying levels of current drawn from the power supply. Thus, IC 195 further includes voltage regulator circuit 192, which is adapted to receive a supply voltage 181 from a power supply such as a battery, and provide a stable supply voltage to circuits of IC 195 under varying load conditions.

Petitioner Micron Ex-1004, 0130

FIG. 2 shows a circuit diagram of an NMOS source follower 100. Source follower 100 includes a pass transistor 102 coupled to a feedback circuit that includes differential amplifier 101 and voltage divider 103. The feedback circuit is arranged so that an output 113 of differential amplifier 101 drives gate 112 of pass transistor 102 in response to a comparison of a voltage at output node 107 and a reference voltage at node 111 of differential amplifier 101. Due to this feedback arrangement, source follower 100 is operative to drive current to load 106 such that a voltage at output node 107 is maintained at a constant level.

Because of this feedback arrangement, source follower 100 is operable to respond to swings in output voltage due to changing load conditions and provide a stable voltage to load 106. However, the ability of source follower 100 to track a voltage is dependent on the size of capacitor 105 across load 106. For many ICs, a larger capacitor is required to ensure enough charge is present to effectively track a voltage at output 107. For purposes of the present invention, a larger capacitor is typically a capacitor or capacitor arrangement having an effective capacitance of at least 30 pico-farads. Such larger capacitors are particularly undesirable due to considerations of size and complexity of implementation. For example, a larger capacitor may add 20-30% in area consumed by a traditional voltage regulator integrated in an IC. In addition, source follower 100 is ineffective at regulating a voltage for circuits operating at certain frequencies, such as below 100kHz.

As discussed above, many solutions have been provided to regulate a power supply voltage. The instant inventors have recognized a need for improvements allowing for effective power supply regulation under varying load conditions at a wide range of frequencies, while at the same time taking up a minimum amount of space on an IC. In addition, the instant inventors

Petitioner Micron Ex-1004, 0131

have recognized a need for a regulator circuit that effectively regulates a power supply while minimizing the need for a large output capacitor.

FIG. 3 illustrates generally a high-level circuit diagram of one embodiment of a power supply regulator circuit 301 according to various aspects of the invention described herein. Regulator 301 is generally constructed to receive as input a power supply that includes a positive terminal 311 and a negative terminal (ground) 312, and is adapted to supply a regulated voltage to a load at output node 360.

Regulator 301 includes feedback circuit 331 coupled to first current path 375. Feedback circuit 331 includes a differential amplifier 333 and a feedback transistor 332. In the embodiment shown, feedback transistor 332 is a Pmos transistor. Feedback circuit 331 is arranged such that a voltage at gate 337 is maintained substantially constant.

Regulator 301 also includes pass transistor 350. As shown, pass transistor 350 includes a gate 351 coupled to a second current path 376. Regulator 301 also includes first current source 322 and second current source 340. In an embodiment, first current source 322 is adapted to supply a first current I1 to second current path 376, and second current source 340 is adapted to supply a second current I2 to second current path 376. Pass transistor 350 is adapted to receive, at pass transistor gate 351, a signal based on a current of second current path 376.

In an embodiment, a magnitude of the current of second current path 376 is based on a magnitude of the first current I1 and the second current I2. Pass transistor 350 may be adapted to supply, to a load coupled to output 360, a load current with a magnitude based on the signal received at pass transistor gate 351.

In an embodiment, the signal received at pass transistor gate 351 may vary at least in part based on a current of second current path 376. The signal received at pass transistor gate 351

Petitioner Micron Ex-1004, 0132

may be a voltage. A difference between first current I1 and second current I2 may cause changes in the voltage at pass transistor gate 351. A difference between first current I1 and second current I2 may cause a charge or discharge of the voltage at pass transistor gate 351.

A voltage at pass transistor gate 351 may have a magnitude that varies based in part on a current of second current path 376 and a parasitic resistance of first current source 322 and second current source 340. In an embodiment, the parasitic resistance of first current source 322 and second current source 340 may be a parasitic resistance between a drain and source of at least one transistor of first current source 322 and/or second current source 340. A change in a voltage at pass transistor gate 351 may cause a change in a magnitude of a current supplied to a load coupled to output 360.

In the embodiment shown, first current source 322 functions to pull up a current supplied to second current path 376 (increase a level of current supplied to second current path 376), while second current source 340 is operative to pull down a current supplied to gate 351 (reduce a level of current supplied to second current path 376). As shown, first current source 322 and second current source 340 are arranged to supply current to a single current path, second current path 376.

In the embodiment of FIG. 3, first current source 322 is a constant current source adapted to mirror a current of master current source 321 to supply, to second current path 376, a current I1 based on a current of first current path 375. In an alternative embodiment, first current source 322 is an independent current source constructed to receive as input a bias voltage and supply a first current I1 with a magnitude based on the bias voltage.

In the depicted embodiment, second current source 340 is a variable current source adapted to supply a current to second current path 376 with a magnitude based on first reference

Petitioner Micron Ex-1004, 0133

signal 341 and second reference signal 342. In one embodiment, first reference signal 341 is based on a voltage at feedback transistor gate 337, and second reference signal 341 is based on a voltage at output node 360.

In an embodiment, second current source 340 is adapted to supply a second current according to the equation $I=K(Vout-Vgate-Vt)^2$, where Vout is a voltage at output node 360, Vgate is a voltage at feedback transistor gate 337, Vt is a threshold voltage of a at least one transistor of second current source 340, and K is a positive constant. In an embodiment, second current source 340 is adapted to supply a second current according to the equation $I=K(Vout-Vgate-Vt)^{2} * (1+\gamma(Vdrain-Vsource))$, where Vdrain is a drain voltage and Vsource is a source voltage, respectively, of at least one transistor of second current source 340, and γ is a positive parameter. In an embodiment, γ is a parameter at least in part based on transistor attributes, such as channel width and/or length.

Regulator 301 may be adapted to operate such that when a voltage at output node 360 decreases (indicating that a current drawn by the load has increased, or additional circuitry has been turned on), second current source 340 is adapted to decrease a magnitude of current supplied to second current path 376, resulting in an increase in a voltage at pass device gate 351, thus causing pass device 350 to increase a magnitude of current supplied to a load coupled to output node 360. Likewise, when a voltage at output node 360 increases, second current source 340 is adapted to increase a magnitude of current supplied to second current path 376, resulting in a decrease in a voltage at pass device gate 351, thus causing pass device 350 to decrease a magnitude of current supplied to output node 360.

The circuit arrangement of regulator 301 is advantageous, because second current source 340 is able to provide a precise comparison between a stable voltage at feedback transistor 331

Petitioner Micron Ex-1004, 0134

and a voltage across a load at output 360. Regulator 301 is further advantageous, because it is constructed to regulate a supply voltage for circuits operating at both low and high frequencies.

FIG. 4 illustrates generally a high-level circuit diagram of an alternative embodiment of a power supply regulator circuit 401. The regulator of FIG. 4 is similar to the regulator depicted in FIG. 3, except feedback transistor 401 is an NMOS transistor instead of a PMOS transistor.

Regulator 401 includes first current source 422 and second current source 440. In an embodiment, first current source 422 is adapted to supply a first current I1 to second current path 476, and second current source 440 is adapted to supply a second current I2 to second current path 476.

As shown, regulator 401 further includes pass transistor 450. Pass transistor 450 may be is adapted to receive, at pass transistor gate 451, a signal based on a current of second current path 476. In an embodiment, a magnitude of the current of second current path 476 is based on a magnitude of the first current I1 and the second current I2. Pass transistor 450 may be adapted to supply, to a load coupled to output 460, a load current with a magnitude based on the signal received at pass transistor gate 451.

In an embodiment, the signal received at pass transistor gate 451 may vary at least in part based on a current of second current path 476. The signal received at pass transistor gate 451 may be a voltage. A difference between first current I1 and second current I2 may cause changes in a voltage at pass transistor gate 451. A difference between first current I1 and second current I2 may cause a charge or discharge of a voltage at pass transistor gate 451.

A voltage at pass transistor gate 451 may have a magnitude that varies based in part on a current of second current path 476 and a parasitic resistance of first current source 422 and second current source 440. In an embodiment, the parasitic resistance of first current source 422

Petitioner Micron Ex-1004, 0135

and second current source 440 may be a parasitic resistance between a drain and source of at least one transistor of first current source 422 and/or second current source 440.

First current source 422 may be a constant current source adapted to supply, to second current path 476, a first current I1 with a substantially constant magnitude. In one embodiment, first current source 422 is a slave of a current mirror. According to this embodiment, first current source 422 is constructed to mirror a current of master current source 421. In an alternative embodiment, first current source 422 is adapted to receive as input a bias voltage and supply a first current I1 to second current path 476 with a magnitude based on a magnitude of the bias voltage.

Second current source 440 may be adapted to supply, to second current path 476, a variable current. In an embodiment, second current source 440 is adapted to receive a first reference signal 441 and a second reference signal 442, and supply a second current I2 with a magnitude based on first reference signal 441 and second reference signal 442. In an embodiment, first reference signal 441 is a voltage at gate 437 of feedback transistor 431, and second reference signal 442 is a voltage at output node 460.

In an embodiment, second current source 440 is adapted to supply a second current according to the equation $I=K(Vgate-Vout-Vt)^2$, where Vout is a voltage at output node 460, Vgate is a voltage at feedback transistor gate 437, Vt is a threshold voltage of at least one transistor of second current source 440, and K is a positive constant. In an embodiment, second current source 340 is adapted to supply a second current according to the equation $I=K(Vgate-Vout-Vt)^2 * (1+\gamma(Vdrain-Vsource))$, where Vdrain is a drain voltage and Vsource is a source voltage, respectively, of at least one transistor of second current source 340, and γ is a positive

Petitioner Micron Ex-1004, 0136

parameter. In an embodiment, γ is a parameter at least in part based on transistor attributes, such as channel width and/or length.

According to the embodiment shown, second current source 440 is operable to pull up a current supplied to gate 451 of pass transistor 450, and first current source 422 is operable to pull down a current supplied to pass transistor gate 451.

In an embodiment, regulator 401 is adapted to operate such that when a voltage at output node 460 decreases (indicating that a current drawn by the load has increased, possibly caused by circuitry of the load that has been turned on), second current source 440 is adapted to increase a magnitude of current supplied to second current path 476, resulting in an increase in a signal at pass device gate 451, thus increasing a magnitude of current supplied to output node 460. Likewise, when a voltage at output node 460 increases, second current source 440 is adapted to decrease a magnitude of current supplied to second current path 476, resulting in a decrease of a signal supplied to pass device gate 451, thus causing a decrease in a magnitude of current supplied to output node 460.

Both of the embodiments depicted in FIGS. 3 and 4 provide an advantage over other known voltage regulators in that they are adapted to control the supply of a relatively large load source current (for example milli-amps, or less than one amp) via feedback signals of relatively small currents (for example micro-amps, or less than one milli-amp). In addition, regulators 301 and 401 are advantageous because they supply a load source current via a single current path, current paths 377 and 477, respectively, thus reducing power consumption compared to other known regulators.

FIG. 5 illustrates generally a circuit diagram of one embodiment of regulator circuit 301. As shown in FIG. 3, regulator circuit 501 includes feedback circuit 531. Feedback circuit 531 is

Petitioner Micron Ex-1004, 0137

operative to maintain a voltage at a gate of feedback transistor 532 substantially constant. To do so, feedback circuit 531 includes differential amplifier 533 and voltage divider 536. Differential amplifier 533 is adapted to receive, at input 535, a feedback voltage proportional to a voltage across the drain and source terminals of feedback transistor 532, and compare the feedback voltage to a reference voltage received at input terminal 534. In one embodiment, the reference voltage is a band gap voltage. In operation, differential amplifier 533 is operable to drive a gate of feedback transistor 532 to maintain a voltage at feedback transistor gate 537 substantially constant.

The embodiment of FIG. 5 also shows one embodiment of first current source 522. First current source 522 may be adapted to supply a substantially constant current. In the depicted embodiment, first current source 522 is a slave transistor 523 of a current mirror. Gate 524 of transistor 523 is electrically coupled to gate 528 of master transistor 521. Master transistor 521 is adapted to receive at gate 528 a bias voltage. As arranged, both master transistor 521 and slave transistor 522 are constructed to supply a substantially constant current based on a magnitude of the bias voltage at gate 528. In an embodiment, the arrangement of transistors 521 and 522 as a current mirror is operative to supply, to current path 576 via slave transistor 522, a first current based on a current of first current path 575. In an embodiment, the first current is a substantially constant current.

FIG. 5 further illustrates one embodiment of a second current source such as current source 340 illustrated in FIG. 3. In various embodiments, second current source 540 is a variable current source adapted to supply a second current to second current path 576. As depicted, second current source 540 includes replica transistor 542 that includes a gate 547 coupled to feedback transistor 532 gate 537. As shown, replica transistor 542 also includes a drain coupled

Petitioner Micron Ex-1004, 0138

to output node 560. According to this arrangement, a voltage between the gate and source of replica transistor 542 is equivalent to a voltage at feedback transistor gate 537 subtracted from a voltage at output 560.

In an embodiment, replica transistor 542 is operated in a saturation region. A basic equation for the current through a MOS transistor in saturation is $I=K(Vgs-Vt)^2$. Thus, replica transistor 542 is adapted to supply current based on a comparison of Vout and Vgate: $I=K(Vout-Vgate-Vt)^2$, where Vout is a voltage at output 560, Vgate is a voltage at feedback transistor gate 537, and Vt is a threshold voltage of replica transistor 542. In various embodiments, K is a positive constant. In some embodiments, K is a positive constant based on transistor process variables. In one such embodiment, K is a positive constant based on transistor width and length for replica transistor 542. In an embodiment, replica transistor 542 is adapted to supply a second current according to the equation $I=K(Vout-Vgate-Vt)^2 * (1+\gamma(Vdrain-Vsource))$, where Vdrain is a drain voltage and Vsource is a source voltage, respectively, of replica transistor 542, and γ is a positive parameter. In an embodiment, γ is a parameter at least in part based on replica transistor 542 attributes, such as channel width and/or length.

In the embodiment shown, second current source 540 also includes transistors 581 and 582. Transistors 581 and 582 are connected such that a current of replica transistor 542 is mirrored at pull down transistor 581, thus pulling down a current through second current path 576. Also shown is an embodiment wherein second current source 540 includes stability capacitor arrangement 586, which is constructed to store charge so as to ensure replicator transistor 542 can supply current quickly in response to changes in output voltage levels. In various embodiments, stability capacitor arrangement 586 has a capacitance in the range of 5-30

Petitioner Micron Ex-1004, 0139

pico-farads. In contrast, known voltage regulators such as nmos source follower 100 typically employ a capacitor arrangement with a larger capacitance, such as greater than 30 pico-farads.

In various embodiments a signal at pass transistor gate 551, such as a voltage, has a magnitude based on a current of second current path 576. In an embodiment, the current of second current path 576 is dependent on the first and second currents supplied by first current source 522 and second current source 540. A voltage at pass transistor gate 551 may vary based on the first and second currents and a parasitic resistance of first current source 522 and second current source 540.

In operation, first current source 522 operates to supply a consistent level of current to second current path 576. This current is "pulled down" by second current source 540 to maintain a relative equilibrium of a current of second current path 576. However, should a load coupled to output node 560 increase in magnitude resulting in a voltage drop at output 560, this drop will result in a decrease in current "pulled" by variable current source 540, and thus cause an increase in a voltage at pass transistor gate 551. Likewise, if a voltage at output 560 increases, indicating a reduction in output load, more current is caused to be "pulled" through second current source 540, and thus cause a decrease in a voltage at pass transistor gate 551.

FIG. 6 illustrates generally a circuit diagram of one embodiment of regulator circuit 401 of FIG. 4 that utilizes an NMOS replica transistor instead of PMOS as shown in FIGS 3 and 5. Regulator circuit 601 operates according to similar principles as regulator circuit 501, with feedback circuit 631 supplying a substantially constant voltage at gate 647 of feedback transistor 632. As shown, replica transistor gate 647 is coupled to feedback transistor gate 631. According to this arrangement, a voltage at gate 647 of replica transistor 642 is based on a voltage at gate 637 of feedback circuit 631 and a voltage at output 660.

Petitioner Micron Ex-1004, 0140

In an embodiment, replica transistor 642 is constantly operated in a saturation region. A basic equation for the current through a MOS transistor in saturation is $I=K(Vgs-Vt)^2$. Thus, replica transistor is adapted to supply current based on a comparison of Vout and Vgate: $I=K(Vgate-Vout-Vt)^2$, where Vout is a voltage at output 660, Vgate is a voltage at replica transistor gate 647, and Vt is a threshold voltage of replica transistor 642. In various embodiments, K is a positive constant. In some embodiments, K is a positive constant based on transistor process variables. In one such embodiment, K is a positive constant based on transistor width and length for replica transistor 642. In an embodiment, replica transistor 642 is adapted to supply a second current according to the equation $I=K(Vgate-Vout-Vt)^2 * (1+\gamma(Vsource -Vdrain))$, where Vdrain is a drain voltage and Vsource is a source voltage, respectively, of replica transistor 642, and γ is a positive parameter. In an embodiment, γ is a parameter at least in part based on replica transistor 642 attributes, such as channel width and/or length.

In the embodiment shown, second current source 640 also includes transistors 681 and 682. These transistors are arranged such that a current of replica transistor 642 is mirrored at transistor 681, supplying current to second current path 676. In an embodiment (not shown in FIG. 6), second current source 640 further includes stability capacitors constructed to store charge so as to ensure replicator transistor 642 can supply current quickly in response to changes in output voltage levels. In various embodiments, the stability capacitor arrangement has a capacitance in the range of 5-30 pico-farads. In contrast, known voltage regulators such as nmos source follower 100 typically employ a capacitor arrangement with a larger capacitance, such as greater than 30 pico-farads.

Petitioner Micron Ex-1004, 0141

In various embodiments a signal at pass transistor gate 651, such as a voltage, has a magnitude based on a current of second current path 676. In an embodiment, the current of second current path 676 is dependent on the first and second currents supplied by first current source 622 and second current source 640. A voltage at pass transistor gate 651 may vary based on the first and second currents and a parasitic resistance of first current source 622 and second current source 640.

In operation, first current source 622 operates to supply a consistent level of pull down current to second current path 676. In the embodiment shown, a bias voltage is applied to gate 671 of transistor 672, which functions to supply a constant current dependent on the bias voltage. In an alternative embodiment not shown in FIG. 6, second current source 622 is a slave transistor of a current mirror, and is adapted to mirror a current of first current path 675.

In the embodiment shown, the first current supplied by first current source 622 is "pulled up" by second current source 640 to maintain a relative equilibrium of a current of second current path 676. However, should current drawn by a load coupled to output node 660 increase in magnitude resulting in a voltage drop at output 660, this drop will result in an increase in current supplied by replica transistor 642 and thus cause an increase in a voltage at pass transistor gate 651. Likewise, if a voltage at output 660 increases, indicating a reduction in output load, less current is caused to be supplied to second current path 676, thus causing a decrease in a voltage at pass transistor gate 651.

FIG. 7 illustrates generally a flow chart of one embodiment of a method of regulating a supply voltage. At 701, a power supply voltage is received from a power supply. At 702, a master current is supplied to a first current path referenced to the power supply voltage. At 703, the master current is received at a feedback transistor. At 704, a voltage at a gate of the feedback

Petitioner Micron Ex-1004, 0142

transistor is maintained substantially constant via a feedback circuit coupled to the feedback transistor. At 705, a first current with a substantially constant magnitude is supplied to a second current path coupled to a pass transistor. At 706, a second current is supplied that is a variable current with a magnitude based on the voltage at the gate of said feedback transistor and a voltage at the variable load. At 707, a signal based on current of the second current path is received at a gate of said pass transistor. At 708, a load current is supplied to the load via the pass transistor. In an embodiment, the load current is supplied such that when a voltage across the variable load increases, a magnitude of the load current is reduced, and when a voltage across said variable load decreases, a magnitude of the load current is increased.

FIG. 8 illustrates generally one embodiment of a method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit. At 801, a substantially constant master current is generated at a first current path. At 802, a first current is supplied to a second current path via a first current source. At 803, a second current is supplied to the second current path via a second current source. In an embodiment, the second current has a magnitude based in part on a voltage at the selectively operable load circuitry. In an embodiment, a magnitude of the first current and a magnitude of the second current are dependent on a magnitude of the master current. At 804, a control signal is received at a pass transistor gate with a magnitude based on the first and second currents. At 805, a load current is supplied to the load circuitry based on a magnitude of the control signal.

Various embodiments of systems, devices and methods have been described herein. These embodiments are given only by way of example and are not intended to limit the scope of the present invention. It should be appreciated, moreover, that the various features of the embodiments that have been described may be combined in various ways to produce numerous

Petitioner Micron Ex-1004, 0143

additional embodiments. Moreover, while various materials, dimensions, shapes, implantation locations, etc. have been described for use with disclosed embodiments, others besides those disclosed may be utilized without exceeding the scope of the invention.

Persons of ordinary skill in the relevant arts will recognize that the invention may comprise fewer features than illustrated in any individual embodiment described above. The embodiments described herein are not meant to be an exhaustive presentation of the ways in which the various features of the invention may be combined. Accordingly, the embodiments are not mutually exclusive combinations of features; rather, the invention may comprise a combination of different individual features selected from different individual embodiments, as understood by persons of ordinary skill in the art.

Any incorporation by reference of documents above is limited such that no subject matter is incorporated that is contrary to the explicit disclosure herein. Any incorporation by reference of documents above is further limited such that no claims included in the documents are incorporated by reference herein. Any incorporation by reference of documents above is yet further limited such that any definitions provided in the documents are not incorporated by reference herein unless expressly included herein.

For purposes of interpreting the claims for the present invention, it is expressly intended that the provisions of Section 112, sixth paragraph of 35 U.S.C. are not to be invoked unless the specific terms "means for" or "step for" are recited in a claim.

Petitioner Micron Ex-1004, 0144

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 April 2004 (01.04.2004)

PCT

(10) International Publication Number
WO 2004/027995 A3

(51) International Patent Classification[7]: H03K 19/0185

(21) International Application Number:
PCT/US2003/024817

(22) International Filing Date: 8 August 2003 (08.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
10/247,127 19 September 2002 (19.09.2002) US
10/247,082 19 September 2002 (19.09.2002) US

(71) Applicant: SUN MICROSYSTEMS, INC. [US/US]; 4150 Network Circle, Santa Clara, CA 95054 (US).

(72) Inventors: AMICK, Brian, W.; 4600 Seton Center Parkway, #320, Austin, TX 78759 (US). WARRINER, Lynn; 1907 Chaparral Drive, Round Rock, TX 78681 (US). GAUTHIER, Claude, R.; 20207 Northbrook Sq., Cupertino, CA 95014 (US). TRAN, Tri, K.; 322 Accolade Dr., San Leandro, CA 94577 (US).

(74) Agents: OSHA, Jonathan, P. et al.; Osha & May L.L.P., 1221 McKinney Street, Suite 2800, Houston, TX 77010 (US).

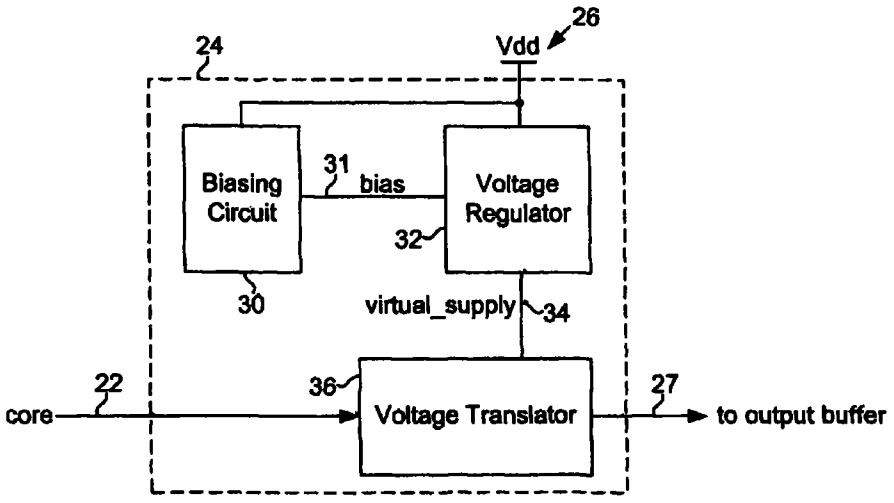
(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations*
— *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for all designations*
— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

[Continued on next page]

(54) Title: INTEGRATED CIRCUIT COMPRISING AN SSTL (STUB SERIES TERMINATED LOGIC) PRE-DRIVER STAGE USING REGULATED POWER SUPPLY AND METHOD FOR PERFORMING AN SSTL OPERATION



(57) Abstract: A SSTL memory interface pre-driver stage (24) that uses a voltage regulator (32) to generate "virtual" supply and ground voltages is provided. The "virtual" supply, being lower than a power supply voltage of the pre-driver stage (24), and the "virtual" ground voltage, being greater than a zero volt ground voltage, allows low voltage transistors to be used, thereby improving interface performance and decreasing system power consumption. The pre-driver stage (24) uses a biasing circuit (30) to bias the voltage regulator (32), formed by a transistor arranged in a source follower configuration, to generate the "virtual" supply and ground voltages off which a voltage translator stage (36) of the pre-driver stage operates to generate an output of the pre-driver stage (24).

WO 2004/027995 A3

Petitioner Micron Ex-1004, 0145

— *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations*

Published:

— *with international search report*

— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
17 June 2004

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Petitioner Micron Ex-1004, 0146

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/24817

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H03K19/0185

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)
EPO-Internal, WPI Data, PAJ

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 087 885 A (TOBITA YOUICHI) 11 July 2000 (2000-07-11) column 1, lines 36-38; figures 11,12,13A,23,24 column 6, lines 61-65 column 19, line 61 - column 23, line 19	1-15
X	GB 2 241 845 A (MITSUBISHI ELECTRIC CORP) 11 September 1991 (1991-09-11) page 7, line 10 - page 8, line 21; figures 2,4A	1,5-7,9, 11-15
Y		2-4,10
Y	US 4 006 491 A (ALASPA ALLAN A ET AL) 1 February 1977 (1977-02-01) column 2, lines 25-32; figure 2	2-4,10
	-/--	

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

° Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
7 May 2004	14/05/2004

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Moll, P

Form PCT/ISA/210 (second sheet) (January 2004)

Petitioner Micron Ex-1004, 0147

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/24817

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 517 375 A (HITACHI LTD) 9 December 1992 (1992-12-09) column 3, line 3 - column 5, line 47; figure 1 column 1, lines 8-12	1,5-7,9, 11-15
X	US 5 731 713 A (PROEBSTING ROBERT J ET AL) 24 March 1998 (1998-03-24) column 6, line 23 - column 10, line 34; figures 2,3 column 12, line 33 - column 13, line 67; figure 6 column 2, lines 39,40	1,5-7,9, 11-15
X	US 4 430 582 A (BOSE BIDYUT K ET AL) 7 February 1984 (1984-02-07) column 3, lines 6-37; figures 2,4	1,5-7,9, 11-14
X	US 6 172 524 B1 (CHO KYU SEOK) 9 January 2001 (2001-01-09) column 4, lines 1-60; figure 4	1,9-14
A	EP 0 905 902 A (SIEMENS AG) 31 March 1999 (1999-03-31) column 12, line 6 - column 13, line 7; figure 5	1-15

Petitioner Micron Ex-1004, 0148

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 03/24817

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6087885 A	11-07-2000	JP 11150469 A	02-06-1999
		CN 1211108 A ,B	17-03-1999
		TW 462143 B	01-11-2001
GB 2241845 A	11-09-1991	JP 3214659 A	19-09-1991
		DE 4101419 A1	25-07-1991
US 4006491 A	01-02-1977	NONE	
EP 0517375 A	09-12-1992	JP 4360312 A	14-12-1992
		EP 0517375 A2	09-12-1992
US 5731713 A	24-03-1998	DE 19502598 A1	14-09-1995
		JP 8051352 A	20-02-1996
US 4430582 A	07-02-1984	NONE	
US 6172524 B1	09-01-2001	KR 2000003606 A	15-01-2000
EP 0905902 A	31-03-1999	US 5939937 A	17-08-1999
		CN 1221256 A	30-06-1999
		EP 0905902 A2	31-03-1999
		JP 11163715 A	18-06-1999
		TW 388981 B	01-05-2000

Petitioner Micron Ex-1004, 0149

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4146.08US01
	Application Number	
Title of Invention	TRANSIENT LOAD VOLTAGE REGULATOR	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ○ Legal Representative under 35 U.S.C. 117 ○ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Tomer	Shaul	Elran	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Petah Tikva	State/Province		Country of Residence [i]	IL

Citizenship under 37 CFR 1.41(b) [i] IL

Mailing Address of Applicant:

Address 1	
Address 2	

City		State/Province	
Postal Code		Country [i]	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	87955		
Email Address	salmela@ptslaw.com	Add Email	Remove Email

Application Information:

Title of the Invention	TRANSIENT LOAD VOLTAGE REGULATOR		
Attorney Docket Number	4146.08US01	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	8	Suggested Figure for Publication (if any)	

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4146.08US01
	Application Number	
Title of Invention	TRANSIENT LOAD VOLTAGE REGULATOR	

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	87955		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status			Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button. Add

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country [i]	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			○ Yes ◉ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

PTO/SB/14 (07-07)
Approved for use through 06/30/2010. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	4146.08US01
	Application Number	
Title of Invention	TRANSIENT LOAD VOLTAGE REGULATOR	

If the Assignee is an Organization check here. ☒			
Organization Name	SanDisk Corporation		
Mailing Address Information:			
Address 1	601 McCarthy Blvd		
Address 2			
City	Milpitas	**State/Province**	CA
Country [i]	US	Postal Code	95035-7932
Phone Number		Fax Number	
Email Address			
Additional Assignee Data may be generated within this form by selecting the **Add** button.		Add	

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.					
Signature	/Amy Salmela/			Date (YYYY-MM-DD)	2009-05-12
First Name	Amy	Last Name	Salmela	Registration Number	55910

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 851 332 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
25.02.2004 Bulletin 2004/09

(51) Int Cl.[7]: **G05F 3/24**, G05F 3/26, G05F 1/575

(21) Application number: **97310344.3**

(22) Date of filing: **19.12.1997**

(54) **A voltage regulator**

Spannungsregler

Régulateur de tension

(84) Designated Contracting States:
DE FR GB IT NL

(30) Priority: **19.12.1996 US 33679 P**

(43) Date of publication of application:
01.07.1998 Bulletin 1998/27

(73) Proprietor: **Texas Instruments Incorporated**
Dallas, Texas 75265 (US)

(72) Inventors:
- **Corsi, Marco**
  Plano, TX 75025 (US)
- **Borden, Robert B.**
  Plano, TX 75023 (US)
- **Kay, Michael R.**
  Greensboro, NC 27407 (US)
- **Salamina, Nicolas**
  Dallas, TX 75048 (US)
- **Rincon, Gabriel A.**
  Margate, FL 33063 (US)

(74) Representative: **Harris, Ian Richard**
D. Young & Co.,
21 New Fetter Lane
London EC4A 1DA (GB)

(56) References cited:
EP-A- 0 316 781
EP-A- 0 733 959
EP-A- 0 745 923

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Jouve, 75001 PARIS (FR)

EP 0 851 332 B1

Petitioner Micron Ex-1004, 0154

Description

FIELD OF THE INVENTION

[0001] This invention generally relates to electronic systems and in particular it relates to voltage regulators.

BACKGROUND OF THE INVENTION

[0002] The function of a voltage regulator is to take a varying input voltage supply and generate a stable output voltage. The efficiency of modern power supply systems, especially battery operated ones, is directly related to the useable operating voltage and current over head required by the system's voltage regulator. The useable operating voltage is called the "drop-out" voltage, which is the difference between the input and output voltages of the regulator while the regulator still maintains regulation. The smaller this difference, the more efficient the system. Additionally, batteries can supply only a finite amount of charge, so the more quiescent current the regulator uses (which is wasted current as far as the system is concerned), the less life the battery will have and therefore the system will be less efficient.

[0003] EP-A-0316781 discloses a voltage regulator circuit comprising: a first transistor coupled between a voltage supply line and an output node; an amplifier coupled to a control region of the first transistor; and negative feedback circuitry arranged for providing negative feedback to the amplifier.

SUMMARY OF THE INVENTION

[0004] According to the invention there is provided a voltage regulator circuit comprising:

a first transistor coupled between a voltage supply line and an output node, the first transistor being arranged for providing a stable voltage on the output node;
a source follower coupled to a control region of the first transistor;
an amplifier coupled to a control region of the source follower for controlling the response of the first transistor;
negative feedback circuitry coupled between the output node and the amplifier, the negative feedback circuitry being arranged for providing feedback to the amplifier;
a current conveyor coupled to the first transistor; and
positive feedback circuitry coupled between the current conveyer and the source follower.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The present invention will now be further described by way of example, with reference to the accompanying drawings in which: the only Figure is a schematic circuit diagram of a preferred embodiment low drop-out (LDO) voltage regulator with PMOS pass element.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0006] Referring to Fig. 1, a circuit diagram of a low drop-out (LDO) voltage regulator with PMOS pass element is illustrated. This preferred embodiment allows an LDO voltage regulator to be compensated while only consuming small currents and substantially improving the load regulation. The circuit includes PMOS pass device 12 (PMOS transistor); PMOS transistor 14; PNP transistors 16 and 18; NMOS transistors 20 and 22; NMOS transistor 24; positive feedback circuit 26 which includes NMOS transistor 28, capacitor 30, and resistor 32; current source 34; PMOS transistor 36; error amplifier 38 (operational amplifier), resistors 40 and 42, voltage reference V_{REF}, output voltage V_{OUT}, and input voltage V_{IN}.

[0007] The operation of the device is explained with reference to the preferred embodiment shown in Figure 1. The output voltage V_{OUT} is regulated by pass transistor 12. The error amp 38, which is an operational amplifier, controls transistor 12 through transistor 24. When the input voltage V_{IN} changes or the current being drawn from an external load at node 44 changes, the output voltage V_{OUT} begins to change causing the voltage across the second resistor 42 to change. The error amp 38 then adjusts the gate voltage of transistor 24 so that the output voltage V_{OUT} is maintained in the desired range.

[0008] Current mirror transistor 14 monitors the current of transistor 12. In the preferred embodiment, the ratio of transistor 14 to transistor 12 is such that the current in transistor 14 is only a small fraction of the current in transistor 12 (for example 1:1000). PNP transistors 16 and 18 together with NMOS transistors 20 and 22 form a current conveyor 46 which forces the current in PNP transistors 20 and 22 to be the same. The current conveyor ensures that the V_{DS} and V_{GS} of transistors 12 and 14 are the same. Since the V_{GS} of transistors 12 and 14 are the same, the currents in PNP transistors 16 and 18 are the same. The current in the current conveyor 46 is equal to the current in transistor 14.

[0009] The current conveyor current is mirrored to transistor 28. Transistor 28 is larger than transistors 20 and 22 in order to provide sufficient current for the source follower transistor 24 which drives output transistor 12. Transistor 24 is an isolated natural NMOS with a low V_T. Resistor 32 and capacitor 30 provide frequency compensation for the positive feedback to make sure the positive feedback never overcomes the negative feedback so that the circuit does not oscillate.

[0010] The current conveyor performs two functions.

Petitioner Micron Ex-1004, 0155

First, it ensures that the external pole and the internal pole remain separated for stability. Second, the positive feedback improves the load regulation by modulating the V_{GS} of transistor 24 proportionately with the V_{GS} of transistor 12. This compensates the output impedance of the circuit.

[0011] If there is no output current at output node 44, there will be no current mirrored to transistor 28. Therefore, in order to make sure that there is some current in transistor 24, current source 34 pulls on transistor 24 so that the circuit works where there is no load at output node 44. In the preferred embodiment, current source 34 provides only a small current on the order of one micro amp. With this small current, the power consumption of the circuit will be extremely small when there is no load on the output. This is an important feature for battery powered devices.

[0012] Transistor 36 is used to enhance the slew rate of the circuit. Transistor 36 allows the circuit to come back into regulation quickly when there is a rapid change in load. Transistor 36 turns on and helps the transient response when going from no load at output node 44 to a full load or some load condition at node 44.

Claims

1. A voltage regulator circuit comprising:

   a first transistor (12) coupled between a voltage supply line and an output node (44), the first transistor being arranged for providing a stable voltage on the output node;
   a source follower (24) coupled to a control region of the first transistor;
   an amplifier (38) coupled to a control region of the source follower for controlling the response of the first transistor;
   negative feedback circuitry (40,42) coupled between the output node and the amplifier, the negative feedback circuitry being arranged for providing feedback to the amplifier;
   a current conveyor (46) coupled to the first transistor; and
   positive feedback circuitry (26) coupled between the current conveyer and the source follower.

2. The circuit of claim 1 further comprising:

   a current source (34) coupled to the source follower.

3. The circuit of claim 1 or claim 2, wherein the first transistor is a MOS transistor.

4. The circuit of claim 1, claim 2 or claim 3, wherein the current conveyer comprises:

   a second transistor (14) having a control region coupled to the control region of the first transistor;
   a first bipolar transistor (16) coupled to the first transistor;
   a second bipolar transistor (18) coupled to the second transistor, a base region of the second bipolar transistor coupled to a base region of the first bipolar transistor;
   a third transistor (20) coupled to the first bipolar transistor; and
   a fourth transistor (22) coupled to the second bipolar transistor and to the base region of the first bipolar transistor, a control region of the fourth transistor coupled to a control region of the third transistor and to the first bipolar transistor.

5. The circuit of claim 4, wherein at least one of the second, third and fourth transistors is a MOS transistor.

6. The circuit of any of claims 1 to 5, wherein the positive feedback circuitry comprises:

   a positive feedback transistor (28) coupled to the source follower;
   a resistor (32) coupled between the current conveyer and a control region of the positive feedback transistor; and
   a capacitor (30) coupled to the control region of the positive feedback transistor.

7. The circuit of claims 1 to 6, wherein the negative feedback circuitry comprises:

   a first resistor (40) having a first end coupled to the output node and a second end coupled to the amplifier; and
   a second resistor (42) coupled to the second end of the first resistor.

8. The circuit of any of claims 1 to 7 further comprising:

   a slew rate enhancement transistor (36) coupled to the source follower, wherein a control region of the skew rate enhancement transistor is coupled to the output of the amplifier.

Revendications

1. Circuit régulateur de tension, comprenant :

   un premier transistor (12) couplé entre une ligne d'alimentation de tension et un noeud de sortie (44), le premier transistor étant disposé pour fournir une tension stable sur le noeud de

Petitioner Micron Ex-1004, 0156

sortie ;
une source suiveuse (24) couplée à une région de contrôle du premier transistor ;
un amplificateur (38) couplé à une région de contrôle de la source suiveuse pour contrôler la réponse du premier transistor ;
une circuiterie de retour négatif (40, 42) couplée entre le noeud de sortie et l'amplificateur, la circuiterie de retour négatif étant disposée pour assurer le retour à l'amplificateur ;
un convoyeur de courant (46) couplé au premier transistor ; et
une circuiterie de retour positif (26) couplée entre le convoyeur de courant et la source suiveuse.

2. Circuit selon la revendication 1, comprenant en outre :

une source de courant (34) couplée à la source suiveuse.

3. Circuit selon la revendication 1 ou la revendication 2, dans lequel le premier transistor est un transistor MOS.

4. Circuit selon la revendication 1, la revendication 2 ou la revendication 3, dans lequel le convoyeur de courant comprend :

un second transistor (14) ayant une région de contrôle couplée à la région de contrôle du premier transistor ;
un premier transistor bipolaire (16) couplé au premier transistor ;
un second transistor bipolaire (18) couplé au second transistor, une région de base du second transistor bipolaire couplée à une région de base du premier transistor bipolaire ;
un troisième transistor (20) couplé au premier transistor bipolaire ; et
un quatrième transistor (22) couplé au second transistor bipolaire et à la région de base du premier transistor bipolaire, une région de contrôle du quatrième transistor couplée à une région de contrôle du troisième transistor et au premier transistor bipolaire.

5. Circuit selon la revendication 4, dans lequel au moins un des second, troisième et quatrième transistors est un transistor MOS.

6. Circuit selon l'une des revendications 1 à 5, dans lequel la circuiterie de retour positif comprend :

un transistor de retour positif (28) couplé à la source suiveuse ;
une résistance (32) couplée entre le convoyeur de courant et une région de contrôle du transistor de retour positif ; et
un condensateur (30) couplé à la région de contrôle du transistor de retour positif.

7. Circuit selon les revendications 1 à 6, dans lequel la circuiterie de retour négatif comprend :

une première résistance (40) ayant une première extrémité couplée au noeud de sortie et une seconde extrémité couplée à l'amplificateur ; et
une seconde résistance (42) couplée à la seconde extrémité de la première résistance.

8. Circuit selon les revendications 1 à 7, comprenant en outre :

un transistor d'amélioration de vitesse de balayage (36) couplé à la source suiveuse, dans lequel une région de contrôle du transistor d'amélioration de vitesse de balayage est couplée à la sortie de l'amplificateur.

Patentansprüche

1. Spannungsreglerschaltung, welche aufweist:

einen ersten Transistor (12), der zwischen eine Spannungsversorgungsleitung und einen Ausgangsschaltungspunkt (44) geschaltet ist, wobei der erste Transistor dafür eingerichtet ist, am Ausgangsschaltungspunkt eine stabile Spannung bereitzustellen,

einen Source-Folger (24), der mit einer Steuerzone des ersten Transistors gekoppelt ist,

einen Verstärker (38), der mit einer Steuerzone des Source-Folgers gekoppelt ist, um das Ansprechen des ersten Transistors zu steuern,

eine Gegenkopplungs-Schaltungsanordnung (40, 42), die zwischen den Ausgangsschaltungspunkt und den Verstärker geschaltet ist, wobei die Gegenkopplungs-Schaltungsanordnung dafür eingerichtet ist, dem Verstärker eine Rückkopplung bereitzustellen,

eine Strom-Übermittlungseinrichtung (46), die mit dem ersten Transistor gekoppelt ist, und

eine Mitkopplungs-Schaltungsanordnung (26), die zwischen die Strom-Übermittlungseinrichtung und den Source-Folger geschaltet ist.

2. Schaltung nach Anspruch 1, welche weiter auf-

Petitioner Micron Ex-1004, 0157

weist:

eine Stromquelle (34), die mit dem Source-Folger gekoppelt ist.

3. Schaltung nach Anspruch 1 oder 2, wobei der erste Transistor ein MOS-Transistor ist.

4. Schaltung nach Anspruch 1, 2 oder 3, wobei die Strom-Übermittlungseinrichtung aufweist:

einen zweiten Transistor (14) mit einer Steuerzone, die mit der Steuerzone des ersten Transistors gekoppelt ist,

einen ersten Bipolartransistor (16), der mit dem ersten Transistor gekoppelt ist,

einen zweiten Bipolartransistor (18), der mit dem zweiten Transistor gekoppelt ist, wobei eine Basiszone des zweiten Bipolartransistors mit einer Basiszone des ersten Bipolartransistors gekoppelt ist,

einen dritten Transistor (20), der mit dem ersten Bipolartransistor gekoppelt ist, und

einen vierten Transistor (22), der mit dem zweiten Bipolartransistor und mit der Basiszone des ersten Bipolartransistors gekoppelt ist, wobei eine Steuerzone des vierten Transistors mit einer Steuerzone des dritten Transistors und mit dem ersten Bipolartransistor gekoppelt ist.

5. Schaltung nach Anspruch 4, wobei wenigstens einer von dem zweiten, dem dritten und dem vierten Transistor ein MOS-Transistor ist.

6. Schaltung nach einem der Ansprüche 1 bis 5, wobei die Mitkopplungs-Schaltungsanordnung aufweist:

einen Mitkopplungs-Transistor (28), der mit dem Source-Folger gekoppelt ist,

einen Widerstand (32), der zwischen die Strom-Übermittlungseinrichtung und eine Steuerzone des Mitkopplungs-Transistors geschaltet ist, und

einen Kondensator (30), der mit der Steuerzone des Mitkopplungs-Transistors gekoppelt ist.

7. Schaltung nach den Ansprüchen 1 bis 6, wobei die Gegenkopplungs-Schaltungsanordnung aufweist:

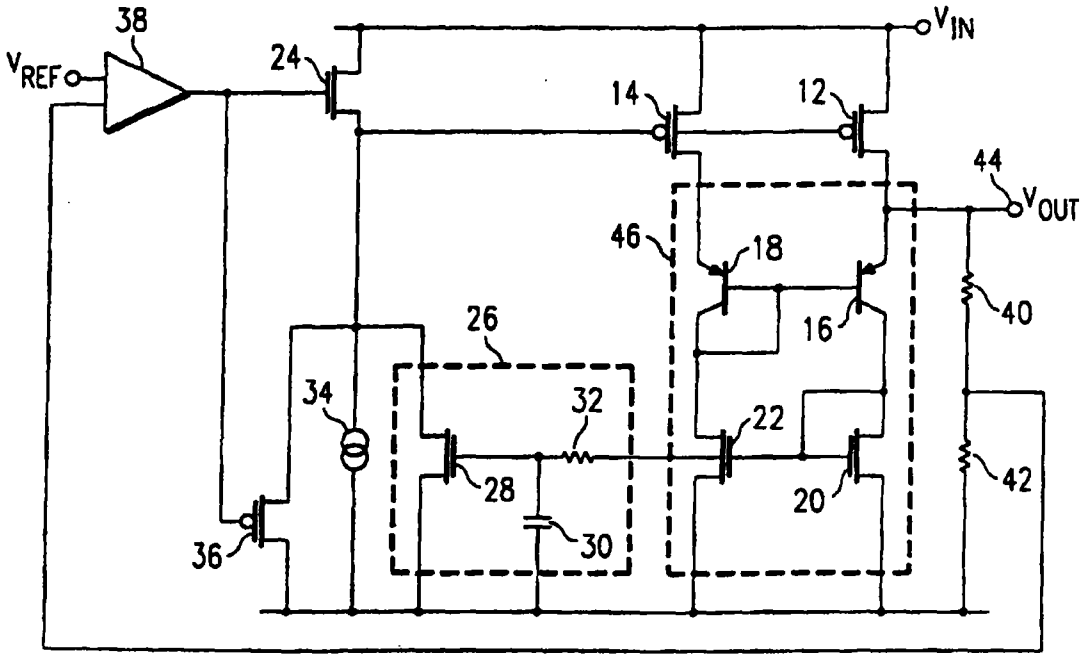
einen ersten Widerstand (40), dessen erstes Ende mit dem Ausgangsschaltungspunkt gekoppelt ist und dessen zweites Ende mit dem Verstärker gekoppelt ist, und

einen zweiten Widerstand (42), der mit dem zweiten Ende des ersten Widerstands gekoppelt ist.

8. Schaltung nach einem der Ansprüche 1 bis 7, welche weiter aufweist:

einen Anstiegsraten-Erhöhungstransistor (36), der mit dem Source-Folger gekoppelt ist, wobei eine Steuerzone des Anstiegsraten-Erhöhungstransistors mit dem Ausgang des Verstärkers gekoppelt ist.

Petitioner Micron Ex-1004, 0158



Petitioner Micron Ex-1004, 0159

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 622 067 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
27.02.2008 Bulletin 2008/09

(51) Int Cl.:
G06K 19/073 *(2006.01)* ***G11C 5/14*** *(2006.01)*
G11C 16/30 *(2006.01)* ***G05F 1/618*** *(2006.01)*
H02M 3/158 *(2006.01)*

(21) Application number: **05108301.2**

(22) Date of filing: **30.07.2002**

(54) **Voltage regulator and semiconductor integrated circuit**

Spannungsregler und integrierter Halbleiterschaltkreis

Régulateur de tension et circuit intégré à semi-conducteur

(84) Designated Contracting States:
DE FR GB

(30) Priority: **30.07.2001 JP 2001229374**

(43) Date of publication of application:
01.02.2006 Bulletin 2006/05

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
02017155.9 / 1 282 072

(73) Proprietor: **Oki Electric Industry Co., Ltd.**
Tokyo (JP)

(72) Inventor: **Takabayashi, Yasutaka**
Tokyo (JP)

(74) Representative: **Betten & Resch**
Patentanwälte
Theatinerstrasse 8
80333 München (DE)

(56) References cited:
EP-A- 1 107 502
FR-A- 2 776 410
US-B1- 6 172 494
US-B1- 6 201 375

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Jouve, 75001 PARIS (FR)

EP 1 622 067 B1

Petitioner Micron Ex-1004, 0160

Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention generally relates to a voltage regulator used for Integrated Circuit Card and a semiconductor integrated circuit (it is called simply IC hereinafter).

[0002] This application relies for priority on Japanese patent application, Serial Number 229374/2001, filed July 30, 2001.

DESCRIPTION OF THE RELATED ART

[0003] Fig. 2 is a system configuration figure showing an example of an integrated circuit card. This integrated circuit card has the internal logic part 2. This internal logic part 2 has EEPROM 1 (it is a nonvolatile memory which can electrically erase data stored therein), and CPU (Central Processing Unit) and ROM.. The EEPROM 1 is a memory for memorizing data, such as personal information. The CPU is the equipment for performing data processing.

[0004] Furthermore, this integrated circuit card has a band gap 4 and a voltage regulator 3. The voltage regulator 3 adjusts a power-supply voltage VDD supplied from an external device, and supplies a constant voltage VREG to the internal logic part 2. The band gap 4 generates a reference voltage VR used as the reference of the voltage VREG and a constant current control signal CS.

[0005] The conventional voltage regulator used for the integrated circuit card is shown in Fig. 3 (a) and Fig. 3 (b). A series type voltage regulator is shown in Fig. 3 (a), and a shunt type voltage regulator is shown in Fig. 3 (b).

[0006] The voltage regulator shown in Fig. 3 (a) has a differential amplification circuit A which has an inverted input terminal to which the reference voltage VR is applied. An output of the differential amplification circuit A is connected to a gate of a P type MOS transistor M1. A power-supply voltage VDD is applied to a source of the transistor M 1 and a drain of the transistor M 1 is connected to an output node N1. A voltage divider circuit which comprised of a resistor R1 and a resistor R2 is connected between the output node N1 and a ground potential GND. Comparison voltage VC generated from the voltage divider circuit is given to an non-inverted input terminal of the amplification circuit A.

[0007] The constant current control signal CS for generating constant current is given to the amplification circuit A. The signal of the output node N 1 is given to the amplification circuit A through a capacitor C1 for phase compensation. A capacitor C2 for voltage flat and smooth is connected between the output node N 1 and the ground potential GND.

[0008] In this voltage regulator, the voltage VREG at the output node N 1 is divided by the resistor R 1 and the resistor R2 and is applied to the non-inverted input terminal of the amplification circuit A as the comparison voltage VC (=VREGxR2/(R1+R2)). The voltage regulator receives the voltage VREG at the output node N1 and the reference voltage VR applied to the inverted input terminal of the amplification circuit A, and compares and amplifies the voltage difference between the voltage VC and the voltage VR.

[0009] Therefore, if the comparison voltage VC is higher than the reference voltage VR, the output voltage VO of the amplification circuit A goes high, internal resistance (resistance between a source and a drain) of the transistor M 1 increases, and the voltage VREG of the output node N 1 falls. Conversely, if the comparison voltage VC is lower than the reference voltage VR, the output voltage VO of the amplification circuit A becomes low, internal resistance of the transistor M1 decreases, and the voltage VREG of the output node N 1 goes up.

[0010] By the above feedback operation, the voltage VREG of the output node N1 is stabilized in the state where the comparison voltage VC coincides with the reference voltage VR. Therefore, it becomes VREG=VRx (1+R1/R2). In addition, since voltage change of the output node N 1 by the feedback operation returns to the amplification circuit A through the capacitor C1, it is prevented that the amplification circuit A will be in an oscillation state. Moreover, since a very small current change caused by a load connected to the output node N1 is absorbed by the capacitor C2, the voltage VREG of the output node N1 is maintained almost uniformly.

[0011] The voltage regulator shown in Fig. 3 (b) is replaced with the transistor M 1 of the voltage regulator shown in Fig. 3 (a), and has a constant current circuit B which supplies constant current to the output node N1 from the power-supply voltage VDD. Furthermore, this voltage regulator has an N type MOS transistor M2 connected between the output node N1 and the ground potential GND and controlled by the output voltage VO of the amplification circuit A.

[0012] In this voltage regulator, the constant current is always supplied to the output node N by the constant current circuit B from the power-supply voltage VDD. Reduction of current which flows for the load connected to the output node N 1 rises voltage VREG of the output node N1. By this, the output voltage VO of the amplification circuit A rises, the internal resistance of the transistor M2 decreases, and current which flows to this transistor M2 increases. Conversely, an increase of current which flows for load reduces voltage VREG of the output node N1. By this, the output voltage VO of the amplification circuit A falls, the internal resistance of the transistor M2 increases, and current which flows to this

Petitioner Micron Ex-1004, 0161

transistor M2 decreases. It is controlled by such feedback operation so that the sum of current which flows for the load connected to the output node N1, and current which flows to the transistor M2 becomes always constant, and the voltage VREG of the output node N 1 is stabilized.

[0013] However, the following subjects occurred in the conventional voltage regulator.

[0014] For example, in the series type voltage regulator, when the power-supply voltage VDD is 5V, the voltage VREG at the output node N1 is 3V and the load current range between 0 and 10mA, 0-10mA current is supplied from the power-supply voltage VDD corresponding to the load current.

[0015] Therefore, the product of the voltage drop (2V) with the transistor M 1 and the load current is lost, and it is satisfactory from the viewpoint of power consumption.

[0016] However, since current supplied from the power-supply voltage VDD corresponded to load current, there is a problem enable it to analyze operation of the internal logic part of the integrated circuit card, by acting as the monitor of the change of current supplied from the exterior.

[0017] When analysis technique, such as DPA/SPA (Differential Power Analysis/Simple Power Analysis), is used especially, there is a possibility that the problem that secret data which should be protected on security will be decoded from a power-supply current waveform may occur.

[0018] On the other hand, at the shunt type voltage regulator shown in Fig. 3 (b), since constant current always flows from the power-supply voltage VDD by the constant current circuit B, there is no possibility that an internal state may be decoded by the monitor of a power-supply current waveform. However, for this reason, regardless of actual load current, current which always exceeds 10mA needed to be supplied and there is a problem in the viewpoint of power consumption.

[0019] Therefore, there are few increases in power consumption and the voltage regulator and IC with difficult analysis of operation of an internal logic circuit have been desired. EP-A-1107502 discloses a system and method for preventing differential power analysis attacks on a cryptographic device. Therein there is disclosed a constant current circuit for preventing differential power analysis attacks.

SUMMARY OF THE INVENTION

[0020] According to one aspect of the present invention, there is provided a circuit as defined in claim 1. The dependent claims define embodiments of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021]

Fig. 1 is a circuit diagram showing a voltage regulator according to a first preferred embodiment of the present invention.

Fig. 2 is a schematic block diagram showing an IC card of the related art.

Fig. 3 (a) and Fig. 3 (b) are circuit diagrams showing voltage regulators of the related art

Fig. 4 (a) and (b) are circuit diagrams showing a voltage regulator according to a first preferred embodiment of the present invention.

Fig. 5 is a circuit diagram showing a voltage regulator according to a second preferred embodiment of the present invention.

Fig. 6 is a circuit diagram showing a voltage regulator according to a third preferred embodiment of the present invention.

Fig. 7 is a circuit diagram showing an amplifier circuit 10A in Fig. 6.

Fig. 8 is a circuit diagram showing a voltage regulator according to a fourth preferred embodiment of the present invention.

Fig. 9 is a circuit diagram showing an amplifier circuit 10B in Fig. 8.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0022] A voltage regulator and a semiconductor integrated circuit according to the present invention will be explained hereinafter with reference to figures.

First preferred embodiment

[0023] Fig. 1 is a circuit diagram showing a voltage regulator according to a first preferred embodiment of the present invention.

Petitioner Micron Ex-1004, 0162

[0024] This voltage regulator has differential type amplification circuit 101 and amplification circuit 102 where a reference voltage VR is applied to an inverted input terminal□, and a comparison voltage VC is given to an non-inverted input terminal +. The amplification circuit 101 and the amplification circuit 102 are the same structures mutually. The output of the amplification circuit 101 is connected to a gate of a P channel MOS transistor 31 (hereinafter referred to as PMOS) and the output of the amplification circuit 102 is connected to a gate of an N channel MOS transistor 32 (hereinafter referred to as NMOS). A source of the PMOS 31 is supplied with the power-supply voltage VDD and a drain of the PMOS 31 is connected to the output node NO. A drain of the NMOS 32 is connected to the output node NO and a source of the NMOS 32 is connected to a ground potential GND.

[0025] The constant current control signal CS for generating constant current is applied to the amplification circuit 101 and the amplification circuit 102. Furthermore, the amplification circuit 101 and the amplification circuit 102 receive phase compensation signal PS through the capacitor 33 and the capacitor 34 for phase compensation so that operation stabilized, without being in an oscillation state may be performed.

[0026] The constant current circuit 40 is connected between the power-supply voltage VDD and the output node NO. The constant current circuit 40 is set up so as to flow constant current having about a half of an average load current. Moreover, between the output node NO and the ground potential GND, the capacitor 35 for voltage flat and smooth is connected.

[0027] Furthermore, between the output node NO and the ground potential GND, a voltage dividing circuit which comprised of resistor 36 and resistor 37 is connected, and the comparison voltage VC generated by the voltage dividing circuit is applied to the non-inverted input terminal + of the amplification circuit 101, and the non-inverted input terminal + of the amplification circuit 102. Voltage VREG adjusted to desired constant voltage is output from the output node NO to the load circuit not illustrated.

[0028] Fig. 4 (a) and Fig. 4 (b) is a circuit diagram showing an example of the amplification circuit in Fig. 1, and a constant current circuit.

[0029] This amplification circuit has a PMOS 1 1 and a PMOS12 which constitute a differential input part. The reference voltage VR is applied to a gate of the PMOS 11and the comparison voltage VC is applied to a gate of PMOS 12. Sources of the PMOS 11 and the PMOS 12 are commonly connected to the power-supply voltage VDD through a PMOS 13. The constant current control signal CS is applied to a gate of the PMOS 11, and constant current supplies the PMOS 11 and the PMOS 12 through this PMOS 13. Drains of the PMOS 11 and the PMOS 12 are connected to the ground potential GND through NMOS 14 and NMOS 15 by which diode connection is made in the direction of order, respectively.

[0030] Furthermore, this amplification circuit has a PMOS 16 constituted so that constant current might be passed based on the constant current control signal CS, source of this PMOS 16 is connected to the power-supply voltage VDD, and drain of this PMOS 16 is connected to the node N11. A drain and a gate of an NMOS 17 are connected to the node N11, and a source of this NMOS 17 is connected to a gate and a source of an NMOS 18. The source of the NMOS 18 is connected to the ground potential GND.

[0031] A gate of an NMOS 19 is connected to the node N11, and a source of this NMOS 19 is connected to the ground potential GND through an NMOS 20. Moreover, a gate of the NMOS 20 and a gate of an NMOS 14 are connected to a drain of the NMOS 14. The Phase compensation signal PS gives the gate of the NMOS 20. A drain of the NMOS19 is connected to a drain and a gate of a PMOS 21, and a source of the PMOS 21 is connected to the power-supply voltage VDD.

[0032] Furthermore, a gate of a NMOS 22 is connected to the node N11, and a source of the NMOS 22 is connected to the ground potential GND through an NMOS 23. Moreover, a gate of the NMOS 23 and a gate of a NMOS15 are connected to a drain of the NMOS 15. A drain of the NMOS 22 is connected to a drain of a PMOS 24. A source and a gate of the PMOS 24 are connected to the power-supply voltage VDD and the PMOS 21, respectively.

[0033] In such an amplification circuit, the voltage difference between the reference voltage VR and the comparison voltage VC which are inputted into the PMOS 11 and the PMOS 12 comprised of a differential input part is amplified. The output voltage VO is output from the connecting point of drains of the NMOS 22 and the PMOS 24.

[0034] On the other hand, as shown in Fig. 4 (b), a constant current circuit has a PMOS 41 so as to flow constant current based on the constant current control signal CS. A source of the PMOS 41 is connected to the power-supply voltage VDD, and a drain of the PMOS 41 is connected to a gate and a drain of an NMOS 42. Source of the NMOS 42 is connected to the ground potential GND.

[0035] A gate of an NMOS 43 which constitutes a current mirror circuit to the NMOS 42 is connected to a drain of the NMOS 42. Source of the NMOS 43 is connected to the ground potential GND, and a drain of the NMOS 43 is connected to a drain and a gate of the PMOS44. Source of the PMOS 44 is connected to the power-supply voltage VDD.

[0036] A gate of a PMOS 45 which constitutes a current mirror circuit to the PMOS 44 is connected to the drain of the PMOS 44.. A Source of the PMOS 45 is connected to the power-supply voltage VDD, and a drain of the PMOS 45 is connected to an output node NO of a voltage regulator.

[0037] In such a constant current circuit, desired constant current is supplied to the output node NO by setting dimension of the gate width and gate length of each transistor so that it may become a predetermined ratio. For example, if current

Petitioner Micron Ex-1004, 0163

of 50μA flows to the PMOS 41 and the NMOS 42 based on the constant current control signal CS, in proportion to current which flows to this NMOS 42, current of 500μA flows to the NMOS 43. Thereby, current of 500μA flows also to the PMOS 44, in proportion to current which flows to the PMOS 44, current of 5mA flows to the NMOS 45. And 5mA constant current is supplied to the output node NO.

[0038] Next, operation of the circuit shown in Fig. 1 is explained.

[0039] First, the load circuit not illustrated is connected to the output node NO. This load circuit has a condition that predetermined voltage VREG of 3V is appeared at the output node NO and load current changes in the range of 0-10mA when the load circuit is connected to the output node NO.

[0040] From the exterior, the power-supply voltage VDD of 5V is supplied, for example, and when stable reference voltage VR and the constant current control signal CS are applied, 5mA constant current is supplied to the output node NO through the constant current circuit 40.

[0041] Simultaneously, the gate of the PMOS 31 serving as constant current source connected in parallel with the constant current circuit 40 is controlled by the output voltage VO 1 of the amplification circuit 101. Moreover, the gate of the NMOS 32 connected in parallel with the load circuit is controlled by the output voltage VO2 of the amplification circuit 102.

[0042] Voltage of the output node NO is divided by the resistor 36 and the resistor 37 and it is given to the input side of the amplification circuit 101 and the amplification circuit 102 as the comparison voltage VC. The reference voltage VR set up so that this output node NO might serve as predetermined voltage VREG is given to the input side of the amplification circuit 101 and the amplification circuit 102

[0043] Thereby, where the output node NO is set to voltage VREG, the output voltage VO1 of the amplification circuit 101 and the output voltage VO2 of the amplification circuit 102 are stabilized, and stable constant voltage VREG is outputted.

[0044] For example, when load current is 10mA, 5mA is supplied through the constant current circuit 40, and 5mA of an insufficiency is supplied to the output node NO through the PMOS 31. And the NMOS 32 enters into an OFF state.

[0045] Moreover, when load current is 1mA, the PMOS 31 enters into an OFF state, 1mA is supplied to the load circuit in 5mA supplied to the output node NO from the constant current circuit 40, and 4mA for a surplus (remaining) flows to the ground potential GND through the NMOS 32.

[0046] As mentioned above, the voltage regulator of the first preferred embodiment has the PMOS 31 provided in parallel with the constant current circuit 40 and the NMOS 32 provided in parallel with the load circuit. These PMOS 31 and NMOS 32 may be controlled so that the output node NO may serve as voltage VREG.

[0047] Since current supplied from the power-supply voltage VDD becomes constant value unless load current which flows in a load circuit exceeds the capability of the constant current circuit 40, the analysis of the internal state of the load circuit (internal logic circuit) by the monitor of a power-supply current waveform becomes impossible.

[0048] Moreover, since only the insufficiency is supplied from the PMOS 31 when load current exceeds the capability of the constant current circuit 40, there is little change of current supplied from the power-supply voltage VDD, and the analysis of the internal state of a load circuit becomes very difficult.

[0049] Therefore, by setting current of the constant current circuit 40 as suitable value, the voltage regulator to which power consumption is not made to almost increase and with the difficult analysis of a load circuit of operation can be obtained.

Second preferred embodiment

[0050] Fig.5 is a circuit diagram showing a voltage regulator according to a second preferred embodiment of the present invention. In Fig. 5, wherein like elements are given like reference characters in Fig. 1.

[0051] The difference between the second embodiment and the first embodiment resides in that a resistor 38 is connected between the resistor 36 and the resistor 37. The sum of resistance value of this resistor 36 and resistance value of the resistor 38 is set as the resistance value of the resistor 36 in Fig. 1. The comparison voltage VC1 appeared at a connection point where the resistor 36 and the resistor 38 are connected to each other may be applied to the non-inverted input terminal + of the amplification circuit 101. The comparison voltage VC2 appeared at a connection point where the resistor 37 and the resistor 38 are connected to each other may be applied to the non-inverted input terminal + of the amplification circuit 102.

[0052] The resistance value of the resistor 38 is set as the resistance value which can give the potential difference more than the variation voltage of offset of the amplification circuit 101 and the amplification circuit 102 to the non-inverted input terminal + of the amplification circuit 101 and the amplification circuit 102. In addition, the resistance ratio of the resistor 36, the resistor 38, and the resistor 37 is set up so that the comparison voltage VC2 equal to the level of the reference voltage VR to the voltage VREG of the output node NO. That is, when the resistance value of the resistor 36, the resistor 38, and the resistor 37 is R36, and R38 and R37, respectively, the reference voltage VR is expressed with the following formula.

Petitioner Micron Ex-1004, 0164

$$VR=VREG\times R37 /(R36+R38) +R37$$

[0053] Moreover, the drive capability of the amplification circuit 102 is set up more greatly than the amplification circuit 102. Other structures are the same as that of Fig. 1.

[0054] Next, operation is explained.

[0055] When the power-supply voltage VDD is supplied and the reference voltage VR, the constant current control signal CS, and the constant current circuit 40 are stabilized, the output voltage VO1 of the amplification circuit 101 tends to control the gate of the PMOS 31 serving as current source so that the comparison voltage VC1 is set to the same level as the reference voltage VR. Moreover, the output voltage VO2 of the amplification circuit 102 controls the gate of the NMOS 32 so that the comparison voltage VC2 is set to the same level as the reference voltage VR.

[0056] At this time, since drive capability of the amplification circuit 101 is larger than that of the amplification circuit 102, the comparison voltage VC2 is set to the reference voltage VR. And the comparison voltage VC1 is set to a level high a little to the reference voltage VR by having formed resistor 38. Therefore, the voltage VREG becomes constant voltage by the amplification circuit 102 and NMOS 32 and comes to be supplied to an inside as internal voltage.

[0057] Since the comparison voltage VC 1 is higher than the reference voltage VR, the output voltage VO 1 of the amplification circuit 101 is H level, and the PNOS 31 serving as current source is in an OFF state. That is, in usual, current supply to inside is performed only by the constant current circuit 40.

[0058] When current consumption of an internal circuit exceeds the supply capability of the constant current circuit 40, the voltage VREG falls gradually and the comparison voltage VC1 approaches the reference voltage VR. When the comparison voltage VC1 is more nearly less than the reference voltage VR, the output voltage VO1 of the amplification circuit 101 falls, the PMOS 31 serving as current source is changed into an ON state and the comparison voltage VC 1 tends to raise. Namely, when current consumption of an internal circuit exceeds the supply capability of the constant current circuit 40, the voltage VREG of the output node NO is controlled by the amplification circuit 101 and the amplification circuit 102, and the PMOS 31 and the NMOS 32.

[0059] As mentioned above, in the voltage regulator of the second embodiment, the comparison voltage VC 1 applied to the amplification circuit 101 is set so that it may become higher than the comparison voltage VC2 applied to the amplification circuit 102. Thereby, priority is given to control of the NMOS 32 over the PMOS 31, and current supply to an internal circuit is supplied from the constant current circuit 40. Therefore, since current is supplied from the PMOS 31 only when the supply capability of the constant current circuit 40 is exceeded, there is an advantage that the monitor of internal current consumption becomes difficult and the effect of the measure against security becomes large further.

Third preferred embodiment

[0060] Fig.6 is a circuit diagram showing a voltage regulator according to a third preferred embodiment of the present invention. In Fig. 6, wherein like elements are given like reference characters in Fig. 5.

[0061] This voltage regulator is replaced with the amplification circuit 102 in Fig. 5, and has amplification circuit 10A whose operation is controlled by the control signal S1. Moreover, while a PMOS 51 for a switch by which ON/OFF control is carried out with a control signal

[0062] 1 is provided between the power-supply voltage VDD and the constant current circuit 40 in series, an NMOS 52 for a switch by which ON/OFF control is carried out with this control signal S1 is provided between the output side of amplification circuit 10A, and the ground potential GND. Other structures are the same as that of Fig. 5.

[0063] Fig.7 is one example of circuit diagram showing an amplifier circuit 10A in Fig.6. In Fig. 7, wherein like elements are given like reference characters in Fig. 4 (a).

[0064] In this amplification circuit 10A, an NMOS2 5, a PMOS2 6, a PMOS 27, and the inverter 28 are added to the amplification circuit of Fig. 4 (a).

[0065] The NMOS 25 is connected between the node N11 and the ground potential GND, and a gate of the NMOS 25 is controlled by the control signal S1. The PMOS 26 is inserted between sources of the PMOS 11 and the PMOS 12, and a drain of the PMOS 13, and a gate of the PMOS 26 is controlled by the control signal S1. Moreover, a PMOS 27 is connected between the gate of a PMOS 24 and a source of the PMOS 24, and a gate of the PMOS 24 is controlled by an inverted control signal S 1 inverted by the inverter 28.

[0066] Next, operation is explained.

[0067] When the control signal S 1 is L level, the PMOS 51 is in an ON state and the NMOS 52 is in an OFF state. In the amplification circuit 10A, the NMOS 25 and the PMOS 27 are in OFF states, and the PMOS 26 is in an ON state. Therefore, operation of the voltage regulator of the Fig. 6 in case the control signal S 1 is L level is the same as that of the voltage regulator of Fig. 5.

[0068] On the other hand, when the control signal S 1 is H level, the PMOS 51 is in an OFF state and the NMOS 52

Petitioner Micron Ex-1004, 0165

is in an ON state. Thereby, while the constant current circuit 40 is disconnected from the power-supply voltage VDD, the output side of amplification circuit 10A is fixed to L level, and the NMOS 32 in an OFF state. In amplification circuit 10A, the NMOS 25 and the PMOS 27 are in ON states, and the PMOS 26 is in an OFF state. Therefore, almost all the current passes of amplification circuit 10A are cut off.

[0069] Therefore, when the control signal S1 is H level, this voltage regulator serves as the same structure as the voltage regulator of the conventional series type of Fig. 3 (a).

[0070] As mentioned above, in the third preferred embodiment, the voltage regulator has the PMOS 51 for disconnecting the constant current circuit 40 from the power-supply voltage VDD according to the control signal S 1 and the NMOS 52 which is connected in parallel with the output node NO and for changing the NMOS 32 into an OFF state. Furthermore, the voltage regulator has the amplification circuit 10A by which almost all operation is stopped with this control signal S1. For this reason, in addition to the same advantage as the second embodiment, in the case of the state of operation where security does not pose a problem, there is an advantage that power consumption is reducible for being carried out by enabling it to constitute a series type voltage regulator, by setting the control signal S 1 as H level.

Fourth preferred embodiment

[0071] Fig. 8 is a circuit diagram showing a voltage regulator according to a fourth preferred embodiment of the present invention. In Fig. 8, wherein like elements are given like reference characters in Fig. 6.

[0072] This voltage regulator is replaced with the amplification circuit 102 in Fig. 6, and has amplification circuit 10B whose operation is controlled by standby signal SA. Moreover, the logic OR gate 53 (hereafter referred to as OR) for taking the logic sum of standby signal SA and the control signal SB is provided. The amplification circuit 10A, and the PMOS 51 and the NMOS 52 are controlled by this output signal of OR 53. Other structures are the same as that of Fig. 6.

[0073] Fig.9 is a circuit diagram showing an amplifier circuit 10B in Fig. 8. In Fig. 9, wherein like elements are given like reference characters in Fig. 4 (a).

[0074] In this amplification circuit 10B, a PMOS 29a and a PMOS 29b connected n-series are added to the amplification circuit of Fig. 4 (a). Furthermore, a PMOS 13a with little current capacity is replaced with the PMOS 13.

[0075] The gate width of the PMOS 13a is set as the minimum size which can drive the PMOS 31 by amplification circuit 10B. And the gate width of the PMOS 13a is set so that the sum total of the gate width of this PMOS 13a and the gate width of the PMOS 29a may become equal to the gate width of the PMOS13.

[0076] A source of the PMOS 29a is connected to the power-supply voltage VDD, and a drain of the PMOS 29a is connected to a source of the PMOS 29b. Furthermore, a drain of the PMOS 29b is connected to a drain of the PMOS 13a. The constant current control signal CS and the standby signal SA are applied to a gate of the PMOS 29a and a gate of the PMOS 29b, respectively. Other structures are the same as that of Fig. 4 (a).

[0077] Next, operation is explained.

[0078] When the both of the standby signal SA and the control signal SB are L level, the PMOS51 is in an ON state and the NMOS 52 is in an OFF state. In the amplification circuit 10A, the NMOS2 5 and the PMOS 27 are in OFF states, and the PMOS 26 is in an ON state. Furthermore, in the amplification circuit 10B, the NMOS 29b is in an ON state and the PMOS 13a and the PMOS 29a are connected in parallel. Therefore, operation of the voltage regulator of the Fig. 8 in case the standby signal SA and the control signal SB are L levels is the same as that of the voltage regulator of Fig. 5.

[0079] When the standby signal SA is L level and the control signal SB is H level, the PMOS 51 is in an OFF state and the NMOS 52 is in an ON state. Thereby, while the constant current circuit 40 is electrically separated from the power-supply voltage VDD and the output side of the amplification circuit 10A is fixed to L level, and thus the NMOS 32 is in an OFF state. Moreover, in the amplification circuit 10A, the NMOS 25 and the PMOS 27 are in ON states, the PMOS 26 is in an OFF state and thus almost all the current passes in this amplification circuit 10A are cut off. Furthermore, in the amplification circuit 10B, the PMOS 29b is in an ON state and the PMOS 13a and the PMOS 29a are connected in parallel. Therefore, where the standby signal is L level and the control signal SB is H level, this voltage regulator serves as the structure as the voltage regulator of the conventional series type of Fig. 3 (a).

[0080] When the standby signal SA is H level, regardless of the level of the control signal SB, the PMOS 51 is in an OFF state and the NMOS 52 will is in an ON state. Thereby, the constant current circuit 40 is electrically separated form the power-supply voltage VDD and the output side of the amplification circuit 10A is fixed to L level, and thus the NMOS 32 is in an OFF state. Moreover, in the amplification circuit 10A, the NMOS 25 and the PMOS 27 is in an ON state, the PMOS 26 is in an OFF state and almost all the current passes in this amplification circuit 10A is cut off. On the other hand, in the amplification circuit 10B, the PMOS 29b is in an OFF state and the PMOS 13b is detached. Thereby, while the drive capability to the PMOS 31 of the amplification circuit 10B declines, the power consumption of this amplification circuit 10b declines. Therefore, when the control signal SA is L level, this voltage regulator serves as the series type structure in the low power-consumption mode.

[0081] As mentioned above, in the fourth embodiment, the voltage regulator has the amplification circuit 10B which enters in to the low power-consumption mode according to the standby signal SA. Therefore, the voltage regulator can

Petitioner Micron Ex-1004, 0166

be operated in the low power-consumption mode at the time of standby, by using standby signal SA and the control signal SB.

[0082] In addition, this invention is not limited to the above-mentioned case of the operation, but various modifications is possible for it. As a modification, there are followings, for example.

(a) A bipolar transistor may be replaced with the PMOS 31 and the NMOS 32

(b) The structure of the amplification circuit 10 or the constant current circuit 40 is not limited to what is illustrated, but if the same operation is possible, it can apply the thing of any circuit structures.

(c) The connection point, where the capacitor 33 for phase compensation and the capacitor 34 for phase compensation are connected to each other, is not limited to the point illustrated in figures. The connection point may be set at a point so that an amplification circuit will not be in an oscillation state by phase compensation.

(d) The PMOS, whose ON/OFF state is controlled by the controls signal S1 and which is connected between output node NO and the NMOS 32, may be replaced with the NMOS 52 in Fig. 6 and Fig. 8.

(e) The OR 53 in Fig. 8 is omitted and the amplification circuit 10A and the amplification circuit 10B may be made to control by the standby signal SA. In this case, a security mode for operation which needs security and a low power-consumption operation mode can be selected by the standby signal SA.

[0083] As explained above in detail, according to the first embodiment of the invention, the voltage regulator has the constant current circuit which supplies constant current, the first transistor provided in parallel to this constant current circuit, and the second transistor provided between an output node and a common potential. Thereby, when load current exceeds the constant current, current of an insufficiency is supplied from the first transistor. Therefore, the increase in power consumption is suppressed and the analysis of the load circuit by the monitor of load current of operation becomes difficult.

[0084] According to the second embodiment of the invention, the voltage regulator has the first amplification circuit which compares the first divided voltage and a reference voltage and which controls the first transistor, and the second amplification circuit which compares the second divided voltage lower than the first divided voltage and reference voltage and which controls the second transistor. Thereby, since the first transistor is controlled previously, penetration current which flows from power-supply voltage to the common potential through the first and the second transistor can be prevented.

[0085] According to the third embodiment of the invention, the voltage regulator has a switch means to stop current which flows to a constant current circuit and the second transistor according to the control signal. Thereby, useless consumption current can be lost in the application which does not need security.

[0086] According to the fourth embodiment of the invention, the voltage regulator has a switch means to stop current which flows to a constant current circuit and the second transistor according to a control signal. Furthermore, it has a structure to stop amplification operation of the second amplification circuit with this control signal. Thereby, in the application which does not need security, consumption current can be reduced further.

[0087] According to the fifth embodiment of the invention, the voltage regulator has a switch means to stop current which flows to a constant current circuit and the second transistor when a standby signal or a control signal is applied. Furthermore, it has a structure so that operation of the second amplification circuit may be stopped. Furthermore, when a standby signal is received, the first amplification circuit may be made into the low consumption current mode. Thereby, in the application which does not need security, while power consumption can be reduced, at the time of standby, reduction of power consumption is further attained by the low consumption current mode.

[0088] According to the sixth to eighth embodiments of the invention, the voltage regulator has the first adjustment means which controls current which flows from an input node to the first node based on the voltage difference of the first divided voltage and reference voltage and the second adjustment means which controls current which flows from the first node to the second node based on the voltage difference of the second divided voltage and reference voltage. Thereby, when load current exceeds the supply capability of the constant current source, current of an insufficiency is supplied from the first adjustment means. Therefore, the analysis of the load circuit by the monitor of load current of operation becomes difficult.

[0089] While the preferred form of the present invention has been described, it is to be understood that modifications will be apparent to those skilled in the art without departing from the invention as defined in the claims. The scope of the invention, namely, is to be determined solely by the following claims.

Claims

1. A semiconductor integrated voltage regulator comprising:

Petitioner Micron Ex-1004, 0167

an input node (VDD) which is supplied with a first voltages (VDD),
an output node (VREG) which is coupled to a first node (10);
a second node (GND) which is supplied with a second voltage (GND) lower than the first voltage (GND) (VDD),
a constant current source (40) which is coupled between the input node (VDD) and the first node (N0);
a first adjustment circuit (31) which controls the amount of current flowing between the input node (VDD) and the first node (N0) according to a voltage level (V01) of a first control signal; and
a second adjustment circuit (32) which controls the amount of current flowing between the first node (N0) and the second node (GND) according to a voltage level (V02) of a second control signal.

2. A voltage regulator according to Claim 1, further comprising;

a first amplification circuit (10_1) which amplifies a voltage difference between a reference voltage (VR); and a first divided voltage (VC_1) and which outputs the first control signal (VR) ; and
a second amplification circuit (V01) which amplifies a voltage difference between a reference voltage (VR) and a second divided voltage (VC_2) and which outputs the second control signal (V02).

3. A voltage regulator according to Claim Z, wherein the first adjustment circuit (31) comprises a P type MOS transistor and wherein the second adjustment circuit (32) comprises an N type MOS transistor.

Patentansprüche

1. Integrierter Halbleiter-Spannungsregler, welcher aufweist:

einen Eingangsknoten (VDD), der mit einer ersten Spannung (VDD) versorgt wird;
einen Ausgangsknoten (VREG), der an einen ersten Knoten (NO) gekoppelt ist;
einen zweiten Knoten (VREG), der mit einer zweiten Spannung (GND), die niedriger ist als die erste Spannung (VDD), versorgt wird;
eine Konstantstromquelle (40), die zwischen den Eingangsknoten (VDD) und dem ersten Knoten (NO) geschaltet ist;
eine erste Anpassungsschaltung (31), die die Strommenge, die zwischen dem Eingangsknoten (VDD) und dem ersten Knoten (NO) in Übereinstimmung mit dem Spannungspegel (V01) eines ersten Steuersignals steuert; und
eine zweite Anpassungsschaltung (32), die die Strommenge, die zwischen dem ersten Knoten (NO) und dem zweiten Knoten (GND) in Übereinstimmung mit einem Spannungspegel (V02) eines zweiten Steuersignals steuert.

2. Spannungsregler nach Anspruch 1, welcher ferner aufweist:

eine erste Verstärkerschaltung (10_1), die eine erste Spannungsdifferenz zwischen einer Referenzspannung (VR) und einer geteilten Spannung (VC_1) verstärkt und das erste Steuersignal (VR) ausgibt; und
eine zweite Verstärkerschaltung (V01), die eine Spannungsdifferenz zwischen einer Referenzspannung (10_2) und einer zweiten geteilten Spannung (VC_2) verstärkt und das zweite Steuersignal (V02) ausgibt.

3. Spannungsregler nach Anspruch 2, wobei die erste Anpassungsschaltung (31) einen P Typ MOS-Transistor aufweist und die zweite Anpassungsschaltung (32) einen N Typ MOS-Transistor aufweist.

Revendications

1. Régulateur de tension intégré à semiconducteur comprenant :

un noeud d'entrée (VDD) qui reçoit une première tension (VDD),
un noeud de sortie (VREG) qui est couplé à un premier noeud (NO),
un deuxième noeud (GND) qui reçoit une deuxième tension (GND) inférieure à la première tension (VDD),
une source de courant constant (40) qui est couplée entre le noeud d'entrée (VDD) et le premier noeud (NO),
un premier circuit de réglage (31) qui commande l'intensité du courant circulant entre le noeud d'entrée (VDD) et le premier noeud (NO) conformément à un niveau de tension (VO1) d'un premier signal de commande, et
un deuxième circuit de réglage (32) qui commande l'intensité du courant circulant entre le premier noeud (NO)

Petitioner Micron Ex-1004, 0168

et le deuxième noeud (GND) conformément à un niveau de tension de tension (VO2) d'un deuxième signal de commande.

2. Régulateur de tension selon la revendication 1, comprenant en outre,
un premier circuit d'amplification (10_1) qui amplifie une différence de tension entre une tension de référence (VR) et une première tension divisée (VC1) et qui fournit en sortie le premier signal de commande (VR), et
un deuxième circuit d'amplification (10_2) qui amplifie une différence de tension entre une tension de référence (VR) et une deuxième tension divisée (VC2) et qui fournit en sortie le deuxième signal de commande (V02).

3. Régulateur de tension selon la revendication 2, dans lequel le premier circuit de réglage (31) comprend un transistor MOS de type P et dans lequel le deuxième circuit de réglage (32) comprend un transistor MOS de type N.

Petitioner Micron Ex-1004, 0169

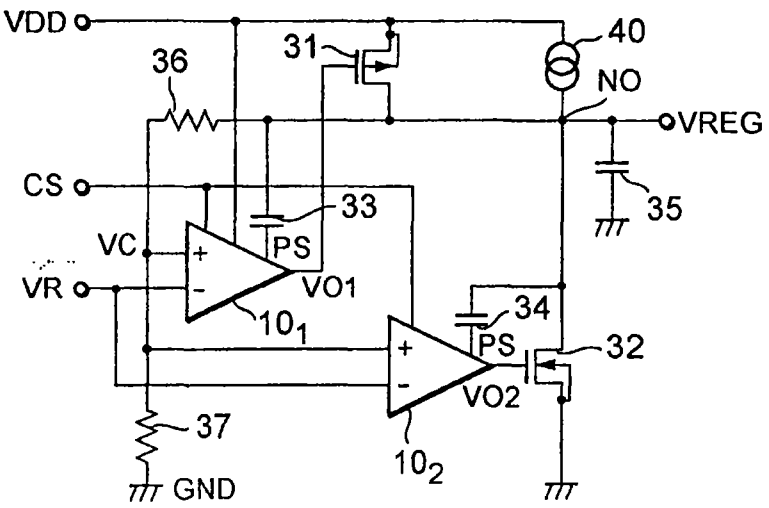


Fig.1

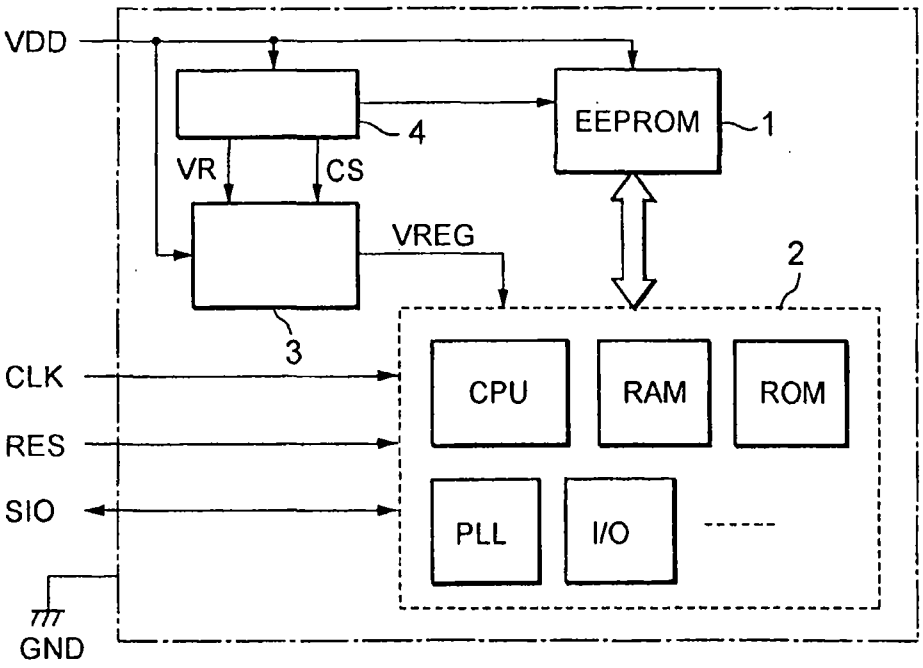


Fig.2

Petitioner Micron Ex-1004, 0170

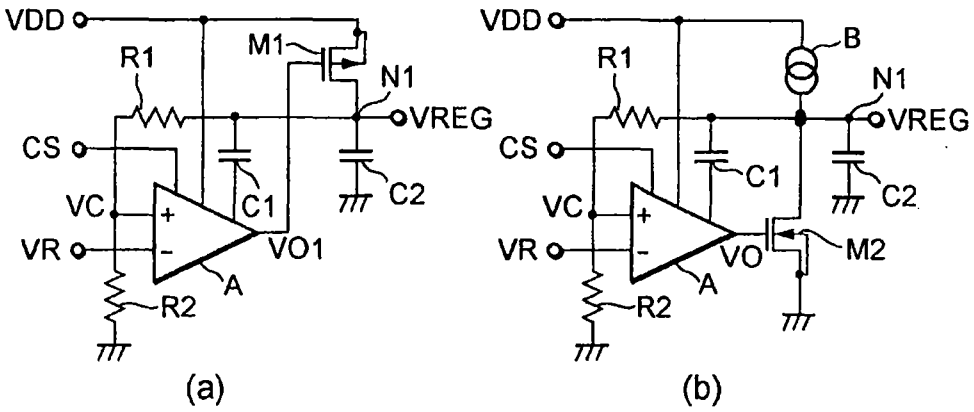


Fig.3

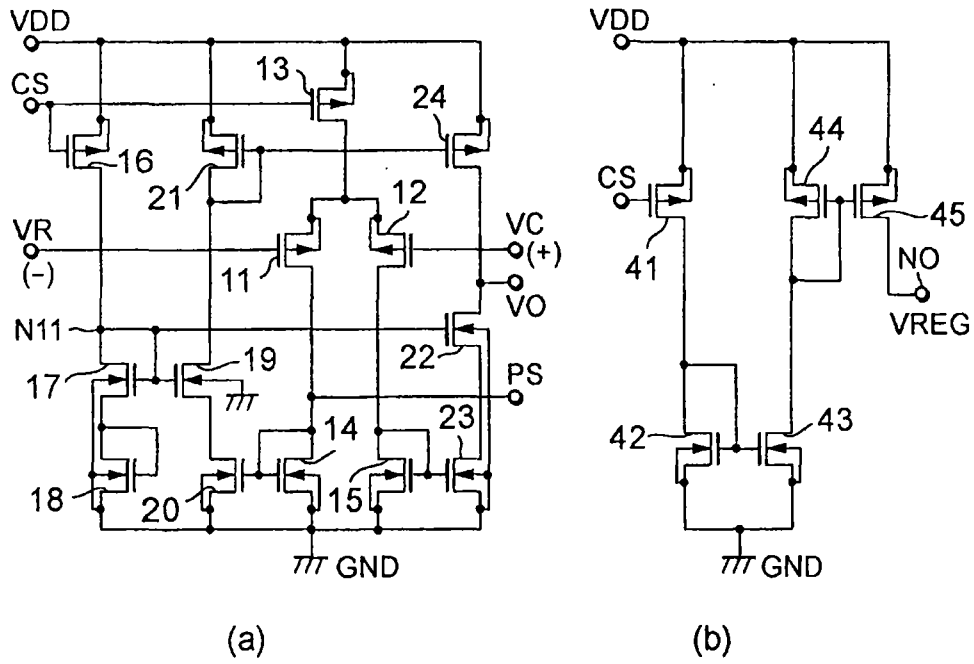


Fig.4

Petitioner Micron Ex-1004, 0171

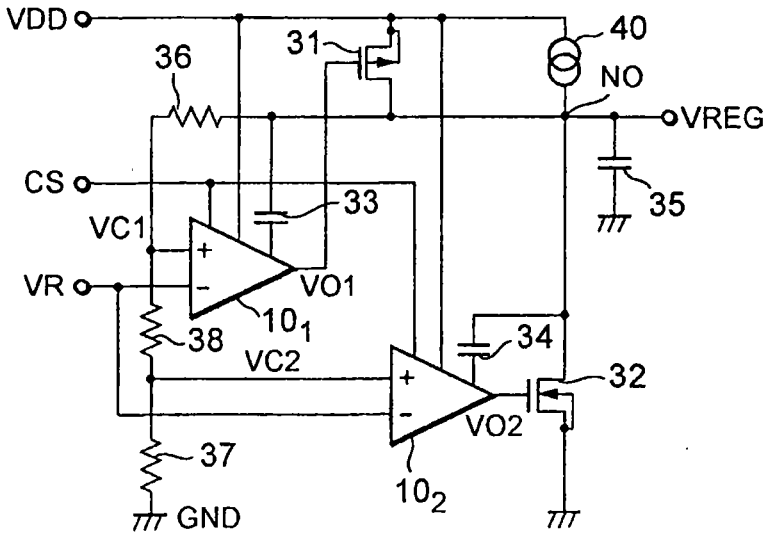


Fig.5

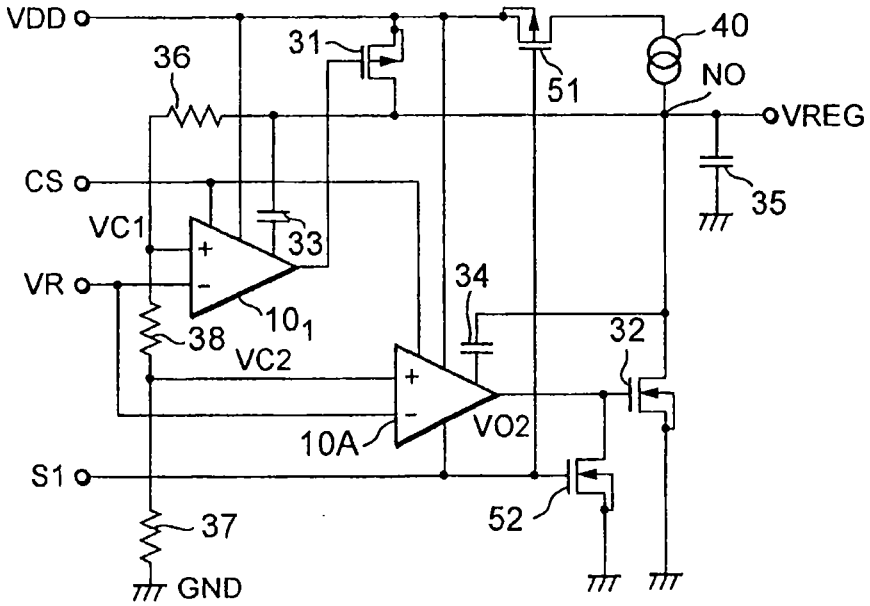


Fig.6

Petitioner Micron Ex-1004, 0172

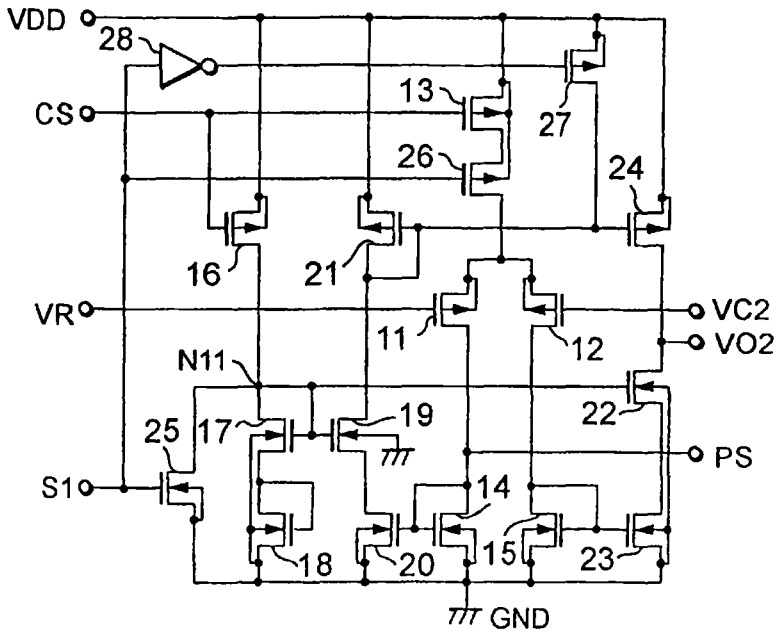


Fig.7

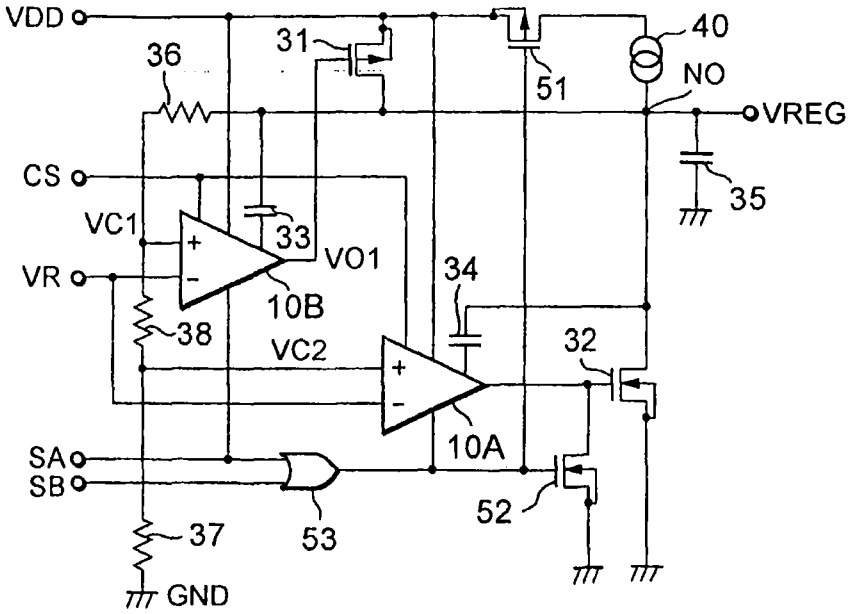


Fig.8

Petitioner Micron Ex-1004, 0173

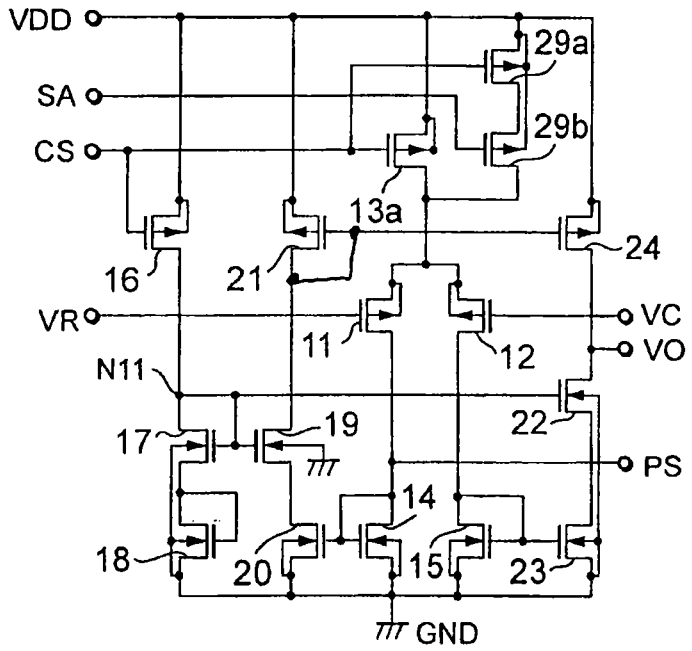


Fig.9

Petitioner Micron Ex-1004, 0174

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- JP 2001229374 A **[0002]**
- EP 1107502 A **[0019]**

Petitioner Micron Ex-1004, 0175

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 661 717 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
29.03.2000 Bulletin 2000/13

(51) Int. Cl.[7]: **G11C 16/06**, G11C 5/14

(21) Application number: **93830545.5**

(22) Date of filing: **31.12.1993**

(54) Voltage regulator for programming non-volatile and electrically programmable memory cells

Spannungsregler zum Programmieren nichtflüchtiger und elektrisch programmierbarer Speicherzellen

Régulateur de tension pour la programmation des cellules de mémoire non volatiles, électriquement programmables

(84) Designated Contracting States:
DE FR GB IT

(43) Date of publication of application:
05.07.1995 Bulletin 1995/27

(73) Proprietor:
STMicroelectronics S.r.l.
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Maccarrone, Marco**
  I-22030 Palestro (PV) (IT)
- **Olivo, Marco**
  I-24100 Bergamo (BG) (IT)
- **Golla, Carla**
  I-20099 Sesto S. Giovanni (MI) (IT)
- **Padoan, Silvia**
  I-47037 Rimini (FO) (IT)

(74) Representative: **Botti, Mario**
Botti & Ferrari S.r.l.
Via Locatelli, 5
20124 Milano (IT)

(56) References cited:
EP-A- 0 397 408
EP-A- 0 525 679
EP-A- 0 538 121
US-A- 4 804 865

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

Printed by Xerox (UK) Business Services
2.16.7/3.6

EP 0 661 717 B1

Petitioner Micron Ex-1004, 0176

Description

Field of the Invention

[0001] This invention relates to a voltage regulator which allows the terminals of a memory cell to be suitably biased.

[0002] More particularly, the invention relates to non-volatile memory device including a voltage regulator for programming non-volatile memory cells, which regulator comprises a differential amplifier stage being powered between a first and a second voltage reference and having a first input terminal connected to a voltage divider of said first reference voltage, a second input terminal connected to a programming line and an output terminal connected to a source-follower transistor which is coupled to said first input through a current mirror and connected to the cells through the programming line

[0003] In a well-known manner, a non-volatile memory cell comprises a MOS transistor having a "floating" gate terminal, that is exhibiting a high DC impedance to all the other terminals of the cell and the circuit in which the cell is connected.

[0004] The cell also has a second electrode, known as the control gate electrode, which is driven by appropriate control voltages. The other electrodes of the MOS transistor are the usual drain, source and body terminals.

[0005] By changing the value of the voltage applied to the control gate, the amount of the charge present in the floating gate can be changed. Thus, the transistor can be placed in either of two logic states: a first state with a "high" threshold voltage, and a second state with a "low" threshold voltage.

[0006] By applying a voltage in between these two values to the control gate, the state of the transistor can be "read", since the transistor will either present a low or a high impedance between its drain and source terminals according to the value of the threshold voltage. The transistor functions, therefore, as a logic storage element.

[0007] Furthermore, since the floating gate presents a high impedance to any other terminals of the cell, the charge stored in the transistor can be held for an indefinite length of time, even if the power supply to the circuit in which it is connected is removed. Thus, the cell has non-volatile memory characteristics.

[0008] The operation whereby charge is stored in the floating gate is referred to as the cell "programming", whereas the operation whereby said charge is removed from the floating gate is referred to as the cell "erasing".

[0009] A non-volatile memory circuit integrated to a semiconductor usually includes a very large number of such cells. The cells are laid in rows (word lines) and columns (bit lines). The cells in one row share the line which drives their respective control gates. The cells in the same bit line share the drain electrode. In order to program a given cell, it is necessary that the appropriate positive voltage values be impressed on the word line and the bit line that locate it.

[0010] A memory cell programming is strongly affected by the voltage applied to the drain terminal, that is the voltage VP present on the bit line to which it belongs.

[0011] Also known is that with non-volatile memory cells, in particular of the flash type, a reduced value of said drain voltage VP gives rise to insufficient and slow cell programming, whereas an exccessively large value results in the cell being partially erased (the so-called "soft erasing" phenomenon). Thus, the optimum range for VP is fairly narrow, typically between about 5 and 6 V.

[0012] The foregoing considerations lead to conclude that the memory circuit should be provided with a particularly sophisticated and accurate voltage regulator to supply the bit line with the appropriate voltage during the programming step.

Background Art

[0013] It is well known that one of the methods employed to program memory cells utilizes the phenomenon of the injection of hot electrons through the gate oxide of the cell.

[0014] For the injection process to be triggered, it is necessary that the cell terminals be suitably polarized; the drain-source voltage should attain a value in the 5 to 6 volts range, in order to accelerate the electrons present in the channel, while the gate-source voltage should be a value of about 12 volts, so as to attract the accelerated electrons.

[0015] However, as previously mentioned, what is critical is the value of the drain voltage VP, and this should be held as stable as possible during the programming.

[0016] The fluctuations in said voltage are tied to the following factors:

- technological changes in the manufacturing processes of the various components;
- increased threshold voltage of the cell during the programming, and consequent decrease in current draw; and,
- voltage drops across the selection transistors present in the bit lines.

[0017] The last-mentioned is a significant effect especially with large capacity memories, wherein in view of the small dimensions involved, the selection transistors have a particularly small W/L (channel width to length) ratio and, therefore, high series resistance.

[0018] Thus, there evidently exists a need for a voltage regulator of sufficiently refined design to take account of all the factors involved. The prior art solves these problems by providing a circuit wherein the output

Petitioner Micron Ex-1004, 0177

voltage from the regulator exceeds that sought for the bit line by an appropriate amount which is continually dependent on the actual current flowing through the selection transistors in the bit line.

[0019] To accomplish this, a polarization technique of the adaptive type is employed which provides for a positive feedback structure. An example of this prior approach is shown schematically in Figure 1 and disclosed in EP 92830340.9 (EP-A-0576774), which falls under Article 54(3) EPC. In essence, a voltage generator generates a constant voltage (VPROG) equal to the voltage that should appear on the selected bit line if optimum programming conditions are to be provided. That voltage is added a varying voltage, designated Vcomp. The value Vcomp is obtained by mirroring the current supplied from the regulator to the bit line on elements which are mirror-images of the bit line selection transistors, thereby producing the same voltage drop across them.More specifically, the regulated voltage is supplied from a source-follower MOS transistor, designated MOUT, which is driven by a suitably fed-back operational amplifier (4). This arrangement includes two feedback loops: a first loop inherent to the voltage regulator, and the second loop (comprising a MOS transistor, designated MPR2, and a generic block H) to compensate for the voltage drop at the bit line. The second loop supplies a current to a drop resistance Rdrop which is proportional to the current from the regulator, and hence, tied to that drawn by the cell being programmed.

[0020] In a storage device, the programming usually takes place in parallel through all the cells of one word; of course, only those cells whereat a voltage rise is to occur, i.e. which are to contain a logic "1", would be actually programmed.

[0021] The current drawn from the bit line at the programming stage will depend, therefore, on the pattern of bits to be stored. To avoid altering the compensation, the drop resistance should be varied accordingly.

[0022] However, this prior approach has some drawbacks, as follows:

- the bias current drawn by the MOS M9, shown in Figure 1, is carried over to the drop resistance to cause an undesired constant component to appear in the compensation voltage Vcomp. This constant voltage component is particularly objectionable where a single cell is programmed, because in this case, the current drawn by the transistor M9 is then no longer negligible against that required for the programming; and

- while the cells are being read, the bit line is polarized to a voltage of about 1 V, and connected to the line VP via a p-channel MOS transistor. This transistor has its gate voltage Vg0 = 0 V (as impressed by a switch being also supplied VP) and its source voltage Vs0 = 1 V, and is therefore in conduction.

[0023] At the reading stage, the programming voltage VP is zero and the p-channel MOS transistor connects the capacitance associated with the junction of the conducting transistor MOUT to the bit line; as a result, the capacitance of the bit line is greatly increased and its reading speed greatly decreased. This is a baffling phenomenon in that it only comes out where the bit line takes a higher voltage than the p-channel threshold voltage; this may happen when the supply voltage exceeds its rated value. Accordingly, this phenomenon should be carefully suppressed.

[0024] The underlying technical problem of this invention is to provide a voltage regulator which can supply the voltage actually needed for proper programming, but also hold the programming line and bit line decoupled while the latter is being read.

Summary of the Invention

[0025] The solutive idea on which the invention stands is to provide a voltage regulator which comprises an amplifier stage controlled by a compensation voltage which is made independent of the voltage drop due to a resistive path connecting the programming line to the device ground reference.

[0026] In addition, this regulator should contain a structure which allows the reading speed of the cells in the bit line to be improved, while decoupling it from the programming line to thereby eliminate the above-outlined drawbacks.

[0027] Based on this solutive idea, the technical problem is solved by a voltage regulator as previously indicated and defined in the characterizing parts of the appended claims.

[0028] The features and advantages of a circuit according to the invention will be apparent from the following detailed description of an embodiment thereof, given by way of example and not of limitation with reference to the accompanying drawings.

Brief Description of the Drawings

[0029]

- Figure 1 is a diagram illustrating the principle which underlies a voltage regulator of a prior approach.

- Figure 2 shows diagramatically a regulator according to the invention.

- Figure 3 shows schematically a circuit generating signals which appear in the regulator of Figure 2.

Detailed Description

[0030] Figure 1 relates to an embodiment of a voltage regulator according to the prior art as previously discussed.

Petitioner Micron Ex-1004, 0178

[0031] With reference to Figure 2, generally and schematically shown at 1 is the circuit architecture of a voltage regulator according to the invention.

[0032] The regulator 1 comprises an amplifier stage 4 incorporating two MOS transistors of the n-channel type, with source terminals connected together and to the drain terminal DG1 of a MOS transistor MG1 which functions as a current generator. The drain terminals of said transistors are connected to the drain terminals of another two MOS transistors of the p-channel type, in a current mirror configuration.

[0033] The amplifier 4 is connected between a first or programming voltage reference VPP, through a further MOS transistor MX, and a second voltage reference, in essence a signal ground GND.

[0034] The gate terminal of the last-mentioned MOS transistor MX is applied a first reference voltage VR1, whereas the voltage reference GND is applied to the source terminal SG1 of the transistor MG1.

[0035] The input I1 of the stage 4 is connected to the drain terminal D1 of a MOS transistor M1, which has its body terminal B1 connected to the voltage reference GND and source S1 and gate G1 terminals connected across a resistive element R2.

[0036] The resistive element R2 is connected in a resistive divider, generally denoted by 2. Said divider 2 comprises a series of three resistive elements and is placed between the voltage reference VPP and the output terminal, O3, of a current mirror generally denoted by 3.

[0037] Said current mirror 3 comprises four MOS transistors, and allows a current IC to be carried over to the input I3 of the divider 2 which is proportional to the current IC' supplied to a transistor MOUT to be described.

[0038] Advantageously, a resistive path 7 is connected to the current mirror 3 which comprises a MOS transistor M2. This transistor M2 has its drain terminal D2 connected to the current mirror 3, its body B2 and source S2 terminals connected to the voltage reference GND, and its gate terminal G2 controlled by a signal A.

[0039] The point of interconnection between the resistive divider 2 and the output of the mirror 3, denoted by I3, is also connected to a network of compensation resistive elements, generally denoted by 5.

[0040] That network 5 consists of a set of MOS transistors which function as resistive elements and are selected on the basis of the bit pattern to be programmed in the memory word; basically, for each bit to be programmed there corresponds a different compensation transistor.

[0041] Said network 5 is connected between the voltage reference GND and a second polarization signal VR2. Advantageously, connected in parallel with the network 5 is a resistive path 8 comprising a MOS transistor M3 which has its gate terminal G3 connected to the reference VR2, its drain terminal D3 connected to the node I3, its body terminal B3 connected to the voltage reference GND, and its source terminal S3 connected to a point CT of a series of two MOS transistors M4 and M5.

[0042] The MOS transistors M4 and M5 are connected between the voltage reference GND and the network 5 of resistive elements, being controlled at their gate terminals G4 and G5, respectively, by a signal PP (Parallel Programming) and an enable signal A.

[0043] These transistors function substantially in lieu of the network 5 during the memory testing procedure.

[0044] The gate G5 of the transistor M5 is connected to the gate terminals GG1 and GG2 of the transistors MG1 and MG2, and receives the enable signal A.

[0045] The transistor MG2 is connected between the current mirror 3 and the voltage reference GND, and has its body BG2 and source SG2 terminals connected together.

[0046] The output O1 of the amplifier stage 4 is connected to ground through the drain terminal D6 of a further MOS transistor M6 which has its body B6 and source S6 terminals connected to the voltage reference GND. The gate terminal G6 of the MOS transistor M6 is applied a negative logic signal AN which allows the output O1 of the amplifier 4 to be connected to ground during the turn-off step.

[0047] This signal AN is expediently also applied to the gate terminal G7 of a MOS transistor M7, connected in series with another MOS transistor, M8.

[0048] These MOS transistors, M7 and M8, are included to a decoupling element, generally denoted by 6. In addition, they have their body terminals connected together and to the voltage reference GND; the source terminal S7 of transistor M7 is connected to the programming line VP.

[0049] The transistor M8, on the other hand, is configured as a diode, with its gate and source terminals connected together and to a further voltage reference VDD.

[0050] The output O1 of the amplifier stage 4 is connected to ground via a parasitic capacitance C1 which ensures the amplifier stability. Further, the output O1 is connected to the source-follower transistor MOUT. The signals A and AN are generated by a circuit, generally shown at 9 in Figure 3. This circuit 9 comprises a logic gate PL of the NOR type having two inputs A9 and B9 and an output O9.

[0051] The inputs A9 and B9 are applied the external signals VO and PW, with the former being brought to negative logic by means of an inverter IN1.

[0052] The output O9 is connected to the source terminal of a MOS transistor M9 whose gate terminal G9 is applied the external signal VCCLOW.

[0053] This signal reveals dangerous drops in the supply voltage to the circuit.

[0054] The body B9 and source S9 terminals of that transistor M9 are connected to the voltage reference GND.

[0055] The output O1 supplies the signal A and signal AN, the latter being obtained from A by means of an inverter IN2. Thus, these signals can enable the on and

Petitioner Micron Ex-1004, 0179

off states of the regulator 1.

[0056] The operation of the voltage regulating circuit of this invention will now be discussed.

[0057] The current mirror 3 allows the compensation to be effected of the voltage drop caused by the series resistance of a bit line for which programming is sought. Said compensation is provided by adding, to the desired reference voltage as obtained through the resistive divider 2 from the voltage reference VPP, a voltage which varies according to the current drawn by the cell or cells being programmed.

[0058] The provision of the transistor MG2, as necessary to maintain a resistive path from VP to ground, brings about an undesired voltage offset component.

[0059] The circuit arrangement of this invention overcomes this problem by the inclusion of the transistor M2, which will substract a fraction of the bias current from the mirrored current. Said fraction is determined by the W/L ratii of the transistors provided in the current mirror 3.

[0060] This allows any offset voltage present on the programming line to be carried over to the input and compensated.

[0061] Furthermore, to improve the regulation linearity as the number of the programmed cells varies, this arrangement provides for the connection of a permanent resistive path 8 in parallel with the resistive elements selected in the network 5, through the transistor M3.

[0062] Finally, the decoupling element 6, comprising the series of the transistors M7 and M8, can bias, upon the regulator being turned off, the programming voltage VP to a value equal to the supply voltage VDD minus the value of the threshold voltage VT of one, M8, of the transistors, thereby causing the selection p-channel MOS transistors to be held in a cutoff state while the memory cells of the bit line are being read. In this way, the capacitance of the bit line will increase not even during the reading step on account of the connection to VP, and the reading process will not be slowed down.

[0063] Through such innovations, the voltage regulating circuit 1 of this invention can overcome the drawbacks with which the prior art is beset, and improve both the stability and reliability of a non-volatile memory programming and the speed of operation of the memory matrix in the read mode.

Claims

1. A non-volatile memory device including a voltage regulator for programming non-volatile memory cells, said non-volatile memory cells being coupled to a programming line (Vp) through a p-channel selection MOS transistor, the voltage regulator comprising a differential amplifier stage (4) being powered between a first (VPP) and a second (GND) reference voltage and having a first input terminal connected to an output of a voltage divider (2) coupled between said first reference voltage (VPP) and a first node (I3), a second input terminal (I2) connected to said programming line (Vp) and an output terminal connected to the gate of a source-follower transistor (MOUT) which has its drain coupled to said first node (I3) through a current mirror (3) and its source connected to said programming line (VP), the voltage regulator further comprising a decoupling element (6) connected between a supply voltage (VDD) and said programming line (VP) to feed said programming line with a predetermined voltage value upon the voltage regulator being turned off during a read mode.

2. A non-volatile memory device according to Claim 1, characterized in that said decoupling element (6) comprises two MOS transistors (M7,M8) connected serially between the power supply line and the programming line.

3. A non-volatile memory device according to Claim 2, characterized in that the transistors (M7,M8) of the decoupling element (6) have their body terminals (B7,B8) connected together and to the second voltage reference (GND).

4. A non-volatile memory device according to Claim 2, characterized in that the second transistor (M8) of the decoupling element (6) is configured as a diode.

5. A non-volatile memory device according to claim 1, characterized in that it comprises a MOS transistor (MG2) connecting the programming line (VP) to ground and a resistive path (7) connected between the current mirror (3) and the second voltage reference (GND).

6. A non-volatile memory device according to Claim 5, characterized in that said resistive path (7) comprises at least one MOS transistor (M2).

7. A non-volatile memory device according to Claim 6, characterized in that said transistor (M2) has its drain terminal (D2) connected to said current mirror (3) and its source (S2) connected to ground.

8. A non-volatile memory device according to Claim 1, characterized in that it comprises a network (5) of resistive elements, selected on the basis of a bit pattern to be programmed in a memory word, connected between the divider (2) and the second voltage reference (GND), and in that it further comprises a resistive path (8) connected in parallel with the resistive network (5).

9. A non-volatile memory device according to Claim 8, characterized in that said resistive path (8) includes a MOS transistor (M3) connected between the sec-

Petitioner Micron Ex-1004, 0180

ond (GND) and a third (VR2) voltage reference.

10. A non-volatile memory device according to Claim 8, characterized in that said transistor (M3) is connected in parallel with a set of transistors forming said resistive network (5).

Patentansprüche

1. Nicht-flüchtiges Speicherbauelement mit einem Spannungsregler zum Programmieren von nichtflüchtigen Speicherzellen, die über einen P-Kanal-Auswahl-MOS-Transistor an eine Programmierleitung (Vp) gekoppelt sind, wobei der Spannungsregler eine Differenzverstärkerstufe (4) aufweist, die zwischen einer ersten (Vpp) und einer zweiten (GND) Referenzspannung gespeist wird und mit einem ersten Eingangsanschluß an einen Ausgang eines Spannungsteilers (2) angeschlossen ist, der zwischen der ersten Referenzspannung (Vpp) und einem ersten Knoten (I3) liegt, mit einem zweiten Eingangsanschluß (I2) an die Programmierleitung (Vp) und mit einem Ausgangsanschluß an das Gatter eines Source-Folger-Transistors (MOUT) angeschlossen ist, dessen Drain mit dem ersten Knoten (I3) über einen Stromspiegel (3) gekoppelt ist, und dessen Source an die Programmierleitung (Vp) angeschlossen ist, wobei der Spannungsregler außerdem ein Entkopplungselement (6) aufweist, welches zwischen einer Versorgungsspannung (Vdd) und der Programmierleitung (Vp) liegt, um die Programmierleitung mit einem vorbestimmten Spannungswert zu speisen, wenn der Spannungsregler während einer Lesebetriebsart abgeschaltet wird.

2. Nicht-flüchtiges Speicherbauelement nach Anspruch 1, dadurch gekennzeichnet, daß das Entkopplungselement (6) zwei MOS-Transistoren (M7, M8) aufweist, die in Reihe zwischen der Versorgungsspannungsleitung und der Programmierleitung liegen.

3. Nicht-flüchtiges Speicherbauelement nach Anspruch 2, dadurch gekennzeichnet, daß die Transistoren (M7, M8) des Entkopplungselements (6) mit ihren Substratanschlüssen (B7, B8) zusammengeschaltet und an die zweite Spannungsreferenz (GND) geschaltet sind.

4. Nicht-flüchtiges Speicherbauelement nach Anspruch 2, dadurch gekennzeichnet, daß der Transistor (M8) des Entkopplungselements (6) als Diode konfiguriert ist.

5. Nicht-flüchtiges Speicherbauelement nach Anspruch 1, dadurch gekennzeichnet, daß es einen MOS-Transistor (MG2) aufweist, der die Programmierleitung (Vp) mit Masse verbindet, und einen Widerstandspfad (7) aufweist, der zwischen dem Stromspiegel (2) und der zweiten Spannungsreferenz (GND) liegt.

6. Nicht-flüchtiges Speicherbauelement nach Anspruch 5, dadurch gekennzeichnet, daß der Widerstandspfad (7) mindestens einen MOS-Transistor (M2) aufweist.

7. Nicht-flüchtiges Speicherbauelement nach Anspruch 6, dadurch gekennzeichnet, daß der Transistor (M3) mit seinem Drainanschluß (D2) an den Stromspiegel (3) und mit seiner Source (S2) an Masse angeschlossen ist.

8. Nicht-flüchtiges Speicherbauelement nach Anspruch 1, dadurch gekennzeichnet, daß es ein Netzwerk (5) aus Widerstandselementen aufweist, ausgewählt auf der Grundlage eines in einem Speicherwort zu programmierenden Bitmusters und zwischen dem Teiler (2) und der zweiten Spannungsreferenz (GND) liegend, und daß es außerdem einen Widerstandspfad (8) aufweist, der parallel zu dem Widerstandsnetzwerk (5) geschaltet ist.

9. Nicht-flüchtiges Speicherbauelement nach Anspruch 8, dadurch gekennzeichnet, daß der Widerstandspfad (8) einen MOS-Transistor (M3) aufweist, der zwischen der zweiten (GND) und einer dritten (VR2) Spannungsreferenz liegt.

10. Nicht-flüchtiges Speicherbauelement nach Anspruch 8, dadurch gekennzeichnet, daß der Transistor (M3) parallel zu einem Satz von das Widerstandsnetzwerk (5) bildenden Transistoren geschaltet ist.

Revendications

1. Dispositif de mémoire non-volatile comprenant un régulateur de tension pour programmer des cellules de mémoire non-volatiles, lesdites cellules de mémoire non-volatiles étant couplées à une ligne de programmation (Vp) par l'intermédiaire d'un transistor MOS de sélection à canal P, le régulateur de tension comprenant un étage d'amplificateur différentiel (4) alimenté entre une première (VPP) et une deuxième (GND) tension de référence et ayant une première borne d'entrée connectée à une sortie d'un diviseur de tension (2) couplé entre la première tension de référence (VPP) et un premier noeud (I3), une seconde borne d'entrée (I2) connectée à la ligne de programmation (Vp) et à une borne de sortie connectée à la grille d'un transistor suiveur de source (MOUT) dont le drain est couplé au premier noeud (I3) par l'intermédiaire d'un miroir

Petitioner Micron Ex-1004, 0181

de courant (3) et dont la source est connectée à la ligne de programmation (VP), le régulateur de tension comprenant en outre un élément de découplage (6) connecté entre une tension d'alimentation (VDD) et la ligne de programmation (VP) pour fournir à la ligne de programmation une valeur de tension prédéterminée lorsque le régulateur de tension est inactivé lors d'un mode de lecture.

2. Dispositif de mémoire non-volatile selon la revendication 1, caractérisé en ce que l'élément de découplage (6) comprend deux transistors MOS (M7, M8) connectés en série entre la ligne d'alimentation et la ligne de programmation.

3. Dispositif de mémoire non-volatile selon la revendication 2, caractérisé en ce que les transistors (M7, M8) de l'élément de découplage (6) ont leurs bornes de substrat (B7, B8) connectées ensemble et à la deuxième référence de tension (GND).

4. Dispositif de mémoire non-volatile selon la revendication 2, caractérisé en ce que le second transistor (M8) de l'élément de découplage (6) est configuré en diode.

5. Dispositif de mémoire non-volatile selon la revendication 1, caractérisé en ce qu'il comprend un transistor MOS (MG2) qui connecte la ligne de programmation (VP) à la masse et un chemin résistif (7) entre le miroir de courant (3) et la deuxième référence de tension (GND).

6. Dispositif de mémoire non-volatile selon la revendication 5, caractérisé en ce que le chemin résistif (7) comprend au moins un transistor MOS (M2).

7. Dispositif de mémoire non-volatile selon la revendication 6, caractérisé en ce que le transistor (M2) a sa borne de drain (D2) connectée au miroir de courant (3) et sa source (S2) connectée à la masse.

8. Dispositif de mémoire non-volatile selon la revendication 1, caractérisé en ce qu'il comprend un réseau (5) d'éléments résistifs, sélectionnés sur la base d'un motif de bits devant être programmé dans un mot de mémoire, connecté entre le diviseur (2) et la deuxième référence de tension (GND), et en ce qu'il comprend en outre un chemin résistif (8) connecté en parallèle avec le réseau résistif (5).

9. Dispositif de mémoire non-volatile selon la revendication 8, caractérisé en ce que le chemin résistif (8) comprend un transistor MOS (M3) connecté entre la deuxième (GND) et une troisième (VR2) référence de tension.

10. Dispositif de mémoire non-volatile selon la revendication 8 caractérisé en ce que le transistor (M3) est connecté en parallèle avec un ensemble de transistors formant le réseau résistif (5).

Petitioner Micron Ex-1004, 0182

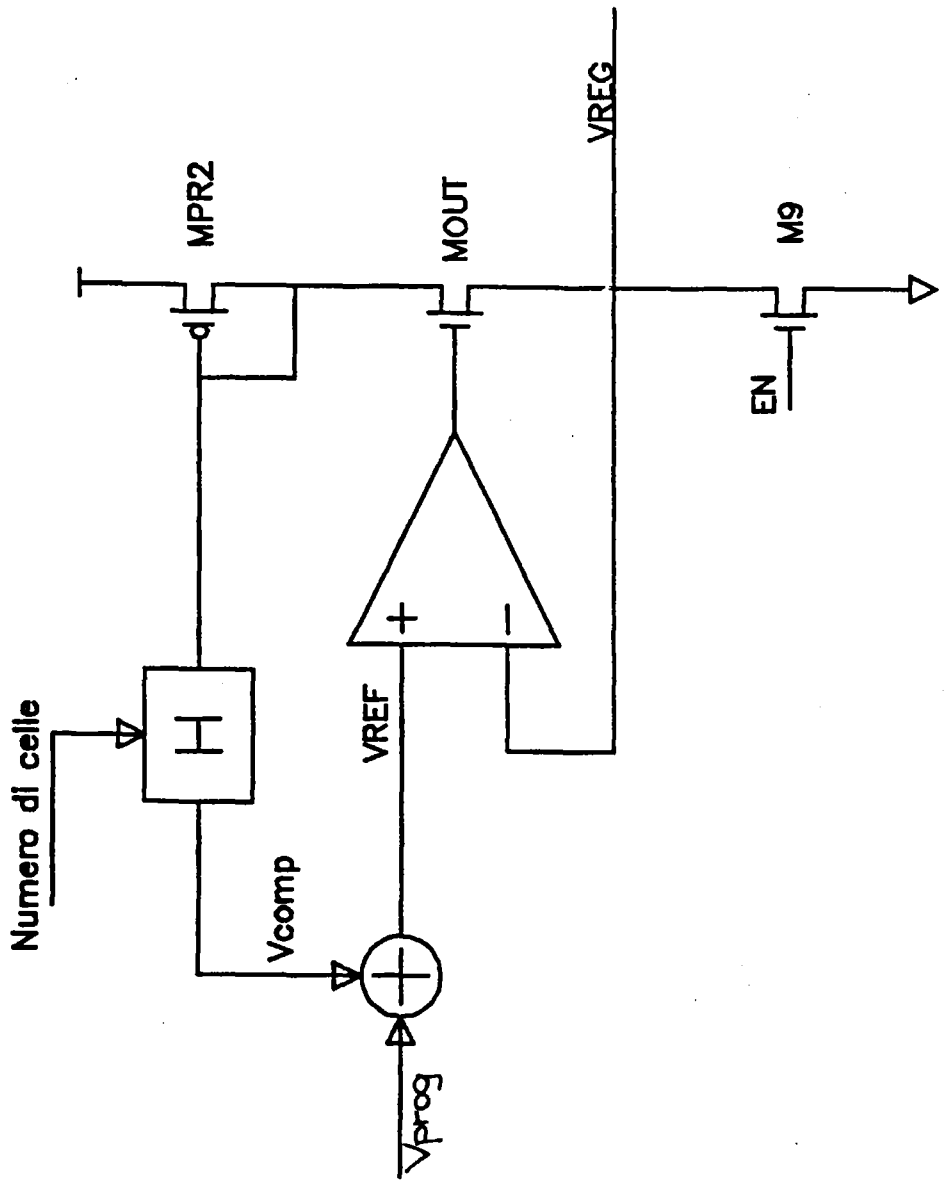


FIG. - 1

Petitioner Micron Ex-1004, 0183

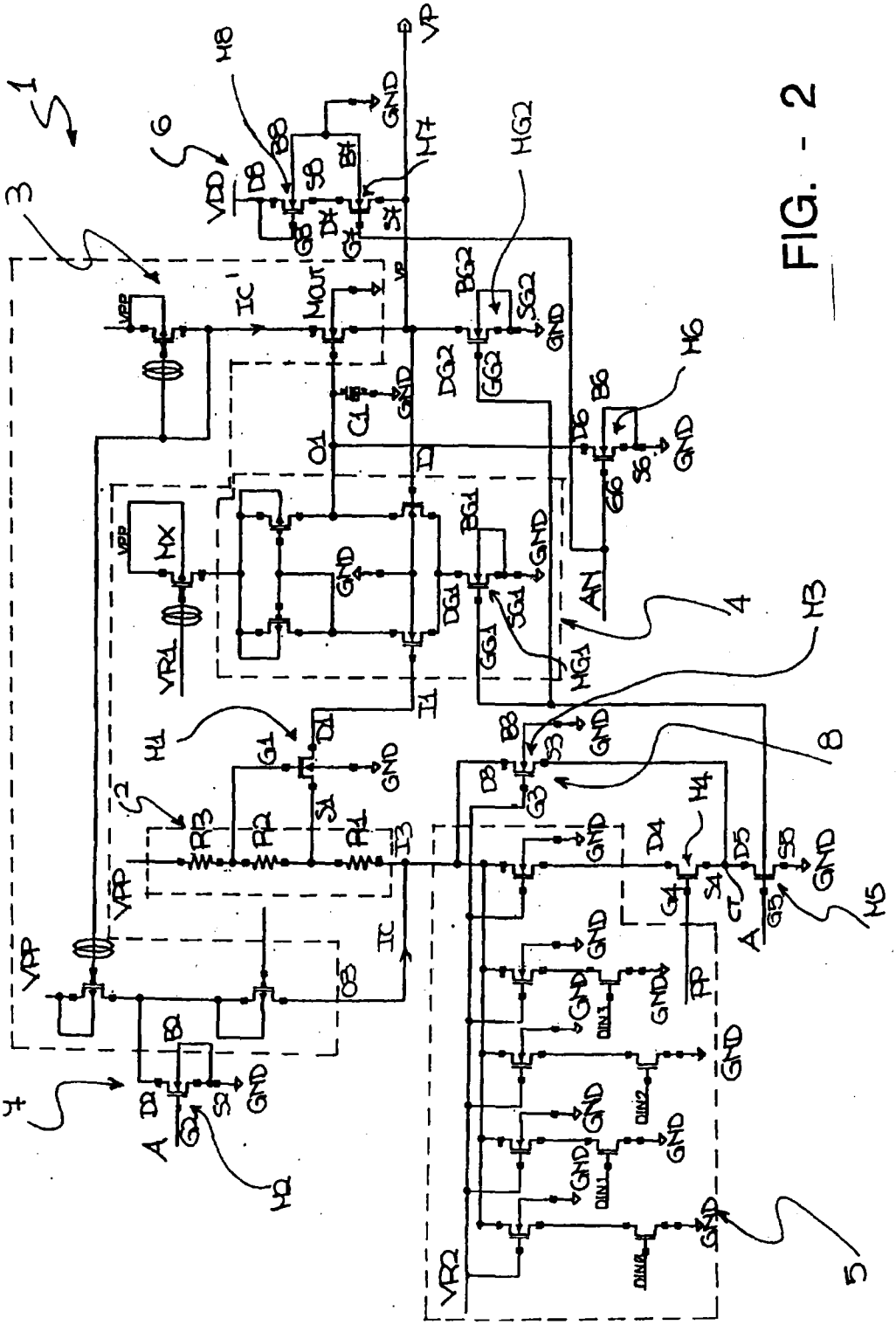


FIG. - 2

Petitioner Micron Ex-1004, 0184

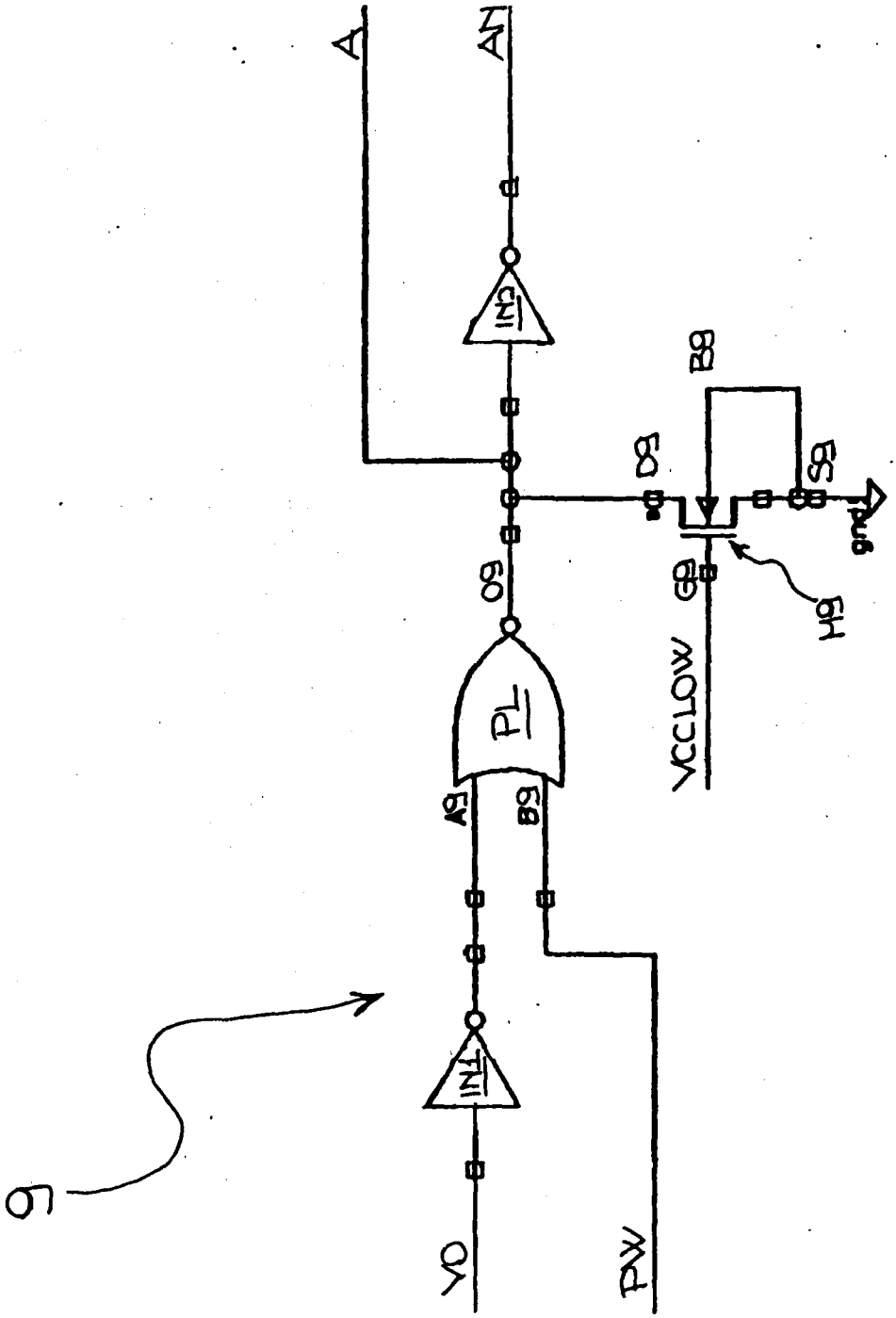


FIG. - 3

Petitioner Micron Ex-1004, 0185

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 4146.08US01

Elran Confirmation No.: *Unknown*

Application No.: *Unknown* Examiner: *Unknown*

Filed: *Unknown* Group Art Unit: *Unknown*

For: CAPLESS SOURCE FOLLOWER REGULATOR

INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

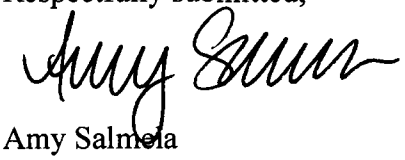
Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of the above-referenced application, and be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

The listing of a reference herein is not an admission that the reference is prior art or is material to patentability. 37 CFR § 1.97(h). Applicant reserves the right to establish the patentability of any claimed invention over any of the information provided herewith, and/or prove that this information may not be prior art, and/or prove that this information may not be enabling for any aspect of the information provided herewith.

This Information Disclosure Statement is being filed without a certification or fee because this Information Disclosure Statement is being filed with the application. No certification or fee is required. 37 CFR § 1.97(b)(1)(2).

Respectfully submitted,



Amy Salmela
Registration No. 55,910

Customer No. 24113
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South 8th Street
Minneapolis, Minnesota 55402-2100
Telephone: (612) 252-1538

Please grant any extension of time necessary for entry; charge any fee due to Deposit Account No. 16-0631.

Petitioner Micron Ex-1004, 0187

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 497 591 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
02.04.1997 Bulletin 1997/14

(51) Int Cl.[6]: **G05F 3/18**, G05F 1/563

(21) Application number: **92300786.8**

(22) Date of filing: **30.01.1992**

(54) Regulated power supply circuit

Stabilisierte Spannungsquelleschaltung

Circuit d'alimentation régulé

(84) Designated Contracting States:
AT BE CH DE ES FR GB GR IT LI LU NL PT SE

(30) Priority: **30.01.1991 ZA 910683**

(43) Date of publication of application:
05.08.1992 Bulletin 1992/32

(73) Proprietor: **CIRCUIT BREAKER INDUSTRIES LIMITED**
Elandsfontein (ZA)

(72) Inventors:
- **Bjorkman, Ivan Newell**
  Johannesburg, Transvaal (ZA)
- **Nusse, Klaus Joachim Rolf**
  Randburg, Transvaal (ZA)

(74) Representative: **Rackham, Stephen Neil et al**
GILL JENNINGS & EVERY,
Broadgate House,
7 Eldon Street
London EC2M 7LH (GB)

(56) References cited:
EP-A- 0 164 193
DE-A- 3 901 560
US-A- 3 535 613
US-A- 4 806 844

- **ELEKTOR ELECTRONICS. vol. 10, no. 7/8, August 1984, CANTERBURY GB page 755 'Dissipation Limiter for Variable Power Supplies'**
- **IBM TECHNICAL DISCLOSURE BULLETIN. vol. 9, no. 10, March 1967, NEW YORK US page 1461 D.D. BAUMANN 'Floating Regulator for a PMT Power Supply'**

Note: Within nine months from the publication of the mention of the grant of the European patent, any person may give notice to the European Patent Office of opposition to the European patent granted. Notice of opposition shall be filed in a written reasoned statement. It shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 0 497 591 B1

Printed by Jouve, 75001 PARIS (FR)

Petitioner Micron Ex-1004, 0188

Description

This invention relates to a regulated power supply circuit, as well as to a voltage regulator which is employed in such a circuit.

In the past, a number of problems have been associated with regulated power supply circuits which have to cope with wide input voltage ranges. At voltages in excess of 1kV, only relatively low biasing currents can be fed to the power supply in order to avoid high power dissipation. The standard zener transistor configuration requires excessive zener biasing current which results in a high power dissipation. High voltage transistors exhibit relatively low current gains, and the basic current drawn by such transistors loads any reference and may drastically affect regulation with dynamic output loads.

At present, there exists no single commercially available transistor capable of efficiently providing a low voltage regulated supply from an unregulated input exceeding 1kV.

US-4,806,844 discloses a DC voltage regulator comprising a primary voltage regulating circuit and a secondary voltage regulating circuit, the primary voltage regulating circuit including a series pass element connected to operate continuously in source follower mode and a primary voltage reference element for providing a gate reference for the series pass element, and the secondary voltage regulating circuit being cascaded to the primary voltage regulating circuit in a voltage sharing configuration. A capacitor is provided to maintain an output voltage which is clamped to a pre-determined maximum value.

According to the present invention there is provided a regulated DC power supply circuit comprising a full wave rectification stage for rectifying an AC input voltage and a regulating stage for regulating an output voltage from the rectification stage, the regulating stage having a primary voltage regulating circuit and a secondary voltage regulating circuit, the primary voltage regulating circuit including a series pass element connected in a source follower configuration and a primary voltage reference element for providing a gate reference voltage for the series pass element, and the secondary voltage regulating circuit being cascaded to the primary voltage regulating circuit in a voltage sharing configuration, and is characterised in that the DC power supply circuit is a high voltage circuit in which the regulating stage is capable of regulating an output voltage from the rectification stage in excess of 1kV, the primary voltage regulating circuit having an open loop configuration and the series pass element being arranged to operate in two modes, namely a first saturated on mode, in which the output voltage from the rectification stage is less than the maximum gate reference voltage and the output from the series pass element follows the output voltage from the rectification stage, and a second on mode, in which the output voltage from the rectification stage exceeds the maximum gate reference voltage determined by the primary voltage reference element, and the output from the series pass element is held at approximately the maximum gate reference voltage provided by the primary voltage reference element, the power supply circuit being capable of handling an output voltage which exceeds a maximum voltage rating of the series pass element.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a circuit diagram of a preferred first embodiment of a regulated power supply of the invention;

Figure 2 shows a circuit diagram of a second embodiment of a regulated power supply;

Figure 3 shows a circuit diagram of a third embodiment of a regulated power supply, and

Figure 4 shows a circuit diagram of a fourth embodiment of a regulated power supply.

DESCRIPTION OF EMBODIMENTS

Referring to Figure 1, a regulated power supply circuit 10 has a full wave rectifying stage 12 and a regulating stage 14. The rectifying stage 12 has a three-phase four wire input comprising a neutral line N and three live lines L1, L2 and L3. All the inputs L1, L2, L3 and N are provided with respective limiting resistors R1, R2 R3 and R8, which are in the form of 330 ohm wire wound resistors.

A standard full-wave rectifier, which requires no further explanation, is provided by diodes D1 to D8. Transorb surge protectors Z1,Z2 and Z3, which have a total rating of 1150 volts, are linked together in series and are shunted between the positive and negative rails 16 and 18 after the rectification diodes D1 to D8. The surge protectors are designed to handle a maximum expected line voltage of 760 volts between any two of the input lines. The DC output from the diodes is bypassed by means of a high frequency capacitor C1. The transorbs Z1, Z2 and Z3, together with the RC network provided by the resistors R1, R2, R3 and R8 and the capacitor C1, provide a high level of transient signal rejection. The transorbs provide protection against high voltage surges, and, by resistor current limiting, they are guarded against unlimited absorption of power, which is an important feature in noisy environments.

The rectifying stage 12 of the power supply is able to rectify any combination of at least two active inputs constituted by two or more of L1, L2, L3 and N. Under normal conditions, the input voltage can vary from 50 volts minimun phase voltage to 760 volts maximum line voltage.

The voltage regulating stage 14 is able to handle from a minimum of 45 volts DC up to a maximum of 1026

Petitioner Micron Ex-1004, 0189

volts DC. This stage comprises a primary voltage regulating circuit 20 and a secondary voltage regulating circuit 22 cascaded to the primary voltage regulating circuit in a voltage dividing of sharing configuration. The primary regulating circuit comprises a 1kV MOSFET transistor T1 biased in a zener-regulated source-follower configuration, and connected to operate continuously in source-follower mode. In this configuration, the MOSFET transistor T1 has a gate reference which comprises three 560K 0,6 watt current limiting resistors R4, R5 and R6 in series with a 110 volt zener Z4, which serve as primary voltage reference elements. At maximum input voltage in a three-phase system, total dissipation in the resistors R4, R5 and R6 is below 0,6 watts, which falls within the maximum power rating of each resistor. Three separate voltage sharing resistors R4,R5 and R6 are required to withstand voltage stress.

At relatively low input voltages, from approximately 50 volts rms to 110 volts rms, the zener diode Z4 is off and the limiting resistors R4, R5 and R6 hold the gate of the MOSFET T1 high at the input potential. The MOSFET transistor T1 in thus saturated on. As the input voltage rises up to 110 volts, the zener diode Z4 begins to turn on and to limit the gate potential, and consequently the output of the MOSFET T1 is held at a value just below 110 volts. Any further increase in the input voltage has no effect on the output of the MOSFET T1 as the zener Z4 is limited to 110 volts maximum under all conditions.

As the MOSFET T1 has a maximum voltage rating of 1kV, it is necessary that, in order to cope with a peak voltage of 1074 volts, some of the maximum DC voltage input has to be shared in series with it. The MOSFET source output of 108 volts, which is controlled by the zener Z4, ensures that in worst case conditions, the MOSFET has to handle a peak voltage of no greater than 966 volts. As the gate of the MOSFET T1 hardly draws any current, the zener Z4 can safely be biased right at the edge of its "knee".

The output 16 of the primary regulating circuit 20 is fed to the input of the secondary voltage regulating circuit 22, which has the same basic configuration as the primary circuit. A Darlington transistor pair, which is constituted by transistors T2 and T3, is provided with a gate reference which is current limited by means of a 120K resistor R7. Regulation is achieved by means of a pair of reference zener Z5 and Z6 having respective ratings of 15V and 18V. A 32V shunt trip output 24 is provided at the emitter of the transistor T3.

A further transistor T4 is shunted biased from zener 26 and supplied from the output 16, with its emitter providing a regulated DC output 26 of 18V under all load conditions, as is determined by zener diode Z6. A further zener diode Z7 is linked between the 32V output from the emitter of transistor T3 and the negative rail 18. This zener serves to protect against induction spikes which may arise as a result of an inductive load on the 32V DC shunt trip output 24.

Power dissipation in the primary MOSFET T1 at maximum input voltage is approximately 1,25 watts. As the device is rated at 75 watts, large heat sink capacity is not necessary. However, under minimum air flow conditions, as in an earth leakage unit shell, a large surface area is required for the heat sink to compensate for the high thermal resistance of the enclosure.

Turning now to Figure 2, a further embodiment of a regulated power supply is shown. The voltage rectification stage 12 and the primary regulating circuit 20 is identical to that illustrated in Figure 1. In the secondary regulating circuit 22A, the principle difference is that regulation of the shunt trip and control outputs 24 and 26 are achieved with MOSFET transistors. A MOSFET transistor T5 replaces the Darlington couple T2 and T3, and a MOSFET transistor T6 replaces the bipolar transistor T4.

Referring now to Figure 3, yet a further more basic embodiment of a regulated power supply is shown in which a secondary voltage regulating circuit 22B is in the form of a Darlington configuration similar to that in Figure 1 comprising npn transistors T2 and T3. A regulated 18V control output 26 is provided, together with an unregulated shunt trip output 28 fed directly from the primary regulating circuit. In Figure 4, MOSFET transistor T7 replaces the Darlington configuration T2 and T3 in a secondary regulating circuit 22C.

The regulated linear power supply enjoys a number of advantages. It is able to handle an extremely wide input voltage range and has a relatively low power dissipation. The voltage regulation over the entire input range is extremely low. Furthermore, the circuit is relatively simple, having a low component count.

Claims

1. A regulated DC power supply circuit (10) comprising a full wave rectification stage (12) for rectifying an AC input voltage and a regulating stage (14) for regulating an output voltage from the rectification stage (12), the regulating stage (14) having a primary voltage regulating circuit (20) and a secondary voltage regulating circuit (22, 22A, 22B, 22C), the primary voltage regulating circuit (20) including a series pass element (T1) connected in a source follower configuration and a primary voltage reference element (Z4) for providing a gate reference voltage for the series pass element (T1), and the secondary voltage regulating circuit (22, 22A, 22B, 22C) being cascaded to the primary voltage regulating circuit (20) in a voltage sharing configuration, characterised in that the DC power supply circuit (10) is a high voltage circuit in which the regulating stage (14) is capable of regulating an output voltage from the rectification stage (12) in excess of 1kV, the primary voltage regulating circuit (20) having an open loop configuration and the series pass element (T1)

Petitioner Micron Ex-1004, 0190

being arranged to operate in two modes, namely a first saturated on mode, in which the output voltage from the rectification stage (12) is less than the maximum gate reference voltage and the output from the series pass element (T1) follows the output voltage from the rectification stage, and a second on mode, in which the output voltage from the rectification stage (12) exceeds the maximum gate reference voltage determined by the primary voltage reference element (Z4), and the output from the series pass element (T1) is held at approximately the maximum gate reference voltage provided by the primary voltage reference element, the power supply circuit (10) being capable of handling an output voltage which exceeds a maximum voltage rating of the series pass element (T1).

2. A regulated DC power supply circuit (10) according to claim 1, characterised in that a plurality of current limiting elements (R4, R5, R6) are connected in series with the primary voltage reference element (Z4) for limiting bias current to the gate of the series pass element (T1) and for sharing major portions of the output voltage from the rectification stage (12).

3. A regulated DC power supply circuit (10) according to claim 1 or 2, characterised in that the primary voltage reference element is a zener diode (Z4) having a voltage rating exceeding 100V, and the series pass element is an N-type MOSFET device (T1) having a maximum voltage rating between 950V and 1050V.

4. A regulated DC power supply circuit according to any one of the preceding claims, characterised in that the full wave rectification stage (12) is a three phase rectification stage, which incorporates limiting resistors (R1, R2, R3, R8) and surge protectors (Z1, Z2, Z3), and the power supply circuit is capable of receiving input voltages ranging from 50V phase voltage to 750V line voltage.

Patentansprüche

1. Regelbarer Gleichspannungsquellenschaltkreis (10), mit einer Vollweg-Gleichrichtungsstufe (12) zur Gleichrichtung einer Eingangs-wechselspannung, und mit einer Regelstufe (14) zur Regelung der Ausgangsspannung von der Vollweg-Gleichrichtungsstufe (12), wobei die Regelstufe (14) einen ersten Spannungsregelschaltkreis (20) mit Längspassierelement (T1) in Eingangsfolgeschaltung sowie mit erstem Spannungsreferenzelement (Z4) zur Erzeugung einer Torreferenzspannung für das Längspassierelement C1 und einen zweite Spannungsregelschaltkreis (22, 22A, 22B, 22C) aufweist, und wobei der zweiten Spannungsregelschaltkreis (22, 22A, 22B, 22C) als Stufenschaltkreis im Sinne eines Spannungsteilers an den ersten Spannungsregelschaltkreis (20) angeschlossen ist, **dadurch gekennzeichnet**, daß der Gleichspannungsquellenschaltkreis (10) ein Hochspannungsschaltkreis ist, in welchem die Regelstufe (14) in der Lage ist Ausgangsspannungen von der Vollweg-Gleichrichtungsstufe (12) von mehr als 1kV zu regeln, daß der erste Sgannungsregelschaltkreis (20) als offener Regelkreis ausgebildet ist und das Längspassierelement (T1) so eingerichtet ist, daß es in zwei Betriebsarten arbeitet, nämlich einer ersten gesättigten Einschaltbetriebsart, bei welcher die Ausgangsspannung von der Vollweg-Gleichrichtungsstufe (12) kleiner als die maximale Torreferenzspannung ist und die Ausgangsspannung des Längspassierelementes (T1) der Ausgangsspannung der Vollweg-Gleichrichtungsstufe (12) folgt, und einer zweiten Einschaltbetriebsart, bei welcher die Ausgangsspannung von der Vollweg-Gleichrichtungsstufe (12) die durch das erste Spannungsreferenzelement (Z4) vorgegebene maximale Torreferenzspannung überschreitet, wobei der Ausgang des Längspassierelementes (T1) in etwa auf maximaler Torspannung - vorgegeben durch das erste Spannungsreferenzelement (Z4) gehalten wird, so daß der Gleichspannungsquellenschaltkreis (10) in der Lage ist, eine Ausgangsspannung zu verarbeiten, die die Grenzspannung des Längspassierelementes (T1) überschreitet.

2. Regelbarer Gleichspannungsquellenschaltkreis (10) nach Anspruch 1, dadurch gekennzeichnet, daß eine Vielzahl von Strombegrenzungsmitteln (R4, R5, R6) in Serie mit dem ersten Spannungsreferenzelement (Z4) geschaltet sind, um den unter Vorspannung fließenden Torstrom des Längspassierelementes (T1) zu begrenzen und um einen Großteil der Ausgangsspannung der Vollweg-Gleichrichtungsstufe (12) herunterzuteilen.

3. Regelbarer Gleichspannungsquellenschaltkreis (10) nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß das erste Spannungsreferenzelement eine Zenerdiode (Z4) mit einer Grenzspannung von mehr als 100 Volt ist, und daß das Längspassierelement (T1) ein N-Typ-MOSFET-Element (T1) mit einer maximalen Grenzspannung zwischen 950 Volt und 1050 Volt ist.

4. Regelbarer Gleichspannungsquellenschaltkreis (10) nach einem der vorherigen Ansprüche, dadurch gekennzeichnet, daß die Vollweg-Gleichrichtungsstufe (12) eine 3-Phasen-Gleichrichtungsstufe ist, welche Strombegrenzungswiderstände (R1, R2, R3, R8) und Spannungsstoßschutzelemente (Z1, Z2, Z3) beinhaltet, und daß der Gleichspan-

Petitioner Micron Ex-1004, 0191

nungsquellenschaltkreis (10) in der Lage ist, Eingangsspannungen zwischen 50 Volt Phasenspannung bis 750 Volt Leitungsspannung zu verarbeiten.

Revendications

1. Circuit d'alimentation régulé (10) en courant continu, comprenant un étage redresseur à deux alternances (12) destiné à redresser une tension alternative d'entrée et un étage de régulation (14) destiné à réguler une tension de sortie provenant de l'étage redresseur (12), l'étage de régulation (14) ayant un circuit (20) de régulation de tension primaire et un circuit (22, 22A, 22B, 22C) de régulation de tension secondaire, le circuit (20) de régulation de tension primaire comprenant un élément (T1) de passage en série connecté avec une configuration à charge de source et un élément (Z4) de référence de tension primaire destiné à donner une tension de référence de grille pour l'élément (T1) de passage en série, et le circuit (22, 22A, 22B, 22C) de régulation de tension secondaire étant monté en cascade avec le circuit (20) de régulation de tension primaire avec une configuration de partage de tension, caractérisé en ce que le circuit d'alimentation en courant continu (10) est un circuit à haute tension dans lequel l'étage de régulation (14) peut réguler une tension de sortie de l'étage redresseur (12) au-delà de 1 kV, le circuit (20) de régulation de tension primaire ayant une configuration en boucle ouverte et l'élément de passage en série (T1) étant destiné à fonctionner suivant deux modes, c'est-à-dire un premier mode de conduction à saturation dans lequel la tension de sortie de l'étage redresseur (12) est inférieure à la tension maximale de référence de grille et le signal de sortie de l'élément de passage en série (T1) suit la tension de sortie de l'étage redresseur, et un second mode de conduction dans lequel la tension de sortie de l'étage redresseur (12) dépasse la tension maximale de référence de grille déterminée par l'élément (Z4) de référence de tension primaire, et le signal de sortie de l'élément de passage en série (T1) est maintenu approximativement à la tension maximale de référence de grille donnée par l'élément de référence de tension primaire, le circuit d'alimentation (10) permettant le traitement d'une tension de sortie qui dépasse une tension maximale nominale de l'élément de passage en série (T1).

2. Circuit d'alimentation régulé (10) en courant continu selon la revendication 1, caractérisé en ce que plusieurs éléments limiteurs de courant (R4, R5, R6) sont connectés en série avec l'élément de référence de tension primaire (Z4) pour la limitation du courant de polarisation de la grille de l'élément de passage en série (T1) et pour le partage des parties principales de la tension de sortie de l'étage redresseur (12).

3. Circuit d'alimentation régulé (10) en courant continu selon la revendication 1 ou 2, caractérisé en ce que l'élément de référence de tension primaire est une diode de Zener (Z4) ayant une tension nominale dépassant 100 V, et l'élément de passage en série est un dispositif à transistor MOSFET de type N (T1) ayant une tension maximale nominale comprise entre 950 et 1 050 V.

4. Circuit d'alimentation régulé en courant continu selon l'une quelconque des revendications précédentes, caractérisé en ce que l'étage redresseur à deux alternances (12) est un étage redresseur triphasé qui comprend des résistances de limitation (R1, R2, R3, R8) et des organes de protection contre les surtensions (Z1, Z2, Z3), et le circuit d'alimentation peut recevoir des tensions d'entrée comprises entre une tension de phase de 50 V et une tension de ligne de 750 V.

Petitioner Micron Ex-1004, 0192

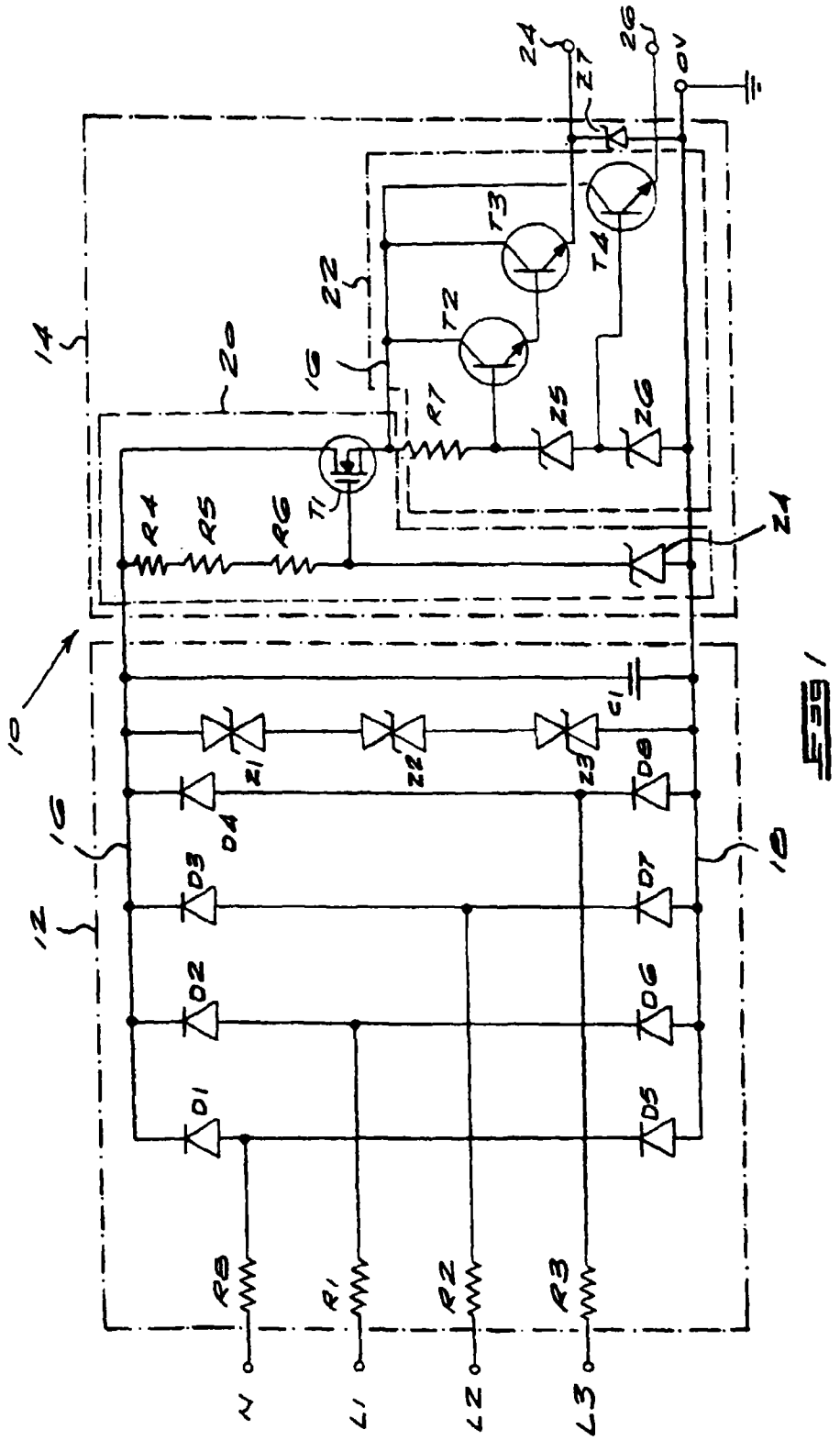


FIG 1

Petitioner Micron Ex-1004, 0193

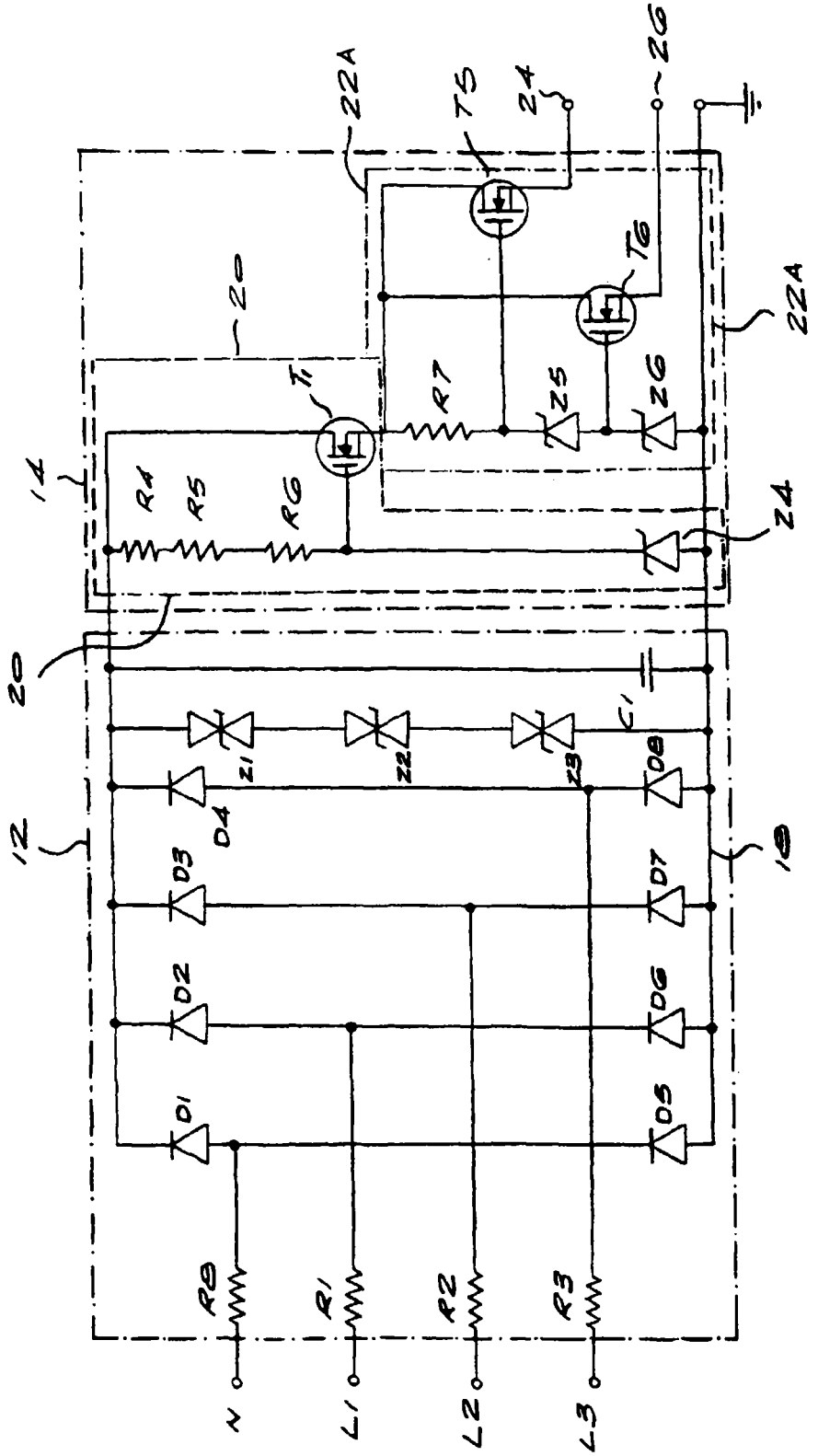


FIG 2

Petitioner Micron Ex-1004, 0194

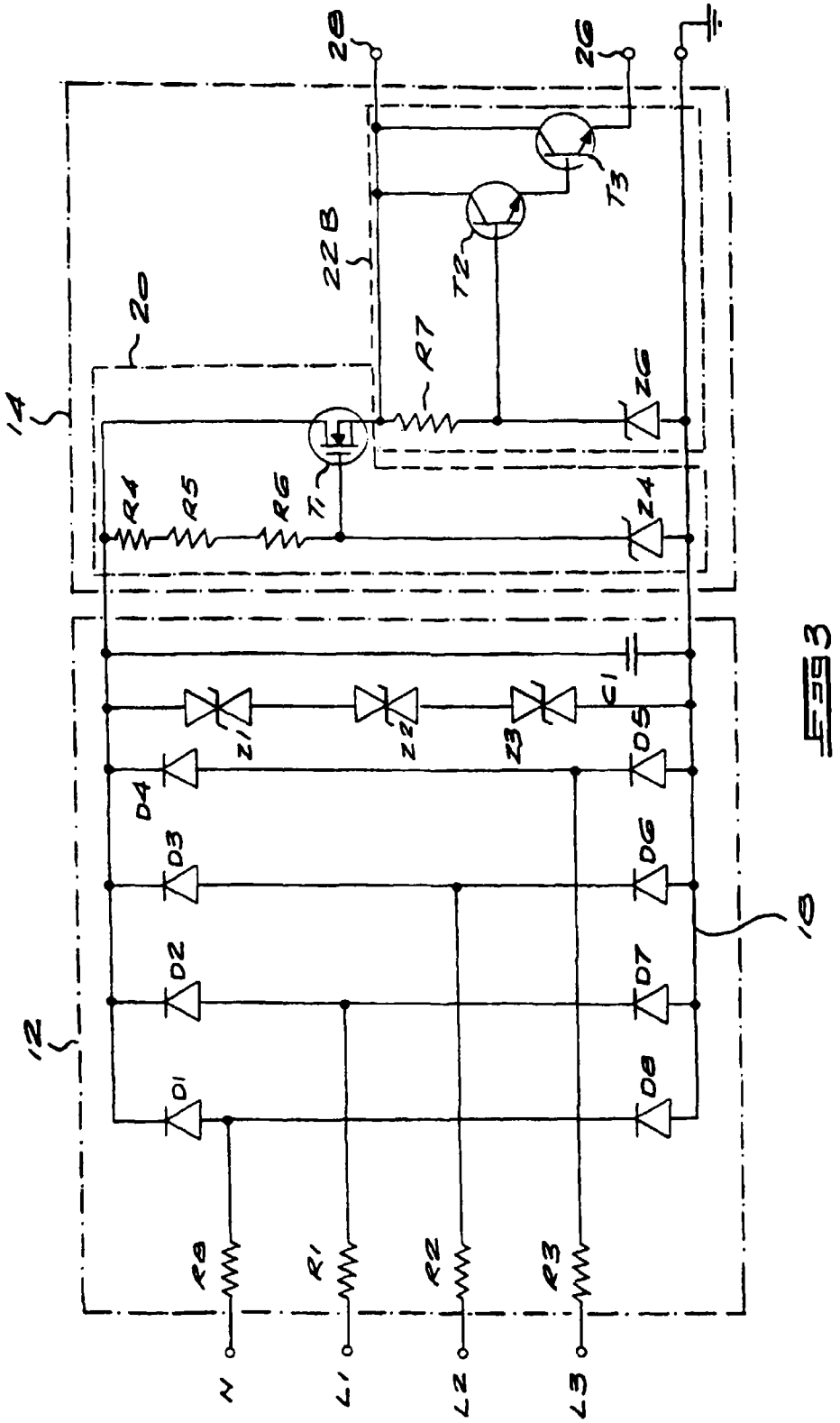


FIG 3

Petitioner Micron Ex-1004, 0195

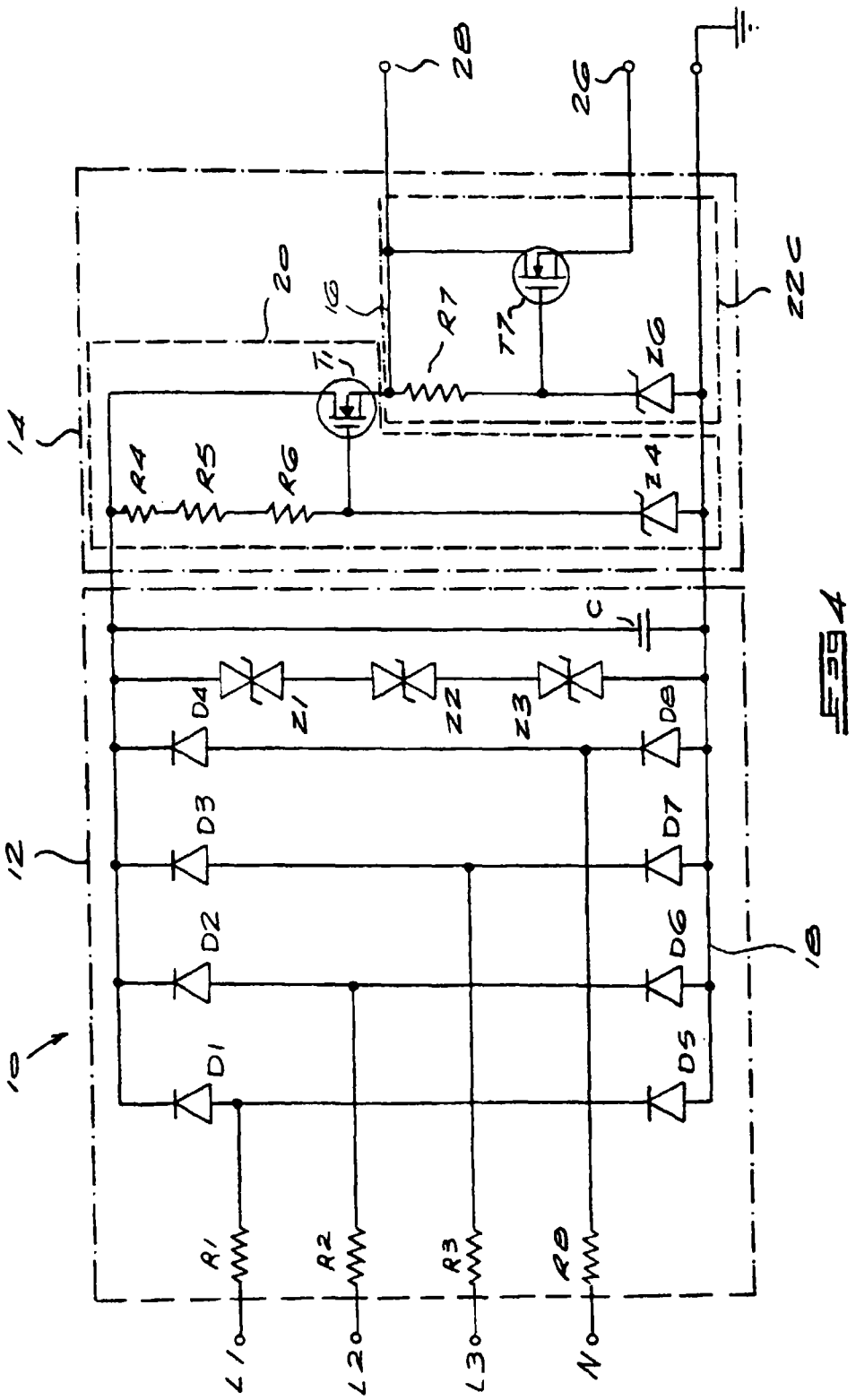


Fig 4

Petitioner Micron Ex-1004, 0196

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) which is claimed and for which a patent is sought by way of the application entitled

TRANSIENT LOAD VOLTAGE REGULATOR

which (check)	☒	is attached hereto.
	☐	and is amended by the Preliminary Amendment attached hereto.
	☐	was filed on _____, 2009 as Application Serial No. _____
	☐	and was amended on (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
Number	Country	Day/Month/Year Filed	Yes	No
N/A			☐	☐

Petitioner Micron Ex-1004, 0197

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

Provisional Application Number	Filing Date
N/A	

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56, which became available between the filing date of the prior application(s) and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status (patented, pending, abandoned)
N/A		

I declare that all statements made herein of my own knowledge are true, all statements made herein on information and belief are believed to be true, and all statements made herein are made with the knowledge that whoever, in any matter within the jurisdiction of the Patent and Trademark Office, knowingly and willfully falsifies, conceals, or covers up by any trick, scheme, or device a material fact, or makes any false, fictitious or fraudulent statements or representations, or makes or uses any false writing or document knowing the same to contain any false, fictitious or fraudulent statement or entry, shall be subject to the penalties including fine or imprisonment or both as set forth under 18 U.S.C. 1001, and that violations of this paragraph may jeopardize the validity of the application or this document, or the validity or enforceability of any patent, trademark registration, or certificate resulting therefrom.

Tomer Shaul Elran
Full name of sole or joint inventor (given name, family name)

Sole or Joint Inventor's signature

10/5/09
Date

Petah Tikva, Israel
Residence (City and either State or Foreign Country)

Israeli
Citizenship

Asire Tzion 5, Petah Tikva, Israel
Mailing Address

Petitioner Micron Ex-1004, 0198

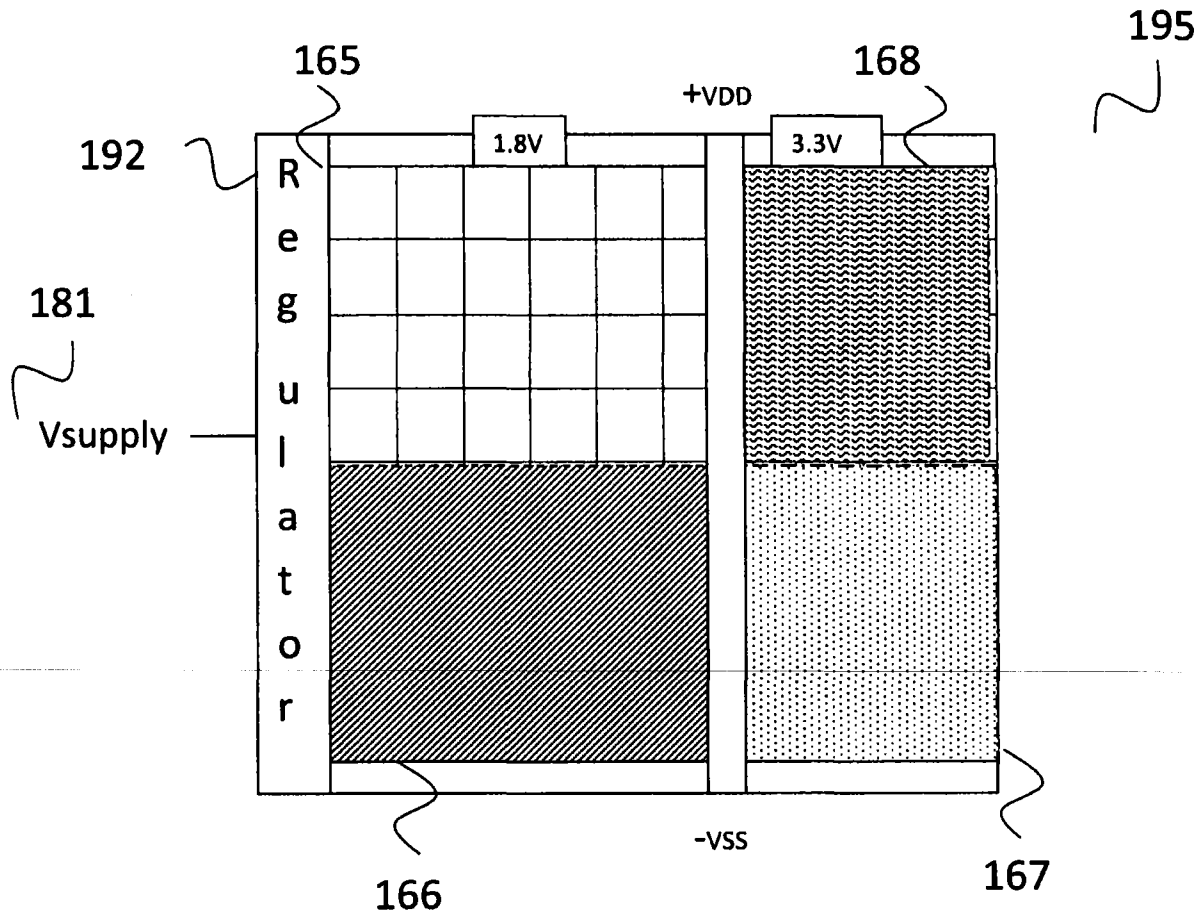


FIG. 1

Prior Art

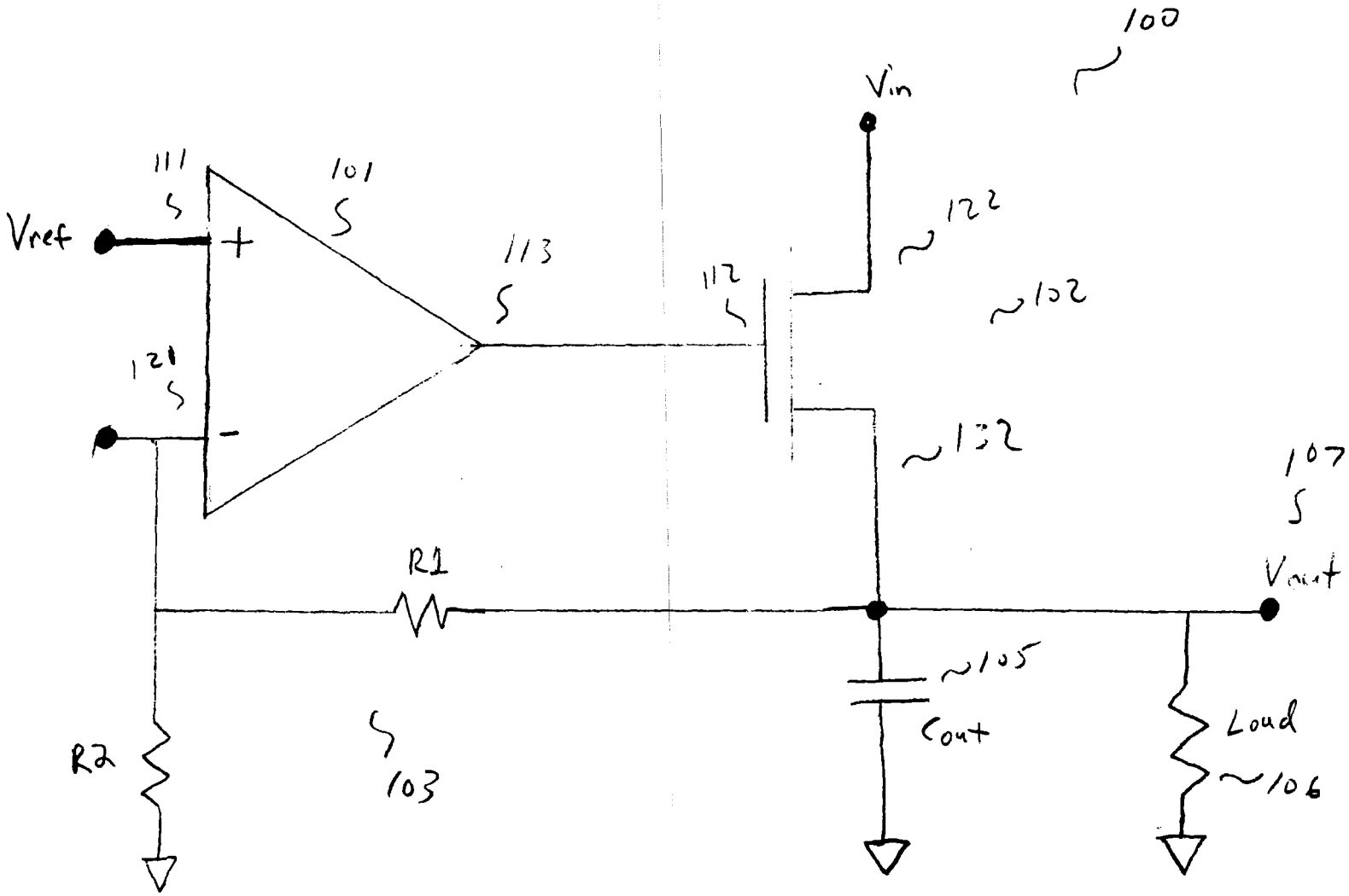


Fig. 2

Prior Art

Petitioner Micron Ex-1004, 0200

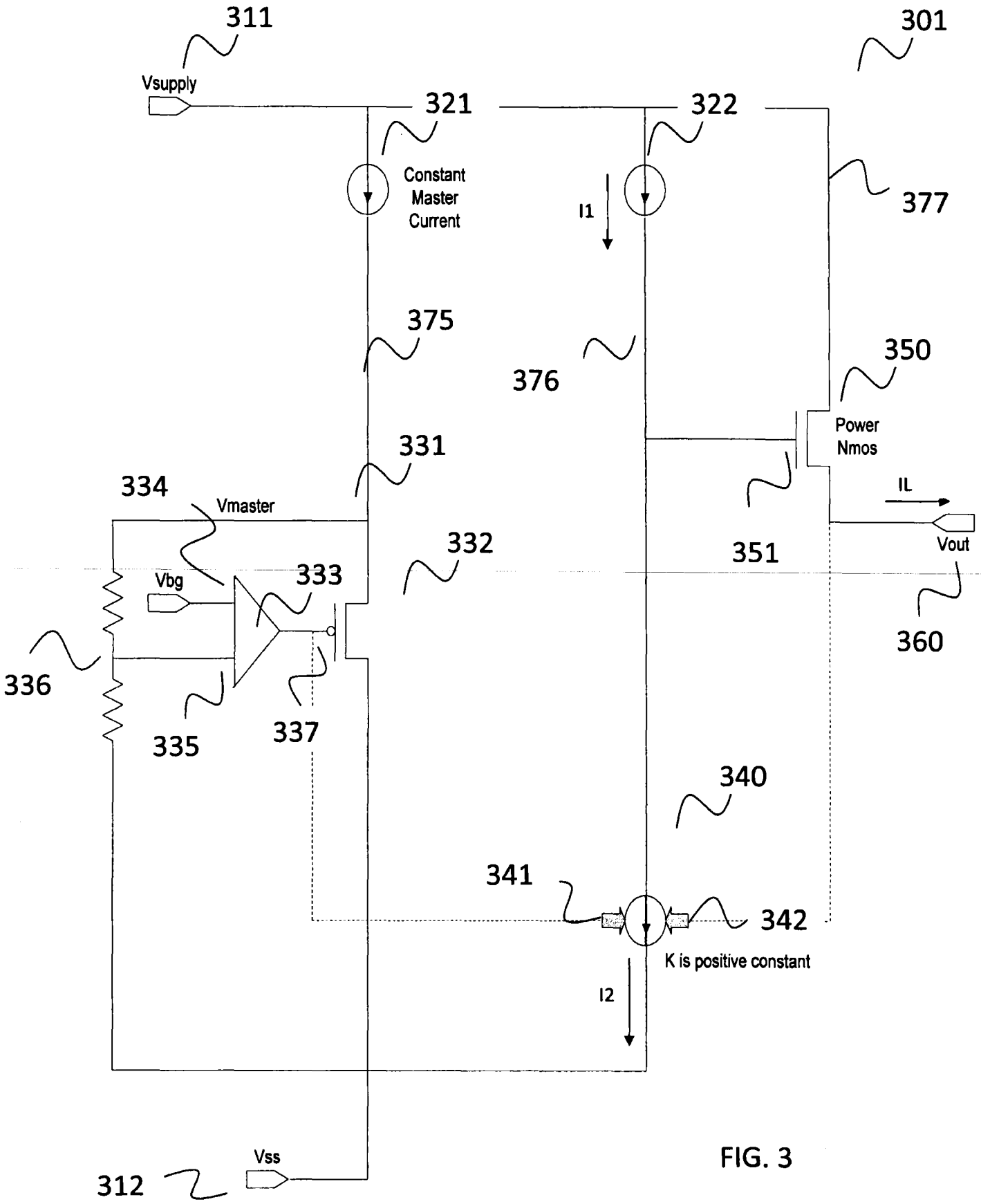

311
Vsupply
301
321
322
Constant
Master
Current
I1
377
375
376
350
Power
Nmos
331
334
Vmaster
IL
332
351
Vout
Vbg
333
360
336
335
337
340
341
342
K is positive constant
I2
312
Vss

FIG. 3

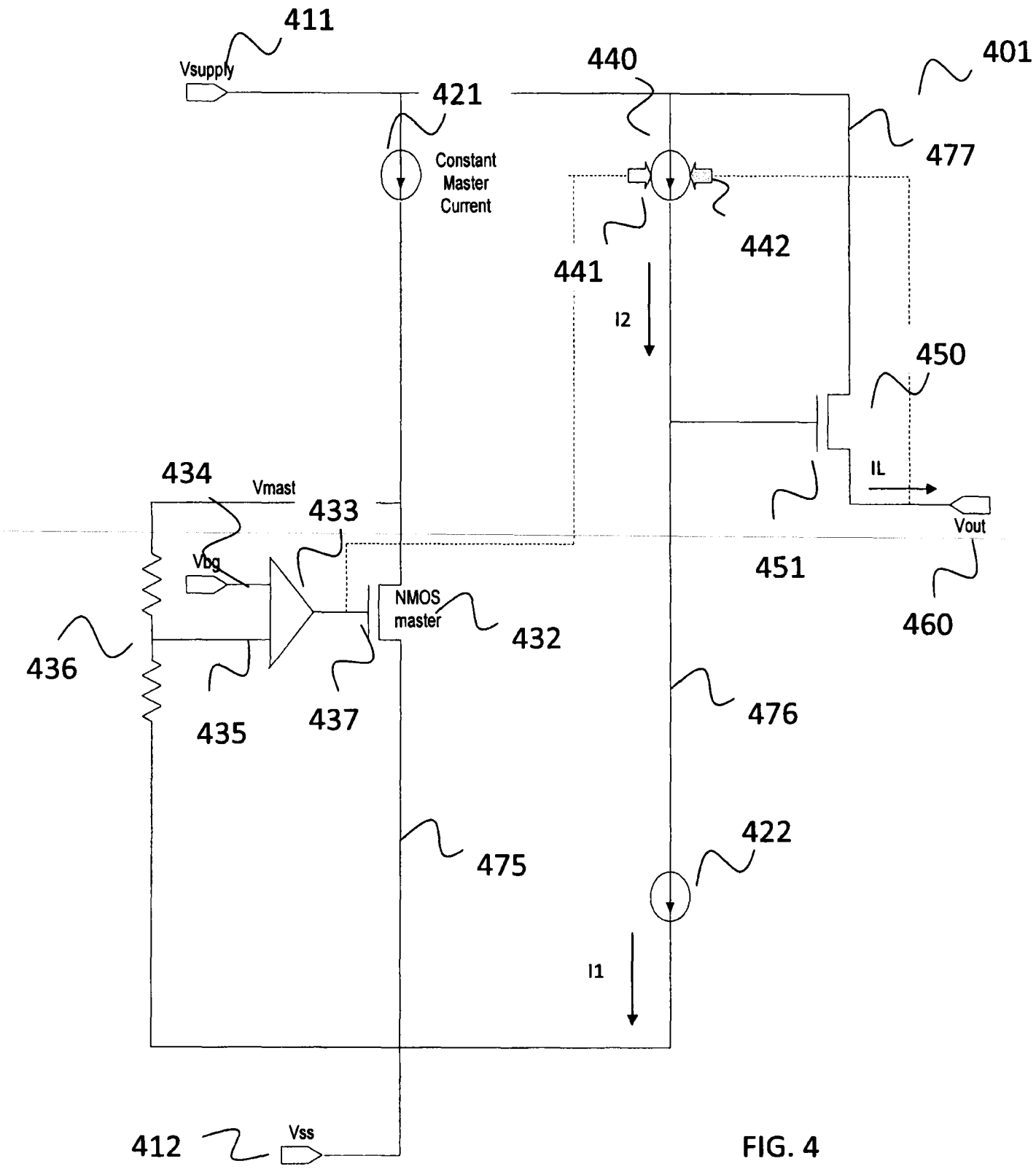

411
Vsupply
421
Constant
Master
Current
440
401
477
442
441
I2
450
IL
Vout
460
451
434
Vmast
433
Vbg
NMOS
master
432
436
435
437
476
475
422
I1
412
Vss

FIG. 4

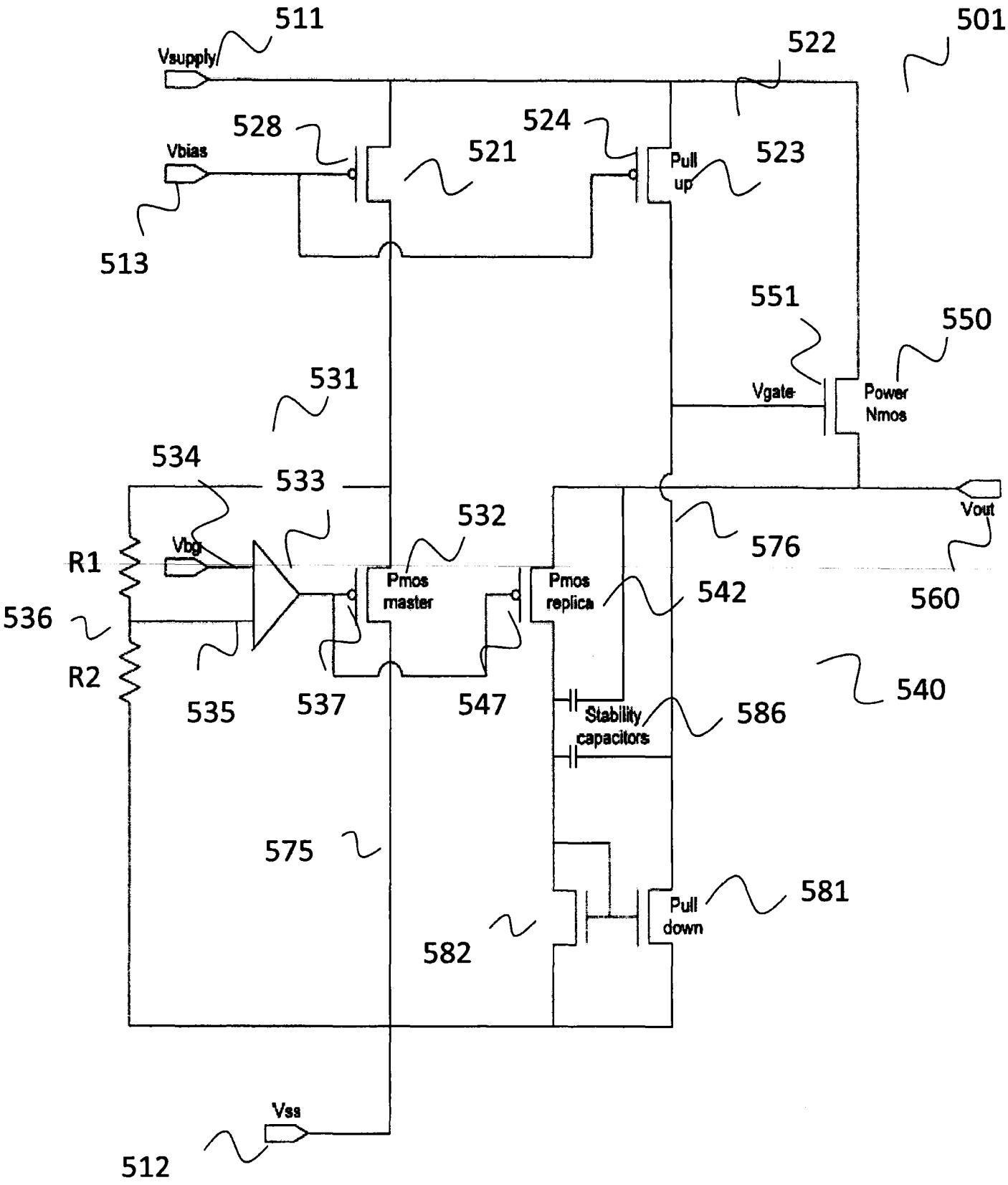

511
Vsupply
501
522
528
524
Vbias
521
Pull up
523
513
551
550
531
Vgate
Power Nmos
534
533
532
Vout
576
Vbg
R1
Pmos master
Pmos replica
542
560
536
R2
540
535
537
547
Stability capacitors
586
575
581
Pull down
582
Vss
512

FIG. 5

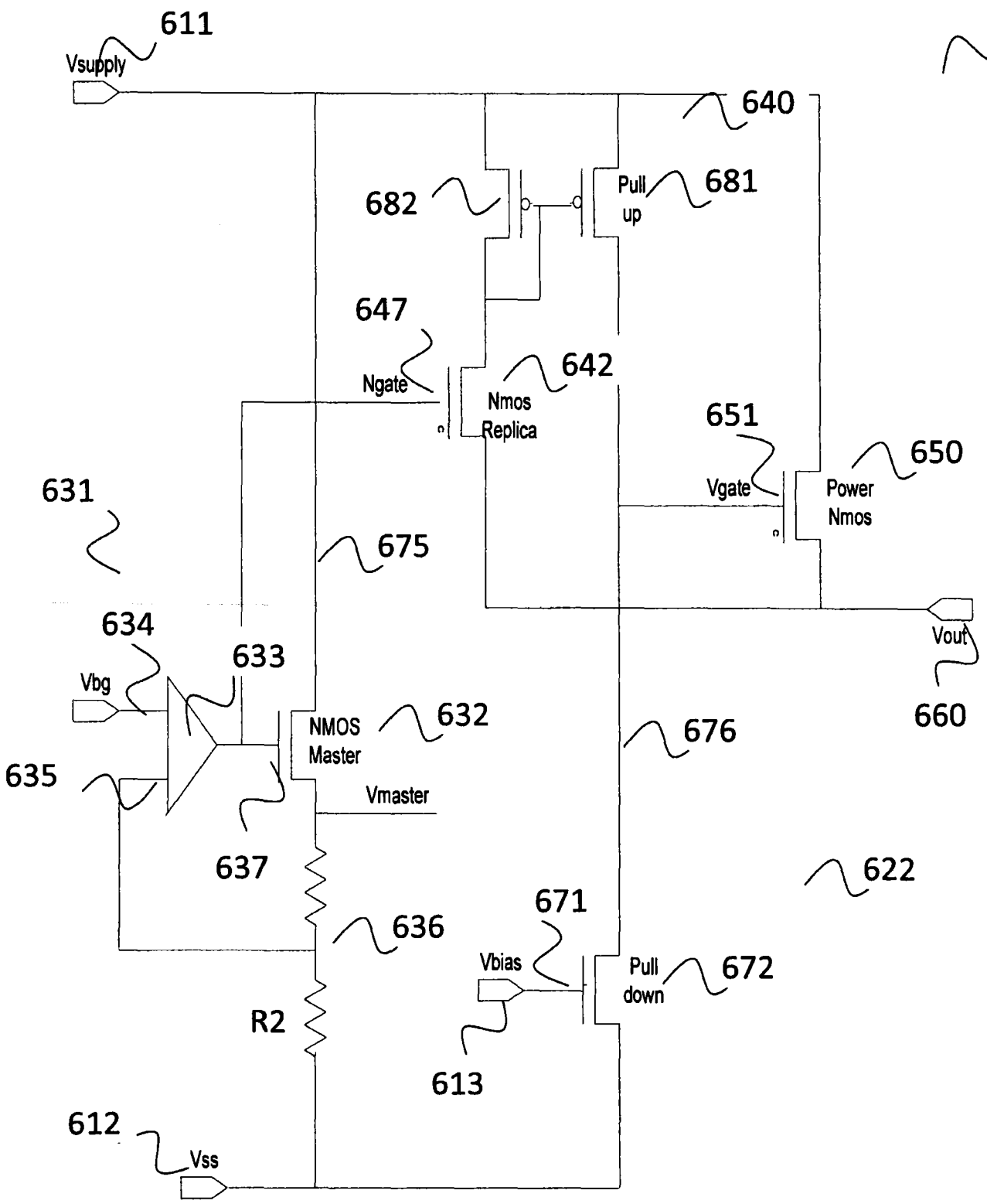

611
Vsupply
601
640
682
Pull
up
681
647
Ngate
642
Nmos
Replica
651
650
Vgate
Power
Nmos
631
675
634
633
Vbg
Vout
660
NMOS
Master
632
676
635
Vmaster
637
622
671
636
Vbias
Pull
down
672
R2
613
612
Vss

Fig. 6

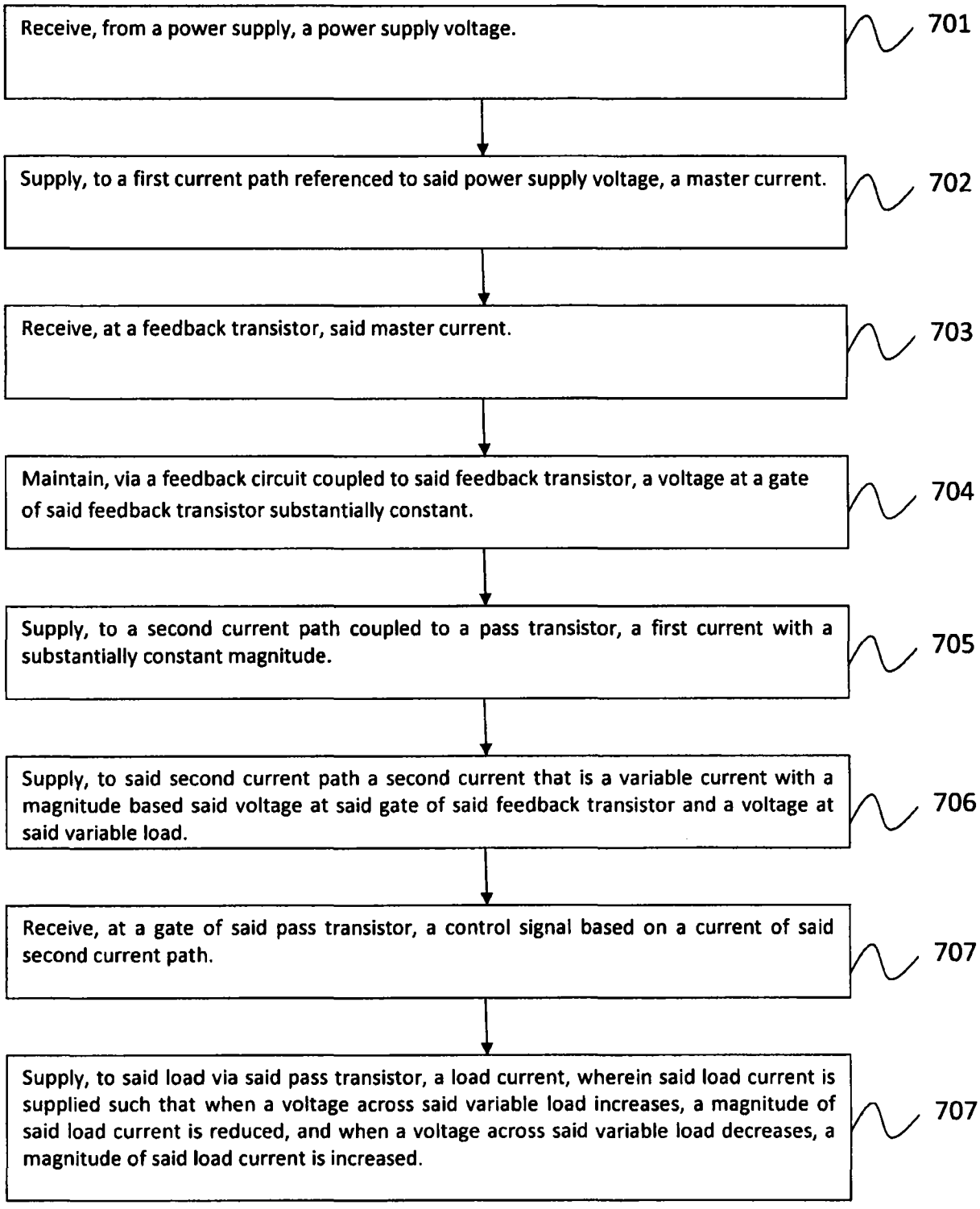

Receive, from a power supply, a power supply voltage.
701
Supply, to a first current path referenced to said power supply voltage, a master current.
702
Receive, at a feedback transistor, said master current.
703
Maintain, via a feedback circuit coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant.
704
Supply, to a second current path coupled to a pass transistor, a first current with a substantially constant magnitude.
705
Supply, to said second current path a second current that is a variable current with a magnitude based said voltage at said gate of said feedback transistor and a voltage at said variable load.
706
Receive, at a gate of said pass transistor, a control signal based on a current of said second current path.
707
Supply, to said load via said pass transistor, a load current, wherein said load current is supplied such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.
707

Fig. 7

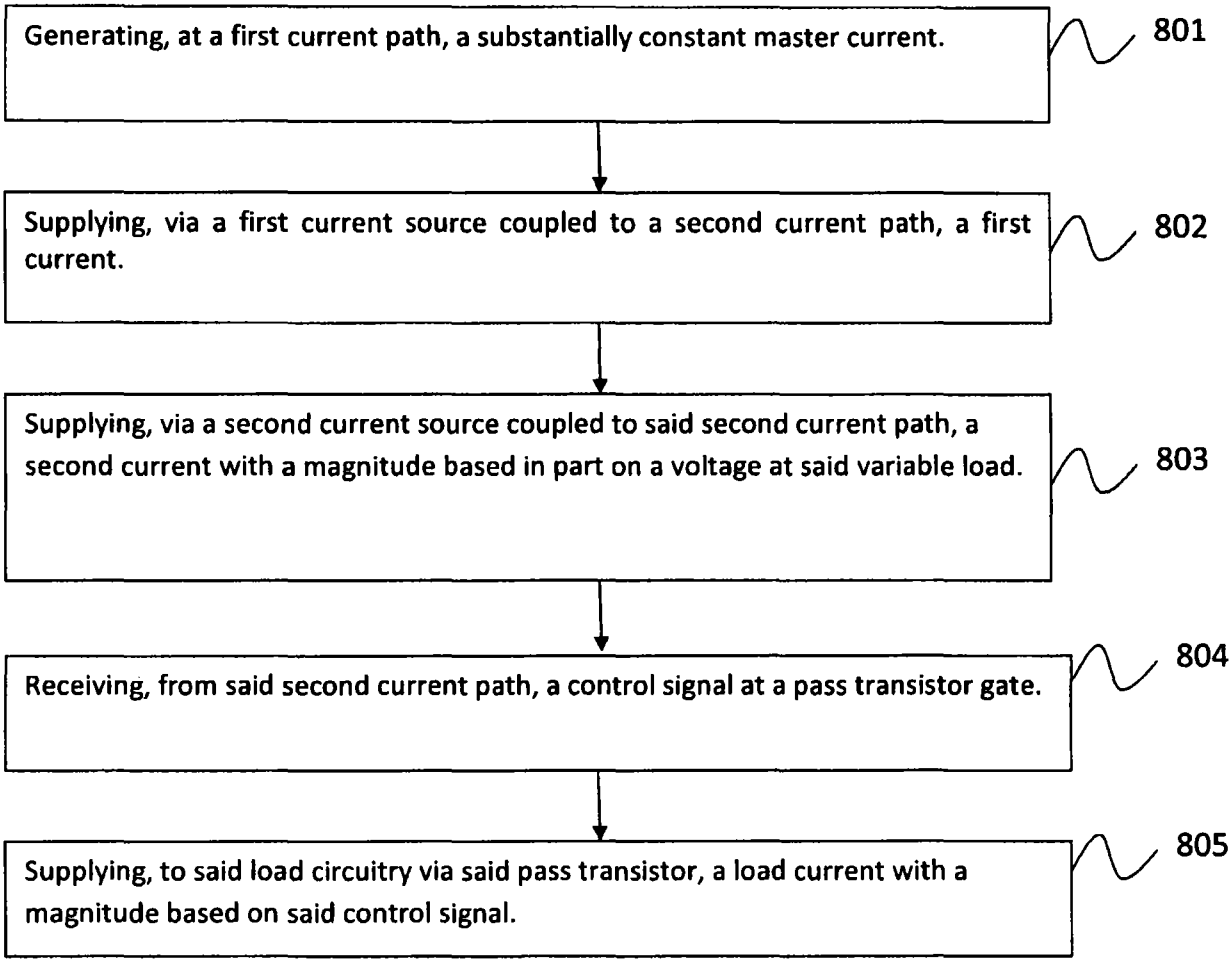

Generating, at a first current path, a substantially constant master current.
801
Supplying, via a first current source coupled to a second current path, a first current.
802
Supplying, via a second current source coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load.
803
Receiving, from said second current path, a control signal at a pass transistor gate.
804
Supplying, to said load circuitry via said pass transistor, a load current with a magnitude based on said control signal.
805

Fig. 8

PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :		(11) International Publication Number:
H03F 3/45	A1	WO 93/05572
		(43) International Publication Date: 18 March 1993 (18.03.93)

(21) International Application Number: PCT/CA92/00381

(22) International Filing Date: 3 September 1992 (03.09.92)

(30) Priority data:
2,050,878 6 September 1991 (06.09.91) CA

(71) Applicant *(for all designated States except US)*: MITEL CORPORATION [CA/CA]; 350 Legget Drive, P.O. Box 13089, Kanata, Ontario K2K 1X3 (CA).

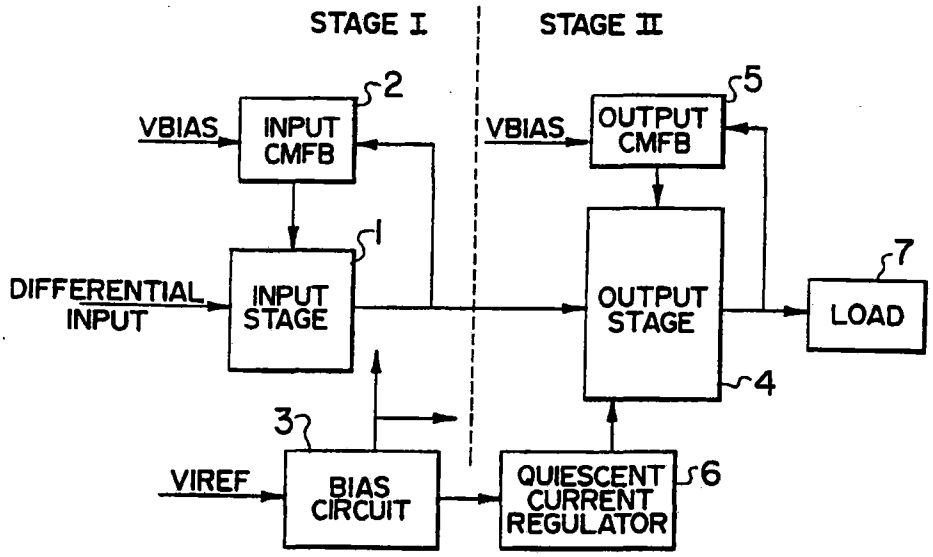
(72) Inventor; and
(75) Inventor/Applicant *(for US only)* : MOLNAR, Gerald [CA/CA]; 2343 Ryan Drive, Ottawa, Ontario K2C 1K8 (CA).

(74) Agent: MITCHELL, Richard, J.; Marks & Clerk, 55 Metcalfe Street, Suite 1380, P.O. Box 957, Station B, Ottawa, Ontario K1P 5S7 (CA).

(81) Designated States: DE, GB, JP, KR, NL, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, SE).

Published
With international search report.

(54) Title: POWER AMPLIFIER WITH QUIESCENT CURRENT CONTROL



(57) Abstract

A power amplifier comprises an input stage having a fully differential amplifier with differential inputs and differential outputs, and a high impedance closed loop common mode feedback control circuit deriving common mode feedback control signals from the differential outputs. The output stage of each differential output of the input stage comprises a class AB amplifier having source followers interfacing with the fully differential amplifier. A common mode output voltage control circuit maintains the common mode output voltage of the class AB amplifiers at a desired level. A quiescent current regulator comprises a circuit for mimicking the behaviour of one of the source followers to derive a control signal for maintaining the quiescent current of the output transistors at a desired value.

Petitioner Micron Ex-1004, 0207

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	FI	Finland	MN	Mongolia
AU	Australia	FR	France	MR	Mauritania
BB	Barbados	GA	Gabon	MW	Malawi
BE	Belgium	GB	United Kingdom	NL	Netherlands
BF	Burkina Faso	GN	Guinea	NO	Norway
BG	Bulgaria	GR	Greece	NZ	New Zealand
BJ	Benin	HU	Hungary	PL	Poland
BR	Brazil	IE	Ireland	PT	Portugal
CA	Canada	IT	Italy	RO	Romania
CF	Central African Republic	JP	Japan	RU	Russian Federation
CG	Congo	KP	Democratic People's Republic of Korea	SD	Sudan
CH	Switzerland			SE	Sweden
CI	Côte d'Ivoire	KR	Republic of Korea	SK	Slovak Republic
CM	Cameroon	LI	Liechtenstein	SN	Senegal
CS	Czechoslovakia	LK	Sri Lanka	SU	Soviet Union
CZ	Czech Republic	LU	Luxembourg	TD	Chad
DE	Germany	MC	Monaco	TG	Togo
DK	Denmark	MG	Madagascar	UA	Ukraine
ES	Spain	ML	Mali	US	United States of America

POWER AMPLIFIER WITH QUIESCENT CURRENT CONTROL

This invention relates to a power amplifier with a differential output and differential input, for example, suitable for use as a driver circuit for moving coil transducers, such as earpieces and speakers employed in telephone sets.

Modern telephone circuitry may be implemented in CMOS integrated circuits. Suitable drivers must be provided to interface with discrete moving coil transducer components, such as the earpieces and speakers employed in modern telephone sets. Generally, the drivers must be capable of supplying high power to the load at low D.C. bias voltages, and for this purpose fully differential amplifiers, which have a differential output and differential input, can be employed to advantage because of their ability to produce a high output power from the 5V CMOS voltage supply (No special power supply is required). The drivers must, however, have linear transfer characteristics, a very high input impedance in order to interface with the CMOS circuitry, a stable frequency response and be insensitive to process variations.

Two major problems must be addressed, namely the control of the common mode voltage associated with fully differential designs and the D.C. quiescent current associated CMOS amplifiers with large output transistors. The high load currents and large dimensions of the output transistors in the amplifier imply a high sensitivity of quiescent current to process variations and biasing. Small deviations in the gate voltages of the output transistors can lead to quiescent currents that greatly exceed desired

Petitioner Micron Ex-1004, 0209

requirements.

The driver should also have high gain, inherent stability and simplicity of implementation. These features have proved difficult in the past to achieve.

According to the present invention there is provided a power amplifier comprising an input stage having a fully differential amplifier with differential inputs and differential outputs, and a high input impedance closed loop common mode feedback control circuit deriving common mode feedback control signals from said differential outputs; and an output stage comprising for each differential output of the input stage a class AB amplifier having source followers interfacing with said fully differential amplifier and a quiescent current control input for maintaining a desired quiescent current, means for maintaining the common mode output voltage of the class AB amplifiers at a desired level, and a quiescent current regulator for supplying a control signal to said quiescent current control inputs, said quiescent current regulator comprising means for mimicking the behaviour of one of said source followers to derive said control signal.

The quiescent current regulator preferably includes a pair of transistors that mimic the N-channel source follower of one of the class AB amplifiers. The gate of one of the mimic transistors is set to the quiescent state voltage of the input stage output. The drain voltage of the second mimic transistor corresponds to the drain voltage of one of a pair of transistors forming the N-channel follower connected to the gate of the N-channel driver transistor in the output stage and thus represents its gate voltage. The

Petitioner Micron Ex-1004, 0210

gate voltage of the second mimic transistor is used to bias the N-channel source follower of the output stage. A reference voltage generated at the input of the quiescent current regulator is effectively mirrored into the N-channel driver transistor of the output stage and can thus be used to determine the quiescent current of the output stage. This circuit results in an amplifier quiescent current that is insensitive to process variations.

The present invention is of two-stage design, in which the input stage is a preferably a folded cascode amplifier, which is characterized by high open loop gain and inherent stability.

In view of the poor output drive capability of the folded cascode amplifier, the common mode voltage control feedback circuit is required to have a very high input impedance (very much greater than 1 Megohm) to the folded cascode amplifier output to prevent the common mode feedback circuit from loading down the first stage and thus reducing its gain. The common mode feedback circuit should also operate in the linear fashion over a wide range of input voltage. Conventional designs are very difficult to realize in, for example, a two micron fabrication process. Thus, the common mode feedback control circuit preferably has a pair of transistors operating in the triode region as a pair of voltage dependent resistors connected to the differential outputs of the folded cascode. Summed current through these transistors is matched a control current used to determine the control signal to the folded cascode common mode control input.

The invention will now be described in more detail, by way of example only, with reference to the

Petitioner Micron Ex-1004, 0211

accompanying drawings, in which:-

Figure 1 is a block diagram of a power amplifier in accordance with the invention;

Figure 2 is a circuit diagram of a bias circuit for the amplifier;

Figure 3 shows the input stage of the circuit, represented by Stage I in Figure 1;

Figure 4 shows the common mode feedback control circuit;

Figure 5 shows a loop response of the common mode control circuit;

Figure 6 shows the first stage with common mode control compensation element;

Figure 7 is a circuit diagram of an output stage speaker driver;

Figure 8 is circuit diagram of a common mode feedback control circuit for the output stage; and

Figure 9 is a circuit diagram of the quiescent current regulator.

Referring now to Figure 1, the driver is broadly divided into two stages, Stage I and Stage II. Stage I includes an input stage 1 receiving a differential input, a common mode feedback control circuit 2, and a circuit 3 for generating bias voltages. The second stage, Stage II comprises an output stage 4, an output common mode feedback control circuit 5, a quiescent

Petitioner Micron Ex-1004, 0212

current regulator 6, and a load 7, which may be a speaker or earpiece. The entire circuit, except of course the load, is implemented in two micron CMOS technology.

The bias circuit is shown in more detail in Figure 2. Its main purpose is to provide various reference voltages, Vb0, Vb1, Vb2, Vb3 that track changes due to process variations and external factors (temperature, voltage, etc.) and ensure that the circuits using the bias voltages can be made invariant to these influences.

The bias circuit 3, shown in more detail in Figure 2, includes field effect transistors 8, 9, and 10. A voltage reference V_{iref} is applied to the circuit and calibrated such that transistor 8 serves as a 20µa current source. This reference current is mirrored throughout the transistor chains of the bias network to create the precise reference voltages referred to above. Since each reference voltage Vb0, Vb1, Vb2, Vb3 is related to the 20µa current source, precision current sources can be realized within the amplifier design. Transistors 9 and 10 are made smaller than the transistors in the associated bias chains to ensure that these latter transistors operate in their respective saturation regions.

The input Pd is a power down input signal, which ensures that all currents in the bias chains are reduced to zero on power down. Subsequently, all other current sources within the driver circuit that utilize Vb0 to Vb3 are shut down.

Referring now to Figure 3, the input stage I provides most of the open loop gain for the amplifier

Petitioner Micron Ex-1004, 0213

circuit. The input stage I plays a major role in influencing PSRR, CMRR, noise and other amplifier characteristics. The input stage is therefore implemented as a fully differential folded cascode amplifier with a differential input and differential output. This approach affords high gain (greater than 60db), inherent stability, and simplicity of implementation.

The differential input has input transistors 11, 12 with respective series transistors 13, 14, having their gates connected together and providing a control input for the stage I output common mode voltage feedback control signal. The outputs of the transistors 11, 12 are connected to transistor chains 15, 16 to which are applied the bias voltage Vb1, Vb2 and Vb3. The outputs of the transistor chains 15, 16 provide the fully differential outputs of the folded cascode amplifier.

The folded cascode implementation has the advantage of providing high gain (greater than 60 dB), inherent stability (folded cascode designs are compensated by the load capacitance), and simplicity of implementation (a small number of transistors).

Transistor 17 provides a 100µa current source for the differential input path 11, 12. Transistors 11, 12 are misfits, which have a channel length of 3µm to promote better matching, i.e minimize output differential offset. The channel width (g_m) associated with these devices (300µm) has a major impact on the overall gain of the first stage. The sizes of transistors 13, 14, and 18, 19 and bias chains 15, 16, are all directly related to the size of the transistors in the reference current (20µa) of the bias chain.

Petitioner Micron Ex-1004, 0214

The differential output signals of the first stage are biased at a DC common mode voltage equal to Vdd/2 (Vbias). The common mode output voltage is controlled by varying the gate voltage of transistors 13, 14.

Figure 4 shows the common mode feedback control circuit, which is implemented in a novel manner. The circuit provides common mode output voltage control of a 5V folded cascode operational amplifier, very high input impedance of the folded cascode output, and is capable of linear operation during high voltage swings.

The common mode feedback control circuit comprises a pair of transistors 20, 21 connected to the fully differential output of the input stage 1. Transistors 20, 21 are connected in a first path 22 with series transistors 23, 24. Current I_1 flows through this path into transistors 20, 21. This path is in parallel with the second path consisting of a series of resistors 25, 26 and the parallel combination of transistors 27, 28 receiving at their gate, bias voltage V_{bias}.

Transistors 27, 28 function as current sources with current I_0 being a function of the reference voltage Vbias. The gate voltage transistor 25 must be such that the drain current is equal to I_0. Once transistors 24 and 25 are matched and the gate voltage is common, I_0 must be equal to I_1 and hence the drain currents of transistors 20, 21 must sum to I_0. This is only be true if the common mode voltage at the output of the folded cascode is equal to V_{bias}.

The transistors 20, 21 thus act as voltage dependent transistors. In order to ensure linearity over wide swings of gate voltage, they are operated in the triode region, and this is accomplished by forcing

Petitioner Micron Ex-1004, 0215

the drains of transistors 27, 28, 20, 21 to a low voltage with transistors 23, 26. The absolute value of I_0 is determined by the size of transistors 27, 28 and the value of the voltage V_{bias}. These transistors have a high impedance (W=15μm, L=40μm) in order to keep the circuit current low.

Since the common mode control is a closed loop system, stability is important. To quantify the gain and phase response, the closed loop must be opened and the appropriate measurements taken (see Figure 5). Compensation elements can then be added to compensate for the frequency response. Figure 6 shows the input stage 1 and common mode feedback control circuit 2 with compensation elements 29.

Figure 7 shows an output stage for the amplifier. Two such output stages are provided, one for each differential output of the input Stage I. The main purpose of the circuit shown in Figure 7 is to buffer, i.e. provide current gain, for the outputs of the folded cascode input stage I.

The circuit shown in figure 7 comprises two output transistors, 30, 31 driven in a class AB manner. The size of transistors 30, 31 is determined by the output current (i.e. minimum load resistance or maximum load gm) that the amplifier must drive. N-channel and P-channel source followers, defined by transistors 32, 33 and 34, 35 respectively are provided. In the quiescent state, which is defined at V_0 equal to V_{bias} (nominally Vdd/2), the gate voltage of transistor 31 is barely over the threshold, and thus the drain current of transistor 31 defines the quiescent current of the output stage. If V_{iset} is assumed to be a bias voltage that ensures the quiescent drain current of transistor

Petitioner Micron Ex-1004, 0216

31 is held at a predetermined level, the quiescent voltage value of the output is controlled by manipulating Vds of transistor 30 given the drain current defined by transistor 31. The gate voltage of transistor 30 is varied by altering the current in the P-channel source follower (transistors 34, 35) by changing the gate voltage of transistor 35. The signal CM_{CTL} is a control signal emanating from the output stage common mode feedback control circuit to be described in more detail below.

Consequently, in the quiescent state the output voltage is fixed at a predetermined value and the supply current drawn by the circuit is controlled. A positive deviation on Vo (the AC signal) results in an increased gate voltage at transistor 31 and a corresponding shut off of transistor 30. A negative deviation of Vo yields an increased turn on of transistor 30 and turn off of transistor 31, thus ensuring the Class AB operating conditions are maintained. Additional transistors 36, 37 ensure that no supply current is used in the power down state. These transistors have no effect on the circuit during normal operation.

The passive components shown in Figure 7 ensure AC compensation of the complete driver. In determining the values of these components, the following requirements must be taken into consideration:

- Reduction of the quiescent current in M1 and M2 reduces phase margin (increased impedance)

- M1 and M2 have large values of C_{GS}. The capacitance forms a pole with the output impedance of the source followers.

Petitioner Micron Ex-1004, 0217

Referring now to figure 8, this shows the common mode feedback control circuit for the output stage. The outputs of each amplifier are resistively summed by resistors 38, 39 to extract the common mode voltage. A differential amplifier consisting of transistors 40, 41 is then used to compare this with the bias (nominally $V_{DD}/2$). The differential amplifier generates the control signal CM_{CTL} (shown in figure 7) to generate the output common mode voltage control signal.

Referring now to Figure 9, the quiescent current regulator is designed to regulate the output stage quiescent current over wide process and temperature variations. The quiescent current regulator meshes with the output stage to effectively control the quiescent current.

In Figure 9, transistor 42 forms a 10μa current source. Transistor 43, in series with transistor 42, is connected as a diode device and thus forms a voltage reference for the circuit. The magnitude of the current I_O and the size of the transistor M2 are both related to quiescent current in the output stage of the amplifier.

The current I_O flowing through transistor 42 is mirrored into transistor 44, which is connected in series with a matched transistor 45. Transistors 44 and 45 are in turn parallel with series combination of transistors 46, 47.

Output transistors 48, 49 have as their main function to mimic the N-channel voltage follower (33, 32) in the output stage (Figure 7). The gate of transistor 48 is set to V_{bias}, which is the desired quiescent state value of the folded cascode output.

Petitioner Micron Ex-1004, 0218

The drain voltage of transistor 49 is connected to the gate of transistor 46. Transistors 45 and 47 are matched and have a common gate voltage.

The current I_O is mirrored into transistor 44 as previously indicated. The drain current of transistor 44 is the same as the drain current of transistor 45, and due to the matching of transistors 45 and 47, as well as their common gate voltage, the drain current of transistor 47 must equal the drain current of transistor 45. This means that the gate voltage of transistor 46 must be the same as the gate voltage of transistor 44, and this will only occur is adequate loop gain exists from the gate of transistor 46 to the drain of transistor 49.

Since the main function of transistors 48, 49 is to mimic the N-channel voltage follower in the output stage of the amplifier, the drain voltage of transistor 49 represents the gate voltage of the N-channel driver transistor in the output stage (transistor 31, Figure 7). This means that the voltage at the drain of transistor 49 is related to the output stage quiescent current.

The gate voltage of transistor 49 (V_{iset}) can therefore be used to bias the N-channel source followers (transistors 32, 33) of each amplifier in the output stage. The voltage generated at transistor 49 is effectively mirrored into the N-channel driver transistor of the output stage, and the sizing of transistor 43 and the magnitude of I_0 determine the quiescent current of the output stage in each amplifier. The above design results in an amplifier quiescent current which is insensitive to process variations.

Petitioner Micron Ex-1004, 0219

The above described circuit provides a simple design for a power amplifier that can implemented in CMOS technology in a simple and effective manner, and which is relatively insensitive to variations in process parameters.

Petitioner Micron Ex-1004, 0220

Claims:

1. A power amplifier characterized in that it comprises an input stage having a fully differential amplifier with differential inputs and differential outputs, and a high input impedance closed loop common mode feedback control circuit deriving common mode feedback control signals from said differential outputs; and an output stage comprising for each differential output of the input stage a class AB amplifier having N-channel and P-channel source followers interfacing with said folded cascode amplifier and a quiescent current control input for maintaining a desired quiescent current, means for maintaining the common mode output voltage of the class AB amplifiers at a desired level, and a quiescent current regulator for supplying a control signal to said quiescent current control inputs, said quiescent current regulator comprising means for mimicking the behaviour of one of said source followers to derive said control signal.

2. A power amplifier as claimed in claim 1, characterized in that the quiescent current regulator includes a pair of transistors that mimic one of the source followers of one of the class AB amplifiers, the gate of one of the mimic transistors is set to the quiescent state voltage of the input stage output, the drain voltage of the second mimic transistor corresponds to the drain voltage of one of a pair of transistors forming said one follower which is connected to the gate of an associated driver transistor in the output stage, and the gate voltage of the second mimic transistor is used to bias said one source follower of the output stage, whereby a reference voltage generated at the input of the

Petitioner Micron Ex-1004, 0221

quiescent current regulator is effectively mirrored into the associated driver transistor of the output stage determines the quiescent current of the output stage.

3. A power amplifier as claimed in claim 2, characterized in that said one source follower is the N-channel source follower and said associated driver transistor is the N-channel driver transistor.

4. A power amplifier as claimed in claim 2, characterized in that for each class AB amplifier a first of said source followers maintains the gate voltage of one driver transistor just over threshold value in the quiescent state so that the drain current of said driver transistor determines the quiescent current of the output stage and having a control input determining the level of said quiescent driver current, and a second of said followers determines the quiescent voltage output by determining the source - drain voltage of the other of said class AB driver transistors in response to an output common mode feedback control signal.

5. A power amplifier as claimed in Claim 4, further comprising means for summing the separate outputs for each class AB driver amplifier, and a differential amplifier for comparing the result of the summation to a reference voltage to produce said output common mode control signal.

6. A power amplifier as claimed in claim 5, characterized in that said quiescent current regulator further comprises a current source transistor supplying current to a diode-connected transistor providing said reference voltage source, a first transistor having its

Petitioner Micron Ex-1004, 0222

gate connected to said diode-connected transistor so that the current generated by the current source transistor is mirrored thereinto, said first transistor being in series with a second transistor, and said first and second transistors being in parallel with a series combination of third and fourth transistors, the said second and fourth transistors being matched and their gates being connected together such that the driver current in the second and fourth transistors is the same, the driver of said mimicking transistor being connected to the gate of the third transistor, and the gate of said one mimicking transistor being connected to the driver of the first transistor.

7. A power amplifier as claimed in claim 1, characterized in that said amplifier of the input stage is a folded cascode amplifier.

8. A power amplifier as claimed in Claim 7, characterized in that said common mode voltage feedback control circuit comprises a pair of voltage-dependent resistor means connected to said differential outputs of the folded cascode amplifier, means for producing a reference current I_o dependent on a bias voltage equal to the desired common mode voltage of the folded cascode amplifier, and means for ensuring that the sum C_1 of the currents flowing through said pair of voltage-dependent resistor means is equal to said reference current, and means for deriving a common mode common mode voltage signal from said reference current to maintain the common mode output voltage of said cascode amplifier equal to said reference voltage.

9. A power amplifier as claimed in Claim 8, characterized in that said voltage-dependent resistor means comprise transistors operating in the triode

Petitioner Micron Ex-1004, 0223

region.

10. A power amplifier as claimed in Claim 8 or 9, characterized in that said common mode voltage feedback control circuit comprises first and second parallel paths through which said respective currents I_o and I_1 flow, said first path including a pair of parallel-connected transistors with their gates tied to said reference voltage serving as a current sources and being in series with a further transistor, and said second path including said pair of voltage-dependent resistors in series with a further transistor, the further transistors of the respective paths being matched and having their gates connected together to ensure the currents in the two paths remain the same, and the common mode feedback control signal being produced at the drain of said further transistor in the first path.

11. A power amplifier as claimed in Claim 10, comprising an additional transistor in each said path, said additional transistors having their gates connected together and tied to a second reference voltage source.

12. A common mode voltage feedback control circuit for a fully differential amplifier comprising a pair of voltage-dependent resistor means for connection to the differential outputs of said amplifier, means for producing a reference current I_o dependent on a bias voltage equal to the desired common mode voltage of the folded cascode amplifier, means for ensuring that the sum C_1 of the currents flowing through said pair of voltage-dependent resistor means is equal to said reference current, and means for deriving a common mode common mode voltage signal from said reference current

Petitioner Micron Ex-1004, 0224

to maintain the common mode output voltage of said cascode amplifier equal to said reference voltage.

Petitioner Micron Ex-1004, 0225

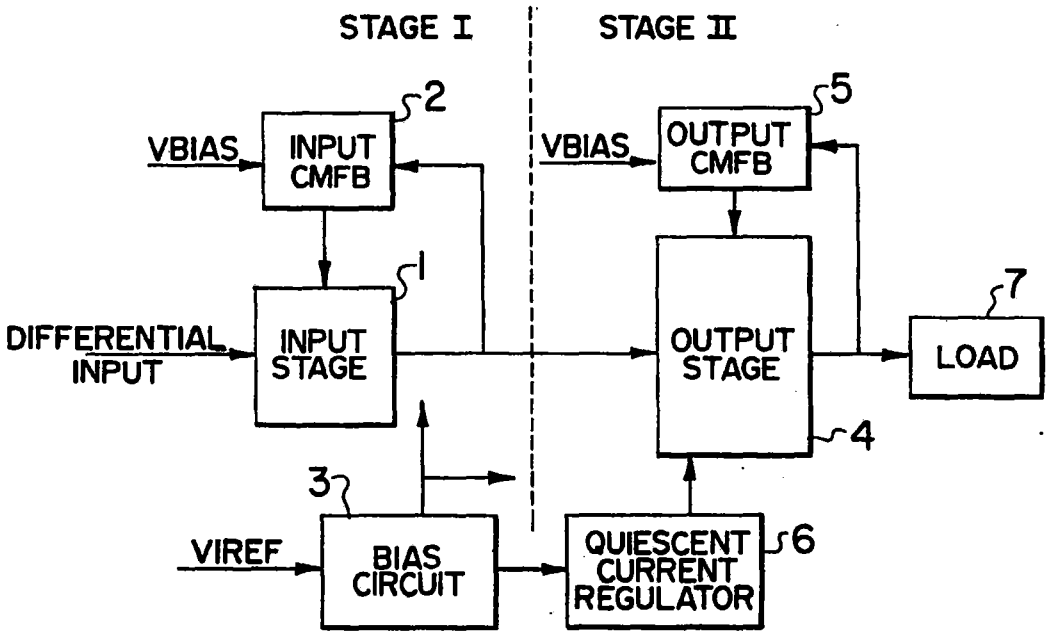


FIG. 1

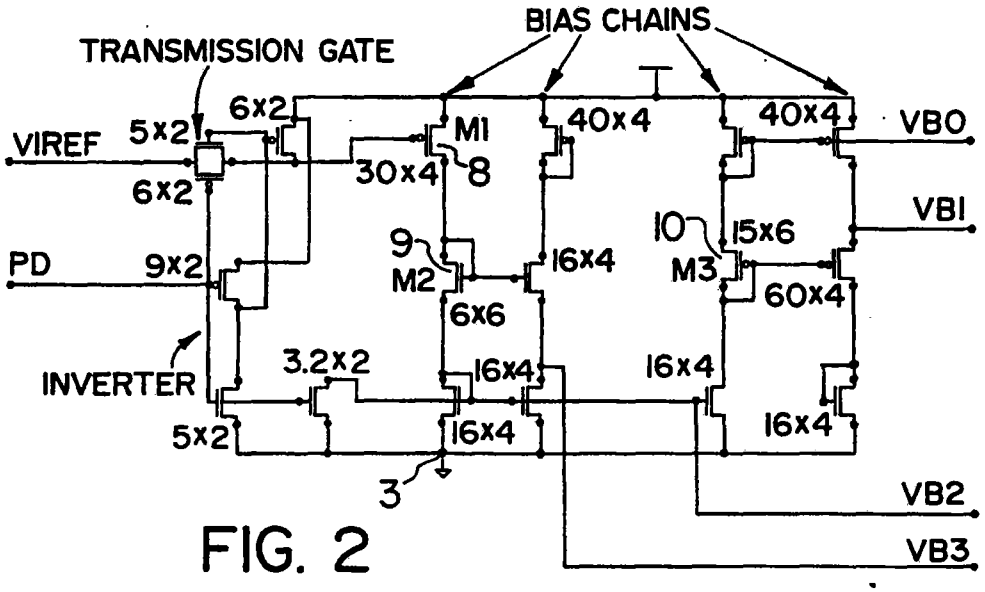


FIG. 2

SUBSTITUTE SHEET

Petitioner Micron Ex-1004, 0226

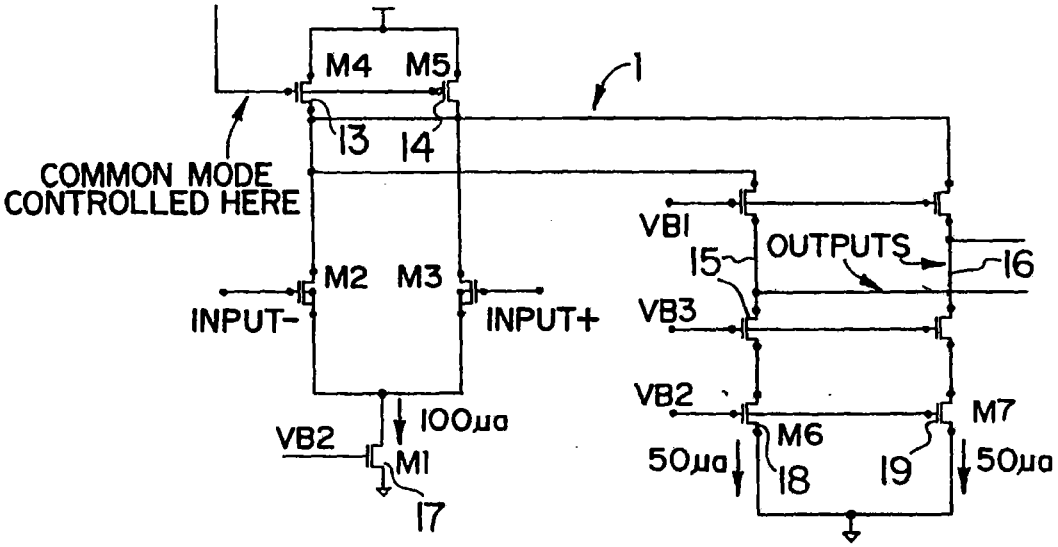


FIG. 3

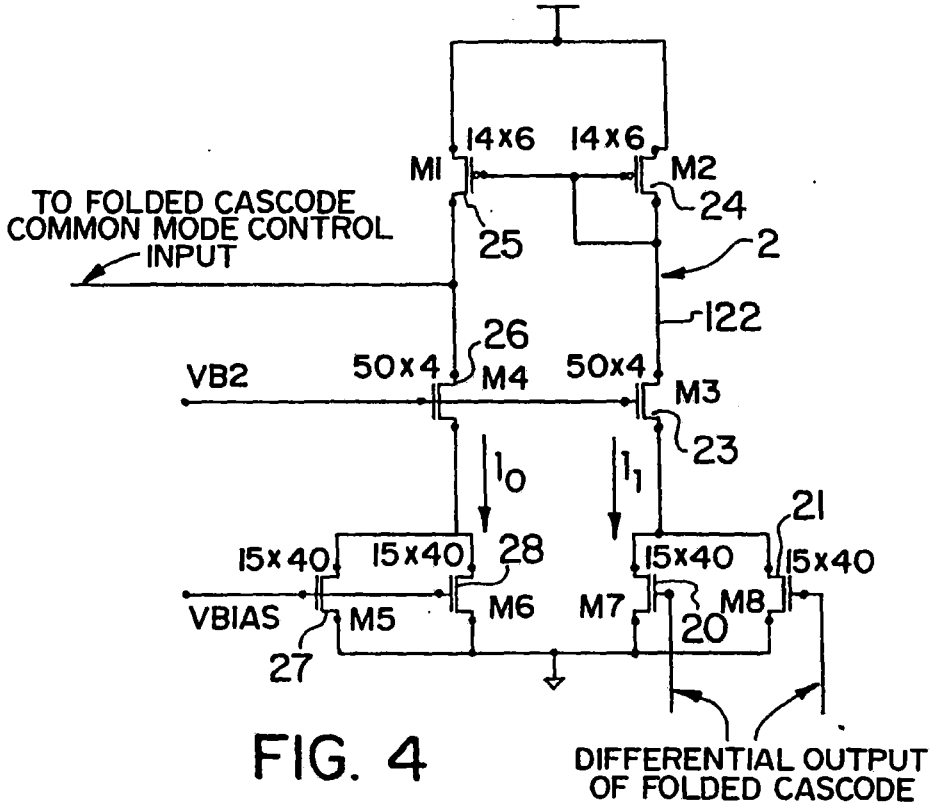


FIG. 4

SUBSTITUTE SHEET

Petitioner Micron Ex-1004, 0227

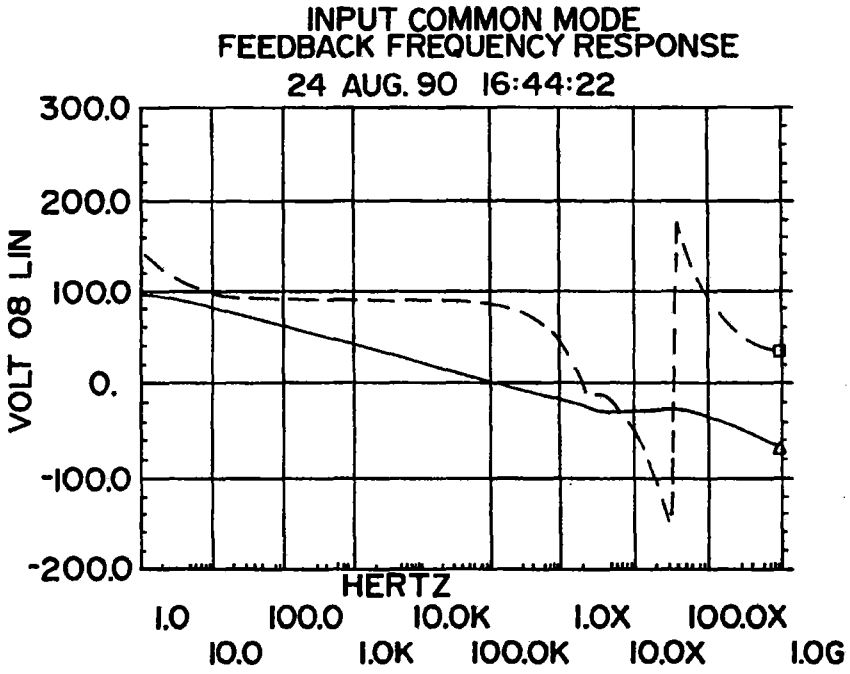


FIG. 5

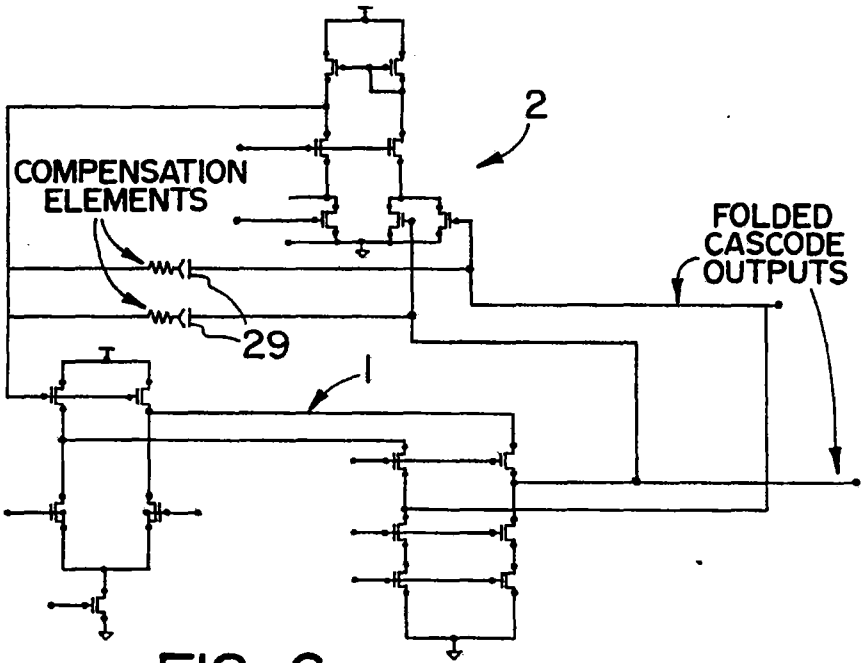


FIG. 6

SUBSTITUTE SHEET

Petitioner Micron Ex-1004, 0228

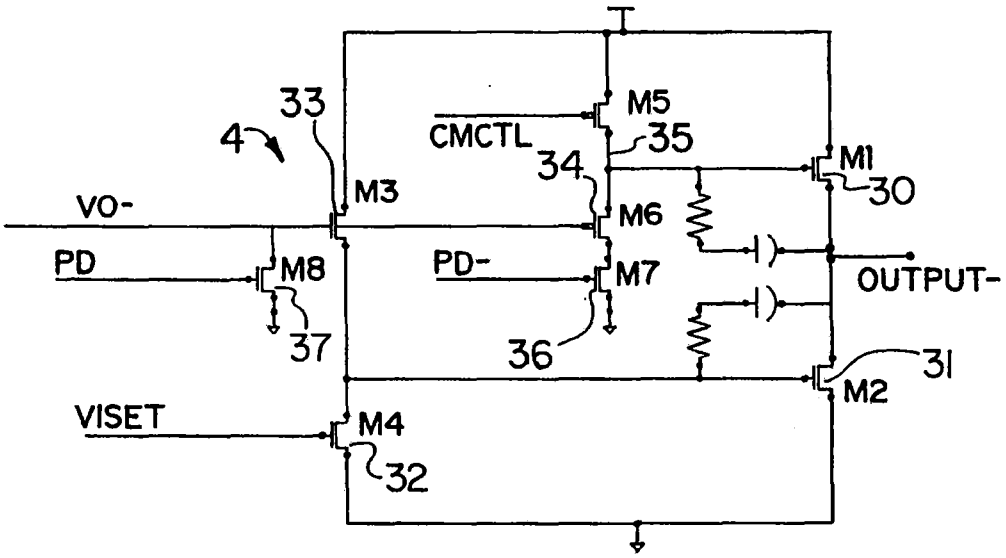


FIG. 7

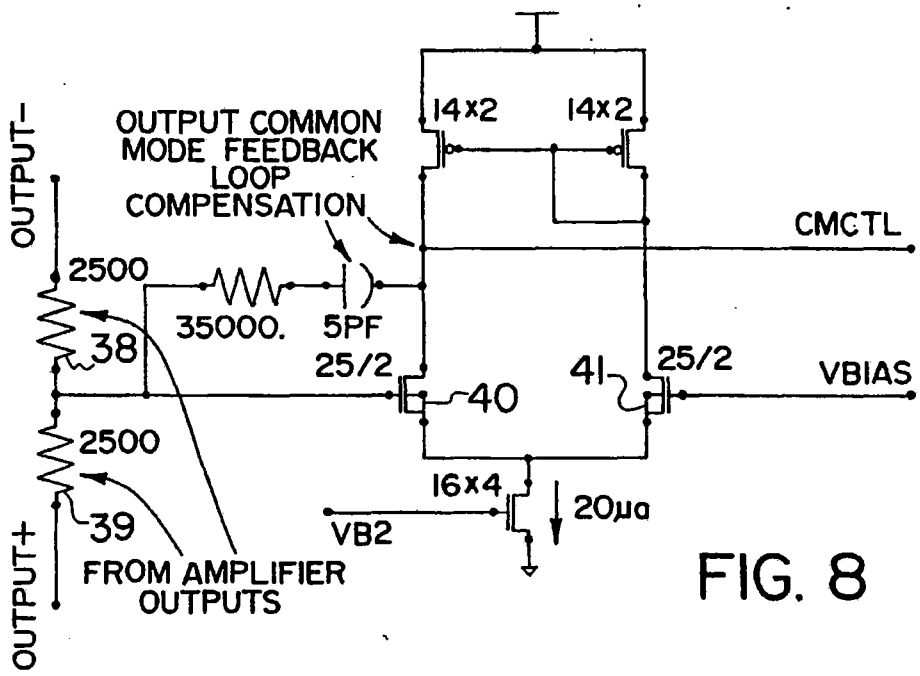


FIG. 8

SUBSTITUTE SHEET

Petitioner Micron Ex-1004, 0229

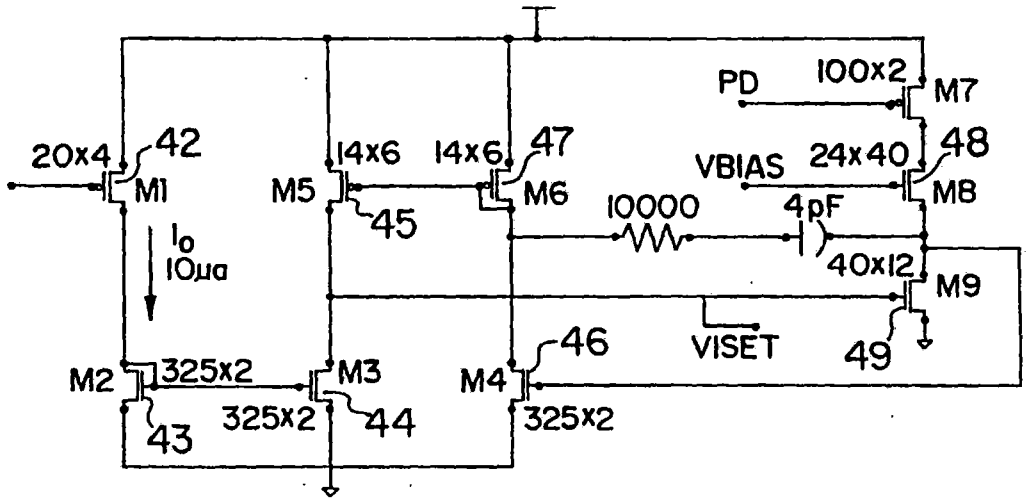


FIG. 9

SUBSTITUTE SHEET

INTERNATIONAL SEARCH REPORT

International Application No PCT/CA 92/00381

I. CLASSIFICATION OF SUBJECT MATTER (If several classification symbols apply, indicate all)[6]

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.Cl. 5 H03F3/45

II. FIELDS SEARCHED

Minimum Documentation Searched[7]

Classification System	Classification Symbols
Int.Cl. 5	H03F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched[8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT[9]

Category[10]	Citation of Document,[11] with indication, where appropriate, of the relevant passages[12]	Relevant to Claim No.[13]
A	IEEE INTERNATIONAL SOLID STATE CIRCUITS CONFERENCE vol. 34, February 1991, NEW YORK US pages 278 - 279 G. NICOLLINI ET AL 'A-78db THD 100 OHM DIFFERENTIAL DRIVER FOR ISDN APPLICATIONS' see the whole document ---	1-12
A	NEUES AUS DER TECHNIK no. 1, 20 February 1987, WURZBURG DE page 1 'OPERATIONSVERSTARKER' see the whole document ---	7-11
A	EP,A,0 325 299 (NEC CORPORATION) 26 July 1989 see column 6, line 44 - column 10, line 18; figures 4-5B ---	1-12

-/--

* Special categories of cited documents :[10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
30 NOVEMBER 1992	04. 12. 92
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	TYBERGHIEN G.M.

Form PCT/ISA/210 (second sheet) (January 1985)

Petitioner Micron Ex-1004, 0231

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category *	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No.
A	EP,A,0 138 261 (AMERICAN MICROSYSTEMS INC.) 24 April 1985 see the whole document	1-12

Petitioner Micron Ex-1004, 0232

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON INTERNATIONAL PATENT APPLICATION NO. CA 9200381 SA 63928

This annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 30/11/92

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP-A-0325299	26-07-89	JP-A- 1188008	27-07-89
		JP-A- 1280911	13-11-89
		US-A- 4963834	16-10-90
EP-A-0138261	24-04-85	US-A- 4533876	06-08-85
		CA-A- 1206217	17-06-86
		JP-A- 60116212	22-06-85

EPO FORM P0479

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

Petitioner Micron Ex-1004, 0233

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	1	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-2009/0033298	02-05-2009	Kleveland
		US-7,482,791	01-27-2009	Stoichita
		US-2008/0180080	07-31-2008	Terry
		US-7,091,709	08-15-2006	Suzuki
		US-6,653,891	11-25-2003	Hazucha
		US-6,573,694	06-03-2003	Pulkin
		US-6,304,131	10-16-2001	Huggins
		US-6,188,211	02-13-2001	Rincon-Mora
		US-6,140,805	10-31-2000	Kaneko
		US-6,058,488	05-02-2000	Eckhardt
		US-5,867,015	02-02-1999	Corsi
		US-5,519,656	05-21-1996	Maccarrone
		US-2003/0001550	01-02-2003	Pulkin
		US-2007/0164810	07-19-2007	Chen
		US-2007/0109052	05-17-2007	Franck
		US-2006/0220730	10-05-2006	Lobb
		US-2005/0225380	10-13-2005	Ingino
		US-2005/0134383	06-23-2005	Franck
		US-2005/0088205	04-28-2005	Jalaleddine

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]
		EP 1622067 B1	02-27-2008	Takabayashi	
		EP 0851332 B1	02-25-2004	Corsi	
		EP 0957421 B1	09-03-2003	Rincon-Mora	
		EP 0783796	07-16-1997	Tran	
		WO 9705696	02-13-1997	Tran	
		WO 9305572	03-18-1993	Molnar	

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	2	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-2004/0095701	05-20-2004	Ingino
		US-2004/0057169	03-25-2004	Amick
		US-2004/0056700	03-25-2004	Amick
		US-2003/0197492	10-23-2003	Kalpakjian
		US-2003/0155964	08-21-2003	Gauthier
		US-2003/0137341	07-24-2003	LeChevalier
		US-2002/0149398	10-17-2002	Ingino
		US-2002/0005710	01-17-2002	Kalpakjian
		US-7,394,306	07-01-2008	Chen
		US-7,368,994	05-06-2008	Franck
		US-7,173,482	02-06-2007	Lobb
		US-7,151,410	12-19-2006	Franck
		US-7,132,880	11-07-2006	Ingino
		US-6,924,674	08-02-2005	Jalaleddine
		US-6,914,476	07-05-2005	Ingino
		US-6,873,503	03-29-2005	Amick
		US-6,847,198	01-25-2005	Kalpakjian
		US-6,828,850	12-07-2004	LeChevalier
		US-6,809,557	10-26-2004	Gauthier

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]
		WO 2004/027995 A3	04-01-2004	Amick	
		EP 1229419 A3	08-04-2004	Ingino	
		EP 0661717 B1	03-29-2000	Maccarrone	
		EP 0602163 B1	01-08-1997	Molnar	
		EP 0497591 B1	04-02-1997	Bjorkman	

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

Substitute for form 1449/PTO				Complete if Known	
				Application Number	*Unknown*
INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Filing Date	Herewith
(Use as many sheets as necessary)				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	3	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-6,734,716	05-11-2004	Amick
		US-6,621,675	09-16-2003	Ingino
		US-6,586,916	07-01-2003	Kalpakjian
		US-6,331,766	12-18-2001	Kalpakjian
		US-6,285,614	09-04-2001	Mulatti
		US-6,175,221	01-16-2001	Kalpakjian
		US-6,118,266	09-12-2000	Manohar
		US-6,101,118	08-08-2000	Mulatti
		US-5,905,399	05-18-1999	Bosnyak
		US-5,739,681	04-14-1998	Allman
		US-5,675,241	10-07-1997	Teggatz
		US-5,631,606	05-20-1997	Tran
		US-5,512,814	04-30-1996	Allman
		US-5,428,316	06-27-1995	Molnar
		US-5,296,800	03-22-1994	Bjorkman
		US-5,202,587	04-13-1993	McLaury
		US-5,162,668	11-10-1992	Chen
		US-4,536,699	08-20-1985	Baker
		US-4,498,058	02-05-1985	Benrud

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	4	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-4,446,383	05-01-1984	Concannon
		US-6,809,504	10-26-2004	Tang
		US-6,975,494	12-13-2005	Tang
		US-7,319,314	01-15-2008	Maheshwari
		US-7,446,515	11-04-2008	Wang
		US-7,218,082	05-15-2007	Walter
		US-7,323,853	01-29-2008	Tang
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	5	of	5	Attorney Docket Number	4146.08US01

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		HAZUCHA et al., "Area-Efficient Linear Regulator With Ultra-Fast Load Regulation", IEEE Journal of Solid State Circuits, Vol. 40. No.4, April 2005. pp. 933-940.	
		HAZUCHA et al., "An Area-Efficient, Integrated, Linear Regulator with Ultra-Fast Load Regulation", Symposium On VLSI Circuits Digest of Technical Papers. 2004. pp. 218-221.	

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PTO/SB/06 (12-04)

Filing Date: 05/12/09

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/464,301

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**20** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**5** minus 3 =	* **2**	x$110			x$220	**440**
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL			TOTAL	**1530**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)	OR	RATE ($)	ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/SB/06 (12-04)

Filing Date: **05/12/09**

Approved for use through 7/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 12/464,301

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	**330**
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	**540**
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	**220**
TOTAL CLAIMS (37 CFR 1.16(i))	**20** minus 20 =		x$26		OR	x$52	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	**5** minus 3 =	* **2**	x$110			x$220	**440**
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $260 ($130 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR						
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))			195			390	
			TOTAL			TOTAL	**1530**

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					N/A		OR	N/A	
						TOTAL ADD'T FEE		OR	TOTAL ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01

CONFIRMATION NO. 1327

87955
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

FORMALITIES LETTER

OC000000036064655

Date Mailed: 05/28/2009

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Filing Date Granted

An application number and filing date have been accorded to this application. The application is informal since it does not comply with the regulations for the reason(s) indicated below. Applicant is given TWO MONTHS from the date of this Notice within which to correct the informalities indicated below. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings must be reasonably free from erasures and must be free from alterations, overwriting, interlineations, folds, and copy marks. See Figure(s) 1-5.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

Petitioner Micron Ex-1004, 0241

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/tketsela/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Micron Ex-1004, 0242

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/464,301	05/12/2009	2838	1530	4146.08US01	20	5

CONFIRMATION NO. 1327

87955
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

FILING RECEIPT

OC000000036064654

Date Mailed: 05/28/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Tomer Shaul Elran, Petah Tikva, ISRAEL;

Assignment For Published Patent Application

SANDISK CORPORATION, Milpitas, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/19/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/464,301**

Projected Publication Date: To Be Determined - pending completion of Corrected Papers

Non-Publication Request: No

Early Publication Request: No

Petitioner Micron Ex-1004, 0243

Title

TRANSIENT LOAD VOLTAGE REGULATOR

Preliminary Class

323

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

Petitioner Micron Ex-1004, 0244

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Petitioner Micron Ex-1004, 0245

Electronic Acknowledgement Receipt

EFS ID:	5644557
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Bradley Pedersen/Aubre Rabe
Filer Authorized By:	Bradley Pedersen
Attorney Docket Number:	4146.08US01
Receipt Date:	06-JUL-2009
Filing Date:	12-MAY-2009
Time Stamp:	13:03:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Power of Attorney	4146_08US01_POA.PDF	61490 4e8e100b78c1533ffb96981590373d71c0e7f272	no	2

Warnings:	
Information:	

Total Files Size (in bytes):	61490

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tomer Shaul Elran

Application No.: 12/464,301

Filed: May 12, 2009

Attorney Docket No.: 4146.08US01
MSA-1303-US

Examiner: *Unassigned*

Group: 2838

Title: **TRANSIENT LOAD VOLTAGE REGULATOR**

POWER OF ATTORNEY BY ASSIGNEE
AND REVOCATION OF PREVIOUS POWERS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SanDisk Corporation, ("Assignee"), a Delaware corporation having a place of business at 601 McCarthy Boulevard, Milpitas, CA 95035, certifies that to the best of Assignee's knowledge and belief it is the Assignee of the entire right, title, and interest in and to the above-referenced patent application and represents that the undersigned are representatives authorized and empowered to sign on behalf of the Assignee.

Documentary evidence pursuant to 37 C.F.R. 3.73(b) of the chain of title from the original owner to the assignee is recorded in the assignment records of the USPTO at Reel 022782 Frame 0600 as of June 4, 2009.

Pursuant to 37 C.F.R. §§1.36 and 3.71, the assignee hereby revokes all powers of attorney previously given and hereby appoints **COUNSEL NAMES & REGISTRATION NUMBERS: Marilyn Glaubensklee (35,521), Loretta Peters (43,855), Leah Sherry (43,918), Douglas W. Pinsky (46,994), Joseph L. Felber (48,109), Thomas N. Toombs (55,681), Tyler Thorp (59,124), Brad Pedersen (32,432), Amy Salmela (55,910), Vadim Braginsky (58,031), and Robert Ray (63,953)** as principal attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Petitioner Micron Ex-1004, 0248

Address all telephone calls to:	Brad Pedersen at telephone number (612) 349-5774.
Address all correspondence to:	Customer Number 87955 Brad D. Pedersen Patterson, Thuente, Skaar & Christensen, P.A. 4800 IDS Center, 80 South 8th Street Minneapolis, MN 55402-2100
Assignee of Interest:	SanDisk Corporation 601 McCarthy Boulevard Milpitas, CA 95035

Date 7/1/09 Signature _____

Name: E. Earle Thompson

Title: VP and Chief IP Counsel

Petitioner Micron Ex-1004, 0249

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01

CONFIRMATION NO. 1327

IMPROPER CPOA LETTER

87955
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

OC000000036831595

Date Mailed: 07/15/2009

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/06/2009. The Power of Attorney in this application is not accepted for the reason(s) listed below:

- The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.

/gbien-aime/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Micron Ex-1004, 0250

Attorney Docket No. MSA-1303-US
4146.08US01

ASSIGNMENT

For good and valuable consideration, receipt of which is hereby acknowledged, we hereby sell, assign and transfer to **SanDisk IL Ltd.** an Israeli corporation, having a place of business at 7 Atir Yeda Street, Kfar Saba, 44425 Israel, its successors and assigns, the entire right, title and interest throughout the world in our invention in:

TRANSIENT LOAD VOLTAGE REGULATOR

for which United States Patent Application No. 12/464,301 has been filed on May 12, 2009, and all patent applications and patents of every country for said invention, including divisions, reissues, continuations and extensions thereof, and all rights of priority resulting from the filing of said applications; I authorize the above-named assignee to apply for patents of foreign countries for said invention, and to claim all rights of priority without further authorization from me; I agree to execute all papers useful in connection with said United States and foreign applications, and generally to do everything possible to aid said assignee, their successors, assigns and nominees, at their request and expense, in obtaining and enforcing patents for said invention in all countries; and I request that the United States Patent and Trademark Office issue all patents granted for said invention to the above-named assignee, its successors and assigns.

Tomer Shaul Elran
Full name of sole or joint inventor (given name, family name)

Sole or Joint Inventor's signature

27/5/09
Date

Petah Tikva, Israel
Residence (City and either State or Foreign Country)

Israeli
Citizenship

Petitioner Micron Ex-1004, 0251

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 4146.08US01

Tomer Shaul Elran Confirmation No.: 1327

Application No.: 12/464,301 Examiner: *Unknown*

Filed: May 12, 2009 Group Art Unit: 2838

For: TRANSIENT LOAD VOLTAGE REGULATOR

PRELIMINARY AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

Prior to examination, and in response to the Notice to File Corrected Application Papers of May 28, 2009, please amend the above-identified application as follows:

The present amendment comprises the following sections:

A. Listing of Claims

B. Amendments to the Drawings

C. Remarks

Please grant any extension of time necessary for entry; charge any fee due to Deposit Account No. 16-0631.

AMENDMENTS TO THE DRAWINGS

Replacement FIGS. 1-7 are submitted herewith in response to the Notice to File Corrected Application Papers of 05/28/2009. Replacement FIG. 2 replaces FIG. 2 of the application as originally filed, which was informal. FIGS. 1 and 3-6 have been amended to reposition reference numerals so as not to interfere with lines of the drawings.

In addition, FIG. 7 is amended herein to correct a typographical error in a reference numeral. In particular, a second instance of reference numeral 707 has been replaced with reference numeral 708 to correspond with the specification as originally filed. No new matter has been added.

Petitioner Micron Ex-1004, 0253

REMARKS

This Preliminary Amendment is submitted in response to the Notice to File Corrected Application Papers of 05/28/2009. Claims 1-20 are pending. By this Amendment, no claims cancelled, amended, or added.

Amendment to the Drawings

Replacement FIGS. 1-7 are submitted herewith in response to the Notice to File Corrected Application Papers of 05/28/2009. Replacement FIG. 2 replaces FIG. 2 of the application as originally filed, which was informal. FIGS. 1 and 3-6 have been amended to reposition reference numerals so as not to interfere with lines of the drawings.

In addition, FIG. 7 is amended herein to correct a typographical error in a reference numeral. In particular, a second instance of reference numeral 707 has been replaced with reference numeral 708 to correspond with the specification as originally filed. No new matter has been added.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested.

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,

Amy M. Salmela
Registration No. 55,910

Petitioner Micron Ex-1004, 0254

Customer No. 24113
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South 8th Street
Minneapolis, Minnesota 55402-2100
Telephone: (612) 252-1538

Petitioner Micron Ex-1004, 0255

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Tomer Shaul Elran

Application No.: 12/464,301

Filed: May 12, 2009

Attorney Docket No.: 4146.08US01
MSA-1303-US

Examiner: *Unassigned*

Group: 2838

Title: **TRANSIENT LOAD VOLTAGE REGULATOR**

POWER OF ATTORNEY BY ASSIGNEE
AND REVOCATION OF PREVIOUS POWERS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

SanDisk Corporation, ("Assignee"), a Delaware corporation having a place of business at 601 McCarthy Boulevard, Milpitas, CA 95035, certifies that to the best of Assignee's knowledge and belief it is the Assignee of the entire right, title, and interest in and to the above-referenced patent application and represents that the undersigned are representatives authorized and empowered to sign on behalf of the Assignee.

Documentary evidence pursuant to 37 C.F.R. 3.73(b) of the chain of title from the original owner to the assignee is recorded in the assignment records of the USPTO at Reel 022782 Frame 0600 as of June 4, 2009.

Pursuant to 37 C.F.R. §§1.36 and 3.71, the assignee hereby revokes all powers of attorney previously given and hereby appoints **COUNSEL NAMES & REGISTRATION NUMBERS: Marilyn Glaubensklee (35,521), Loretta Peters (43,855), Leah Sherry (43,918), Douglas W. Pinsky (46,994), Joseph L. Felber (48,109), Thomas N. Toombs (55,681), Tyler Thorp (59,124), Brad Pedersen (32,432), Amy Salmela (55,910), Vadim Braginsky (58,031), and Robert Ray (63,953)** as principal attorneys to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Petitioner Micron Ex-1004, 0256

Address all telephone calls to:	Brad Pedersen at telephone number (612) 349-5774.
Address all correspondence to:	Customer Number 87955 Brad D. Pedersen Patterson, Thuente, Skaar & Christensen, P.A. 4800 IDS Center, 80 South 8th Street Minneapolis, MN 55402-2100
Assignee of Interest:	SanDisk Corporation 601 McCarthy Boulevard Milpitas, CA 95035

Date 7/1/09 Signature _____

Name: E. Earle Thompson

Title: VP and Chief IP Counsel

Petitioner Micron Ex-1004, 0257

LISTING OF CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remain(s) under examination in the application is presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough; and 2. added matter is shown by underlining.

Petitioner Micron Ex-1004, 0258

1. (Original) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;

a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;

a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit;

a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;

wherein said second current source is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases; and

Petitioner Micron Ex-1004, 0259

wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit.

2. (Original) The voltage regulator circuit of claim 1, wherein said second current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current source is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor.

3. (Original) The voltage regulator circuit of claim 2, wherein said replica transistor is an nmos transistor.

4. (Original) The voltage regulator of claim 2, wherein said second current source is constructed to supply said second current based on $K(Vgate - Vout - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

5. (Original) The voltage regulator circuit of claim 2, wherein said replica transistor is a pmos transistor.

Petitioner Micron Ex-1004, 0260

6. (Original) The voltage regulator of claim 2, wherein said second current source is constructed to supply said second current based on $K(Vout - Vgate - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

7. (Original) The voltage regulator circuit of claim 1, wherein said second current source further comprises at least one stability capacitor arrangement.

8. (Original) The voltage regulator circuit of claim 8, wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads.

9. (Original) The voltage regulator of claim 1, wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path.

10. (Original) The voltage regulator of claim 1, wherein said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp.

Petitioner Micron Ex-1004, 0261

11. (Original) The voltage regulator of claim 1, wherein said signal received at said pass device gate is a voltage.

12. (Original) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

an input adapted to receive a voltage from said power supply, wherein said input includes a positive node and a negative node;

an output adapted to be coupled to said load;

a current mirror that includes

a first transistor coupled to a first current path that includes a gate constructed to receive a bias voltage and a first end coupled to said positive node;

a second transistor coupled to a second current path that includes a gate coupled to said gate of said first transistor; and

wherein said current mirror is operable to mirror a current of said first current path at said second current path;

a feedback circuit coupled to said first current path that includes:

a differential amplifier that includes a first input, a second input, and an output, wherein said differential amplifier is adapted to provide, at said output, an output voltage based on a difference between a voltage at said first input and a voltage at said second input, and wherein said first input is constructed to receive a reference voltage;

Petitioner Micron Ex-1004, 0262

a feedback transistor that includes a gate, a first end, and a second end, wherein said first end is coupled to a second end of said first transistor of said current mirror, and wherein said second end is coupled to said negative node;

a voltage divider that includes a first end coupled to said second end of said first transistor of said current mirror and a second end coupled to said negative node;

wherein said second input of said differential amplifier is coupled to said voltage divider such that a voltage at said second input is based on a voltage across said first end and said second end of said feedback transistor, wherein said gate of said feedback transistor is coupled to said output of said differential amplifier; and

wherein said differential amplifier, said feedback transistor, and said voltage divider are constructed and arranged such that a voltage at said gate of said feedback transistor is maintained at a substantially constant magnitude;

a current source that includes a first end coupled to a second end of said second transistor of said current mirror and a second end coupled to said negative node, and wherein said current source is constructed to receive a first voltage reference based on a voltage at said gate of said feedback transistor and a second voltage reference based on a voltage at said output of said voltage regulator circuit and supply a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;

a pass device that includes a first end coupled to said positive node, a second end constructed to be coupled to said load at said output of said voltage regulator circuit, and a gate coupled to said second end of said second transistor of said current mirror and said first end of

Petitioner Micron Ex-1004, 0263

said current source, wherein said gate is adapted to receive a signal based on a magnitude of a current of said second current path;

wherein said current source is constructed to, if said second voltage reference increases in magnitude, cause a decrease said signal received at said gate of said pass device, and if said second voltage reference decreases in magnitude, cause an increase in a magnitude of said signal received at said gate of said pass device;

wherein said pass device is constructed to supply a load current to a load coupled to said output of said voltage regulator circuit with a magnitude based on said signal received at said gate of said pass device; and

wherein said current mirror, said feedback circuit, said current source, and said pass device are integrated in an integrated circuit.

13. (Original) The voltage regulator circuit of claim 16, wherein said current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and said output of said voltage regulator circuit, and wherein said current source is adapted to supply a current with a magnitude based on said signal received at said gate of said replica transistor.

14. (Original) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions, comprising:

Petitioner Micron Ex-1004, 0264

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a first current path referenced to said input;

feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;

first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;

second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;

means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;

wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage at said load increases, a magnitude of said load current is decreased; and

wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit.

Petitioner Micron Ex-1004, 0265

15. (Original) The voltage regulator circuit of claim 14, wherein said second current supply means includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current supply means are for supplying said second current with a magnitude based on said voltage at said gate of said replica transistor.

16. (Original) A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

receiving, from a power supply, a power supply voltage;

supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current;

receiving, at a feedback transistor integrated in said integrated circuit, said master current;

maintaining, via a feedback circuit integrated in said integrated circuit and coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant;

supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude;

supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load;

Petitioner Micron Ex-1004, 0266

receiving, at a gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path; and

supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.

17. (Original) A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

generating, at a first current path integrated in said integrated circuit, a substantially constant master current;

supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current;

supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load;

receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path;

supplying, to said load circuitry via said pass transistor, a load current in response to said control signal; and

Petitioner Micron Ex-1004, 0267

wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current.

18. (Original) The method of claim 8, wherein supplying said second current includes supplying a current based on a difference between a voltage at a gate of a feedback transistor of a feedback circuit and a voltage at said load circuitry.

19. (Original) The method of claim 1, wherein supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases.

20. (Original) The method of claim 11, wherein supplying said load current includes supplying a current with a magnitude of less than one amp, and wherein supplying first current and supplying said second current includes supplying a current with a magnitude of less than one milli-amp.

Petitioner Micron Ex-1004, 0268

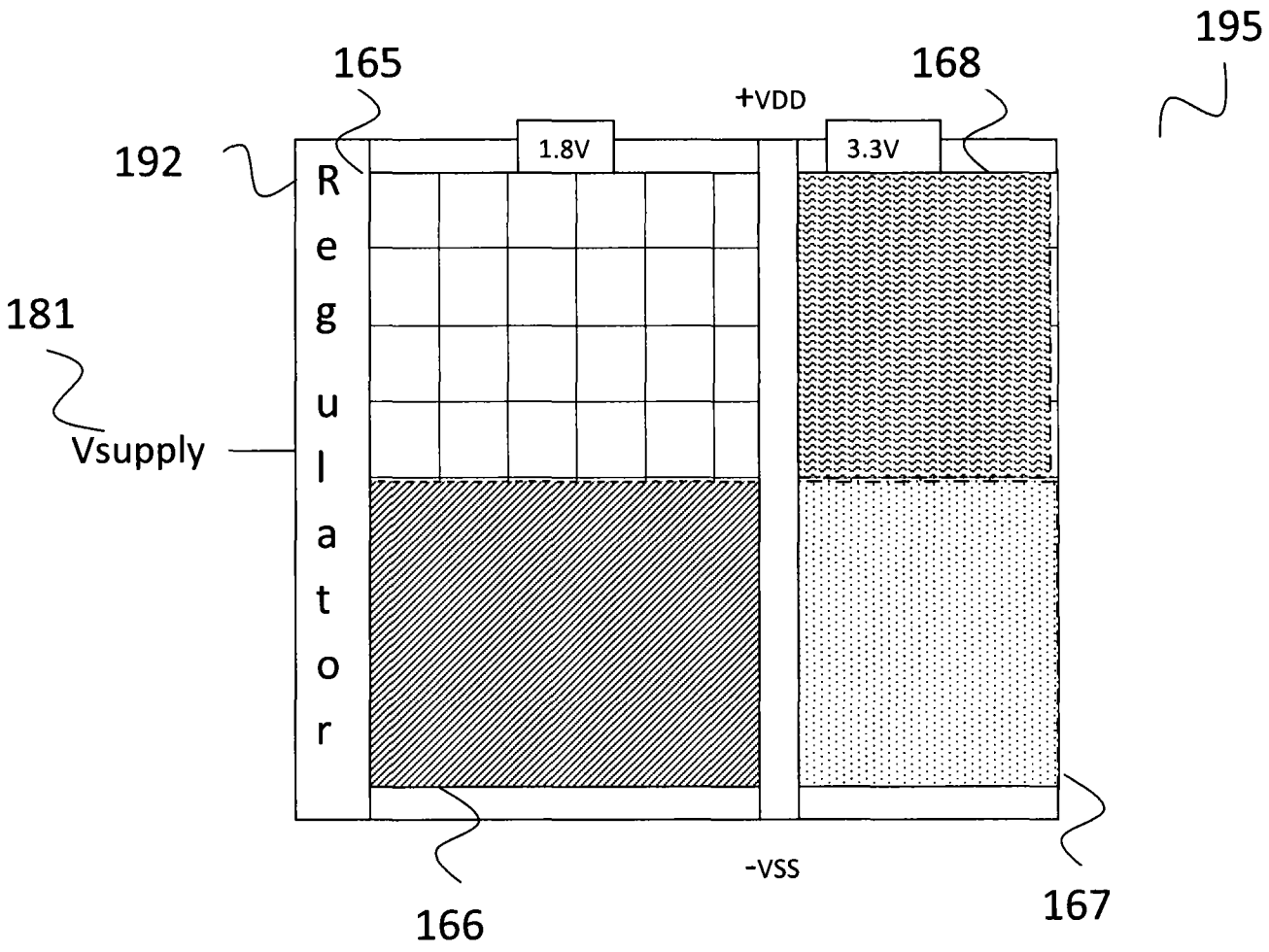


FIG. 1

Prior Art

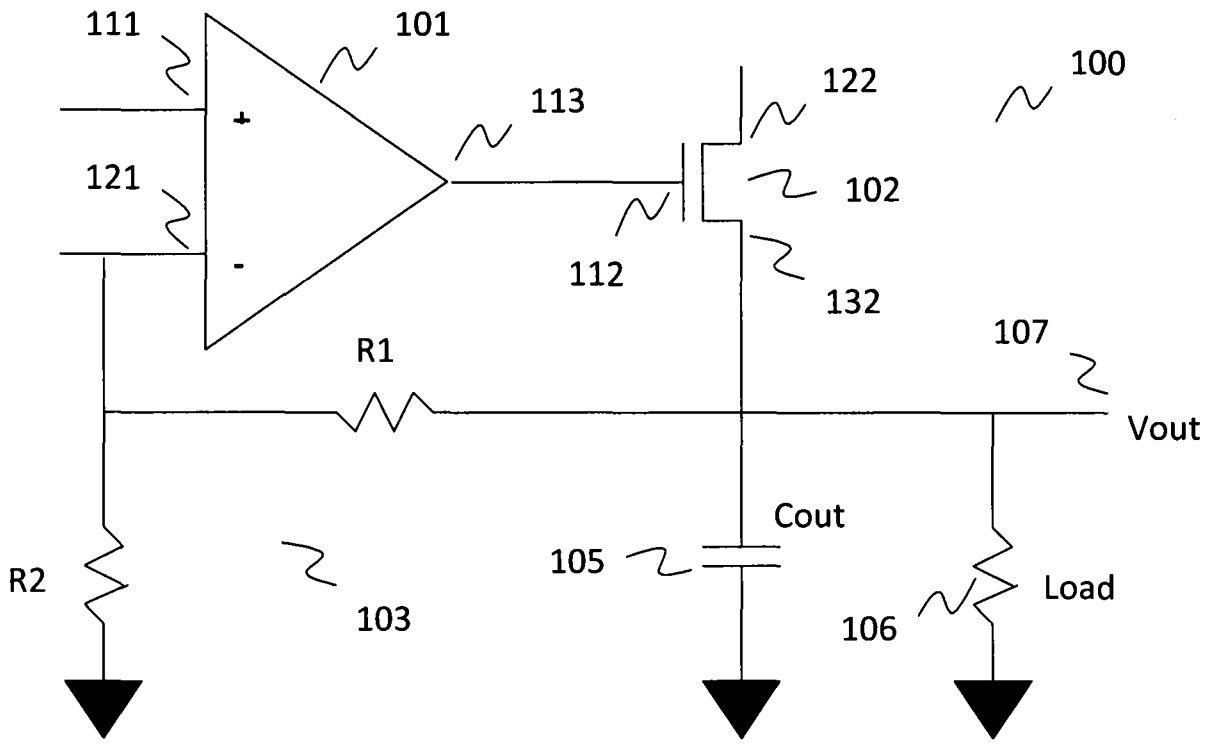


FIG. 2

Prior Art

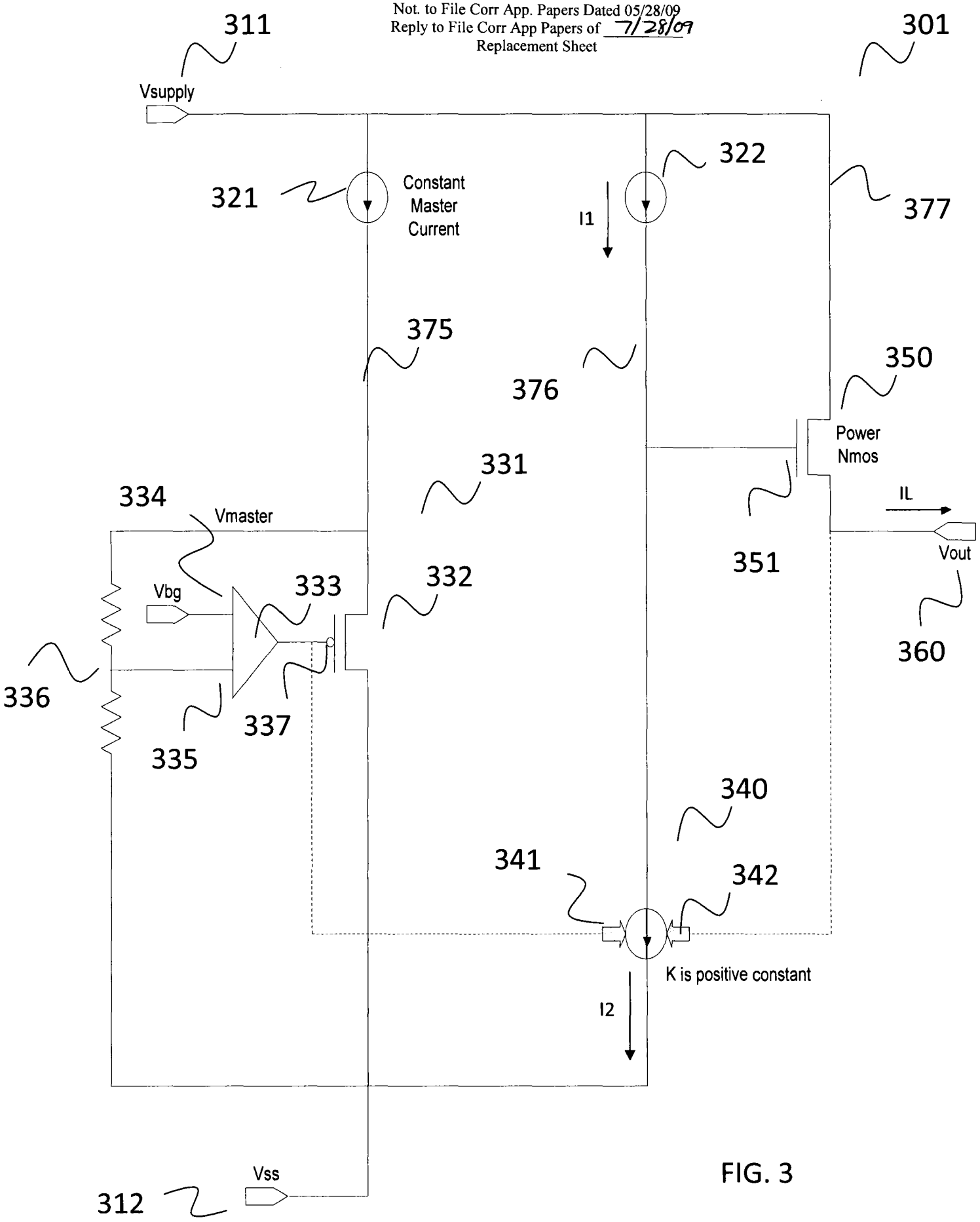

311
301
Vsupply
322
321
Constant
Master
Current
I1
377
375
376
350
Power
Nmos
331
334
IL
Vmaster
351
Vout
Vbg
333
332
360
336
337
335
340
341
342
K is positive constant
I2
Vss
312

FIG. 3

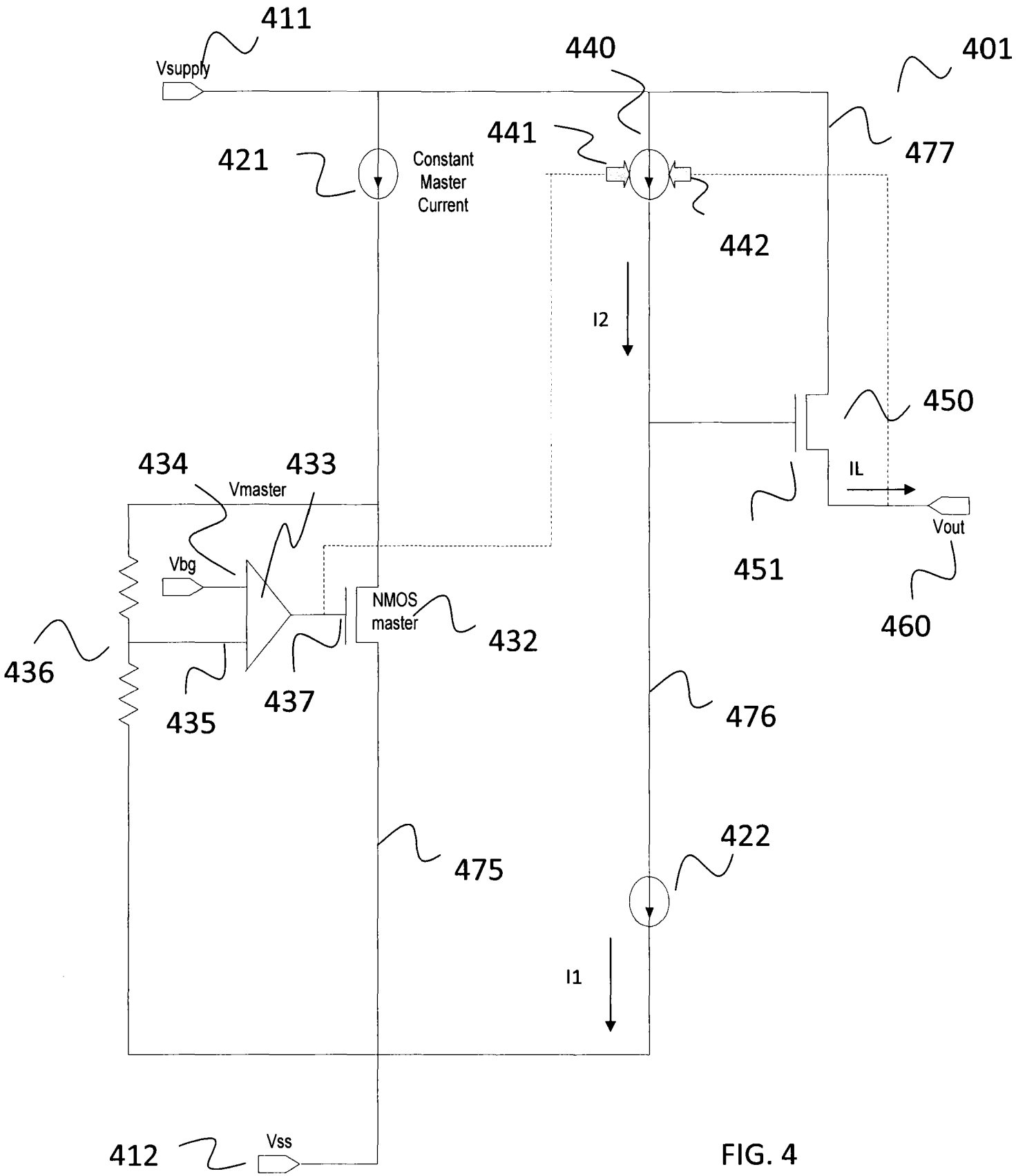

411
Vsupply
440
401
441
421
Constant
Master
Current
477
442
I2
450
434
433
Vmaster
IL
Vout
Vbg
NMOS
master
451
460
436
432
435
437
476
475
422
I1
412
Vss

FIG. 4

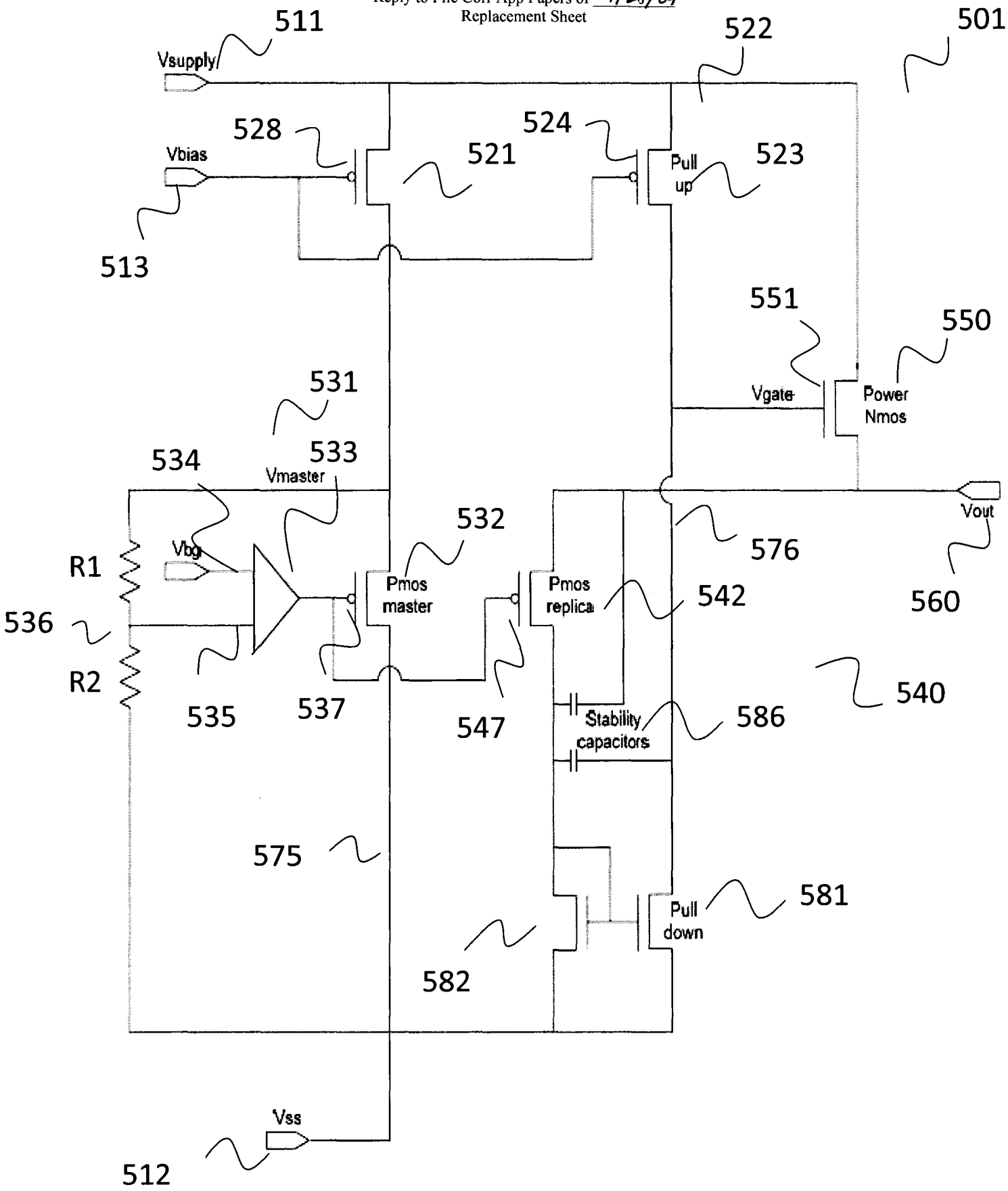

511
Vsupply
522
501
528
524
Vbias
521
Pull up
523
513
551
550
531
Vgate
Power Nmos
534
533
Vmaster
532
Vout
576
R1
Vbg
Pmos master
Pmos replica
542
560
536
R2
540
535
537
547
Stability capacitors
586
575
581
Pull down
582
Vss
512

FIG. 5

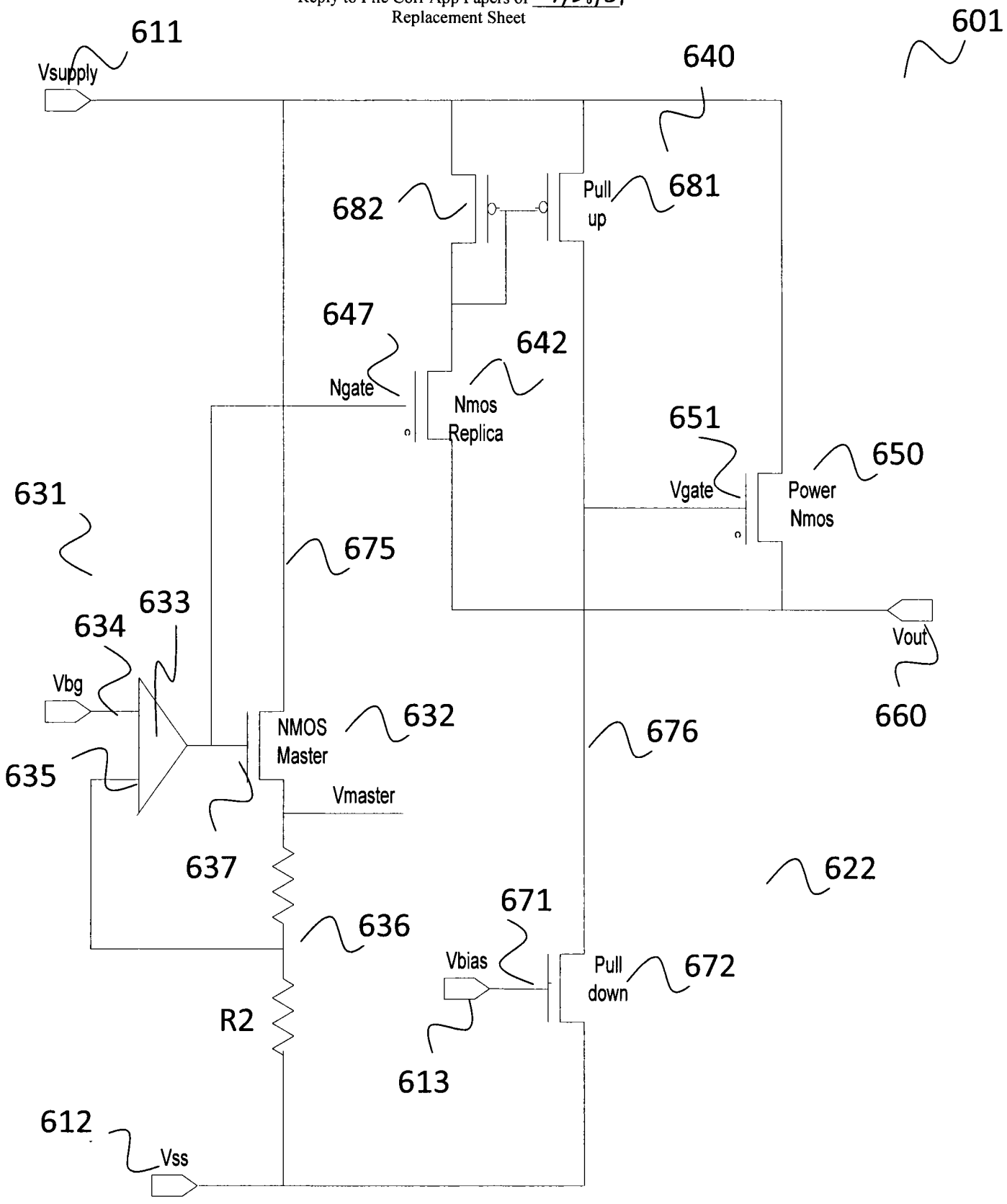

601
611
Vsupply
640
682
Pull
up
681
647
642
Ngate
Nmos
Replica
651
650
Vgate
Power
Nmos
631
675
633
634
Vbg
Vout
660
NMOS
Master
632
676
635
Vmaster
637
622
671
636
Vbias
Pull
down
672
R2
613
612
Vss

Fig. 6

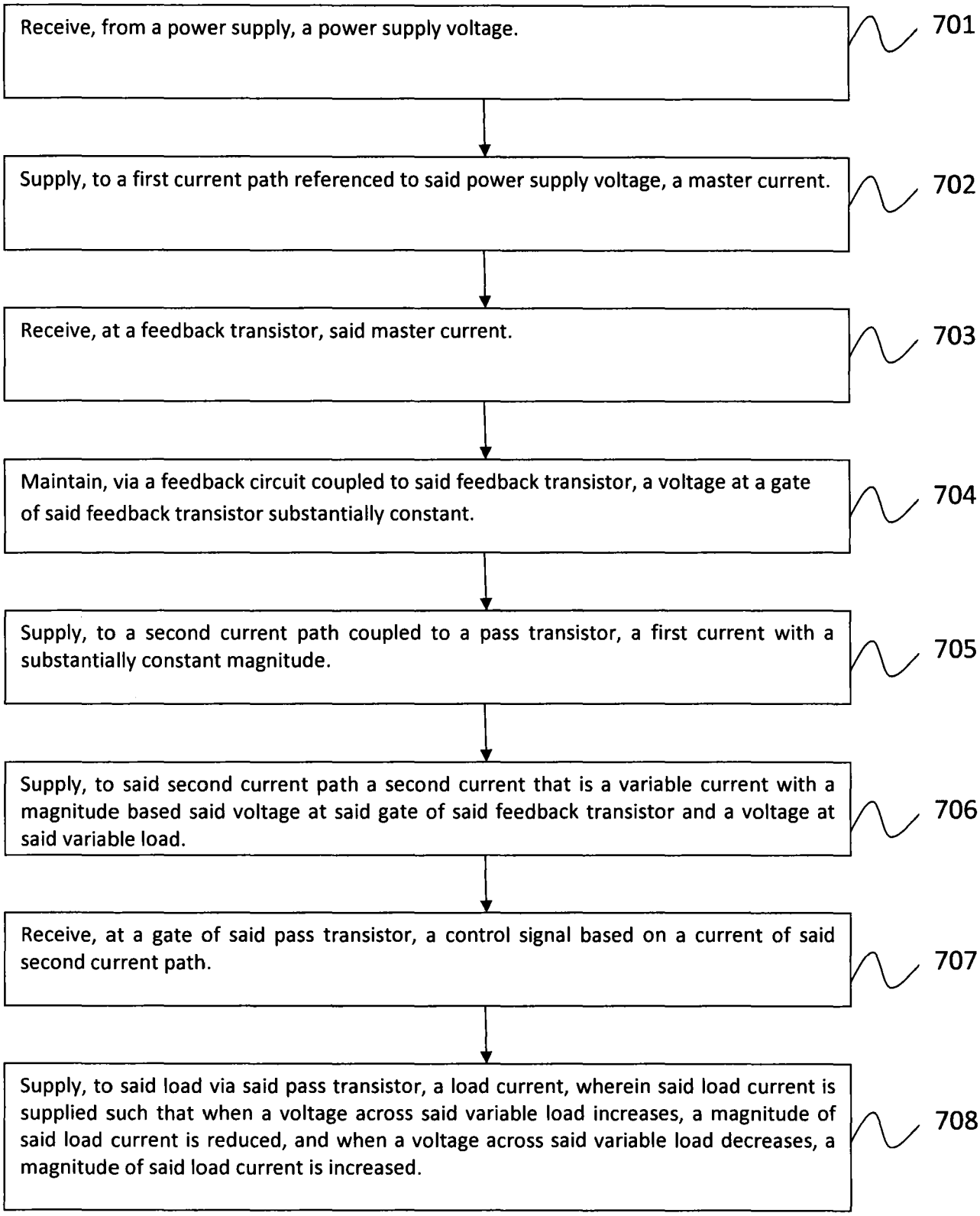

Receive, from a power supply, a power supply voltage.
701
Supply, to a first current path referenced to said power supply voltage, a master current.
702
Receive, at a feedback transistor, said master current.
703
Maintain, via a feedback circuit coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant.
704
Supply, to a second current path coupled to a pass transistor, a first current with a substantially constant magnitude.
705
Supply, to said second current path a second current that is a variable current with a magnitude based said voltage at said gate of said feedback transistor and a voltage at said variable load.
706
Receive, at a gate of said pass transistor, a control signal based on a current of said second current path.
707
Supply, to said load via said pass transistor, a load current, wherein said load current is supplied such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.
708

Fig. 7

Electronic Acknowledgement Receipt

EFS ID:	5780050
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Amy M. Salmela/Aubre Rabe
Filer Authorized By:	Amy M. Salmela
Attorney Docket Number:	4146.08US01
Receipt Date:	28-JUL-2009
Filing Date:	12-MAY-2009
Time Stamp:	10:26:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		4146_08US01_PreAmend_Corr Drwgs.PDF	650835 0a5492b2478b571d2f2cc0d5896a261d2e5f6a91	yes	22

	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Preliminary Amendment		1	1	
	Claims		2	12	
	Drawings-only black and white line drawings		13	13	
	Applicant Arguments/Remarks Made in an Amendment		14	15	
	Drawings-only black and white line drawings		16	22	
Warnings:					
Information:					
2		4146_08US01_POA.PDF	106633 98c3c1216351858fd79a094cc0ce42ee9398f2be	yes	3
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Power of Attorney		1	2	
	Assignee showing of ownership per 37 CFR 3.73(b).		3	3	
Warnings:					
Information:					
		Total Files Size (in bytes):	757468		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/464,301	05/12/2009	

APPLICATION AS FILED – PART I

	(Column 1)	(Column 2)	SMALL ENTITY ☐		OR	OTHER THAN SMALL ENTITY	
FOR	NUMBER FILED	NUMBER EXTRA	RATE ($)	FEE ($)		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT	07/28/2009	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $52=	0
	Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $220=	0
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
	☐ Application Size Fee (37 CFR 1.16(s))									
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/KAREN VESTAL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
12/464,301	05/12/2009	2838	1530	4146.08US01	20	5

CONFIRMATION NO. 1327

UPDATED FILING RECEIPT

87955
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

OC000000037202745

Date Mailed: 08/05/2009

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Tomer Shaul Elran, Petah Tikva, ISRAEL;

Assignment For Published Patent Application

SANDISK CORPORATION, Milpitas, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/19/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 12/464,301**

Projected Publication Date: 11/18/2010

Non-Publication Request: No

Early Publication Request: No

Petitioner Micron Ex-1004, 0279

Title

TRANSIENT LOAD VOLTAGE REGULATOR

Preliminary Class

323

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

Petitioner Micron Ex-1004, 0280

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

Petitioner Micron Ex-1004, 0281

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01

CONFIRMATION NO. 1327

IMPROPER CPOA LETTER

87955
Patterson, Thuente, Skaar & Christensen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

OC000000037174833

Date Mailed: 08/05/2009

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 07/28/2009. The Power of Attorney in this application is not accepted for the reason(s) listed below:

- The Power of Attorney you provided did not comply with the new Power of Attorney rules that became effective on June 25, 2004. See 37 CFR 1.32.

/mayalew/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01

CONFIRMATION NO. 1327

87955
Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

PUBLICATION NOTICE

OC000000044555106

Title:TRANSIENT LOAD VOLTAGE REGULATOR

Publication No.US-2010-0289465-A1
Publication Date:11/18/2010

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Micron Ex-1004, 0283

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

87955 7590 11/30/2010

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
11/30/2010	PAPER

Notice of Erroneous Early Release of Patent Application Information on November 11, 2010

On November 11, 2010, the United States Patent and Trademark Office (USPTO), unintentionally and as a result of a processing error, made available to subscribers of patent application data the patent application publications that were not scheduled to publish under 35 U.S.C. 122(b) until November 18, 2010. The USPTO's subscription service allows a member of the public to obtain copies of all patents or application publications from the USPTO on the date of grant or publication for a fee. One subscriber who had access to the early-published data made these premature patent application publications available on its free Web service, known as Free Patents Online, on November 11, 2010 - one week prior to the scheduled publication date. At the USPTO's request, the subscriber removed access to the patent application publications dated November 18, 2010 on November 15, 2010 until November 18, 2010. While the premature release of application information on November 11, 2010, is not considered a publication of such applications under 35 U.S.C. 122(b), the USPTO acknowledges that there are potential international ramifications in certain very limited circumstances such as where an applicant whose application information was released early did not file a foreign application within the Paris Convention priority period but did file in a foreign country between November 11, 2010 and November 18, 2010.

The USPTO did not post the publications on its Web site until November 18, 2010, and it did not provide access to the public Patent Application Information Retrieval (PAIR) System based on the early release of the publication data. Moreover, the USPTO did not record in its records that a publication occurred until November 18, 2010. Copies of, and access to, any of the affected applications described in this document were not provided by the USPTO under 37 CFR 1.14 based on the error described in this document. The USPTO regrets this error and is instituting controls to prevent similar processing errors in the future.

Inquiries regarding this matter may be directed to Mark Polutta, Senior Legal Advisor, Office of Patent Legal Administration at (571) 272-7709 or via email addressed to mark.polutta@uspto.gov.

M327

71045

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
SANFORD T. COLB & CO.
P.O. BOX 2273
76122 REHOVOT
ISRAEL

ס. קולב ושות'
עורכי-דין ועורכי פטנטים
07 -09- 2010
נתקבל
רחובות

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

Date of mailing *(day/month/year)*	03 SEP 2010
Applicant's or agent's file reference 71045	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/IL 10/00377	International filing date *(day/month/year)* 12 May 2010 (12.05.2010)
Applicant SANDISK IL LTD.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 8270

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
SANFORD T. COLB & CO.
P.O. BOX 2273
76122 REHOVOT
ISRAEL

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 03 SEP 2010
Applicant's or agent's file reference 71045	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/IL 10/00377	International filing date *(day/month/year)* 12 May 2010 (12.05.2010)
Applicant SANDISK IL LTD.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 8270

   For more detailed instructions, see the notes on the accompanying sheet.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to the protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with the applicant's request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau as provided in Rules 90*bis*.1 and 90*bis*.3, respectively, before the completion of the technical preparations for international publication.

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. These comments would also be made available to the public but not before the expiration of 30 months from the priority date.

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   See the Annex to Form PCT/IB/301 and, for details about the applicable time limits, Office by Office, see the *PCT Applicant's Guide*, Volume II, National Chapters and the WIPO Internet site.

Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/220 (January 2004) *(See notes on accompanying sheet)*

Petitioner Micron Ex-1004, 0286

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	12/464,301
				Filing Date	May 12, 2009
				First Named Inventor	Tomer Shaul Elran
				Art Unit	2838
				Examiner Name	Jue Zhang
Sheet	1	of	2	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
		US-7,352,210	04-01-2008	Luo
		US-2008/0174289	07-24-2008	Gurcan, et al.
		US-2007/0268008	11-22-2007	Gicquel, et al.
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	12/464,301
				Filing Date	May 12, 2009
				First Named Inventor	Tomer Shaul Elran
				Art Unit	2838
				Examiner Name	Jue Zhang
Sheet	2	of	2	Attorney Docket Number	4146.08US01

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
		Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority, or the Declaration (PCT Rule 44.1) Mailing Date of September 3, 2010	
		International Search Report for International Application No. PCT/IL 10/00377 Dated May 12, 2010	
		Written Opinion of the International Searching Authority for International Application No. PCT/IL 10/00377 Dated May 12, 2010	

EXAMINER SIGNATURE		DATE CONSIDERED	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: SANFORD T. COLB & CO.
P.O. BOX 2273
76122 REHOVOT
ISRAEL

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	03 SEP 2010

Applicant's or agent's file reference	FOR FURTHER ACTION
71045	See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/IL 10/00377	12 May 2010 (12.05.2010)	12 May 2009 (12.05.2009)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G05F 3/04 (2010.01)
USPC - 323/311

Applicant SANDISK IL LTD.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	20 August 2010 (20.08.2010)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2009)

Petitioner Micron Ex-1004, 0289

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL 10/00377

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)

      ☐ on paper

      ☐ in electronic form

   b. (time)

      ☐ in the international application as filed

      ☐ together with the international application in electronic form

      ☐ subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Petitioner Micron Ex-1004, 0290

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL 10/00377

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	none	NO
Inventive step (IS)	Claims	none	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	none	NO

2. Citations and explanations:

Claims 1, 7-8, 10-11, 14 and 16-20 lack an inventive step under PCT Article 33(3) for being obvious over US 7,446,515 B2 to WANG (hereafter "Wang") in view of US 7,352,210 B2 to LUO (hereafter "Luo").

Regarding claim 1, Wang discloses a voltage regulator circuit integrated in an integrated circuit (IC) (col 2, ln 17-34; col 7, ln 12-14) and adapted to provide a voltage from a power supply to a load under varying load conditions (col 3, ln 56-60), comprising: a feedback circuit coupled to a first current path and including a feedback transistor (col 2, ln 43-53), wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant (col 6, ln 66 to col 7, ln 6); a first current supply circuit constructed to supply to a second current path a first current that is substantially constant (col 4, ln 52-67); said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit (col 4, ln 52 to col 5, ln 7); a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal (col 4, ln 35-50); wherein said second current source is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases (col 7, ln 36-42) and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases (col 7, ln 22-29); and wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit (col 2, ln 17-34) and referenced to said input of said voltage regulator circuit (col 2, ln 41-43; col 3, ln 37-56). While not expressly disclosed in Wang, Luo discloses an input adapted to receive a voltage from said power supply (col 5, ln 49-53); an output adapted to be coupled to said load (col 5, ln 44-45); and a second current supply circuit coupled to said first current supply circuit (col 3, ln 13-17). It would have been obvious to one skilled in the art to combine the voltage regulator features of Luo with the voltage regulator of Wang because Luo expressly discloses a power supply that must also be present in Wang and Luo's second current supply circuit coupled to the first current supply in Wang is disclosed in a feedback network for regulating the output such as that disclosed in Wang.

Regarding claim 7, Wang discloses said second current source further comprises at least one stability capacitor arrangement (col 7, ln 50-57).

Regarding claim 8, Luo discloses said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads (col 6, ln 58-59). It would have been obvious to one skilled in the art to combine the stability capacitor value of Luo with the voltage regulator of Wang because both Wang and Luo disclose a filter capacitor in the feedback network for stabilizing the network, while Luo discloses a value range encompassing the claimed value.

Regarding claim 10, Wang discloses said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp. These values are arbitrary and obvious in that other value relations between load current and second current pump magnitude are possible in similar voltage regulators and the application assigns no inventive significance to the claimed values.

Regarding claim 11, Wang discloses said signal received at said pass device gate is a voltage (col 2, ln 35-41).

(Continued in Supplemental Box)

Petitioner Micron Ex-1004, 0291

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL 10/00377

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:
Box V 2: Citations and explanations (continued)

Regarding claim 14, Wang discloses a voltage regulator circuit integrated in an integrated circuit (IC) (col 2, ln 17-34) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions (col 3, ln 56-60), comprising: feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant (col 7, ln 16 to col 7, ln 6); first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant (col 4, ln 52-67); said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference (col 4, ln 52 to col 5, ln 7); means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal (col 4, ln 35-51); wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage at said load increases, a magnitude of said load current is decreased (col 7, ln 36-42); and wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit (col 2, ln 17-34). though not expressly disclosed in Wang, Luo discloses an input adapted to receive a voltage from said power supply (col 5, ln 49-53); an output adapted to be coupled to said load (col 5, ln 44-45); a first current path referenced to said input (col 6, ln 16-28); and second current supply means coupled to said first current supply means (col 3, ln 13-17). It would have been obvious to one skilled in the art to combine the voltage regulator features of Luo with the voltage regulator of Wang because Luo expressly discloses a power supply that must also be present in Wang and Luo's second current supply circuit coupled to the first current supply in Wang is disclosed in a feedback network for regulating the output such as that disclosed in Wang.

Regarding claim 16, Wang discloses a method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising: receiving, at a feedback transistor integrated in said integrated circuit, said master current (col 2, ln 43-53); maintaining, via a feedback circuit integrated in said integrated circuit and coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant (col 6, ln 16 to col 7, ln 6); supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude (col 4, ln 52-67); supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load (col 4, ln 35-50); receiving, at a gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path (col 5, ln 18-22); and supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced (col 7, ln 36-42), and when a voltage across said variable load decreases, a magnitude of said load current is increased (col 7, ln 22-29). Though not expressly disclosed by Wang, Luo discloses receiving, from a power supply, a power supply voltage (col 5, ln 49-53); and supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current (col 5, ln 54-67). It would have been obvious to one skilled in the art to combine the voltage regulator features of Luo with the voltage regulator of Wang because Luo expressly discloses a power supply that must also be present in Wang and Luo's master current supply circuit coupled to the first current supply in Wang is disclosed in a feedback network for regulating the output such as that disclosed in Wang.

Regarding claim 17, Wang discloses a method of regulating a supply voltage for selectively operable load circuitry of a integrated circuit (col 2, ln 17-34), comprising: supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current (col 4, ln 52-67); receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path (col 7, ln 36-42); supplying, to said load circuitry via said pass transistor, a load current in response to said control signal (col 7, ln 22-29); and wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current (col 4, ln 52-67). Though not expressly disclosed by Wang, Luo discloses generating, at a first current path integrated in said integrated circuit, a substantially constant master current (col 5, ln 54-67); supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load (col 3, ln 13-17; col 4, ln 52 to col 5, ln 7). It would have been obvious to one skilled in the art to combine the voltage regulator features of Luo with the voltage regulator of Wang because Luo expressly discloses a dual current source network for feedback regulation of the voltage regulator having a master current and a second current that varies with the output voltage, a relation common to feedback regulated circuits, Wang's included.

Regarding claim 18, Wang discloses supplying said second current includes supplying a current based on a difference between a voltage at a gate of a feedback transistor of a feedback circuit and a voltage at said load circuitry (col 2, ln 35-47; col 3, ln 5-6).

Regarding claim 19, Wang discloses supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases (col 7, ln 22-29, ln 36-42).

(continued in next Supplemental Box)

Petitioner Micron Ex-1004, 0292

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:
Box V 2: Citations and explanations (continued)

Regarding claim 20, Wang discloses supplying said load current includes supplying a current with a magnitude of less than one amp, and wherein supplying first current and supplying said second current includes supplying a current with a magnitude of less than one milli-amp. These values are arbitrary and obvious in that other value relations between load current and second current pump magnitude are possible in similar voltage regulators and the application assigns no inventive significance to the claimed values.

Claims 2-4, 6, 9, 13 and 15 lack an inventive step under PCT Article 33(3) for being obvious over Wang in view of Luo and further in view of US 2008/0174289 A1 to GURCAN et al. (hereafter "Gurcan").

Regarding claim 2, Wang discloses a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit (col 2, ln 35-47; col 3, ln 5-11). Though not expressly disclosed in Wang, Gurcan discloses said second current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor (para [0046]-[0047]), and wherein said second current source is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor (para [0047]-[0048], [0050], [0056]). It would have been obvious to one skilled in the art to combine the features of Gurcan with the Wang/Luo regulator because the Gurcan disclosure describes a species of first and second current source transistor networks common to feedback controlled voltage regulator circuits.

Regarding claim 3, Gurcan discloses said replica transistor is an nmos transistor (para [0046]).

Regarding claim 4, Gurcan discloses said second current source is constructed to supply said second current based on K(Vgate - Vout - Vth)2, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant (para [0046]-[0050], [0056]). It would have been obvious to one skilled in the art to combine the disclosure of Gurcan with the Wang/Luo regulator references because the expressed voltage relation can be chosen from among other potential relations determined by the current network configuration and the application assigns no inventive significance to the formulation.

Regarding claim 6, Gurcan discloses said second current source is constructed to supply said second current based on K(Vout - Vgate - Vth)2, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant (para [0046]-[0050], [0056]). It would have been obvious to one skilled in the art to combine the disclosure of Gurcan with the Wang/Luo regulator references because the expressed voltage relation can be chosen from among other potential relations determined by the current network configuration and the application assigns no inventive significance to the formulation.

Regarding claim 9, Gurcan discloses said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path. It would have been obvious to one skilled in the art to combine the disclosure of Gurcan with the Wang/Luo regulator references because the expressed voltage relation can be chosen from among other potential relations determined by the current network configuration and the application assigns no inventive significance to the formulation.

Regarding claim 13, Wang discloses a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit (col 2, ln 35-47; col 3, ln 5-11). Though not expressly disclosed in Wang, Gurcan discloses said second current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor (para [0046]-[0047]), and wherein said second current source is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor (para [0047]-[0048], [0050], [0056]). It would have been obvious to one skilled in the art to combine the features of Gurcan with the Wang/Luo regulator because the Gurcan disclosure describes a species of first and second current source transistor networks common to feedback controlled voltage regulator circuits.

Regarding claim 15, Wang discloses a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit (col 2, ln 35-47; col 3, ln 5-11). Though not expressly disclosed in Wang, Gurcan discloses said second current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor (para [0046]-[0047]), and wherein said second current source is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor (para [0047]-[0048], [0050], [0056]). It would have been obvious to one skilled in the art to combine the features of Gurcan with the Wang/Luo regulator because the Gurcan disclosure describes a species of first and second current source transistor networks common to feedback controlled voltage regulator circuits.

(Continued in next Supplemental Box)

Petitioner Micron Ex-1004, 0293

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/IL 10/00377

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box V 2: Citations and explanations (continued)

Claim 12 lacks an inventive step under PCT Article 33(3) for being obvious over Wang in view of Luo and further in view of US 2007/0268008 A1 to GICQUEL et al. (hereafter "Gicquel").

Regarding claim 12, Wang discloses a voltage regulator circuit integrated in an integrated circuit (Ie) (col 2, ln 17-34; col 7, ln 12-14) and adapted to provide a voltage from a power supply to a load under varying load conditions (col 3, ln 56-60), comprising: said second input of said differential amplifier is coupled to said voltage divider such that a voltage at said second input is based on a voltage across said first end and said second end of said feedback transistor, wherein said gate of said feedback transistor is coupled to said output of said differential amplifier (col 4, ln 52 to col 5, ln 7); and wherein said differential amplifier, said feedback transistor, and said voltage divider are constructed and arranged such that a voltage at said gate of said feedback transistor is maintained at a substantially constant magnitude (col 6, ln 66 to col 7, ln 6); a pass device that includes a first end coupled to said positive node, a second end constructed to be coupled to said load at said output of said voltage regulator circuit, and a gate coupled to said second end of said second transistor of said current mirror and said first end of said current source, wherein said gate is adapted to receive a signal based on a magnitude of a current of said second current path (col 4, ln 35-51); wherein said current source is constructed to, if said second voltage reference increases in magnitude, cause a decrease said signal received at said gate of said pass device, and if said second voltage reference decreases in magnitude, cause an increase in a magnitude of said signal received at said gate of said pass device (col 7, ln 36-42); wherein said pass device is constructed to supply a load current to a load coupled to said output of said voltage regulator circuit with a magnitude based on said signal received at said gate of said pass device (col 4, ln 35-57); and wherein said current mirror, said feedback circuit, said current source, and said pass device are integrated in an integrated circuit (col 2, ln 17-34). Though not expressly disclosed in Wang, Gurcan discloses a voltage divider that includes a first end coupled to said second end of said first transistor of said current mirror and a second end coupled to said negative node (para [0037]); while Luo discloses an input adapted to receive a voltage from said power supply (col 5, ln 49-53), wherein said input includes a positive node and a negative node; an output adapted to be coupled to said load (col 5, ln 44-45); a current mirror that includes a first transistor coupled to a first current path that includes a gate constructed to receive a bias voltage and a first end coupled to said positive node (col 6, ln 16-28); a second transistor coupled to a second current path that includes a gate coupled to said gate of said first transistor (col 6, ln 16-28); and wherein said current mirror is operable to mirror a current of said first current path at said second current path (col 6, ln 16-28); a feedback circuit coupled to said first current path that includes: a differential amplifier that includes a first input, a second input, and an output, wherein said differential amplifier is adapted to provide, at said output, an output voltage based on a difference between a voltage at said first input and a voltage at said second input (col 5, ln 54-67), and wherein said first input is constructed to receive a reference voltage (col 5, ln 54-59); a feedback transistor that includes a gate, a first end, and a second end, wherein said first end is coupled to a second end of said first transistor of said current mirror, and wherein said second end is coupled to said negative node; a current source that includes a first end coupled to a second end of said second transistor of said current mirror and a second end coupled to said negative node, and wherein said current source is constructed to receive a first voltage reference based on a voltage at said gate of said feedback transistor and a second voltage reference based on a voltage at said output of said voltage regulator circuit and supply a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference (col 2, ln 47 to col 3, ln 12). It would have been obvious to combine the disclosures of Luo and Gurcan with Wang because Luo discloses a form of current source regulator network coupled to a power supply input and particulars of the transistor network that the current sources comprise, while Gurcan discloses the replica transistor feature within a voltage regulator control network as claimed in the application.

Claim 5 lacks an inventive step under PCT Article 33(3) for being obvious over Wang in view of Luo and Gurcan and further in view of Gicquel.

Regarding claim 5, Gicquel discloses said replica transistor is a pmos transistor (para [0040]). It would have been obvious to combine the Gicquel disclosure of a pmos replica transistor with the Wang/Luo/Gurcan regulator circuit because there are only two options for the mos form of transistor, nmos as claimed in a prior claim and pmos as claimed in the present claim, while the application assigns no inventive significance to this feature.

Claims 1-20 have industrial applicability under PCT Article 33(4) because their subject matter may be made and used in industry.

Petitioner Micron Ex-1004, 0294

SEQUENCE LISTINGS AND TABLES RELATED THERETO IN INTERNATIONAL APPLICATIONS FILED IN THE U.S. RECEIVING OFFICE

The Administrative Instructions (AIs) under the Patent Cooperation Treaty (PCT), in force as of **July 1, 2009**, contain important changes relating to the manner of filing, and applicable fees for, sequence listings and/or tables related thereto (sequence-related tables) in international applications. The complete text may be accessed at http://www.wipo.int/pct/en/texts/index.htm.

Effective July 1, 2009, Part 8 and Annex C-*bis* will no longer form part of the AIs. Part 8 was introduced in 2001 as a temporary solution to problems arising from the filing of very large sequence listings on paper and provided for a *sequence listing forming part of the international application* to be filed in electronic form on physical medium (*e.g.*, CD), together with the remainder of the application on paper. In 2002, Part 8 was expanded to include sequence-related tables and Annex C-*bis* was added to provide technical requirements. All applicants may now file complete international applications in electronic form, eliminating the need for these temporary provisions.

I. AIS PART 8 AND ANNEX C-*BIS DELETED AS OF JULY 1, 2009*

A) **Sequence-related tables cannot be filed as a separate part of the description or in text format.** They must be provided as an integral part of the international application either:
- in PDF format as part of an international application filed in electronic form via EFS-Web; or
- on paper as part of an international application filed on paper.

B) A ***sequence listing forming part of an international application*** may be provided either:
- in electronic form, as part of an international application filed in electronic form via EFS-Web, in
  - Annex C/ST.25 text format (preferred), or
  - PDF format; or
- on paper as part of an international application filed on paper.

C) A ***sequence listing not forming part of the international application*** **(for search under PCT Rule 13*ter*) in Annex C/ST.25 text format**
- is not required where the *sequence listing forming part of the international application* was filed in Annex C/ST.25 text format as part of an international application filed in electronic form via EFS-Web
- is required for search where the *sequence listing forming part of the international application* was filed in PDF
- is required for search on physical medium (*e.g.*, CD) where the *sequence listing forming part of the international application* was filed on paper as part of an international application filed on paper.

II. CALCULATION OF THE INTERNATIONAL FILING FEE AND FEE REDUCTION UNDER AI § 707

A) **A sequence-related table** must form an integral part of the international application and will incur FULL page fees with no upper limit.

B) A ***sequence listing forming part of an international application*** filed:
- via EFS-Web in Annex C/ST.25 text format will incur NO page fees;
- on paper or in PDF format will incur FULL page fees with no upper limit.

III. AVAILABILITY OF SEQUENCE LISTINGS SUBMITTED FOR SEARCH UNDER PCT RULE *13TER*

International Searching Authorities will be required to transmit to the International Bureau a copy of an Annex C/ST.25 text format sequence listing provided for search under PCT Rule 13*ter*. Any such sequence listing will be made available on PATENTSCOPE® (*sequence listings forming part of the international application* are already available).

IV. JULY 2009 REQUEST (PCT/RO/101)

The Request now has two options for the last sheet: one for paper filings; and one for EFS-Web filings. The July 2009 Request may be accessed at http://www.wipo.int/pct/en/forms/index.htm.

Petitioner Micron Ex-1004, 0295

NOTES TO FORM PCT/ISA/220

These Notes are intended to give the basic instructions concerning the filing of amendments under Article 19. The Notes are based on the requirements of the Patent Cooperation Treaty, the Regulations and the Administrative Instructions under that Treaty. In case of discrepancy between these Notes and those requirements, the latter are applicable. For more detailed information, see also the *PCT Applicant's Guide*.

In these Notes, "Article," "Rule" and "Section" refer to the provisions of the PCT, the PCT Regulations and the PCT Administrative Instructions, respectively.

INSTRUCTIONS CONCERNING AMENDMENTS UNDER ARTICLE 19

The applicant has, after having received the international search report and the written opinion of the International Searching Authority, one opportunity to amend the claims of the international application. It should however be emphasized that, since all parts of the international application (claims, description and drawings) may be amended during the international preliminary examination procedure, there is usually no need to file amendments of the claims under Article 19 except where, e.g. the applicant wants the latter to be published for the purposes of provisional protection or has another reason for amending the claims before international publication. Furthermore, it should be emphasized that provisional protection is available in some States only (see *PCT Applicant's Guide*, Annex B).

The attention of the applicant is drawn to the fact that amendments to the claims under Article 19 are not allowed where the International Searching Authority has declared, under Article 17(2), that no international search report would be established (see *PCT Applicant's Guide*, International Phase, paragraph 296).

What parts of the international application may be amended?

Under Article 19, only the claims may be amended.

During the international phase, the claims may also be amended (or further amended) under Article 34 before the International Preliminary Examining Authority. The description and drawings may only be amended under Article 34 before the International Preliminary Examining Authority.

Upon entry into the national phase, all parts of the international application may be amended under Article 28 or, where applicable, Article 41.

When? Within 2 months from the date of transmittal of the international search report or 16 months from the priority date, whichever time limit expires later. It should be noted, however, that the amendments will be considered as having been received on time if they are received by the International Bureau after the expiration of the applicable time limit but before the completion of the technical preparations for international publication (Rule 46.1).

Where not to file the amendments?

The amendments may only be filed with the International Bureau and not with the receiving Office or the International Searching Authority (Rule 46.2).

Where a demand for international preliminary examination has been/is filed, see below.

How? Either by cancelling one or more entire claims, by adding one or more new claims or by amending the text of one or more of the claims as filed.

A replacement sheet or sheets containing a complete set of claims in replacement of all the claims previously filed must be submitted.

Where a claim is cancelled, no renumbering of the other claims is required. In all cases where claims are renumbered, they must be renumbered consecutively in Arabic numerals (Section 205(a)).

The amendments must be made in the language in which the international application is to be published.

What documents must/may accompany the amendments?

Letter (Section 205(b)):

The amendments must be submitted with a letter.

The letter will not be published with the international application and the amended claims. It should not be confused with the "Statement under Article 19(1)" (see below, under "Statement under Article 19(1)").

The letter must be in English or French, at the choice of the applicant. However, if the language of the international application is English, the letter must be in English; if the language of the international application is French, the letter must be in French.

Petitioner Micron Ex-1004, 0296

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 4146.08US01

Tomer Shaul Elran Confirmation No.: 1327

Application No.: 12/464,301 Examiner: Jue Zhang

Filed: May 12, 2009 Group Art Unit: 2838

For: TRANSIENT LOAD VOLTAGE REGULATOR

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

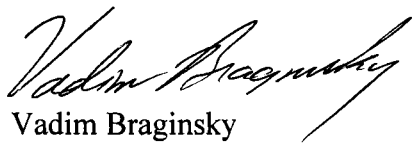
Sir:

Pursuant to 37 CFR § 1.56, and in addition to information disclosed in any prior Information Disclosure Statements filed, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached Form PTO-1449. It is respectfully requested that the information be expressly considered during the prosecution of the above-referenced application, and be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

The listing of a reference herein is not an admission that the reference is prior art or is material to patentability. 37 CFR § 1.97(h). Applicant reserves the right to establish the patentability of any claimed invention over any of the information provided herewith, and/or prove that this information may not be prior art, and/or prove that this information may not be enabling for any aspect of the information provided herewith.

This Information Disclosure Statement is being filed without a certification or fee because this Supplemental Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No certification or fee is required. 37 CFR § 1.97(b)(3).

Respectfully submitted,



Vadim Braginsky
Registration No. 58,031

Customer No. 24113
Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South 8th Street
Minneapolis, Minnesota 55402-2100
Telephone: 612.252.1542

Please grant any extension of time necessary for entry; charge any fee due to Deposit Account No. 16-0631.

Petitioner Micron Ex-1004, 0298

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 71045	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/IL 10/00377	International filing date *(day/month/year)* 12 May 2010 (12.05.2010)	(Earliest) Priority Date *(day/month/year)* 12 May 2009 (12.05.2009)
Applicant SANDISK IL LTD.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

   a. With regard to the **language**, the international search was carried out on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).

   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (see Box No. II).

3. ☐ **Unity of invention is lacking** (see Box No. III).

4. With regard to the **title**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

   ☒ the text is approved as submitted by the applicant.

   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

   a. the figure of the **drawings** to be published with the abstract is Figure No. 3

   ☐ as suggested by the applicant.

   ☐ as selected by this Authority, because the applicant failed to suggest a figure.

   ☒ as selected by this Authority, because this figure better characterizes the invention.

   b. ☐ none of the figures is to be published with the abstract.

Petitioner Micron Ex-1004, 0299

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IL 10/00377

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G05F 3/04 (2010.01)
USPC - 323/311
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
323/311

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
313/234, 265, 266, 304, 311, 313, 316, 371

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DB=PGPB,USPT,EPAB,JPAB; Google Scholar Terms: voltage regulator integrated feedback transistor constant current_source gate pass signal load_current increase magnitude decrease IC replica_transistor difference nmos pmos stability_capacitor load_current second_current_path load near2 amp milliamp current_mirror differential

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 7,446,515 B2 (WANG) 04 November 2008 (04.11.2008) entire document, especially (col 2, ln 17-53; col 3, ln 5-6; ln 37-60; col 4, ln 35-50; col 4, ln 52 to col 5, ln 7; col 6, ln 58-59; col 6, ln 66 to col 7, ln 6; col 7, ln 12-14, ln 22-29; ln 36-42, ln 50-57)	1-20
Y	US 7,352,210 B2 (LUO) 01 April 2008 (01.04.2008) entire document, especially (col 3, ln 13-17; col 5, ln 44-45; col 6, ln 58-59)	1-20
Y	US 2008/0174289 A1 (GURCAN et al.) 24 July 2008 (24.07.2008) entire document, especially (para [0046]-[0048], [0050], [0056])	2-6, 9, 13, 15
Y	US 2007/0268008 A1 (GICQUEL et al.) 22 November 2007 (22.11.2007) entire document, especially (para [0040])	5, 12

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 August 2010 (19.08.2010)	03 SEP 2010
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

Petitioner Micron Ex-1004, 0300

Electronic Acknowledgement Receipt

EFS ID:	9122522
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Vadim Braginsky/Timothy Douma
Filer Authorized By:	Vadim Braginsky
Attorney Docket Number:	4146.08US01
Receipt Date:	28-DEC-2010
Filing Date:	12-MAY-2009
Time Stamp:	12:07:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal Letter	Supplemental_IDS.PDF	56559 398459e956d0115093485de5f8d1b8d69f843167	no	2

Warnings:	
Information:	

2	Information Disclosure Statement (IDS) Filed (SB/08)	1449_IDS.PDF	107088 d8712221c7e85e39c38c2e9450acdef27a4b9b03	no	2
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
3	NPL Documents	IDS_Ref_1.PDF	128651 beb93bee6d124f32a55a08aa3f732adfe5507b26	no	2
Warnings:					
Information:					
4	NPL Documents	IDS_Ref_2.PDF	95779 2dde80fced429cbe0cb70e6732a20c270d441df3	no	2
Warnings:					
Information:					
5	NPL Documents	IDS_Ref_3.PDF	518051 3338272d8e9b4e87e3490e319f07ccdf0931c577	no	8
Warnings:					
Information:					
		Total Files Size (in bytes):	906128		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	12/464,301
Filing Date	May 12, 2009
First Named Inventor	Tomer Shaul Elran
Art Unit	2838
Examiner Name	Jue Zhang
Attorney Docket Number	4146.08US01

Sheet	1	of	2

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/J.Z./		US-7,352,210	04-01-2008	Luo
/J.Z./		US-2008/0174289	07-24-2008	Gurcan, et al.
/J.Z./		US-2007/0268008	11-22-2007	Gicquel, et al.
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Complete if Known	
Application Number	12/464,301
Filing Date	May 12, 2009
First Named Inventor	Tomer Shaul Elran
Art Unit	2838
Examiner Name	Jue Zhang
Attorney Docket Number	4146.08US01

Sheet	2	of	2

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
/J.Z./		Notification of Transmittal of the International Search Report and the Written Opinion of the International Searching Authority, or the Declaration (PCT Rule 44.1) Mailing Date of September 3, 2010	
/J.Z./		International Search Report for International Application No. PCT/IL 10/00377 Dated May 12, 2010	
/J.Z./		Written Opinion of the International Searching Authority for International Application No. PCT/IL 10/00377 Dated May 12, 2010	

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z

Notice of References Cited	Application/Control No. 12/464,301	Applicant(s)/Patent Under Reexamination ELRAN, TOMER SHAUL	
	Examiner JUE ZHANG	Art Unit 2838	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-2008/0174289	07-2008	Gurcan et al.	323/280
*	B	US-7,352,210	04-2008	Luo, Wenzhe	323/311
*	C	US-7,095,272	08-2006	Morishita, Fukashi	323/316
*	D	US-5,982,226	11-1999	Rincon-Mora, Gabriel A.	323/273
*	E	US-5,909,109	06-1999	Phillips, Timothy A.	323/277
*	F	US-5,864,227	01-1999	Borden et al.	323/280
*	G	US-7,218,082	05-2007	Walter et al.	323/273
*	H	US-6,201,375	03-2001	Larson et al.	323/277
*	I	US-6,285,246	09-2001	Basu, Sudip	323/316
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Petitioner Micron Ex-1004, 0305

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

87955 7590 08/16/2011

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
08/16/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	12/464,301	ELRAN, TOMER SHAUL	
	Examiner	Art Unit	
	JUE ZHANG	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *12 May 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13-17* is/are allowed.

6)☒ Claim(s) *1-12, 18-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 July 2009* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *5/12/2009 and 12/28/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Petitioner Micron Ex-1004, 0307

DETAILED ACTION

1. This office action is in response to the application filed on 5/12/2009. Claims 1-20 are pending.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification. The entire disclosure, i.e., specification, abstracts and claims should be revised carefully. For example: Claims 1-7 recite "said second current source", there is insufficient antecedent basis for this limitation in the claims. Claim 12 recites "a gate constructed to receive a bias voltage…", "a gate coupled to said gate of said first transistor …", "a gate coupled to said second end of said second transistor … ", and further recites "said gate" in 1st Para of page 8. It is not clear which gate is referring to.

Applicant is reminded to use consistent language throughout the disclosure in order to facilitate finding support for the recited limitations, as well as to provide proper antecedence for all claimed limitations.

Drawing

2. The drawing submitted on 7/28/2009 is acknowledged and accepted by the examiner.

Information Disclosure Statement

3. The information disclosure statements (IDS) submitted on 5/12/2009 and 12/28/2010 have been considered by the examiner.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-12, 18-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-7 recite “said second current source”, there is insufficient antecedent basis for this limitation in the claims.

Claim 12 recites “a gate constructed to receive a bias voltage…”, “a gate coupled to said gate of said first transistor …”, “a gate coupled to said second end of said second transistor … “, and further recites “said gate” in 1st Para of page 8. It is not clear which gate is referring to.

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jue Zhang whose telephone number is (571) 270-1263.

The examiner can normally be reached on M-TH 8:00-5:00PM EST, Other F 8:00AM-4:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jue Zhang/
Primary Examiner, Art Unit 2838
August 14, 2011

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

BIB DATA SHEET

CONFIRMATION NO. 1327

SERIAL NUMBER	FILING or 371(c) DATE RULE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
12/464,301	05/12/2009	323	2838	4146.08US01

APPLICANTS
Tomer Shaul Elran, Petah Tikva, ISRAEL;

**** CONTINUING DATA ***************************

**** FOREIGN APPLICATIONS ***************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****
05/19/2009

Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /JUE ZHANG/ Examiner's Signature	☐ Met after Allowance Initials	STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
		ISRAEL	8	20	5

ADDRESS

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402
UNITED STATES

TITLE

TRANSIENT LOAD VOLTAGE REGULATOR

FILING FEE RECEIVED		
1530	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

BIB (Rev. 05/07).

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12464301	ELRAN, TOMER SHAUL
	Examiner	Art Unit
	JUE ZHANG	2838

SEARCHED			
Class	Subclass	Date	Examiner
323	267-280,311-316	8/14/2011	JZ
327	538,540,541	8/14/2011	JZ

SEARCH NOTES		
Search Notes	Date	Examiner
See east search notes.	8/14/2011	JZ
Inventor name search	8/14/2011	JZ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

Substitute for form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT
(Use as many sheets as necessary)

Complete if Known	
Application Number	*Unknown*
Filing Date	Herewith
First Named Inventor	Elran
Art Unit	*Unknown*
Examiner Name	*Unknown*
Attorney Docket Number	4146.08US01

Sheet	1	of	5

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/J.Z./		US-2009/0033298	02-05-2009	Kleveland
		US-7,482,791	01-27-2009	Stoichita
		US-2008/0180080	07-31-2008	Terry
		US-7,091,709	08-15-2006	Suzuki
		US-6,653,891	11-25-2003	Hazucha
		US-6,573,694	06-03-2003	Pulkin
		US-6,304,131	10-16-2001	Huggins
		US-6,188,211	02-13-2001	Rincon-Mora
		US-6,140,805	10-31-2000	Kaneko
		US-6,058,488	05-02-2000	Eckhardt
		US-5,867,015	02-02-1999	Corsi
		US-5,519,656	05-21-1996	Maccarrone
		US-2003/0001550	01-02-2003	Pulkin
		US-2007/0164810	07-19-2007	Chen
		US-2007/0109052	05-17-2007	Franck
		US-2006/0220730	10-05-2006	Lobb
		US-2005/0225380	10-13-2005	Ingino
		US-2005/0134383	06-23-2005	Franck
		US-2005/0088205	04-28-2005	Jalaleddine

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]
/J.Z./		EP 1622067 B1	02-27-2008	Takabayashi	
		EP 0851332 B1	02-25-2004	Corsi	
		EP 0957421 B1	09-03-2003	Rincon-Mora	
		EP 0783796	07-16-1997	Tran	
		WO 9705696	02-13-1997	Tran	
		WO 9305572	03-18-1993	Molnar	

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z~~

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	2	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/J.Z./		US-2004/0095701	05-20-2004	Ingino
		US-2004/0057169	03-25-2004	Amick
		US-2004/0056700	03-25-2004	Amick
		US-2003/0197492	10-23-2003	Kalpakjian
		US-2003/0155964	08-21-2003	Gauthier
		US-2003/0137341	07-24-2003	LeChevalier
		US-2002/0149398	10-17-2002	Ingino
		US-2002/0005710	01-17-2002	Kalpakjian
		US-7,394,306	07-01-2008	Chen
		US-7,368,994	05-06-2008	Franck
		US-7,173,482	02-06-2007	Lobb
		US-7,151,410	12-19-2006	Franck
		US-7,132,880	11-07-2006	Ingino
		US-6,924,674	08-02-2005	Jalaleddine
		US-6,914,476	07-05-2005	Ingino
		US-6,873,503	03-29-2005	Amick
		US-6,847,198	01-25-2005	Kalpakjian
		US-6,828,850	12-07-2004	LeChevalier
		US-6,809,557	10-26-2004	Gauthier

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]
/J.Z./		WO 2004/027995 A3	04-01-2004	Amick	
		EP 1229419 A3	08-04-2004	Ingino	
		EP 0661717 B1	03-29-2000	Maccarrone	
		EP 0602163 B1	01-08-1997	Molnar	
		EP 0497591 B1	04-02-1997	Bjorkman	

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z~~

Substitute for form 1449/PTO				Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	3	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/J.Z./		US-6,734,716	05-11-2004	Amick
		US-6,621,675	09-16-2003	Ingino
		US-6,586,916	07-01-2003	Kalpakjian
		US-6,331,766	12-18-2001	Kalpakjian
		US-6,285,614	09-04-2001	Mulatti
		US-6,175,221	01-16-2001	Kalpakjian
		US-6,118,266	09-12-2000	Manohar
		US-6,101,118	08-08-2000	Mulatti
		US-5,905,399	05-18-1999	Bosnyak
		US-5,739,681	04-14-1998	Allman
		US-5,675,241	10-07-1997	Teggatz
		US-5,631,606	05-20-1997	Tran
		US-5,512,814	04-30-1996	Allman
		US-5,428,316	06-27-1995	Molnar
		US-5,296,800	03-22-1994	Bjorkman
		US-5,202,587	04-13-1993	McLaury
		US-5,162,668	11-10-1992	Chen
		US-4,536,699	08-20-1985	Baker
		US-4,498,058	02-05-1985	Benrud

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.Z

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	4	of	5	Attorney Docket Number	4146.08US01

U.S. PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Document Number Number-Kind Code[2] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document
/J.Z./		US-4,446,383	05-01-1984	Concannon
		US-6,809,504	10-26-2004	Tang
		US-6,975,494	12-13-2005	Tang
		US-7,319,314	01-15-2008	Maheshwari
		US-7,446,515	11-04-2008	Wang
		US-7,218,082	05-15-2007	Walter
		US-7,323,853	01-29-2008	Tang
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		
		US-		

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] *(if known)*	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	T[6]

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]Applicant's unique citation designation number (optional). [2]See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 901.04. [3]Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). [4]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [5]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. [6]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.~~ /J.Z

Substitute for form 1449/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT *(Use as many sheets as necessary)*				*Complete if Known*	
				Application Number	*Unknown*
				Filing Date	Herewith
				First Named Inventor	Elran
				Art Unit	*Unknown*
				Examiner Name	*Unknown*
Sheet	5	of	5	Attorney Docket Number	4146.08US01

NON PATENT LITERATURE DOCUMENTS

EXAMINER INITIAL*	Cite No.[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
/J.Z./		HAZUCHA et al., "Area-Efficient Linear Regulator With Ultra-Fast Load Regulation", IEEE Journal of Solid State Circuits, Vol. 40. No.4, April 2005. pp. 933-940.	
/J.Z./		HAZUCHA et al., "An Area-Efficient, Integrated, Linear Regulator with Ultra-Fast Load Regulation", Symposium On VLSI Circuits Digest of Technical Papers. 2004. pp. 218-221.	

EXAMINER SIGNATURE	/Jue Zhang/	DATE CONSIDERED	08/14/2011

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. [1]Applicant's unique citation designation number (optional). [2]Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 120 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450 Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 (1-800-786-9199) and select option 2.

~~ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH.~~ /J.Z

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L3	4137	323/311-316.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 14:24
L4	65	differential adj amplifier (current near source and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:27
L5	1	3 4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:27
L6	36693	"323"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 14:28
L7	3	4 6	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:28
L8	1454	differential adj amplifier (current near source and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:28
L9	70	3 8	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:28
L10	1496	differential adj amplifier (current near (source or path) and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:30
L11	65	differential adj amplifier (current near (source or path) and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:30

Petitioner Micron Ex-1004, 0318

EAST Search History (Prior Art)

L12	69	differential adj amplifier (current near (source or path or mirror) and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:32
L13	1602	differential adj amplifier (current near (source or path or mirror) and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:33
L14	201	6 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:33
L15	123	(("20090033298") or ("7,482,791") or ("20080180080") or ("7,091,709") or ("6,653,891") or ("6,573,694") or ("6,304,131") or ("6,188,211") or ("6,140,805") or ("6,058,488") or ("5,867,015") or ("5,519,656") or ("20030001550") or ("20070164810") or ("20070109052") or ("20060220730") or ("20050225380") or ("20050134383") or ("20050088205") or ("20040095701") or ("20040057169") or ("20040056700") or ("20030197492") or ("20030155964") or ("20030137341") or ("20020149398") or ("20020005710") or ("7,394,306") or ("7,368,994") or ("7,173,482") or ("7,151,410") or ("7,132,880") or ("6,924,674") or ("6,914,476") or ("6,873,503") or ("6,847,198") or ("6,828,850") or ("6,809,557") or ("6,734,716") or ("6,621,675") or ("6,586,916") or ("6,331,766") or ("6,285,614") or ("6,175,221") or ("6,734,716") or ("6,621,675") or ("6,586,916") or ("6,331,766") or ("6,285,614") or ("6,175,221") or ("6,118,266") or ("6,101,118") or ("5,905,399") or ("5,739,681") or ("5,675,241") or ("5,631,606") or ("5,512,814") or ("5,428,316") or ("5,296,800") or ("5,202,587") or ("5,162,668") or ("4,536,699") or ("4,498,058") or ("4,446,383") or ("6,809,504") or ("6,975,494") or ("7,319,314") or ("7,446,515") or ("7,218,082") or ("7,323,853") or ("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/08/14 14:53
L16	4704	323/267-280.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 14:56

Petitioner Micron Ex-1004, 0319

EAST Search History (Prior Art)

L17	63	16 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:56
L18	4347	327/536,540,546,548.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 14:58
L19	28	18 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 14:58
L20	3	("5982226" | "6861827" | "7015680").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/08/14 15:01
L21	10	("5412309" | "5490005" | "5563501" | "5631598" | "5682093" | "5686820" | "5850139" | "5864227" | "5867015" | "5909109").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/08/14 15:02
L22	25	("5982226").URPN.	USPAT	OR	ON	2011/08/14 15:04
L23	2040	327/538.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 15:09
L24	20	23 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 15:09
L25	1206	327/541.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/14 15:27
L26	36	25 13	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/08/14 15:27
S1	6	(("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/07/30 12:57
S2	3	((TOMER) near2 (ELRAN)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2011/07/30 12:58

Petitioner Micron Ex-1004, 0320

EAST Search History (Prior Art)

S3	8	(("7446515") or ("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/07/30 13:52
S4	329	323/311.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/08/04 15:18
S5	37	(("7,091,709") or ("6,653,891") or ("6,573,694") or ("6,304,131") or ("6,188,211") or ("6,140,805") or ("6,058,488") or ("5,867,015") or ("5,519,656") or ("20030001550") or ("20070164810") or ("20070109052") or ("20060220730") or ("20050225380") or ("20050134383") or ("20050088205") or ("20090033298") or ("7,482,791") or ("20080180080")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/08/04 15:24

EAST Search History (Interference)

		<This search history is empty>				

Petitioner Micron Ex-1004, 0321

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	☐ To be Mailed
12/464,301	05/12/2009	

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY ☐ FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 11/16/2011	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	X $ =		OR	X $60=	0
Independent (37 CFR 1.16(h))	* 5	Minus	***5	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0

AMENDMENT	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)		RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/KAREN VESTAL/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

REMARKS

Claims 1-20 are pending. By this Amendment, claims 1-2, 4, 6-7, 12-13, and 18-20 are amended to make clarifications of antecedent basis and to correct various typographical errors. This amendment makes no changes to the scope of the claims.

Claim rejections under 35 U.S.C. § 112

Claims 1-12 and 18-20 were rejected under 35 U.S.C. § 112, second paragraph, for various ambiguities due to lack of antecedent basis, as indicated in the Office Action. By this Amendment, all causes for the § 112 rejection are believed to be resolved. For instance, in claim 1 and the claims depending therefrom, the term "current source" is corrected to be "current supply circuit," which is now consistent with the antecedent basis for the term. In claim 12, the ambiguous term "said gate" is now clarified to state "said gate of said pass device." Unambiguous support for this clarified term is found in FIG. 6 and its associated description in the specification. Claims 18-20 are corrected to properly depend from claim 17.

Withdrawal of the § 112 rejection is respectfully requested.

In view of the foregoing, it is submitted that this application is in condition for allowance. Favorable consideration and prompt allowance of the application are respectfully requested.

Petitioner Micron Ex-1004, 0323

The Examiner is invited to telephone the undersigned if the Examiner believes it would be useful to advance prosecution.

Respectfully submitted,



Vadim Braginsky
Registration No. 58031

Customer No. 87955
Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South 8th Street
Minneapolis, Minnesota 55402-2100
Telephone: 612.252.1542

Petitioner Micron Ex-1004, 0324

AMENDMENTS TO THE CLAIMS

A detailed listing of all claims that are, or were, in the present application, irrespective of whether the claim(s) remain(s) under examination in the application is presented below. The claims are presented in ascending order and each includes one status identifier. Those claims not cancelled or withdrawn but amended by the current amendment utilize the following notations for amendment: 1. deleted matter is shown by strikethrough for six or more characters and double brackets for five or fewer characters; and 2. added matter is shown by underlining.

Petitioner Micron Ex-1004, 0325

1. (Currently Amended) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a feedback circuit coupled to a first current path and including a feedback transistor, wherein said feedback circuit is constructed to maintain a voltage at a gate of said feedback transistor substantially constant;

a first current supply circuit constructed to supply to a second current path a first current that is substantially constant;

a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit;

a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal;

wherein said second current supply circuit ~~source~~ is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases; and

Petitioner Micron Ex-1004, 0326

wherein said feedback circuit, said first current supply circuit, said second current supply circuit, and said pass device are integrated in an integrated circuit and referenced to said input of said voltage regulator circuit.

2. (Currently Amended) The voltage regulator circuit of claim 1, wherein said second current supply circuit ~~source~~ includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current supply circuit ~~source~~ is adapted to supply said second current with a magnitude based on said voltage at said gate of said replica transistor.

3. (Original) The voltage regulator circuit of claim 2, wherein said replica transistor is an nmos transistor.

4. (Currently Amended) The voltage regulator circuit of claim 2, wherein said second current supply circuit ~~source~~ is constructed to supply said second current based on $K(Vgate - Vout - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

Petitioner Micron Ex-1004, 0327

5. (Original) The voltage regulator circuit of claim 2, wherein said replica transistor is a pmos transistor.

6. (Currently Amended) The voltage regulator circuit of claim 2, wherein said second current supply circuit ~~source~~ is constructed to supply said second current based on $K(Vout - Vgate - Vth)^2$, wherein Vout is said voltage at said output of said voltage regulator circuit, Vgate is said voltage at said gate of said feedback transistor, and Vth is a threshold voltage of said replica transistor, and K is a positive constant.

7. (Currently Amended) The voltage regulator circuit of claim 1, wherein said second current supply circuit ~~source~~ further comprises at least one stability capacitor arrangement.

8. (Original) The voltage regulator circuit of claim 8, wherein said at least one stability capacitor arrangement has a capacitance of less than 30 pico-farads.

9. (Original) The voltage regulator of claim 1, wherein said load current has a magnitude that is at least one order of magnitude greater than a magnitude of a current of said second current path.

10. (Original) The voltage regulator of claim 1, wherein said load current has a magnitude of less than one amp, and wherein said current of said second current path has a magnitude of less than one milli-amp.

Petitioner Micron Ex-1004, 0328

11. (Original) The voltage regulator of claim 1, wherein said signal received at said pass device gate is a voltage.

12. (Currently Amended) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions, comprising:

an input adapted to receive a voltage from said power supply, wherein said input includes a positive node and a negative node;

an output adapted to be coupled to said load;

a current mirror that includes

a first transistor coupled to a first current path that includes a gate constructed to receive a bias voltage and a first end coupled to said positive node;

a second transistor coupled to a second current path that includes a gate coupled to said gate of said first transistor; and

wherein said current mirror is operable to mirror a current of said first current path at said second current path;

a feedback circuit coupled to said first current path that includes:

a differential amplifier that includes a first input, a second input, and an output, wherein said differential amplifier is adapted to provide, at said output, an output voltage based on a difference between a voltage at said first input and a voltage at said second input, and wherein said first input is constructed to receive a reference voltage;

Petitioner Micron Ex-1004, 0329

a feedback transistor that includes a gate, a first end, and a second end, wherein said first end is coupled to a second end of said first transistor of said current mirror, and wherein said second end is coupled to said negative node;

a voltage divider that includes a first end coupled to said second end of said first transistor of said current mirror and a second end coupled to said negative node;

wherein said second input of said differential amplifier is coupled to said voltage divider such that a voltage at said second input is based on a voltage across said first end and said second end of said feedback transistor, wherein said gate of said feedback transistor is coupled to said output of said differential amplifier; and

wherein said differential amplifier, said feedback transistor, and said voltage divider are constructed and arranged such that a voltage at said gate of said feedback transistor is maintained at a substantially constant magnitude;

a current source that includes a first end coupled to a second end of said second transistor of said current mirror and a second end coupled to said negative node, and wherein said current source is constructed to receive a first voltage reference based on a voltage at said gate of said feedback transistor and a second voltage reference based on a voltage at said output of said voltage regulator circuit and supply a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;

a pass device that includes a first end coupled to said positive node, a second end constructed to be coupled to said load at said output of said voltage regulator circuit, and a gate coupled to said second end of said second transistor of said current mirror and said first end of

Petitioner Micron Ex-1004, 0330

said current source, wherein said gate of said pass device is adapted to receive a signal based on a magnitude of a current of said second current path;

wherein said current source is constructed to, if said second voltage reference increases in magnitude, cause a decrease said signal received at said gate of said pass device, and if said second voltage reference decreases in magnitude, cause an increase in a magnitude of said signal received at said gate of said pass device;

wherein said pass device is constructed to supply a load current to a load coupled to said output of said voltage regulator circuit with a magnitude based on said signal received at said gate of said pass device; and

wherein said current mirror, said feedback circuit, said current source, and said pass device are integrated in an integrated circuit.

13. (Currently Amended) The voltage regulator circuit of claim 12~~claim 16~~, wherein said current source includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and said output of said voltage regulator circuit, and wherein said current source is adapted to supply a current with a magnitude based on said signal received at said gate of said replica transistor.

14. (Original) A voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load conditions, comprising:

Petitioner Micron Ex-1004, 0331

an input adapted to receive a voltage from said power supply;

an output adapted to be coupled to said load;

a first current path referenced to said input;

feedback means for maintaining a voltage at a gate of a feedback transistor substantially constant;

first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant;

second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference;

means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal;

wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage said load increases, a magnitude of said load current is decreased; and

wherein said feedback means, said first current supply means, said second current supply means, and said means for supplying current to said load are integrated in an integrated circuit.

Petitioner Micron Ex-1004, 0332

15. (Original) The voltage regulator circuit of claim 14, wherein said second current supply means includes a replica transistor that includes a gate coupled to said gate of said feedback transistor, wherein a voltage at said gate of said replica transistor is based on a difference between a voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit, and wherein said second current supply means are for supplying said second current with a magnitude based on said voltage at said gate of said replica transistor.

16. (Original) A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

receiving, from a power supply, a power supply voltage;

supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current;

receiving, at a feedback transistor integrated in said integrated circuit, said master current;

maintaining, via a feedback circuit integrated in said integrated circuit and coupled to said feedback transistor, a voltage at a gate of said feedback transistor substantially constant;

supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude;

supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load;

Petitioner Micron Ex-1004, 0333

receiving, at a gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path; and

supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.

17. (Original) A method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit, comprising:

generating, at a first current path integrated in said integrated circuit, a substantially constant master current;

supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current;

supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load;

receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path;

supplying, to said load circuitry via said pass transistor, a load current in response to said control signal; and

Petitioner Micron Ex-1004, 0334

wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current.

18. (Currently Amended) The method of claim 17~~claim 8~~, wherein supplying said second current includes supplying a current based on a difference between a voltage at a gate of a feedback transistor of a feedback circuit and a voltage at said load circuitry.

19. (Currently Amended) The method of claim 17~~claim 1~~, wherein supplying, to said load circuitry via said pass transistor, a load current includes increasing a magnitude of said load current if a voltage at said output decreases, and decreasing a magnitude of said load current if a voltage at said output increases.

20. (Currently Amended) The method of claim 17~~claim 11~~, wherein supplying said load current includes supplying a current with a magnitude of less than one amp, and wherein supplying first current and supplying said second current includes supplying a current with a magnitude of less than one milli-amp.

Petitioner Micron Ex-1004, 0335

Electronic Acknowledgement Receipt

EFS ID:	11424503
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Vadim Braginsky/Ralynn Thompson
Filer Authorized By:	Vadim Braginsky
Attorney Docket Number:	4146.08US01
Receipt Date:	16-NOV-2011
Filing Date:	12-MAY-2009
Time Stamp:	18:13:13
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		4146_08US01.PDF	452663 43d4953b3e4c9e1b6959239bbae36a71c47db77c	yes	14

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	12
	Applicant Arguments/Remarks Made in an Amendment	13	14
Warnings:			
Information:			
	Total Files Size (in bytes):	452663	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the application of: Attorney Docket No.: 4146.08US01

Elran Confirmation No.: 1327

Application No.: 12/464,301 Examiner: Jue Zhang

Filed: May 12, 2009 Group Art Unit: 2838

For: TRANSIENT LOAD VOLTAGE REGULATOR

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

INTRODUCTORY COMMENTS

In response to the Office Action of August 16, 2011, amendment to the above-identified patent application is requested.

The present amendment comprises the following sections:

A. Amendments to the Claims

B. Remarks

Please grant any extension of time necessary for entry; charge any fee due to Deposit Account No. 16-0631.

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12464301	ELRAN, TOMER SHAUL
	Examiner	Art Unit
	JUE ZHANG	2838

SEARCHED			
Class	Subclass	Date	Examiner
323	267-280,311-316	8/14/2011	JZ
327	538,540,541	8/14/2011	JZ
	above search updated	11/22/2011	JZ
323	281	11/22/2011	JZ

SEARCH NOTES		
Search Notes	Date	Examiner
See east search notes.	8/14/2011	JZ
Inventor name search	8/14/2011	JZ
East search updated	11/22/2011	JZ

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
	See east search in claim context	11/22/2011	JZ

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	12464301	ELRAN, TOMER SHAUL
	Examiner	**Art Unit**
	JUE ZHANG	2838

ORIGINAL		INTERNATIONAL CLASSIFICATION	
CLASS	SUBCLASS	CLAIMED	NON-CLAIMED
323	281	G 0 5 F 1 / 00 (2006.01)	

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				

☒ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		17												
	2		18												
	3		19												
	4		20												
	5														
	6														
	7														
	8														
	9														
	10														
	11														
	12														
	13														
	14														
	15														
	16														

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	20	
/JUE ZHANG/ Primary Examiner.Art Unit 2838	11/22/2011	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	5

Petitioner Micron Ex-1004, 0340

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	425	323/281.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:48
L2	1470	differential adj amplifier (current near source and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:49
L3	7	1 L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:49
L4	1621	differential adj amplifier (current near (source or path or mirror) and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:49
L5	8	1 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:49
L9	3	((TOMER) near2 (ELRAN)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2011/11/22 20:57
L10	6	(("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/11/22 20:57
L11	3	((TOMER) near2 (ELRAN)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2011/11/22 20:57
L12	8	(("7446515") or ("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/11/22 20:57
L13	356	323/311.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57

Petitioner Micron Ex-1004, 0341

EAST Search History (Prior Art)

L14	37	(("7,091,709") or ("6,653,891") or ("6,573,694") or ("6,304,131") or ("6,188,211") or ("6,140,805") or ("6,058,488") or ("5,867,015") or ("5,519,656") or ("20030001550") or ("20070164810") or ("20070109052") or ("20060220730") or ("20050225380") or ("20050134383") or ("20050088205") or ("20090033298") or ("7,482,791") or ("20080180080")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/11/22 20:57
L15	4215	323/311-316.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L16	65	differential adj amplifier (current near source and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L17	1	L15 L16	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L18	37213	"323"/$.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L19	3	L16 L18	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L20	1470	differential adj amplifier (current near source and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L21	70	L15 L2	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L22	1512	differential adj amplifier (current near (source or path) and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57

Petitioner Micron Ex-1004, 0342

EAST Search History (Prior Art)

L23	65	differential adj amplifier (current near (source or path) and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L24	69	differential adj amplifier (current near (source or path or mirror) and feedback) near constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L25	1621	differential adj amplifier (current near (source or path or mirror) and feedback) with constant	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L26	203	L18 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L27	123	(("20090033298") or ("7,482,791") or ("20080180080") or ("7,091,709") or ("6,653,891") or ("6,573,694") or ("6,304,131") or ("6,188,211") or ("6,140,805") or ("6,058,488") or ("5,867,015") or ("5,519,656") or ("20030001550") or ("20070164810") or ("20070109052") or ("20060220730") or ("20050225380") or ("20050134383") or ("20050088205") or ("20040095701") or ("20040057169") or ("20040056700") or ("20030197492") or ("20030155964") or ("20030137341") or ("20020149398") or ("20020005710") or ("7,394,306") or ("7,368,994") or ("7,173,482") or ("7,151,410") or ("7,132,880") or ("6,924,674") or ("6,914,476") or ("6,873,503") or ("6,847,198") or ("6,828,850") or ("6,809,557") or ("6,734,716") or ("6,621,675") or ("6,586,916") or ("6,331,766") or ("6,285,614") or ("6,175,221") or ("6,734,716") or ("6,621,675") or ("6,586,916") or ("6,331,766") or ("6,285,614") or ("6,175,221") or ("6,118,266") or ("6,101,118") or ("5,905,399") or ("5,739,681") or ("5,675,241") or ("5,631,606") or ("5,512,814") or ("5,428,316") or ("5,296,800") or ("5,202,587") or ("5,162,668") or ("4,536,699") or ("4,498,058") or ("4,446,383") or ("6,809,504") or ("6,975,494") or ("7,319,314") or ("7,446,515") or ("7,218,082") or ("7,323,853") or ("7,352,210") or ("20080174289") or ("20070268008")).PN.	US-PGPUB; USPAT; USOCR; JPO; DERWENT	OR	OFF	2011/11/22 20:57

Petitioner Micron Ex-1004, 0343

EAST Search History (Prior Art)

L28	4808	323/267-280.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L29	63	L28 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L30	4435	327/536,540,546,548.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L31	28	L30 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L32	3	("5982226" | "6861827" | "7015680").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/11/22 20:57
L33	10	("5412309" | "5490005" | "5563501" | "5631598" | "5682093" | "5686820" | "5850139" | "5864227" | "5867015" | "5909109").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2011/11/22 20:57
L34	25	("5982226").URPN.	USPAT	OR	ON	2011/11/22 20:57
L35	2076	327/538.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L36	20	L35 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57
L37	1215	327/541.ccls.	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	OR	ON	2011/11/22 20:57
L38	36	L37 L4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT	AND	ON	2011/11/22 20:57

Petitioner Micron Ex-1004, 0344

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L6	1	323/281	UPAD	OR	ON	2011/11/22 20:50
L7	46	323/281	US-PGPUB	OR	ON	2011/11/22 20:50
L8	1105	323/281	USPAT	OR	ON	2011/11/22 20:51

Petitioner Micron Ex-1004, 0345

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

87955 7590 11/29/2011

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

EXAMINER	
ZHANG, JUE	
ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 11/29/2011

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

TITLE OF INVENTION: TRANSIENT LOAD VOLTAGE REGULATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	02/29/2012

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

Petitioner Micron Ex-1004, 0346

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

87955 7590 11/29/2011

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

TITLE OF INVENTION: TRANSIENT LOAD VOLTAGE REGULATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	02/29/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZHANG, JUE	2838	323-281000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:

❑ Issue Fee

❑ Publication Fee (No small entity discount permitted)

❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**

❑ A check is enclosed.

❑ Payment by credit card. Form PTO-2038 is attached.

❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

❑ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.

❑ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Petitioner Micron Ex-1004, 0347

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

87955 7590 11/29/2011

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

DATE MAILED: 11/29/2011

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 400 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 400 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Petitioner Micron Ex-1004, 0348

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No.	Applicant(s)	
	12/464,301	ELRAN, TOMER SHAUL	
	Examiner	Art Unit	
	JUE ZHANG	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/16/2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-20*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Jue Zhang/
Primary Examiner, Art Unit 2838
November 22, 2011

Petitioner Micron Ex-1004, 0350

REASONS FOR ALLOWANCE

1. Claims 1-20 are allowed.

2. The following is an examiner's statement of reasons for the indication of allowable subject matters:

For claim 1, None of the prior art alone or in combination discloses voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions having: … a first current supply circuit constructed to supply to a second current path a first current that is substantially constant; a second current supply circuit coupled to said first current supply circuit, said gate of said feedback transistor, and said output of said voltage regulator circuit and constructed to supply a second current to said second current path with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said output of said voltage regulator circuit; a pass device including a gate coupled to said second current path and adapted to receive a signal based on said current of said second current path and supply a load current to said load via said output of said voltage regulator circuit with a magnitude based on said signal; wherein said second current supply circuit is adapted to, via said pass device, cause an increase in magnitude of said load current supplied to said output if a voltage at said output decreases and cause a decrease in magnitude of said load current supplied to said output if a voltage at said output increases.

For claim 12, None of the prior art alone or in combination discloses a voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load under varying load conditions having: … wherein said first end is coupled to a second end of said first transistor of said current mirror, and wherein said second end is coupled to said negative node; … a current source that includes a first end coupled to a second end of said second transistor of said current mirror and a second end coupled to said negative node, … a pass device that includes a first end coupled to said positive node, a second end constructed to be coupled to said load at said output of said voltage regulator circuit, and a gate coupled to said second end of said second transistor of said current mirror and said first end of said current source, wherein said gate of said pass device is adapted to receive a signal based on a magnitude of a current of said second current path; wherein said current source is constructed to, if said second voltage reference increases in magnitude, cause a decrease said signal received at said gate of said pass device, and if said second voltage reference decreases in magnitude, cause an increase in a magnitude of said signal received at said gate of said pass device; wherein said pass device is constructed to supply a load current to a load coupled to said output of said voltage regulator circuit with a magnitude based on said signal received at said gate of said pass device.

For claim 14, None of the prior art alone or in combination discloses a voltage regulator circuit integrated in an integrated circuit (IC) and adapted to provide a voltage from a power supply to a load integrated in the IC under selectively variable load

conditions having: … first current supply means for supplying to a second current path referenced to said input a first current that is substantially constant; second current supply means coupled to said first current supply means, said gate of said feedback transistor, and said output of said voltage regulator circuit for receiving a first voltage reference and a second voltage reference and for supplying a second current to said second current path with a magnitude based on said first voltage reference and said second voltage reference; means for supplying current to said load for receiving a signal based on a magnitude of said first current and a magnitude of said second current and for supplying a load current to said load via said output of said voltage regulator circuit with a magnitude based on a magnitude of said signal; wherein said first current supply means, said second current supply means and said means for supplying current to said load are arranged such that, if a voltage at said load decreases, a magnitude of said load current is increased and, if a voltage said load increases, a magnitude of said load current is decreased.

For claim 16, None of the prior art alone or in combination discloses a method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit having: … supplying, to a first current path integrated in said integrated circuit and referenced to said power supply voltage, a master current; … supplying, to a second current path integrated in said integrated circuit and coupled to a pass transistor, a first current with a substantially constant magnitude; supplying, to said second current path, a second current that is a variable current with a magnitude based on said voltage at said gate of said feedback transistor and a voltage at said variable load; receiving, at a

gate of said pass transistor integrated in said integrated circuit, a control signal based on a magnitude of a current of the second current path; and

supplying, to said load via said pass transistor, a load current based on the control signal such that when a voltage across said variable load increases, a magnitude of said load current is reduced, and when a voltage across said variable load decreases, a magnitude of said load current is increased.

For claim 17, None of the prior art alone or in combination discloses a method of regulating a supply voltage for selectively operable load circuitry of an integrated circuit having: … supplying, via a first current source integrated in said integrated circuit and coupled to a second current path, a first current; supplying, via a second current source integrated in said integrated circuit and coupled to said second current path, a second current with a magnitude based in part on a voltage at said variable load; receiving, from said second current path, a control signal at a pass transistor integrated in said integrated circuit, wherein said control signal has a magnitude based a current of said second current path; supplying, to said load circuitry via said pass transistor, a load current in response to said control signal; and wherein a magnitude of said first current and a magnitude of said second current are at least in part dependent on a magnitude of said master current.

The aforementioned limitations in combination with all remaining limitations of the respective claims are believed to render the aforementioned indicated claim and any dependent claims thereof patentable over the art of record.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUE ZHANG whose telephone number is (571)270-1263. The examiner can normally be reached on M-Th 7:30-5:00PM EST, Other F 7:30AM-5:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jue Zhang/

Primary Examiner, Art Unit 2838

November 22, 2011

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

87955 7590 01/18/2012

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

EXAMINER	
ZHANG, JUE	

ART UNIT	PAPER NUMBER
2838	

MAIL DATE	DELIVERY MODE
01/18/2012	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Petitioner Micron Ex-1004, 0357

Supplemental Notice of Allowability	Application No.	Applicant(s)	
	12/464,301	ELRAN, TOMER SHAUL	
	Examiner	Art Unit	
	JUE ZHANG	2838	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *11/16/2011*.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are *1-20*.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Jue Zhang/
Primary Examiner, Art Unit 2838

Petitioner Micron Ex-1004, 0358

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Vadim Braginsky on 1/11/2012.

The application has been amended as follows:

- Claim 8 line 1 has been amended to

"8. (Original) The voltage regulator circuit of claim 7, wherein said at least one stability".

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JUE ZHANG whose telephone number is (571)270-1263. The examiner can normally be reached on M-Th 7:30-5:00PM EST, Other F 7:30AM-5:00PM EST

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Monica Lewis can be reached on 571-272-1838. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jue Zhang/

Primary Examiner, Art Unit 2838

January 11, 2012

Electronic Patent Application Fee Transmittal

Application Number:	12464301
Filing Date:	12-May-2009
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Filer:	Vadim Braginsky/Ralynn Thompson
Attorney Docket Number:	4146.08US01

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl issue fee	1501	1	1740	1740
Publ. Fee- early, voluntary, or normal	1504	1	300	300

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**2040**

Electronic Acknowledgement Receipt

EFS ID:	12180685
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Vadim Braginsky/Ralynn Thompson
Filer Authorized By:	Vadim Braginsky
Attorney Docket Number:	4146.08US01
Receipt Date:	28-FEB-2012
Filing Date:	12-MAY-2009
Time Stamp:	16:25:11
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	$2040
RAM confirmation Number	3863
Deposit Account	160631
Authorized User	BRAGINSKY,VADIM

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.19 (Document supply fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	PARTB_FEETRANS.PDF	84549 a8f947866a637135b3c112fe0b6faa4da6237eb2	no	1
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31951 7caa1939663dc54af6cad5537b2b6ced3a49db36	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	116500		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

87955 7590 11/29/2011
Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01	1327

TITLE OF INVENTION: TRANSIENT LOAD VOLTAGE REGULATOR

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	$1740	$300	$0	$2040	02/29/2012

EXAMINER	ART UNIT	CLASS-SUBCLASS
ZHANG, JUE	2838	323-281000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) the names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Patterson Thuente
2 Christensen Pedersen, P.A.
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: SANDISK IL Ltd.

(B) RESIDENCE: (CITY and STATE OR COUNTRY): Kfar Saba, Israel

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
☐ Issue Fee
☒ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): **(Please first reapply any previously paid issue fee shown above)**
☐ A check is enclosed.
☒ Payment by credit card.
☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number 16-0631 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27.
☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____ Date FEB. 28. 2012

Typed or printed name VADIM BRAGINSKY Registration No. 58031

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Petitioner Micron Ex-1004, 0365

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
12/464,301	04/03/2012	8148962	4146.08US01	1327

87955 7590 03/14/2012

Patterson Thuente Christensen Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 400 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Tomer Shaul Elran, Petah Tikva, ISRAEL;

Electronic Acknowledgement Receipt

EFS ID:	16642886
Application Number:	12464301
International Application Number:	
Confirmation Number:	1327
Title of Invention:	TRANSIENT LOAD VOLTAGE REGULATOR
First Named Inventor/Applicant Name:	Tomer Shaul Elran
Customer Number:	87955
Filer:	Joseph F. Hetz/Maggie Pieczonka
Filer Authorized By:	Joseph F. Hetz
Attorney Docket Number:	4146.08US01
Receipt Date:	21-AUG-2013
Filing Date:	12-MAY-2009
Time Stamp:	12:08:12
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		10519-2366POAandChangeAddressPTO.pdf	206432 f3adc7c6436613a8c92fc572d19e287ca06ce0f4	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Miscellaneous Incoming Letter	1	1
	Power of Attorney	2	2
	Change of Address	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	206432	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

CHANGE OF CORRESPONDENCE ADDRESS

Address to:
Commissioner For Patents
PO Box 1450
Alexandria, VA 22313-1450

Patent Number	8,148,962
Issue Date	April 3, 2012
First Named Inventor	Tomer Shaul Elran
Art Unit	2838
Examiner Name	Zhang, Jue
Attorney Docket No.	10519/2366 (SDA-1303-US)
Confirmation No.:	1327

Please change the Correspondence Address for the above-identified patent application to:

☒ Address associated with **Customer No. 67813 - SanDisk/BHGL**

OR

☐ **Firm *or* Individual Name**					
Address					
City		**State**		**Zip**	
Country					
Telephone		**Email**			

This form cannot be used to change the data associated with a Customer Number. To change the data associated with an existing Customer Number use "Request for Customer Number Data Change" (PTO/SB/124).

I am the:

☐ Applicant/Inventor

☐ Assignee of record of the entire interest.
Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96).

☒ Attorney or agent of record. Registration Number 37,834.

☐ Registered practitioner named in the application transmittal letter in an application without an executed oath or declaration. See 37 CFR 1.33(a)(1). Registration Number _____.

Signature: /Joseph F. Hetz/

Typed or Printed Name: Joseph F. Hetz

Date: August 21, 2013 **Telephone No.:** 312.321.4719

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☒ *Total of 1 forms are submitted.

This collection of information is required by 37CFR 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Inforamtion Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

CERTIFICATE OF EFS FILING UNDER 37 CFR §1.8

I hereby certify that this correspondence is being electronically transmitted to the United States Patent and Trademark Office, Commissioner for Patents, via the EFS pursuant to 37 CFR §1.8 on the below date:

Date: August 21, 2013 Name: Joseph F. Hetz Signature: /Joseph F. Hetz/

BRINKS HOFER GILSON &LIONE

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Appln. of:	Tomer Shaul Elran		
Patent No.:	8,148,962	Examiner:	Zhang, Jue
Issued:	April 3, 2012	Art Unit:	2838
For:	TRANSIENT LOAD VOLTAGE REGULATOR	Conf. No.:	1327
Docket No:	10519/2366 (SDA-1303-US)		

TRANSMITTAL

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Sir:

Attached is/are:

☒ Transmittal Letter; Power of Attorney Document; Change of Correspondence Address Document.

Fee calculation:

☒ No additional fee is required.

☐ Small Entity.

☐ An extension fee in an amount of $_____ for a _____-month extension of time under 37 CFR § 1.136(a).

☐ A petition or processing fee in an amount of $_____ under 37 CFR § 1.17(_____).

☐ An additional filing fee has been calculated as shown below:

						Small Entity			Not a Small Entity	
	Claims Remaining After Amendment		Highest No. Previously Paid For	Present Extra		Rate	Add'l Fee	OR	Rate	Add'l Fee
Total		Minus				x $26=			x $52=	
Indep.		Minus				x 110=			x $220=	
First Presentation of Multiple Dep. Claim						+$195=			+ $390=	
						Total	$		Total	$

Fee payment:

☐ Please charge Deposit Account No. 23-1925 in the amount of $_____ for _____.

☐ Payment by credit card in the amount of $_____ (Form PTO-2038 is attached).

☒ The Director is hereby authorized to charge payment of any additional filing fees required under 37 CFR § 1.16 and any patent application processing fees under 37 CFR § 1.17 associated with this paper (including any extension fee required to ensure that this paper is timely filed), or to credit any overpayment, to Deposit Account No. 23-1925.

Respectfully submitted,

August 21, 2013
Date

/Joseph F. Hetz/
Joseph F. Hetz (Reg. No. 41,070)

Attorney Docket No. 10519/2366 (MSA-1303-US)

Inventors: Tomer Shaul Elran

Title of Appln.: TRANSIENT LOAD VOLTAGE REGULATOR

POWER OF ATTORNEY BY ASSIGNEE AND CORRESPONDENCE ADDRESS INDICATION

The specification of the above-identified patent application:

☐ is attached hereto.

☒ was issued on April 3, 2012 as U.S. Patent No. 8,148,962.

As required by 37 CFR 3.73(b)(1), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

SanDisk IL LTD., a corporation organized under the laws of Israel, ("ASSIGNEE") certifies that it is the assignee of the entire right, title and interest in the patent application identified above by virtue of either:

☒ An assignment from the inventor(s) of the patent application identified above,

- ☒ a copy of which was recorded in the Patent and Trademark Office at Reel 022782, frame 0600, or
- ☐ a copy thereof which is attached hereto and another copy thereof which is being recorded concurrently herewith pursuant to 37 CFR 3.11; OR

☐ A chain of title from the inventor(s) of the patent application identified above, to the current assignee as shown below:

1. From to .
   The document was recorded in the Patent and Trademark Office at Reel , Frame , or a copy thereof is attached.
2. From to .
   The document was recorded in the Patent and Trademark Office at Reel , Frame , or a copy of which is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet.

ASSIGNEE hereby revokes all previously granted powers of attorney in the above identified patent application and appoints the Practitioners associated with the following Customer Number as its attorneys, with full power of substitution and revocation, to prosecute this application and any continuations, divisions, reissues, and reexaminations thereof, to receive the patent(s), to transact all business in the United States Patent and Trademark Office connected therewith, and to act on ASSIGNEE'S behalf before the competent International Authorities in connection with any and all international applications filed by ASSIGNEE:

Customer No.: 67813 - SanDisk/BHGL

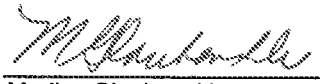
Please recognize or change the correspondence address for this application to the address associated with the above-mentioned Customer Number. Please direct all telephonic and facsimile communications to:

Joseph F. Hetz
Tel.: (312) 321-4200; Fax: (312) 321-4299

The undersigned hereby authorizes the Practitioners associated with the above Customer Number to accept and follow instructions from SanDisk Patent Department as to any action to be taken in the Patent and Trademark Office regarding this application without direct communication between the Practitioners and the undersigned. In the event of a change in the persons from whom instructions may be taken, the Practitioners will be so notified by the undersigned.

The undersigned (whose title is supplied below) is empowered to act on behalf of ASSIGNEE.

I hereby declare that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true; and further, that these statements are made with the knowledge that willful false statements, and the like so made, are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature  Date: August 14, 2013

Name: Marilyn Glaubensklee

Title: Sr. Director, IP Counsel

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	10519/2366(MSA-1303-US)

CONFIRMATION NO. 1327

POA ACCEPTANCE LETTER

67813
BRINKS HOFER GILSON & LIONE
P.O. BOX 10395
CHICAGO, IL 60610

OC00000063509711

Date Mailed: 08/29/2013

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/21/2013.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	4146.08US01

CONFIRMATION NO. 1327

POWER OF ATTORNEY NOTICE

87955
Patterson Thuente Pedersen, P.A.
4800 IDS Center
80 South Eighth Street
Minneapolis, MN 55402

OC000000063509587

Date Mailed: 08/29/2013

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/21/2013.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

/dtvernon/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

Petitioner Micron Ex-1004, 0373

PATENT ASSIGNMENT COVER SHEET

Electronic Version v1.1
Stylesheet Version v1.2

Assignment ID: PATI432478

SUBMISSION TYPE:	NEW ASSIGNMENT
NATURE OF CONVEYANCE:	ASSIGNMENT

CONVEYING PARTY DATA

Name	Execution Date
SanDisk Technologies LLC	08/12/2024

RECEIVING PARTY DATA

Company Name:	Palisade Technologies, LLP
Street Address:	1468 James Rd.
City:	Gardnerville
State/Country:	NEVADA
Postal Code:	89460

PROPERTY NUMBERS Total: 14

Property Type	Number
Patent Number:	9530716
Patent Number:	8148962
Patent Number:	9501398
Patent Number:	9448876
Patent Number:	9454448
Patent Number:	8327051
Patent Number:	9466383
Patent Number:	9281314
Patent Number:	8996838
Patent Number:	9373408
Patent Number:	9524974
Patent Number:	9349458
Patent Number:	7743258
Patent Number:	8135961

CORRESPONDENCE DATA

Fax Number:

Correspondence will be sent to the e-mail address first; if that is unsuccessful, it will be sent using a fax number, if provided; if that is unsuccessful, it will be sent via US Mail.

Phone: 3129194254
Email: dave@gerasimowlaw.com

Correspondent Name:	David Gerasimow
Address Line 1:	FL3 PMB1717
Address Line 2:	211 W Wacker Dr
Address Line 4:	Chicago, ILLINOIS 60606

NAME OF SUBMITTER:	David Gerasimow
SIGNATURE:	David Gerasimow
DATE SIGNED:	08/15/2024
	This document serves as an Oath/Declaration (37 CFR 1.63).

Total Attachments: 2
source=SDTL Palisade Assignment#page1.tiff
source=SDTL Palisade Assignment#page2.tiff

SDTL PALISADE ASSIGNMENT

For good and valuable consideration, the receipt of which is hereby acknowledged, **SanDisk Technologies LLC**, with a registered address at 7501 N Capital of Texas Hwy, Building A, Suite #100, Austin, TX 78731, ("Assignor"), does hereby assign, transfer and convey unto **Palisade Technologies, LLP**, with an office at 1468 James Rd., Gardnerville, NV 89460, USA, ("Assignee"), all of Assignor's entire right, title and interest in and to all patents and patent applications listed in the attached Schedule A (collectively "Patent Rights").

In addition, Assignor agrees to and hereby does sell, assign, transfer and convey unto Assignee all rights (i) in and to causes of action and enforcement rights for the Patent Rights including all rights to pursue damages, injunctive relief and other remedies for past, present and future infringement of the Patent Rights, (ii) the right to apply (or continue prosecution) in any and all countries of the world for patents, design patents, utility models, certificates of invention or other governmental grants for the Patent Rights, including under the Paris Convention for the Protection of Industrial Property, the International Patent Cooperation Treaty, or any other convention, treaty, agreement or understanding, and (iii) the rights, if any, to revive prosecution of any abandoned Patent Rights.

Assignor also hereby authorizes the respective patent office or governmental agency in each jurisdiction to issue any and all patents or certificates of invention or equivalent which may be granted upon any of the Patent Rights in the name of Assignee, as the assignee to the entire interest therein.

The terms and conditions of this Assignment shall inure to the benefit of Assignee, its successors, assigns and other legal representatives, and shall be binding upon Assignor, its successor, assigns and other legal representatives.

This assignment is made effective as of: August 7, 2024.

IN WITNESS WHEREOF, this Assignment of Patent Rights is executed at Sandy, UT, USA on 8/12/24.

ASSIGNOR SanDisk Technologies LLC,

By: _____

Name: David Dutcher
Title: VP, Chief IP and Licensing Counsel

STATE OF Utah)
) ss.
COUNTY OF Salt Lake)

On 08-12-2024 before me,

R. Scott Siler, *Notary Public*

Personally appeared David Dutcher, who proved to me on the basis of satisfactory evidence to be the person whose name is subscribed to the within instrument and acknowledged to me that she executed the same in her authorized capacity, and that by her signature on the instrument the person, or the entity upon behalf of which the person acted, executed the instrument.

I certify under PENALTY OF PERJURY under the laws of the State of Utah that the foregoing paragraph is true and correct.

WITNESS my hand and official seal.

R. Scott Siler
Notary Public

R SCOTT SILER
Notary Public State of Utah
My Commission Expires on:
October 10, 2025
Comm. Number: 720245

SCHEDULE TO ASSIGNMENT

Country	Patent/Publication Number	Application Number
US	9,530,716	13/452,767
KR	10-1774059	2011-7028490
US	8,148,962	12/464,301
CN	ZL201380072287.2	201380072287.2
US	9,501,398	13/831,218
US	9,448,876	14/454,667
US	9,454,448	14/454,672
US	8,327,051	11/986,389
US	9,466,383	14/144,056
US	9,281,314	14/511,834
US	8,996,838	14/273,031
TW	TW201606496	104112604
CN	ZL201510626779.2	201510626779.2
DE	102015116905	102015116905.3
US	9,373,408	14/508,274
US	9,524,974	14/806,111
US	9,349,458	14/515,762
US	7,743,258	11/511,766
US	8,135,961	12/760,359

Docusign Envelope ID: B4E95A0D-813C-4878-AB85-C33B64EA8594

PTO/AIA/81A (02-15)
Approved for use through 03/31/2021. OMB 0651-0035
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995 no persons are required to respond to a collection of information unless it displays a valid OMB control number

PATENT - POWER OF ATTORNEY OR REVOCATION OF POWER OF ATTORNEY WITH A NEW POWER OF ATTORNEY AND CHANGE OF CORRESPONDENCE ADDRESS

Patent Number	8148962
Issue Date	04/03/2012
First Named Inventor	Tomer Shaul ELRAN
Title	Transient load voltage regulator
Attorney Docket No.	9062-0005

I hereby revoke all previous powers of attorney given in the above-identified patent.

☐ A Power of Attorney is submitted herewith.

OR

☒ I hereby appoint Practitioner(s) associated with the Customer Number identified in the box at right as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith: 174899

OR

☐ I hereby appoint Practitioner(s) named below as my/our attorney(s) or agent(s) with respect to the patent identified above, and to transact all business in the United States Patent and Trademark Office connected therewith:

Practitioner(s) Name	Registration Number

Please recognize or change the correspondence address for the above-identified patent to:

☒ The address associated with the above-identified Customer Number.

OR

☐ The address associated with the Customer Number identified in the box at right:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the:

☐ Applicant.

OR

☒ Patent owner.

Statement under 37 CFR 3.73(c) (Form PTO/AIA/96) submitted herewith or filed on _____.

	SIGNATURE of Applicant or Patent Owner		
Signature	Peter Hardigan 844132A3B7D3424...	Date	8/29/2024
Name	Peter Hardigan	Telephone	(917) 622-0926
Title and Company	Manager, Palisade Technologies, LLP		

NOTE: Signatures of all the applicants or patent owners of the entire interest or their representative(s) are required. If more than one signature is required, submit multiple forms, check the box below, and identify the total number of forms submitted in the blank below.

☐ A total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.31, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public, which is to update (and by the USPTO to process) the file of a patent or reexamination proceeding. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Docusign Envelope ID: B4E95A0D-813C-4878-AB85-C33B64EA8594

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
12/464,301	**08/29/2024 04:16:48 PM Z ET**	**10519/2366(MSA-1303-US)**

Title of Invention

TRANSIENT LOAD VOLTAGE REGULATOR

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	8148962
CONFIRMATION #	1327	FILED BY	David Gerasimow
PATENT CENTER #	66982078	FILING DATE	05/12/2009
CUSTOMER #	67813	FIRST NAMED INVENTOR	Tomer Shaul Elran
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	-

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
POA8148962.pdf	2	Power of Attorney	265 KB
Warning: The PDF file has been signed with a digital signature and the legal effect of the document will be based on the contents of the file not the digital signature.			
POA8148962 3.73c.pdf	3	Assignee showing of ownership per 37 CFR 3.73	119 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
POA8148962.pdf	40C6D1B3D73F0D70F1E202781F7E5FA972A844F99B3DAA85F 51DA393AD276147B05367BF9EC96E90F1B38EB4F7B11E6115 AB1A8F1552D4EB8FFB1E6FE3683CD9

POA8148962 3.73c.pdf

15D9C5BF5F411FF8CE492F3F323D296D071329BDBDA1CFC5
C71C09D551511ADDD57D9FE6A01ECB9E57B9F19C273E378B
28945D9FE29B63B1CB590E1737B811AE

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

Applicant/Patent Owner: PALISADE TECHNOLOGIES, LLP

Application No./Patent No.: 8148962 Filed/Issue Date: 4/3/2012

Titled: TRANSIENT LOAD VOLTAGE REGULATOR

PALISADE TECHNOLOGIES, LLP, a LIMITED LIABILITY PARTNERSHIP

(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.)

states that, for the patent application/patent identified above, it is (choose **one** of options 1, 2, 3 or 4 below):

1. ☑ The assignee of the entire right, title, and interest.

2. ☐ An assignee of less than the entire right, title, and interest (check applicable box):

   ☐ The extent (by percentage) of its ownership interest is _____%. Additional Statement(s) by the owners holding the balance of the interest must be submitted to account for 100% of the ownership interest.

   ☐ There are unspecified percentages of ownership. The other parties, including inventors, who together own the entire right, title and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

3. ☐ The assignee of an undivided interest in the entirety (a complete assignment from one of the joint inventors was made). The other parties, including inventors, who together own the entire right, title, and interest are:

   Additional Statement(s) by the owner(s) holding the balance of the interest must be submitted to account for the entire right, title, and interest.

4. ☐ The recipient, via a court proceeding or the like (*e.g.*, bankruptcy, probate), of an undivided interest in the entirety (a complete transfer of ownership interest was made). The certified document(s) showing the transfer is attached.

The interest identified in option 1, 2 or 3 above (not option 4) is evidenced by either (choose **one** of options A or B below):

A. ☐ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel _____, Frame _____, or for which a copy thereof is attached.

B. ☑ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: TOMER SHAUL ELRAN To: SANDISK IL LTD.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 022782, Frame 0600, or for which a copy thereof is attached.

2. From: SANDISK IL LTD. To: WESTERN DIGITAL ISRAEL LTD.

   The document was recorded in the United States Patent and Trademark Office at
   Reel 053574, Frame 0513, or for which a copy thereof is attached.

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PTO/AIA/96 (08-12)
Approved for use through 01/31/2013. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

STATEMENT UNDER 37 CFR 3.73(c)

3. From: WESTERN DIGITAL ISRAEL LTD. To: SANDISK TECHNOLOGIES LLC

The document was recorded in the United States Patent and Trademark Office at
Reel 067735, Frame 0774, or for which a copy thereof is attached.

4. From: SANDISK TECHNOLOGIES LLC To: PALISADE TECHNOLOGIES, LLP

The document was recorded in the United States Patent and Trademark Office at
Reel 068301, Frame 0100, or for which a copy thereof is attached.

5. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

6. From: _____ To: _____

The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☑ As required by 37 CFR 3.73(c)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (i.e., a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/David Gerasimow/	08-29-2024
Signature	Date
David Gerasimow	57,512
Printed or Typed Name	Title or Registration Number

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	9062-0005

CONFIRMATION NO. 1327

174899
The Law Offices of David A. Gerasimow, P.C.
211 W. Wacker Dr.
Ste. 1717
Chicago, IL 60606

POA ACCEPTANCE LETTER

OC000000077842420

Date Mailed: 09/13/2024

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

Petitioner Micron Ex-1004, 0385

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
12/464,301	05/12/2009	Tomer Shaul Elran	10519/2366(MSA-1303-US)

CONFIRMATION NO. 1327

67813
Crowell/
P.O. BOX 10395
CHICAGO, IL 60610

POWER OF ATTORNEY NOTICE

OC000000077842324

Date Mailed: 09/13/2024

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 08/29/2024.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/dtdinh/

Petitioner Micron Ex-1004, 0386