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EXAMINER
VO, NGUYEN THANH

ART UNIT	PAPER NUMBER
2649	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

pto.nsip@gmail.com
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Office Action Summary	Application No. 15/898,316	Applicant(s) HONG et al.	
	Examiner NGUYEN T VO	Art Unit 2649	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on January 25, 2019.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1-28 is/are pending in the application.

5a) Of the above claim(s) 16-28 is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1-15 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 112

2. The following is a quotation of 35 U.S.C. 112(b):

> (b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.

The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-15 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor, or for pre-AIA the applicant regards as the invention.

As to claim 1, the recitation "a discrete element" at line 5 has no clear meaning, because it is not clear as to what is the function of this "discrete element".

As to claim 3, the recitation "<u>separate voltages of circuits</u> in a chip including the processor" has no clear meaning.

As to claim 7, the recitation "electrodes" has no clear meaning, because it is not clear as to which elements of the claim the "electrodes" actually belong to.

As to claim 12, the recitation "an embedded element" at line 2 has no clear meaning because it is not clear as to what is the function of this "embedded element".

As to claim 14, the recitation "the processor is connected to electrodes arranged to cover a target" has no clear meaning. It is not clear as to what is "a target". It is not clear which elements of the claim the "electrodes" actually belong to.

As to claim 15, the recitations “a sensing channel”, and “stimulating channel” have no clear meaning. It is not clear as to what “a sensing channel”, and “stimulating channel” are.

Claim Rejections - 35 USC § 103

4. In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

5. This application currently names joint inventors. In considering patentability of the claims the examiner presumes that the subject matter of the various claims was commonly owned as of the effective filing date of the claimed invention(s) absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and effective filing dates of each claim that was not commonly owned as of the effective filing date of the later invention in order for the examiner to consider the applicability of 35 U.S.C. 102(b)(2)(C) for any potential 35 U.S.C. 102(a)(2) prior art against the later invention.

6. The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

> A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-4, 7, 13-14 are rejected under 35 U.S.C. 103 as being unpatentable over Kuroda (US 2004/0124983) in view of Sudo (JP 10203059; please also see the provided English translation).

As to claim 1, Kuroda discloses a communication device 10A (see at least figure 1A), comprising: a coil 2 disposed around a core area of the communication device; a processor 3 disposed in the core area and configured to establish communication with an external device through the coil (see paragraph

[0005]); and a discrete element 5 connected to the processor 3 through a via 8b (see paragraph [0035]). Kuroda fails to disclose that the discrete element 5 is disposed on the coil 2. Sudo discloses discrete element 5 disposed on a coil 2 (see at least figures 2-3; see also paragraphs [0041], [0043] of the English translation). Therefore, it would have been obvious, before the effective filing date of the claimed invention, to one of ordinary skill in the art to provide the above teaching of Sudo to Kuroda, in order to simplify the manufacturing process and reduce the cost (as suggested by Sudo at paragraph [0044]).

As to claim 2, Kuroda discloses that the processor 3 is disposed in a layer distinguished from the coil 2 (see paragraphs [0027], [0036]).

As to claim 3, Kuroda discloses that the discrete element 5 comprises a passive element (see the capacitor 5) configured to separate voltages of circuits in a chip 3 including the processor (since one of the basic operations of a capacitor is blocking DC voltages and passing AC voltages, the capacitor 5 is inherently configured to separate voltages of circuits in a chip 3 including the processor).

As to claim 4, the combination of Kuroda and Sudo discloses that the discrete element 5 comprises any one or any combination of any two or more of a capacitor, an inductor, and a resistor (see the capacitor 5 as taught by Kuroda), which is connected to a chip 3 comprising the processor through the via 8b; and is arranged in an outer edge ring area of the coil (see Sudo, at least figures 2-3) in a layer distinguished from the coil 2 (see Sudo, paragraph [0039] which discloses that the discrete element 5 is disposed on a film layer 4 which is distinguished from the coil 2.

As to claim 7, Kuroda discloses an electrode router circuit connected to electrodes, wherein the electrode router circuit is included in a chip 3 comprising the processor (see paragraphs [0026], [0029], and [0035]).

As to claim 13, Kuroda discloses a chip 3 comprising the processor is spaced from the coil by a distance greater than or equal to a threshold distance (see at least figure 1A; in this case, “a threshold distance” reads on a distance closed to zero in figure 1A).

As to claim 14, Kuroda discloses that the processor 3 is connected to electrodes arranged to cover a target (see paragraphs [0026], [0029], and [0035]; in this case "a target" as claimed reads on an external device as disclosed in paragraph [0005]); and is configured to receive an electrical signal from or provide an electrical signal to some of the electrodes (see paragraphs [0026], [0029], and [0035]).

8. Claim 5 is rejected under 35 U.S.C. 103 as being unpatentable over Kuroda (US 2004/0124983) in view of Sudo as applied to claim 1 above and further in view of Rappaport (US 2013/0328723).

As to claim 5, the combination of Kuroda and Sudo fails to disclose a first transceiver circuit configured to transmit and receive, through the coil, a signal of a first bandwidth; and a second transceiver circuit configured to transmit and receive, through the coil, a signal of a second bandwidth that is different from the first bandwidth. Rappaport discloses a first transceiver circuit 36 (see at least figures 3-4) configured to transmit and receive, through a coil 28, a signal of a first bandwidth (see paragraphs [0032], [0033]); and a second transceiver circuit 38 configured to transmit and receive, through the coil 28, a signal of a second bandwidth that is different from the first bandwidth (see paragraphs [0032], [0033]). Therefore, it would have been obvious, before the effective filing date of the claimed invention, to one of ordinary skill in the art to provide the above teaching of Rappaport to the combination of Kuroda and Sudo, in order to provide more communication bandwidths to the communication device with a low cost, high performance antenna tuner (as suggested by Rappaport, paragraph [0033]).

9. Claim 6 is rejected under 35 U.S.C. 103 as being unpatentable over Kuroda (US 2004/0124983) in view of Sudo, and Rappaport as applied to claim 5 above and further in view of Pihet (US 2016/0196230).

As to claim 6, the modified Kuroda fails to disclose that the first transceiver circuit is configured to operate at a voltage less than or equal to a first threshold voltage, and the second transceiver circuit is configured to operate at a voltage greater than or equal to a second threshold voltage that is greater

than the first threshold voltage. Pihet discloses that a first transceiver circuit is configured to operate at a voltage less than or equal to a first threshold voltage, and a second transceiver circuit is configured to operate at a voltage greater than or equal to a second threshold voltage that is greater than the first threshold voltage (see paragraph [0053]). Therefore, it would have been obvious, before the effective filing date of the claimed invention, to one of ordinary skill in the art to provide the above teaching of Pihet to the modified Kuroda, in order to provide a proper supplied voltage to each transceiver.

10. Claim 10 is rejected under 35 U.S.C. 103 as being unpatentable over Kuroda (US 2004/0124983) in view of Sudo as applied to claim 1 above, and further in view of Oh (US 2003/0103015).

As to claim 10, the combination of Kuroda and Sudo fails to disclose a first partial coil configured to resonate in a first bandwidth, and a second partial coil configured to resonate in a second bandwidth that is different from the first bandwidth, and the first partial coil and the second partial coil share a loop. Oh discloses a first partial coil configured to resonate in a first bandwidth (see paragraphs [0056], [0066]; in this case, the claimed "a first partial coil" reads on both outside and inside loops), and a second partial coil configured to resonate in a second bandwidth that is different from the first bandwidth (see paragraphs [0056], [0066]; in this case, the claimed "a second partial coil" reads on outside loop), and the first partial coil and the second partial coil share a loop (i.e., inside loop). Therefore, it would have been obvious, before the effective filing date of the claimed invention, to one of ordinary skill in the art to provide the above teaching of Oh to the combination of Kuroda and Sudo, in order to provide more communication bandwidths to the communication device.

Allowable Subject Matter

11. Claims 8-9, 11-12, 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

As to claims 8-9, the prior art of record fail to disclose that the electrode router circuit is configured to connect a first electrode among the electrodes to a sensing circuit, and connect a second electrode among the electrodes to a driving circuit, the sensing circuit is configured to detect, through the first electrode, an electrical signal corresponding to a point to which the first electrode is attached, and the driving circuit is configured to apply, through the second electrode, an electrical signal to a point to which the second electrode is attached, as specified in claim 8.

As to claim 11, the prior art of record fail to disclose that the first partial coil comprises a loop configured to generate a magnetic field in a first direction, and the second partial coil comprises a loop configured to generate an electric field in the first direction.

As to claim 12, the prior art of record fail to disclose an embedded element disposed in a layer distinguished from a layer comprising the coil and a layer including the processor, and connected to the processor through the via; and a motion sensor configured to sense a motion of the communication device.

As to claim 15, the prior art of record fail to disclose that the processor is configured to allocate a sensing channel to one or more electrodes among the electrodes, and allocate a stimulating channel to one or more remaining electrodes among the electrodes, based on the received electrical signal.

Response to Arguments

12. Applicant's arguments filed January 25, 2019 have been fully considered but they are not persuasive.

<u>Rejections Under 35 U.S.C. §112</u>

Regarding claim 1, applicants assert that:

"With respect to claim 1, Applicants respectfully argue that the meaning of "a discrete element" is clear because this is a term of art that would have had a clear meaning to one of ordinary skill in the art. Moreover, paragraph [0083] of the Specification, reproduced below, discusses various example attributes of such a "discrete element":

[0083] Referring to FIG. 5, a discrete element 510 is an element arranged on a coil and connected to a chip through a vertical interconnect access (via). In one example, the discrete element 510 is a passive element configured to separate voltages of circuits in the chip, which includes a processor. The discrete element 510 is, for example, a capacitor, an inductor, and a resistor connected to the chip, which includes the processor, through the via. A size of the discrete element 510 is less than or equal to, for example, 0.6 x 0.3 millimeters (mm)."
The examiner, however, disagrees.

According to MPEP 2111.01:

II. IT IS IMPROPER TO IMPORT CLAIM LIMITATIONS FROM THE SPECIFICATION

"Though understanding the claim language may be aided by explanations contained in the written description, it is important not to import into a claim limitations that are not part of the claim. For example, a particular embodiment appearing in the written description may not be read into a claim when the claim language is broader than the embodiment."

Accordingly, applicants' argument is moot.

Applicants further assert that:

"With respect to the Office's argument "it is not clear as to what is the function of this 'discrete element'" presented on page 2 of the Office Action, Applicants argue that it is not necessary to explicitly state what the function of a structural element is, when the element's structure is defined sufficiently that one of ordinary skill would have understood what structure corresponds to the element and the corresponding structure would have inherently led to a function of the element in the context of the claim".
The examiner, however, disagrees.

Claim 1 just merely recites "a discrete element". Therefore, one of ordinary skill would have not understand what structure corresponds to "the discrete element" and the corresponding structure would have inherently led to a function of "the discrete element" in the context of the claim, as alleged by applicants.

Regarding claim 3 with respect to the recitation "separate voltages of circuits", it is discussed for similar reasons regarding claim 1 as set forth above.

Regarding claim 7, applicants assert that:

"With respect to claim 7, the Office has argued that the recitation "electrodes" has no clear meaning, because it is not clear as to which elements of the claim the "electrodes" actually belong to. Applicants respectfully traverse. Claim 7 recites "an electrode router circuit connected to electrodes." There is no antecedent basis for "an electrode router circuit" or "electrodes," and these claims are recited as new elements in the claim. Hence, claim 7 merely recites features directed to an example in which there is an electrode router circuit (and the electrode router circuit is included in a chip comprising the processor and the electrodes are arbitrary electrodes to which the electrode router circuit is connected. Applicants submit that this would correspond to what is claimed and would not have been indefinite to one of ordinary skill."

The examiner, however, disagrees.

Claim 7 just merely recites "electrodes". Therefore, the claim is indefinite because it is not clear which elements of the claim the "electrodes" actually belong to.

Regarding claim 12, applicants assert that:

"With respect to claim 12, Applicants respectfully argue that the meaning of "an embedded element" is clear because this is a term of art that would have had a clear meaning to one of ordinary skill in the art. As noted above, it is not necessary to specify a particular function for an element if the element's structure defines its role in an embodiment. Additionally, the Office argues that it is not clear with respect to what the embedded element is embedded to. However, the adjective "embedded" is used to characterize the type of element, and the location of the element is sufficiently characterized in the claim, in that the claim recites that the embedded element is "disposed in a layer distinguished from a layer comprising the coil and a layer including the processor" and this can be read as to how the embedded element is "embedded."

The examiner, however, disagrees.

Claim 12 just merely recites "an embedded element". Therefore, the claim is indefinite because it is not clear as to what is the function of this "embedded element".

Regarding claim 14 with respect to the recitation "a target", it is discussed for similar reasons regarding claim 1 as set forth above.

Regarding claim 15 with respect to the recitations "a sensing channel", and "stimulating channel", it is discussed for similar reasons regarding claim 1 as set forth above.

Rejections Under 35 U.S.C. §103

Applicants assert that:

"These rejections are respectfully traversed. As an initial point, Applicants note that with respect to the Sudo reference, the foreign reference is identified as Japanese Reference IQ-203059, but the provided English translation is marked as being a translation of Japanese Reference 10-203060. While Applicants' arguments assume that the provided English translation is a valid translation of Japanese Reference 10-203059, Applicants request that the Examiner confirm, on the record, that the provided translation is correct and explain the numerical discrepancy, or provide a correct translation. Furthermore, if the Office cannot adequately explain the numerical discrepancy, Applicants respectfully submit that it is the Office's responsibility to issue a new Non-Final Office Action in which a correct translation is provided and cited to."

Upon careful review, the examiner notes that the provided English translation marked as being a translation of Japanese Reference 10-203060 does not correspond to the cited Japanese Reference JP10-203059.

A correct English translation of the cited Japanese Reference JP10-203059 is now provided. Per applicants' request, this action is made Non-Final.

Regarding claim 1, applicants assert that paragraph [0005] of Kuroda does not explicitly teach the presence or operation of a processor as claimed, in particular not explicitly teaching that the processor is not only located as claimed, but that that it is "configured to establish communication with an external device through the coil."

The examiner, however, disagrees.

Kuroda discloses a processor 3 included in a responder, wherein the responder communicates with an external device (such as an interrogator as disclosed in paragraph [0005]) through the coil 2 (see figure 1). Therefore, Kuroda does disclose that the processor 3 is disposed in the core area and configured to establish communication with an external device through the coil 2.

Applicants further assert that while the portion [0035] of Kuroda discloses certain aspects of an 1C chip being connected to a capacitor terminal, it does not specify that the connection of these elements occurs through a via.

The examiner, however, disagrees.

Kuroda does disclose a discrete element 5 connected to the processor 3 through a via 8b (see paragraph [0035]; see also at least figure 1A).

Applicants further assert that the combination of Kuroda and Sudo fails to meet the claimed limitations, because Sudo discloses that both the discrete element and processor are mounted on a coil, and they are not connected through a via.

The examiner, however, disagrees.

It appears that applicants' arguments are against the references individually. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this case, Sudo discloses a discrete element 5 disposed on a coil 2 (see at least figures 2-3; see also paragraphs [0041], [0043] of the English translation). As this teaching of Sudo is provided to Kuroda, the combination of Kuroda and Sudo would clearly result a processor 3 (see Kuroda, figure 1A) disposed in a core area of a coil 2, and a discrete element 5 (see Kuroda, figure 1A) disposed on the coil 2 (as taught by Sudo), and connected to the processor 3 through a via 8b (see Kuroda, paragraph [0035];

at least figure 1A). Accordingly, the combination of Kuroda and Sudo would clearly meet the claimed limitations.

Applicants further assert that there is no motivation to combine Kuroda with Sudo.

The examiner, however, disagrees.

In response to applicant's argument that there is no teaching, suggestion, or motivation to combine the references, the examiner recognizes that obviousness may be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988), *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992), and *KSR International Co. v. Teleflex, Inc.*, 550 U.S. 398, 82 USPQ2d 1385 (2007).

In this case, the motivation is found in the references themselves (see Sudo, i.e., in order to simplify the manufacturing process and reduce the cost, as suggested at paragraph [0044]).

Regarding claim 2, applicants assert that Kuroda fail to disclose that the processor 3 is disposed in a layer distinguished from the coil.

The examiner, however, disagrees.

As to claim 2, Kuroda does disclose that the processor 3 is disposed in a layer distinguished from the coil 2 (see figure 5C, paragraphs [0027], [0036]).

Regarding claim 7, applicants assert that Kuroda fail to disclose "an electrode router circuit connected to electrodes, wherein the electrode router circuit is included in a chip comprising the processor."

The examiner, however, disagrees.

Kuroda does disclose an electrode router circuit connected to electrodes, wherein the electrode router circuit is included in a chip 3 comprising the processor (see paragraphs [0026], [0029], and

[0035]). In this case, the circuit inside the chip 3 reads on the claimed "electrode router circuit" with the broadest reasonable interpretation).

Regarding claim 13, applicants assert that "a distance closed to zero" in Kuroda is not reasonable reading of the claimed feature of "a threshold distance."

The examiner, however, disagrees.

Claim 13 merely recites "a threshold distance". Kuroda discloses a chip 3 comprising the processor is spaced from the coil 2 by a distance greater than zero (see at least figure 1A; in this case, "a threshold distance" reads on a distance closed to zero in figure 1A). Accordingly, Kuroda does meet the claimed limitations "greater than or equal to a threshold distance" with the broadest reasonable interpretation.

Regarding claim 14, applicants assert that Kuroda fails to disclose the processor 3 is connected to electrodes arranged to cover a target (see paragraphs [0026], [0029], and [0035]; in this case "a target" as claimed reads on an external device as disclosed in paragraph [0005]);

The examiner, however, disagrees.

The processor 3 in Kuroda is connected to electrodes (see paragraphs [0026], [0029], and [0035]) and communicates with an external device (such as an interrogator disclosed at paragraph [0005]). Accordingly, Kuroda meets the claimed limitations with the broadest reasonable interpretation.

Regarding claims 4, 5-6, 10, the examiner now provides references in order to support his taken Official Notices.

For the foregoing reasons, the examiner contends that the rejections to claims 1-15 are proper.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to NGUYEN THANH VO whose telephone number is (571)272-7901. The examiner can normally be reached on Mon-Fri 8-5.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at http://www.uspto.gov/interviewpractice.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, EDWARD URBAN can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/NGUYEN T VO/
Primary Examiner, Art Unit 2649