

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ACCELIGHT TECHNOLOGIES, INC.,
Petitioner,

v.

APPLIED OPTOELECTRONICS, INC.
Patent Owner.

IPR2025-01566
U.S. Patent No. 10,042,116

**PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT 10,042,116**

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<i>In re Huang</i> , 100 F.3d 135 (Fed. Cir. 1996)	69
<i>Iron Grip Barbell Co. v. USA Sports, Inc.</i> , 392 F.3d 1317 (Fed. Cir. 2004)	69
<i>Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.</i> , 868 F.3d 1013 (Fed. Cir. 2017)	11
<i>Titanium Metals Corp. v. Banner</i> , 778 F.2d 775 (Fed. Cir. 1985)	33, 68
<i>UCB, Inc. v. Actavis Labs. UT, Inc.</i> , 65 F.4th 679 (Fed. Cir. 2023)	32, 68

STATUTES

35 U.S.C. § 102	3, 4, 5
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LISTING OF CHALLENGED CLAIMS

CLAIM TERM	CLAIM LIMITATION
1[PRE]	AN ARRAYED WAVEGUIDE GRATING (AWG) CHIP COMPRISING:
1[A]	A FIRST END FOR COUPLING TO AN OPTICAL COUPLING RECEPTACLE TO RECEIVE AN OPTICAL SIGNAL COMPRISING A PLURALITY OF CHANNEL WAVELENGTHS
1[B]	A SUBSTRATE;
1[C]	A PLANAR LIGHTWAVE CIRCUIT (PLC) DISPOSED ON THE SUBSTRATE, THE PLC COUPLED TO THE FIRST END AND CONFIGURED TO DE-MULTIPLEX EACH CHANNEL WAVELENGTH OF THE PLURALITY OF CHANNEL WAVELENGTHS;
1[D]	A PLURALITY OF OUTPUT WAVEGUIDES COUPLED TO THE PLC, EACH OF THE OUTPUT WAVEGUIDES CONFIGURED TO RECEIVE LIGHT CORRESPONDING TO AN ASSOCIATED DE-MULTIPLEXED CHANNEL WAVELENGTH LAUNCHED FROM THE PLC AND PROVIDE THE LIGHT ALONG A FIRST LIGHT PATH THAT EXTENDS TOWARDS A SECOND END OF THE AWG CHIP; AND
1[E]	A TAPERED REGION DISPOSED AT THE SECOND END OF THE AWG CHIP CONFIGURED TO RECEIVE LIGHT VIA THE PLURALITY OF OUTPUT WAVEGUIDES AND REFLECT THE SAME TOWARDS AN EXPOSED OUTPUT INTERFACE REGION OF THE AWG CHIP, WHEREIN THE EXPOSED OUTPUT INTERFACE REGION EMITS THE RECEIVED LIGHT FROM THE AWG CHIP ON THE SAME SIDE AS THE SUBSTRATE WITHOUT PASSING THE RECEIVED LIGHT THROUGH THE SUBSTRATE.

2	THE AWG CHIP OF CLAIM 1, WHEREIN THE EXPOSED OUTPUT INTERFACE REGION IS CONFIGURED TO PASS THE REFLECTED LIGHT RECEIVED VIA THE PLURALITY OF OUTPUT WAVEGUIDES OUT OF THE AWG CHIP ALONG A SECOND LIGHT PATH THAT IS SUBSTANTIALLY ORTHOGONAL TO THE FIRST LIGHT PATH.
3	THE AWG CHIP OF CLAIM 1, WHEREIN THE AWG CHIP DEFINES A PLURALITY OF SIDEWALLS EXTENDING LONGITUDINALLY FROM THE FIRST END TO THE SECOND END, AND WHEREIN THE TAPERED REGION OF THE SECOND END DEFINES AN ANGLED SURFACE THAT EXTENDS FROM A FIRST SIDEWALL OF THE PLURALITY OF SIDEWALLS TO A SECOND SIDEWALL OF THE PLURALITY OF SIDEWALLS.
4	THE AWG CHIP OF CLAIM 3, WHEREIN THE ANGLED SURFACE HAS AN INTERIOR ANGLE OF ABOUT 41 TO 45 DEGREES RELATIVE TO THE EXPOSED OUTPUT INTERFACE REGION.
10	THE AWG CHIP OF CLAIM 1, WHEREIN THE AWG CHIP IS CONFIGURED AS A 1×N DEMULTIPLEXER DEVICE WHEREBY A SINGLE OPTICAL INPUT SIGNAL IS DE-MULTIPLEXED INTO N DIFFERENT CHANNEL WAVELENGTHS.
11	THE AWG CHIP OF CLAIM 1, WHEREIN THE AWG CHIP IS IMPLEMENTED IN AN AWG DEVICE PACKAGE.
12[PRE]	AN OPTICAL TRANSCEIVER MODULE COMPRISING:
12[A]	A TRANSCEIVER HOUSING;
12[B]	A MULTI-CHANNEL RECEIVER OPTICAL SUB-ASSEMBLY (ROSA) LOCATED IN THE TRANSCEIVER HOUSING AND INCLUDING AN ARRAYED WAVEGUIDE GRATING (AWG) CHIP, THE AWG CHIP COMPRISING:

12[c]	A FIRST END FOR COUPLING TO AN OPTICAL COUPLING RECEPTACLE TO RECEIVE AN OPTICAL SIGNAL COMPRISING A PLURALITY OF CHANNEL WAVELENGTHS, WHEREIN THE FIRST END FOR COUPLING TO THE OPTICAL COUPLING RECEPTACLE INCLUDES AN ANGLED SURFACE TO REDUCE BACK REFLECTIONS OF AN OPTICAL SIGNAL LAUNCHED INTO THE AWG CHIP;
12[d]	A PLANAR LIGHTWAVE CIRCUIT (PLC) COUPLED TO THE FIRST END CONFIGURED TO DE-MULTIPLEX EACH CHANNEL WAVELENGTH OF THE PLURALITY OF CHANNEL WAVELENGTHS;
12[e]	A PLURALITY OF OUTPUT WAVEGUIDES COUPLED TO THE PLC, EACH OF THE OUTPUT WAVEGUIDES CONFIGURED TO RECEIVE LIGHT CORRESPONDING TO AN ASSOCIATED DE-MULTIPLEXED CHANNEL WAVELENGTH LAUNCHED FROM THE PLC AND PROVIDE THE LIGHT ALONG A FIRST LIGHT PATH THAT EXTENDS TOWARDS A SECOND END OF THE AWG CHIP; AND
12[f]	A TAPERED REGION DISPOSED AT THE SECOND END OF THE AWG CHIP CONFIGURED TO RECEIVE LIGHT VIA THE PLURALITY OF OUTPUT WAVEGUIDES AND REFLECT THE SAME TOWARDS AN OUTPUT INTERFACE REGION OF THE AWG CHIP;
12[g]	AN ARRAY OF DETECTOR DEVICES DISPOSED ADJACENT TO THE OUTPUT INTERFACE REGION OF THE AWG CHIP; AND
12[h]	A MULTI-CHANNEL TRANSMITTER OPTICAL ASSEMBLY (TOSA) INCLUDING AT LEAST ONE LASER PACKAGE LOCATED IN THE TRANSCEIVER HOUSING FOR TRANSMITTING OPTICAL SIGNALS AT DIFFERENT CHANNEL WAVELENGTHS.

13	THE OPTICAL TRANSCEIVER MODULE OF CLAIM 12, WHEREIN THE OUTPUT INTERFACE REGION OF THE AWG CHIP IS AN EXPOSED REGION ADJACENT AN AIR GAP, AND WHEREIN THE AIR GAP SEPARATES THE OUTPUT INTERFACE REGION OF THE AWG CHIP AND THE ARRAY OF DETECTOR DEVICES.
15	THE OPTICAL TRANSCEIVER MODULE OF CLAIM 12, WHEREIN THE AWG CHIP DEFINES A PLURALITY OF SIDEWALLS EXTENDING LONGITUDINALLY FROM THE FIRST END TO THE SECOND END, AND WHEREIN THE TAPERED REGION OF THE SECOND END DEFINES AN ANGLED SURFACE THAT EXTENDS FROM A FIRST SIDEWALL OF THE PLURALITY OF SIDEWALLS TO A SECOND SIDEWALL OF THE PLURALITY OF SIDEWALLS.
16	THE OPTICAL TRANSCEIVER MODULE OF CLAIM 15, WHEREIN THE ANGLED SURFACE HAS AN INTERIOR ANGLE OF ABOUT 41 TO 45 DEGREES RELATIVE TO THE OUTPUT INTERFACE REGION.

TABLE OF EXHIBITS

Exhibit	Description
1001	U.S. Patent No. 10,042,116 to Ho et al. (“the ’116 patent”)
1002	Prosecution history of the ’116 patent
1003	Declaration of Michael Lebby, Ph.D.
1004	U.S. Patent Application Publication No. 2014/0183344 to Lee et al. (“Lee”)
1005	U.S. Patent Application Publication No. 2014/0169389 to Kim et al. (“Kim”)
1006	U.S. Patent Application Publication No. 2014/0341578 to Ho et al. (“Ho”)
1007	P. Bernasconi et al., <i>Design and Challenges in a 100 Gb/s Hybrid-Integrated Photonic Circuit</i> , 38TH EUROPEAN CONFERENCE AND EXHIBITION ON OPTICAL COMMUNICATIONS, Amsterdam, Netherlands, 2012, pp. 1-3, paper Tu.4.E.3. (“Bernasconi”)
1008	U.S. Patent No. 9,768,901 to Soldano et al. (“Soldano”)
1009	U.S. Patent Application Publication No. 2005/0286839 to Yoshikawa et al. (“Yoshikawa”)
1010	U.S. Patent No. 5,351,327 to Lurie et al.

I. INTRODUCTION

Petitioner Accelight Technologies, Inc. requests *inter partes* review of U.S. Patent No. 10,042,116 (“the ’116 patent”) based on prior art that was not reviewed by the patent examiner during prosecution of the ’116 patent. Nor was the prior art reviewed by the PTAB for an *inter partes* review petition filed by an unrelated petitioner, Cambridge Industries USA Inc., in IPR2025-00435. The prior art and grounds presented here clearly show that the challenged claims of the ’116 patent (claims 1-4, 10-13, 15, and 16) are unpatentable and should not have been granted. Yet, Patent Owner Applied Optoelectronics, Inc. has asserted the ’116 patent against multiple defendants in district court to monetize the patent—years after it was issued—by alleging infringement by defendants’ products that have been in the U.S. market for almost as long as the life of the patent. Furthermore, Patent Owner has been pressing for quick settlements before the cases reach any significant milestone in district court and before *inter partes* review petition(s) are filed.¹

¹ The undersigned counsel is representing Petitioner against Patent Owner’s claims in district court case no. 4:24-cv-09041-HSG (N.D. Cal.). Undersigned counsel is also representing another defendant, Eoptolink Technology USA Inc., against Patent

More specifically, the challenged claims of the '116 patent recite devices and techniques that were well known and standard practices in the field of optical transceivers before the '116 patent application was filed. For example, the challenged claims recite a combination of components, such as a receiver optical sub-assembly (ROSA), a transmitter optical sub-assembly (TOSA), an arrayed waveguide grating (AWG) chip, a planar lightwave circuit (PLC), photodetectors, etc., that were well known, individually and collectively, long before the '116 patent application was filed. Ex. 1003, ¶46. The only claimed technique that may be considered comparatively newer is the use of an inclined/angled surface on an AWG demultiplexer chip to directly couple demultiplexed output signals with photodetectors through reflection instead of using waveguides or fibers. *See* Ex. 1001, 12:38-45 (claim 1), 13:42-14:2 (claim 12). But even this direct coupling technique was known before the filing of the '116 patent application, as demonstrated by analogous prior art references Lee (Ex. 1004), Kim (Ex. 1005), Bernasconi (Ex. 1007), and Soldano (Ex. 1008), which

Owner in case no. 5:24-cv-08165-NW (N.D. Cal.) and previously represented Molex, LLC against Patent Owner in case no. 4:23-cv-04787-JST (N.D. Cal.) (now dismissed).

are in the same field of optical transceivers and disclose the claimed direct coupling technique. The challenged claims are therefore unpatentable.

II. PRIOR ART REFERENCES, GROUNDS, AND PETITIONER’S STIPULATION

A. Prior Art References and Grounds

Claims 1-4, 10-13, 15, and 16 are challenged based on the following prior art references. Some other references are discussed throughout the Petition to demonstrate the relevant state of the art and well-established techniques in the field of optical transceivers.

Prior Art	
Ex. 1004	U.S. Patent Publication No. 2014/0183344 to Lee et al., filed Aug. 22, 2013, and published July 3, 2014 (“Lee”); prior art under 35 U.S.C. § 102(a)(1).
Ex. 1005	U.S. Patent Publication No. 2014/0341578 to Ho et al., filed November 25, 2013 and published November 20, 2014 (“Ho”); prior art under 35 U.S.C. § 102(a)(1).
Ex. 1006	U.S. Patent Publication No. 2014/0161457 to Ho et al., filed December 7, 2012, and published Jun. 12, 2014 (“Ho”); prior art under 35 U.S.C. § 102(a)(1).

Ex. 1007	P. Bernasconi et al., <i>Design and Challenges in a 100 Gb/s Hybrid-Integrated Photonic Circuit</i> , 38TH EUROPEAN CONFERENCE AND EXHIBITION ON OPTICAL COMMUNICATIONS, Amsterdam, Netherlands, 2012, pp. 1-3, paper Tu.4.E.3. (“Bernasconi”); prior art under 35 U.S.C. § 102(a)(1).
Ex. 1008	U.S. Patent No. 9,768,901 to Soldano et al., filed February 12, 2015, and issued September 19, 2017 (“Soldano”); prior art under 35 U.S.C. § 102(a)(2).
Ex. 1009	U.S. Patent Publication No. 2005/0286839 to Yoshikawa; filed June 15, 2005, and published December 29, 2005 (“Yoshikawa”); prior art under 35 U.S.C. § 102(a)(1).

The presented prior art grounds are:

Ground	Claims ²	Basis Under 35 U.S.C. § 103
1	1-4, 10, 11 (“Group 1 Challenged Claims”)	Lee in view of Kim
2	12, 13, 15, 16 (“Group 2 Challenged Claims”)	Ho in view of Lee and Kim and further in view of Yoshikawa

² A listing of the challenged claims is provided at the beginning of the Petition.

3	Group 1 Challenged Claims	Bernasconi in view of Soldano
4	Group 2 Challenged Claims	Ho in view of Bernasconi and Soldano and further in view of Yoshikawa

B. Petitioner's Stipulation for the Parallel District Court Action

If the Board institutes an IPR based on this Petition (and does not subsequently vacate or withdraw institution), Petitioner will not pursue in the parallel district court litigation (case no. 4:24-cv-09041-HSG (N.D. Cal.)), (i) the specific grounds raised in this Petition, (ii) any other grounds that reasonably could have been raised under §§ 102 or 103 on the basis of prior art patents or printed publications, or (iii) any ground based on a combination of system prior art and the prior art references asserted in this Petition (identified in Section II.A, above).

III. TECHNICAL BACKGROUND OF THE '116 PATENT

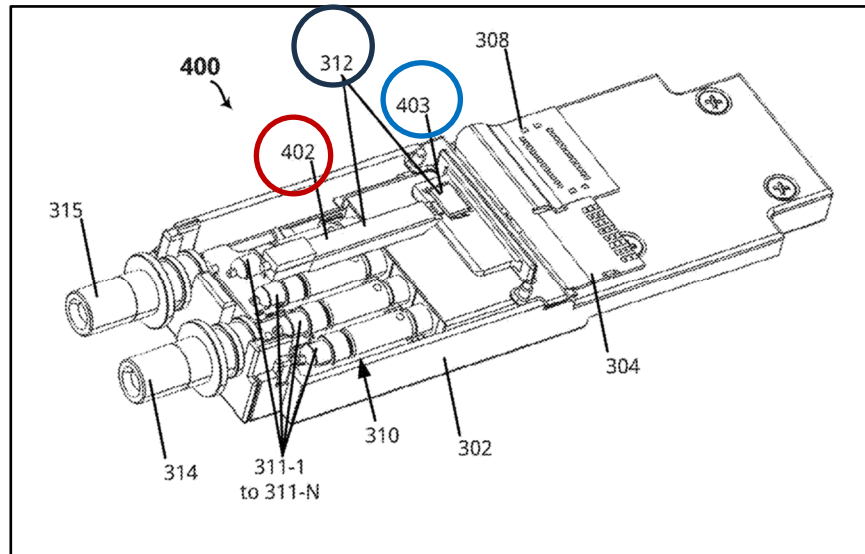
A. The '116 Patent

The '116 patent discloses a technique for direct optical coupling of a plurality of photodetectors to the outputs of an optical demultiplexer (e.g., an AWG demultiplexer), and an optical transceiver module that uses this disclosed direct optical coupling technique. Ex. 1001, Title, Abstract, 1:9-12.

As disclosed in the '116 patent, operation of an optical transceiver module includes transmitting a multiplexed optical signal through an optical fiber to a multi-

channel ROSA. The input signal is then demultiplexed into separate channel wavelengths by an AWG demultiplexer for detection, amplification, and conversion to electrical signals. *Id.*, 1:26-29, 2:15-27, 11:47-12:3. Detectors, such as photodiodes, receive the demultiplexed outputs of the AWG, with a single detector receiving a single channel wavelength, and provide the same to associated circuitry for amplification and conversion. *Id.*, 4:26-34. The disclosed optical transceiver further includes a multi-channel TOSA having at least one laser package for transmitting optical signals at different channel wavelengths. *Id.*, 11:47-12:3.

Specifically, the '116 patent claims to have invented an optical transceiver 400 having a transceiver housing 302, a multi-channel TOSA 310, and a multi-channel ROSA 312. *Id.*, 7:3-7, Fig. 4. ROSA 312 further includes an AWG device 402 for demultiplexing multi-channel optical signals and direct optical coupling of the demultiplexed optical signals to an array of photodetectors and associated TIAs (transimpedance amplifiers) to reduce insertion loss associated with using fibers or waveguides. *Id.*, Title, Abstract, 1:9-12, 3:1-22, 7:40-51, Fig. 4.

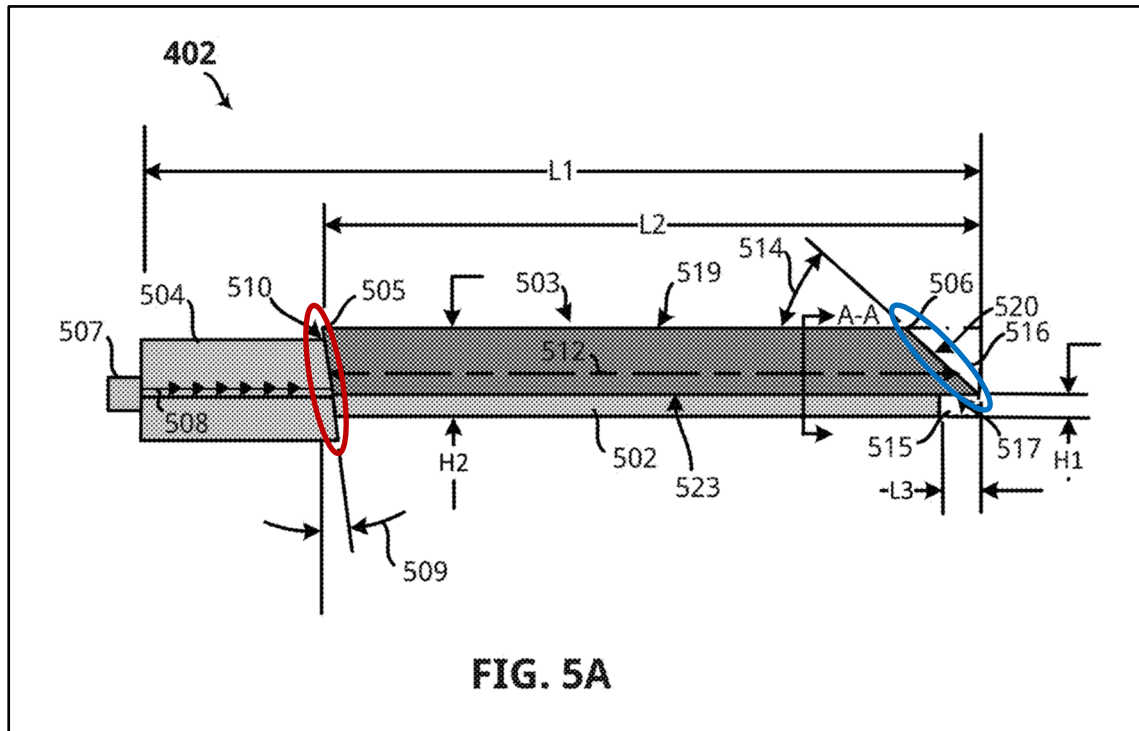


Ex. 1001, FIG. 4 (showing transceiver 400 having TOSA 310 and **ROSA 312**, and ROSA 312 further including an **AWG device 402** for demultiplexing input signals and for direct coupling the demultiplexed signals to an array of photodetectors and **TIAs 403**).

The AWG device 402 includes an AWG chip 503 having a first end 505 coupled to an input coupling region 504, and a second end 506 adjacent to a direct coupling interface region 517. *Id.*, 7:60-66. In some embodiments, the end of input coupling region 504 includes a mounting surface 510 having an angle of about 8 degrees to reduce back reflection when launching light into AWG chip 503. *Id.*, 8:20-30, Fig. 5A. In other embodiments, the first end 505 of the AWG chip may include a mounting surface with an angle of about 8 degrees. *Id.*

AWG chip 503 comprises a planar lightwave circuit (PLC) formed on a substrate 502, and the PLC is configured to demultiplex a multi-channel input signal

into a plurality of channel wavelengths and to launch the channel wavelengths into respective output waveguides 511. *Id.*, Abstract, 8:31-43, 8:53-57. Output waveguides 511 transmit the channel wavelengths along a first light path 806 that extends longitudinally towards the second end (direct coupling end) 506 of AWG chip 503. *Id.*, 10:11-14. Second end 506 has an inclined/angled surface 520 with an angle 514 of about 40 to 45 degrees relative to light path 806. *Id.*, 10:17-24. According to the '116 patent, angle 514 allows “a substantial amount of light, e.g., at least 80 percent,” to reflect towards detectors 804 along a second light path 530 that is “generally orthogonal” to first light path 806 and to pass through direct coupling interface region 517. *Id.*, 10:30-37, Fig. 8. A portion of substrate 502 (on which the PLC is formed) is removed to expose direct coupling interface region 517, so that optical signals traveling along light path 530 do not pass through the substrate. *Id.*, 9:46-50, Figs. 5A and 8. Light traveling along second light path 530 is received by detectors 804 of a photodetector array 801. *Id.*, 11:1-4. Each detector 804 is aligned beneath the direct coupling interface region 517, and specifically beneath a respective output waveguide 511, to directly couple each demultiplexed output of AWG chip 503 with a detector 804, without requiring any waveguide or fiber therebetween. *Id.*, 11:10-27, Fig. 9.



Ex. 1001, Fig. 5A (showing AWG chip 502 having an **angled surface 505** at a first (input) end and an **angled surface 520** at a second (output) end)

But as discussed below, optical transceivers with TOSAs and ROSAs, AWG demultiplexers, and direct coupling of demultiplexed outputs to a photodetector array using an angled surface, were each known before the filing of the '116 patent. Ex. 1003, ¶46.

B. Prosecution History of the '116 Patent

U.S. Patent Application No. 15/137,823 ("the '823 Application"), which issued as the '116 patent, was filed on April 25, 2016. Ex. 1001, cover page. On June 7, 2017, the Office required a restriction between claims 1-19, directed to an AWG chip, and claim 20, directed to a method of forming an AWG. Ex. 1002, 54-

58. On August 7, 2017, Applicant elected claims 1-19 for examination and withdrew claim 20. *Id.*, 64.

On August 21, 2017, the Office issued a non-final office action rejecting claims 1-11 as anticipated by Bai (U.S. Patent No. 7,532,783). *Id.*, 70-75. The Office also rejected claims 12-19 as obvious over Dallesasse (U.S. Patent No. 7,941,053) in view of Bai or Welch et al. (U.S. Patent No. 7,058,263). *Id.*, 75-81. In response, applicant amended independent claim 1 to recite that the PLC was “disposed on” a “substrate,” that the output interface region was “exposed,” and further that “the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.” *Id.*, 111-120. Independent claim 12 was amended to recite that the first end “includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip.” *Id.* Applicant argued that Bai, Dallesasse, and Welch did not teach the added claim limitations. *Id.* On June 4, 2018, the Office issued a Notice of Allowance, allowing claims 1-19 because the amended claims limitations were supposedly not disclosed by the prior art of record. *Id.*, 182-88. The ’116 patent issued on August 7, 2018. Ex. 1001, cover page.

IV. LEVEL OF ORDINARY SKILL

At the effective filing date of the ’116 patent, a person of ordinary skill in the art (“POSITA”) would have had (1) a bachelor’s degree in electrical or electronics

engineering or an equivalent degree, and (2) 2-4 years of work experience in optoelectronics, optical networking, optical communications, or a closely related field. Ex. 1003, ¶39.

V. CLAIM CONSTRUCTION

Claims must be construed only to the extent necessary to resolve a controversy. *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017). Only the term “substrate,” recited in claim 1, would benefit from claim construction to resolve the disputes in this forum.

A. “Substrate”

The claim term “substrate” should be construed to mean “a supporting base that is part of the AWG chip and on which the planar lightwave circuit (PLC) is mounted.” This construction is fully supported by claim 1, which recites that the AWG chip comprises a “substrate,” and that the PLC is “disposed on the substrate.” Ex. 1001, 12:23-31.

The specification of the ’116 patent also supports this construction. Specifically, the specification discloses that AWG chip 503 comprises a substrate 502, and thus specifies that the substrate is part of the AWG chip. Ex. 1001, 9:55-57, 9:46-49, Fig. 5A; Ex. 1003, ¶49. The specification also discloses that the substrate is a supporting base of the AWG chip on which the PLC is formed. Ex. 1003, ¶50. For example, the specification discloses that “[p]rocesses for AWG chips can include,

for example, forming a circuit pattern using photolithography, etching and deposition and/or epitaxial growth on a substrate, e.g., a silicon or silicon-based substrate.” Ex. 1001, 8:31-38; *see also id.*, 12:4-11 (method of forming an AWG comprises “depositing sequential layers of cladding and core material onto a substrate to form a planar lightwave circuit (PLC), removing a portion of the substrate to expose an output interface region of the PLC[.]”).

Thus, claim 1 and the ’116 patent specification disclose an AWG chip comprising a PLC and a substrate. In the pending district court litigation, however, Patent Owner has taken a position that the substrate may be a supporting base outside the AWG chip, and on which the AWG chip is mounted. This is incorrect. The substrate is not a component separate from (or external to) the AWG chip. Ex. 1003, ¶51. The term “substrate” should be construed to mean “a supporting base that is part of the AWG chip and on which the planar lightwave circuit (PLC) is mounted.” *Id.*

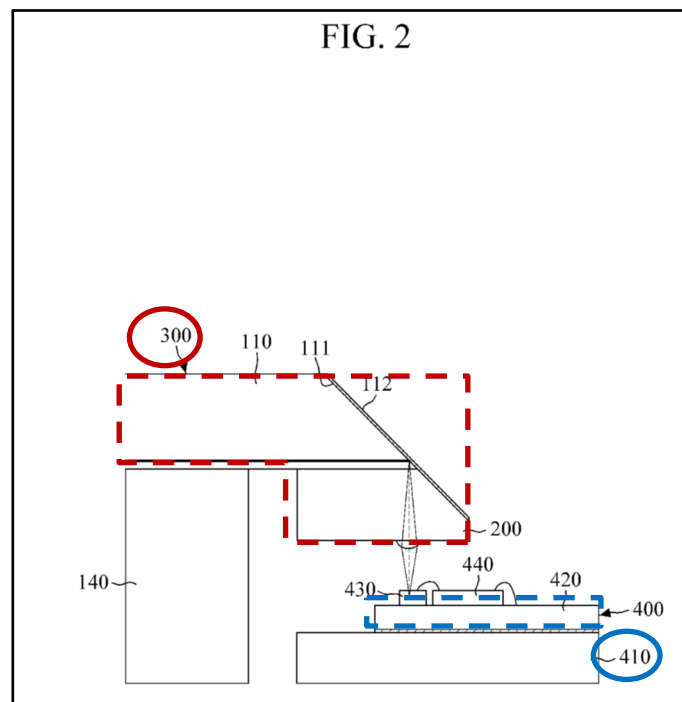
VI. LEE-BASED GROUNDS

A. [Ground 1] The Group 1 Claims are Rendered Obvious by Lee in View of Kim

1. Lee (Ex. 1004)

Lee discloses a hybrid optical coupling module comprising an optical unit for transmitting light and an electrical unit for converting an optical signal into an electrical signal. Ex. 1004, Abstract, ¶[0003]. Specifically, Lee discloses an optical

module comprising 1) an optical unit 300 that includes an optical transmission means in the form of a planar lightwave circuit (PLC) 110 and array lens 200, and 2) an electrical unit 400 that includes a photodiode (PD) 430, transimpedance amplifier (TIA) 440, and substrate 420. *Id.*, ¶¶[0033], [0036], [0038], [0043]-[0045], Figs. 2, 8.



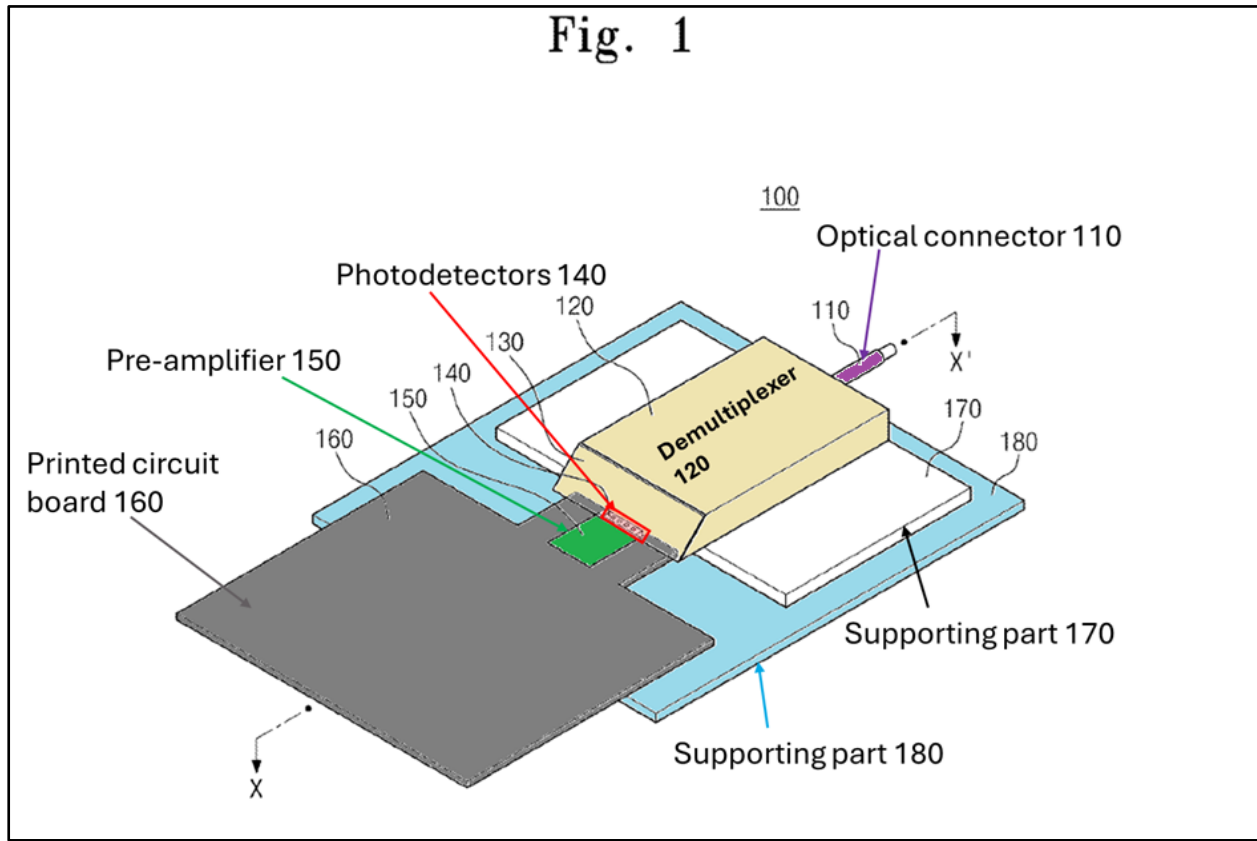
Ex. 1004, Figs. 2 (annotated to show direct optical coupling between **optical unit 300** and **electrical unit 400**)

Lee discloses that one application of the optical coupling module and the PLC is a demultiplexer comprising an arrayed waveguide grating (AWG). *Id.*, ¶[0009].

Lee further discloses that the optical coupling between optical unit 300 and electrical unit 400 is achieved by having an inclined surface 111 formed at an angle of 45 degrees on one side of PLC 110, and a reflection layer 112 formed on inclined surface 111 for vertically reflecting an optical signal from optical unit 300 to photodiode 430 of electrical unit 400. *Id.*, ¶¶[0049]-[0054], [0073]-[0074], Figs. 2, 8.

2. Kim (Ex. 1005)

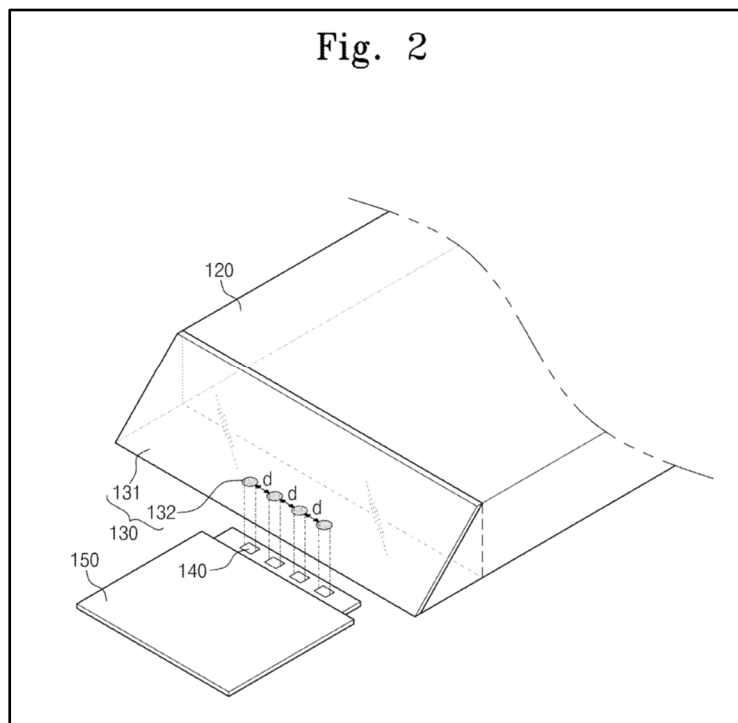
Kim discloses an optical receiver module 100 comprising, among other things, an **optical connector 110**, a **demultiplexer 120** having an integrated optical device 130, a **photodetector array 140**, a **pre-amplifier 150**, supporting part 170, and **supporting part 180**, as shown in Figure 1. Ex. 1005, ¶[0022], Fig. 1; *see also id.*, Abstract, ¶[0025] (discussing that optical device 130 and demultiplexer 120 may have a “united structure”).



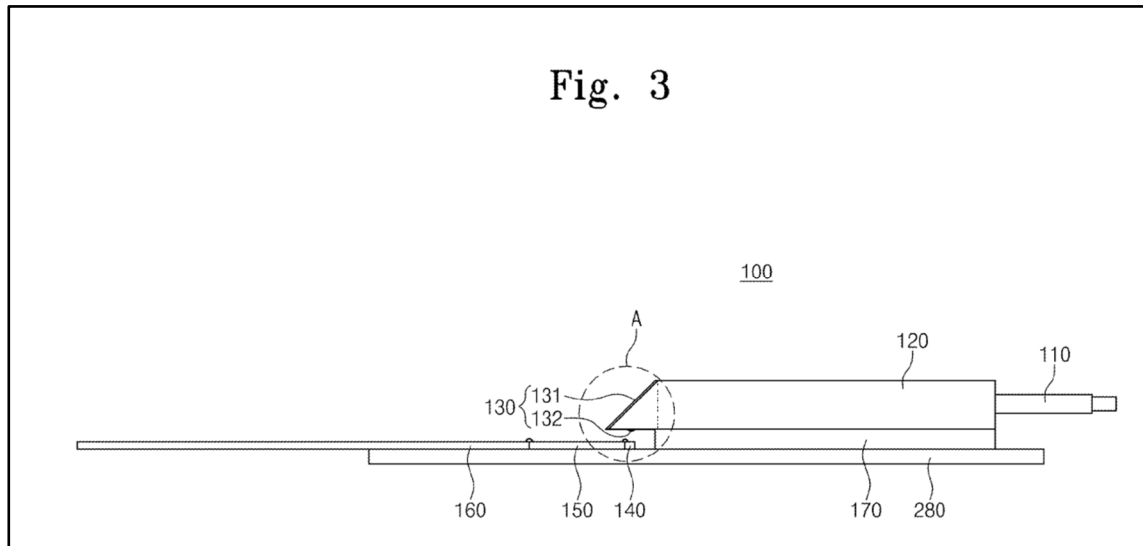
Ex. 1005, Fig. 1 (annotations added)

Optical connector 110 receives a multi-channel optical signal through an optical fiber and transmits the input signal to demultiplexer 120. *Id.*, ¶[0023]. Demultiplexer 120, which may have an AWG structure, divides the multi-channel input signal into separate signals corresponding to each channel and transmits each channel to optical device 130, which may be integrated with AWG 120. *Id.*, ¶¶[0024], [0025], [0040]. Optical device 130 includes a single mirror 131 and N lenses 132 (where N represents the number of input channels). *Id.*, ¶¶[0032], [0033]. An end portion of optical device 130 may be cut at an angle of 45 degrees and then the cut

surface may then be polished. *Id.*, ¶[0034]. A silica-based material may be coated on the outer side of the cut surface to form mirror 131. *Id.* “The mirror 131 reflects the optical signal transmitted in a horizontal direction through the demultiplexer 120, and the reflected optical signal is transmitted in a vertical direction to the lenses 132.” *Id.*, ¶¶[0034], [0041], Fig. 4. Each optical signal (corresponding to a channel wavelength) passes through one of the lenses 132 and is optically coupled with a corresponding photodetector 140, which converts the optical signal into an electrical signal and transmits the electrical signal to a pre-amplifier 150, which then transmits the amplified signal to a printed circuit board 160 for external transmission. *Id.* ¶¶[0029], [0030], [0041], [0042], Figs. 2 and 3 (reproduced below).



Ex. 1005, Fig. 2.



Id., Fig. 3.

3. A POSITA would have been motivated to combine Lee and Kim and would have reasonably expected success

Lee and Kim are in the same field of optoelectronics and have the same applicant. *Compare* Ex. 1004 (cover page), *with* Ex. 1005 (cover page). They both describe modules for optical communication. Ex. 1003, ¶75. Specifically, Lee discloses that one application of the optical module is an optical transceiver, wherein the PLC is used as a demultiplexer comprising an AWG. Ex. 1004, ¶¶[0008]-[0009]. Similarly, Kim describes “wavelength division multiplexing (WDM) type optical receiver modules capable of increasing optical coupling efficiency between a demultiplexer and a photodetector.” Ex. 1005, ¶[0002]. Therefore, a POSITA would have considered Lee and Kim together when designing or developing an optical module, such as the one disclosed in the ’116 patent, to optically couple an optical unit (e.g.,

an AWG demultiplexer) with an electrical unit (e.g., a photodetector array). Ex. 1003 ¶¶73-75.

Lee discloses every aspect of the claimed invention of the '116 patent, as discussed below. While Lee does not explicitly disclose a connector for providing input signals to optical unit 300, it would have been obvious to a POSITA that an input connector is essential for inputting incoming signals into the optical unit, and would have been motivated to use Kim's input connector 110 to provide input signals to Lee's optical unit. Ex. 1003, ¶¶78, 79. Furthermore, a POSITA would have readily recognized the design compatibility between Lee's and Kim's optical modules and would thus have been motivated to use Kim's connector 110 with Lee's optical unit 300. *Id.* A POSITA would also have reasonably expected success in combining Lee and Kim for the same reason. *Id.*

Relatedly, although Lee discloses that its optical unit may be used as an AWG demultiplexer, Lee does not provide additional details of the AWG structure or the demultiplexer functionality. *See* Ex. 1004, ¶[0009]. Kim, however, provides explicit details about AWG demultiplexer 120. *See* Ex. 1005, ¶¶[0022]-[0024]. Therefore, a POSITA would have considered Lee and Kim together. Ex. 1003, ¶79. More specifically, a POSITA would have known that AWGs are commonly used for optical demultiplexing in WDM systems to retrieve individual channels of different wavelengths at the receiving end of an optical communication network, because of the

minimal insertion loss and reduced cross-talk of AWG structures. Ex. 1003, ¶84. Accordingly, when implementing an optical transceiver module in a WDM system, such as the one disclosed in Lee (*see* Ex. 1004, ¶¶[0007]-[0009]), a POSITA would have found it obvious to use an AWG demultiplexer and would have been motivated to consider and apply the elementary AWG demultiplexer disclosed in Kim because of its simplicity and ease of implementation. Ex. 1003, ¶84.

For the same reasons, applying nothing more than ordinary skill and basic knowledge of optical components, a POSITA would have reasonably expected success in combining Kim's AWG with the optical module of Lee. *Id.*, ¶79. Indeed, combining Lee with an input connector and AWG demultiplexer, as disclosed in Kim, would have been a combination of known prior art elements according to their established functions. *Id.* The combination would have yielded the predictable result of an AWG chip with efficient and effective demultiplexing of optical signals and direct coupling of the demultiplexer outputs with respective photodetectors. *Id.*

4. Independent claim 1

Lee in view of Kim discloses each and every limitation of claim 1.

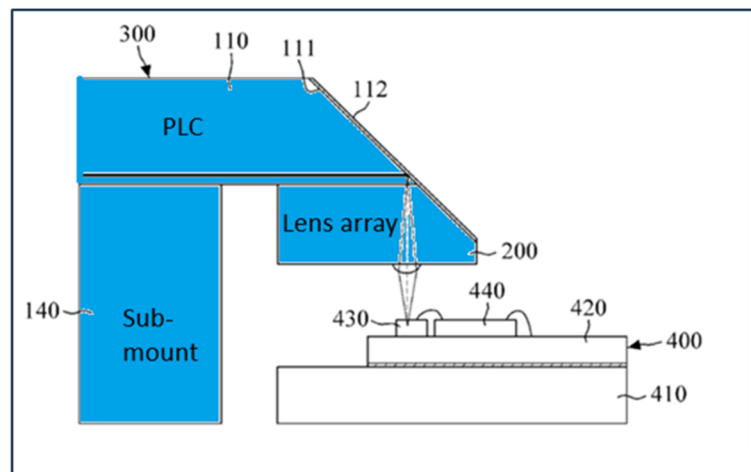
a. Claim 1[preamble]

Lee discloses an optical unit 300 that is mounted on a sub-mount 140 and includes a planar lightwave circuit (PLC) 110. Ex. 1004, ¶¶[0033], [0035], [0036], [0038], [0042]-[0046]. Lee further discloses that one application of the PLC is a

demultiplexer comprising AWG. *Id.*, ¶[0009]. While Lee does not explicitly disclose the AWG structure and functionality within the PLC, Kim discloses such an AWG demultiplexer chip. Ex. 1003, ¶73.

Kim also discloses “an optical receiver module 100 [which] includes an optical connector 110, a demultiplexer 120, an optical device 130, a photodetector 140, a pre-amplifier 150, a printed circuit board 160, a first supporting part 170, and a second supporting part 180.” Ex. 1005, ¶[0022]. Kim further discloses that demultiplexer 120 may be an AWG demultiplexer. *Id.*, ¶¶[0022]-[0024].

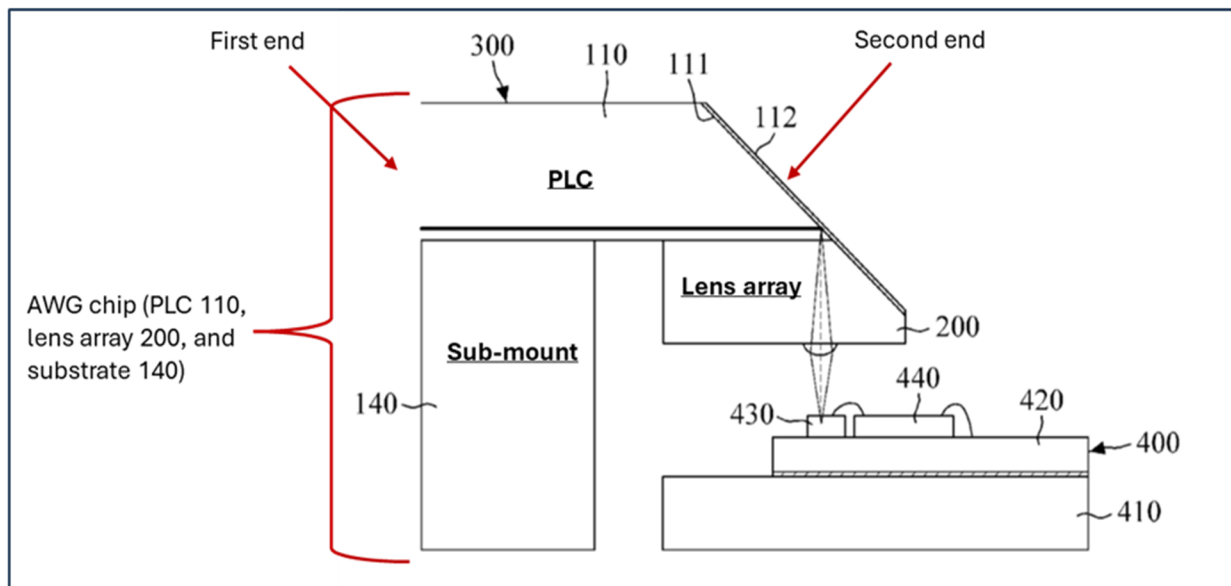
As discussed in Section VI.A.3, above, a POSITA would have known to consider Lee and Kim together given their design compatibility and similar teachings. Lee’s optical unit 300 and sub-mount 140, wherein PLC 110 is modified in view of Kim to have AWG structure and functionality, together form an “AWG chip.”



Ex. 1004, Fig. 2 (showing **AWG chip** comprising PLC 110, sub-mount 140, and lens array 200)

b. Claim term 1[a]

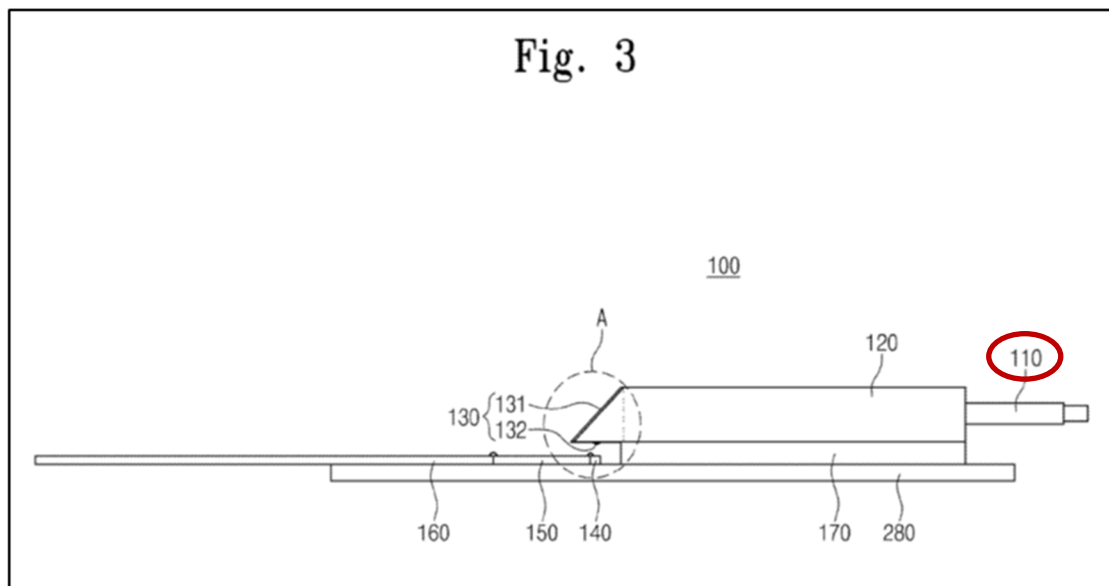
Although Lee does not expressly disclose how the AWG chip receives an optical signal, a POSITA would have understood that Lee's AWG chip necessarily has a first end that couples with an optical connector to receive an input signal. Ex. 1003, ¶76.



Ex. 1004, Fig. 2 (annotations added)

Kim explicitly discloses an AWG chip having an optical connector 110, which “receives an optical signal inputted through a single optical fiber and then transmits the optical signal to the demultiplexer 120.” Ex. 1005, ¶[0023]. Optical connector 110 of Kim has “a pigtail-shape or a **receptacle-shape.**” *Id.*, ¶[0023] (emphasis added), Fig. 3. Kim additionally discloses that “**the optical signal may be 4-channel input optical signals which have four wavelengths different from each other,**

respectively. The 4-channel input optical signals may be multiplexed optical signals. The 4-channel input optical signals are transmitted to the optical connector 110 through the single optical fiber.” *Id.* (emphasis added). Thus, Kim discloses a demultiplexer 120 having a first end for coupling to an optical connector 110, which may be implemented as an optical coupling receptacle, to receive an optical signal comprising a plurality of channel wavelengths. Ex. 1003, ¶77.



Ex. 1005, Fig. 3 (showing **optical connector 110** coupling with a first (input) end of Kim’s AWG demultiplexer 120)

It would have been obvious to a POSITA that, when the AWG chip of Lee is used as a demultiplexer, the first end of Lee’s AWG chip would have been modified (in view of Kim) to couple to an optical coupling receptacle, such as Kim’s optical

connector 110, to receive an optical signal comprising a plurality of channel wavelengths. Ex. 1003, ¶78.

c. Claim term 1[b]

The AWG chip of Lee includes a substrate, specifically, a sub-mount 140 on which optical unit 300 is mounted. Ex. 1004, ¶[0042], Figs. 2, 8. A POSITA would have understood that the sub-mount provides support and structure to optical unit 300 and is included within, i.e., it is a part of, Lee's AWG chip. Ex. 1003, ¶80.

d. Claim term 1[c]

Lee discloses an optical unit 300 which includes a PLC 110, which may be applied as an AWG demultiplexer. Ex. 1004, ¶¶[0009], [0033], [0036], [0038], [0043]-[0046]. PLC 110 is disposed on a substrate (sub-mount 140). *Id.*, Fig. 2. It would have been obvious to a POSITA that PLC 110 of Lee's AWG chip would have been coupled to the first end of the AWG chip to receive the input optical signal provided via an optical coupling receptacle, as taught by Kim (discussed above). Ex. 1003, ¶81. A POSITA would have been motivated to directly couple the PLC to the first end to receive the input signals without any intermediate fiber or other components to reduce signal insertion loss and other disruptions. *Id.* Indeed, the first (input) end of Kim's AWG demultiplexer 120 is coupled directly to optical connector 110, without any intermediate element. *Id.* Accordingly, in the AWG chip of Lee in view of Kim, PLC 110 would have been coupled to the first end of the chip. *Id.*

Kim further discloses that “demultiplexer 120 is connected to one end of the optical connector 110 [at the first end] to receive the 4-channel input optical signals. The demultiplexer 120 divides the 4-channel optical signal into optical signals corresponding to channels, respectively.” Ex. 1005, ¶[0024].

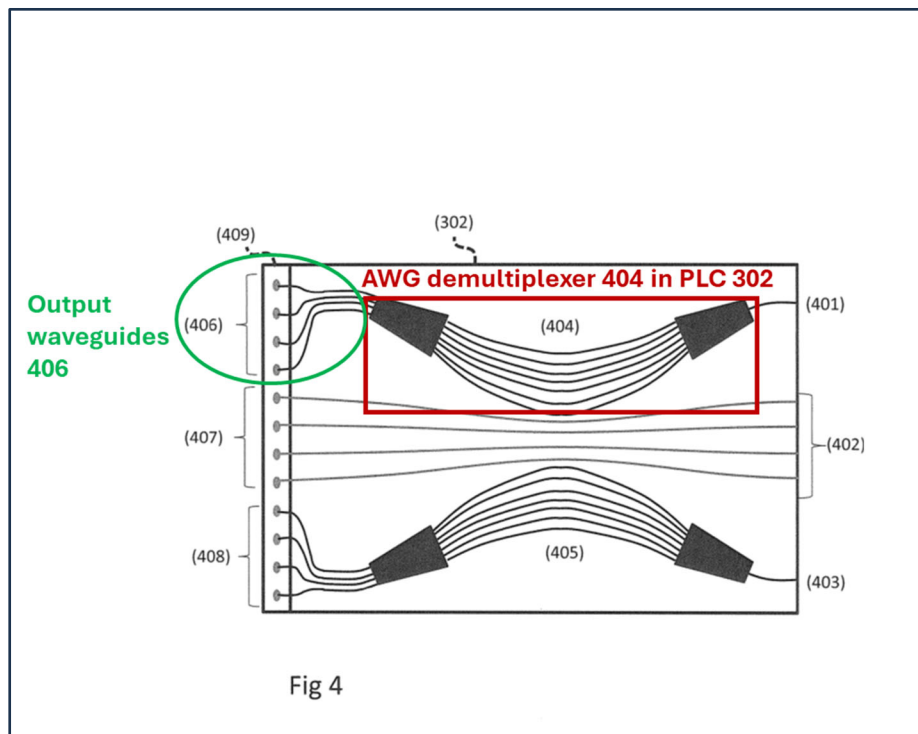
Thus, Lee in view of Kim discloses an AWG demultiplexer on PLC 110 of Lee to demultiplex each channel wavelength of the plurality of channel wavelengths. Ex. 1003, ¶83; Ex. 1004, ¶[0009]; Ex. 1005, ¶[0024].

e. Claim term 1[d]

Lee discloses that output light is “transmitted through a core 113 of the PLC 110[.]” Ex. 1004, ¶[0045], Fig. 6. A POSITA would have known that a core of a PLC is necessarily an optical waveguide to guide light through the PLC. *See, e.g.*, Ex. 1008, 9:56-58 (“The PLC waveguides have two outer cladding regions 502 and 504, and a higher index core region 503.”); Ex. 1003, ¶85. Therefore, it would have been obvious to a POSITA that in Lee in view of Kim, the demultiplexed light from PLC 110 would have been passed along separate optical waveguides paths (i.e., cores 113) corresponding to each channel wavelength, because that is how AWG-based demultiplexing is commonly implemented to avoid cross-talk between the channels. Ex. 1003, ¶85.

Moreover, other prior art references explicitly disclose such output waveguides. For example, Soldano explicitly discloses a PLC 302 having an AWG

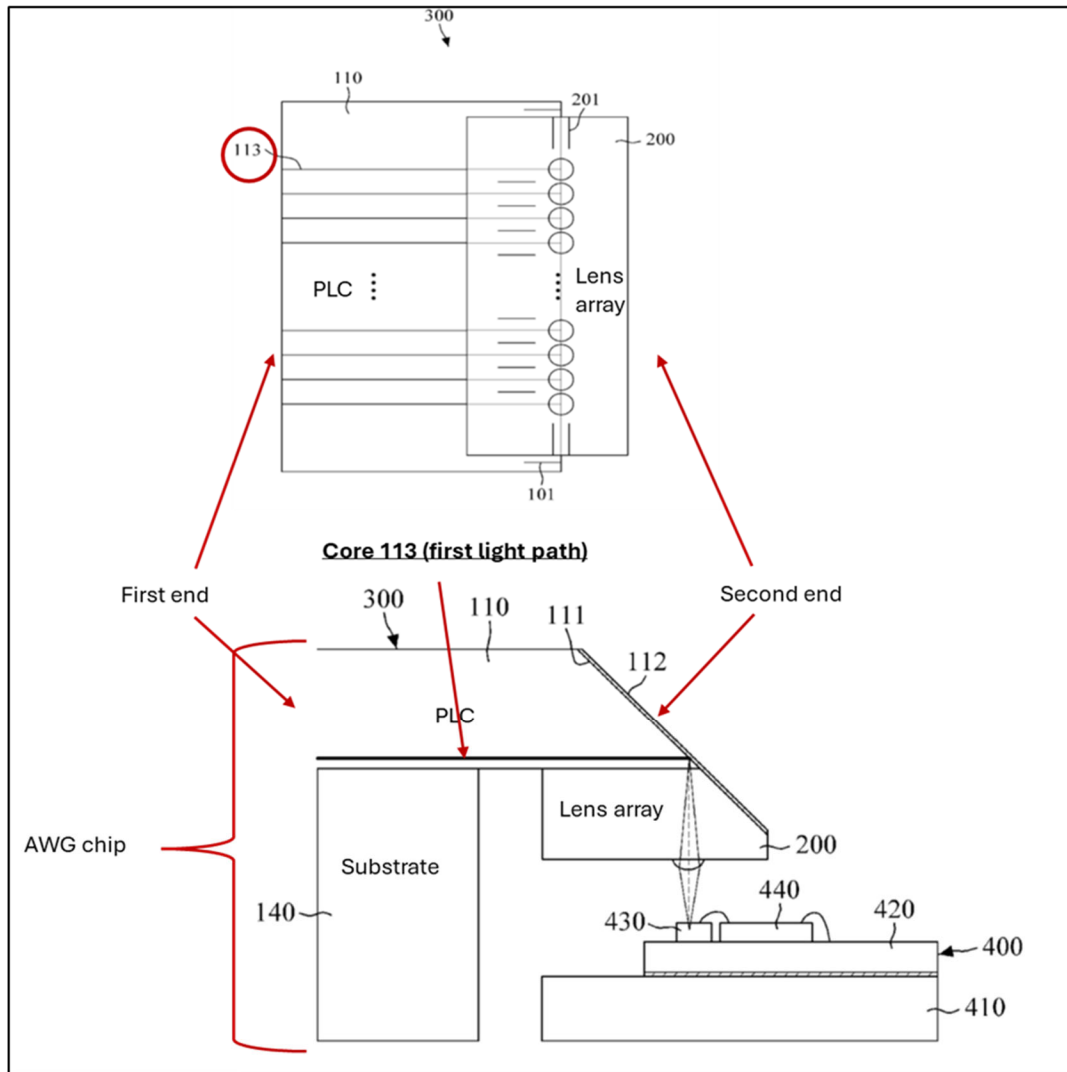
demultiplexer 404, which is connected to four output waveguides 406 coupled with the PLC, with each output waveguide 406 receiving light corresponding to a demultiplexed channel wavelength launched from the AWG 404. Ex. 1008, Fig. 4 (annotated below), 8:61-9:12; 8:1-8. It would have been obvious to a POSITA that the PLC-based AWG demultiplexer of Lee in view of Kim would have output waveguides in cores 113 to pass the demultiplexed light horizontally along separate waveguides towards a second end of the AWG chip to mitigate signal losses and crosstalk amongst the demultiplexed channels. Ex. 1003, ¶85.



Ex. 1008, Fig. 4 (annotations added)

Lee additionally teaches that output light is provided along cores 113 (first light paths) that extend towards a second end of the AWG chip having an inclined

surface 111. Ex. 1003, ¶86. Soldano additionally discloses that the demultiplexed light from the demultiplexer AWG 404 is provided along a first light path that extends towards a second end of the AWG chip having an angle polish 409. *Id.*; Ex. 1008, Figs. 3, 4, 8:1-8.



Ex. 1004, Figs. 2 and 6 (showing output light is provided along cores 113 (first light paths) that extend towards a second end of the AWG chip having an inclined surface 111) (annotations added)

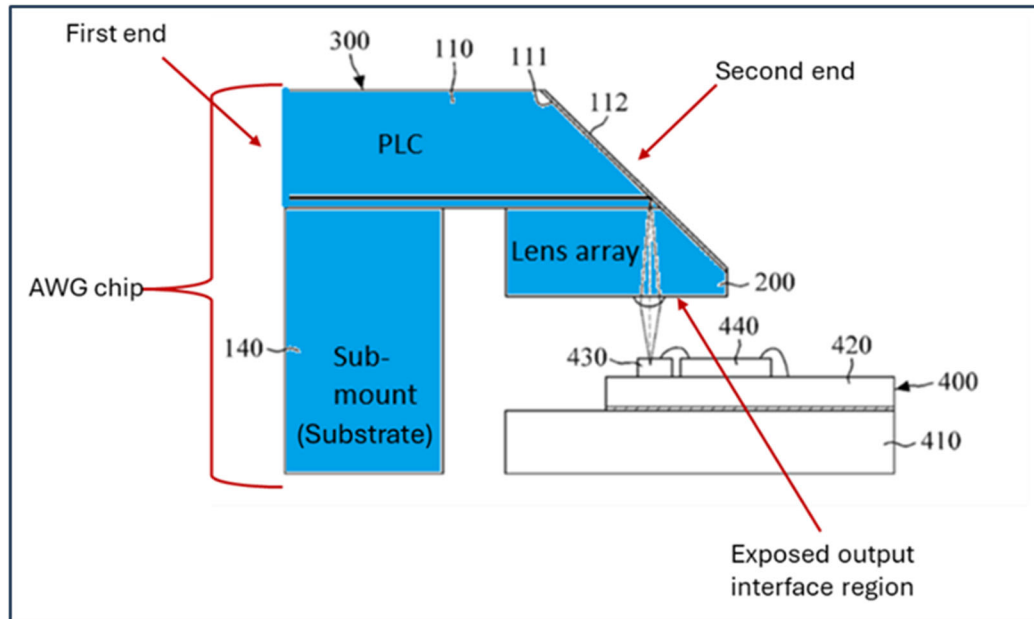
Kim further teaches that “demultiplexer 120 divides the 4-channel optical signal into optical signals corresponding to channels, respectively. ... The demultiplexer 120 transmits the divided optical signal corresponding to each of the channels to a mirror of the optical device 130.” Ex. 1005, ¶[0024]. It would have been obvious to a POSITA based on Kim that each of Lee’s output waveguides (cores 113) receives light corresponding to a demultiplexed channel wavelength launched from PLC 110. Ex. 1003, ¶87.

Thus, Lee in view of Kim discloses a PLC-based AWG demultiplexer that transmits the demultiplexed channels wavelengths through a plurality of output waveguides along a first light path that extends towards a second end of the AWG chip that has an angled/tapered finish. Ex. 1003, ¶88; Ex. 1004, Fig. 2.

f. Claim term 1[e]

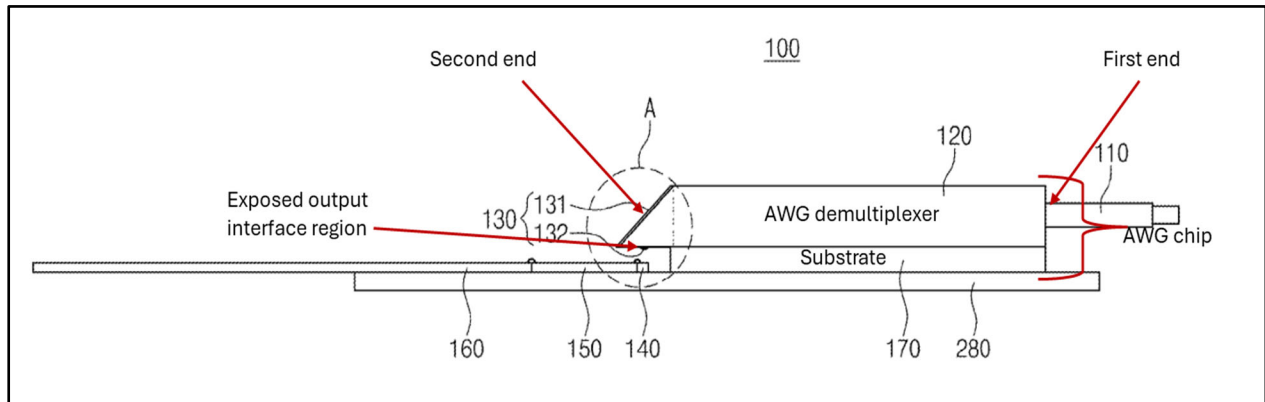
Lee discloses that an optical signal is provided to a second end of the AWG chip, which has a tapered region defined by an inclined surface 111 and a reflection layer 112 formed on the inclined surface. Ex. 1004, Fig. 2, ¶¶[0050], [0051]. Inclined surface 111 receives light via output waveguides (cores 113). Ex. 1003, ¶89. Inclined surface 111 and the reflection layer 112 reflect the received light through an exposed output interface region of the AWG chip, wherein the exposed output interface

region emits the light on the same side as the substrate 140 without passing the light through the substrate. *Id.*, Ex. 1004, Fig. 2.



Ex. 1004, Fig. 2 (annotations added)

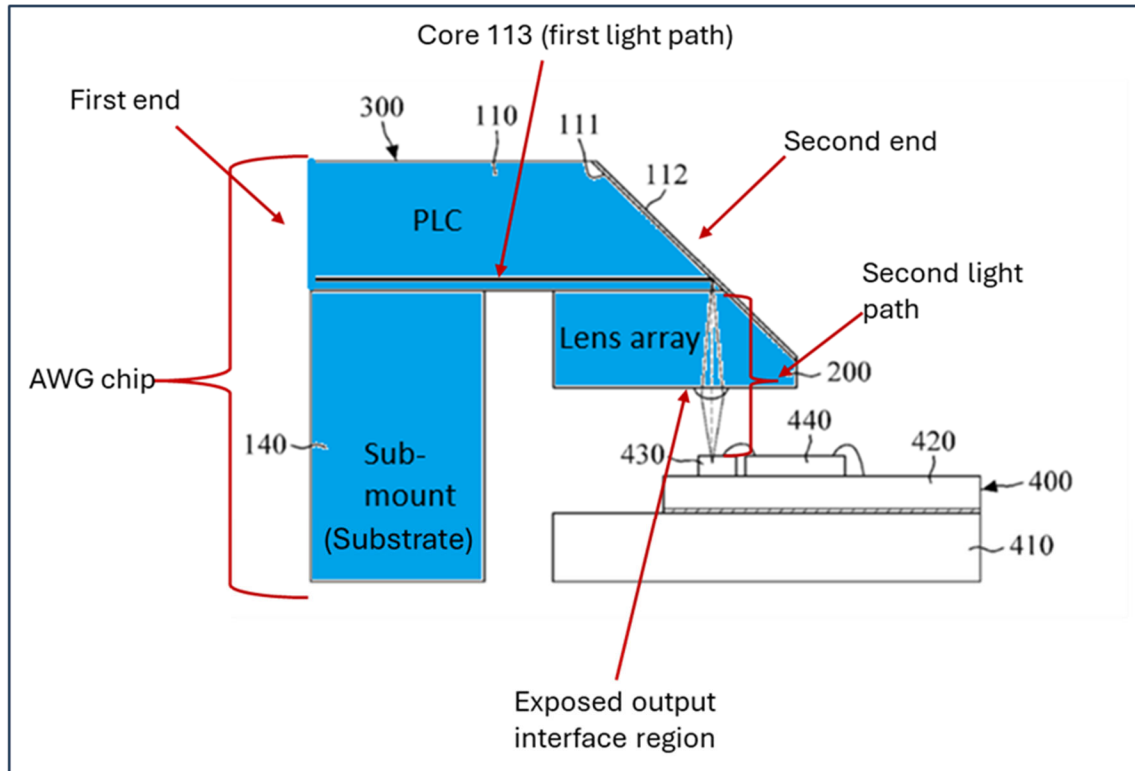
Kim additionally teaches that demultiplexed light is provided to the second end of the AWG demultiplexer 120 having a tapered region defined by an inclined surface 130 and mirror 131 formed on the inclined surface. Ex. 1005, ¶¶[0033]-[0034], Fig. 3. Mirror 131 reflects the demultiplexed light through an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light on the same side as the substrate 170 without passing the received light through the substrate. *Id.*; Ex. 1003, ¶90.



Ex. 1005, Fig. 3 (annotations added)

5. Claim 2

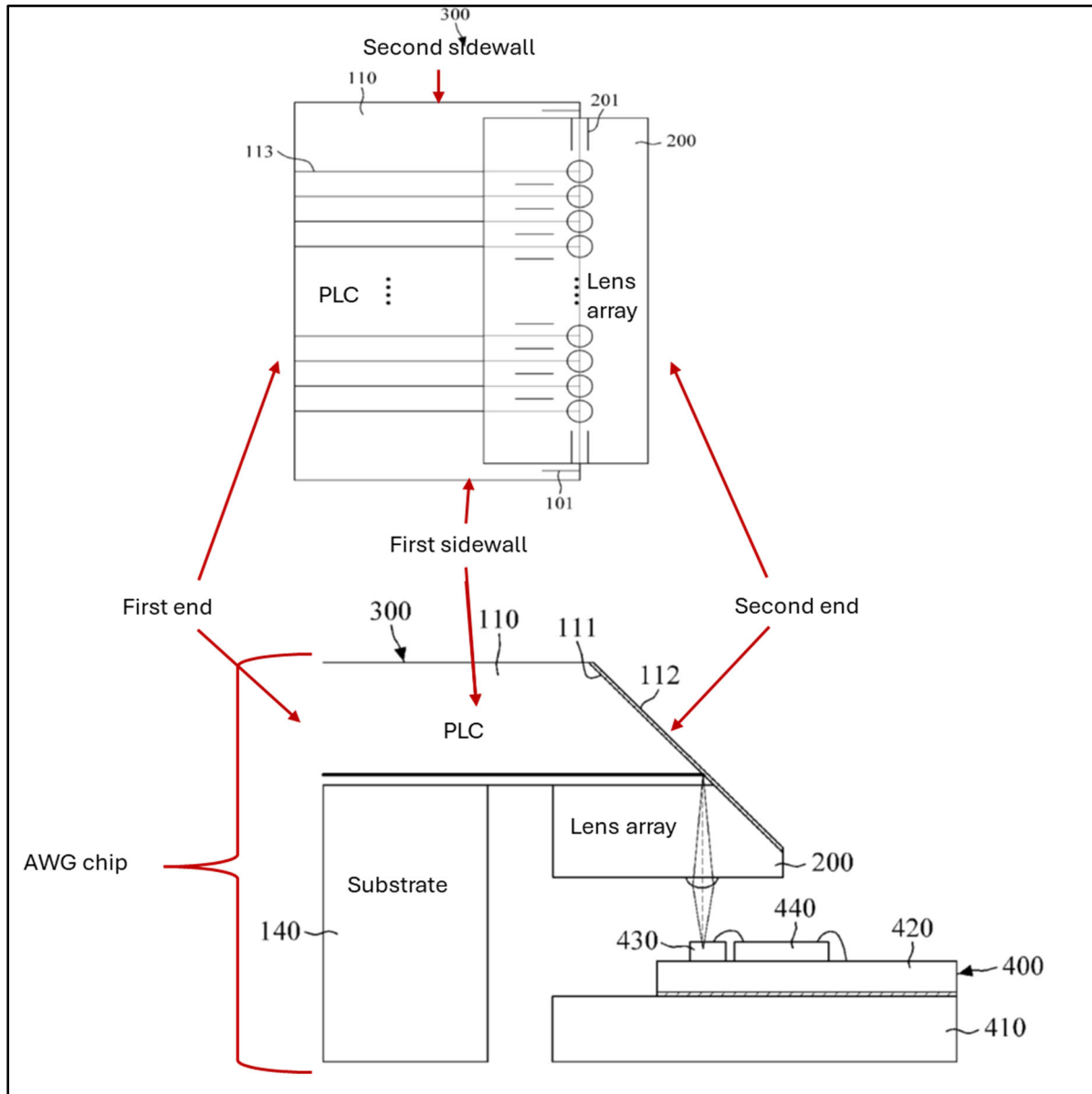
In Lee's AWG chip, the exposed output interface region is configured to reflect light received via the plurality of output waveguides (cores 113) out of the AWG chip along a second light path that is substantially orthogonal to the first light path, as shown in Figure 2. Ex. 1003, ¶¶91, 92.



Ex. 1004, Fig. 2 (annotations added)

6. Claim 3

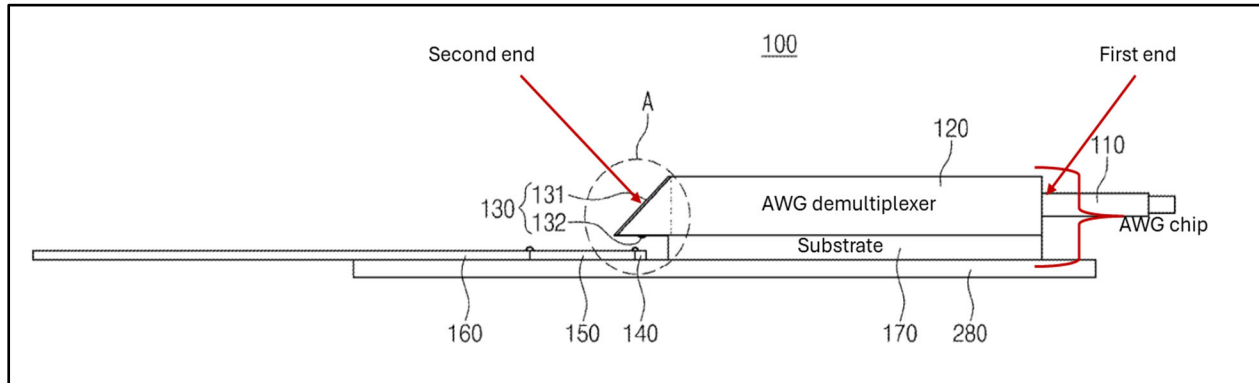
As shown below in Figures 2 and 6 of Lee, annotated below, PLC 110 of Lee's AWG chip includes a plurality of longitudinal sidewalls that extend between the first end and the second end, wherein the tapered region defines an angled surface extending from the first sidewall to the second sidewall. Ex. 1003, ¶93.



Ex. 1004, Fig. 6 (above) and Fig. 2 (below) (annotations added)

Figure 3 of Kim additionally shows that demultiplexer 120 includes a plurality of longitudinal sidewalls that extend between the first end (receiving optical connector 110) and the second end (having optical device 130), wherein the tapered

region defines an angled surface extending from the first sidewall to the second sidewall. Ex. 1003, ¶94.



Ex. 1005, Fig. 3 (annotations added)

7. Claim 4

Both Lee and Kim disclose that the angled surface has an interior angle of about 45 degrees relative to the exposed output interface region. Ex. 1003, ¶¶95, 96. Specifically, Lee discloses that “[t]he angle of the inclined surface 111 [i.e., the angled surface] is most desirably 45 degrees, but not limited to 45 degrees because it is difficult to accurately polish the inclined surface 111 in the actual implementation.” Ex. 1004, ¶[0051]; *see also* Ex. 1005, ¶¶[0033]-[0034] (Kim disclosing that “[a]n end portion of the optical device 130 [i.e., angled surface] may be cut at an angle of 45 degrees[.]”).

Lee’s disclosure that an interior angle of the angled/tapered surface “is most desirably 45 degrees, but not limited to 45 degrees,” which falls within the recited range of about 41 to 45 degrees, renders claim 4 obvious. *See UCB, Inc. v. Actavis*

Labs. UT, Inc., 65 F.4th 679, 687 (Fed. Cir. 2023) (“If the prior art discloses a point within the claimed range, the prior art anticipates the claim.”); *see also Titanium Metals Corp. v. Banner*, 778 F.2d 775, 776-77, 782-83 (Fed. Cir. 1985) (Claims to titanium (Ti) alloy with 0.6-0.9% nickel (Ni) and 0.2-0.4% molybdenum (Mo) were held anticipated and rendered obvious by a graph in a Russian article on Ti-Mo-Ni alloys because the graph contained an actual data point corresponding to a Ti alloy containing 0.25% Mo and 0.75% Ni and this composition was within the claimed range of compositions).

8. Claim 10

Although Lee does not explicitly disclose that the AWG chip is configured as a 1xN demultiplexer device, Kim explicitly discloses that the input signal “**may be 4-channel input optical signals which have four wavelengths different from each other**, respectively. The 4-channel input optical signals may be multiplexed optical signals.” Ex. 1005, ¶[0023] (emphasis added). Kim further discloses that “[t]he demultiplexer 120 divides the 4-channel optical signal into optical signals corresponding to channels, respectively.” *Id.*, ¶[0024] (emphasis added). It would have been obvious to a POSITA that the AWG chip of Lee in view Kim is a 1×N demultiplexer device, wherein a single optical input signal is de-multiplexed into N different channel wavelengths. Ex. 1003, ¶97.

9. Claim 11

The AWG chip of Lee in view of Kim is implemented in a hybrid optical coupling module, which serves as an AWG device package. Ex. 1003, ¶98. A POSITA would have understood that Lee's optical unit 300 (PLC 110 and lens array 200), electrical unit 400 (substrate 420, photo diodes 430, TIAs 440), and submounts 140 and 410 together form Lee's "AWG device package." *Id.*; Ex. 1004, ¶[0016], Fig. 2.

Similarly, Kim also discloses that its AWG demultiplexer 120 is implemented in an optical receiver module 100, i.e., an AWG device package, which includes "an optical connector 110, a demultiplexer 120, an optical device 130, a photodetector 140, a pre-amplifier 150, a printed circuit board 160, a first supporting part 170, and a second supporting part 180." Ex. 1005 ¶[0022].

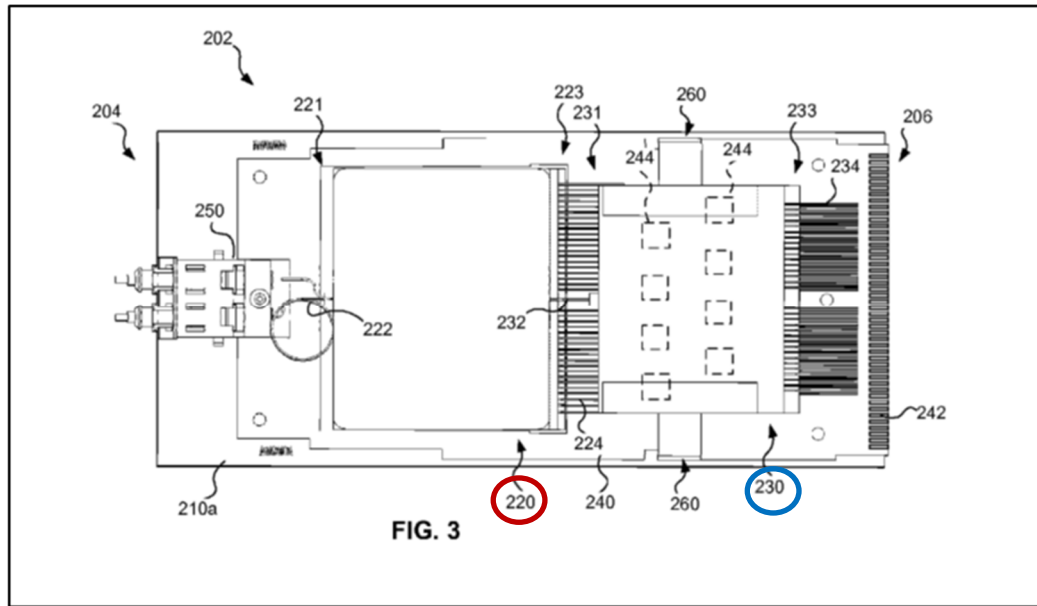
B. [Ground 2] The Group 2 Challenged Claims Are Rendered Obvious by Ho in View of Lee and Kim and Further in View of Yoshikawa

1. Ho (Ex. 1006)

Ho discloses an optical transceiver module for use in a wavelength division multiplexed (WDM) optical system, for example, in an optical line terminal (OLT) in a WDM passive optical network (PON). Ex. 1006, ¶[0018]. Specifically, Ho discloses a WDM-PON 100, which includes at least one OLT 110 coupled to a plurality of optical networking terminals (ONTs) or optical networking units (ONUs) 112-1

$\lambda_{C2}, \dots \lambda_{Cn}$) from an upstream WDM signal. *Id.* The OLT 110 may thus include multi-channel optical transceivers 102a, 102b, and each transceiver may include a multi-channel TOSA 120 for generating and combining the optical signals at the multiple channel wavelengths and a multi-channel ROSA 130 for receiving and separating the optical signals at the multiple channel wavelengths. *Id.*

Ho further discloses an exemplary optical transceiver module 202, as shown in Figure 3 (reproduced below), for use in OLT 110. *See also id.*, Fig. 2, ¶[0033]. Optical transceiver module 202 includes a transceiver housing 210a, 210b containing a multi-channel TOSA 220, a multi-channel ROSA 230, and a dual fiber type direct link adapter 250 directly linked to the TOSA 220 and the ROSA 230 for providing the optical input and output. *Id.* TOSA 220 includes an array of lasers that are coupled to a multiplexer (such as an AWG) 225. *Id.*, ¶[0037]. Each laser generates light at a different channel wavelength and the AWG combines the different channel wavelengths into a single, multiplexed optical signal. *Id.*, ¶¶[0028], [0029], [0037], [0058].

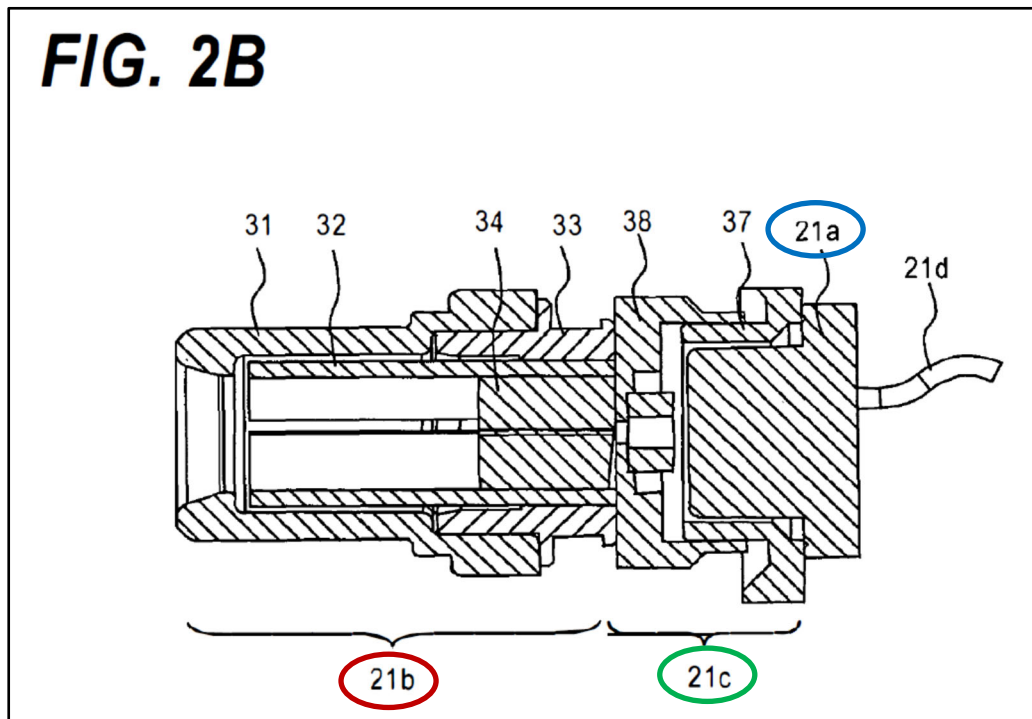


Ex. 1006, Fig. 3 (showing an optical transceiver 202 having a housing portion 210a and including a **TOSA 220** and a **ROSA 230**)

Likewise, ROSA 230 includes an AWG demultiplexer 235. *Id.*, ¶[0042]. The ROSA is configured to receive a WDM optical signal on multiple channel wavelengths and to demultiplex (divide) the WDM signal into individual channel wavelengths. *Id.*, ¶[0057]. Optical outputs 237 of the demultiplexer 235 are “directly optically coupled” to an array of photodetector 236, having photodiodes 270, without any intermediate fibers. *Id.*, ¶¶[0042], [0043]. The outputs of photodetectors 236 are electrically connected to the ROSA pins 234 at the electrical connection end 233 via TIAs (transimpedance amplifiers) 274. *Id.*, ¶¶[0042]-[0045], Fig. 3.

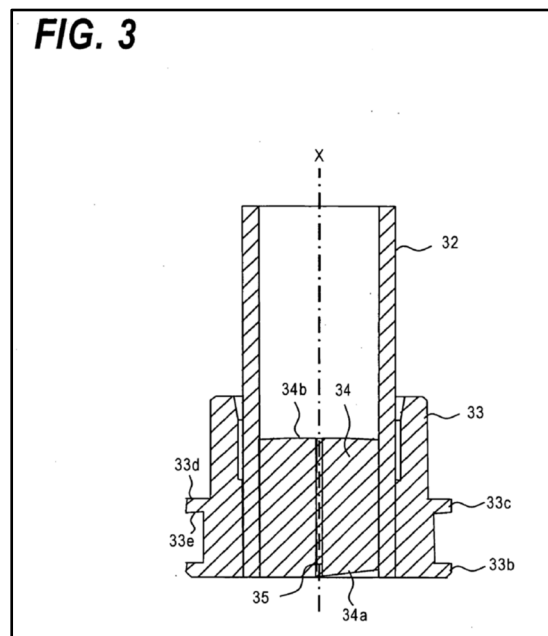
2. Yoshikawa (Ex. 1009)

Yoshikawa discloses an optical transceiver 1 that comprises a TOSA 21 and a ROSA 22, each of which is configured to have a package 21a/22a, a sleeve assembly 21b/22b, and alignment member 21c/22c. Ex. 1009, ¶¶[0036], [0040], Figs. 2A, 2B; *see also id.*, ¶[0039] (noting that same description applies to TOSA 21 and ROSA 22). As shown in Figure 2B, below, “[t]he sleeve assembly 21b includes, from the side of the alignment member 21c, a bush 33, a stub 34, a sleeve 32 and a sleeve cover 31.” *Id.*, ¶[0042].



Ex. 1009, Fig. 2B (showing components of TOSA 21: **package 21a**, **sleeve assembly 21b**, and **alignment member 21c** between the package and the sleeve assembly)

Yoshikawa discloses that “one end surface 34a of the stub 34, i.e., the surface [that] optically couples with the alignment member 21[c] is processed to incline by 5 to 7 degrees to a plane perpendicular to an optical axis X of the sleeve assembly 21b. This arrangement suppresses light emitted from the laser diode in the package 21a from being reflected by this end surface 34a to the direction parallel to the optical axis X. Accordingly, the reflected light is prohibited from entering the laser diode and causing the optical noise source.” Ex. 1009, ¶[0043]; *see also id.*, Fig. 3. A POSITA would have understood that for ROSA 22, the angled junction would prevent back reflection of the optical signal received by package 22a via sleeve assembly 22b. Ex. 1003, ¶71.



Ex. 1009, Fig. 3 (showing surface 34a, which optically couples with alignment member 21c, is at an angle of 5 to 7 degrees)

3. A POSITA would have been motivated to combine Ho with Lee and Kim and further with Yoshikawa, and would have reasonably expected success

Lee discloses an optical component of a transceiver module that “performs optical transmission and reception functions” in an optical communication system. Ex. 1004, ¶¶[0008]-[0009]. Similarly, Ho discloses a multi-channel optical transceiver module 202 comprising a TOSA 220, a ROSA 230, and a direct link adapter 250 for providing optical inputs and outputs. Ex. 1006, ¶[0033]. Therefore, a POSITA would have considered Lee and Ho together when designing an optical transceiver module, such as the one disclosed in the ’116 patent. Ex. 1003, ¶104. Although Lee does not provide many details of a transceiver module, Ho explicitly discloses that the ROSA includes an AWG demultiplexer but does not provide details of the demultiplexer. But a POSITA would have known that it is common to have an AWG demultiplexer in a ROSA to separate a received signal into individual channel wavelengths. *Id.*, ¶103. As discussed above in Section VI.A, Lee and Kim disclose the details of an AWG demultiplexer. Thus, when developing a transceiver module, a POSITA would have been motivated to consider Lee and Kim with Ho to build an efficient and effective transceiver module having a ROSA with an AWG demultiplexer. *Id.*, ¶104. A POSITA would have reasonably expected success in using the AWG chip discussed in Lee (modified in view of Kim) with the ROSA in Ho, and would have been motivated to do so, because of the simple and efficient

method of direct coupling demultiplexed light with respective photodetectors without using optical fibers or waveguides, as discussed in Lee and Kim. *Id.*, ¶107.

Specifically, a POSITA would have recognized that the direct coupling technique disclosed in Lee and Kim provides more efficient, reliable, and effective coupling between the AWG and the photodetectors and minimizes manufacturing concerns associated with the passive alignment requirements outlined in Ho. *Id.* At a minimum, the direct coupling technique described in Lee and Kim is a good alternative to the optical coupling mechanism described in Ho to achieve desired coupling efficiency. *Id.* Furthermore, a POSITA would have readily recognized the design compatibility between the optical module of Lee (modified in view of Kim) and the transceiver of Ho, and would have been motivated to and reasonably expect success in using them together. *Id.* Combining Ho's transceiver module with the AWG chip of Lee and Kim would have required nothing more than ordinary skill and basic knowledge of optical components. *Id.* Indeed, it would have been a combination of known prior art elements according to their established functions, and the combination would have yielded the predictable result of a transceiver with an AWG chip that provides direct optical coupling of the demultiplexed outputs with corresponding photodetectors. *Id.*

A POSITA would also have been motivated to combine the AWG chip of Lee and Kim with Yoshikawa to have an angled junction between the input coupling

receptacle and the AWG chip to reduce back reflections of the input optical signals. *Id.*, ¶109. A POSITA would also have reasonably expected success in providing an angled surface at the first end of the AWG chip of Lee (modified in view of Kim) because such angled junctions were routinely used in optoelectronics and it would have only required the exercise of ordinary skill and knowledge of a POSITA. *Id.*, ¶110.

1. Independent Claim 12

Ho in view of Lee and Kim and further in view of Yoshikawa renders claim 12 obvious.

a. Claim 12[preamble]

Ho discloses a multi-channel optical transceiver module 202. Ex. 1006, ¶[0033]; Ex. 1003, ¶101.

b. Claim term 12[a]

Ho's optical transceiver module 202 includes a transceiver housing 210*a*, 210*b*. Ex. 1006 ¶[0033], Figs. 2 and 3.

c. Claim term 12[b]

Ho discloses a multi-channel ROSA 230 located in the transceiver housing 210*a*, 210*b*. Ex. 1006, ¶[0033]. Ho further discloses that ROSA 230 includes an AWG-type demultiplexer. *Id.*, ¶¶[0042], [0043]. Indeed, a POSITA would have

known that it is common to have an AWG demultiplexer in a ROSA to separate a received signal into individual channel wavelengths. Ex. 1003, ¶103.

Although Ho does not provide details of the AWG within the ROSA, Lee in view of Kim describes a ROSA with an AWG demultiplexer chip. *Id.*, ¶104. Therefore, a POSITA would have considered Ho, Lee, and Kim together when developing an optical transceiver module. *Id.*

Specifically, Lee discloses an optical unit 300 that is mounted on a sub-mount 140 and includes a PLC 110. Ex. 1004, ¶¶[0033], [0035], [0036], [0038], [0043]-[0046]. Lee further discloses that one application of the PLC is an AWG demultiplexer. *Id.*, ¶[0009]. Kim further discloses an AWG demultiplexer 120. Ex. 1005, ¶¶[0022]-[0024]. Lee's optical unit 300 and sub-mount 140, wherein PLC 110 is modified in view of Kim to have an AWG demultiplexer, together form an "AWG chip." Ex. 1003, ¶106.

A POSITA would have reasonably expected success in using the AWG chip of Lee (modified in view of Kim) with the ROSA in Ho, and would have been motivated to do so, because of the simple, reliable, and efficient method of direct coupling demultiplexed light with respective photodetectors without using optical fibers or waveguides, as discussed in Lee and Kim. Ex. 1003, ¶107.

d. Claim term 12[c]

Although Lee does not expressly disclose how the AWG chip receives an optical signal, a POSITA would have understood that Lee's AWG chip necessarily has a first end that couples with an optical connector to receive an input signal. Ex. 1003, ¶108. Kim explicitly discloses an AWG chip having an optical connector 110, which "receives an optical signal inputted through a single optical fiber and then transmits the optical signal to the demultiplexer 120." Ex. 1005, ¶[0023]. Optical connector 110 of Kim has a "pigtail-shape or a receptacle-shape." *Id.*, ¶[0023], Fig. 3. Kim additionally discloses that "the optical signal may be 4-channel input optical signals which have four wavelengths different from each other, respectively. The 4-channel input optical signals may be multiplexed optical signals. The 4-channel input optical signals are transmitted to the optical connector 110 through the single optical fiber." *Id.* Thus, Kim discloses an AWG demultiplexer 120 having a first end for coupling to an optical connector 110, which may be implemented as an optical coupling receptacle, to receive an optical signal comprising a plurality of channel wavelengths. *Id.*

Although neither Lee nor Kim discloses that the first end of the AWG chip that couples to the optical coupling receptacle includes an angled surface, such angled surfaces for reducing back reflection of incoming light were well known when the '116 patent application was filed. Ex. 1003, ¶109. Yoshikawa (Ex. 1009), for

example, discloses an optical connector receptacle (formed by sleeve assembly 21b/22b) of a TOSA 21 or ROSA 22, wherein one end 34a of stub (ferrule) 34 that interfaces with the optical elements of the TOSA/ROSA is “processed to incline by 5 to 7 degrees to a plane perpendicular to an optical axis X of the sleeve assembly 21b [or 22b].” Ex. 1009, ¶¶[0039], [0043]. This arrangement suppresses light from being reflected by the end surface 34a in the direction parallel to the optical axis X. *Id.* It would have been obvious to a POSITA to provide an angled junction between the first end of the AWG chip of Lee and the optical coupling receptacle of Kim—by having an inclined surface at the first end of Lee’s AWG chip—to prevent back reflection of the input optical signal comprising a plurality of channel wavelengths. Ex. 1003, ¶¶109-110.

Indeed, angled junctions between optical components to reduce back reflections were routinely used in optoelectronic components, as discussed in US 5,351,327 to Lurie et al. (Ex. 1011), 1:35-41. *Id.*, ¶110. By 2010, angled physical contact (APC) connectors polished at $\sim 8^\circ \pm 1^\circ$ were universal in optics to suppress back reflections. *Id.*, ¶109. Accordingly, a POSITA would have been motivated to provide an angled surface at the first end of the AWG chip of Lee to reduce back reflection of the optical signal received via Kim’s optical coupling receptacle 110. Ex. 1003, ¶110.

e. Claim term 12[d]

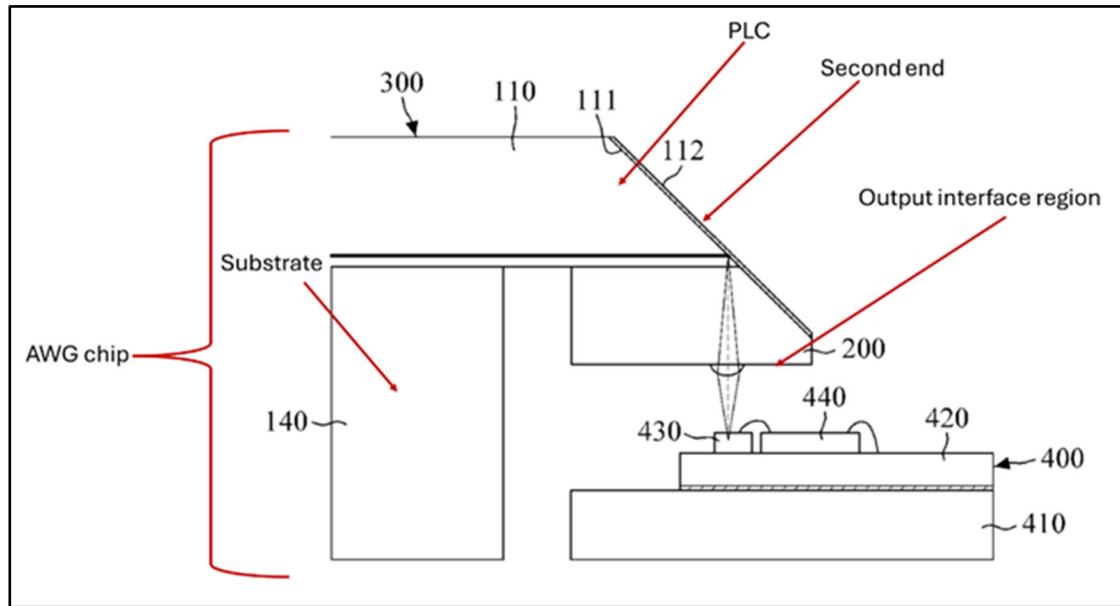
Claim element 12[d] is similar to 1[c]. As discussed in Section VI.A.4.d regarding 1[c], the AWG chip of Lee in view of Kim includes a PLC that is coupled to the first end of the AWG chip and is configured to demultiplex each channel wavelength of the plurality of channel wavelengths. Ex. 1003, ¶111.

f. Claim term 12[e]

Claim element 12[e] is identical to 1[d]. As discussed in Section VI.A.4.e regarding 1[d], Lee in view of Kim discloses the limitation of 12[e]. Ex. 1003, ¶112.

g. Claim term 12[f]

The AWG chip of Lee includes a tapered region disposed at the second end of the AWG chip, as shown in Lee Figure 2, below. Ex. 1003, ¶113. The second end of the AWG chip is configured to receive light via a plurality of output waveguides, as discussed with reference to claim terms 1[d] and 12[e], above. The light received by the second end is reflected towards an output interface region of the AWG chip. Ex. 1004, Fig. 2 (showing light from the AWG is reflected down by the inclined surface 111 into an array of photodiodes 430 through an output interface region of the AWG chip).



Ex. 1004, Fig. 2 (annotations added)

Kim additionally teaches that demultiplexed light is provided to the second end of the AWG demultiplexer 120 having a tapered region that reflects the demultiplexed light through an exposed output interface region of the AWG chip. Ex. 1005 ¶¶[0033]-[0034]; Ex. 1003, ¶114.

h. Claim term 12[g]

Lee discloses an array of photodiodes (PD) 430, which are a type of photodetector, adjacent to the output interface region of the AWG chip to convert the optical signals to electrical signals. Ex. 1004, Figs. 2, 8; Ex. 1003, ¶115.

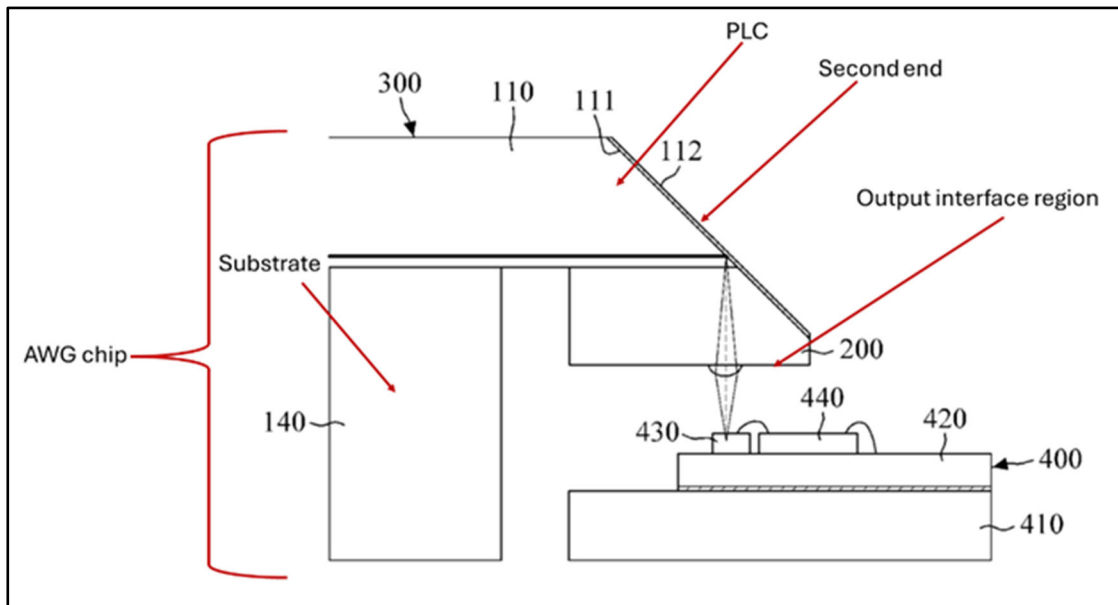
Kim also discloses an array of photodetectors 140 adjacent to the output interface region of the AWG demultiplexer 120. Ex. 1005, Fig. 3, ¶[0028]; Ex. 1003, ¶116.

i. Claim term 12[h]

Ho's optical transceiver module 202 includes a multi-channel TOSA 220 within the transceiver housing 210a, 210b. Ex. 1006, ¶[0033]. TOSA 220 includes an array of lasers coupled to an AWG multiplexer 225. *Id.*, ¶[0037]. The array of lasers generates and transmits optical signals at different channel wavelengths. *Id.*, ¶¶[0028], [0029]. Ho also incorporates by reference U.S. Application No. 13/708,569 (U.S. Patent Pub. No. 2014/0161457) (hereinafter Ex. 1010), which describes a similar TOSA 220 in more detail. *Id.*, ¶[0037]. As discussed in Ex. 1010 at ¶¶[0034]-[0035], TOSA 220 includes an array of lasers 226-1 to 226-n coupled to AWG 225, and "[e]ach laser 226-1 may be provided as a laser package including, but not limited to, a laser diode chip mounted on a laser mounting structure. The laser package may also include optical components, such as a lens for optically coupling the laser light into a respective one of the optical fibers, and/or optoelectronic components, such as a monitor photodiode." It would have been obvious to a POSITA that the lasers of TOSA 220 in Ho generate and transmit optical signals at different channel wavelengths. Ex. 1003, ¶117. Indeed, it was common knowledge to a POSITA that TOSAs include lasers modulated to transmit optical signals at different channel wavelengths. *Id.*

2. Claim 13

Lee discloses that the output interface region of the AWG chip is an exposed region adjacent an air gap that separates the output interface region and the array of PDs 430. Ex. 1004, Fig. 2; Ex. 1003, ¶118.



Ex. 1004, Fig. 2 (annotations added)

Kim also discloses that the output interface region of AWG demultiplexer 120 is an exposed region adjacent an air gap that separates the output interface region and the array of photodetectors 140. Ex. 1005, Fig. 3; Ex. 1003, ¶119.

3. Claim 15

As discussed above regarding claim 3 (Section VI.A.6), which is identical to claim 15, Lee discloses the limitations of claim 15. Ex. 1003, ¶120.

4. Claim 16

As discussed above in Section VI.A.7 regarding claim 4, which is identical to claim 16, Lee discloses that the angled surface at the second end has an interior angle of about 45 degrees relative to the output interface region of the AWG chip to reflect light orthogonally onto photodiodes 430. Ex. 1004, ¶[0051]. Kim also discloses an AWG demultiplexer chip having an inclined end surface of 45 degrees to effectively couple demultiplexed light reflected by the inclined surface with corresponding photodetectors 140. Ex. 1005, ¶[0034]. A POSITA would have known to design an AWG chip with an angled surface having an interior angle in the range of about 41-45 degrees, based on Lee and Kim, and through routine experimentation and design considerations, to optimize the direct coupling of demultiplexed light with respective photodetectors. Ex. 1003, ¶122; *see also* Section VI.A.7, above.

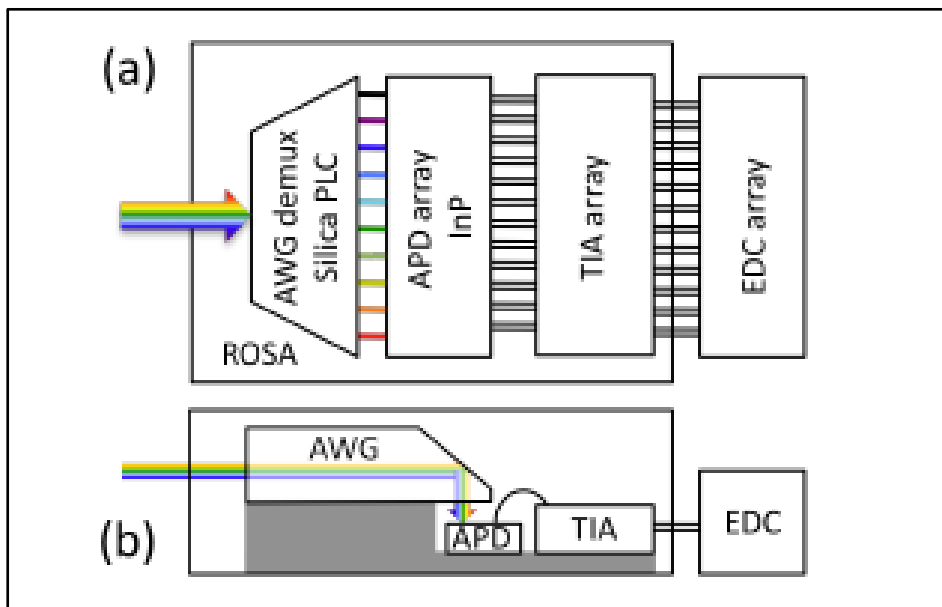
VII. BERNASCONI-BASED GROUNDS

A. [Ground 3] The Group 1 Challenged Claims Are Rendered Obvious by Bernasconi in View of Soldano

1. Bernasconi (Ex. 1007)

Bernasconi discloses a hybrid-integrated photonic circuit having “10-channel parallel transmitter and receiver optical subassemblies (TOSA & ROSA) with an integrated capacity of 107 Gbps.” Ex. 1007, pg. 1 col. 1. The TOSA and ROSA include “arrays of DFB lasers and avalanche photodiodes (APD) combined with silica arrayed waveguide gratings as multi-demultiplexer.” *Id.* The ROSA comprises

“[f]ree-space collimating optics” to “feed the incoming stream into a silica AWG demultiplexer that separates the 100-GHz spaced channels.” *Id.*, pg. 2 col. 1. The AWG includes a PLC circuit for demultiplexing and an angled facet on one end redirecting the demultiplexed light onto an array of APDs. *Id.* “By careful control of the design of the optical path from the AWG facet to the APDs,” the circuit “achieve[s] high coupling without having to add any intermediate lenses.” *Id.* Bernasconi’s circuit design thus “allows for the use of low-loss, low-crosstalk, PLC-based demultiplexers combined with high-sensitivity III-V-based APDs.” *Id.*

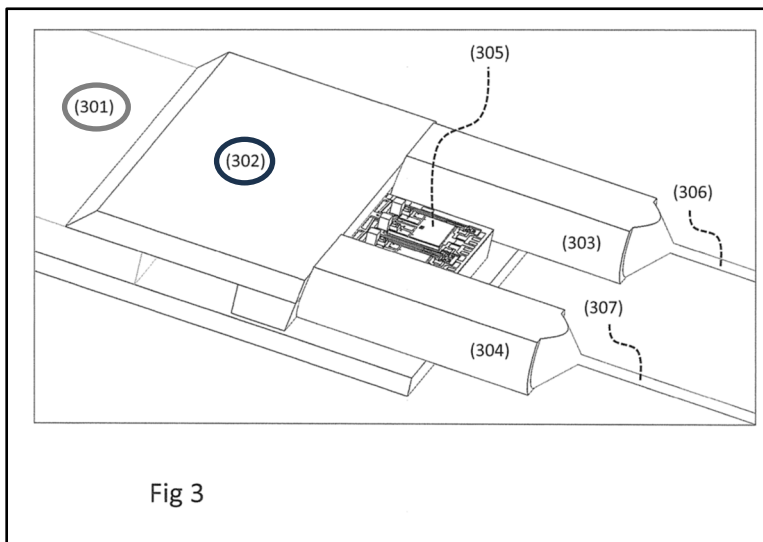


Ex. 1007, Fig. 2 (showing ROSA schematic, top view (a) and side view (b)).

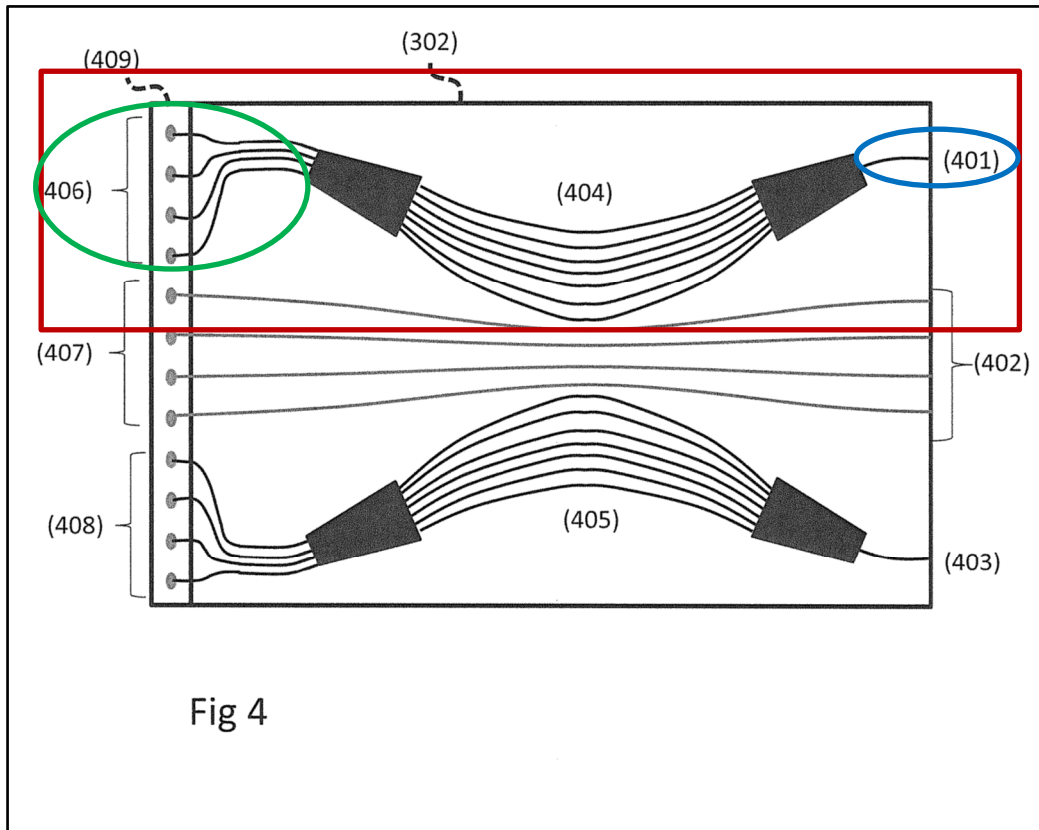
2. Soldano (Ex. 1008)

Soldano discloses a method of coupling light in and out of silicon photonics chips by using AWG-based demultiplexers in glass PLCs to divide multiple

wavelength light into individual channels. Ex. 1008, 2:64-3:5, 3:17-25; Ex. 1003, ¶67. Specifically, Soldano discloses a photonic integrated circuit chip having a silicon photonics substrate 301 and a PLC 302, which includes an AWG demultiplexer 404 to demultiplex an optical signal carrying many modulated channel wavelengths into N individual channels. Ex. 1008, 7:24-8:28, Figs. 3-5; Ex. 1003, ¶67.



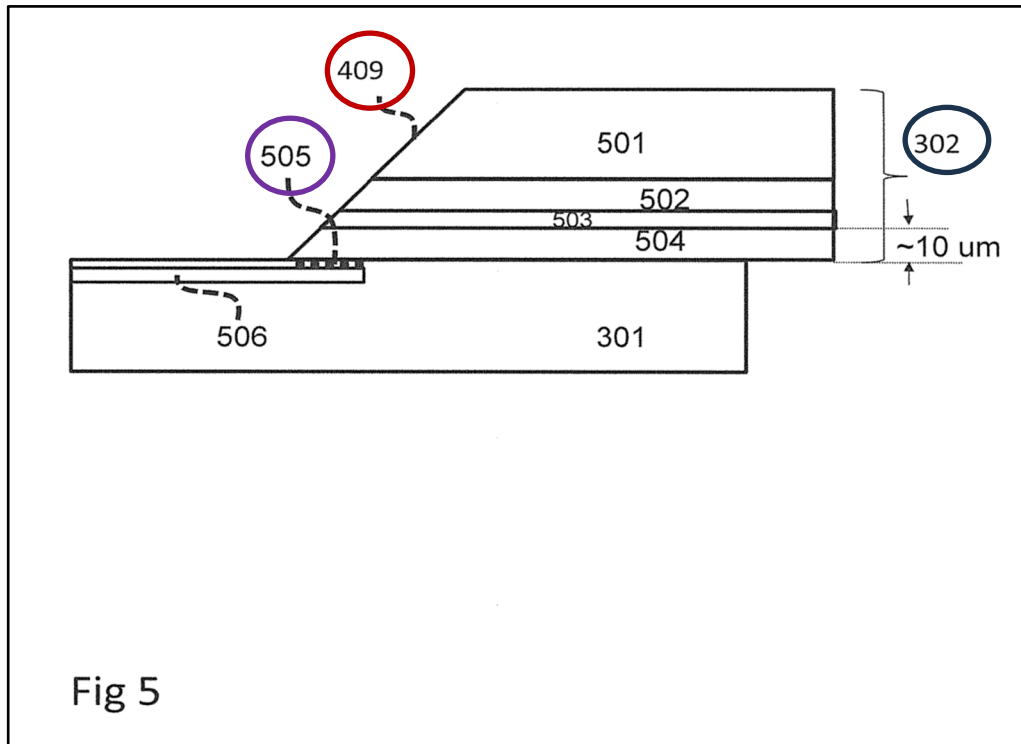
Ex. 1008, Fig. 3 (showing Soldano's photonic integrated circuit chip having a **substrate 301** and a **PLC 302**)



Ex. 1008, Fig. 4 (showing PLC 302 includes **demultiplexer AWG 404**, which is connected to **an input waveguide 401** on one end and **four output waveguides 406** at the other end); Ex. 1003, ¶67

Soldano further discloses that PLC 302 includes an inclined region defined by an angle polish 409. Ex. 1008, Fig. 5, 8:8-20, 9:15-37. Demultiplexed light is reflected downwards by angle polish 409 into a grating coupler 505, which is a periodic grating etched onto the surface of waveguide 506. *Id.*, Fig. 5, 9:28-37, 9:58-10:9. Soldano further teaches that instead of using a grating coupler 505,

demultiplexed light may be received by a photodetector array 601 provided on substrate 301 to convert the light into electrical signals. *Id.*, 10:10-19, Fig. 5; Ex. 1003, ¶168.



Ex. 1008, Fig. 5 (showing PLC 302 having an **angled end 409** to reflect demultiplexed light onto a **grating coupler 505** or photodetector array 601)

3. A POSITA would have been motivated to combine Bernasconi and Soldano, and would have reasonably expected success

Bernasconi and Soldano are in the same field of optoelectronics, specifically photonic integrated circuits having AWG multiplexers and demultiplexers. Ex. 1007, pg. 1 col. 1; Ex. 1008, Ex. 2:64-3:5, 3:17-25; Ex. 1003, ¶130. Therefore, a

POSITA would have considered Bernasconi and Soldano together when designing or developing an AWG chip, such as the one disclosed in the '116 patent, to optically couple an AWG demultiplexer chip with a photodetector array for optical-to-electrical conversion. Ex. 1003, ¶¶128, 130.

Bernasconi discloses every aspect of the claimed invention of the '116 patent, except an input coupling receptacle and output waveguides. But a POSITA would have known that in place of free-space collimating optics as taught by Bernasconi, the input signal may be provided through an optical connector that couples with the first end of the AWG chip, such as the one taught by Soldano. *Id.*, ¶129. And a POSITA would have been motivated to use an optical connector having a receptacle or a pigtail-shape, instead of using free-space collimating optics, to reduce or mitigate signal losses caused by misalignment, vibrations, and pointing inaccuracies of free-space optical connections when transmitting the multi-wavelength input signal to the AWG chip. *Id.*, ¶¶129, 130.

Relatedly, although Bernasconi does not explicitly disclose a plurality of output waveguides coupled to the PLC to receive demultiplexed light launched from the PLC, a POSITA would have known that demultiplexed light from the PLC would have been passed along output waveguides corresponding to each channel wavelength, as taught by Soldano, because that is how AWG-based demultiplexing is commonly implemented to avoid cross-talk between the channels. Ex. 1008, Fig. 4,

8:61-9:12, 8:1-8; Ex. 1003, ¶139. It would have been obvious to a POSITA to implement output waveguides in the PLC-based AWG demultiplexer of Bernasconi (in view of Soldano) to pass the demultiplexed light along separate waveguides towards a second end of the AWG chip to mitigate signal losses and cross-talk amongst the demultiplexed channels. Ex. 1003, ¶141.

A POSITA would also have reasonably expected success in combining Bernasconi with Soldano, and it would have required nothing more than the application of ordinary skill and basic knowledge of optical components. Ex. 1003, ¶142. Combining Bernasconi with an input coupling receptacle and output waveguides, as disclosed in Soldano, would have been a combination of known prior art elements according to their established functions, and the combination would have yielded the predictable result of an AWG chip with efficient and effective direct coupling of the demultiplexed output with photodetectors. *Id.*

4. Independent Claim 1

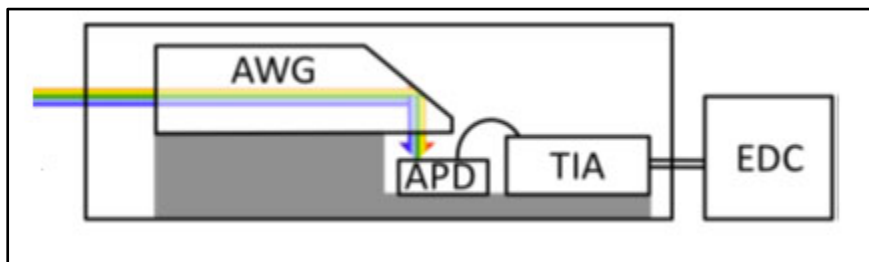
Bernasconi in view of Soldano renders claim 1 obvious.

a. Claim 1[preamble]

Bernasconi discloses an arrayed waveguide grating (AWG) chip. Ex. 1003, ¶124. Specifically, Bernasconi discloses “10-channel parallel transmitter and receiver optical sub-assemblies (TOSA & ROSA) with an aggregated capacity of 107 Gbps. [The TOSA and ROSA] consist of arrays of DFB lasers and avalanche

photodiodes (APD) combined with silica arrayed waveguide gratings as multi-demultiplexers.” Ex. 1007, pg. 1 col. 1; *see also id.*, pg. 2 col. 1.

Bernasconi further discloses that “[t]he APDs [avalanche photodiodes], the linear TIAs [transimpedance amplifiers] and all the passive electronic components are assembled on the base ceramic substrate.” Ex. 1007, pg. 2 col. 1, Fig. 2(b) (showing the AWG demultiplexer, APD, and TIA mounted on the ceramic base). The AWG demultiplexer and the ceramic base together form an “AWG chip” because it includes AWG functionality and structure Ex. 1003, ¶126.

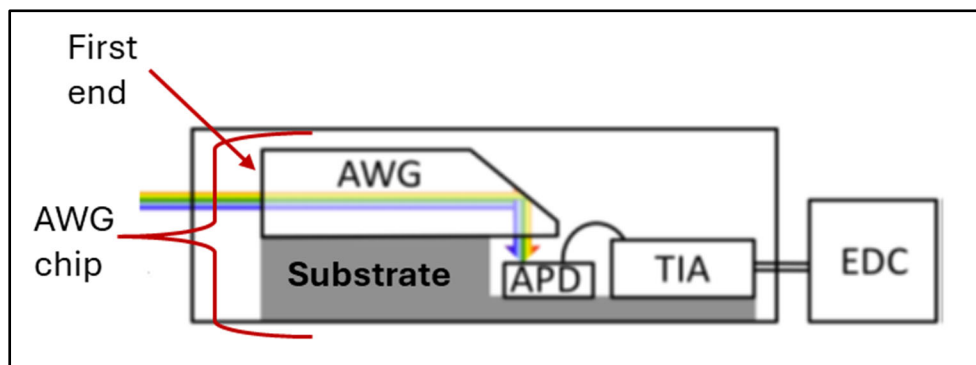


Ex. 1007, Fig. 2(b) (showing sideview of ROSA schematic)

Soldano discloses a photonic integrated circuit chip having a silicon photonics substrate 301 and a PLC 302, which includes an AWG demultiplexer. Ex. 1008, 7:24-8:28, Figs. 3-5. Soldano’s substrate 301 and PLC 302 form an “AWG chip.” Ex. 1003, ¶127.

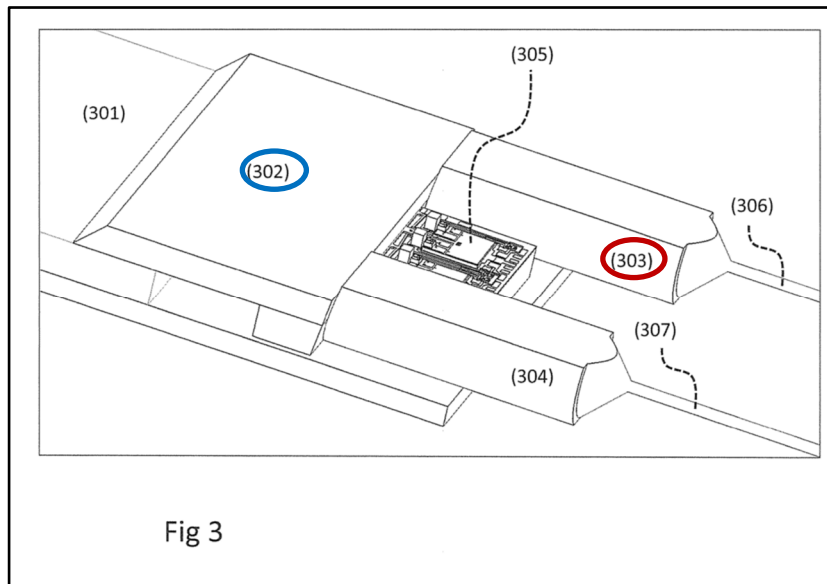
b. Claim term 1[a]

Bernasconi's AWG chip has a first end that receives an incoming optical signal through "[f]ree-space collimating optics" and feeds it into the AWG demultiplexer. Ex. 1007, pg. 2 col. 1, Fig. 2. Bernasconi also discloses that the incoming optical signal has 10-channels that are spaced 100-GHz apart. *Id.*, pg. 1 col. 1, pg. 2 col. 2, Fig. 2(a) (showing that the ROSA demultiplexes the multi-wavelength input optical signal into ten separate output channels). A POSITA would have understood that in place of free-space collimating optics, the multi-wavelength optical signal may be inputted through an optical connector that couples with the first end of the AWG chip, as taught by Soldano, to provide a more reliable and secure physical link and to minimize signal losses caused by, for example, misalignment of the free-space optics. Ex. 1003, ¶129.



Ex. 1007, Fig. 2(b) (annotations added)

For example, the AWG chip of Soldano has a first end that couples to an optical coupling receptacle 303 that receives from a fiber 306 an optical signal comprising a plurality of channel wavelengths. Ex. 1008, 7:29-35, 7:62-65, Fig. 3.



Ex. 1008, Fig. 3 (showing that a first end of **PLC 302** is coupled to an **optical coupling receptacle 303** to receive a multiwavelength optical signal from fiber 306)

It would have been obvious to a POSITA to modify the first end of the AWG chip of Bernasconi to couple to an optical coupling receptacle, such as the optical coupling receptacle 303 of Soldano, to receive a multiwavelength input optical signal from a fiber with minimal losses and cross-talk. Ex. 1003, ¶132.

c. Claim term 1[b]

The AWG chip of Bernasconi includes a substrate, specifically, a ceramic base on which the AWG, APDs, and TIAs are mounted. Ex. 1007, pg. 2 col. 1, Fig. 2(b).

The ceramic based provides support to the AWG and is part of the AWG chip. *Id.* The AWG chip of Soldano also includes a substrate, specifically, a silicon photonics chip 301. Ex. 1008, 7:29-35, 8:8-10, Figs. 3 and 5.

d. Claim term 1[c]

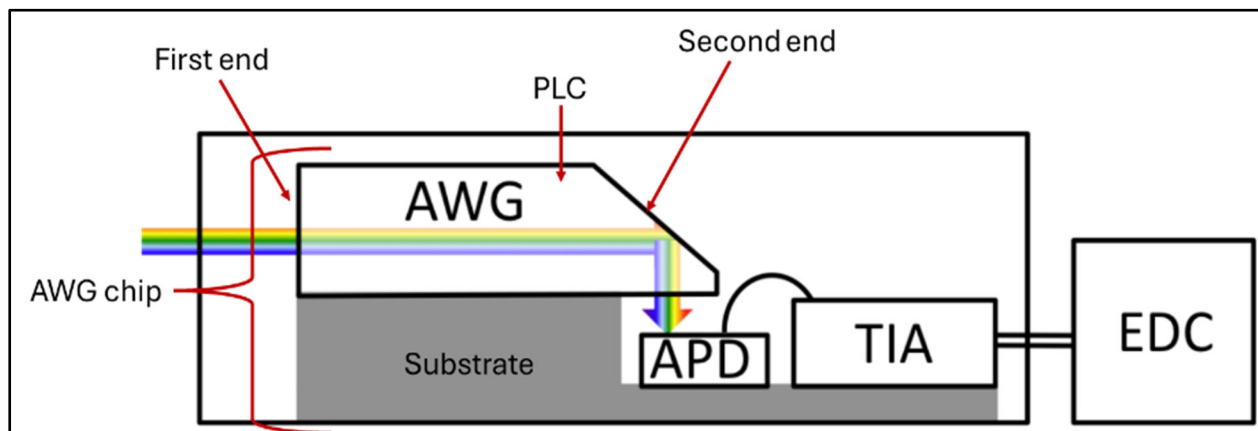
The AWG chip of Bernasconi includes a planar lightwave circuit (PLC) disposed on the substrate (ceramic base), wherein the PLC is coupled to the first end of the AWG chip and configured to demultiplex each channel wavelength of the plurality of channel wavelengths. Ex. 1003, ¶135.

Specifically, Bernasconi discloses that its AWG demultiplexer is a PLC, which is mounted on the ceramic substrate, and is coupled to the first end of the AWG chip. Ex. 1007, pg. 2 col. 1 (“hybrid integration allows for the use of low-loss, low-crosstalk, PLC-based demultiplexers combined with high-sensitivity III-V-based APDs.”), pg. 2 col. 1 (disclosing “a silica AWG demultiplexer that separates the 100-GHz spaced channels.”), Fig. 2(a) (stating AWG demultiplexer is a “Silica PLC”). Bernasconi further discloses that the PLC-based AWG demultiplexer is configured to demultiplex the incoming optical signal carrying 10 modulated channel wavelengths into individual channels. Bernasconi, pg. 2 col. 2, Fig. 2(a) (showing that the AWG demultiplexes the multi-wavelength input signal into 10 separate output channels); Ex. 1003, ¶136.

Soldano also discloses a PLC 302 disposed on substrate 301. Ex. 1008, Fig. 3, 8:8-10. The PLC is coupled to the optical coupling receptacle 303 at the first end, as shown in Figure 3. The PLC is configured to demultiplex the multiwavelength light carrying many modulated channel wavelengths into individual channels. *Id.*, 7:62-8:1; Ex. 1003. ¶137.

e. Claim term 1[d]

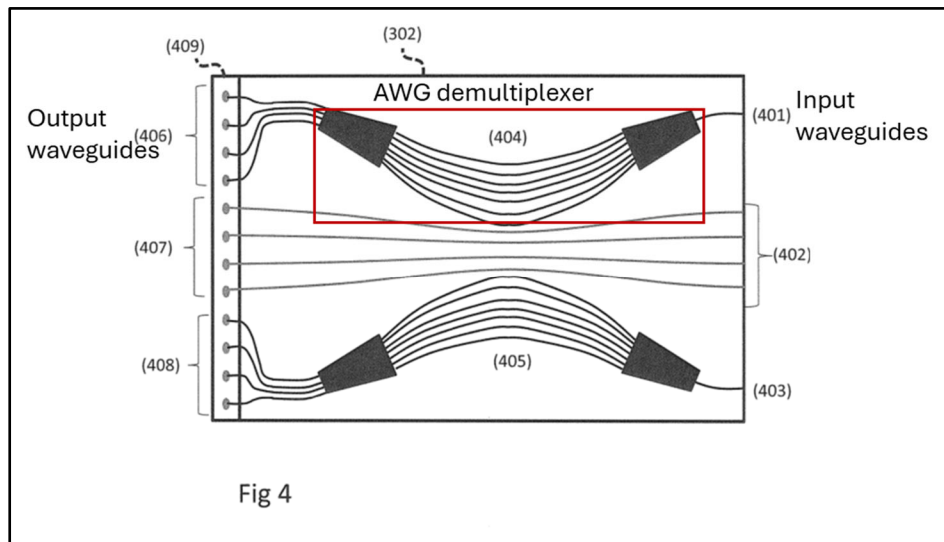
Bernasconi discloses a PLC-based demultiplexer that transmits the demultiplexed channels along a first light path that extends towards a second end of the AWG chip that has an angled/tapered finish. Ex. 1007, Fig. 2(b); Ex. 1003, ¶138.



Ex. 1007, Fig. 2(b) (annotations added)

Although Bernasconi does not explicitly disclose a plurality of output waveguides coupled to the PLC to receive demultiplexed light launched from the PLC, a POSITA would have known that demultiplexed light from the PLC would have been passed along separate output waveguides corresponding to each channel wavelength,

because that is how AWG-based demultiplexing is commonly implemented to avoid cross-talk between the channels. Ex. 1003, ¶139. Moreover, other prior art references explicitly disclose such output waveguides. For example, Soldano discloses a PLC 302 having a demultiplexer AWG 404, which is connected to four output waveguides 406 coupled with the PLC, with each output waveguide 406 receiving light corresponding to a demultiplexed channel wavelength launched from the AWG 404. Ex. 1006, Fig. 4, 8:61-9:12, 8:1-8, Ex. 1003, ¶139.



Ex. 1008, Fig. 4 (annotations added)

Soldano additionally discloses that the demultiplexed light from the demultiplexer AWG 404 is provided along a first light path that extends towards a second end of the AWG chip having an angle polish 409. *Id.*, Fig. 3, Fig. 4, 8:1-8 (“The four channels are then in four separate waveguides, each waveguide carrying one wavelength of light. **The waveguides terminate, in the embodiment of FIG. 3, at the**

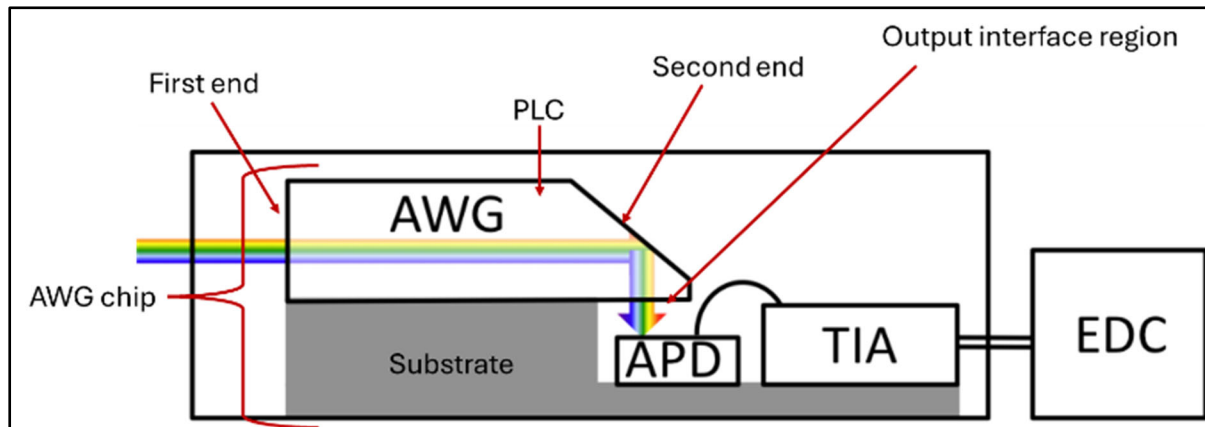
other end of the PLC. In some embodiments the other end of the PLC includes a structure for directing, or deflecting, this light down into the silicon photonics chip 301.”) (emphasis added).

It would have been obvious to a POSITA to implement output waveguides in the PLC-based AWG demultiplexer of Bernasconi (in view of Soldano) to pass the demultiplexed light along separate waveguides towards a second end of the AWG chip to mitigate signal losses and cross-talk among the demultiplexed channels. Ex. 1003, ¶141.

f. Claim term 1[e]

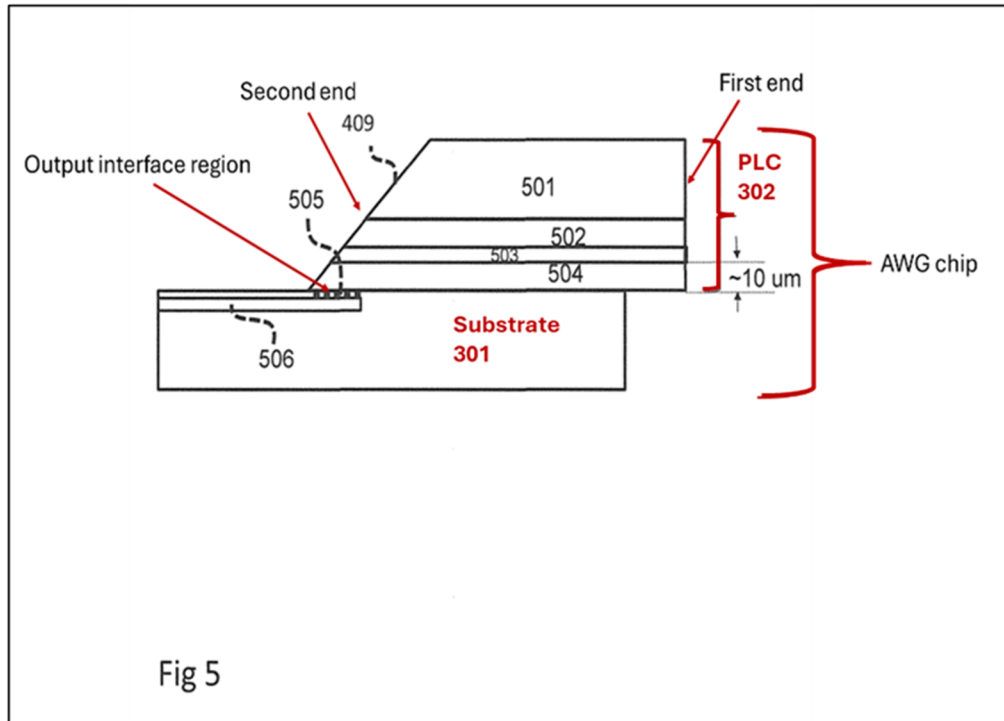
The AWG chip of Bernasconi includes a tapered region disposed at the second end of the AWG chip, as shown in Bernasconi’s Figure 2(b), below. The second end of the AWG chip is configured to receive light via a plurality of output waveguides in view of Soldano, as discussed with reference to claim term 1(d), above. The light received by the second end is reflected towards an exposed output interface region of the AWG chip, and wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate. Ex. 1007, Fig. 2(b) (showing demultiplexed light from the AWG is reflected down by the turning mirror at the second end into an array of APDs through an exposed output interface region, which emits the received light to the APD on the same side as the ceramic substrate without passing the light

through the substrate); *see also id.*, pg. 2 col. 1 (“An external turning mirror redirects the light onto an array of APDs. By careful control of the design of the optical path from the AWG facet to the APDs, we achieve high coupling without having to add any intermediate lenses.”); Ex. 1003, ¶143.



Ex. 1007, Fig. 2(b) (annotations added).

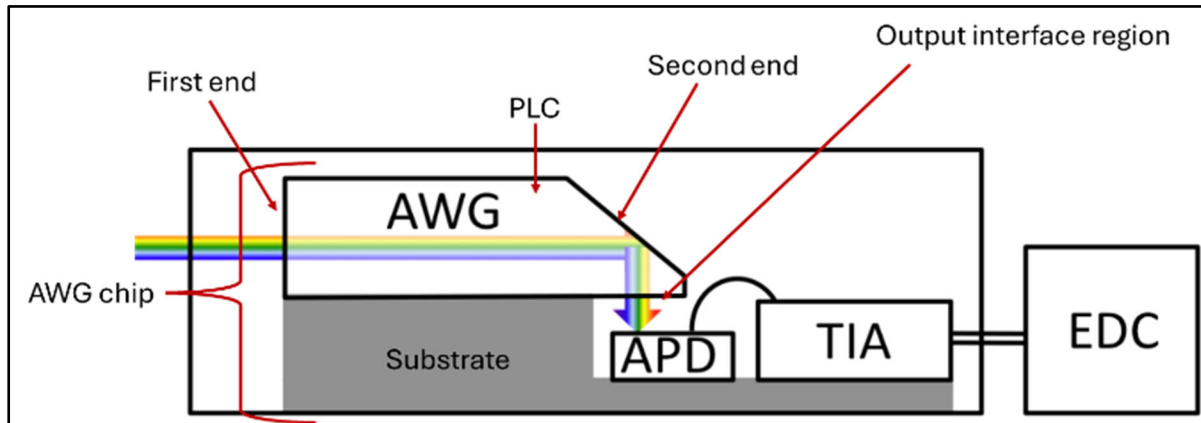
Soldano additionally discloses that demultiplexed light from PLC 302 is transmitted via output waveguides 406 to a second end of the AWG chip having a tapered region defined by an angle polish 409. Ex. 1008, Fig. 3, Fig. 4, 8:1-8, 9:15-37. Soldano further teaches that light from output waveguides 406 is reflected downward by angle polish 409 through an output interface region of PLC 302 onto a grating coupler 505, which is a periodic grating etched onto the surface of waveguide 506 provided in substrate 301. *Id.*, Fig. 5, 9:28-37, 9:58-10:9.



Ex. 1008, Fig. 5 (annotations added)

5. Claim 2

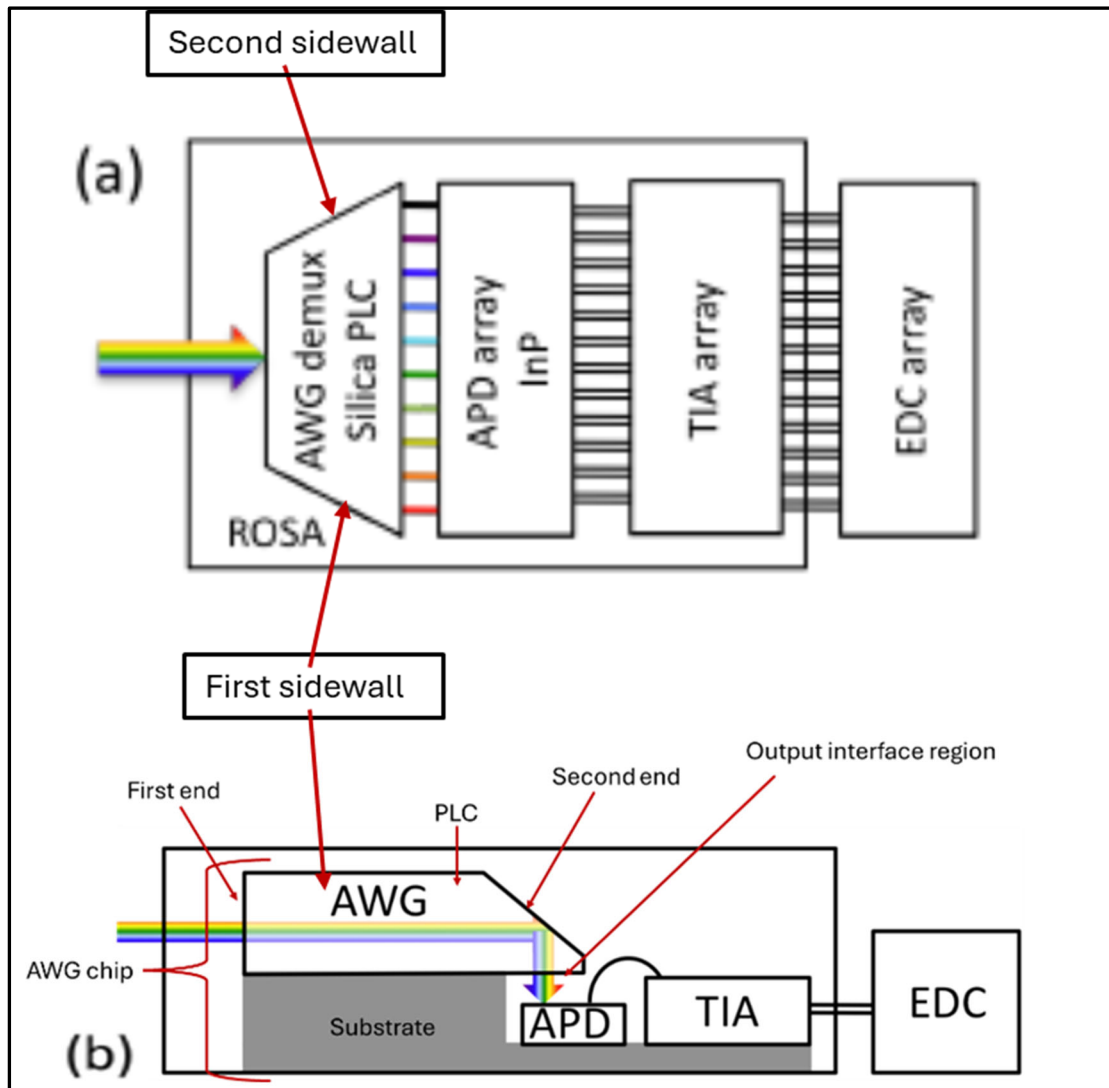
In Bernasconi's AWG chip modified in view of Soldano, the exposed output interface region is configured to pass light reflected by the tapered end along a second light path that is substantially orthogonal to the first light path of the output waveguides. Ex. 1007, Fig. 2(b); Ex. 1003, ¶145. Specifically, Bernasconi discloses that light from the AWG demultiplexer is reflected downward by the turning mirror at the second end and into an array of APDs through an exposed output interface region of the AWG chip along a second light path that is substantially orthogonal to the first light path. Ex. 1007, pg. 2 col. 1; Ex. 1003, ¶145.



Ex. 1007, Fig. 2(b) (annotations added)

6. Claim 3

As shown in Figures 2(a) and 2(b), annotated below, the AWG chip of Bernasconi includes at least two longitudinal sidewalls that extend between the first end and the second end of the AWG chip, and wherein the tapered region defines an angled surface extending from the first sidewall to the second sidewall. Ex. 1003, ¶146.



Ex. 1007, Figs. 2(a) and 2(b), (annotated)

7. Claim 4

Although Bernasconi does not explicitly disclose the interior angle of the tapered second end of the AWG chip, a POSITA would have understood from Figure 2(b) of Bernasconi that the tapered/angled surface at the second end has an interior angle of about 41 to 45 degrees relative to the exposed output interface region of the

AWG chip to effectively reflect light onto the APDs. Ex. 1003, ¶147. Indeed, another prior art reference, Kim (Ex. 1005), explicitly discloses an AWG demultiplexer chip having an inclined end surface of 45 degrees to effectively reflect the demultiplexed light onto the corresponding photodetectors 140. Ex. 1005, ¶[0034]. Specifically, as discussed above in Section VI.A.2, Kim discloses an AWG demultiplexer 120 having a tapered region defined by an inclined optical device 130 having mirror 131. *Id.*, ¶¶[0033]-[0034], Fig. 3. The mirror 131 reflects the light through an exposed output interface region of the demultiplexer onto a photodetector array 140. *Id.*, ¶¶[0033]-[0034] (“An end portion of the optical device 130 may be cut at an angle of 45 degrees and then the cut surface of the optical device 130 may be polished. Subsequently, a silica-based material may be coated on one side of the optical device 130 to form the mirror 131.”). Kim’s disclosure of an inclined surface of 45 degree at the second (output) end of an AWG demultiplexer renders claim 4 obvious. *See UCB, Inc.*, 65 F.4th at 687; *Titanium Metals*, 778 F.2d at 776-77, 782-83.

Moreover, a POSITA would have known that having the angle of the tapered second end in the range of about 41 to 45 degrees relative to the exposed output interface region is an obvious design choice and obvious-to-try based on multiple considerations, as discussed below. Ex. 1003, ¶148.

Specifically, a POSITA would have known the physics of internal reflection and that the ability of the AWG chip to effectively reflect light onto the

photodetectors depends on the interior angle of the tapered/angled surface relative to the exposed output interface region. Ex. 1003, ¶149. That is, the interior angle of the tapered/angled surface relative to the exposed output interface region is a result-effective variable that affects the reflection of light onto the photodetectors. *Id.* And the law is clear that the determination of the optimum range of a result-effective variable is within the grasp of a POSITA. *In re Boesch*, 617 F.2d 272, 276 (C.C.P.A. 1980) (“[D]iscovery of an optimum value of a result effective variable ... is ordinarily within the skill of the art.”). Moreover, the ’116 patent does not show that “the claimed ranges are ‘critical’ or ‘produce a new and unexpected result which is different in kind and not merely in degree from the results of the prior art.’” *In re Applied Materials, Inc.*, 692 F.3d 1289, 1295, 1297 (Fed. Cir. 2012) (quoting *In re Aller*, 220 F.2d 454, 456 (C.C.P.A. 1955)); *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1322 (Fed. Cir. 2004). Therefore, optimization of the interior angle of the tapered/angle surface was nothing other than the exercise of ordinary skill in the art. *In re Huang*, 100 F.3d 135, 139 (Fed. Cir. 1996); *Iron Grip*, 392 F.3d at 1322.

Indeed, a POSITA would have known to design an AWG chip with a tapered surface having a suitable interior angle, e.g., an angle in the range of about 41-45 degrees, based on Bernasconi and Soldano, and through routine experimentation and design considerations, to optimize the direct coupling of demultiplexed light with

respective photodetectors. Ex. 1003, ¶150. For example, based on Kim, a POSITA would have known how to adjust interior angle for other AWG demultiplexers using routine experimentation and design considerations to effectively reflect light onto photodetectors. *Id.* Thus, the recited range of about 41 to 45 degrees would have been obvious to a POSITA. *Id.*

8. Claim 10

Bernasconi discloses that its AWG chip is configured to demultiplex multi-wavelength light carrying many modulated channel wavelengths into individual channels, i.e., a single input optical signal is demultiplexed into N different channel wavelengths. Ex. 1007, pg. 2 col. 2 (“Free-space collimating optics (not shown) feed the incoming stream into a silica AWG demultiplexer that separates the 100-GHz spaced channels.”), pg. 3 col. 2 (discussing “10-channel” demultiplexer), Fig. 2(a) (showing incoming light demultiplexed into 10 channels). A POSITA would thus have understood that the AWG chip of Bernasconi is configured as a $1 \times N$ demultiplexer. Ex. 1003, ¶151.

9. Claim 11

The AWG chip of Bernasconi is implemented in an AWG device package, specifically in a ROSA, as shown in Figs. 2(a) and 2(b). Ex. 1007, pg. 2 col. 2. Bernasconi further describes that a ROSA is part of “10-channel parallel transmitter and receiver optical subassemblies (TOSA & ROSA) with an aggregated capacity

of 107 Gbps. [The TOSA and ROSA] consist of arrays of DFB lasers and avalanche photodiodes (APD) combined with silica arrayed waveguide gratings as multi-demultiplexers.” *Id.*, pg. 1 col. 1. A POSITA would thus have understood that the AWG chip of Bernasconi is implemented in an AWG device package. Ex. 1003, ¶152.

B. [Ground 4] The Group 2 Challenged Claims Are Rendered Obvious by Ho in View of Bernasconi and Further in View of Soldano

1. A POSITA would have been motivated to combine Ho with Bernasconi and Soldano, and would have reasonably expected success

Bernasconi discloses a hybrid-integrated photonic circuit having “10-channel parallel transmitter and receiver optical subassemblies (TOSA & ROSA) with an integrated capacity of 107 Gbps.” Ex. 1007, pg. 1 col. 1. Similarly, Ho discloses a multi-channel optical transceiver module 202 comprising a TOSA 220, a ROSA 230, and a direct link adapter 250 directly linked to the TOSA and the ROSA for providing optical inputs and outputs. Ex. 1006, ¶[0033]. Therefore, a POSITA would have considered Bernasconi and Ho together when designing or developing an optical transceiver module, such as the one disclosed in the ’116 patent. Ex. 1003, ¶¶158, 159. Although Bernasconi does not provide many details of a transceiver module, Ho explicitly discloses that the transceiver comprises a ROSA and a TOSA. Ex. 1006, ¶[0033]. Ho further discloses that the ROSA includes an AWG demultiplexer, but does not provide details of the demultiplexer. Ex. 1003, ¶156. But a POSITA

would have known that it is common to have an AWG demultiplexer in a ROSA to separate a received signal into individual channel wavelengths. *Id.* As discussed above in Section VII.A, Bernasconi and Soldano disclose the details of an AWG demultiplexer. Ex. 1003, ¶157. Thus, when designing a transceiver module having a ROSA, a POSITA would have been motivated to consider Bernasconi and Soldano with Ho to build an efficient and effective transceiver module having a ROSA with an AWG demultiplexer. *Id.* A POSITA would have reasonably expected success in using the AWG chip discussed in Bernasconi (modified in view of Soldano) with the ROSA in Ho, and would have been motivated to do so, because of the simple and efficient method of direct coupling demultiplexed light with respective photodetectors without using optical fibers or waveguides, as discussed in Bernasconi and Soldano. *Id.*, ¶158.

Combining Ho's transceiver module with the AWG chip of Bernasconi and Soldano would have required nothing more than the application of ordinary skill and basic knowledge of optical components. Ex. 1003, ¶¶159, 160. Indeed, combining Ho with Bernasconi and Soldano would have been a combination of known prior art elements according to their established functions, and the combination would have yielded the predictable result of a transceiver with an AWG chip that provides efficient and reliable direct optical coupling of the demultiplexed outputs with corresponding photodetectors. *Id.*

A POSITA would also have been motivated to combine the AWG chip of Bernasconi and Soldano with Yoshikawa to have an angled junction between the input coupling receptacle and the AWG chip to reduce back reflections of the input optical signals. Ex. 1003, ¶¶163-164. A POSITA would also have reasonably expected success in providing an angled surface at the first end of the AWG chip of Bernasconi (modified in view of Soldano) because such angled junctions were routinely used in optoelectronics and it would have only required the exercise of ordinary skill and knowledge of a POSITA. *Id.*, ¶164.

2. Independent Claim 12

Ho in view of Bernasconi and Soldano and further in view Yoshikawa renders claim 12 obvious.

a. Claim 12[preamble]

Ho discloses a multi-channel optical transceiver module 202. Ex. 1006, ¶[0033]; Ex. 1003, ¶154.

b. Claim term 12[a]

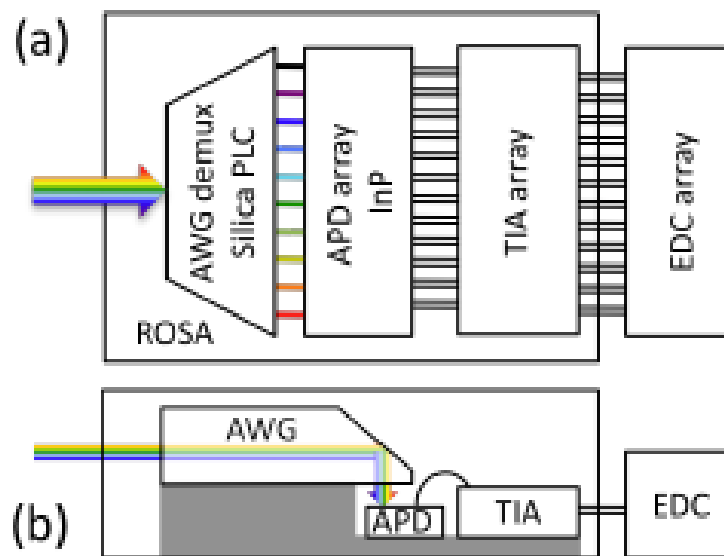
Ho's optical transceiver module 202 includes a transceiver housing 210a, 210b. Ex. 1006, ¶[0033], Figs. 2 and 3.

c. Claim term 12[b]

Ho discloses a multi-channel ROSA 230 located in the transceiver housing 210a, 210b. Ex. 1006, ¶[0033]. Ho further discloses that ROSA 230 includes an

AWG-type demultiplexer. *Id.*, ¶¶[0042], [0043]. Indeed, a POSITA would have known that it is common to have an AWG demultiplexer in a ROSA to separate a received signal into individual channel wavelengths for optical-to-electrical conversion and amplification. Ex. 1003, ¶156.

Although Ho does not provide details of an AWG chip within the ROSA, Bernasconi describes a ROSA with an AWG demultiplexer chip. Ex. 1007, Fig. 2.



Ex. 1007, Fig. 2 (showing top and side views of a ROSA with an AWG demultiplexer chip).

A POSITA would have reasonably expected success in using the AWG chip of Bernasconi with ROSA 230 in Ho, and would have been motivated to do so, because of the simple and efficient method of direct coupling demultiplexed light with

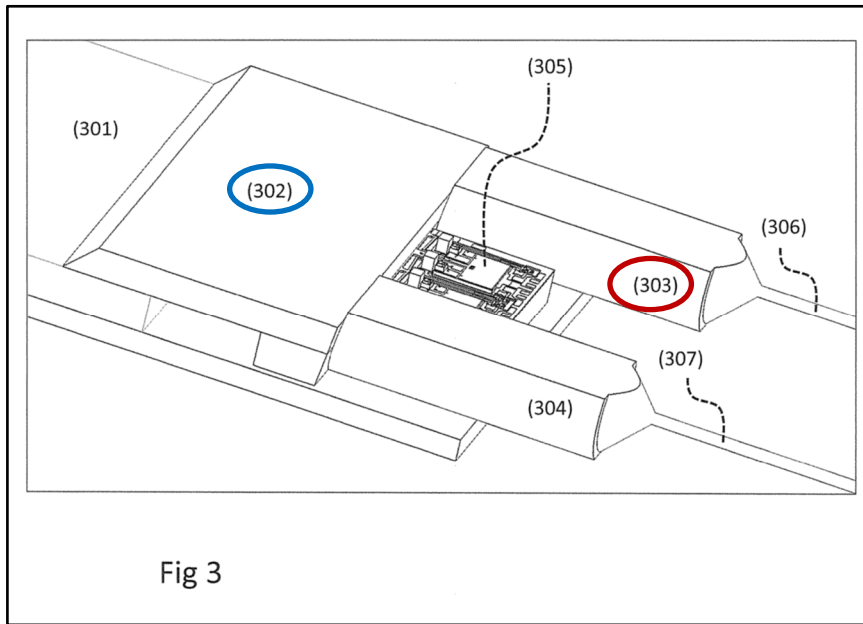
respective photodetectors without using optical fibers or waveguides, as discussed in Bernasconi. Ex. 1003, ¶158; *see also id.*, ¶¶159, 160.

d. Claim term 12[c]

Although Ho does not provide details of the AWG chip, Bernasconi in view of Soldano describes a ROSA with an AWG chip. *See* Section VII.A.4, above. A POSITA would have reasonably expected success in using the AWG chip discussed in Bernasconi (modified in view of Soldano to have an input coupling receptacle and output waveguides) with the ROSA of Ho and would have been motivated to do so because of the simple and efficient method of coupling light in and out of the AWG as discussed in Bernasconi. Ex. 1003, ¶161.

Specifically, the AWG chip of Bernasconi has a first end that receives an incoming multiwavelength optical signal stream through “[f]ree-space collimating optics” and feeds it into a silica AWG demultiplexer. Ex. 1007, pg. 2 col. 1, Fig. 2. A POSITA would have understood that in place of free-space collimating optics, optical fibers including an optical coupling receptacle could have been used, and a POSITA would have been motivated to do so with a reasonable expectation of success to reduce or mitigate signal losses. Ex. 1003, ¶162; *see* Section VII.A.4.b, above. For example, Soldano discloses an AWG chip having a first end that couples to a capillary (optical coupling receptacle) 303 to receive an optical signal comprising a plurality of channel wavelengths through fiber 306. Ex. 1008, 7:29-35, 7:62-

65, Fig. 3. It would have been obvious to a POSITA to use the optical coupling receptacle 303 of Soldano with the AWG chip of Bernasconi to provide a secure physical link and to mitigate signal losses caused by misalignment, vibrations, and pointing inaccuracies of free-space optical connections. Ex. 1003, ¶162.



Ex. 1008, Fig. 3 (showing coupling between optical **coupling receptacle 303** and **PLC 302**)

Although neither Bernasconi nor Soldano discloses that the first end of the AWG chip that couples to the optical coupling receptacle includes an angled surface, such angled/inclined surfaces for reducing back reflection of incoming light were well known when the '116 patent application was filed. Yoshikawa (Ex. 1009), for example, discloses an optical connector receptacle (formed by sleeve assembly 21b/22b) of a TOSA 21 or ROSA 22, wherein one end 34a of stub (ferrule) 34 that

interfaces with the optical elements of the TOSA/ROSA is “processed to incline by 5 to 7 degrees to a plane perpendicular to an optical axis X of the sleeve assembly 21b [or 22b].” Ex. 1009, ¶¶[0039], [0043]. This arrangement suppresses light from being reflected by the end surface 34a in the direction parallel to the optical axis X. *Id.* It would have been obvious to a POSITA to provide an angled junction between the first end of the AWG chip of Bernasconi and the optical coupling receptacle of Soldano—by having an inclined surface at the first end of Bernasconi’s AWG chip—to prevent back reflection of the input optical signal comprising a plurality of channel wavelengths. Ex. 1003, ¶163.

Indeed, angled junctions between optical components to reduce back reflections of received optical signals were routinely used in optoelectronic components. *See, e.g.*, U.S. Pat. No. 5,351,327 to Lurie et al. (Ex. 1010), 1:35-41 (citing other prior art references). Accordingly, a POSITA would have been motivated to provide an angled surface at the first end of the AWG chip of Bernasconi to reduce back reflection of the optical signal received via Soldano’s optical coupling receptacle 303. Ex. 1003, ¶164.

e. Claim term 12[d]

As shown in Section VII.A.4.d discussing 1[c], which is similar to 12[d], the AWG chip of Bernasconi includes a PLC that is coupled to the first end of the AWG

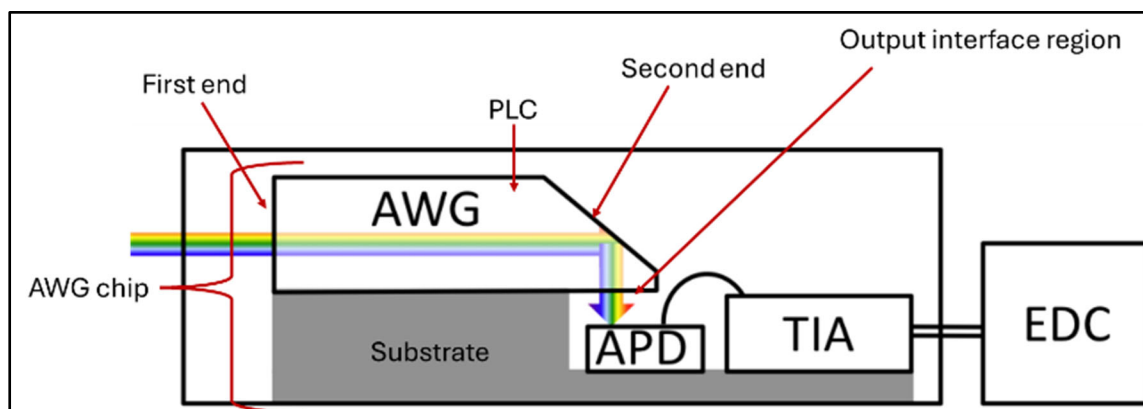
chip and is configured to demultiplex each channel wavelength of the plurality of channel wavelengths. Ex. 1003, ¶165.

f. Claim term 12[e]

Claim element 12[e] is identical to 1[d]. As discussed above with respect to claim term 1[d] (Section VII.A.4.e), Bernasconi in view of Soldano discloses the limitations of 12[e]. Ex. 1003, ¶166.

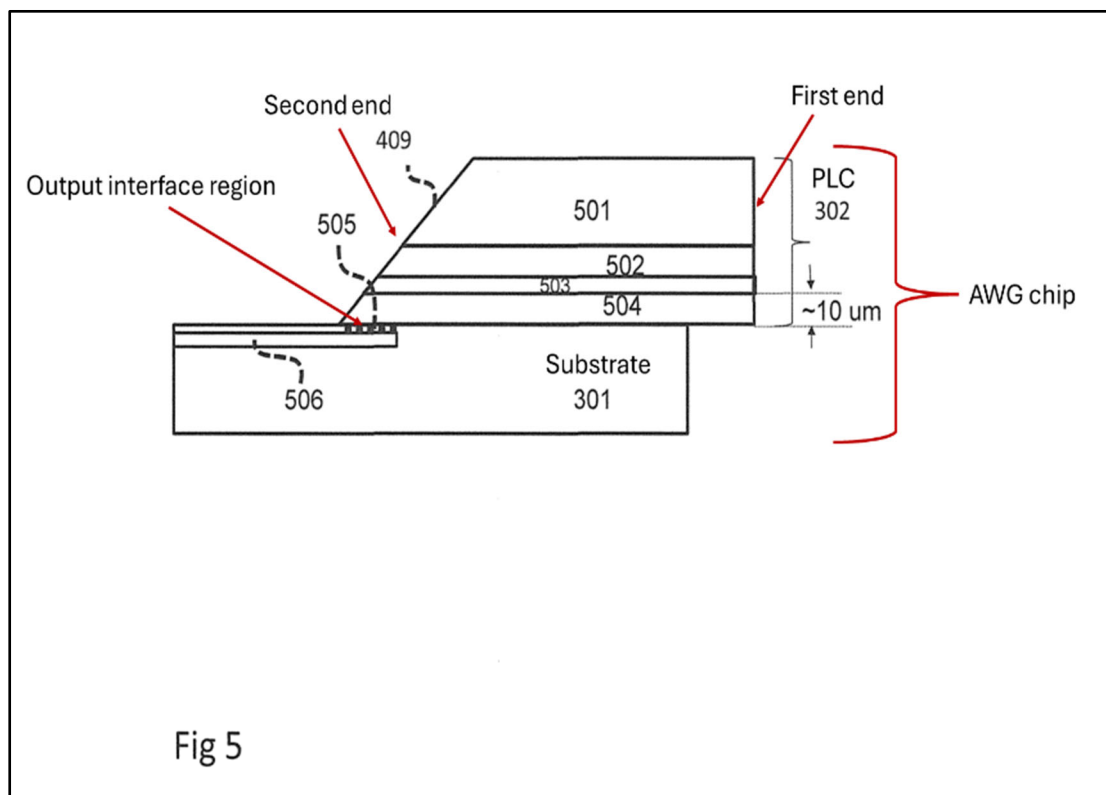
g. Claim term 12[f]

The AWG chip of Bernasconi includes a tapered region disposed at the second end of the AWG chip, as shown in Bernasconi's Figure 2(b), below. In view of Soldano, the second end of the AWG chip is configured to receive light via a plurality of output waveguides, as discussed with reference to claim elements 1[d] and 12[e], above. The light received by the second end is reflected towards an output interface region of the AWG chip. Ex. 1007, Fig. 2(b) (showing that light from the AWG is reflected downward by the turning mirror at the second end and into an array of APD through an output interface region of the AWG chip); *see also id.*, pg. 2 col. 1.



Ex. 1007, Fig. 2(b) (annotations added)

Soldano additionally discloses that demultiplexed light from PLC 302 is transmitted via output waveguides 406 to a second end of the AWG chip having a tapered region defined by an angle polish 409. Ex. 1008, Fig. 3, Fig. 4, 8:1-8, 9:15-37. Soldano further teaches that light from output waveguides 406 is reflected downward by angle polish 409 through an output interface region of PLC 302 onto a grating coupler 505, which is a periodic grating etched onto the surface of waveguide 506 provided in substrate 301. *Id.*, Fig. 5, 9:28-37, 9:58-10:9.



Ex. 1008, Fig. 5 (annotations added)

h. Claim term 12[g]

Bernasconi discloses an array of APDs (avalanche photodiodes), which is a type of photodetector, disposed adjacent the output interface region of the AWG chip. Ex. 1007, Fig. 2(b), pg. 2 col. 1; Ex. 1003, ¶170.

Soldano also discloses that, in some embodiments, an array of photodetectors 601 is provided on the silicon photonics chip 301 in lieu of grating coupler 505, and the photodetectors are thus disposed adjacent to the output interface region of the AWG chip. Ex. 1008, Fig. 6, 8:8-20, 10:10-19; Ex. 1003, ¶171.

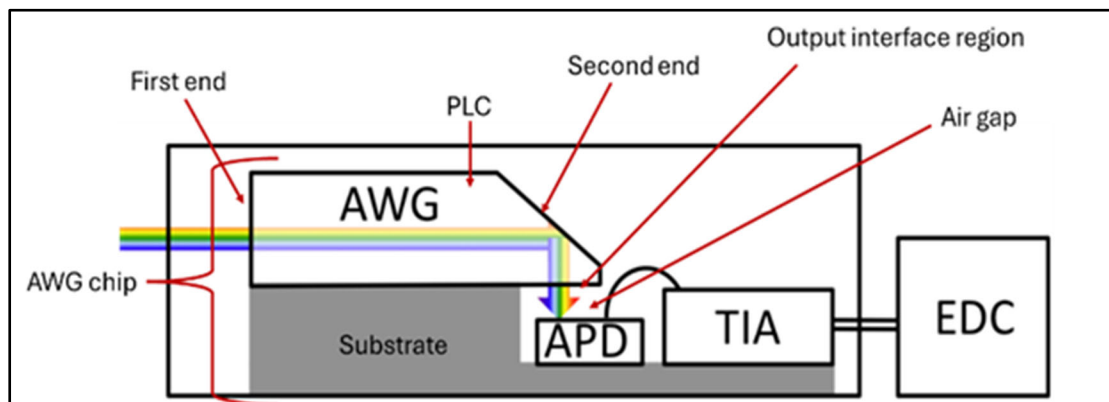
i. Claim term 12[h]

Ho's optical transceiver module 202 includes a multi-channel TOSA 220 within the transceiver housing 210a, 210b. Ex. 1006, ¶[0033]. TOSA 220 includes an array of lasers coupled to an AWG multiplexer 225. *Id.*, ¶[0037]. The array of lasers generates and transmits optical signals at different channel wavelengths. *Id.*, ¶¶[0028], [0029]. Ex. 1010, incorporated by reference in Ho, describes a similar TOSA 220 in more detail. *Id.*, ¶[0037]. As discussed in Ex. 1010 at ¶¶[0034]-[0035], TOSA 220 includes an array of lasers 226-1 to 226-n coupled to AWG 225, and "[e]ach laser 226-1 may be provided as a laser package including, but not limited to, a laser diode chip mounted on a laser mounting structure. The laser package may also include optical components, such as a lens for optically coupling the laser light into a respective one of the optical fibers, and/or optoelectronic components, such

as a monitor photodiode.” It would have been obvious to a POSITA that the lasers of TOSA 220 in Ho generate and transmit optical signals at different channel wavelengths. Ex. 1006, ¶[0058]; Ex. 1003, ¶172. Indeed, it was common knowledge to those skilled in the art that TOSAs include lasers modulated to transmit optical signals at different channel wavelengths. Ex. 1003, ¶172.

3. Claim 13

Bernasconi discloses that the output interface region of the AWG chip is an exposed region adjacent an air gap, wherein the air gap separates the output interface region and the array of photodetectors (APDs). Ex. 1003, ¶173.



Ex. 1008, Fig. 2(b) (annotations added).

4. Claim 15

Claim 15 is identical to claim 3. As discussed above with regard to claim 3 (Section VII.A.6), Bernasconi discloses the limitations of claim 15. Ex. 1003, ¶174.

5. Claim 16

As discussed above in Section VII.A.7 with regard to claim 4, a POSITA would have understood from Figure 2(b) of Bernasconi that the angled surface at the second end has an interior angle of about 45 degrees relative to the output interface region of the AWG chip to reflect light orthogonally onto the APDs, as shown in Figure 2(b). Ex. 1003, ¶175. Indeed, another prior art reference, Kim (Ex. 1005), explicitly discloses an AWG demultiplexer chip having an inclined end surface of 45 degrees to effectively couple the demultiplexed light reflected by the inclined surface with corresponding photodetectors. Ex. 1005, ¶[0034]. Moreover, a POSITA would have known to design an AWG chip with a tapered surface having an interior angle in the range of about 41-45 degrees, based on Bernasconi and Soldano, and through routine experimentation and design considerations, to optimize the direct coupling of demultiplexed light with respective photodetectors. Ex. 1003, ¶175. For example, based on the teachings of Kim, designing Bernasconi's AWG chip to have a tapered surface with an angle of about 41-45 degrees would have been obvious to a POSITA. Ex. 1003, ¶175; *see* Section VII.A.7, above.

VIII. Mandatory Notices

A. Real Parties-in-Interest

The real parties-in-interest for this Petition are Accelight Technologies, Inc. and Accelight Technologies (Wuhan) Inc.

B. Related Matters

To Petitioner's knowledge, the '116 patent is involved in the following:

Name	Number	Court	Filed
<i>Applied Optoelectronics, Inc. v. Accelight Technologies, Inc.</i>	4:24-cv-09041	N.D. Cal.	Dec. 13, 2024
<i>Applied Optoelectronics, Inc. v. Cambridge Industries USA, Inc.,</i>	5:24-cv-01010	N.D. Cal.	Feb. 20, 2024

C. Lead and Back-Up Counsel

Lead Counsel	Back-Up Counsel
<p>Arpita Bhattacharyya (Reg. No. 63,681) Bhattacharyya-ptab@perkinscoie.com PERKINS COIE LLP 3150 Porter Drive Palo Alto, CA 94304 Tel: 650.838.4300 Fax: 650.838.4350</p>	<p>Robert F. McCauley (<i>pro hac vice</i> to be filed) rmccauley@perkinscoie.com PERKINS COIE LLP 3150 Porter Drive Palo Alto, CA 94304 Tel: 650.838.4300 Fax: 650.838.4350</p> <p>Aaron E. Schindler (Reg. No. 79,026) aschindler@perkinscoie.com PERKINS COIE LLP 33 East Main Street, Suite 201 Madison, WI 53703 Tel: 608.663.7460 Fax: 608.663.7499</p>

D. Service Information

Please address correspondence to counsel at the email addresses above. Petitioner consents to service by e-mail.

IX. STANDING

The '116 patent is eligible for IPR and Petitioner is not barred or estopped from requesting IPR challenging the patent claims on the grounds identified herein.

X. CONCLUSION

For the foregoing reasons, Petitioner submits that the challenged claims of the '116 patent should be cancelled.

Dated: September 26, 2025

Respectfully submitted,

/Arpita Bhattacharyya/

Arpita Bhattacharyya, Reg. No. 63,681
Counsel for Petitioner

CERTIFICATION UNDER 37 C.F.R. § 42.24(d)

Pursuant to 37 C.F.R. § 42.24(a)(1)(i), the undersigned hereby certifies that the foregoing **Petition for *Inter Partes* Review** contains 13,945 words, excluding the parts of this Petition that are exempted under 37 C.F.R. § 42.24(a), as measured by the word-processing system used to prepare this paper.

/Arpita Bhattacharyya/

Arpita Bhattacharyya, Reg. No. 63,681
Counsel for Petitioner

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. §§ 42.6(e) and 42.105(a), the undersigned certifies that on September 26, 2025, a copy of the foregoing Petition for *Inter Partes* Review, the associated power of attorney, and Exhibits 1001-1011 were served by FedEx Priority Overnight on the correspondence address of record indicated in the Patent Office's website for U.S. Patent No. 10,042,116:

APPLIED OPTOELECTRONICS, INC.
13115 Jess Pirtle Blvd.
Sugar Land, TX 77478

Courtesy copies were provided to Patent Owner's litigation counsel via email at the following addresses:

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Date: September 26, 2025

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