

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

ACCELIGHT TECHNOLOGIES, INC.,

Petitioner,

v.

APPLIED OPTOELECTRONICS, INC.,

Patent Owner.

Case IPR2025-01566

Patent No. 10,042,116

**PATENT OWNER RESPONSE TO PETITION FOR *INTER PARTES*
REVIEW OF U.S. PATENT 10,042,116**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND	5
A.	'116 Patent.....	5
B.	Relevant File History.....	8
C.	Alleged Prior Art References.....	9
1.	Lee (Exhibit 1004)	9
2.	Kim (Exhibit 1005)	10
3.	Ho (Exhibit 1006)	10
4.	Bernasconi (Exhibit 1007)	11
5.	Soldano (Exhibit 1008)	12
6.	Yoshikawa (Exhibit 1009)	12
III.	DEFINITION OF A PERSON OF ORDINARY SKILL IN THE ART	13
IV.	CLAIM CONSTRUCTION.....	13
	“Substrate”	13
V.	GROUND 1: ACCELIGHT HAS NOT SHOWN THAT LEE IN VIEW OF KIM RENDERS OBVIOUS CLAIMS 1–4, 10, AND 11.....	19
A.	Lee in View of Kim Does Not Disclose “An arrayed waveguide grating (AWG) chip” as Required by Claim 1 [1pre].....	19
B.	Lee in View of Kim Does Not Disclose “a substrate” as	

	Required by Claim 1, Limitation [1b].....	21
C.	Lee in View of Kim Does Not Disclose “a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths” as Required by Claim 1, Limitation [1c].	23
D.	Lee in View of Kim Does Not Disclose “a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip” as Required by Claim 1, Limitation [1d].	24
E.	Lee in View of Kim Does Not Disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as Required by Claim 1, Limitation [1e].....	26
F.	Claims 2–4, 10, 11.....	29
VI.	GROUND 2: ACCELIGHT HAS NOT SHOWN THAT HO IN VIEW OF LEE AND KIM AND IN FURTHER VIEW OF YOSHIKAWA RENDERS OBVIOUS CLAIM 13.	30
A.	Ho in view of Lee and Kim and in Further View of Yoshikawa Does Not Disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the	

	AWG chip and the array of detector devices” as Required by Claim 13, Limitation [13].....	30
VII.	GROUND 3: ACCELIGHT HAS NOT SHOWN THAT BERNASCONI IN VIEW OF SOLDANO RENDERS OBVIOUS CLAIMS 1–4, 10, AND 11.	31
A.	Bernasconi in View of Soldano Does Not Disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as Required by Claim 1, Limitation [1e].....	31
B.	Claims 2–4, 10, 11.....	33
VIII.	GROUND 4: ACCELIGHT HAS NOT SHOWN THAT HO IN VIEW OF BERNASCONI AND SOLDANO AND IN FURTHER VIEW OF YOSHIKAWA RENDERS OBVIOUS CLAIM 13.....	33
A.	Ho in View of Bernasconi and Soldano in Further View of Yoshikawa Does Not Disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices” as Required by Claim 13, Limitation [13].....	33
IX.	CONCLUSION.....	34

EXHIBITS

Exhibit No.	Description
2010	Declaration of Alan E. Willner, Ph. D.
2011	Excerpts from Deposition Transcript of Dr. Michael Lebby

I. INTRODUCTION

Patent Owner Applied Optoelectronics, Inc. (“AOI”) submits this Patent Owner Response to the petition (“Petition”) of Accelight Technologies, Inc. (“Petitioner” or “Accelight”) for an *inter partes* review (“IPR”) of U.S. Patent No. 10,042,116 (the “’116 patent”, Exhibit 1001) entitled “Techniques for Direct Optical Coupling of Photodetectors to Optical Demultiplexer Outputs and an Optical Transceiver Using the Same.” The Petition challenges the patentability of Claims 1–4, 10–13, 15, and 16 (the “Challenged Claims”).

On March 17, 2026, the Board granted institution of *Inter Partes* Review. The ’116 patent generally relates to an arrayed waveguide grating (AWG) device for use in an optical transceiver that can de-multiplex an optical signal into N number of channel wavelengths. Exhibit 1001, Abstract.

Accelight presents four grounds of invalidity in its Petition. *See* Petition at pp. 4–5.

In Ground 1, Accelight challenges claims 1–4, 10, and 11 (Group 1 challenged claims) as obvious over Lee (U.S. Patent Application Publication No. 2014/0183344, Ex. 1004) in view of Kim (U.S. Patent Application Publication No. 2014/0169389, Ex. 1005).

In Ground 2, Accelight challenges claims 12, 13, 15, and 16 (Group 2 challenged claims) as obvious over Ho (U.S. Patent Application Publication No. 2014/0341578, Ex. 1005) in view of Lee and Kim and further in view of Yoshikawa (U.S. Patent Application Publication No. 2005/0286839, Ex. 1009).

In Ground 3, Accelight challenges claims 1–4, 10, and 11 as obvious over Bernasconi (Ex. 1007) in view of Soldano (U.S. Patent No. 9,768, 901, Ex. 1008).

In Ground 4, Accelight challenges claim 12, 13, 15, and 16 as obvious over Ho in view of Bernasconi and Soldano.

None of the prior art references cited in Grounds 1 or 3, separately or in combination, expressly disclose every feature of independent claim 1 or the challenged claims 2–4, 10, or 11 that depend from claim 1. Specifically, Lee in view of Kim does not disclose at least the following limitations as recited in claims 1–4, 10, and 11:

- [1pre] “An arrayed waveguide grating chip;”
- [1b] “a substrate;”
- [1c] “a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths;”

- [1d] “a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip;” and
- [1e] “ a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.”

See Exhibit 2010 (June 9, 2026 Declaration of Alan Willner) at ¶ 45.

None of the prior art references cited in Ground 2, separately or in combination, expressly disclose every feature of dependent claim 13. Specifically, Ho in view of Lee and Kim and further in view of Yoshikawa does not disclose at least the following limitation as recited in claim 13.

- “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the

output interface region of the AWG chip and the array of detector devices.”

See Exhibit 2010 at ¶ 46.

None of the prior art references cited in Ground 3, separately or in combination, expressly disclose every feature of independent claim 1 or the challenged claims 2–4, 10, or 11 that depend from claim 1. Specifically, Bernasconi in view of Soldano does not disclose at least the following limitation as recited in claims 1–4, 10, and 11.

- [1e] “ a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate”

See Exhibit 2010 at ¶ 47.

None of the prior art references cited in Ground 4, separately or in combination, expressly disclose every feature of dependent claim 13. Specifically, Ho in view of Bernasconi and Soldano and further in view of Yoshikawa does not

disclose at least the following limitation as recited in claim 13.

- [13] “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.”

See Exhibit 2010 at ¶ 48.

While Patent Owner remains silent as to Grounds 2 and 4 for claims 12, 15, and 16, Petitioner still bears the burden of proving unpatentability by a preponderance of the evidence. *See* 35 U.S.C. § 316(e). The Board must find that the Petition as to Grounds 2 and 4 for claims 12, 15, and 16 meets the legal standards for obviousness.

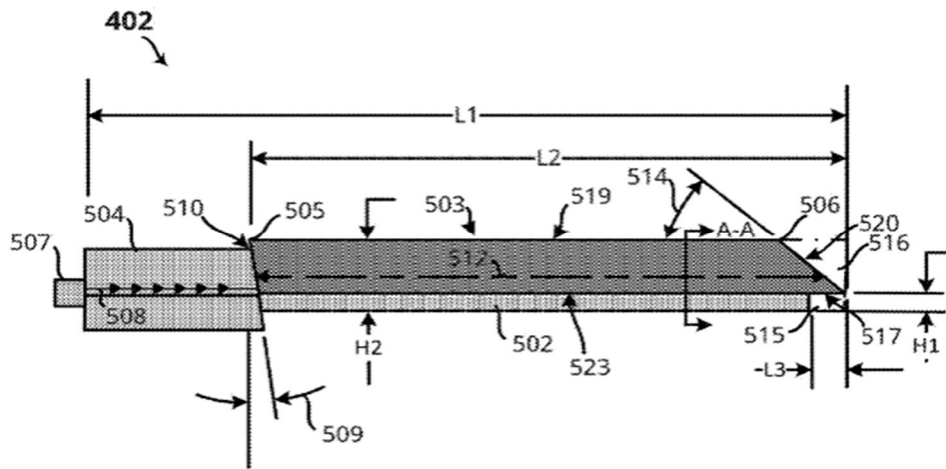
II. BACKGROUND

A. '116 Patent

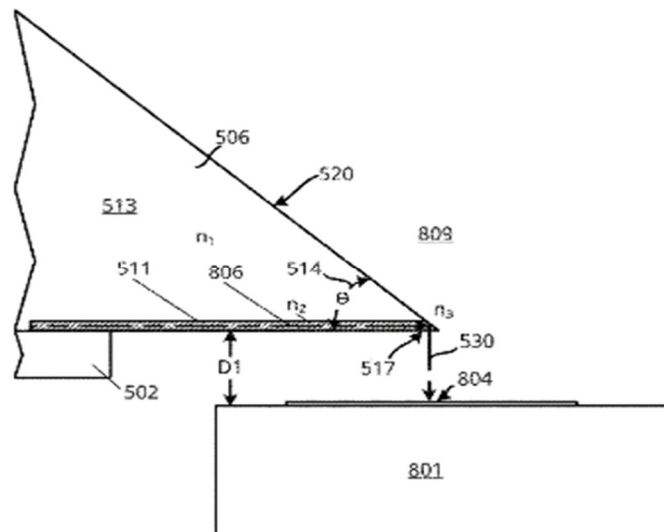
The '116 patent is directed to an arrayed waveguide grating (AWG) device for use in an optical transceiver that can de-multiplex an optical signal into N number of channel wavelengths. The AWG device can include an AWG chip, with the AWG chip providing a planar lightwave (PLC) circuit configured to de-multiplex channel wavelengths and launch the same into output waveguides. A

region of the AWG chip may be tapered such that light traveling via the output waveguides encounters an angled surface of the tapered region and reflects towards an output interface region of the AWG chip. Detector devices may optically couple to the output interface region of the AWG chip directly and can avoid losses introduced by other approaches which couple an output of an AWG to detectors by way of a fiber array or other intermediate device. Exhibit 1001, Abstract; *see also* Exhibit 2010 at ¶ 60.

Figure 5A (reproduced below) shows one example of the direct-coupling AWG device 402. As shown, the AWG device 402 includes an AWG chip 503 having a first end 505 coupled to an input coupling region 504 and having a second end 506, with the second end 506 being proximal to a direct coupling interface 517. The input coupling region 504 can include an optical coupling port 507, with the optical coupling port 507 being configured to receive and optically couple to a fiber of the optical coupling receptacle 215. *Id.* at Col. 7:60–65; *see also* Exhibit 2010 at ¶ 61.



The AWG device is formed on a substrate such as a silicon wafer or any other suitable substrate and may include depositing sequential layers of cladding and core material thereon. *Id.* at Col. 3:35–38. The '116 Patent explains “formation of the AWG chip 503 can include removing a portion of the substrate generally indicated at 515 to expose the output interface region 517. The exposed output interface region 517 may be polished to ensure a suitable optical coupling.” *Id.* at Col. 9:46–49; *see also* Exhibit 2010 at ¶ 62. Figure 8 shows this direct coupling end of the AWG device:



B. Relevant File History

Application no. 15/137,823 for the '116 Patent was filed on April 25, 2016. See "'116 Patent File History," Exhibit 1002. (See Exhibit 1002 for the full prosecution history.) On January 29, 2018, AOI filed an Information Disclosure Statement that listed U.S. Patent Application Publication No. 2016/0149662 to Soldano, et al., among others. *Id.* The '116 Patent issued on August 7, 2018, with 19 claims, including two independent claims.

During prosecution, on January 29, 2018, AOI filed an Information Disclosure Statement that listed U.S. Patent Application Publication No. 2016/0149662 to Soldano, et al., among others. *Id.* at p. 197.

In the Notice of Allowance, the Examiner said Claims 1–11 are allowable because the prior art of record at least “fails to teach a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.” *Id.* at p. 187. The examiner also said Claims 12–19 are allowable because the prior art of record at least “fails to teach a first end for coupling to an optical coupling receptacle to receive an optical signal comprising a plurality of channel wavelengths, wherein the first end for coupling to the optical coupling receptacle includes an angled surface to reduce back reflections of an optical signal launched into the AWG chip.” *Id.* at pp. 187–88; *see also* Exhibit 2010 at ¶¶ 63-65.

C. Alleged Prior Art References

1. Lee (Exhibit 1004)

Lee discloses a hybrid optical coupling module and a manufacturing method thereof. The hybrid optical coupling module includes an optical unit configured to include an optical transmission means that transmits an optical signal, and an array

lens that is bonded at a point where the optical signal of the optical transmission means is output and focuses the output optical signal, and an electrical unit configured to receive the optical signal focused through the array lens and convert the received optical signal into an electrical signal. *See* Exhibit 1004, Abstract; *see also* Exhibit 2010 at ¶ 68.

2. Kim (Exhibit 1005)

Kim discloses an optical receiver module that includes a demultiplexer, an optical device including a right-angled mirror reflecting individual optical signals transmitted from the demultiplexer and a plurality of lenses receiving the reflected optical signals, and a plurality of photodetectors spaced apart from the plurality of lenses by a predetermined distance. The plurality of photodetectors converts the individual optical signals into electrical signals. The optical device and the demultiplexer are formed into a united structure. A distance between the lenses is equal to a distance between the photodetectors. *See* Exhibit 1005, Abstract; *see also* Exhibit 2010 at ¶ 69.

3. Ho (Exhibit 1006)

Ho discloses a multi-channel receiver optical subassembly (ROSA) such as an arrayed waveguide grating (AWG), with outputs directly optically coupled to

respective photodetectors such as photodiodes. In one embodiment, an AWG may be configured such that optical components of the AWG do not interfere with direct optical coupling, and the wire bonding points on the photodiodes may also be configured such that wire bonding does not interfere with direct optical coupling. The photodetectors may also be mounted on a photodetector mounting bar with a pitch sufficiently spaced to allow connection to floating grounds. A passive alignment technique may be used to determine the mounting locations on the photodetector mounting bar such that the photodetectors are aligned with the optical outputs; *see also* Exhibit 2010 at ¶ 70.

4. Bernasconi (Exhibit 1007)

Bernasconi discloses a 100 Gb/s hybrid-integrated photonic circuit. In Bernasconi, “[h]ybrid-integrated, 10×10.7-Gbps WDM transmitters and receivers are built upon DML arrays and APD arrays combined with electronic dispersion compensation.” Exhibit 1007, Abstract. Bernasconi describes its apparatus as follows: “the hybrid-integrated *TOSA comprises* four main parts: *a ceramic board* hosting the laser driver circuitry, a DML bar, *an array waveguide grating (AWG) optical multiplexer*, and a free-space optics assembly for signal spectral filtering and wavelength locking, as in Fig. 1.” Exhibit 1007 at p. 1, col. 1 (emphasis

added). Regarding the ROSA shown in Fig. 2, Bernasconi states that “[t]he APDs, the linear TIAs *and all the passive electronic components are assembled on the base ceramic substrate.*” *Id.* at p.2, col. 1 (emphasis added). Therefore, Bernasconi considers the “ceramic board” or “base ceramic substrate” wholly separate from the AWG chip. *See* Exhibit 2010 at ¶ 71.

5. Soldano (Exhibit 1008)

Soldano is directed to an assembly of waveguide wavelength multiplexers and demultiplexers, together with continuous wave (CW) laser transmitters that interface to grating couplers on a silicon photonics chip, providing CW sources, multiplexed output and optionally multiplexed input, all using a single photonic lightwave circuit (PLC). Exhibit 1008, Abstract; *see also* Exhibit 2010 at ¶ 72.

6. Yoshikawa (Exhibit 1009)

Yoshikawa discloses an optical transceiver that suppresses the EMI radiation through the optical receptacle and the discharge of the static electricity attributed to the optical connector through the optical receptacle. The optical transceiver of the invention includes an optical subassembly comprising a resin made sleeve cover in addition to a metal package and the metal sleeve assembly. Since the resin sleeve cover secures the tip of the sleeve assembly, the EMI discharge and the noise

radiation through this sleeve cover can be suppressed. Moreover, the sleeve cover and the bush both included in the sleeve assembly form a united flange.

Accordingly, the frame and the holder for positioning the optical subassembly are unnecessary to provide a specific structure. Exhibit 1009, Abstract; *see also* Exhibit 2010 at ¶ 73.

III. DEFINITION OF A PERSON OF ORDINARY SKILL IN THE ART

For the purposes of this Patent Owner Response, AOI applies Petitioner's proposed level of skill in the art: A person of ordinary skill in the art ("POSITA") knowledgeable of the technical field of the '116 Patent would have had (1) a bachelor's degree in electrical or electronics engineering or an equivalent degree, and (2) 2–4 years of work experience in optoelectronics, optical networking, optical communications, or a closely related field. *See* Petition at pp. 10–11; *see also* Exhibit 2010 at ¶¶ 40-43.

IV. CLAIM CONSTRUCTION

"Substrate"

Petitioner states that only the term "substrate" should be construed. *See* Petition at pp. 11–12. Petitioner argues that the claim term "substrate" should be construed to mean "a supporting base that is part of the AWG chip and on which

the planar lightwave circuit (PLC) is mounted.” *Id.* Petitioner asserts that its proposed construction is supported by claim 1, which recites that the AWG chip comprises a “substrate,” and that the PLC is “disposed on the substrate.” *Id.* (citing Exhibit 1001 at Col. 12:23–31).

Petitioner’s proposed claim construction attempts to improperly narrow the term “substrate” using additional terms that are inconsistent with and not mentioned in the ’116 Patent. In addition, Petitioner’s proposed construction improperly reads other claim limitations into the term “substrate” in a manner that both impermissibly changes the meaning of the other limitations and effectively renders the other limitations duplicative.

First, Claim 1 recites, “An arrayed waveguide grating (AWG) chip comprising: ... a substrate ...” *See* Exhibit 1001 at Claim 1. The plain and ordinary meaning of this claim language indicates that the AWG chip comprises a substrate. Petitioner’s proposed construction attempts to read and redefine the preamble to be part of the limitation “substrate” in its proposal that substrate should be “a supporting base *that is part of the AWG chip* and on which the planar lightwave circuit (PLC) is mounted.”

The preamble is a separate portion of the claim and the term “comprising” in

the preamble is a standard, well understood term in patent law. *See, e.g.*, Manual of Patent Examining Procedure (“MPEP”) at § 2111.03 (“The transitional term ‘comprising’, which is synonymous with ‘including,’ ‘containing,’ or ‘characterized by,’ is inclusive or open-ended and does not exclude additional, unrecited elements or method steps.”) (*citing e.g.*, *Mars Inc. v. H.J. Heinz Co.*, 377 F.3d 1369, 1376, 71 USPQ2d 1837, 1843 (Fed. Cir. 2004)). “Comprising” requires no construction, yet ATI’s proposal would not only duplicate the preamble as part of the construction of “substrate”, but also improperly redefine “comprising” to mean “is part of.” ATI’s proposed construction is attempting to narrow the meaning of “comprising” and is thus improper under the canons of claim construction.

Second, ATI’s proposed construction attempts to read another claim limitation into the term substrate. Specifically, Claim 1 recites in part:

a substrate;

a planar lightwave circuit (PLC) disposed on the substrate

As shown above, Claim 1 has a limitation requiring “a substrate” and a then subsequent *separate* limitation requiring “a planar lightwave circuit (PLC) *disposed on* the substrate” (“the PLC limitation”). *See* Exhibit 1001 at Claim 1

(emphasis added). Petitioner only proposed construing the term “substrate,” and not the separate limitation for “a planar lightwave circuit (PLC) *disposed on* the substrate.” *See id.* It is improper to attempt to read a construction for the PLC limitation into the construction of “substrate” that would impermissibly render the PLC limitation meaningless. Not only does Petitioner’s proposed construction improperly do just that, but it also attempts to improperly change the meaning of the PLC limitation.

Further, while the PLC limitation should not be read into the construction for “substrate,” the PLC limitation also would not be understood to include Petitioner’s language that the PLC “is mounted” on a substrate. Instead, the claim language requires (and specification discloses) that the PLC “is disposed” on a substrate. *See id.* Petitioner’s expert even notes “Claim 1 explicitly recites that the AWG chip comprises a ‘substrate’ and a PLC is *disposed on* the substrate.” *See* Exhibit 1003 at p. 21 (emphasis added). In fact, there is nothing in Claim 1 or the ’116 Patent specification that requires “the planar lightwave circuit (PLC) *is mounted*” on a substrate. *See MBO Labs., Inc.*, 474 F.3d at 1330–31 (“[W]e cannot endorse a construction analysis that does not identify ‘a textual reference in the actual language of the claim with which to associate a proffered claim

construction.”).

The '116 Patent specification further explains “[i]n an embodiment, the AWG device is formed on a substrate such as a silicon wafer or any other suitable substrate...” *See* Exhibit 1001 at Col. 3:35–38; *see also id.* at Col. 2:30–34 (“The AWG device 100...can include depositing doped and un-doped layers of silica on a substrate, such as silicon.”); *id.* at Col. 8, lines 35–38 (“Processes for AWG chips can include, for example, forming a circuit pattern using photolithography, etching and deposition and/or epitaxial growth on a substrate, e.g., a silicon or silicon-based substrate.”)

In other words, while the claims require a “substrate,” they do not require that the PLC is “mounted on” a substrate. Moreover, Dr. Lebby also could not explain: (1) what “mounted” means in the context of the term at-issue, (2) why he believes the construction of “substrate” should include the added phrase when the claim includes the separate PLC limitation, or (3) why the proposed construction uses words that were not even in the patent. Exhibit 2002 (Lebby Depo.) at 70:18–87:2. Finally, Dr. Lebby admits that if the term “substrate” is replaced with ATI’s proposed construction, Claim 1 would read as follows:

....

a supporting base that is part of the AWG chip and on which the planar lightwave circuit (PLC) is mounted;

a planar lightwave circuit (PLC) disposed on the supporting base that is part of the AWG chip and on which the planar lightwave circuit (PLC) is mounted

See, e.g., id. at 74:5–75:22.

Such a reading is non-sensical on its face. In fact, the only portion of Petitioner’s proposed construction that actually attempts to construe the term “substrate” are the words “a supporting base.” Petitioner’s attempt to add rewritten versions of the preamble and the separate PLC limitation into its proposed construction for the term “substrate” goes against the canons of claim construction. Such a construction would essentially read out the PLC limitation and improperly replace it with a limitation using the word *mounted* instead of the plain language (“disposed”) of the claim. Petitioner’s construction would also attempt to change the plain meaning of standard claim term “comprising” in the preamble. Petitioner’s proposed construction should be rejected. *Diamond Coating*, 2014 WL 5698445, at *11 (rejecting “[u]nnecessary language” that “may inject ambiguity in the [c]ourt’s construction or invite the trier of fact to interpret the court’s construction, thus defeating the purpose of claim construction.”); *see also Tessenderlo Kerley, Inc. v. Or-Cal, Inc.*, 2012 WL 3276981, at *3 (N.D. Cal. Aug.

9, 2012) (rejecting defendants’ construction because “[a] purpose of claim construction is to remove ambiguity. Here, construing the term [as proposed by defendants] would add ambiguity”); *j2 Glob. Commc ’ns, Inc. v. Vitelity Commc ’ns, LLC*, 2013 WL 5220173, at *18 (C.D. Cal. Sept. 13, 2013) (rejecting improper attempts to add “unnecessary verbiage” that is “likely to confuse the jury, and, thus, frustrate one of claim construction’s chief purposes.”)

Petitioner’s proposal should be rejected and the term should be given its plain and ordinary meaning. *See* Exhibit 2010 at ¶¶ 66-67.

V. GROUND 1: ACCELIGHT HAS NOT SHOWN THAT LEE IN VIEW OF KIM RENDERS OBVIOUS CLAIMS 1–4, 10, AND 11.

A. Lee in View of Kim Does Not Disclose “An arrayed waveguide grating (AWG) chip” as Required by Claim 1 [1pre].

Claim 1 [1pre] recites “[a]n arrayed waveguide grating (AWG) chip.” Lee does not disclose this limitation, and Petitioner fails to cure this deficiency with Kim. *See* Exhibit 2010 at ¶ 74.

Petitioner fails to show where Lee discloses an AWG. Petitioner argues that Lee discloses an optical unit that includes an optical transmission means in the form of a planar lightwave circuit (PLC) 110. Petitioner argues that the PLC further includes a demultiplexer structure comprising an arrayed waveguide grating

(AWG). For support, Petitioner only refers to their illusory proposed structure as the “300 AWG chip.” *See* Petition at p. 17–18; *see also* Exhibit 2010 at ¶ 75.

However, Petitioner fails to show where PLC 110 of Lee is directed to an AWG chip. First, an AWG is mentioned only in the Background of Lee, whereas PLC 110 is described as a generic planar lightwave circuit. A POSITA understands that a planar lightwave circuit can take many different forms and none of the embodiments describe an AWG. *See* Exhibit 2010 at ¶ 76. Moreover, Lee discloses PLC 110 as shown in FIGS. 8–10 is a *fiber array*. *See* Exhibit 1004 at ¶ 34 (stating: “As a parallel transmission method is increasingly used along with an increase in the speed of optical communication, an optical fiber array using a planar lightwave circuit (PLC) in which an optical output is established in the form of multi-core process or a V-groove of a silicon optical bench (SiOB) is widely used in the ROSA module.”) (emphasis added). Therefore, Lee describes a fiber array in the presented embodiments, not an AWG. Consequently, Petitioner fails to demonstrate that Lee discloses an AWG chip *at all*. *See* Exhibit 2010 at ¶ 76.

Petitioner acknowledges that Lee does not provide “additional details” of the AWG structure or the demultiplexer functionality. *See* Petition at p. 19. Hence, Petitioner looks to Kim which discloses an optical receiver module 100 [which]

includes an optical connector 110, a demultiplexer 120, an optical device 130, a photodetector 140, a pre-amplifier 150, a printed circuit board 160, a first supporting part 170, and a second supporting part 180. *See* Exhibit 1005 at ¶ [0022]. Petitioner argues that a POSITA would know to combine the structures in Lee and Kim. *Id.*; *see also* Exhibit 2010 at ¶ 77.

But a POSITA would not be motivated to combine the disclosures of Lee and Kim in the way Petitioner alleges. Lee is directed towards a coupling scheme between a PLC optical waveguide (or waveguides) and converting an optical signal (or signals) into an electrical signal (or signals). *See, e.g.*, Exhibit 1004, Abstract. If Lee and Kim are combined, the AWG of Kim would be located upstream from Lee's optical waveguide(s) and would not change any of the claimed elements of Lee. Therefore, Petitioner has not shown a POSITA would be motivated to combine the disclosures of Lee and Kim. *See* Exhibit 2010 at ¶ 78.

For at least these reasons the Lee-Kim combination does not disclose “[a]n arrayed waveguide grating (AWG) chip” of Claim 1. Accordingly, Petitioner has not shown that the combination renders obvious Claim 1. *See* Exhibit 2010 at ¶ 79.

B. Lee in View of Kim Does Not Disclose “a substrate” as Required by Claim 1, Limitation [1b].

Limitation [1b] of Claim 1 recites “a substrate.” Petitioner has not shown that either Lee or Kim discloses this limitation. *See* Exhibit 2010 at ¶ 80.

Petitioner argues under its construction for “substrate” that a POSITA reading Lee would understand that the sub-mount 140 onto which the optical unit 300 is mounted provides support and structure to the optical unit and therefore is part of an AWG chip (notwithstanding that Lee does not disclose an AWG chip as discussed above). *See* Petition at p. 23. However, although Lee refers to part 140 as a sub-mount, Lee describes the component parts of the electrical unit 400 as including a sub-mount 410 wherein a **substrate 420** is mounted on the sub-mount 410. *Id.* at ¶ 39 (emphasis added). Consequently, Lee’s own language does not consider the sub-mount a “substrate.” Petitioner may use “sub-mount” and “substrate” interchangeably, but Lee does not. Consequently, Lee does not disclose a substrate included with the optical unit as required by the claims. *See* Exhibit 2010 at ¶ 81.

Petitioner does not attempt to correct this deficiency with Kim. Instead, Petitioner argues that support 170 constitutes a substrate for the AWG. *See* Petition at p. 23. However, Kim does not use the word “substrate” for this part, but instead uses the word “substrate” in connection with “lens” “array” and “detector” “array”.

Exhibit 1005 at ¶ 35. Consequently, Kim’s own language does not point a person of ordinary skill to consider the support 170 to necessarily be a “substrate.” Exhibit 1005 at ¶ 31. Consequently, Kim does not clearly disclose a substrate as required by the claims. *See* Exhibit 2010 at ¶ 82.

For at least these reasons, the Lee-Kim combination does not disclose “a substrate” of Claim 1. Accordingly, Petitioner has not shown that the combination renders obvious Claim 1. *See* Exhibit 2010 at ¶ 83.

C. Lee in View of Kim Does Not Disclose “a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths” as Required by Claim 1, Limitation [1c].

Limitation [1c] of Claim 1 recites “a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths.” Petitioner does not identify where Lee discloses this limitation, and Petitioner does not seek support in Kim for this limitation. *See* Exhibit 2010 at ¶ 84.

Petitioner argues that PLC 100 of Lee is disposed on a substrate and that it would be obvious to have been coupled to the first end to receive an input optical signal provided via an optical coupling receptacle, as taught by Kim. *See* Petition

at p. 23. *See* Exhibit 2010 at ¶ 85.

For the reasons set out above, Petitioner does not identify where Lee discloses a planar lightwave circuit disposed on a substrate. This deficiency of Lee is not made up by Kim which also does not disclose a planar lightwave circuit disposed on a substrate. *See* Exhibit 2010 at ¶ 86.

For at least this reason the Lee-Kim combination does not disclose “a planar lightwave circuit (PLC) disposed on the substrate, the PLC coupled to the first end and configured to de-multiplex each channel wavelength of the plurality of channel wavelengths” of Claim 1. Accordingly, Petitioner has not shown that the Lee-Kim combination renders obvious Claim 1. *See* Exhibit 2010 at ¶ 87.

D. Lee in View of Kim Does Not Disclose “a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip” as Required by Claim 1, Limitation [1d].

Limitation [1d] of Claim 1 recites “a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from

the PLC and provide the light along a first light path that extends towards a second end of the AWG chip.” Lee does not disclose this limitation, and Petitioner does not seek support in Kim to remedy this deficiency. *See* Exhibit 2010 at ¶ 88.

Petitioner argues that Lee discloses that an optical signal is provided to a second end of the chip which receives light via cores 113. Petition at pp. 27–28. Petitioner argues that it would be obvious to a POSITA that in Lee in view of Kim, the demultiplexed light from PLC 110 would have been passed along separate optical waveguides paths (i.e., cores 113) corresponding to each channel wavelength, because that is how AWG based demultiplexing is commonly implemented to avoid cross-talk between the channels. *Id.*; *see also* Exhibit 2010 at ¶ 89.

As discussed above, a POSITA would not be motivated to combine the disclosures of Lee and Kim. Lee is directed towards a coupling scheme between a PLC optical waveguide (or waveguides) and converting an optical signal (or signals) into an electrical signal (or signals). *See, e.g.*, Exhibit 1004, Abstract. If Lee and Kim are combined, the AWG of Kim would be located upstream from Lee’s optical waveguide(s) and would not change any of the claimed elements of Lee. Therefore, Petitioner has not shown a POSITA would be motivated to

combine the disclosures of Lee and Kim. *See* Exhibit 2010 at ¶ 90.

For at least these reasons the Lee-Kim combination does not disclose “a plurality of output waveguides coupled to the PLC, each of the output waveguides configured to receive light corresponding to an associated de-multiplexed channel wavelength launched from the PLC and provide the light along a first light path that extends towards a second end of the AWG chip” of Claim 1. Accordingly, Petitioner has not shown that the combination renders obvious Claim 1. *See* Exhibit 2010 at ¶ 91.

- E. Lee in View of Kim Does Not Disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as Required by Claim 1, Limitation [1e].**

Limitation [1e] of Claim 1 recites “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received

light through the substrate.” The Lee-Kim combination fails to disclose this limitation. Specifically, it at least fails to disclose the AWG chip’s features of (a) an exposed output interface region and (b) emitting light towards the same side as the substrate without passing through the substrate. *See* Exhibit 2010 at ¶ 92.

The plain and ordinary meaning of “exposed output interface region” to a POSITA is a region that has been uncovered. The examples given in the ‘116 patent specification are supportive of this plain and ordinary meaning. For example, the ‘116 Patent describes that the AWG is formed on a substrate. Exhibit 1001 at Col. 3:35–40. The ‘116 Patent then describes that formation of the AWG chip 503 can include removing a portion of the substrate generally indicated at exposed area 515 to expose the output interface region 517. *Id.*; *see also* Exhibit 2010 at ¶ 93.

Fig. 5A of the ‘116 Patent shows as follows with exposed area 515 identified to expose the output interface region 517:

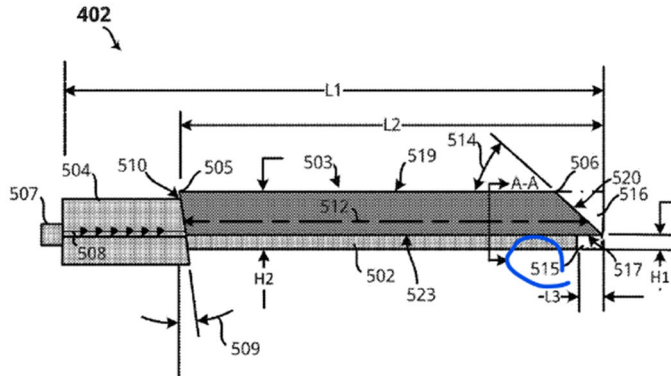


FIG. 5A

See Exhibit 2010 at ¶ 94.

Petitioner argues that Lee discloses an optical chip that has a tapered region that emits light on the same side as the sub-mount 140 without passing the light through the sub-mount. *See* Petition at p. 27. In similar fashion, Petitioner argues that Kim discloses that demultiplexed light which emits the received light on the same side as the sub-mount 170 without passing the received light through support 170. *Id.* at p. 28; *See* Exhibit 2010 at ¶ 95.

First, as already discussed above, Petitioner fails to show that Lee and Kim disclose the claimed substrate at all. Therefore, neither Kim nor Lee discloses an AWG emitting received light on the same side as a substrate without passing the received light through the substrate because Petitioner fails to identify where the references disclose the claimed substrate. *See* Exhibit 2010 at ¶ 96.

Furthermore, Petitioner fails to show that either Lee or Kim discloses an “exposed output interface region” as required by Claim 1. Assuming *argumendo* that either reference discloses a “substrate,” which they do not, neither reference discloses removing a portion of the alleged substrate in order to form an output interface region. Further, Petitioner does not argue that either reference discloses such a feature. *See* Exhibit 2010 at ¶ 97.

For at least these reasons, the Lee-Kim combination does not disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” of Claim 1. Accordingly, Petitioner has not shown that the combination renders obvious Claim 1. *See* Exhibit 2010 at ¶ 98.

F. Claims 2–4, 10, 11.

Each of Claims 2–4, 10, and 11 depend from Claim 1. For each of the reasons discussed above, the Petitioner fails to identify where the Lee-Kim combination discloses all of the limitations of Claim 1. Therefore, for each of these

reasons, the Lee-Kim combination also does not disclose all of the limitations of Claims 2–4, 10, and 11, which depend from Claim 1. Accordingly, Petitioner has not shown the combination renders obvious Claims 2–4, 10, or 11. *See* Exhibit 2010 at ¶ 99.

VI. GROUND 2: ACCELIGHT HAS NOT SHOWN THAT HO IN VIEW OF LEE AND KIM AND IN FURTHER VIEW OF YOSHIKAWA RENDERS OBVIOUS CLAIM 13.

A. Ho in view of Lee and Kim and in Further View of Yoshikawa Does Not Disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices” as Required by Claim 13, Limitation [13].

Limitation [13] of Claim 13 recites “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.” The cited references do not disclose an “output interface region” that is an “exposed region” of the AWG chip as required by Claim 13. *See* Exhibit 2010 at ¶ 100.

Neither Lee nor Kim discloses an “exposed output interface region” or an “output interface region” that is an “exposed region” as required by the Claim.

Yoshikawa does not make up for this deficiency, nor does Petitioner cite to Yoshikawa for that purpose. *See, e.g.*, Petition at p. 49; *see also* Exhibit 2010 at ¶ 101.

For at least this reason, the combination of Ho-Lee-Kim-Yoshikawa does not disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices” as required by Claim 13. Accordingly, Petitioner has not shown that the combination renders obvious Claim 13. *See* Exhibit 2010 at ¶ 102.

VII. GROUND 3: ACCELIGHT HAS NOT SHOWN THAT BERNASCONI IN VIEW OF SOLDANO RENDERS OBVIOUS CLAIMS 1–4, 10, AND 11.

- A. Bernasconi in View of Soldano Does Not Disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” as Required by Claim 1, Limitation [1e].**

Limitation [1e] of Claim 1 recites “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output

waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate.” Neither Bernasconi nor Soldano disclose this limitation. *See* Exhibit 2010 at ¶ 103.

Neither Bernasconi nor Soldano disclose an “exposed output interface region” as required by Claim 1. Neither reference disclose removing a portion of the alleged substrate in order to form an output interface region. *See* Exhibit 2010 at ¶ 103. Moreover, Petitioner does not argue that either reference discloses this limitation requiring an “exposed output interface region.” *See, e.g.,* Petition at pp. 63-65; *see also* Exhibit 2010 at ¶ 104.

For at least this reason, neither Bernasconi nor Soldano, separately or together, disclose “a tapered region disposed at the second end of the AWG chip configured to receive light via the plurality of output waveguides and reflect the same towards an exposed output interface region of the AWG chip, wherein the exposed output interface region emits the received light from the AWG chip on the same side as the substrate without passing the received light through the substrate” of Claim 1. Accordingly, Petitioner has not shown that Bernasconi in view of

Soldano renders obvious Claim 1. *See* Exhibit 2010 at ¶ 105.

B. Claims 2–4, 10, 11.

Each of Claims 2–4, 10, and 11 depend from Claim 1. For each of the reasons discussed above, the Bernasconi-Soldano combination does not disclose all of the limitations of Claim 1. Therefore, for each of these reasons, the Bernasconi-Soldano combination also does not disclose all of the limitations of Claims 2–4, 10, and 11. Accordingly, for each of these reasons, Petitioner also has not shown the combination renders obvious Claims 2–4, 10, or 11. *See* Exhibit 2010 at ¶ 106.

VIII. GROUND 4: ACCELIGHT HAS NOT SHOWN THAT HO IN VIEW OF BERNASCONI AND SOLDANO AND IN FURTHER VIEW OF YOSHIKAWA RENDERS OBVIOUS CLAIM 13.

A. Ho in View of Bernasconi and Soldano in Further View of Yoshikawa Does Not Disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices” as Required by Claim 13, Limitation [13].

Limitation [13] of Claim 13 recites “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices.” None of the cited references disclose an “output interface region” that is

an “exposed region as required by Claim 13. *See* Exhibit 2010 at ¶ 107.

The deficiencies of the Bernasconi-Soldano combination are discussed above, including that neither reference discloses an “output interface region” that is an “exposed region” as required by claim 13. Yoshikawa does not make up for this deficiency, nor does Petitioner cite Yoshikawa for that purpose. *See, e.g.*, Petition at p. 81; *see also* Exhibit 2010 at ¶ 108.

For at least this reason, the combination of Ho-Bernasconi-Soldano-Yoshikawa does not disclose “wherein the output interface region of the AWG chip is an exposed region adjacent an air gap, and wherein the air gap separates the output interface region of the AWG chip and the array of detector devices” of Claim 13. Accordingly, Petitioner has not shown that the combination renders obvious Claim 13. *See* Exhibit 2010 at ¶ 109.

IX. CONCLUSION

For the reasons set forth above, Petitioner has failed to prove by a preponderance of the evidence that the challenged claims of the ’116 Patent are unpatentable. Therefore, Patent Owner respectfully requests that the Board deny Petitioner’s request to cancel the challenged claims of the ’116 Patent.

Dated: June 9, 2026

/Jo Dale Carothers/

IPR2025-01566
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CERTIFICATE OF WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(d), the undersigned hereby certifies that the Microsoft Office word count including all footnotes for the foregoing Patent Owner Response, excluding the table of contents, table of authorities, certificate of word count, appendix and certificate of service, totals 6812 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(2).

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CERTIFICATE OF SERVICE

The undersigned hereby certifies service on the Petitioner, pursuant to 37 C.F.R. §42.6(e) and by agreement of counsel, by electronic (e-mail) delivery of a true copy of the foregoing **PATENT OWNER RESPONSE** which was served on June 9, 2026 to the following Counsel for Petitioner via e-mail:

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