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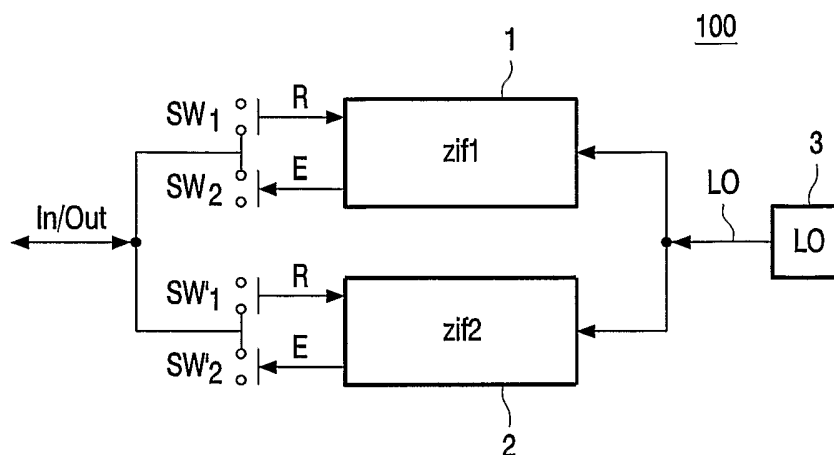
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(54) Title: MULTI-BAND TRANSCEIVER



(57) Abstract: A multi-band transceiver (100) for receiving or transmitting signals situated in substantially different frequency ranges comprising first transceiver (1) coupled to an input/output terminal (In/Out) via a first pair of switches (SW₁, SW₂). The multi-band transceiver further comprises a second transceiver (2) coupled to the input/output terminal (In/Out) via second pair of switches (SW'₁, SW'₂) and only one local oscillating system (3) comprising only one voltage controlled oscillator (VCO).



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Multi-band transceiver

The invention relates to a multi-band transceiver.

Transceivers are very much used nowadays in many applications, which may
5 be wired or wireless. The most known wireless application is mobile telephony and the most
known wired application is computer networking. There are recognized standards for
communications, which allocate frequency ranges or bands where emitted and received
information must be situated as e.g. IEEE 802.11a, b, g.

Besides allocated bands there are in the frequency spectrum not-allocated
10 ranges as e.g. 17 GHz for personal area networks. A vast majority of the transceivers are built
for being used in only one band, the more the bands the more transceivers. Relatively recent,
multi-band transceivers and accordingly multi-band receivers and multi-band transmitters
have been considered. Their main advantage is that they may work with signals situated in
different bands and being adapted to different communication protocols as standard ones as
15 Bluetooth and a not yet standard one as Ultra Wide Band (UWB).

US-A- 2002/0008585 describes a method and an apparatus for synthesizing
dual band high frequency signals for wireless communication. A Phase Locked Loop (PLL)
comprises first and second voltage controlled oscillators (VCOs) each for a respective
frequency band. Use of two VCOs creates some problems as e.g. different control patterns
20 for the VCO, increase in design complexity and increase in price of the transceiver, and
increase in the area.

It is an object of present invention to provide a relatively low cost multi-band
25 transceiver. The invention is defined by the independent claims. The dependent claims define
advantageous embodiments.

This object is achieved in a multi-band transceiver system for receiving or
transmitting signals situated in substantially different frequency bands comprising:

- first transceiver coupled to an input/output terminal via a first pair of switches,

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- second transceiver coupled to the input/output terminal via a second pair of switches, and
- only one local oscillating system comprising only one voltage controlled oscillator, that is coupled to said first and second transceivers.

5 The transceiver according to the invention has only one VCO for at least two frequency bands. The VCO generates a signal having a frequency, the signal being combined with an input signal having a carrier frequency in a mixer. The mixer generates an intermediate frequency (IF) signal, which may have a substantially lower frequency than the frequency of the VCO in so called LOW IF transceiver. Furthermore, in a Zero IF (ZIF) or

10 direct conversion transceiver the frequency of the signal generated by the VCO is substantially equal to the frequency of the carrier of the input signal.

 In an embodiment of the invention the oscillating system is a Phase Locked Loop (PLL). The PLL comprises a divider by 2 coupled to a divider by N for dividing the frequency of the signal generated by the voltage-controlled oscillator. In the multi-band

15 transceiver, at least one of the first and the second zero IF transceiver comprises a divider by 3.

 The PLL is used for generating the signal that is used in mixer. The PLL uses the stability of a quartz crystal and the frequency of the VCO is digitally controlled via a digital frequency divider. For a multi-band transceiver e.g. according to IEEE 802.11a and

20 17 GHz band, or IEEE 802.11a and IEEE 802.11b, it is cheaper to have only one VCO, if this is possible. Choosing a suitable oscillation range for the VCO e.g. 30.9 – 32.1 GHz and 34.2 – 34.6 GHz we may cover two frequency ranges for the input signals. Dividing by 2 the frequency of the oscillator we obtain an oscillation situated in 17 GHz band i.e. 17.1 – 17.3 GHz. Dividing by 6 i.e. first dividing by 2 and then dividing by 3 the frequency

25 of the signal generated by the oscillator i.e. situated in the range 30.9 – 32.1 GHz we obtain a signal situated in IEEE 802.11a band i.e. 5.15 – 5.35 GHz. It may be observed that a divide by two is necessary for signals situated in both input frequency ranges. As a consequence a divide by two circuit may be added either in the PLL or in both transceivers. Preferably, the signals generated by the VCO are quadrature signals i.e. the VCO generates 4 output

30 signals I , $\bar{I}$, Q and $\bar{Q}$, The signals I , Q and $\bar{I}$, $\bar{Q}$ being mutually phase shifted with 90 degrees, respectively. Let us further observe that if the signal situated in IEEE 802.11a band is further divided by 2 we obtain a signal situated in IEEE 802.11b range and therefore a three band receiver is obtained. The divider by N is digitally controllable, a digital controllable word determining VCO's oscillation frequency.

In an embodiment of the invention the divider by 3 comprises a divide by 4 circuit coupled to a decoder system. The divide by 4 circuit is conceived for receiving quadrature signals. The decoder system comprises a first decoder coupled to a second decoder, the first decoder receiving a vector of quadrature signals generated by the divide by 4 circuit, the second decoder receiving a quadrature signal having a frequency, which is substantially triple the frequency of the signal generate by the divider. Use of quadrature signals determines a relative simple structure for the divide by 3 circuit. The outputs of the divide by 4 circuit are decoded in a decoding circuit. The decoding circuit comprises two serially coupled decoders. As the signals that appear in the divide by 3 circuit are described by a system of wave-forms, or as a state table it results that there are possible a plurality of implementations e.g. using logic gates, using multiplexers etc.

The above and other features of the invention will be apparent from the following description of the exemplary embodiments of the invention with reference to the accompanying drawings, in which:

Fig. 1 depicts a block diagram of a multi-band transceiver according to the invention,

Fig. 2 depicts a more detailed block diagram of a Phased Lock Loop included in the multi-band transceiver according to an embodiment of the invention,

Fig. 3 depicts a more detailed block diagram of a transceiver included in the multi-band transceiver according to another embodiment of the invention,

Fig. 4 depicts a block diagram of a divide by 3 circuit according to an embodiment of the invention,

Fig. 5 depicts a more detailed diagram of a divide by 4 circuit, according to another embodiment of the invention,

Fig. 6 depicts a block diagram of a decoder used in divide by 3 circuit, according to an embodiment of the invention,

Fig. 7 depicts wave-forms of quadrature input signals and quadrature output signals of a divide by 3 circuit according to a preferred embodiment of the invention, and

Fig. 8 depicts a more detailed implementation of a decoder circuit for a divide by 3 according to an embodiment of the invention.

Fig. 1 depicts a block diagram of a multi-band transceiver according to the invention. The multi-band transceiver comprises a first transceiver 1 coupled to an input/output terminal In/Out via a first pair of switches SW1, SW2. The switches are all the time in mutual different states i.e. if SW1 is ON then SW2 is OFF and reciprocally. When

5 SW1 is ON the first transceiver receives a signal inputted through the input/output terminal. When SW2 is ON, a signal generated by the first transceiver is transmitted via input/output terminal In/Out. The multi-band transceiver further comprises a second transceiver 2 coupled to the input/output terminal In/Out via second pair of switches SW1', SW2'. The functional features of the switches SW1, SW2 and to the first transceiver apply mutates mutandis to the

10 switches SW1', SW2' and the second transceiver. A local oscillating system 3 comprising only one voltage controlled oscillator (VCO) is used for both first and second transceivers 1, 2. The VCO generates a signal LO having a frequency, the signal LO being combined with an input signal having a carrier frequency in a mixer (not figured). The mixer generates an intermediate frequency (IF) signal, which may have a substantially lower frequency than the

15 frequency of the VCO in so called LOW IF transceiver. Furthermore, in a Zero IF (ZIF) or direct conversion transceiver the frequency of the signal generated by the VCO LO is substantially equal to the frequency of the carrier. The multi-band transceiver 100 as claimed in claim 1, wherein the oscillating system 3 is a Phase Locked Loop (PLL) as shown in Fig. 2. The PLL comprises the VCO coupled to a divide by 2 circuit generating the

20 signal LO, which is represented in this embodiment as a quadrature signal having two components I and Q. The signals I and Q have the same frequency but they are mutually phase-shifted with 90 degrees. The signal LO may also be differential or single-ended i.e. having additional components $\bar{I}$, $\bar{Q}$ which are 180 degrees mutually phase shifted with respect I and Q, respectively or the signal LO may have only one component. The signal LO

25 is inputted to a divider by N Dn. A division factor of the divider by N is digitally controlled by a vector C. The divider by N Dn generates a signal that is inputted into a series connection of a phase-frequency detector PFD coupled to a charge-pump, which is coupled to a low-pass filter. A signal generated by the low-pass filter LPF controls the frequency generated by the VCO. A quartz i.e. very stable oscillator determines a step used for locking the PLL. A signal

30 generated by the quartz f_c is inputted to the phase-frequency detector PFD as reference signal. Let us consider that the input signal in the multi-band transceiver 100 is situated in two bands determined by IEEE 802.11a standard and in 17GHz range. In this case VCO's frequency will be situated between 30.9 - 32.1 GHz and 34.2 - 34.6 GHz for respective two ranges. It results that the divider must divide with factors situated in the range 1710 - 1730 for input

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signals situated in the 17 GHz range and with numbers situated in the range 1545-1605 for input signals situated in the range defined by IEEE 802.11a standard, if the quartz frequency is 10 MHz. In the multi-band transceiver 100 at least one of the first and the second transceiver 1, 2 is coupled to a divider by 3 D3. This means that either first transceiver 1 or second transceiver 2 is coupled to the local oscillator system 3 via the D3 circuit. The divider D3 makes possible for the transceiver to receive signals situated in two separate frequency ranges as it was shown before. It must be observed that the divide by 3 circuit D3 may be further coupled to a divide by 2 circuit and afterwards coupled to first 1 or second 2 transceiver, not shown in Fig. 3. In this situation the transceiver 100 would be able to receive signals situated in 2.5 GHz range according to IEEE 802.11 b, g standard, which make the transceiver capable of receiving signals situated in three frequency ranges corresponding to different standards.

As could be easily observed, a divider by 3 is necessary for obtaining an at least 2 band transceiver. In an embodiment of the invention the divide by 3 looks like the circuit depicted in Fig. 4. The divider by 3 D3 comprises a divide by 4 circuit 41 coupled to a decoder system 42. The decoder system 42 receives an input signal having a frequency designated as Ck and generates a signal having a frequency substantially a third part of Ck. The decoder system 42 transmits a signal having the frequency Ck to the divide by 4 circuit 41 and receives a signal Vout having a frequency substantially a third of Ck. Input signal Vin and the signal generated by the divide by 4 circuit 41 are preferably quadrature signals.

Fig. 5 depicts a more detailed diagram of a divide by 4 circuit, according to another embodiment of the invention. the circuit comprises two D flip-flops driven by a clock signal Ck. At the outputs of the flip-flops, a quadrature signal Vout is obtained. When coupled to the decoder system 42, a frequency of the quadrature signal Vout is substantially a third the frequency of the clock signal Ck. The decoder system 42 comprises, according to Fig. 6, a first decoder DEC1 coupled to a second decoder DEC2, the first decoder DEC1 receiving the vector of quadrature signals generated by the divide by 4 circuit 41. The second decoder DEC2 receives a quadrature signal Vin having a frequency, which is substantially triple, the frequency of the signal generated by the divider. The relationship between the quadrature signal Vin and the quadrature signals obtained at the output of the flip-flops is shown in Fig. 6. It should be mentioned here that an alternative states table might be written using the waveforms shown in Fig. 7. Alternatively, a design process could lead to different implementations using different types of logic circuits as gates, multiplexers, switches, etc.

In an embodiment of the invention, the decoder system 42 was designed starting from the waveforms shown in Fig. 7 and using logic gates, as shown in Fig. 8. It is observed that resulted an implementation using AND gates having only 2 inputs, which is very convenient in practical implementation i.e. uniformity of design. In Fig. 8, first
5 decoder DEC1 and second decoder DEC2 are identified in dotted squares. It should be observed that starting from the waveforms shown in Fig. 7, a transition table could be derived, the transition table being further used in synthesis of the decoders as shown in J.P. Hayes, Introduction to Digital Logic Design, Addison – Wesley, 1993, Ch. 7.

It is remarked that the scope of protection of the invention is not restricted to
10 the embodiments described herein. Neither is the scope of protection of the invention restricted by the reference signs in the claims. The word ‘comprising’ does not exclude other parts than those mentioned in the claims. The word ‘a(n)’ preceding an element does not exclude a plurality of those elements. Means forming part of the invention may both be implemented in the form of dedicated hardware or in the form of a programmed purpose
15 processor. The invention resides in each new feature or combination of features.

CLAIMS:

1. A multi-band transceiver (100) for receiving or transmitting signals situated in substantially different frequency ranges comprising:
 - first transceiver (1) coupled to an input/output terminal (In/Out) via a first pair of switches (SW1, SW2),
 - 5 - second transceiver (2) coupled to the input/output terminal (In/Out) via second pair of switches (SW1', SW2'), and
 - only one local oscillating system (3) comprising only one voltage controlled oscillator (VCO) that is coupled to said first and second transceivers.
- 10 2. A multi-band transceiver (100) as claimed in claim 1, wherein the first transceiver (1) and the second transceiver (2) are low intermediate frequency transceivers.
3. A multi-band transceiver (100) as claimed in claim 1, wherein the first transceiver (1) and the second transceiver (2) are zero intermediate frequency transceivers.
- 15 4. A multi-band transceiver (100) as claimed in claim 1, wherein the oscillating system (3) is a Phase Locked Loop (PLL).
5. A multi-band transceiver (100) as claimed in claim 2, wherein the PLL
- 20 comprises a divider by 2 (D2) coupled to a divider by N (Dn) for dividing the frequency of the signal (LO) generated by the voltage controlled oscillator.
6. A multi-band transceiver (100) as claimed in claims 1 to 3, wherein at least one of the first and the second transceiver (1, 2) is coupled to a divider by 3 (D3).
- 25 7. A multi-band transceiver (100) as claimed in claim 6, wherein the divider by 3 (D3) comprises a divide by 4 circuit (41) coupled to a decoder system (42).

8. A multi-band transceiver (100) as claimed in claim 7, wherein the divide by 4 circuit (41) is conceived for receiving quadrature signals.

9. A multi-band transceiver (100) as claimed in claim 7, wherein the decoder
5 system (42) comprises a first decoder (DEC1) coupled to a second decoder (DEC2), the first decoder receiving a vector of quadrature signals generated by the divide-by-4 circuit (41), the second decoder (DEC2) receiving a quadrature signal (Vin) having a frequency, which is substantially triple the frequency of the signal generated by the divide-by-4 circuit (41).

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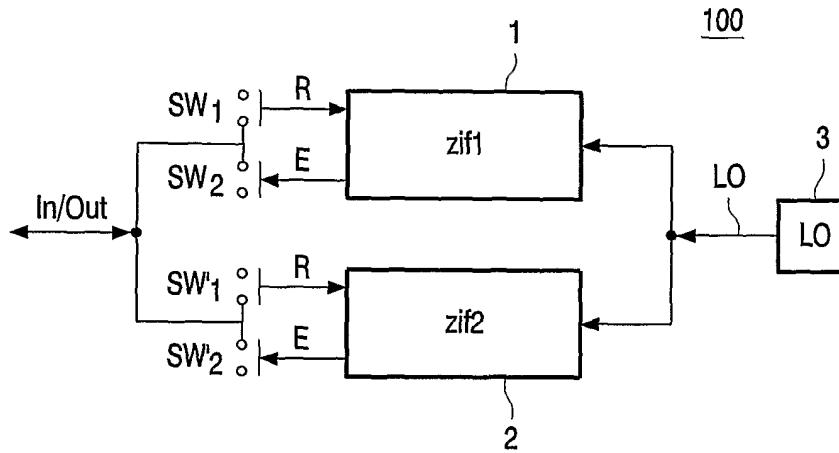


FIG. 1

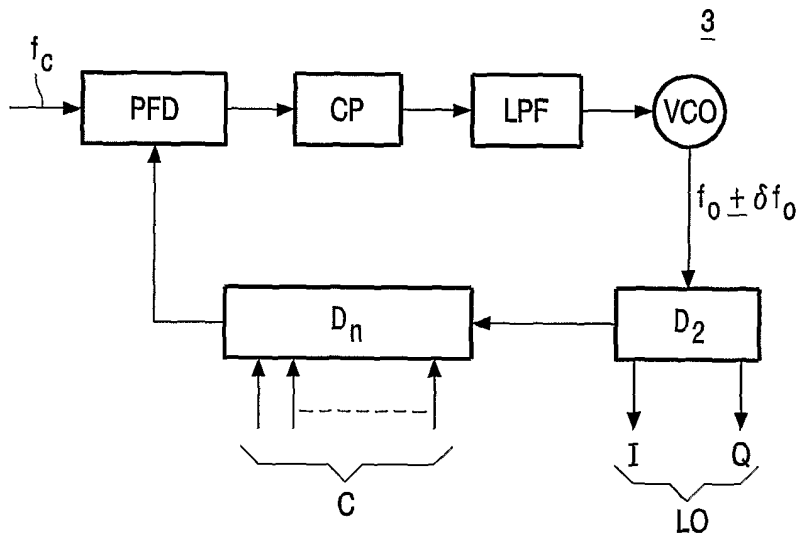


FIG. 2

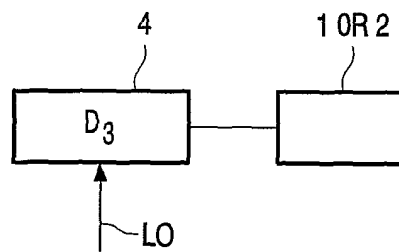


FIG. 3

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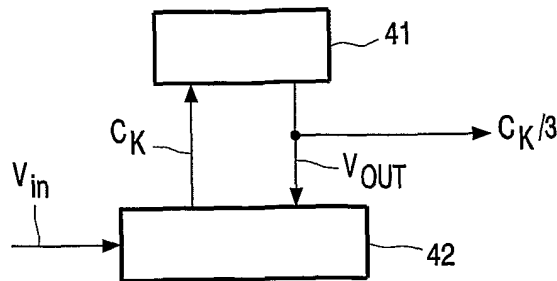


FIG. 4

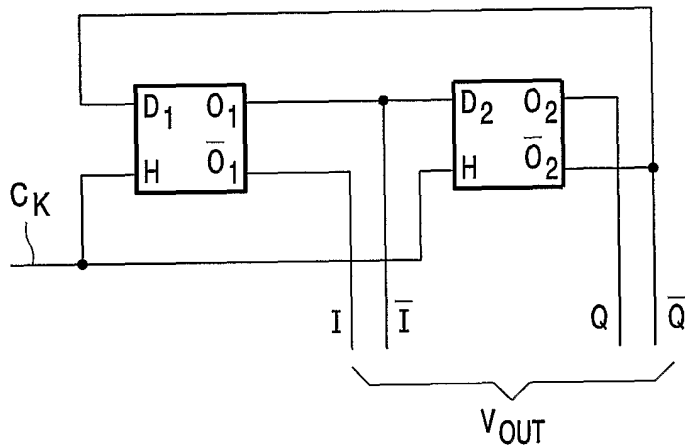


FIG. 5

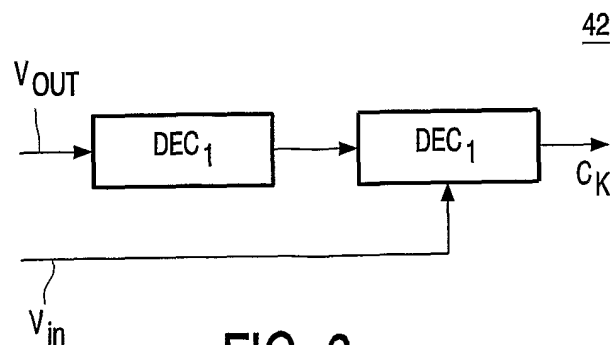


FIG. 6

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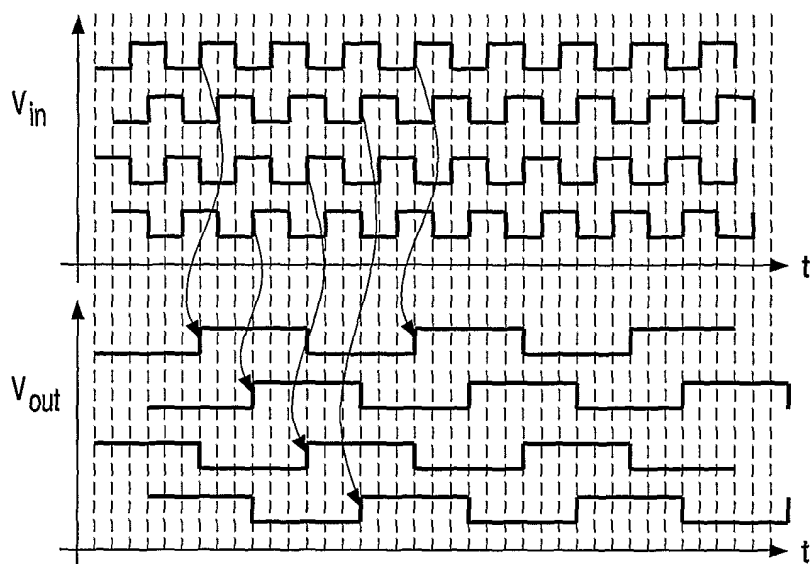


FIG. 7

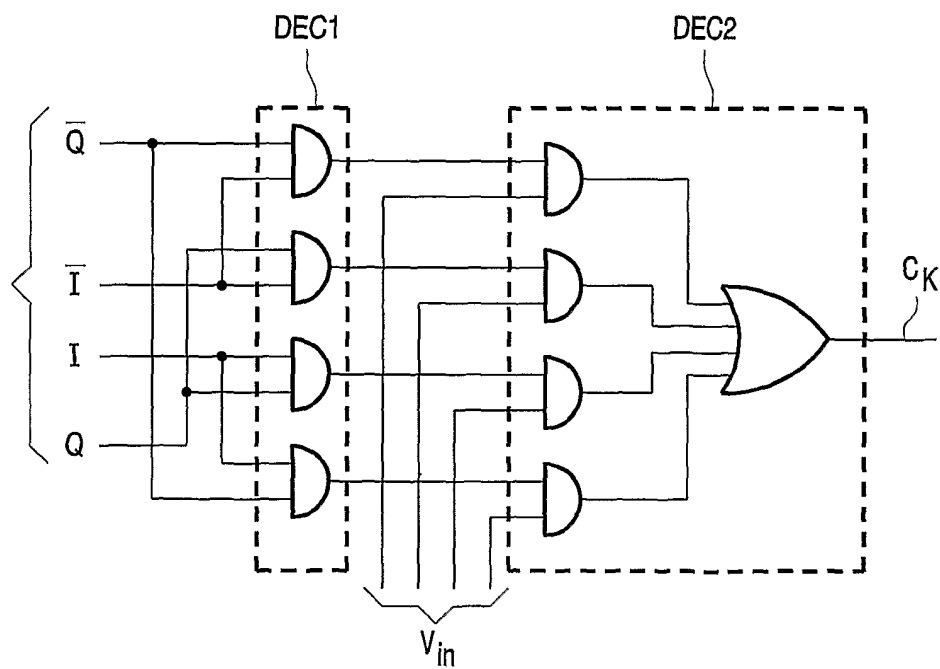


FIG. 8

INTERNATIONAL SEARCH REPORT

International Application No
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A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H04B1/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	EP 0 800 283 A (NOKIA MOBILE PHONES LTD) 8 October 1997 (1997-10-08) abstract column 6, line 7 - column 10, line 50 figure 3	1-9
X	EP 0 798 880 A (NOKIA MOBILE PHONES LTD) 1 October 1997 (1997-10-01) abstract page 5, line 34 - page 9, line 34	1-9
A	EP 1 020 994 A (SANYO ELECTRIC CO ; TOKYO SANYO ELECTRIC CO (JP)) 19 July 2000 (2000-07-19) abstract figures 7,8	1-9

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/IB2004/051691

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