

Electronic Acknowledgement Receipt

EFS ID:	44844095
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Ryan Scott Davidson/David Edwards
Filer Authorized By:	Ryan Scott Davidson
Attorney Docket Number:	1458-190070
Receipt Date:	26-JAN-2022
Filing Date:	28-JUN-2019
Time Stamp:	17:39:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 260
RAM confirmation Number	E20221PH40083643
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

NVIDIA 1003
(Part 4 of 4)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	1458-190070-IDS.pdf	70586	no	4
			19b50f965ecd315d73fc22066f90974d2057cadd		

Warnings:**Information:**

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2	Non Patent Literature	190141-NFOA.pdf	342819	no	11
			d1e3eb36c87a74c1851ff6f64e7ab33d7078625f		

Warnings:**Information:**

3	Fee Worksheet (SB06)	fee-info.pdf	38198	no	2
			70cf0d48c6dbcebc755540ecf7d85848c162c25		

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Total Files Size (in bytes):

451603

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16456287
	Filing Date		2019-06-28
	First Named Inventor	Skyler J. SALEH	
	Art Unit	2135	
	Examiner Name	Jae Un YU	
	Attorney Docket Number	1458-190070	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS						
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20170365580		2017-12-21	SHIH et al.	
	2	20200294181		2020-09-17	MATAM et al.	
	3	20190051633		2019-02-14	BHAGAVAT et al.	
	4	20170062383		2017-03-02	YEE et al.	
	5	20210020602		2021-01-21	CHEN et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

6	20140001645		2014-01-02	LIN, Jing-Cheng and Chen-Hua Yu	
7	20200176384		2020-06-04	WU et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ^{2j}	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Non-Final Office Action issued August 17, 2021 in Application No. 16/585,480 (Attorney Docket No. 1458-190142), 20 pages.	☐
	2	Final Office Action issued July 30, 2021 in Application No. 16/585,452 (Atty. Docket No. 1458-190141), 12 pages.	☐
	3	Notice of Allowance issued September 15, 2021 in Application No. 16/698,624 (Atty. Docket No. 1458-190143), 18 pages.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

- ☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

- ☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

- ☐ See attached certification statement.
- ☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
- ☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Adam D. Sheehan/	Date (YYYY-MM-DD)	2021-09-30
Name/Print	Adam D. Sheehan	Registration Number	42146

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	16456287			
Filing Date:	28-Jun-2019			
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS			
First Named Inventor/Applicant Name:	Skyler J. SALEH			
Filer:	Adam D. Sheehan/David Edwards			
Attorney Docket Number:	1458-190070			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt

EFS ID:	43913635
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Adam D. Sheehan/David Edwards
Filer Authorized By:	Adam D. Sheehan
Attorney Docket Number:	1458-190070
Receipt Date:	30-SEP-2021
Filing Date:	28-JUN-2019
Time Stamp:	13:46:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$260
RAM confirmation Number	E20219TD46221889
Deposit Account	
Authorized User	

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	190070-US-IDS.pdf	66609	no	5
			5e710c9dabe26306ca5aeffee0b55e8835fc39d6		
Warnings:					
Information:					
This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	190141-Final-Rejection.pdf	301910	no	9
			087d1f83e657e582dffa540ce88b317c233e3589		
Warnings:					
Information:					
3	Non Patent Literature	190142-NFOA.pdf	701437	no	19
			75fdccf0c8f46156082d9900c4445e4aad41516a		
Warnings:					
Information:					
4	Non Patent Literature	190143-NOA.pdf	1088002	no	18
			4c79f39cd414c8b711a4e02ae2411a31b013db4d		
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	38220	no	2
			255a31f403b5954dcff4a090c6c02ca7f0f4e575		
Warnings:					
Information:					
Total Files Size (in bytes):			2196178		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Doc Code: AP.PRE.REQ

PTO/AIA/33 (03-13)

Approved for use through 11/30/2020. OMB 0651-0031

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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) 1458-190070	
I hereby certify that this correspondence is being facsimile transmitted to the USPTO, EFS-Web transmitted to the USPTO, or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on <u>September 15, 2021</u> Signature <u>/Rachelle Chery/</u> Typed or printed name <u>Rachelle CHery</u>		Application Number 16/456,287	
		Filed June 28, 2019	
		First Named Inventor SALEH, Skyler J.	
		Art Unit 2135	
		Examiner YU, Jae Un	
Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a notice of appeal. The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.			
I am the		<u>/Thomas S. Grzesik/</u>	
☐ applicant.		Signature Thomas S. Grzesik	
☒ attorney or agent of record.		Typed or printed name	
Registration number <u>54139</u>		<u>512582-2455</u>	
☐ attorney or agent acting under 37 CFR 1.34.		Telephone number	
Registration number if acting under 37 CFR 1.34 _____		<u>September 15, 2021</u>	
		Date	
NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.			
☒ *Total of <u>1</u> forms are submitted.			

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):	SALEH, Skyler J. et al.		
Title:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		
App. No.:	16/456,287	Filed:	June 28, 2019
Examiner:	YU, Jae Un	Group Art Unit:	2135
Atty. Dkt. No.:	1458-190070	Confirmation No.:	4820

REMARKS IN SUPPORT OF THE PRE-APPEAL REQUEST FOR REVIEW

In response to the Final Office Action mailed May 17, 2021 (hereinafter the “Final Action”) and pursuant to the Notice of Appeal and Pre-Appeal Brief Request for Review submitted herewith, the Applicant requests review of the following issues on appeal.

Request for at least three examiners on the panel

In order to facilitate full consideration of the remarks filed herewith, the Applicant respectfully requests that the Art Unit Supervisor designate a panel composed of at least three examiners.

Claims 1-4, 7, and 10 are novel in view of the cited reference Teig

On page 2 of the Final Action, claims 1-4, 7, and 10 are rejected under 35 U.S.C. § 102(a)(1) as being anticipated by Teig (US 2019/0123022). As explained further below, these rejections are improper, as the cited reference fail to disclose or suggest at least one feature of each of claims 1-4, 7, and 10.

To illustrate, claim 1 recites:

A system, comprising:
a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array, wherein the GPU chiplet array includes:
the first GPU chiplet communicably coupled to the CPU via a bus; and
a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications.

Thus, claim 1 provides for a GPU chiplet array comprising a first GPU communicably coupled to a CPU via a bus and a second CPU chiplet that is communicably coupled to the first GPU chiplet via a passive crosslink dedicated for inter-chiplet communications. An example of these features is illustrated at FIG. 1 of the application, reproduced below:

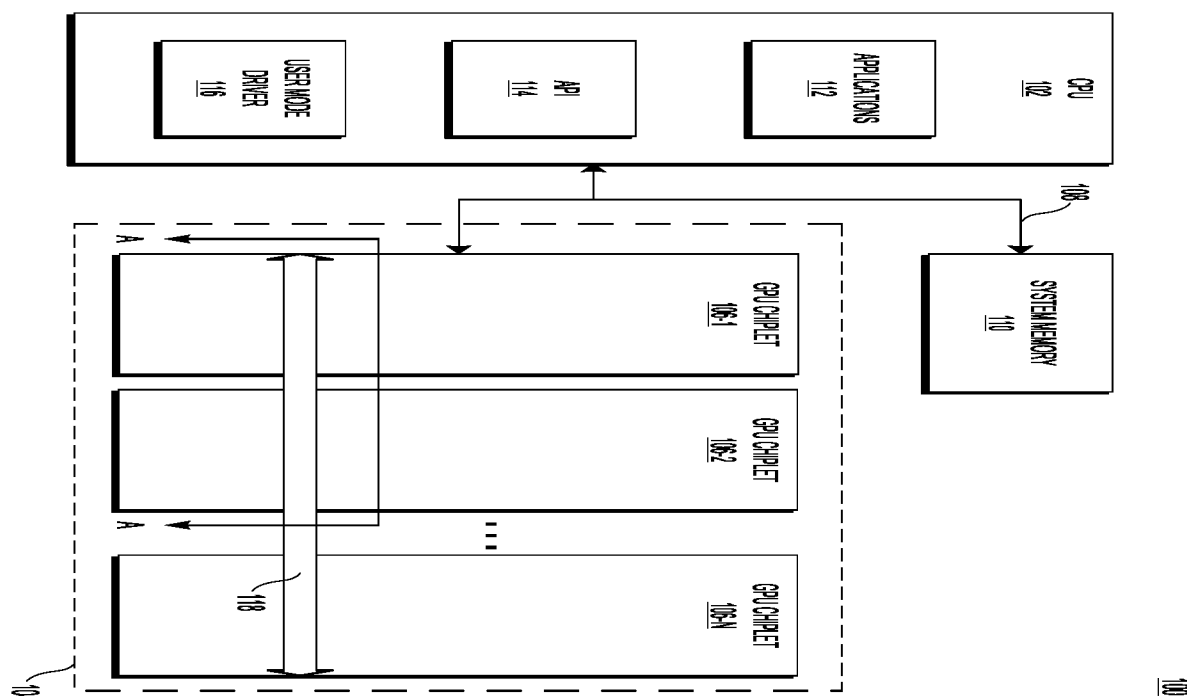


Figure 1 of Present Application

Regarding the features of claim 1, on page 2, the Final Action directs the Applicant to the CPU and GPU in FIG. 9 of Teig and the passive interposer in paragraph [0148] of Teig. Teig describes FIG. 9, the CPU, and the GPU in paragraphs [0090] and [0091] as follows:

FIG. 9 illustrates yet another 3D processor 900 of some embodiments. This processor 900 is identical to the processor 400 of FIG. 4, except that it only has one L1 cache 932 on a die 910 for each of six CPU (central processing unit) cores 922 and one L1 cache 934 for each of two GPU (graphical processing unit) cores 924 that are defined on a die 905 that is face-to-face mounted to the die 910 through a DBI bonding process. The processor 900 does not use layers 2 and 3 caches as it uses large L1 caches for its CPU and GPU cores. The L1 caches can be larger than traditional L1 caches as they are defined on another die than the die on which the cores are defined, and hence face less space restrictions on their placement and the amount of space that they consume on the chip.

In FIG. 9, the processor 900 has its I/O interface defined on a third die 415 that is face-to-back mounted on the die 910. In other embodiments, the processor 900 does not include the third die 415, but just includes the first and second dies 905 and 910. In some of these embodiments, the I/O interface of the processor 900 is defined on the first and/or second dies 905 and 910. Also, in other embodiments, one L1 cache 932 is shared across multiple CPU cores 922 and/or multiple GPU cores 924.

As shown, Teig generally mentions GPU cores. Nowhere does Teig disclose that the GPU cores are GPU chiplets. Also, even assuming *arguendo* that Teig's GPU cores are comparable to the GPU chiplets of claim 1, nowhere does Teig disclose both that a first GPU core is communicably coupled to the CPU via a bus and a second GPU core is coupled to the first GPU chiplet via a passive crosslink. The cited sections of Teig fail to provide any details regarding how the GPU cores are coupled to the CPU and each other. Also, regarding the passive crosslink of claim 1, this claim requires that "the passive crosslink is dedicated for inter-chiplet communications." In contrast, paragraph [0148] of Teig merely states, "the first IC die is face-to-face mounted with a passive interposer that electrically connects the die to circuits outside of the 3D chip or to other dies that are face-to-face mounted or back-to-face mounted on the interposer." Nowhere in paragraph [0148] does Teig disclose that the passive interposer is dedicated for inter-chiplet communications. Teig, therefore, fails to disclose at least the aforementioned features of claim 1. As such, Teig fails to anticipate claim 1 since each and every element set forth in claim 1 is not found or literally present in Teig. Claim 1 is, therefore, novel over Teig.

Teig also fails to teach the features of dependent claims 2-4, 7, and 10, at least by virtue of their dependence on claim 1. Claims 2-4, 7, and 10 are, therefore, novel over Teig.

Claims 5, 6, 8, and 11-20 are novel and non-obvious in view of Tieg and Yasuda

On page 4 of the Final Action, claims 65, 6, 8, and 11-20 are rejected under 35 U.S.C. § 103 as being unpatentable over Tieg in view of Yasuda (US 2001/0005873).

Claims 5, 6, and 8 depend on claim 1. As explained above, Teig fails to disclose or render obvious the features of claim 1. Further, Yasuda does not remedy the deficiencies of Teig. Accordingly, the cited references, individually and in combination, fail to disclose or render obvious the features of independent claim 1. Therefore, the cited references fail to

disclose the features of dependent claims 5, 6, and 8, at least by virtue of their dependence on claim 1. In addition, these dependent claims recite additional novel and non-obvious features. For example, regarding the feature of “wherein the first PHY region of the first GPU chiplet comprises a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the first GPU chiplet” set forth in claim 5, the Final Action on page 4 asserts “Teig discloses the system recited in claims 1 and 4” and “Yasuda discloses cache coherency protocol in the abstract.” However, the Final Action fails to provide any identification of the sections in Teig that disclose or suggest the features of claim 5. As discussed above, paragraph [0148] of Teig simply states a passive interposer electrically connects the die to circuits outside of the 3D chip or to other dies that are face-to-face mounted or back-to-face mounted on the interposer. Nowhere does Teig disclose or suggest the specific features of “wherein the first PHY region of the first GPU chiplet comprises a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the first GPU chiplet” required by claim 5. Yasuda fails to remedy these deficiencies of Teig. As such, Teig and Yasuda, individually and in combination, fail to disclose or render obvious claim 5. Claim 4 is, therefore, novel and non-obvious over Teig and Yasuda.

Regarding independent claims 11 and 16, on page 4, the Final Action states, “the examiner directs the applicant’s attention to claims rejection above.” As such, since the Final Action appears to be comparing claims 11 and 16 to claim 1, these claims are novel over Teig for at least the reasons presented above with respect to claim 1.

Claims 12-15 and 17-20 depend on claims 11 and 16, respectively. As explained above, Teig fails to disclose or render obvious the features of claims 11 and 16. Further, Yasuda does not remedy the deficiencies of Teig. Accordingly, the cited references, individually and in combination, fail to disclose or render obvious the features of independent claims 11 and 16. Therefore, the cited references fail to disclose the features of dependent claims 12-15 and 17-20, at least by virtue of their respective dependence on claims 11 and 16. In addition, these dependent claims recite additional novel and non-obvious features.

Furthermore, method claim 11 and computer-readable medium (CRM) claim 16 include different features than system claim 1. As such, by applying the rejection of system claim 1 to

method claim 11 and CRM claim 16 without providing a clear articulation of the reason(s) why the operational features of these claims are anticipated or obvious in view of the cited art, the Final Action has placed an undue burden on the Applicant. MPEP § 2143, citing *KSR*, states that “[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit.” See also *KSR Intl Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1395-97 (2007). The Applicant notes that while *KSR* and the cited section of the MPEP are directed to obviousness rejections under 35 U.S.C. § 103, it is apparent that the Supreme Court believes that a clear articulation of reasons is “the key” to supportable rejections by the USPTO under both 35 U.S.C. §102 and §103. Without proper guidance on which “element” of the claims is believed to correspond with which section cited in the rejection, the Applicant is forced to guess which features in the cited art the Examiner believes to disclose each of the claimed features. Because reasons for the rejection of claims 11-20 were not presented in the Final Action and the Applicant cannot reasonably determine which feature of Teig is believed to correspond with which feature recited in claims, the Applicant respectfully submits that the rejection is improper and must be withdrawn.

Conclusion

The Applicant respectfully submits that, for at least the reasons set forth above, the present rejections of claims 1-8 and 10-20 are improper. Withdrawal of the rejections and reconsideration of the claims 1-8 and 10-20 is respectfully requested.

Respectfully submitted,

/Thomas S. Grzesik/
Thomas S. Grzesik, Reg. No. 54,139
DAVIDSON SHEEHAN LLPs
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Austin, Texas 78731
(512) 582-2455 (phone)
(512) 355-1119 (fax)

September 15, 2021
Date

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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NOTICE OF APPEAL FROM THE EXAMINER TO THE PATENT TRIAL AND APPEAL BOARD		Docket Number (Optional) 1458-190070								
I hereby certify that this correspondence is being facsimile transmitted to the USPTO, EFS-Web transmitted to the USPTO, or deposited with the United States Postal Service with sufficient postage in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, on Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on <u>September 15, 2021</u> . Signature <u>/Rachelle Chery/</u> Typed or printed name <u>Rachelle Chery</u>	<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2" style="padding: 5px;">In re Application of SALEH, Skyler J. et al.</td> </tr> <tr> <td style="width: 60%; padding: 5px;">Application Number 16/456,287</td> <td style="padding: 5px;">Filed June 28, 2019</td> </tr> <tr> <td colspan="2" style="padding: 5px;">For GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS</td> </tr> <tr> <td style="padding: 5px;">Art Unit 2135</td> <td style="padding: 5px;">Examiner YU, Jae Un</td> </tr> </table>		In re Application of SALEH, Skyler J. et al.		Application Number 16/456,287	Filed June 28, 2019	For GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		Art Unit 2135	Examiner YU, Jae Un
In re Application of SALEH, Skyler J. et al.										
Application Number 16/456,287	Filed June 28, 2019									
For GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS										
Art Unit 2135	Examiner YU, Jae Un									
Applicant hereby appeals to the Patent Trial and Appeal Board from the last decision of the examiner.										
The fee for this Notice of Appeal is (37 CFR 41.20(b)(1)) \$ <u>840.00</u>										
☐ Applicant asserts small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by 50%, and the resulting fee is: \$ <u> </u>										
☐ Applicant certifies micro entity status. See 37 CFR 1.29. Therefore, the fee shown above is reduced by 75%, and the resulting fee is: Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously. \$ <u> </u>										
☐ A check in the amount of the fee is enclosed.										
☐ Payment by credit card. Form PTO-2038 is attached.										
☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. <u>50-5933</u> .										
☒ Payment made via EFS-Web.										
☐ A petition for an extension of time under 37 CFR 1.136(a) (PTO/AIA/22 or equivalent) is enclosed. For extensions of time in reexamination proceedings, see 37 CFR 1.550.										
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☐ applicant ☒ attorney or agent of record Registration number <u>54139</u> ☐ attorney or agent acting under 37 CFR 1.34 Registration number <u> </u>										
Signature <u>/Thomas S. Grzesik/</u>										
Typed or printed name <u>Thomas S. Grzesik</u>										
Telephone Number <u>512-582-2455</u>										
Date <u>September 15, 2021</u>										
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☒ * Total of <u>1</u> forms are submitted.										

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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Electronic Patent Application Fee Transmittal				
Application Number:		16456287		
Filing Date:		28-Jun-2019		
Title of Invention:		GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		
First Named Inventor/Applicant Name:		Skyler J. SALEH		
Filer:		Ryan Scott Davidson/Rachelle Chery		
Attorney Docket Number:		1458-190070		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
NOTICE OF APPEAL	1401	1	840	840
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Extension - 1 month with \$0 paid	1251	1	220	220
Miscellaneous:				
Total in USD (\$)				1060

Electronic Acknowledgement Receipt

EFS ID:	43767666
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Ryan Scott Davidson
Filer Authorized By:	
Attorney Docket Number:	1458-190070
Receipt Date:	15-SEP-2021
Filing Date:	28-JUN-2019
Time Stamp:	11:00:02
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1060
RAM confirmation Number	E20219EB00254076
Deposit Account	505933
Authorized User	Ryan Davidson

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37 CFR 1.17 (Patent application and reexamination processing fees)

37 CFR 1.16 (National application filing, search, and examination fees)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Pre-Brief Conference request	190070_US_PABR.pdf	222265	no	2
			d9c993e7a3a61ebc9fd5efc42259b76410c6e871		
Warnings:					
Information:					
2	Pre-Brief Conference request	190070_US_Pre_Appeal_Brief.pdf	135962	no	5
			d48f52e78b77965c6b338ee00d702422fd2959e3		
Warnings:					
Information:					
3	Notice of Appeal Filed	190070_US_Notice_of_Appeal.pdf	278581	no	2
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Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	40712	no	2
			b260d8d9bbebcc689774f7b92291e5a1cd7c2431		
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Information:					
Total Files Size (in bytes):			677520		

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16456287
	Filing Date		2019-06-28
	First Named Inventor	Skyler J. SALEH	
	Art Unit	2135	
	Examiner Name	Jae Un Yu	
	Attorney Docket Number	1458-190070	

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		16456287
Filing Date		2019-06-28
First Named Inventor	Skyler J. SALEH	
Art Unit	2135	
Examiner Name	Jae Un Yu	
Attorney Docket Number	1458-190070	

1	Notice of Allowance issued June 10, 2021 in Application No. 16/698,624 (Atty. Docket No. 1458-190143), 29 pages.	☐
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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un Yu
Attorney Docket Number	1458-190070

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/RYAN DAVIDSON/	Date (YYYY-MM-DD)	2021-06-30
Name/Print	Ryan Davidson	Registration Number	51,596

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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Electronic Acknowledgement Receipt

EFS ID:	43141242
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Ryan Scott Davidson/David Edwards
Filer Authorized By:	Ryan Scott Davidson
Attorney Docket Number:	1458-190070
Receipt Date:	30-JUN-2021
Filing Date:	28-JUN-2019
Time Stamp:	18:11:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	190070-IDS.pdf	70609	no	4
			e1795fbf56bb02a25a2121560a81df23a866a2b5		

Warnings:

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2	Non Patent Literature	190143-NOA.pdf	497867	no	9
			b2aeceaa59b2cc77305d7cdd997dac704f6c63f3		

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National Stage of an International Application under 35 U.S.C. 371

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/456,287	06/28/2019	Skyler J. SALEH	1458-190070	4820
109712	7590	05/17/2021	EXAMINER	
Advanced Micro Devices, Inc. c/o Davidson Sheehan LLP 6836 Austin Center Blvd. Suite 320 Austin, TX 78731			YU, JAE UN	
			ART UNIT	PAPER NUMBER
			2135	
			NOTIFICATION DATE	DELIVERY MODE
			05/17/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

AMD@DS-patent.com
docketing@ds-patent.com

Office Action Summary	Application No. 16/456,287	Applicant(s) SALEH et al.	
	Examiner JAE U YU	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 2/25/21.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-8 and 10-20 is/are rejected.
- 8) ☒ Claim(s) 9 is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 3/9/21.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date ____.
- 4) ☐ Other: ____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

1. Claims 1-4, 7, and 10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Teig et al. (US 2019/0123022), “Teig”.
2. As per **claim 1**, Teig discloses a central processing unit (CPU) **[CPU, figure 9]** communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array **[GPU, figure 9]**, wherein the GPU chiplet array includes: the first GPU chiplet **[GPU cores, figure 9]** communicably coupled to the CPU via a bus **[CPU cores, figure 9]**; and a second GPU chiplet **[GPU cores, figure 9]** communicably coupled to the first GPU chiplet via a passive crosslink **[CPU cores, figure 9]**, wherein the passive crosslink is dedicated for inter-chiplet communications **[a passive interposer, paragraph 148]**.
3. As per **claim 2**, Teig discloses wherein the passive crosslink comprises a passive interposer die **[a passive interposer, paragraph 148]**.

4. As per **claim 3**, Teig discloses wherein the first GPU chiplet comprises a first PHY region including conductor structures for chiplet-to-chiplet communications, and further wherein the second GPU chiplet comprises a second PHY region including conductor structures for chiplet-to-chiplet communications [**passive interposers, paragraph 148**].
5. As per **claim 4**, Teig discloses a third GPU chiplet communicably coupled to the first GPU chiplet via the passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications, wherein the third GPU chiplet comprises a third PHY region including conductor structures for chiplet-to-chiplet communications [**passive interposers, paragraph 148**].
6. As per **claim 7**, Teig discloses wherein the passive crosslink communicably couples all GPU chiplets in the GPU chiplet array [**passive interposers, paragraph 148**].
7. As per **claim 10**, Teig discloses a plurality of conductive pillars coupling a circuit board substrate to a first non-PHY region of the first GPU chiplet and a second non-PHY region of the second GPU chiplet [**z-axis interconnects, figure 16**].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 5, 6, 8, and 11-20 are rejected under 35 U.S.C. 103 as being unpatentable over Teig et al. (US 2019/0123022), "Teig", in view of Yasuda et al. (US 2001/0005873), "Yasuda".

2. As per **claims 5, 6, and 8**, Teig discloses the system recited in claims 1 and 4.

Teig does not disclose expressly a last level cache.

Yasuda discloses cache coherency protocol in the abstract.

Teig and Yasuda are analogous art because they are from the same field of endeavor of storage device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Teig by including the cache coherency protocol as taught by Yasuda in the abstract.

The motivation for doing so would have been better addressing performance as expressly taught by Yasuda in paragraph 19.

3. As per **claims 11-20**, the examiner directs the applicant's attention to claims rejection above.

Arguments Concerning Prior Art Rejections

The applicant argues that the cited prior art does not disclose the claimed limitation(s). Specifically, the applicant asserts that the cited prior art fails to teach the claimed GPU chiplets. However, there is no patentable distinction between such GPU chiplets and the GPU cores disclosed in figure 9 of Teig.

Further, the applicant argues that the cited prior art does not disclose coupling a GPU chiplet with a CPU with a bus. However, figure 9 and paragraphs 90-91 of Teig disclose GPU(s) and CPU(s) sharing a cache. Thus, the components are "coupled" to each other, and the rejection is maintained.

Moreover, the applicant asserts that the cited “passive interposer” can’t be interpreted as the claimed “passive crosslink”. However, Teig discloses implanting the “passive interposer” for inter-chip communication in paragraph 148. Thus, Teig discloses coupling GPUs with the “passive interposer” (claimed “passive crosslink”), and the rejection is maintained.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Allowable Subject Matter

Claim 9 is objected to.

The primary reasons for allowance of claim 9 in the instant application is the combination with the inclusion in these claims that “a unified cache memory including both a last level of the first cache memory hierarchy and a last level of the second cache memory hierarchy, wherein the unified cache memory is coherent across all chiplets of the GPU chiplet array”. The prior art of record neither anticipates nor renders obvious the above recited combination.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

B. Claims Rejected

Claims 1-8 and 10-20 are rejected.

C. Direction for Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAE UN YU whose telephone number is (571)272-1133. The examiner can normally be reached on M-F 9-5.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 16/456,287
Art Unit: 2135

Page 7

/JAE U YU/
Primary Examiner, Art Unit 2135

<i>Index of Claims</i> 	Application/Control No. 16/456,287	Applicant(s)/Patent Under Reexamination SALEH et al.
	Examiner JAE U YU	Art Unit 2135

✓	Rejected
=	Allowed

-	Cancelled
÷	Restricted

N	Non-Elected
I	Interference

A	Appeal
O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	09/08/2020								
	1	✓								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	O								
	10	✓								
	11	✓								
	12	✓								
	13	✓								
	14	✓								
	15	✓								
	16	✓								
	17	✓								
	18	✓								
	19	✓								
	20	✓								

<i>Search Notes</i> 	Application/Control No. 16/456,287	Applicant(s)/Patent Under Reexamination SALEH et al.
	Examiner JAE U YU	Art Unit 2135

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	118	05/12/2021	/J.U.Y/

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST	05/12/2021	/J.U.Y/
NPL Search	05/12/2021	/J.U.Y/

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/J.U.Y/ Primary Examiner, Art Unit 2135	
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16456287
	Filing Date		2019-06-28
	First Named Inventor	Skyler J. SALEH	
	Art Unit	2135	
	Examiner Name	Jae Un YU	
	Attorney Docket Number	1458-190070	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8860741	B1	2014-10-14	JUFFA et al.	
	2	10282811	B2	2019-05-07	RAY et al.	
	3	10803548	B2	2020-10-13	MATAM et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add
U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20180102251	A1	2018-04-12	DELACRUZ et al.	
	2	20190245582	A1	2019-08-08	BURTON	
	3	20180246814	A1	2018-08-30	JAYASENA et al.	

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.U.Y/

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

4	20180102338	A1	2018-04-12	MCLELLAN
5	20150243528	A1	2015-08-27	WHITING et al.
6	20180233470	A1	2018-08-16	KILLER et al.
7	20110087864	A1	2011-04-14	DULUK, JR. et al.
8	20130286034	A1	2013-10-31	DIARD
9	20180293205	A1	2018-10-11	KOKER et al.
10	20180300098	A1	2018-10-18	VEMBAR et al.

If you wish to add additional U.S. Published Application citation information please click the Add button.

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FOREIGN PATENT DOCUMENTS

Remove

Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ^{2,i}	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	2019032322	WO	A1	2019-02-14	ADVANCED MICRO DEVICES, INC.		

If you wish to add additional Foreign Patent Document citation information please click the Add button

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NON-PATENT LITERATURE DOCUMENTS

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.U.Y/

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Non-Final Office Action issued January 4, 2021 in Application No. 16/585,452 (Atty. Docket No. 1458-190141), 25 pages.	
	2	International Search Report and Written Opinion issued December 30, 2020 in Application No. PCT/US2020/052433 (Atty. Docket No. 190141-PCT, 12 pages.	
	3	BURD, Thomas, et al., "Zeppelin": An SoC for Multichip Architectures", IEEE Journal of Solid-State Circuits, vol. 54, no. 1, January 2019, pp. 133-143.	
	4	International Search Report and Written Opinion issued December 30, 2020 in Application No. PCT/US2020/052444 (Atty. Docket No. 190142-PCT), 12 pages.	
	5	Non-Final Office Action issued November 13, 2020 in Application No. 16/698,624 (Atty. Docket No. 1458-190143), 40 pages.	

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/JAE U YU/	Date Considered	05/12/2021
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.U.Y/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ryan S. Davidson/	Date (YYYY-MM-DD)	2021-03-09
Name/Print	Ryan S. Davidson	Registration Number	51596

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	7,783	(711/118).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/07 19:15
S2	184	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:17
S3	0	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:18
S4	0	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab. and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20
S5	0	(cpu near5 gpu\$2).ab. and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20
S6	28	(cpu near5 gpu\$2) and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20
S7	244	gpu near7 cpu near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 15:03
S8	410	gpu with cpu with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 15:03
S9	2,120	(cach\$3 near5 coheren\$4).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:01

S10	151	gpu same cpu same cach\$3 same (level\$2 low\$3 "l2" level-2) and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:01
S11	901	(cach\$3 near5 coheren\$4).ti. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:02
S12	1,550	(cach\$3 near5 coheren\$4).ab. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:02
S13	66	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31
S14	918	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31
S15	94	gpu with (coheren\$4 dirty invalid\$4) with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31
S16	35	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:32
S17	126	gpu near7 cpu near7 cach\$3 near7 (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:22
S18	178	gpu with cpu with cach\$3 with (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	OFF	2020/09/08 17:23

			DERWENT; IBM_TDB			
S19	123	("8645640" "8650367" "8683160" "9372797" "9858188" "10331563" "20120330802" "20120330803" "20120331231" "20150227464" "20150269076" "20180052771" "20190266093" "8125418" "8207954" "8279145" "8456387" "8497821" "8698391" "8803857" "9070323" "9492993" "10468363" "20100123694" "20100207848" "20100207849" "20100207851" "20100265224" "20100277440" "20100328196" "20120206499" "20150251402" "20170048976" "20190371753" "20200051961" "20200105697" "10295588" "20180180665" "8679861" "8796047" "20100015732" "20140159803" "20190243700" "5663854" "5963397" "6049443" "6425109" "6966042" "7243325" "7733127").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:24
S20	73	gpu near7 cpu near7 cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:26
S21	131	gpu with cpu with cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:26
S22	39	(SALEH near2 SKYLER).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:31
S23	446	(NAFFZIGER near2 SAMUEL).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:31
S24	110	(BHAGAVAT near2 MILIND).in.	US-PGPUB; USPAT; USOCR; FPRS;	OR	OFF	2020/09/08 17:32

			EPO; JPO; DERWENT; IBM_TDB			
S25	163	(AGARWAL near2 RAHUL).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:33
S26	214	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2021/05/12 16:32
S27	32	(cpu near5 gpu\$2) and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2021/05/12 16:32
S28	297	gpu near7 cpu near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:33
S29	494	gpu with cpu with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:33
S30	151	gpu same cpu same cach\$3 same (level\$2 low\$3 "l2" level-2) and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:33
S31	73	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:44
S32	102	gpu with (coheren\$4 dirty invalid\$4) with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:44
S33	35	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 and 711/\$.ccls.	US-PGPUB; USPAT;	OR	OFF	2021/05/12 16:44

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S34	136	gpu near7 cpu near7 cach\$3 near7 (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:44
S35	244	gpu with cpu with cach\$3 with (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:44
S36	78	gpu near7 cpu near7 cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:54
S37	137	gpu with cpu with cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:54
S38	7,813	(711/118).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/05/12 16:54

5/12/2021 8:02:34 PM

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PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16456287
	Filing Date		2019-06-28
	First Named Inventor	Skyler J. SALEH	
	Art Unit	2135	
	Examiner Name	Jae Un YU	
	Attorney Docket Number	1458-190070	

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	2	10282811	B2	2019-05-07	RAY et al.	
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	2	20190245582	A1	2019-08-08	BURTON	
	3	20180246814	A1	2018-08-30	JAYASENA et al.	

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Application Number	16456287
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First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

4	20180102338	A1	2018-04-12	MCLELLAN
5	20150243528	A1	2015-08-27	WHITING et al.
6	20180233470	A1	2018-08-16	KILLER et al.
7	20110087864	A1	2011-04-14	DULUK, JR. et al.
8	20130286034	A1	2013-10-31	DIARD
9	20180293205	A1	2018-10-11	KOKER et al.
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	1	2019032322	WO	A1	2019-02-14	ADVANCED MICRO DEVICES, INC.		

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Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

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	1	Non-Final Office Action issued January 4, 2021 in Application No. 16/585,452 (Atty. Docket No. 1458-190141), 25 pages.	
	2	International Search Report and Written Opinion issued December 30, 2020 in Application No. PCT/US2020/052433 (Atty. Docket No. 190141-PCT, 12 pages.	
	3	BURD, Thomas, et al., "'Zeppelin': An SoC for Multichip Architectures", IEEE Journal of Solid-State Circuits, vol. 54, no. 1, January 2019, pp. 133-143.	
	4	International Search Report and Written Opinion issued December 30, 2020 in Application No. PCT/US2020/052444 (Atty. Docket No. 190142-PCT), 12 pages.	
	5	Non-Final Office Action issued November 13, 2020 in Application No. 16/698,624 (Atty. Docket No. 1458-190143), 40 pages.	

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Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2135
Examiner Name	Jae Un YU
Attorney Docket Number	1458-190070

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Ryan S. Davidson/	Date (YYYY-MM-DD)	2021-03-09
Name/Print	Ryan S. Davidson	Registration Number	51596

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H01L 23/31 (2006.01)
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- (71) **Applicant:** **ADVANCED MICRO DEVICES, INC.** [US/US]; 2485 Augustine Drive, Santa Clara, CA 95054 (US).
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- (74) **Agent:** **HONEYCUTT, Timothy Mark**; 37713 Parkway Oaks Lane, Magnolia, TX 77355 (US).
- (81) **Designated States** (*unless otherwise indicated, for every kind of national protection available*): AE, AG, AL, AM, AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ, CA, CH, CL, CN, CO, CR, CU, CZ, DE, DJ, DK, DM, DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IR, IS, JO, JP, KE, KG, KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY, MA, MD, ME, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO, RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, SM, ST, SV, SY, TH, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.
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(54) **Title:** MOLDED CHIP COMBINATION

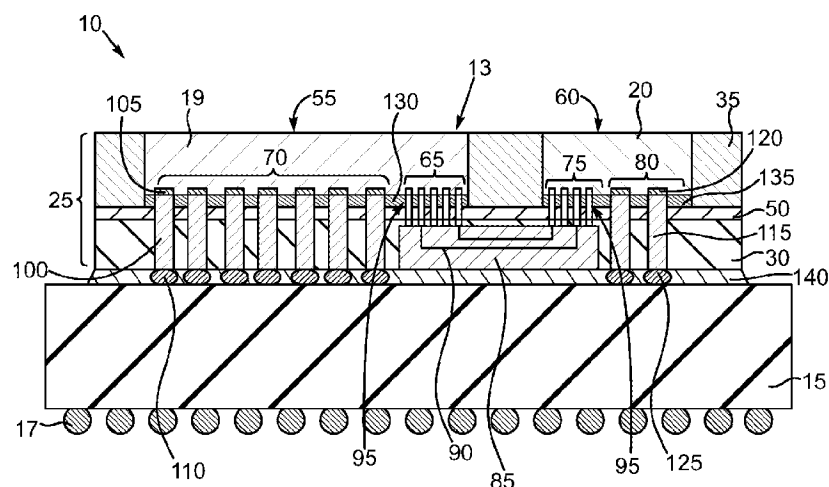


FIG. 2

(57) **Abstract:** Various molded chip combinations and methods of manufacturing the same are disclosed. In one aspect, a molded chip combination is provided that includes a first semiconductor chip (20) that has a first PHY region (75), a second semiconductor chip (19) that has a second PHY region (65), an interconnect chip (85) interconnecting the first PHY region to the second PHY region, and a molding (25) joining together the first semiconductor chip, the second semiconductor chip and the interconnect chip.

[Continued on next page]

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TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*

Published:

- *with international search report (Art. 21(3))*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments (Rule 48.2(h))*

MOLDED CHIP COMBINATION

BACKGROUND OF THE INVENTION

[0001] A conventional type of multi-chip module includes two semiconductor chips mounted side-by-side on a carrier substrate or in some cases on an interposer (so-called “2.5D”) that is, in-turn,
5 mounted on a carrier substrate. The semiconductor chips are flip-chip mounted to the carrier substrate and interconnected thereto by respective pluralities of solder joints. The carrier substrate is provided with plural electrical pathways to provide input/output pathways for the semiconductor chips both for inter-chip power, ground and signal propagation as well as input/output from the interposer itself. The semiconductor chips include respective underfill material layers to lessen the effects of
10 differential thermal expansion due to differences in the coefficients of thermal expansion of the chips, the interposer and the solder joints.

[0002] One conventional variant of 2.5D interposer-based multi-chip modules uses a silicon interposer with multiple internal conductor traces for interconnects between two chips mounted side-by-side on the interposer. The interposer is manufactured with multitudes of through-silicon vias
15 (TSVs) to provide pathways between the mounted chips and a package substrate upon which the interposer is mounted. The TSVs and traces are fabricated using large numbers of processing steps.

[0003] Another conventional multi-chip module technology is 2D wafer-level fan-out (or 2D WLFO). Conventional 2D WLFO technology is based on embedding die into a molded wafer, also called “wafer reconstitution.” The molded wafer is processed through a standard wafer level
20 processing flow to create the final integrated circuit assembly structure. The active surface of the dies are coplanar with the mold compound, allowing for the “fan-out” of conductive copper traces and solder ball pads into the molded area using conventional redistribution layer (RDL) processing. Conventional 3D WLFO extends the 2D technology into multi-chip stacking where a second package substrate is mounted on the 2D WLFO.

[0004] Some other conventional designs use embedded interconnect bridges (EMIB). These are
25 typically silicon bridge chips (but occasionally organic chiplets with top side only input/outputs) that are embedded in the upper reaches of a package substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] The foregoing and other advantages of the invention will become apparent upon reading the following detailed description and upon reference to the drawings in which:

[0006] FIG. 1 is a pictorial view of an exemplary semiconductor chip device that includes an exemplary molded chip combination;

[0007] FIG. 2 is a sectional view of FIG. 1 taken at section 2-2;

[0008] FIG. 3 is a portion of FIG. 2 shown at increased magnification;

[0009] FIG. 4 is a sectional view depicting exemplary temporary multi-chip mounting;

[0010] FIG. 5 is a sectional view depicting exemplary temporary multi-chip mounting;

[0011] FIG. 6 is a sectional view depicting exemplary molding of multiple chips;

[0012] FIG. 7 is a sectional view depicting additional processing of the chips;

[0013] FIG. 8 is a sectional view depicting additional processing of the chips;

[0014] FIG. 9 is a sectional view depicting additional processing of the chips;

[0015] FIG. 10 is a sectional view depicting additional processing of the chips;

[0016] FIG. 11 is a sectional view depicting a portion of FIG. 10 at greater magnification;

[0017] FIG. 12 is a sectional view depicting additional processing of the chips;

[0018] FIG. 13 is a sectional view depicting additional processing of the chips;

[0019] FIG. 14 is a sectional view depicting a portion of FIG. 13 at greater magnification;

[0020] FIG. 15 is a sectional view depicting exemplary mounting of an interconnect chip on the chips;

[0021] FIG. 16 is a sectional view depicting a portion of FIG. 15 at greater magnification;

[0022] FIG. 17 is a sectional view depicting additional processing of the chips;

[0023] FIG. 18 is a sectional view depicting additional processing of the chips;

[0024] FIG. 19 is a sectional view depicting additional processing of the chips;

[0025] FIG. 20 is a sectional view depicting exemplary mounting of the chips on an exemplary circuit board;

[0026] FIG. 21 is a sectional view depicting exemplary mounting of a heat sink on the chips;

[0027] FIG. 22 is a sectional view like FIG. 2, but of an alternate exemplary semiconductor chip device with an alternate exemplary molded chip combination;

[0028] FIG. 23 is a sectional depicting exemplary interconnect chip mounting on the device of FIG. 22;

[0029] FIG. 24 is a sectional view depicting exemplary board mounting and molding;

[0030] FIG. 25 is a sectional view depicting exemplary mounting of a heat sink on the molded chip combination;

[0031] FIG. 26 is a sectional view depicting exemplary initial processing of small portions of PHY region and non-PHY region pads of a semiconductor chip;

5 [0032] FIG. 27 is a plan view of the PHY region and non-PHY regions depicted in FIG. 26;

[0033] FIG. 28 is a sectional view like FIG. 26, but depicting exemplary additional processing of the chip;

[0034] FIG. 29 is a sectional view like FIG. 28, but depicting exemplary additional processing of the chip;

10 [0035] FIG. 30 is a plan view of the portion of the chip depicted in FIG. 29;

[0036] FIG. 31 is a pictorial view of the masking layer depicted in FIG. 30;

[0037] FIG. 32 is a plan view of the portion of the chip depicted in FIG. 29 but after additional processing;

[0038] FIG. 33 is an exploded pictorial view depicting additional processing of the chip;

15 [0039] FIG. 34 is a sectional view like 28, but depicting exemplary additional processing of the chip;

[0040] FIG. 35 is a plan view of a portion of the chip depicted in FIG. 34; and

[0041] FIG. 36 is a pictorial view of an exemplary reconstituted molded chip combination wafer.

DETAILED DESCRIPTION

[0042] Chip geometries have continually fallen over the past few years. However the shrinkage in chip sizes has been accompanied by an attendant increase in the number of input/outputs for a given chip. This has led to a need to greatly increase the number of chip-to-chip interconnects for multi-chip modules. Current 2D and 3D WLFO have limited minimum line spacing, on the order of 2.0 μm /line and space. In addition, conventional WLFO techniques use multiple cured polyimide films to create the requisite RDL layers. These polyimide films tend to be mechanical stress, and thus warpage, sources and their relatively high bake temperatures can adversely impact other sensitive devices. Finally, pick and place accuracy of chips in both WLFO and EMIB remains a challenge.

[0043] In accordance with one aspect of the present invention, a molded chip combination is provided that includes a first semiconductor chip that has a first PHY region, a second semiconductor chip that has a second PHY region, an interconnect chip interconnecting the first PHY region to the second PHY region, and a molding joining together the first semiconductor chip, the second semiconductor chip and the interconnect chip.

[0044] The molded chip combination wherein the first semiconductor chip includes a first plurality of interconnects to connect to a circuit board when the molded chip combination is mounted on the circuit board and the second semiconductor chip includes a second plurality of interconnects to connect to the circuit board when the molded combination is mounted on the circuit board.

[0045] The molded chip combination wherein the first semiconductor chip includes a first non-PHY region connected to the first interconnects and the second semiconductor chip includes a second non-PHY region connected to the second interconnects.

[0046] The molded chip combination wherein the molding includes a first molding material layer and a second molding material layer.

[0047] The molded chip combination including a polymer layer positioned between the first molding material layer and the second molding material layer.

[0048] The molded chip combination including a circuit board and the molded chip combination mounted on the circuit board.

[0049] The molded chip combination wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.

[0050] In accordance with another aspect of the present invention, a molded chip combination is provided that includes a first semiconductor chip that has a first PHY region, a second semiconductor chip that has a second PHY region, an interconnect chip interconnecting the first PHY region to the second PHY region, a first molding material layer joining together the first semiconductor chip and

the second semiconductor chip, and a second molding material layer joined to the first molding material layer and at least partially encapsulating the interconnect chip.

[0051] The molded chip combination wherein the first semiconductor chip includes a first plurality of interconnects to connect to a circuit board when the molded chip combination is mounted on the circuit board and the second semiconductor chip includes a second plurality of interconnects to connect to the circuit board when the molded combination is mounted on the circuit board.

[0052] The molded chip combination wherein the first semiconductor chip includes a first non-PHY region connected to the first interconnects and the second semiconductor chip includes a second non-PHY region connected to the second interconnects.

[0053] The molded chip combination including a polymer layer positioned between the first molding material layer and the second molding material layer.

[0054] The molded chip combination including a circuit board and the molded chip combination mounted on the circuit board.

[0055] The molded chip combination wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.

[0056] In accordance with another aspect of the present invention, a method of manufacturing a molded chip combination is provided. The method includes interconnecting a first PHY region of a first semiconductor chip to a second PHY region of a second semiconductor chip with an interconnect chip, and molding together the first semiconductor chip, the second semiconductor chip and the interconnect chip.

[0057] The method including fabricating a first plurality of interconnects on the first semiconductor chip to connect to a circuit board when the molded chip combination is mounted on the circuit board and a second plurality of interconnects on the second semiconductor chip to connect to the circuit board when the molded combination is mounted on the circuit board.

[0058] The method wherein the first semiconductor chip includes a first non-PHY region connected to the first interconnects and the second semiconductor chip includes a second non-PHY region connected to the second interconnects.

[0059] The method wherein the molding comprises molding the first semiconductor chip to the second semiconductor chip with a first molding material layer and molding a second molding material layer to at least partially encapsulate the interconnect chip.

[0060] The method including applying a polymer layer between the first molding material layer and the second molding material layer.

[0061] The method including mounting the molded chip combination on a circuit board.

[0062] The method wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.

[0063] In the drawings described below, reference numerals are generally repeated where identical elements appear in more than one figure. Turning now to the drawings, and in particular to FIG. 1 which is a pictorial view of an exemplary semiconductor chip device 10. The semiconductor chip device 10 includes a molded chip combination 13, which can be mounted on a circuit board 15, which can be a system board, circuit card, a semiconductor chip package substrate or otherwise. The circuit board 15 can interface electrically with some other electrical structure, such as another circuit board or other structure by way of plural interconnect structures 17 which in this arrangement constitute solder balls. However, the skilled artisan will appreciate that various types of interconnect structures could be used other than solder balls, such as, pins, land grid array structures or other types of interconnects. The molded chip combination 13 includes plural semiconductor chips, two of which are shown and labeled 19 and 20, respectively, and both of which are at least partially encapsulated in a molding material 25. In this arrangement, the molding material 25 can consist of two molding layers 30 and 35. As described in more detail below, the semiconductor chips 19 and 20 can be electronically connected by way of another semiconductor chip that is obscured by the molding material 25, and thus not visible in FIG. 1, but will be described below and shown in subsequent figures.

[0064] Additional details of the semiconductor chip device 10 can be understood by referring now also to FIG. 2, which is a sectional view of FIG. 1 taken at section 2-2. The molding material 25 of the molded chip combination 13 consists of the molding layer 30, the molding layer 35 and a polymer layer 50 sandwiched between the molding layers 30 and 35. The molding layer 35 surrounds the semiconductor chips 19 and 20 laterally but the respective upper surfaces 55 and 60 of the semiconductor chips 19 and 20 remain exposed to facilitate the subsequent optional placement of a heat spreader on the semiconductor chips 19 and 20. It is desirable for the materials selected for the molding layers 30 and 35 to exhibit suitable viscosity at the applicable molding temperatures and have molding temperatures lower than the melting points of any of the solder structures present at the time of the molding processes. In an exemplary arrangement the materials for the molding layers 30 and 35 can have a molding temperature of about 165°C. Two commercial variants are Sumitomo EME-G750 and G760.

[0065] The semiconductor chips 19 and 20 can be any of a variety of integrated circuits. A non-exhaustive list of examples includes microprocessors, graphics processing units, application processing units that combines aspects of both, memory devices, an application integrated specific circuit or other. The semiconductor chip 19 is constructed with a physical device or “PHY” region,

which has various internal and external conductor structures dedicated to the transmission of chip-to-chip signals, and a non-PHY region 70, which has conductor structures that are tailored more to the conveyance of power and ground and/or chip-to-circuit board signals. The semiconductor chip 20 similarly includes a PHY region 75 and a non-PHY region 80 that had the same functions as the PHY region 65 and the non-PHY region 70 of the semiconductor chip 19. As noted briefly above, the semiconductor chips 19 and 20 are connected electrically by way of another semiconductor chip, namely, an interconnect chip 85. The semiconductor chips 19 and 20 and the interconnect chip 85 can be constructed of silicon, germanium or other semiconductor materials and be bulk semiconductor, semiconductor on insulator or other designs. The interconnect chip 85 includes multitudes of internal conductor traces, which can be on multiple levels or single levels as desired. Two of the traces are shown and labeled collectively 90. The traces 90 interface electrically with conductor structures of the PHY regions 65 and 75 of the semiconductor chips 19 and 20 by way of conducting pathways 95, which are of such scale and size in FIG. 2 that cross-hatching is not practical and thus are depicted as multitudes of white stacks of three rectangles each. However, a subsequent figure will depict additional details of these conductive pathways 95. The non-PHY region 70 of the semiconductor chip 19 can interface electrically with the circuit board 15 by way of plural conductive pillars 100. Each conductive pillar 100 is connected electrically to the semiconductor chip 19 by way of a respective conductor pad 105 and to the circuit board 15 by way of a solder interconnect 110, which can be a solder bump or micro bump as desired. The non-PHY region 80 of the semiconductor chip 20 is similarly electrically connected to the circuit board 15 by way of plural conductive pillars 115, conductor pads 120 and solder bumps 125, which can be substantially like the conductive pillars 100, pads 105 and solder bumps 110 of the semiconductor chip 19. Note that the conductive pillars 100 traverse plural insulating layers, namely, starting from bottom to top, the molding layer 30, the polymer layer 50 and a passivation structure 130. The passivation structure 130 can be a laminate of various insulating materials such as, silicon dioxide, silicon nitride, or other dielectric materials. The conductive pillars 115 similarly traverse the molding layer 30, the polymer layer 50, and a passivation structure 135 of the semiconductor chip 20, which can be like the passivation structure 130 just described. The conductive pillars 100 and 115 can be composed of various conductor materials, such as copper and others to be described in more detail below. The conductive pads 105 and 120 can be composed of aluminum, copper or various other conductor materials. The solder bumps 110 and 125 can be composed of various well-known solder compositions, such as tin-silver, tin-silver-copper or others. The polymer layer 50 is preferably composed of polybenzoxazoles, although other polymeric materials could be used, such as benzocyclobutene, low temperature polyimide or other polymers with

a cure temperature below about 200°C. The polymer layer 50 is designed to act as a stress buffer, an isolation film and can enable redistribution layer routing.

[0066] The circuit board 15 can be organic or ceramic and single, or more commonly, multilayer. To cushion against the effects of mismatched coefficients of thermal expansion, an underfill material 140 can be positioned between the molding layer 30 and the upper surface of the circuit board 15 and can extend laterally beyond the left and right edges (and those edges not visible) of the molding layer 30 as desired. The underfill material 140 can be composed of well-known polymeric underfill materials.

[0067] Additional details of the conductive pathways 95 between the PHY regions 65 and 75 and the interconnect chip 85 can be understood by referring now also to FIG. 3, which depicts a portion of one of the conductive pathways 95 associated with the interconnect chip 85 and the PHY region 65 of the chip 19. It should be understood that this description will be illustrative of the other conductive pathways 95 as well. The portion of the conductive pathway 95 associated with the semiconductor chip 19 can include a conductor pad 145 that is connected to other conductor traces or vias in the semiconductor chip that are not visible and a conductive micro pillar 150 that is capped with a nickel-gold cap 155. The nickel-gold cap 155 functions as a barrier layer and solder wettable surface. Other possible materials include nickel-vanadium, platinum, palladium, pure gold or the like. An underbump metallization 160 is positioned between the conductive pillar 150 and the conductor pad 145. The conductor pad 145 can be constructed of aluminum, copper, gold, silver, combinations of these or the like. The UBM structure 160 can be composed of sputtered titanium, tungsten and copper and can also include nickel, vanadium or other materials. Note that the combination of the underbump metallization 160, the conductive micro pillar 150 and the nickel-gold cap 155 traverse the passivation structure 130 of the semiconductor chip 19 and the polymer layer 50. The portion of the conductive pathway 95 associated with the interconnect chip 85 can include a conductor pad 165 that, like the conductor pad 145, is connected electrically to one or more conductive traces or vias that are disposed in the interconnect chip 85, but which are not shown for simplicity of illustration. A passivation structure 166, composed of the same types of materials as the passivation structures 130 and 135 described elsewhere herein, partially covers the conductor pad 165. A barrier/adhesion layer 167 is formed on the conductor pad 165 and composed preferably of Ti-W and copper, followed by and proceeding upward in the figure, a copper layer 170, a nickel layer 175 and another copper layer 180. The copper layer 180 is capped with a solder micro bump 185. The skilled artisan will appreciate that the selection of conductor materials can be varied depending upon the constituents involved. For example, nickel, gold and nickel and gold or even vanadium can serve as barrier layers to prevent the migration of solder constituents into other conductive layers or vice versa. The solder

micro bump 185 can be composed of a variety of preferably lead-free solder, such as, tin-copper-silver, tin-silver or other types of solders. The nickel-gold cap 155 is designed to provide a good solder wettable layer for the solder micro bump 185 while also providing a barrier layer functionality. As noted above, the conductor pathway 95 depicted in FIG. 3 can be used for the other conductive pathways 95 depicted in FIG. 2 and described above.

[0068] An exemplary process to fabricate the semiconductor chip device 10 depicted in FIGS. 1 and 2 can be understood by referring now to FIGS. 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19 and 20 and initially to FIG. 4. FIG. 4 depicts the semiconductor chips 19 and 20 in section and as free standing semiconductor chips in the state that they would be in prior to assembly into the molded chip combo 13 depicted in FIGS. 1 and 2. Note that in FIG. 4, the semiconductor chips 19 and 20 are shown flipped over from the orientation depicted in FIGS. 1 and 2. The semiconductor chips 19 and 20 can be manufactured en masse in semiconductor wafers (not shown) which are subsequently singulated to yield the individual semiconductor chips 19 and 20. During these fabrication processes, the various electronic structures that include transistors, capacitors, inductors and whatever other logic elements and circuit structures that are appropriate for the chips 19 and 20 can be constructed and the aforementioned PHY regions 65 and 75 and non-PHY regions 70 and 80 can be established in the chips 19 and 20, respectively. In this regard, the semiconductor chip 19 can be manufactured up to the point where the conductor pads 105 and 145 have been fabricated along with the passivation structure 130 and plural openings 190 in the passivation structure 130 that expose the underlying conductor pads 105 and plural openings 195 through the passivation structure 130 that lead to the conductor pads 145. The semiconductor chip 20 can be similarly manufactured up to the point where the conductor pads 120 in the non-PHY region 80 have been fabricated and the conductor pads 145 in the PHY region 75 have been established as well as openings 200 in the passivation structure 135 and plural openings 205 also in the passivation structure 135 that lead to the conductor pads 145. The conductor pads 105, 120 and 145 can be fabricated using well-known material deposition techniques, such as, plating, sputtering, chemical vapor deposition, combinations of these or the like. The openings 190, 195, 200 and 205 can be formed using well-known photolithography and directional etching techniques.

[0069] Next and as shown in FIG. 5, the semiconductor chips 19 and 20 can be flipped over from the orientation shown in FIG. 4 and mounted to a carrier substrate 210. The semiconductor chips 19 and 20 can be secured to the carrier substrate 210 by way of a light-activated adhesive (not shown) or other temporary fastening technique since it is intended that the carrier wafer 210 be subsequently removed following various processing steps.

[0070] Next and as depicted in FIG. 6, the molding layer 35 is formed by compression molding of a suitable compound, such as, Sumitomo EME-G750 or G760 at about 165 °C for about 60 to 120 minutes. This compression molding process will initially encapsulate the semiconductor chips 19 and 20 and cover the otherwise uncovered portions of the carrier substrate 210. Because it is desirable to expose the upper surfaces 55 and 60 of the semiconductor chips 19 and 20, respectively, the molding layer 35 can undergo a grinding process as depicted in FIG. 7 to expose those surfaces 55 and 60. At this point, the semiconductor chips 19 and 20 remain mounted on the carrier substrate 210 but mechanically joined laterally by way of the molding layer 35.

[0071] Next, and as shown in FIG. 8, the semiconductor chips 19 and 20 and molding layer 35 can be separated from the carrier substrate 210 depicted in FIG. 7 and flipped over from the orientation depicted in FIG. 7. At this point, the polymer layer 50 can be applied over both the semiconductor chips 19 and 20 and the molding layer 35. The polymer layer 50 can be applied using well-known spin coating and baking techniques, and since a blanket deposition process can be used, the various openings 190, 195, 200 and 205 can fill with the polymer layer 50 material at this point. As shown in FIG. 9, in order to re-expose the various conductor pads 105 and 145 of the semiconductor chip 19 and the conductor pads 120 and 145 of the semiconductor chip 20, the polymer layer 50 can be suitably masked and lithographically patterned, that is, by way of photolithography, in order to establish openings 215 to the conductor pads 105, openings 220 to the conductor pads 145 and the semiconductor chip 19 and openings 220 and 225 to the conductor pads 145 and 120 of the semiconductor chip 20, respectively.

[0072] Next and as shown in FIG. 10, a resist mask 235 is applied over the polymer layer 50 and suitably patterned to establish openings 240 that lead to the conductor pads 145 of the semiconductor chip 19 and openings 245 that lead to the conductor pads 145 of the semiconductor chip 20. Here, the purpose of the resist mask 235 is to mask the conductor pads 105 and 120 of the semiconductor chips 19 and 20, respectively, so that the various conductor structures associated with the conductor pads 145 of each of the chips 19 and 20 can be fabricated. Additional details of this fabrication step can be understood by referring now also to FIG. 11, which is the portion of FIG. 10 circumscribed by the dashed rectangle 250, shown at greater magnification. Note that box 250 circumscribes a portion of the PHY region 65 of the semiconductor chip 19 and thus one of the conductor pads 105 and one of the conductor pads 145. It should be understood that the structures illustrated in FIG. 11 are illustrative of the other similar conductor structures of the semiconductor chip 19 and those conductor structures in the PHY region 75 of the chip 20. It should also be understood that, as shown in FIG. 11, prior to the application of the resist mask 235, the UBM 160 (also depicted in FIG. 3) can be deposited using well-known sputter and/or CVD techniques. This sputter process can blanket deposit

the UBM 160 as shown. Thereafter, the resist mask 235 can be applied by spin coating and baking using well-known techniques. The openings 240, one of which is illustrated in FIG. 11, can be photolithographically patterned in the resist mask 235 and thereafter, the micro pillar 150 can be fabricated using the techniques described above in conjunction with FIG. 3 as well as the nickel-gold cap 155. Application of multiple conductor materials 252 is by way of the openings 240 and the similar openings 245. As noted above, the micro pillar 150 traverses the passivation structure 130 of the semiconductor chip 19 and a portion of the polymer layer 50. Note that the conductor pads 145 and 105 in this illustrated arrangement are fabricated with respective lateral dimensions (diameters or possibly other shapes) x_1 and x_2 where $x_2 > x_1$. However, in another arrangement described below, the semiconductor chip 19 is manufactured with x_1 and x_2 being approximately the same size. This circumstance presents a technical issue that is addressed by a another disclosed technique.

[0073] Next and as shown in FIG. 12, the resist mask 235 shown in FIG. 11 is stripped using well-known ashing and solvent stripping techniques and another resist mask 260 is applied using well-known spin coating and baking techniques and patterned so as to cover the conductor pads 145 and micro pillars 150 of each of the semiconductor chips 19 and 20 but with openings 265 that lead to the underlying conductor pads 105 of the semiconductor 19 and openings 270 that lead to the underlying conductor pads 120 of the semiconductor chip 20.

[0074] Next and as shown in FIG. 13, a plurality of material deposition steps are performed to deposit conductor materials schematically represented by the droplets 275 to fabricate conductive pillars 100 and 115 of the semiconductor chips 19 and 20, respectively. Additional details of these material fabrication processes can be understood by referring now also to FIG. 14, which is the portion of FIG. 13 circumscribed by the dashed rectangle 280 shown at greater magnification. As shown in FIG. 14, prior to the application of the resist mask 260 and the patterning of the openings 270 therein, the aforementioned UBM structure 160 deposited prior to the resist mask 235 depicted in FIG. 10 is still in position. Here, the conductive pillars 115 can be fabricated using well-known plating techniques that can consist of a biased plating process using the UBM structure 160 as a plating electrode. Copper, copper and silver, copper and tin or other types of materials can be used. Following the plating of the conductive pillar 115, a solder cap 285 is fabricated on the pillar 115 by plating, or alternatively by a stencil and paste process. Note how the UBM structure 160 is positioned on and in ohmic contact with the conductor pad 120 and the combination of the UBM structure 160 and the lower reaches of the conductive pillar 115 extend vertically through the passivation structure 135 and a portion of the polymer layer 50 on the semiconductor chip 20.

[0075] The mounting of the interconnect chip 85 to the semiconductor chips 19 and 20 will now be described in conjunction with FIGS. 15 and 16. As shown in FIG. 15, the resist mask 260 depicted in

FIGS. 13 and 14 is stripped using well-known ashing and solvent stripping techniques to leave the conductive pillars 100 and 115 projecting up from the semiconductor chips 19 and 20, respectively. Prior to mounting the interconnect chip 85, the combination of the semiconductor chips 19 and 20 and the molding layer 35 can undergo a material removal process such as a wet etch, to remove excess portions of the UBM structure 150 that are positioned on the polymer layer 50 but lateral to the pillars 100 and 115. This etch is necessary to prevent the subsequent electrical shorting between adjacent pillars 100 and 115, etc. Up to this point, the interconnect chip 85 is fabricated using various well-known techniques to establish not only the internal conductive traces 90 but also that portion of the conductive pathways 95 associated with the interconnect chip 85 and as depicted in FIG. 3. For example, FIG. 16 depicts the portion of FIG. 15 and in particular the small portion of the interconnect chip 85 circumscribed by the dashed square 290 at greater magnification. As described above, that portion of the conductive pathway 95 shown in FIG. 3 associated with the interconnect chip 85 consists of the conductor pad 165, the passivation structure 166, the seed layer 167, and the various layers 170, 175 and 180 followed by the solder cap 185, all which are depicted flipped over from the orientation reflected in FIG. 3. It should be noted that when the interconnect chip 85 is positioned on the polymer layer 50, a reflow is performed in order to establish metallurgical bonds between the solder caps 185 and the underlying nickel-gold caps 155 positioned on the micro pillars 150 of the semiconductor chips 19 and 20.

[0076] Next and as shown in FIG. 17, a second molding process is performed to form the molding layer 30 over the interconnect chip 85, the conductive pillars 100 and 115 and the otherwise exposed portions of the polymer layer 50. The molding layer 30 is fabricated using a compression molding process at about 165 °C for about 60 to 120 minutes and Sumitomo EME-G750 or G760 or the other molding materials disclosed herein. It is necessary to expose the conductive pillars 100 and 115 so the molding layer 30 undergoes a grinding process as shown in FIG. 18. This grinding process is designed to expose the conductive pillars 100 and 115 and, depending upon the height of the interconnect chip 85, can also thin the backside of the interconnect chip 85 as well. With the pillars 100 and 115 exposed as shown in FIG. 19, the solder interconnects 110 are fabricated on the pillars 100, the solder interconnects 125 are fabricated on the pillars 115. The solder interconnects 110 and 125 can be formed by pick and place placement of solder bumps, by well-known solder plating and/or paste stencil processes or other techniques.

[0077] Next and as shown in FIG. 20, the now completed molded chip combination 13 can be flipped over from the orientation shown in FIG. 19 and mounted to the circuit board 15 by way of a reflow process of the solder interconnects 110 and 125. Thereafter, the underfill 140 is established by dispensing underfill as a liquid and capillary action.

[0078] For thermal management purposes, an optional heat spreader or sink 300 can be mounted on the molded chip combination 13 and placed in thermal contact with the semiconductor chips 19 and 20, respectively as shown in FIG. 21. A suitable thermal interface material, such as a thermal grease or paste (not shown), can be positioned between the heat spreader 300 and the upper surfaces 55 and 60 of the semiconductor chips 19 and 20, respectively.

[0079] FIG. 22 is a sectional view like FIG. 2, but of an alternate exemplary semiconductor chip device 10'. The semiconductor chip device 10' shares most attributes with the semiconductor chip device 10 depicted and described elsewhere herein. The chief difference is that, whereas the semiconductor chip device 10 utilizes the underfill material layer 140 as shown in FIG. 2, the semiconductor chip device 10' eliminates the underfill material layer 140 in favor of increasing the overall height of the molding layer 30 of an alternative molded chip combination 13'. The molding layer 35 and the polymer layer 50 are used as in the earlier described arrangement. However, as shown in FIG. 22, the molding layer 30, rather than terminating near or at the lower ends of the conductive pillars 110 and 115, instead extends down and molds to the circuit board 15 and also extends upwards to at least partially encapsulate the combination of the chips 19 and 20, the molding material 35 and the polymer layer 50. The fabrication steps described elsewhere herein to mold the semiconductor chips 19 and 20 with the molding layer 35 and the construction of the various conductor structures in and around the PHY region 65 and the non-PHY region 70 of the semiconductor chip 19 are used here as well. The PHY region 75 and the non-PHY region 80 of the semiconductor chip 20 will be repeated or be the same as described elsewhere herein for the semiconductor chip device 10. Similarly, the interconnect chip 85 will be constructed as generally described elsewhere herein for the semiconductor chip device 10. However, there are some process flow differences between fabrication processes used for the semiconductor chip device 10 and the semiconductor chip device 10', which will now be described initially in conjunction with FIG. 23. FIG. 23 depicts the molded combination of the semiconductor chips 19 and 20 and the molding layer 35, after fabrication of the polymer layer 50 and mounting of the interconnect chip 85. In addition, the conductive pillars 100 and 115 have been fabricated and exposed using the techniques described above leading to the depiction in FIG. 15. However, at this stage, the solder interconnects 110 and 125 are mounted on the conductive pillars 100 and 115, respectively. This can be accomplished using a drop process, which is essentially a pick and place process. It can also be possible to position a stencil (not shown) in order to place the solder interconnects 110 and 125. A brief reflow can be accomplished at this point in order to establish an initial metallurgical bonding between the solder interconnects 110 and the conductive pillars 100 and the solder interconnects 125 and the conductive pillars 115. Next and as shown in FIG. 24, the semiconductor chips 19 and 20 and the molding layer

35 along with the interconnect chip 85 can be flipped over from the orientation shown in FIG. 23 and mounted to the circuit board 15. This entails a reflow process to establish metallurgical connections between the solder interconnects 110 and 125 and conductive pads (not shown) of the circuit board 15. Next, molding material 30 can be molded between the polymer layer 50 and the circuit board 15 using transfer molding or other techniques to establish the molding layer 30 shown in completed form in FIG. 22. This establishes the completed molded chip combination 13'. As shown in FIG. 25, the optional heat spreader 300 can be mounted on the molded chip combination 13' as described above. Note that the molding process for the molding layer 30 could alternatively make the lateral edges of the molding layer 30 co-terminus with the lateral edges of the molding layer 35 and the polymer layer 50 if desired. Again, a thermal interface material (not shown) can be positioned between the heat sink 300 and the semiconductor chips 19 and 20.

[0080] In the foregoing disclosed arrangements, the conductor pads in the PHY regions 65 and 75 of the semiconductor chips 19 and 20 are more numerous and have some smaller dimension x_1 than the conductor pads of the non-PHY regions 70 and 80 with lateral dimensions x_2 . However, the semiconductor chips 19 and 20 can be manufactured with a single lateral dimension x_1 for all of the conductor pads, that is, for both the PHY regions 65 and 75 and the non-PHY regions 70 and 80. However, this represents a technical complexity in that it is desirable to be able to use larger conductive pillars, such as the pillars 100 and 115, even if the non-PHY regions of a device 70 and 80 have the smaller lateral dimension x_1 size pads. A technical solution to this issue will be illustrated and described in conjunction with FIGS. 26, 27, 28, 29, 30, 31, 32, 33, 34 and 35 and initially with reference to FIG. 26. FIG. 26 is a sectional view of the semiconductor chip 20 and a portion of the PHY region 75 and a portion of the non-PHY region 80 thereof. Here, the PHY regions 75 includes plural conductor pads 120 with some lateral dimension x_1 that have been fabricated as described generally elsewhere herein. However, the non-PHY region 80, in lieu of the larger conductor pads 120 with the lateral dimension x_2 depicted elsewhere herein, has instead an additional plurality of conductor pads 145 with the lateral dimension x_1 . This can occur where the semiconductor chip 20 is manufactured using the process that does not require constructing and patterning top level conductor pads with two separate lateral dimensions. The passivation structure 135 has been applied and patterned with plural openings 225 to all of the conductor pads 145 both in the PHY region 75 and the non-PHY region 80. FIG. 27 shows an overhead view of the passivation structure 135, the openings 225 as well as some of the underlying conductor pads 145. It should be understood that just a few of the conductor pads 145 are depicted and that the semiconductor chip can include hundreds or thousands of such pads depending on its complexity. The dashed line 308 in FIG. 27 and elsewhere in the figures represents the border between the PHY region 75 and the non-PHY region 80. The two

dashed circles 310 represent the locations where the later-formed conductive pillars 115 destined to be in ohmic contact with the underlying conductor pads 145 will be formed. Note that smaller micro pillars 150 will be formed in ohmic contact with the conductor pads 145 in the PHY region 75. A technical goal is to be able to ultimately fabricate the large-size conductive pillars 115 at the locations of the dashed circles 310 in ohmic contact with the underlying undersized conductor pads 145.

Initially and as shown in FIG. 28, the polymer layer 50 is applied to the passivation structure 135 of the semiconductor chip 20 over the PHY region 75 and the non-PHY region 80 and filling the openings 225. The polymer layer 50 preferably includes a photoactive compound. As shown in FIG. 29, a resist mask 320 is applied to the polymer layer 50 and patterned with suitable openings 322 that are in alignment with those openings 225 in the passivation structure 135 over the PHY region 75 and other suitable openings 323 that are in alignment with those openings 225 over the non-PHY region 80 in the passivation structure 135. The openings 322 and 323 are shown in plan and pictorial views in FIGS. 30 and 31, respectively. Note that the openings 322 and the openings 323 have different footprints. The openings 322 have footprints that track the underlying openings 225 in the PHY region 75. However, the openings 323 consist of a combination of criss-crossing connecting portions 340 and openings 345 where the openings 345 are aligned with the underlying 225 in the non-PHY region 80. With the mask 320 in place and patterned, the polymer layer 50 is exposed and developed, and the mask 320 stripped as shown in the plan view in FIG. 32 to yield openings 347 in the PHY region 75 and with the footprint of the mask openings 322 (see FIG. 31), and openings 349 of criss-crossing connecting portions 350 and openings 352 in the non-PHY region 80 with the footprint of the mask openings 323 (see FIG. 31). The underlying conductor pads 145 in both the PHY region 75 and the non-PHY region 80 are now exposed.

[0081] Next and as shown in the exploded pictorial view depicted in FIG. 33, another resist mask 330 is applied to the polymer layer 50 and patterned to provide appropriate openings 354 over the PHY region 75 that are in alignment with the openings 347 in the polymer layer 50 and another set of openings 356 over the non-PHY region 80 that are in alignment with the openings 349 in the passivation structure 135. The openings 354 have the same footprint as the openings 347 in the polymer layer 50 and the openings 356 have the same footprint as the openings 349 in the polymer layer 50. With the mask 330 in place, discrete conductive pillars 150 are fabricated in the openings 347 and interconnected conductive pillars 150' are fabricated in the openings 349 using plating and the materials described elsewhere herein. The conductive pillars 150 and the conductive pillars 150' will have the same metallurgical composition, but different footprints. The conductive pillars 150' consist of pillars 358 that extend down through the polymer layer 50 to the underlying conductor pads 145 (not visible) interconnected by conductor bars 359. It should be understood that, through

subsequent processing, larger diameter conductive pillars 370 (in dashed) will be fabricated on top of the conductive pillars 150' in the non-PHY region 80. The plating mask 330 is ultimately stripped using the techniques described elsewhere herein to leave the conductive pillars 150 and conductive pillars 150'. Like the conductor bars 359, conductor traces (not shown) could also be fabricated in this way such that the polymer layer 50 enables fabrication of redistribution layer traces. The basic construction of the conductive pillars 150 in the PHY region 75 is the same general construction depicted in FIG. 11 for the conductive pillars 150. While the conductive pillars 150' will also have the same layers, the footprint thereof will differ from the conductive pillars 150 as shown in FIG. 33.

[0082] Next and as shown in FIG. 34, a plating mask 360 is fabricated over the polymer layer 50 and patterned with suitable openings 365 which are positioned and sized to correspond to the size and locations of the dashed circles 310 depicted in FIG. 27. The objective is to enable a subsequent plating process to establish the conductive pillars 370 that are in ohmic contact with the underlying interconnected conductive pillars 150' that consist of the interconnected pillars 358 and bars 359 shown in FIG. 33. FIG. 35 shows an overhead view of the plating mask 360 and the plated conductive pillars 370 over the non-PHY region 80. Note that the underlying discrete conductive pillars 150 are obscured (and thus shown in dashed) by the plating mask 460 and the interconnected conductive pillars 150 are obscured by both the conductive pillars 370 and a portion of the plating mask 360 and the conductive pillars 150 are similarly obscured and thus shown in dashed. The plating mask 360 is ultimately stripped using well-known techniques.

[0083] The skilled artisan will appreciate that the molded chip combos 13 described herein can be fabricated as single units or en masse in a wafer-like structure (a reconstituted wafer) 380 in what amounts to a wafer level process. For example, and as shown in FIG. 36, which is a pictorial view, the plural molded chip combinations 13 can be molded together using, for example, the molding layers 35 and 30 in large numbers at the same time and if desired, interconnect chips 85 can be mounted on the molded chip combinations 13 at this wafer level stage. Thereafter, the molded chip combinations 13 can be singulated into the individual units depicted in the other figures herein.

[0084] While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and have been described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling within the spirit and scope of the invention as defined by the following appended claims.

CLAIMS

What is claimed is:

1. A molded chip combination, comprising:
a first semiconductor chip (20) having a first PHY region (75);
5 a second semiconductor chip (19) having a second PHY region (65);
an interconnect chip (85) interconnecting the first PHY region to the second PHY region;
a first molding layer (35) laterally joining together the first semiconductor chip and the
second semiconductor chip;
a second molding layer (30) at least partially encapsulating the interconnect chip; and
10 a polymer layer (50) positioned between the first molding layer and the second molding layer.

2. The molded chip combination of claim 1, wherein the first semiconductor chip includes a first
plurality of interconnects (125) to connect to a circuit board (15) when the molded chip
combination is mounted on the circuit board and the second semiconductor chip includes a
15 second plurality of interconnects (110) to connect to the circuit board when the molded chip
combination is mounted on the circuit board.

3. The molded chip combination of claim 2, wherein the first semiconductor chip includes a first
non-PHY region (80) connected to the first interconnects and the second semiconductor chip
20 includes a second non-PHY region (70) connected to the second interconnects.

4. The molded chip combination of claim 1, wherein the first semiconductor chip includes a first
non-PHY region (80), the first semiconductor chip PHY region (75) having a first group of
conductor pads (145) each having a first lateral dimension (X_1) and the first semiconductor
25 chip non-PHY region has a second group of conductor pads (145) each having substantially
the same first lateral dimension, the polymer layer (50) having a plurality of openings (347)
aligned with the first group of conductor pads and a plurality of interconnected openings
(349) aligned with the second group of conductor pads, the polymer layer having a
conductive pillar (150) in each of the openings and interconnected conductive pillars (150') in
30 each of the interconnected openings.

5. The molded chip combination of claim 4, comprising another conductive pillar (370) on the
interconnected conductive pillars, the another conductive pillar having a second lateral
dimension larger than the first lateral dimension.

6. The molded chip combination of claim 1, comprising a circuit board and the molded chip combination mounted on the circuit board.
- 5 7. The molded chip combination of claim 1, wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.
8. A molded chip combination, comprising:
 - 10 a first semiconductor chip (20) having a first PHY region (75) and a first non-PHY region (80);
 - a second semiconductor chip (19) having a second PHY region (65) and a second non-PHY region (70);
 - an interconnect chip (85) interconnecting the first PHY region to the second PHY region;
 - a first molding layer (35) laterally joining together the first semiconductor chip and the
 - 15 second semiconductor chip;
 - a second molding layer (30) joined to the first molding layer and at least partially encapsulating the interconnect chip and the first molding layer; and
 - a polymer layer (50) positioned between the first molding layer and the second molding layer.
- 20 9. The molded chip combination of claim 8, wherein the first semiconductor chip includes a first plurality of interconnects (125) to connect to a circuit board (15) when the molded chip combination is mounted on the circuit board and the second semiconductor chip includes a second plurality of interconnects (110) to connect to the circuit board when the molded chip combination is mounted on the circuit board.
- 25 10. The molded chip combination of claim 9, wherein the first semiconductor chip first non-PHY region (80) is connected to the first interconnects and the second semiconductor chip second non-PHY region (70) is connected to the second interconnects.
- 30 11. The molded chip combination of claim 8, wherein the first semiconductor chip PHY region (75) includes a first group of conductor pads (145) each having a first lateral dimension (X_1) and the first semiconductor chip non-PHY region (80) includes a second group of conductor pads (145) each having substantially the same first lateral dimension, the polymer layer (50) having a plurality of openings (347) aligned with the first group of conductor pads and a

plurality of interconnected openings (349) aligned with the second group of conductor pads, the polymer layer having a conductive pillar (150) in each of the openings and interconnected conductive pillars (150') in each of the interconnected openings, the first semiconductor chip non-PHY region including another conductive pillar (370) on the interconnected conductive pillars, the another conductive pillar having second lateral dimension larger than the first lateral dimension.

12. The molded chip combination of claim 8, comprising a circuit board and the molded chip combination mounted on the circuit board.

13. The molded chip combination of claim 8, wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.

14. A method of manufacturing a molded chip combination, comprising:
interconnecting a first PHY region (75) of a first semiconductor chip (20) to a second PHY region (65) of a second semiconductor chip (19) with an interconnect chip (85); and molding together the first semiconductor chip and the second semiconductor chip with a first molding layer (35);
at least partially encapsulating the interconnect chip with a second molding layer (30); and applying a polymer layer (50) between the first molding layer and the second molding layer.

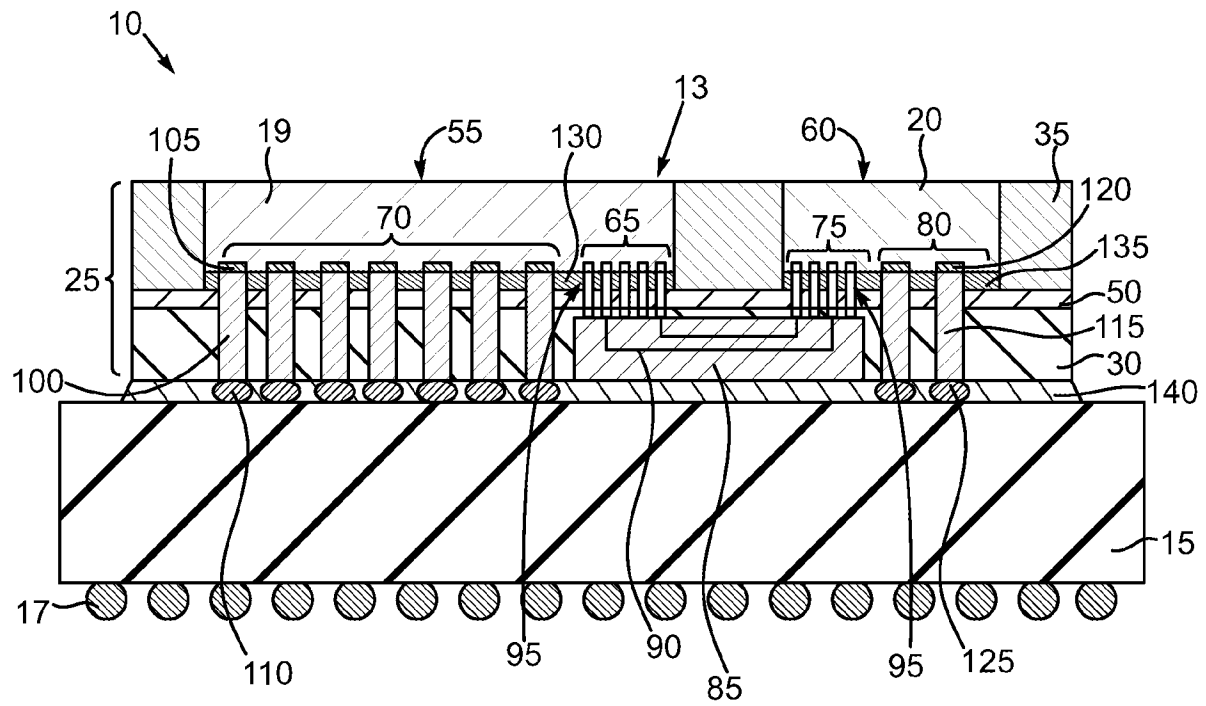
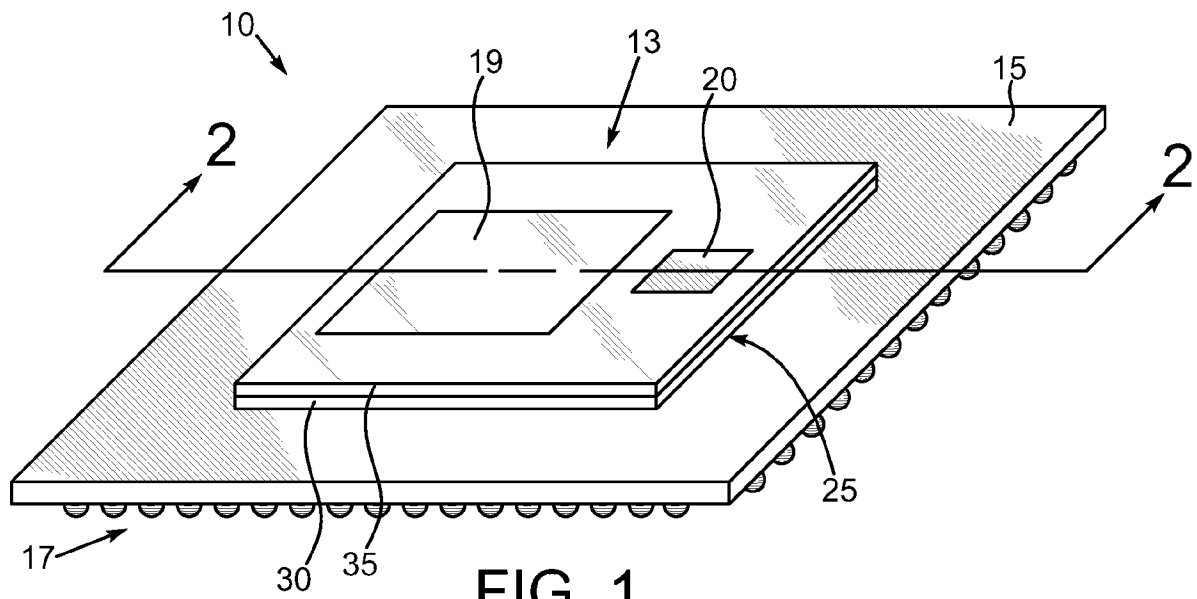
15. The method of claim 14, comprising fabricating a first plurality of interconnects (125) on the first semiconductor chip to connect to a circuit board (15) when the molded chip combination is mounted on the circuit board and a second plurality of interconnects (110) on the second semiconductor chip to connect to the circuit board when the molded chip combination is mounted on the circuit board.

16. The method of claim 15, wherein the first semiconductor chip includes a first non-PHY region connected (80) to the first interconnects and the second semiconductor chip includes a second non-PHY region (70) connected to the second interconnects.

17. The method of claim 14, wherein the first semiconductor chip includes a first non-PHY region (80), the method comprises fabricating a first group of conductor pads (145) of the first semiconductor chip PHY region each having a first lateral dimension (X_1) and a second group

- 5 of conductor pads (145) of the first semiconductor chip non-PHY region each having substantially the same first lateral dimension, providing the polymer layer (50) with a plurality of openings (347) aligned with the first group of conductor pads and a plurality of interconnected openings (349) aligned with the second group of conductor pads, and
10 fabricating a conductive pillar (150) in each of the openings and interconnected conductive pillars (150') in each of the interconnected openings.
18. The method of claim 17, comprising positioning another conductive pillar (370) on the interconnected conductive pillars, the another conductive pillar having second lateral
10 dimension larger than the first lateral dimension.
19. The method of claim 14, comprising mounting the molded chip combination on a circuit board.
- 15 20. The method of claim 14, wherein the first semiconductor chip comprises a processor and the second semiconductor chip comprises a memory chip.

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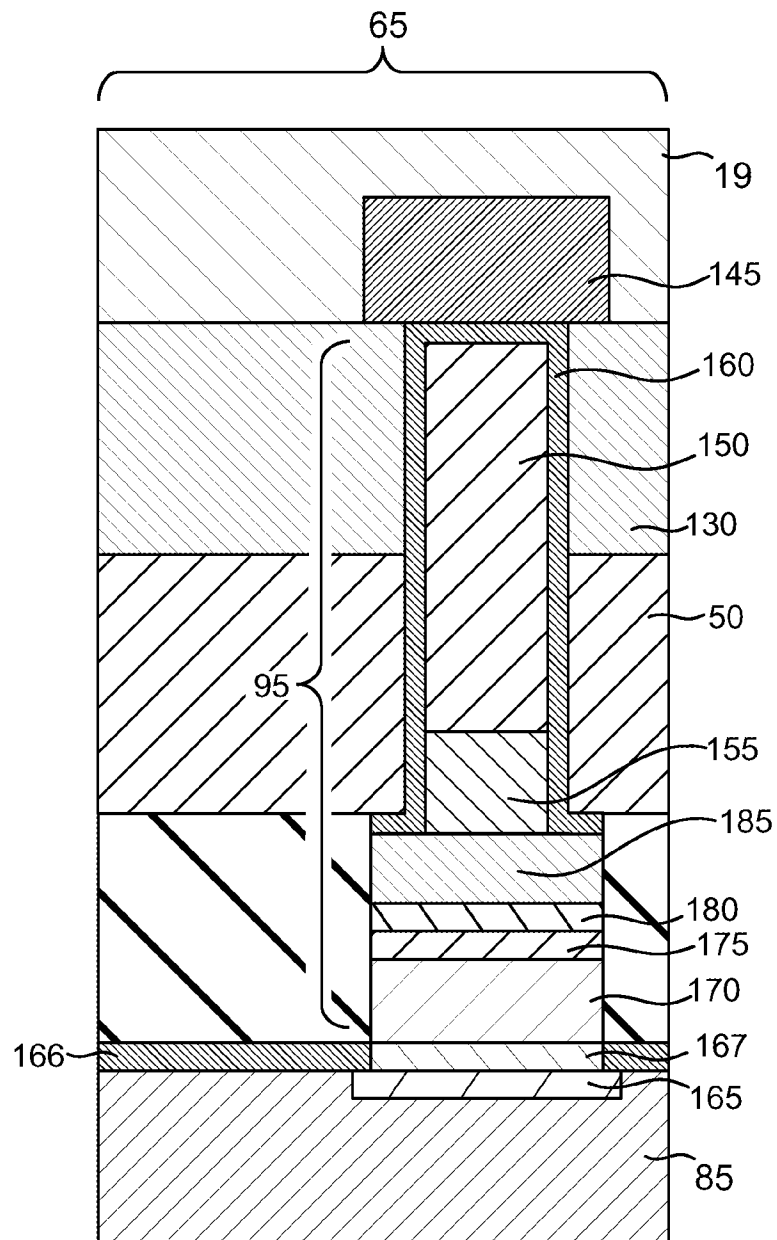


FIG. 3

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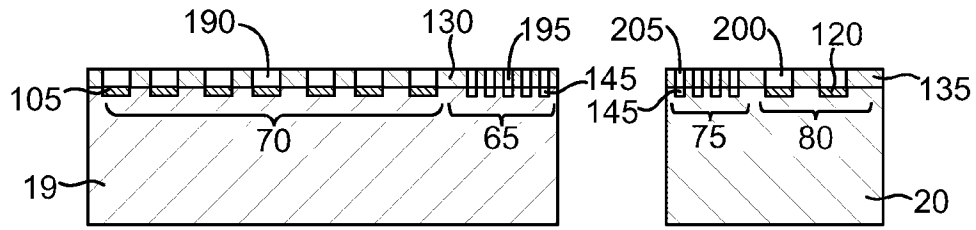


FIG. 4

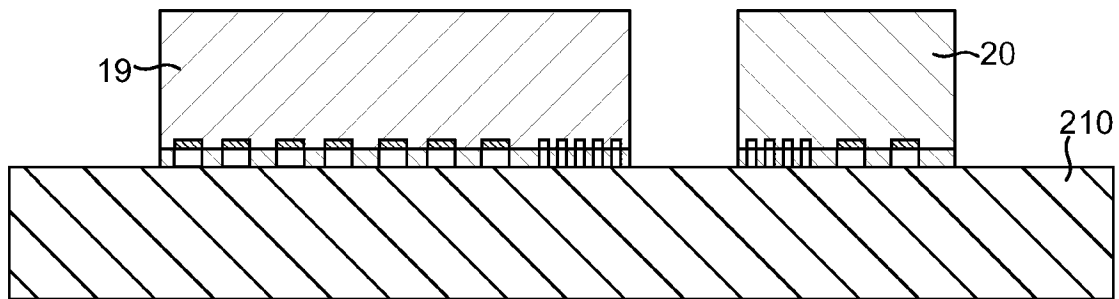


FIG. 5

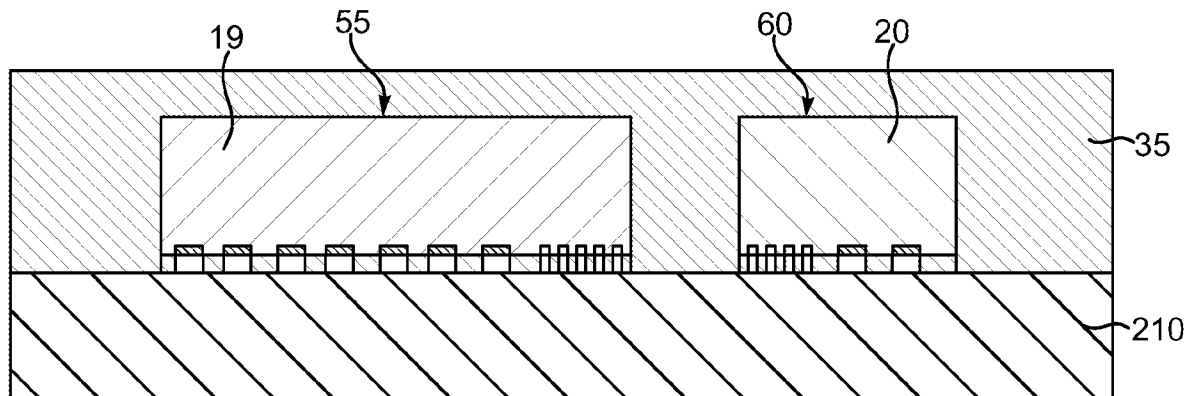


FIG. 6

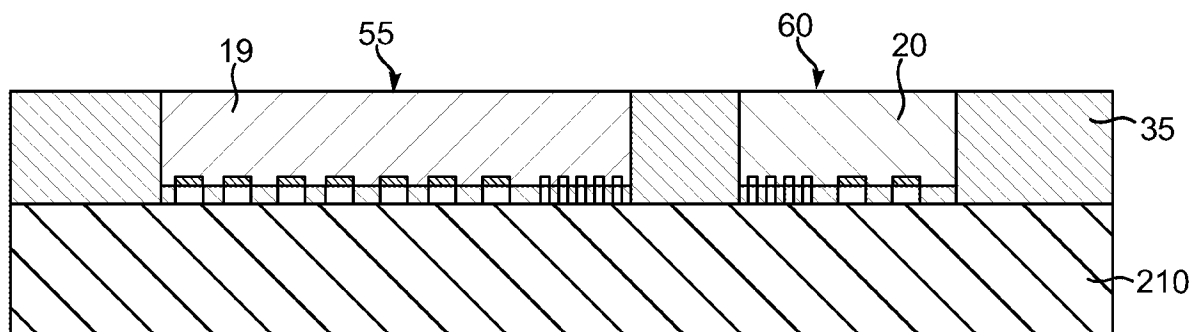


FIG. 7

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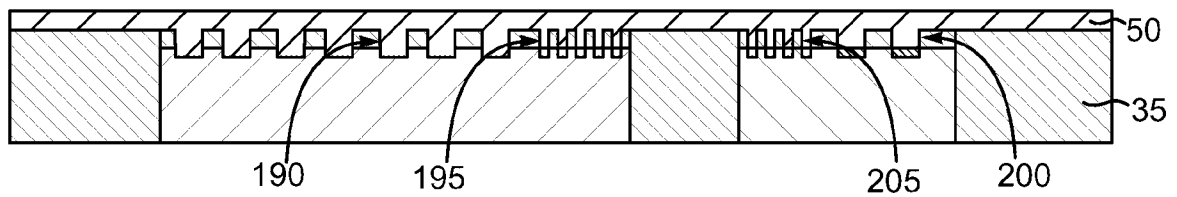


FIG. 8

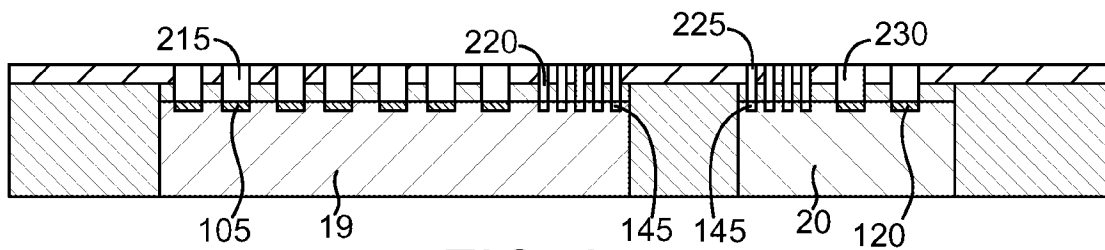


FIG. 9

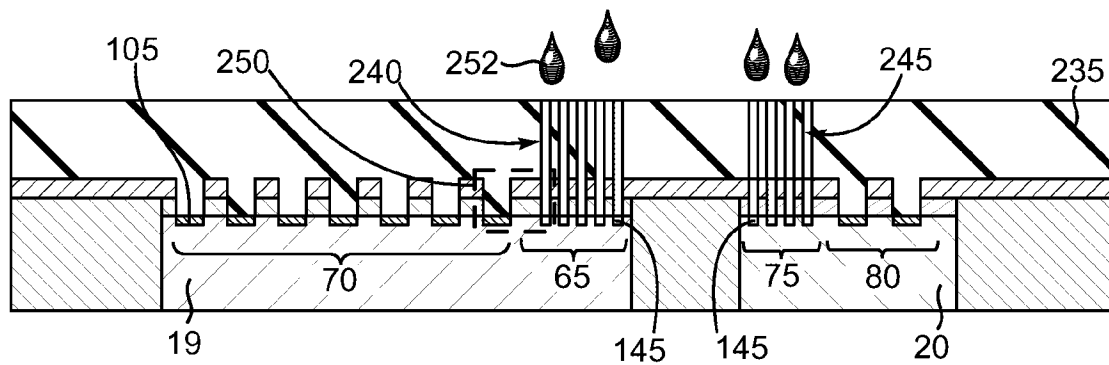


FIG. 10

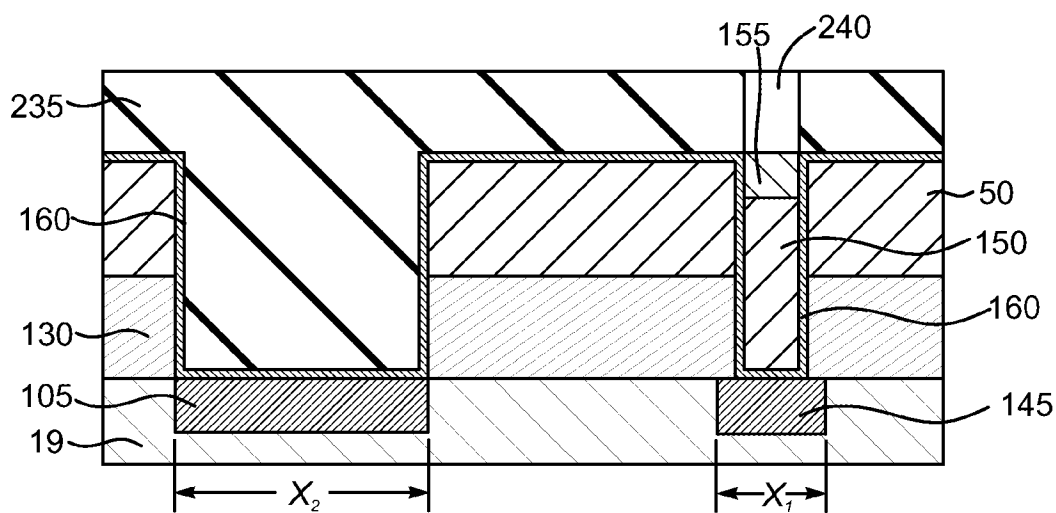


FIG. 11

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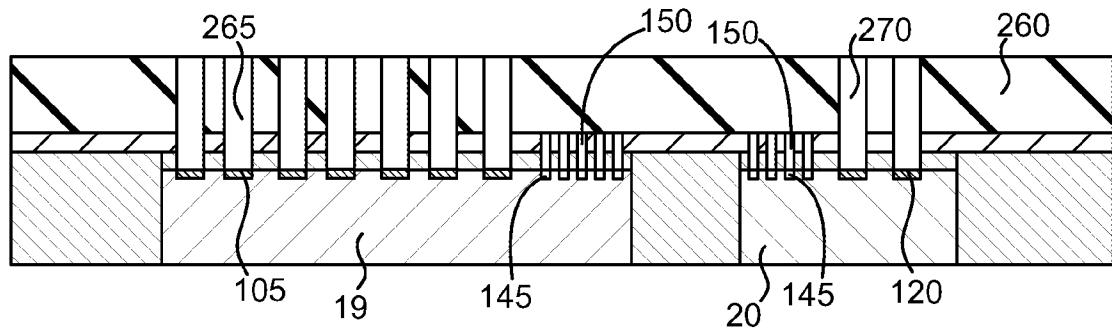


FIG. 12

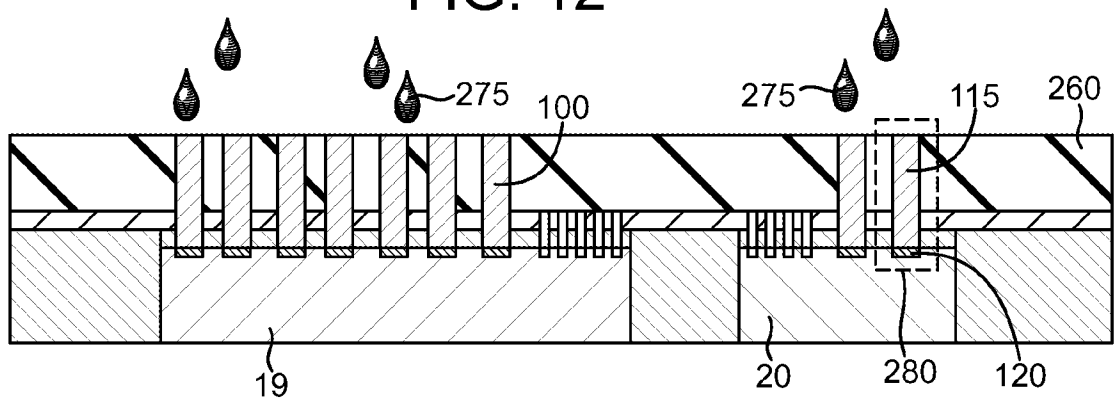


FIG. 13

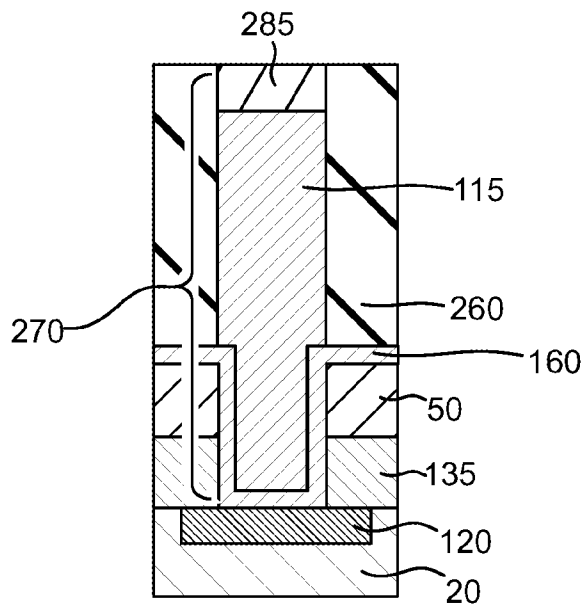


FIG. 14

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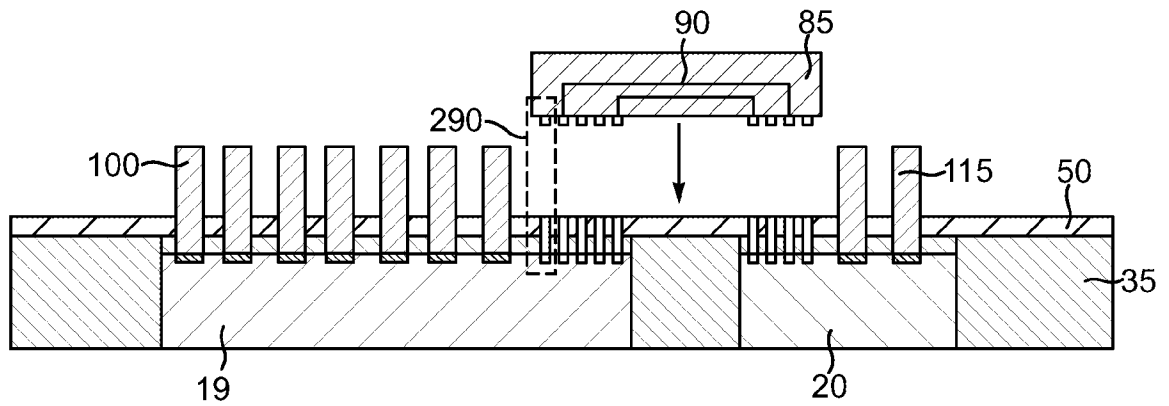


FIG. 15

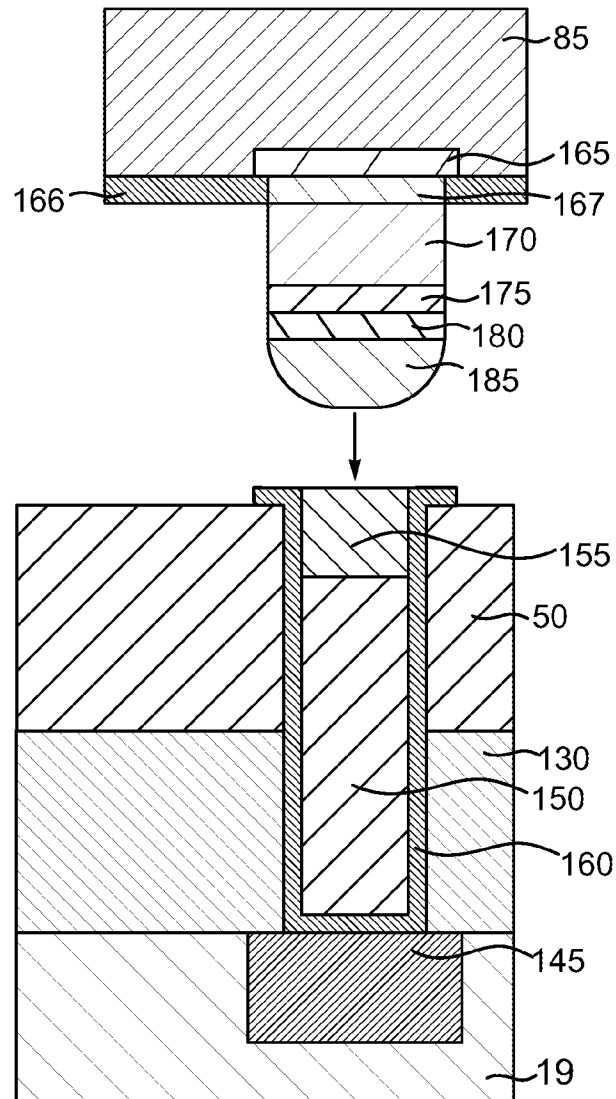


FIG. 16

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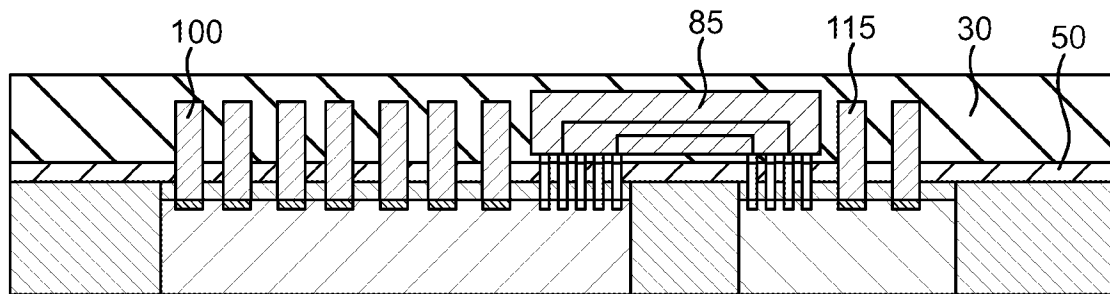


FIG. 17

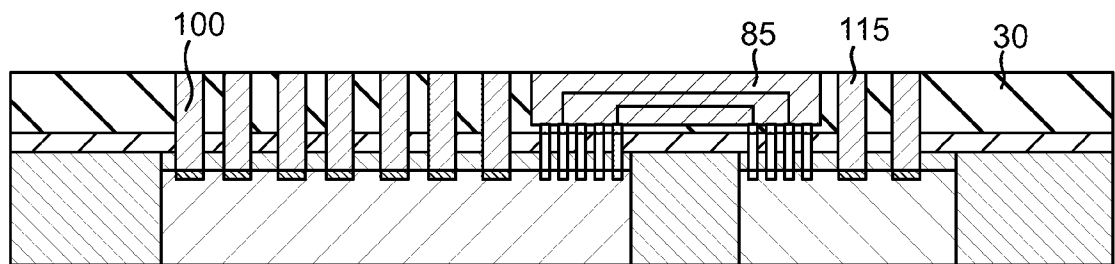


FIG. 18

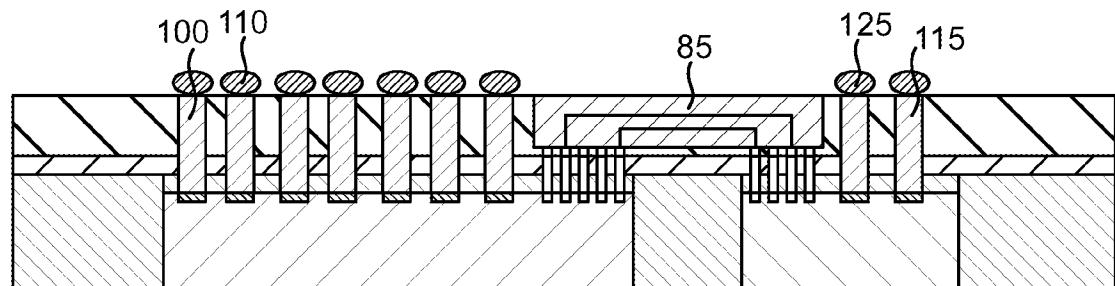


FIG. 19

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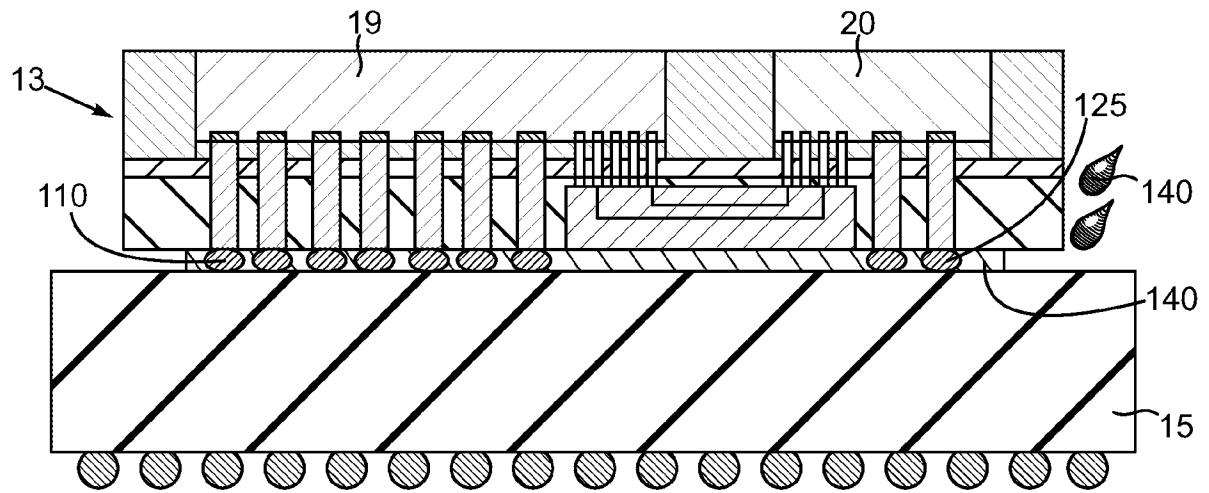


FIG. 20

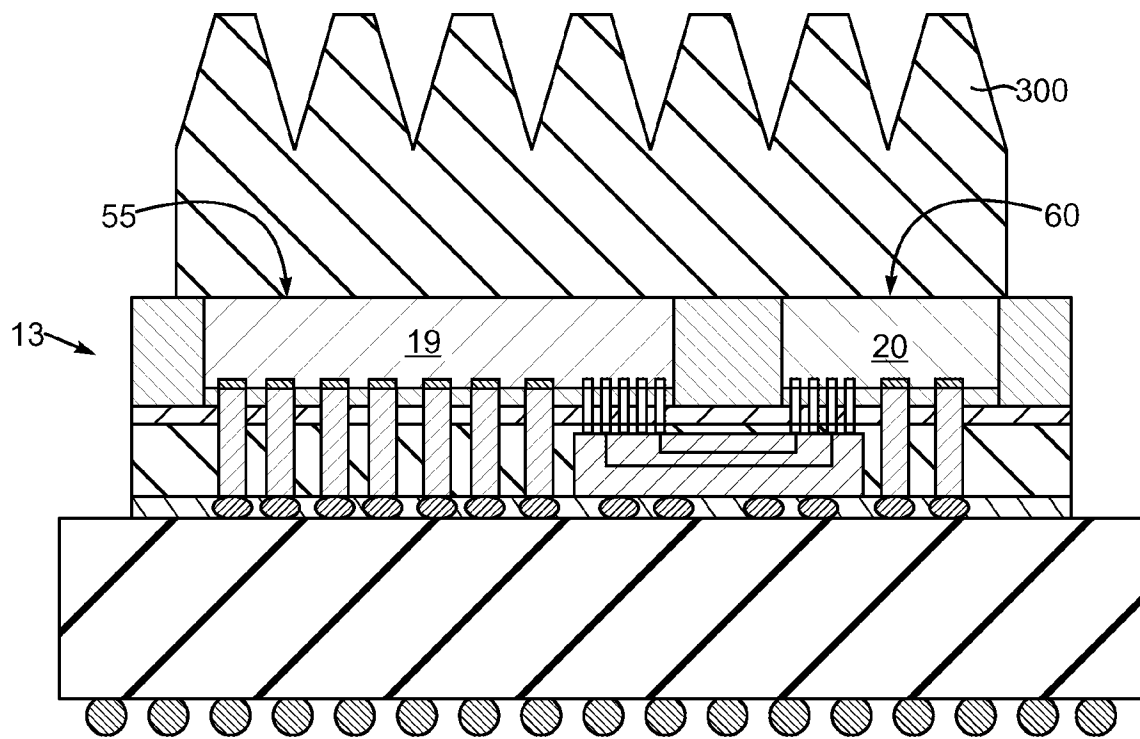


FIG. 21

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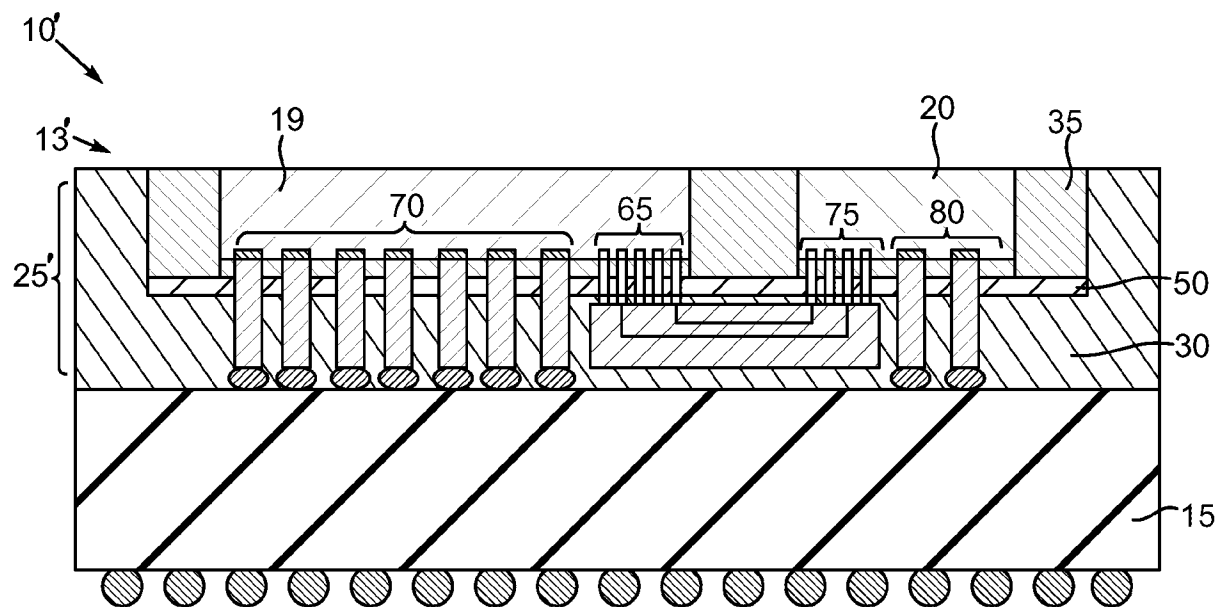


FIG. 22

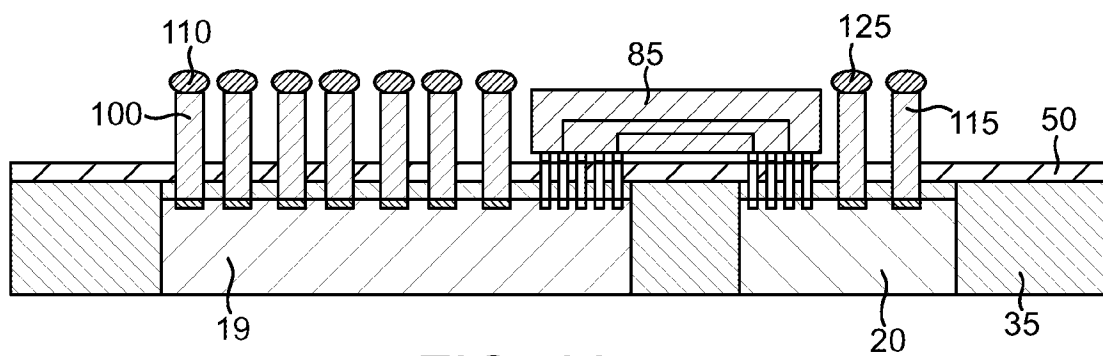


FIG. 23

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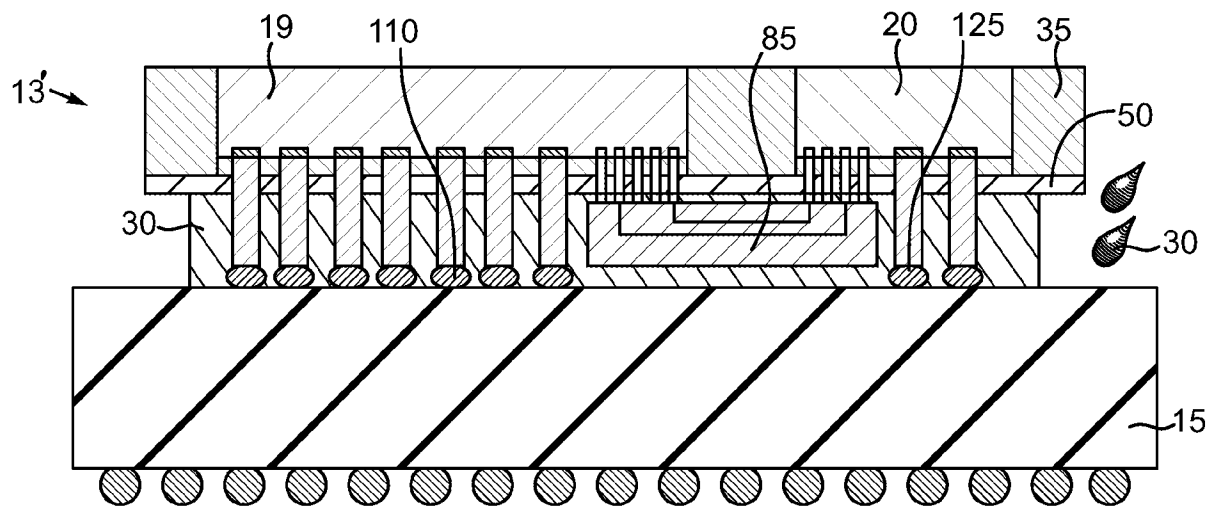


FIG. 24

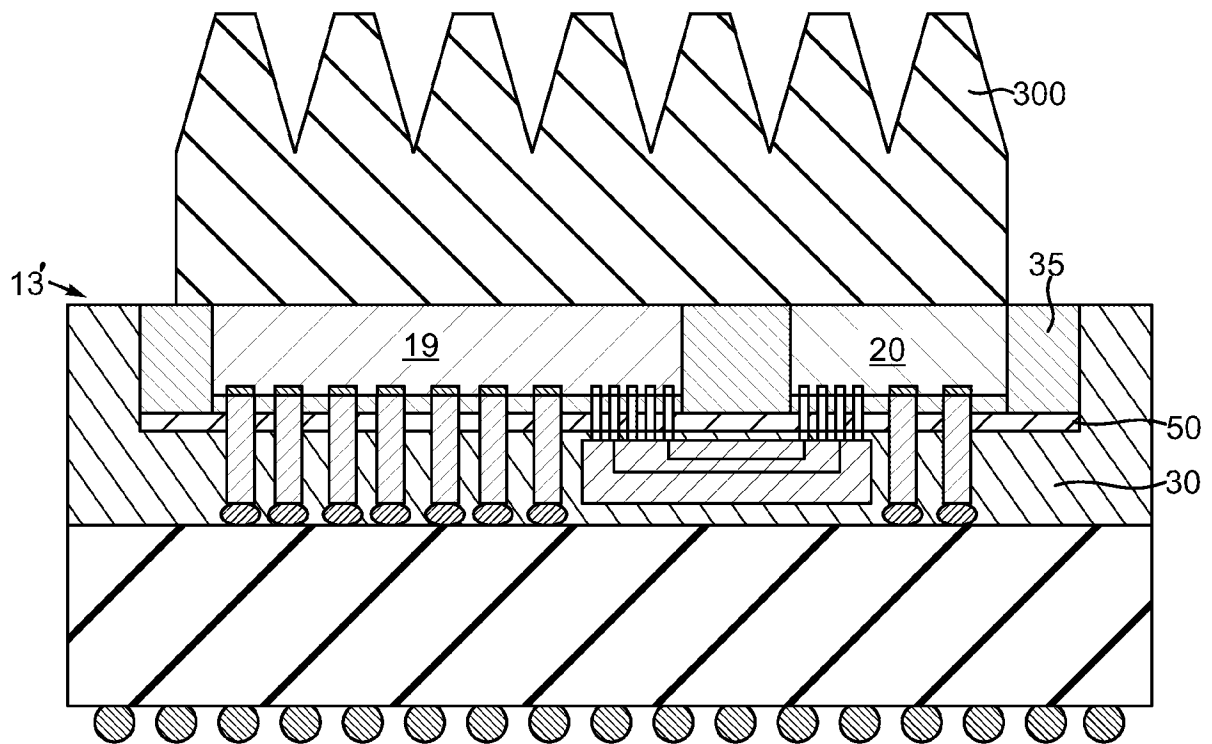


FIG. 25

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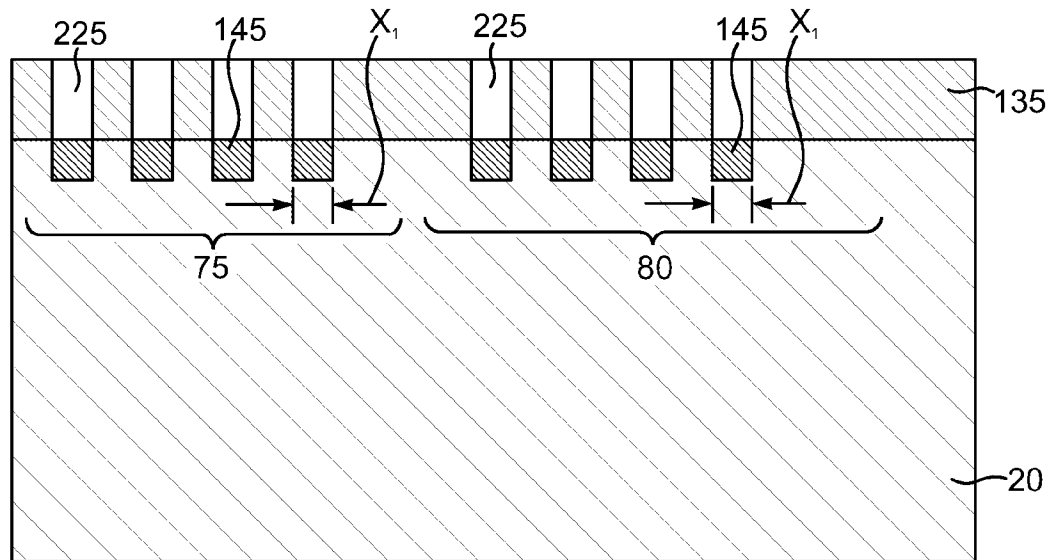


FIG. 26

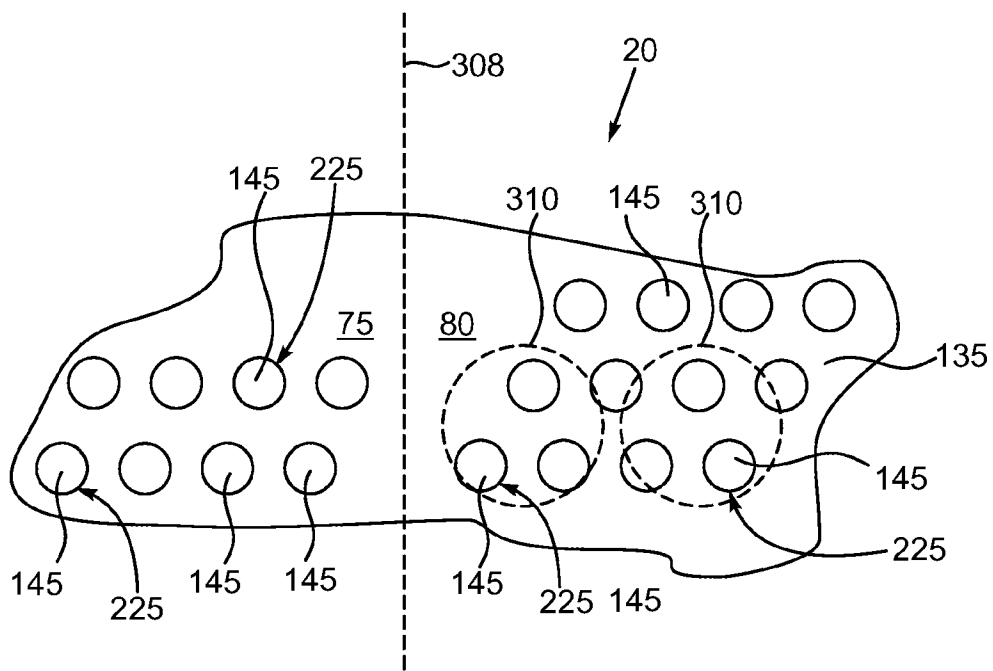


FIG. 27

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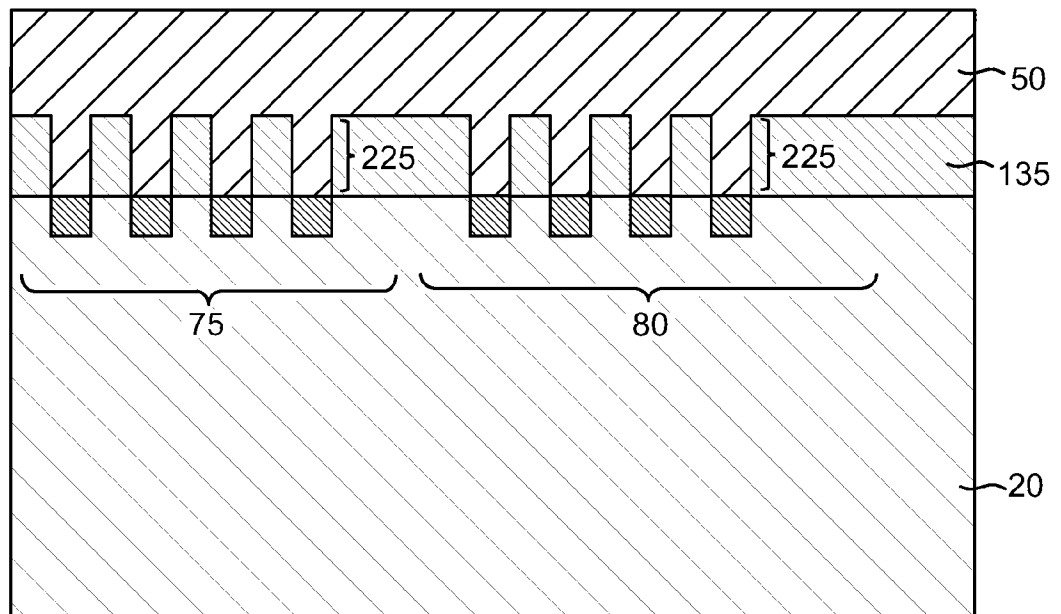


FIG. 28

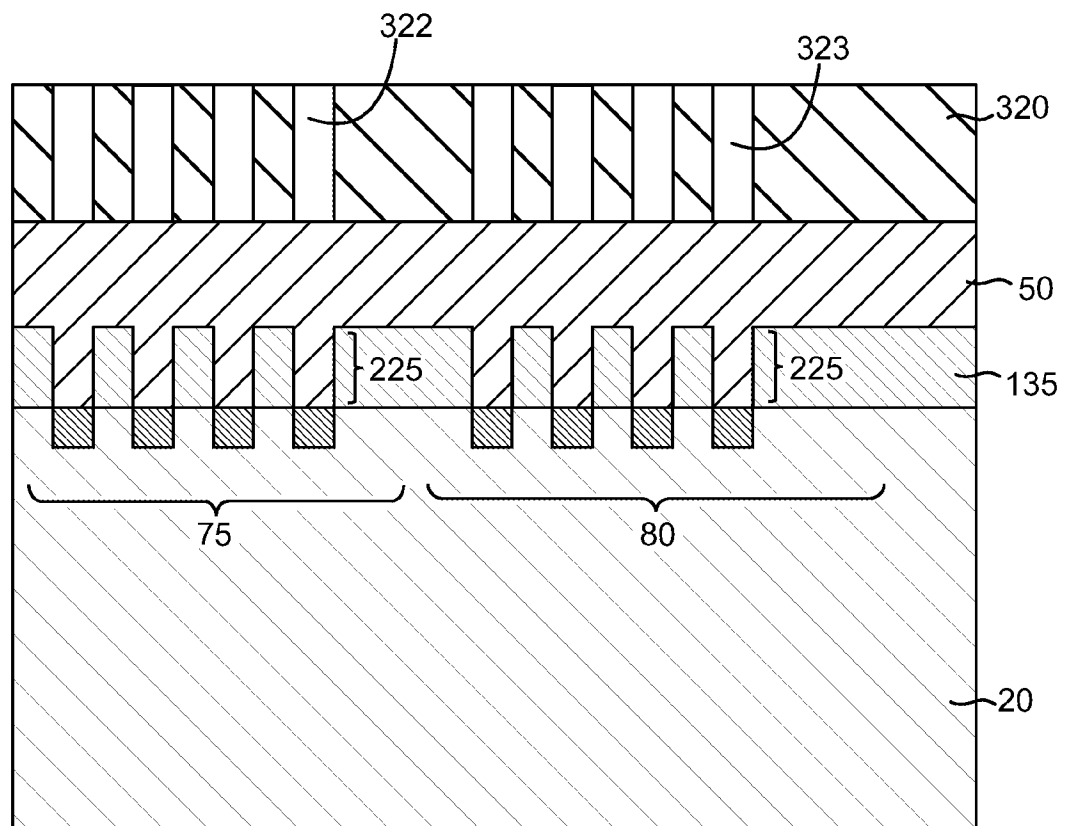


FIG. 29

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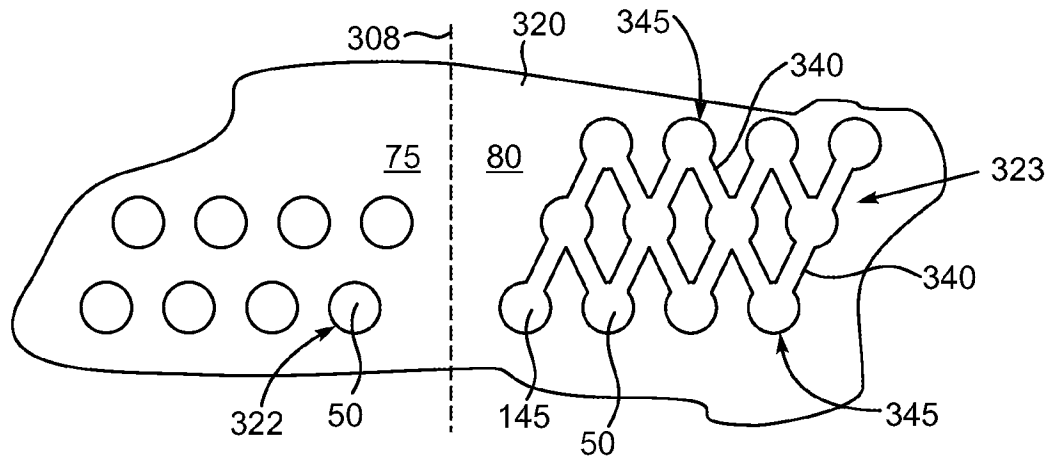


FIG. 30

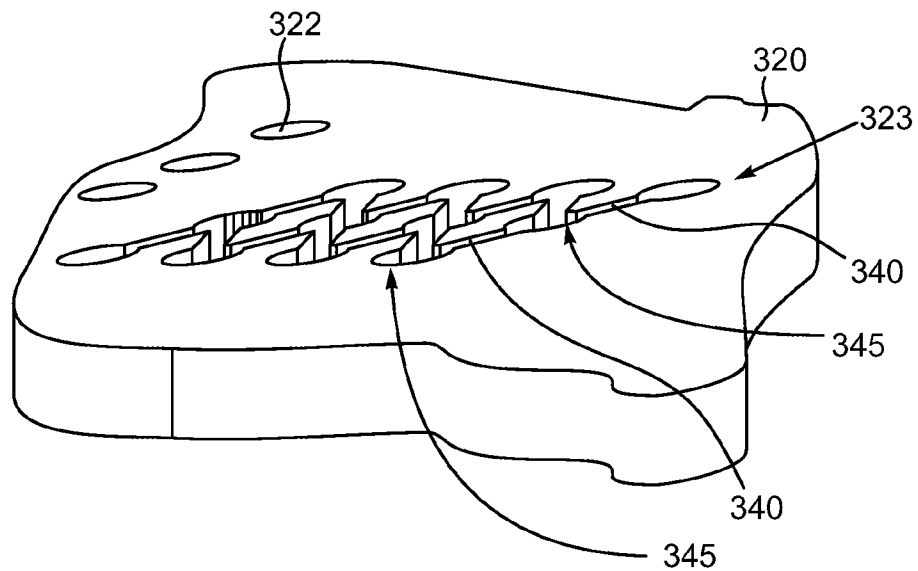


FIG. 31

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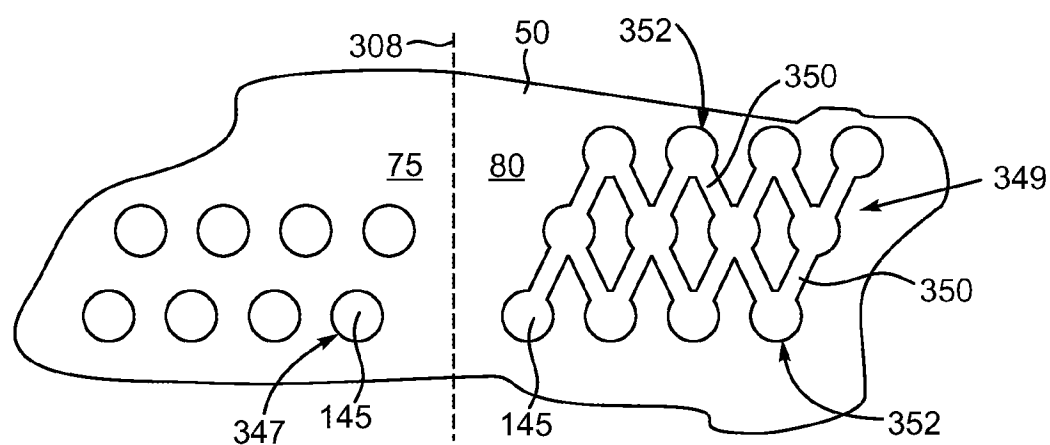


FIG. 32

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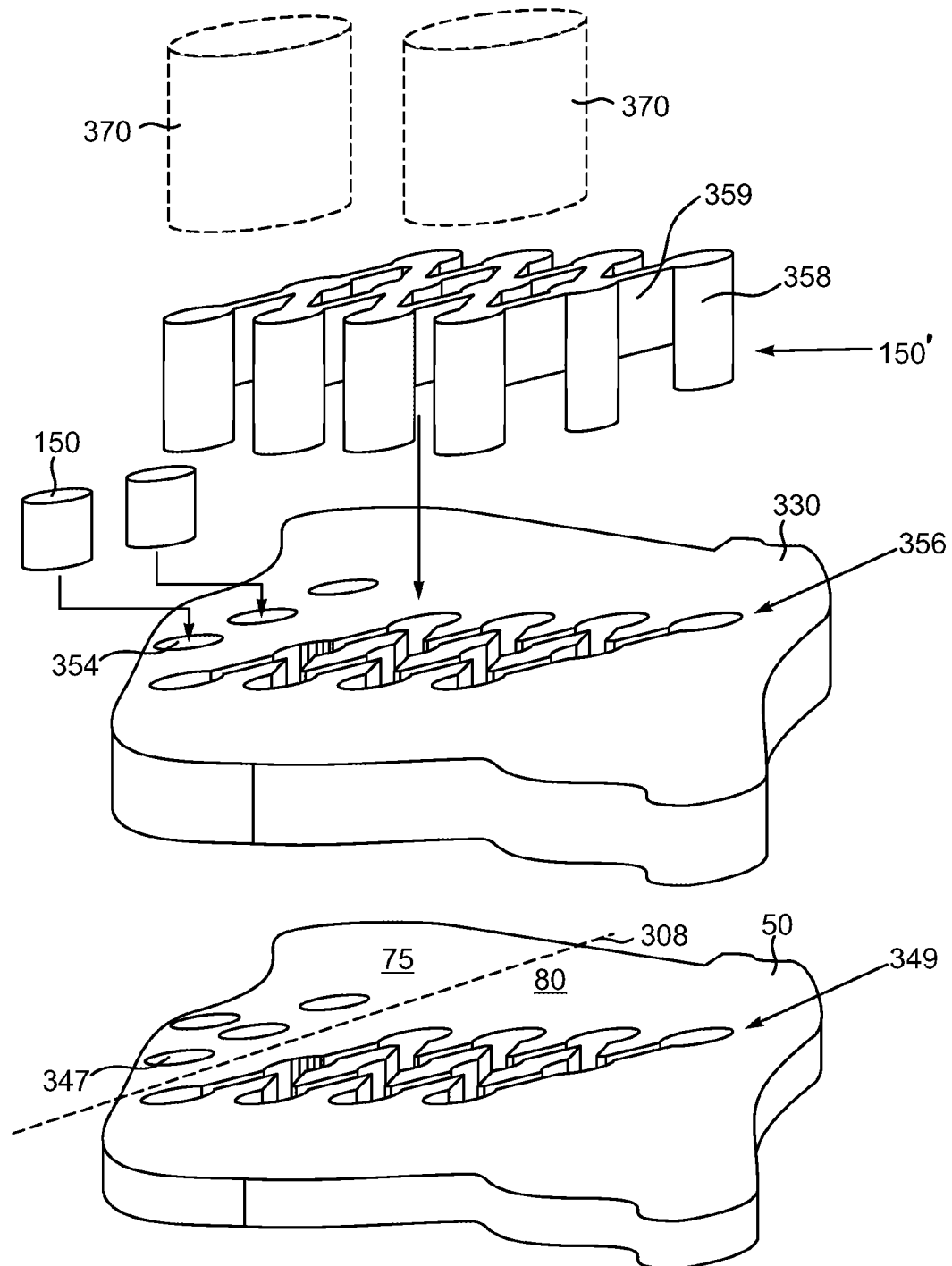


FIG. 33

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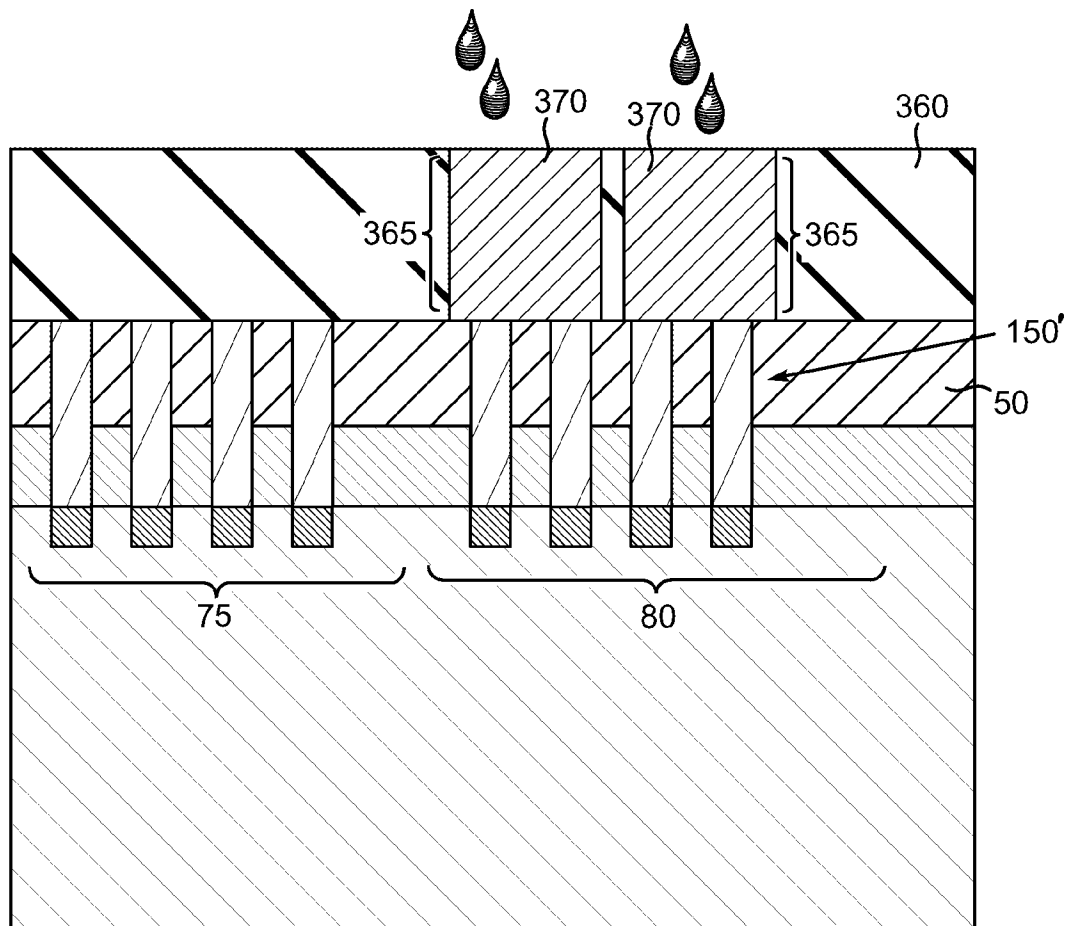


FIG. 34

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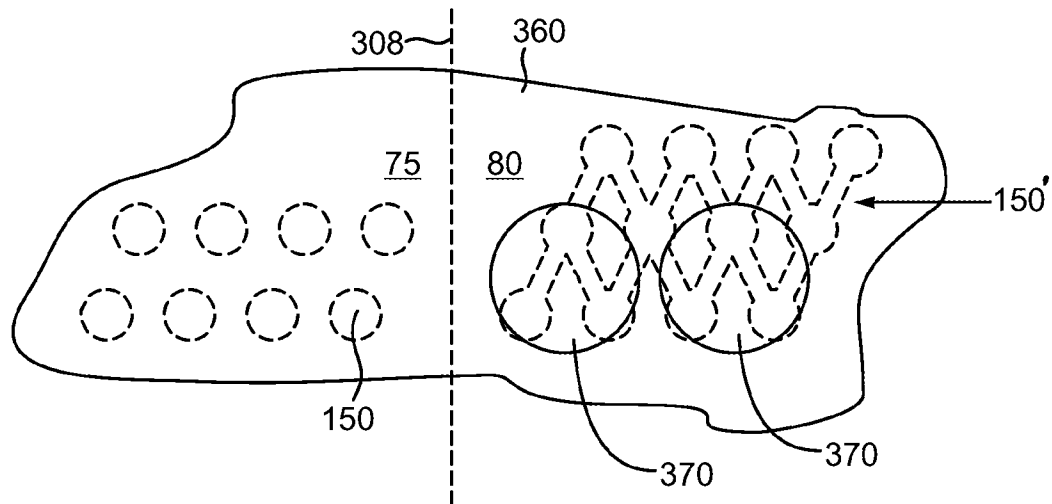


FIG. 35

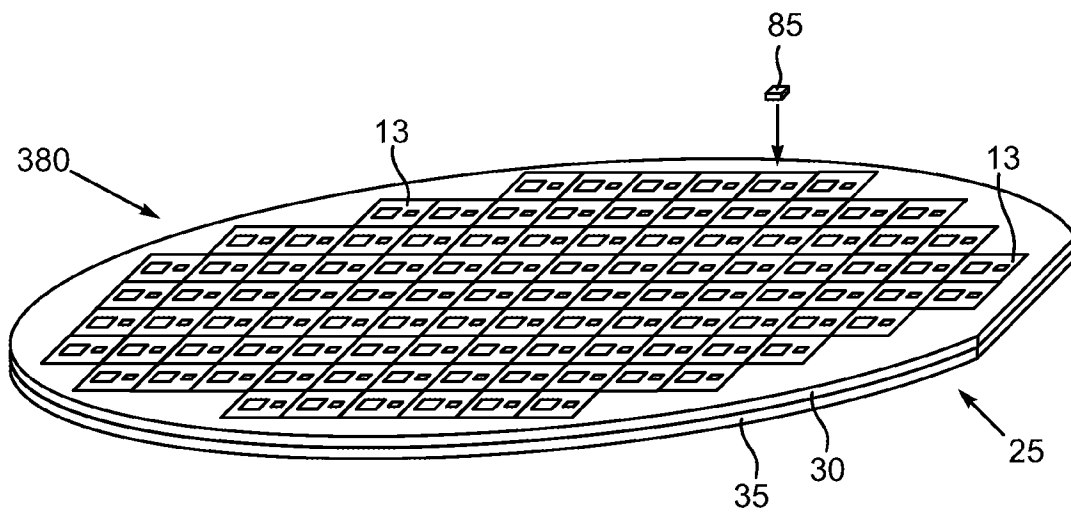


FIG. 36

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2018/044342**A. CLASSIFICATION OF SUBJECT MATTER****H01L 25/065(2006.01)i, H01L 23/31(2006.01)i, H01L 23/00(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

H01L 25/065; H01L 21/56; H01L 21/768; H01L 21/78; H01L 23/00; H01L 23/498; H01L 23/522; H01L 23/538; H01L 25/07; H01L 23/31

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: package, bridge, interconnection, embedded, molding, polymer, chip-to-chip

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 2017-111957 A1 (INTEL CORPORATION) 29 June 2017 See paragraphs [0016], [0024]-[0048]; claims 1, 11, 12; and figures 1A-2.	1-20
X	US 2011-0285006 A1 (CHAO-FU WENG et al.) 24 November 2011 See paragraphs [0047]-[0068]; and figures 24-41.	1-20
A	US 2014-0264791 A1 (MATHEW J. MANUSHAROW et al.) 18 September 2014 See paragraphs [0015]-[0023]; claim 1; and figure 1.	1-20
A	US 2014-0159228 A1 (WENG HONG TEH et al.) 12 June 2014 See paragraphs [0021]-[0025]; and figures 2, 4A-4G.	1-20
A	US 2016-0133571 A1 (QUALCOMM INCORPORATED) 12 May 2016 See claim 1; and figures 2, 7.	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 November 2018 (30.11.2018)

Date of mailing of the international search report

30 November 2018 (30.11.2018)

Name and mailing address of the ISA/KR

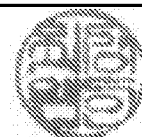
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

CHOI, Sang Won

Telephone No. +82-42-481-8291



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2018/044342

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2017-111957 A1	29/06/2017	DE 112015007213 T5 TW 201733053 A	13/09/2018 16/09/2017
US 2011-0285006 A1	24/11/2011	US 8288854 B2	16/10/2012
US 2014-0264791 A1	18/09/2014	BR 102014005946 A2 CN 104051420 A CN 104051420 B EP 2808891 A1 JP 2014-179613 A JP 5876093 B2 KR 10-1812373 B1 KR 10-2014-0113467 A US 8901748 B2	06/01/2015 17/09/2014 15/08/2017 03/12/2014 25/09/2014 02/03/2016 26/12/2017 24/09/2014 02/12/2014
US 2014-0159228 A1	12/06/2014	US 2015-0194406 A1 US 2016-0079196 A1 US 2017-0053887 A1 US 2018-0145047 A1 US 9171816 B2 US 9190380 B2 US 9437569 B2 US 9929119 B2	09/07/2015 17/03/2016 23/02/2017 24/05/2018 27/10/2015 17/11/2015 06/09/2016 27/03/2018
US 2016-0133571 A1	12/05/2016	CN 107078101 A EP 3216055 A1 US 9595496 B2 WO 2016-073790 A1	18/08/2017 13/09/2017 14/03/2017 12/05/2016

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: SHEEHAN, Adam D. DAVIDSON SHEEHAN LLP 6836 Austin Center Blvd., Suite 320 Austin, Texas 78731 USA	PCT NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION (PCT Rule 44.1)
Applicant's or agent's file reference 190141-PCT	Date of mailing (day/month/year) 30 December 2020 (30.12.2020)
International application No. PCT/US2020/052433	International filing date (day/month/year) 24 September 2020 (24.09.2020)
Applicant ADVANCED MICRO DEVICES, INC.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.
- Filing of amendments and statement under Article 19:**
 The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):
- When?** The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.
- How?** Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70
- For more detailed instructions, see** *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9-011.
2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.
3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
- ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.
- ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.
4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **22 months** from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority, that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR International Application Division Korean Intellectual Property Office 189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea Facsimile No. 82-42-481-8578	Authorized officer COMMISSIONER Telephone No. 82-42-481-5571
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* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2021.06.30**) from the date of mailing of the international search report.

<http://www.kipo.go.kr/en/> => PCT ISA Portal => PCT Status

ID : PCT international application number

PW : **8297ZDRJ@**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: <http://www.ipkcenter.com>

Email: ipkc@ipkcenter.com

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 190141-PCT	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US2020/052433	International filing date (<i>day/month/year</i>) 24 September 2020 (24.09.2020)	(Earliest) Priority Date (<i>day/month/year</i>) 27 September 2019 (27.09.2019)
Applicant ADVANCED MICRO DEVICES, INC.		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of :

- ☒ the international application in the language in which it was filed
☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☐ **Unity of invention is lacking** (See Box No. III)

4. With regard to the **title**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 1
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/052433**A. CLASSIFICATION OF SUBJECT MATTER****G06F 15/78(2006.01)i, H01L 25/065(2006.01)i, H01L 25/10(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 15/78; G06F 12/1009; G06F 12/1027; G06F 15/173; H01L 21/20; H01L 21/48; H04B 3/32; H01L 25/065; H01L 25/10

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: graphics processing unit (GPU), chiplet, active bridge, cache memory, scalable data fabric, hierarchy, level

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JIEMING YIN et al., 'Modular Routing Design for Chiplet-Based Systems', In: 2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA), pp. 726-738, 01-06 June 2018 pages 727, 733; and figure 2	1-20
Y	US 2018-0102251 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 12 April 2018 paragraphs [0039], [0118]; claim 1; and figure 2	1-20
Y	NOAH BECK et al., 'Zeppelin': An SoC for multichip architectures', In: 2018 IEEE International Solid - State Circuits Conference - (ISSCC), pp. 40-41, 11-15 February 2018 page 40; and figure 2.4.2	5-6, 11-14, 17-20
A	US 2019-0245582 A1 (INTEL CORPORATION) 08 August 2019 paragraphs [0011]-[0069]; and figures 1-8	1-20
A	US 2018-0246814 A1 (ADVANCED MICRO DEVICES, INC.) 30 August 2018 paragraphs [0020]-[0041]; and figures 1-10	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 December 2020 (30.12.2020)

Date of mailing of the international search report

30 December 2020 (30.12.2020)

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. +82-42-481-8578

Authorized officer

YANG, Jeong Rok

Telephone No. +82-42-481-5709



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/052433

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2018-0102251 A1	12/04/2018	CN 110088897 A	02/08/2019
		KR 10-2019-0053275 A	17/05/2019
		TW 201834083 A	16/09/2018
		TW 201931551 A	01/08/2019
		TW 201933578 A	16/08/2019
		TW I691037 B	11/04/2020
		US 10522352 B2	31/12/2019
		US 10580735 B2	03/03/2020
		US 10580757 B2	03/03/2020
		US 10586786 B2	10/03/2020
		US 10593667 B2	17/03/2020
		US 10600691 B2	24/03/2020
		US 10600735 B2	24/03/2020
		US 10600780 B2	24/03/2020
		US 10607136 B2	31/03/2020
		US 10672663 B2	02/06/2020
		US 10672743 B2	02/06/2020
		US 10672744 B2	02/06/2020
		US 10672745 B2	02/06/2020
		US 10832912 B2	10/11/2020
		US 2018-0330992 A1	15/11/2018
		US 2018-0330993 A1	15/11/2018
		US 2018-0331037 A1	15/11/2018
		US 2018-0331038 A1	15/11/2018
		US 2018-0331072 A1	15/11/2018
		US 2018-0331094 A1	15/11/2018
		US 2018-0331095 A1	15/11/2018
		US 2018-0350775 A1	06/12/2018
		US 2019-0042377 A1	07/02/2019
		US 2019-0042912 A1	07/02/2019
		US 2019-0042929 A1	07/02/2019
		US 2019-0043832 A1	07/02/2019
		US 2019-0123022 A1	25/04/2019
		US 2019-0123023 A1	25/04/2019
		US 2019-0123024 A1	25/04/2019
		US 2020-0194262 A1	18/06/2020
		US 2020-0203318 A1	25/06/2020
		US 2020-0219771 A1	09/07/2020
		US 2020-0357641 A1	12/11/2020
		WO 2018-067719 A2	12/04/2018
		WO 2018-067719 A3	26/07/2018
		WO 2019-079625 A1	25/04/2019
		WO 2019-079631 A1	25/04/2019
US 2019-0245582 A1	08/08/2019	CN 111834334 A	27/10/2020
US 2018-0246814 A1	30/08/2018	US 10282309 B2	07/05/2019

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

SHEEHAN, Adam D.

DAVIDSON SHEEHAN LLP 6836 Austin Center Blvd., Suite
320 Austin, Texas 78731 USA

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **30 December 2020 (30.12.2020)**

Applicant's or agent's file reference
190141-PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.

PCT/US2020/052433

International filing date (day/month/year)

24 September 2020 (24.09.2020)

Priority date(day/month/year)

27 September 2019 (27.09.2019)

International Patent Classification (IPC) or both national classification and IPC

G06F 15/78(2006.01)i, H01L 25/065(2006.01)i, H01L 25/10(2006.01)i

Applicant

ADVANCED MICRO DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☒ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon,
35208, Republic of Korea
Facsimile No. +82-42-481-8578



Date of completion of this opinion

30 December 2020 (30.12.2020)

Authorized officer

YANG, Jeong Rok

Telephone No. +82-42-481-5709



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433**Box No. I Basis of this opinion**

1. With regard to the **language**, this opinion has been established on the basis of :

- ☒ the international application in the language in which it was filed
- ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

- a. ☐ forming part of the international application as filed:
- ☐ in the form of an Annex C/ST.25 text file.
- ☐ on paper or in the form of an image file.
- b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
- c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
- ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
- ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: JIEMING YIN et al., 'Modular Routing Design for Chiplet-Based Systems', In: 2018 ACM/IEEE 45th Annual International Symposium on Computer Architecture (ISCA), pp. 726-738, 01-06 June 2018

D2: US 2018-0102251 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 12 April 2018

D3: NOAH BECK et al., "Zeppelin": An SoC for multichip architectures', In: 2018 IEEE International Solid - State Circuits Conference - (ISSCC), pp. 40-41, 11-15 February 2018

I. Novelty and Inventive Step (PCT Article 33(2) and (3))

1. Claims 1-9 (Note: The search report and written opinion have been established on the assumption that claims 5, 7-8 refer to claim 1.)

I.1. Claim 1

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a system, comprising: four GPU chiplets; one CPU chiplet; and an active interposer, wherein these five chiplets are stacked on the active interposer that implements its own NoC (network-on-chip) to interconnect the chiplets and other common system functionality (see pages 727, 733; and figure 2).

Claim 1 differs from D1 in that it further comprises "a second GPU chiplet [106-2] communicably coupled to the first GPU chiplet via an active bridge chiplet [118], wherein the active bridge chiplet includes a level of cache memory [210] that is shared by the first and second GPU chiplets of the GPU chiplet array". However, the different feature would be easily derived from the disclosure of D2 (see paragraph [0118]; and figure 2: "The active base die 108 can enable chiplets of various technologies to share one or more common memories,

Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433**Box No. VII Certain defects in the international application**

The following defects in the form or contents of the international application have been noted:

Claims 5, 7-8, 15, which are multiple dependent claims, do not comply with PCT Rule 6.4(a) because the claims refer to other multiple dependent claims. (Note: The search report and written opinion have been established on the assumption that: claims 5, 7-8 refer to claim 1; and claim 15 refers to claim 10.)

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box No. V

whereas conventionally each processor has its own dedicated coupled memory. The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

It would have been obvious to a person skilled in the art to arrive at the matter defined in claim 1 by combining the teachings of D1 and D2. Therefore, claim 1 lacks an inventive step.

1.2. Claims 2-9

The additional features of claims 2-3, 8-9 would be easily derived from a combination of the disclosure of D1 (see page 733; and figure 2: “The CPU chiplet consists of CPU cores, private CPU L1 and L2 caches, and a last level cache. Each GPU chiplet consists of 16 compute units (CUs) and 8 GPU L2 cache banks”) with the disclosure of D2 (see paragraph [0118]; and figure 2: “The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

The additional feature of claim 4 would be easily derived from the disclosure of D2 (see paragraph [0039]; and figure 2: “The example active base die 108 can be designed to place relevant functional blocks 202 near the native interconnects 210 of the chiplets 110 they are to connect with”).

The additional features of claims 5-6 would be easily derived from the disclosure of D3 (see page 40; and figure 2.4.2: “the Scalable Data Fabric (SDF) plane is designed to provide the coherent data transport between cores using the cache-coherent master (CCM), memory using the unified memory controller (UMC), and IO using the IO master/slave (IOMS”).

The additional feature of claim 7 would be easily derived from the disclosure of D2 (see claim 1: “direct-bonding a native core-side conductor of a first die with a conductor of a second die to make a native interconnect between the first die and the second die, the native interconnect extending a circuit of the first die across a die boundary between the first die and the second die, the circuit spanning across the native interconnect”).

Therefore, claims 2-4, 7-9 lack an inventive step as being obvious over D1 in view of D2, and claims 5-6 lack an inventive step as being obvious over D1 in view of D2, further in view of D3.

Continued on The Next Page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Previous Page

2. Claims 10-15 (Note: The search report and written opinion have been established on the assumption that claim 15 refers to claim 10.)

2.1. Claim 10

D1, which is considered to be the closest prior art to the subject matter of claim 10, discloses a method, comprising providing a central CPU chiplet to support CPU phases of GPGPU workloads (see page 727; and figure 2).

Claim 10 differs from D1 in that it further comprises “determining, at an active bridge chiplet controller [502] of the first GPU chiplet, that data associated with the memory access request is cached at an active bridge chiplet shared by the first GPU chiplet and a second GPU chiplet of the GPU chiplet array” and “routing the memory access request to a unified last level cache at the active bridge chiplet”. However, the different features would be easily derived from the disclosure of D2 (see paragraph [0118]; and figure 2: “The active base die 108 can enable chiplets of various technologies to share one or more common memories, whereas conventionally each processor has its own dedicated coupled memory. The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

It would have been obvious to a person skilled in the art to arrive at the matter defined in claim 10 by combining the teachings of D1 and D2. Therefore, claim 10 lacks an inventive step.

2.2. Claims 11-15

The additional features of claims 11-14 would be easily derived from the disclosure of D3 (see page 40; and figure 2.4.2: “the Scalable Data Fabric (SDF) plane is designed to provide the coherent data transport between cores using the cache-coherent master (CCM), memory using the unified memory controller (UMC), and IO using the IO master/slave (IOMS”).

The additional feature of claim 15 would be easily derived from a combination of the disclosure of D1 (see page 733; and figure 2: “The CPU chiplet consists of CPU cores, private CPU L1 and L2 caches, and a last level cache. Each GPU chiplet consists of 16 compute units (CUs) and 8 GPU L2 cache banks”) with the disclosure of D2 (see paragraph [0118]; and figure 2: “The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

Continued on The Next Page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052433**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Previous Page

Therefore, claim 15 lacks an inventive step as being obvious over D1 in view of D2, and claims 11-14 lack an inventive step as being obvious over D1 in view of D2, further in view of D3.

3. Claims 16-20

Claims 16-20 relate to a processor and have substantially the same technical features as claims 10-14. Accordingly, the same reasoning as in claims 10-14 can be applied to claims 16-20.

Therefore, claims 16-20 lack an inventive step.

II. Industrial Applicability (PCT Article 33(4))

Claims 1-20 are industrially applicable.

[Note] The phrase “The system of claim any preceding claim” in claim 4 seems to be a writing error for “The system of any preceding claim”.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:
SHEEHAN, Adam D.

Davidson Sheehan LLP 6836 Austin Center Blvd., Suite 320
Austin, Texas 78731 USA

PCT

**NOTIFICATION OF TRANSMITTAL OF
THE INTERNATIONAL SEARCH REPORT AND
THE WRITTEN OPINION OF THE INTERNATIONAL
SEARCHING AUTHORITY, OR THE DECLARATION**

(PCT Rule 44.1)

Date of mailing
(day/month/year) 30 December 2020 (30.12.2020)

Applicant's or agent's file reference
190142-PCT

FOR FURTHER ACTION See paragraphs 1 and 4 below

International application No.
PCT/US2020/052444

International filing date
(day/month/year) **24 September 2020 (24.09.2020)**

Applicant

ADVANCED MICRO DEVICES, INC.

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

How? Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9-011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. Reminders

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **22 months** from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority, that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea
Facsimile No. 82-42-481-8578

Authorized officer

COMMISSIONER

Telephone No. 82-42-481-5571



* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2021.06.30**) from the date of mailing of the international search report.

<http://www.kipo.go.kr/en/> => PCT ISA Portal => PCT Status

ID : PCT international application number

PW : **V6YTBW6TS**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC' (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: <http://www.ipkcenter.com>

Email: ipkc@ipkcenter.com

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 190142-PCT	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US2020/052444	International filing date (<i>day/month/year</i>) 24 September 2020 (24.09.2020)	(Earliest) Priority Date (<i>day/month/year</i>) 27 September 2019 (27.09.2019)
Applicant ADVANCED MICRO DEVICES, INC.		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 4 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of :

- ☒ the international application in the language in which it was filed
☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☐ **Unity of invention is lacking** (See Box No. III)

4. With regard to the **title**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the drawings,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 2
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
 b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/052444**A. CLASSIFICATION OF SUBJECT MATTER****G06F 15/78(2006.01)i, H01L 23/538(2006.01)i, H01L 25/065(2006.01)i, H01L 25/10(2006.01)i, H01L 23/32(2006.01)i, H01L 23/48(2006.01)i, H01L 23/498(2006.01)i, H01L 23/525(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 15/78; H01L 21/20; H01L 21/3065; H01L 21/48; H01L 21/78; H01L 23/00; H01L 23/31; H01L 25/065; H01L 23/538; H01L 25/10; H01L 23/32; H01L 23/48; H01L 23/498; H01L 23/525

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & keywords: graphics processing unit (GPU), chiplet, active bridge, cache memory, carrier wafer, bonding, substrate, share

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	WO 2019-032322 A1 (ADVANCED MICRO DEVICES, INC.) 14 February 2019 paragraphs [0069], [0071], [0076]-[0077], [0081]; claim 1; and figures 5, 8, 15, 17, 20, 33	1-20
Y	US 2018-0102251 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 12 April 2018 paragraph [0118]; and figure 2	1-20
A	US 2018-0102338 A1 (ADVANCED MICRO DEVICES, INC.) 12 April 2018 paragraphs [0022]-[0034]; and figures 1-7	1-20
A	US 2015-0243528 A1 (PALO ALTO RESEARCH CENTER INCORPORATED) 27 August 2015 paragraphs [0021]-[0036]; and figures 1-5	1-20
A	US 2018-0233470 A1 (INFINEON TECHNOLOGIES AG) 16 August 2018 paragraphs [0064]-[0080]; and figures 1-7	1-20



Further documents are listed in the continuation of Box C.



See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

30 December 2020 (30.12.2020)

Date of mailing of the international search report

30 December 2020 (30.12.2020)

Name and mailing address of the ISA/KR

International Application Division
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189 Cheongsu-ro, Seo-gu, Daejeon, 35208, Republic of Korea

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Authorized officer

YANG JEONG ROK

Telephone No. +82-42-481-5709



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/052444

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2019-032322 A1	14/02/2019	CN 111033731 A	17/04/2020
		EP 3665721 A1	17/06/2020
		JP 2020-528220 A	17/09/2020
		KR 10-2020-0030563 A	20/03/2020
		US 10510721 B2	17/12/2019
		US 2019-0051633 A1	14/02/2019
US 2018-0102251 A1	12/04/2018	CN 110088897 A	02/08/2019
		KR 10-2019-0053275 A	17/05/2019
		TW 201834083 A	16/09/2018
		TW 201931551 A	01/08/2019
		TW 201933578 A	16/08/2019
		TW I691037 B	11/04/2020
		US 10522352 B2	31/12/2019
		US 10580735 B2	03/03/2020
		US 10580757 B2	03/03/2020
		US 10586786 B2	10/03/2020
		US 10593667 B2	17/03/2020
		US 10600691 B2	24/03/2020
		US 10600735 B2	24/03/2020
		US 10600780 B2	24/03/2020
		US 10607136 B2	31/03/2020
		US 10672663 B2	02/06/2020
		US 10672743 B2	02/06/2020
		US 10672744 B2	02/06/2020
		US 10672745 B2	02/06/2020
		US 10832912 B2	10/11/2020
		US 2018-0330992 A1	15/11/2018
		US 2018-0330993 A1	15/11/2018
		US 2018-0331037 A1	15/11/2018
		US 2018-0331038 A1	15/11/2018
		US 2018-0331072 A1	15/11/2018
		US 2018-0331094 A1	15/11/2018
		US 2018-0331095 A1	15/11/2018
		US 2018-0350775 A1	06/12/2018
		US 2019-0042377 A1	07/02/2019
		US 2019-0042912 A1	07/02/2019
		US 2019-0042929 A1	07/02/2019
		US 2019-0043832 A1	07/02/2019
		US 2019-0123022 A1	25/04/2019
		US 2019-0123023 A1	25/04/2019
		US 2019-0123024 A1	25/04/2019
		US 2020-0194262 A1	18/06/2020
		US 2020-0203318 A1	25/06/2020
		US 2020-0219771 A1	09/07/2020
		US 2020-0357641 A1	12/11/2020
		WO 2018-067719 A2	12/04/2018
		WO 2018-067719 A3	26/07/2018
		WO 2019-079625 A1	25/04/2019

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/052444

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
		WO 2019-079631 A1	25/04/2019
US 2018-0102338 A1	12/04/2018	None	
US 2015-0243528 A1	27/08/2015	US 9305807 B2	05/04/2016
US 2018-0233470 A1	16/08/2018	CN 108428662 A	21/08/2018
		DE 102017103095 A1	16/08/2018

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:

SHEEHAN, Adam D.

Davidson Sheehan LLP 6836 Austin Center Blvd., Suite 320
Austin, Texas 78731 USA

PCT

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

Date of mailing
(day/month/year) **30 December 2020 (30.12.2020)**

Applicant's or agent's file reference
190142-PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No.
PCT/US2020/052444

International filing date (day/month/year)
24 September 2020 (24.09.2020)

Priority date(day/month/year)
27 September 2019 (27.09.2019)

International Patent Classification (IPC) or both national classification and IPC

G06F 15/78(2006.01)i, H01L 23/538(2006.01)i, H01L 25/065(2006.01)i, H01L 25/10(2006.01)i, H01L 23/32(2006.01)i, H01L 23/48(2006.01)i, H01L 23/498(2006.01)i, H01L 23/525(2006.01)i

Applicant

ADVANCED MICRO DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon,
35208, Republic of Korea
Facsimile No. +82-42-481-8578



Date of completion of this opinion

30 December 2020 (30.12.2020)

Authorized officer

YANG JEONG ROK

Telephone No. +82-42-481-5709



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052444**Box No. I Basis of this opinion**

1. With regard to the **language**, this opinion has been established on the basis of :

- ☒ the international application in the language in which it was filed
- ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

- a. ☐ forming part of the international application as filed:
- ☐ in the form of an Annex C/ST.25 text file.
- ☐ on paper or in the form of an image file.
- b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
- c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
- ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
- ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052444

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-20	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: WO 2019-032322 A1 (ADVANCED MICRO DEVICES, INC.) 14 February 2019

D2: US 2018-0102251 A1 (INVENSAS BONDING TECHNOLOGIES, INC.) 12 April 2018

I. Novelty and Inventive Step (PCT Article 33(2) and (3))

1. Claims 1-11

1.1. Claim 1

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a method of manufacturing a molded chip combination, comprising: mounting semiconductor chips 19 and 20 to a carrier substrate 210; and mounting a completed molded chip combination 13 to a circuit board 15 by way of a reflow process of solder interconnects 110 and 125 (see paragraphs [0069], [0077]; and figures 5, 20).

Claim 1 differs from D1 in that it further comprises “bonding a face surface of an active bridge chiplet to a face surface of the first and second GPU chiplets, wherein the active bridge chiplet includes a level of cache memory that is shared by the first and second GPU chiplets”. However, the different feature would be easily derived from a combination of the disclosure of D1 (see claim 1; and figure 15: “an interconnect chip 85 interconnecting the first PHY region to the second PHY region; a first molding layer 35 laterally joining together the first semiconductor chip and the second semiconductor chip”) with the disclosure of D2 (see paragraph [0118]; and figure 2: “The active base die 108 can enable chiplets of various technologies to share one or more common memories, whereas conventionally each processor has its own dedicated coupled memory. The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052444**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Box No. V

It would have been obvious to a person skilled in the art to arrive at the matter defined in claim 1 by combining the teachings of D1 and D2. Therefore, claim 1 lacks an inventive step.

1.2. Claims 2-11

The additional feature of claim 2 would be easily derived from the disclosure of D1 (see paragraph [0069]; and figure 5: mounting the semiconductor chips 19 and 20 to the carrier substrate 210).

The additional features of claims 3-4 would be easily derived from the disclosure of D1 (see claim 1; and figure 17: “a second molding layer 30 at least partially encapsulating the interconnect chip; and a polymer layer 50 positioned between the first molding layer and the second molding layer”).

The additional feature of claim 5 would be easily derived from the disclosure of D1 (see paragraph [0071]; and figure 8: “the semiconductor chips 19 and 20 and molding layer 35 can be separated from the carrier substrate 210”).

The additional features of claims 6-7 would be easily derived from the disclosure of D1 (see paragraph [0076]; and figure 17: “a second molding process is performed to form the molding layer 30 over the interconnect chip 85, the conductive pillars 100 and 115 and the otherwise exposed portions of the polymer layer 50”).

The additional features of claims 8-9 would be easily derived from the disclosure of D1 (see paragraph [0081]; and figure 33: “Like the conductor bars 359, conductor traces (not shown) could also be fabricated in this way such that the polymer layer 50 enables fabrication of redistribution layer traces”).

The additional feature of claim 10 would be easily derived from the disclosure of D1 (see paragraph [0076]; and figure 17: “This grinding process is designed to expose the conductive pillars 100 and 115 and, depending upon the height of the interconnect chip 85, can also thin the backside of the interconnect chip 85 as well”).

The additional feature of claim 11 would be easily derived from the disclosure of D1 (see

Continued on The Next Page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2020/052444

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Previous Page

paragraph [0077]; and figure 20: mounting the completed molded chip combination 13 to the circuit board 15 by way of the reflow process of the solder interconnects 110 and 125).

Therefore, claims 2-11 lack an inventive step as being obvious over D1 in view of D2.

2. Claims 12-18

2.1. Claim 12

D1, which is considered to be the closest prior art to the subject matter of claim 12, discloses a method of manufacturing a molded chip combination, comprising: mounting semiconductor chips 19 and 20 to a carrier substrate 210; and mounting a completed molded chip combination 13 to a circuit board 15 by way of a reflow process of solder interconnects 110 and 125 (see paragraphs [0069], [0077]; and figures 5, 20).

Claim 12 differs from D1 in that it further comprises “bonding a face surface of an active bridge chiplet to a back surface of the first and second GPU chiplets, wherein the active bridge chiplet includes a level of cache memory that is shared by the first and second GPU chiplets”. However, the different feature would be easily derived from a combination of the disclosure of D1 (see claim 1; and figure 15: “an interconnect chip 85 interconnecting the first PHY region to the second PHY region; a first molding layer 35 laterally joining together the first semiconductor chip and the second semiconductor chip”) with the disclosure of D2 (see paragraph [0118]; and figure 2: “The active base die 108 can enable chiplets of various technologies to share one or more common memories, whereas conventionally each processor has its own dedicated coupled memory. The active base die 108 can allow external memory to be utilized as embedded memory with process sharing”).

It would have been obvious to a person skilled in the art to arrive at the matter defined in claim 12 by combining the teachings of D1 and D2. Therefore, claim 12 lacks an inventive step.

2.2. Claims 13-18

The additional feature of claim 13 would be easily derived from the disclosure of D1 (see paragraph [0076]; and figure 17: “This grinding process is designed to expose the conductive pillars 100 and 115 and, depending upon the height of the interconnect chip 85, can also thin

Continued on The Next Page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/052444**Supplemental Box**

In case the space in any of the preceding boxes is not sufficient.

Continuation of: Previous Page

the backside of the interconnect chip 85 as well”).

The additional features of claims 14, 17 would be easily derived from the disclosure of D1 (see paragraph [0069]; and figure 5: mounting the semiconductor chips 19 and 20 to the carrier substrate 210).

The additional feature of claim 15 would be easily derived from the disclosure of D1 (see claim 1; and figure 17: “a second molding layer 30 at least partially encapsulating the interconnect chip; and a polymer layer 50 positioned between the first molding layer and the second molding layer”).

The additional feature of claim 16 would be easily derived from the disclosure of D1 (see paragraph [0071]; and figure 8: “the semiconductor chips 19 and 20 and molding layer 35 can be separated from the carrier substrate 210”).

The additional feature of claim 18 would be easily derived from the disclosure of D1 (see paragraph [0076]; and figure 17: “a second molding process is performed to form the molding layer 30 over the interconnect chip 85, the conductive pillars 100 and 115 and the otherwise exposed portions of the polymer layer 50”).

Therefore, claims 13-18 lack an inventive step as being obvious over D1 in view of D2.

3. Claims 19-20

Claims 19-20 relate to a processor and have substantially the same technical features as claims 1-2. Accordingly, the same reasoning as in claims 1-2 can be applied to claims 19-20.

Therefore, claims 19-20 lack an inventive step.

II. Industrial Applicability (PCT Article 33(4))

Claims 1-20 are industrially applicable.

Electronic Patent Application Fee Transmittal

Application Number:	16456287			
Filing Date:	28-Jun-2019			
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS			
First Named Inventor/Applicant Name:	Skyler J. SALEH			
Filer:	Ryan Scott Davidson/Emily Stalder			
Attorney Docket Number:	1458-190070			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt

EFS ID:	42124580
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Ryan Scott Davidson/Emily Stalder
Filer Authorized By:	Ryan Scott Davidson
Attorney Docket Number:	1458-190070
Receipt Date:	09-MAR-2021
Filing Date:	28-JUN-2019
Time Stamp:	10:01:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$260
RAM confirmation Number	E202139A02073406
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	190070_IDS.pdf	1035257	no	5
			ebcb00d5f6024c24de920f402cbb30fd581bffb2d		
Warnings:					
Information:					
2	Foreign Reference	WO2019032322A1.pdf	4191877	no	41
			25d2eae99dadd44c518d4706fb77ae2da853a52e		
Warnings:					
Information:					
3	Non Patent Literature	01-04-21_190141_NFOA.pdf	17429613	no	25
			121f2e06680a58dd8c9f68f137efba8f13457550		
Warnings:					
Information:					
4	Non Patent Literature	12-30-20_190141-PCT_ISR-WO.pdf	3949924	no	12
			a2d624b259275b0e29b8c9144a78d01c9c2c2f37		
Warnings:					
Information:					
5	Non Patent Literature	BURD-Zeppelin_An_SoC_for_Multichip_Architectures.pdf	4831305	no	11
			6d98598785a610026e1cd993ab9a66972bfb958d		
Warnings:					
Information:					
6	Non Patent Literature	12-30-20_190142-PCT_ISR-WO.pdf	3965621	no	12
			ed06cae4c73cb6ccc47d4134f1f62645f34fde2b		
Warnings:					
Information:					

7	Non Patent Literature	11-13-20_190143_NFOA.pdf	13296570	no	19
			830939c3756bb546afe10f069e8147bc1d16c715		

Warnings:**Information:**

8	Fee Worksheet (SB06)	fee-info.pdf	30689	no	2
			0370ae04f0adc4b33c7dc946681985266ae0ab69		

Warnings:**Information:**

Total Files Size (in bytes):			48730856
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Skyler J. SALEH et al.

Title: GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

App. No.: 16/456,287

Filed: June 28, 2019

Examiner: Jae Un YU

Group Art Unit: 2135

Atty. Dkt. No.: 1458-190070

Confirmation No.: 4820

RESPONSE TO OFFICE ACTION

Dear Sir:

In response to the Office Action mailed September 11, 2020, please amend the above-identified application as follows:

A Claim Listing begins on page 2.

Remarks begin on page 7.

Electronic Patent Application Fee Transmittal

Application Number:	16456287			
Filing Date:	28-Jun-2019			
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS			
First Named Inventor/Applicant Name:	Skyler J. SALEH			
Filer:	Ryan Scott Davidson/Emily Stalder			
Attorney Docket Number:	1458-190070			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 3 months with \$0 paid	1253	1	1480	1480
Miscellaneous:				
Total in USD (\$)				1480

Electronic Acknowledgement Receipt

EFS ID:	42020947
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Ryan Scott Davidson
Filer Authorized By:	
Attorney Docket Number:	1458-190070
Receipt Date:	25-FEB-2021
Filing Date:	28-JUN-2019
Time Stamp:	14:00:54
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1480
RAM confirmation Number	E20212OE01090036
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		190070_Response_NFOA-Final.pdf	129185	yes	11
			1adff9dbae9fa42727ea2427da39715970fb1540		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Applicant Arguments/Remarks Made in an Amendment		7	11	
	Claims		2	6	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31210	no	2
			84c824bc86ef61758d719d0c7a21ea22569c5dc0		
Warnings:					
Information:					
Total Files Size (in bytes):			160395		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REMARKS

The Office Action dated September 11, 2020 has been received and considered. No claims have been amended. Reconsideration of the pending rejections in the present application is respectfully requested based on the following remarks.

Allowability of Claim 9

The Applicant notes with appreciation the indication on page 4 that claim 9 would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. The Applicant has opted to forgo rewriting these claims as suggested in view of the following remarks.

35 U.S.C. § 102 Rejection of Claims 1-4, 7, and 10

On page 2 of the Office Action, claims 1-4, 7, and 10 are rejected under 35 U.S.C. § 102(a)(1) as being anticipated by Teig (US 2019/0123022). This rejection is hereby respectfully traversed.

As explained below, Teig fails to disclose “a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array” and “wherein the GPU chiplet array includes: the first GPU chiplet communicably coupled to the CPU via a bus; and a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications.”

In particular, MPEP § 2131 states that “[a] claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.’ See *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).” “‘The identical invention must be shown in as complete detail as is contained in the ... claim.’ *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).” Moreover, “[e]very element of the claimed invention must be literally present, arranged as in the claim.” See *Id.*

In the present case, the Office Action has not established that each element of the claims is disclosed in Teig. For example, regarding the features of claim 1, the Office Action, on page 2, merely directs the Applicant to the CPU and GPU in FIG. 9 of Teig and also paragraph [0148]

of Teig. Teig describes FIG. 9, the CPU, and the GPU in paragraphs [0090] and [0091] as follows:

FIG. 9 illustrates yet another 3D processor 900 of some embodiments. This processor 900 is identical to the processor 400 of FIG. 4, except that it only has one L1 cache 932 on a die 910 for each of six CPU (central processing unit) cores 922 and one L1 cache 934 for each of two GPU (graphical processing unit) cores 924 that are defined on a die 905 that is face-to-face mounted to the die 910 through a DBI bonding process. The processor 900 does not use layers 2 and 3 caches as it uses large L1 caches for its CPU and GPU cores. The L1 caches can be larger than traditional L1 caches as they are defined on another die than the die on which the cores are defined, and hence face less space restrictions on their placement and the amount of space that they consume on the chip.

In FIG. 9, the processor 900 has its I/O interface defined on a third die 415 that is face-to-back mounted on the die 910. In other embodiments, the processor 900 does not include the third die 415, but just includes the first and second dies 905 and 910. In some of these embodiments, the I/O interface of the processor 900 is defined on the first and/or second dies 905 and 910. Also, in other embodiments, one L1 cache 932 is shared across multiple CPU cores 922 and/or multiple GPU cores 924.

As shown, Teig generally mentions GPU cores. Nowhere does Teig disclose that the GPU cores are GPU chiplets. Also, even assuming *arguendo* that Teig's GPU cores are comparable to the GPU chiplets of claim 1, nowhere does Teig disclose both that a first GPU core is communicably coupled to the CPU via a bus and a second GPU core is coupled to the first GPU chiplet via a passive crosslink. The cited sections of Teig fail to provide any details regarding how the GPU cores are coupled to the CPU and each other. Also, regarding the passive crosslink of claim 1, this claim requires that "the passive crosslink is dedicated for inter-chiplet communications". In contrast, paragraph [0148] of Teig merely states, "the first IC die is face-to-face mounted with a passive interposer that electrically connects the die to circuits outside of the 3D chip or to other dies that are face-to-face mounted or back-to-face mounted on the interposer." Nowhere in paragraph [0148] does Teig disclose that the passive interposer is dedicated for inter-chiplet communications. Teig, therefore, fails to disclose at least the aforementioned features of claim 1. As such, Teig fails to anticipate claim 1 since each and every element set forth in claim 1 is not found or literally present in Teig. Claim 1 is, therefore, novel over Teig.

Claims 2-4, 7, and 10 depend on claim 1. Accordingly, Teig fails to disclose the features of these dependent claims, at least by virtue of their respective dependence on claim 1. In addition, these dependent claims recite additional novel features.

In view of the foregoing, withdrawal of the above-referenced anticipation rejection and reconsideration of the claims is respectfully requested.

35 U.S.C. § 103 Rejection of Claims 5, 6, 8, and 11-20

On page 4 of the Office Action, claims 5, 6, 8, and 11-20 are rejected under 35 U.S.C. § 103 as being unpatentable over Teig in view of Yasuda (US 2001/0005873). This rejection is hereby respectfully traversed.

Claims 5, 6, and 8 depend on claim 1. As explained above, Teig fails to disclose or render obvious the features of claim 1. Further, Yasuda does not remedy the deficiencies of Teig. Accordingly, the cited references, individually and in combination, fail to disclose or render obvious the features of independent claim 1. Therefore, the cited references fail to disclose the features of dependent claims 5, 6, and 8, at least by virtue of their dependence on claim 1. In addition, these dependent claims recite additional novel and non-obvious features.

Regarding independent claims 11 and 16, on page 4, the Office Action states, “the examiner directs the applicant’s attention to the claims (*Sic*) rejection above.” As such, since the Office Action appears to be comparing claims 11 and 16 to claim 1, these claims are novel over Teig for at least the reasons presented above with respect to claim 1.

Claims 12-15 and 17-20 depend on claims 11 and 16, respectively. As explained above, Teig fails to disclose or render obvious the features of claims 11 and 16. Further, Yasuda does not remedy the deficiencies of Teig. Accordingly, the cited references, individually and in combination, fail to disclose or render obvious the features of independent claims 11 and 16. Therefore, the cited references fail to disclose the features of dependent claims 12-15 and 17-20, at least by virtue of their respective dependence on claims 11 and 16. In addition, these dependent claims recite additional novel and non-obvious features.

Furthermore, by applying the rejection of system claim 1 to method claim 11 and computer-readable medium (CRM) claim 16 without providing a clear articulation of the reason(s) why the operational features of these claims are anticipated or obvious in view of the

cited art, the Office has placed an undue burden on the Applicant. MPEP § 2143, citing *KSR*, states that “[t]he key to supporting any rejection under 35 U.S.C. 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. The Supreme Court in *KSR* noted that the analysis supporting a rejection under 35 U.S.C. 103 should be made explicit.” See also *KSR Intl Co. v. Teleflex Inc.*, 82 USPQ2d 1385, 1395-97 (2007). The Applicant notes that while *KSR* and the cited section of the MPEP are directed to obviousness rejections under 35 U.S.C. § 103, it is apparent that the Supreme Court believes that a clear articulation of reasons is “the key” to supportable rejections by the USPTO under both 35 U.S.C. §102 and §103. Without proper guidance on which “element” of the claims is believed to correspond with which section cited in the rejection, the Applicant is forced to guess which features in the cited art the Examiner believes to disclose each of the claimed features. Because reasons for the rejection of claims 11-20 were not presented in the Office Action and the Applicant cannot reasonably determine which feature of Teig is believed to correspond with which feature recited in claims, the Applicant respectfully submits that the rejection is improper and must be withdrawn.

In view of the foregoing, withdrawal of the above-referenced obviousness rejection and reconsideration of the claims is respectfully requested.

Conclusion

The Applicant respectfully submits that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present application to issue, if any comments, questions, or suggestions arise in connection with the present application.

PATENT

The Applicant believes no additional fees are due, but if the Commissioner believes additional fees are due, the Commissioner is hereby authorized to charge any fees, which may be required, or credit any overpayment, to Deposit Account Number 50-5933.

Respectfully submitted,

/Thomas S. Grzesik/

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(512) 582-2455 (phone)
(512) 355-1119 (fax)

February 25, 2021

Date

CLAIMS LISTING

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A system, comprising:
 - a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array, wherein the GPU chiplet array includes:
 - the first GPU chiplet communicably coupled to the CPU via a bus; and
 - a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications.
2. (Original) The system of claim 1, wherein the passive crosslink comprises a passive interposer die.
3. (Original) The system of claim 1, wherein the first GPU chiplet comprises a first PHY region including conductor structures for chiplet-to-chiplet communications, and further wherein the second GPU chiplet comprises a second PHY region including conductor structures for chiplet-to-chiplet communications.
4. (Original) The system of claim 3, further comprising:
 - a third GPU chiplet communicably coupled to the first GPU chiplet via the passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications, wherein the third GPU chiplet comprises a third PHY region including conductor structures for chiplet-to-chiplet communications.
5. (Original) The system of claim 4, wherein the first PHY region of the first GPU chiplet comprises a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the first GPU chiplet.

6. (Original) The system of claim 4, wherein:
 - the second PHY region of the second GPU chiplet comprises a second passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the second GPU chiplet; and
 - the third PHY region of the third GPU chiplet comprises a third passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the third GPU chiplet.
7. (Original) The system of claim 1, wherein the passive crosslink communicably couples all GPU chiplets in the GPU chiplet array.
8. (Original) The system of claim 1, further comprising:
 - a first cache memory hierarchy at the first GPU chiplet, wherein a first level of the first cache memory hierarchy is coherent within the first GPU chiplet; and
 - a second cache memory hierarchy at the second GPU chiplet, wherein a first level of the second cache memory hierarchy is coherent within the second GPU chiplet.
9. (Original) The system of claim 8, further comprising:
 - a unified cache memory including both a last level of the first cache memory hierarchy and a last level of the second cache memory hierarchy, wherein the unified cache memory is coherent across all chiplets of the GPU chiplet array.
10. (Original) The system of claim 1, further comprising:
 - a plurality of conductive pillars coupling a circuit board substrate to a first non-PHY region of the first GPU chiplet and a second non-PHY region of the second GPU chiplet.
11. (Original) A method, comprising:
 - receiving, at a first GPU chiplet of a GPU chiplet array, a memory access request from a central processing unit (CPU);

determining, at a passive crosslink controller of the first GPU chiplet, a caching GPU chiplet corresponding to a location at which data associated with the memory access request is stored;

routing, via a passive crosslink dedicated for inter-chiplet communications in the GPU chiplet array, the memory access request to a last level cache of the caching GPU chiplet; and

returning data associated with the memory access request to the CPU.

12. (Original) The method of claim 11, wherein routing the memory access request further includes a scalable data fabric requesting data associated with the memory access request from the caching GPU chiplet.

13. (Original) The method of claim 11, wherein routing the memory access request to the last level cache of the caching GPU chiplet further comprises:

routing, based on determining the first GPU chiplet is the caching GPU chiplet, the memory access request via a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the first GPU chiplet.

14. (Original) The method of claim 11, wherein routing the memory access request to the last level cache of the caching GPU chiplet further comprises:

routing, based on determining a second GPU chiplet is the caching GPU chiplet, the memory access request via a second passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the second GPU chiplet.

15. (Original) The method of claim 11, further comprising:

returning data associated with the memory access request to the first GPU chiplet via a passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the caching GPU chiplet.

16. (Original) A non-transitory computer readable medium embodying a set of executable instructions, the set of executable instructions to manipulate at least one processor to:

receive, at a first GPU chiplet of a GPU chiplet array, a memory access request from a central processing unit (CPU);

determine, at a passive crosslink controller of the first GPU chiplet, a caching GPU chiplet corresponding to a location at which data associated with the memory access request is stored;

route, via a passive crosslink dedicated for inter-chiplet communications in the GPU chiplet array, the memory access request to a last level cache of the caching GPU chiplet; and

return data associated with the memory access request to the CPU.

17. (Original) The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to: request, via a scalable data fabric, data associated with the memory access request from the caching GPU chiplet.

18. (Original) The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:

route, based on determining the first GPU chiplet is the caching GPU chiplet, the memory access request via a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the first GPU chiplet.

19. (Original) The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:

route, based on determining a second GPU chiplet is the caching GPU chiplet, the memory access request via a second passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the second GPU chiplet.

20. (Original) The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:

return data associated with the memory access request to the first GPU chiplet via a passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the caching GPU chiplet.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 16/456,287		Filing Date 06/28/2019		☐ To be Mailed	
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO									
APPLICATION AS FILED - PART I									
		(Column 1)	(Column 2)						
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)		
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A				
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A				
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A				
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *		x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *		x \$460 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).							
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL				
APPLICATION AS AMENDED - PART II									
		(Column 1)		(Column 2)	(Column 3)				
AMENDMENT	02/25/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 20	Minus	** 20	= 0	x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)	(Column 3)				
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE			
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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/456,287	06/28/2019	Skyler J. SALEH	1458-190070

CONFIRMATION NO. 4820

PUBLICATION NOTICE



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109712
 Advanced Micro Devices, Inc.
 c/o Davidson Sheehan LLP
 6836 Austin Center Blvd.
 Suite 320
 Austin, TX 78731

Title:GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

Publication No.US-2020-0409859-A1

Publication Date:12/31/2020

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The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

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Doc code: IDS

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PTO/SB/08a (02-18)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		16456287
	Filing Date		2019-06-28
	First Named Inventor		Skyler J. SALEH
	Art Unit		2139
	Examiner Name	Reginald Glenwood BRAGDON	
	Attorney Docket Number		1458-190070

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	2	20120330802	A1	2012-12-27	GUTHRIE et al.	
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Art Unit	2139	
Examiner Name	Reginald Glenwood BRAGDON	
Attorney Docket Number	1458-190070	

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	1	International Search Report and Written Opinion for counterpart Application No. PCT/US2020/039326 dated October 13, 2020, 10 pages.	
	2	AKHIL ARUNKUMAR et al., "MCM-GPU: Multi-Chip-Module GPUs for Continued Performance Scalability", 2017 [retrieved on 2019.10.05]. Retrieved from <URL: https://research.nvidia.com/sites/default/files/publications/SCA_2017_MCMGPU.pdf >	
	3	JIEMING YIN et al., "Modular Routing Design for Chiplet-based Systems", pp. 726-738, 2018 [retrieved on 2019.10.05]. Retrieved from <URL: https://www.eecg.utoronto.ca/~enright/modular-isca.pdf >	

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(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2139
Examiner Name	Reginald Glenwood BRAGDON
Attorney Docket Number	1458-190070

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Adam D. Sheehan/	Date (YYYY-MM-DD)	2020-10-29
Name/Print	Adam D. Sheehan	Registration Number	42146

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To:

SHEEHAN, Adam D.

Davidson Sheehan LLP 6836 Austin Center Blvd., Suite 320
Austin, Texas 78731 USA

PCT

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THE WRITTEN OPINION OF THE INTERNATIONAL
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(PCT Rule 44.1)

Date of mailing
(day/month/year) 13 October 2020 (13.10.2020)Applicant's or agent's file reference
190070-PCT**FOR FURTHER ACTION** See paragraphs 1 and 4 belowInternational application No.
PCT/US2020/039326International filing date
(day/month/year) **24 June 2020 (24.06.2020)**

Applicant

ADVANCED MICRO DEVICES, INC.

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:

The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.**How?** Directly to the International Bureau of WIPO preferably through ePCT or on paper to, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70**For more detailed instructions, see** *PCT Applicant's Guide*, International Phase, paragraphs 9.004 - 9-011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:
☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. Reminders

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. These comments will be made available to the public after international publication. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90bis.1 and 90bis.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices. In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months. For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Within **22 months** from the priority date, the applicant may request that a supplementary international search be carried out by a different International Searching Authority, that offers this service (Rule 45bis.1). The procedure for requesting supplementary international search is described in the *PCT Applicant's Guide*, International Phase, paragraphs 8.006-8.032.

Name and mailing address of the ISA/KR

International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon, 35208, Republic of Korea

Facsimile No. 82-42-481-8578

Authorized officer

COMMISSIONER

Telephone No. 82-42-481-5571



* Attention

Copies of the documents cited in the international search report can be searched in the following Korean Intellectual Property Office English website for six months(expire date : **2021.04.13**) from the date of mailing of the international search report.

<http://www.kipo.go.kr/en/> => PCT ISA Portal => PCT Status

ID : PCT international application number

PW : **Y26PWRUR@**

Inquiries related to PCT International Search Report or Written Opinion prepared by KIPO as an International Searching Authority can be answered not only by KIPO but also through IPKC (Intellectual Property Korea Center), located in Vienna, VA, which functions as a PCT Help Desk for PCT applicants.

Homepage: <http://www.ipkcenter.com>

Email: ipkc@ipkcenter.com

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 190070-PCT	FOR FURTHER ACTION see Form PCT/ISA/220 as well as, where applicable, item 5 below.	
International application No. PCT/US2020/039326	International filing date (<i>day/month/year</i>) 24 June 2020 (24.06.2020)	(Earliest) Priority Date (<i>day/month/year</i>) 28 June 2019 (28.06.2019)
Applicant ADVANCED MICRO DEVICES, INC.		

This International search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 3 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**

a. With regard to the **language**, the international search was carried out on the basis of :

- ☒ the international application in the language in which it was filed
☐ a translation of the international application into _____, which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6bis(a)).

c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.

2. ☐ **Certain claims were found unsearchable** (See Box No. II)

3. ☐ **Unity of invention is lacking** (See Box No. III)

4. With regard to the **title**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established by this Authority to read as follows:

5. With regard to the **abstract**,

- ☒ the text is approved as submitted by the applicant.
☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.

6. With regard to the **drawings**,

- a. the figure of the **drawings** to be published with the abstract is Figure No. 1
☒ as suggested by the applicant.
☐ as selected by this Authority, because the applicant failed to suggest a figure.
☐ as selected by this Authority, because this figure better characterizes the invention.
- b. ☐ none of the figures is to be published with the abstract.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US2020/039326**A. CLASSIFICATION OF SUBJECT MATTER****G06F 15/78(2006.01)i, G06F 15/173(2006.01)j, G06F 12/0811(2016.01)i, G06F 13/16(2006.01)i**

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

G06F 15/78; G06F 12/08; G06Q 30/00; H01L 21/683; H01L 23/538; H01P 1/208; H01P 3/16; G06F 15/173; G06F 12/0811; G06F 13/16

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Korean utility models and applications for utility models

Japanese utility models and applications for utility models

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

eKOMPASS(KIPO internal) & Keywords: GPU (graphics processing unit), chiplet array, inter, communication, crosslink, cache

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 2019-0089036 A1 (INTEL CORPORATION) 21 March 2019 paragraphs [0035], [0038]-[0039], [0044], [0047]; claims 13, 18-19; and figures 3-6	1-4, 7, 10
Y		8
A		5-6, 9, 11-20
Y	US 2012-0330802 A1 (GUY L. GUTHRIE et al.) 27 December 2012 paragraphs [0016]-[0017]; and figure 1	8
A	US 2018-0130751 A1 (X-CELEPRINT LIMITED) 10 May 2018 paragraph [0069]; claim 11; and figure 1A	1-20
A	JIEMING YIN et al., 'Modular Routing Design for Chiplet-based Systems', pp. 726-738, 2018 [retrieved on 2019.10.05]. Retrieved from <URL: https://www.ee.utoronto.ca/~enright/modular-isca.pdf > section 2	1-20
A	AKHIL ARUNKUMAR et al., 'MCM-GPU: Multi-Chip-Module GPUs for Continued Perfo rmance Scalability', 2017 [retrieved on 2019.10.05]. Retrieved from <URL: https://research.nvidia.com/sites/default/files/publications/ISCA_2017_MCMGPU.pdf > section 3	1-20



Further documents are listed in the continuation of Box C.



See patent family amex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"D" document cited by the applicant in the international application

"E" earlier application or patent but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search

12 October 2020 (12.10.2020)

Date of mailing of the international search report

13 October 2020 (13.10.2020)

Name and mailing address of the ISA/KR

International Application Division

Korean Intellectual Property Office

189 Cheongsa-ro, Seo-gu, Daejeon, 35208, Republic of Korea



Facsimile No. +82-42-481-8578

Authorized officer

YANG JEONG ROK

Telephone No. +82-42-481-5709



INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.

PCT/US2020/039326

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2019-0089036 A1	21/03/2019	None	
US 2012-0330802 A1	27/12/2012	US 8683160 B2	25/03/2014
US 2018-0130751 A1	10/05/2018	US 10418331 B2	17/09/2019
		US 2012-0126229 A1	24/05/2012
		US 9899329 B2	20/02/2018

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43bis.1)

To:
SHEEHAN, Adam D.

Davidson Sheehan LLP 6836 Austin Center Blvd., Suite 320
Austin, Texas 78731 USA

Date of mailing
(day/month/year) **13 October 2020 (13.10.2020)**

Applicant's or agent's file reference
190070-PCT

FOR FURTHER ACTION

See paragraph 2 below

International application No. PCT/US2020/039326	International filing date (day/month/year) 24 June 2020 (24.06.2020)	Priority date(day/month/year) 28 June 2019 (28.06.2019)
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International Patent Classification (IPC) or both national classification and IPC

G06F 15/78(2006.01)i, G06F 15/173(2006.01)i, G06F 12/0811(2016.01)i, G06F 13/16(2006.01)i

Applicant
ADVANCED MICRO DEVICES, INC.

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43bis. I(a)(i) with regard to novelty, inventive step and industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1bis(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/KR
International Application Division
Korean Intellectual Property Office
189 Cheongsu-ro, Seo-gu, Daejeon,
35208, Republic of Korea
Facsimile No. +82-42-481-8578



Date of completion of this opinion

12 October 2020 (12.10.2020)

Authorized officer

YANG JEONG ROK

Telephone No. +82-42-481-5709



**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2020/039326

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of :

- ☒ the international application in the language in which it was filed
- ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b))

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(b))

3. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing:

- a. ☐ forming part of the international application as filed:
- ☐ in the form of an Annex C/ST.25 text file.
- ☐ on paper or in the form of an image file.
- b. ☐ furnished together with the international application under PCT Rule 13*ter*.1(a) for the purposes of international search only in the form of an Annex C/ST.25 text file.
- c. ☐ furnished subsequent to the international filing date for the purposes of international search only:
- ☐ in the form of an Annex C/ST.25 text file (Rule 13*ter*.1(a)).
- ☐ on paper or in the form of an image file (Rule 13*ter*.1(b) and Administrative Instructions, Section 713).

4. ☐ In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that forming part of the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.

PCT/US2020/039326

Box No. V Reasoned statement under Rule 43bis.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. Statement

Novelty (N)	Claims	1-20	YES
	Claims	NONE	NO
Inventive step (IS)	Claims	5-6,9,11-20	YES
	Claims	1-4,7-8,10	NO
Industrial applicability (IA)	Claims	1-20	YES
	Claims	NONE	NO

2. Citations and explanations :

Reference is made to the following documents:

D1: US 2019-0089036 A1 (INTEL CORPORATION) 21 March 2019

D2: US 2012-0330802 A1 (GUY L. GUTHRIE et al.) 27 December 2012

D3: US 2018-0130751 A1 (X-CELEPRINT LIMITED) 10 May 2018

D4: JIEMING YIN et al., 'Modular Routing Design for Chiplet-based Systems', pp. 726-738, 2018

D5: AKHIL ARUNKUMAR et al., 'MCM-GPU: Multi-Chip-Module GPUs for Continued Performance Scalability', 2017

I. Novelty and Inventive Step (PCT Article 33(2) and (3))

1. Claims 1-10

1.1. Claim 1

D1, which is considered to be the closest prior art to the subject matter of claim 1, discloses a computing device comprising: a processor that includes a plurality of chiplets, such as a general processing unit (GPU), respective ones of the chiplets physically and communicatively coupled with an on-chip dielectric waveguide including a substrate, a waveguide material disposed within the substrate, wave launchers (see paragraphs [0035], [0038]; claim 13; and figures 3-6), wherein a first chiplet of the plurality of chiplets is to communicate with a second chiplet of the plurality of chiplet by a radio frequency (RF) signal that propagates through the on-chip dielectric waveguide and the on-chip dielectric waveguide is physically coupled with a package substrate by one or more interconnects (see paragraphs [0038]-[0039]; claim 13; and figures 3-6).

Claim 1 differs from D1 in that it further comprises a GPU chiplet array includes a first

Continued on Supplemental Box

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2020/039326

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of : Box No. V

GPU chiplet [106-1] communicably coupled to the CPU via a bus [108]. However, the different feature is merely a variation of the disclosure of D1 (see claim 19: "The first chiplet is physically coupled with a package substrate by one or more interconnects.").

It would have been obvious to a person skilled in the art to arrive at the matter defined in claim 1 over D1. Therefore, claim 1 lacks an inventive step.

1.2. Claims 2-10

The additional feature of claim 2 would be easily derived from the disclosure of D1 (see paragraph [0047]; and figure 5: "The on-chip waveguide may be used as an interposer.").

The additional features of claims 3-4 would be easily derived from the disclosure of D1 (see paragraph [0044]; and figure 4: "The chiplets 420 may include a "front-side" 455. The front-side of the chiplet 420 may be the portion of the chiplet 420 wherein communication or logic components are located.").

The additional feature of claim 7 would be easily derived from the disclosure of D1 (see paragraph [0039]; and figure 3: "In this manner, the chiplets 320 may be communicatively coupled with one another by the interconnects 350, the vias 335, the interconnects 340, and the on-chip waveguide 300. Additionally, use of the on-chip waveguide 300 may allow communication between the chiplets 320 in the high-frequency range discussed above such as on the order of several hundred GHz, a THz, or above.").

The additional feature of claim 10 would be easily derived from the disclosure of D1 (see claim 18: "The on-chip dielectric waveguide is physically coupled with a package substrate by one or more interconnects.").

The additional feature of claim 8 would be easily derived from the disclosure of D2 (see paragraphs [0016]-[0017]; and figure 1: "A data processing system 10 includes multiple chiplets 11a-11n coupled to a system memory 21 and various input/output (I/O) devices 22 via a system fabric 20. " and "Chiplet 11a includes a processor core 12 having an instruction fetching unit (IFU) 13 and a load/store unit (LSU) 14, a level-2 (L2) cache 15, and a level-3 cache 16.").

Continued on The Next Page

**WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY**

International application No.
PCT/US2020/039326

Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of : Previous Page

The additional features of claims 5-6, 9 are not disclosed in any of the documents, nor are they obvious to a person skilled in the art over the documents individually or in combination.

Therefore, claims 2-4, 7, 10 lack an inventive step as being obvious over D1, claim 8 lacks an inventive step as being obvious over D1 in view of D2, and claims 5-6, 9 are novel and involve an inventive step.

2. Claims 11-15

None of the cited documents discloses the features of claim 11: "routing, via passive crosslink [118] dedicated for inter-chiplet communications in a GPU chiplet array, a memory access request to a last level cache [310] of a caching GPU chiplet." And it is not obvious to a person skilled in the art from the cited documents, when taken individually or in any combination.

Claims 12-15 are dependent on claim 11.

Therefore, claims 11-15 are novel and involve an inventive step.

3. Claims 16-20

Claim 16 relates to a non-transitory computer readable medium and has substantially the same technical features as claim 11. Accordingly, the same reasoning as in claim 11 can be applied to claim 16.

Claims 17-20 are dependent on claim 16.

Therefore, claims 16-20 are novel and involve an inventive step.

II. Industrial Applicability (PCT Article 33(4))

Claims 1-20 are industrially applicable.

Electronic Acknowledgement Receipt

EFS ID:	40986605
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Adam D. Sheehan/Brenda Thom
Filer Authorized By:	Adam D. Sheehan
Attorney Docket Number:	1458-190070
Receipt Date:	29-OCT-2020
Filing Date:	28-JUN-2019
Time Stamp:	16:13:22
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
------------------------	----

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	190070_IDS2.pdf	1007075	no	4
			804d63bfd6b0c82e4889dcc31303540eacbc911		

Warnings:

Information:									
2	Non Patent Literature	190070PCTISRWO.pdf	1538976	no	10				
			ff7e1e46906ad6ded2f950b783e95ae7614bd4cb						
Warnings:									
Information:									
3	Non Patent Literature	ISCA_2017_MCMGPU.pdf	2734164	no	13				
			f32ee96694dbf9f6db54cb4aa1d2e716bf677318						
Warnings:									
Information:									
4	Non Patent Literature	modular-isca.pdf	1126947	no	13				
			8745635f23a0ba7039f224ca2a314e51d3013b8b						
Warnings:									
Information:									
Total Files Size (in bytes):			6407162						
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.									



UNITED STATES PATENT AND TRADEMARK OFFICE

 UNITED STATES DEPARTMENT OF COMMERCE
 United States Patent and Trademark Office

Address: COMMISSIONER FOR PATENTS

 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
16/456,287	06/28/2019	Skyler J. SALEH	1458-190070	4820
109712	7590	09/11/2020	EXAMINER	
Advanced Micro Devices, Inc.			YU, JAE UN	
c/o Davidson Sheehan LLP			ART UNIT	
6836 Austin Center Blvd.			PAPER NUMBER	
Suite 320			2135	
Austin, TX 78731			NOTIFICATION DATE	
			DELIVERY MODE	
			09/11/2020	
			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

AMD@DS-patent.com
 docketing@ds-patent.com

Office Action Summary	Application No. 16/456,287	Applicant(s) SALEH et al.	
	Examiner JAE U YU	Art Unit 2135	AIA (FITF) Status Yes

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 6/28/19.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-20 is/are pending in the application.
5a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) _____ is/are allowed.
- 7) ☒ Claim(s) 1-8 and 10-20 is/are rejected.
- 8) ☒ Claim(s) 9 is/are objected to.
- 9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☐ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 6/28/19 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date 6/28/19.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
- 4) ☐ Other: _____.

DETAILED ACTION

Notice of Pre-AIA or AIA Status

The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a)(1) the claimed invention was patented, described in a printed publication, or in public use, on sale, or otherwise available to the public before the effective filing date of the claimed invention.

1. Claims 1-4, 7, and 10 are rejected under 35 U.S.C. 102(a)(1) as being anticipated by Teig et al. (US 2019/0123022), “Teig”.

2. As per **claim 1**, Teig discloses a central processing unit (CPU) [**CPU, figure 9**] communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array [**GPU, figure 9**], wherein the GPU chiplet array includes: the first GPU chiplet [**GPU cores, figure 9**] communicably coupled to the CPU via a bus [**CPU cores, figure 9**]; and a second GPU chiplet [**GPU cores, figure 9**] communicably coupled to the first GPU chiplet via a passive crosslink [**CPU cores, figure 9**], wherein the passive crosslink is dedicated for inter-chiplet communications [**a passive interposer, paragraph 148**].

3. As per **claim 2**, Teig discloses wherein the passive crosslink comprises a passive interposer die [**a passive interposer, paragraph 148**].

4. As per **claim 3**, Teig discloses wherein the first GPU chiplet comprises a first PHY region including conductor structures for chiplet-to-chiplet communications, and further wherein the second GPU chiplet comprises a second PHY region including conductor structures for chiplet-to-chiplet communications [**passive interposers, paragraph 148**].
5. As per **claim 4**, Teig discloses a third GPU chiplet communicably coupled to the first GPU chiplet via the passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications, wherein the third GPU chiplet comprises a third PHY region including conductor structures for chiplet-to-chiplet communications [**passive interposers, paragraph 148**].
6. As per **claim 7**, Teig discloses wherein the passive crosslink communicably couples all GPU chiplets in the GPU chiplet array [**passive interposers, paragraph 148**].
7. As per **claim 10**, Teig discloses a plurality of conductive pillars coupling a circuit board substrate to a first non-PHY region of the first GPU chiplet and a second non-PHY region of the second GPU chiplet [**z-axis interconnects, figure 16**].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent for a claimed invention may not be obtained, notwithstanding that the claimed invention is not identically disclosed as set forth in section 102, if the differences between the claimed invention and the prior art are such that the claimed invention as a whole would have been obvious before the effective filing date of the claimed invention to a person having ordinary skill in the art to which the claimed invention pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claims 5, 6, 8, and 11-20 are rejected under 35 U.S.C. 103 as being unpatentable over Teig et al. (US 2019/0123022), "Teig", in view of Yasuda et al. (US 2001/0005873), "Yasuda".

2. As per **claims 5, 6, and 8**, Teig discloses the system recited in claims 1 and 4.

Teig does not disclose expressly a last level cache.

Yasuda discloses cache coherency protocol in the abstract.

Teig and Yasuda are analogous art because they are from the same field of endeavor of storage device.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Teig by including the cache coherency protocol as taught by Yasuda in the abstract.

The motivation for doing so would have been better addressing performance as expressly taught by Yasuda in paragraph 19.

3. As per **claims 11-20**, the examiner directs the applicant's attention to claims rejection above.

Conclusion

A. Allowable Subject Matter

Claim 9 is objected to.

The primary reasons for allowance of claim 9 in the instant application is the combination with the inclusion in these claims that "a unified cache memory including both a last level of the first cache memory hierarchy and a last level of the second cache memory hierarchy, wherein the unified cache memory is coherent across all chiplets of the GPU chiplet array". The prior art of record neither anticipates nor renders obvious the above recited combination.

As allowable subject matter has been indicated, applicant's response must either comply with all formal requirements or specifically traverse each requirement not complied with. See 37 C.F.R. § 1.111(b) and § 707.07(a) of the MPEP.

B. Claims Rejected

Claims 1-8 and 10-20 are rejected.

C. Direction for Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAE UN YU whose telephone number is (571)272-1133. The examiner can normally be reached on M-F 9-5.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <https://ppair-my.uspto.gov/pair/PrivatePair>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Application/Control Number: 16/456,287
Art Unit: 2135

Page 6

/JAE U YU/
Primary Examiner, Art Unit 2135

<i>Notice of References Cited</i>	Application/Control No. 16/456,287	Applicant(s)/Patent Under Reexamination SALEH et al.	
	Examiner JAE U YU	Art Unit 2135	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20010005873-A1	06-2001	Yasuda, Yoshiko	G06F12/0813	710/305
*	B	US-20190123022-A1	04-2019	Teig; Steven L.	H01L24/32	1/1
	C					
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FOREIGN PATENT DOCUMENTS

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	N					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)

Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 16/456,287	Applicant(s)/Patent Under Reexamination SALEH et al.
	Examiner JAE U YU	Art Unit 2135

CPC - Searched*		
Symbol	Date	Examiner

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Text Search in EAST	09/08/2020	/J.U.Y/
Inventor Search in EAST and Palm	09/08/2020	/J.U.Y/
PLUS	09/08/2020	/J.U.Y/
NPL Search	09/08/2020	/J.U.Y/

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

/J.U.Y/ Primary Examiner, Art Unit 2135	
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<i>Index of Claims</i> 	Application/Control No. 16/456,287	Applicant(s)/Patent Under Reexamination SALEH et al.
	Examiner JAE U YU	Art Unit 2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

[illegible]

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	244	gpu near7 cpu near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 15:03
L2	410	gpu with cpu with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 15:03
L3	2,120	(cach\$3 near5 coheren\$4).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:01
L4	151	gpu same cpu same cach\$3 same (level\$2 low\$3 "l2" level-2) and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:01
L5	901	(cach\$3 near5 coheren\$4).ti. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:02
L6	1,550	(cach\$3 near5 coheren\$4).ab. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/08 16:02
L7	66	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 near7 (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31
L8	918	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31

L9	94	gpu with (coheren\$4 dirty invalid\$4) with cach\$3 with (level\$2 low\$3 "l2" level-2)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:31
L10	35	gpu near7 (coheren\$4 dirty invalid\$4) near7 cach\$3 and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 16:32
L11	126	gpu near7 cpu near7 cach\$3 near7 (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:22
L12	178	gpu with cpu with cach\$3 with (coheren\$4 dirty invalid\$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:23
L13	123	("8645640" "8650367" "8683160" "9372797" "9858188" "10331563" "20120330802" "20120330803" "20120331231" "20150227464" "20150269076" "20180052771" "20190266093" "8125418" "8207954" "8279145" "8456387" "8497821" "8698391" "8803857" "9070323" "9492993" "10468363" "20100123694" "20100207848" "20100207849" "20100207851" "20100265224" "20100277440" "20100328196" "20120206499" "20150251402" "20170048976" "20190371753" "20200051961" "20200105697" "10295588" "20180180665" "8679861" "8796047" "20100015732" "20140159803" "20190243700" "5663854" "5963397" "6049443" "6425109" "6966042" "7243325" "7733127").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:24
L14	73	gpu near7 cpu near7 cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:26

L15	131	gpu with cpu with cach\$3 and (amd "advanced micro").asnm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:26
L16	39	(SALEH near2 SKYLER).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:31
L17	446	(NAFFZIGER near2 SAMUEL).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:31
L18	110	(BHAGAVAT near2 MILIND).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:32
L19	163	(AGARWAL near2 RAHUL).in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/08 17:33
S1	7,783	(711/118).CCLS.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2020/09/07 19:15
S2	184	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:17
S3	0	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab. and 711/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:18
S4	0	(cpu near5 gpu\$2 near5 (second\$3 plurality)).ab. and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20

S5	0	(cpu near5 gpu\$2).ab. and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20
S6	28	(cpu near5 gpu\$2) and "passive interposer"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO	OR	OFF	2020/09/07 19:20

9/8/2020 6:15:18 PM

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BIB DATA SHEET

CONFIRMATION NO. 4820

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
16/456,287	06/28/2019	711	2135	1458-190070		
RULE						
APPLICANTS ADVANCED MICRO DEVICES, INC., Santa Clara, CA; INVENTORS Skyler J. SALEH, San Diego, CA; Samuel NAFFZIGER, Fort Collins, CO; Milind S. BHAGAVAT, Santa Clara, CA; Rahul AGARWAL, Santa Clara, CA; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 07/11/2019						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☐ No Verified and Acknowledged <u>/JAE UN YU/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 6	TOTAL CLAIMS 20	INDEPENDENT CLAIMS 3
ADDRESS Advanced Micro Devices, Inc. c/o Davidson Sheehan LLP 6836 Austin Center Blvd. Suite 320 Austin, TX 78731 UNITED STATES						
TITLE GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS						
FILING FEE RECEIVED 1880	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit		

Doc code: IDS

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PTO/SB/08a (02-18)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16456287
	Filing Date	2019-06-28
	First Named Inventor	Skyler J. SALEH
	Art Unit	2139
	Examiner Name	Reginald Glenwood BRAGDON
	Attorney Docket Number	1458-190070

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /J.U.Y/

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2139
Examiner Name	Reginald Glenwood BRAGDON
Attorney Docket Number	1458-190070

1	J.S. Application No. 16/585,452 filed September 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190141).
2	J.S. Application No. 16/585,480 filed September 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190142).
3	J.S. Application No. 16/698,624 filed November 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190143).

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EXAMINER SIGNATURE

Examiner Signature	/JAE U YU/	Date Considered	09/08/2020
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2139
Examiner Name	Reginald Glenwood BRAGDON
Attorney Docket Number	1458-190070

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Adam D. Sheehan/	Date (YYYY-MM-DD)	2019-12-27
Name/Print	Adam D. Sheehan	Registration Number	42146

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PLUS Search Results for S/N 16456287, Searched Tue May 26 15:40:20 EDT 2020

The Patent Linguistics Utility System (PLUS) is a USPTO automated search system for U.S. Patents from 1971 to the present PLUS is a query-by-example search system which produces a list of patents that are most closely related linguistically to the application searched. This search was prepared by the staff of the Scientific and Technical Information Center, SIRA.

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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (02-18)

Approved for use through 11/30/2020. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	16456287
	Filing Date	2019-06-28
	First Named Inventor	Skyler J. SALEH
	Art Unit	2139
	Examiner Name	Reginald Glenwood BRAGDON
	Attorney Docket Number	1458-190070

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		16456287
Filing Date		2019-06-28
First Named Inventor	Skyler J. SALEH	
Art Unit	2139	
Examiner Name	Reginald Glenwood BRAGDON	
Attorney Docket Number	1458-190070	

1	J.S. Application No. 16/585,452 filed September 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190141).
2	J.S. Application No. 16/585,480 filed September 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190142).
3	J.S. Application No. 16/698,624 filed November 27, 2019 in the name of Skyler J. SALEH, et al. (Docket No. 1458-190143).

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	16456287
Filing Date	2019-06-28
First Named Inventor	Skyler J. SALEH
Art Unit	2139
Examiner Name	Reginald Glenwood BRAGDON
Attorney Docket Number	1458-190070

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Adam D. Sheehan/	Date (YYYY-MM-DD)	2019-12-27
Name/Print	Adam D. Sheehan	Registration Number	42146

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	38152187
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Adam D. Sheehan/Emily Stalder
Filer Authorized By:	Adam D. Sheehan
Attorney Docket Number:	1458-190070
Receipt Date:	27-DEC-2019
Filing Date:	28-JUN-2019
Time Stamp:	15:45:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	190070_IDS.pdf	1034370	no	4
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Warnings:

Information:

A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.

2	Non Patent Literature	09-27-19_190141_Application_ as_Filed.pdf	1222490	no	26
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Warnings:**Information:**

3	Non Patent Literature	09-27-19_190142_Application_ as_Filed.pdf	1094710	no	28
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Warnings:**Information:**

4	Non Patent Literature	11-27-19_190143_Application_ as_Filed.pdf	1487521	no	35
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Warnings:**Information:**

Total Files Size (in bytes):			4839091
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DECLARATION

Pursuant to an application entitled:

GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

which (check) ☐ is filed with this Declaration and marked with the above title and/or Attorney Docket Number, and which is the final application provided to me by Davidson Sheehan LLP
☐ and is amended by the Preliminary Amendment attached hereto.
☒ was filed on June 28, 2019 as United States Application or PCT International Application No. 16/456,287,

as a below named inventor, I hereby declare that:

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. §1001 by fine or imprisonment of not more than five (5) years, or both.

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the firm named below:

Customer Number 109712
Davidson Sheehan LLP
6836 Austin Center Blvd., Suite 320
Austin, TX 78731
Telephone: 512-582-2455
Facsimile: 512-355-1119

Legal name of first joint inventor: **Skyler J. SALEH**

Inventor's Signature: _____

Date: 7-3-2019

Legal name of second joint inventor: **Samuel NAFFZIGER**

Inventor's Signature: _____

Date: _____

DECLARATION

Pursuant to an application entitled:

GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

which (check) ☐ is filed with this Declaration and marked with the above title and/or Attorney Docket Number, and which is the final application provided to me by Davidson Sheehan LLP

☐ and is amended by the Preliminary Amendment attached hereto.

☒ was filed on June 28, 2019 as United States Application or PCT International Application No. 16/456,287,

as a below named inventor, I hereby declare that:

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. §1001 by fine or imprisonment of not more than five (5) years, or both.

Please direct all correspondence concerning this application to the USPTO Customer Number, if provided, or otherwise to the firm named below:

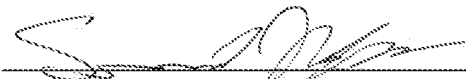
Customer Number 109712
Davidson Sheehan LLP
6836 Austin Center Blvd., Suite 320
Austin, TX 78731
Telephone: 512-582-2455
Facsimile: 512-355-1119

Legal name of first joint inventor: **Skyler J. SALEH**

Inventor's Signature: _____

Date: _____

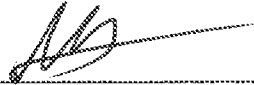
Legal name of second joint inventor: **Samuel NAFFZIGER**

Inventor's Signature:  _____

Date: 7/30/19

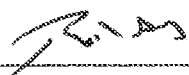
Attorney Docket No. 1458-190070

Legal name of third joint inventor: **Milind S. BHAGAVAT**

Inventor's Signature: 

Date: 7/8/19

Legal name of fourth joint inventor: **Rahul AGARWAL**

Inventor's Signature: 

Date: 7/8/19

Electronic Acknowledgement Receipt

EFS ID:	36754505
Application Number:	16456287
International Application Number:	
Confirmation Number:	4820
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS
First Named Inventor/Applicant Name:	Skyler J. SALEH
Customer Number:	109712
Filer:	Adam D. Sheehan/Danielle Haynes
Filer Authorized By:	Adam D. Sheehan
Attorney Docket Number:	1458-190070
Receipt Date:	01-AUG-2019
Filing Date:	28-JUN-2019
Time Stamp:	13:13:06
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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1	Oath or Declaration filed	190070_Declaration.pdf	114266	no	3
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Information:
Total Files Size (in bytes):

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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 P.O. Box 1450
 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
16/456,287	06/28/2019		1880	1458-190070	20	3

CONFIRMATION NO. 4820

FILING RECEIPT



0000000109377462

109712

Advanced Micro Devices, Inc.
 c/o Davidson Sheehan LLP
 6836 Austin Center Blvd.
 Suite 320
 Austin, TX 78731

Date Mailed: 07/15/2019

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Skyler J. SALEH, San Diego, CA;
 Samuel NAFFZIGER, Fort Collins, CO;
 Milind S. BHAGAVAT, Santa Clara, CA;
 Rahul AGARWAL, Santa Clara, CA;

Applicant(s)

ADVANCED MICRO DEVICES, INC., Santa Clara, CA;

Power of Attorney: None

Domestic Applications for which benefit is claimed - None.

A proper domestic benefit claim must be provided in an Application Data Sheet in order to constitute a claim for domestic benefit. See 37 CFR 1.76 and 1.78.

Foreign Applications for which priority is claimed (You may be eligible to benefit from the Patent Prosecution Highway program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 07/11/2019

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 16/456,287**

Projected Publication Date: 12/31/2020

Non-Publication Request: No

Early Publication Request: No

Title

GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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 Alexandria, Virginia 22313-1450
 www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
16/456,287	06/28/2019	Skyler J. SALEH	1458-190070

CONFIRMATION NO. 4820**INFORMAL NOTICE**

109712
 Advanced Micro Devices, Inc.
 c/o Davidson Sheehan LLP
 6836 Austin Center Blvd.
 Suite 320
 Austin, TX 78731

Date Mailed: 07/15/2019

INFORMATIONAL NOTICE TO APPLICANT

Applicant is notified that the above-identified application contains the deficiencies noted below. No period for reply is set forth in this notice for correction of these deficiencies. However, if a deficiency relates to the inventor's oath or declaration, the applicant must file an oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each actual inventor no later than the expiration of the time period set in the "Notice of Allowability" to avoid abandonment. See 37 CFR 1.53(f).

The item(s) indicated below are also required and should be submitted with any reply to this notice to avoid further processing delays.

- A properly executed inventor's oath or declaration has not been received for the following inventor(s):
 Skyler J. SALEH
 Samuel NAFFZIGER
 Milind S. BHAGAVAT
 Rahul AGARWAL

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at (571) 272-4000 or (571) 272-4200 or 1-888-786-0101.

/tnguyen/

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 16/456,287				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	300			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	660			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	760			
TOTAL CLAIMS (37 CFR 1.16(j))	20	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	3	minus 3 = *				x 460 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
			TOTAL			TOTAL	1720			
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2:

☐	Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
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Inventor Information:

Inventor	1				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Skyler	J.	SALEH			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
City	San Diego	State/Province	CA	Country of Residence	US	

Mailing Address of Inventor:

Address 1	2485 Augustine Drive					
Address 2						
City	Santa Clara	State/Province	CA			
Postal Code	95054	Country	US			

Inventor	2				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Samuel		NAFFZIGER			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						
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Address 2						
City	Santa Clara	State/Province	CA			
Postal Code	95054	Country	US			

Inventor	3				Remove	
Legal Name						
Prefix	Given Name	Middle Name	Family Name	Suffix		
	Milind	S.	BHAGAVAT			
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service						

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
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City	Santa Clara	State/Province	CA	Country of Residence	US
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Mailing Address of Inventor:

Address 1	2485 Augustine Drive				
Address 2					
City	Santa Clara	State/Province	CA		
Postal Code	95054	Country	US		
Inventor	4				Remove
Legal Name					

Prefix	Given Name	Middle Name	Family Name	Suffix	
	Rahul		AGARWAL		
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service					
City	Santa Clara	State/Province	CA	Country of Residence	US

Mailing Address of Inventor:

Address 1	2485 Augustine Drive				
Address 2					
City	Santa Clara	State/Province	CA		
Postal Code	95054	Country	US		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add					

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).			
☐ An Address is being provided for the correspondence information of this application.			
Customer Number	109712		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		
Attorney Docket Number	1458-190070	Small Entity Status Claimed	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	6	Suggested Figure for Publication (if any)	1

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number	109712		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status		Remove
Application Number	Continuity Type	Prior Application Number
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.		Add

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX)ⁱ the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.

NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant	1	Remove
If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section. Clear		
☒ Assignee	Legal Representative under 35 U.S.C. 117	Joint Inventor
Person to whom the inventor is obligated to assign.		Person who shows sufficient proprietary interest
If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:		
Name of the Deceased or Legally Incapacitated Inventor:		
If the Applicant is an Organization check here. ☒		
Organization Name	ADVANCED MICRO DEVICES, INC.	
Mailing Address Information For Applicant:		
Address 1	2485 Augustine Drive	
Address 2		
City	Santa Clara	State/Province
Country	US	Postal Code
Phone Number		Fax Number
Email Address		
Additional Applicant Data may be generated within this form by selecting the Add button. Add		

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

Assignee 1				
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.				
Remove				
If the Assignee or Non-Applicant Assignee is an Organization check here. ☐				
Prefix	Given Name	Middle Name	Family Name	Suffix
Mailing Address Information For Assignee including Non-Applicant Assignee:				
Address 1				
Address 2				
City		State/Province		
Country ⁱ		Postal Code		
Phone Number		Fax Number		
Email Address				
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button. Add				

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). However, if this Application Data Sheet is submitted with the **INITIAL** filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Allen Tomg/		Date (YYYY-MM-DD)	2019-06-28
First Name	Allen	Last Name	Tomg	Registration Number
				61298
Additional Signature may be generated within this form by selecting the Add button. Add				

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	1458-190070
		Application Number	
Title of Invention	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS		

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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100

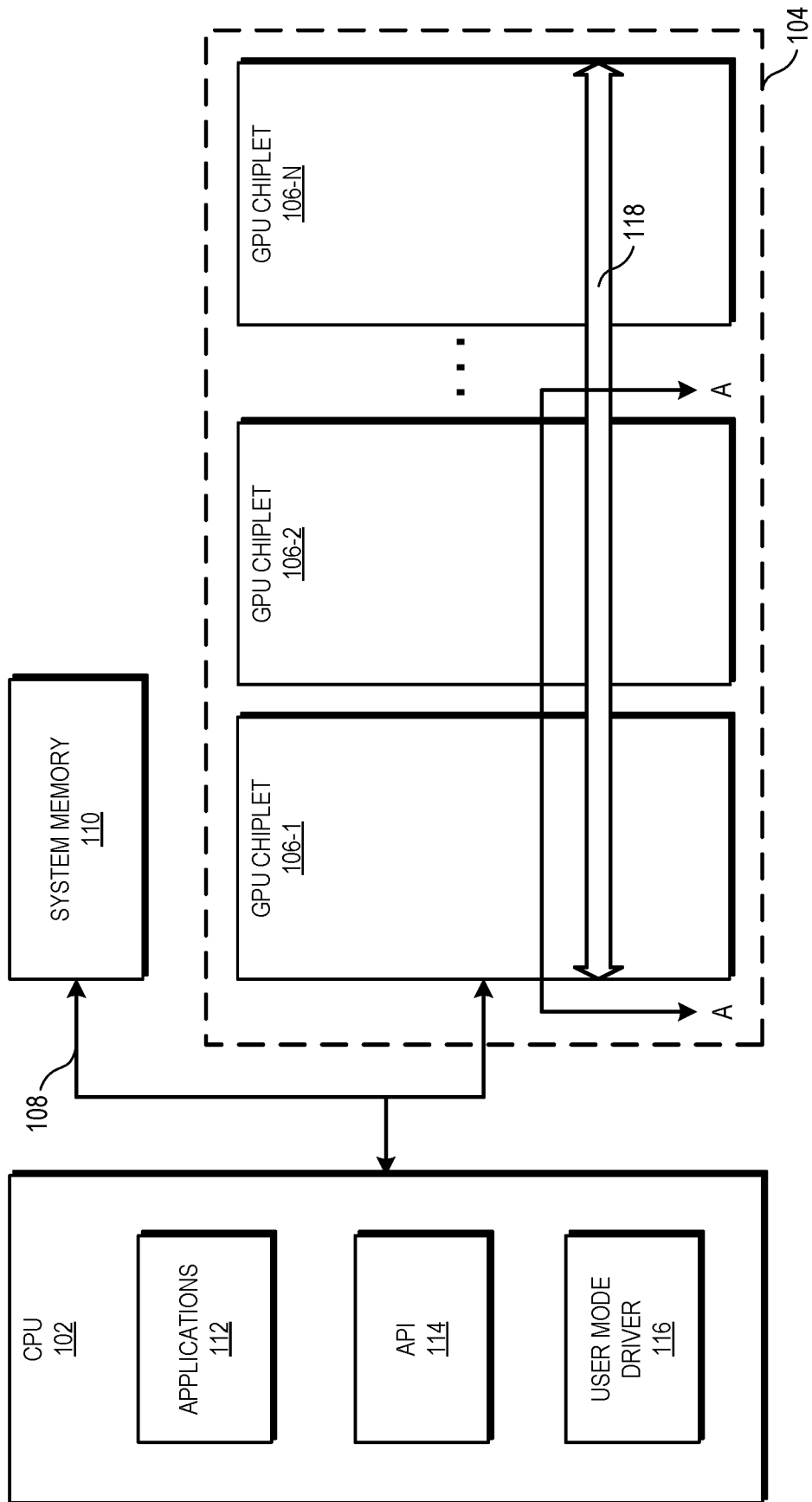


FIG. 1

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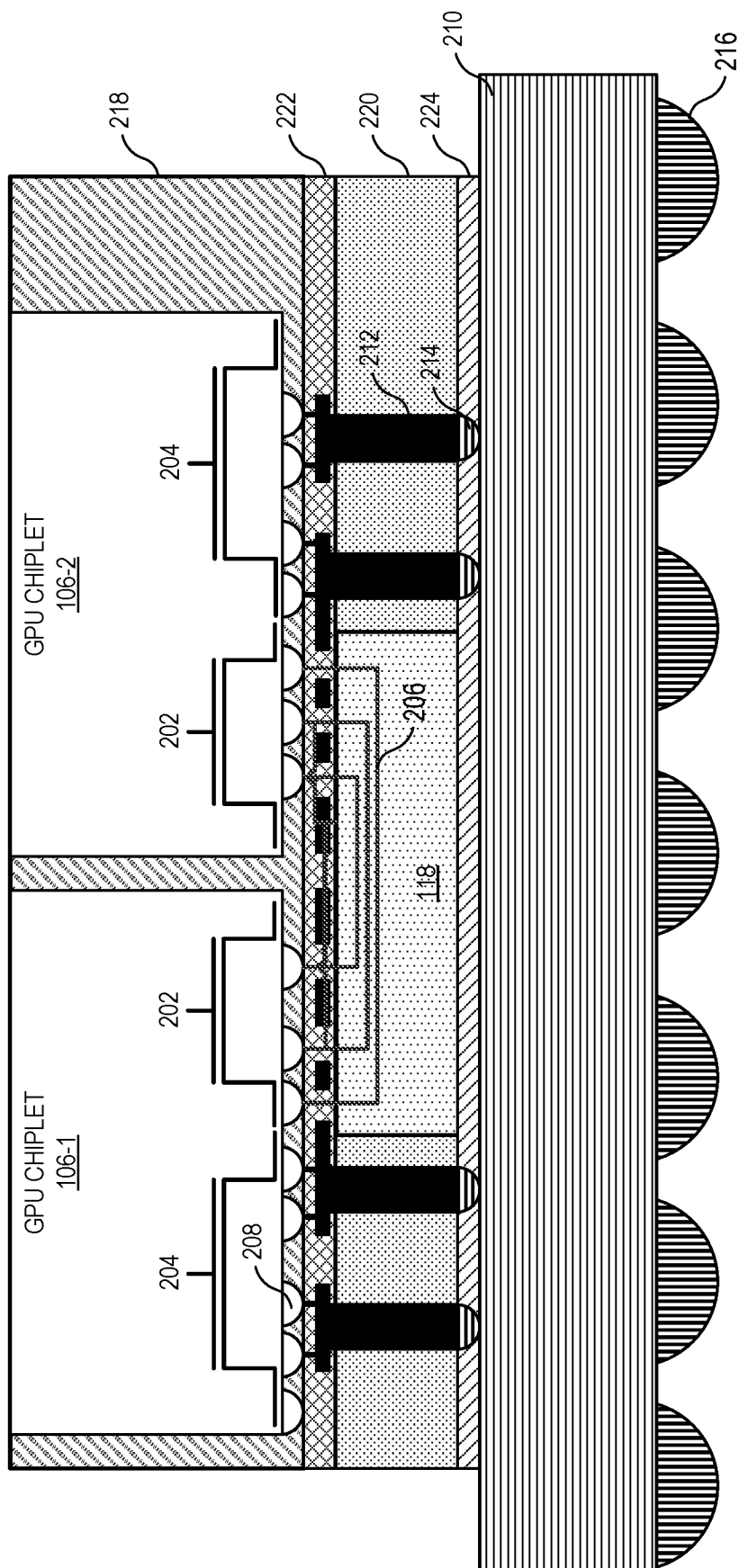


FIG. 2

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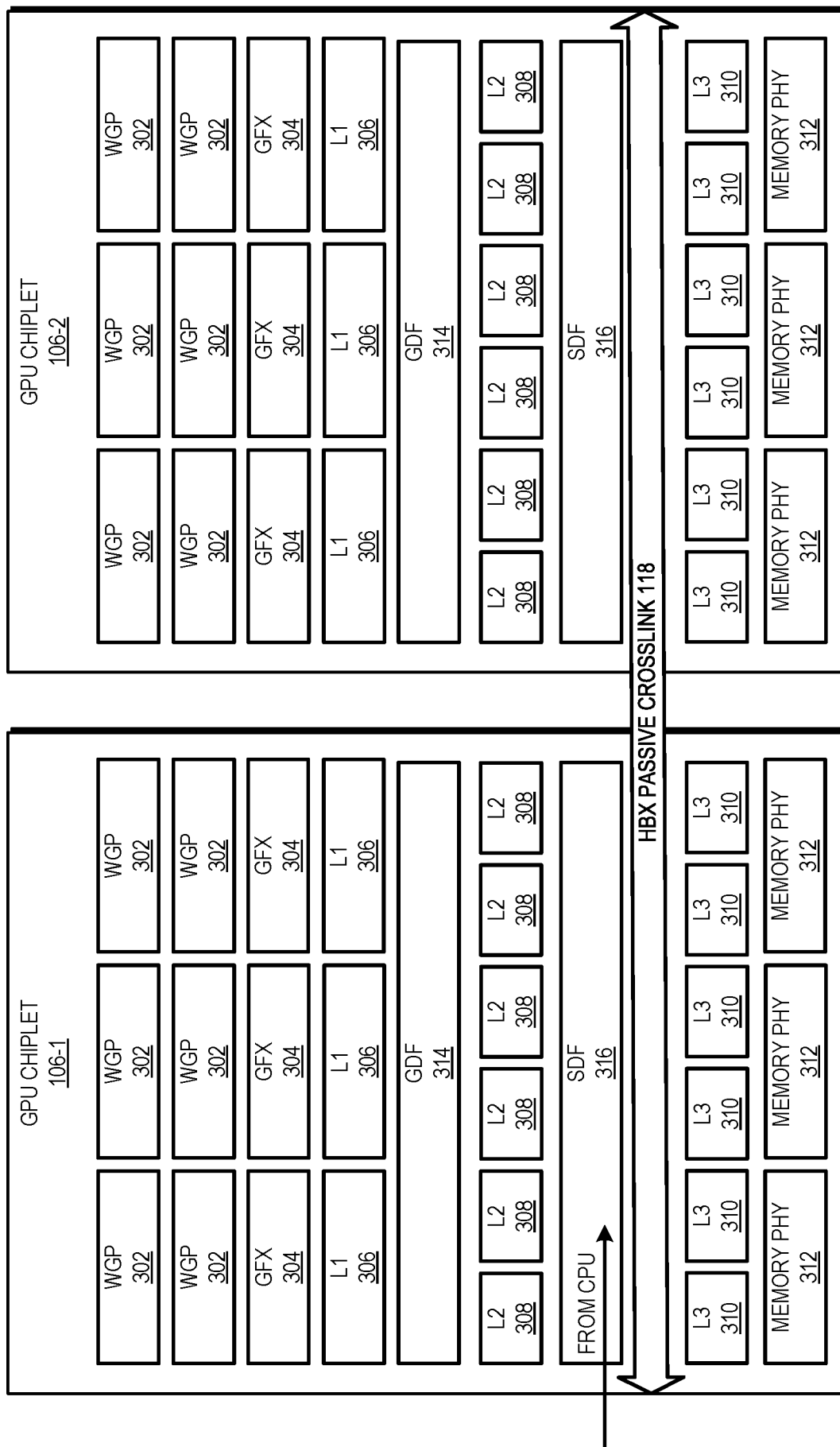


FIG. 3

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400



FIG. 4

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500

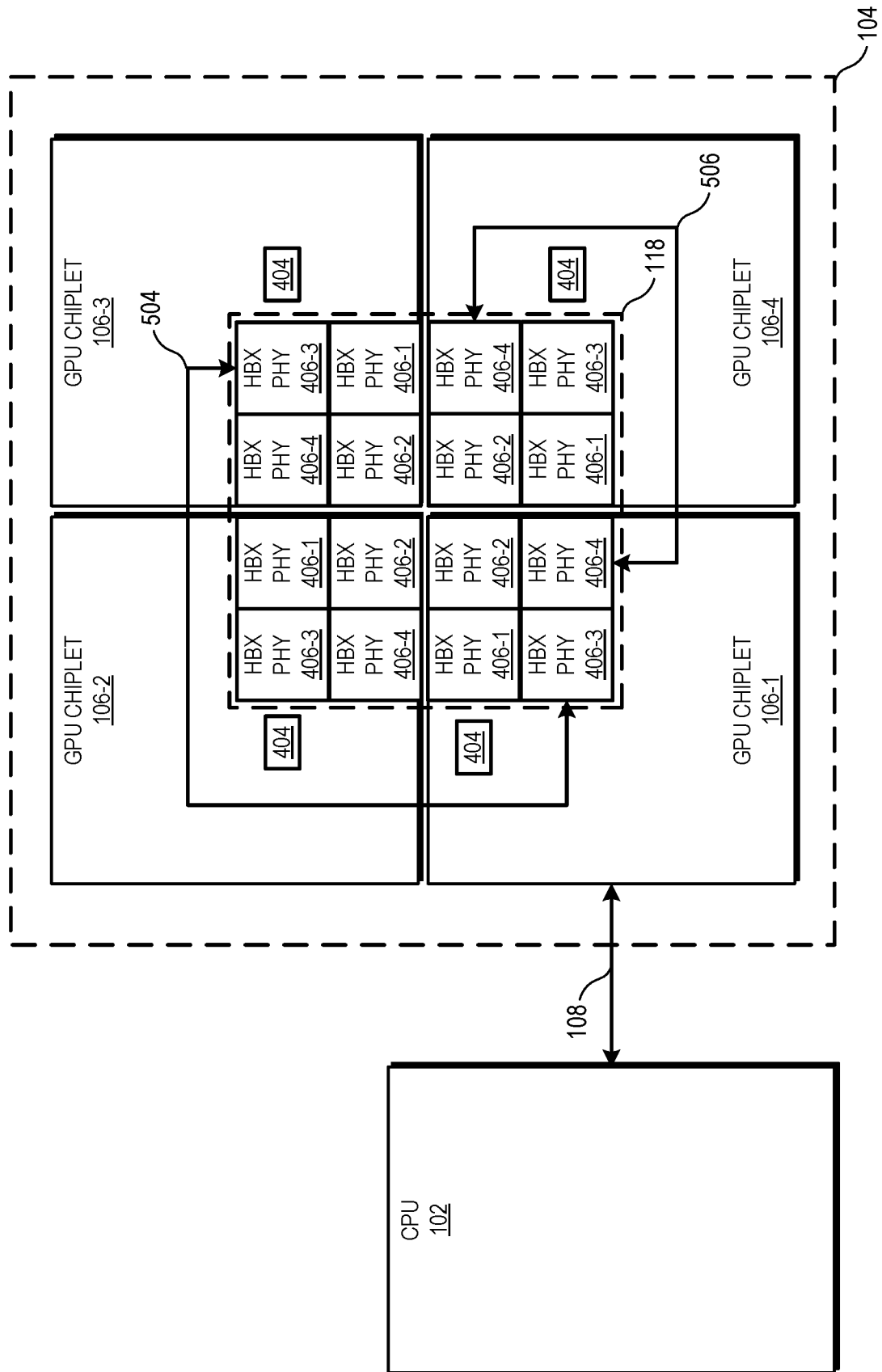


FIG. 5

6/6

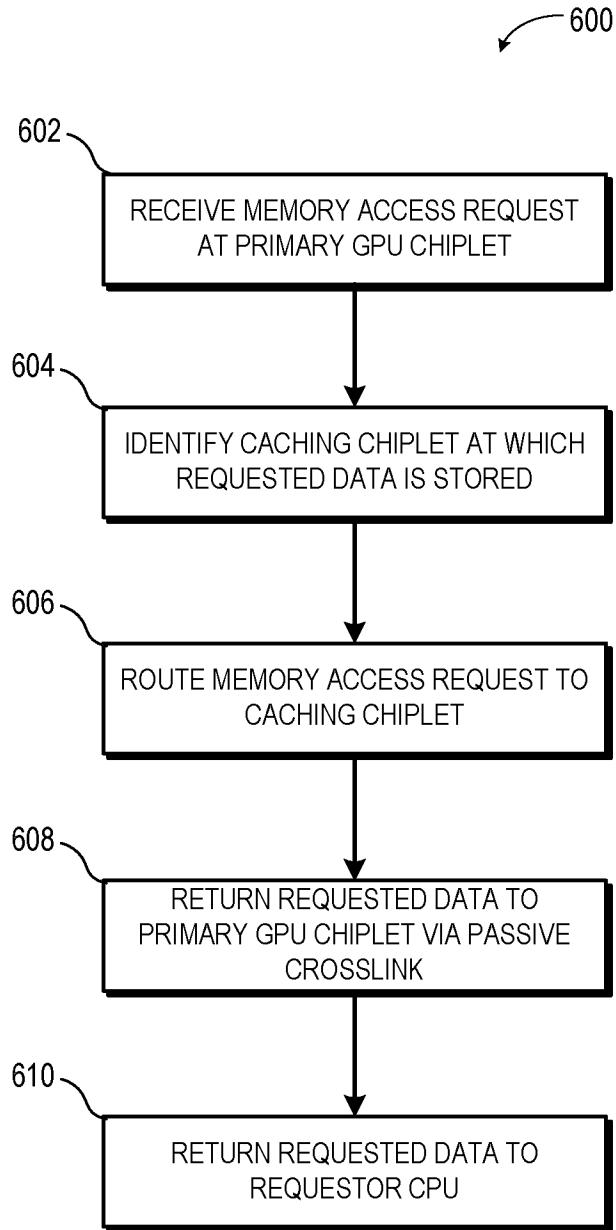


FIG. 6

GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS

BACKGROUND

[0001] Computing devices such as mobile phones, personal digital assistants (PDAs), digital cameras, portable players, gaming, and other devices requires the integration of more performance and features into increasingly smaller spaces. As a result, the density of processor dies and number of dies integrated within a single integrated circuit (IC) package have increased. Some conventional multi-chip modules include two or more semiconductor chips mounted side-by-side on a carrier substrate or in some cases on an interposer (so-called “2.5D”) that is, in-turn, mounted on a carrier substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0002] The present disclosure may be better understood, and its numerous features and advantages made apparent to those skilled in the art by referencing the accompanying drawings. The use of the same reference symbols in different drawings indicates similar or identical items.

[0003] FIG. 1 is a block diagram illustrating a processing system employing high bandwidth passive crosslinks for coupling GPU chiplets in accordance with some embodiments.

[0004] FIG. 2 is a block diagram illustrating a sectional view of GPU chiplets and passive crosslinks in accordance with some embodiments.

[0005] FIG. 3 is a block diagram illustrating a cache hierarchy of GPU chiplets coupled by a passive crosslink in accordance with some embodiments.

[0006] FIG. 4 is a block diagram illustrating a floor plan view of a GPU chiplet in accordance with some embodiments.

[0007] FIG. 5 is a block diagram illustrating a processing system utilizing a four-chiplet configuration in accordance with some embodiments.

[0008] FIG. 6 is a flow diagram illustrating a method of performing inter-chiplet communications in accordance with some embodiments.

DETAILED DESCRIPTION

[0009] Conventional monolithic die designs are becoming increasingly expensive to manufacture. Chiplets have been used successfully in CPU architectures to reduce cost of manufacture and improve yields, as its heterogeneous computational nature is more naturally suited to separate CPU cores into distinct units that do not require much inter-communication. GPU work by its nature includes parallel work. However, the geometry that a GPU processes includes not only sections of fully parallel work but also work that requires synchronous ordering between different sections. Accordingly, a GPU programming model that spreads sections of work on different threads is often inefficient because the parallelism is difficult to distribute across multiple different working groups and chiplets as it is difficult and expensive computational to synchronize the memory contents of shared resources throughout the entire system to provide a coherent view of the memory to applications. Additionally, from a logical point of view, applications are written with the view that the system only has a single GPU. That is, even though a conventional GPU includes many GPU cores, applications are programmed as addressing a single device. So, it has been historically challenging to bring chiplet design methodology to GPU architectures.

[0010] To improve system performance by using GPU chiplets while preserving the current programming model, FIGS. 1-6 illustrate systems and methods that utilize high bandwidth passive crosslinks for coupling GPU chiplets. In various embodiments, a system includes a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array. The GPU chiplet array includes the first GPU chiplet communicably coupled to the CPU via a bus and a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink. In various embodiments, the passive crosslink is a passive interposer die dedicated for inter-chiplet communications. The GPU chiplet breaks up systems-on-a-chip (SoC) into

smaller functional groupings referred to as “chiplets” that perform functions of the various cores of the SoC (e.g., a GPU).

[0011] Currently, various architectures already have at least one level of cache (e.g., L3 or other last level cache (LLC)) that is coherent across the entire conventional GPU die. Here, the chiplet-based GPU architecture positions those physical resources (e.g., LLC) on different dies and communicably couples those physical resources such that the LLC level is unified and remains cache coherent across all GPU chiplets. Thus, although operating in a massively parallel environment, the L3 cache level to be coherent. During operations, a memory address request from the CPU to the GPU is transmitted only to a single GPU chiplet, which then communicates with a high bandwidth passive crosslink to locate the requested data. From the CPU’s point of view, it appears to be addressing a single die, monolithic GPU. This allows for use of a large-capacity, multi-chiplet GPU that appears as a single device to an application.

[0012] FIG. 1 is a block diagram illustrating a processing system 100 employing high bandwidth passive crosslinks for coupling GPU chiplets in accordance with some embodiments. In the depicted example, the system 100 includes a central processing unit (CPU) 102 for executing instructions and an array 104 of one or more GPU chiplets, such as the three illustrated GPU chiplets 106-1, 106-2, and through 106-N (collectively, GPU chiplets 106). In various embodiments, and as used herein, the term “chiplet” refers to any device including, but is not limited to, the following characteristics: 1) a chiplet includes an active silicon die containing part of the computational logic used to solve a full problem (i.e., the computational workload is distributed across multiples of these active silicon dies); 2) chiplets are packaged together as a monolithic unit on the same substrate; and 3) the programming model preserves the concept that these separate computational dies are a single monolithic unit (i.e., each chiplet is not exposed as a separate device to an application that uses the chiplets for processing computational workloads).

[0013] In various embodiments, the CPU 102 is connected via a bus 108 to a system memory 110, such as a dynamic random access memory (DRAM). In various

embodiments, the system memory 110 can also be implemented using other types of memory including static random access memory (SRAM), nonvolatile RAM, and the like. In the illustrated embodiment, the CPU 102 communicates with the system memory 110 and also the GPU chiplet 106-1 over bus 108 that is implemented as a peripheral component interconnect (PCI) bus, PCI-E bus, or other type of bus. However, some embodiments of the system 100 includes the GPU chiplet 106-1 communicating with the CPU 102 over a direct connection or via other buses, bridges, switches, routers, and the like.

[0014] As illustrated, the CPU 102 includes a number of processes, such as executing one or more application(s) 112 to generate graphic commands and a user mode driver 116 (or other drivers, such as a kernel mode driver). In various embodiments, the one or more applications 112 include applications that utilizes the functionality of the GPU chiplets 106, such as applications that generate work in the system 100 or an operating system (OS). An application 112 may include one or more graphics instructions that instruct the GPU chiplets 106 to render a graphical user interface (GUI) and/or a graphics scene. For example, the graphics instructions may include instructions that define a set of one or more graphics primitives to be rendered by the GPU chiplets 106.

[0015] In some embodiments, the application 112 utilizes a graphics application programming interface (API) 114 to invoke a user mode driver 116 (or a similar GPU driver). User mode driver 116 issues one or more commands to the array 104 of one or more GPU chiplets for rendering one or more graphics primitives into displayable graphics images. Based on the graphics instructions issued by application 112 to the user mode driver 116, the user mode driver 116 formulates one or more graphics commands that specify one or more operations for GPU chiplets to perform for rendering graphics. In some embodiments, the user mode driver 116 is a part of the application 112 running on the CPU 102. For example, the user mode driver 116 may be part of a gaming application running on the CPU 102. Similarly, a kernel mode driver (not shown) may be part of an operating system running on the CPU 102.

[0016] In the depicted embodiment of FIG. 1, a passive crosslink 118 communicably couples the GPU chiplets 106 (i.e., GPU chiplets 106-1 through 106-N) to each other. Although three GPU chiplets 106 are shown in FIG. 1, the number of GPU chiplets in the chiplet array 104 is a matter of design choice and may vary in other embodiments, such as described in more detail below. In various embodiments, the passive crosslink 118 includes an interconnect chip such as a high density crosslink (HDCL) die interposer or other similar technology for inter-chiplet communications. As a general operational overview, the CPU 102 is communicably coupled to a single GPU chiplet (i.e., GPU chiplet 106-1) through the bus 108. CPU-to-GPU transactions or communications from the CPU 102 to the array 104 of chiplets 106 is received at the GPU chiplet 106-1. Subsequently, any inter-chiplet communications is routed through the passive crosslink 118 as appropriate to access memory channels on other GPU chiplets 106. In this manner, the GPU chiplet-based system 100 includes GPU chiplets 106 that are addressable as a single, monolithic GPU from a software developer's perspective (e.g., the CPU 102 and any associated applications / drivers are unaware of the chiplet-based architecture), and therefore avoids requiring any chiplet-specific considerations on the part of a programmer or developer.

[0017] Additional details of the chiplet-based architecture may be understood with reference to FIG. 2, which is a block diagram illustrating a sectional view of GPU chiplets and passive crosslink in accordance with some embodiments. The view 200 provides a sectional view of GPU chiplets 106-1, 106-2, and passive crosslink 118 of FIG. 1 taken at section A-A. In various embodiments, each GPU chiplet 106 is constructed with a physical device (PHY) region 202, which has various internal and external conductor structures dedicated to the transmission of chiplet-to-chiplet signals, and a non-PHY region 204, which has conductor structures that are tailored more to the conveyance of power and ground and/or chiplet-to-circuit board signals.

[0018] As previously noted, the GPU chiplets 106 are communicably coupled by way of the passive crosslink 118. In various embodiments, the passive crosslink 118 is an interconnect chip constructed of silicon, germanium or other semiconductor materials and may be bulk semiconductor, semiconductor on insulator or other designs. The passive

crosslink 118 includes a plurality of internal conductor traces, which may be on a single level or multiple levels as desired. Three of the traces are illustrated in FIG. 2 and labeled collectively as traces 206. The traces 206 interface electrically with conductor structures of the PHY regions 202 of the GPU chiplets 106 by way of conducting pathways. It is noted that the passive crosslink 118 does not contain any through silicon vias (TSVs). In this manner, the passive crosslink 118 is a passive interposer die that communicably couples and routes communications between the GPU chiplets 106, thereby forming a passive routing network.

[0019] The non-PHY regions 204 of the GPU chiplets 106 interface electrically with a circuit board 210 (or any other substrate) by way of a plurality of conductive pillars 212. Each conductive pillar 212 is connected electrically to the GPU chiplets 106 by way of a solder interconnect 208, which may include a solder bump, micro bump, and the like. In various embodiments, the circuit board 210 interfaces electrically with other electrical structure, such as another circuit board or other structures, by way of a plurality of interconnect structures 214 (e.g., solder balls and the like). However, those skilled in the art will appreciate that various types of interconnect structures such as pins, land grid array structures, other interconnects, and the like may be used without departing from the scope of this disclosure.

[0020] The conductive pillars 212 connect signals between the GPU chiplets 106 and the substrate in areas where the HDCL die is not present (e.g., areas with vertical discrepancy between the GPU chiplets 106 and the circuit board 210), with empty spaces filled with epoxy or other gap fill materials. In this manner, power and input/output (I/O) lines of the non-PHY regions 204 are routed around the interposer die (i.e., passive crosslink 118) using redistribution (RDL) technology, thereby replacing usage of conventional TSVs. For example, as illustrated in the embodiment of FIG. 2, the GPU chiplets 106 and passive crosslink 118 are at least partially encapsulated in a molding material, such as the two molding layers 218 and 220 of FIG. 2. The conductive pillars 212 traverse a plurality of insulating layers, such as the molding layer 220 and a polymer layer 222. In various embodiments, the polymer layer 222 is a RDL layer designed to act as a stress buffer and/or an isolation film for enabling redistribution layer routing. The conductive

pillars 212 include various conductor materials, such as copper and the like. Similarly, the solder interconnects 208 and interconnect structures 214 include materials using various solder compositions, such as tin-silver, tin-silver-copper, and the like.

[0021] The circuit board 210 may include organic or ceramic and single, or more commonly, multilayer materials. To cushion against the effects of mismatched coefficients of thermal expansion, an underfill material 224 (e.g., polymeric underfill) may be positioned between the molding layer 220 and an upper surface of the circuit board 210. The underfill material 224 may extend laterally beyond the left and right edges (and other edges not visible in FIG. 2) of the molding layer 220 as desired.

[0022] FIG. 3 is a block diagram illustrating a cache hierarchy of GPU chiplets coupled by a passive crosslink in accordance with some embodiments. The view 300 provides a hierarchical view of GPU chiplets 106-1, 106-2, and passive crosslink 118 of FIG. 1. Each of the GPU chiplets 106-1, 106-2 include a plurality of workgroup processors 302 (WGP) and a plurality of fixed function blocks 304 (GFX) that communicate with a given channel's L1 cache memory 306. Each GPU chiplet 106 also includes a plurality of L2 cache memory 308 banks that are individually accessible, a plurality of L3 cache memory 310 channels, and a plurality of memory PHY 312 (denoted as graphics double data rate (GDDR) in FIG. 3 for indicating connection to GDDR memory) channels mapped to the L3 channels. The L2 level of cache is coherent within a single chiplet and the L3 level (or other last level) of cache is unified and coherent across all of the GPU chiplets 106.

[0023] A graphics data fabric 314 (GDF) of each GPU chiplet 106 connects all of the L1 cache memories 306 to each of the channels of the L2 cache memory 308, thereby allowing each of the workgroup processors 302 and fixed function blocks 304 to access data stored in any bank of the L2 cache memory 308. Each GPU chiplet 106 also includes a scalable data fabric 316 (SDF) (also known as a SOC memory fabric) that routes across the graphics core (GC) and system on chip (SOC) IP cores to the passive crosslink 118. The GC includes CUs/WGPs, fixed function graphics blocks, caches above L3, and the like. Portions of the GPU used for traditional graphics and compute (i.e., the GC) are differentiable from other portions of the GPU used for handling

auxiliary GPU functionality such as video decode, display output, and various system supporting structures that are contained on the same die. The passive crosslink 118 routes to both local L3 cache memory 310 of a chiplet (e.g., of GPU chiplet 106-1) and the L3 cache memory 310 of all other external GPU chiplets (e.g., GPU chiplet 106-2 in FIG. 3). In this manner, a memory address request is routed to the appropriate lanes on the passive crosslink 118 to access L3 cache memory 310 locally or at L3 cache memory 310 of a different GPU chiplet 106 (as discussed in more detail with respect to FIG. 5).

[0024] FIG. 4 is a block diagram illustrating a floor plan view of a GPU chiplet in accordance with some embodiments. The view 400 provides a floor plan view of GPU chiplet 106-1 of FIGs. 1 and 2. As previously described in more detail with respect to FIG. 3, the GPU chiplet 106-1 includes a plurality of workgroup processors 302 (WGP) and a plurality of fixed function blocks 304 (GFX). The GPU chiplet 106-1 also includes a hierarchical cache memory 402 (e.g., L1 cache memory 306, L2 cache memory 308, and L3 cache memory 310 of FIG. 3) and memory PHY 312. The GPU chiplet 106-1 further includes a passive crosslink controller 404 and one or more passive crosslink PHY tiles, such as the four illustrated passive crosslink PHYs 406-1, 406-2, 406-3, and 406-4 (collectively, passive crosslink PHYs 406), at a first corner (e.g., top-right corner of GPU chiplet 106-1 in FIG. 4).

[0025] The passive crosslink controller 404 connects to the last level cache (LLC) of the GPU chiplet 106-1 (e.g., L3 cache memory as discussed herein), and handles routing between the LLC and electrically-active portions of the logic of data fabric crossbars (e.g., SDF 316 of FIG. 3). The passive crosslink PHYs 406 (e.g., passive crosslink PHYs 406-1, 406-2, 406-3, and 406-4) include the wire transport of data across various GPU chiplets 106. In particular, the passive crosslink PHYs 406 correspond to traces 206 of FIG. 2 that form dedicated communication channels between GPU chiplets 106 that the GPU chiplet 106-1 interconnects with.

[0026] In various embodiments, passive crosslink PHY 406-1 corresponds to a dedicated communications channel that routes to the local L3 cache memory 310 of GPU chiplet 106-1. In contrast, passive crosslink PHY 406-2 corresponds to a dedicated

communications channel that routes to the L3 cache memory 310 of an external GPU chiplet on a different chiplet die (e.g., GPU chiplet 106-2 of FIG. 1). That is, the dedicated communications channel of passive crosslink PHY 406-2 do not communicate with any chiplet other than GPU chiplet 106-2. Similarly, passive crosslink PHY 406-3, 406-4 correspond to dedicated communications channels that route to the L3 cache memory 310 of GPU chiplets 106-3 and 106-4, respectively. That is, the dedicated communications channels of passive crosslink PHY 406-3, 406-4 do not communicate with any chiplet other than GPU chiplets 106-3 and 106-4, respectively.

[0027] In some embodiments, the GPU chiplet 106-1 further includes an optional (as indicated by the dotted lines) second set of crosslink PHYs 408 at a second corner of the GPU chiplet 106-1 for communicating with additional GPU chiplets 106. The passive crosslink 118 thus operates as an extension cord between routing fabric of two or more dies and provides coherent L3 memory access with uniform memory access behavior (or mostly uniform memory access behavior). Those skilled in the art will recognize that the performance of a processing system generally scales linearly based on the number of GPU chiplets utilized by nature of physical duplication (e.g., as the number of GPU chiplets increases, so does the number of memory PHYs 312, WGP 302, and the like).

[0028] Referring now to FIG. 5, illustrated is a block diagram of a processing system utilizing a four-chiplet configuration in accordance with some embodiments. The processing system 500 is similar to the processing system 100 of FIG. 1 but omits certain elements for ease of illustration. As illustrated, the system 500 includes the CPU 102 and four GPU chiplets, such as the illustrated GPU chiplets 106-1, 106-2, 106-3, and 106-4. The CPU 102 communicates with GPU chiplet 106-1 via the bus 108. With reference back to FIG. 4, the passive crosslink PHY 406-1 corresponds to a dedicated communications channel that routes to the local L3 cache memory 310 of GPU chiplet 106-1 (not shown). Passive crosslink PHY 406-2 corresponds to a dedicated communications channel that routes to the L3 cache memory 310 of GPU chiplet 106-2 (labeled as signal route 502 in FIG. 5). Passive crosslink PHY 406-3 corresponds to a dedicated communications channel that routes to the L3 cache memory 310 of GPU chiplet 106-3 (labeled as signal route 504 in FIG. 5). Passive crosslink PHY 406-4

corresponds to a dedicated communications channel that routes to the L3 cache memory 310 of GPU chiplet 106-4 (labeled as signal route 506 in FIG. 5).

[0029] As a general operational overview, the processing system 500 utilizes a master-slave topology in which a single GPU chiplet in direct communication with the CPU 102 (i.e., GPU chiplet 106-1) is designated as the master chiplet (hereinafter, primary GPU chiplet or host GPU chiplet). The other GPU chiplets communicate with the CPU 102 indirectly via the passive crosslink 118 and are designated as the slave chiplets (hereinafter, secondary GPU chiplet(s)). Accordingly, the primary GPU chiplet 106-1 serves as the singular entry point from the CPU 102 to the entire GPU chiplet array.

[0030] As illustrated in FIG. 5, in one example, the CPU 102 transmits an access request (e.g., read request) for memory address XYZ to the primary GPU chiplet 106-1. The passive crosslink controller 404 determines that data associated with memory address XYZ is cached in L3 cache memory 310 of secondary GPU chiplet 106-4. Based on that determination, the access request is routed via signal route 506 of the passive crosslink 118 to secondary GPU chiplet 106-4. The secondary GPU chiplet 106-4 returns the result back to primary GPU chiplet 106-1, which subsequently returns the requested data to the originating requestor (i.e., CPU 102). In this manner, the CPU 102 only has a single external view and does not require direct communications to two or more GPU chiplets 106 via bus 108.

[0031] Those skilled in the art will recognize that although FIG. 5 is described here in the specific context of square GPU chiplet dies and a corner positions for the passive crosslink, various other configurations, die shapes, and geometries may be utilized in various embodiments without departing from the scope of this disclosure. For example, in some embodiments, the GPU chiplets may be constructed as pentagon-shaped dies such that five GPU chiplets may be coupled together in a chiplet array. In other embodiments, GPU chiplets may include passive crosslinks at two or more corners of a square GPU chiplet (e.g., optional second set of crosslink PHYs 408 of FIG. 4) such that multiple GPU chiplets may be tiled together in a chiplet array. Similarly, in other embodiments, GPU chiplets may include passive crosslinks spanning an entire side of a

square GPU chiplet such that multiple GPU chiplets may be strung together in a long row/column configuration to an intervening passive crosslink.

[0032] FIG. 6 is a flow diagram illustrating a method 600 of performing inter-chiplet communications in accordance with some embodiments. At block 602, a primary GPU chiplet of a GPU chiplet array receives a memory access request from a requesting CPU. For example, with reference to FIG. 5, the primary GPU chiplet 106-1 receives an access request for memory address XYZ from the CPU 102. In some embodiments, the primary GPU chiplet 106-1 receives the access request at its scalable data fabric 316 via the bus 108.

[0033] At block 604, the primary GPU chiplet 106-1 identifies a caching chiplet corresponding to the GPU chiplet at which the requested data is cached (also referred to interchangeably as the “secondary chiplet”). For example, with reference to FIG. 5, a passive crosslink controller 404 of the primary GPU chiplet 106-1 determines that data associated with memory address XYZ is cached in L3 cache memory 310 of secondary GPU chiplet 106-4. In some embodiments, the memory address range is address-sliced across the multiple GPU chiplets 106. In other embodiments, the processing system 100 utilizes other addressing topologies (e.g., flat address partitioning, addressing based on page settings from virtual to physical address translation, and the like). If the requesting data is not cached in the L3 of the secondary chiplet (i.e., the caching chiplet responsible for caching data associated with memory address XYZ), the memory access request is treated as an L3 miss and the secondary chiplet fetches the requested data from GDDR memory attached to that secondary chiplet.

[0034] At block 606, the primary GPU chiplet 106-1 routes the memory access request to the caching chiplet corresponding to the GPU chiplet at which the requested data is cached based on determination of block 604 and via the passive crosslink 118. For example, with reference to FIG. 5, the access request is routed via signal route 506 of the passive crosslink 118 to secondary GPU chiplet 106-4. In some embodiments, routing the memory access request includes the scalable data fabric 316 communicating with the

passive crosslink 118, the scalable data fabric 316 requesting a data associated with the memory access request from the caching chiplet (e.g., secondary GPU chiplet 106-4).

[0035] In other embodiments, after determining that the requested data is cached locally at the L3 cache 310 of the primary GPU chiplet 106-1, the scalable data fabric 316 routes the access request via the passive crosslink 118 to the L3 cache 310 of the primary GPU chiplet 106-1. For example, with reference to FIG. 4, the scalable data fabric 316 routes the memory access request via passive crosslink PHY 406-1 corresponding to a dedicated communications channel between the local L3 cache memory 310 of GPU chiplet 106-1 and the passive crosslink 118.

[0036] At block 608, the caching chiplet returns data corresponding to the memory access request back to the primary GPU chiplet via the passive crosslink 118. For example, with reference to FIG. 5, the secondary GPU chiplet 106-4 returns the result back to primary GPU chiplet 106-1. In particular, the return communication is routed via the same signal route 506 of the passive crosslink 118 from which the memory access request was routed in block 606. Similarly, with reference to FIG. 4, the return communication is routed via passive crosslink PHY 406-1 corresponding to a dedicated communications channel between the local L3 cache memory 310 of GPU chiplet 106-1 and the passive crosslink 118 when the caching chiplet is the same as the primary GPU chiplet. In other embodiments, the request data port and the return data port do not share the same physical route.

[0037] At block 610, the primary GPU chiplet returns the requested data to the originating requestor (i.e., CPU 102) via the bus 108. In some embodiments, returning the requested data to the CPU 102 includes receiving the requested data from the caching chiplet at the scalable data fabric 316 of the primary GPU chiplet (i.e., GPU chiplet 106-1) and transmitting the requested data to the CPU 102 via bus 108.

[0038] Accordingly, as discussed herein, a passive die interposer deploys monolithic GPU functionality using a set of interconnected GPU chiplets in a manner that makes the chiplet implementation appear as a traditional monolithic GPU from a programmer model/developer perspective. The scalable data fabric of one GPU chiplet is able to

access the lower level cache(s) on other GPU chiplets in nearly the same time as to access the lower level cache on its same chiplet, and thus allows the GPU chiplets to maintain cache coherency without requiring additional inter-chiplet coherency protocols. This low-latency, inter-chiplet cache coherency in turn enables the chiplet-based system to operate as a monolithic GPU from the software developer's perspective, and thus avoids chiplet-specific considerations on the part of a programmer or developer.

[0039] A computer readable storage medium may include any non-transitory storage medium, or combination of non-transitory storage media, accessible by a computer system during use to provide instructions and/or data to the computer system. Such storage media can include, but is not limited to, optical media (e.g., compact disc (CD), digital versatile disc (DVD), Blu-Ray disc), magnetic media (e.g., floppy disc, magnetic tape, or magnetic hard drive), volatile memory (e.g., random access memory (RAM) or cache), non-volatile memory (e.g., read-only memory (ROM) or Flash memory), or microelectromechanical systems (MEMS)-based storage media. The computer readable storage medium may be embedded in the computing system (e.g., system RAM or ROM), fixedly attached to the computing system (e.g., a magnetic hard drive), removably attached to the computing system (e.g., an optical disc or Universal Serial Bus (USB)-based Flash memory), or coupled to the computer system via a wired or wireless network (e.g., network accessible storage (NAS)).

[0040] In some embodiments, certain aspects of the techniques described above may be implemented by one or more processors of a processing system executing software. The software includes one or more sets of executable instructions stored or otherwise tangibly embodied on a non-transitory computer readable storage medium. The software can include the instructions and certain data that, when executed by the one or more processors, manipulate the one or more processors to perform one or more aspects of the techniques described above. The non-transitory computer readable storage medium can include, for example, a magnetic or optical disk storage device, solid state storage devices such as Flash memory, a cache, random access memory (RAM) or other non-volatile memory device or devices, and the like. The executable instructions stored on the non-transitory computer readable storage medium may be in source code, assembly language

code, object code, or other instruction format that is interpreted or otherwise executable by one or more processors.

[0041] Note that not all of the activities or elements described above in the general description are required, that a portion of a specific activity or device may not be required, and that one or more further activities may be performed, or elements included, in addition to those described. Still further, the order in which activities are listed are not necessarily the order in which they are performed. Also, the concepts have been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present disclosure as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of the present disclosure.

[0042] Benefits, other advantages, and solutions to problems have been described above with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any feature(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature of any or all the claims. Moreover, the particular embodiments disclosed above are illustrative only, as the disclosed subject matter may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. No limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope of the disclosed subject matter. Accordingly, the protection sought herein is as set forth in the claims below.

WHAT IS CLAIMED IS:

1. A system, comprising:
 - a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array, wherein the GPU chiplet array includes:
 - the first GPU chiplet communicably coupled to the CPU via a bus;
 - and
 - a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications.
2. The system of claim 1, wherein the passive crosslink comprises a passive interposer die.
3. The system of claim 1, wherein the first GPU chiplet comprises a first PHY region including conductor structures for chiplet-to-chiplet communications, and further wherein the second GPU chiplet comprises a second PHY region including conductor structures for chiplet-to-chiplet communications.
4. The system of claim 3, further comprising:
 - a third GPU chiplet communicably coupled to the first GPU chiplet via the passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications, wherein the third GPU chiplet comprises a third PHY region including conductor structures for chiplet-to-chiplet communications.
5. The system of claim 4, wherein the first PHY region of the first GPU chiplet comprises a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the first GPU chiplet.

6. The system of claim 4, wherein:
 - the second PHY region of the second GPU chiplet comprises a second passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the second GPU chiplet; and
 - the third PHY region of the third GPU chiplet comprises a third passive crosslink PHY including conductor traces solely for communications between the passive crosslink and a last level cache of the third GPU chiplet.
7. The system of claim 1, wherein the passive crosslink communicably couples all GPU chiplets in the GPU chiplet array.
8. The system of claim 1, further comprising:
 - a first cache memory hierarchy at the first GPU chiplet, wherein a first level of the first cache memory hierarchy is coherent within the first GPU chiplet; and
 - a second cache memory hierarchy at the second GPU chiplet, wherein a first level of the second cache memory hierarchy is coherent within the second GPU chiplet.
9. The system of claim 8, further comprising:
 - a unified cache memory including both a last level of the first cache memory hierarchy and a last level of the second cache memory hierarchy, wherein the unified cache memory is coherent across all chiplets of the GPU chiplet array.
10. The system of claim 1, further comprising:
 - a plurality of conductive pillars coupling a circuit board substrate to a first non-PHY region of the first GPU chiplet and a second non-PHY region of the second GPU chiplet.

11. A method, comprising:
 - receiving, at a first GPU chiplet of a GPU chiplet array, a memory access request from a central processing unit (CPU);
 - determining, at a passive crosslink controller of the first GPU chiplet, a caching GPU chiplet corresponding to a location at which data associated with the memory access request is stored;
 - routing, via a passive crosslink dedicated for inter-chiplet communications in the GPU chiplet array, the memory access request to a last level cache of the caching GPU chiplet; and
 - returning data associated with the memory access request to the CPU.
12. The method of claim 11, wherein routing the memory access request further includes a scalable data fabric requesting data associated with the memory access request from the caching GPU chiplet.
13. The method of claim 11, wherein routing the memory access request to the last level cache of the caching GPU chiplet further comprises:
 - routing, based on determining the first GPU chiplet is the caching GPU chiplet, the memory access request via a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the first GPU chiplet.
14. The method of claim 11, wherein routing the memory access request to the last level cache of the caching GPU chiplet further comprises:
 - routing, based on determining a second GPU chiplet is the caching GPU chiplet, the memory access request via a second passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the second GPU chiplet.
15. The method of claim 11, further comprising:
 - returning data associated with the memory access request to the first GPU chiplet via a passive crosslink PHY including conductor traces solely for

communications between the passive crosslink and the caching GPU chiplet.

16. A non-transitory computer readable medium embodying a set of executable instructions, the set of executable instructions to manipulate at least one processor to:
 - receive, at a first GPU chiplet of a GPU chiplet array, a memory access request from a central processing unit (CPU);
 - determine, at a passive crosslink controller of the first GPU chiplet, a caching GPU chiplet corresponding to a location at which data associated with the memory access request is stored;
 - route, via a passive crosslink dedicated for inter-chiplet communications in the GPU chiplet array, the memory access request to a last level cache of the caching GPU chiplet; and
 - return data associated with the memory access request to the CPU.
17. The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to: request, via a scalable data fabric, data associated with the memory access request from the caching GPU chiplet.
18. The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:
 - route, based on determining the first GPU chiplet is the caching GPU chiplet, the memory access request via a first passive crosslink PHY including conductor traces solely for communications between the passive crosslink and the last level cache of the first GPU chiplet.
19. The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:
 - route, based on determining a second GPU chiplet is the caching GPU chiplet, the memory access request via a second passive crosslink PHY including

conductor traces solely for communications between the passive crosslink and the last level cache of the second GPU chiplet.

20. The non-transitory computer readable medium of claim 16, the set of executable instructions further to manipulate at least one processor to:
return data associated with the memory access request to the first GPU chiplet via
a passive crosslink PHY including conductor traces solely for
communications between the passive crosslink and the caching GPU
chiplet.

ABSTRACT OF THE DISCLOSURE

A chiplet system includes a central processing unit (CPU) communicably coupled to a first GPU chiplet of a GPU chiplet array. The GPU chiplet array includes the first GPU chiplet communicably coupled to the CPU via a bus and a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink. The passive crosslink is a passive interposer die dedicated for inter-chiplet communications and partitions systems-on-a-chip (SoC) functionality into smaller functional chiplet groupings.

Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	GPU CHIPLETS USING HIGH BANDWIDTH CROSSLINKS			
First Named Inventor/Applicant Name:	Skyler J. SALEH			
Filer:	Allen Torng/Emily Stalder			
Attorney Docket Number:	1458-190070			
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Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	300	300
UTILITY SEARCH FEE	1111	1	660	660
UTILITY EXAMINATION FEE	1311	1	760	760
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	190070_ADS.pdf	1256031	no	9
			3a822b2279c53832a83cd9b4f948c1d325c1264e		
Warnings:					
Information:					
2	Drawings-only black and white line drawings	190070_Figures--Final.pdf	86258	no	6
			f28c70868efc5a8650eb8faa16c3ccdfdfb8b740		
Warnings:					
Information:					
3		190070_Specification--Final.pdf	124658	yes	20
			4a0cfec5dc06e23bc20a08a5bbc51dc083f1a567		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	14	
	Claims		15	19	
	Abstract		20	20	
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	36815	no	2
			a278c9ea503e67d60ae1263cdfc421d323374cb2		
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