John H. Lau

Heterogeneous Integrations

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Preface

Due to the drive of Moore's law, compounded with the demands of mobile products such as smartphones, tablets, and wearables, SoC (system-on-chip) has been very popular in the past 10+ years. SoC integrates ICs with different functions into a single chip for the system or subsystem. Unfortunately, the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make the SoC. Heterogeneous integration contrasts with SoC. Heterogeneous integration uses packaging technology to integrate dissimilar chips, photonic devices, or components (either side-by-side, stack, or both) with different materials and functions, and from different fabless design houses, foundries, wafer sizes, feature sizes and companies into a system or subsystem. System-in-package (SiP) is very similar to heterogeneous integration, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance.

In general, heterogeneous integrations can be classified as heterogeneous integrations on organic substrates, heterogeneous integrations on silicon substrates (with TSV (through-silicon via)-interposers), heterogeneous integrations on silicon substrates (with TSV-less interposers such as bridges), heterogeneous integrations on fan-out RDL (redistribution-layer) substrates, and heterogeneous integrations on ceramic substrates. For the next few years, we will see more implementations of a higher level of heterogeneous integrations on these various substrates, whether it is for performance, form factor, power consumption, signal integrity, or cost.

Unfortunately, for most of the practicing engineers and managers, as well as scientists and researchers, build-up organic package substrates, thin-film layer on top of the build-up substrates, organic interposers, TSV-interposers, fabrication of TSV and RDLs, TSV-less interposers, bridges, fan-out RDL substrates, package-on-package, memory stacks, chip-to-chip stacks, wafer bumping, thermoscompression bonding, low-temperature bonding, chip-to-wafer bonding, and wafer-to-wafer bonding are not well understood. Thus, there is an urgent need, both in industry and research institute, to create a comprehensive book on the current state of knowledge of these key enabling technologies. This book is written so that

readers can quickly learn about the basics of problem-solving methods and understand the trade-offs inherent in making system-level decisions.

There are 11 chapters in this book, namely: (1) overview of heterogeneous integrations, (2) heterogeneous integrations on organic substrates, (3) heterogeneous integrations on silicon substrates (TSV-interposers), (4) heterogeneous integrations on silicon substrates (TSV-less interposers such as bridges), (5) fan-out wafer/panel-level packaging for heterogeneous integrations, (6) heterogeneous integrations on fan-out RDL substrates, (7) heterogeneous integration of PoP (package-on-package), (8) heterogeneous integration of memory stacks, (9) heterogeneous integration of chip-to-chip stacks, (10) heterogeneous integration of CIS (CMOS image sensor), LED (light-emitting diode), MEMS (microelectromechanical systems), and VCSEL (vertical cavity surface emitted laser) and PD (photodiode), and (11) trends in heterogeneous integrations.

Chapter 1 simply defines and classifies heterogeneous integrations. Various applications of heterogeneous integrations will also be briefly mentioned.

Chapter 2 presents the heterogeneous integrations on organic substrates. Emphasis is placed on various organic substrates such as the build-up, thin-film layer on top of the build-up, organic interposer, coreless substrate, bump-on-lead, and embedded trace substrate for heterogeneous integrations.

Chapter 3 details the heterogeneous integration on silicon substrates (TSV-interposers). Emphasis is placed on the thermal performance, mechanical characterization, and fabrication of a heterogeneous integration of chips on both sides of a TSV interposer. The fabrication of TSVs and RDLs of interposers will be briefly mentioned first.

Chapter 4 presents the heterogeneous integration on silicon substrates (TSV-less interposers such as bridges). Emphasis is placed on the electrical performance and fabrication of a heterogeneous integration of chips on both sides of a bridge. Intel's EMIB (embedded multi-die interconnect bridge) and imec's bridge for logic and memories interconnections will be briefly mentioned first.

Chapter 5 overviews the fan-out wafer/panel-level packaging (FOW/PLP) for heterogeneous integrations. Emphasis is placed on the formation of FOW/PLP and the fabrication of RDLs. The opportunities of FOW/PLP for heterogeneous integrations will also be briefly mentioned.

Chapter 6 provides the heterogeneous integrations on fan-out RDL substrates. Emphasis is placed on using the FOW/PLP technology to make RDLs to eliminate the TSV-interposer for heterogeneous integrations.

Chapter 7 presents the heterogeneous integration of PoP (package-on-packaging). Examples on using PoPs for smartphones and smartwatches will be briefly mentioned.

Chapter 8 discusses the heterogeneous integration of memory stacks. Emphasis is placed on the heterogeneous integration of two memory chips stacked on one ASIC and the heterogeneous integration of memory chips and logic chip with low-temperature bonding.

Chapter 9 provides two examples of heterogeneous integrations of chip-to-chip and face-to-face. One is with TSVs in the bottom chip to let go of the signals, powers, and grounds and the other is without TSVs but with solder bumps on the larger chip.

Chapter 10 presents the heterogeneous integration of CIS, LED, MEMS, and VCSEL and PD. Emphasis is placed on providing some examples of each of these heterogeneous integrations.

Chapter 11 provides the trends in heterogeneous integrations. Emphasis is placed on the fabrication processes, selection criterions, and application ranges (size and pin-count) of various heterogeneous integrations.

For whom is this book intended? Undoubtedly it will be of great interest to three groups of specialists: (1) those who are active or intend to become active in research and development of the key enabling technologies of heterogeneous integrations such as build-up organic package substrates, thin-film layer on top of the build-up substrates, organic interposers, TSV-interposers, fabrication of TSV and RDLs, TSV-less interposers, bridges, fan-out RDL substrates, package-on-package, memory stacks, chip-to-chip stacks, wafer bumping, thermocompression bonding, low-temperature bonding, chip-to-wafer bonding, and wafer-to-wafer bonding; (2) those who have encountered practical heterogeneous integration problems and wish to understand and learn more methods for solving such problems; and (3) those who have to choose a reliable, creative, high performance, high density, low power consumption, and cost-effective heterogeneous integration technique for their products. This book can also be used as a text for college and graduate students who have the potential to become our future leaders, scientists, and engineers in the electronics and optoelectronics industry.

I hope that this book will serve as a valuable reference source for all those faced with the challenging problems created by the ever-increasing interest in heterogeneous integrations. I also hope that it will aid in stimulating further research and development on key enabling technologies and more sound applications to heterogeneous integration products. The organizations that learn how to design and manufacture heterogeneous integrations in their semiconductor packaging systems have the potential to make major advances in the electronics and optoelectronics industry, and to gain great benefits in performance, functionality, density, power, bandwidth, quality, size, and weight. It is my hope that the information presented in this book may assist in removing roadblocks, avoiding unnecessary false starts, and accelerating design, materials, process, and manufacturing development of key enabling technologies of heterogeneous integrations.

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About the Author

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His professional competences are design, analysis, materials, process, manufacturing, qualification, reliability, testing, and thermal management of electronic, optoelectronic, LED, CIS, and MEMS components and systems, with emphases on solder mechanics and manufacturing, RoHS-compliant products, SMT, flip chip, fan-in and fan-out WLP, SiP, heterogeneous integration, and TSV and other enabling technologies for 3D IC integration.

With more than 40 years of R&D and manufacturing experience, he has authored or coauthored more than 470 peer-reviewed technical publications, invented more than 30 issued or pending US patents, and given more than 300 lectures/workshops/keynotes worldwide. He has authored or coauthored 20 textbooks on fan-out wafer-level packaging, 3D IC integration and packaging, TSV for 3D integration, advanced MEMS packaging, reliability of 2D and 3D IC interconnects, flip chip, WLP, MCM, area-array packages, WLCSP, high-density PCB, SMT, DCA, TAB, lead-free materials, soldering, manufacturing, and solder joint reliability.

He earned a Ph.D. degree in theoretical and applied mechanics from the University of Illinois at Urbana–Champaign, an M.A.Sc. degree in structural engineering from the University of British Columbia, a second M.S. degree in engineering mechanics from the University of Wisconsin at Madison, and a third M.S. degree in management science from Fairleigh Dickinson University. He also has a B.E. degree in civil engineering from National Taiwan University.

He has received many awards from the American Society of Mechanical Engineers (ASME), the Institute of Electrical and Electronics Engineers (IEEE), the Society of Manufacturing Engineers (SME) and other societies, including for the

best IEEE/ECTC proceedings paper (1989), outstanding IEEE/EPTC paper (2009), best ASME transactions paper (Journal of Electronic Packaging, 2000), and best IEEE transactions paper (CPMT, 2010), and the ASME/EEP Outstanding Technical Achievement Award (1998), IEEE/CPMT Manufacturing Award (1994), IEEE/CPMT Outstanding Contribution Award (2000), IEEE/CPMT Outstanding Sustained Technical Contribution Award (2010), SME Total Excellence in Electronics Manufacturing Award (2001), Pan Wen Yuan Distinguished Research Award (2011), IEEE Meritorious Achievement in Continuing Education Award (2000), IEEE Components, Packaging, and Manufacturing Technology Field Award (2013), and ASME Worcester Reed Warner Medal (2015). He is an elected ASME fellow, IEEE fellow, and IMAPS fellow, and has been heavily involved in many of ASME's, IEEE's, and IMAPS' technical activities.

Chapter 1
Overview of Heterogeneous Integrations



1.1 Introduction

Multichip module (MCM), system-in-package (SiP), and heterogeneous integration use packaging technology to integrate dissimilar chips, optical devices, and/or packaged chips with different materials and functions, from different fabless houses, foundries, wafer sizes, and feature sizes into a system or subsystem on different substrates or stand alone. What is the difference between MCM, SiP, and heterogeneous integration? The traditional MCM is mainly a 2D integration. The SiP can also be a 3D integration or called vertical-MCM or 3D-MCM. Heterogeneous integration is very similar to SiP, except heterogeneous integration is for finer pitches, more inputs/outputs (I/Os), higher density, and higher performance applications. Actually, SiP can be considered a big subset of heterogeneous integration [1–97]. In this chapter various applications of heterogeneous integrations will be presented. The MCM and SiP will be briefly mentioned first.

1.2 Multichip Module (MCM)

MCM integrates different chips and discrete components side-by-side on a common substrate such as ceramic, silicon, or organic to form a system or subsystem for high-end networking, telecommunication, servers, and computer applications. Basically, there are three different kinds of MCM, namely, MCM-C, MCM-D, and MCM-L.

1.2.1 MCM-C

MCM-C are multichip modules that use thick film technology such as fireable metals to form the conductive patterns, and are constructed entirely from ceramic or glass-

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ceramic materials, or possibly, other materials having a dielectric constant above five. In short, an MCM-C is constructed on ceramic (C) or glass-ceramic substrates [98].

1.2.2 MCM-D

MCM-D are multichip modules on which the multilayered signal conductors are formed by the deposition of thin-film metals on unreinforced dielectric materials with a dielectric constant below 5 over a support structure of silicon, ceramic, or metal. In short, MCM-D uses deposited (D) metals and unreinforced dielectrics on a variety of rigid bases [98].

1.2.3 MCM-L

MCM-L are multichip modules which use laminate structures and employ PCB (printed circuit board) technology to form predominantly copper conductors and vias. These structures may sometimes contain thermal expansion controlling metal layers. In short, MCM-L utilizes PCB technology of reinforced organic laminates (L) [98].

There was much research performed on MCMs during the 1990s. Unfortunately, at that time, due to the high cost of ceramic and silicon substrates and the limitation of line width and spacing of the laminate substrate, compounded with business models such as difficulty in getting the bare chips, the high-volume manufacturing (HVM) of MCMs never materialized, except some niche applications. Actually, since then, MCM has been a "dirty" word in semiconductor packaging.

1.3 System-in-Package (SiP)

1.3.1 Intention of SiP

SiP integrates different chips and discrete components, as well as 3D chip stacking of either packaged chips or bare chips (e.g., wide-bandwidth memory cubes and memory on logic with TSVs) side-by-side on a common (either silicon, ceramic, or organic) substrate to form a system or subsystem for smartphones, tablets, high-end networking, telecommunication, server, and computer applications. SiP technology performs horizontal as well as vertical integrations. Some people also called SiP vertical-MCM or 3D-MCM.

1.3.2 Actual Applications of SiP

Unfortunately, because of the high cost of TSV technology [99, 100] for smartphones and tablets, it never materialized. Most SiPs that went into HVM in the past 10 years are actually MCM-L for low-end applications such as smartphones, tablets, smart watches, medical, wearable electronics, gaming systems, consumer products, and internet of things (IoT)-related products [101] such as smart homes, smart energy, and smart industrial automation. Most actual applications of SiPs by OSATs (outsourced semiconductor assembly and test) integrate two or more dissimilar chips, components, and some discrete components on a common laminated substrate.

1.3.3 Potential Applications of SiP

The applications of SiP for the high-price, high-margin, and high-end products are, e.g., dual-lens camera modules. However, right now this SiP cannot be all done by the OSAT, but also involves optical design, testing, lenses, micromotors, flexible substrate, and system integration capabilities which still need to be strengthened.

1.4 System-on-Chip (SoC)

Moore's law [102] has been driving the system-on-chip (SoC) [103–105] platform. Especially in the past 10 years, SoCs have been very popular for smartphones, tablets, and the like. SoCs integrate different-function ICs into a single chip for a system or subsystem. Three typical SoC examples are shown in the followings.

1.4.1 Apple Application Processor (A10)

The application processor (AP) A10 is designed by Apple and manufactured by TSMC using its 16 nm process technology. It consists of a 6-core graphics processor unit (GPU), two dual-core central processing unit (CPUs), 2 blocks of static random access memories (SRAMs), etc. The chip area (11.6 mm $\times$ 10.8 mm) is 125 mm^2, Fig. 1.1a.

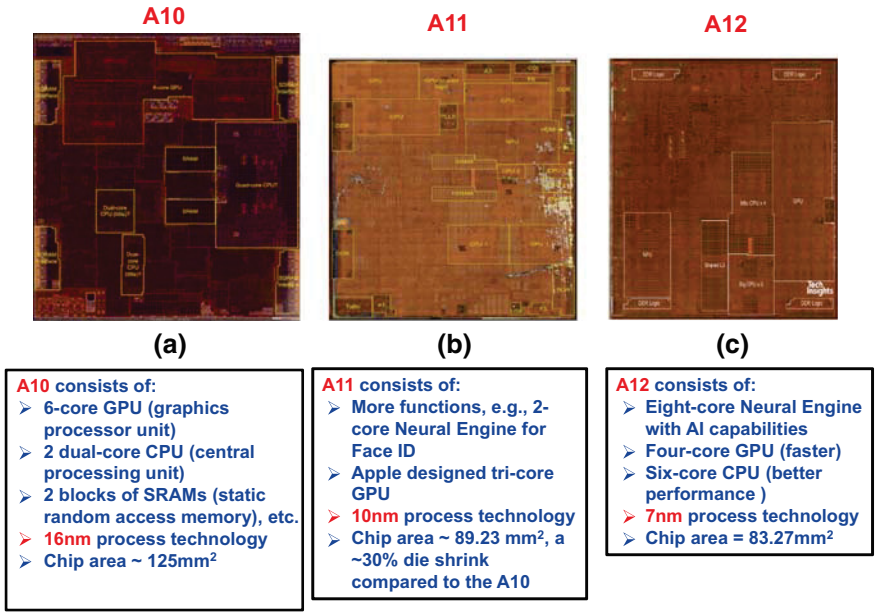


Fig. 1.1 SoC platforms for the A10, A11, and A12 APs

1.4.2 Apple Application Processor (A11)

The application processor A11 is also designed by Apple and manufactured using TSMC's 10 nm process technology. The A11 consists of more functions, including a tri-core Apple-designed GPU, neural engine for face ID, etc. However, the chip area (89.23 mm^2) is about 30% smaller than that of the A10 because of Moore's law, i.e., the feature size is from 16 nm down to 10 nm, Fig. 1.1b.

1.4.3 Apple Application Processor (A12)

The application processor A12, Fig. 1.1c, is also designed by Apple and manufactured using TSMC's 7 nm process technology. The A12 consists of much more functions, including an eight-core neural engine with artificial intelligence (AI) capabilities, four-core GPU which can run faster, six-core CPU which can performance better, etc. However, the chip area (83.27 mm^2) is about the same as that of A11.

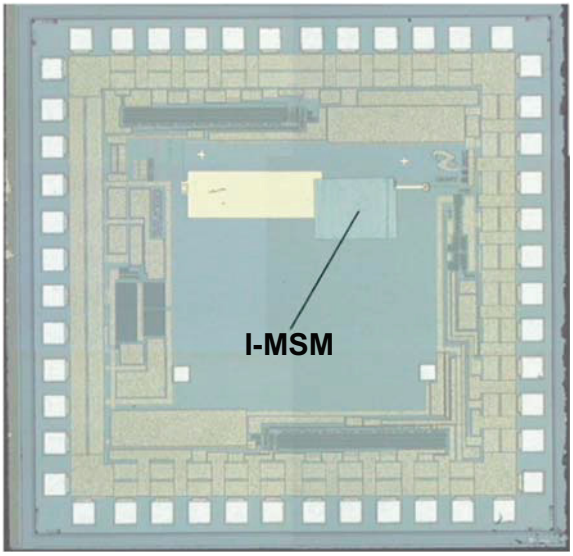


Fig. 1.2 InGaAs/InP I-MSM integrated onto differential Si CMOS receiver IC

1.5 Heterogeneous Integration

Some of the early researches in heterogeneous integration have been provided by Georgia Institute of Technology [106–108], where they reported a differential Si CMOS (complementary metal–oxide semiconductor) receiver IC (operating at 1 Gbps) integrated with a large-area thin-film InGaAs/InP I-MSM (metal–semiconductor–metal) photodetector (Fig. 1.2). Today, most heterogeneous integrations focus on higher density, finer pitch, and more complex system.

1.5.1 Heterogeneous Integration Versus SoC

Why is the heterogeneous integration of such great interest? One of the key reasons is because the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make SoCs. Heterogeneous integration contrasts with SoCs as follows. The heterogeneous integration uses packaging technology to integrate dissimilar chips (either side-by-side or stack) or components with different materials and functions from different fabless houses, foundries, wafer sizes, and feature sizes (as shown in Fig. 1.3) into a system or subsystem on different (e.g., organic, silicon, or RDL) substrates or stand alone, rather than integrating most of the functions into a single chip and going for a finer feature size.

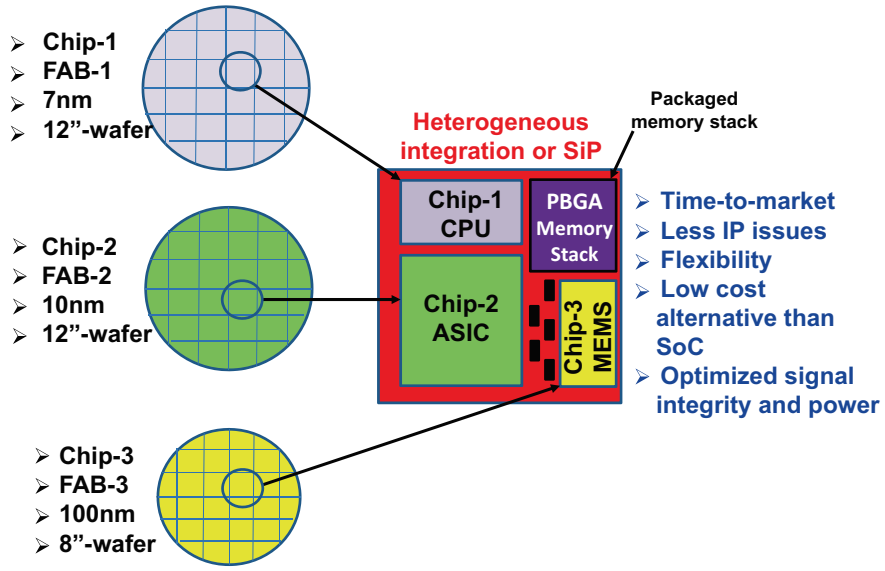


Fig. 1.3 Heterogeneous Integration or SiP

1.5.2 Advantages of Heterogeneous Integration

For the next few years, we will see more of a higher level of heterogeneous integrations, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost. Heterogeneous integration is going to take some of the market shares away from SoCs on high-end applications such as high-end smartphones, tablets, wearables, networkings, telecommunications, and computing devices. How should these dissimilar chips talk to each other, however? The answer is redistribution layers (RDLs) [109, 110]! In this chapter, the RDLs for heterogeneous integrations on organic substrates, silicon substrates (through-silicon via (TSV)-interposers), silicon substrates (bridges), and fan-out substrates will be discussed. Also, various applications of heterogeneous integrations of PoP (package-on-package), memory stacks, chip-to-chip stacks, LED (light-emitting diode), CIS (CMOS image sensors), MEMS (micro-electro-mechanical systems), and VCSEL (vertical-cavity surface-emitting laser) will be briefly mentioned. SiP [37–97] is very similar to heterogeneous integration [1–36], except SiP is for coarser pitches, less inputs/outputs (I/Os), lower density, and lower performance applications.

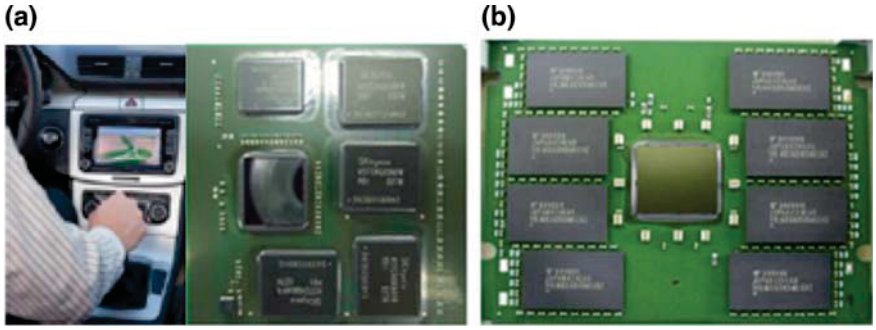


Fig. 1.4 Amkor's SiP for automobiles. **a** 42.5 mm × 42.5 mm infotainment. **b** 55 mm × 72 mm organic substrate

1.6 Heterogeneous Integration on Organic Substrates

Today, the most common applications of heterogeneous integration are on organic substrates, or the so-called SiP. The assembly methods are usually SMT (surface mount technology) including solder bumped flip chips with mass reflow and wire bonding chips on board. In general, this is for low-end to middle-end applications. For more information on heterogeneous integration on organic substrates, please read Chap. 2 of this book.

1.6.1 Amkor's SiP for Automobiles

Amkor's SiP for automobiles focuses on autonomous driving, infotainment, and ADAS (advanced drive assist systems), and computer in a car. Figure 1.4a, b, show a couple of examples of Amkor's SiP for automobiles. It can be seen from Fig. 1.4a that the 42.5 mm × 42.5 mm infotainment organic substrate is supporting the processor and DDR (double data rate) memories. While from Fig. 1.4b, the 55 mm × 72 mm organic substrate is supporting the network switch, ASIC (application-specific integrated circuit), and memories.

1.6.2 Apple Watch III (SiP) Assembled by ASE

Through USI (Universal Scientific Industrial), ASE is a sole backend provider for Apple's custom-designed S3 SiP modules (Fig. 1.5) for use in the Apple Watch III. It can be seen from Fig. 1.5 that there are >40 chips and are on an organic substrate. Some of these chips are discrete passive components such as capacitors and resistors, ASIC, processors, controller, converter, DRAM (dynamic random access memory),

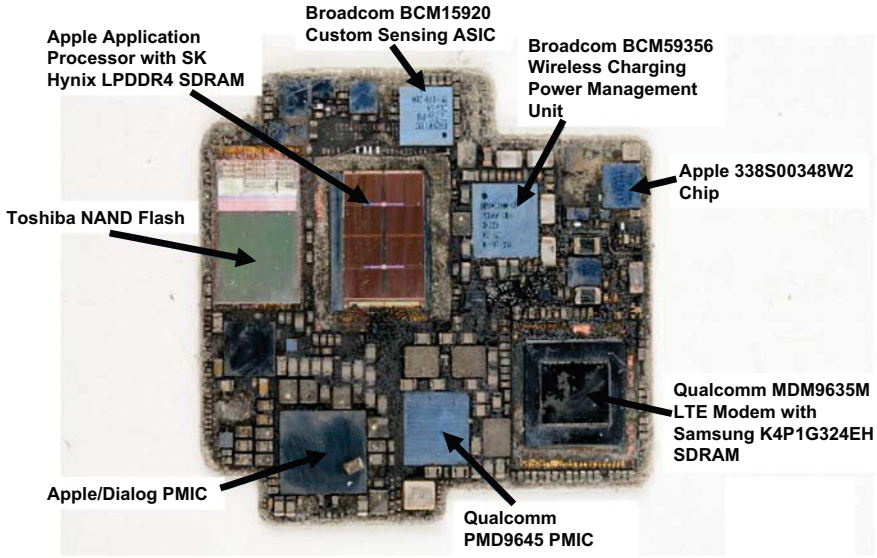


Fig. 1.5 Apple's smart watch SIII assembled by ASE

NAND, Wi-Fi, NFC (near-field communication), GPS (global positioning system), sensors, etc.

1.6.3 Cisco's ASIC and HBM on Organic Substrate

Figure 1.6 shows a 3D system-in-package (SiP) designed and manufactured with a large organic interposer (substrate) with fine-pitch and fine-line interconnections by Cisco [82]. The organic interposer has a size of 38 mm × 30 mm × 0.4 mm. The linewidth, spacing, and thickness of the front-side and backside of the organic interposer are the same and are, respectively, 6, 6, and 10 μm. A high-performance ASIC die measured at 19.1 mm × 24 mm × 0.75 mm is attached on top of the organic interposer along with four HBM (high-bandwidth memory) DRAM die stacks. The 3D HBM die stack with a size of 5.5 mm × 7.7 mm × 0.48 mm includes one base buffer die and four DRAM core dice, which are interconnected with TSVs and fine-pitch micro-pillars with solder caps. This is for the high-end application.

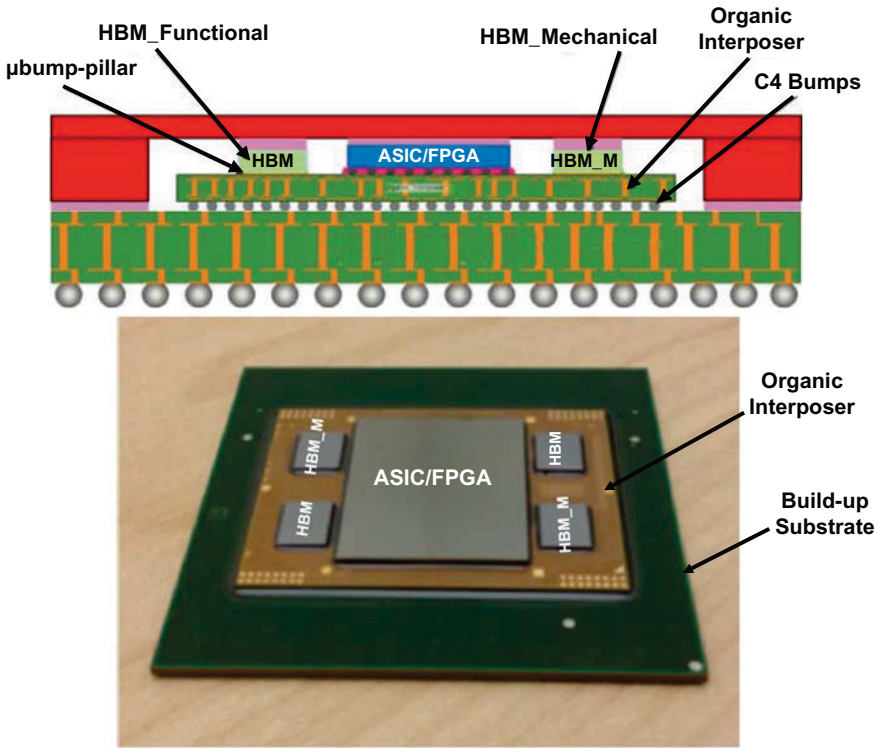


Fig. 1.6 Cisco's networking system with organic interposer

1.6.4 Intel's CPU and Micron's HMC on Organic Substrate

Figure 1.7 shows Intel's Knights Landing CPU with Micron's HMC (hybrid memory cube), which have been shipping to Intel's favorite customers since the second-half of 2016. It can be seen that the 72-core processor is supported by 8 multi-channel DRAMs (MCDRAM) based on Micron's HMC technology. Each HMC consists of 4 DRAMs and a logic controller (with TSVs), and each DRAM has >2000 TSVs with Cu-pillar bump with solder cap. The CPU and the DRAM + logic controller stack are attached to an organic package substrate. This is for the high-end application.

1.7 Heterogeneous Integration on Silicon Substrates (TSV-Interposer)

In general, heterogeneous integrations on silicon substrates are for multichip on silicon wafer or system-on-wafer (SoW). The assembly methods are usually flip

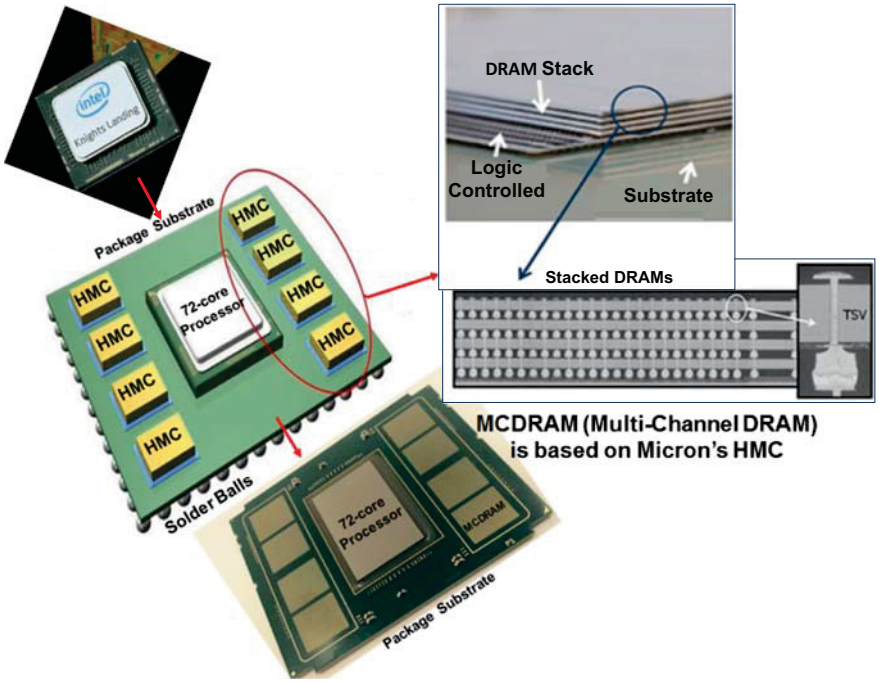


Fig. 1.7 Intel's Knights Landing and Micron's HMC on organic substrate

chips-on-wafers (CoW) with TSVs (through-silicon vias) with mass reflow or with thermocompression bonding for very fine pitches. In general, this is for high-end applications. For more information on heterogeneous integration on silicon substrates (TSV-interposers), please read Chap. 3 of this book.

1.7.1 Leti's SoW

One of the early applications of SoW is given by Leti [35, 36] as shown in Fig. 1.8. It can be seen that a system of chips such as ASIC and memories, PMIC (power management IC) and MEMS are on a silicon wafer with TSVs (through-silicon vias). After dicing, the individual unit becomes a system or subsystem and can be attached on an organic substrate or stand alone.

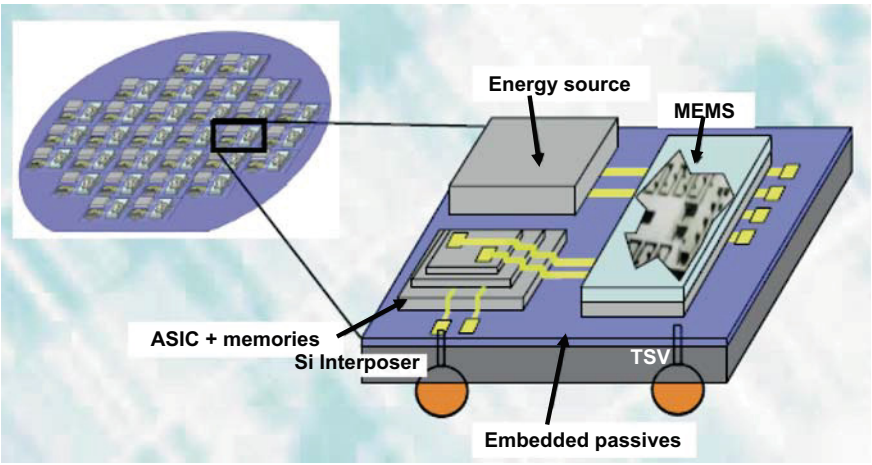


Fig. 1.8 Leti's heterogeneous integration (SoW)

1.7.2 IME's SoW

Mobile electronic products demand multifunctional module comprising digital, RF and memory functions. TSV technology provides a means of implementing complex, multi-functional integration with a higher packing density for a heterogeneous integration. Figure 1.9 shows a 3D module with silicon carrier [37]. The package consists of two stacks assembled with three chips. The module dimensions are 12 mm × 12 mm × 1.3 mm. The silicon carrier size is 12 mm × 12 mm with 168 peripherally populated via. Carrier 1 is assembled with a 5 mm × 5 mm flip-chip. The carrier 2 is assembled with a 5 mm × 5 mm flip-chip and two 3 mm × 6 mm wirebond-chip. The carrier 2 is over molded to protect the wire bonds. The silicon carrier has been fabricated with two metal layers with SiO_2 as dielectric/passivation layer. Electrical connections through the carrier are formed by TSVs. The right-hand side of Fig. 1.9 shows the assembled structure.

1.7.3 ITRI's Heterogeneous Integrations

Figure 1.10 shows a heterogeneous integration of various chips on a TSV interposer [38, 39]. It can be seen that the interposer (with 15 μm-vias) supports four memory chips (with 10 μm-vias) stacked, one thermal chip, and one mechanical chip. It is over molded for pick-and-place purpose as well as protecting the chips from harsh environments. There are RDLs on both top and bottom sides of the interposer. Also, stress sensors are implanted on the top side and IPDs (integrated passive devices) are fabricated through the thickness (100 μm) of the interposer (12.3 mm × 12.2 mm).

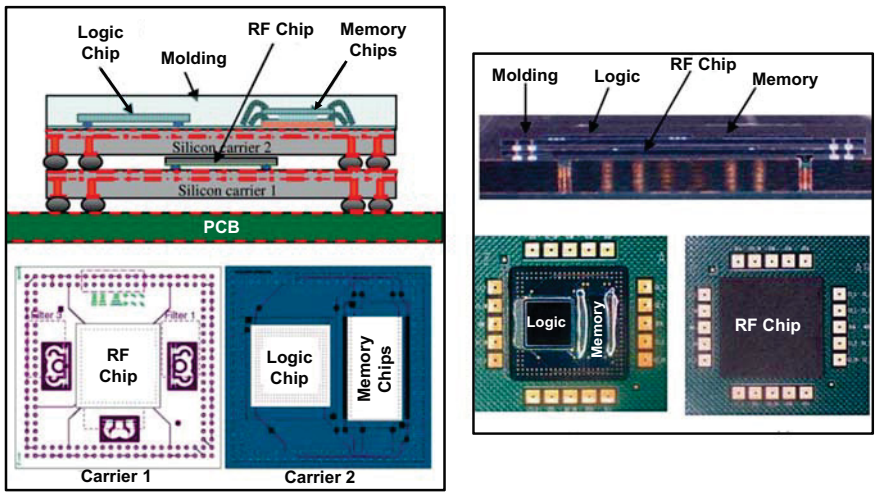


Fig. 1.9 IME's heterogeneous integration of RF chip, logic chip, and memory chips

This test vehicle can be degenerated to the case of: (a) wide I/O DRAM if there are not mechanical and thermal chips and the interposer is an ASIC chip; (b) wide I/O memory if there is not the memory-chip stacking nor the TSVs in the mechanical/thermal chips and the interposer is either an ASIC or microprocessor; and (c) wide I/O interface if there is not the memory-chip stacking and there is not any TSV in the thermal/mechanical chips. Thus, the enabling technologies developed with this test vehicle can have very broad applications.

1.7.4 Xilinx/TSMC's CoWoS

In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field-programmable gate array (FPGA), even a 12 build-up layers (6-2-6) organic package substrate is not enough to support the chips and a TSV-interposer is needed [42–54]. For example, Fig. 1.11 shows the Xilinx/TSMC's sliced FPBG chip-on-wafer-on-substrate (CoWoS) [50–53]. It can be seen that the TSV (10 μm-diameter) interposer (100 μm-deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000 + of lateral interconnections between the sliced FPGA chips are connected mainly by the 0.4 μm pitch (minimum) RDLs of the interposer. The minimum thickness of the RDLs and passivation is <1 μm. Each FPGA has more than 50,000 microbumps (200,000 + microbumps on the interposer) at 45 μm pitch as shown in Fig. 1.11.

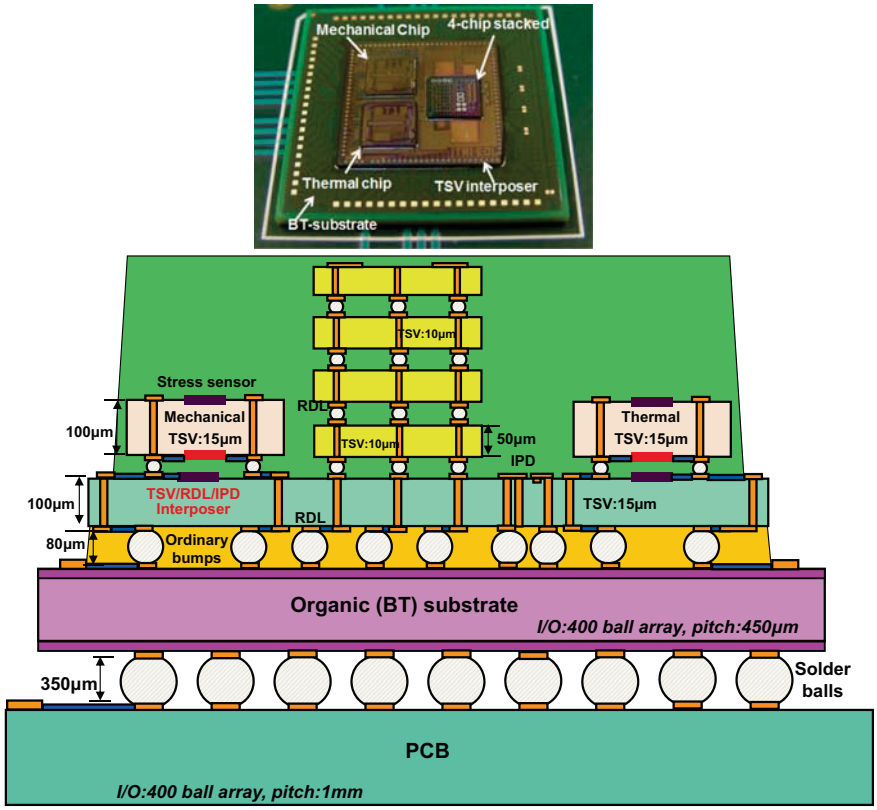


Fig. 1.10 ITRI's heterogeneous integration of memory cube, mechanical chip, and electrical chip

1.7.5 TSV/RDL Interposer with Chips on Both Sides

Figure 1.12 shows the 3D IC heterogeneous integration of an interposer that supported one CPU or ASIC chip on its top side and two memory chips on its bottom side [55–59]. TSVs are embedded in the interposer uniformly and the sizes are 25 μm in diameter, 150 μm in depth, and 150 μm in pitch; the thickness of passivation layer (SiO_2) on TSV sidewall is 0.5 μm. The interposer is attached to an organic substrate with ordinary bumps and the substrate is attached to a PCB (printed circuit board) with solder balls. The interposer is 28 mm × 28 mm × 150 μm, the CPU/ASIC is 22 mm × 18 mm × 400 μm, and the DRAM is 10 mm × 10 mm × 100 μm. The package substrate is 40 mm × 40 mm × 950 μm and the PCB is 114.3 mm × 101.6 mm × 1600 μm.

The diameter of micro solder bumps between all the chips and the interposer is 25 μm and on 250 μm pitch. The diameter of the ordinary solder bumps is 150 μm and on 250 μm pitch. The diameter of the solder balls is 600 μm and on 1000 μm

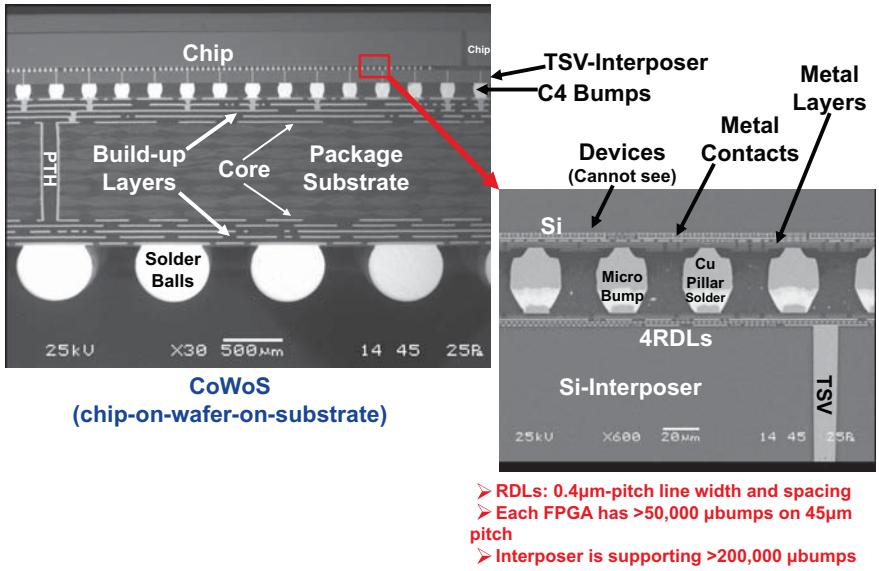


Fig. 1.11 Xilinx/TSMC's CoWoS

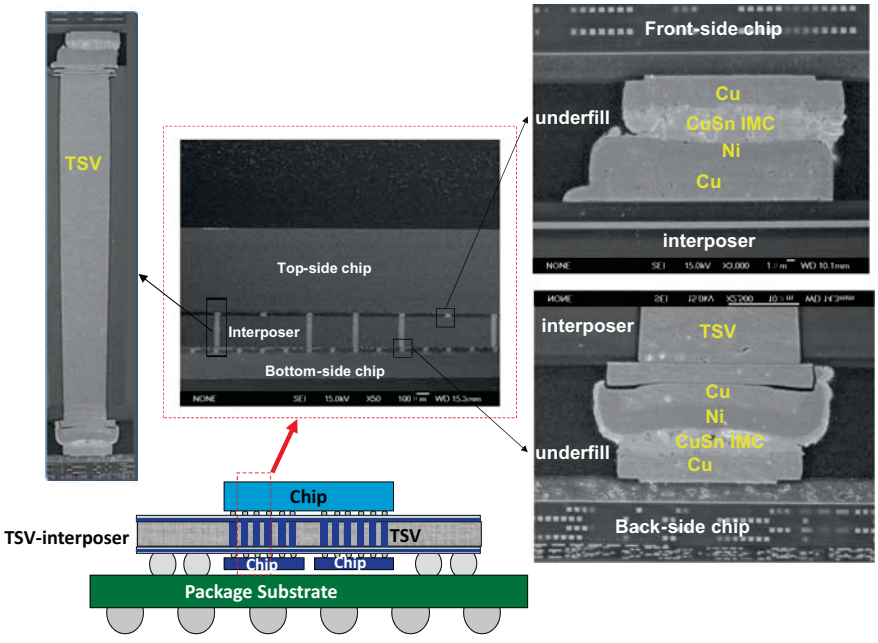


Fig. 1.12 TSV/RDL interposer with chips on both sides

pitch. The SEM image of a cross-section of the 3D IC heterogeneous integration assembly is shown in Fig. 1.12. It can be seen that there is a larger and thicker chip on the top side of the passive interposer and a smaller and thinner chip on its bottom side. The micro solder joint between the top chip and the interposer is also enlarged and shown in Fig. 1.12. It can be seen that: (a) the UBM on the interposer is Cu and Ni; (b) the solder becomes the IMC (intermetallic compound), Cu_6Sn_5; and (c) the Cu UBM from the larger chip. Similarly, the micro solder joint between the interposer with a TSV and the smaller chip is enlarged and shown in Fig. 1.12.

1.7.6 Interposer with Double-Sided Chip Attachments

The upper drawing of Fig. 1.13 shows the double-sided interposer for 3D IC heterogeneous integration of two chips on top and one chip at bottom [60–62]. The size of the package substrate is 35 mm × 35 mm × 970 μm. Underfills are used between the chips and interposer and the interposer and package substrate. The TSVs' diameter is 10 μm and on 150 μm pitch. The diameter of the solder bumps between the chips and interposer and between the interposer and package substrate is 90 μm and on 125 μm pitch. The diameter of the solder balls between the package substrate and the PCB is 600 μm and on 1000 μm pitch. The bottom images of Fig. 1.13 shows the cross-sections of the fully assembly module. It can be seen that the interposer is properly supporting the three chips with underfill. This interposer is soldered (with underfill) to a 4-2-4 package substrate.

1.7.7 AMD's GPU and Hynix's HBM on TSV-Interposer

Figure 1.14 shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28 nm process technology and is supported by four HBM cubes manufactured by Hynix. Each HBM consists of four DRAMs with Cu-pillar + solder cap bumps and a logic base with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28 mm × 35 mm), which is fabricated by UMC with a 64 nm process technology. The final assembly of the TSV interposer with C4 (controlled collapse chip connection) bumps on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

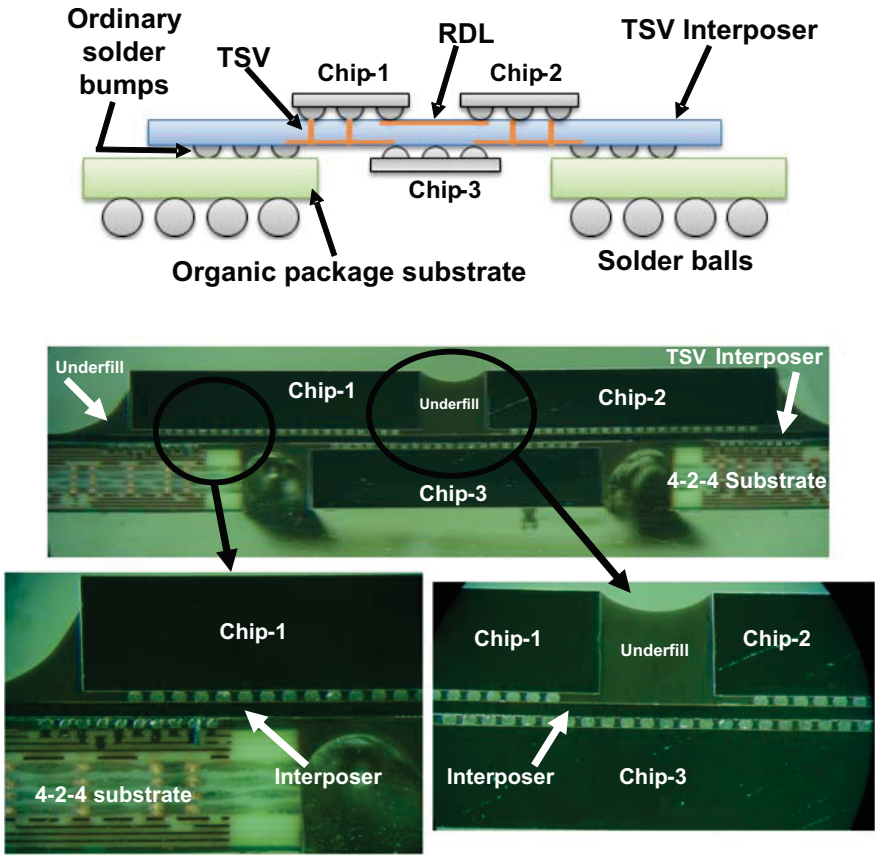


Fig. 1.13 Silicon interposer with double-sided chip attachments

1.7.8 NVidia's GPU and Samsung's HBM2 on TSV-Interposer

Figure 1.15 shows NVidia's Pascal 100 GPU, which was shipped in the second-half of 2016 [41]. The GPU is built on TSMC's 16 nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with Cu-pillar + solder cap bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are on top of a TSV interposer (1200 mm^2), which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with C4 bumps.

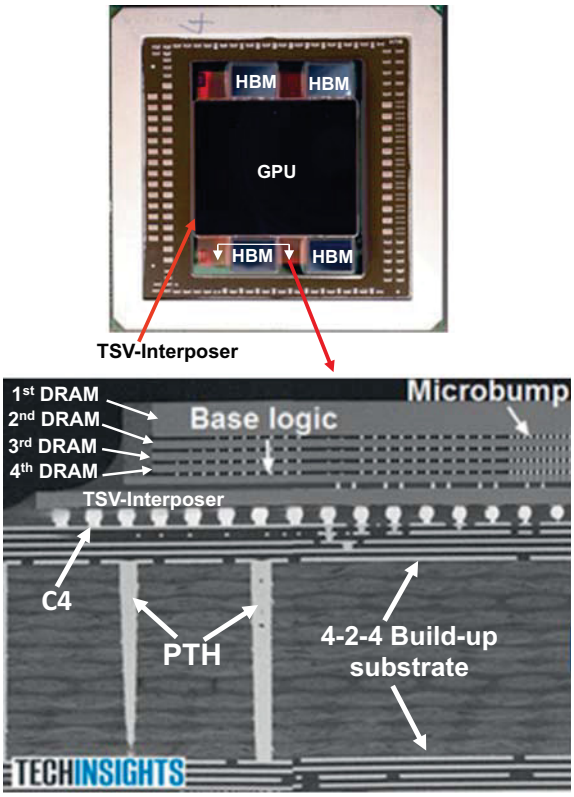


Fig. 1.14 AMD's heterogeneous integration of GPU and HBM

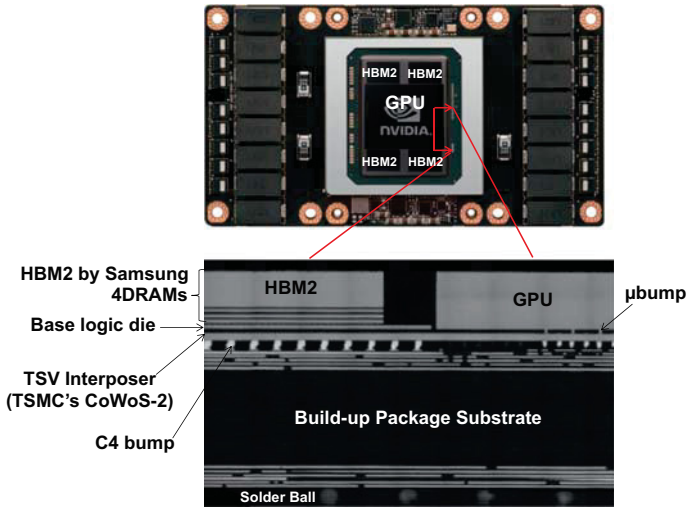


Fig. 1.15 NVidia's heterogeneous integration of GPU and HBM2

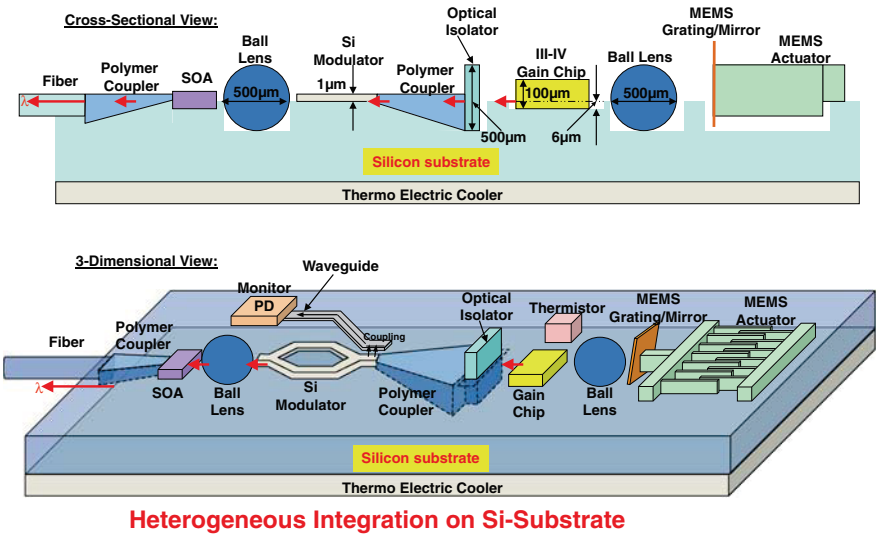


Fig. 1.16 IME's MEMS based tunable laser source with Si-modulator

1.7.9 IME's MEMS Based Tunable Laser Source on Si-Substrate

In 2007, IME proposed a MEMS based tunable laser source with Si-modulator, polymer couplers, and III-IV gain chip on a silicon optical bench, which is cooled by a thermoelectric cooler as shown schematically in Figure 1.16. The key features of the MEMS actuator are: driving voltage = 30 V @ 30 μm displacement, resonant frequency = 2.559 kHz, crosstalk < −60 dB, polarization dependent loss < 0.1 dB, wavelength-dependent loss < 0.05 dB, rising time = 75.6 μs, falling time = 63.4 μm, and reliability > 1×10^7 times. The key features of the Si-modulator are: total length = 3500 μm, splitter = 30 μm, combiner = 30 μm, modulator length ~3440 μm, cross section ~0.4 μm × 0.35 μm, designed maximum frequency > 20 GHz, and designed propagation loss < 20 dB/cm.

1.7.10 UCSB/AMD's Chiplets on TSV-Interposers

Excited by the Defense Advanced Research Projects Agency (DARPA) program called Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS), UCSB and AMD [63] proposed a future very high-performance system shown in Fig. 1.17. This system comprises a CPU chiplet and several GPU chiplets, as well as HBMs on a passive TSV-interposer and/or on an active TSV-interposer with RDLs.

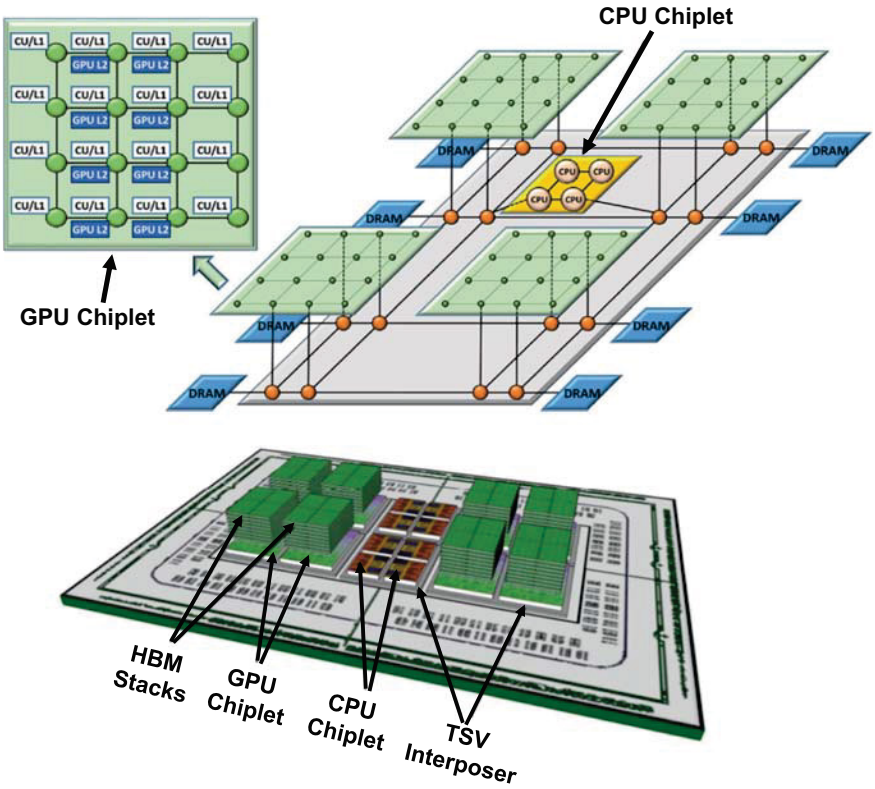


Fig. 1.17 UCSB/AMD's heterogeneous integration of GPU chiplets and CPU chiplet on TSV interposers

1.8 Heterogeneous Integration on Silicon Substrates (Bridges)

Basically, a bridge is a piece of dummy silicon with RDLs and contact pads, but without TSVs. Usually, the RDLs and contact pads are fabricated on a dummy silicon wafer and then diced into individual bridges. For more information on heterogeneous integration on silicon substrates (bridges), please read Chap. 4 of this book.

1.8.1 Intel's EMIB for Heterogeneous Integration

Intel proposed embedded multi-die interconnect bridge (EMIB) [30, 31] RDLs to replace the TSV-interposer in heterogeneous integration systems. The lateral communication between the chips will be taken care of by the silicon embedded bridge

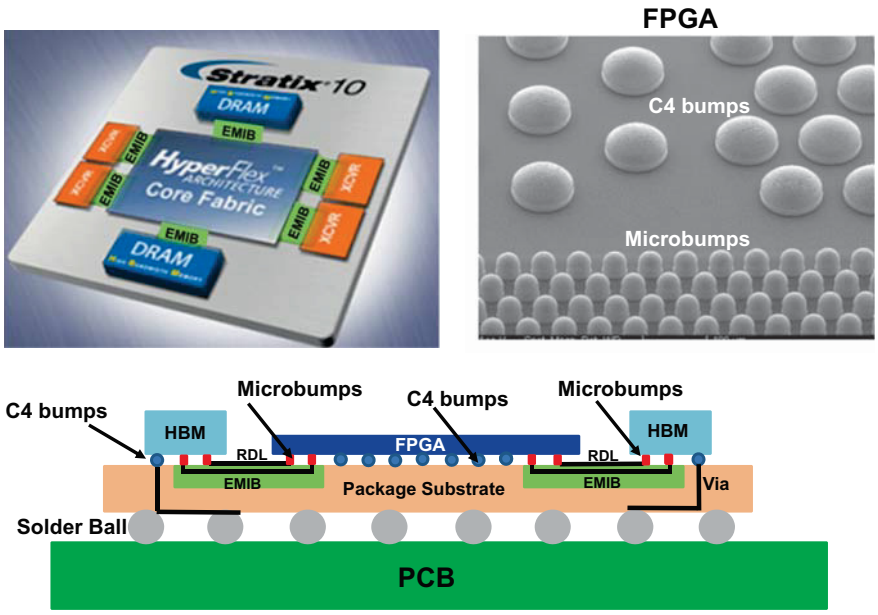


Fig. 1.18 Heterogeneous integration using Intel's EMIB and FPGA technology

with RDLs, and the power/ground and some signals will go through the organic package substrate (or PCB) as shown in Fig. 1.18. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB. To make the EMIB, one must first build the RDLs (including the contact pads on a Si wafer, which will be discussed in Sect. 4.3). Finally, attach the non-RDL side of the Si wafer to a die-attach film (DAF), and then singulate the Si wafer into individual bridges. To make the organic substrate with an EMIB, first place the singulated EMIB with the DAF on top of the Cu foil in the cavity of the organic substrate. That step is followed by the standard organic package substrate build-up process all the way to the Cu-contact pads (please read Sect. 4.4). The organic package substrate with the EMIB is ready for bonding of the chips such as the GPU and HBM cube, shown in Fig. 1.19.

1.8.2 Imec's Bridges for Heterogeneous Integrations

Ever since Intel's proposal of using EMIB to serve as the high-density interconnects between chips in a heterogeneous integration system was put forth, the "bridge" has been very popular. For example, recently, imec proposed [33] the use of the bridges + fan-out wafer-level packaging (FOWLP) technology to interconnect the logic chip,

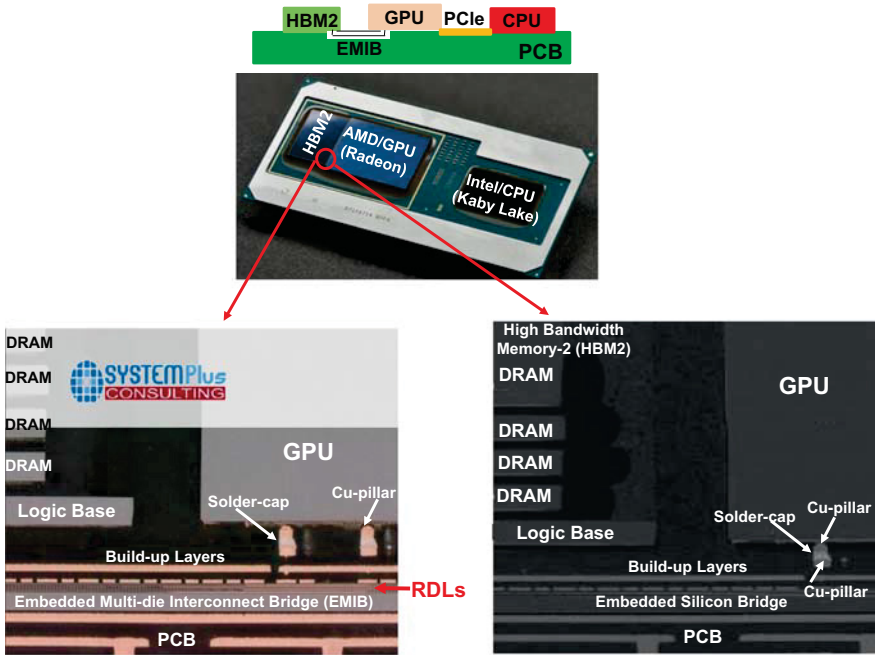


Fig. 1.19 Heterogeneous integration of Intel's CPU, AMD's GPU, and HBM with EMIB

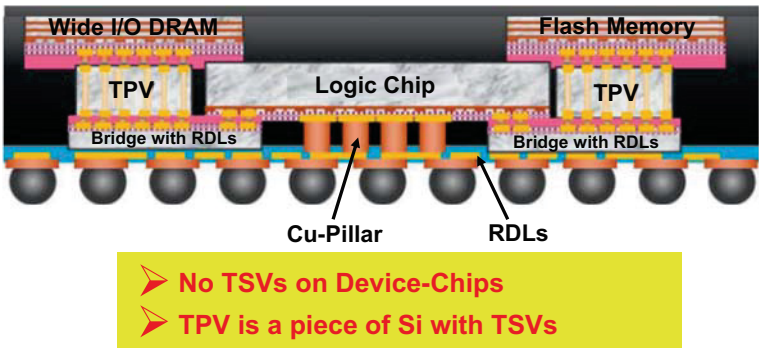


Fig. 1.20 Imec's heterogeneous integration system with silicon bridges

wide I/O DRAM, and the flash memory as shown in Fig. 1.20. Their objective is not to use TSVs for all the device chips.

1.8.3 ITRI's Bridge for Heterogeneous Integrations

Figure 1.21 shows a heterogeneous integration with a TSH (through silicon hole) interposer (a bridge) supporting a few chips on its top and bottom side [34]. The key feature of TSH interposers is that there is no metallization in the holes. Thus, dielectric layer, barrier and seed layers, via filling, CMP for removing overburden copper, and Cu revealing are not necessary. Comparing to the TSV interposers, TSH interposers only need to make holes (by either laser or DRIE) on a piece of silicon wafer. Just like the TSV interposers, RDLs are needed by the TSH interposers. The TSH interposers can be used to support the chips on its top side as well as bottom side. The holes can let the signals of the chips on the bottom side transmit to the chip on the top side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH interposer. Physically, the top chips and bottom chips are connected through Cu pillars and micro solder joints. Also, the peripherals of all the chips are soldered to the TSH interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom side of the TSH interposer have ordinary solder bumps which are attached to a package substrate. Figure 1.21 shows the SEM image of a cross-section of a SiP [34], which includes all the key elements such as the top chip, TSH interposer, bottom chip, package substrate, PCB, microbumps, solder bumps, solder ball, TSH, and Cu pillars. It can be seen through the X-ray and SEM images that the key elements of SiP structure are properly fabricated.

1.9 FOW/PLP for Heterogeneous Integrations

Fan-out wafer/panel level packaging (FOW/PLP) [111–131] is very suitable for heterogeneous integrations. Two examples, one for FOWLP and the other for FOPLP are briefly mentioned. For more information on FOW/PLP for heterogeneous integrations, please read Chap. 5 of this book.

1.9.1 FOWLP for Heterogeneous Integrations

Figure 1.22 shows a reconstituted wafer which consists of 629 (10 mm $\times$ 10 mm) packages [7, 21]. Each package has 4 (one 5 mm $\times$ 5 mm and three 3 mm $\times$ 3 mm) chips and 4 (0402) capacitors. The spacing between the large chip and the small chip is 100 μm. There are two RDLs for each package. It should be emphasized that FOWLP is a very high-throughput process. In this case, one shot, it can produce 629 10 mm $\times$ 10 mm packages. Figure 1.23 shows the cross section of the package. It can be seen that there are two RDLs and the thickness of the metal layer of RDL1 is 3 μm and that of RDL2 is 7.5 μm. The linewidth and spacing of RDL1 are 10 μm

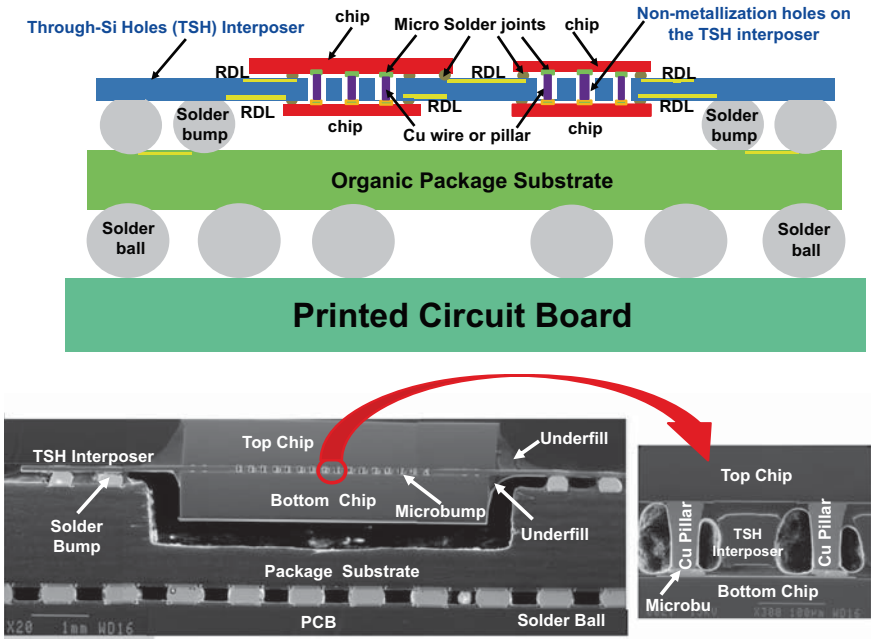


Fig. 1.21 ITRI's bridge (TSH-interposer) for heterogeneous integrations

and those of RDL2 are 15 μm. The dielectric layer thickness of DL1 and DL2 is 5 μm, and DL3 is 10 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm, and the ball pitch is 0.4 mm.

1.9.2 FOPLP for Heterogeneous Integrations

Figure 1.24 shows a reconstituted panel which consists of 1512 (10 mm × 10 mm) packages [3, 22]. Again, each package has 4 (one 5 mm × 5 mm and three 3 mm × 3 mm) chips. Figure 1.25 shows the x-ray image and the cross section of the package. It can be seen that there are two RDLs and the thickness of the metal layer of RDL1 and RDL2 is 10 μm. The linewidth and spacing of RDL1 are 20 μm and those of RDL2 are 25 μm. The dielectric layer thickness of DL1, DL2, and DL3 is 20 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm, and the ball pitch is 0.4 mm.

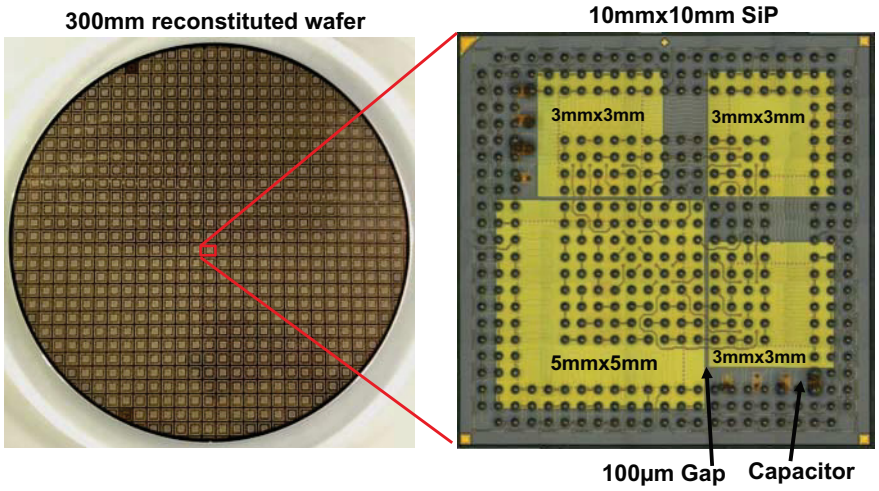


Fig. 1.22 Heterogeneous integration of 4 chips by FOWLP

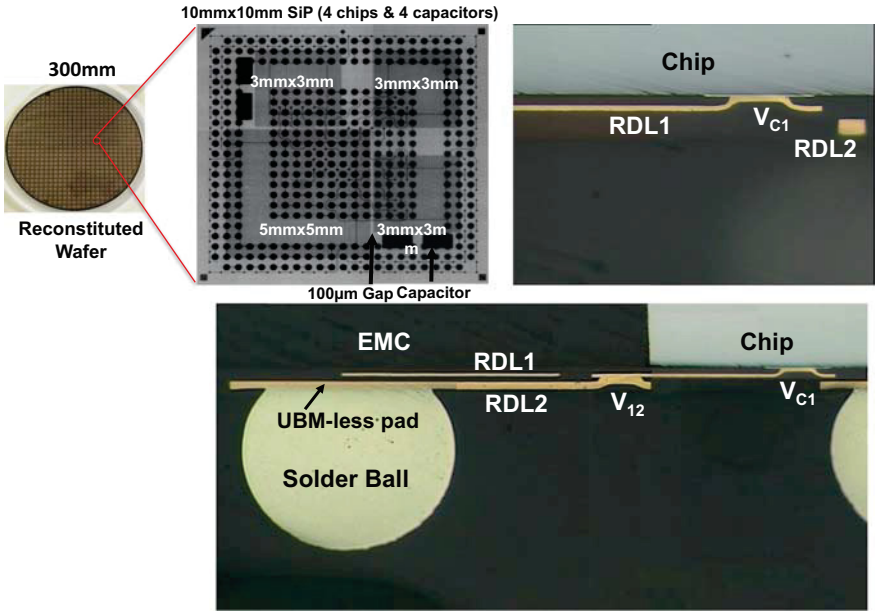


Fig. 1.23 Cross section of the heterogeneous integration package (by FOWLP) showing the RDLs

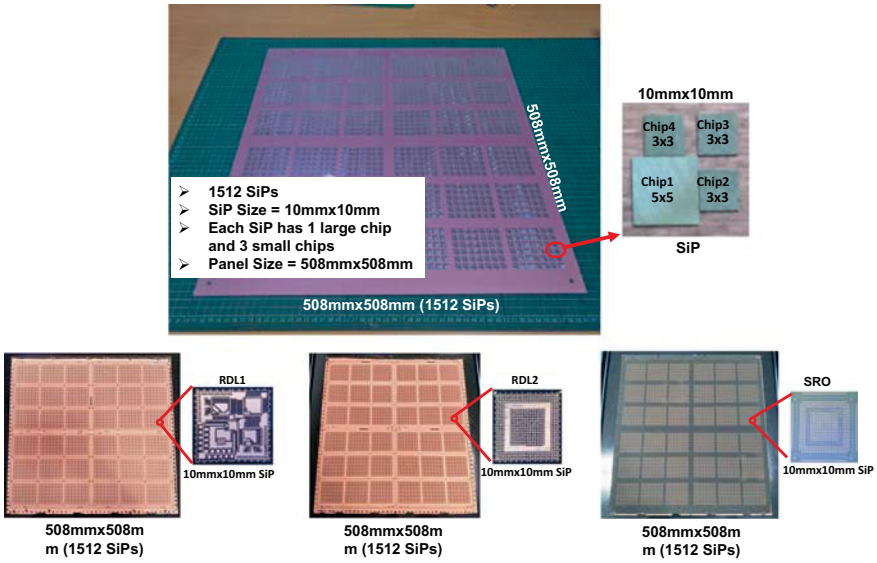


Fig. 1.24 Heterogeneous integration of 4 chips by FOPLP

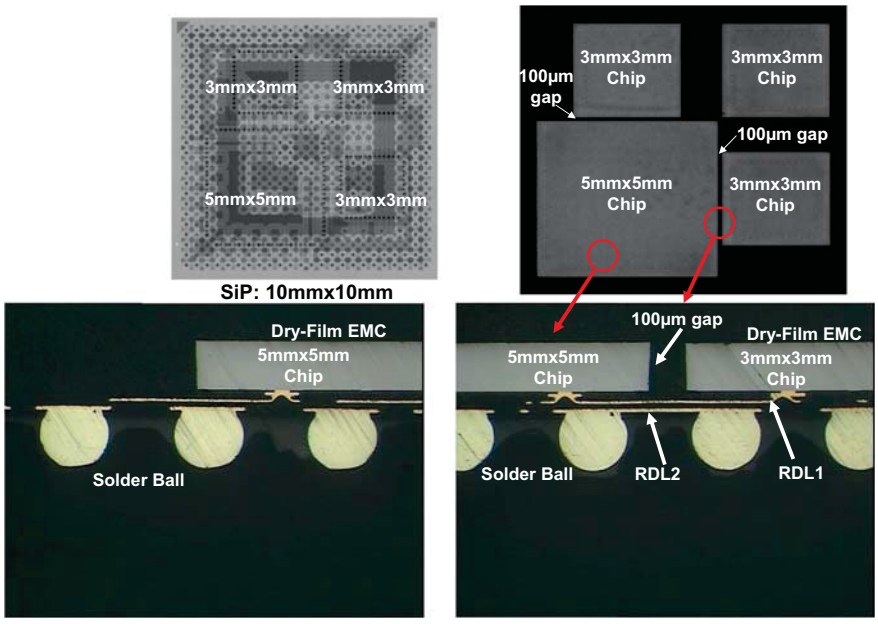


Fig. 1.25 Cross section of the heterogeneous integration package (by FOPLP) showing the RDLs

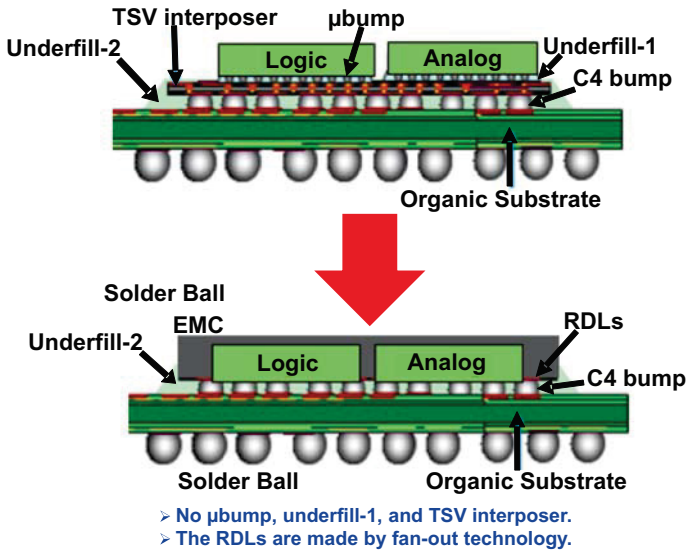


Fig. 1.26 STATSChipPac's fan-out RDL substrate (FOFC-eWLB)

1.10 Heterogeneous Integrations on Fan-Out RDL Substrates

Recently, in order to lower the package profile, enhance the performance, and lower the cost, the heterogeneous integration on RDLs have been very popular, especially with the FOWLP technology. In general, this is for middle-end to high-end applications. For more information on heterogeneous integrations on fan-out RDL substrates, please read Chap. 6 of this book.

1.10.1 STATSChipPAC's FOFC-eWLB

At ECTC2013, STATSChipPAC proposed [26, 132] using the fan-out flip chip (FOFC)-eWLB to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 1.26. It can be seen that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated.

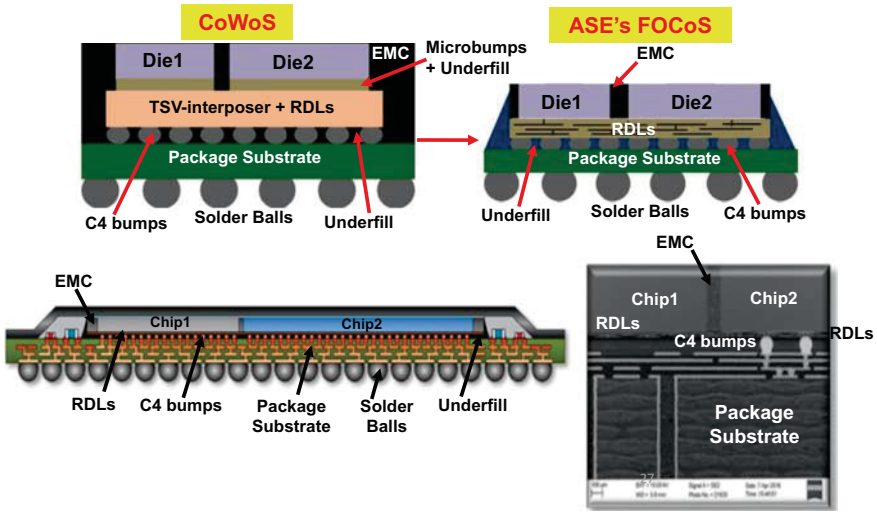


Fig. 1.27 ASE's FOCoS

1.10.2 ASE's FOCoS

In 2016, ASE [27] proposed using the fan-out wafer-level packaging (FOWLP) technology (chip-first and die-down on a temporary wafer carrier and then overmolded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 1.27; the technology is called fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 bump as shown in Fig. 1.27.

1.10.3 MediaTek's RDLs by FOWLP

In 2016, MediaTek [133] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in Fig. 1.28. Instead of the C4 bump, they used a microbump (Cu pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate.

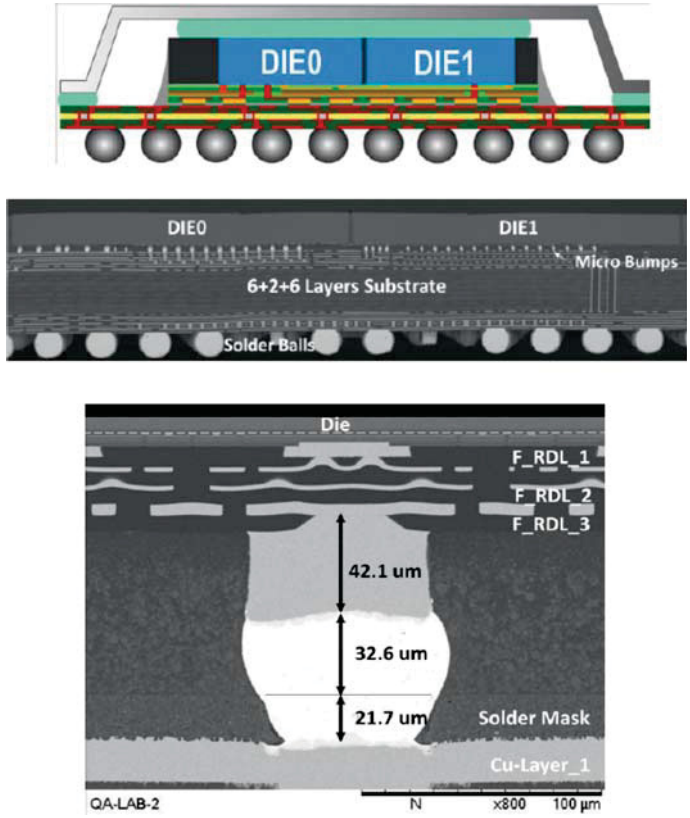


Fig. 1.28 MediaTek's fan-out RDL substrate

1.10.4 Samsung's Si-Less RDL Interposer

Recently, Samsung [32] proposed using chip-last or RDL-first FOWLP to eliminate the TSV-interposer as shown in Fig. 1.29. First of all, they build the RDL on a silicon or glass wafer. In parallel, wafer bumping of the logic and HBM. Then, perform fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing. It is followed by EMC compression molding. Then, backgrind the silicon wafer and C4 wafer bumping. It is followed by attaching the whole module on the package substrate. Finally, perform solder ball mounting and lid attachment.

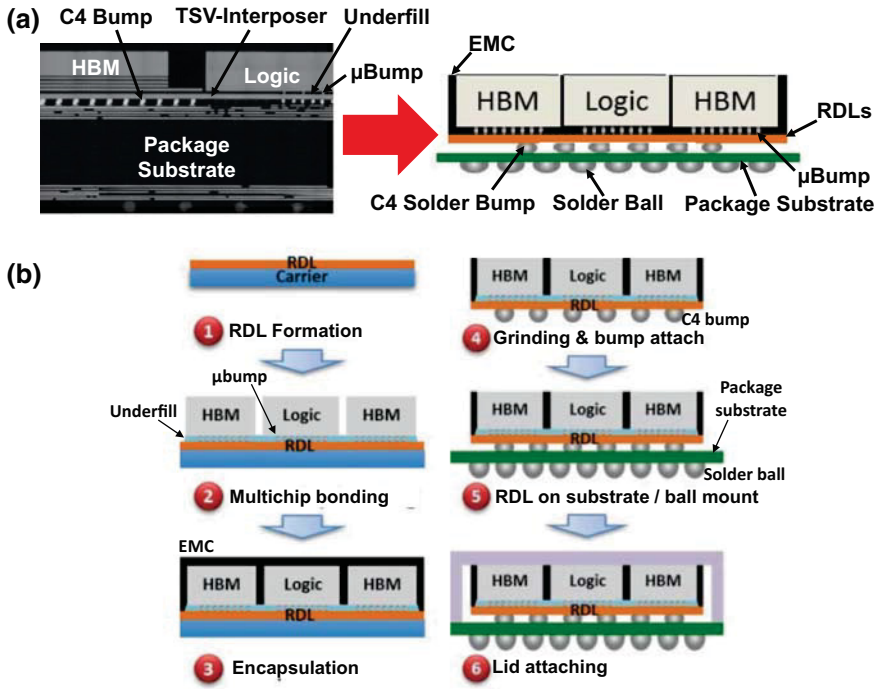


Fig. 1.29 Samsung's fan-out (chip-last) substrate (Si-less RDL interposer)

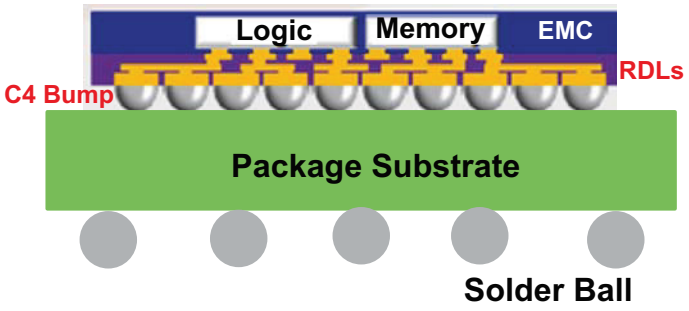
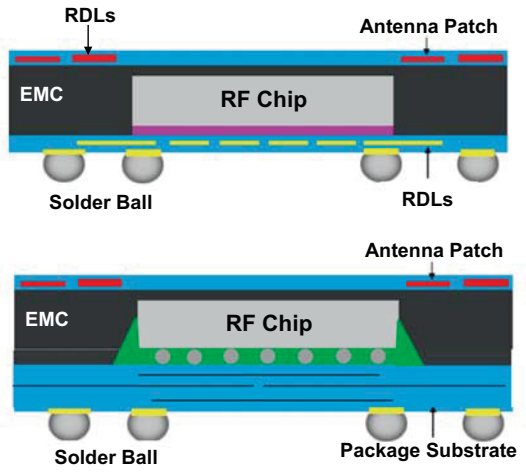


Fig. 1.30 TSMC's InFO_oS (integrated fan-out on substrate)

1.10.5 TSMC's InFO_oS

Figure 1.30 shows the schematic of TSMC's InFO_oS (integrated fan-out on substrate) [134]. The RDLs are fabricated by TSMC's InFO chip-first and die face-up technology. This InFO_oS is for high performance applications but not as high as those with CoWoS technology.



THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

Frequency	InFO RDLs	Substrate Trace
28GHz	0.175dB/mm	0.288dB/mm
38GHz	0.225dB/mm	0.377dB/mm

Fig. 1.31 TSMC's AiP with InFO and compare with flip chip on substrate

1.11 Heterogeneous Integration of AiP and Baseband Chipset

Two examples of heterogeneous integration of AiP (antenna-in-package) by FOWLP are briefly mentioned. One is by TSMC and the other is a new proposal.

1.11.1 TSMC's AiP with FOWLP

TSMC [135] demonstrated that the InFO_AiP for high performance and compact 5G millimeter wave system integration is superior than that of solder bumped flip chip AiP on substrate as shown in Fig. 1.31. It can be seen that: (a) in the 28 GHz frequency range, InFO RDLs transmission loss (0.175 dB/mm) is 65% less than that on flip chip substrate trace (0.288 dB/mm), and (b) in the 38 GHz frequency range, the transmission loss for InFO RDLs (0.225 dB/mm) is 53% less than that (0.377 dB/mm) on flip chip substrate trace.

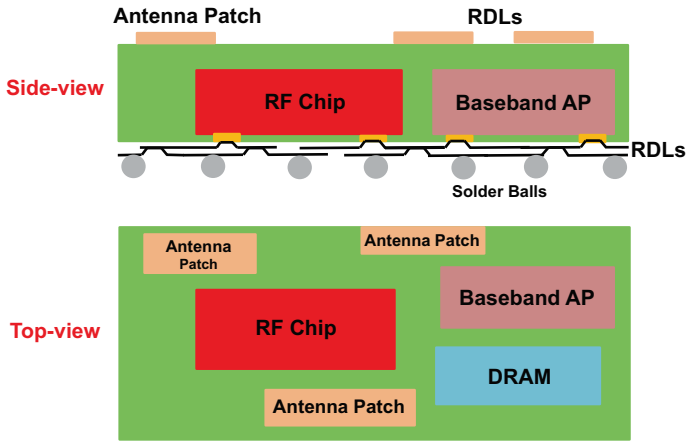


Fig. 1.32 A proposal on heterogeneous integration of RF chip, baseband AP, DRAM, and AiP

1.11.2 Heterogeneous Integration of AiP and Baseband Chipset

Figure 1.32 schematically shows a heterogeneous integration of AiP and baseband chipset by FOWLP, It can be seen that the RF Chip and the baseband chipset (modem AP and the DRAM) are placed side-by-side with RDLs and coupled with the antenna patches.

1.12 Heterogeneous Integration of PoP

PoP (package-on-package) is one of the heterogeneous integrations. A few heterogeneous integration of PoPs are briefly mentioned in this section. For more information on heterogeneous integration of PoP, please read Chap. 7 of this book.

1.12.1 Amkor/Qualcomm/Shinko's PoP

High-bonding force thermocompression of the Cu-pillar + solder cap bumps with nonconductive paste (TC-NCP) underfill on the substrate was first studied by Amkor [136] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone for the bottom package of a PoP as shown in Fig. 1.33. The NCP underfills can be spun on, dispensed by a needle, or vacuum assisted. The molded core embedded package (MCeP) substrate was manufactured by Shinko.

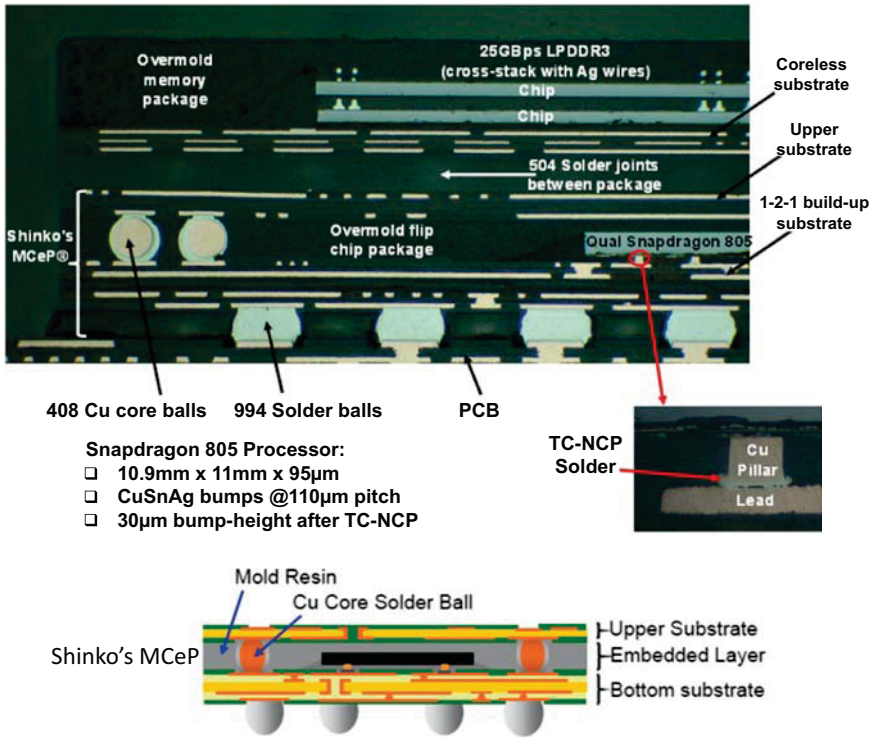


Fig. 1.33 Amkor/Qualcomm/Shenko's PoP with TC-NCF

1.12.2 Apple/TSMC's PoP for AP A10

Figure 1.34 shows the cross section of iPhone 6 Plus. It can be seen that the A9 application processor is housed in a PoP format and the solder bumped flip chip is mass reflowed on a 2-2-2 organic package substrate and then underfilled. Figure 1.35 shows the cross section of iPhone 7.

Figure 1.35 shows the schematic and scanning electron microscope (SEM) images of the cross section of the PoP that houses the Apple A10 AP and mobile dynamic random access memories (DRAMs) of the iPhone 7/7+. This PoP is fabricated by TSMC with its InFO WLP technology [94–96]. It can be seen from the bottom package that the wafer bumping, fluxing, flip-chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the A9 AP shown in Fig. 1.34) have been eliminated and are replaced by the RDLs (for the A10 AP as shown in Fig. 1.35). This results in a lower cost, higher performance, and lower profile package. For the packaging of A11 and A12, please read Chap. 7.

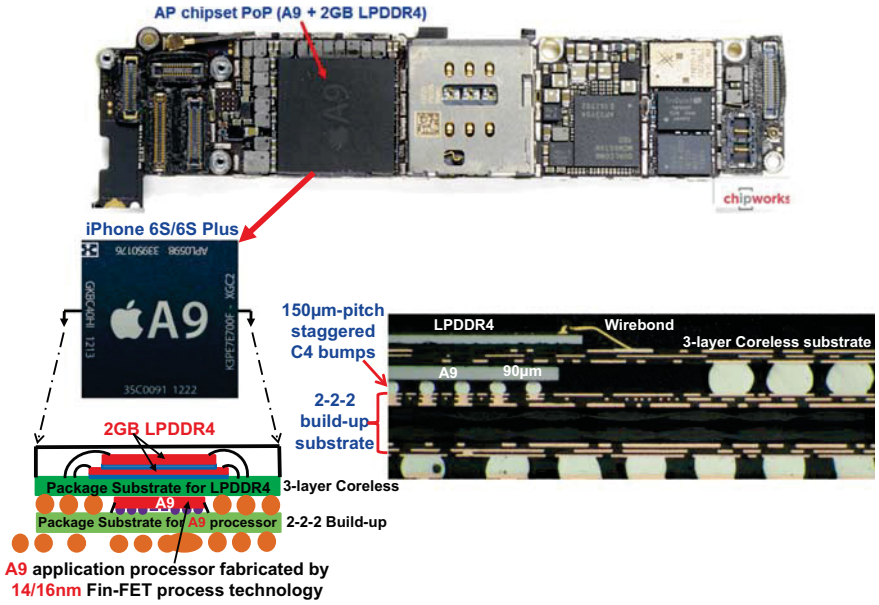


Fig. 1.34 Apple's PoP with solder bumped flip chip on substrate for the AP

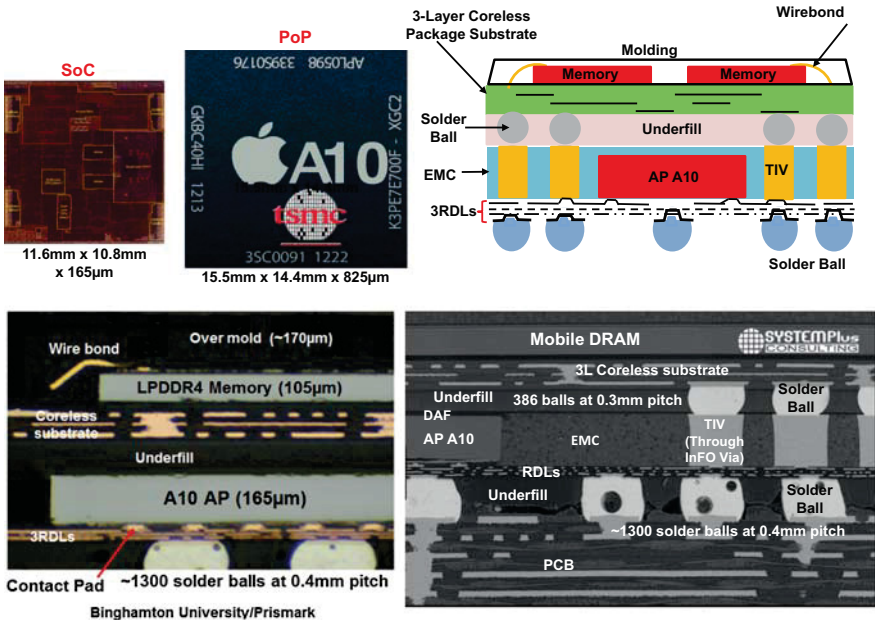


Fig. 1.35 Apple/TSMC's PoP with InFO for the AP

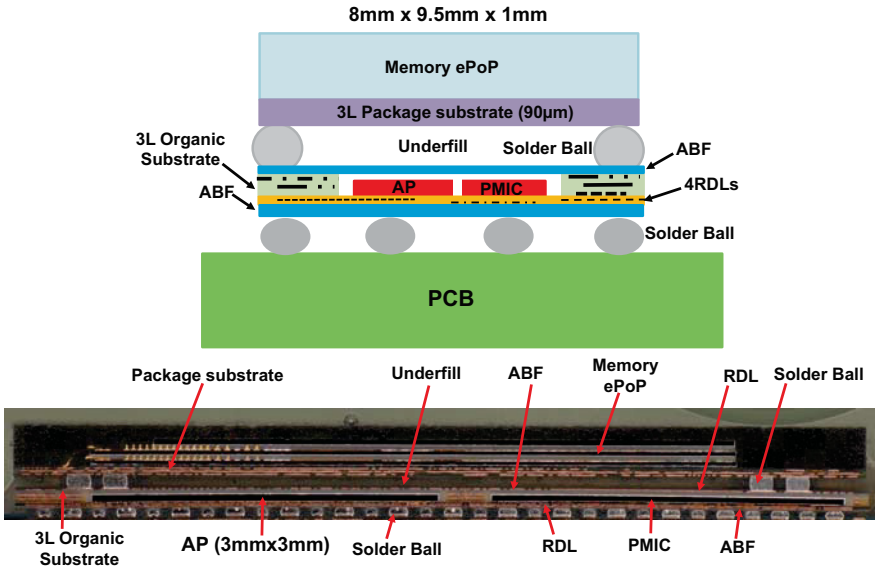


Fig. 1.36 Samsung's PoP for the luxury smart watch. The AP and PMIC are packaged with Samsung's FOPLP

1.12.3 Samsung's PoP for Smartwatch

Figure 1.36 shows Samsung's luxury smart watch shipped in July 2018. It is a PoP. It can be seen that the upper package is housing the memory ePoP which consists of 2 DRAMs, 2 NANDs and one controller. The bottom package is housing the AP and PMIC (power management IC) in the cavity of a 3-layer organic substrate by their fan-out panel level packaging. There are underfills between the upper and bottom packages. The chip size of the AP and PMIC is about 3 mm × 3 mm.

1.13 Heterogeneous Integration of Memory Stacks

1.13.1 Heterogeneous Integration of Memory Chips by Wire Bonding

Figure 1.37 shows the heterogeneous integration of two memory chips and a logic chip [137]. They are stacked by wire bonding. The assembly and reliability will be shown in Chap. 8.

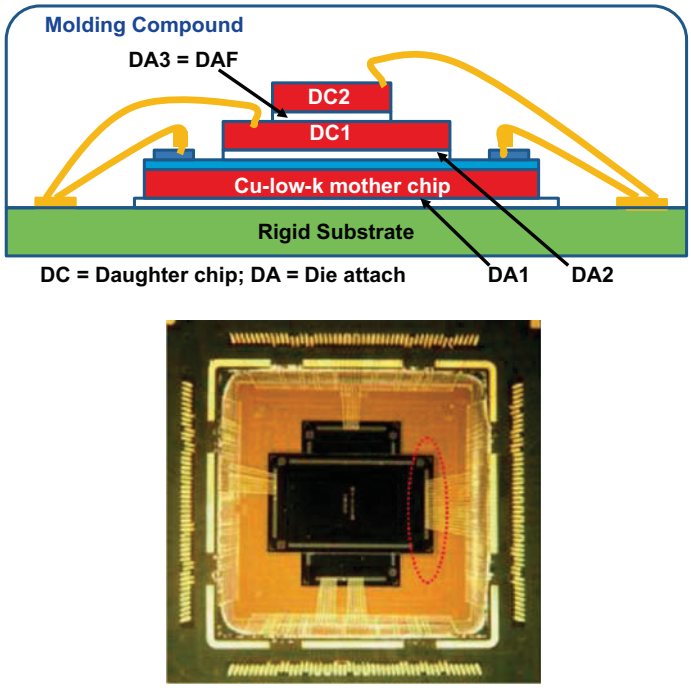


Fig. 1.37 IME's heterogeneous integration of three chips with wire bonding

1.13.2 Heterogeneous Integration of Memory Chips by Low Temperature Bonding

Figure 1.38 shows the heterogeneous integration of memory chips and a logic chip. They are stacked by low temperature bonding [138]. The assembly and reliability are shown in Chap. 8.

1.14 Heterogeneous Integration of Chip-to-Chip Stacks

1.14.1 Intel's Modem Chipset for iPhone XR

Figure 1.39 shows the modem chipset by Intel for the second most important chipset of the iPhone XR. It can be seen that the baseband AP is solder bumped flip chip on a 3-layer ETS (embedded trace substrate). The DRAM is die attached on the backside of the AP and is wire bonded on the ETS. This is an example of chip-to-chip and back-to-back.

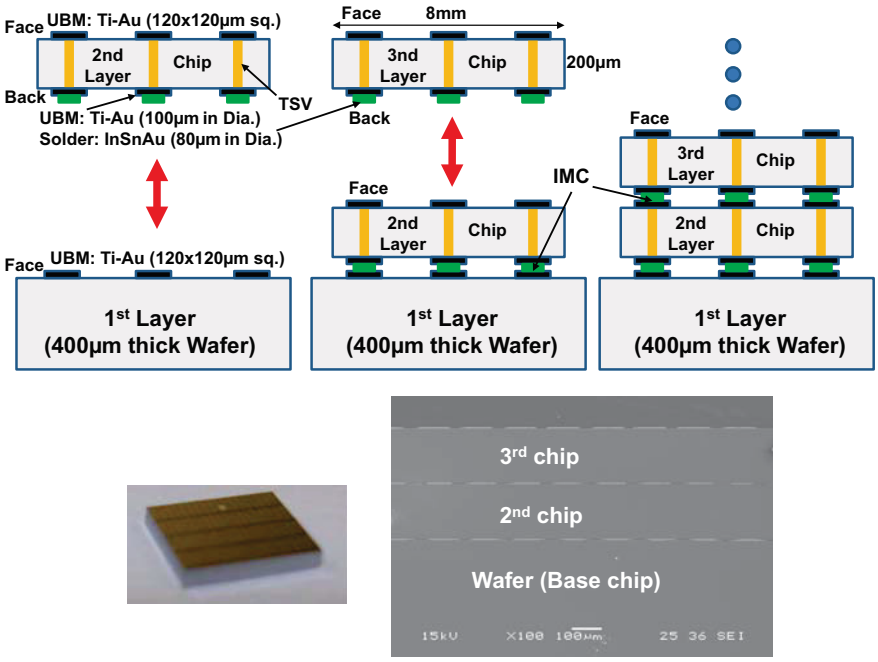


Fig. 1.38 IME's heterogeneous integration of a few chips with low temperature bonding

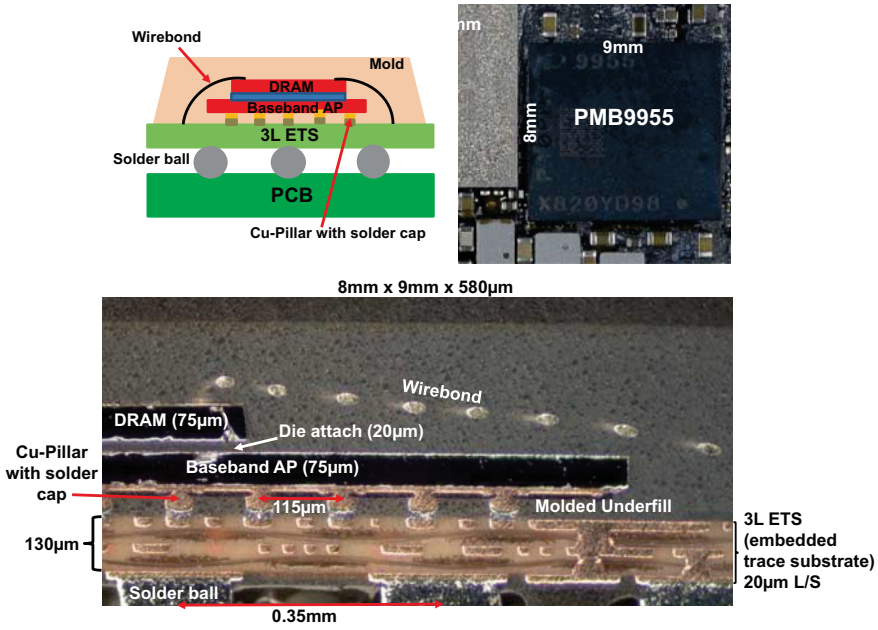


Fig. 1.39 Intel's heterogeneous integration of the modem chipset (baseband AP and DRAM)

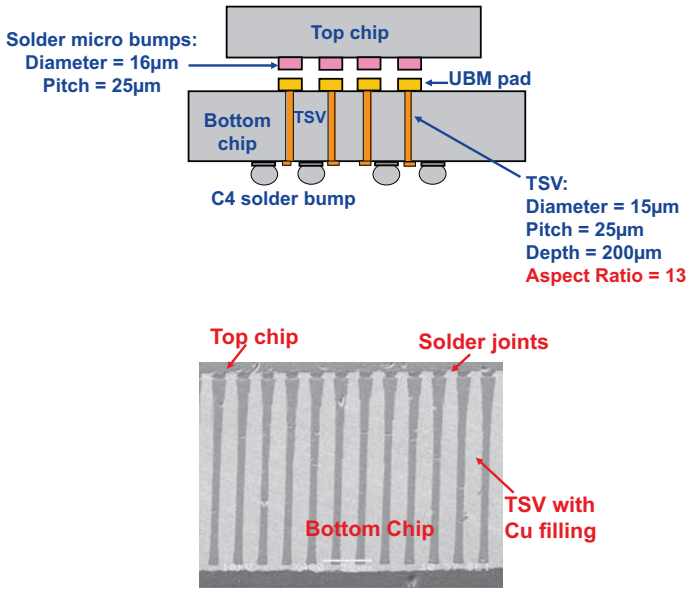


Fig. 1.40 IME's face-to-face and chip-to-chip (with TSV) heterogeneous integration

1.14.2 IME's Chip-to-Chip Stack with TSVs

Figure 1.40 shows the heterogeneous integration of chip-to-chip and face-to-face [139, 140]. The top chip could be a memory and the bottom chip could be a logic with TSVs. The assembly and characteristic can be found in Chap. 9

1.14.3 IME's Chip-to-Chip Stack Without TSV

Figure 1.41 shows the heterogeneous integration of chip-to-chip and face-to-face but without TSVs [141, 142]. The connection to the substrate is through the solder ball on the larger (mother) chip. Please see Chap. 9 for more assembly and reliability information.

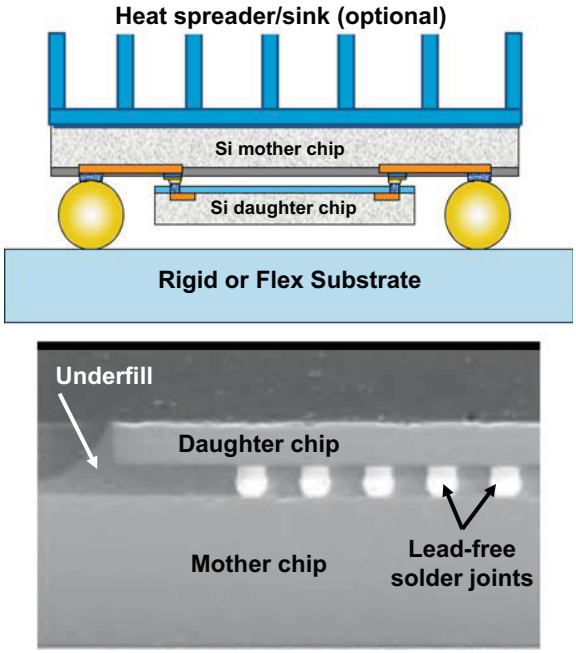


Fig. 1.41 IME's chip-to-chip and face-to-face (without TSV) heterogeneous integration

1.15 Heterogeneous Integration of CIS

1.15.1 Heterogeneous Integration of Sony's CIS

Sony is the first to use Cu-Cu direct hybrid bonding (which bonds the metal pads and dielectric layer on both sides of the wafers at the same time) in HVM. Sony produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results [143] showed that their robust Cu-Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A cross section of the IMX260 BI-CIS is shown in Fig. 1.42. It can be seen that, unlike in [144] for Sony's ISX014 stacked camera sensor, the TSVs are gone and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu-Cu direct bonding. The signals are coming from the package substrate with wire bonds to the edges of the processor chip. Please read Chap. 10 for more information.

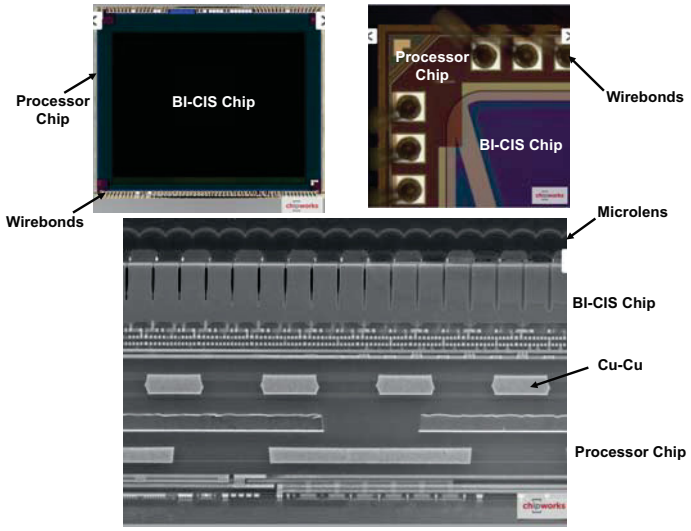


Fig. 1.42 Cross section image of Sony's CIS heterogeneous integration by Cu-Cu hybrid bonding

1.15.2 Heterogeneous Integration of STMicroelectronics' CIS

Figure 1.43 shows a 3D CIS and IC integration presented in [145]. It consists of the CIS, coprocessor IC, and glass carrier. The I/O count of the CIS is 80 and that of the IC is 164. The size of the CIS and the coprocessor is not the same. The dimensions of the CIS are 5 mm × 4.4 mm and of the IC are 3.4 mm × 3.5 mm. The IC and the CIS are bonded face-to-back, as shown in Fig. 1.43. The interconnects of the CIS and IC are Cu-pillar with SnAg solder cap. The TSVs are in the CIS, which are connected to the substrate with solder bump and RDLs. Figure 1.43 shows the 3D prototypes during the assembly process (balling first): mounted IC coprocessors and untreated sites. For more information, please read Chap. 10.

1.16 Heterogeneous Integration of LED

1.16.1 Heterogeneous Integration of HKUST's LED

Figure 1.44 shows the top view and cross-section view of a Si-substrate with cavity for phosphor printing and Cu-filled TSVs for interconnection LED [146, 147]. It can be seen that the Si-substrate is about 400 μm thick with 3 μm-thick low temperature oxide on both sides. The dimensions of the cavity are 1.3 mm × 1.3 mm × 0.22 mm.

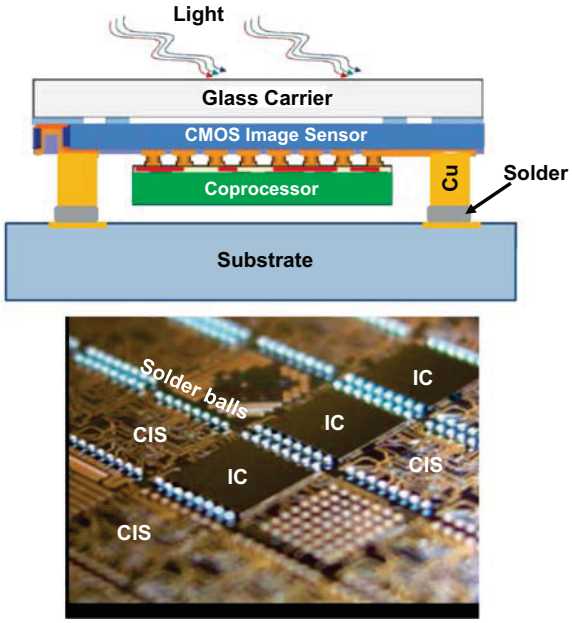


Fig. 1.43 STMicroelectronics' (face-to-back) CIS heterogeneous integration

The diameter of the TSV is 100 μm and is filled with Cu. The exposed tip of the Cu TSV is 30 μm and plated with solder. Figure 1.44a, b and c show the images, respectively, of the top-view and cross-sectional view of the LED package. The Si-substrate, the RDL, the cavity, and the TSV tips with solder bumps (before LED mounting) can be clearly seen. Please see Chap. 10 for more information.

1.16.2 Heterogeneous Integration of JCAP's LED

Figure 1.45 schematically shows a wafer level packaging with LED devices in the cavities of a Si substrate [148, 149]. It can be seen that the Si-substrate has cavities on its top side to house the LED devices and TSVs to connect the LEDs to the RDLs on its bottom side. The Si-substrate is covered by a glass with yellow phosphor. Figure 1.45 shows the SEM images of the cross-section of the LED package without phosphor. It can be seen that: (a) the LED device is attached on the bottom of the cavity of the Si-substrate, (b) the glass is bonded on the top of the Si-substrate, (c) the LED pads are connected to the RDL through the TSV with contactor size of about 20 μm, and (d) the encapsulation separates the Si-substrate from the RDL, which prevents electrical shortage between the cathode and the anode. For more information please read Chap. 10.

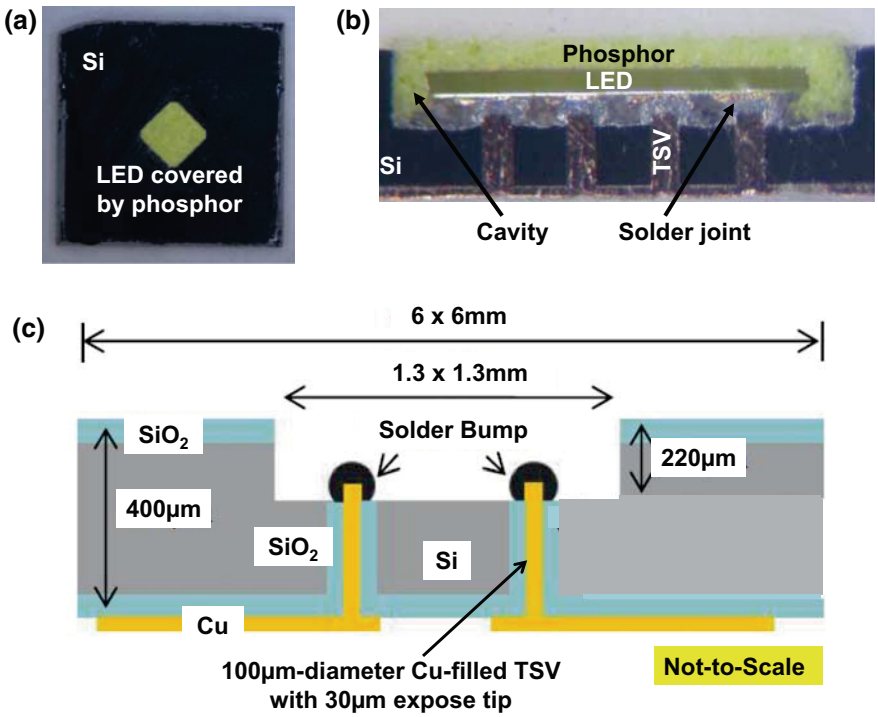


Fig. 1.44 HKUST's heterogeneous integration of LED on TSV interposer

1.17 Heterogeneous Integration of MEMS

1.17.1 Heterogeneous Integration of IME's MEMS

Figure 1.46 shows the cross-section and bird-view of the wafer-level packaging of a RF MEMS device [150, 151]. It consists of the MEMS wafer (RF MEMS device, high resistivity silicon (HR-Si) substrate with RDLs, and AuSn solder for sealing ring and bonding pads) and the cap wafer (cap with a cavity, TSVs, and RDLs, and the solder bump). It is a 2.25D MEMS and IC integration. Main objective of [150, 151] is to study the insertion loss of RF-MEMS wafer during packaging with TSV cap wafer. Two different types of CPW (coplanar waveguide) structures (1 mm-CPW and 2 mm-CPW), as shown in Fig. 1.46, are designed and fabricated. Please read Chap. 10 for more information.

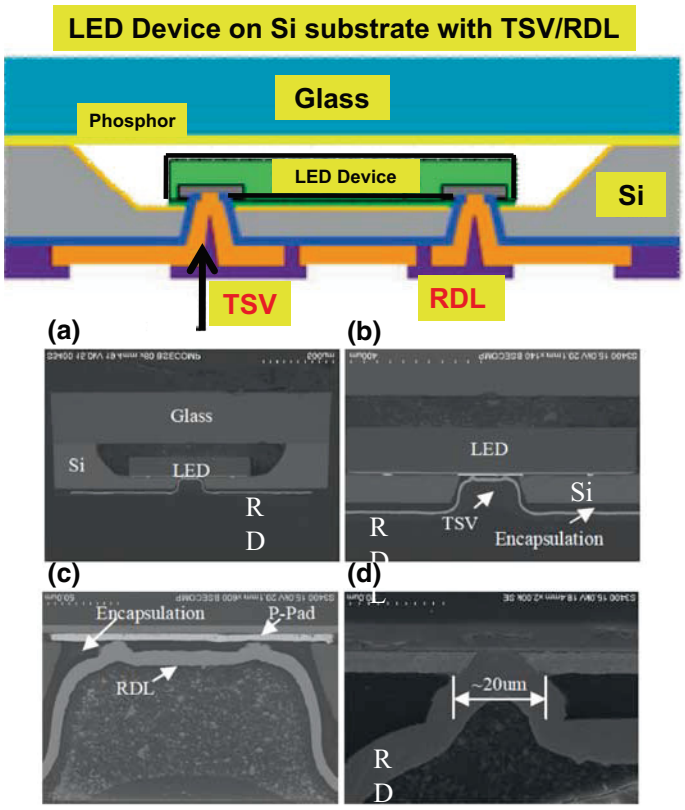


Fig. 1.45 JCAP's heterogeneous integration LED on TSV interposer

1.17.2 Heterogeneous Integration of Imec's MEMS

Figure 1.47 shows the zero-level packaging for RF-MEMS device [152, 153]. It consists of the RF-MEMS, HR-Si substrate with RDLs, and Cu-Sn-Cu for sealing ring and bonding pads, the HR-Si cap with TSVs and RDLs, and the solder bump. Again, it is a 2.25D MEMS package. One of the main objectives of [152, 153] is to study the bonding characteristics (sealing ring and interconnect bumps) of the MEMS wafer and the cap wafer.

1.17.3 Heterogeneous Integration of IZM's MEMS

Figure 1.48 schematically shows a MEMS package based on interposer wafer [154]. It can be seen that the MEMS device is attached to a Si-interposer wafer with Cu-

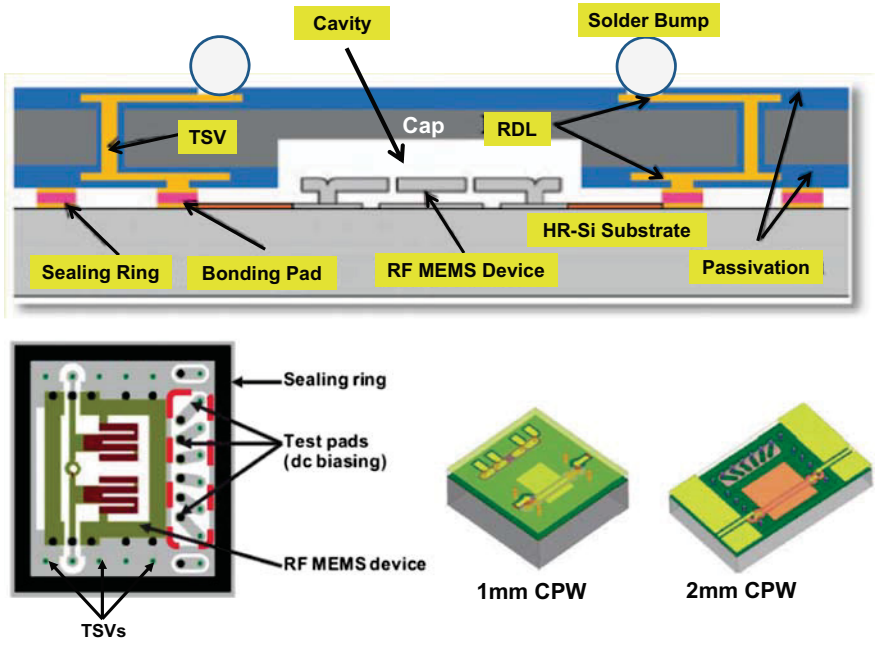


Fig. 1.46 IME's 3D MEMS packaging with lateral electrical feed-through

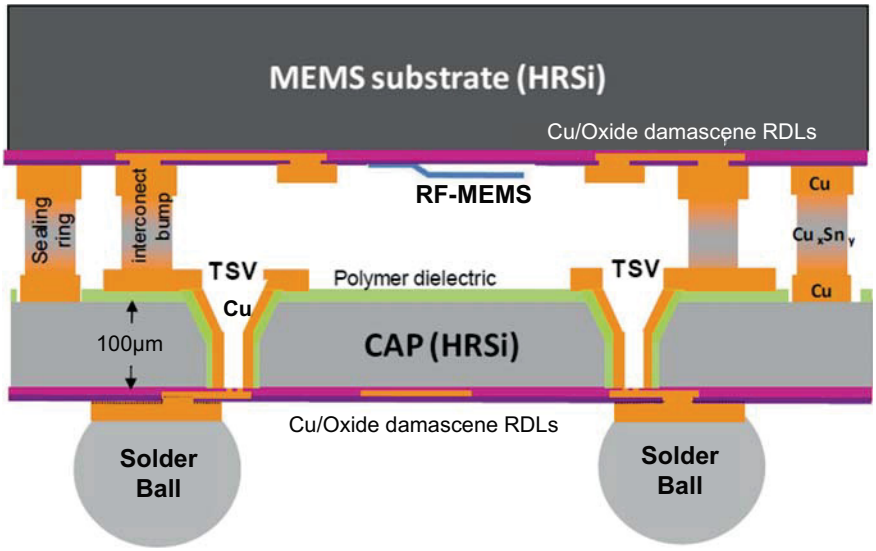


Fig. 1.47 Imec's heterogeneous integration of MEMS and cap with TSV

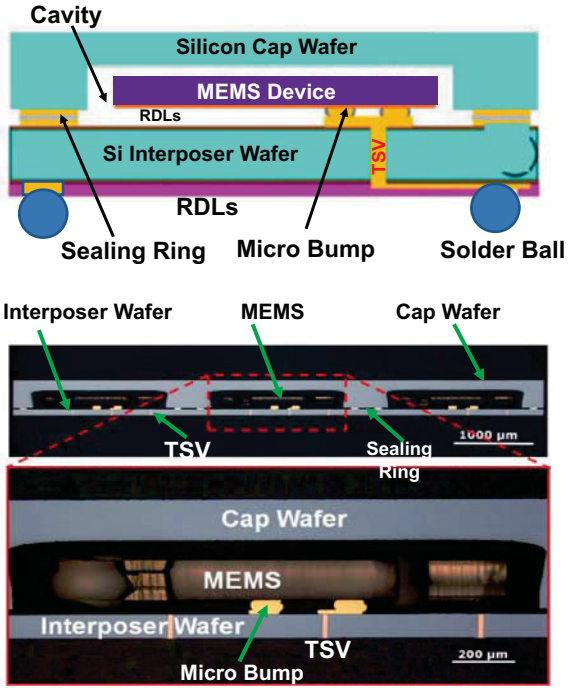


Fig. 1.48 IZM's heterogeneous integration of MEMS on TSV interposer

filled TSVs and RDLs and is hermetic sealed with a cap wafer with cavity. This is a 2.5D MEMS and IC integration. A typical cross-section image of the final assembly is shown in Fig. 1.48. It can be seen that all the key elements of the MEMS package, such as the MEMS device, Si interposer, TSV, microbump, and sealing ring, are in proper position.

1.17.4 Heterogeneous Integration of Discera's MEMS

Discera produced the MEMS resonator with TSVs shown in Fig. 1.49. It can be seen that: (a) the MEMS resonator is right on top of the ASIC, (b) the connections between the ASIC and the TSV are by wirebonds, and (c) the TSVs are in the Si substrate of the MEMS resonator.

1.17.5 Heterogeneous Integration of Analog Devices' MEMS

Figure 1.50 shows the heterogeneous integration of the MEMS device and the ASIC provided by Analog Devices. It is assembled by chip (MEMS) to (ASIC) wafer

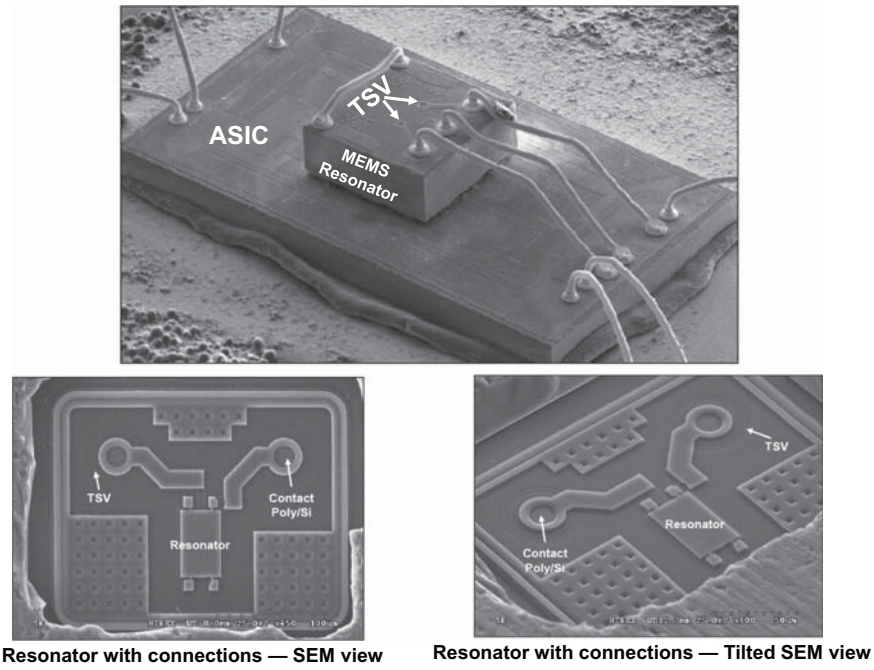


Fig. 1.49 Discera's heterogeneous integration of MEMS with TSV on ASIC

bonding. The interconnection between the MEMS and the ASIC is by RDLs and TSVs.

1.17.6 Heterogeneous Integration of IME's MEMS

Figure 1.51 shows the heterogeneous integration of the MEMS device on ASIC and is hermetic sealed by a silicon cap [155]. It is assembled by chip (MEMS) to (ASIC) wafer bonding and (cap) wafer to (ASIC with MEMS) wafer bonding. For the assembly and characterization of the MEMS package, please read Chap. 10.

1.17.7 Heterogeneous Integration of Avago's MEMS

Avago produced the FBAR (film bulk acoustic resonator) MEMS filter, ACMD-7612: UMTS Band I Duplexer shown in Fig. 1.52 [156, 157]. It can be seen that: (a) there are circuits in the cap, (b) TSVs are in the Tx (transceiver) chip and the Rx (receiver)

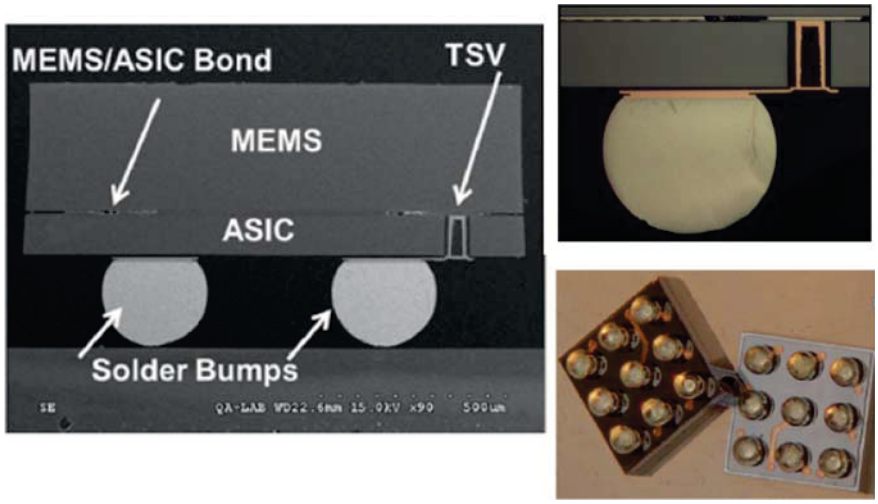


Fig. 1.50 Analog Devices' heterogeneous integration of MEMS on ASIC with TSV

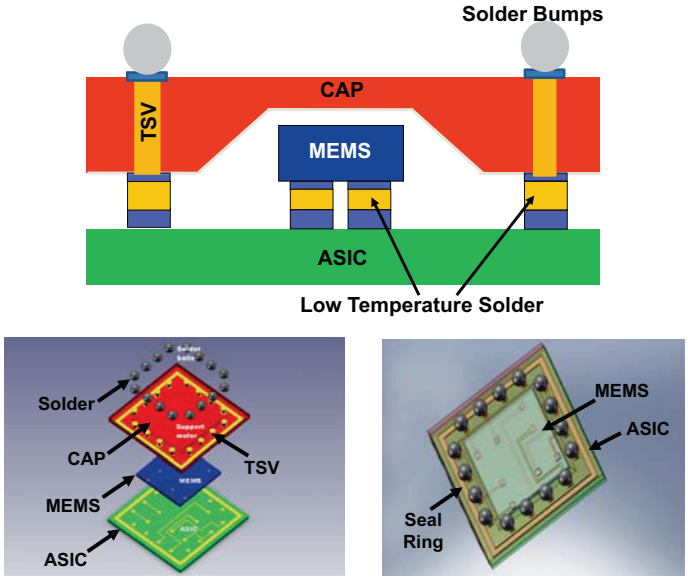


Fig. 1.51 IME's heterogeneous integration of the MEMS device on ASIC and is hermetic sealed by a silicon cap

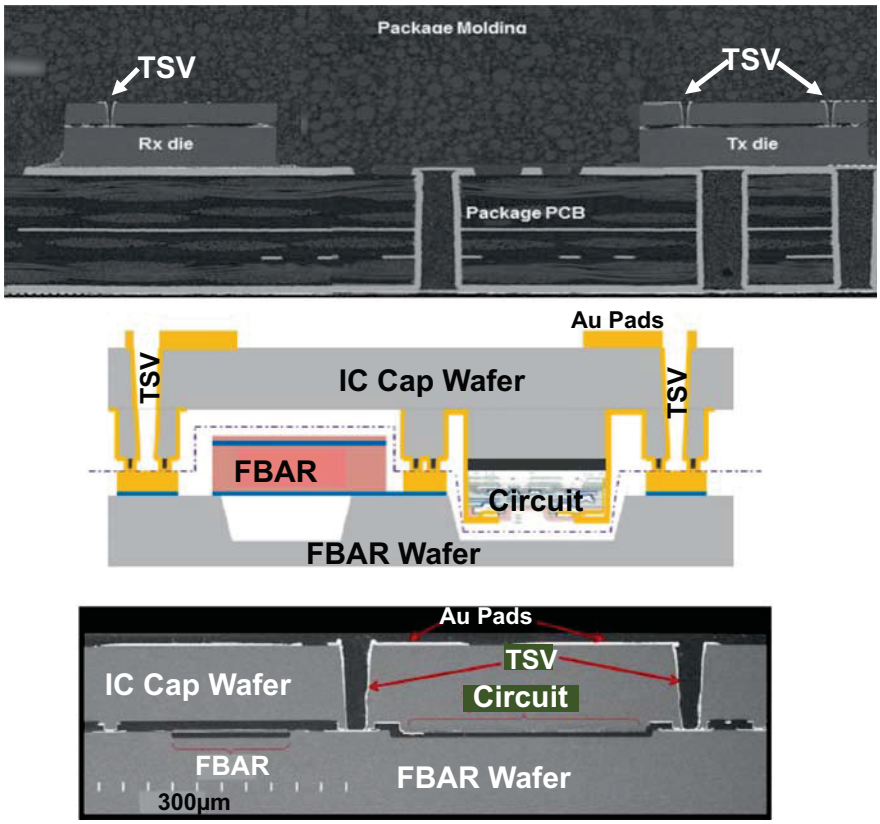


Fig. 1.52 Photo images of the FBAR hermetic package

chip, and (c) the sidewall of the TSVs is metallized and the TSVs are not filled. For more details of Avago's FRAR MEMS filter, please read Chap. 10.

1.18 Heterogeneous Integration of VCSEL

1.18.1 Heterogeneous Integration of IME's VCSEL

Figure 1.53 shows a single-channel OECB (opto-electrical circuit board) with embedded waveguide using traditional PCB manufacturing process [158–163]. The OECB is made up of four electrical layers and one optical layer embedded below a 60-μm-thick BT substrate. Two optical vias with 100 μm diameter are formed to guide the optical beam from VCSEL (vertical-cavity surface-emitting laser) to the 45° mirror coupler. Likewise, optical beam exiting the waveguide is diverted from the 45° mir-

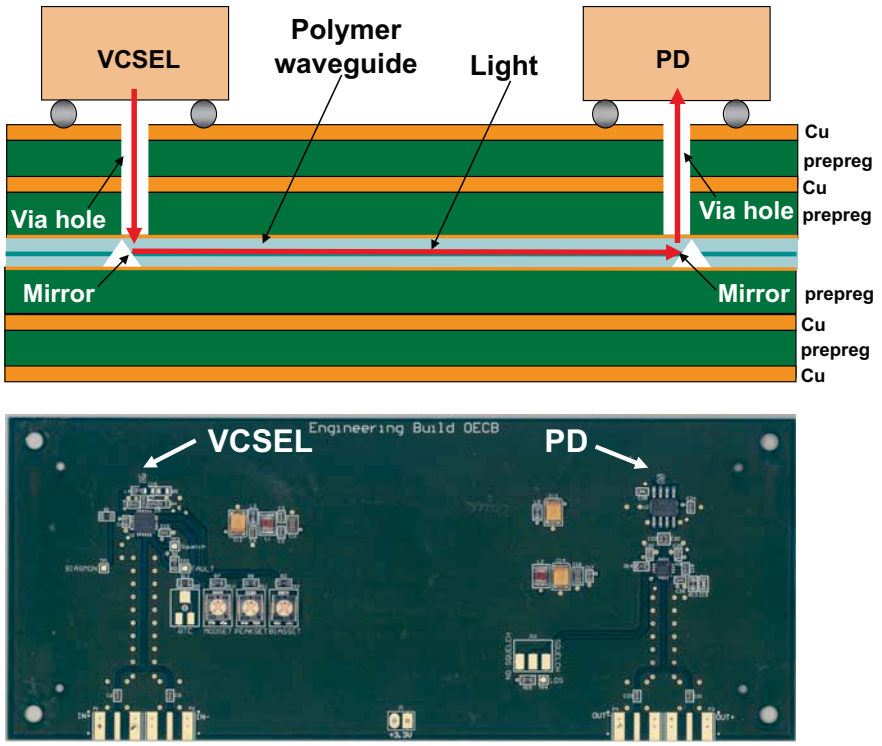


Fig. 1.53 IME's embedded OECB

ror coupler through the optical via and received by the photodetector. A 10 cm-long embedded polymer waveguide consists of a 70 μm × 70 μm core and a 15 μm thick top and bottom cladding. Two 45° mirror couplers are formed at both corners of the waveguide by using 90° diamond dicing blade. These mirrors convert optical beam emitted from VCSEL in the vertical path to the planar direction and into the waveguide. Please read Chap. 10 for more information.

1.18.2 Heterogeneous Integration of HKUST's VCSEL

Figure 1.54 shows an embedded hybrid 3D heterogeneous integration for optoelectronic interconnects [75, 164, 165]. It can be seen that the VCSEL is flip chip bumped with any materials on the VCSEL driver chip with TSV, which is solder bumped flip chip on the serializer chip. Larger bumps with any materials are mounted on the serializer chip while it is in a wafer format. After dicing the 3D hybrid IC chipset, it is placed on the PCB (or substrate) on top of the polymer waveguide. Special encapsulant (underfill) such as the transparent polymer may be needed to protect

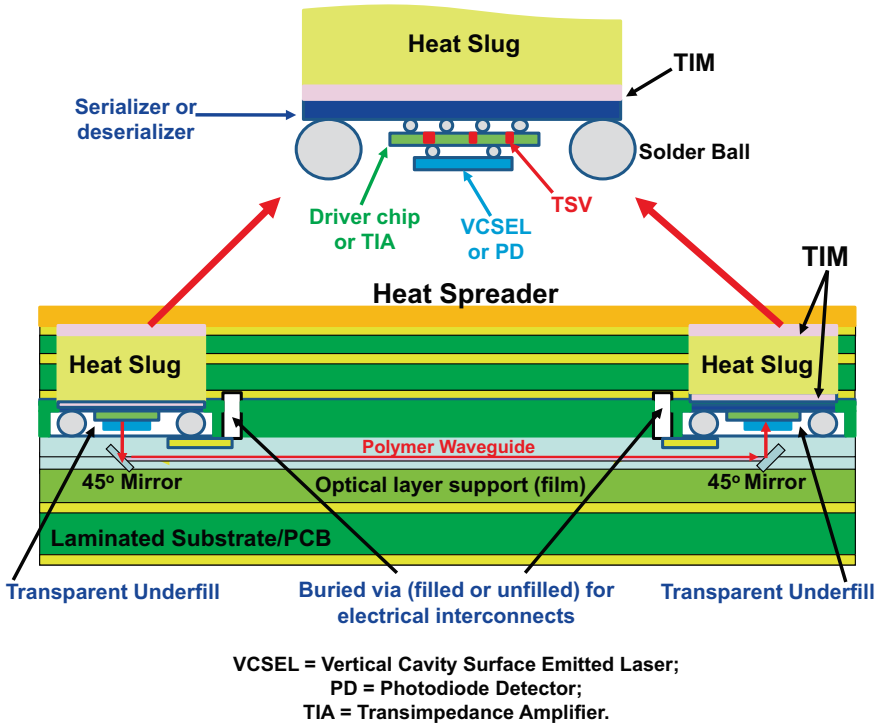


Fig. 1.54 HKUST's embedded 3D heterogeneous integration of opto-electronic interconnects

the chipset. If it is needed, a heat slug or any conductive material can be attached to the back side of the serializer chip by a thermal interface material (TIM). Again, if it is needed, a heat spreader can be attached to the top side of the heat slug with a TIM. Similarly, the photodetector chip is solder bumped flip chip on the TIA chip, which is then solder bumped flip chip on the deserializer chip. The thermal management and encapsulant techniques are the same as those of the VCSEL chipset. For more information, please read Chap. 10.

1.19 Summary and Recommendations

Some important results and recommendations are as follows:

- Heterogeneous integration, in this book, is defined as using packaging technology to integrate dissimilar chips/components (either side-by-side or stack) with different materials and functions, and designs from different fabless houses, and fabricated from different foundries, wafer sizes, and feature sizes into a system or subsystem on different substrates or stand alone.

- Heterogeneous integrations, in this book, is classified as: (1) heterogeneous integrations on organic substrates, (2) heterogeneous integrations on silicon substrates (TSV-interposers), (3) heterogeneous integrations on silicon substrates (bridges), (4) heterogeneous integrations on fan-out RDL substrates, and (5) heterogeneous integrations on ceramic substrates (which will not be elaborated in this books).
- Examples for heterogeneous integrations on organic substrates, silicon substrates (TSV-interposers), silicon substrates (bridges), and fan-out RDL substrates have been provided.
- In the next few years, we will see more of a higher level of heterogeneous integrations, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost.
- Heterogeneous integrations of chip-to-chip, face-to-face, face-to-back, memory stacks, PoP, AiP, LED, CIS, MEMS, and VCSEL, etc. have also been briefly mentioned.

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Chapter 2
Heterogeneous Integrations on Organic Substrates



2.1 Introduction

As of today and in general for high-volume manufacturing (HVM), 70% of the RDLs (redistribution-layers) for heterogeneous integrations are on organic substrates and the metal line width and spacing are $\geq$10 μm. Most of these heterogeneous integrations are actually SiPs (system-in-package). No more than 5% of the RDLs for heterogeneous integrations are on organic substrates, and the metal line width and spacing are <10 μm.

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates [1–5] by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up layer, shrinking the dimensions of the metal line width and spacing, reducing the pad size and pitch, eliminating the core [6–29], making the BOL (bump-on-lead) [30–38], and laminating the ETS (embedded trace substrate) [39–44]. In this chapter, the origin of build-up organic package substrates will be briefly mentioned. The fabricating thin-film layers on top of the build-up layer will be discussed. Finally, the organic interposer for supporting heterogeneous integration will be presented. The conventional SiPs by Amkor and Apple/ASE will be briefly mentioned first.

2.2 Amkor's SiP for Automobiles

Amkor's SiP for automobiles focuses on autonomous driving, infotainment, and ADAS (advanced drive assist systems), and computer in a car. Figure 2.1a and b, show a couple of examples of Amkor's SiP for automobiles. It can be seen from Fig. 2.1a that the 42.5 mm × 42.5 mm infotainment organic substrate is supporting the processor and DDR (double data rate) memories. While from Fig. 2.1b, the 55 mm ×

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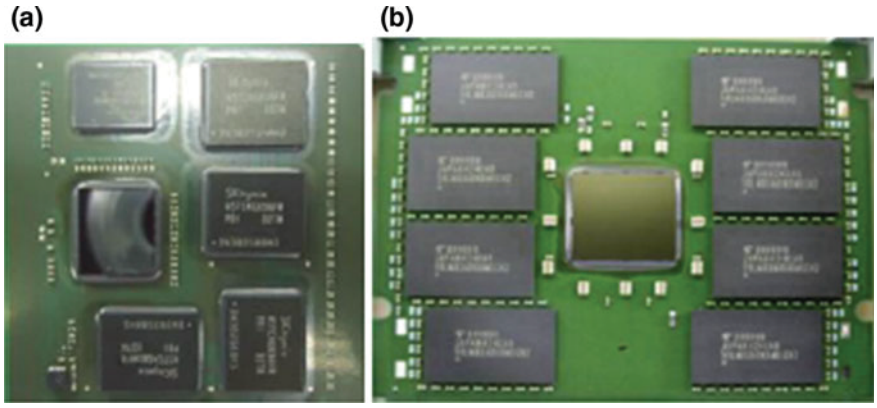


Fig. 2.1 Amkor's SiPs for Automobiles. **a** 42.5 mm × 42.5 mm infotainment. **b** 55 mm × 72 mm organic substrate

72 mm organic substrate is supporting the network switch, ASIC (application-specific integrated circuit), and memories.

2.3 Apple Watch III (SiP) Assembled by ASE

Through USI (Universal Scientific Industrial), ASE is a sole backend provider for Apple's custom-designed S3 SiP modules (Fig. 2.2) for use in the Apple Watch III. It can be seen from Fig. 2.2 that there are >40 chips and are on an organic substrate. Some of these chips are discrete passive components such as capacitors and resistors, ASIC, processors, controller, converter, DRAM (dynamic random access memory), NAND, Wi-Fi, NFC (near-field communication), GPS (global positioning system), sensors, etc.

2.4 IBM's SLC Technology

More than 25 years ago, IBM in Japan at Yasu invented the surface laminar circuit (SLC) technology, Fig. 2.3 [1–4]. SLC formed the basis of today's very popular low-cost organic package substrates with buildup layers vertically connected through microvias [5] to support heterogeneous integrations such as flip chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo-sensitive epoxy and the conductor plane of copper plating, i.e., using a semi-additive process (SAP). In general, a package substrate with twelve layers [e.g., two

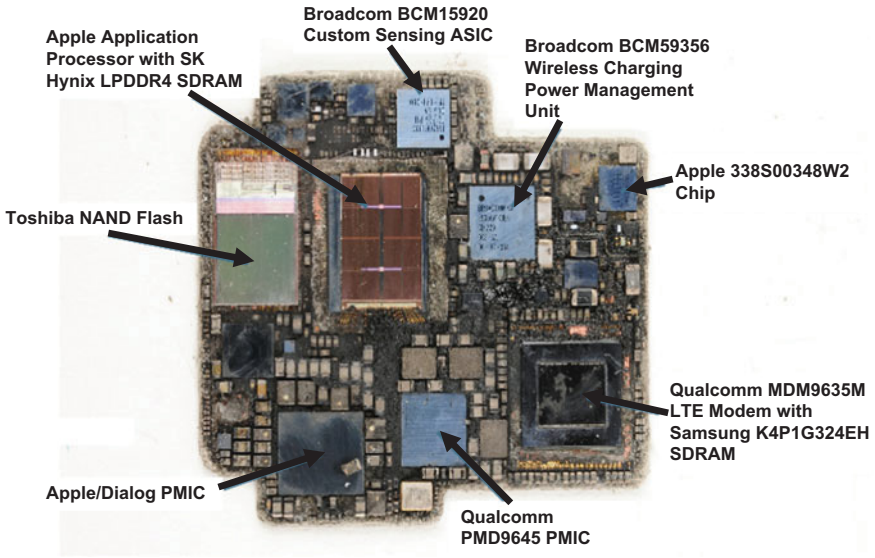


Fig. 2.2 Apple's smart watch SIII assembled by ASE

core layers and ten buildup layers (5-2-5)] and a 10 μm line width and spacing are more than adequate to support most of the chips.

2.5 Coreless Substrate

Coreless substrate was first proposed by Fujitsu [6] in 2006. Figure 2.4 shows the comparison between the conventional organic package substrate with build-up layers and the organic coreless package substrate. It can be seen that the biggest difference is that there is not a core in the coreless package substrate and all the layers of the coreless package substrate are the build-up layers [6–29].

The advantages of the coreless package substrate are [6–29]: (a) because of eliminating the core, the cost of the coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical performance because of good high-speed transmission characteristic; and (d) definitely smaller form factor. On the other hand, the disadvantages are [6–29]: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity; and (d) new manufacturing infrastructure is necessary. In 2010, Sony manufactured the first coreless package substrate for the cell processor of their PlayStation 3 [18].

Even though coreless substrates have many advantages, they are not so popular because of the warpage control issue. One of the key factors affecting the warpage

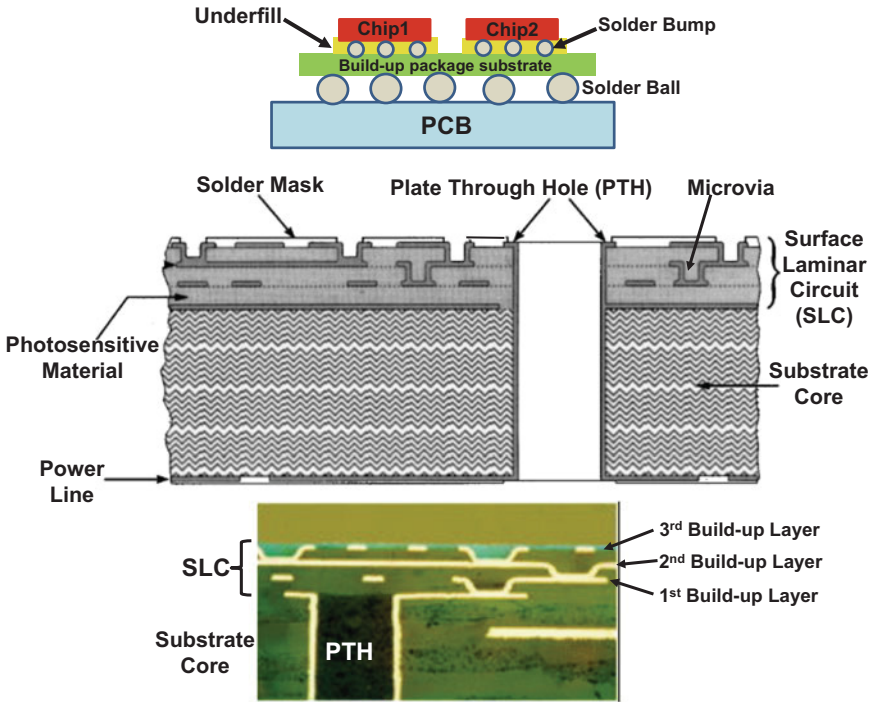


Fig. 2.3 IBM's SLC for flip chip organic build-up package substrate

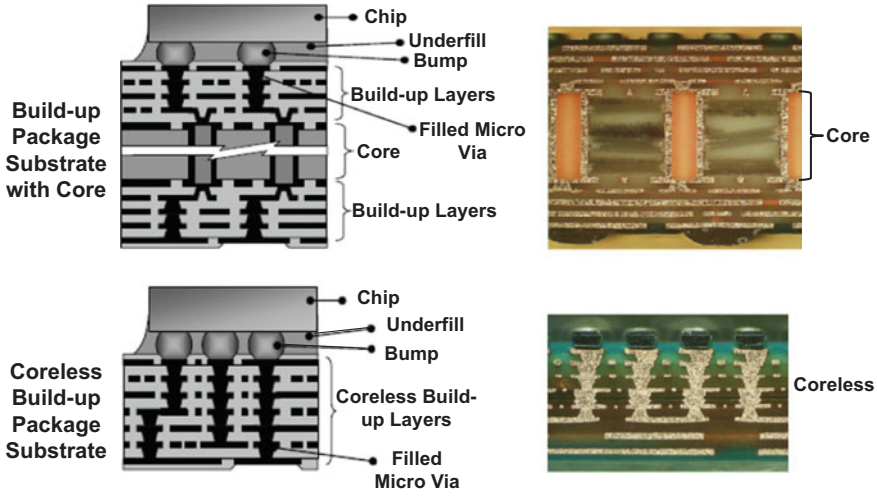


Fig. 2.4 (Top) flip chip on conventional build-up package substrate. (Bottom) flip chip on coreless substrate

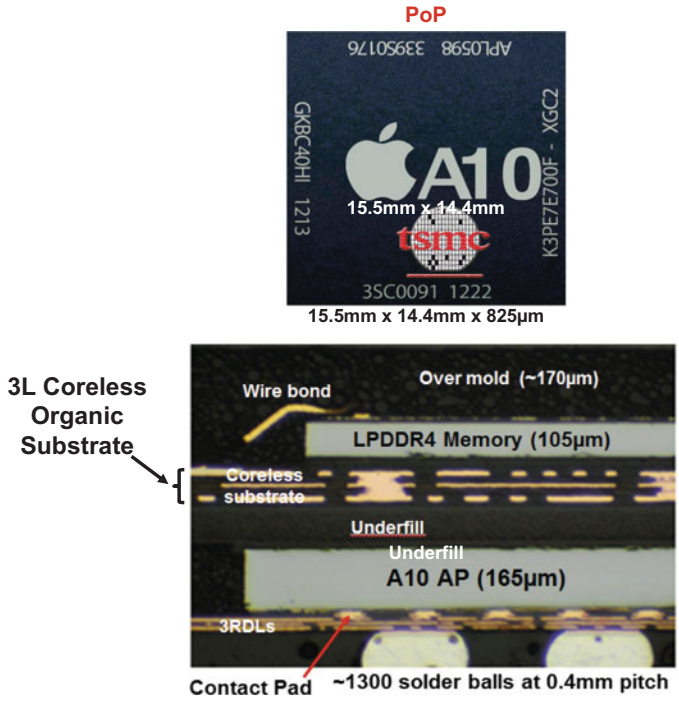


Fig. 2.5 3-layer coreless substrate in iPhone 7

is the coefficient of thermal expansion mismatch of substrate materials. Thus, a proper control of this factor will help reduce the warpage issue of coreless substrates. Another factor affecting the warpage is the package assembly. Thus, a proper package assembly warpage correction control (with vacuum and pressure) will help improve the warpage problem of coreless substrate.

Figure 2.5 shows an example of the application of coreless substrate. It can be seen that the upper package of the application processor chipset is housing the mobile DRAMs on a 3-layer coreless organic package substrate with wirebondings.

2.6 Bump-on-Lead (BOL)

BOL was first proposed by STATSChipPAC [30–34] and was used by Qualcomm [35] and others [36–38]. A conventional bump-on-capture pad (BOC) or simply bump-on-pad (BOP) flip chip organic substrate layout is shown in Fig. 2.6a. It can be seen that the flip chip pads are on a 210 µm area-array pitch in a solder mask (SR) defined configuration with one signal escape between bump pads resulting in an effective escape pitch of 105 µm. The BOL methodology is shown in Fig. 2.6b;

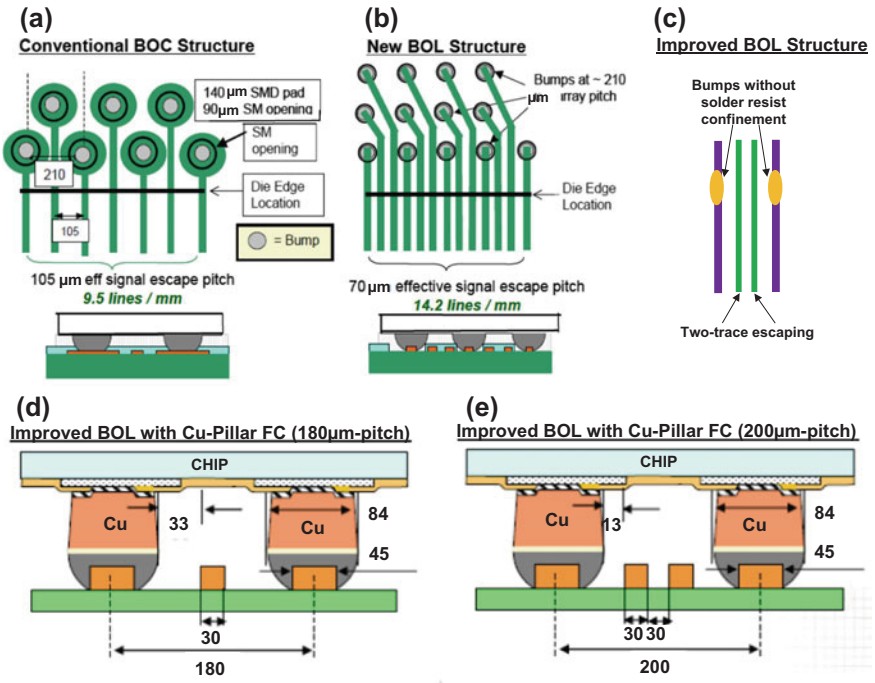


Fig. 2.6 BOL. **a** conventional BOP, **b** new BOL, **c** improved BOL, **d** improved BOL with Cu-pillar FC (180 µm-pitch), and **e** improved BOL with Cu-pillar FC (200 µm-pitch)

here, the landing pad on the substrate is merely the trace (lead) itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 7 µm without changing the design rules (trace width and space) of the substrate. The improved BOL structure is shown in Fig. 2.6c. It can be seen that the bump pads are without any solder resist confinement, i.e., open SR [35].

The test vehicles, Cu column on BOL, used in [35] are shown in Fig. 2.6d and e. It can be seen that one trace between the 180 µm bump pitch and up to two traces with the 20 µm bump pitch can be comfortably routed. Figure 2.7 shows the cross section image of the Cu column (pillar) on solder BOL. Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL are also shown in the Fig. 2.7.

2.7 Embedded Trace Substrate (ETS)

ETS is one of the coreless substrates with fine line width/spacing embedding the top metal trace pattern into prepreg layer [39–44]. The process flow of ETS is shown in Fig. 2.8a. It starts from a carrier board with a removable Cu foil. It is followed by

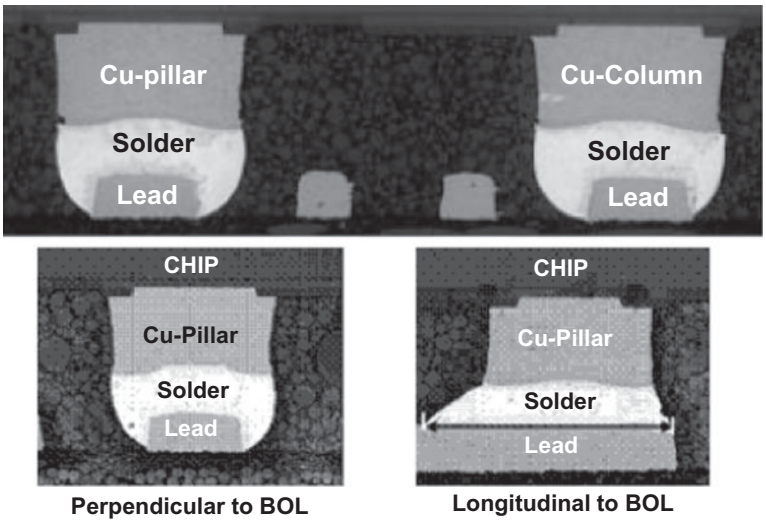


Fig. 2.7 Qualcomm's Cu column on BOL. Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL

using a typical electrolytic copper plating method to form the first layer of copper pattern. Then, laminate a prepreg on the copper pattern. It is followed by laser via drilling, electroless copper coating, dry film laminating, exposing and developing, second-layer copper pattern plating, stripping, and micro-etching. Once all the copper pattern layers have been completed, the carrier board will be removed. Since the Cu foil is connected to the first copper pattern, micro-etching is necessary before SR coating. After the SR opening process, it is completed by metal finishes treatment, e.g., organic solderability preservatives (OSPs). Figure 2.8b shows a cross section of a Cu pillar flip chip on ETS assembly by SPIL [42]. Another example is shown in Fig. 2.9, which is the heterogeneous integration of the modem chipset manufactured by Intel for iPhones XS and XR. Most line width/spacing of ETS in use today is 15/15 μm. However, 13/13 μm line width/spacing is in production by Simmtech [43].

2.8 Shinko's Build-up Substrate with Thin-Film Layer

Since 2013 and 2014, Shinko have been proposing to make thin-film layers (down to 2 μm) on top of the build-up layer of an organic package substrate and called it "i-THOP" substrate [45, 46] intended for high performance heterogeneous integration applications as shown in Fig. 2.10.

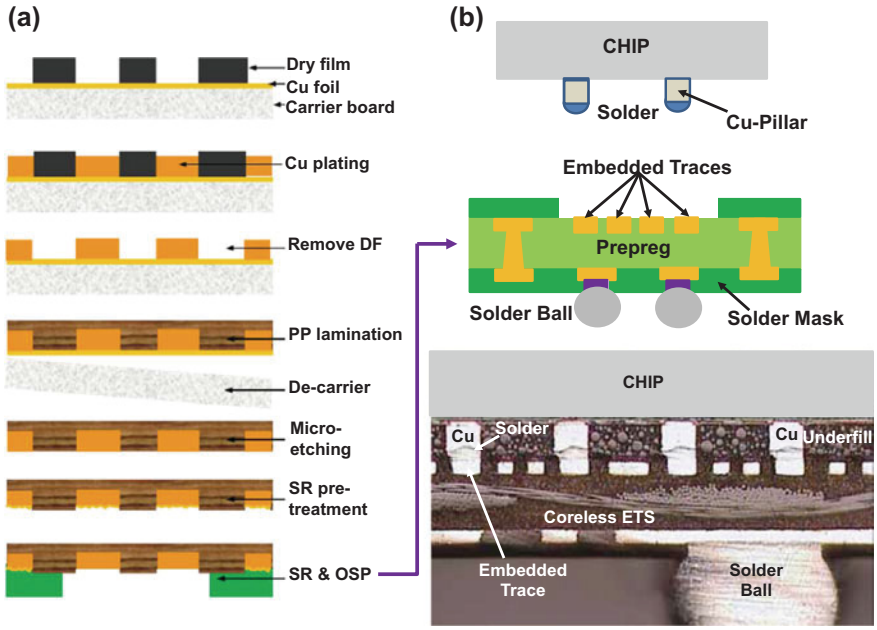


Fig. 2.8 **a** Process flow for fabricating the ETS and **b** flip chip with micro bumps on ETS

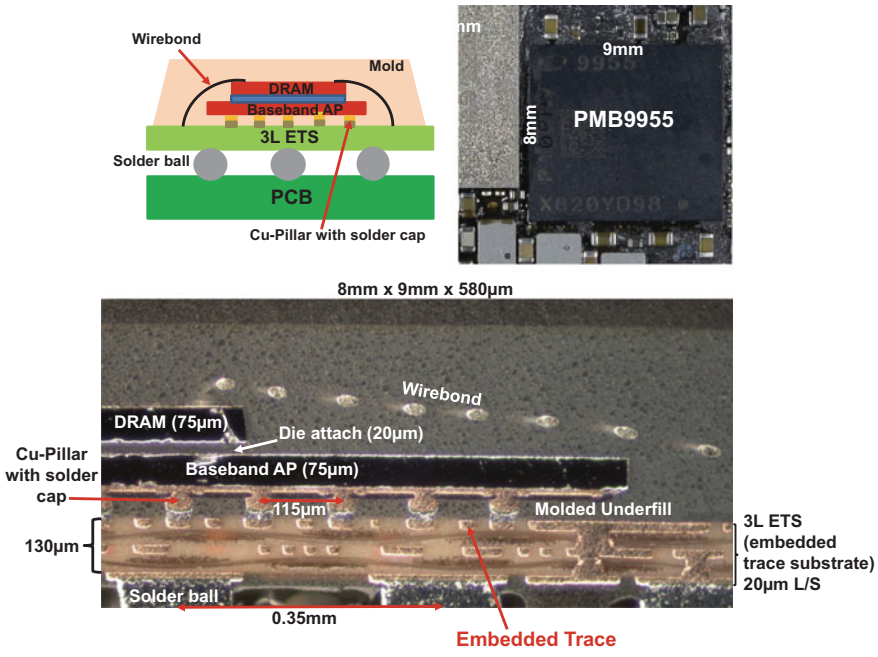


Fig. 2.9 Intel's modem chipset on ETS

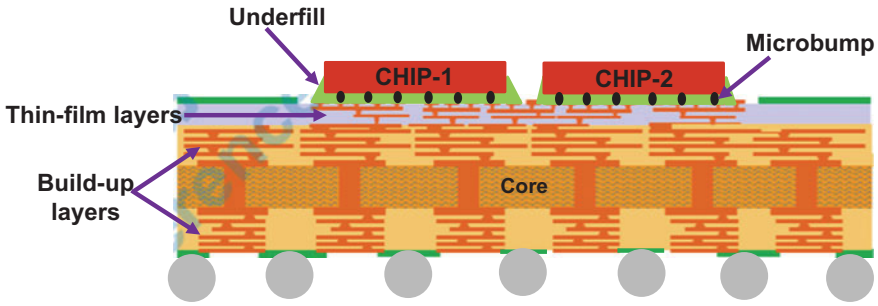


Fig. 2.10 Shinko's i-THOP substrate for heterogeneous integration

2.8.1 The Structure

Figures 2.11, 2.12 and 2.13 show Shinko's integrated thin-film high density organic package (i-THOP) substrate [45] for high performance applications. It is a 4 + (2-2-3) test vehicle, which means there is a 2-layer metal core, 3 build-up metal layers at the bottom (PCB-side), 2 build-up metal layers on the top (chip-side), and the first number "4" represents there are 4 thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer. The thickness, line width and spacing of the Cu RDLs can be as small as 2 μm (Fig. 2.12). The thin-film Cu RDLs are vertically connected through a 10 μm via as shown in Fig. 2.11. The surface Cu pad-pitch is 40 μm (Fig. 2.13) and the Cu pad diameter is 25 μm with a height of 10–12 μm (Fig. 2.13).

2.8.2 Assembly Process

The assembly process of Shinko's substrate is followed. First, the conventional build-up layers are laminated on both sides of the core (with 100 μm plated through hole) of the package substrate and the Cu metal build-up layers are formed by the normal semi-additive techniques and vertically connected through a ~50 μm build-up microvia [45] (Fig. 2.11). After the backside is coated with a (25 μm-thick) solder mask layer for the ball grid array (BGA) solder balls, the topside surface is finished by chemical-mechanical polishing (CMP) to flatten the laser-drilled and Cu filled vias and to smooth the surface in preparation for applying the fine wiring insulating resin layers.

A thin-film process is used to deposit the insulating resin layers. Then normal processes are applied to open small diameter vias and a Ti/Cu seed layer is sputtered on the resin layer. A photoresist is then spun on and exposed by a stepper to make the 2 μm wiring trace (RDL) pattern. The wiring thickness is formed by electrolytic Cu plating. Finally, the Cu pads on the top layer are treated by organic solderability preservative (OSP).

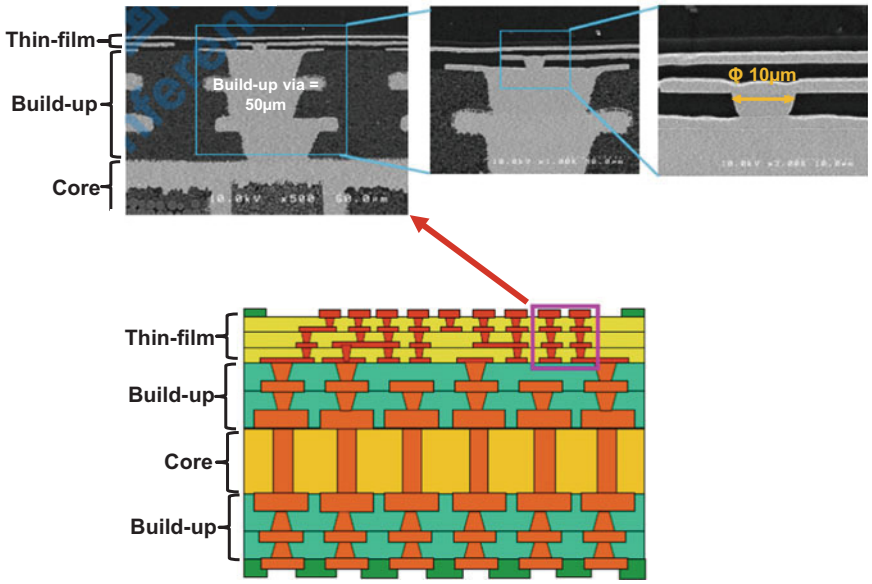


Fig. 2.11 Shinko's i-THOP. Thin-film layers (with 10 μm-via) on build-up layer

Figure 2.14 shows the warpage measurement results of the 4 + (2-2-3) i-THOP substrate (40 mm × 40 mm) under a temperature variation from room temperature (RT) to 260 °C and then back to the RT. It can be seen that: (a) for all the temperatures the deformed shape (warpage) of the package substrate is convex, (b) when the substrate is heated to the lead-free temperature (260 °C) the warpage increases to only 10 μm, and (c) overall, the warpage is stable and acceptable.

2.8.3 Qualification Tests

Qualification tests have also been conducted on the i-THOP substrate structure. These tests are: (a) pre-condition: MSL (moisture sensitivity level) 3A and reflow (to 260 °C) 3 times, (b) thermal cycling (−55 °C ↔ 125 °C) for 1000 cycles, and (c) HAST (highly accelerated stress test): 130 °C/85%RH/3.5 V for 150 h. iTHOP substrate passed the tests and there was no via delamination observed.

2.8.4 Demonstration of i-THOP

In 2014, Shinko demonstrated that [46] ultrafine pitch flip chips can be successfully assembled on the i-THOP substrate. Figure 2.15 schematically shows the two chips'

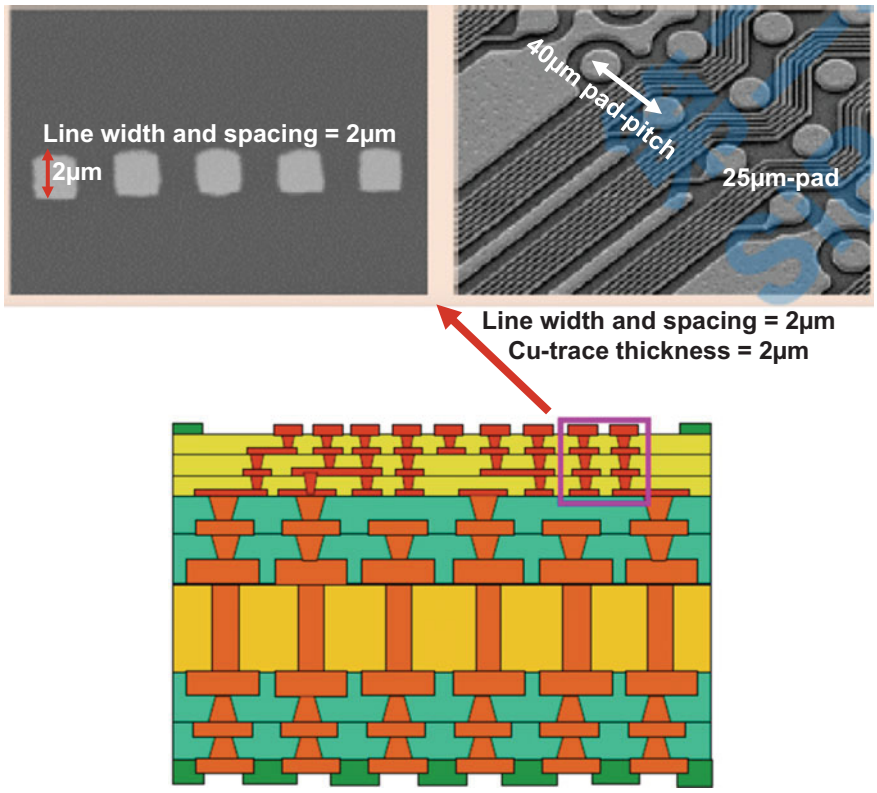


Fig. 2.12 Shinko's i-THOP. Metal line width and spacing of thin film layer = 2 μm

lateral communications by the 2 μm line width and spacing RDLs of the two thin-film layers, which are built on top of the 1-2-2 build-up organic substrate, i.e., 2 + (1-2-2). Figure 2.16 shows the 40 μm-pitch microbumps (Cu pillar + NiSnAg) of the test chips and the 40 μm pitch flip chip bonding pads (25 μm-diameter). Typical images of the cross section of the flip chip assembly with optimized conditions are shown in Fig. 2.16. It can be seen that good solder joints are confirmed at all areas of the assembly [46].

2.9 Cisco's Organic Interposer

2.9.1 The Structure

Figure 2.17 shows a 3D heterogeneous integration designed and manufactured with a large organic interposer with fine-pitch and fine-line interconnections by Cisco

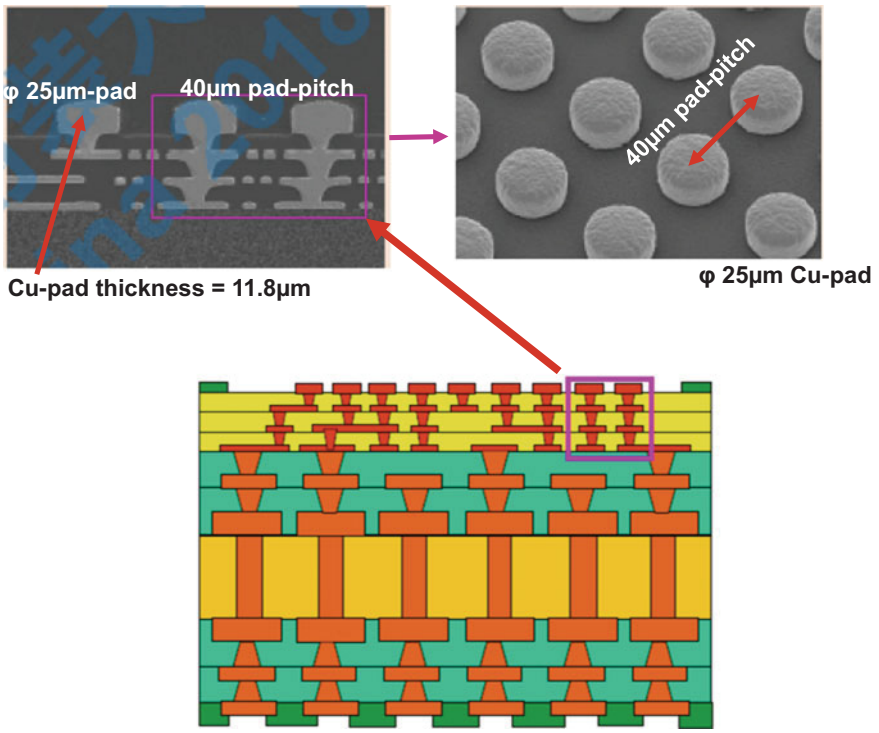


Fig. 2.13 Shinko's i-THOP. Cu-pad thickness = 11.8 μm. Cu-pads φ = 25 μm and are on 40 μm-pitch

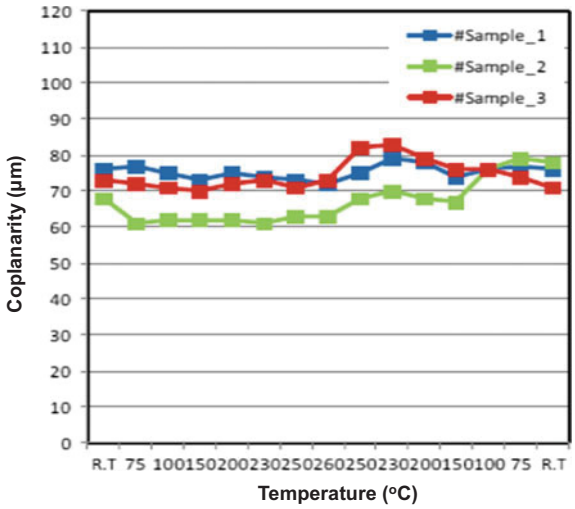


Fig. 2.14 Warpage measurement results of the 4 + (2-2-3) i-THOP substrate

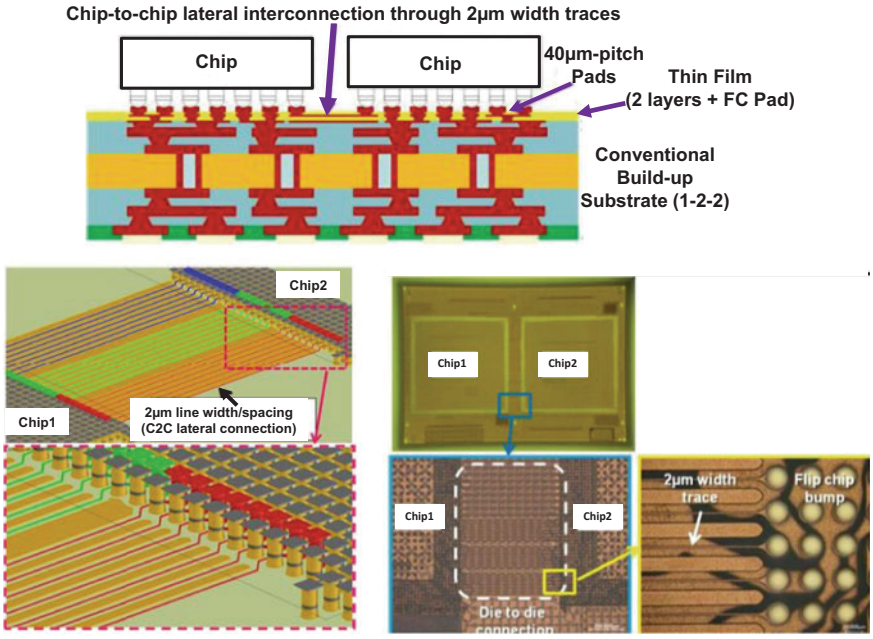


Fig. 2.15 Shinko's i-THOP test vehicle. Two thin film layers are built on top of the 1-2-2 build-up package substrate

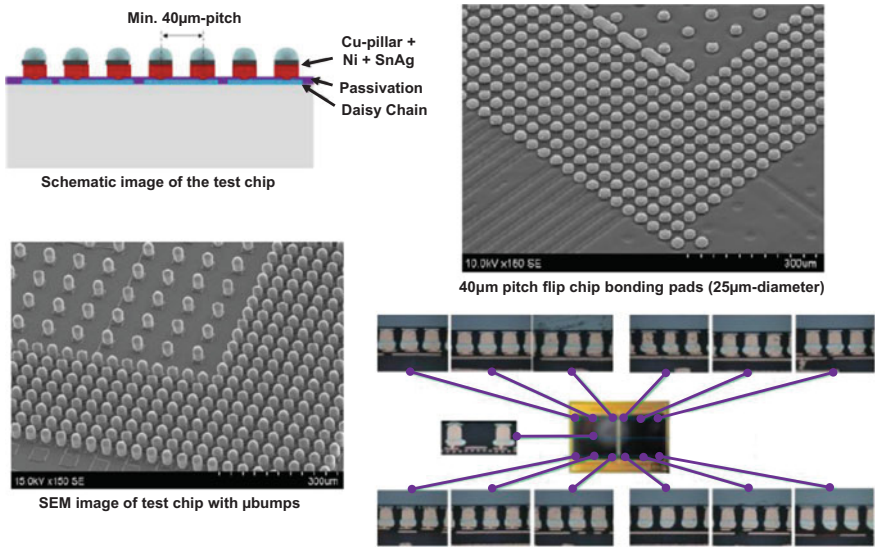


Fig. 2.16 Microbumps at 40 μm-pitch and the bonding pads (25 μm-diameter) on the i-THOP substrate. Good solder joints from optimized condition

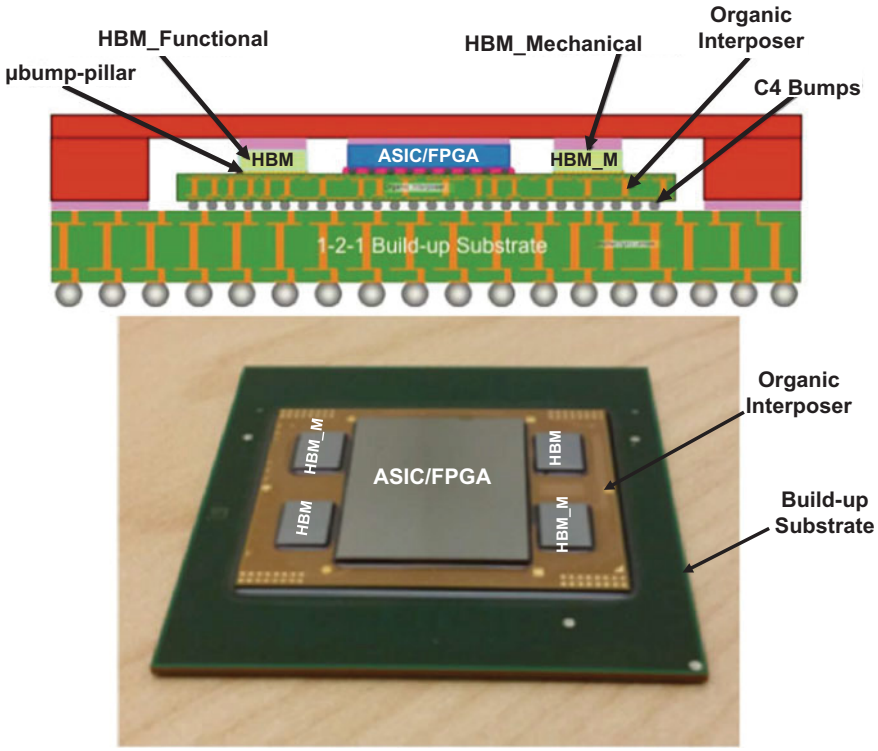


Fig. 2.17 Cisco's 3D heterogeneous integration on an organic interposer

[47]. The organic interposer has a size of 38 mm × 30 mm × 0.4 mm (Fig. 2.18). The minimum line width, spacing, and thickness of the front side and back side of the organic interposer are the same and are, respectively, 6, 6, and 10 μm. It is a 10-layer high density organic interposer (substrate) and the via size is 20 μm. A high-performance application-specific IC (ASIC) die measured at 19.1 mm × 24 mm × 0.75 mm is attached on top of the organic interposer along with four high-bandwidth memory (HBM) dynamic random access memory (DRAM) die stacks. The 3D HBM die stack with a size of 5.5 mm × 7.7 mm × 0.48 mm includes one base buffer die and four DRAM core dies that are interconnected with TSVs and fine-pitch micro-pillars with solder cap bumps. The pad size and pitch of the front side of the organic interposer are 30 and 55 μm, respectively.

2.9.2 The Assembly Process

The major manufacturing steps for making the organic interposer are the same as those for the organic build-up package substrate. These include [47]: (a) plating

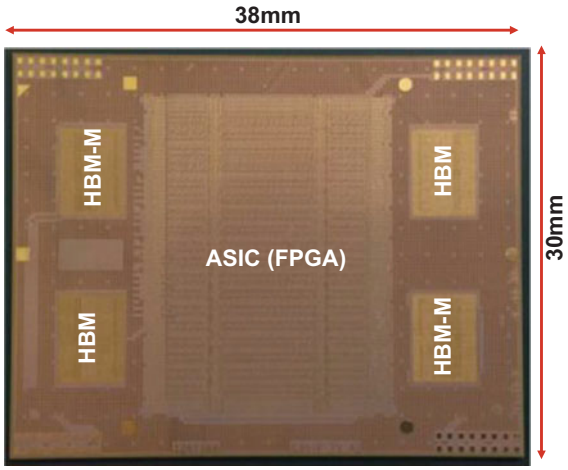


Fig. 2.18 Top view of the organic interposer (38 mm × 30 mm × 0.4 mm)

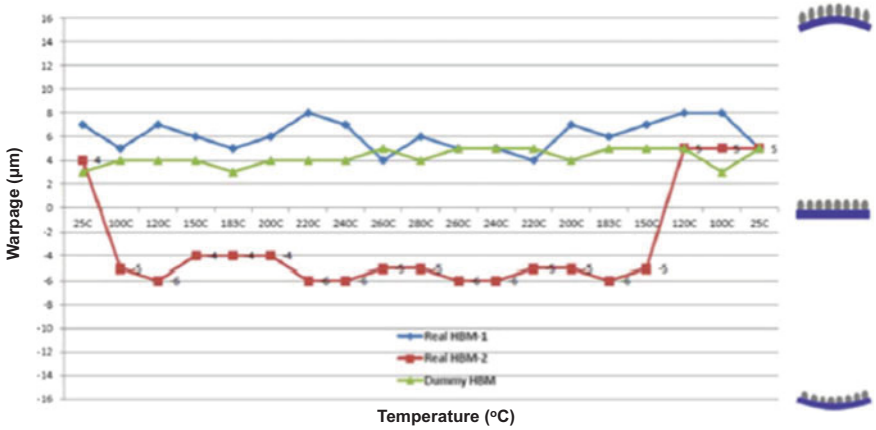


Fig. 2.19 Warpage measurement results of the HBM versus temperatures

through-hole (PTH) generation and filling for the core layer, (b) circuitization of the core layer, and (c) building Cu wiring layers on two sides of the core layer with SAP.

The warpage of the HBM and HBM-M and the warpage of the organic interposer are measured by the Shadow Moire method and the results are shown, respectively in Figs. 2.19 and 2.20. It can be seen from Fig. 2.19 that the warpage measurement results for the HBM die stacks over the temperature range from room temperature to 280 °C are, as expected, very small (<8 μm) and do not change much with temperatures. The warpage measurement results for the organic interposer w/o solder bumps (Fig. 2.20) from room temperature to 280 °C are also very small (about 100 μm) and do not change much with temperatures.

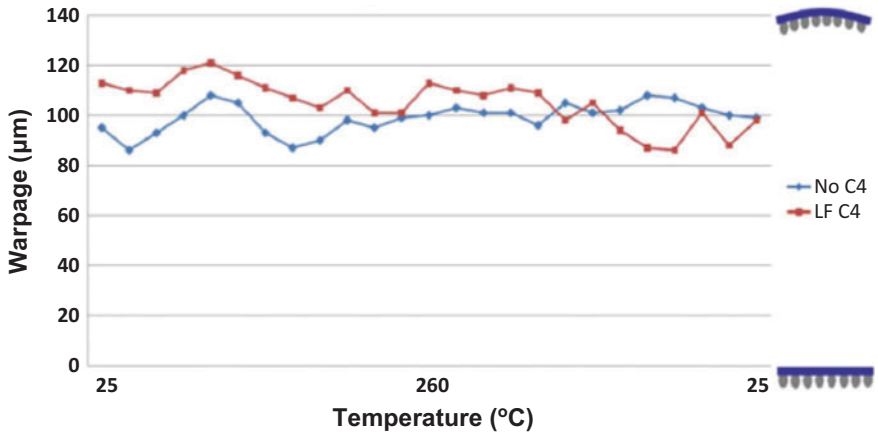


Fig. 2.20 Warpage measurement results of the organic interposer versus temperatures

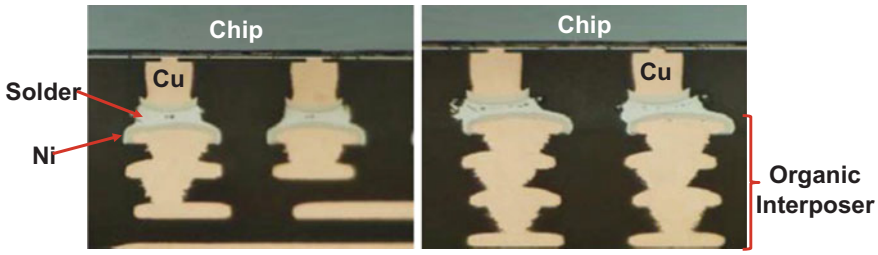


Fig. 2.21 Micro solder joints between the HBM and the organic interposer

Since the warpages of the HBM and organic interposer are small and do not change much with temperature, the FPGA die and HBM are assembled onto the interposer to form the FPGA and HBM subassembly first. Underfill encapsulation is used to protect the joints made of microbumps and regular bumps. A top view of the 3D SiP subassembly is shown in Fig. 2.17. Figure 2.21 shows the cross sections of the micro Cu-pillar solder joints between the HBM chip and the organic interposer. There is nothing abnormal.

2.10 Summary and Recommendations

Some important results and recommendations are as follows:

- Recent advances in ordinary, high-density, substrate-like PCB, and low-cost organic package substrates have promoted more heterogeneous integrations (actually, SiPs) applications.

- Also, the developments of organic build-up substrate, organic build-up substrate with thin film layers, organic interposers, coreless substrate, bump-on-lead (BOL), and embedded-trace-substrate (ETS) further enlarge the application ranges of heterogeneous integrations.
- The trends of the RDLs of heterogeneous integrations on organic substrates are in the development of finer metal line width and spacing (say 5 μm) at high yield.
- Most assemblies of heterogeneous integrations on organic substrates (SiPs) are by surface mount technology equipments.

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Chapter 3
Heterogeneous Integrations on Silicon Substrates (TSV-Interposers)



3.1 Introduction

Because of the drive of AI (artificial intelligence), ML (machine learning), and 5G, the semiconductors such as the CPU (central processor unit) or GPU (graphic processor unit), HBM (high bandwidth memory), and sliced field-programmable gate array (FPGA)'s density and I/Os increase and pad-pitch decreases. Even a 12 build-up layers (6-2-6) organic package substrate mentioned in Chap. 2 is not enough to support the sliced chips and a TSV (through-silicon via) interposer is needed [1–28]. TSMC called this kind of structure CoWoS (chip-on-wafer-on substrate) [6–11]. Leti [12, 13] called it SoW (system-on-wafer).

Heterogeneous integrations on silicon substrates (TSV-interposers) are for multi-chips on silicon wafer or system-on-wafer (SoW). The assembly methods are usually flip-chips-on-wafers with TSVs with mass reflow (Fig. 24a of [29]) for pitch $\geq$50 μm or with thermocompression bonding (Fig. 24b–d of [29]) for very fine pitches (<50 μm). In general, the RDLs (redistribution-layers) for heterogeneous integration on silicon substrates (TSV-interposers) are for ultrafine line width and spacing (down to submicron) applications.

In this chapter, the fabrication of TSVs and RDLs of a TSV interposer will be presented. Then, the thermal analyses, thermomechanical analyses, and feasibility analyses of a heterogeneous integration on silicon substrates (TSV-interposers) are discussed. First, the original heterogeneous integration on silicon substrates (TSV-interposers) and the TSV-interposers in production are briefly mentioned.

3.2 Leti's SoW

One of the early applications of SoW is given by Leti [12, 13] as shown in Fig. 3.1. It can be seen that a system of chips such as ASIC (application specific integrated circuit) and memories, power management ICs (PMICs) and microelectromechanical

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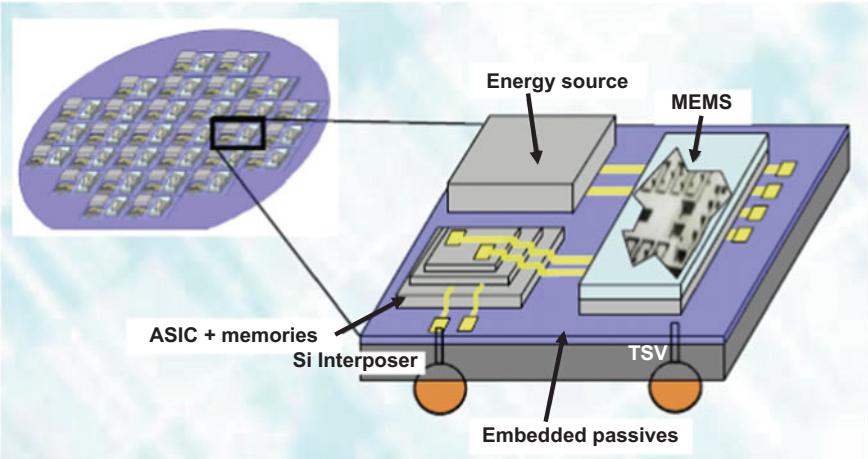


Fig. 3.1 Leti's SoW (system-on-wafer)

systems (MEMS) are on a silicon wafer with TSVs. After dicing, the individual unit becomes a heterogeneous integration system or subsystem on a silicon substrate with RDLs and TSVs (which is called a TSV-interposer) and can be attached on an organic substrate, or stand alone.

3.3 TSMC's CoWoS and CoWoS-2

Later, TSMC put SoW into production and called it chip-on-wafer-on-substrate (CoWoS) for the TSV-interposer size = 800 mm^2 [7–10] and CoWoS-2 for the TSV-interposer size = 1200 mm^2 [6] as shown in Fig. 3.2. It can be seen that a SoC (system-of-chip) such as the CPU (central processor unit) or GPU (graphic processor unit) and HBMs which consist of a stack of DRAMs (dynamic random access memories) and a base logic vertically interconnect through TSVs and microbumps are side-by-side attached through microbumps on a TSV-interposer with RDLs. The TSV-interposer is attached (through Cu-C4 bumps) on a package build-up substrate, which is then solder-ball attached to a PCB.

Figure 3.3a shows the TSMC/Xilinx sliced field-programmable gate array (FPGA) CoWoS [7–10]. It can be seen that the TSV (10 μm-diameter) interposer (100 μm-deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000 + of lateral interconnections between the sliced FPGA chips are connected mainly by the 0.4 μm pitch (minimum) RDLs of the interposer. Figure 3.3b shows NVidia's Pascal 100 graphic processor unit (GPU) [5], which is built on TSMC's 16 nm process technology and is supported by four HBM2 memories (16 GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with Cu-pillar and solder-

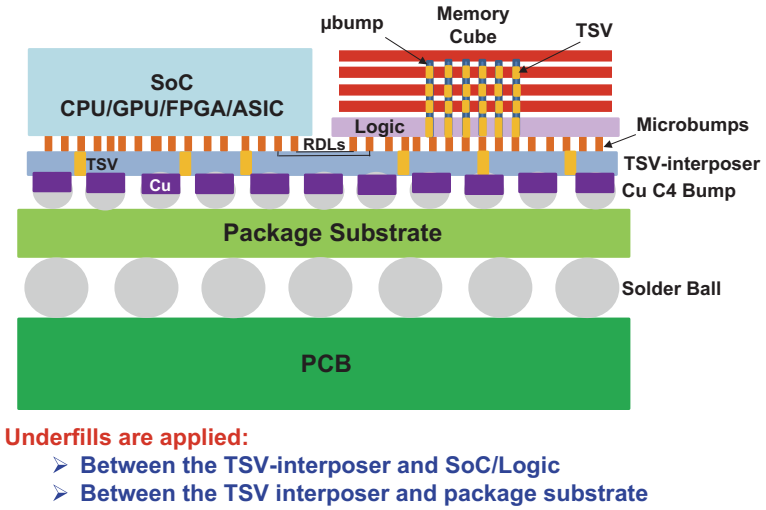


Fig. 3.2 TSMC's CoWoS (chip-on-wafer-on-substrate) and CoWoS-2

cap bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2 s are on top of a TSV interposer (1200 mm^2), i.e., CoWoS-2, which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with controlled collapse chip connection (C4) bumps.

3.4 Fabrication of TSVs

Figure 3.4 shows the key process steps in making a TSV [30, 31]. It starts with a SiNx/SiOx insulation layer by either thermal oxidation or plasma-enhanced chemical vapor deposition (PECVD). After photoresist and TSV lithography, the TSV is etched into the Si substrate by a Bosch-type deep reactive ion etch (DRIE) to form a high-aspect ratio (10.5) via structure. The etched TSV structure is then processed with a SiOx liner by sub-atmosphere chemical vapor deposition (SACVD), a Ta barrier layer and a Cu seed layer by physical vapor deposition (PVD). Cu electro-chemical deposition (ECD) is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10 µm in diameter and a depth of about 105 µm, which give an aspect ratio of 10.5. In such a high-aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness at the field. The scanning electron microscopy (SEM) cross-section images are shown in Fig. 3.5. It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from the etching process point of view. The Cu thickness at the field is <5 µm. The post-plating anneal is at 400 °C for

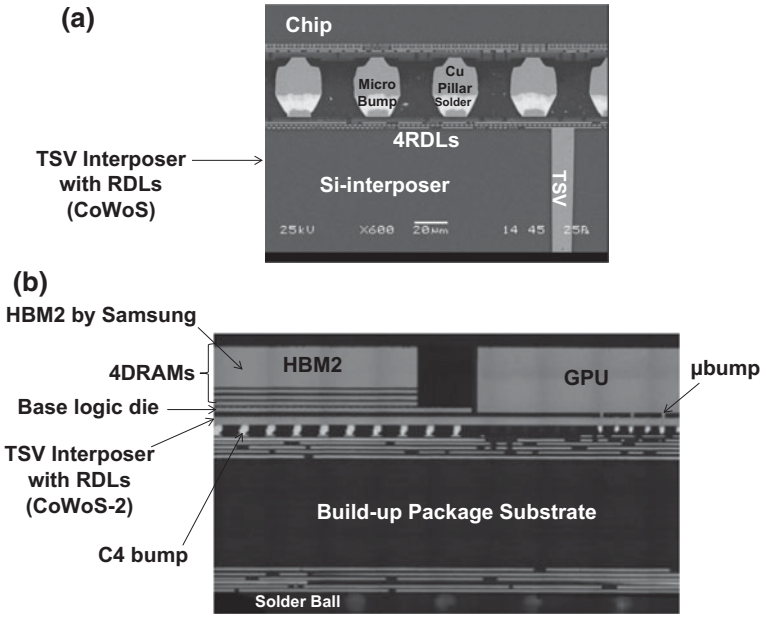


Fig. 3.3 Heterogeneous integrations. **a** Xilinx/TSMC's CoWoS. **b** NVidia/TSMC's CoWoS-2

30 min. To complete the TSV process, excess Cu at the field is removed by chemical mechanical polishing (CMP).

3.5 RDLs by Dual Cu-Damascene Process

Figure 3.6 shows the key process steps in making the RDLs from the TSV of an interposer. First, the SiO_2 layer is fabricated by PECVD. The step is followed by applying photoresist and mask or stepper, then using photolithography techniques (align and expose) to open vias on the SiO_2. Then, reactive ion etch (RIE) of the SiO_2 is accomplished. Next, apply mask or stepper, and then use photolithography techniques to open the redistribution trace locations. Then, use RIE to etch off more of the SiO_2, strip off the photoresist, and sputter Ti and Cu. Then use ECD to deposit Cu over the entire wafer. Those steps are followed by CMP of the Cu and Ti/Cu, which then results in RDL1 being obtained. Repeat all the above steps to obtain V_{12} (the via connecting the RDL1 to RDL2) and RDL2, and any additional layers. Figure 3.7 shows the image of the cross section of the fabricated RDLs on a TSV of an interposer. It can be seen that there are three RDLs and these RDLs are called inorganic RDLs made by PECVD and dual Cu-damascene + CMP.

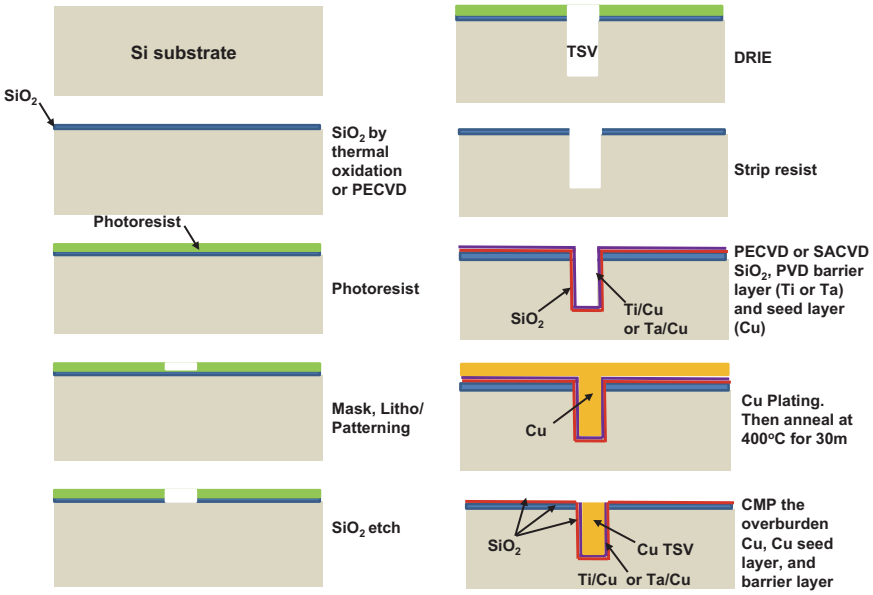


Fig. 3.4 Key process steps for making a TSV

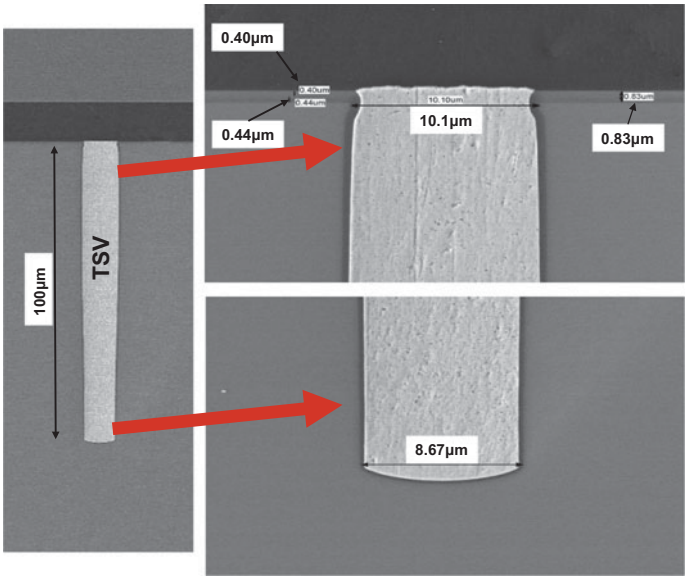


Fig. 3.5 SEM image of the cross-section of a TSV

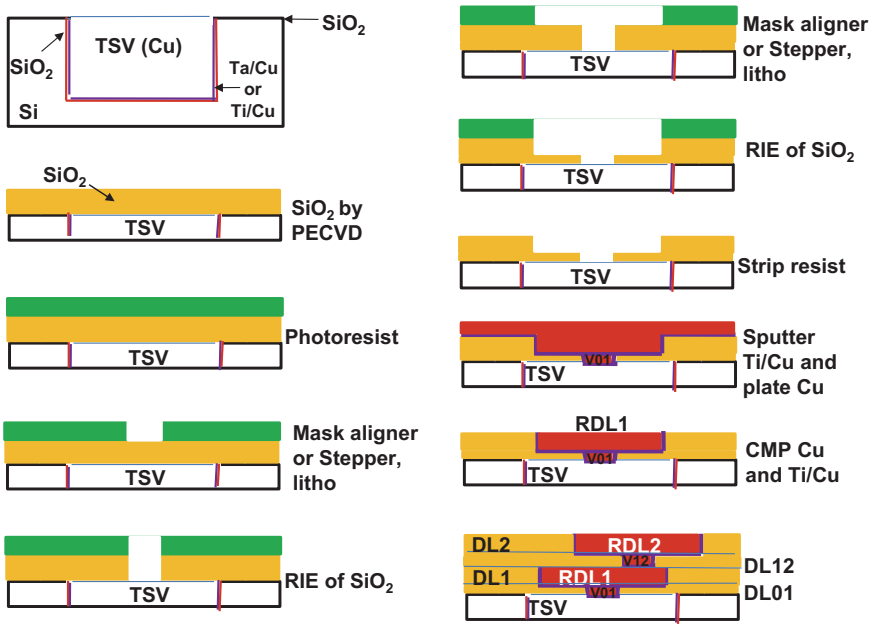
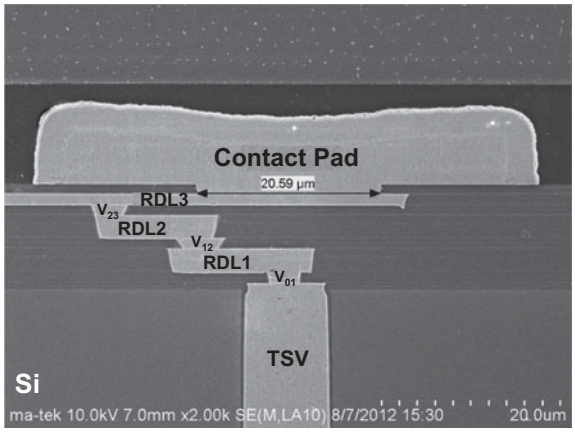


Fig. 3.6 Key process steps for making RDLs from a TSV

Fig. 3.7 SEM image of the cross-section of 3RDLs



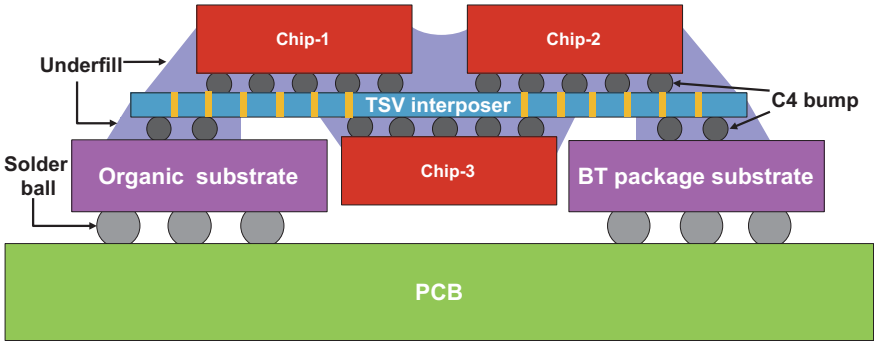


Fig. 3.8 Schematics of the TSV-interposer (with two chips on its top side and one chip on its bottom side) for heterogeneous integration

3.6 Double-Sided Interposer for Heterogeneous Integrations

3.6.1 The Structure

Figure 3.8 shows the schematics of the double-sided interposer for heterogeneous integration under consideration. Figure 3.9 shows the layout of the interposer. It can be seen that (a) on the left side, there are pads for the top two chips and (b) on the right side; there are pads for the bottom chip and the organic package substrate. The size of the package substrate is 35 mm $\times$ 35 mm $\times$ 970 μm. Underfills are used between the chips and interposer and the interposer and package substrate. The TSVs' diameter is 10 μm and on 150 μm pitch. The diameter of the solder bumps between the chips and interposer and between the interposer and package substrate is 90 μm and on 125 μm pitch. The diameter of the solder balls between the package substrate and the PCB is 600 μm and on 1000 μm pitch. Table 3.1 summarizes the geometry of the heterogeneous integration with a TSV interposer supporting chips on both sides [24–28].

3.6.2 Thermal Analysis—Boundary Conditions

Boundary conditions for the thermal analyses of the heterogeneous integration module are shown schematically in Fig. 3.10; the thermal loading conditions are included in Tables 3.1 and 3.2 along with the boundary conditions. As for the part's geometries, the dimensions are listed in Tables 3.1 and 3.2. It can be seen that (a) the power dissipation of each chip soldered on the interposer is 5 W; (b) the thermal resistance,

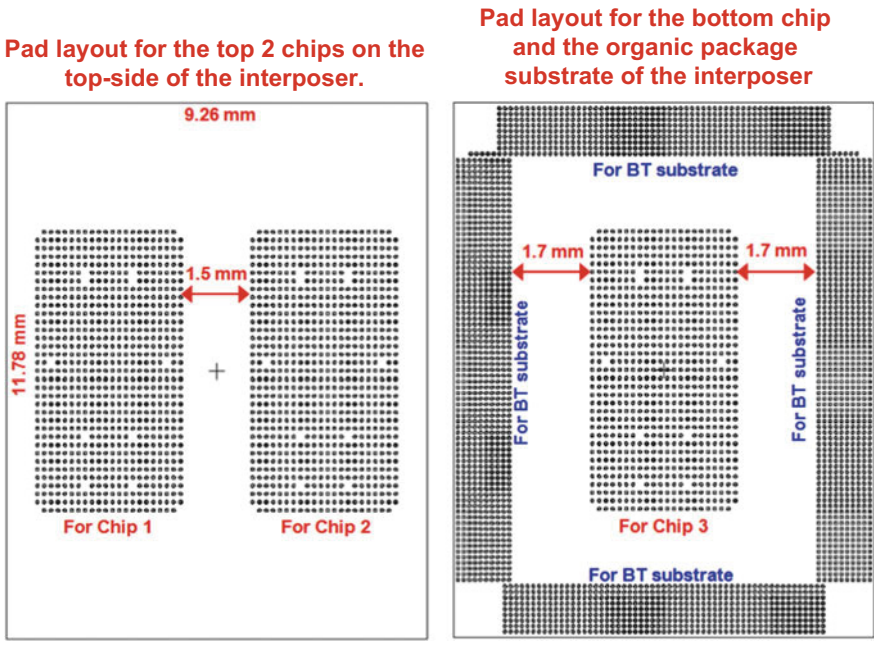


Fig. 3.9 (Left) pad layout for the top two chips on the top side of the TSV-interposer. (Right) pad layout for the bottom chip and the organic package substrate of the TSV-interposer

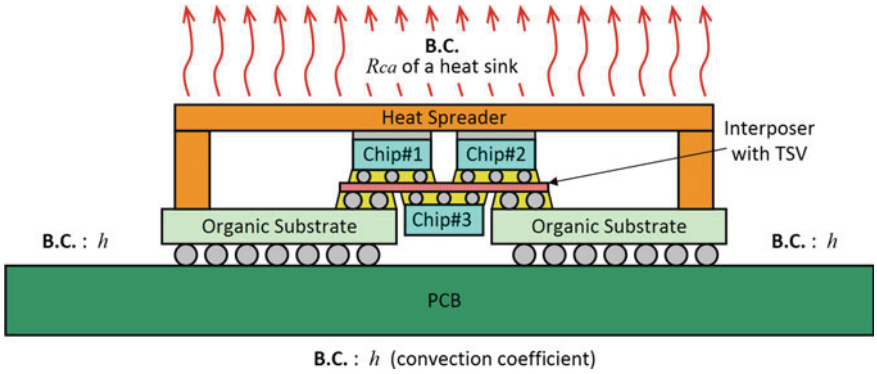


Fig. 3.10 Schematic of the thermal analysis model and the boundary conditions

Rca, to imitate the cooling capability of a suppositional heat sink that is attached on the heat spreader is from 0.1 to 4.0 °C/W; and (c) the heat transfer coefficient (h) of both sides of the PCB is 20 W/m^2 °C.

Table 3.1 Geometry parameter of the 3D IC heterogeneous integration module

	Length	Width	Height	Diameter	Pitch	Note
Chip #l–3	6.5 mm	3.8 mm	850 μm	–	–	The three chips are in the same sizes
Interposer	11.9 mm	9.4 mm	100 μm	–	–	
Organic substrate	35 mm	35 mm	970 μm	–	–	
Cavity	5.74 mm	8.46 mm	–	–	–	The cavity is in the organic substrate
PCB	60 mm	60 mm	1600 μm	—	–	
Heat spreader	3.35 mm	3.35 mm	500 μm	–	–	
C4 bump	–	–	–	90 μm	125 μm	Between chip and interposer
C4 bump	–	–	–	75 μm	125 μm	Between interposer and organic substrate
Solder ball	–	–	–	600 μm	1000 μm	Between organic substrate and PCB
TSV	–	–	–	10 μm	150 μm	Regular distribution in the interposer

Table 3.2 Thermal loading and boundary conditions used in the Analyses

Thermal loading	5W per chip (#1, #2, #3)
Boundary conditions	The thermal resistance (*Rca*) of a heat sink: tunable for parameter study
	The convection coefficient (h): 20 W/m^2 K on PCB both sides
	Other surfaces are regarded as adiabatic

3.6.3 Thermal Analysis—TSV Equivalent Model

An equivalent model is used to replace the real detail TSV model for simplifying the thermal simulations. In the conversion, the arrays of TSV, solder bump, and solder ball can be replaced by many coupled equivalent zones with their equivalent thermal conductivities (Fig. 3.11). Particularly, the SiO_2 layer on interposer has to be retained in the equivalent model for accurateness. For example, a 2 × 2 TSV array with 10 μm in diameter, 0.2 μm in thickness of sidewall SiO_2, 100 μm in height (thickness), and 50 μm in pitch, could be converted to an equivalent zone with 100 μm × 100 μm in area and having 144.56 W/m K of kxy and 156.34 W/m K of kz.

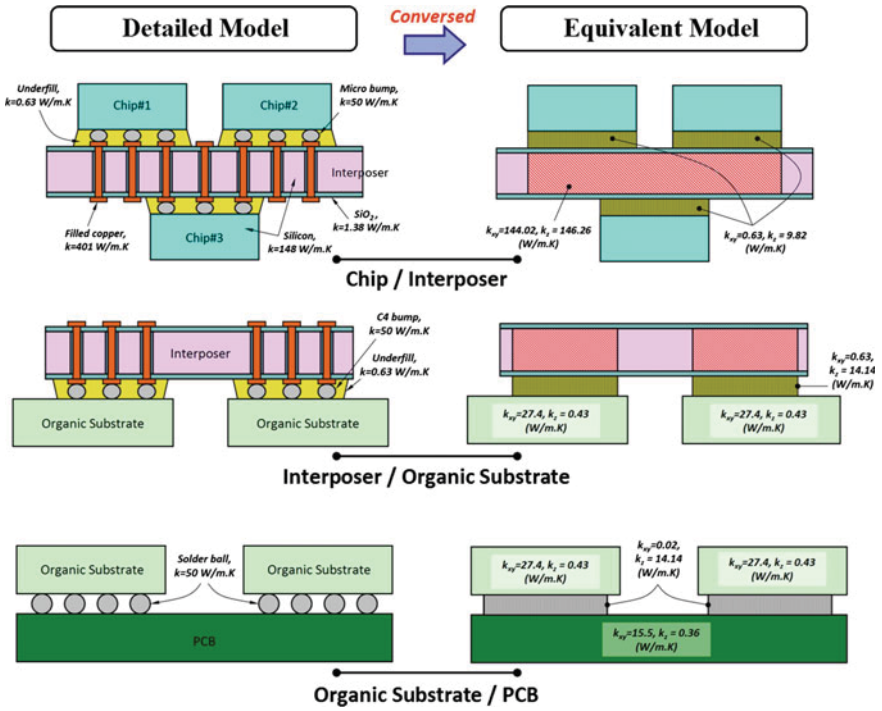


Fig. 3.11 Model conversion rules and the calculated thermal conductivities of each equivalent zone

3.6.4 Thermal Analysis—Solder Bump/Underfill Equivalent Model

The equivalent thermal conductivities of solder bump and solder ball should be determined by thermal resistance parallel-series correlation. Because of disconnection and large pitch, the equivalent thermal conductivity of a bump array that is with underfill material should approach to that of the underfill in the x-y direction. For the same reason, a solder ball array without underfill, its equivalent kxy should be very small and is nearly equal to zero. Figure 3.11 shows the model conversion rules and the calculated thermal conductivities of each equivalent zone.

3.6.5 Thermal Analysis—Results

Figure 3.12 shows the top view temperature contours of each chip (applied boundary condition: $Rca = 1.0$ °C/W on heat spreader), and Fig. 3.13 shows the 3D temperature distribution of the heterogeneous integration module. From these temperature

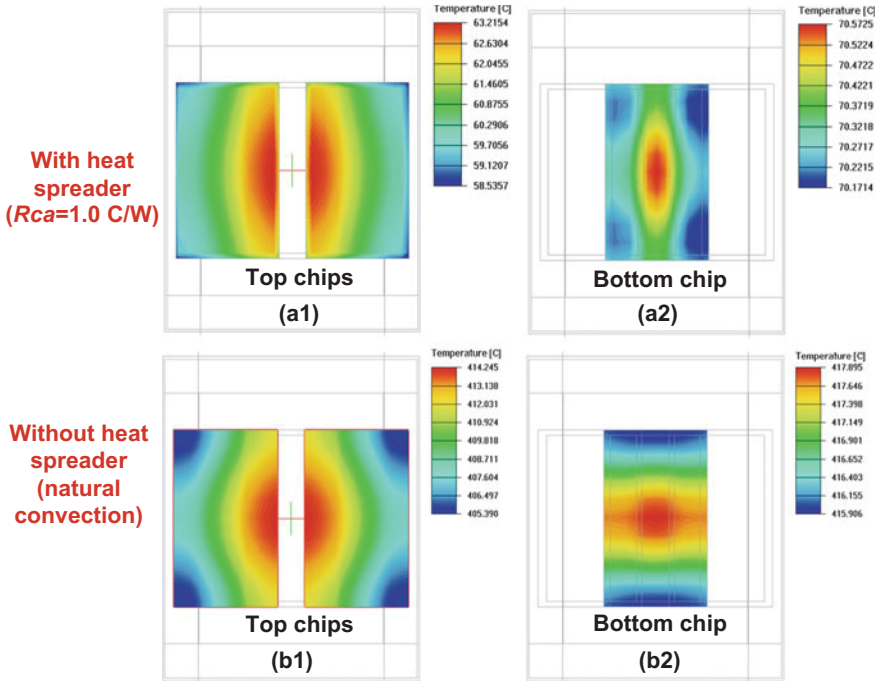


Fig. 3.12 Temperature distribution of (a1) chips #1 and #2 and (a2) chip #3 (Rcs = 1.0 C/W); and (b1) Chips #1 and #2 and (b2) chip #3 (without heat spreader, natural convention). The four temperature bars are not in the same scale

distribution contours, it can be seen that the temperature distribution of chip #1 and chip #2 are rather non-uniform, but that of chip #3 is not. The maximum temperature difference of chips #1 and #2 is about 4.7 °C (63.2–58.5 °C), and that of chip #3 is just about 0.4 °C (70.6–70.2 °C). Therefore, chips #1 and #2 have a more severe thermal issue about temperature non-uniformity than that of chip #3; the issue can damage the chips' quality and reliability performance. Also, from the same temperature distribution contours, it can be seen that a heat sink is necessary for cooling the heterogeneous integration module, because chips #1 and #2, and chip #3 can reach to very high temperatures, 410 and 417 °C, respectively, under a natural convection condition and without heat spreader attachment.

The relationships between chip's average temperature and the applied cooling capability (*Rca*) to the heat spreader/sink are shown in Fig. 3.14. The figure can help us select an appropriate heat sink that is attached on the heat spreader. For instance, if the temperature specification of the chips is 100 °C, a heat sink with cooling capability, *Rca*, less than 3.7 °C/W, is essential to cool the heterogeneous integration module. On the other hand, if the chips' temperatures must be under 60 °C, then we have to choose a very powerful heat sink that has an *Rca* less than 0.3 °C/W.

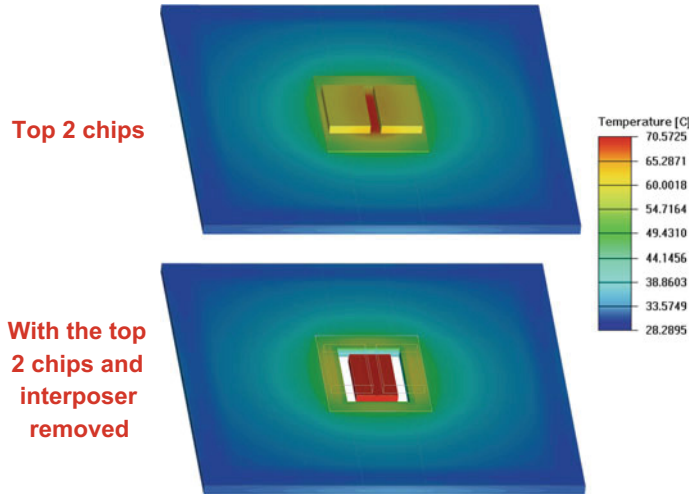


Fig. 3.13 The temperature contour of the integration of organic substrate, TSV-interposer, and chips #1, #2 and #3. (Top) chip #3 is shielded. (Bottom) TSV-Interposer and chips #1 and #2 are invisible

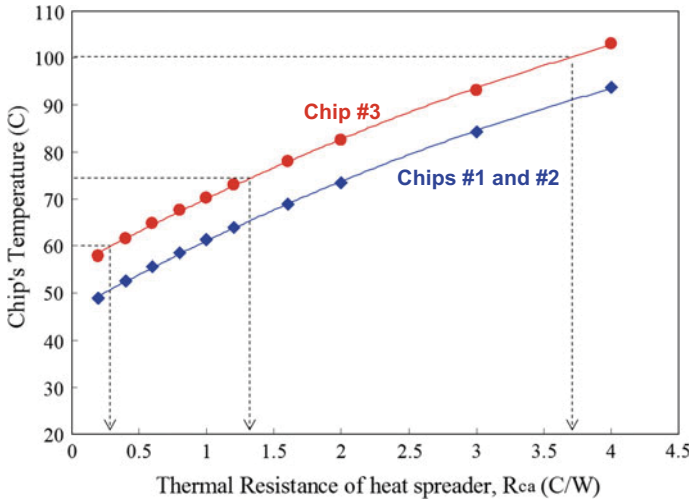


Fig. 3.14 Correlation between the chips' average temperatures and the applied cooling capability on the heat spreader

Figure 3.14 shows a severe thermal issue for the heterogeneous integration structure. The issue is that the chip planted on the bottom side of the interposer is always hotter than the chips planted on the top side of the interposer. This is because the chips on top side of interposer can be in direct contact with the main cooling mechanism—heat spreader and heat sink—but the chip on the bottom side of interposer cannot. The difference in the chips' average temperature is equal to 9.0 °C. The higher temperature of chip #3 is inevitable because the heat spreader plays a major role to dissipate the chips' generated heat, and the temperatures of chips #1 and #2 barricade the heat dissipation from the chip #3 to the heat spreader. It is very hard to solve the severe issue without any structural change in the heterogeneous integration module. Thickening of the heat spreader could reduce the chips' temperatures, but the enhancement is limited. A useful and simple technique has been proposed in [32], which is to insert a metallic heat slug from the PCB side and to directly contact the back side of chip #3. The inserted slug can effectively drain out the heat of chip #3 and also help to reduce the temperature of chips #1 and #2 noticeably.

3.6.6 *Thermomechanical Analysis—Boundary Conditions*

For thermomechanical simulations, nonlinear finite element modeling and analysis are conducted to realize the thermal stress/strain distributions of the structure. At the same time, the reliability estimation of solder joints in the architecture is examined. In order to realize the nonlinear temperature and time-dependent creep behavior of solder joints, the structure is simulated under a thermal cycling condition of −25 to 125 °C for 5 cycles (Fig. 3.15).

3.6.7 *Thermomechanical Analysis—Material Properties*

All the thermomechanical material properties such as the Young's modulus, Poisson's ratio, and coefficient of thermal expansion for the material used in the structure are shown in Table 3.3. Since lead-free solders are temperature and time dependent, the following nonlinear temperature and time-dependent constitutive equations are used [33]:

$$\frac{\mathrm{d}\varepsilon}{\mathrm{d}t} = C_1[\sinh(C_2\sigma)]^{C_3}\exp\left(-\frac{C_4}{T}\right)$$

$$E(\mathrm{GPa}) = 49 - 0.07 \times T(^{\circ}C)$$

$$\alpha(\mathrm{ppm}/^{\circ}C) = 21.301 + 0.017 \times T(^{\circ}C)$$

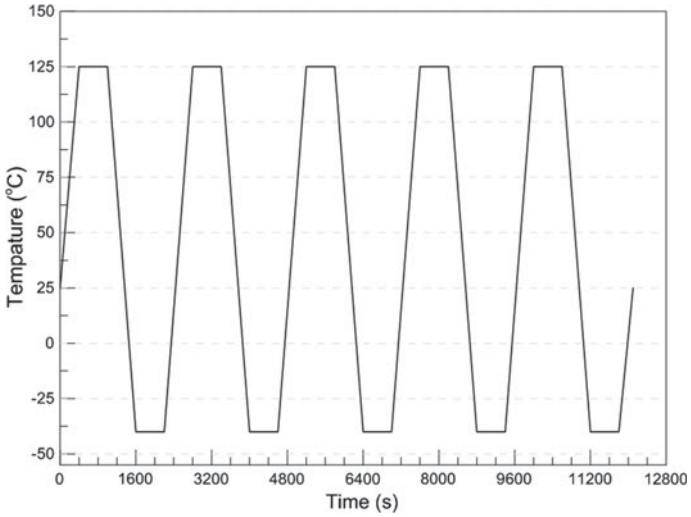


Fig. 3.15 Thermal cycling boundary condition (−25 °C ↔ 125 °C)

Table 3.3 Material properties for finite element analyses

	Young's modulus (GPa)	Poisson's ratio	CTE (ppm/K)
Silicon	130	0.28	2.8
BT substrate	X: 26 Y: 11	0.39	X: 15 Y: 52
FR4	X: 22 Y: 10	0.28	X: 18 Y: 70
Underfill	9.07	0.3	40.75
Solder alloy	Temp. dependent	0.35	Temp. dependent
Electroplated Cu	70	0.34	18
Cu low-k pad	8	0.3	10
SiO_2	70	0.16	0.6
IMC (Cu_6Sn_5)	125	0.3	18.2
Nickel	131	0.3	13.4

where

C1 = 50,000 (1/s)
C2 = 0.01 (1/MPa)
C3 = 5
C4 = 0.5 (K).

In these equations, E is the Young's modulus, α is the coefficient of thermal expansion, ε is the creep strain, K is in degree Kevin, and t is time.

Only 2D finite element modeling is performed in the thermomechanical analyses. Since the structure is symmetry and thus only half of the structure is modeled. The symmetry axis is the y-axis and proper displacement and rotational boundary conditions are applied. The temperature cycling condition is shown in Fig. 3.15, which is −25 °C ↔ 125 °C on a 60-min cycle. Stress-free is at 25 °C.

3.6.8 Thermomechanical Analysis—Results

The 2D element (PLANE182) of ANSYS Mechanical R14 is used to construct the half finite element model as shown in Figs. 3.16 and 3.17. It can be seen that the symmetry axis is the y-axis. Detailed modeling of the TSVs in the interposer and the surrounding areas is shown in Fig. 3.16. Detailed modeling of the solder bumps between the chips and interposer and the interposer and package substrate, and the solder balls between the package substrate and PCB is shown in Fig. 3.17. The whole model is subjected to the thermal cycling loading shown in Fig. 3.15 and the results are shown in the following section.

Figure 3.18 shows the von Mises stress contours in the corner TSVs at 125 °C (stress-free is at 25 °C). It can be seen that the maximum stress is ~135 MPa and the critical locations are near the interface between the filled Cu and SiO_2 of the TSV and underfill.

It is important to study the creep responses for multiple cycles by observing when the hysteresis loops become stabilized. Figure 3.19 shows the shear stress and shear creep strain hysteresis loops for multiple cycles at the corner solder bumps between Chip-2 and the interposer. It can be seen that the shear creep strain versus shear stress loop is quite stabilized after the third cycle. As a matter of fact, for those solder bumps their hysteresis loops are stabilized after the first cycle. Figure 3.19 shows the creep strain energy density history for the corner solder bumps between Chip-2 and the interposer. It can be seen that the creep strain energy density per cycle of the corner solder bumps between Chip-2 and the interposer is 0.0107 MPa. This magnitude is too small to create solder joint thermal-fatigue reliability problem under the environmental condition: −25 °C ↔ 125 °C on a 60-min cycle. Underfill helps! For the creep responses at other solder joint locations, pleased see [27].

3.6.9 Fabrication of the TSV

The schematic of the present TSV/RDL Si interposer is shown in Fig. 3.20. It can be seen that the interposer has three RDLs (TR1, TR2, and TR3) on its front side (top side) and the RDLs are formed by a Cu damascene technique. Lithography using a contact aligner provides a low-cost process as compared to a stepper/scanner under the same resolution requirements. The five layers pose challenges for manufacturing

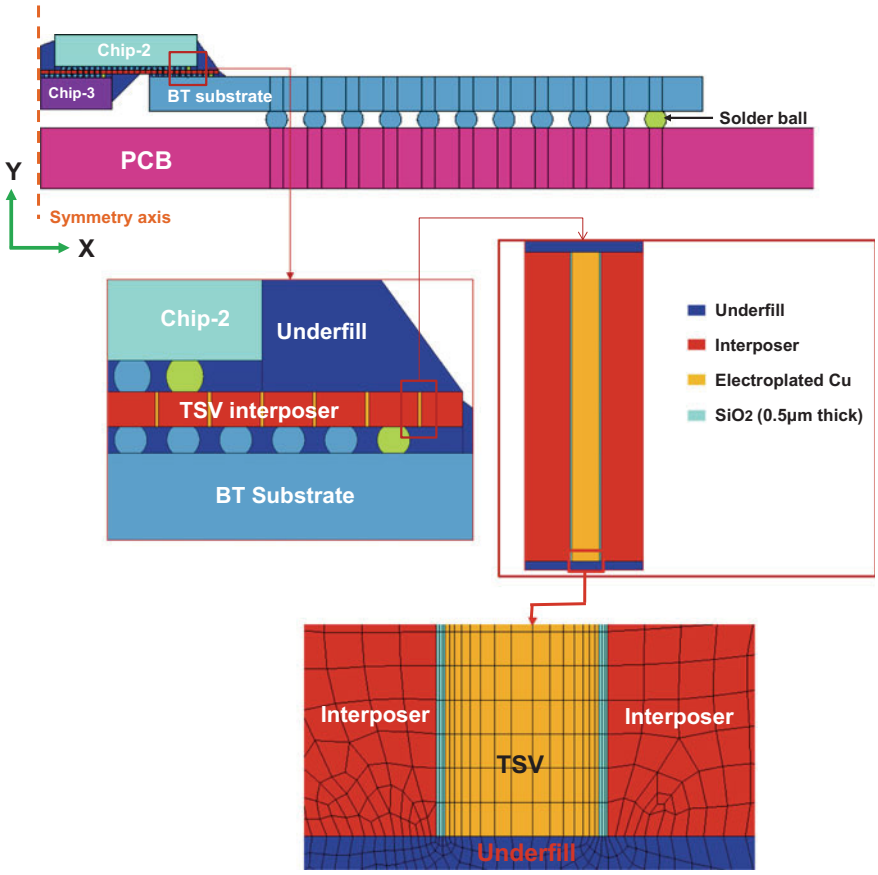


Fig. 3.16 Finite element analysis model of half of the heterogeneous integration module (showing the details of TSV and surrounding areas)

the back-side RDL using a Cu damascene process. The process flow of this TSV/RDL interposer is listed in Table 3.4.

The process starts with a SiN*x*/SiO*x* insulation layer by PECVD. After TSV lithography, the TSV is etched into the Si substrate by Boschtype DRIE to form a high-aspect ratio via structure. The etched TSV structure is then processed with a procedure of SiO*x* liner by SACVD, Ta barrier and Cu seed layers by PVD. Cu electroplating is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10 μm in diameter and a depth about 105 μm, which give an aspect ratio of 10.5. In such a high-aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness at the field. The SEM cross-section images are shown in Fig. 3.21. It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from

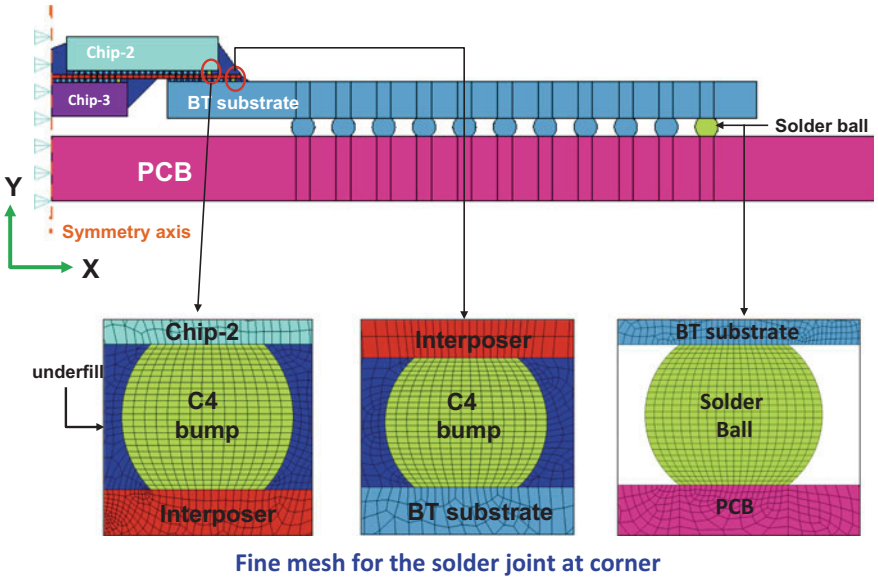


Fig. 3.17 Finite element analysis model of half of the heterogeneous integration module (showing the details of solder bumps between chip #2 and interposer and between interposer and package substrate, and solder ball between the package substrate and PCB (not-to-scale)

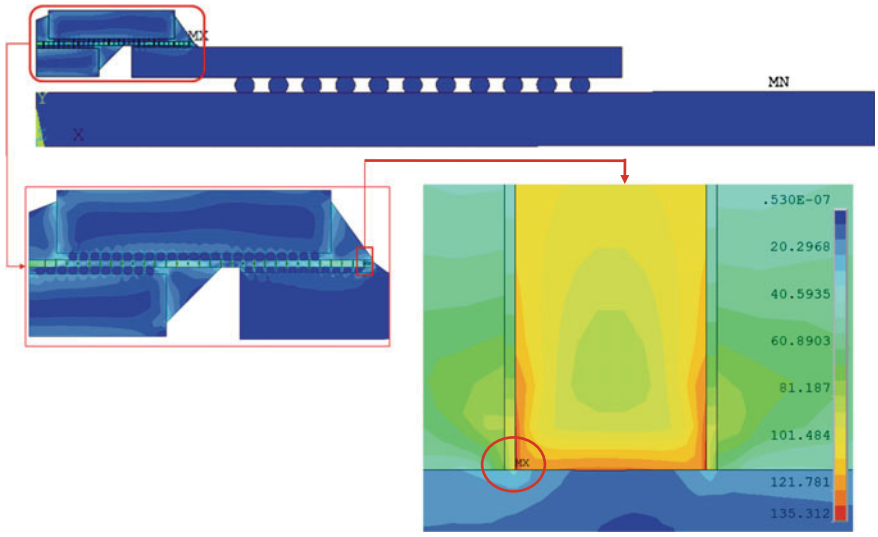


Fig. 3.18 Maximum stress acting at the TSV at 125 °C (stress free is at 25 °C)

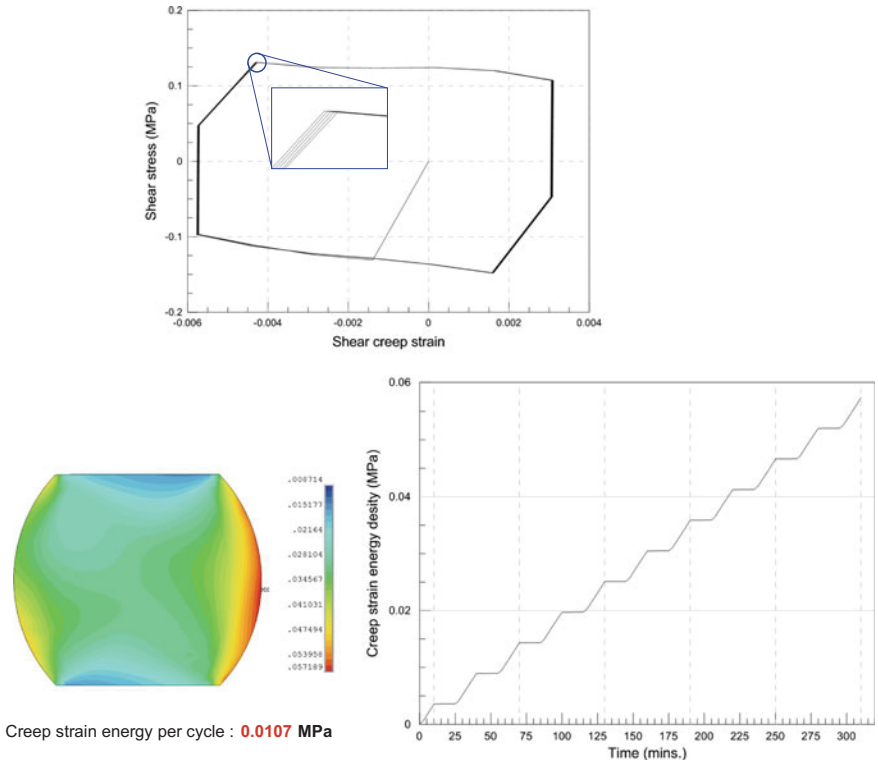


Fig. 3.19 (Top) hysteresis loop (five cycles) at the corner solder bump between chip #2 and interposer. (Bottom) creep strain energy density versus time at the corner solder bump between chip #2 and interposer

the etching process point of view. The Cu thickness at the field is less than 5 μm. After annealing (400 °C for 30 min), to complete the TSV process, excess Cu at the field is removed by CMP.

3.6.10 Fabrication of the Interposer with Top-Side RDLs

After the TSV formation, the Si interposer wafer goes through three RDL processes on the front side, using a Cu damascene technology, primarily modified from the conventional Cu BEOL (back-end-of-line) process. The CD (critical dimension) of these RDL layers is 3 μm, which is limited by the resolution of the contact aligner. Three RDL layers are built sequentially, followed by the front side UBM pads for flip chip solder bumps attachment. The UBM consists of Cu-UBM pad and NiPdAu finishing, which gives room for underfill between the active chip and the interposer and also lowers the possibility of bonding failure. Figure 3.22 shows the SEM cross-

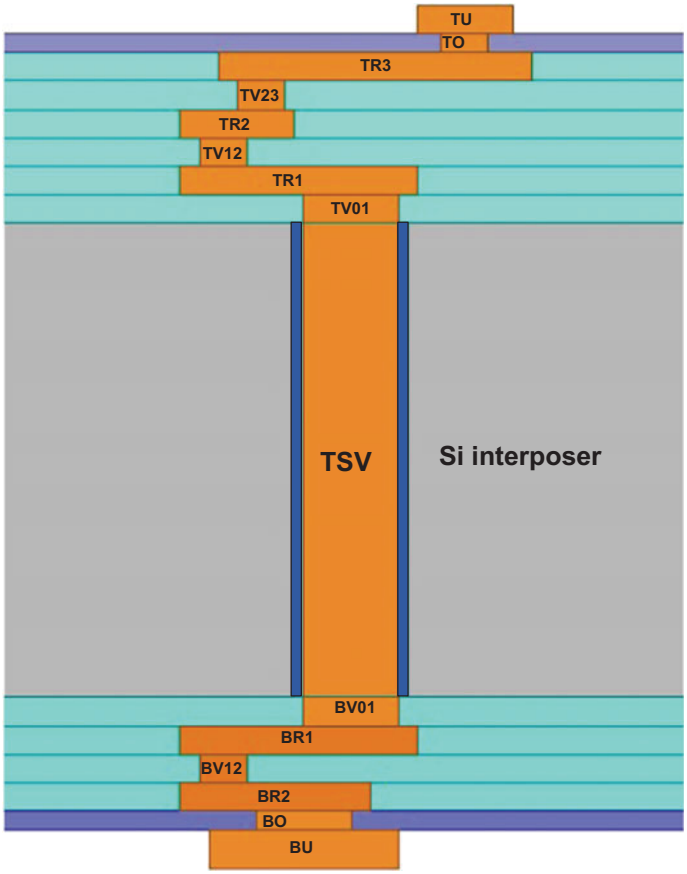


Fig. 3.20 Schematic of the cross section of the TSV-interposer with three RDLs on top and two RDLs at the bottom

sectional images of the front-side layers (TSV, three front side RDLs, and top UBM). Figure 3.23 shows the top-view of the interposer. As shown in the top-view photo, interconnecting region refers to the area for the two active die attachments, while the rest of the area is designed for passive test structures.

3.6.11 TSV Reveal of the Cu-Filled Interposer with Top-Side RDLs

After the front-side process is done, wafers thinning starts with the temporary bonding process. The Si interposer wafer is temporarily bonded to a Si carrier before being grounded and polished at the back side of the Si interposer wafer, which stops before

Table 3.4 Fabrication process flow of TSV/RDL interposer

Process stage	
Inter-layer dielectric (ILD)	
TSV	• TSV diameter = 10 μm • TSV depth = 105 μm • TSV SiO liner (SACVD) = 0.5 μm @ top • Ta barrier = 0.08 μm @ top
3 front-side RDLs	• Cu damascene • Minimum line-width = 3 μm • Minimum via diameter = 3 μm • Metal thickness = 2 and 1.5 μm • Ta barrier = 0.05 μm
Top passivation opening	• Opening diameter = 60 μm
Top UBM	• UBM size = 75 μm • Cu thickness = 5 μm • NiPdAu = 2 μm
Front-side temporary bonding to Si carrier	• Glue thickness = 25 μm
Backside thinning	• Grinding + CMP
Si recess & TSV backside reveal	• Dry etching
Backside isolation	• PECVD SiO • Temperature < 200 °C • Thickness = 1 μm
CMP for TSV Cu exposion	• Backside isolation remained > 0.8 μm on the field area
2 backside RDLs	• Cu dual-damascene • Minimum line-width = 5 μm • Minimum via diameter = 5 μm • Metal thickness = 2 μm • Ta barrier = 0.05 μm
Bottom passivation opening	• Opening diameter = 60 μm
Bottom UBM	• UBM size = 75 μm • Cu thickness = 5 μm • NiPdAu = 2 μm

the TSV is revealed. The thickness distribution across the wafer for the remaining Si-substrate after the back side grinding/polishing process is very uniform. The profile distribution is shown in Fig. 3.24. The wafer back side was then dry-etched to reveal the TSV and also to recess the Si surface. The isolation dielectrics are deposited before CMP to expose the TSV back side Cu surface for connecting to back side RDL. Due to the maximum working temperature of the temporary bonding adhesive, the temperature of the back-side processes is restricted to less than 200 °C.

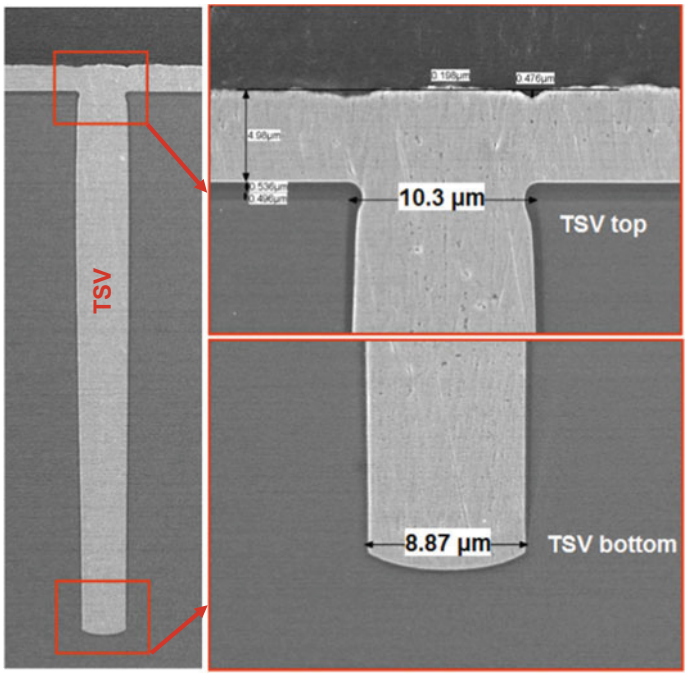


Fig. 3.21 SEM cross-section images of the TSV

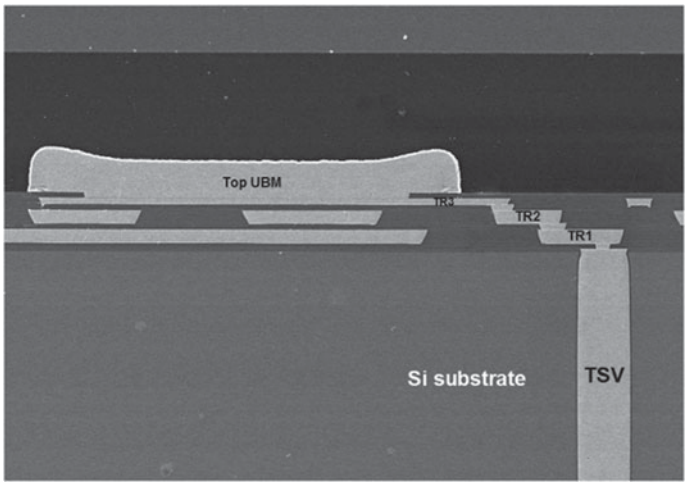


Fig. 3.22 SEM cross-sectional images of the top side of the interposer (TSV, RDLs: TR1, TR2, TR3, and the top UBM)

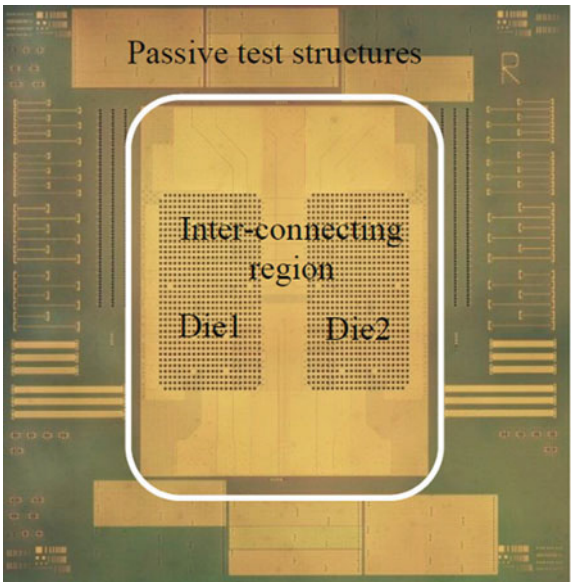


Fig. 3.23 Top-view of the TSV/RDL interposer

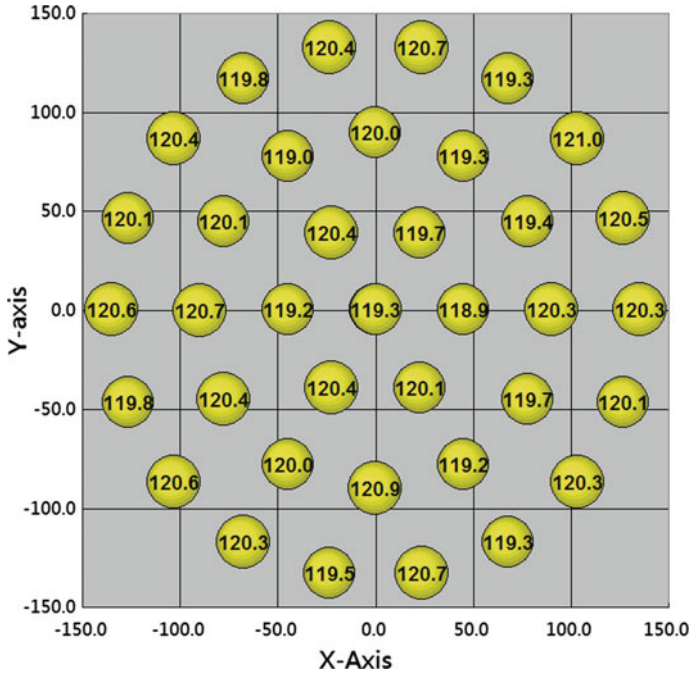


Fig. 3.24 Mapping of the Si-substrate remained thickness after back side grinding

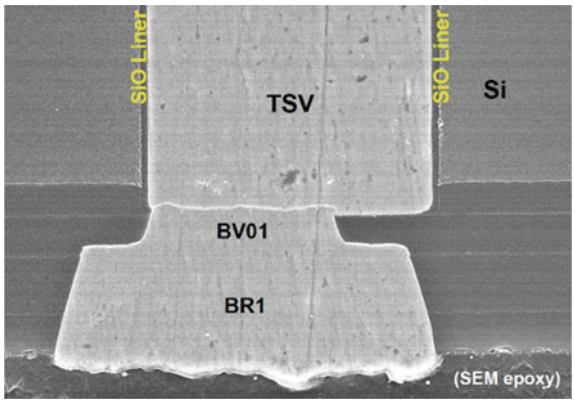


Fig. 3.25 SEM cross-sectional image of Cu dual-damascened first back side RDL (BR1 + BV01) connecting to the bottom of TSV

3.6.12 Fabrication of the Interposer with Bottom-Side RDLs

Due to the concerns of mask alignment capabilities with the contact aligner and the wafer warpage from both front-side processing and the temporary bonding process, the minimum CD of the back-side RDL is relaxed to 5 μm. Also, to reduce process-induced cracking or chipping on the thinned wafer, the back-side RDL process utilizes Cu dual-damascene technique (RDL + via formation with one ECD and CMP). The SEM cross-section image of the first back-side RDL/via Cu dual-damascene metallization (connecting to the TSV backside) is shown in Fig. 3.25. Similar to the front-side process, two back-side RDLs were done sequentially, followed by the back-side UBM pads for the solder bumps for the back-side flip chip attachment and for the organic substrate, respectively.

Figure 3.26 shows the SEM cross-section of all back-side layers (TSV, 2 back-side RDLs, and bottom UBM), and Fig. 3.27 shows the bottom-view of the interposer. To complete the Si interposer process, de-bonding of the thinned Si interposer wafer from the Si carrier is performed before the thinned Si interposer wafer is diced. The diced interposer die is ready for heterogeneous integration assembly and also for passive electrical characterization on the interposer and package.

3.6.13 Passive Electrical Characterization of the Interposer

Measurement and modeling results for various micro-striplines, striplines, and coplanar waveguide lines of the fabricated interposer have been reported in [24]. Figure 3.28 shows the electrical performance (insertion loss and return loss) for three different cases. There is discrepancy shown between the measured and the 3D field solver modeling results when nominal design dimensions are used. However, when actual manufactured dimensions are used (from Fig. 3.29), the correlation between the model and measured results is very good.

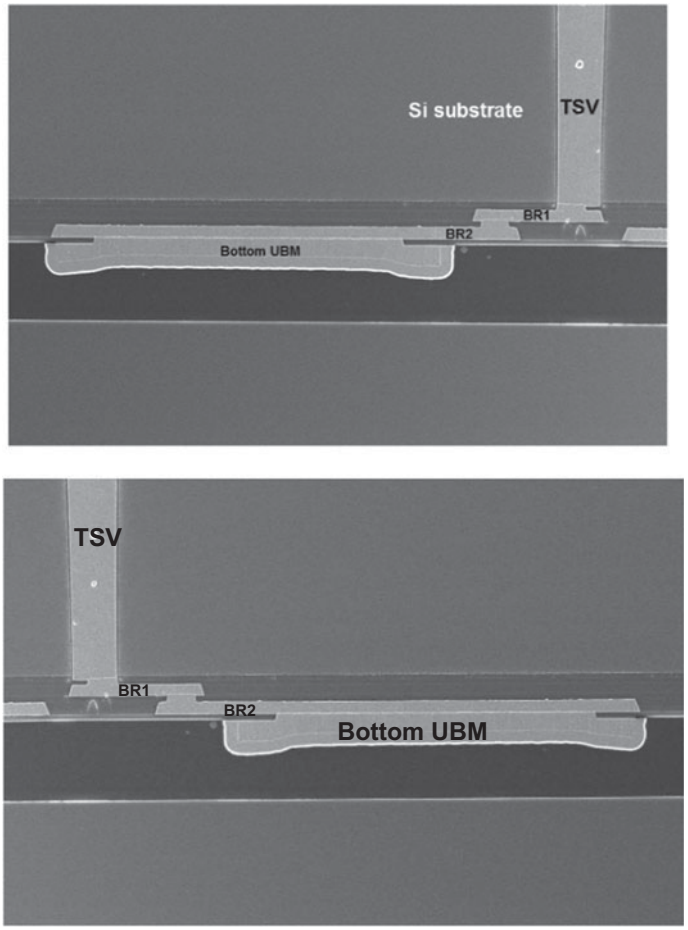


Fig. 3.26 SEM cross-sectional images of the back-side of the interposer (TSV, RDLs: BR1, BR2, and bottom UBM)

3.6.14 Final Assembly

Figure 3.30 schematically shows the process flow of the final module assembly. First, attach the back-side chip on the interposer, then naturally reflow the solder, apply and cure the underfill. Attach the interposer on the top side of the organic package substrate and naturally reflow. Then apply the underfill and cure. Attach the two top-side chips on the top side of the interposer, naturally reflow the solder, then apply and cure the underfill. Finally, solder ball mounting on the bottom side of the package substrate and reflow as shown in steps 7 and 8 of Fig. 3.30.

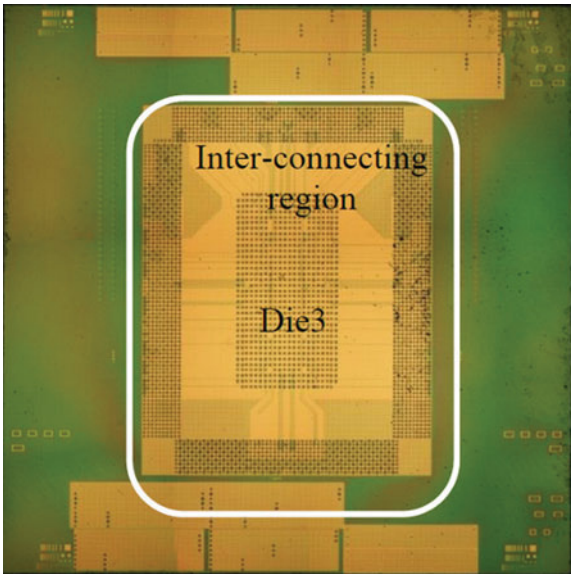


Fig. 3.27 Bottom-view of the TSV-interposer

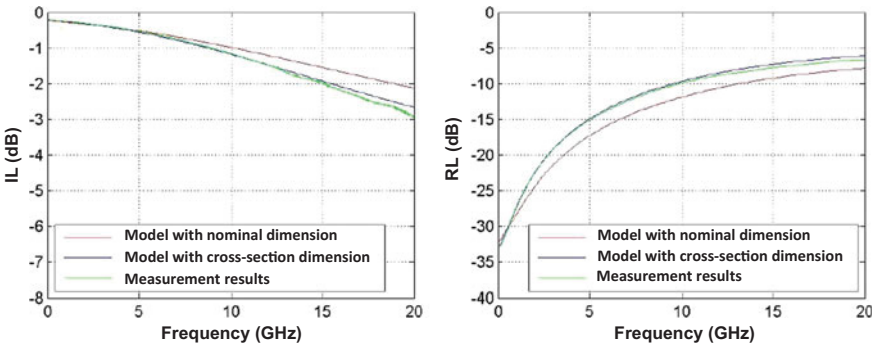


Fig. 3.28 Simulation and measurement correlation results

Figure 3.31 shows an assembled package, which consists of a passive TSV-interposer supporting two active chips on the top side (with underfill) (left-hand side of Fig. 3.31) and one active chip on the bottom side (with underfill) (right-hand side of Fig. 3.31). This interposer with the chip set is soldered to the top side of a package substrate with cavity.

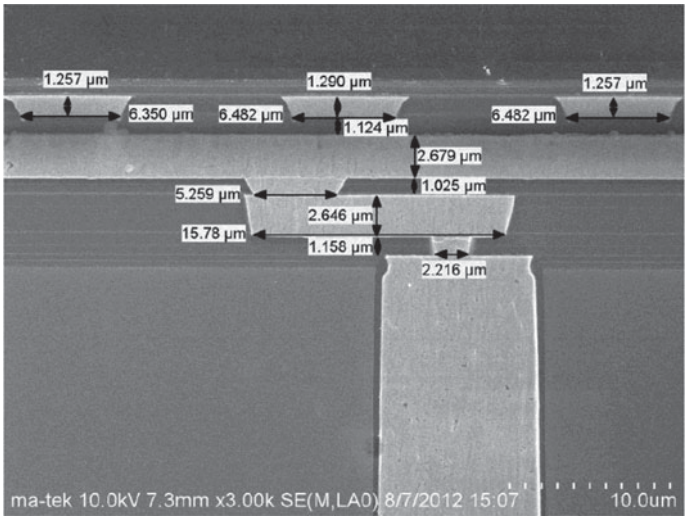


Fig. 3.29 SEM cross-sectional image of the TSV-interposer for simulation and measurement

Figure 3.32 shows the cross-sections of the fully assembly module. It can be seen that the interposer is properly supporting the three chips with underfill. This interposer is soldered (with underfill) to a 4-2-4 package substrate. Figure 3.33 shows the X-ray image from the top-view of the fully assembly module, demonstrating the assembly is done properly. It can be seen that the two dies (un-thinned) at the front side and one die at the back side are perfectly aligned, with solder bumps (connecting the interposer to the package BT-substrate) at the peripheral regions on the interposer back side.

3.7 Summary and Recommendations

Some important results and recommendations are summarized as follows:

- Because of the drive of AI, the semiconductors such as the CPU, GPU, HBM, or FPGA's density and I/Os increase, pad-pitch decreases, and chip size increases. Even a 12 build-up layers (6-2-6) organic package substrate is not enough to support the semiconductor chips and a TSV-interposer is needed.

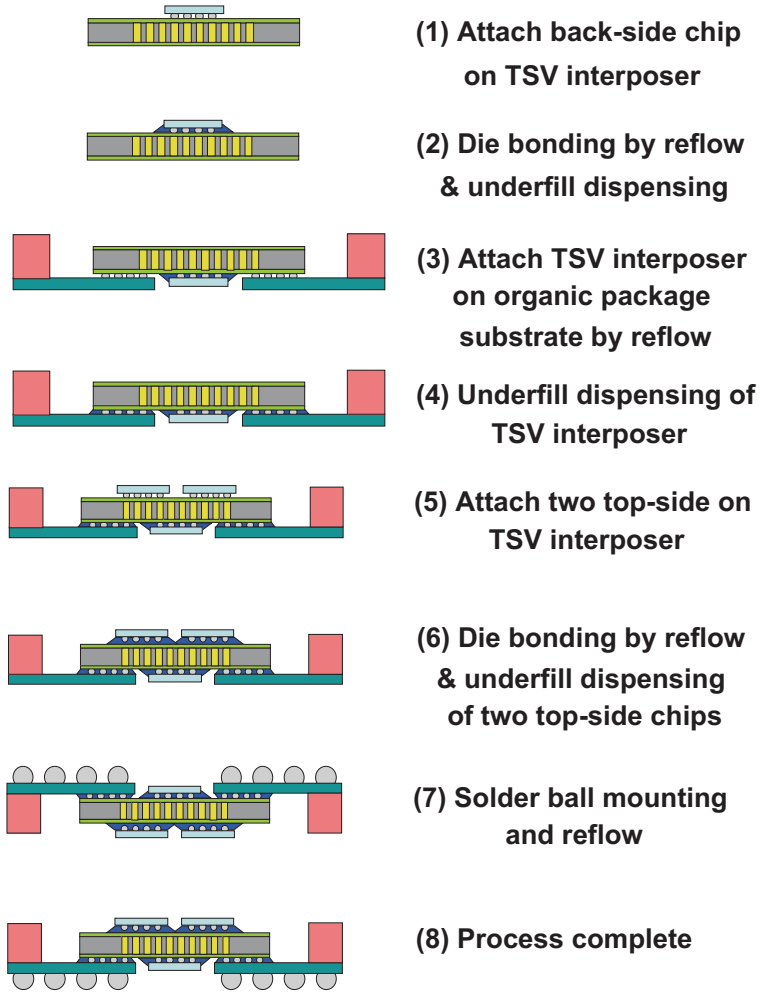


Fig. 3.30 Final TSV-interposer and chips assembly process flow

- The RDLs of heterogeneous integrations on silicon substrates (TSV-interposers) are made by the PECVD and Cu-damascene + CMP method. Thus, the metal line width and spacing of the RDLs can go down to sub-micron and this kind of heterogeneous integration can achieve the best performance.
- However, the heterogeneous integrations on silicon substrates (TSV-interposers) are the most expensive. Thus, lower cost TSV-interposers should be developed.
- Currently, heterogeneous integrations on silicon substrates (TSV-interposers) are used by companies such as Xilinx, NVidia, and AMD and the TSV-interposers are fabricated by TSMC and UMC.

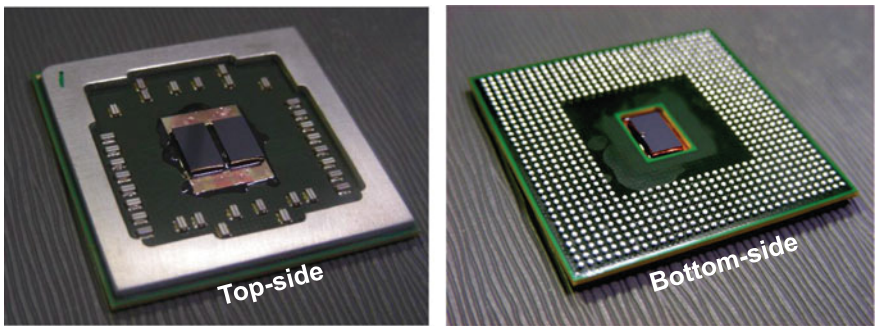


Fig. 3.31 Fully assembled heterogeneous integration module. (Left) top side showing the two chips. (Right) bottom side showing the one chip

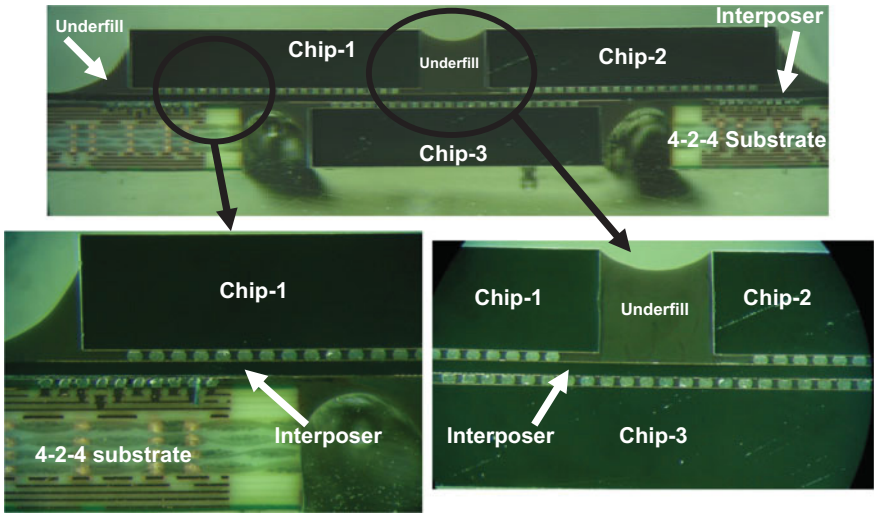


Fig. 3.32 Cross-section of the fully assembled module (three chips, TSV-interposer, package substrate, and underfill)

- For the double-sided interposer for heterogeneous integrations, the interposer is supporting chips on its top and bottom sides. In this case, the size of the interposer can be smaller (or more chips can be placed on the same size of interposer), and the electrical performance can be better because the chip-to-chip interconnects are face-to-face instead of side-to-side. Also, it is truly a 3D (not 2.5D) IC integration with TSV-interposer.

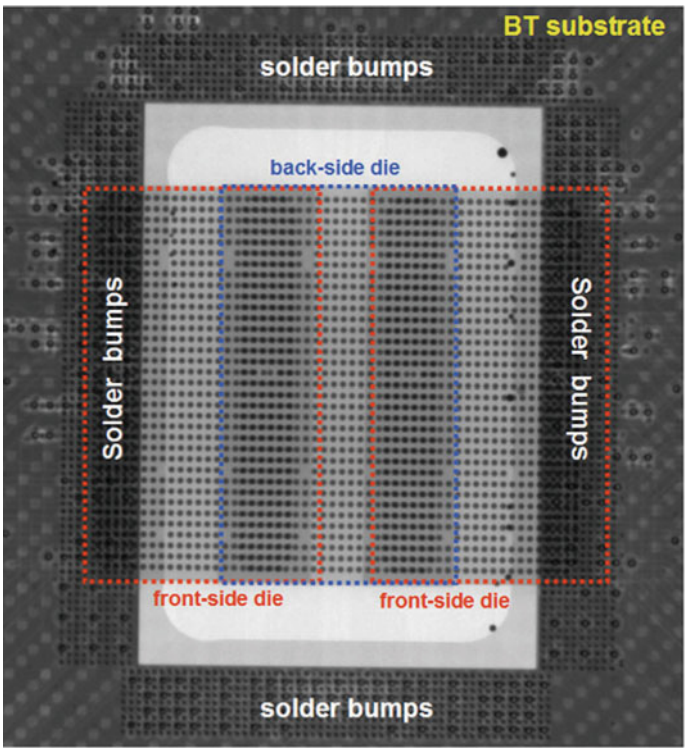


Fig. 3.33 X-ray image from the top-view of the fully assembled heterogeneous integration

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Chapter 4
Heterogeneous Integrations on Silicon Substrates (Bridges)



4.1 Introduction

Through-silicon via (TSV)-interposer is very expensive [1–10]. Silicon bridges are one form of silicon substrates to support heterogeneous integrations. Basically, a bridge is a piece of dummy silicon with RDLs (redistribution-layers) and contact pads, but without TSVs (through-silicon vias), i.e., a TSV-less interposer. Usually, the RDLs and contact pads are fabricated on a dummy silicon wafer and then diced into individual bridges. In this chapter, the fabrication of Intel's EMIB (embedded multi-die interconnect bridge) [11–13] will be mentioned. Also, imec's bridges [14] for the communications of heterogeneous integrations will be briefly discussed. Finally, ITRI's TSH (through-silicon hole) interposer (bridge) [15–18] will be presented.

4.2 TSV-Less Interposer: Intel's EMIB

Usually, TSV interposer is very expensive [1–10]. Intel proposed an embedded multi-die interconnect bridge (EMIB) [11, 12] to replace the TSV interposer. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the organic package substrate as shown in Figs. 4.1 and 4.2 [11, 12]. On November 9, 2015, Altera/Intel announced the industry's first heterogeneous integration devices that integrate stacked HBM from SK Hynix with high-performance Stratix® 10 FPGAs and SoCs as shown in Fig. 4.1. It can be seen that the TSV interposer is gone and replaced by Intel's EMIB. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB.

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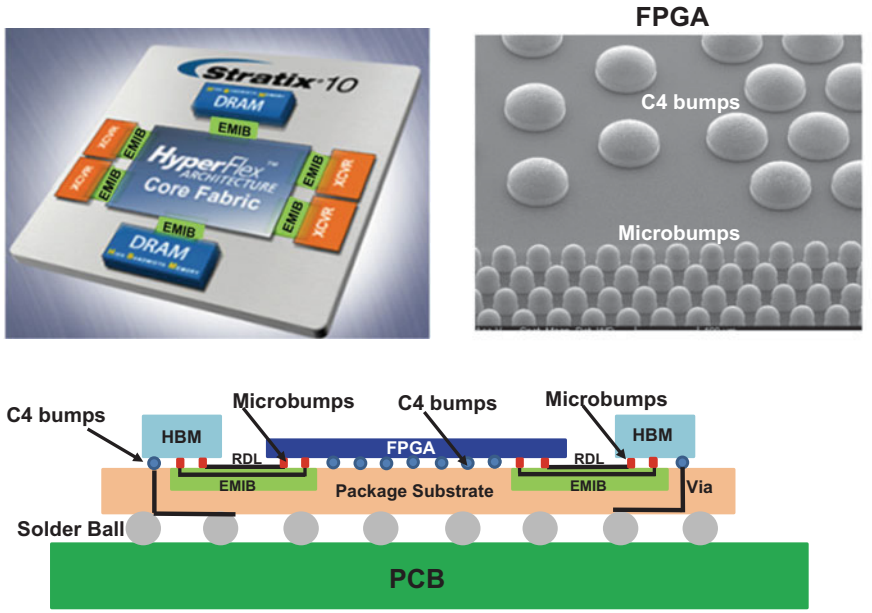


Fig. 4.1 Heterogeneous integration using Intel's EMIB for HBM and FPGA interconnections

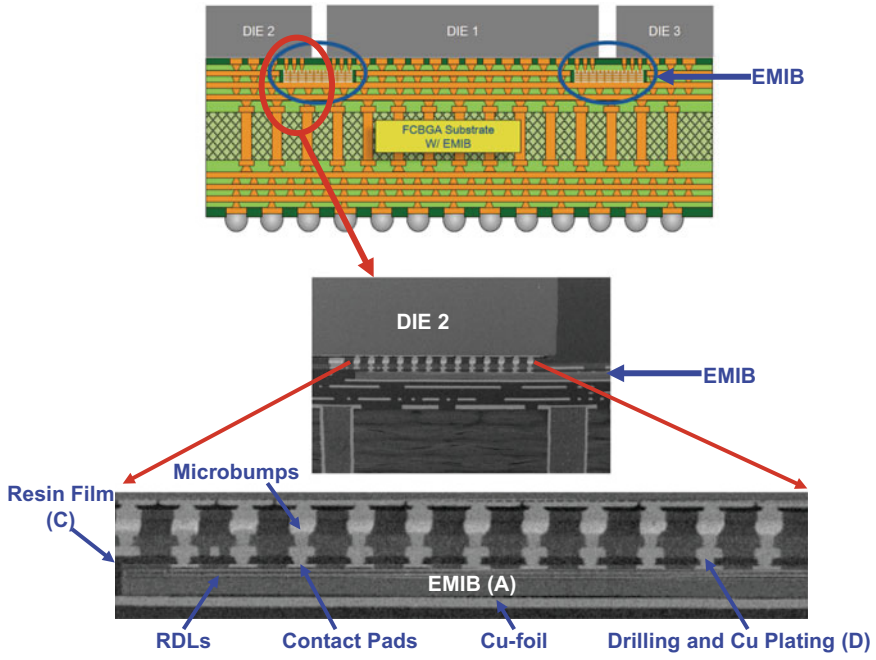


Fig. 4.2 Intel's EMIB: TSV-less interposer

4.3 Fabrication of the EMIB

To make the EMIB, one must first build the RDLs (including the contact pads) on a Si-wafer. The way to make the RDLs depends on the line width/spacing of the conductive wiring of the RDLs. Finally, attach the non-RDL side of the Si-wafer to a die-attach film, and then singulate the Si-wafer into individual bridges.

4.3.1 Fabrication of Bridges with Fine RDLs

For fine line width and spacing (>2 μm) of the metal of RDLs, the organic RDLs (polymer and ECD Cu+ etching) should be adequate. If the line width and spacing are ultra-fine (≤2 μm or even in the submicron region), then inorganic RDLs (PECVD and dual Cu-damascene + CMP) should be used.

The key process steps for fabricating organic RDLs for fine line width and spacing are shown in Fig. 4.3. It can be seen that for the PI (polyimide) development, the whole Si-wafer is spin-coated with a photosensitive PI. It is followed by applying a mask aligner or stepper (for higher yields) and then using photolithography techniques to align, expose, and develop the vias of the PI. Finally, the PI is cured at 200 °C for one hour- this will form a 5 μm-thick PI layer. It is followed by sputtering Ti and Cu by PVD at 175 °C over the entire Si-wafer. Then, apply a photoresist and a mask aligner or stepper and use photolithography techniques to open the redistribution trace's locations. Next, electroplate the Cu by ECD at room temperature on the Ti/Cu in the photoresist openings. These steps are followed by stripping off the photoresist and etching off the Ti/Cu; RDL1 is thereby obtained. Finally, repeat all the above steps to obtain other RDLs. For example, the RDLs in Fig. 4.4 are fabricated by this method. The line width and spacing of the metal of the RDLs can be as little as 5 μm for high yield.

4.3.2 Fabrication of Bridges with Ultra-Fine RDLs

The key process steps for fabricating bridges with ultra-fine line width and spacing of the metals of RDLs are shown in Fig. 4.5. This is the oldest back-end semiconductor process. This process uses SiO_2 or SiN for the dielectric layer and ECD to deposit the Cu on the whole wafer. That is followed by using CMP (chemical-mechanical polishing) to remove the overburden Cu and seed layer to make the Cu conductor layer of the RDLs. First, use plasma enhance chemical vapor deposition (PECVD) to form a thin layer of SiO_2 (or SiN) on a full thickness bare silicon wafer and then use a spin coater to laminate the photoresist. These steps are followed by using a stepper to open the resist and a reactive ion etch (RIE) to remove the SiO_2. Then, a stepper is used to open the resist wider and RIE to etch more of the SiO_2. Next, strip

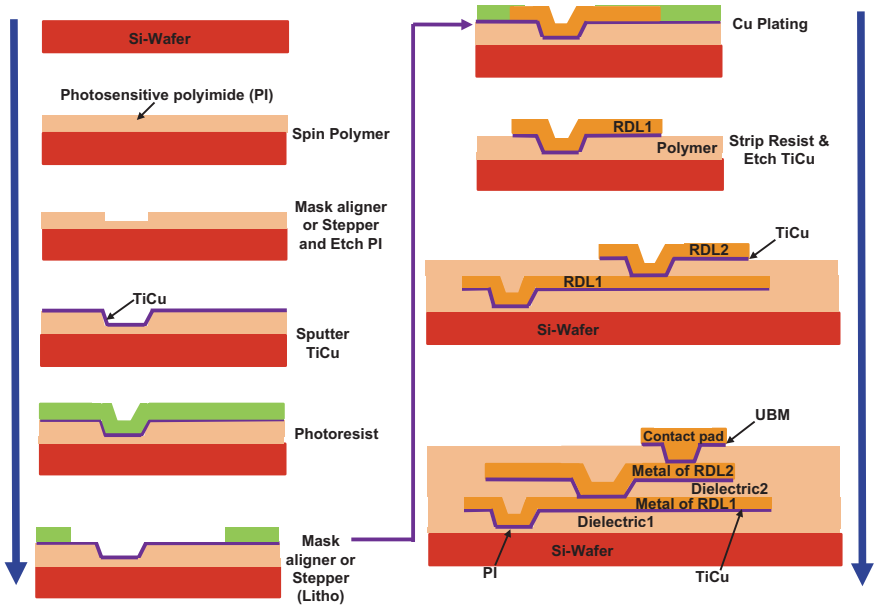


Fig. 4.3 Key Process steps for making fine line width and spacing RDLs on a Si-wafer

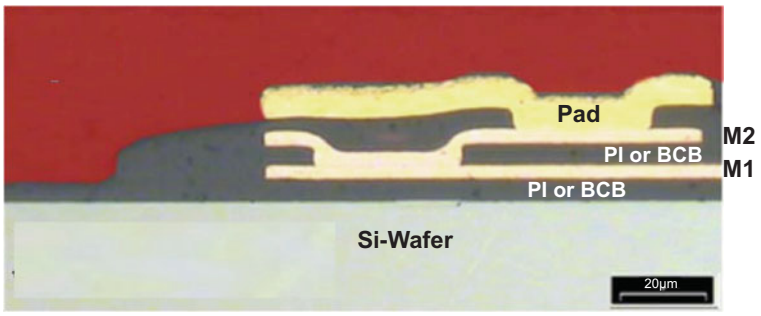


Fig. 4.4 Cross section of 2RDLs on a Si-wafer by organic RDL method

off the resist, sputter the TiCu, and ECD the Cu on the whole wafer. These steps are followed by CMP to remove the overburden Cu and the TiCu, and then we have the first RDL1 and V01 (the via connecting the Si and RDL1) as shown in Fig. 4.6. This is called the dual Cu-damascene method [19]. Finally, repeat all the processes to get the other RDLs. The line width and spacing of the metals of RDLs can be $\leq 2\ \mu m$ and down to submicron.

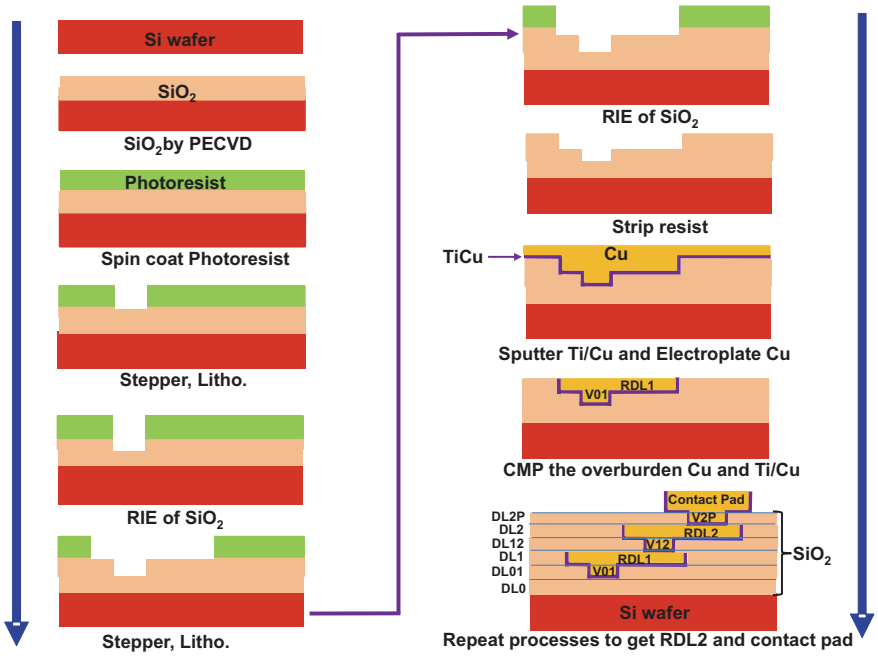


Fig. 4.5 Key Process steps for making ultra-fine line width and spacing RDLs on a Si-wafer

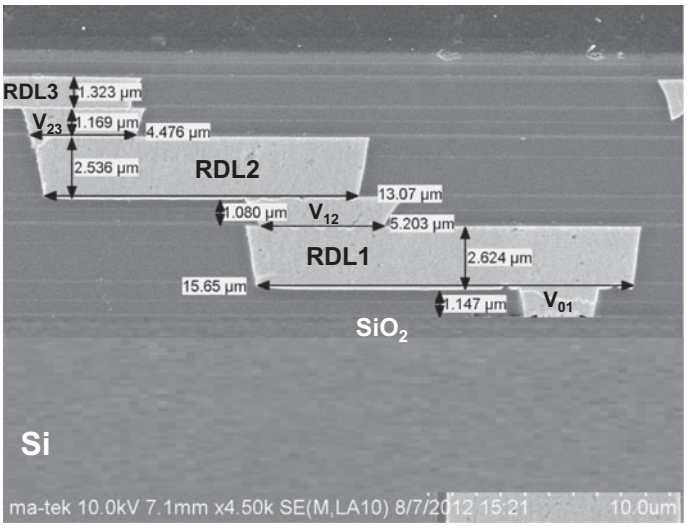


Fig. 4.6 Cross section of 3RDLs on a Si-wafer by inorganic RDL method

4.4 Fabrication of Intel's Organic Substrate with EMIB

To make the substrate with an EMIB, first place the singulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate, Fig. 4.7a. It is followed by laminating a resin film on the whole organic package substrate. Then, drilling (on epoxy resin) and Cu plating to fill the holes (vias) to make connections to the contact pads of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown in Fig. 4.7b. Then, it is followed by laminating another resin film on the whole substrate and drilling (on resin) and Cu plating to fill the holes and make contact pads, Fig. 4.7c. (Smaller pads on a finer pitch are for microbumps, while larger pads on a gross pitch are for ordinary bumps.) The organic package substrate with an EMIB is ready for bonding of the chips as shown in Fig. 4.7d. The build-up of the organic substrate on top of the EMIB can also be fabricated by semi-additive process as shown in Chap. 2.

4.5 Final Assembly

It is interesting to note that in order to use the EMIB, the chips will have different kinds/sizes of bumps as shown in Fig. 4.1, i.e., C4 bumps and microbumps (Cu-pillar + solder cap). Wafer bumping and flip-chip assembly could be challenging and required more works in assembly developments. Figure 4.8 shows an example

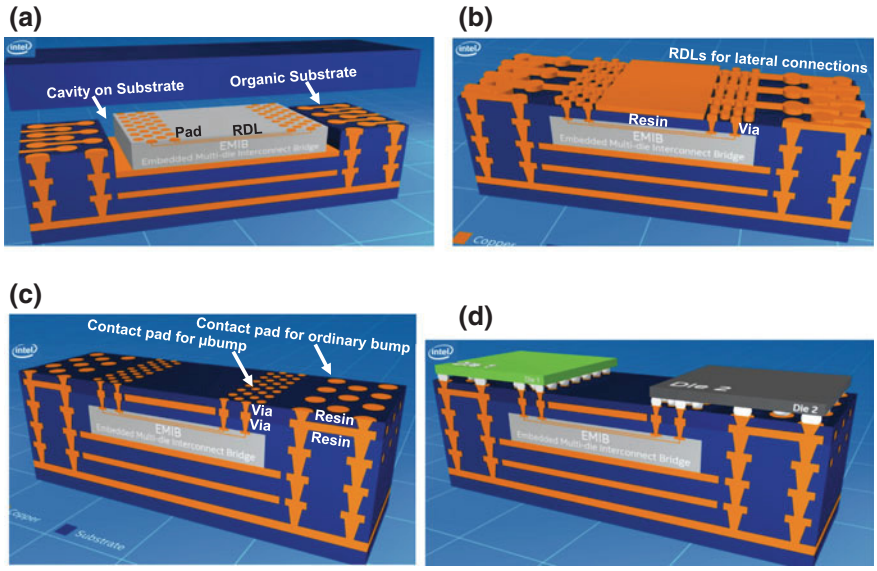


Fig. 4.7 Key process steps for making Intel's organic substrate with EMIB

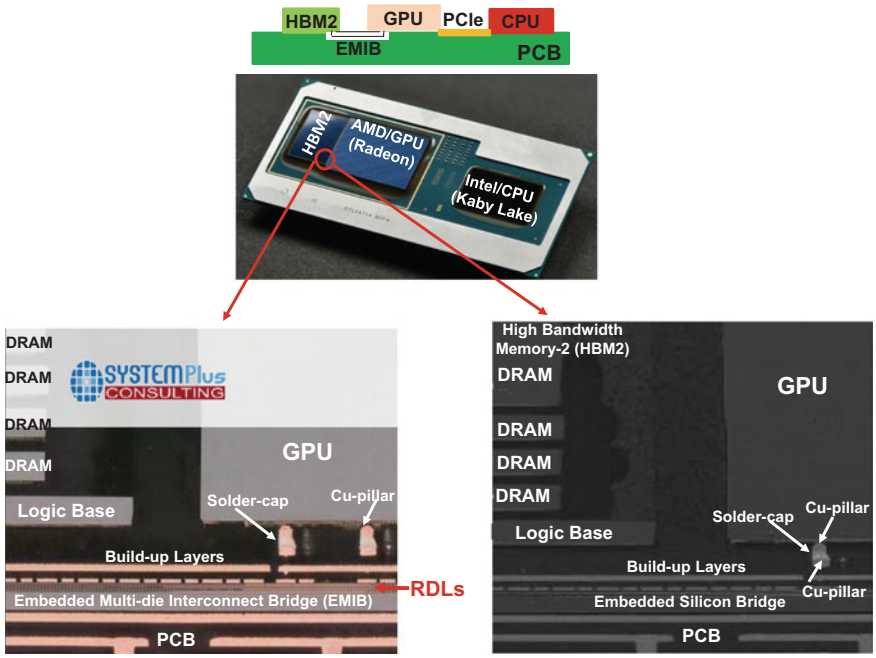


Fig. 4.8 Intel's heterogeneous integration of CPU, GPU, and HBM with EMIB for their NB

of heterogeneous integration of Intel's CPU and AMD's GPU + HBM. The GPU and HBM are on an organic substrate with EMIB and build-up layers. Figure 4.9 shows [13] a future heterogeneous integration of Intel's CPU, AMD's GPU, and Hynix's HBM. They are connected through EMIBs.

4.6 Imec's Bridges for Heterogeneous Integration

Ever since Intel's proposal of using EMIB to serve as the high-density interconnects between chips in a heterogeneous integration system was put forth, the "bridge" has been very popular. For example, recently, imec proposed [14] the use of the bridges + fanout wafer-level packaging (FOWLP) technology to interconnect the logic chip, wide I/O DRAM, and the flash memory as shown in Fig. 4.10. Their objective is not to use TSVs for all the device chips.

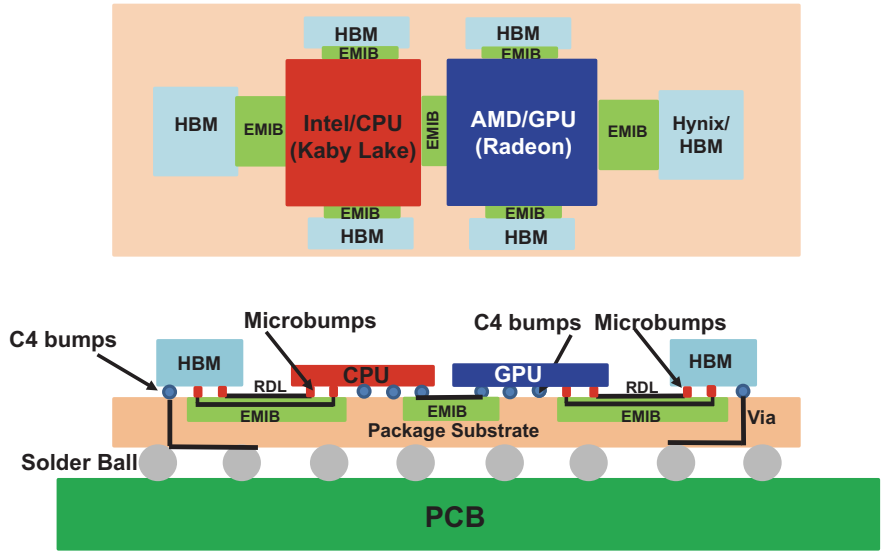


Fig. 4.9 Intel's future heterogeneous integration of CPU, GPU, and HBM with EMIBs for their HPC

4.7 Assembly Process Steps for Imec's Heterogeneous Integration with Bridges

Figure 4.11 shows the key process steps in assembling of the heterogeneous integration system shown in Fig. 4.10. First, micro wafer bumping of all the chips, bridges, and TPVs (through package vias). Also, fabricate the RDLs on the bridges. It is followed by attaching the logic chip and TPVs on a carrier-1. Then, stack the bridges on the logic chip and TPVs (through package vias). Compression molding and back-

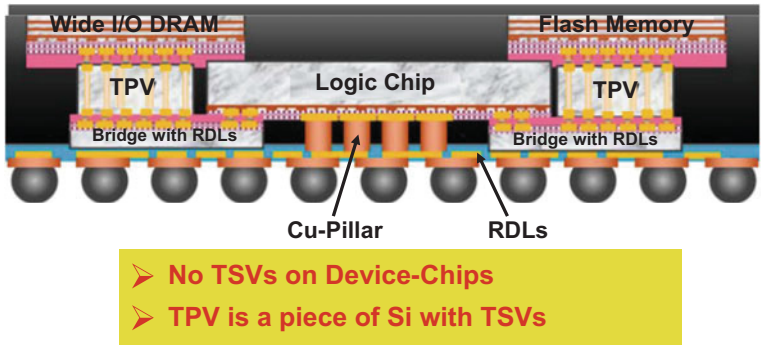


Fig. 4.10 Imec's heterogeneous integration of logic, memory, and flash with bridges

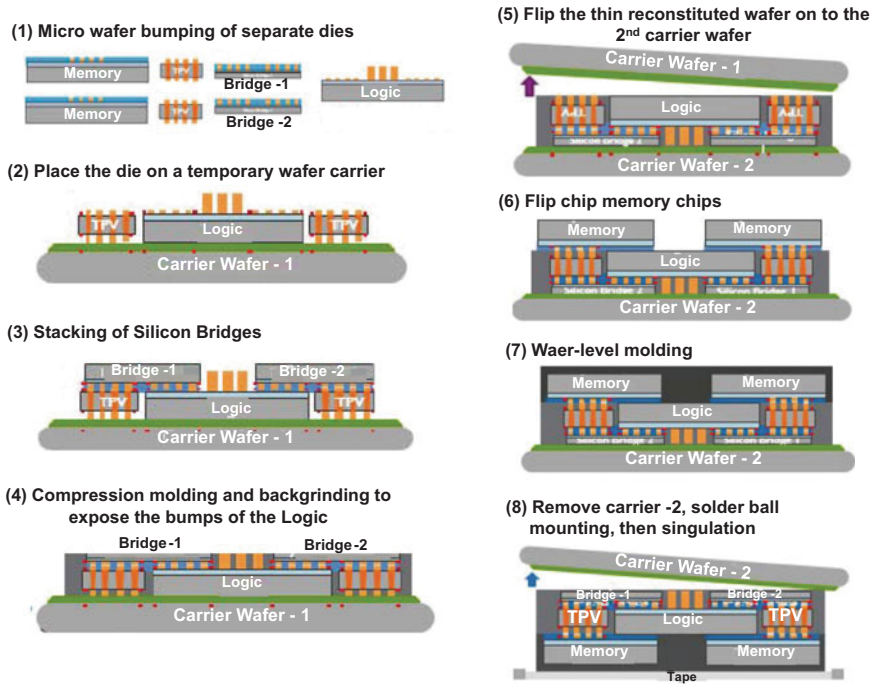


Fig. 4.11 Key process steps for making imec's heterogeneous integration with bridges

grinding to expose the bumps of the logic chip. Then, make RDLs form the Cu-pillars of the logic chip. It is followed by attaching the reconstituted wafer to another carrier-2 and remove carrier-1. Then attach the memory chips to the logic chip and TPVs. Finally, remove carrier-2, attach solder balls, and singulate the reconstituted wafer individual heterogeneous integration package.

4.8 Low-Cost TSH Interposer (Bridge) for Heterogeneous Integrations

As mentioned in Chap. 3 that usually there are six key steps in making a TSV and it is expensive. Thus, how to make low-cost TSV-less interposer is one of the important research topics for heterogeneous integration. In this section, a class of very low-cost interposer (bridge) with through-silicon holes (TSHs) and with chips on its both sides is proposed and developed [15–18].

4.8.1 The Structure

Figure 4.12 schematically shows a heterogeneous integration with a TSH interposer (bridge) supporting a few chips on its top and bottom side. The key feature of TSH interposers is that there is no metallization in the holes. Thus, dielectric layer, barrier and seed layers, via filling, CMP for removing overburden copper, and Cu revealing are not necessary. Comparing to the TSV interposers, TSH interposers only need to make holes (by either laser or DRIE) on a piece of dummy silicon wafer. Just like all the bridges, RDLs are needed by the TSH interposers.

The TSH interposers can be used to support the chips on its top side as well as bottom side. The holes can let the signals of the chips on the bottom side transmit to the chip on the top side (or vice versa) through the Cu pillars and solders. The chips on the same side can communicate to each other with the RDLs of the TSH interposer. Physically, the top chips and bottom chips are connected through Cu pillars and micro solder joints. Also, the peripherals of all the chips are soldered to the TSH interposer for structural integrity to resist shock and thermal conditions. In addition, the peripherals of the bottom side of the TSH interposer have ordinary solder bumps which are attached to a package substrate.

In this section, a very simple test vehicle is fabricated to demonstrate the feasibility of this heterogeneous integration with TSH interposer (bridge) technology. The design, materials, and process of the top chip with Cu pillars, bottom-chip with solder bumps, and TSH interposer will be presented. The final assembly of the heterogeneous integration test vehicle which consists of the chips, bridge, package substrate,

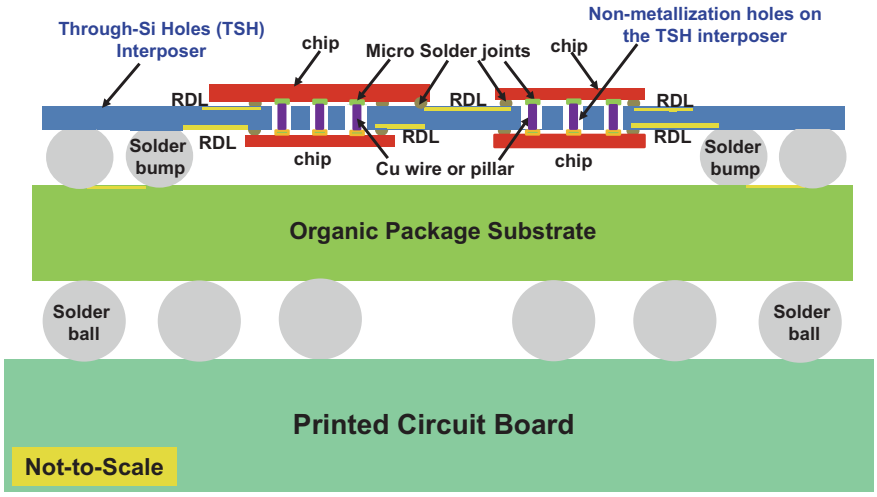


Fig. 4.12 A heterogeneous integration which consists of a TSH interposer (bridge) supporting chips with Cu pillars on its top side and chips with solder bumps on its bottom side

and PCB will also be provided. Shock and thermal cycling tests will be performed to demonstrate the integrity of the heterogeneous integration structure. Electrical simulations of the proposed structure and the results compared with the structure with TSVs will be briefly mentioned first.

4.8.2 Electrical Simulation

Figure 4.13 shows the material, geometry, and dimension of the TSV and TSH under simulations. It can be seen that 3D axial-symmetry structure is used and the finite element code is ANSYS-HFSS and simulation frequency is up to 20 GHz. The thickness of both interposers is the same (100 μm). Two different pitches are considered, one is 100 μm and the other is 200 μm. The diameter of the TSV is 15 μm and two different SiO_2 thicknesses are considered, 0.2 and 0.5 μm. Two different sizes of the air-hole are considered, 7.5 and 15 μm.

The simulation results are shown in Figs. 4.14 and 4.15 for via pitches equal to 100 and 200 μm, respectively. It can be seen that (1) for both pitches, there is very small difference in S21 for the two sizes of air-hole considered in TSH; this gives more freedom for mechanical design without affecting the electrical performance, and (2) for both pitches, the S21 of the TSH is much better than TSV, which means the TSH has much smaller insertion loss than TSV for high frequency signal transit.

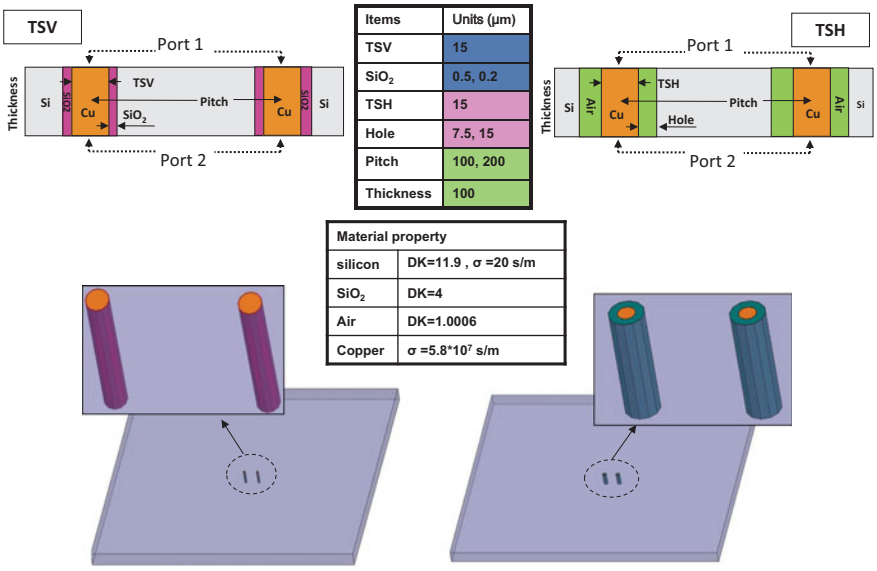


Fig. 4.13 Electrical simulation structure of the TSV and TSH (bridge) interposers

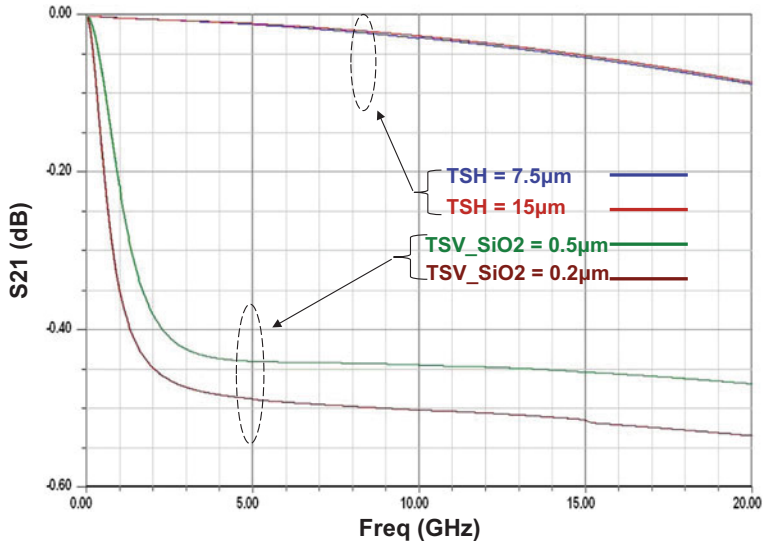


Fig. 4.14 S21 for TSH (bridge) and TSV interposers (pitch = 100 µm)

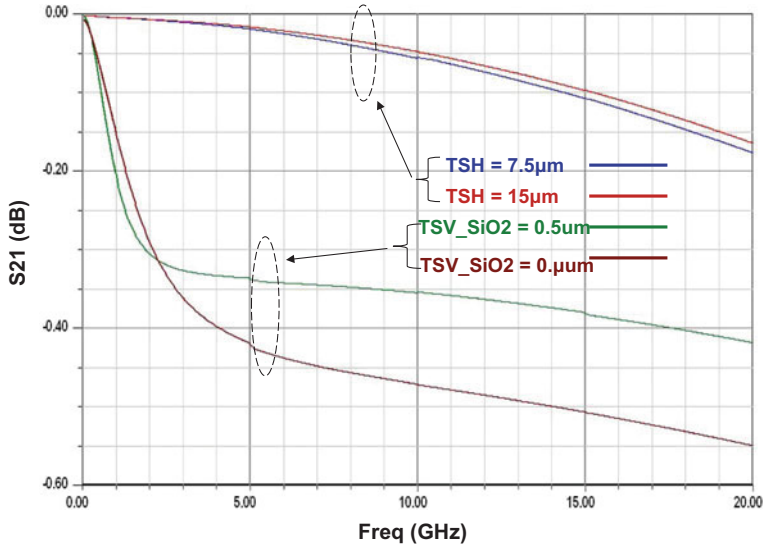


Fig. 4.15 S21 for TSH (bridge) and TSV interposers (pitch = 200 µm)

Thus, as expected, the electrical performance of the new design TSH is better that the conventional TSV [17, 18].

4.8.3 *Test Vehicle*

The test vehicle is shown in Fig. 4.16. It can be seen that it consists of a TSH interposer (bridge), which is supporting a top chip with Cu pillars and a bottom chip with UBM and solder. The bridge is connected to a package substrate and then attached to a PCB.

The dimensions of the top chip are 5 mm × 5 mm × 725 μm. The chip has (16 × 16 = 256) Cu pillars at its central portion and two-row (176) of Cu UBM/pads at its peripherals. The diameter of the Cu pillars is 50 μm. They are 100 μm tall and on 200 μm pitch as shown in Fig. 4.17 and Table 4.1. The thickness of the peripheral Cu UBM/pads is 9 μm and with electroless (2 μm) Ni and immersion (0.05 μm) Au (ENIG). The dimensions of the bottom chip are also 5 mm × 5 mm × 725 μm. The chip has 432 Cu UBM/pads (4 μm) and coated with Sn solders (5 μm). The central 256 are for the interconnections of the Cu pillars of the top chip.

The dimensions of the bridge (TSH interposer) are 10 mm × 10 mm × 70 μm (Figs. 4.17 and 4.18). It has 256 holes at its central portion to let the Cu pillars to pass through. The diameter of the holes is 100 μm and the pitch of the holes is 200 μm. There are two rows (176) of peripheral Cu UBM/pads (4 μm) coated with Sn solders (5 μm) on the top side of the bridge for the interconnections of the top chip. On the other hand, there are two rows (176) of peripheral Cu UBM/pads (9 μm) with ENIG (2 μm) on the bottom side of the bridge or the interconnections of the bottom chip.

The dimensions of the organic package substrate are 15 mm × 15 mm × 1.6 mm. There is a cavity (6 mm × 6 mm × 0.5 mm) on the top side of the substrate for the bottom-chip. The dimensions of the PCB are 132 mm × 77 mm × 1.6 mm, which is a standard size of the JEDEC (JESD22-B111) specification [20].

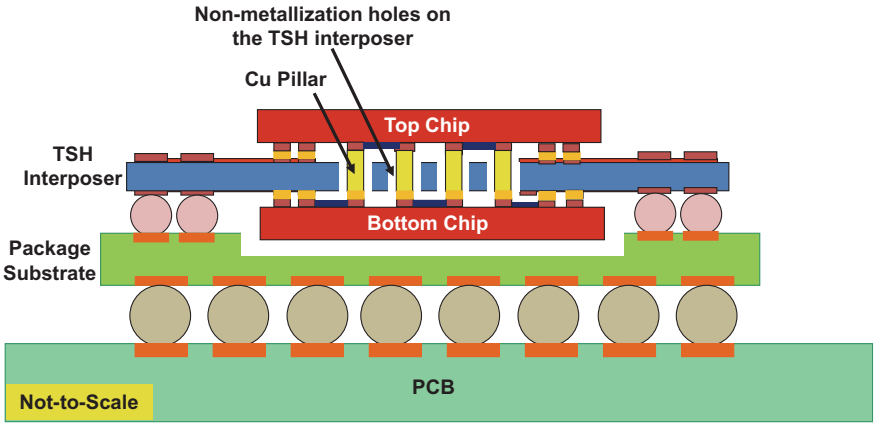


Fig. 4.16 Heterogeneous integration test vehicle which consists of a top chip with Cu pillars and a bottom chip with solder bumps on a TSH interposer (bridge)

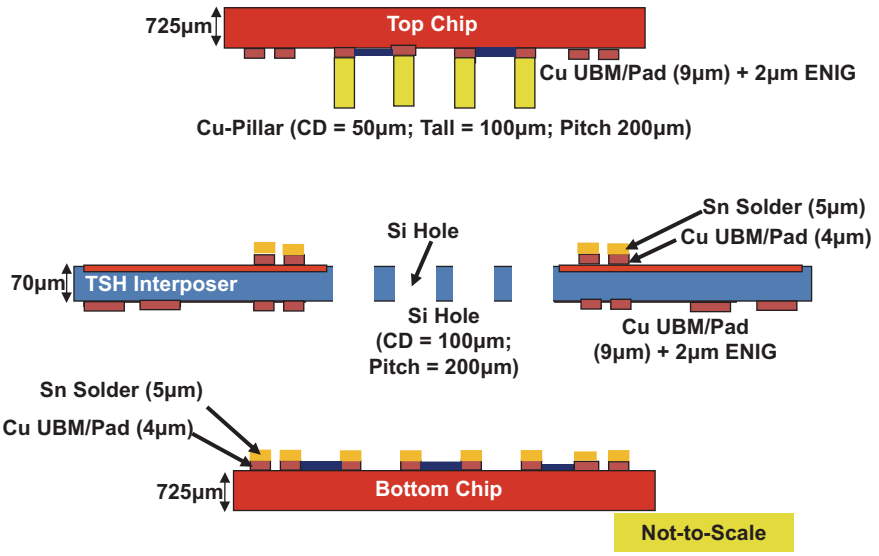


Fig. 4.17 Geometry, dimension, and interconnects of the top chip, bottom chip, and TSH interposer (bridge)

Table 4.1 Key elements of the heterogeneous integration structure and their dimensions

Top-chip with Cu-pillar	
Dimension	5 mm × 5 mm × 725 µm
Cu-pillar	CD = 50 µm; Tall = 100 µm; Pitch = 200 µm
Cu UBM/pad	9 µm + 2 µm (ENIG)
Bottom-chip without Cu-pillar	
Dimension	5 mm× 5 mm× 725 µm
Cu UBM/pad	4 µm
Sn solder	5 µm
TSH interposer	
Dimension	10 mm× 10 mm× 70 µm
TSH	CD = 100 µm; Pitch = 200 µm; Depth = 70 µm
Top-side: Cu UBM/Pad and Sn solder	4 µm (Cu) and 5 µm (Sn)
Bottom-side: Cu UBM/Pad	9 µm + 2 µm (ENIG)
Package substrate (cavity)	15 mm× 15 mm× 1.6 mm (6 mm× 6 mm× .9 mm)
PCB	132 mm× 77 mm× 1.6 mm

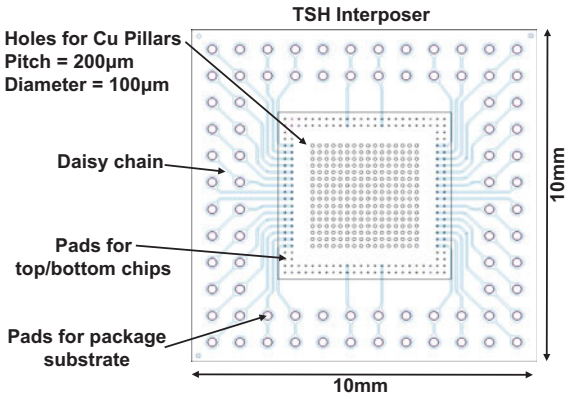


Fig. 4.18 Layout of the TSH interposer (bridge)

4.8.4 Top Chip with UBM/Pad and Cu Pillar

The process flow of fabricating the top chip with Cu-pillar is shown in Fig. 4.19. Since this is not a device chip but a piece of silicon, thus the daisy chain (RDL) will be fabricated first. SiO_2 is deposited on a Si wafer with PECVD at 200 °C. Then, (0.1 μm) Ti and (0.3 μm) Cu are sputtered. It is followed by spin coating a photoresist and patterning with a mask using a photolithography technique (align and expose). Electroplate the Cu (2 μm) RDL. Then, strip off the photoresist and etch off the TiCu. SiO_2 (0.5 μm) is deposited on top of the whole wafer with PECVD. Again, photoresist and patterning are carried out. Then, dry etch the SiO_2 by RIE (reactive ion etch). It is followed by stripping off the photoresist and now it is ready for wafer bumping.

First, sputter the seed layer: (0.1 μm) Ti and (0.3 μm) Cu. Then, photoresist (9.5 μm) and patterning of all 432 pads are carried out. It is followed by electroplating the Cu UBM/pad (9 μm). Strip off the photoresist and etch off the TiCu seed layer. Then, a positive type of photoresist (100 μm) provided by HD Microsystems is laminated hard pressed on the whole wafer and it is followed by patterning only the central 256 pads, and Cu plating (90 μm) at room temperature. Then, the top surface of the wafer is flattened by DISCO's fly cut. It is followed by stripping off the photoresist and etching off the seed layer TiCu. Finally, electroless Ni (2 μm) and immersion Au (0.05 μm). Figure 4.20 shows the SEM (scanning electron microscopy) images of the Cu pillars, Cu UBM/pads, and Cu RDLs (daisy chains) on the top chip. The smaller diameter (45 μm) on top of the Cu pillars is because of the smaller opening on top of the dry film photoresist.

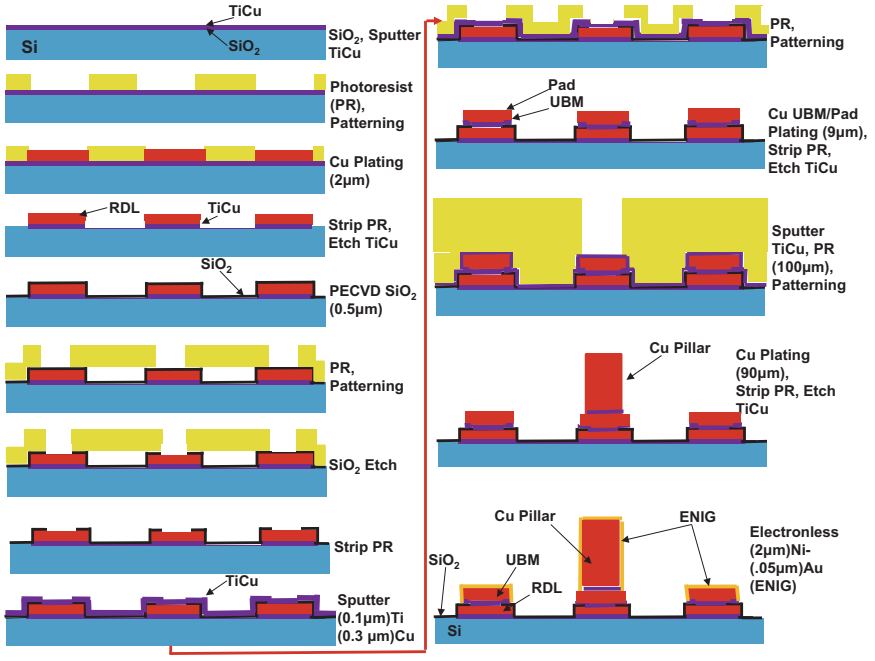


Fig. 4.19 Process flow in fabricating the top chip with RDL, Cu UBM/pad, and Cu pillars

4.8.5 Bottom Chip with UBM/Pad/Solder

The process flow in fabricating the bottom chip with UBM/pad and solder is shown in Fig. 4.21. It can be seen that the process in making the Cu RDL is the same as those of the top chip. For most of the wafer bumping processes, they are the same except the photoresist thickness and solder. After photoresist (9.5 μm) and patterning of all (432) pads, it is followed by electroplating the Cu UBM/pad (4 μm) and electroplating the Sn solder (5 μm). Strip off the photoresist and etch off the TiCu seed layer. A photo image of the RDL, Cu UBM/pad, and Sn solder cap on the bottom chip is shown in Fig. 4.21.

4.8.6 Bridge Fabrication

The process flow in fabricating the bridge with Cu UBM/pad + Sn solder on its top side and Cu UBM/pad on its bottom side is shown in Fig. 4.22. It can be seen that the RDL and Cu UBM/pad on the bottom side of the interposer will be fabricated first and the processes are basically the same as those of the top chip. Except after the strip off of the photoresist and etch off of the seed layer (TiCu) of the 9 μm-

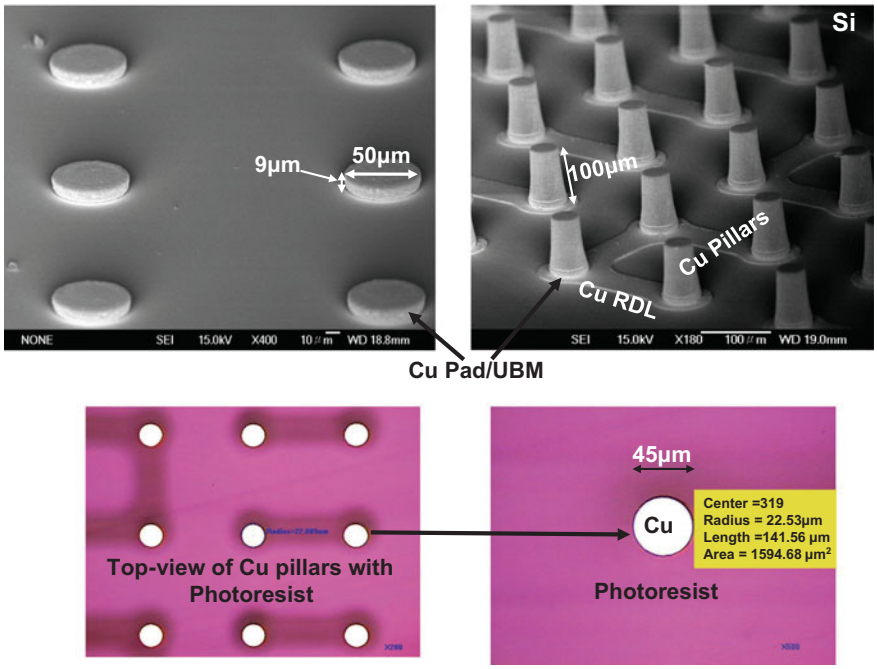


Fig. 4.20 SEM images of the Cu UBM/pads and Cu pillars on the to-chip

thick UBM/pad, it is followed by ENIG (2 μmNi–0.05 μmAu). Then, the bottom side of the bridge wafer with UBM/pad is temporarily bonded with an adhesive to a 750 μm-thick silicon supporting wafer (carrier). It is followed by thinning the top side of the dummy bridge wafer down to 70 μm. Then, repeat all the process steps in fabricating the UBM/pad + Sn solder of the bottom chip mentioned earlier. Finally, de-bond the carrier wafer from the bridge wafer at room temperature. At this stage, the bridge wafer with 176 peripheral UBM/pads + Sn solders on its top side and 176 peripheral UBM/pads at its bottom side, as shown in Figs. 4.21 and 4.22, is achieved. The 256 holes are fabricated with UV laser drilling. The power is 3400 mW. Figure 4.23 shows the photo images of the 70 μm-thick bridge wafer with RDLs, pads for the package substrate, peripheral pads for the chips, and 100 μm-diameter holes on 200 μm-pitch.

4.8.7 Final Assembly

The process flow of the final assembly of the heterogeneous integration with a bridge test vehicle is shown in Fig. 4.24. First, the top chip with the 176 peripheral UBM/pads is TC (thermocompression) bonded to the peripheral UBM/pads + Sn solders on the

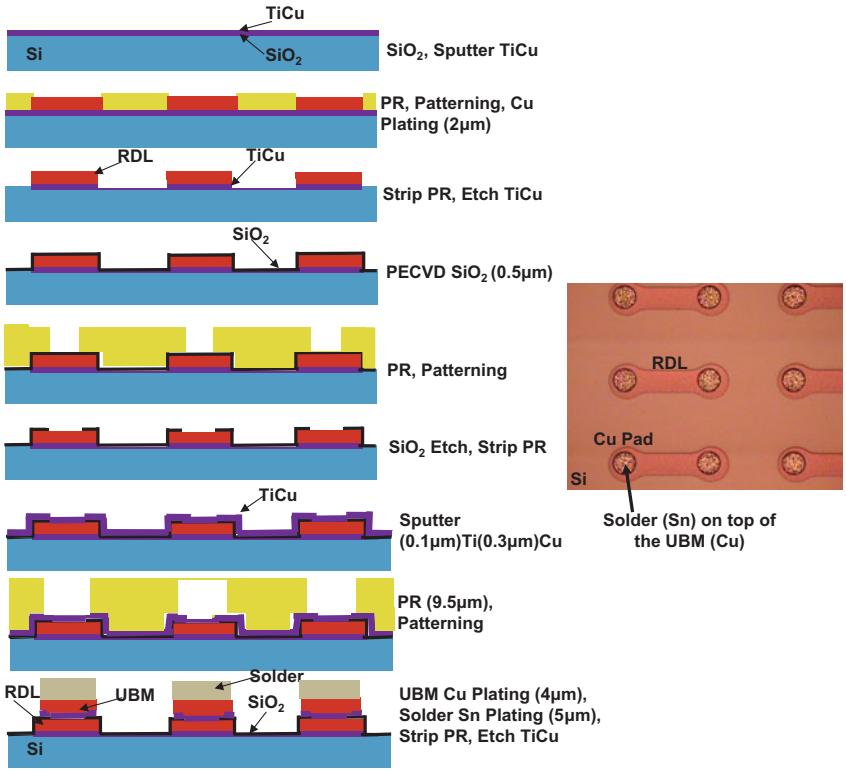


Fig. 4.21 Process flow in fabricating the bottom chip with RDL, and Cu UBM/pad + Sn solder

top side of the bridge. (The Cu pillars passed through the holes of the bridge.) The TC bonding conditions are shown in Fig. 4.25. It can be seen that (a) the maximum bonding force is 1600 g, (b) the maximum temperature of the chuck is 150 °C, (c) the maximum temperature of the head is 250 °C, and (d) the cycle time is 120 s.

Then, all the 432 UBM/pads + Sn solders on the bottom chip are TC bonded to the tip of the 256 central Cu pillars and 176 peripheral UBM/pads on the bottom side of the bridge. The bonding conditions are basically the same as those of the top chip except the bonding force is reduced to 800 g. It is followed by solder (Sn3 wt%Ag0.5 wt%Cu) bump (350 μm diameter) mounting on the bottom side of the bridge. Then, a capillary type underfill with 50% filler contents (average filler size = 0.3 μm and maximum filler size = 1 μm) is dispensed along two adjacent sides of the top chip. After the underfill (a) fills the gap between the top chip and the TSH interposer, (b) flows through the holes of the TSH interposer, and (c) fills the gap between the bottom chip and the bridge, then it is cured at 150 °C for 30 min.

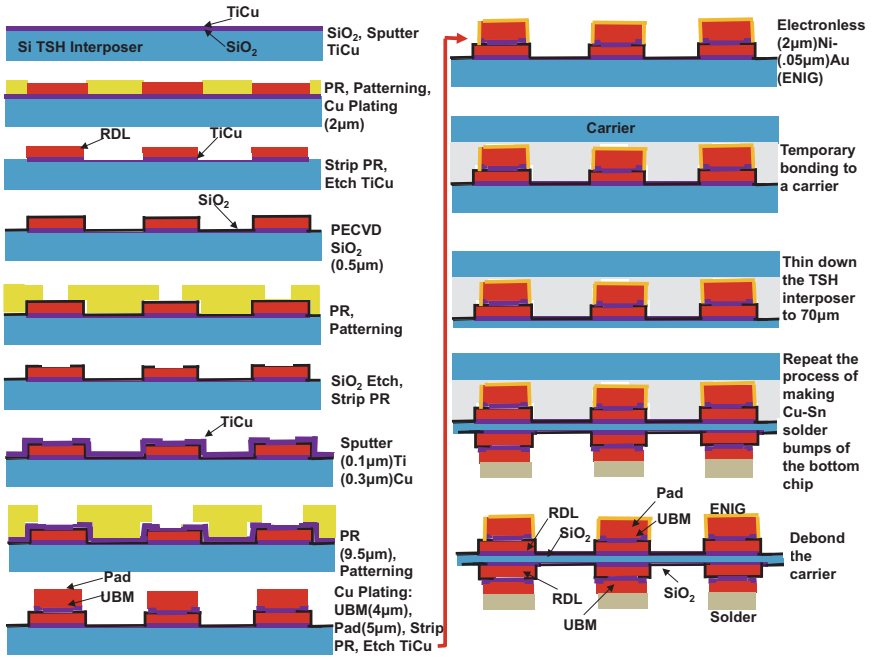


Fig. 4.22 Process flow in fabricating the TSH interposer (bridge) with Cu UBM/pad + Sn solder on its top side and Cu UBM/pad on its bottom side

The whole TSH interposer (bridge) module is solder reflowed on the package substrate by a standard lead-free temperature profile with a maximum at 240 °C. In order to enhance the solder joint reliability, the underfill is applied between the bridge and the organic package substrate. It is followed by solder (Sn3 wt%Ag0.5 wt%Cu) ball (450 μm diameter) mounting on the bottom side of the package substrate. Finally, the whole heterogeneous integration package is solder reflowed on the PCB with the same lead-free reflow temperature profile just mentioned. The final assembled heterogeneous integration test vehicle is shown in Fig. 4.26. It can be seen that the PCB is supporting the package substrate, which is supporting the bridge, which is supporting the top chip. The bottom chip is blocked by the bridge and cannot be seen.

Figure 4.27 shows the X-ray images of the final assembled heterogeneous integration. It can be seen that (a) the Cu pillars are not contacting the sidewall of the bridge, and (b) the Cu pillars are almost at the center of the bridge. Figure 4.28 shows the SEM image of a cross-section of the heterogeneous integration, which includes all the key elements such as the top chip, TSH interposer (bridge), bottom chip, package substrate, PCB, microbumps, solder bumps, solder ball, and Cu pillars. It can be seen through the X-ray and SEM images that the key elements of SiP structure are properly fabricated.

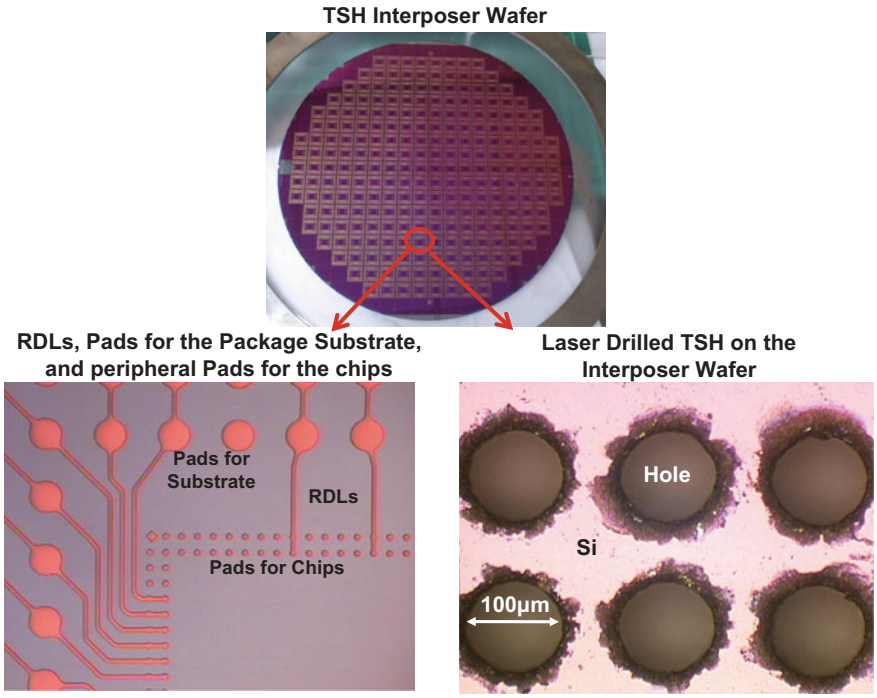


Fig. 4.23 TSH interposer (bridge) wafer with laser drilled holes (right) and RDL and pads for chip (left)

4.8.8 Reliability Assessments—Shock (Drop) Test and Result

The reliability assessments to verify the structural and thermal integrity of the assembled heterogeneous integration are drop test and thermal cycling test. The drop test board and setup are based on JESD-B111 [19]. The heterogeneous integration assembly are facing upward during the test. Four standoffs on the fixture provide the support and the spacing for deflections of the PCB during impacts as shown in Fig. 4.29. The drop height is 460 mm, which leads to the acceleration = 1500 g as shown in Fig. 4.30. After 10 drops, there is no failure, i.e., no resistances change of the daisy chains and there is no obvious failure.

4.8.9 Reliability Assessments—Thermal Cycling Test and Results

The thermal cycling test conditions are: −55 °C ↔ 125 °C, and 1 h cycle (15 min ramp up and ramp down and 15 min at dwells). Figure 4.31 shows a Weibull plot of

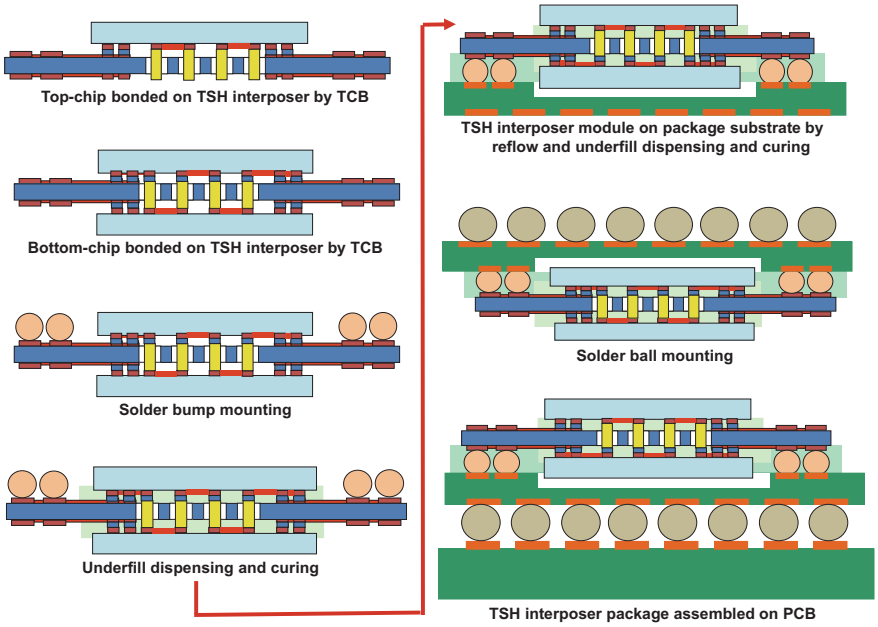


Fig. 4.24 Process flow in the final assembly of the heterogeneous integration

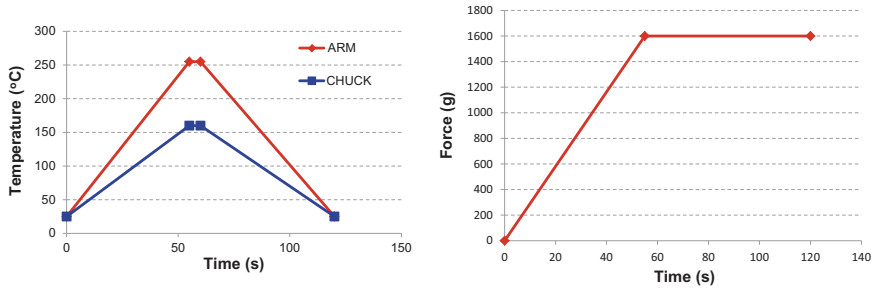


Fig. 4.25 TCB conditions in bonding the top chip to the top side of TSH interposer (bridge): temperature (left) and force (right)

the test results and it can be seen that for the median (50%) rank, the Weibull slop is 2.52, and the sample characteristic life (at 63.2% failures) is 1175 cycles. (For the given test conditions, if the characteristic life is larger than 1000 cycles, then it is considered acceptable.) The sample mean life of the daisy chained solder joints is defined as the mean time to failure (MTTF) $= 1175\Gamma(1 + 1/2.52) = 1036$ cycles, where Γ is the Grammar function. This mean life occurs at $F(1036) = 1 - \exp[-(1036/1175)2.52] = 0.52$, i.e., 52% failures.

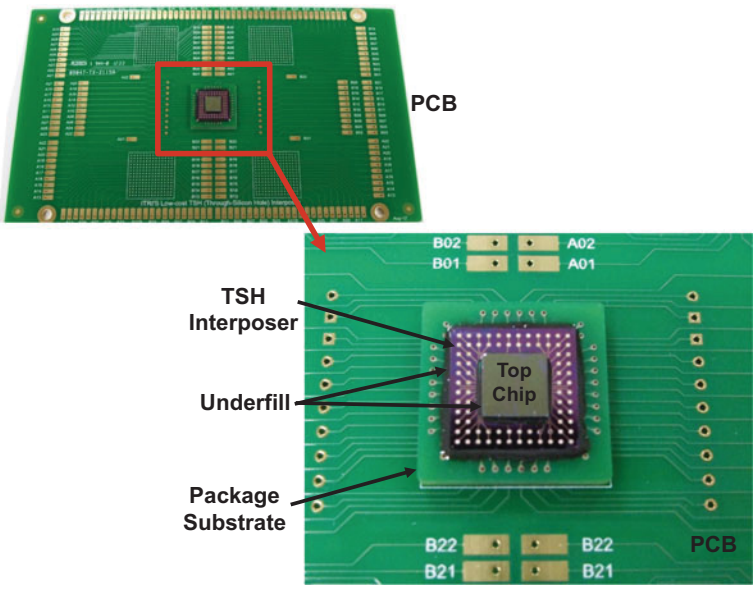


Fig. 4.26 The final assembled heterogeneous integration system

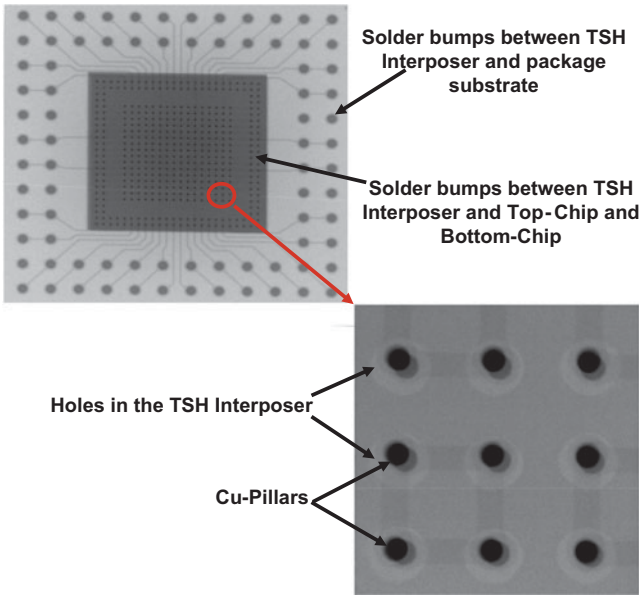


Fig. 4.27 X-ray images showing the location of Cu pillars and TSHs of the heterogeneous integration which consists of the top chip, TSH interposer (bridge), bottom chip, package substrate, and PCB

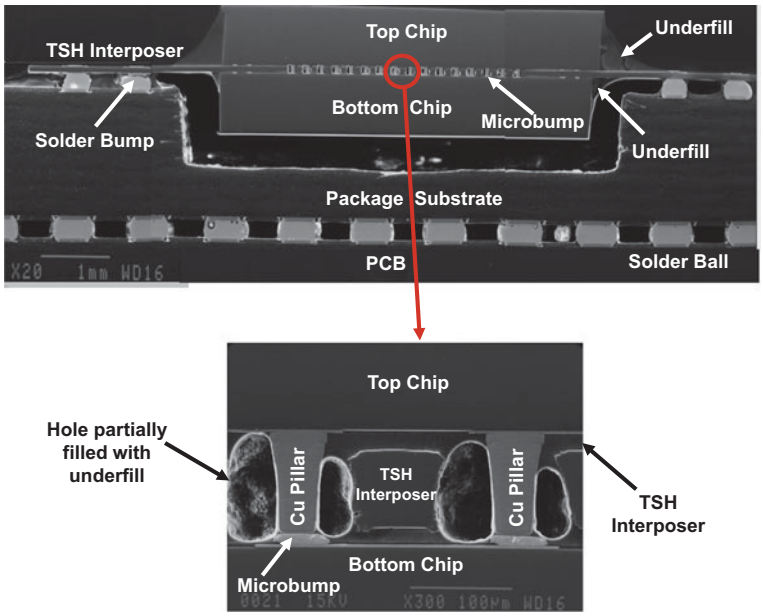


Fig. 4.28 SEM image showing a cross-section of the heterogeneous integration which consists of the top chip, TSH interposer (bridge), bottom chip, package substrate, and PCB

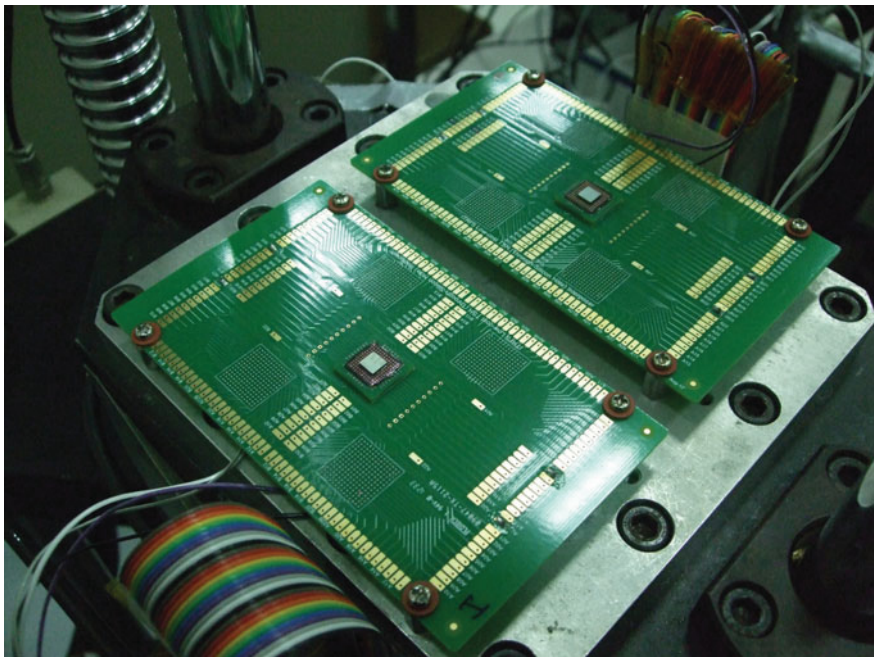


Fig. 4.29 Drop test of the heterogeneous integration system set-up

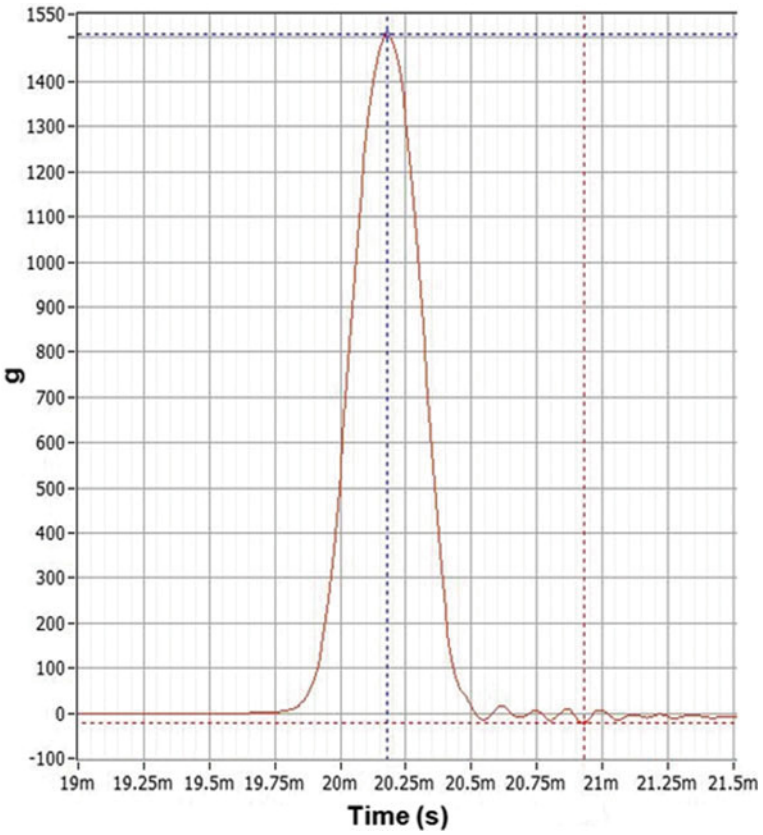


Fig. 4.30 Drop test profile according to JESD22-B111

Figure 4.31 also shows the test results at 90% confidence level, i.e., in 9 of 10 cases we would like to find out the intervals for the true Weibull slope and the true mean life of the daisy chained solder joints. It can be seen that the true mean life of the solder joints (in 90 of 100 cases, the other 10 cases, no one knows) will be no less than 843 cycles but no larger than 1524 cycles. Also, the true Weibull slope (β) falls into the intervals $2.16 \leq \beta \leq 2.88$.

One of the typical failure modes is shown in Fig. 4.32. It can be seen that there is a crack in the solder bump between the bridge and the pad of the organic package substrate. The failure (crack) location is in the solder bump near the interface between the solder and the UBM of the TSH interposer. It failed at 1764 cycles and the failure criterion is infinitive resistance changed.

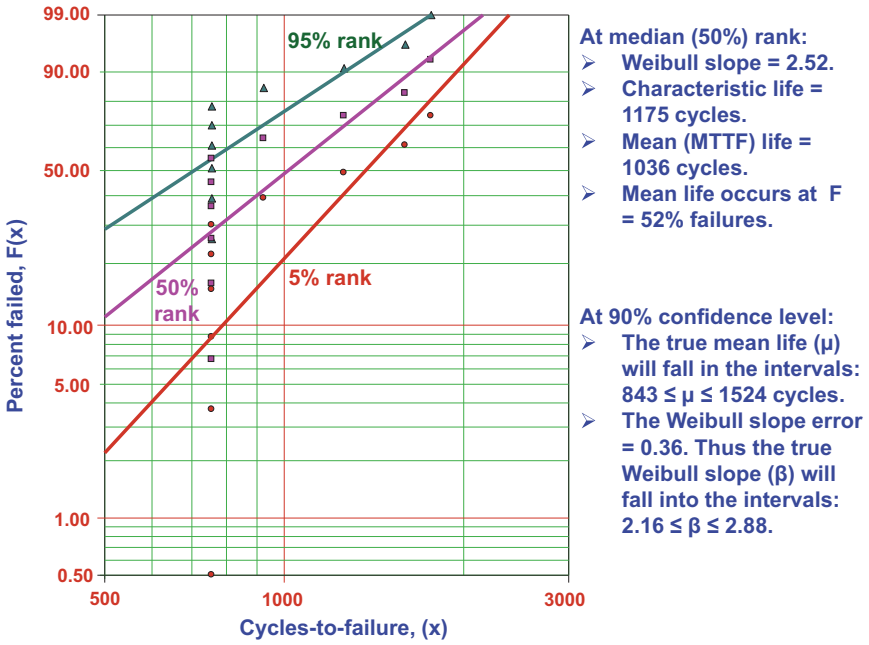


Fig. 4.31 Weibull plot of daisy-chained solder joint under thermal cycling testing, −55 °C ↔ 125 °C, and one hour cycle (15 min ramp up and ramp down and 15 min at dwells). The required confidence level was 90%

4.9 Summary and Recommendations

Some important results and recommendations are summarized as follows:

- TSV-less interposers such as bridges are very effective ways to make RDLs for heterogeneous integrations. It is not only less process step but potentially lower cost.
- The size of bridges is usually less than that of the TSV-interposers.
- The metal line width and spacing of bridges are at best equal to those of the TSV-interposers.
- The low-cost TSH interposer could be a potential candidate for heterogeneous integrations on silicon substrates (bridges). Because (a) the electrical performance of the TSH interposer (bridge) has been shown is better than that of the TSV interposer, (b) the feasibility of design, materials, and process of the TSH interposer has been demonstrated, and (c) the test vehicle passed the thermal-cycling and shock tests.

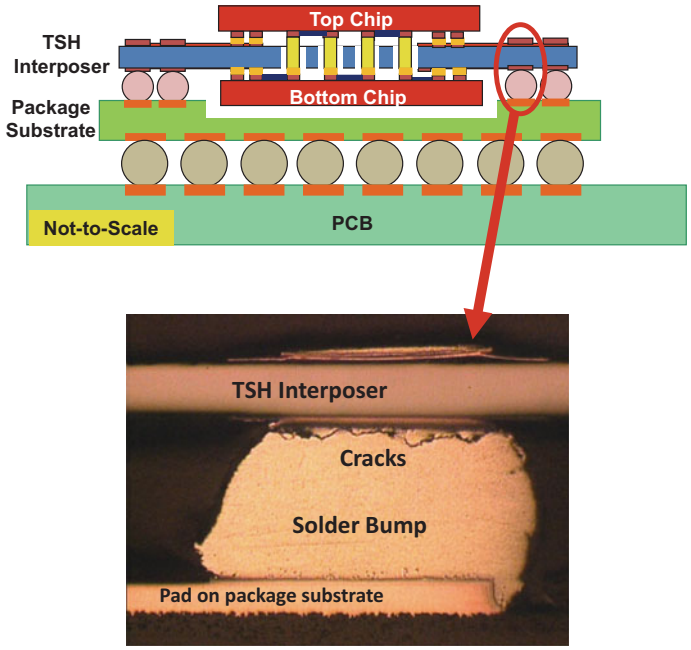


Fig. 4.32 Failure (solder joint cracking) modes due to thermal cycling test

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Chapter 5
Fan-Out Wafer/Panel-Level Packaging for Heterogeneous Integrations



5.1 Introduction

The first fan-out wafer-level packaging (FOWLP) U.S. patent was filed by Infineon on October 31, 2001 [1, 2], and the first technical papers were also published (at IEEE/ECTC2006 and IEEE/EPTC2006) by Infineon and their industry partners: Nagase et al. [3, 4]. At that time, they called it embedded wafer-level ball (eWLB) grid array. This technology eliminates wirebonding or wafer bumping and leadframe or package substrate, and potentially leads to a high throughput, lower cost, better performance, and lower profile package [2]. Alternatively, this technology requires a temporary (reconstituted) carrier for the known-good die (KGD), epoxy molding compound (EMC), compression or lamination molding, and the fabrication of the RDLs (redistribution-layers) [2].

It should be emphasized out that the concept of FOWLP was first proposed by Infineon [1]. Even though some of the knowledge of this technology has been patented by General Electric [5, 6] and EPIC [7], however, Infineon's patent [1] specifically pointed out the use of RDLs to fan-out the circuitry from the metal pad of the chip on a wafer and solder ball to the metal pads on a PCB, for example, Fig. 5.1. Infineon [1] also specifically pointed out that some of the RDLs have a portion that extends beyond (fan-out) the edges of the chip. These are the major claimed in [1], which were not claimed by GE and EPIC [2, 5–7].

The advantages of FOWLP, Fig. 5.2a, over fcPBGA (flip chip plastic ball grid array) package, Fig. 5.2b, are [2, 8]: (1) lower cost, (2) lower profile, (3) eliminating the substrate, (4) eliminating the wafer bumping, (5) eliminating the flip chip reflow, (6) eliminating the flux cleaning, (7) eliminating the underfill, (8) better electrical performance, (9) better thermal performance, and (10) easier to go for heterogeneous integration and 3D IC packaging [9–11].

The advantages of FOWLP over WLCSP (wafer-level chip scale package), Fig. 5.2c, are [2, 8]: (1) the use of known good die (KGD), (2) better wafer-level yield, (3) using the best of silicon, (4) single or multichip, (5) embedded integrated

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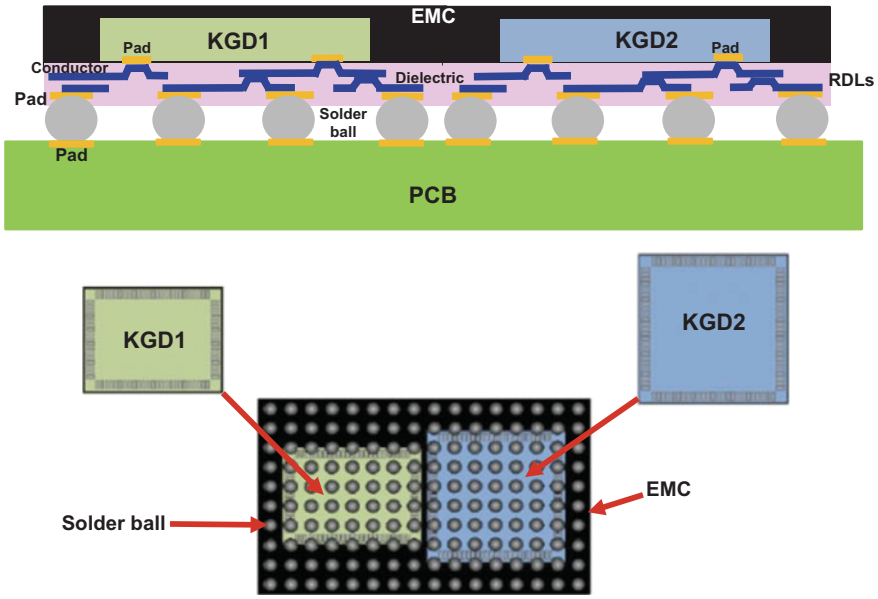


Fig. 5.1 Fan-out wafer/panel-level packaging with two chips

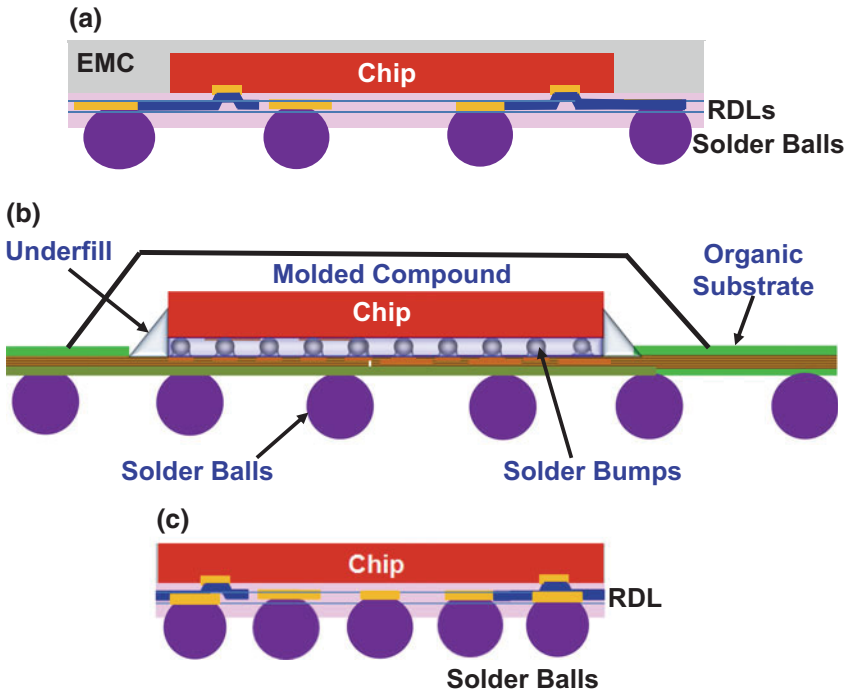


Fig. 5.2 **a** FOW/PLP. **b** fcPBGA. **c** WLCSP

passive devices, (6) more layer of RDLs, (7) higher pin counts, (8) better thermal performance, (9) easier to go for SiP and 3D IC packaging [9–11], and (10) higher PCB level reliability.

During ECTC2007, Freescale (now NXP) presented a similar technology and called it redistributed chip package [12]. IME extended the FOWLP technology to multi-die and stacked multi-die in 3-D format and presented at ECTC2008 [13]. During ECTC2009, IME presented four papers on: (1) a novel method to predict die shift during compression molding [14]; (2) laterally placed and vertically stacked thin dies [15]; (3) the reliability of 3-D FOWLP [16]; and (4) the demonstration of high quality and low-loss millimeter-wave passives on FOWLP [17]. In [1, 3, 4, 12–17], they used chip-first and die face-down [18] fan-out wafer-level processing.

During IEEE/ESTC2010 and ECTC2011, NEC (now Renesas) presented a couple of papers on system in wafer-level package (SiWLP) [19], and "RDL-first" FOWLP [20]. These papers are based on their SMAFTI (SMArt chip connection with feed through interposer) packaging technology for inter-chip wide-band data transfer [21, 22] and 3D stacked memory integrated on logic devices [23–27]. The feed through interposer (FTI) used in SMAFTI is a film with ultra-fine linewidth and spacing RDLs. The dielectric of the FTI is usually SiO_2 or a polymer, and the conductor wiring of the RDLs is Cu. The FTI not only supports the RDLs underneath within the chip, it also provides support beyond the edges of the chip. Area array solder balls are mounted at the bottom-side of the FTI, which are to be connected to the PCB. EMC is used to embed the chip and support the RDLs and solder balls. Their technology requires besides the fabrication of the RDLs, wafer bumping, fluxing, flip chip assembly, cleaning, and underfills dispensing and curing, and thus is very high-cost. Their potential applications are for very high-density and high-performance products such as super computers, high-end servers, telecommunications, and networking systems. Their technology is chip-last or RDL-first FOWLP processing [18].

At ECTC2012, Statschippac proposed a package-on-package (PoP) for the application processor (AP) chipset with the FOWLP technology [28]. TSMC [29, 30] presented two papers on FOWLP at ECTC2016: one is their integrated fan-out (InFO) wafer-level packaging for housing the most advanced AP for mobile applications [31], and the other is to compare the thermal and electrical performance between their InFO technology and the conventional flip chip on buildup package substrate technology [32]. During September 2016, TSMC put the PoP of AP of iPhones with their FOWLP (InFO) technology into high-volume manufacturing. This is very significant since this means that FOWLP is not just only for packaging for small chips such as baseband, power management IC, radio frequency (RF) switch/transceiver, RF radar, audio codec, microcontroller unit, connectivity ICs, etc., it can also be used for packaging high performance and large (>120 mm^2) system-on-chip (SoC) such as APs. TSMC used chip-first and die face-up FOWLP processing [18].

Recently, through-silicon via (TSV)-less interposer [33] to support multiple flip chips is a very hot topic in semiconductor packaging. At ECTC2013, Statschippac proposed [34] using the fan-out flip chip-eWLB to make the RDLs for the chips to perform mostly lateral communications. During ECTC2016, ASE [35] and Mediatek [36] used a similar technology to fabricate the RDLs with FOWLP and showed that

the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated, i.e., TSV-less interposers.

All pervious mentioned fan-out papers are using the round 200- or 300-mm wafers as the reconstituted carriers for supporting the KGDs and making the molds, RDLs, etc. (This is because of the existing equipment for fabricating the device wafers.) In order to increase the throughput, fan-out panel-level packaging (FOPLP) has been proposed. For examples, starting from EPTC2011, J-Devices have been presenting their FOPLP (320 mm × 320 mm) called WFOP™ (Wide Strip Fan-Out Package) [37–39]. Starting from ECTC2013, Fraunhofer have been presenting their evaluation results on compression molding of a large area (610 mm × 457 mm) FOPLP [40–42]. At ECTC2014, SPIL published two papers on FOPLP called P-FO, one is to develop and characterize a 370 mm × 470 mm [43] and the other is to measure their warpage [44]. One of the bottlenecks for FOPLP is the availability of panel equipment such as the spin coating, physical vapor deposition (PVD), patterning/photolithography, electrochemical deposition, etching, backgrinding, solder ball mounting, and dicing for making the molds, RDLs, packages, etc., due to the lack of the standard of panel sizes. Thus, the potential FOPLP users are unanimously calling for the panel-size industry standards.

In this chapter, the following important topics of FOW/PLP for heterogeneous integrations will be examined, discussed and update: (A) the package formations such as (a) chip first and die face-down, (b) chip first and die face-up, and (c) chip last or RDL-first; (B) the RDL fabrications such as **a** organic RDLs, (b) inorganic RDLs, (c) hybrid RDLs, and (d) LDI/PCB RDLs; (C) warpage; (D) thermal performance; (E) the temporary wafer versus panel carriers; and (F) the reliability of the fan-out packages on PCB subjected to thermal cycling.

5.2 FOW/PLP Formations

There are many FOW/PLP formations. However, basically there are three different kinds, namely chip-first (die face-down), chip-first (die face-up), and chip-last or RDL-first.

5.3 Chip-First (Die Face-Down)

FOW/PLP with the chip-first and die face-down processing is actually the eWLB first proposed by Infineon [1, 2] and high-volume manufacturing (HVM) by such as STATSChipPac, ASE, STMicroelectronics, Infineon, Intel, and NANIUM (now AMKOR). This is the most conventional method to form FOW/PLPs, and most FOW/PLP products being manufacturing today are using this method.

5.3.1 Chip-First (Die Face-Down) Process

Figure 5.3 shows, in general, the process flow of chip-first with die face-down FOW/PLP [3, 4, 12–18, 45–73]. First, the device wafer is tested for known-good dies (KGDs) and then singulated into individual dies. This is followed by picking up the KGDs and placing them face-down on a temporary carrier (which can be metal, silicon, glass, or organic) that can be round (wafer) or rectangular (panel), Fig. 5.3b, with a double-sided thermal release tape, Fig. 5.3a. (The most common used tape is the REVALPHA, Fig. 5.4, provided by Nitto Denko) Then, the reconstituted (temporary) carrier with the KGDs are molded with EMC, Fig. 5.3c, using the compression method (Fig. 5.5) + PMC (post mold cure) or the lamination method + post annealing before removing the carrier and the peeling off the double-sided tape, Fig. 5.3d. (The most common used EMC is the liquid-like material R4507 by Nagase, Table 5.1). After EMC, next comes building the RDLs (which will be detailed in Sect. 5.6) for signals, power, and grounds from the Al or Cu pads of the KGD, Fig. 5.3e. Finally, solder balls are mounted and the whole reconstituted carrier (with KGDs, RDLs, and solder balls) is diced into individual packages, Fig. 5.3f.

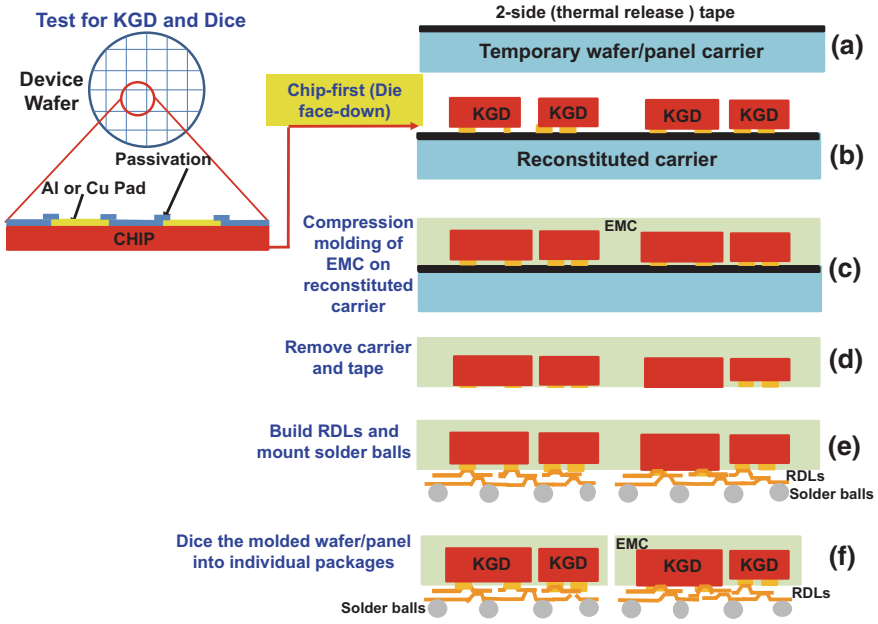


Fig. 5.3 Key process steps for chip-first and die face-down FOWLP

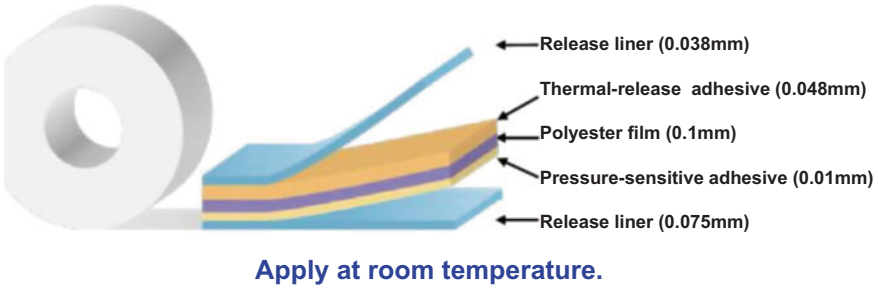


Fig. 5.4 Nitto Denko REVALPHA two-side tape

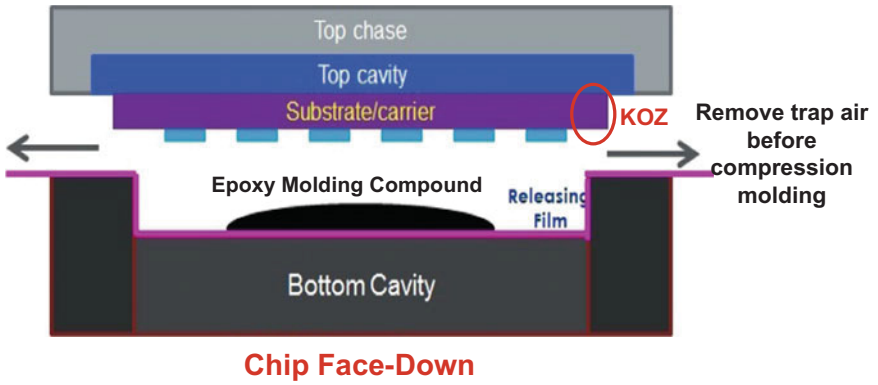


Fig. 5.5 Keep-out-zone compression molding

5.3.2 *Chip-First (Die Face-Down) with Wafer Carrier*

The chips under consideration are shown in Fig. 5.6a, b, respectively, for the large test chip (5 mm × 5 mm × 150 μm) and the small chip (3 mm × 3 mm × 150 μm). There are 160 pads with a pitch = 100 μm (the inner rows) for the large chip and 80 pads with a 100-μm pitch (the inner rows) for the small chip. For both chips, the SiO_2 passivation opening of the Al-pad is 50 μm × 50 μm, and the size of the Al-pad is 70 μm × 70 μm, Fig. 5.6c.

The 10 mm × 10 mm package under consideration is shown in Fig. 5.7a, which consists of one 5 mm × 5 mm chip, three 3 mm × 3 mm chips, and 4 (0402) capacitors. The spacing between the large chip and the small chip is only 100 μm. One practical application of the package is for the application processor chipset, i.e., the large chip could be a processor and the small chips could be memories.

Figure 5.7b schematically shows the cross-sectional view of the test package. It can be seen that there are two RDLs and the thickness of the metal layer of RDL1 is 3 μm and that of RDL2 is 7.5 μm. The linewidth and spacing of RDL1 are 10 μm and those of RDL2 are 15 μm. The dielectric layer thickness of DL1 and DL2 is

Table 5.1 Material properties of EMC (Nagase R4507)

Item	R4507
Filler content (%)	85
Filler to cut (μm)	25
Filler average size (μm)	8
Specific gravity	1.96
Viscosity (Pa.s)	250
Flexural Modulus (GPa)	19
Tg (DMA) (°C)	150
CTE1 (ppm/K)	10
CTE2 (ppm/K)	41

- High flowability as suitable for large surface areas and thin film molds
- Liquid at room temperature and able to be dispensed, and dust-free as suitable for clean room environments
- Capable of low temperature form molding (125 °C)
- Delivers low reflection in large surface area molds with low stress design
- High reliability
- High purity

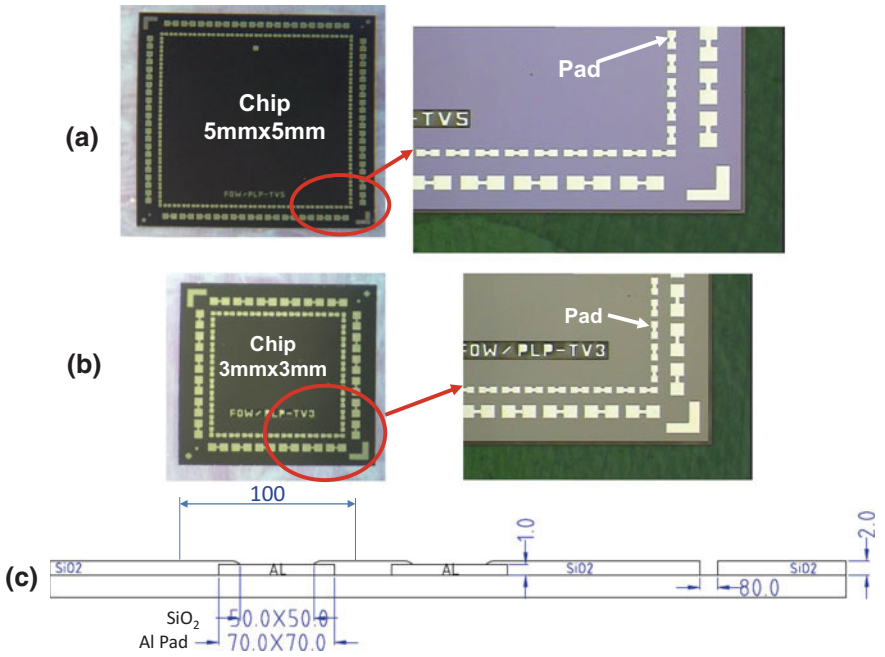


Fig. 5.6 Test chips for FOWLP. **a** 5 mm × 5 mm chip. **b** 3 mm × 3 mm chip. **c** Cross-section of the test chips

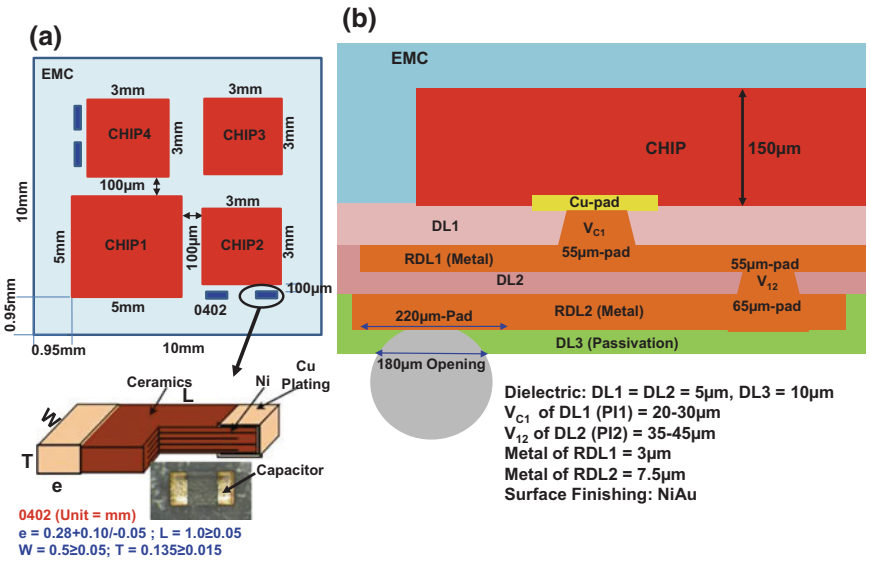


Fig. 5.7 Test package for FOWLP. **a** Top-view of the FOWLP (one 5 mm × 5 mm chip, three 3 mm × 3 mm chips, and four 0402 capacitors). **b** Cross-section view of the FOWLP (two RDLs)

5 μm, and DL3 is 10 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm, and the ball pitch is 0.4 mm.

Figure 5.8 shows a 300 mm reconstituted wafer carrier with 629 (10 mm × 10 mm) packages [45–47]. Each package has 4 (one 5 mm × 5 mm and three 3 mm × 3 mm) chips and 4 (0402) capacitors. The spacing between the large chip and the small chip is 100 μm. There are two RDLs for each package. It should be emphasized that FOWLP is a very high-throughput process. In this case, one shot, it can produce 629 10 mm × 10 mm heterogeneous integration packages.

5.3.3 Chip-First (Die Face-Down) with Panel Carrier

Figure 5.9 shows a special process flow of chip-first with die face-down with a panel carrier [48–50]. Since the panel carrier involves the PCB process, thus work must be done on the device wafer by electroplating an 8 μm Cu-pad on top of the Al-pad, the left-hand side of Fig. 5.9. (The purpose of the Cu-pad is to stop the laser drilling to the Al-pad.) Also, unlike those processes shown in Fig. 5.3, this process uses an organic carrier, Fig. 5.9a, pick and place the KDGs face-down on the carrier, Fig. 5.9b, and then EMC lamination or compression molding, Fig. 5.9c, and forms an ECM-panel. (In this section, the EMC with the KGDs embedded is called ECM-panel.) It is followed by attaching the ECM-panels on both sides of a core substrate with epoxy resin, Fig. 5.9d. Then, perform the 5-layer PCB lamination. It is followed

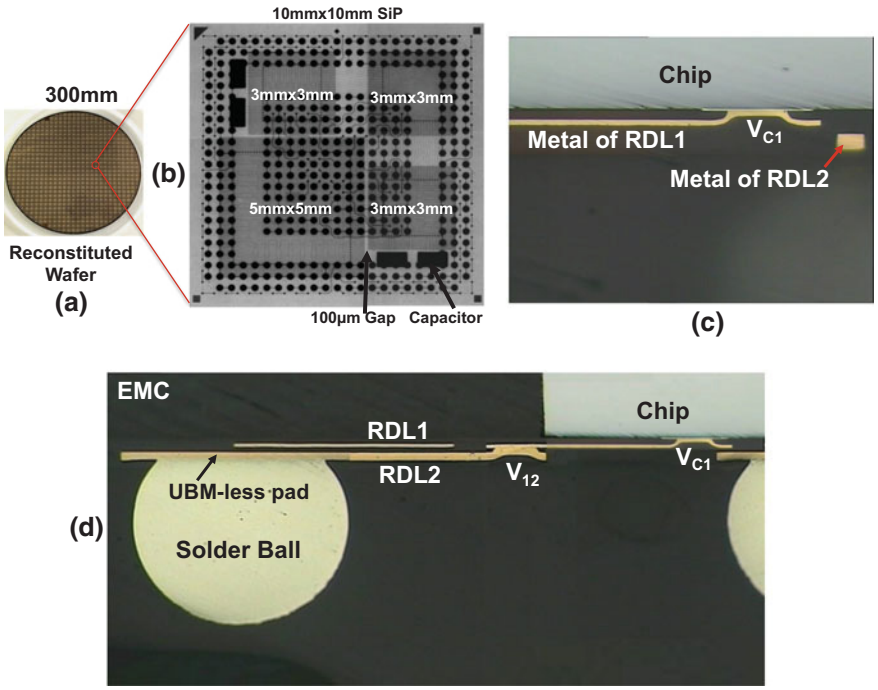


Fig. 5.8 FOWLP. **a** The 300 mm reconstituted wafer. **b** X-ray image of the test package (one 5 mm × 5 mm chip, three 3 mm × 3 mm chips, and four 0402 capacitors). **c** Cross-section of the package. **d** Cross-section of the package with solder balls

by removing the carrier and peeling off the two-sided tapes, Fig. 5.9e, and making the RDLs, which will be discussed in Sect. 5.6.

The 10 mm × 10 mm test package on the panel carrier also consists of 4 chips as shown in Figs. 5.10 and 5.11. The chip sizes are also 5 mm × 5 mm and 3 mm × 3 mm. However, there are 88 pads on a pitch = 180 μm (the outer rows) for the large chip and 48 pads on a 180 μm-pitch (the outer rows) for the small chip. The SiO_2 passivation opening of the Al-pad is 110 μm × 110 μm, and the size of the Al-pad is 130 μm × 130 μm. The Cu contact-pad is 110 μm in diameter and is 8 μm tall from the Al-pad. Figure 5.11b schematically shows the cross-sectional view of the test package. It can be seen that there are two RDLs and the thickness of the metal layer of RDL1 and RDL2 is 10 μm. The linewidth and spacing of RDL1 are 20 μm and those of RDL2 are 25 μm. The dielectric layer thickness of DL1, DL2, and DL3 is 20 μm. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm, and the ball pitch is 0.4 mm.

Figure 5.12 shows a panel carrier of 340 mm × 340 mm with 378 (10 mm × 10 mm) heterogeneous integration packages [48, 49]. Figure 5.13 shows a panel carrier of 508 mm × 508 mm with 1512 (10 mm × 10 mm) heterogeneous integration packages [50]. It can be seen that there is not any void (inspected by the C-mode

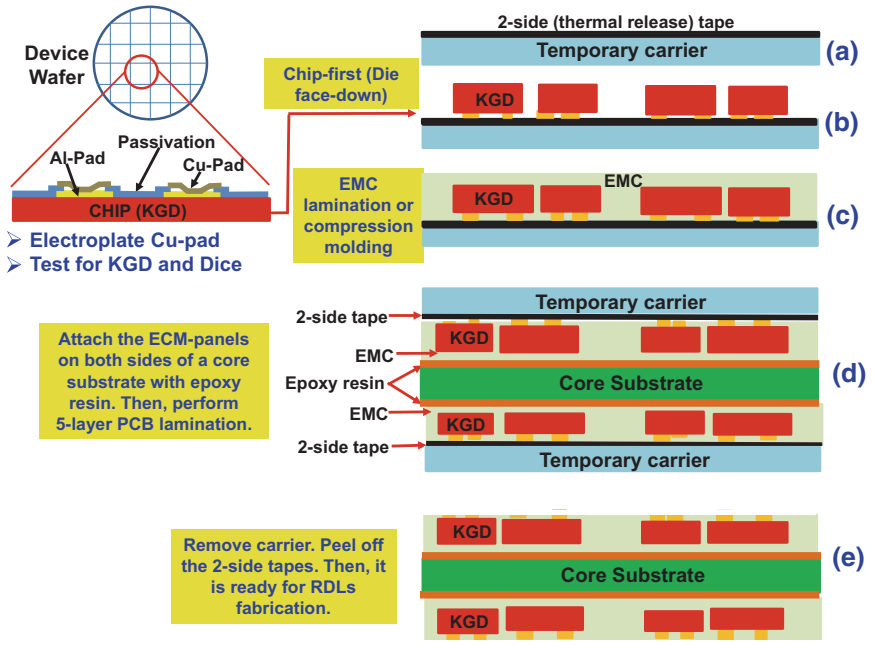


Fig. 5.9 Key process steps for chip-first and die face-down FOPLP

scanning acoustic microscopy) in the EMC even in the 100 μm gap between the large chip and the small chip.

5.3.4 Thermal Cycling of the Chip-First (Die Face-Down) Package Assembly

The package shown in Figs. 5.8, 5.12, and 5.13 is assembled on a 6-layer PCB with 405 (Sn3 wt%Ag0.5 wt%Cu) solder joints [47]. The sample sizes for the thermal-cycling test is equal to 60. The thermal cycling test results of the solder joint (without underfill) reliability are shown in Fig. 5.14. The thermal cycling test stops at 1300 cycles. It can be seen that the characteristic life (63.2% failed) of the Weibull plot is 1070 cycles which is more than adequate for the expecting life (usually is less than 3 years) of mobile products such as the smartphones and tablets. The failure mode and location are shown in Fig. 5.15. It can be seen that the solder joint cracks near the interface between the bulk solder and the package contact pad and it occurs under the chips' corners near the package corners—the longest DNP (distance to neutral point) [74].

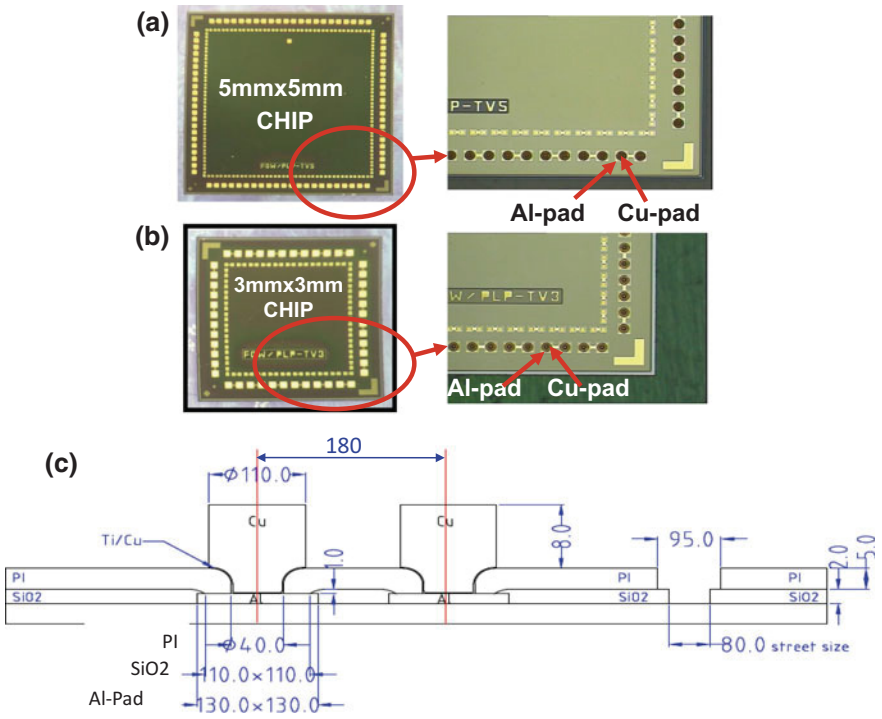


Fig. 5.10 Test chips for FOPLP. **a** 5 mm × 5 mm chip. **b** 3 mm × 3 mm chip. **c** Cross-section of the test chips

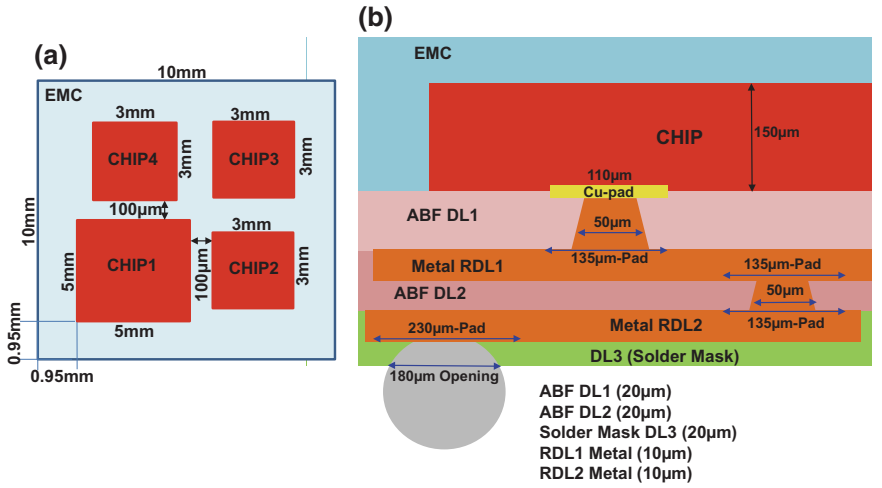


Fig. 5.11 Test package for FOPLP. **a** Top-view of the FOPLP (one 5 mm × 5 mm chip and three 3 mm × 3 mm chips). **b** Cross-section view of the FOPLP (two RDLs)

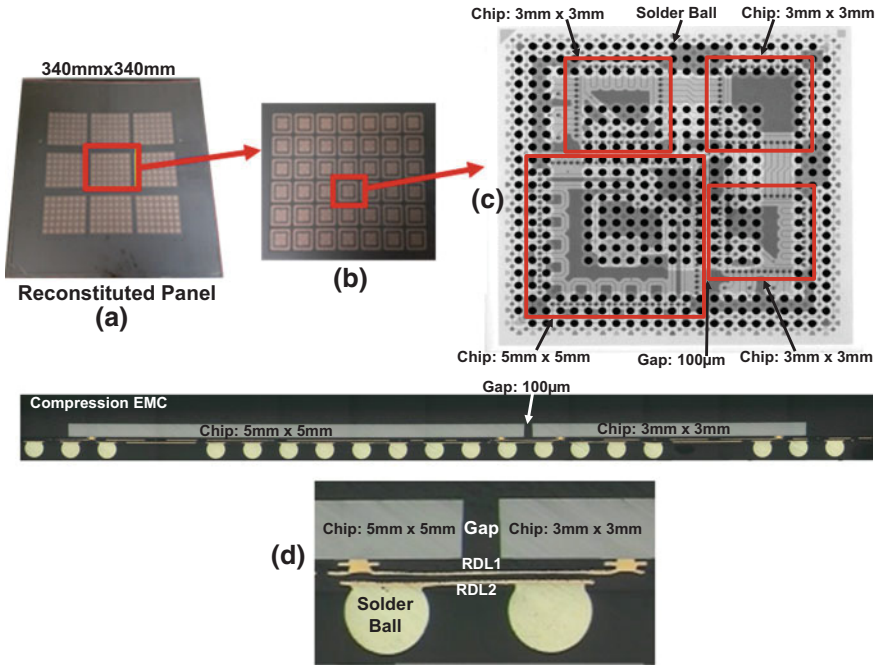


Fig. 5.12 FOPLP. **a** The 340 mm × 340 mm reconstituted panel. **b** Enlarge-view of the panel. **c** X-ray image of the test package (one 5 mm × 5 mm chip and three 3 mm × 3 mm chips). **d** Cross-section of the package showing the compression molded EMC, the 100 μm-gap, the two RDLs, and the solder balls

The PCB assembly of the fan-out SiP shown in Figs. 5.8, 5.12, and 5.13 is modeled as a 3D strip that captures the construction along a diagonal path from the assembly (Fig. 5.16) with the proper boundary conditions. Using exclusively hexahedral solid elements, the model can capture the precise shape of the packages' solder joint and potential DNP effects while retaining significant computational efficiency over full octant models. Despite the overall economy of elements in the strip model, selective mesh refinement is used to concentrate highly refined elements in the solder joints where failure is anticipated. In the present PCB assembly, failure would be predicted in the solder joints with the greatest DNP (the package corner) and near the chip corners as shown in Fig. 5.16. Thus, highly refined meshes are applied to these solder joints. The other solder joints are coarsely meshed. The ABAQUS 6.12 (C3D8R) is used for the model. The Sn3 wt%Ag0.5 wt%Cu is assumed to follow the generalized Garofalo creep equation [9]: $d\varepsilon/dt = 500{,}000\ \mathrm{Sinh}^5\ (\sigma/1 \times 10^8)\exp(-5807/T(K))$, where ε is the strain, σ is the stress in Pa, and T is the temperature in Kevin. The other material properties are shown in Table 5.2.

The temperature profile shown in Fig. 5.14 is to be imposed on the PCB assembly. Five temperature cycles are executed. The largest accumulated creep strain occurs at the solder joint under the 3 mm × 3 mm chip corner and the 5 mm × 5 mm chip

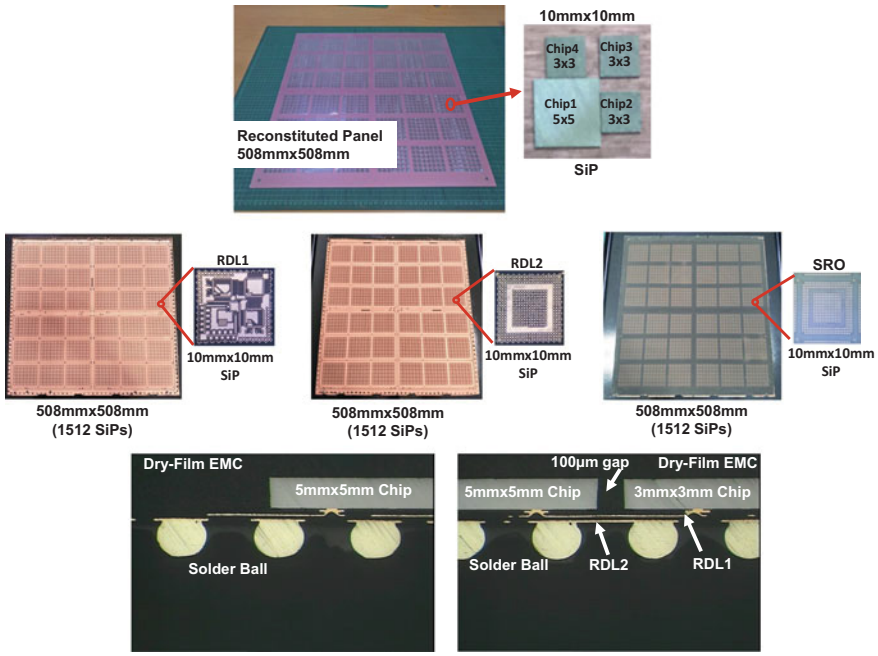


Fig. 5.13 FOPLP. (Top) The 508 mm × 508 mm reconstituted panel. (Middle) The reconstituted panel with RDL1, RDL2, and solder mask opening. (Bottom) Cross-section of the package showing the lamination dry-film EMC, the 100 µm-gap, the two RDLs, and the solder balls

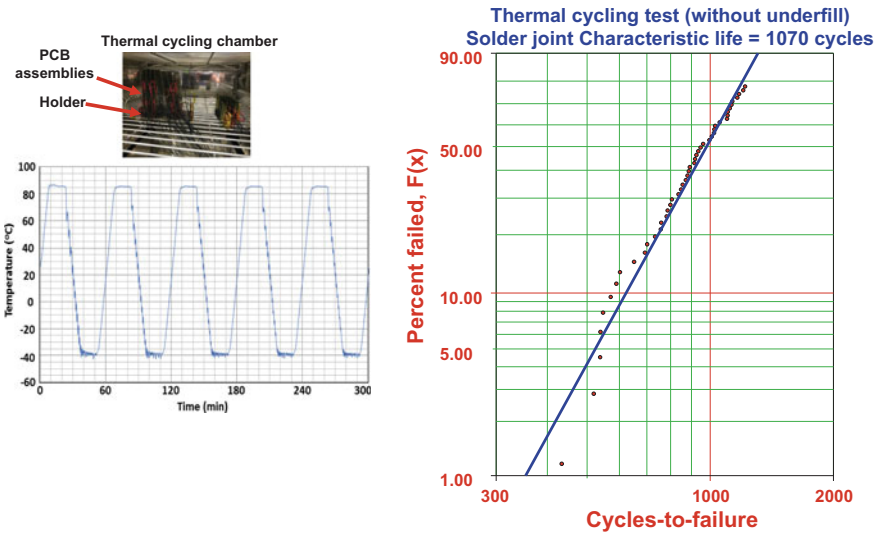


Fig. 5.14 Thermal cycling test set up, temperature cycling profile, and Weibull life distribution of the FOWLP

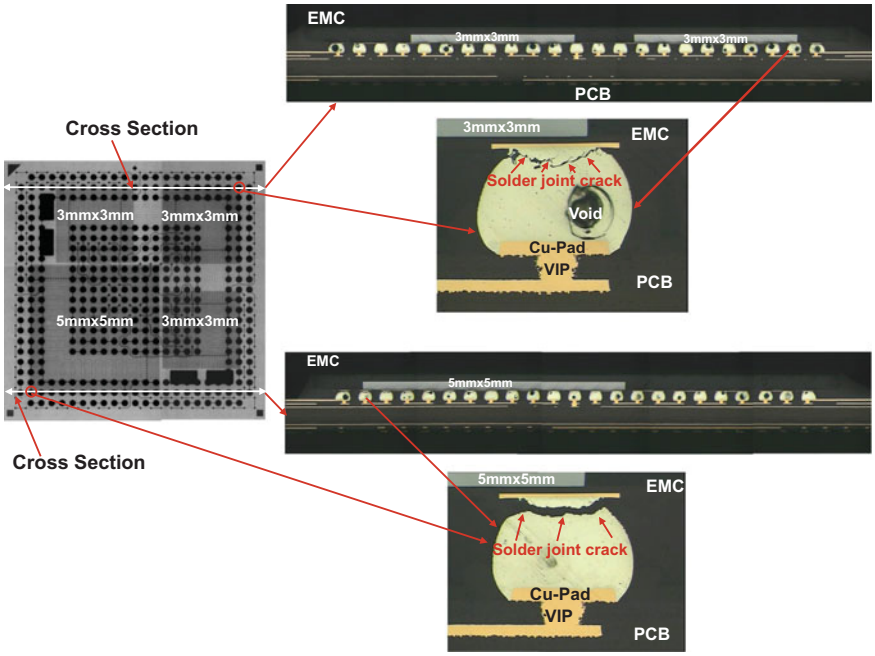


Fig. 5.15 Thermal cycling test failure location and failure mode

corner as shown in Fig. 5.16. The location is at the interface between the bottom of the package and the bulk solder. Thus, any failure should occur at this location. This correlates very well with the thermal cycling test failure mode and location as shown in Fig. 5.15. For drop test and simulation results, please read [47].

5.3.5 Applications of Chip-First and Die Face-Down FOW/PLP

Most of the applications of chip-first and die face-down are for small dies and not so high pin-counts. Also, the metal line width and spacing of the RDLs are not small, e.g., 10 to 15 μm or larger. The semiconductors to be packaged are, e.g., baseband, power management IC, radio frequency (RF) switch/transceiver, RF radar, audio codec, microcontroller unit, and connectivity ICs. With the popularity of SiP or heterogeneous integration, fan-out (which can handle multiple dies and discrete components) will be used more because the fan-in WLCSP [75] can only handle single die.

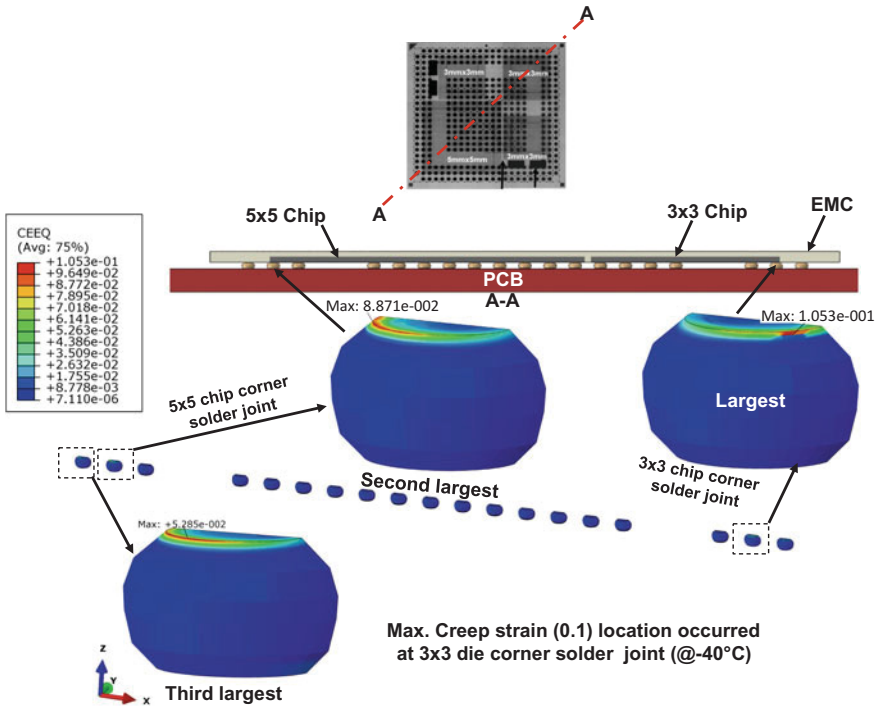


Fig. 5.16 Temperature and time dependent simulation results—cumulated creep

Table 5.2 Material properties for thermal cycling analysis

	CTE (ppm/°C)	Young's modulus (Gpa)	Poisson's ratio
Copper	16.3	121	0.34
PCB	$\alpha_1 = 18, \alpha_2 = 18, \alpha_3 = 70$	$E_1 = 22, E_2 = 22, E_3 = 10$	0.28
Silicon	2.8	131	0.278
Solder	$21.3 + 0.017T$	$49 - 0.07T$	0.3
Polyimide	35	3.3	0.3
EMC	10(<150 °C)	19	0.25

5.4 Chip-First (Die Face-Up)

Figure 5.17 shows schematically the FOW/PLP with chip-first and die face-up assembly process [18, 29–32, 76–87]. Unlike chip-first and die face-down (Figs. 5.3 and 5.11), basically, works must be done on the device wafer, Fig. 5.17a, b, and the reconstituted wafer, Fig. 5.17c–h.

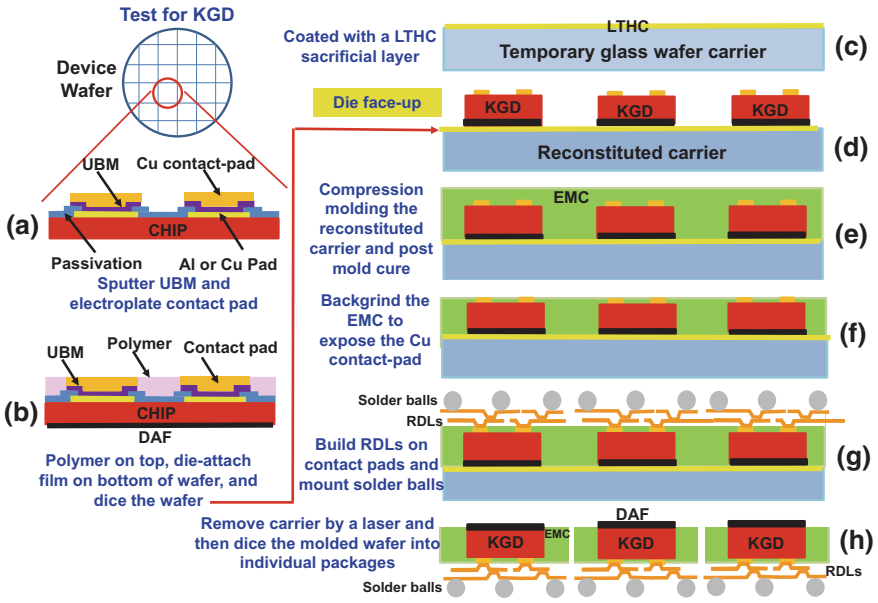


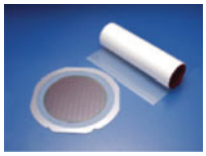
Fig. 5.17 Key process steps for chip-first and die face-up FOWLP

5.4.1 Chip-First (Die Face-Up) Process

First, the device wafer must be modified by sputtering a Ti/Cu as a bottom layer of under bump metallurgy (UBM) with a physical vapor deposition (PVD) on the Al (or Cu) pad, and a Cu contact-pad is electroplated on the UBM, as shown in Fig. 5.17a. (This is unique for chip-first and die face-up and these Cu-contact pads are for building the RDLs later.) This step is followed by spin coating a polymer on top of the device wafer and laminating (at ~ 70 °C) with a (~20 μm) die-attach film (DAF) provided by, e.g., Hitachi (Fig. 5.18) at the bottom of the device wafer as shown in Fig. 5.17b. The device wafer is then tested and diced into individual KGDs. In this section, the chip size is 10 mm × 10 mm (Fig. 5.19) and the package size is 13.42 mm × 13.42 mm (Fig. 5.20).

On the reconstituted glass carrier, a light-to-heat conversion (LTHC) layer (about 1 μm) provided by, e.g., 3 M (Fig. 5.21) is spin-coated onto the glass carrier as shown in Fig. 5.17c. The individual KGDs are picked and placed face-up on the LTHC carrier as shown in Fig. 5.17d. In order to cure the DAF, a bonder with temperature and pressure should be used. The DAF process is carried out at 120 °C (both bond-head and bond-stage) with the bond force of 2 kg for 2 s. Thus, the reconstituted carrier will expand during chips pick and place. However, during patterning/photolithography of the RDLs, it is operated at room temperature. Thus, pitch compensation due to the DAF heating is needed [76–78].

Item			Unit	FH-9011	Test method
Adhesive Thickness			μm	10, 20, 25, 40	–
DC tape properties	Exposure doze		mJ/cm²	150~400	–
	Adhesive strength between DCT and DBF	Before UV	N/25mm	1.4	–
		After UV	N/25mm	<0.1	–
Wafer laminating temp.			°C	60~80	–
Die bonding condition	Temp.		°C	100~160	–
	Load		MPa	0.05~2.0	–
Elastic modulus (35°C)			MPa	200	DMA
Tg			°C	180	TMA
Die shear strength (260°C)			N/chip	>100	5x5mm chip



Wafer backside lamination: 60 - 70°C

Curing: 125°C for one hour

Fig. 5.18 Hitachi FH-9011 die-attach-film

The EMC used in this study [76–78] is a liquid-like material (Nagase R4507). After EMC dispensing, it is followed by the compression molding. After a few experiments, the optimal compression molding parameters are: temperature = 125 °C, pressure = 45 kg/cm^2, time = 10 min and removing trap air before compression molding. It is followed by PMC with a temperature = 150 °C, time ≥ 60 min, and a dead weight = 15 kg for a better warpage control. Because of the DAF, the die shift due to compression molding is very small (≤±4 μm) [76–78].

The process in fabricating the RDLs will be discussed in Sect. 5.6. The thickness of dielectric-layer 1 (DL1), DL2, and DL3 is 5 μm, and that of DL4 is 10 μm (Fig. 5.20). The thickness of the metal of redistribute-layer 1 (RDL1) and RDL2 is 3 μm, and that of RDL3 is 7.5 μm. (The thicker metal of RDL3 is for the UBM-less thicker Cu-pads to "resist" the Cu consumption from the solder ball reflow and during operation.) The line width and spacing of the RDLs are 5 μm for RDL1, 10 μm for RDL2, and 15 μm for RDL3. The RDLs are shown in Fig. 5.22d. Overall, it can be seen that all the RDLs are properly done.

There are two different stencils for the solder ball mounting: one is for stencil printing the flux, and the other is for stencil mounting the solder balls. The solder (Sn3 wt%Ag0.5 wt%Cu) balls (200 μm diameter) used are from Indium. The peak temperature for solder reflow is 245 °C. Figure 5.22b shows the individual package, and Fig. 5.22c shows the close-up view of solder balls on the package.

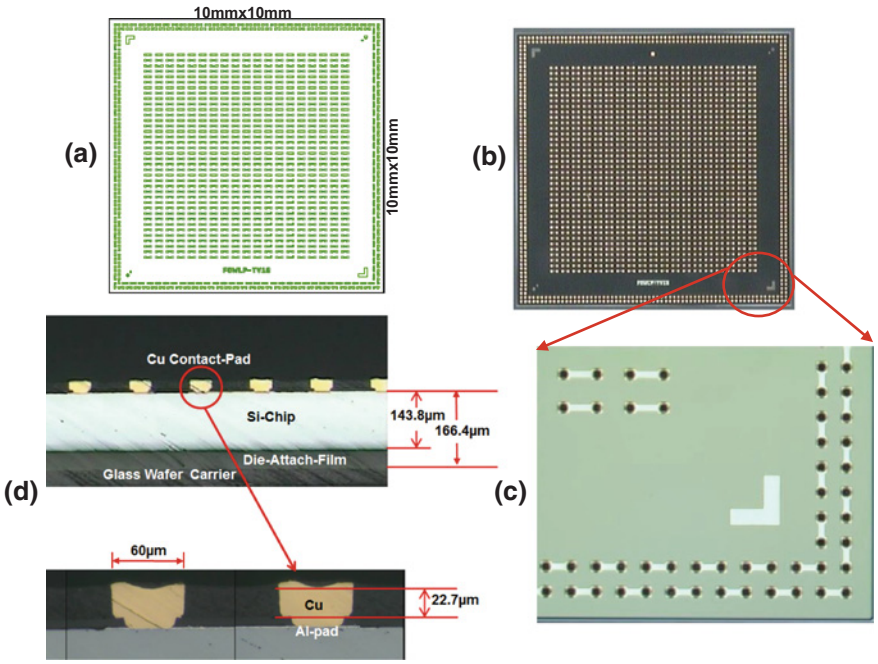


Fig. 5.19 Test chip for FOWLP. **a** 10 mm × 10 mm chip. **b** Fabricated chip. **c** Enlarge portion of the fabricated chip. **d** Cross-section of the fabricated chip

The debonding of the glass carrier as shown in Fig. 5.17h is by scanning a laser (355-nm DPSS Nd: YAG UV laser source is used) from the glass carrier side. The laser spot-size is 240 μm, the scanning speed is 500 mm/s, and the scanning pitch is 100 μm. When the LTHC layer "sees" the laser light, it converts into powders, and the glass carrier is easily removed. It is followed by chemical cleaning.

5.4.2 Thermal Cycling of Chip-First (Die Face-Up) Package

The thermal cycling test setup, data acquisition system, and temperature profile are exactly the same as those shown in the left-hand side of Fig. 5.14. The sample size is also 60. The thermal cycling test stops at 1100 cycles and there are 14 failures (including one early failed at 58 cycles.) It can be seen that the characteristic life (63.2% failed) of the Weibull plot is 2382 cycles which is more than adequate for the expecting life (usually is less than 3 years) of mobile product such as the smartphones and tablets [87]. The failure mode is shown in the right-hand side of Fig. 5.23. It can be seen that the solder joint cracks at the interface between the bulk solder and the RDL3 and it occurs near the package corners.

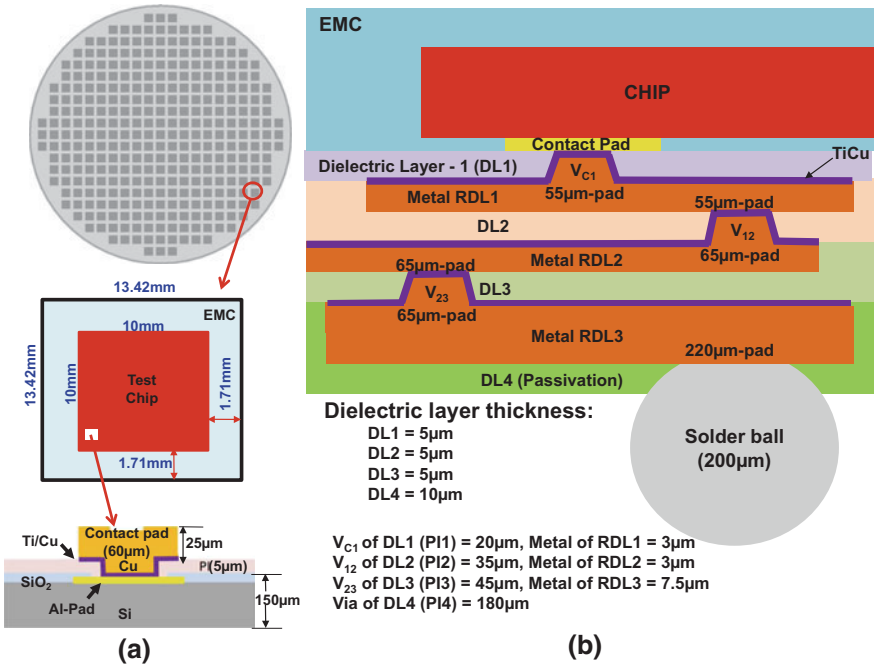


Fig. 5.20 Test package. **a** Top-view of the reconstituted wafer and test package (13.42 mm × 13.42 mm). **b** Cross-section of the test package (three RDLs)

The basic philosophy of simulation of this case (Fig. 5.24) is the same as the heterogeneous integration case (Fig. 5.16), except for the geometry of the structure. The boundary (Temperature and kinematic) conditions are the same. The simulation (creep strain) results are shown in Fig. 5.24. It can be seen that the maximum strain occurs in the solder joint near the package corner and the chip corner and the failure mode is the cracking of the solder joint near the interface between the package and the bulk solder. These correlate very well with the experimental observation.

5.4.3 *Thermal Performance of Chip-First (Die Face-Up) Package*

Figure 5.25 schematically shows the top view and cross-sectional view of the FOWLP structure shown in Fig. 5.22 for thermal analyses [79, 80]. It can be seen that the chip size is 10 mm × 10 mm with various thicknesses (10, 25, 50, 100, 150, 200, 250, and 300 μm). There are a 100 μm EMC covering the top of the chip and 40 μm-RDLs to fan-out the circuitry from the bottom of the chip. The package is with 1024

Product Description
3M™ Light-To-Heat-Conversion Release Coating (LTHC) ink is a solvent based coating applied using a spin coating method. This coating forms the light to heat conversion layer on a glass substrate for 3M™ Wafer Support System.
Features and Benefits
• Enables stress free, room temperature debonding of adhesive
Typical Properties Note
The following technical information and data should be considered representative or typical only and should not be used for specification purposes.
Base Resin: Acrylic
Color: Black Thixotropic liquid
Specific Gravity: 1.00
Solid: 11%
Solvent: 1-Methoxy-2-propyl acetate
2-Butoxy Ethanol
Flash Point: 45°C
General Information
Standard container is 20L Stainless steel drum (UN: 1A1/X/250).
Storage
Store this product under normal conditions of 5°C to 35°C in original cont
storage life.
Shelf Life
Six months after the date of shipping from 3M.
Method of Usage
• Product must be stirred/mixed at 600-700 RPM for 12 hours before usage.
• Product must be stirred continuously while in use.



Fig. 5.21 3 M light-to-heat-conversion release coating

(0.2 mm-diameter) solder balls on a 0.4 mm-pitch, which are reflowed on a PCB. The dimensions of the PCB are 25 mm × 25 mm × 0.8 mm.

The ambient temperature is assumed to be 25 °C. The boundary condition on the top side and bottom side of the PCB and the top side of the chip is with a convective heat transfer coefficient, $h = 10$ W/m^{2}K, which is to imitate a natural convection condition. The heat dissipation of the chip is 5 W. The junction-to-ambient thermal resistance (Rja) of the 10 mm × 10 mm chip with various thicknesses is shown in Fig. 5.25. It can be seen that the thinner the chip the higher the Rja (i.e., the lower the thermal performance). This is because of the inferior thermal spreading capability of thinner chips. The thermal performance degrades rapidly as the chip thickness goes below 100 μm, as shown in Fig. 5.25. A typical temperature contour distribution is shown in Fig. 5.25 and it can be seen that: (1) the maximum temperature is 101.5 °C; (2) the minimum temperature is 89.9 °C; and (3) the Rja is 15.3 °C/W.

5.4.4 Applications of Chip-First and Die Face-Up FOW/PLP

Figure 5.26 shows the schematic and SEM images of the cross sections of the PoP (package-on-package) that houses the Apple application processor (AP) A10 and the mobile dynamic random access memories (DRAMs) of the iPhones. The PoP is

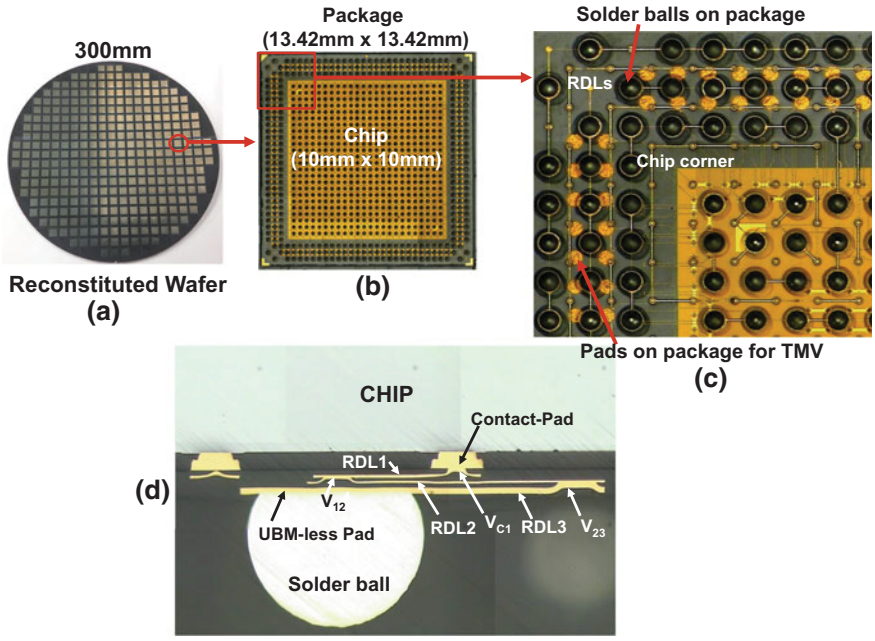


Fig. 5.22 Fabricated test package. **a** The reconstituted wafer. **b** Individual package. **c** Enlarge portion of the individual package. **d** Cross-section of the individual package showing the three RDLs and solder ball

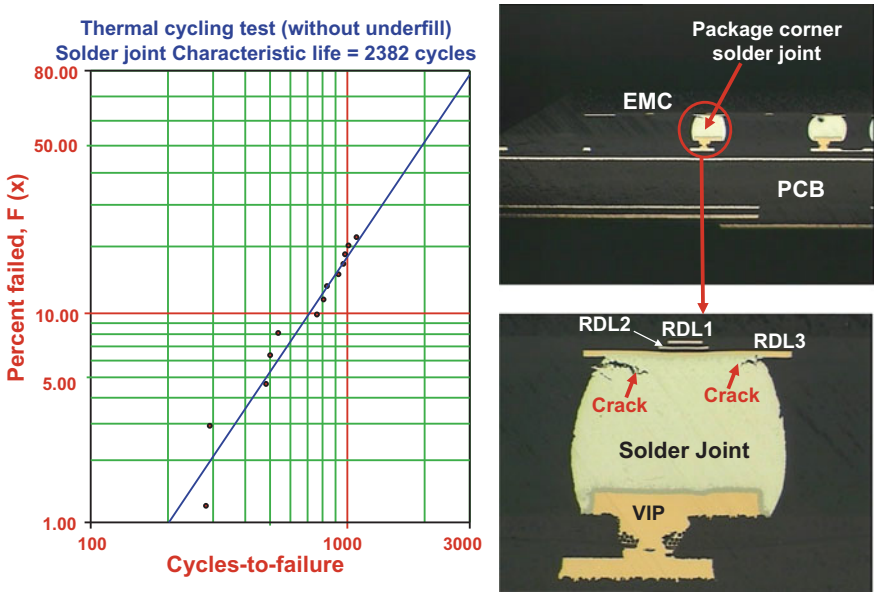


Fig. 5.23 Thermal cycling test results of the test package on a 6-layer PCB without underfill. Failure location and failure mode

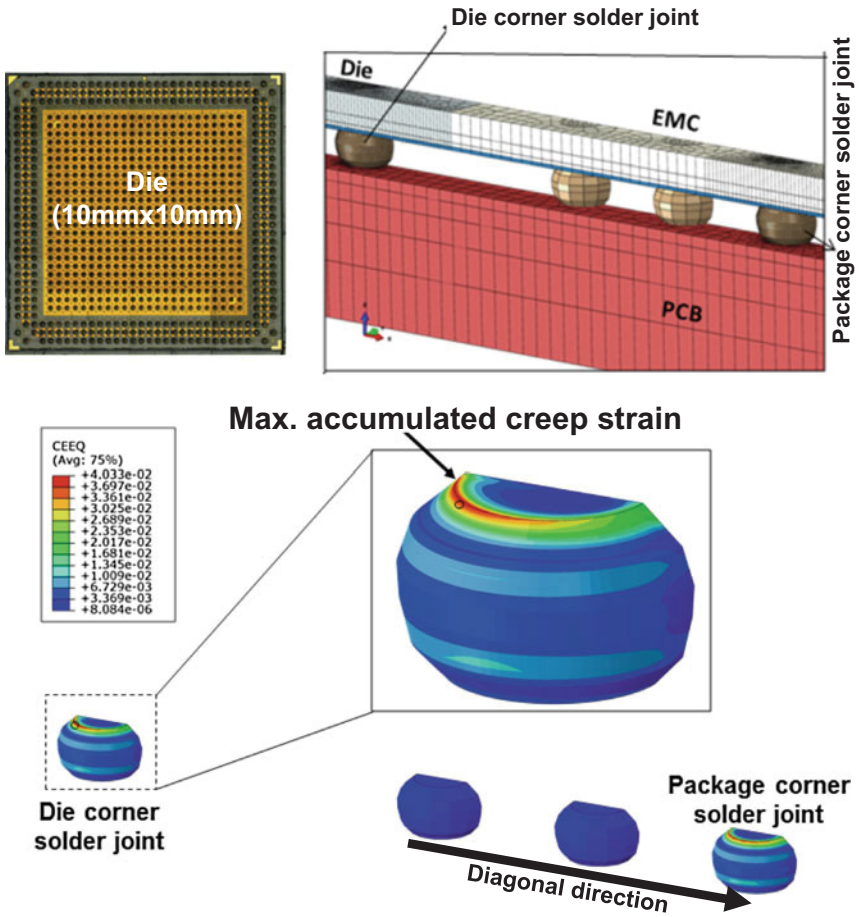


Fig. 5.24 Temperature and time dependent simulation results—cumulated creep showing the failure location and failure mode

fabricated by TSMC with its integrated fan-out (InFO) WLP technology [29–32]. It can be seen from the bottom package that the wafer bumping, fluxing, flip-chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the AP A9 shown in Fig. 3 of [89]) have been eliminated and are replaced by the RDLs (for the A10 as shown in Fig. 5.26). This results in a lower cost, higher performance, and lower profile package. The InFO is a chip-first and die face-up FOWLP.

The points noted above are very significant because Apple and TSMC are the trendsetters. Once they used the technology, it became likely that many others will

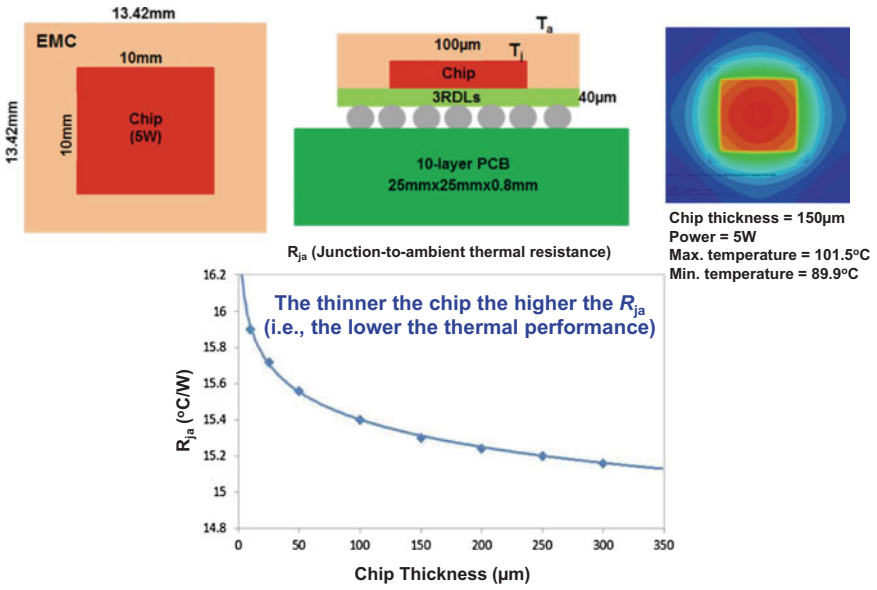


Fig. 5.25 Heat transfer analysis of a FOWLP on PCB assembly. Thermal resistance versus chip thickness

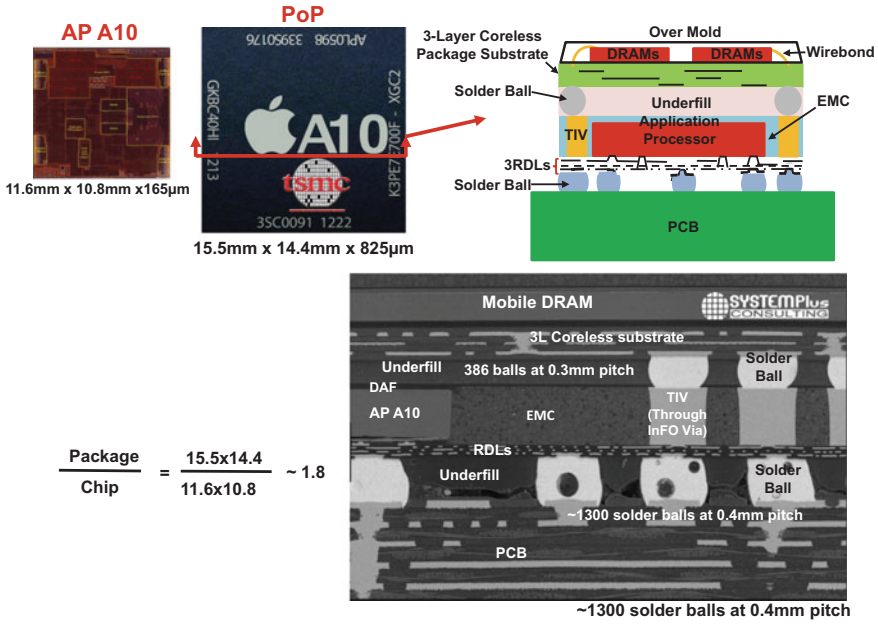


Fig. 5.26 TSMC's InFO-WLP for the application processor (A10) chipset of Apple's iPhones. (*Sources* SystemPlus)

follow. Also, this means that FOWLP is not only for packaging baseband, power management integrated circuits, radio-frequency (RF) switch/transceiver, audio codec, micro control unit, RF radar, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120 mm^2) SoC, such as APs. Furthermore, with the popularity of SiP or heterogeneous integration, fan-out chip-first and die face-up will be used more for fine (say 5 μm) line width and spacing RDLs.

5.5 Chip-Last or RDL-First

5.5.1 Reasons for Chip-Last or RDL-First

According to [19, 20], one of the challenges of chip-first (either die face-up or face-down) FOWLP and the key reasons for them to introduce the chip-last or RDL-first FOWLP is the production yield during the RDL process is low because the KGDs are already embedded. This is true only if the chip-last (RDL-first) FTI is fully functionally tested before the chip-to-wafer bonding. Otherwise, the KGDs still have to be thrown away for the case of a FTI with bad RDLs after a system test. Also, it should be noted that fully functionally tests of RDLs on a FTI are not only very costly but very difficult, if not possible.

5.5.2 Chip-Last or RDL-First Process

Figure 5.27 shows the process flow of the chip-last or RDL-first FOWLP. This is very different from the chip-first FOWLP discussed in Sects. 5.3 and 5.4. First of all, RDL-first FOWLP requires: (1) building up the RDLs on a bare silicon wafer (the FTI) or a glass wafer, (2) performing the wafer bumping, (3) performing the fluxing, chip-to-wafer bonding, and cleaning, and (4) performing the underfill dispensing and curing. As to wafer bumping, chip-to-wafer bonding and underfilling, e.g., please see [89, 90]. Each of these tasks is a major undertaking and requires additional materials, process, equipment, manufacturing floor space, and personal effort. Therefore, comparing to chip-first FOWLP, chip-last (RDL-first) FOWLP incurs very high cost and has a higher probability of greater yield losses. It can only be afforded by very-high density and performance applications such as high-end servers and computers.

The very first step in RDL-first is to build the RDLs on a bare silicon or glass wafer or panel, Fig. 5.27A–F. First, spin coat a sacrificial layer on a glass wafer or panel, Fig. 5.27A. Then, build up the Cu-pads and the dielectric-layer, and make the openings on the dielectric-layer, Fig. 5.27B. It is followed by electroplating the Cu metal-layer for RDL1, Fig. 5.27C. Repeat all the process to fabricate the other RDLs, Figs. 5.27D, E. Then, make the final dielectric-layer (passivation) and the micro-bump pads, Fig. 5.27F.

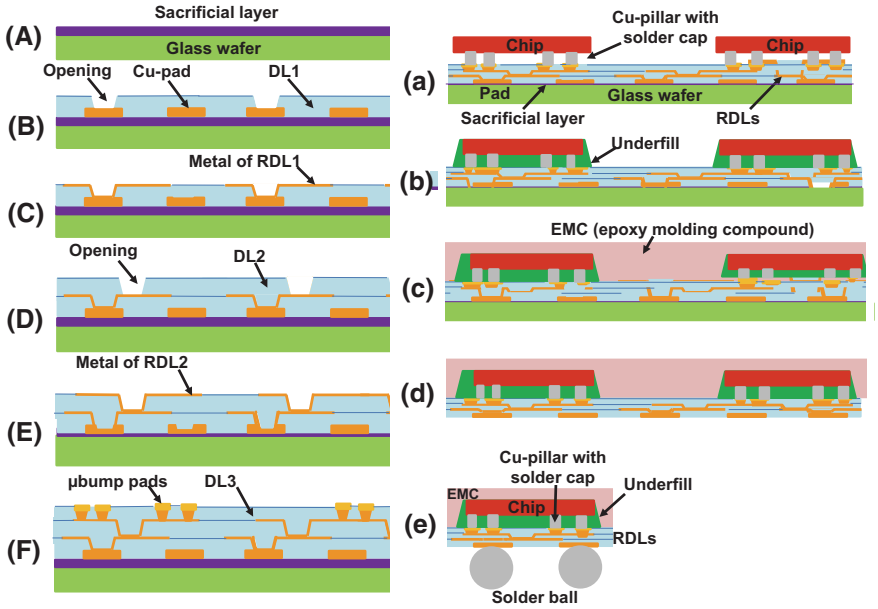
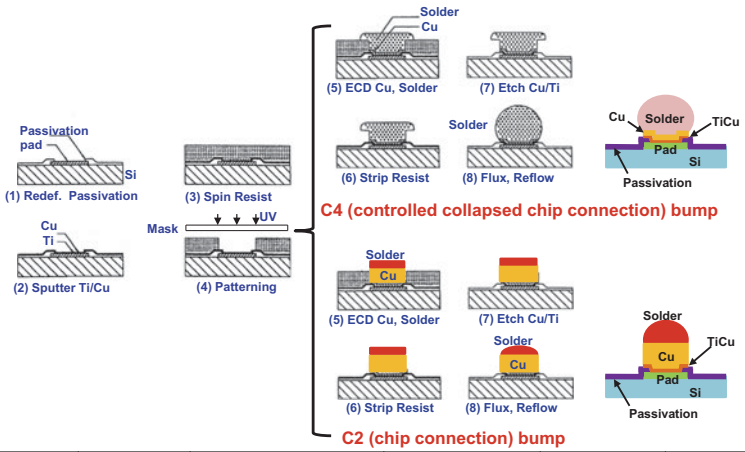


Fig. 5.27 Chip-last or RDL-first key process steps. Left-hand side is for making the RDLs on a glass wafer. Right-hand side is for making the package on the glass wafer

In parallel, on the device wafers, the first step is to perform wafer bumping as shown in Fig. 5.28 [89]. The next step is to test for KGDs and then dice the wafer into individual KGDs. Next, the KGDs are picked up, flux is applied, and then the KGDs are placed face down on the micro-bump contact pad (which is on top of the RDLs) of the full-thickness glass or silicon wafer (or panel) prior to performing chip-to-wafer bonding, Fig. 5.27a. That step is followed by cleaning the flux residue and then dispensing the underfill and curing, Fig. 5.27b. Next comes molding the whole reconstituted wafer carrier using the compression method with EMC, Fig. 5.27c. Then, remove the glass carrier, Fig. 5.27d. Finally, the solder balls are mounted on the bottom RDL and the reconstituted wafer is diced into individual packages, Fig. 5.27e.

5.5.3 Applications of Chip-Last or RDL-First FOW/PLP

In contrast to TSMC's chip-first and die face-up InFO PoP for Apple's AP chipset, Samsung proposed to use chip-last or RDL-first for their AP chipset [91–93] as shown in Fig. 5.29. It can be seen that the AP and the mobile DRAMs are placed side-by-side (not-PoP) with the chip-last FOW/PLP. The package profile of Samsung's side-by-side should be lower than Apple/TSMC's PoP. On the other hand, Samsung's



Structure	Major Material	Thermal conductivity (W/m K)	Electrical resistivity (μΩm)	Pad pitch	Self alignment
C2 bump	Cu	400	0.0172	Smaller	Smaller
C4 bump	Solder	55ó60	0.12ó0.14	Larger	Larger

Fig. 5.28 Wafer bumping key process steps for C4 bumps and C2 bumps

package horizontal dimensions should be larger. For other chip-last or RDL-first potential applications, please see [94–104].

The chip size with chip-last FOWLP can be very large and the metal line width and spacing of the RDLs can be very small. However, it is very expensive and can only be afforded by very-high density and performance applications. On the other hand, for high-density and high-performance applications, why insist on the FOWLP technology because there are many packaging alternatives?

5.6 RDLs Fabrications

RDLs [105–108] are the most integral part of wafer-level packaging (WLP) or panel-level packaging. The RDL consists of two layers, the dielectric layer and the Cu conducting layer. There are at least 8 ways to fabricate the RDLs for FOW/PLP [108]. In this chapter, only 4 ways are briefly mentioned.

5.6.1 Organic RDLs (Polymer and ECD Cu + Etching)

This is the oldest method to make RDLs for fan-in WLP, for examples, see [88]. The dielectric layer is made of a polymer, e.g., polyimide (PI), benzocyclobutene (BCB),

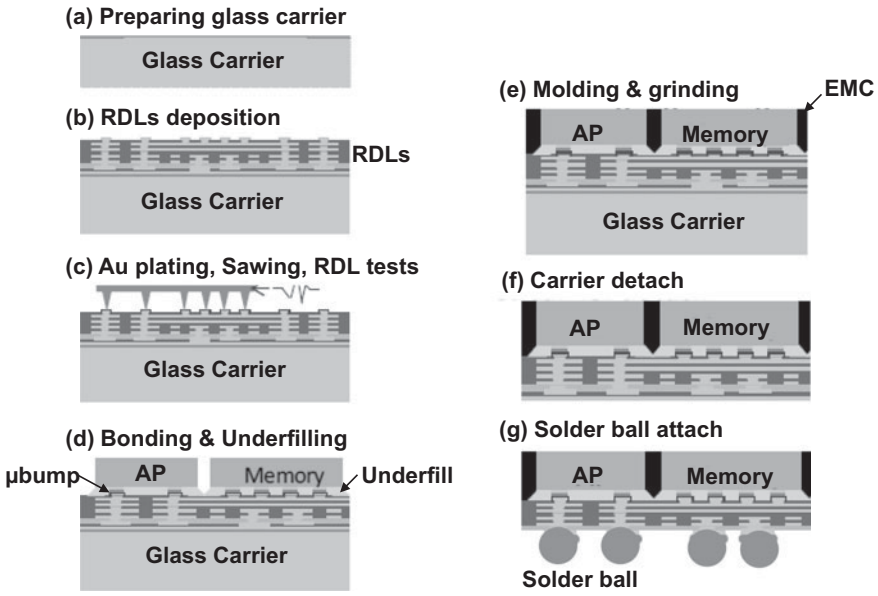


Fig. 5.29 Samsung's chip-last for the application processor chipset of smartphones

or polybenzobisoxazole (PBO) and the conductor layer is made by electrochemical deposition (ECD) of Cu and etching. The key process steps are described as follows: (1) First, spin coat a polymer on the whole wafer; (2) That step is followed by spin coating a photoresist; (3) Then the photoresist is opened with a mask aligner or stepper. (4) The polymer is then etched, and the resist is stripped off; (5) Next, the adhesive/seed layer (Ti/Cu) is sputtered using physical vapor deposition (PVD); (6) The photoresist is then spin coated, and then the photoresist is opened with a mask aligner or stepper; and (7) Next comes electroplating the Cu. After the resist is stripped off and the TiCu is etched off, we have the first RDL. If one repeats the processes, you get the other RDLs. Today, most outsourced semiconductor assembly and test (OSAT) use this method to make RDLs for FOWLP with chip-first and chip-last processing.

A better and simpler process is shown in Fig. 5.30 [46, 77]. It can be seen that for the PI (polyimide) development, the whole reconstituted wafer is spin-coated with a photosensitive PI. It is followed by applying a stepper (for high-yield) and then using photolithography techniques to align, expose, and develop the vias of the PI. Finally, the PI is cured at 200 °C for 1 h—this will form a 5 μm-thick PI layer. It is followed by sputtering Ti and Cu by PVD at 175 °C over the entire reconstituted wafer. Then, apply a photoresist and a stepper and use photolithography techniques to open the redistribution trace's locations. Next, electroplate the Cu by ECD at room temperature on the Ti/Cu in the photoresist openings. These steps are followed by stripping off the photoresist and etching off the Ti/Cu; RDL1 is thereby obtained.

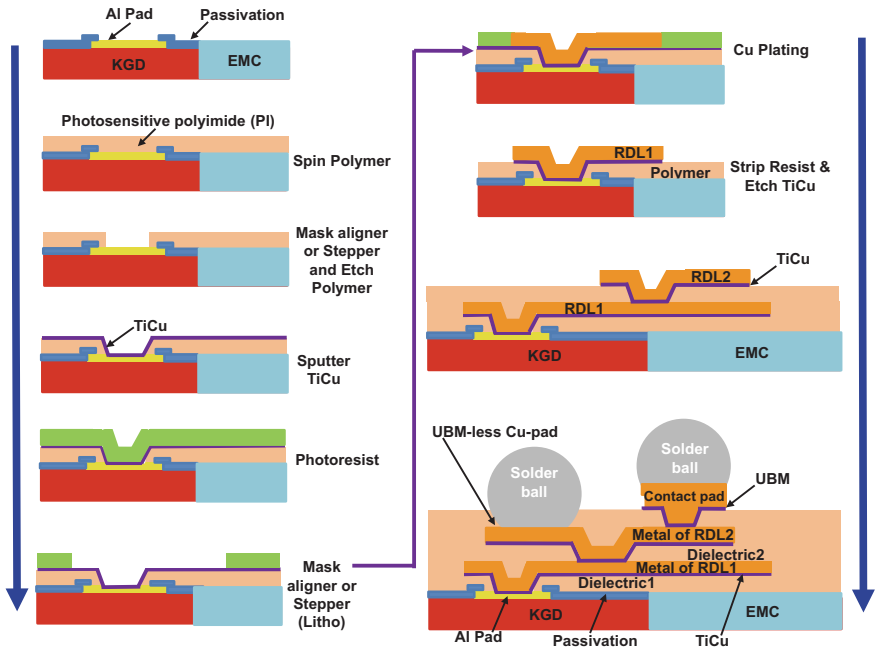


Fig. 5.30 Organic RDL (photosensitive polymer and ECD Cu + etching) key process steps

Finally, repeat all the above steps to obtain other RDLs. For example, the RDLs in Figs. 5.8 and 5.22 are fabricated by this method. This can be used for FOWLP with chip-first and chip-last processing. The RDLs made by the polymer (either photosensitive or not) and ECD Cu + etching are called organic RDLs. The metal line width and spacing of the RDLs can be as little as 5 μm for high yield. The organic RDLs are applied to chip-first as well as chip-last formations.

5.6.2 Inorganic RDLs (PECVD and Cu-Damascene + CMP)

This is the oldest back-end semiconductor process. This process uses SiO_2 or SiN for the dielectric layer and ECD to deposit the Cu on the whole wafer or panel carrier. That is followed by using CMP (chemical-mechanical polishing) to remove the overburden Cu and seed layer to make the Cu conductor layer of the RDLs. The key process steps are shown in Fig. 5.31. First, use plasma enhance chemical vapor deposition (PECVD) to form a thin layer of SiO_2 (or SiN) on a full thickness bare silicon wafer (or glass panel) and then use a spin coater to laminate the photoresist. These steps are followed by using a stepper to open the resist and a reactive ion etch (RIE) to remove the SiO_2. Then, a stepper is used to open the resist wider and RIE to etch more of the SiO_2. Next, strip off the resist, sputter the TiCu, and ECD the Cu on

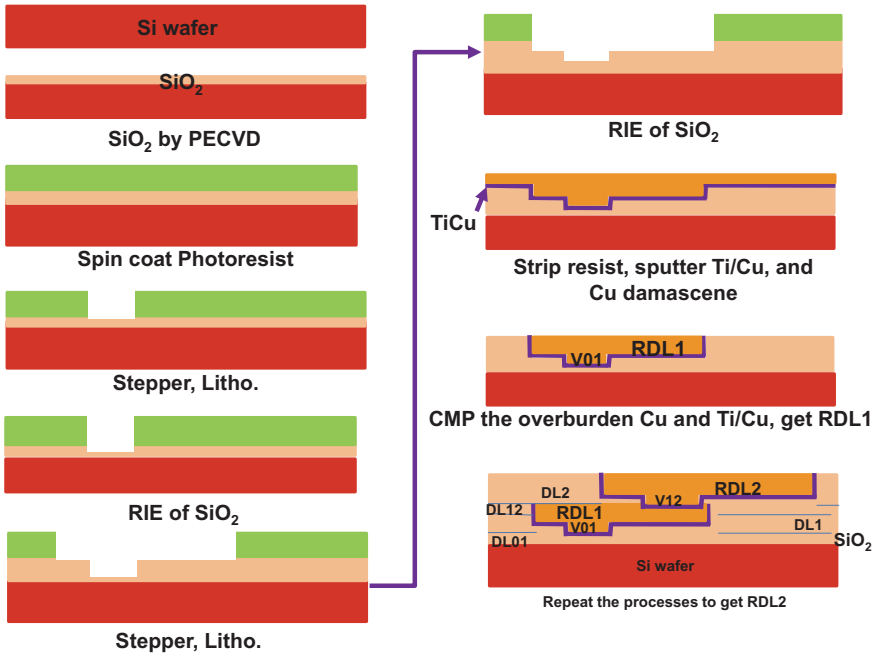


Fig. 5.31 Inorganic RDL (PECVP and Cu damascene + CMP) key process steps

the whole wafer or panel. These steps are followed by CMP to remove the overburden Cu and the TiCu, and then we have the first RDL1 and V01 (the via connecting the Si and RDL1) as shown in Fig. 5.32. This is called the dual Cu-damascene method [105, 106]. Finally, repeat all the processes to get the other RDLs. This method can be used for FOWLP with chip-first and chip-last processing. The RDLs made by PECVD and Cu-damascene + CMP are called inorganic RDLs. The metal line width and spacing of the RDLs can be $\leq 2\,\mu$m and down to submicron. The inorganic RDLs are sometimes applied to chip-last formations for very high-performance applications.

5.6.3 Hybrid-RDLs (First Inorganic RDLs and then Organic RDLs)

As of today, the hybrid-RDL method only applies to chip-last or RDL-first, i.e., wafer bumping and chip-to-wafer bonding are necessary. The key process steps for chip-last by hybrid RDLs are shown in Fig. 5.33. It can be seen that a glass carrier-1 is coated with a sacrificial layer, Fig. 5.33a. The contact pad and the first RDL (RDL1) are then fabricated by the PECVD for the SiO_2 dielectric layer and dual Cu-damascene + CMP for the conductor layer, Fig. 5.33b. The remaining RDLs are

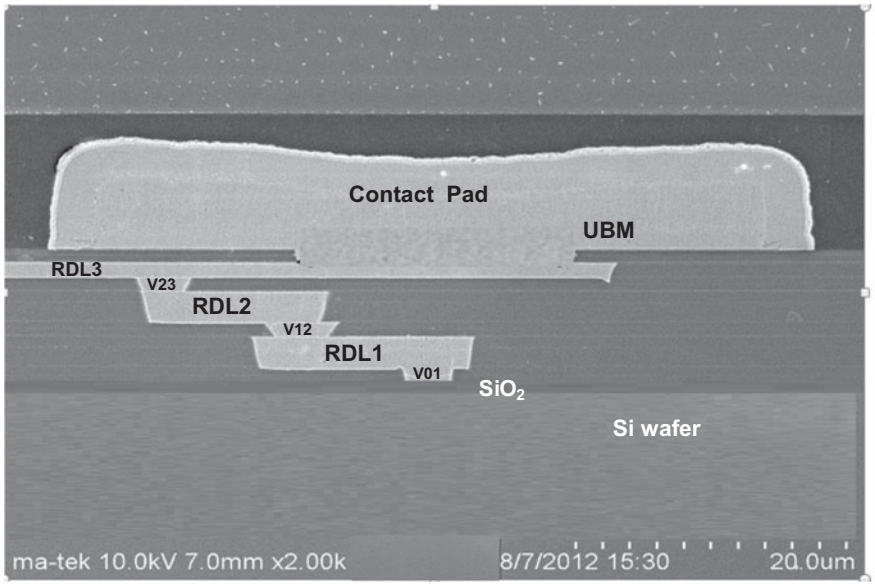


Fig. 5.32 Cross-section image of RDLs and Cu contact pad by PECVP and Cu damascene + CMP

fabricated by the ordinary polymer (or photosensitive polymer) and Cu-plating + etching method. Another carrier-2 is then attached to the other side of the reconstituted wafer, Fig. 5.33c. That step is followed by debonding of the carrier-1 as shown in Fig. 5.33d. That, in turn, is followed by fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing as shown in Fig. 5.33e. Then, the reconstituted wafer is molded with EMC by the compression method, Fig. 5.33f. Next comes debonding of the carrier-2 and solder ball mounting as shown in Fig. 5.33g. Figure 5.34 shows the cross section of a FOWLP with hybrid RDLs published by SPIL in [109]. For other hybrid-RDLs, please see [110, 111].

5.6.4 RDLs by Pure PCB Technology (ABF/SAP/LDI and Cu Plating + Etching)

Figure 5.35 shows a process flow for fabricating the RDLs on a panel published in [48–50]. It starts off by laminating an Ajinomoto buildup film (ABF) on the reconstituted ECM-panel. It is followed by laser drilling and electroless Cu seed layer plating. Then, follow those steps with dry film lamination, LDI lithography, dry film developing, and PCB Cu plating for RDL1. Follow those steps with stripping off the dry film and etching off the seed layer. These steps are then repeated to get the other RDLs. The final RDL can be used as a contact pad. The next steps are laminating, photolithography, and curing the solder mask (in either a solder mask

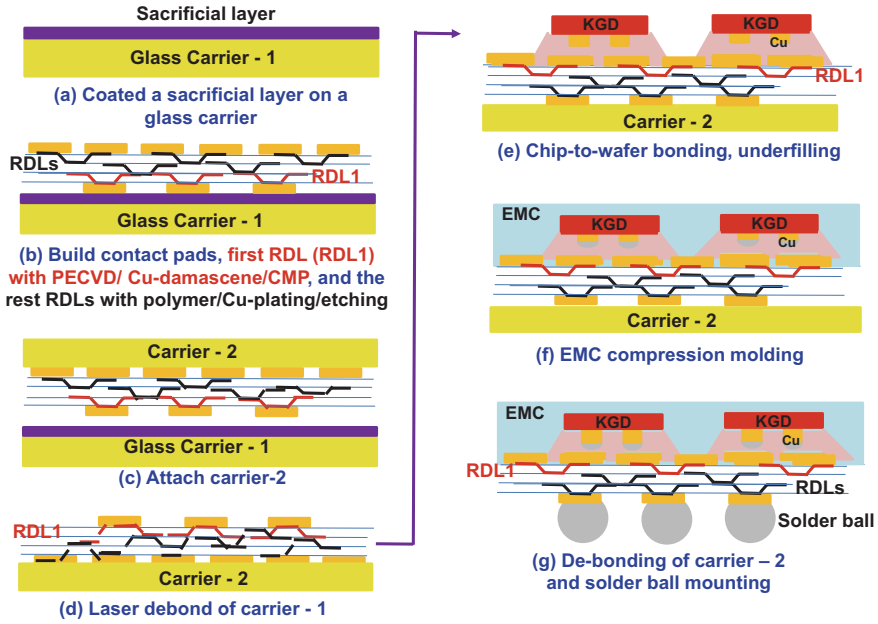


Fig. 5.33 Hybrid RDLs (first inorganic RDL and then organic RDLs) key process steps

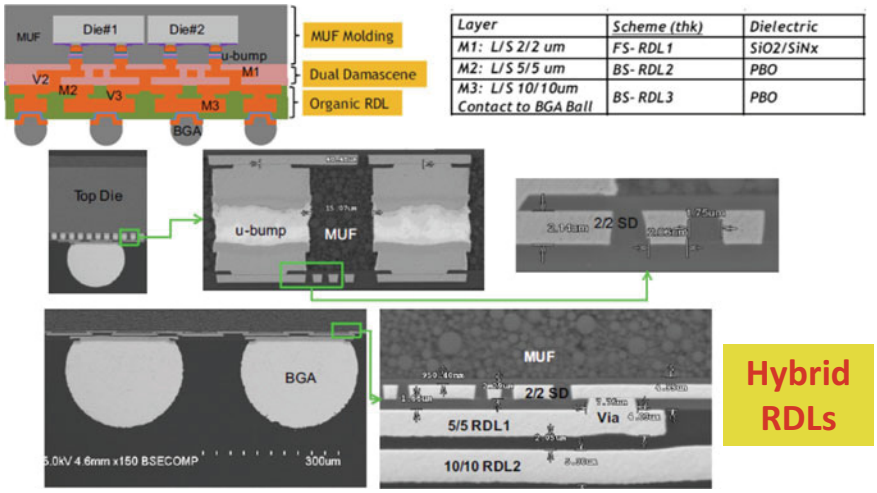


Fig. 5.34 SPIL's hybrid RDLs

defined, or a non-solder mask defined format) before mounting the solder balls. In this case, the dielectric layer thickness can be as little as 10 μm and the conductor layer thickness can be as little as 5 μm. For examples, the RDLs in Figs. 5.12 and 5.13 are fabricated by this method. In general, the metal line width and spacing of the pure PCB technology RDLs are ≥10 μm.

5.7 Warpage

Warpage is a critical issue for FOW/PLP and has been studied by Lin et al. [112] for wafer-level chip-first and die face down, Che et al. [113] is for wafer level mold first, Che et al. [114] is for wafer-level chip-last or RDL-first, Hou et al. [115] for panel-level packaging, Shen et al. [116] is for individual package with solder bumped flip chip with underfill on package substrate with a metal cap., and Lau, et al. [117, 118] are for chip-first and die face-up.

5.7.1 Various Kinds of Warpages in FOW/PLP

Depending on the formation of the package and the number of RDLs, there are a few different warpages affecting the FOW/PLP process. Let us use the chip-first and die face-up with 3 RDLs on a 300 mm FOWLP as an example such as those shown in Figs. 5.17 and 5.22. In this case, there are at least six different warpages affecting the FOWLP process.

The first warpage is right after PMC (see Fig. 5.17e) of the reconstituted wafer. If the warpage is too large, then the reconstituted wafer cannot be placed and/or operated on the backgrinding equipment to perform the backgrinding of EMC to expose the Cu-contact pads.

The second warpage is right after the backgrinding of the EMC to expose the Cu-contact pads (see Fig. 5.17f). If the warpage is too large, then the reconstituted wafer cannot be placed and/or operated on the RDL equipment such as the stepper, lithographic, physical vapor deposition (PVD), electrochemical deposition, and etching.

The third warpage is right after the fabrication of the first RDL. (The temperature of the PVD is about 200 °C, so there is a thermal expansion mismatch among the EMC, Si chip, and glass carrier.) If the warpage is too large, then there are issues in making the second RDL. The fourth warpage is right after the fabrication of the second RDL. If the warpage is too large, then there are issues in making the third RDL. The fifth warpage is right after the fabrication of the third RDL. If the warpage is too large, then there are issues (such as holding and/or operating of the reconstituted wafer on the equipment and controlling the accuracy of ball drops) in performing the solder ball mounting (see Fig. 5.17g).

The sixth warpage is right after the solder ball mounting. (The temperature of the lead-free reflow temperature is about 250 °C, so there is a very large thermal expansion mismatch among the EMC, Si chip, and glass carrier.) If the warpage of the diced individual package is too large (see Fig. 5.17h), then there are issues (such as solder joint standoff height variation, stretched solder joints, and titled component) in PCB assembly.

5.7.2 *Maximum Allowable Warpages*

What are the maximum allowable warpages? The rule of thumb is for a 300-mm reconstituted wafer, the maximum allowable warpage of the first five kinds of warpage is 1 mm, but 0.5 mm is preferred for high yield. The maximum allowable warpage of the individual package ($\leq$20 mm $\times$ 20 mm) is 0.2 mm, but 0.1 mm is preferred for high yield.

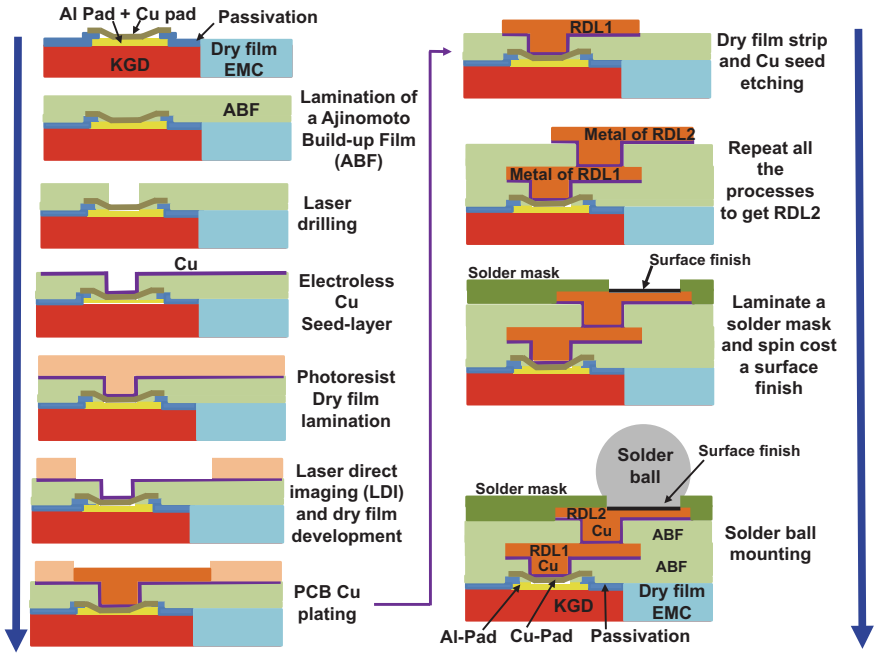


Fig. 5.35 RDLs by pure PCB process (SAP/LDI/Cu-plating and etching)

5.7.3 *Warpages: Measurements Versus Simulations*

Figure 5.36a shows the shadow Moire warpage measurements of the 300 mm reconstituted wafer (Fig. 5.22) right after PMC (609 μm in a smiling face), Fig. 5.17e, and right after backgrinding of the EMC to expose the Cu-contact pads (811.9 μm in a crying face), Fig. 5.17f. It should be emphasized that the warpage of the reconstituted wafer without RDLs and solder balls right after backgrinding of the EMC to expose the Cu-contact pads has been found to be changing from a smiling face to a crying face. Similar trend has been found by the simulation method shown in Fig. 5.36b [117, 118]. In order to reduce the warpage of the reconstituted wafer after PMC, the CTE of the glass carrier and EMC should be as close as possible. Also, in order to reduce the warpage of the reconstituted wafer after backgrinding, the CTE of the EMC should be larger than that of the glass carrier (to create a bigger smiling face). However, it should not be large enough to produce a warpage of the reconstituted wafer right after PMC >1 mm so the reconstituted wafer cannot be placed on the backgrinding machine.

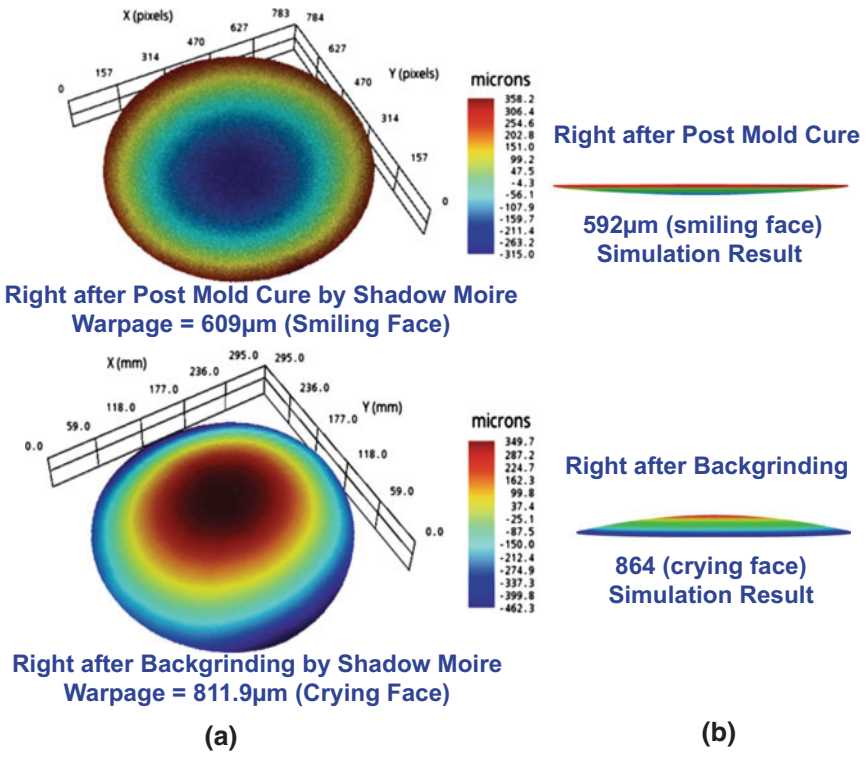


Fig. 5.36 Warpage of FOWLP (chip-first and die face-up) 300 mm wafer right after PMC and backgrinding. **a** Shadow Moire measurement. **b** Simulation results

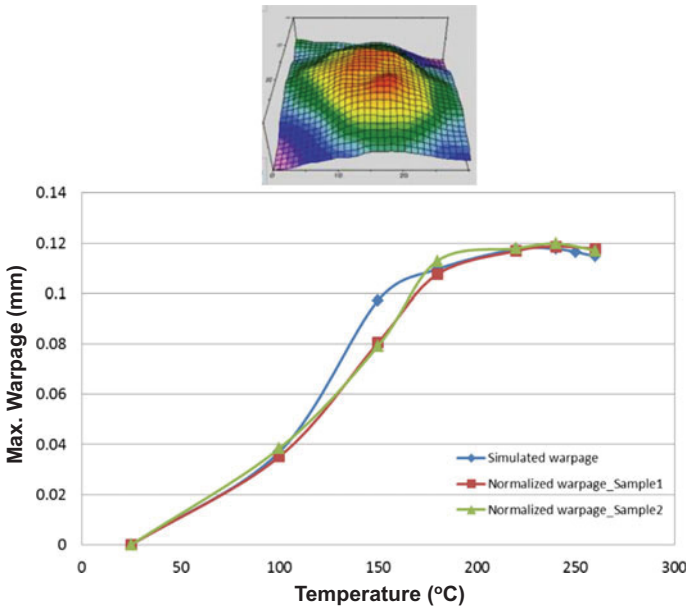


Fig. 5.37 (Top) Warpage contours by laser reflection method. (Bottom) Maximum warpage of individual package versus temperatures

According to JEDEC Standard (JESD22-B112A) [119], the laser reflection method (confocal displacement metrology) is used to measure the warpage of the individual package. Typical measured warpage contours of the present package are shown in the top of Fig. 5.37. The warpage measurements of two different individual package samples versus temperatures are shown in the bottom of Fig. 5.37, where the simulation results are also presented. They compared very well.

5.8 Temporary Wafer Versus Panel Carriers

First of all, FOWLP is itself a very high throughput WLP technology. Theoretically speaking, FOPLP is potentially higher throughput and lower cost than FOWLP. However, in order to achieve these goals, the following issues [120–123] for FOPLP need to be noted and/or resolved:

- Most OSATS and foundries already have the necessary equipment for FOWLP. For FOPLP, new capital will have to be expended on newly developed equipment.
- Inspection of wafers is a well-known process. FOPLP inspection must be developed.
- The yield of FOWLP is higher than that of FOPLP (assuming the size of the panel is larger than that of the wafer).

- The cost advantages of panel over wafer need to be carefully determined. (Yes, the throughput is higher, but the pick & place and EMC dispensing times are longer, and the yield is lower.)
- A fully loaded high-yield wafer line might be cheaper than a partially loaded low-yield panel line.
- The panel equipment takes longer to clean than wafer equipment.
- Unlike FOWLP, FOPLP is for medium chip size and metal line-width and spacing.
- If indeed, the panel processing is developed and is high yield for fine line-width and spacing, there is a chance to produce a major oversupply of capacity.
- Intellectual property, materials background, equipment automation, and management of the dimensional stability and yield of the panel in a large format are needed.
- The lack of a panel standard for FOPLP means equipment suppliers cannot make the equipment.

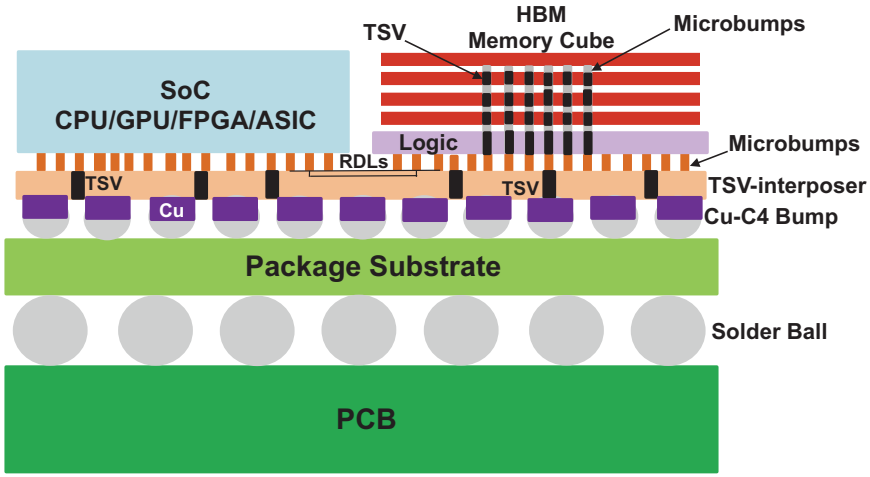
5.9 FOW/PLP Opportunities for Heterogeneous Integrations

Because of the drive of artificial intelligence, the semiconductors' density and I/Os increase and pad-pitch decreases. Even a 12 build-up layers (6-2-6) organic package substrate is not enough to support the semiconductors and a TSV-interposer is needed [124–142]. TSMC called this kind of structure CoWoS (chip-on-wafer-on substrate) [140, 141]. Leti [124, 125] called it SoW (system-on-wafer).

Figure 5.38 schematically [126] shows a heterogeneous integration of a SoC (system-of-chip) such as the CPU (central processor unit) or GPU (graphic processor unit) and HBMs which consist of a stack of DRAMs (dynamic random access memories) and a base logic vertically interconnect through TSVs (through-silicon vias) and microbumps. These SoC and HBMs are side-by-side attached through microbumps on a TSV-interposer with RDLs. The TSV-interposer is attached (through Cu-C4 bumps) on a package build-up substrate, which is then solder-ball attached to a PCB. NVidia's Pascal 100 GPU is an example. Since TSV-interposer is very expensive [10, 11], which leads to an opportunity for FOWLP.

STATSchipPAC proposed [34, 143] using the fan-out flip chip (FOFC)-eWLB to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 5.39. It can be seen that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated.

ASE [35] proposed using the FOWLP technology (chip-first and die face-down on a temporary wafer carrier and then overmolded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 5.40. ASE called it fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected



Underfills are applied:

- **Between the TSV-interposer and SoC/Logic + Memory Cube**
- **Between the TSV interposer and package substrate**

Fig. 5.38 TSMC's CoWoS-2

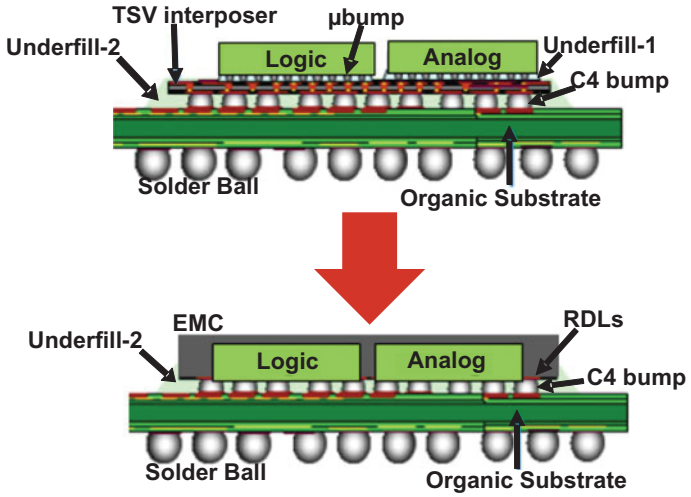


Fig. 5.39 STATSChipPac's FOCoS with chip-first process

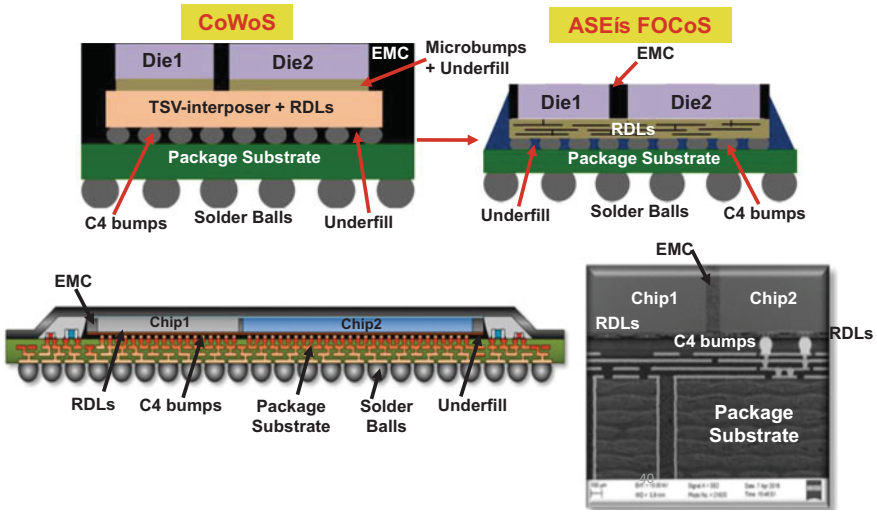


Fig. 5.40 ASE's FOCoS with chip-first process

to the package substrate using under bump metallurgy (UBM) and the C4 bump as shown in Fig. 5.40. Recently, TSMC [144] called this InFO_oS (integrated fan-out on substrates).

Recently, Samsung [145] proposed using chip-last or RDL-first FOWLP to eliminate the TSV-interposer as shown in Fig. 5.41. First of all, they build the RDL on a silicon wafer or glass panel. In parallel, wafer bumping of the logic and HBM. Then, perform fluxing, chip-to-wafer or panel bonding, cleaning, underfill dispensing and curing. It is followed by EMC compression molding. Then, backgrind the silicon wafer and C4 wafer bumping. It is followed by attaching the whole module on the package substrate. Finally, perform solder ball mounting and lid attachment. Samsung called it Si-less RDL interposer [145].

TSMC [146] proposed to use the FOWLP technology + Cu-pillar/solder bump to eliminate the TSVs in the HBM cube. In the individual chip (DRAM without bumps), by using the FOWLP to make the RDLs to fan-out all the circuitries to the peripherals of the package. The vertical interconnects of the individual packages are through the Cu-pillars and solder bumps, as shown in Fig. 5.42. Figure 5.43 shows another example [147], where 6 layers of chips are vertically interconnected together without TSVs. FOWLP has been used to build the RDLs to fan-out the circuitries to the peripheral of the packages and the vertical interconnects are through the Cu-pillar and microbumps.

Since the Intel's proposal [148, 149] of using EMIB (embedded multi-die interconnect bridge) to serve as the high-density interconnects between chips in a heterogeneous integration system, Fig. 5.44, the "bridge" has been very popular. Basically, a bridge is a piece of dummy (deviceless) silicon with RDLs and contact pads but without TSVs. For example, recently IMEC proposed [150] to use the bridges +

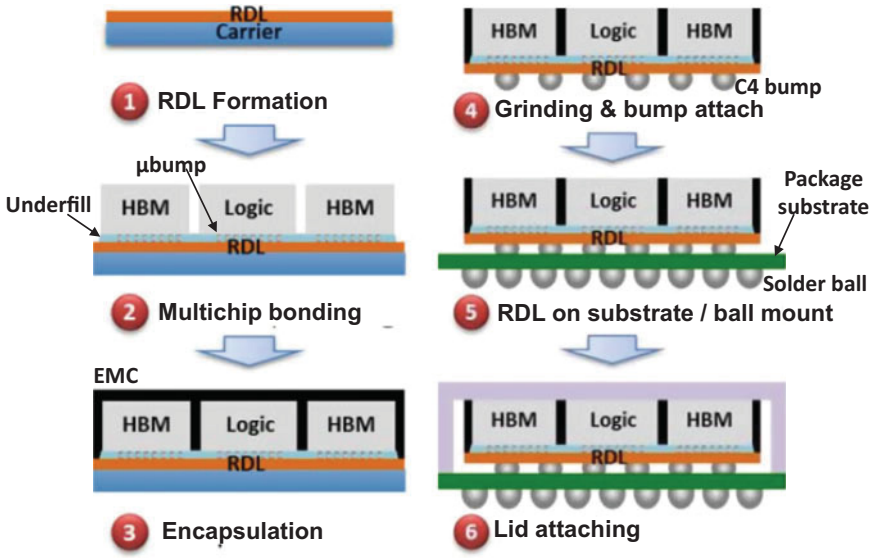


Fig. 5.41 Samsung's Si-less RDL interposer with chip-last process

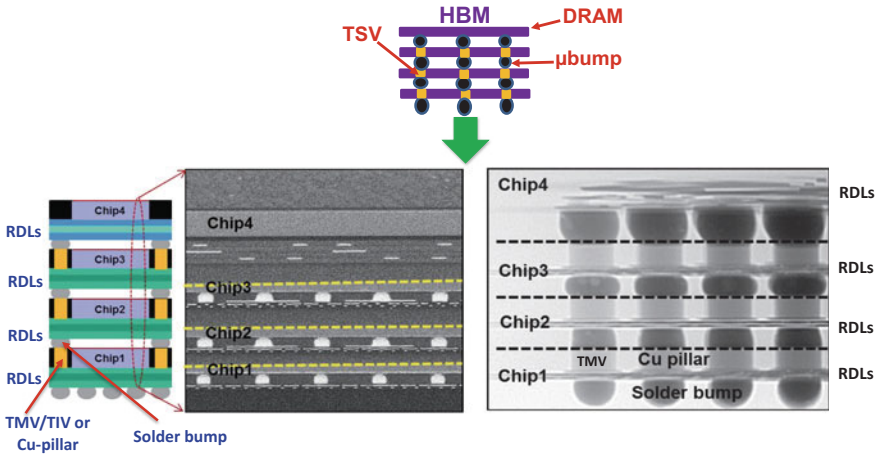


Fig. 5.42 TSMC's InFO-WLP + Cu-pillar/solder bumps for HBM

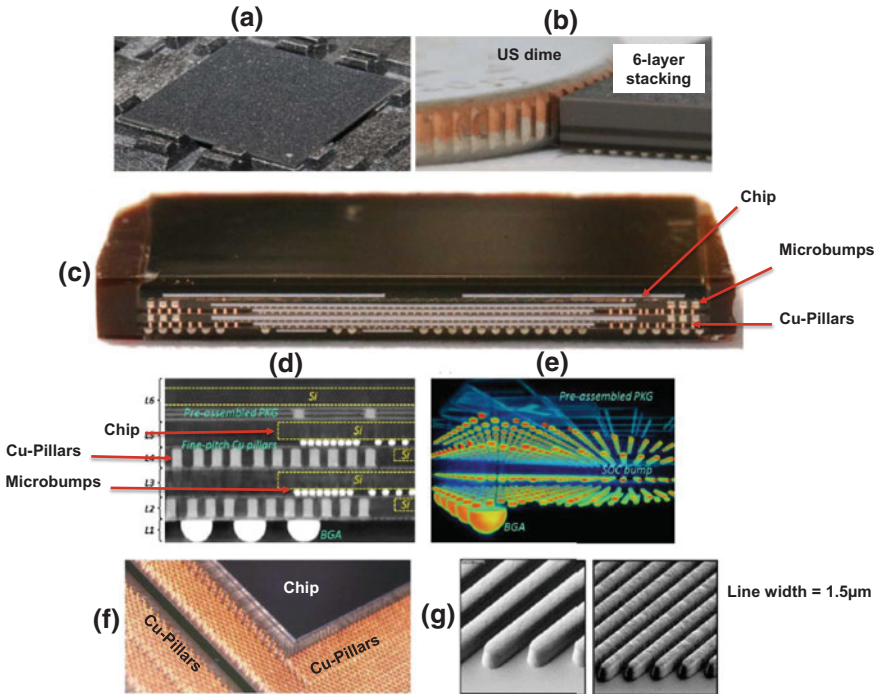


Fig. 5.43 TSMC's InFO-WLP + Cu-pillar/μbumps for high-performance system

FOWLP to interconnect the logic chip, wide I/O DRAM, and the flash memory as shown in Fig. 5.45. Their objective is not to use TSVs for all the device chips.

TSMC [151] demonstrated that the InFO_AiP (antenna-in-package) for high performance and compact 5G millimeter wave system integration is superior than that of solder bumped flip chip AiP on substrate as shown in Fig. 5.46. It can be seen that: (a) in the 28 GHz frequency range, InFO RDLs transmission loss (0.175 dB/mm) is 65% less than that on flip chip substrate trace (0.288 dB/mm), and (b) in the 38 GHz frequency range, the transmission loss for InFO RDLs (0.225 dB/mm) is 53% less than that (0.377 dB/mm) on flip chip substrate trace.

5.10 Summary and Recommendations

The recent advances and trends of FOW/PLP have been presented in this chapter. Some important results and recommendations are summarized in the follows.

- Chip-first is a good choice for heterogeneous integration of semiconductor ICs such as baseband, RF/analog, PMIC, AP, and low-end ASIC, CPUs and GPUs for portable, mobile, and wearable products. While chip-last (RDL-first) is potentially

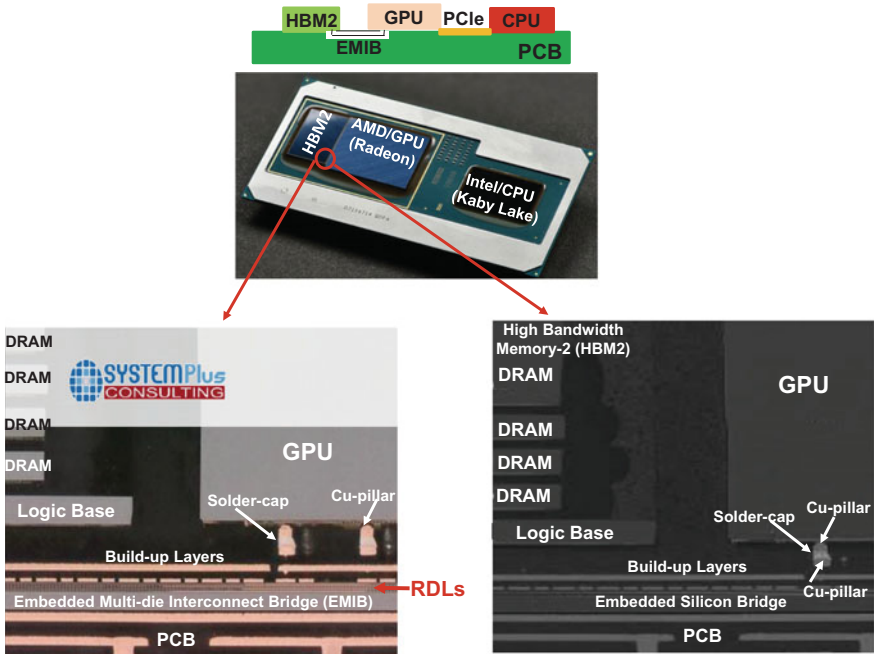


Fig. 5.44 Intel's EMIB. *Sources* SystemPlus

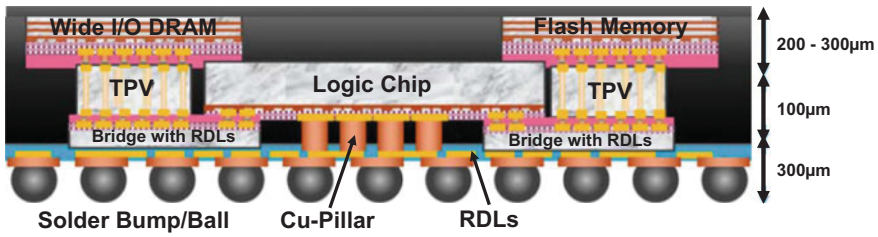
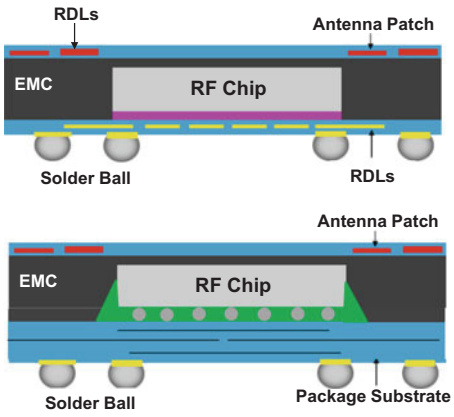


Fig. 5.45 IMEC's bridge for heterogeneous integration system

suitable for heterogeneous integration of semiconductor IC devices such as high-end CPUs, GPUs, ASICs, and FPGAs (field programmable gate arrays) for super computers, servers, networking, and telecommunication products.

- Chip-first and die face-down is the most simple and low cost formation. In general, this applies to smaller chips and the metal line width and spacing of the RDLs are $\geq$10 µm.
- The process steps of chip-first and die face-up are a little more complicated than chip-first and die face-down and thus slightly higher cost. In general, this applies to larger chips and the metal line width and spacing of the RDLs are $\geq$5 µm.
- The process steps of chip-last or RDL-first are the most complex and high cost. However, it applies to very large chips and the metal line width and spacing of the



THE TRANSMISSION LOSS FOR RDL AND SUBSTRATE TRACE AT 28 AND 38GHZ

Frequency	InFO RDLs	Substrate Trace
28GHz	0.175dB/mm	0.288dB/mm
38GHz	0.225dB/mm	0.377dB/mm

Fig. 5.46 TSMC's InFO-AiP for 5G

RDLs are <5 μm to submicron. Thus, this process can only be afforded by very-high density and performance applications. On the other hand, for high-density and high-performance applications, why insist on the FOWLP technology because there are many other packaging alternatives?

- Organic RDLs fabricated by polymer (either photosensitive or not) and ECD Cu + etching is the most common method for FOWLP by OSATS or even foundries. It can be applied to the chip-first and chip-last formations.
- Inorganic RDLs fabricated by PECVD and Cu damascene + CMP is a backend semiconductor method for the chip-last FOWLP formation. By viewing the change of the metal line width and spacing (from 5 μm to 10 μm) of the RDLs of the application processor chipsets (from A10 of iPhone 7 to A11 of iPhone 8), the chance of using PECVD and Cu- damascene + CMP in fabricating the RDLs for FOWLP is very slim (may be only for niche applications). If there is a need for inorganic RDLs, however, why insist on the FOWLP technology?
- Hybrid RDLs fabricated by inorganic RDL first and then organic RDLs are a mixed method for the chip-last FOWLP formation. Again, if there is a need for hybrid RDLs, why insist on the FOWLP technology?
- RDLs by pure PCB/LDI technology is for FOPLP. There is not any semiconductor equipment required and is the highest throughput and lowest cost technology. However, the chip sizes are small (<8 mm × 8 mm) and the metal line width and spacing of the RDLs are large (≥10 μm).

- In order to increase the throughput and yield and reduce the cost with FOPLP some important issues (should be noted and resolved) have been highlighted.
- Warpage is a critical issue for FOW/PLP. Depending on the formation of the package and the number of RDLs, there are a few different warpages affecting the FOW/PLP process. What are the maximum allowable warpages? The rule of thumb is for a 300-mm reconstituted wafer, the maximum allowable warpage of the reconstituted wafer is 1 mm, but 0.5 mm is preferred for high yield. The maximum allowable warpage of the individual package ($\leq$20 mm $\times$ 20 mm) is 0.2 mm, but 0.1 mm is preferred for high yield.

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Chapter 6
Heterogeneous Integrations on Fan-Out RDL Substrates



6.1 Introduction

As mentioned in Chap. 4 that TSV (through-silicon via) interposer is very expensive [1–10] and a few silicon bridges have been proposed to replace the TSV interposers for heterogeneous integration applications. Recently, using the fan-out wafer/panel packaging technology [11–20] to make RDLs (redistribution-layers) on substrates to eliminate the TSV-interposer for heterogeneous integrations has been getting traction. At ECTC2013, Statschippac proposed using the fan-out flip chip to make the RDLs for the chips to perform mostly lateral communications. During ECTC2016, ASE and Mediatek used a similar technology to fabricate the RDLs with FOWLP and showed that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated, i.e., TSV-less interposers. At ECTC2018, Samsung used chip-last or RDL-first to make the RDLs for the TSV-interposer. During SEMICON Taiwan 2018, TSMC also mentioned this technology and called it InFO_oS (integrated fan-out on substrate).

6.2 STATSChipPAC's FOFC-eWLB

On December 23, 2011, STATSChipPAC filed a patent called "Semiconductor device and method of forming extended semiconductor device with fan-out interconnect structure to reduce complexity of substrate" [21]. At ECTC2013, STATSchipPAC proposed and published in [22] using the fan-out flip chip (FOFC)-eWLB (embedded wafer-level ball grid array) to make the RDLs for the chips to perform mostly lateral communications in the heterogeneous integration system as shown in Fig. 6.1. It can be seen that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated.

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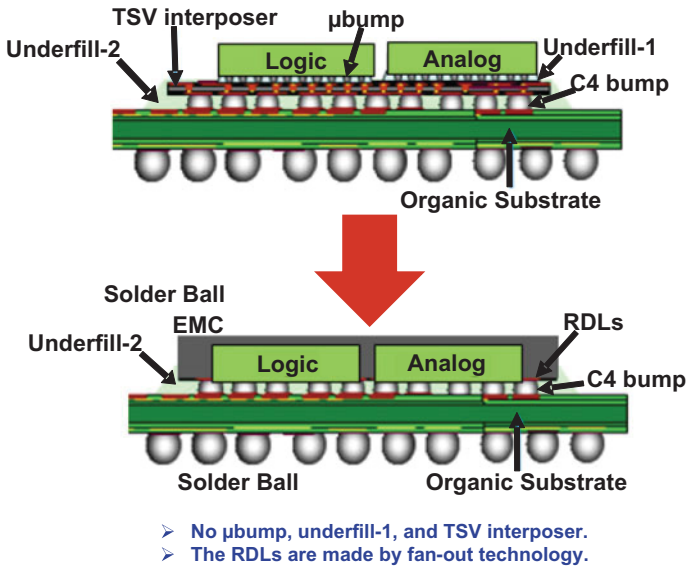


Fig. 6.1 STATSChipPac's fan-out substrate (FOFC-eWLB) for heterogeneous integrations

6.3 ASE's FOCoS

In 2016, ASE [23] proposed using the fan-out wafer-level packaging (FOWLP) technology (chip-first and die-down on a temporary wafer carrier and then overmolded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 6.2; the technology is called fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 (controlled collapse chip connection) bump as shown in Fig. 6.2.

6.3.1 Key Process Steps

The assembly process steps for the ASE FOCoS are shown in Fig. 6.3. It can be seen that there are three major tasks, namely, reconstitution wafer and molding, RDL formation, and flip chip bonding. A chip-first and die face-down fan-out wafer-level formation (e.g., Sect. 5.3) is used. That is to put the chips face-down side-by-side on a two-side thermal release tape on a reconstituted wafer carrier. Then, compression molding the EMC (epoxy molding compound) and post mold curing. It is followed by removing the tape and performing the RDLs fabrication (e.g., Sect. 5.6.1). There

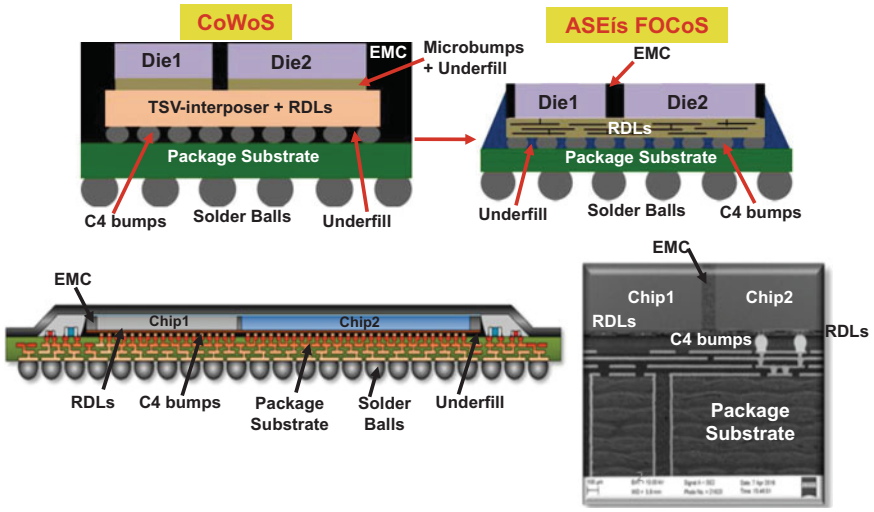


Fig. 6.2 ASE's fan-out (chip-first) substrate (FOCoS) for heterogeneous integrations

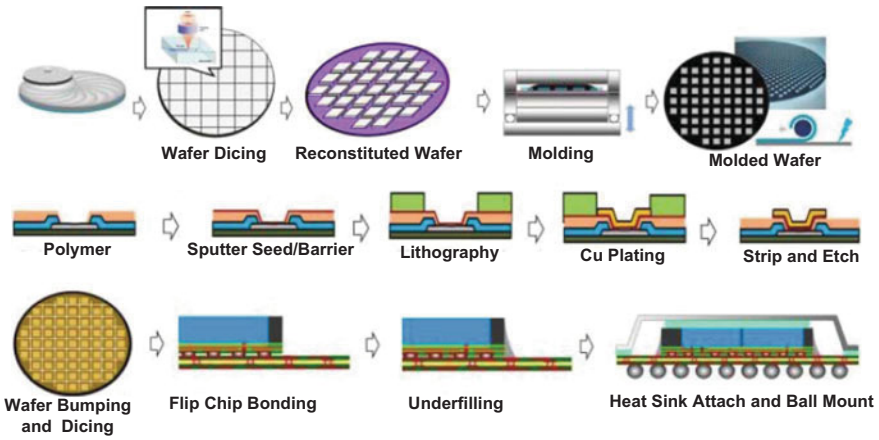


Fig. 6.3 ASE FOCoS key process steps

are 3 metal layers and 4 polymer layers for the RDLs. The third major step is to perform wafer bumping of the chips with C4 bumps and dice the reconstituted wafer into individual packages. It is followed by flip chip bonding and underfill dispensing and curing. Finally, attach a heat sink and mount the solder balls. Figure 6.4 shows the image of cross section of the ASE FOCoS.

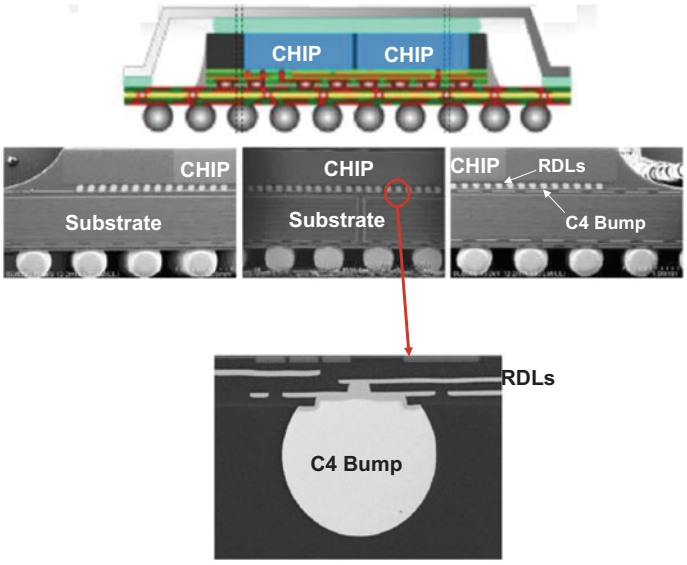


Fig. 6.4 SEM images of cross section of FOCoS

6.3.2 Reliability of FOCoS

In heterogeneous integrations, the spacing between chips has to be as small as possible in order to achieve the best electrical performance. However, if the chips are placed too close to each other, the reliability of the "short" RDLs between them could be an issue. During thermal cycling test, high temperature storage test, and thermal shock test, etc. ASE found that the RDLs may crack if the RDLs are not properly designed [24].

Figure 6.5 schematically shows the thermal-mechanical behavior during thermal cycling test. It can be seen that at low temperature the package is in a crying-face and the RDL1 is subjected to compression. On the other hand, when it is at high temperature, the package is in a smiling-face and the RDL1 is subjected to tension. After certain temperature cycles, the Cu conductor wiring is cracked as shown in Fig. 6.6.

Four different RDL designs, as shown in Fig. 6.7, have been modelled by finite element method and built and experimental measured [24]. The designs in Fig. 6.7a, b both have angle bend on RDL under the chip area and the designs in Fig. 6.7c, d are the RDLs of no angle bend under chip area. Designs in Fig. 6.7a, b, c have increase RDL lines to enhance the RDL strength, on the other hand the design in Fig. 6.7d has non-right-angle trace layout near RDL terminal pads.

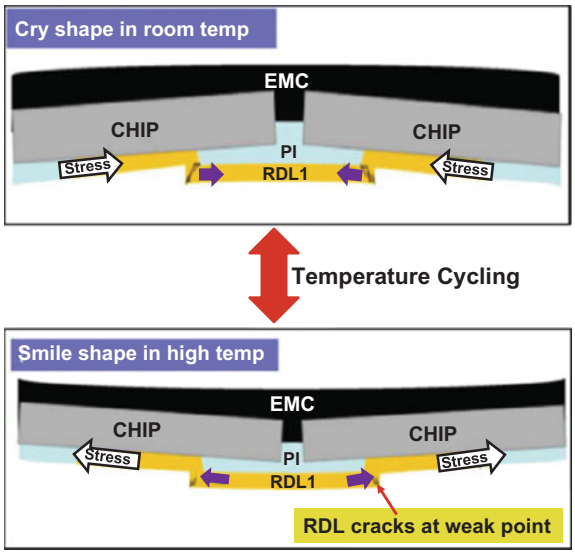


Fig. 6.5 Mechanical behaviors of FOCoS during temperature cycling

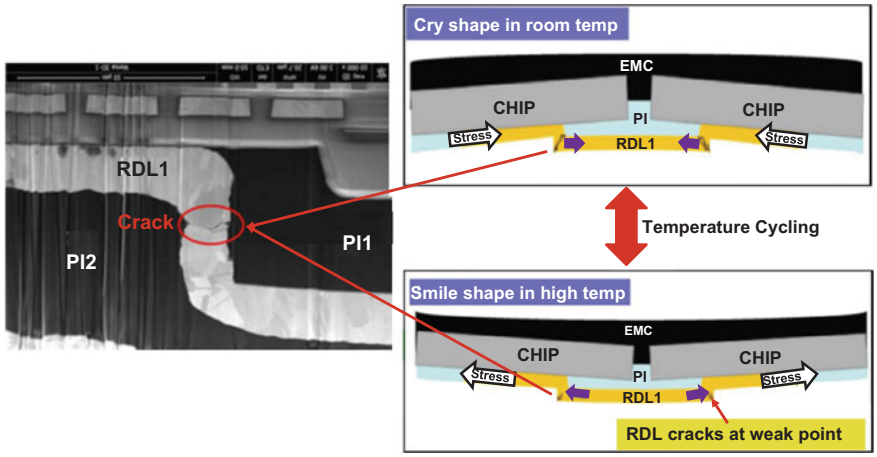


Fig. 6.6 Cracking of RDLs in FOCoS during temperature cycling

The simulation results demonstrated that the stresses in the designs of Fig. 6.7c, d are less than those in the designs of Fig. 6.7a, b. The temperature cycling results also demonstrated there is no failure over 1000 cycles in the designs of Fig. 6.7c, d. However, there are failures under 500 cycles in the designs of Fig. 6.7a, b. Thus, the RDL designs of Fig. 6.7c, d should be used.

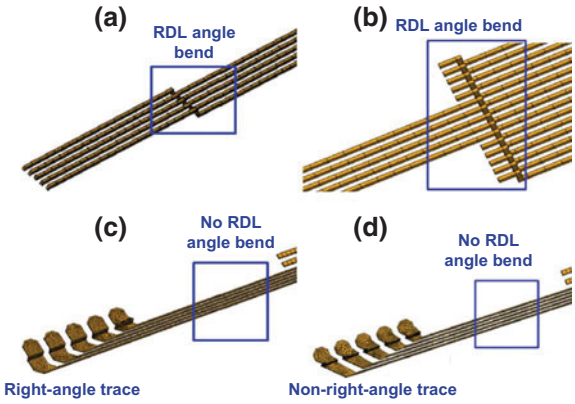


Fig. 6.7 Designs of RDLs for FOCoS

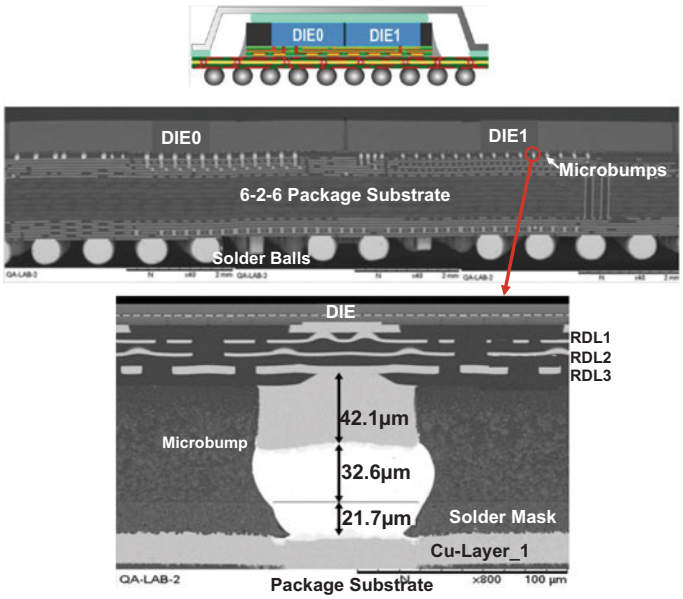


Fig. 6.8 TSV-less interposer: Mediatek's RDLs by FOWLP

6.4 Mediatek's RDLs by FOWLP

In 2016, Mediatek [25] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in Figs. 6.8 and 6.9. Instead of the C4 bump, they used a microbump (Cu-pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate (Fig. 6.8).

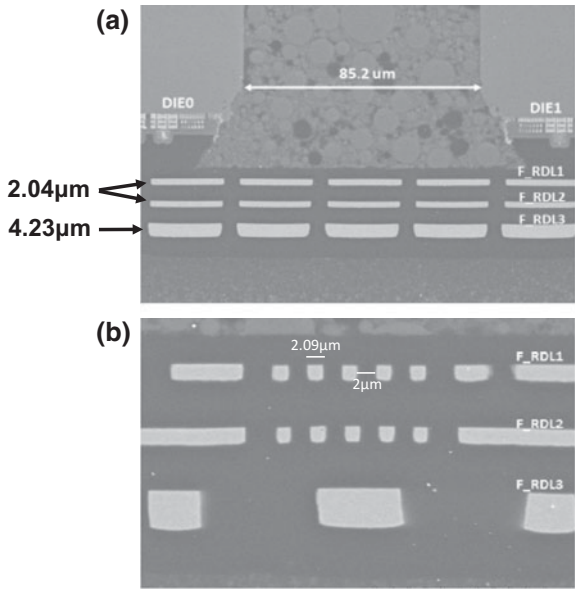


Fig. 6.9 Cross section images of Mediatek's TSV-less interposer. **a** Horizontal view. **b** Vertical view

The bump height after reflow is about 96.4 μm. The horizontal cut cross-section image of a fan-out chip (DIE0/1) is shown in Fig. 6.9a. It can be seen that the average metal thickness of RDL1 and RDL2 is 2.04 μm and of RDL3 is 4.23 μm. The vertical cut cross-section image between DIE0 and DIE1 is shown in Fig. 6.9b. It can be seen that the average metal trace width and spacing are 2.09 and 2.00 μm, respectively.

6.5 TSMC's InFO_oS

Figure 6.10 shows the schematic of TSMC's InFO_oS (integrated fan-out on substrate) [26]. The RDLs are fabricated by TSMC's InFO chip-first and die face-up technology. This InFO_oS is for high performance applications but not as high as those with CoWoS or CoWoS-2 technology. From Sect. 6.2 through 6.5, chip-first fan-out wafer-level packaging has been used to elimination the TSV interposers.

6.6 Samsung's Si-Less RDL Interposer

Recently, Samsung [27] proposed the use of chip-last or RDL-first fan-out wafer/panel level packaging to eliminate the TSV-interposer (Fig. 6.11) for high performance computing heterogeneous integration applications. Samsung called the resulting structure a Si-less RDL interposer [27].

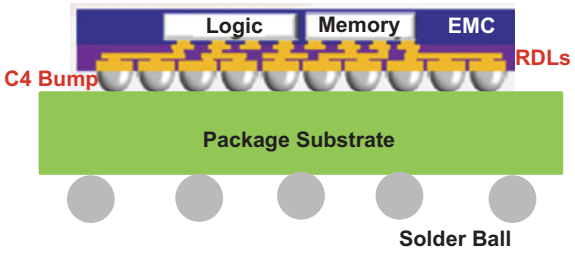


Fig. 6.10 TSMC's TSV-less interposer (InFO_oS) for heterogeneous integrations

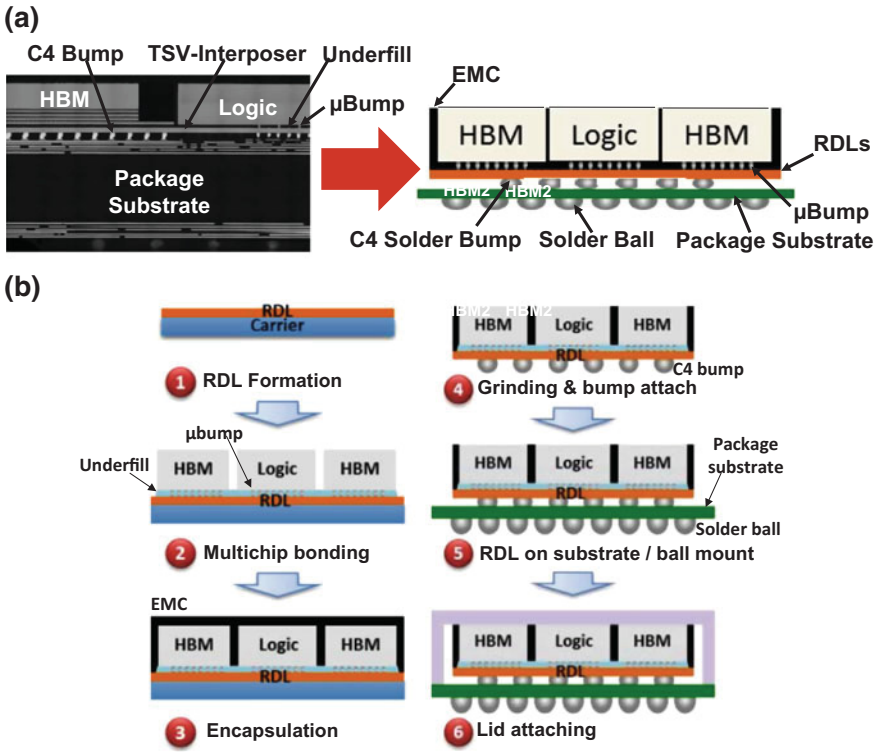


Fig. 6.11 Samsung's TSV-less interposer (Si-less RDL interposer) for heterogeneous integrations

6.6.1 Key Process Steps

First of all, the RDLs are built on a bare glass—either in a wafer or a panel format. In parallel, wafer bumping of the logic and HBM chips are being done. Then, the following processes are done: fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfill dispensing and curing. Those steps are followed by EMC compression molding. Then, backgrinding the EMC, chips, and HBM cube and C4 wafer bumping

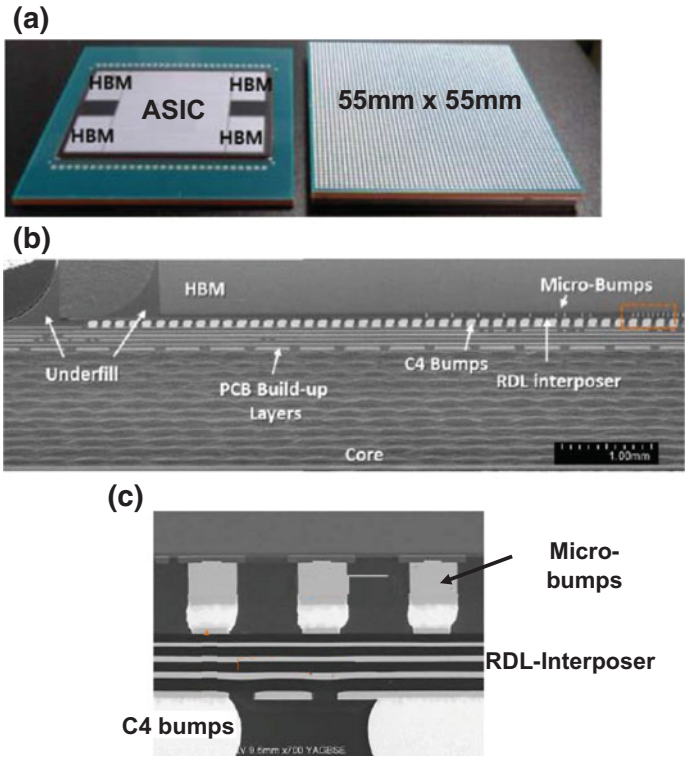


Fig. 6.12 Test vehicle and cross section of Si-less RDL interposer

are done. After those steps, one can attach the whole module on the package substrate. Finally, solder ball mounting and lid attachment are done. Figure 6.12 shows the test vehicle reported in [27]. It can be seen that the package (RDL interposer) substrate size is 55 mm $\times$ 55 mm and there are 5-layer of RDLs including the bonding layer, signal, and ground layers.

6.6.2 Reliability of Si-Less RDL Interposer

Figure 6.13 shows the Si-less RDL interposer heterogeneous integration. While Fig. 6.14 shows the conventional CoWoS. Because of the thermal expansion mismatch between the TSV interposer and the organic package substrate is larger than that between the EMC/Si chips and the organic package substrate, the stress in the C4 solder joints of the Si-less RDL interposer is less than that of the CoWoS. Actually, according to the modelling results from Samsung, it is 34% less. Also, the maxi-

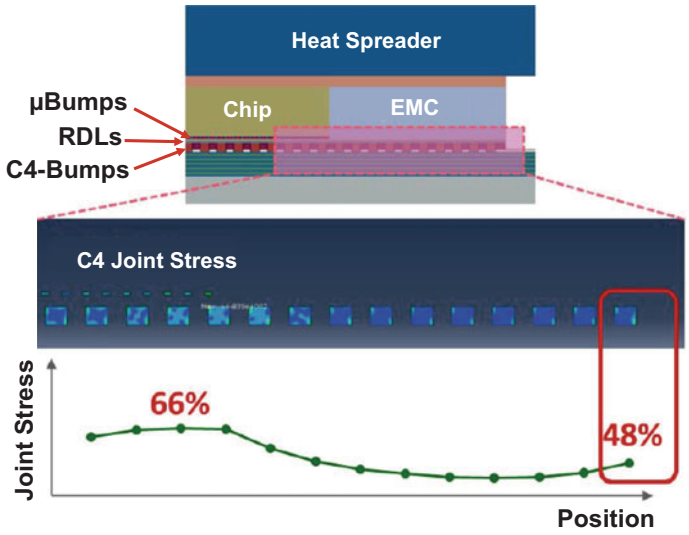


Fig. 6.13 Modelling and results of Samsung's Si-less RDL interposer

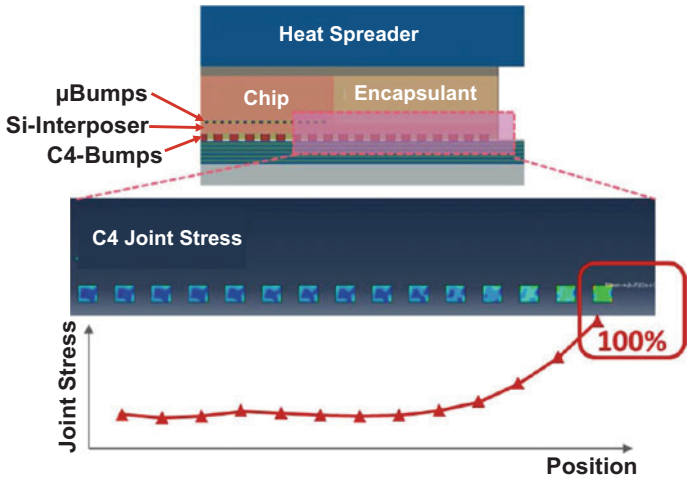


Fig. 6.14 Modelling and results of conventional CoWoS

mum stress location is different. For the Si-less RDL interposer, the maximum stress occurs near the chip corner. On the other hand, for the conventional CoWoS, the maximum stress occurs near the TSV-interposer corner [27].

6.7 Summary and Recommendations

Some important results and recommendations are summarized as follows:

- TSV-less interposers such as fan-out substrates are very effective ways to make RDLs for heterogeneous integrations. It is not only less process step but potentially lower cost than those of heterogeneous integrations on TSV-interposers.
- The heterogeneous integrations (of a SoC and a memory) on fan-out RDL substrates made by the chip-first formation such as the FOCoS by ASE have been in small volume production.
- The heterogeneous integrations on fan-out RDL substrates made by the chip-last formation are finding their ways into volume production.
- The size of the heterogeneous integrations on fan-out RDL substrates made by the chip-first formation is usually smaller than that by the chip-last formation.
- The metal line width and spacing of RDLs of heterogeneous integrations on fan-out substrates made by the chip-first formation are usually larger than those made by the chip-last formation.

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Chapter 7
Heterogeneous Integration of PoP



7.1 Introduction

PoP (package-on-package) [1–21] is one of the heterogeneous integrations. It integrates more than one chip into a PoP format. In the past 10 years, PoP has been used to house the application processor (AP) and memory for mobile applications.

7.2 Wirebonding PoP

Figure 7.1a shows the schematic of an example of wirebonding PoP. It consists of the stacking of the top package that houses two chips cross-stacked and wirebonded on a package substrate, and the bottom package that houses one chip wirebonded on another package substrate. All these chips are over molded and all these substrates are with solder balls.

7.3 Flip Chip PoP

Figure 7.1b shows the schematic of an example of flip chip PoP. It consists of the stacking of two identical solder bumped flip chip on substrate packages. All these flip chips are with underfill and all the substrates are with solder balls.

7.4 Wirebonding Package on Flip Chip Package

Figure 7.2 schematically shows the cross-section of a wirebonding package on flip chip package. It can be seen that the top package houses the wirebonding chips and

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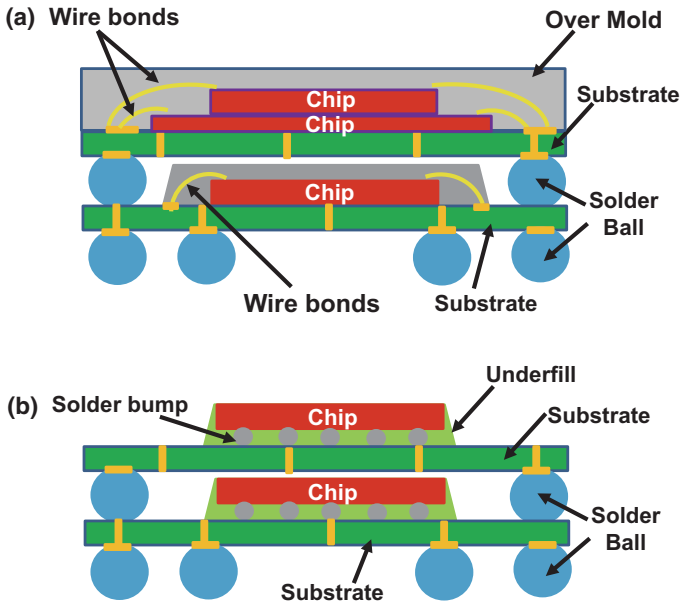


Fig. 7.1 PoP. **a** Wirebonding PoP. **b** Flip chip PoP

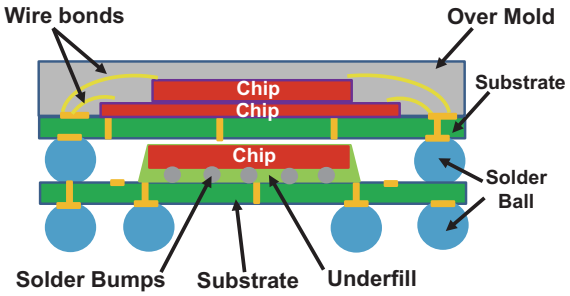


Fig. 7.2 PoP. Wirebonding package on flip chip package

the bottom package houses the flip chip. A real example is shown in Fig. 7.3 which is the cross-section of iPhone 5s.

7.5 PoP in iPhone 5s

iPhone 5s is one of the high-end smartphones. Figure 7.3 shows the AP chipset in a PoP inside iPhone 5s. It can be seen from the schematic cross-section that the top package houses the Elpida (now Micron)'s 1 GB LPDDR3 (low-power double data rate type-3) mobile RAM (random access memory) chips (~11 mm × 7.8 mm),

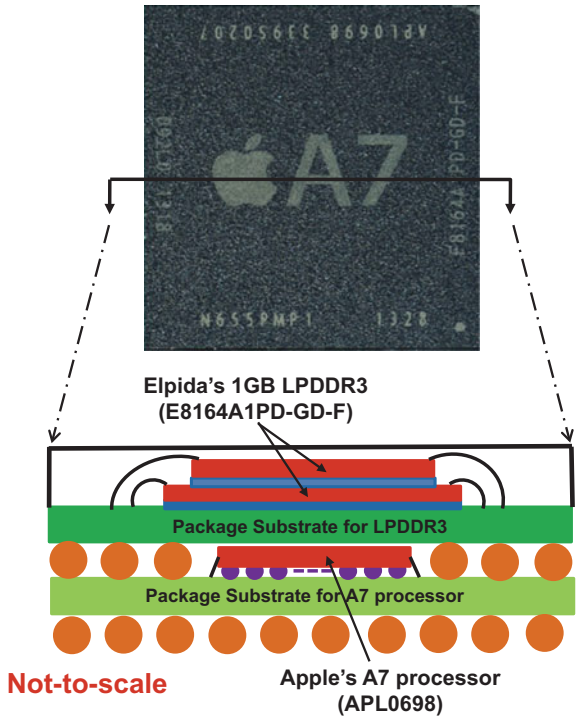


Fig. 7.3 Top-view and cross-sectional view of the PoP (for mobile DRAM and application processor A7) inside iPhone 5s

which are cross-stacked and wirebonded on a coreless FBGA (fine-pitch ball grid array) package substrate and then over-molded. There are three rows (456) solder balls on the FBGA (Fig. 7.4). The bottom package houses the 64-bit A7 processor chip (~10 mm × 10 mm), which is solder-bumped flip chip on a build-up package substrate with 38 × 34 = 1292 solder balls. Figure 7.5 shows the cross-section of the package substrate that supports the AP A7. It can be seen that it is a 2-2-2 (two core layers and two build-up layers on its top side and bottom side) simple substrate with two 0201 and one 0402 embedded passives. The pad pitch for the C4 (controlled-collapse chip connection) bumped AP A7 chip is ~200 μm and for the ball grid array solder ball is ~400 μm.

7.6 Amkor/Qualcomm/Shinko's PoP

High-bonding force thermocompression of the Cu-pillar + solder cap bumps with nonconductive paste (TC-NCP) underfill on the substrate was first studied by Amkor [4] and has been used to assemble Qualcomm's SNAPDRAGON AP for Samsung's Galaxy smartphone for the bottom package of a PoP as shown in Fig. 7.6. The NCP underfills can be spun on, dispensed by a needle, or vacuum assisted. The molded

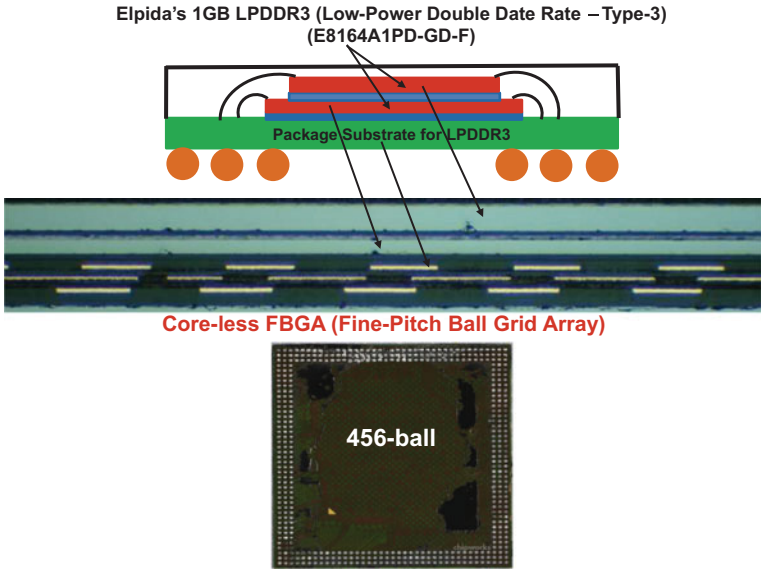


Fig. 7.4 The mobile DRAMs in the top package of the PoP inside iPhone 5s

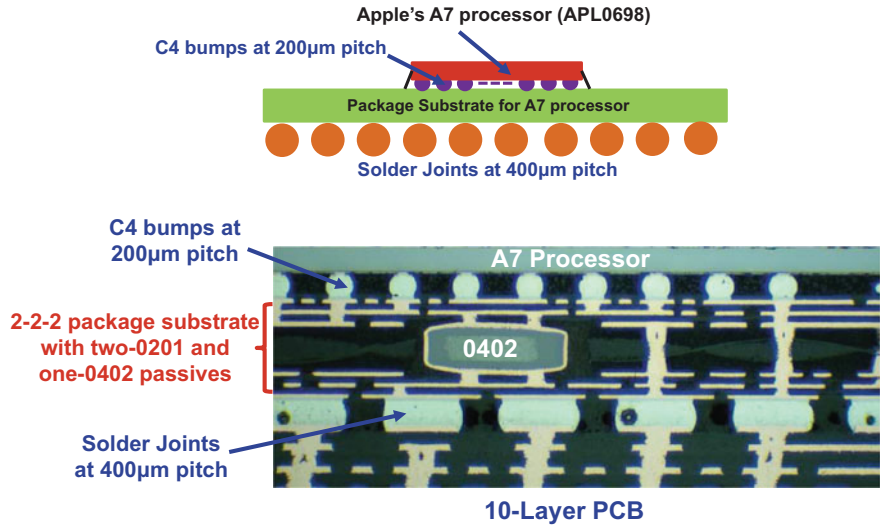


Fig. 7.5 The application processor A7 is flipped chip on the bottom package of the PoP

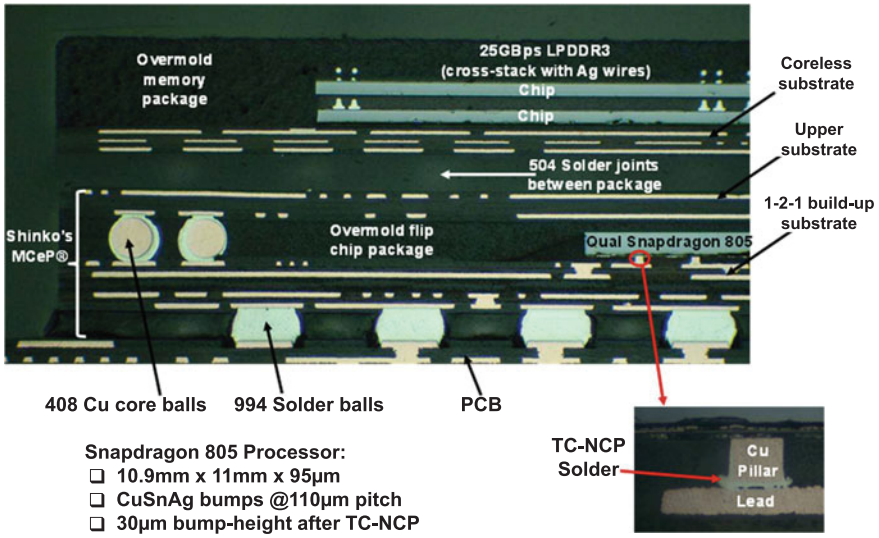


Fig. 7.6 Amkor/Qualcomm/Shinko's PoP for Samsung's AP chipset

core embedded package (MCeP) substrate was manufactured by Shinko (Fig. 7.7). It can be seen that the Cu core balls provide the standoff for the AP. The assembly process is shown in Fig. 7.8. First, the MCeP substrate is prebaked to remove volatile compounds and moisture. The NCP is pre-dispensed and then TC bonding using a proper heating profile and compression.

7.7 Apple's PoP with Solder Bumped Flip Chip

Figure 7.9 shows the cross section of an iPhone 6 Plus. It can be seen that the AP A9 is housed in the bottom package of a PoP format and the C4 solder bumped flip chip is mass reflowed on a 2-2-2 organic build-up package substrate with underfill. The upper package is housing the LPDDR4 (low power double data rate type 4) memory.

7.8 STATSChipPac's PoP for AP

In order to get a lower profile package than the PoP shown in Figs. 7.3, 7.4, 7.5, 7.6, 7.7, 7.8 and 7.9, Fig. 7.10 shows the cross-section SEM images of a 3D eWLB [6] proposed by STATSChipPac. It consists of a bottom package, which is an eWLB (i.e., to replace the solder bumped flip chip package of Figs. 7.3, 7.4, 7.5, 7.6, 7.7, 7.8 and 7.9), and a top package, which is a memory package. It can be seen that: (a)

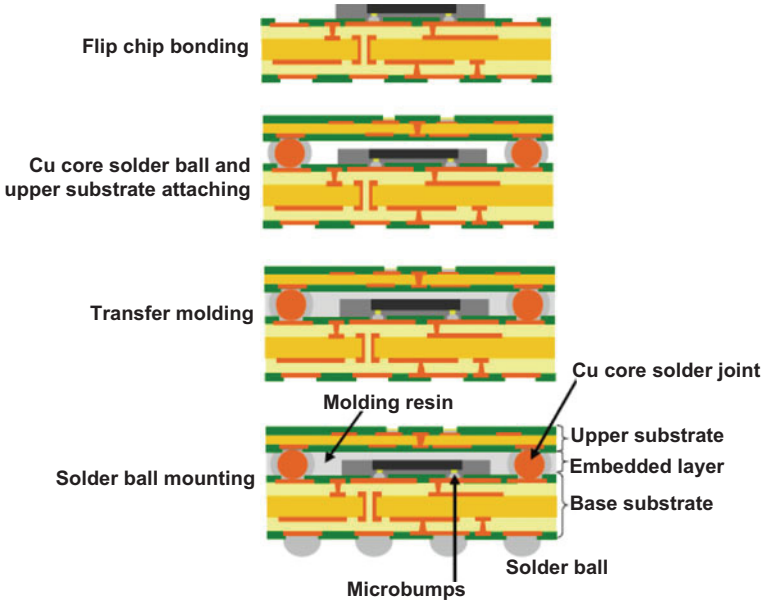


Fig. 7.7 Shinko's MCeP (molded core embedded package)

the eWLB is only 450 μm thick, (b) the eWLB houses an application processor, (c) the top package is 520 μm thick and it houses the memory chips with wirebonding, and (d) the interconnection is from the PCB, solder balls, RDLs, to processor, and solder balls, RDL, to the memory chips.

7.9 3D Infineon's eWLB on eWLB

Figure 7.11 shows Infineon's eWLB on eWLB [10, 11]. The vertical interconnects between the eWLBs are through the solder joints and TEVs (through encapsulant vias). The TEV is made by laser drilling through the molding compound. The adhesion layer is Ti, which is made by sputtering. It is followed by a thin sputtered copper layer as plating base and an electrode for the electrochemical deposition of Cu. The cross-sections and SEM images are shown in Fig. 7.11. It can be seen that the TEV is not filled. The TEV diameter is 150 μm and the plated Cu thickness ranges from 15 to 30 μm.

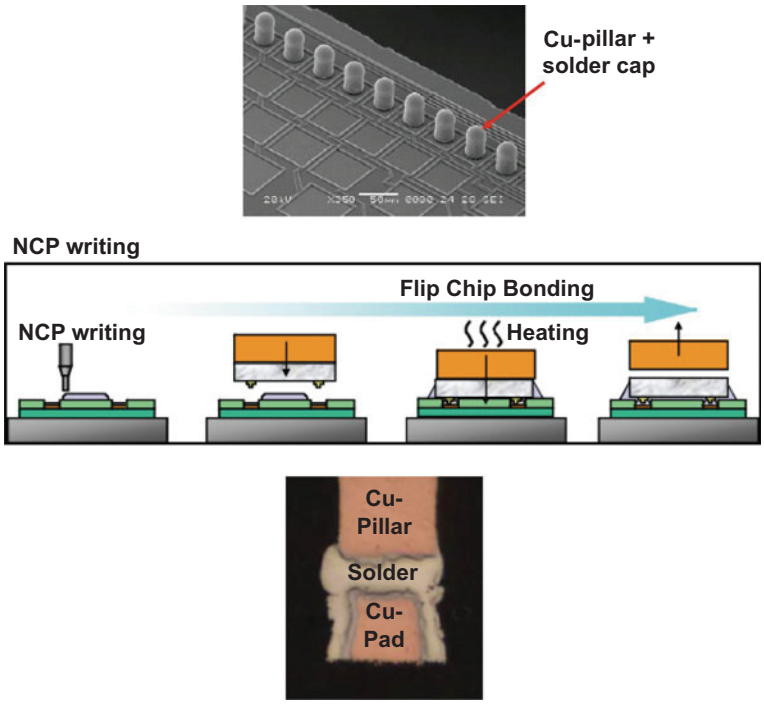


Fig. 7.8 Amkor's key process steps for TC-NCP

7.10 TSMC/Apple's PoP for AP

7.10.1 TSMC/Apple's PoP for AP A10

During September 2016, TSMC put the AP chipset with their InFO-PoP technology into HVM-the very first in the world [12]. Figure 7.12 shows the schematic and the SEM images of the cross sections of the PoP for the AP (A10) chipset by InFO-WLP technology manufactured by TSMC. It can be seen that (1) the dimensions of the A10 are 11.6 mm × 10.8 mm × 150 μm, (2) the package dimensions are 15.5 mm × 14.4 mm × 825 μm, (3) the package/chip ratio = 1.8, (4) there are 3 RDLs, (4) the TIV (through InFO via) is electroplated with Cu, (5) the mobile DRAMs are wirebonded on a three-layer coreless package substrate, (6) the DRAMs and the wires are over molded, (7) there are 386 solder balls (at 0.3 mm pitch) between the top package and the bottom package, (8) there is underfill between the top and bottom packages, (9) there are ~1300 solder balls (at 200 μm diameter and 0.4 mm pitch) at the bottom package, and (10) there is underfill between the PoP and the PCB (printed circuit board) to resist drop condition.

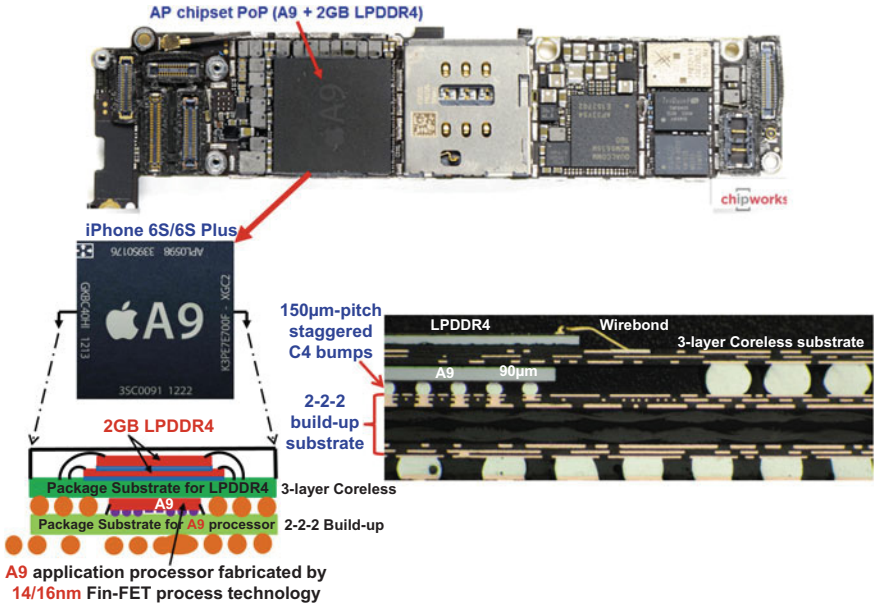


Fig. 7.9 Apple's PoP for their AP A9 with flip chip technology

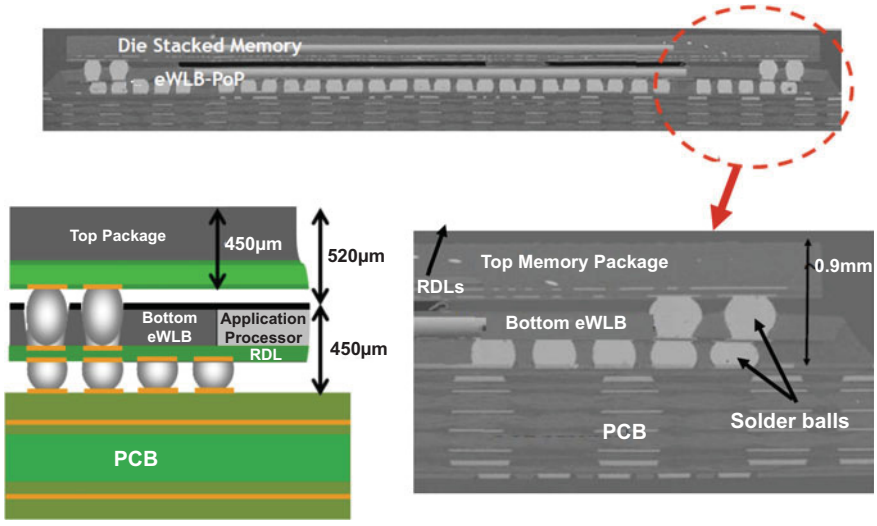


Fig. 7.10 STATSChipPac's PoP for AP chipset with eWLB

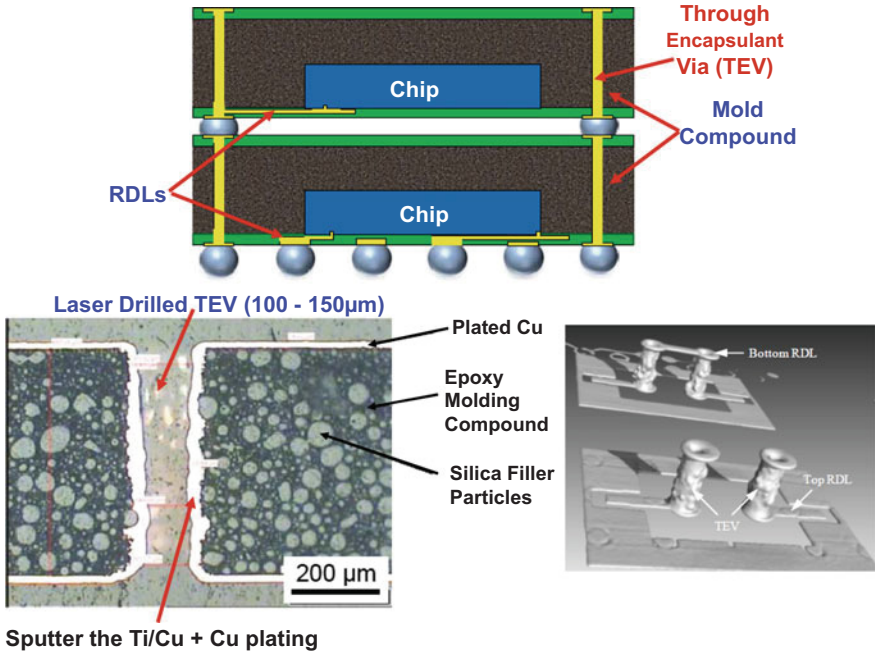


Fig. 7.11 Infineon's PoP with eWLB on eWLB

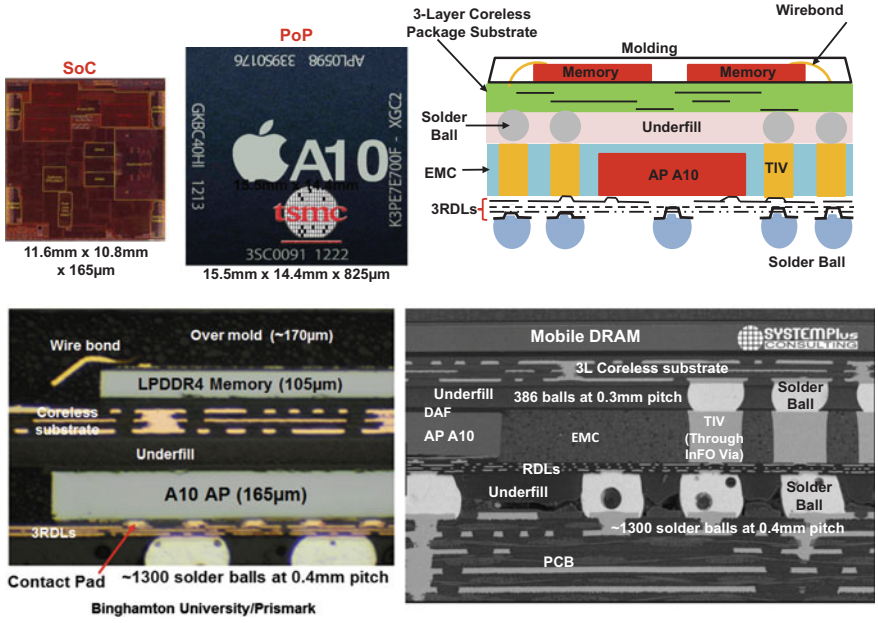


Fig. 7.12 TSMC/Apple's PoP for their AP A10 with InFO-WLP

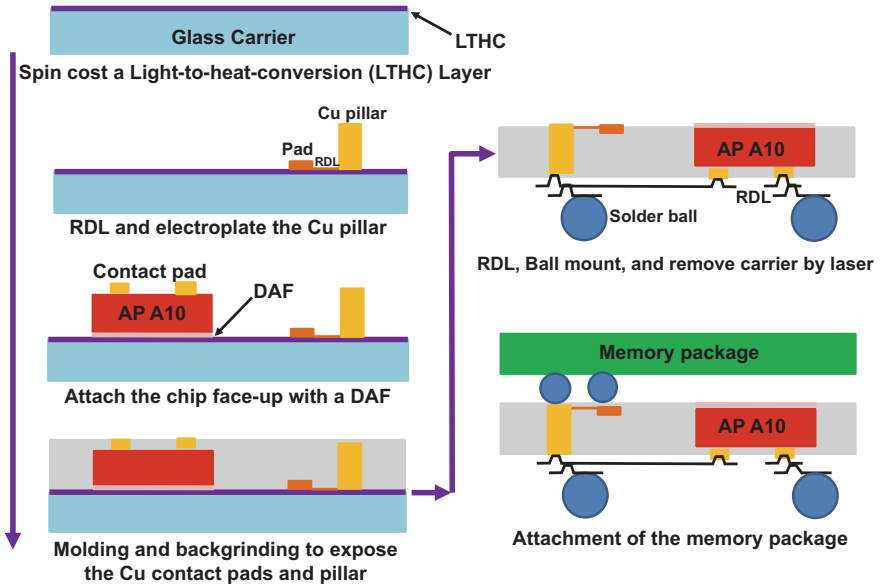


Fig. 7.13 TSMC key process step in making the PoP

The key process steps are shown in Fig. 7.13. First, spin coat a very thin LTHC (light-to-heat-conversion) layer on a glass wafer. Then, build a RDL (redistribution layer), contact pads, and Cu pillars by electroplating. Attach the KGDs (A10) face-up with DAF and Cu contact-pad on the carrier. It is followed by compression molding of an EMC + post mold cure. Then, backgrind the EMC to expose the Cu contact-pad and Cu-pillars. It is followed by removing the wafer carrier, building the RDLs, and mounting the solder balls. Finally, dice the reconstituted wafer into individual packages.

7.10.2 TSMC/Apple's PoP for AP A11

Figure 7.14 shows the schematic and SEM images of the PoP for the AP (A11) chipset by InFO-WLP technology HVM by TSMC during September 2017. Basically, the PoP for both APs (A10 and A11) is very similar. However, because TSMC used 10 nm process technology to fabricate the A11 (instead of the 16 nm process technology for the A10), the chip dimensions are much smaller (10 mm × 8.7 mm × 150 μm), ~30% chip area reduction from A10. Since the dimensions of the new package do not change much (13.9 mm × 14.8 mm), only ~8% package area reduction from the old one, thus the package/chip ratio of A11 increases from 1.8 to 2.3. Also, the number of RDLs increases from 3 to 4. The line width and spacing of those 4 RDL are 10 μm.

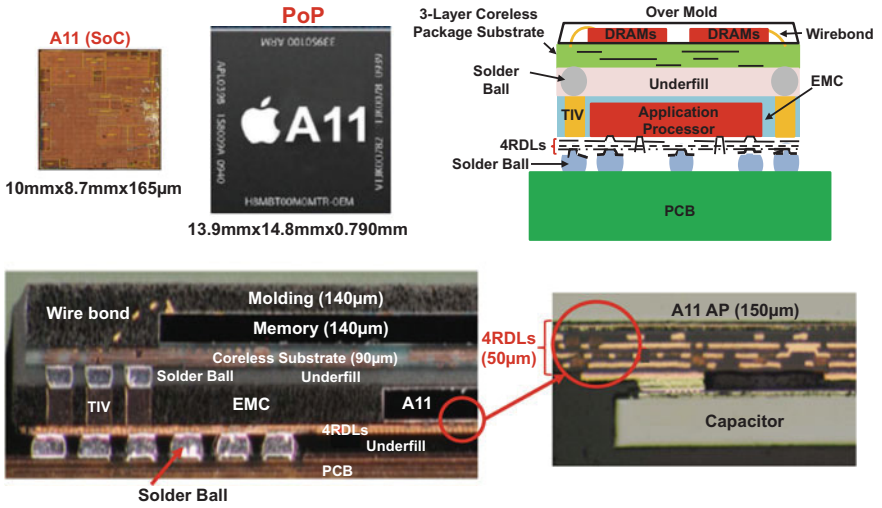


Fig. 7.14 TSMC/Apple's PoP for their AP A11 with InFO-WLP

7.10.3 TSMC/Apple's PoP for AP A12

Figure 7.15 shows the schematic and SEM images of the PoP for the AP (A12) chipset by InFO-WLP technology HVM by TSMC during October 2018. Basically, the PoP for all the APs (A10, A11, and A12) is very similar. However, because TSMC used 7 nm process technology to fabricate the A12, the chip dimensions are slightly smaller than that of A11 even more functions such as the artificial intelligence are included. In order to have a better electrical performance there are a few IPDs (integrated passive devices) which are solder bumped flip chip at the bottom of the fan-out package as shown in Fig. 7.15. There are 4 RDLs and the minimum metal line width and spacing are 8 μm.

7.11 Samsung's Smartwatch PoP

Figure 7.16 shows Samsung's smartwatch in a PoP format shipped in the summer of 2018. The upper package is housing the memory ePoP (embedded package-on-package) which consists of 2DRAM, 2NAND flash, and 1NAND-controller. These memories are wirebonding on a 3-layer coreless package substrate, as shown in Fig. 7.17. The dimensions of the upper package are 8 mm × 9.5 mm × 1 mm. The bottom package is housing the AP and PMIC (power management IC) side-by-side by their fan-out panel level packaging technology, as shown in Fig. 7.18. The chip size of the AP and PMIC is about 3 mm × 3 mm. The key process steps are shown

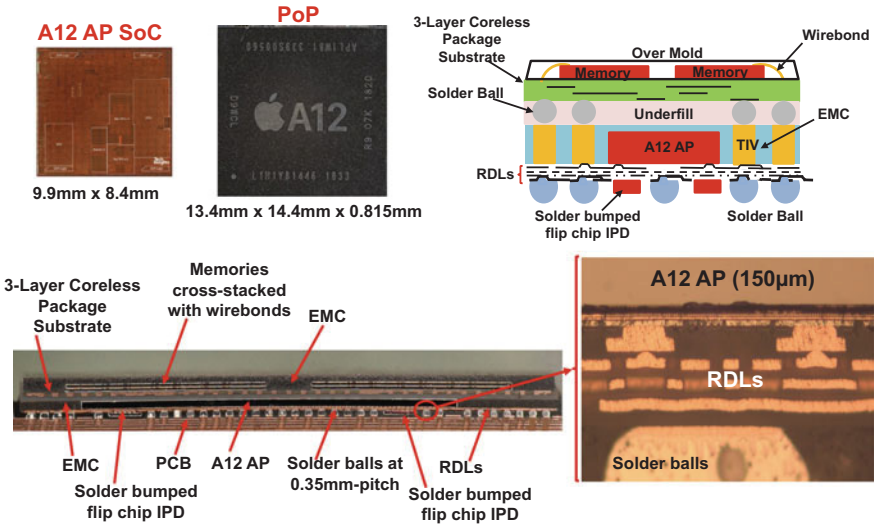


Fig. 7.15 TSMC/Apple's PoP for their AP A12 with InFO-WLP

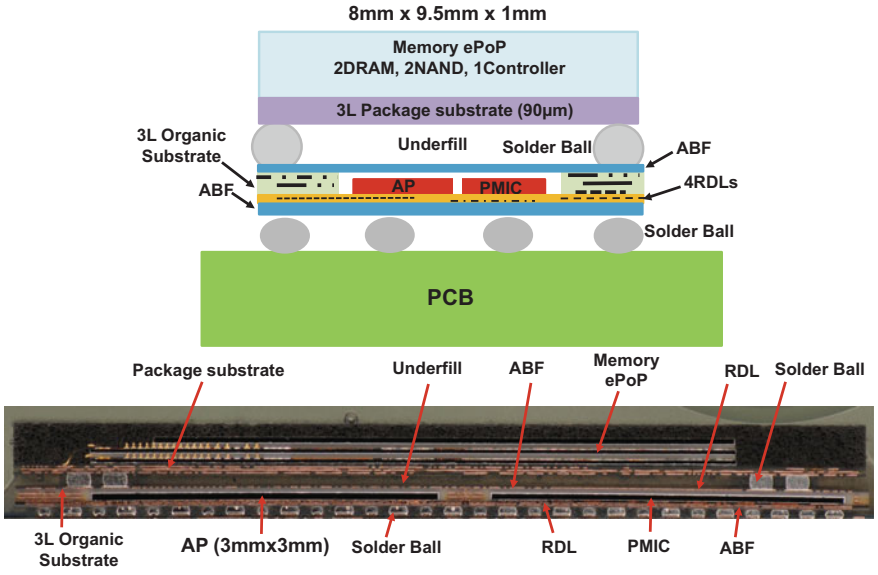


Fig. 7.16 Samsung's PoP for their smartwatch with their FOPLP

in Fig. 7.19 [15]. First, make a cavity on a PCB. Then, place the chips on the cavity and laminate an EMC (epoxy molding compound). It is followed by attaching to a carrier, making the RDLs, and mounting the solder balls.

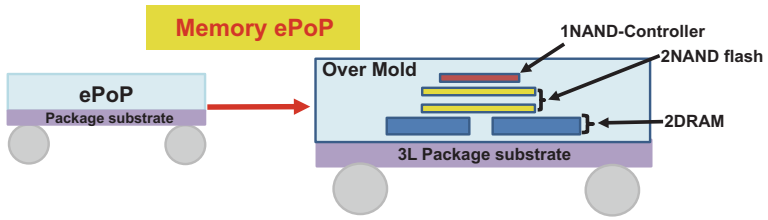


Fig. 7.17 Samsung memory ePoP

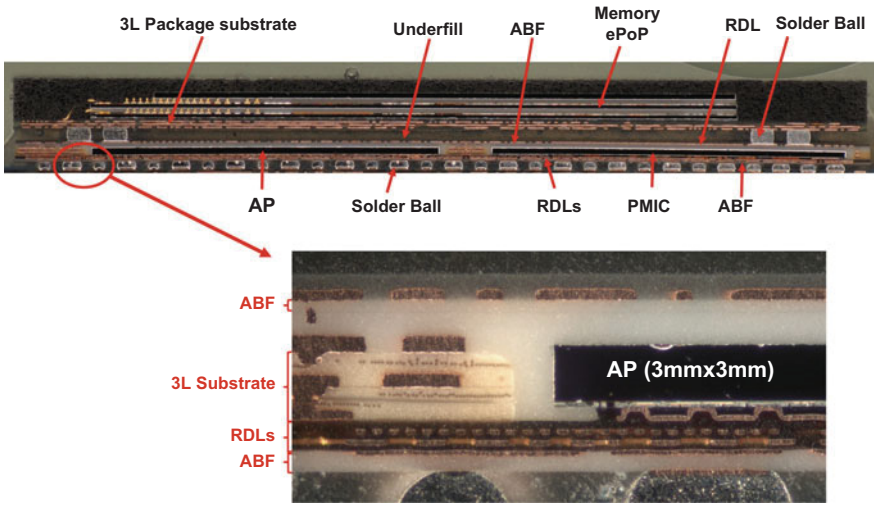


Fig. 7.18 PoP cross section of Samsung's smartwatch

7.12 Summary and Recommendations

Some important results and recommendations are summarized as follows.

- PoPs are one of the heterogeneous integrations.
- PoPs have been used to house the application chipsets (application processor + memory) for tablets, smartphones smartwatches, etc.
- The key interconnect of PoPs is the connection between the upper package and the bottom package. For examples, Amkor use TMV (through mold via) [22], STATSChipPac use solder ball [6], Infineon use TEV (through encapsulant via) [10, 11], TSMC use TIV (through InFO via) [12], and Invensas use BVA (Bond Via Array) [23].

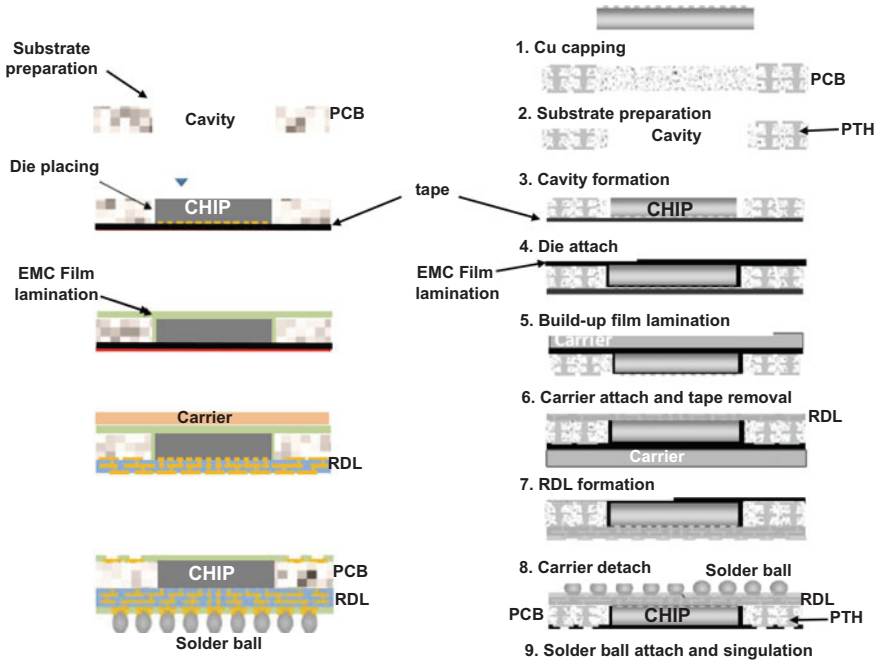


Fig. 7.19 Key process steps for Samsung's FOPLP

- Fan-out wafer-level packaging has been used by TSMC's InFO to house the application chipsets of the PoP for Apple's tablets and iPhones.
- Fan-out panel-level packaging has been used by Samsung's FOPLP to house the application chipsets of the PoP for their smartwatches.

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Chapter 8
Heterogeneous Integration of Memory Stacks



8.1 Introduction

The first paper on stacking of memory chips in 3D by die-attach material and wire bonding was published by nCHIP [1] 25 years ago, Fig. 8.1. Since then, memory chips (especially the NAND Flash) stacking by wire bonding have been in high volume production for, e.g., the smartphones, tablets, and solid state drives as shown in Figs. 8.2 and 8.3 by Samsung. It can be seen that 16 48-layer V-NAND 3D flash memory chips are stacked by wirebonding technology. The thickness of each chip is only 40 μm. These are the homogeneous integration of memory stacks.

Figure 8.4 shows a heterogeneous integration of memory stack (memory + ASIC) with die-attach material and wire bonding. Recently, there are many applications of this kind of structure. In the first part of this chapter, heterogeneous integration of two memory chips stacked on one ASIC will be presented.

In order to increase the bandwidth, density, and performance, the memory chips are stacked through microbumps and TSVs (through-silicon vias). Samsung mass-produced (August 2014) the industry's first TSV-based 64 GB double data rate type-4

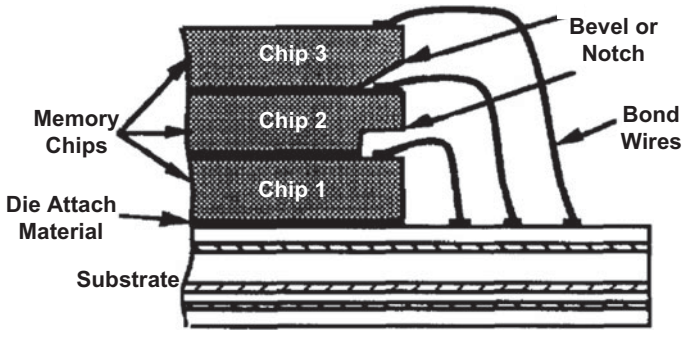


Fig. 8.1 Memory chips stacking by die attach and wire bonding

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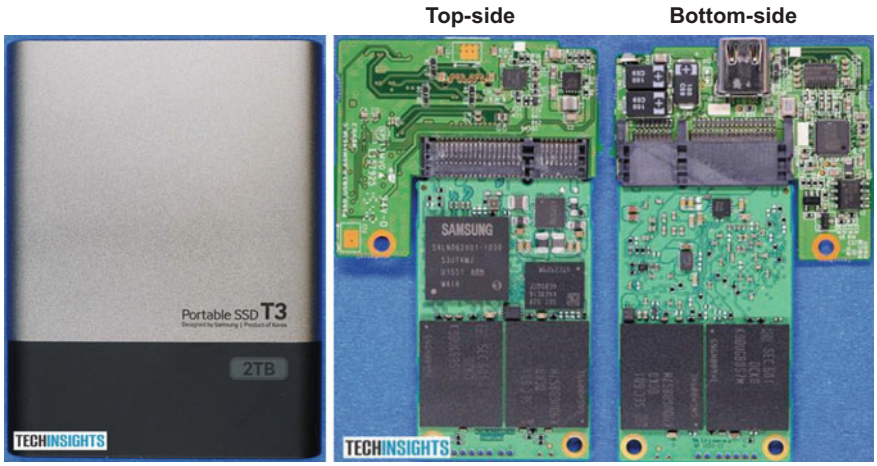


Fig. 8.2 Samsung's 48-layer V-NAND 3D flash memory in a solid state drives (SSD)

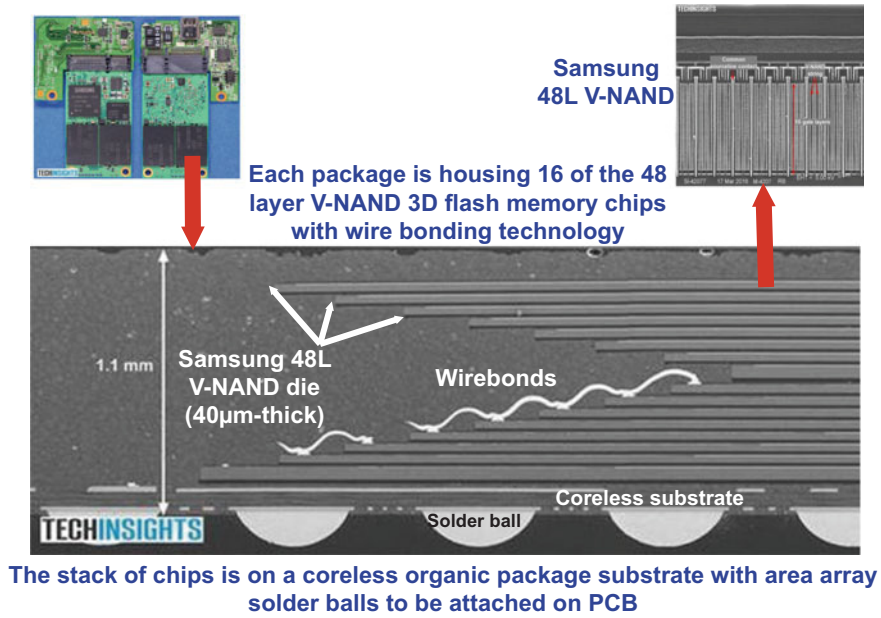


Fig. 8.3 16 Stacking of Samsung 48L V-NAND dies

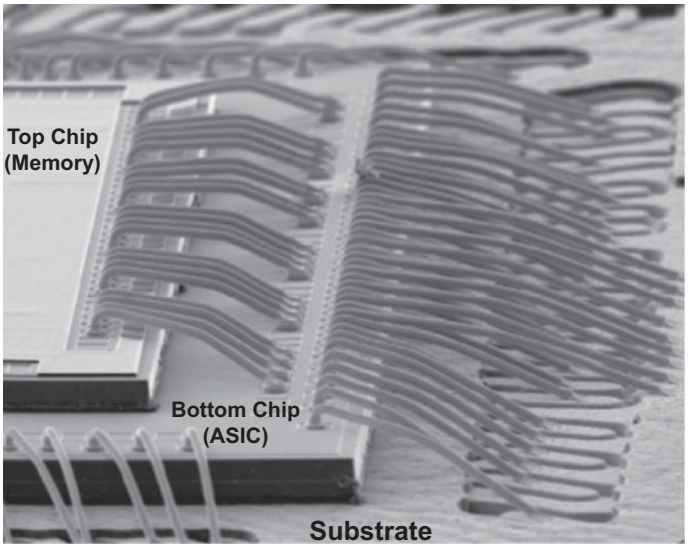


Fig. 8.4 Heterogeneous integration of chips with wirebonds

(DDR4) DRAM stack module (Fig. 8.5). Each stack has 4 DRAMs, each DRAM die has 78 TSVs, and the 64 GB DDR4 DRAM stacks are on a printed circuit board (PCB). The module performs twice as fast as a module that uses wire bonding packaging technology, while consuming approximately half the power. The module is for environmentally friendly server applications. On November 26, 2015, Samsung started to produce the 128 GB registered dual inline memory module (RDIMM). This is the homogeneous integration of memory stack.

Figure 8.6 shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28 nm process technology and is supported by four high-bandwidth memory (HBM) cubes manufactured by Hynix with 128 GB/s bandwidth. Each HBM consists of four DRAMs with C2 bumps and a logic base with TSVs straight through them. This is heterogeneous integration of memory chips and logic chip. Each DRAM chip has >1000 TSVs and 2 Gb density at 1Gbps speed per pin. The GPU and HBM cubes are on top of a TSV interposer (28 mm $\times$ 35 mm), which is fabricated by UMC with a 64 nm process technology. The final assembly of the TSV interposer (with C4 bumps) on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

Figure 8.7 shows NVidia's Pascal 100 GPU, which shipped in the second-half of 2016. The GPU is built on TSMC's 16 nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung with 256 GB/s bandwidth. Each HBM2 consists of four DRAMs with C2 bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs and 8 Gb density at 2 Gbps speed per pin. The GPU and HBM2 s are on top of a TSV interposer (1200 mm^2), which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached

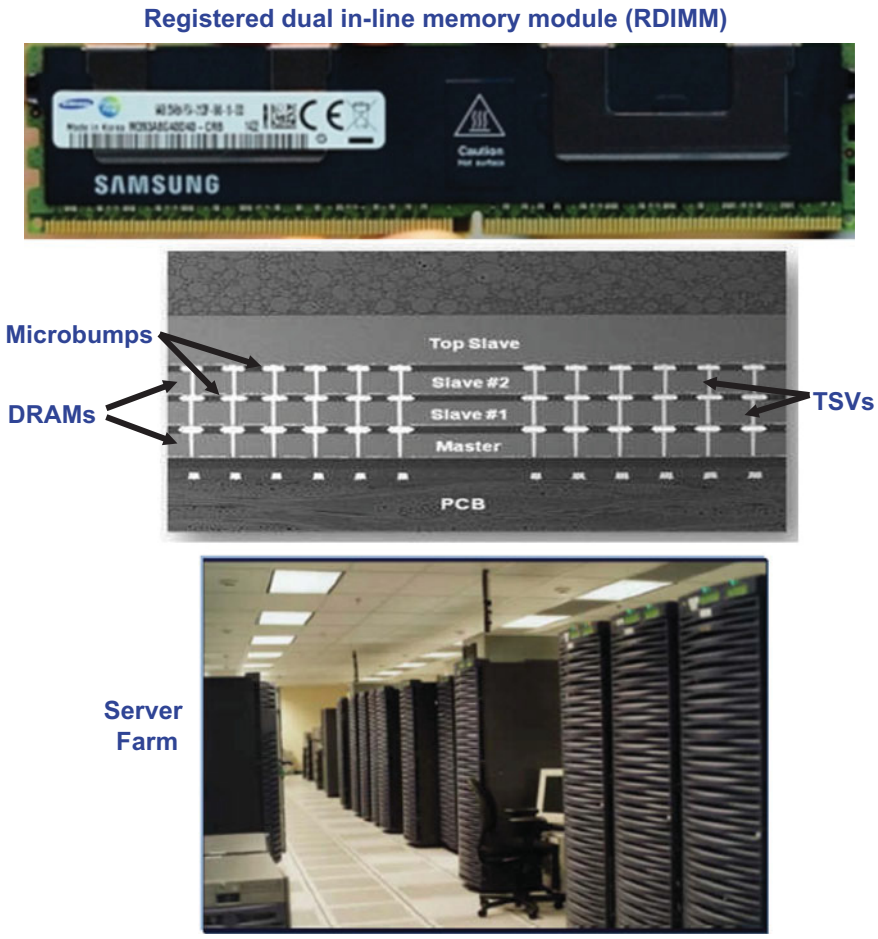


Fig. 8.5 Samsung mass-produces industry's first TSV-based DDR4 DRAM for server farms

to a 5-2-5 organic package substrate with C4 bumps. Again, this is heterogeneous integration of memory chips and logic chip.

Both Samsung and Hynix use the high-bonding force TCB (thermocompression bonding) of the microbumped DRAMs and logic with NCF (non-conductive film) as shown in Fig. 24d of [2] to fabricate the 3D heterogeneous integration stack. This 3D memory cube is stacked one chip at a time (Fig. 8.8) and each chip takes ~10 s for the underfill film to gel, the solder to melt, the underfill film to cure, and the solder to solidify. Throughput is a problem!

In order to resolve this problem, Toray [3, 4] proposed a collective bonding method which is shown in Fig. 8.9. It can be seen that the microbumped chip with NCF is pre-bond (bond force = 30 N, temperature = 150 °C, and time <1 s) on a stage with temperature = 80 °C. For post-bond (first step (3 s): bond-force = 50 N, temperature

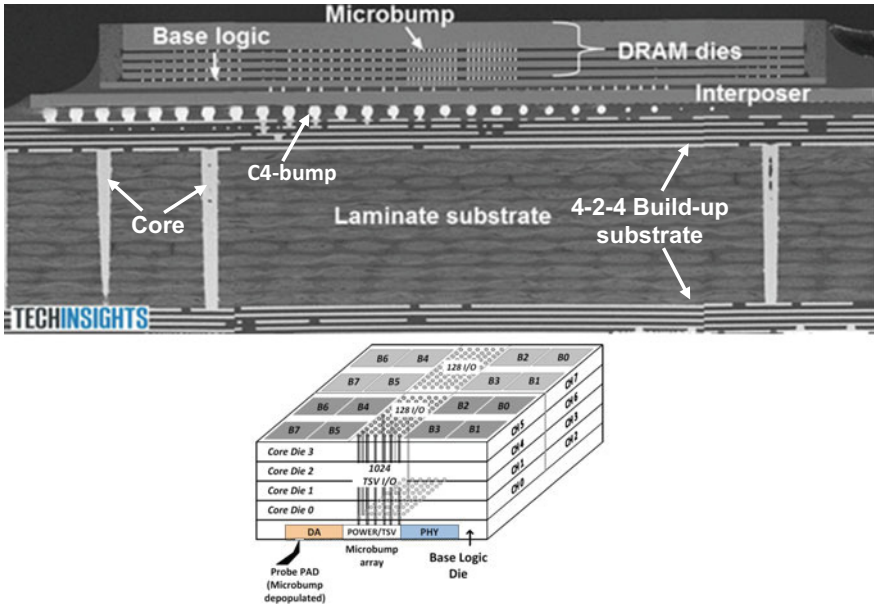


Fig. 8.6 AMD's graph card made by Hynix's HBM, which is TCB of the NCF DRAM chips one by one

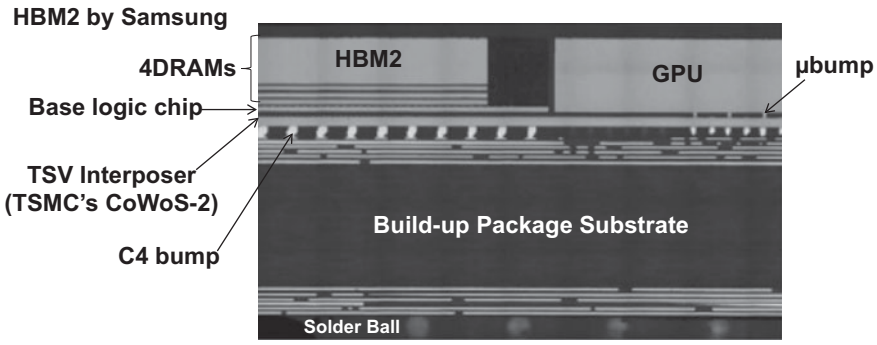


Fig. 8.7 NVidia's graph card made by Samsung's HBM2, which is TCB of the NCF DRAM chips one by one

= 220–260 °C, second step (7 s): bond-force = 70 N, temperature = 280 °C) on a stage temperature = 80 °C. Thus, instead of using 40 s in stacking up four chips by the conventional method, it only takes less than 14 s by the collective method. Some images of the cross section of the proposed collective bonding method are shown in Fig. 8.9. Reasonable good joints are achieved with optimized conditions.

In the second part of this chapter, the heterogeneous integration of memory chips and logic chip with low-temperature bonding will be presented. After aligning and

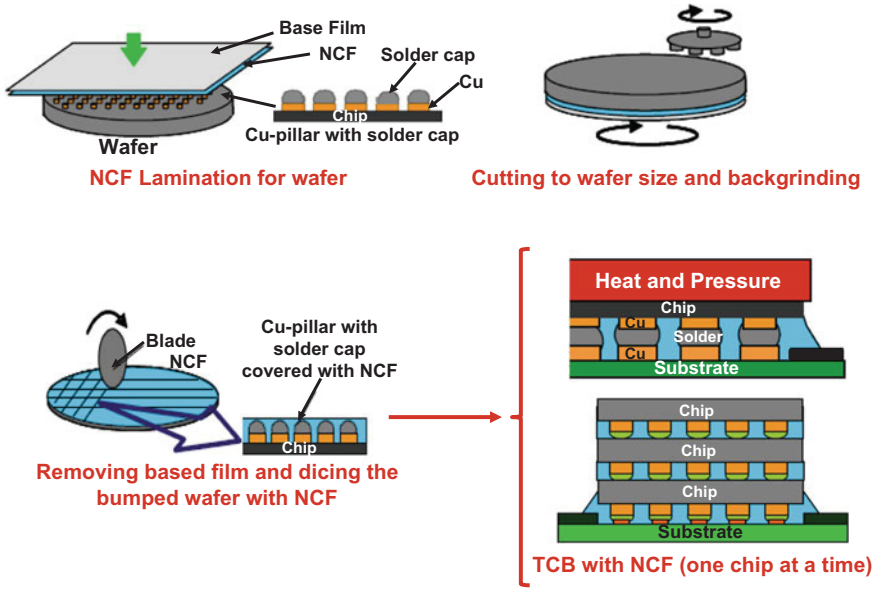


Fig. 8.8 Lamination of NCF on a Cu-pillar/solder-cap bumped wafer, dicing, and TCB of NCF flip chips one by one

bonding at a temperature of less than 200 °C, all the solders will react with the UBM (under bump metallurgy) on the chips/wafers and become IMCs (intermetallic compounds) with melting points that are a couple of hundred degrees higher than that of the solders. This feature is welcome by 3D IC chip stacking. For example, after bonding the first two chips at a low temperature, all the bonding interconnects are converted into IMC with a much higher remelting temperature. When the third chip is bonded on top of these two chips with the low temperature, the interconnects (IMC) between those two chips will not be reflowed and moved.

8.2 Wire Bonding of Stack Dies (Memories) on Cu–Low-*K* Chip

8.2.1 Test Vehicles

Figure 8.10 shows the two test vehicles. For both test vehicles, the bottom chip is a 65 nm Cu–low-*k* die that is die-attached to an organic substrate. This Cu–low-*k* die supports (1) two daughter chips with a wire-embedded film (WEF) between them, as shown in Fig. 8.10a, test vehicle-1 (TV1), and (2) two daughter chips with a die-attach film (DAF) between them, as shown in Fig. 8.10b, test vehicle-2 (TV2).

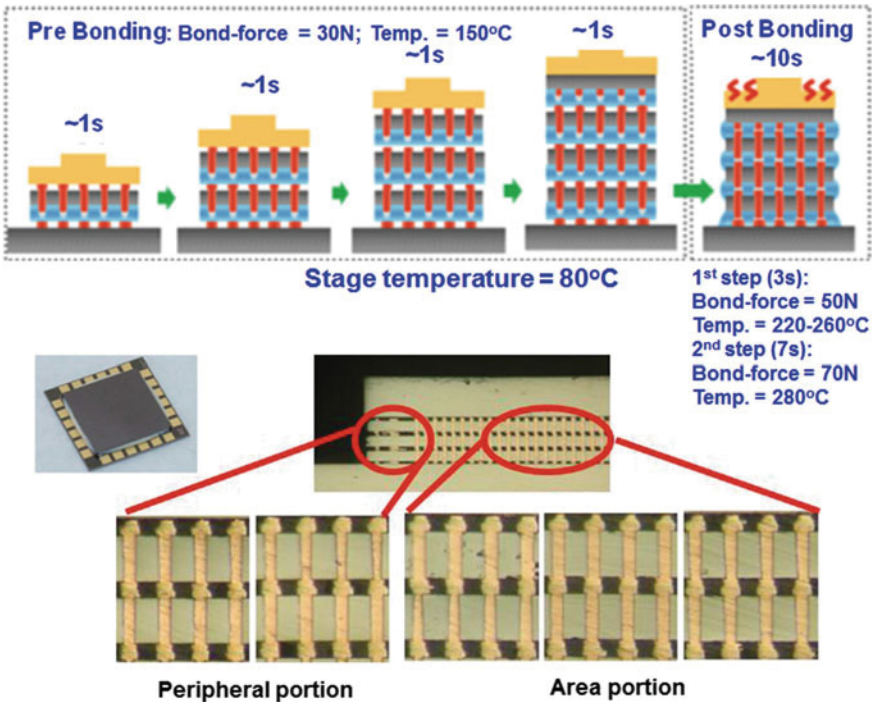


Fig. 8.9 Toray's collective TCB with high-force with NCF flip chips

For both test vehicles, (1) the DAF is used between the bottom daughter die and the Cu–low-*k* die, and (2) a die-attach paste is used between the Cu–low-*k* die and the substrate.

The 65 nm Cu–low-*k* die has six metal layers with 408 input/output pins (I/Os) and is 7 mm × 7 mm in size. Its thickness is 0.3 mm. The daughter die dimension is 3 mm × 5 mm × 0.075 mm. The organic substrate used is two metal layers with a plastic ball-grid-array (PBGA) substrate. The final package dimension is 17 mm × 17 mm × 1.1 mm. The substrate and mold compounds are of green materials in line with environmental legislation.

*8.2.2 Stresses at the Cu–Low-*k *Pads*

The inferior mechanical properties of the Cu–low-*k* material complicate the packaging process in terms of low-*k* peeling during the dicing process, bond-pad cratering after wire bonding, and delamination of the passivation layer during reliability tests [5–7]. Common failure patterns encountered when dicing low-*k* wafers include metal/interlayer dielectric (ILD) delamination, metal/ILD peeling, and discoloration

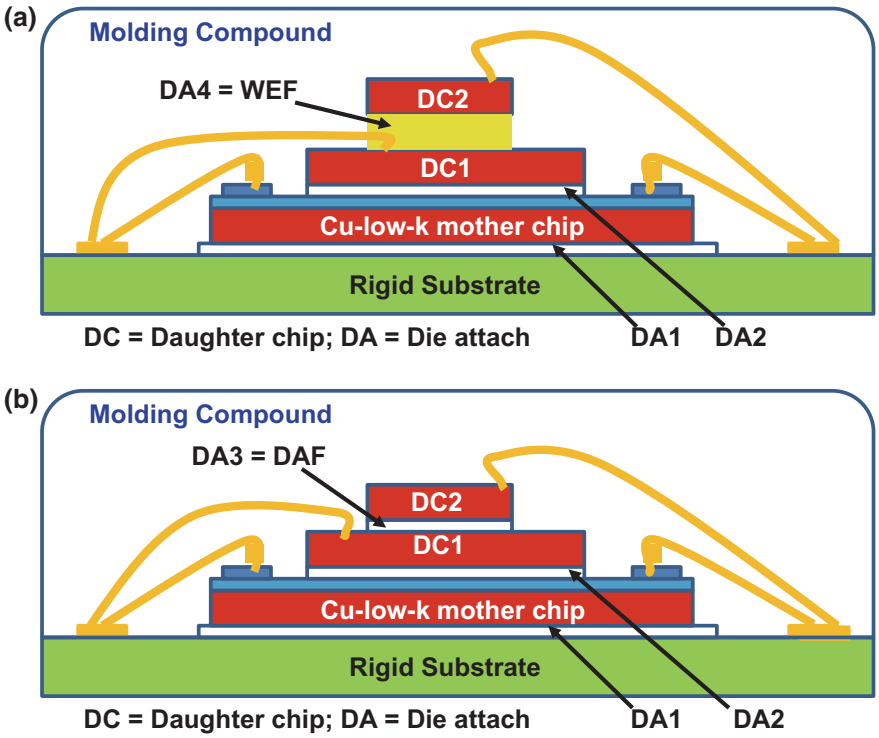


Fig. 8.10 Schematic diagram of a 65 nm Cu–low-*k* stack die package: **a** test vehicle 1 (TV1) using wire-embedded film (WEF), **b** test vehicle 2 (TV2) using die-attach film (DAF) for two daughter chips that are placed at right angles to each other

of the metal layer [8–15]. Under the Cu–low-*k* packaging program, the Institute of Microelectronics, Singapore, has developed polymer encapsulated dicing-lane (PEDL) technology [8, 16] to address the dicing challenges of Cu–low-*k* packaging and simultaneously improve the reliability of the packages by reducing the corner stress of the Cu–low-*k* die compared with the conventional dicing method.

The local maximum shear-stress concentration is located at the outermost corner of the silicon die. This is due to thermal coefficient of expansion (TCE) mismatch among different materials plus the stress singularity at the corners of the die. The shear stress around the die corner is one of the major contributors to delamination failure between the low-*k* layer and the fluorinated silicate glass (FSG) layer [16]. Results have shown that by chamfering the edge of the silicon die at a 45° angle for 35 μm, the maximum stress can be reduced by 34% or more [16].

The package configuration analyzed is shown in Fig. 8.10b and the materials properties are shown in Table 8.1. PEDL technology, i.e., bevel-cut and benzocyclobutene (BCB) coating is adopted here to reduce the stress in the low-*k* layer as shown in Fig. 8.11. Figure 8.12 shows the finite-element analysis (FEA) results with

Table 8.1 Material properties used in FEA

Materials	CTE (ppm/°C)	*E* (GPa)	Poisson's ratio
BCB	52	3	0.35
Low-*k* (BD)	10	8	0.3
FTEOS	2	105.44	0.3
TEOS	0.57	66	0.18
Silicon	2.7	131	0.28
Cu	17	110	0.34
Mold compound	8.9/40.4 (Tg = 147.8 °C)	20.7 (25 °C) 0.296 (250 °C)	0.3
Die attach paste	50/100 (Tg = 150 °C)	5.9 (25 °C) 0.56 (260 °C)	0.3
DAF	80/170 (Tg = 128 °C)	1.66 (25 °C) 0.037 (200 °C)	0.3
Substrate	15	29	0.3
Solder mask	52	4	0.4

a boundary condition of temperature change of the whole structure from 175 to 25 °C [17]. Figure 8.12a shows the finite element model, Fig. 8.12b shows the shear-stress distributions for the low-*k* layer near die attach 2, whereas Fig. 8.12c shows the shear-stress distributions in low-*k* corner. It is observed that the maximum stresses are almost at the same location for four cases.

Figure 8.13 shows the shear stresses in the low-*k* layer, die-attach layers, and epoxy-mold compound for the three case studies with or without using bevel cut and BCB coating, namely (1) straight cut without BCB; (2) bevel cut without BCB; (3) BCB without bevel cut; and (4) bevel cut with BCB. Since the low-*k* layer is easy to delaminate, the shear stress in the low-*k* layer at two critical locations is closely monitored—one at the low-*k* corner and another near die attach 2. It is found that a bevel cut is effective in reducing the shear stresses at the low-*k* corner. When the base case (i.e., without a bevel cut and without BCB coating) is replaced by the case with a bevel cut and without BCB coating, the shear stress at the low-*k* corner is reduced from 100.90 to 58.68 MPa. When the base case is replaced by the case with a bevel cut and BCB coating, the shear stress at the low-*k* corner is reduced from 100.90 to 23.75 MPa. On the other hand, it is found that the BCB coating is effective in reducing the shear stress in the low-*k* layer near die attach 2. When the base case is replaced by the case with BCB coating and with a bevel cut, the shear stress in the low-*k* layer near die attach 2 is reduced from 32.30 to 11.90 MPa.

In summary, as shown in Fig. 8.13, both a bevel cut and BCB coating have to be presented to reduce the stresses in the overall low-*k* layer. Thus PEDL technology implemented in the package not only reduces the stress at the die corner but also reduces the stress at the low-*k* layer directly under the second-stack die (i.e., daughter die 1).

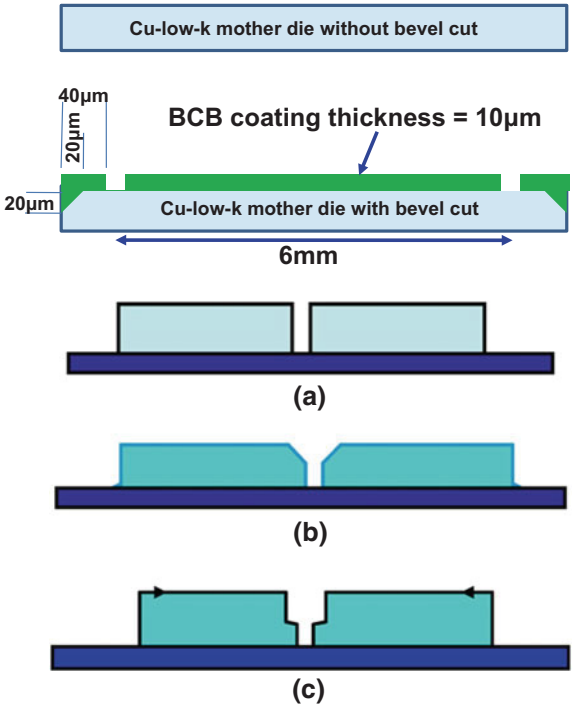


Fig. 8.11 (Top-1) schematic of a stack die without BCB coating and without a bevel cut. (Top-2) schematic of a stack die with BCB coating and with a bevel cut. Different types of cuts: **a** straight; **b** bevel; **c** two-step

8.2.3 Assembly and Process

All 3D heterogeneous integration requires thin wafers and chips. In this study, the Cu–low-*k*-pad wafers are thinned down to 300 µm, and the Al-pad wafers (for the daughter dies) are thinned to 75 µm. All wafers are first thinned by means of coarse mechanical grinding, followed by fine mechanical grinding. In order to remove the microcracks on the backside of the thinned wafers, an additional process (namely, dry polishing) also is needed. The intra-to-inter wafer thickness variation of all the Cu–low-*k*-pad wafers is 2.21 µm total thickness variation (TTV). The TTV for the Al-pad wafers is 2.28 µm.

8.2.4 Evaluation of Dicing Methods

Die singulation is a major process that every individual IC chip goes through. With the trend toward 3D heterogeneous integration and thinner the low-*k* wafers, this singulation process becomes critical. In this study, comparison among (1) straight-cut (Fig. 8.11a), (2) bevel-cut (Fig. 8.11b), and (3) two-step-cut (Fig. 8.11c) wafers

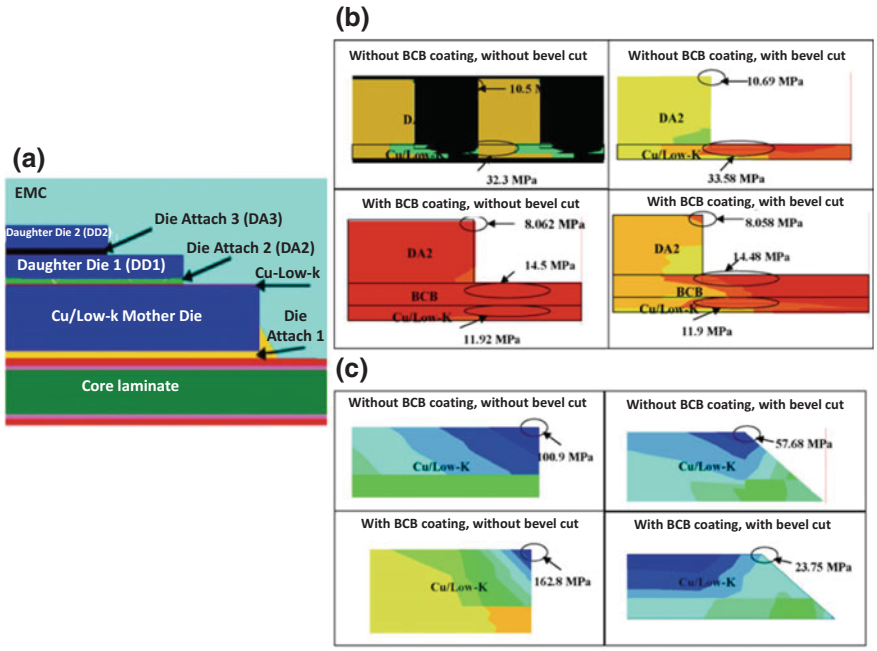


Fig. 8.12 **a** Finite element model. Shear stress distributions **b** for low-*k* layer near die attach 2 (DA2) **c** in low-*k* corner

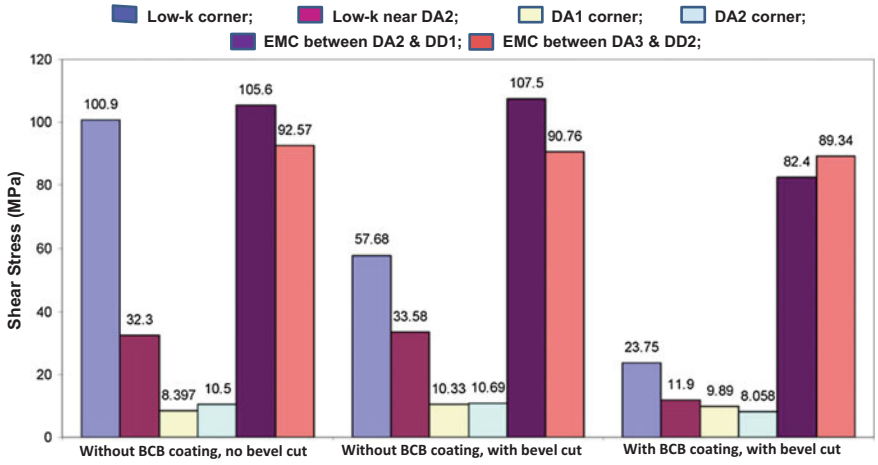


Fig. 8.13 Sheer stresses in the low-*k* layer at the low-*k* corner and near die attach 2 for different cases using BCB coating and a bevel cut

Table 8.2 Dicing parameters for three dicing methods

Dicing method	Parameter	Blade selection	Blade speed (rpm)	Feed speed (mm/s)	Blade height (mm)
Straight cut		27 HCAA	30,000	15	0.06
Bevel cut	Blade 1	2050D-TI	30,000	30	0.115
	Blade 2	HDCC-B	30,000	30	0.06
Two-step cut	Blade 1	27 HCCC	30,000	20	0.1
	Blade 2	27 HAAA	30,000	20	0.06

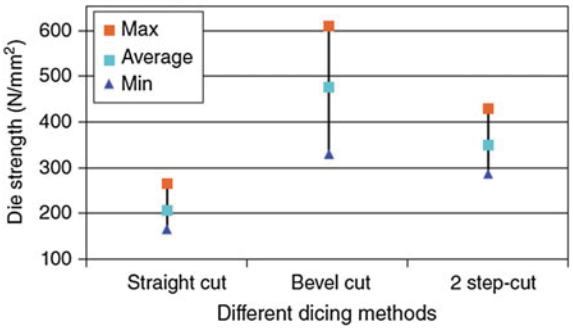


Fig. 8.14 Die strength for 300 μm-thick Cu–low-*k* chips using different dicing methods

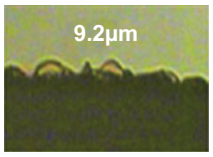
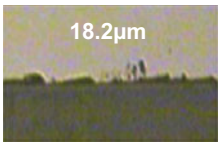
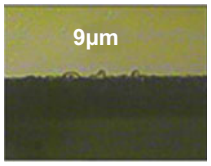
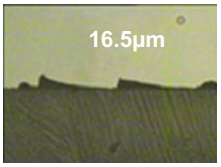
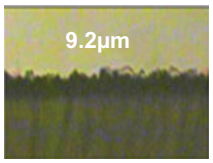
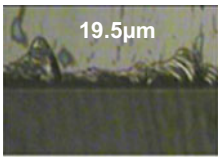
is performed in terms of die strength and chipping results. The dicing parameters for straight-cut, bevel-cut, and two-step-cut wafers are shown in Table 8.2.

To ascertain the die strength, a bending test has been shown to be a reliable measurement method [18]. In this study, a three-point bending test is used to determine the die strength, and the results are shown in Fig. 8.14 and Table 8.3. The sample size is 33 for each case. It was found that: (1) a bevel cut results in higher die strength than the other two dicing methods, (2) a bevel-cut instead of a straight-cut would lead to a 130% increase in die strength, (3) a bevel-cut induced less chipping than a straight-cut or a two-step cut, (4) a bevel-cut instead of a straight-cut would lead to a 10% decrease in front-side chipping, and (5) a bevel-cut instead of a two-step-cut would lead to a 15% decrease in front-side chipping.

8.2.5 Die-Attach Process

Thin dies are very flexible and require full support during pick and place to avoid die bending and to ensure uniform bond-line thickness, both of which are critical to packaging reliability. Thin die-attach layers are easier to control with film-type materials. Thus DAF is used for the two top daughter dies in TV2, whereas WEF is used for the two top daughter dies in TV1 (see Fig. 8.10). For both TV1 and TV2, the die attach used between daughter die 1 and the Cu–low-*k* mother die also is DAF.

Table 8.3 Die strength results for 300 μm thick Cu/Low-*k* chips using different dicing methods

	Back-side chipping (μm)	Front-side chipping (μm)
Straight cut		
Bevel cut		
Two-step cut		

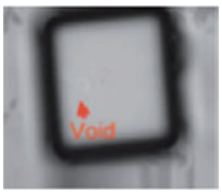
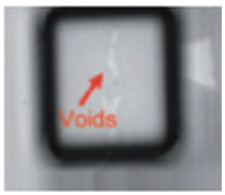
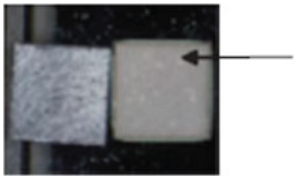
Die-attach paste is used for the Cu–low-*k* mother die attached onto the substrate, which usually has an uneven surface and requires material flow for good coverage without voids or delamination.

Table 8.4a shows the bonding-process setup for DAF. It is found that the voids disappeared when no. 4 process parameters are used. Therefore, the final bonding-process parameters for DAF are obtained. The key challenge for the DAF process is film voiding. Typical DAF temperature is around 120–150 °C [19]. Our final DAF temperature is 150 °C. Once the DAF is void-free or fully cured, employing a transfer-mold process is less effective at pushing out any trapped voids in the DAF.

WEF is a die-attach-material technology that allows same-sized wire-bonded dies to be stacked directly on top of each other. WEF is applicable to both center and peripheral wire-bond pads. The final bonding parameters for the WEF are obtained as follows: (1) bond force = 0.3 kgf, (2) bond temperature = 150 °C, and (3) hold time at 150 °C for 1 s. Comparison between one-step and two-step post cure for the WEF process is made in Table 8.4b. According to the optical images of die-shear samples, a two-step post cure profile is better than a one-step post cure profile. Thus a two-step post cure profile is used for the WEF.

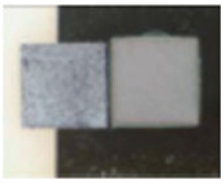
Figure 8.15 shows an x-ray image (with computed tomographic [CT] reconstruction) of the wire between two daughter dies in TV1 when the final WEF process parameters are used. The WEF wets the wire and fully encapsulates the wire within it. No wire distortion is observed. In this example, the WEF has two layers. The top layer, which is attached to the back of a top die, has very limited flowability under the die-bonding conditions. The bottom layer of the film, which is facing the wire bond-

Table 8.4 (a) Bonding process setup for die-attach film (DAF), (b) postbond cure process setup for wire-embedded film (WEF)

(a)	**No.**	**Process parameters**	**CSAM after post bond cure (1-step post cure: 160 °C for 60 min)**
	1	Bond force: 1.0 kgf; Bond temp: 150 °C; Hold time: 1 s	
	2	Bond force: 1.0 kgf; Bond temp: 150 °C; Hold time: 2 s	
	3	Bond force: 2.0 kgf; Bond temp: 150 °C; Hold time: 2 s	
	4	Bond force: 2.5 kgf; Bond temp: 150 °C; Hold time: 2 s	
(b)	**Postbond cure parameters**	**Optical images after different postbond cure and die shear testing**	**Observation**
	1-step post cure: 160 °C for 60 min		Light region after die shear testing

(continued)

Table 8.4 (continued)

	2-step post cure: 120 °C for 60 min, followed by 140 °C for 60 min		Uniform contrast on the film after die shear testing

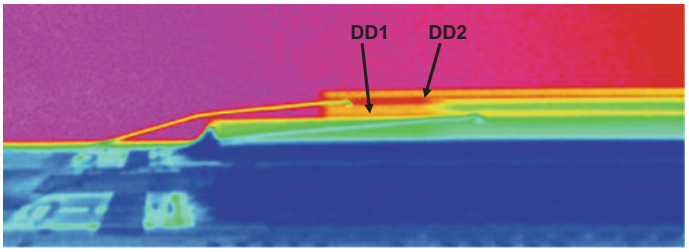


Fig. 8.15 X-ray image showing the wire between the two daughter chips in TV1

ing of the bottom die, has low viscosity under the die-bonding conditions to prevent wire distortion and achieve complete gap filling of the bottom-die topography.

8.2.6 Wire-Bonding Process

Wire bonding is one of the key interconnection methods in 3D heterogeneous integrations. State-of-the-art wire bonders with software and capabilities for complex looping, long and thin wires, and high bond-placement accuracy are required for the stacking of dies with different sizes, bonding on thin overhanging dies, forward and reverse bonding with very low loop heights, bonding on pads with low-*k* dielectrics, and bonding over active circuits under pad structures.

The upper part of Fig. 8.16 shows the ultralow-loop-height (50 μm) wire bonds on the first daughter die in TV1 [17]. It uses a new forward-motion method with the loop profile (as shown in the bottom part of Fig. 8.16) specially designed for the 50 μm loop height. The wire used is 0.8 mil (20 μm) NL4 gold wire. The wire bonder used is an ASM Eagle 60. The wire pitch is 53 μm, and the passivation opening is 43 μm × 100 μm. The key wire-bonding parameters are shown in Table 8.5. The new forward motion provides several benefits for stack-die packages. In addition to offering a lower loop height and less neck damage than traditional forward bonding, it provides for reduced pad damage, higher throughput, and better mold sweep than reverse bonding. It also offers a finer pitch capability than reverse bonding because of the low deformation on the first bond.

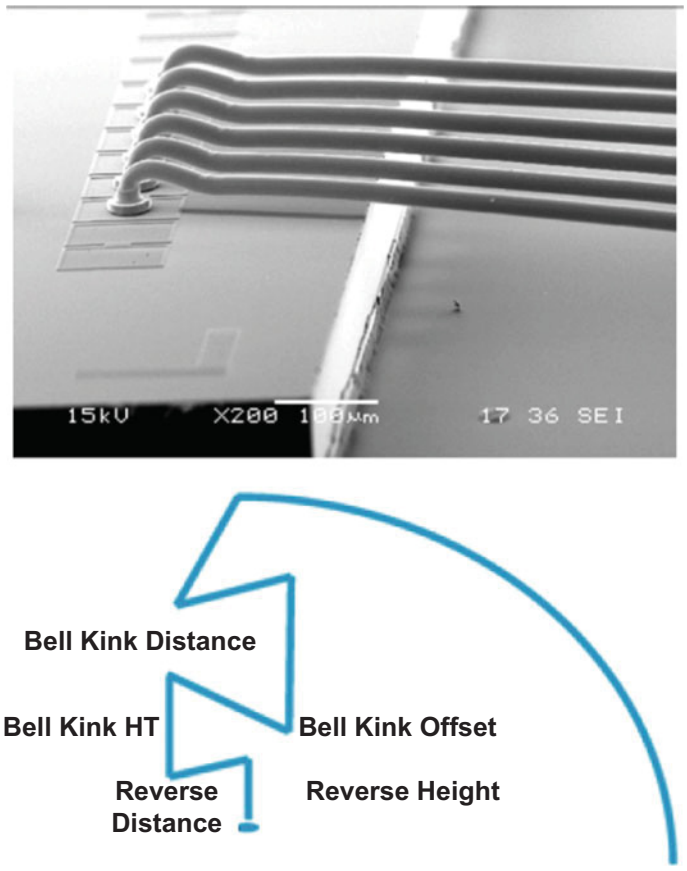


Fig. 8.16 (*Above*) ultralow-loop-height (50 µm) gold wire–bonding process established. (*Below*) ultralow-loop motion profile: bell loop

Table 8.5 Key wire bonding parameters

Bonding parameters	Setting	
	First bond	Second bond
Bond time (ms)	10	8
Bond power (Dac)	36	30
Bond force (g)	8	27
EFO current (mA)	3800	
EFO time (ms)	223	
Bond temperature (°C)	170	

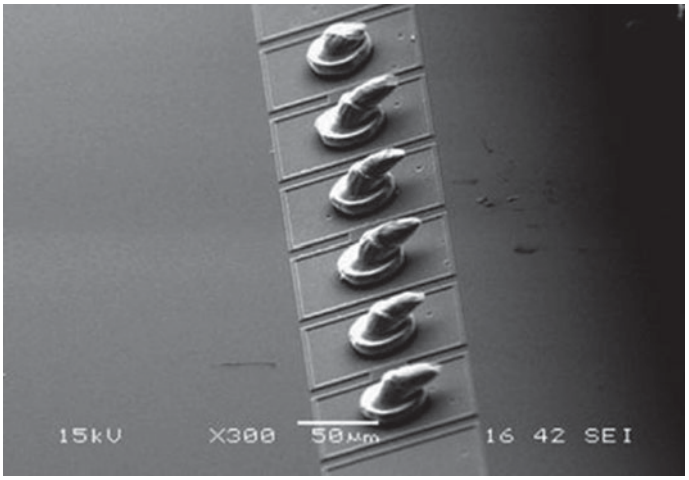


Fig. 8.17 Failure mode of neck break after wire-pull test

After wire bonding, the samples underwent the wire-pull test and the ball-shear test. It is found that: (1) all ball-shear readings are above the minimum requirement (8gf) with a desired shear failure mode, (2) no peeling is observed for all test samples during the ball-shear test, and (3) wire-pull readings are above the minimum requirement (3gf) with a desired wire-pull failure mode—neck break (Fig. 8.17). Finally, some of the wire-bonded test vehicles (TV1, TV2) are built as shown in Fig. 8.18.

8.2.7 Molding Process

Increased wire density and wire length in 3D die stacking makes the mold process more difficult compared with conventional single dies. Different layers of wire-bond loops that are subjected to varying amounts of drag force can result in wire-sweep differences. This increases the possibility of wire shorts. Therefore, a careful selection of molding-compound (MC) materials is needed for a reliable 3D die stacking package.

For the selection of MC materials, an adhesion test (pull test) and moisture-sensitive-level (MSL) tests (MSL 2 and MSL 3) are performed on four MCs (Table 8.6). The sample preparation is shown as follows: (1) dummy low-*k* dies are attached to the organic substrate, (2) four MCs are used to encapsulate the packages, and (3) molded substrates are diced into 17 mm × 17 mm packages for the MSL test and 8 mm × 8 mm packages for the pull test. The pull test (adhesion test) is done after the samples are subjected to MSL 1 with three reflows at a peak temperature of 260 °C. The fourth column of Table 8.6 shows that there are no significant differences in the pull values for all four MC [17].

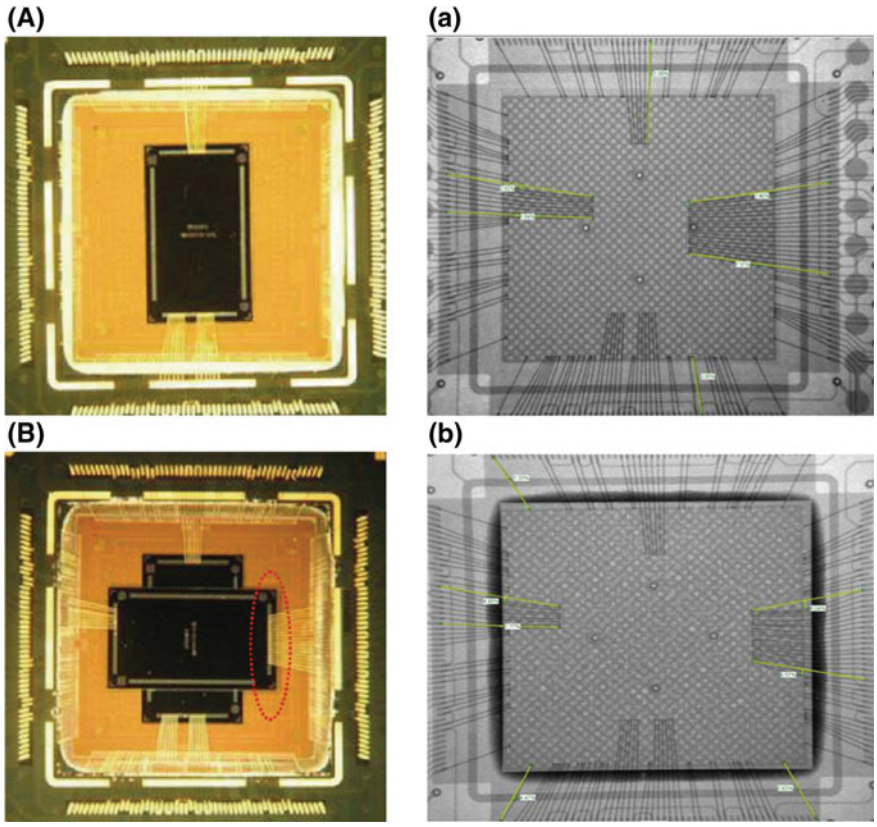


Fig. 8.18 Wire-bonded test vehicles: (**A**) TV1, (**B**) TV2. **a** Wire-sweep measurement for TV1 with a maximum wire sweep of 9.51%. **b** Wire-sweep measurement for TV2 with a maximum wire sweep of 9.04%

Table 8.6 Molding compound (MC) selection

MC code	MSL 3 (failed samples/total samples)	MSL 2 (failed samples/total samples)	Pull value in the pull test (kgf)	Warpage (μm)
MC1	0/7	1/6	2.33	377
MC2	0/7	0/7	2	504
MC3	0/7	5/7	2.33	692
MC4	0/7	3/7	1.33	620

Table 8.7 Reliability results for the 65 nm Cu/Low-*k* stack die FBGA package during thermal cycling and during high temperature storage

Reliability test	Group	Sample size	Electrical test	CSAM
			Fail	Delamination
Thermal cycling (−40 °C/125 °C)	TV1	22	0	0
	TV2	21	0	0
High temperature storage (150 °C)	TV1	22	0	0
	TV2	21	2	0

For MSL test evaluation, the samples are subjected to MSL 3 and MSL 2, respectively, and three reflows at a peak temperature of 260 °C. Both CSAM and Thru-Scan analyses are carried out to check the performance of the assembled packages with four MCs. A failure criterion based on the Joint Electron Device Engineering Council (JEDEC) recommendation of 10% delamination is employed. The second column of Table 8.6 shows that all four MCs passed MSL 3 without any voids and delamination. As to MSL 2, MC2 passed MSL 2 without any failure in seven samples (see the third column of Table 8.6). However, one sample out of six of MC1 failed at MSL 2. Five samples out of seven of MC3 failed at MSL 2. Three samples out of seven of MC4 failed at MSL 2. Therefore, MC2 is selected for use in subsequent assembly builds.

After selection of the MC material is done, molding is performed on TV1 and TV2. Wire sweeps are measured for TV1 and TV2, as shown in Fig. 8.19. All maximum wire sweeps are less than 10%, which is within acceptance limits.

8.2.8 Reliability Testing and Results

The final TV1 and TV2 are subjected to reliability tests (Table 8.7) according to JEDEC standards for components. Both CSAM and Thru-Scan are performed to examine the occurrence of delamination. No delamination have been observed on all samples up to 1000 cycles in thermal cycling (TC) tests and 1000 h in high-temperature storage (HTS) tests (Fig. 8.19).

An electrical test also is performed to monitor electrical resistance along the daisy-chain routing during reliability TC and HTS testing. No electrical failure is encountered on all samples up to 1000 cycles in TC testing (−40 to 125 °C) and 1000 h of HTS testing (150 °C) except for two TV2 samples in HTS testing (Table 8.7). The two samples are shown to be open circuit in the daisy chain. Failure analysis is performed by decapsulation of the MC followed by pull testing and shear testing on the wire bonds. Both tests showed the wire bonds with lower bond strength. In the worst case, the ball bond is detached from the pad, indicating a typical Kirkendall void failure (Fig. 8.20). It is found that the failed wire bond occurred at the right side of the top die (i.e., daughter die 2). It should be noted that there is a 1 mm overhang between daughter die 2 and daughter die 1 in TV2 samples (see Fig. 8.18b). However, TV1

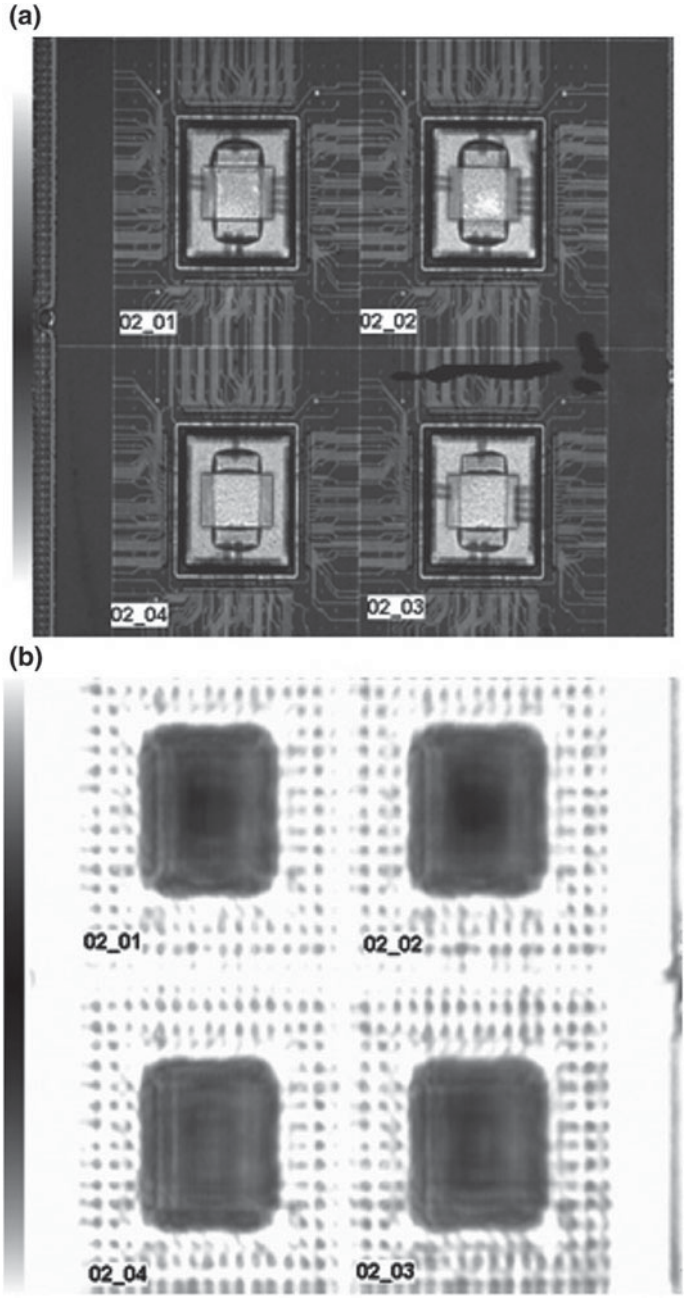


Fig. 8.19 **a** Typical CSAM result showing no delamination after 1000 cycles in a TC test (−40 ↔ 125 °C). **b** Typical Thru-Scan result showing no delamination after 1000 cycles in a TC test (−40 ↔ 125 °C)

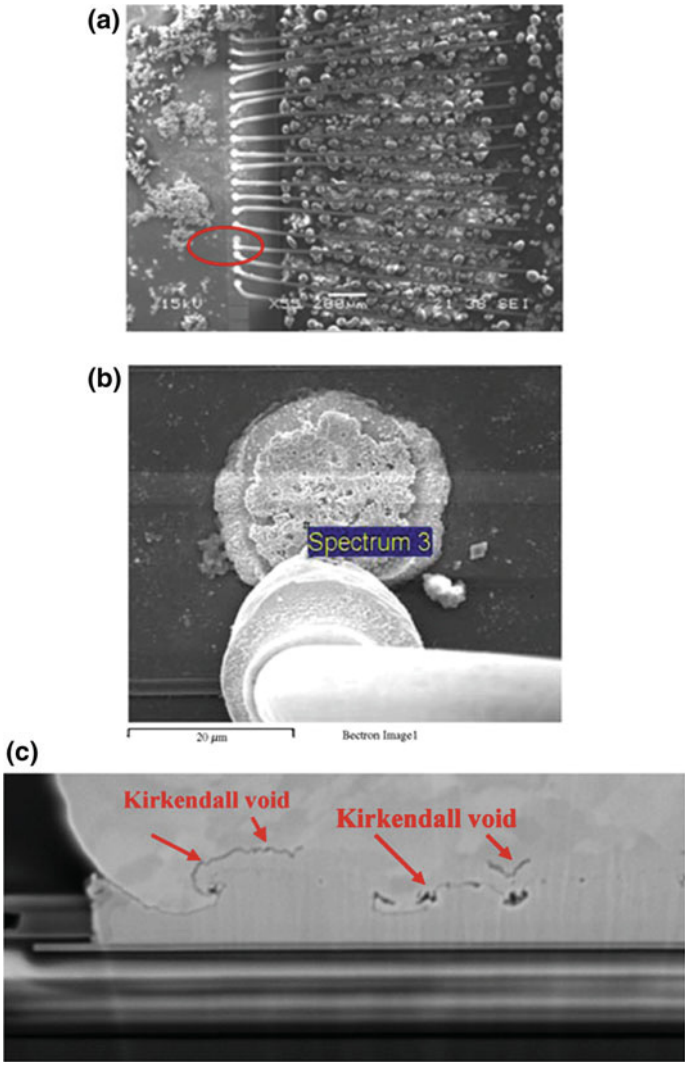


Fig. 8.20 **a** Failed wire-bond location of one TV2 sample after decapsulation of the MC. **b** Top view of the failed wire bond. **c** Cross section of a wire bond of the TV2 sample showing Kirkendall voids

does not have any overhang issues. It might be the overhang of 1 mm that causes the poor wire-bond strength at time zero, although all ball-shear readings and wire-pull readings of the TV2 samples are above the minimum requirement.

8.2.9 Summary and Recommendations

Some important results and recommendations are summarized as follows [17]:

- More than 70% semiconductor chips used in the whole world are with wirebonding. Since 2015, the usages of Cu (including PdCu) wires are more than Au wires. In the past few years, Ag wires are attracting some attention.
- PEDL technology has been adopted to reduce delamination of the Cu–low-*k* layer by reducing the stress. The stress in the Cu–low-*k* layer has been reduced by a factor of 4.2.
- Based on the dicing evaluation, the bevel-cut dicing methodology is better than the single-step dicing methodology in terms of chipping and die-strength results: The front-side chipping has been reduced by 15%, and the die strength has been increased by a factor of 2.3.
- An ultralow-loop (50 μm) wire-bonding process has been established.
- The wire-embedded-film process has been established, and it allows the special die-attach film to penetrate between gold wires such that the dummy die (or spacer die) can be removed.
- The 65 nm Cu–low-*k* stack-die heterogeneous integration package (i.e., TV1) has been developed, and it has successfully passed JEDEC component-level tests such as TC for 1000 cycles (−40 to 125 °C) and HTS (150 °C) for 1000 h.

8.3 Low-Temperature Bonding of Memory Chips and Logic Chip

Low-melting solders such as InAg, InCu, InSn, InNi, and InSnCu, with bonding temperatures of less than 200 °C, will be considered for stacking memory chips and logic chip in this chapter.

8.3.1 How Does Low-Temperature Bonding with Solder Work?

The basics of low-temperature bonding are shown in Fig. 8.21. In this book, low-temperature bonding [20–55] is the same as such well-defined processes as transient liquid-phase (TLP) bonding, solid-liquid interdiffusion (SLID) bonding, and intermetallic compound (IMC) bonding. The low-temperature solder (e.g., InAg, InCu, InSn, InNi, InAu, InSnAu, InCuNi, and InSnCu) is coated on the specially designed and fabricated under bump metallurgy (UBM; e.g., Cu, Cu/Au, Ti/Au, Ni/Au, Ti/Cu, and Cu/Ti/Au). After aligning and bonding at a temperature of less than 200 °C, all the solders will react with the UBM on the chips/wafers and become intermetallic

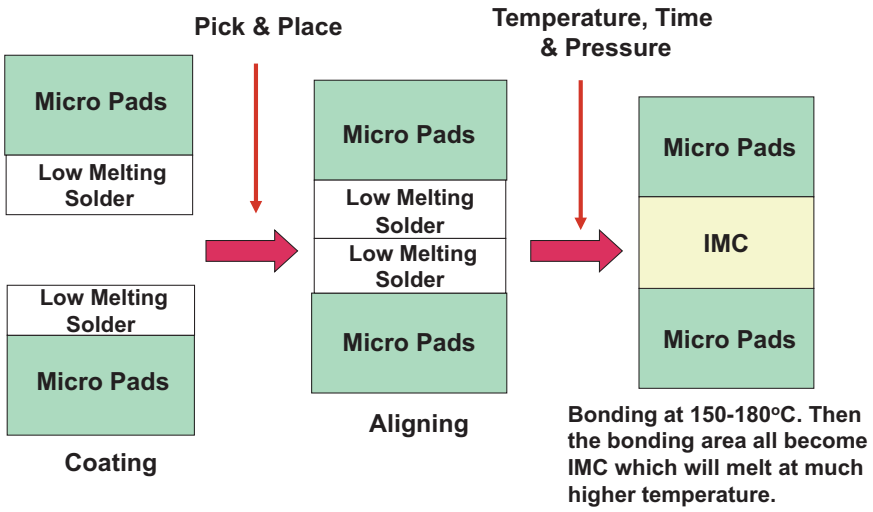


Fig. 8.21 Fundamental of transient liquid-phase or low-temperature bonding

compounds (IMCs) with melting points that are a couple of hundred degrees higher than that of the solders.

8.3.2 Low-Temperature [(SiO_2/Ti/Au/Sn/In/Au) to (SiO_2/Ti/Au)] Bonding

Low-melting solders such as InAg, InCu, InSn, InNi, InAu, InSnAu, InCuNi, and InSnCu with a bonding temperature of less than 200 °C [20–55] are desired to reduce damage (warpage) to the microstructures resulting from the thermal-expansion mismatch of the bonding chips [some of them with copper-filled through-silicon vias (TSVs)]. Also, the solder joints form robust IMC interconnects with high remelting temperatures, which allows stable 3D IC chip stacking.

It should be emphasized that with the In-base solder (melting point ≈ 156 °C), the choice of the right composition of solder and UBM to form nothing but IMCs with a high remelting temperature is extremely important. Since the In atoms with additional elements tend to form a ternary eutectic phase, which has an even lower melting temperature than the In binary eutectic point [22], it is necessary to avoid forming the ternary eutectic phase by properly designing the suitable layer combination.

8.3.3 Solder Design

The use of indium with Ni, Cu, or Au has been studied for the low temperature bonding in 3D integrations [20–23]. Usually, a barrier layer such as Ti is inserted between the In layer and the other metal layers to prevent the excessive inter-diffusion [24].

In this section, the In-based solder layer is chosen for the low temperature solder and bonded to a thin Au layer to form AuIn-based IMCs after bonding. Since the diffusion of Au into the In layer is fast enough to form AuIn intermetallic even at room temperature, a thin layer of Sn is inserted between the In and Au layers to minimize the inter-diffusion before bonding; that is, the Sn reacts with the Au and temporarily forms a diffusion barrier layer before bonding so that the In layer is able to be preserved. On the other hand, this barrier layer should not interrupt the interfacial reaction between the In and Au layers during and after bonding to form the IMCs completely.

8.3.4 Test Vehicle

The test vehicle for the 3D IC chip stacking is shown in Figs. 8.22, 8.23, 8.24 and Table 8.8. The silicon test chip (8 mm × 8 mm) has approximately 1700 solder bumps, and each consists of 100 μm-diameter Ti/Au (0.1 μm/1 μm) UBM and 80 μm-diameter Sn/In (0.5 μm/2 μm) solder with a flesh of Au (0.05 μm). The other side of the chip has 120 μm × 120 μm of Ti/Au (0.1 μm/1 μm) UBM only.

The test vehicle is fabricated on a 200 mm Si wafer with SiO_2 coating. On the front side (face) of the wafer, 0.1 μm of Ti and 1 μm of Au are sputtered on the SiO_2 and are patterned to form the 120 μm × 120 μm UBM. Then the backside (back) of the wafer is sequentially (1) backgrinded to 200 μm thick, (2) coated with SiO_2 for the passivation layer, (3) deposited with 0.1 μm of Ti and 1 μm of Au (in a sputter chamber), (4) wet etched to pattern the 100 μm-diameter (Ti/Au) UBM pads, (5) laminated with a 20 μm dry film, (6) opened for the solder bumps, (7) deposited the Sn (0.5 μm) on the Au (of the UBM) and then the In (2 μm) on the Sn in an evaporation chamber, and (8) stripped (a lift-off process) the dry film. Figure 8.23 shows the top view of the as-evaporated composite coating surface morphology. The surface is rough and has a granular structure with a grain size of 2 to 3 μm. In order to bond a surface with such rough features, a molten-solder layer and high pressure are necessary to fill the gaps between surfaces.

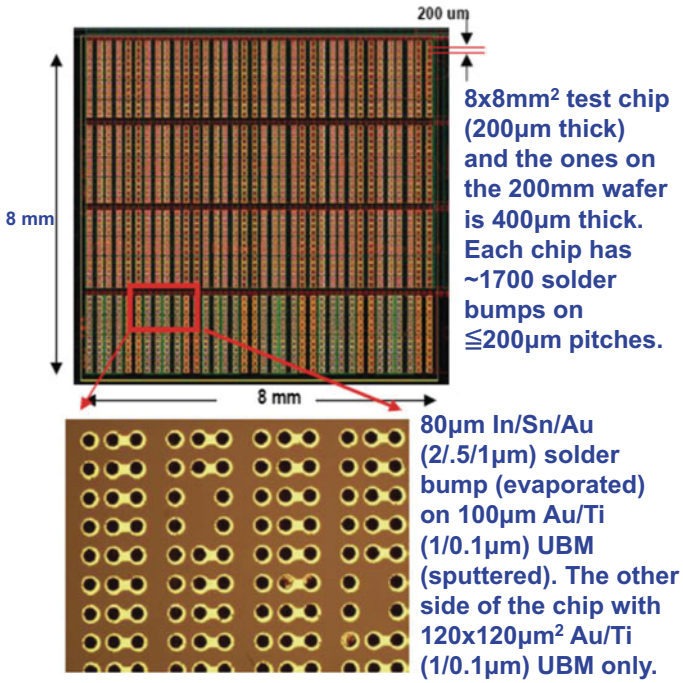


Fig. 8.22 Solder bumps and pads on the top surface of the test vehicle

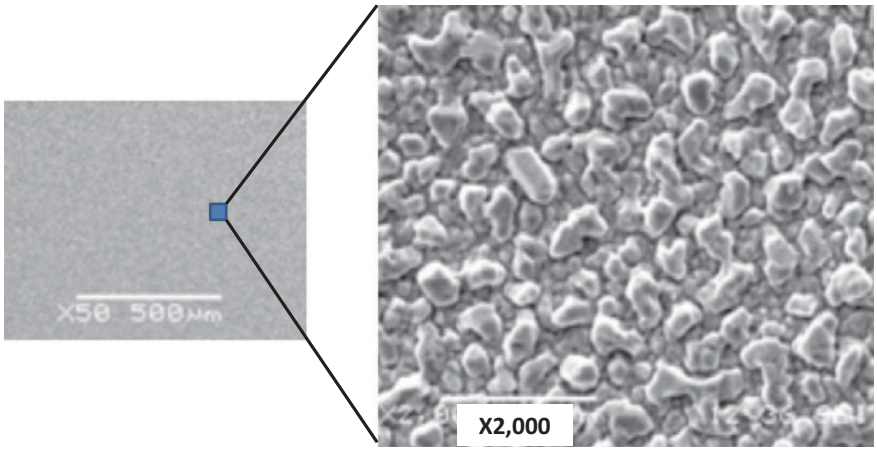


Fig. 8.23 SEM images of as-evaporated composite coating surface morphology

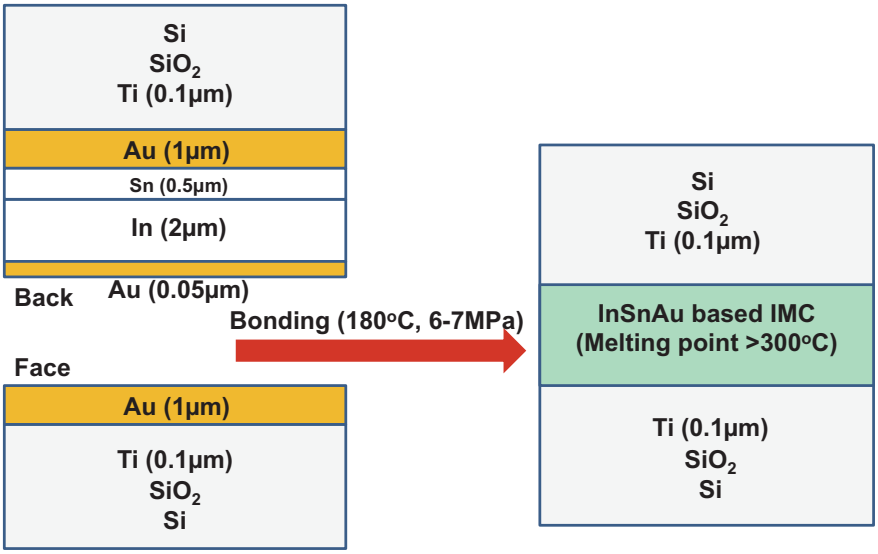


Fig. 8.24 Schematic of (left) the chip with UBM + solder bump and the chip with UBM only and (right) the IMCs after bonding

Table 8.8 Test vehicle dimensions

Items	Values
Wafer size	200 mm
Chip size	8 mm
Stacking chip thickness	200 mm
Base chip thickness	400 mm
Solder bump diameter	80 μm
Solder bump pitch	≦200 mm
Number of bumps	~1700
UBM (Ti/Au)	0.1/1 μm
Solder (In) bump	2.5 μm
Total bump height	3.6 μm

8.3.5 3D IC Chip Stacking with InSnAu Low-Temperature Bonding

Figure 8.25 shows the assembly process of 3D IC chip stacking with low-temperature bonding. The first layer (ASIC) is the 200 μm wafer (400 μm thick) with the 120 μm × 120 μm UBM (face). The second chip (memory) with the lead-free InSnAu solder bump (back) is bonded on the face of the wafer at 180 °C and 6 to 7 MPa for 45 s. After bonding, the lead-free solder interconnects become InSnAu IMCs, and the remelt temperature is a couple hundred degrees higher than the melting point of In.

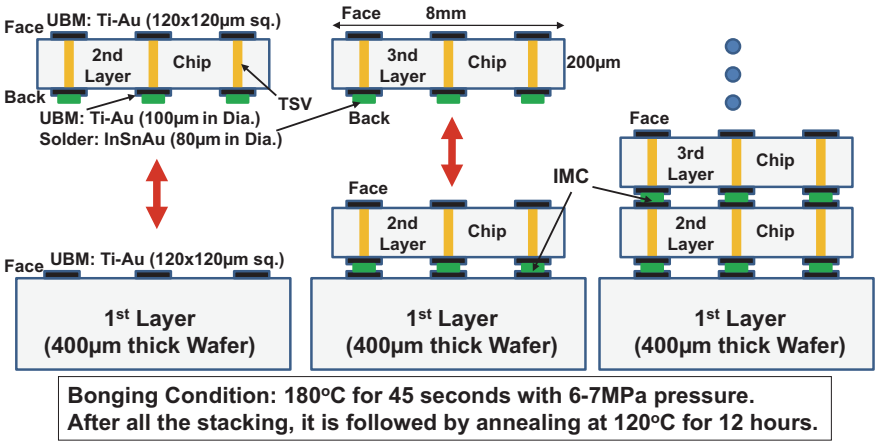


Fig. 8.25 3D heterogeneous integration with low-temperature bonding

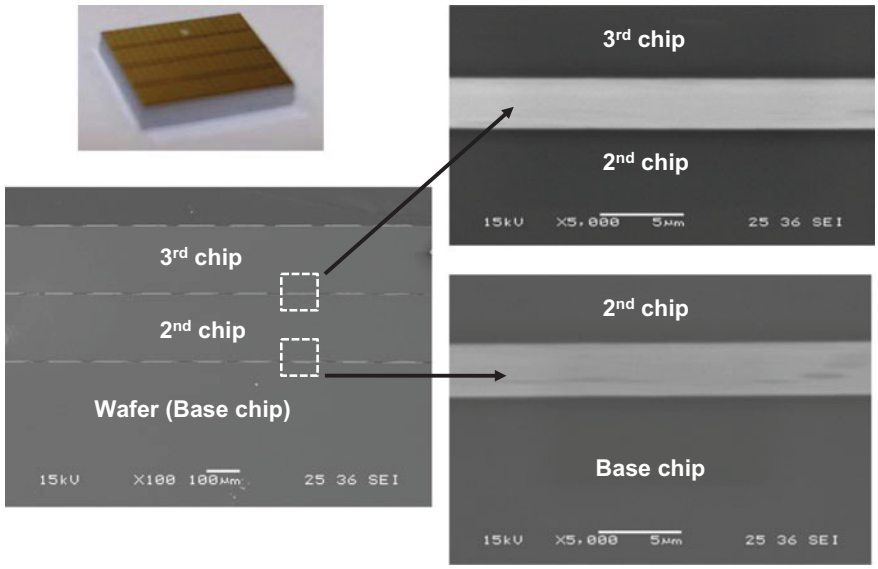


Fig. 8.26 The assembled module and SEM cross-sectional views of the three-layer stacked chips consisting of 1700 solder microjoints on each interconnect layer

Then the back of the third chip (memory) with solder bumps is bonded to the face of the second chip under the same conditions. The stacking is followed by annealing at 120 °C for 12 h. Figure 8.26 shows the assembled three-chip stacking by the present low-temperature bonding process. The cross sections show that the bonding is in very good condition, and there are no visible voids. The design of experiments leads to the present optimal bonding condition given in [26].

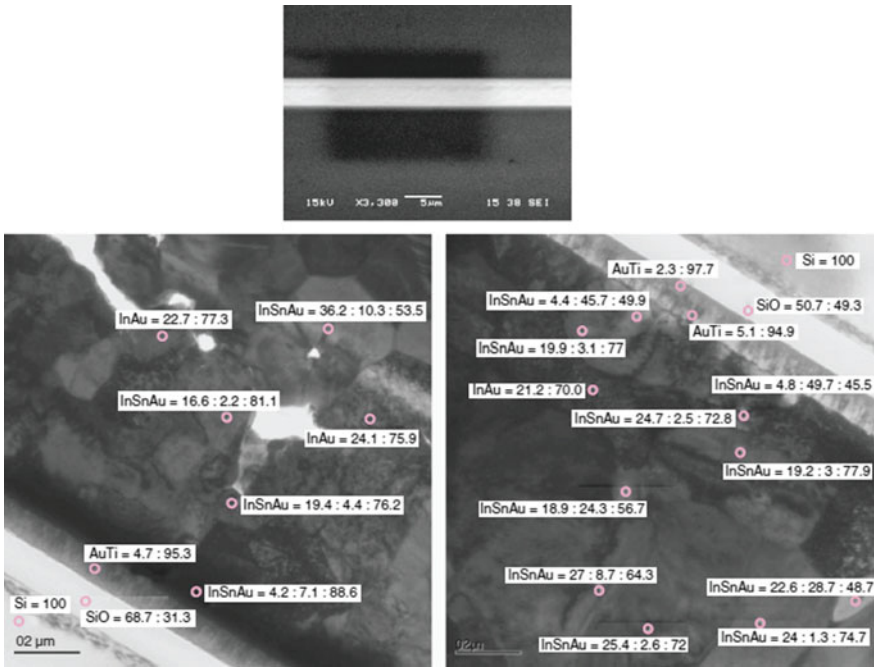


Fig. 8.27 SEM (*above*) and TEM (*below*) images at the interface region

8.3.6 SEM, TEM, XDR, and DSC of the InSnAu IMCs

Since the IMC layers are relatively thin, the TEM (transmission electron microscopy) technique is used because it provides local chemical analysis. Figure 8.27 shows TEM images of the region close to the base-material silicon and interfacial reaction region between the AuTi and solder intermediate layers. The interfaces between each layer are void-free, uniform, and fully converted to IMCs. The elemental composition results (at.%) of the selected points are labeled in Fig. 8.27. Two IMCs are identified along the main reaction zone, that is, InAu and InSnAu. This result is consistent with the XRD (x-ray diffraction) results, which confirmed the presence of these two IMCs in the bonding interface. Figure 8.28 shows the DSC (differential scanning calorimetry) curve indicating that the remelting temperature is higher than 365 °C. The SEM image (Fig. 8.29) shows that uniform bonding has occurred without any defects.

8.3.7 Young's Modulus and Hardness of the InSnAu IMCs

The elastic modulus and hardness of the AuSnIn-based IMC interconnects are determined by a nano-indentation method. Since the size of the IMC layers from the cross

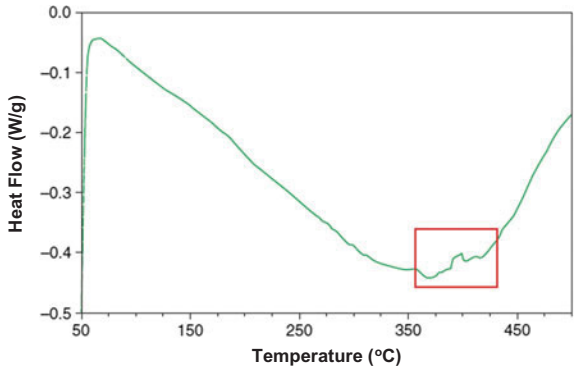


Fig. 8.28 The DSC curve clearly shows the melting point at approximately 360 °C

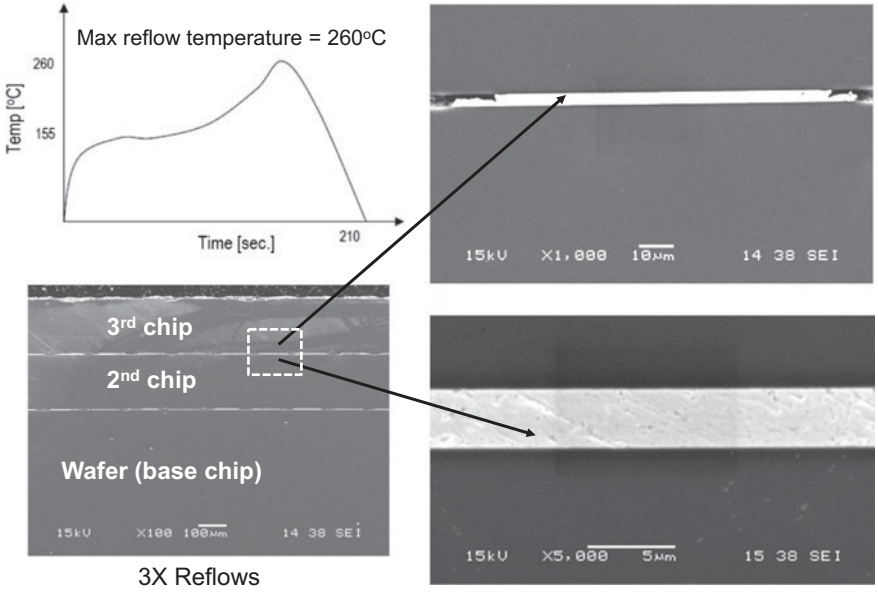


Fig. 8.29 Cross sections of the 3D IC stacking after three reflows with a maximum temperature of 260 °C

section of a sample is too thin for the tip of an optical microscope, the measurements are carried out along the fractured surfaces of the chips after shear tests. It is found that the Young's modulus of InSnAu is about 81 GPa, which is a little higher than that of Au (78 GPa) [56] and much lower than that of Cu_6Sn_5 (112.6 GPa) and Cu_3Sn (132.7 GPa) [57]. The measured hardness is approximately 1.5 GPa.

8.3.8 Three Reflows of the InSnAu IMCs

There are at least two different kinds of low-temperature assemblies—namely, one is for chip-level interconnects in a package and the other is for board-level interconnects. For board-level interconnects, because it is the final assembly, low-melting solders can be used to attach the packages on the board as long as the solder joints are reliable. However, for chip-level interconnects in a package, because the package has to be assembled on the board with lead-free solders, the package must be qualified before it is mounted on the PCB. Some of the qualifying tests, among others, include: (a) temperature cycling test ($-40 \leftrightarrow 125$ °C for 1000 cycles) where the package should be preconditioned with humidity exposure and at least three lead-free SMT reflow cycles, (b) biased HAST (highly accelerated stress test) (130 °C/85% relative humidity, 1.8 V for 100 h), and (c) pressure-cook (steam) test (121 °C, 100% relative humidity, at 2 atm for 168 h).

In general, the quality and reliability requirements of the chip level interconnects are always tougher than those of board-level interconnects; that is, the low-temperature solders that work for board-level interconnects may not work for chip-level interconnects. Figure 8.29 shows a typical reflow profile for qualifying packages. It also shows the cross section at different magnifications of the IMC interconnects. After three reflows, there is no visible change in the InSnAu IMC interconnects of the 3D IC chip stacking.

8.3.9 Shear Strength of the InSnAu IMCs

Since the InSnAu IMC interconnects are very strong and can resist shear, many of the 200 μm chips are broken during shear (horizontal push) tests. Thus, to determine the shear strength of the InSnAu IMC interconnects, 400 μm chips are used for the tests. Figure 8.30 shows the typical failure mode of the InSnAu IMC interconnects under shear tests. The fracture surfaces occur along the IMC joint and the interface between the TiAu UBM and the InSnAu IMC joint.

Figure 8.31 shows the shear-strength test results of the InSnAu IMC interconnects as fabricated and after three reflows. It can be seen that (1) the shear strength of the first IMC joint (between the base chip and the second chip) and the second IMC joint (between the second chip and the third chip) is reduced by approximately 15% because of the three reflows; (2) even with the reduction, however, the shear strength is still much higher than the required 20 MPa; and (3) for both cases, the shear strength of the first IMC joint is slightly higher (~8%) than that of the second IMC joint. This could be due to the shear-test setup: (1) first shear (horizontal push) the third chip and hold the bottom two chips to obtain the second IMC strength and (2) then push the second chip and hold the base chip to get the first IMC strength. Since the holders are not 100% rigid, some of the push forces become relaxed. Also, the larger the holder, the more the push force relaxes.

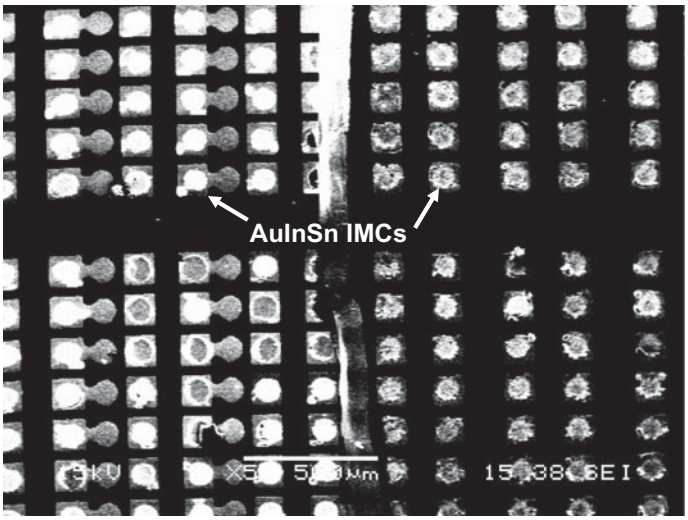


Fig. 8.30 The shearing fracture surfaces occur along the IMC joints and the interface between the UBM and IMC joints

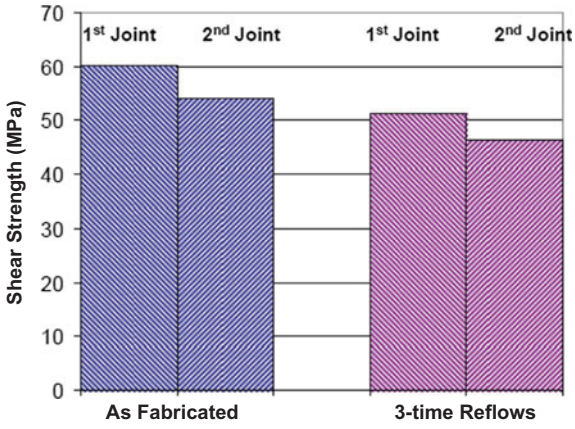


Fig. 8.31 Bonding shearing strength of the three-layer stack: as fabricated and with three reflows

8.3.10 Electrical Resistance of the InSnAu IMCs

The electrical resistance of the InSnAu IMC interconnects can be measured by Kelvin's four-point measurement method, as shown in Fig. 8.32. Two bumps of 200 μm diameter are formed far away (800 μm) from each other. Figure 8.33 shows the measurement results, and it can be seen that the electrical resistance of the InSnAu IMC joint is approximately 0.12 Ω, and it is not degraded even after three reflows at 260 °C.

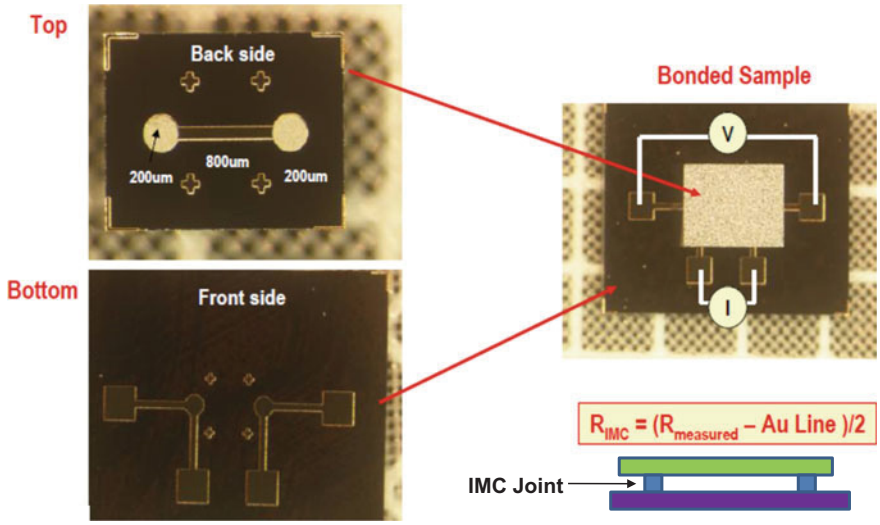


Fig. 8.32 The test fixtures for the electrical resistance measurement

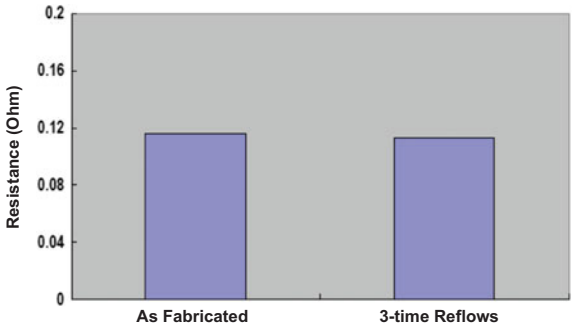


Fig. 8.33 IMC joint electrical resistance: as fabricated and after three reflows

8.3.11 When Does the InSnAu IMC Become Unstable?

It has been shown earlier by the DSC method that the remelting temperature of the InSnAu IMC interconnects is greater than 365 °C. It would be interesting to find out the temperature when the IMC interconnects of the 3D IC chip stack collapse. However, owing to the size limit of the platinum crucible of the DSC equipment, the whole 3D IC chip stack cannot be put in and measured. Instead, an indirect method is adopted that employs a TMA (thermomechanical analyzer) to measure the expansion of the whole 3D IC chip stack versus temperature, as shown in Fig. 8.34. Before the InSnAu IMC interconnects start to remelt, the curve should be moving upward (very close to a straight line) with temperature. However, when the InSnAu IMC interconnects start to remelt, the expansion curve starts to become unstable until it drops, which means that the 3D IC chip stack is totally collapsed. Thus, based on

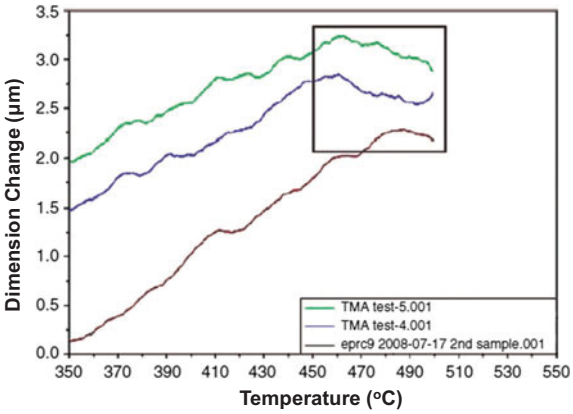


Fig. 8.34 TMA results: remelting happens around 400 °C

the three samples tested under TMA and shown in Fig. 8.34, the IMC in the 3D IC chip stack could start remelting at around 380–400 °C (these are higher than 365 °C because the whole 3D IC chip stack is being measured and has absorbed more heat) and collapse at around 450–480 °C.

8.3.12 Summary and Recommendations

Some important results and recommendations are summarized as follows [26, 27]:

- The advantage of memory chips stacking with low-temperature solder bonding is when you stack the higher chips, the bondings of the lower chips will not be remelt and the lower chips will not be moved.
- A low-temperature solder system (InSnAu) has been designed for 3D heterogeneous integration of chip-stacking applications. The bonding conditions are 180 °C and 6 MPa for 45 s. After bonding, the whole assembly is annealed at 120 °C for 12 h.
- SEM, XDR, and TEM images show that uniform bonding has been achieved without any defects, and all the bonding areas have been converted into InSnAu and InAu IMCs. Also, DSC results show that the remelting temperature of the IMCs is greater than 365 °C.
- After three reflows (with a maximum temperature of 260 °C), there is (1) no visible change of the InSnAu IMCs of the 3D IC chip stacking and (2) no change in the electrical contact resistance of the IMCs.
- For 3D IC chip stacking, because the chip could be as thin as 20 μm, which makes the ordinary characterization methods very difficult or impossible, new methods and equipment are desperately needed.

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Chapter 9
Heterogeneous Integration of Chip-to-Chip Stacks



9.1 Introduction

As pointed out by Intel [1] sometimes ago that the holy grail to address the memory bandwidth challenge for tera-scale computing is to have 3D chip-to-chip and face-to-face stacked MCP (multi-chip packaging), Fig. 9.1. The top chip is a memory and the bottom chip is a logic or CPU (central processing unit). In this chapter, two examples of heterogeneous integration of chip-to-chip and face-to-face are presented. One is with TSVs in the bottom chip to let go the signals, powers, and grounds and the other is without TSVs but with solder bumps on the larger chip.

9.2 Heterogeneous Integration of Chip-to-Chip with TSVs

Figure 9.2 shows a schematic drawing of the packaging structure with a top Si chip (which could be a memory) and a bottom Si chip (which could be a CPU). On the top chip, there are Cu pillars + Sn solder caps fabricated on it whereas on the bottom chip, there are TSVs that are filled with Cu and on top of the TSV, electroless nickel and immersion gold (ENIG) under bump metallurgy (UBM) pads are made. The top chip and the bottom chip are stacked together by joining the solder microbumps and the ENIG pads. The main focuses of this study are to demonstrate the fabrication process of TSV with Cu filling and develop the chip-to-chip assembly process.

9.2.1 Design of TSV and UBM Pads on the Bottom Chip

Figure 9.3 shows a cross-sectional view of the bottom chip with detailed information of TSV and UBM pad on top. The designed diameter of the TSV is 15 μm. Above the TSV is UBM pad. In this section, ENIG is used as the UBM layer. For very fine pitch

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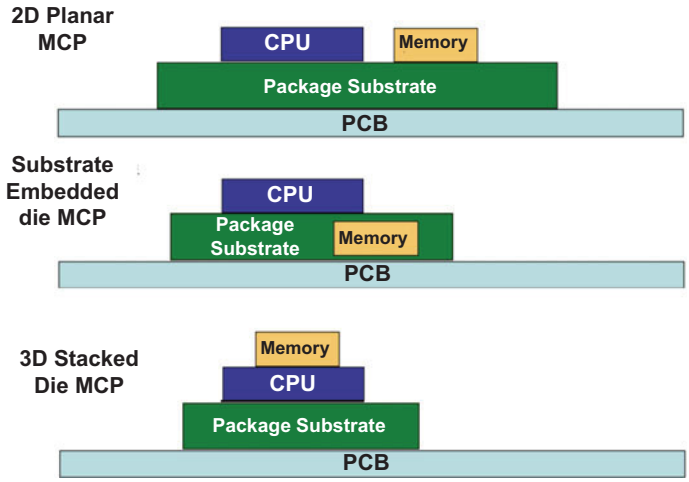


Fig. 9.1 Intel's packaging technology address the memory bandwidth challenge for tera-scale computing

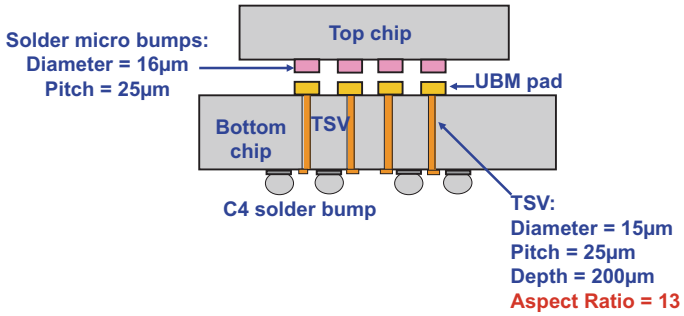
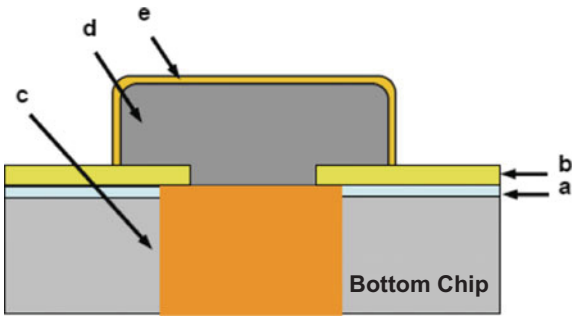


Fig. 9.2 Schematic drawing of heterogeneous integration of chip-to-chip with TSVs

UBM pads, normal UBM metal films, such as TiCuNiAu or AlNiVCu, are difficult to pattern with traditional photolithography and wet etching process, because the undercut caused by the wet etching process can damage the small UBM pads. ENIG formation does not require any high vacuum or photolithography equipment to form the metal stack on top of the bond pads, therefore it is a simple and low cost solution for high density and high pin-count build-up integrated circuit packages.

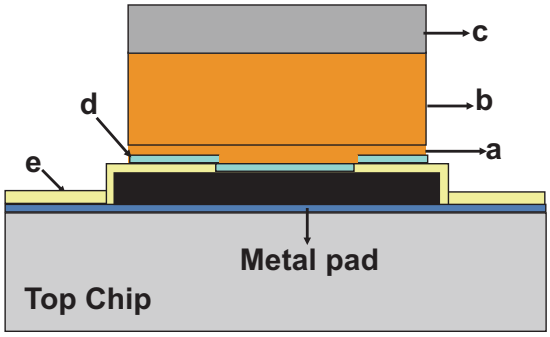
9.2.2 Design of Solder Microbump on the Top Chip

Figure 9.4 shows a cross-sectional view of the top chip with detailed structure of a solder microbump, which consists of Cu pillar with Sn solder cap. Total thickness of



a	passivation layer 1
b	passivation layer 2
c	TSV filled with Cu
d	electroless plated Ni
e	immersion Au

Fig. 9.3 Schematic cross-sectional view of UBM pad (ENIG) on the bottom chip



a	Cu seed layer
b	Plated Cu
c	Plated Sn
d	Ti adhesion layer
e	Passivation layer

Fig. 9.4 Schematic cross-sectional view of the Cu pillar and Sn cap on the top chip

the Cu pillar and the Sn solder cap is 10 μm and they are fabricated with electroplating process. In order to make sure there is enough Sn solder to achieve reliable joining and at the same time to avoid sidewall wetting, the Sn cap thickness is designed between 3 and 4 μm and the Cu pillar thickness varies between 6 and 7 μm [2, 3].

9.2.3 *Fabrication of TSV*

The high aspect ratio TSVs are etched in an inductive coupled plasma based deep reactive ion etch (DRIE) system with BOSCH process [4]. In the DRIE process, two process cycles, e.g., the Si etch cycle and the sidewall passivation cycle, run alternatively. During the Si etch cycle, Si is etched isotropically whereas in the passivation cycle, sidewall of the TSVs are protected by a thin layer of polymer. Figure 9.5 shows the fabrication process flow.

As shown in Fig. 9.5a, first, a layer of SiO_2 is deposited on the wafer as hard mask. Then a thin layer of photoresist is spin coated and patterned Fig. 9.5b. After etching the SiO_2 layer and stripping the photoresist Fig. 9.5c, TSVs are etched to the desired depth and the SiO_2 hard mask is removed after etching Fig. 9.5d. After that, a layer of plasma-enhanced tetraethylorthosilicate (PETEOS) is deposited on the front side of the wafer for sidewall passivation, Fig. 9.5e. For deviceless wafer, the sidewall passivation can also be achieved by thermal oxidation, which can give better uniformity and smoothness of the sidewall. Then the wafer is thinned down to expose the backside of the TSVs, Fig. 9.5f. In order to fully passivate the sidewall of the TSVs, another layer of SiO_2 is deposited on the backside of the wafer in a Plasma-Therm 790 series plasma enhanced chemical vapor deposition (PECVD)/reactive ion etch (RIE) system, Fig. 9.5g and then a Ti adhesion layer with thickness of 0.3 μm and a Cu seed layer with thickness of 2 μm are sputtered onto the backside of the

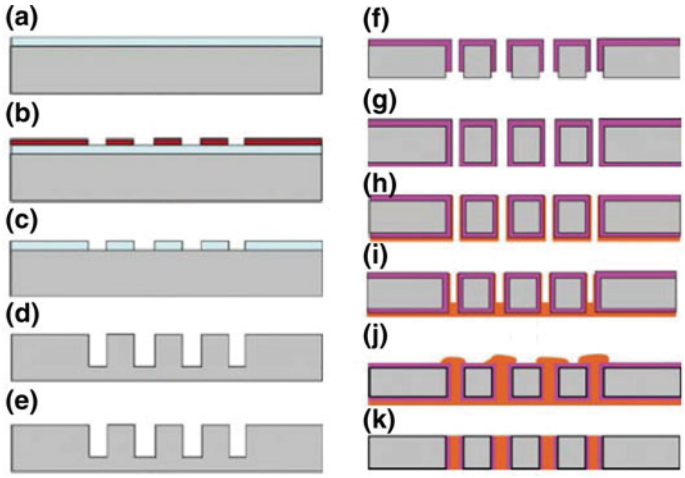


Fig. 9.5 Process flow for TSV fabrication and Cu filling. **a** SiO_2 deposition as hard mask. **b** Photoresist coating and patterning. **c** SiO_2 etch and photoresist stripping. **d** TSV etching and SiO_2 hard mask removing. **e** PETEOS deposition for sidewall passivation. **f** Wafer thinning to expose the backside of the TSV. **g** SiO_2 deposition on the backside of the wafer. **h** Layer of Ti/Cu is sputtered at the backside of the wafer as seed layer. **i** Wafer level plating to seal the TSV from the backside of the wafer. **j** Bottom-up plating till all the TSV is filled. **k** Cu overburden on the top of the wafer removed by CMP and further thinning down to 170 μm

wafer in a Balzer LLS 801 sputtering system, Fig. 9.5h. Thick adhesion and seed layers can make sure TSV sidewalls are covered. In both steps of Fig. 9.5g, h, the wafers are mechanically clamped in the machines and no vacuum chuck required. If these two steps are processed with tools having vacuum chuck, such as the low temperature PECVD deposition system from Sumitomo process technology systems and the physical vapor deposition system from Tango Systems, Inc., a temporary carrier is required [5]. The TSVs are then sealed with Cu electroplating process from the backside of the wafer, Fig. 9.5i. In this process, because the diameter of via is only 15 μm, it is easy to seal the vias from the bottom with high plating current (1 A in this study). After that, bottom-up plating is carried out till all the TSVs are filled, Fig. 9.5j. To reduce voids in the TSVs, the plating current is reduced to 0.1 A. This bottom-up plating step can be processed without support wafer. Therefore, after bottom-up plating, it is not necessary to remove the support wafer, which is difficult and can lead to wafer break easily, as was tested in reference [6]. After bottom-up plating, the Cu overburden on the top of the wafer is removed by chemical-mechanical polish (CMP). In order to remove the void in the TSVs, the wafer is further thinned down with another 30 μm, Fig. 9.5k. After CMP, the wafer can be processed with Cu annealing and another step of CMP to remove the Cu protrusion after annealing if required [7], these steps are skipped in this study.

9.2.4 Fabrication of ENIG UBM Pads on the Bottom Chip

The ENIG UBM pads are fabricated on top of the TSVs. Figure 9.6 shows the process flow. First, a layer of dielectric is deposited on the top of the wafer, Fig. 9.6a. Then a thin layer of photoresist is spin coated and patterned, Fig. 9.6b. After that, the dielectric layer is etched to expose the TSVs and the photoresist is stripped, Fig. 9.6c. Finally, electroless Ni-P plating with immersion of Au is done to form the UBM pads, Fig. 9.6d.

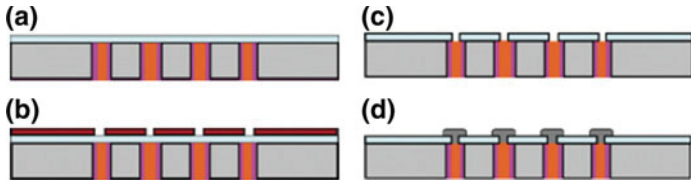


Fig. 9.6 Process flow for ENIG plating on top of TSV. **a** SiO_2 deposition as dielectric layer. **b** Photoresist coating and patterning. **c** SiO_2 etching to expose the TSV and photoresist stripping. **d** Electroless Ni-P plating and electroless Au plating to form UBM pads

9.2.5 *Fabrication of Cu Pillars and Sn Caps on the Top Chip*

Figure 9.7 shows the process flow for fabrication of Cu pillars and Sn caps on the top chip. First, a passivation layer of SiO_2 and a metallization layer of Al film are deposited on the wafer, Fig. 9.7a. Then a layer of 2 μm thick photoresist is spin coated and patterned, Fig. 9.7b. The Al film is etched to form the metal pad and the photoresist is removed, Fig. 9.7c. Another passivation layer is deposited and patterned, Figs. 9.7d–f. Then Ti/Cu of adhesion/seed layers are sputtered, Fig. 9.7g. To form a plating mold, a 10 μm thick layer of photoresist is coated and patterned, Fig. 9.7h. Cu/Sn is then plated sequentially, Fig. 9.7i, and the photoresist is stripped and the Ti/Cu adhesion/seed layers are etched back, Fig. 9.7j. After plating, a reflow was performed to reshape the solder microbumps in order to achieve uniform bump heights.

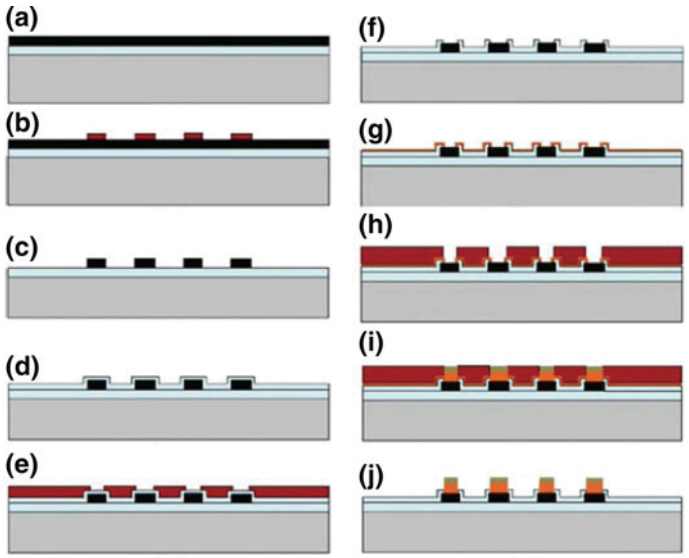


Fig. 9.7 Process flow for CuSn solder microbump fabrication on the Si chip. **a** SiO_2 and Al deposition. **b** Photoresist coating and patterning. **c** Al etching to form the metal pad and photoresist stripping. **d** SiO_2 deposition. **e** Photoresist coating and patterning. **f** SiO_2 etch and photoresist stripping. **g** Ti/Cu of adhesion layer and seed layer deposition. **h** 10 μm thick photoresist coating and patterning as plating mold. **i** Cu/Sn plating sequentially. **j** Photoresist stripping and the Ti/Cu adhesion/seed layers etch back

9.2.6 TSV DRIE Results

During the DRIE process, many variables can affect the profile of the high aspect ratio TSVs, such as the SF6/C4F8 flow rate, etching/passivation active time, electrode power, and automatic pressure valve orientation etc. [8, 9]. Among these parameters, it is found that the etching/passivation cycling time ratio ($R_{t)}$ is the most critical one. To evaluate R_t effect, Fig. 9.8 shows a design of test structure with square shape vias. It should be pointed out that because of mask sharing with other projects, the designed square vias are 10 μm in width and 25 μm in pitch. Figure 9.9a, b show the cross section of the TSVs etched with $R_t = 1.8$ and zoomed-in view of upside, respectively. The sidewall is narrower than 7 μm (original designed value is 15 μm) with narrowest width (w) only about 4 μm. The undercut at this etching condition is about 2.5 μm and a big bow shape appears at the upside of the TSVs. Figure 9.9c, d show the cross section of the TSVs etched with $R_t = 1$ and zoomed-in view of upside, respectively. The overall sidewall is reasonably straight with the narrowest width of 14 μm. The undercut is less than 0.3 μm and no obvious bow shape appears. In order to investigate how R_t affects the sidewall of the TSVs after etching, a series of experiments are carried out. Figure 9.10 illustrates how R_t affects R_w (R_w is the ratio between the narrowest sidewall width and the original designed sidewall width). During these experiments, other etching parameters are kept as constants and are listed in Table 9.1. From Fig. 9.10, several conclusions can be made. First, larger R_t (longer etch cycling time or shorter passivation cycling time) results in thinner sidewall, second, for a specific R_t, the sidewall becomes wider at the bottom of TSVs. As a result, the TSV shows positive taped shape.

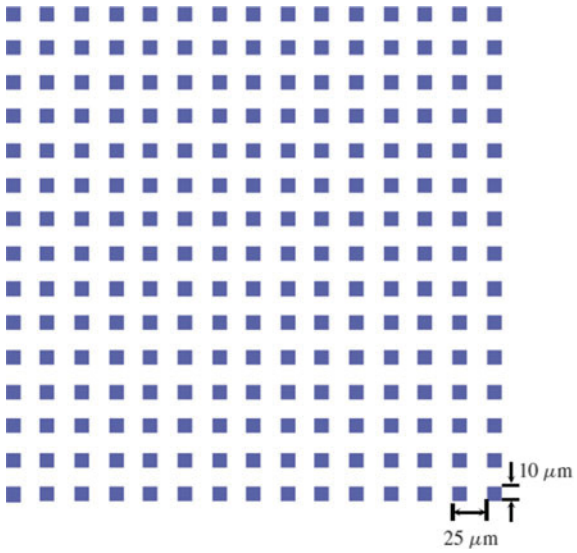


Fig. 9.8 Layout of test vehicle for evaluation of TSV etching process

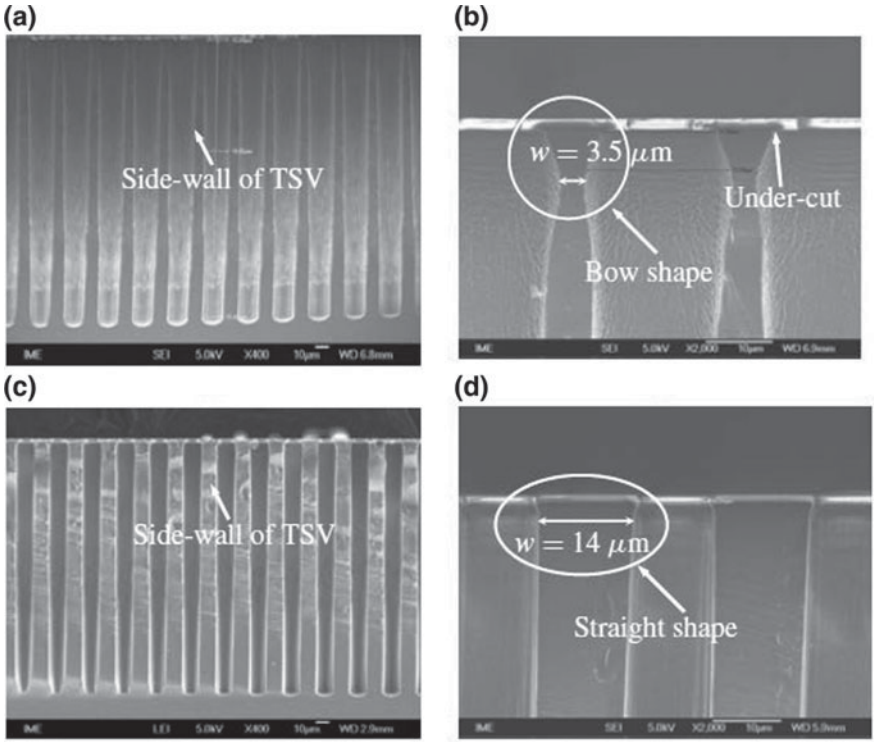


Fig. 9.9 Effects of time ratio between etch cycle and passivation cycle on undercut and bow shape of TSV. **a** Cross section of the etched TSVs when $R_t = 1.8$; the sidewall becomes narrower than 7 μm (designed width is 15 μm). **b** Upside of the TSVs when $R_t = 1.8$. **c** Cross section of the etched TSVs when $R_t = 1$; the sidewall is straight. **d** Upside of the TSVs when $R_t = 1$

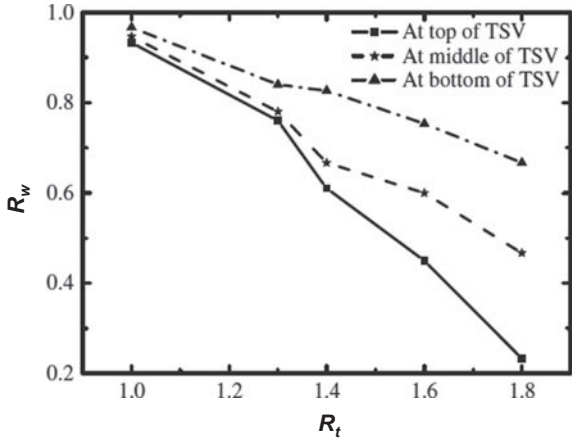


Fig. 9.10 Relationship between R_w and R_t at different positions of TSV

Table 9.1 Process parameters for DRIE of TSVs

Parameters		Values
Platten power (W)		12
Ramp rate (W/min)		0.1
Gas flow during etching cycle (sccm)	SF_6	130
	O_2	10
Gas flow during passivation cycle (sccm)	C_4F_8	100

The results can be explained as follows. During the Si etch cycle, Si is etched isotropically (as shown in Fig. 9.11a) whereas in the passivation cycle, the sidewall is protected by a thin layer of polymer (as shown in Fig. 9.11b). In the following etch step, first the polymer at the via bottom would be etched away, and then the bottom Si could be etched down (as shown in Fig. 9.11c). The alternating of etching and passivating cycles forms scallops on the sidewall of etched features. If R_t is optimized properly, straight sidewall as shown in Fig. 9.11d could be achieved. However, if R_t is too large, the polymer on the sidewall is not thick enough to protect the sidewall during the etching cycle. Therefore the scallop becomes larger (as shown in Fig. 9.11e). Besides, because of isotropic Si etch, undercut appears in the region below the SiO_2 hard-mask and increases with etch time. Especially for high aspect ratio via etch, the ion flux that arrives at the entrance of via is larger than the ion flux that arrives at the bottom of via. Therefore the Si at the entrance of via is more easily isotropic etched. As a result, with the etch process going on, the bow shape becomes larger at the entrance of via (as shown in Fig. 9.11f). In order to reduce the bow shape, R_t should be reduced, which means to reduce the etching cycle time or increase the passivation cycle time in order to make sure the passivation layer on the sidewall is thick enough to protect the sidewall during the Si etch cycle, especially for high aspect ratio vias.

9.2.7 Sidewall Passivation Results

After TSV formation, PETEOS with thickness of 2 μm is deposited from the front side of the wafer to form an insulation layer. Figure 9.12 shows the passivation results. It is found that the step coverage of the sidewall at the top and the middle of the TSV is 0.6 and 0.2 μm, respectively. At the bottom of the TSVs, the thickness of the PETEOS is 40 nm.

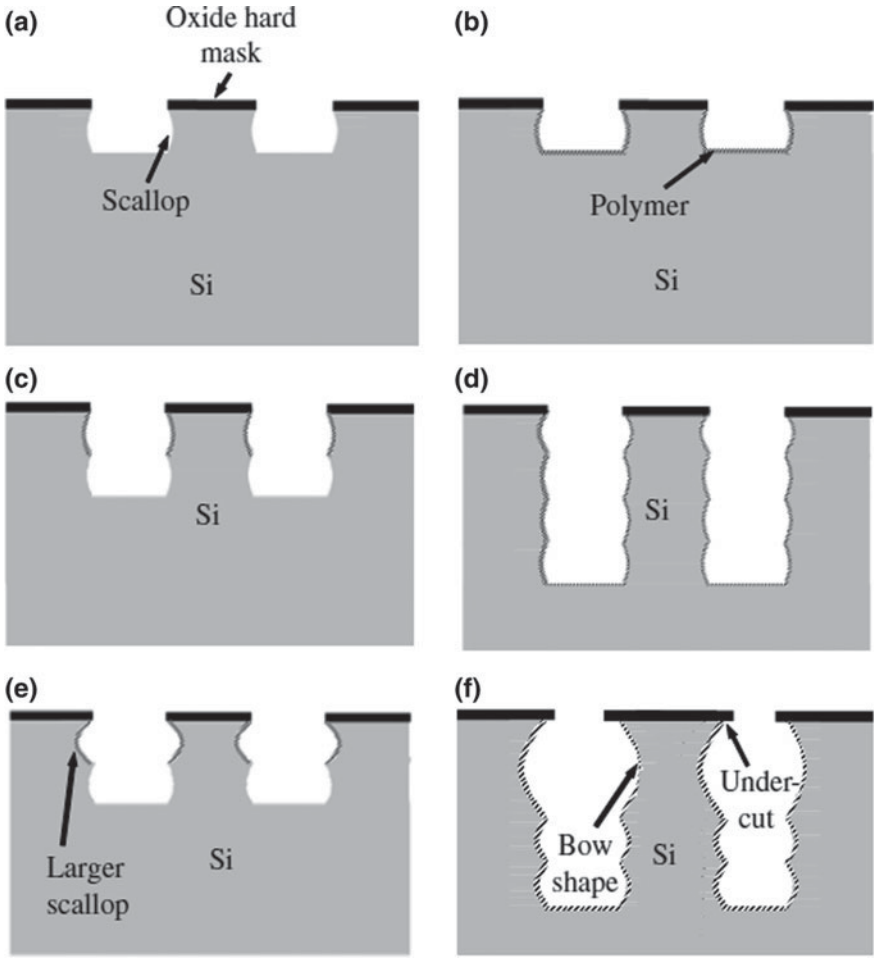


Fig. 9.11 Illustration showing DRIE of TSV process. **a** Etching cycle. **b** Passivation cycle, a thin layer of polymer coated on the sidewall. **c** Bottom polymer remove and continue Si etch. **d** Final Si via with straight shape. **e** For larger R_t, scallop becomes larger [compared to (**c**)]. **f** Final shape of Si via with larger R_t. Big bow shape appears at the entrance with larger undercut

9.2.8 Bottom-up Plating Results

Figure 9.13 shows the top view of Cu filling results. After plating, Cu overburden appears on top of the wafer, as shown in Fig. 9.13a–c. After removing the overburden, there are a few voids that remain on top of the TSVs, as shown in Fig. 9.13c. The reason for voids is that the Cu filling rate in TSV is different, and some TSVs' top surfaces are covered by the adjacent Cu overburden, as shown in Fig. 9.13c. As a result, these TSVs could not be filled completely.

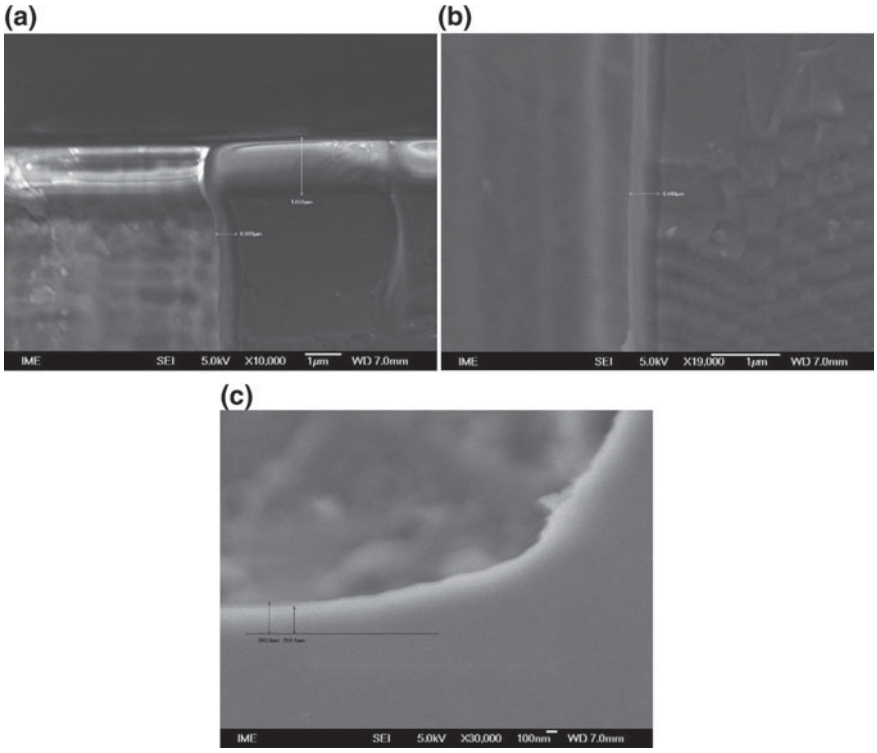


Fig. 9.12 Passivation step coverage of the **a** top: 30%, **b** passivation step coverage of the middle sidewall: 10%, and **c** passivation step coverage of the bottom: 2%

To completely remove the voids, the wafer is further thinned down for another 30–50 μm. As shown in Fig. 9.14, there is not any void and all the TSVs are fully filled with Cu. Further thinning down the Si wafer after Cu plating will lead to higher cost. Therefore optimization of Cu filling process to achieve more uniform Cu plating rate is required.

Figure 9.15 shows a cross section of the TSVs after further thinning down with another 30 μm (final thickness is 170 μm). Figure 9.15a, b show that all the TSVs are filled with Cu whereas some tiny voids still exist at the top side of the TSV. On further thinning down the wafer, those tiny voids can be fully removed. Figure 9.15c shows that there is no separation of the plated Cu from the Si via sidewall when a sputtered Ti layer is used as adhesion layer. For better adhesion and diffusion barrier, TiW, Ta, or TaN can also be used.

From Fig. 9.15a, it is seen that there is about 4 μm thick Cu plated on the backside of the wafer in order to seal the bottom of the TSV. This layer can be removed after Cu plating by using CMP method.

Wafer warpage has been measured after Cu CMP [process step (k) in Fig. 9.5] using optical FSM Echoprobe TM 413 with IR interferometry. The measured average

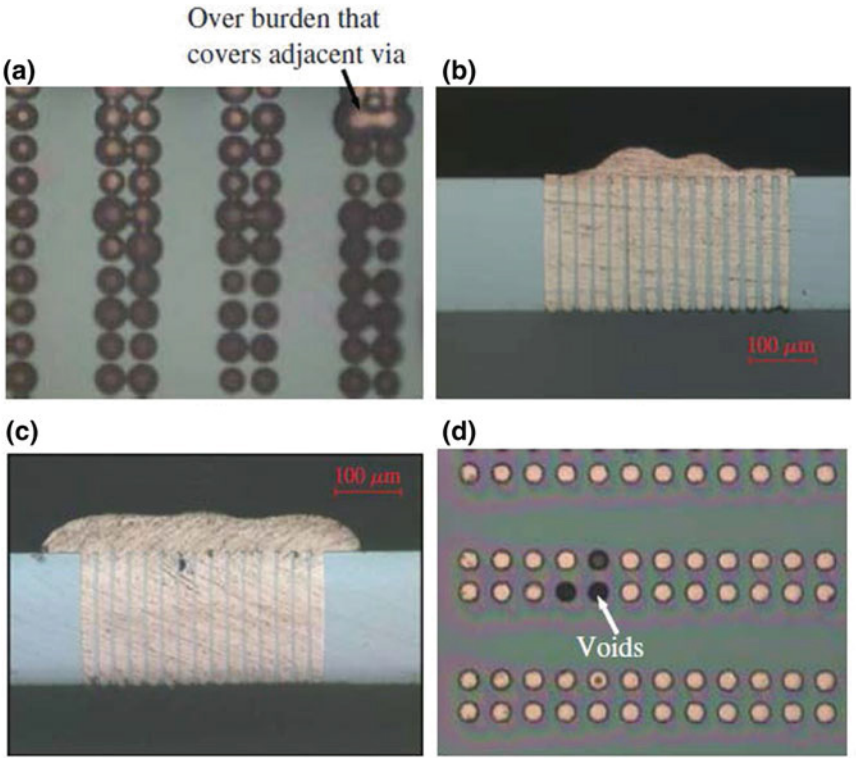


Fig. 9.13 Cu filling results **a** before CMP, **b** cross-sectional view of TSV after Cu plating and before CMP without voids, **c** cross-sectional view of TSV after Cu plating and before CMP with voids on top of TSV, and **d** after CMP, there are a few voids on top of TSVs

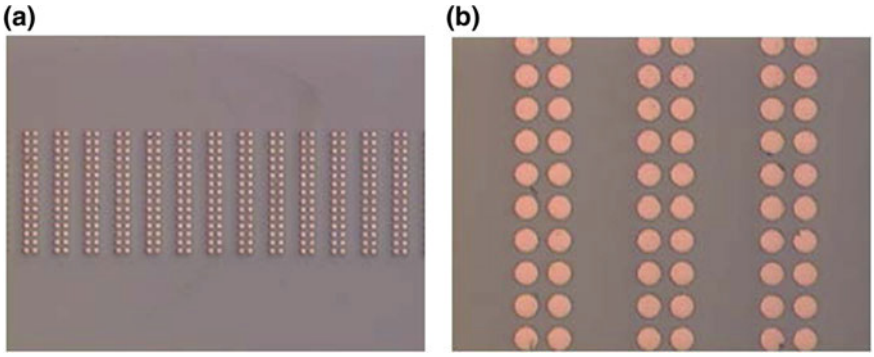


Fig. 9.14 After wafer is thinned down to another 30 μm, all the voids in TSV are removed. **a** Overview. **b** Zoomed-in view

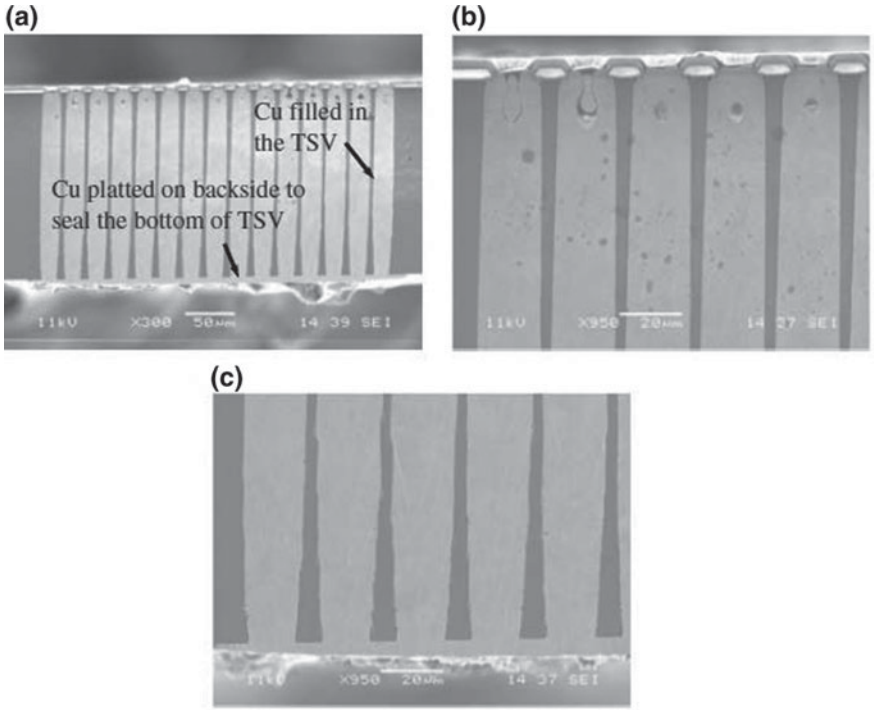


Fig. 9.15 Cross section of TSVs after Cu plating and thinning down to 170 μm shows some tiny voids at the upside of TSVs **a** overview, **b** zoomed-in view of TSV upside (with some smears on the cross-sectional surface because of polishing and cleaning process), and **c** zoomed-in view of TSV bottom side

wafer warpage is less than 100 μm. As the total area of TSV is less than 1% of the whole wafer area, TSV induced wafer warpage is low.

To evaluate the electrical performance of TSV, DC resistance of TSV has been measured. The measured average TSV resistance is 63 mΩ. Preliminary insulation measurements have been done between TSV and bulk Si. TSV capacitance and current leakage are measured by precision LCR meter and Agilent 4156C precision Semiconductor Parameter Analyzer, respectively. The average capacitance is about 2.4 pF at 1 MHz whereas the average leakage current is lower than $1E^{-10}$A under 10 V bias voltage.

9.2.9 ENIG Plating Results

Figure 9.16a shows the top view of ENIG pads on top of the TSVs. After plating, the diameter of the ENIG pads is about 4 μm larger than the diameter of TSV because of

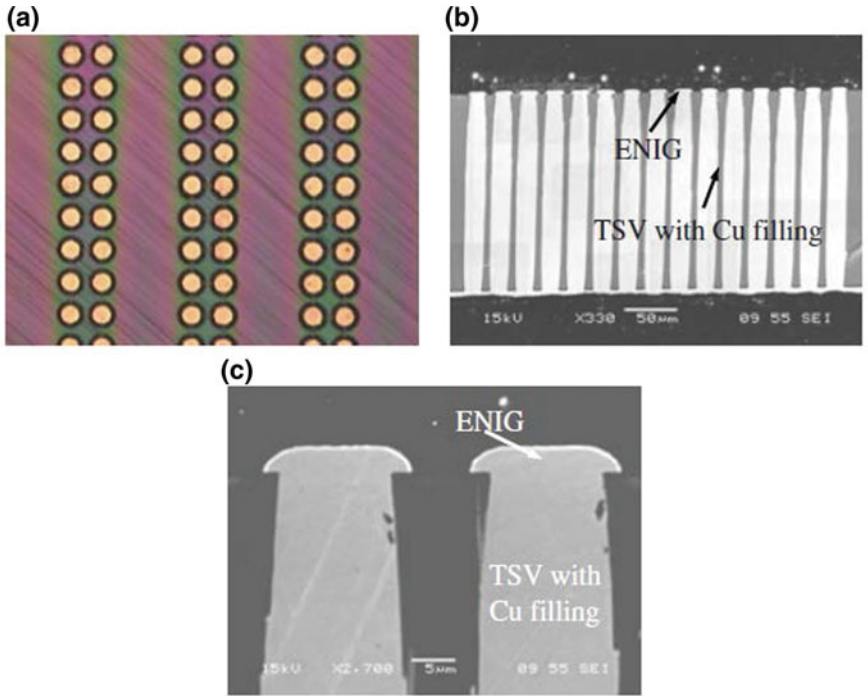


Fig. 9.16 SEM images of UBM layer of ENIG on top of TSV. **a** Top view. **b** Cross section. **c** Zoomed-in view

radial Ni growth on the passivation layer [10]. Figure 9.16b shows the cross section of ENIG pads on top of TSV and Fig. 9.16c illustrates the zoomed-in view.

9.2.10 CuSn Solder Bump Fabrication Results

After plating, a reflow is performed to reshape the microbumps and uniform bump heights are obtained. The reflow temperature is 265 °C. During reflow, a flux of WS3543 from Indium Corporation of America is used and after reflow, the wafer is cleaned in deionized (Ic) water to remove the flux residues. Figure 9.17 shows SEM (scanning electron microscope) images of the fabricated Cu pillars + Sn caps and Al pad, and Fig. 9.18 shows the FIB (focus ion beam) images of solder bumps. Figure 9.18 also indicates that after reflow, the thickness of the formed IMCs is about 1.5 μm, and occupies nearly 50% of the solder volume. However, the remaining Sn is still sufficient for assembling of the two Si chips.

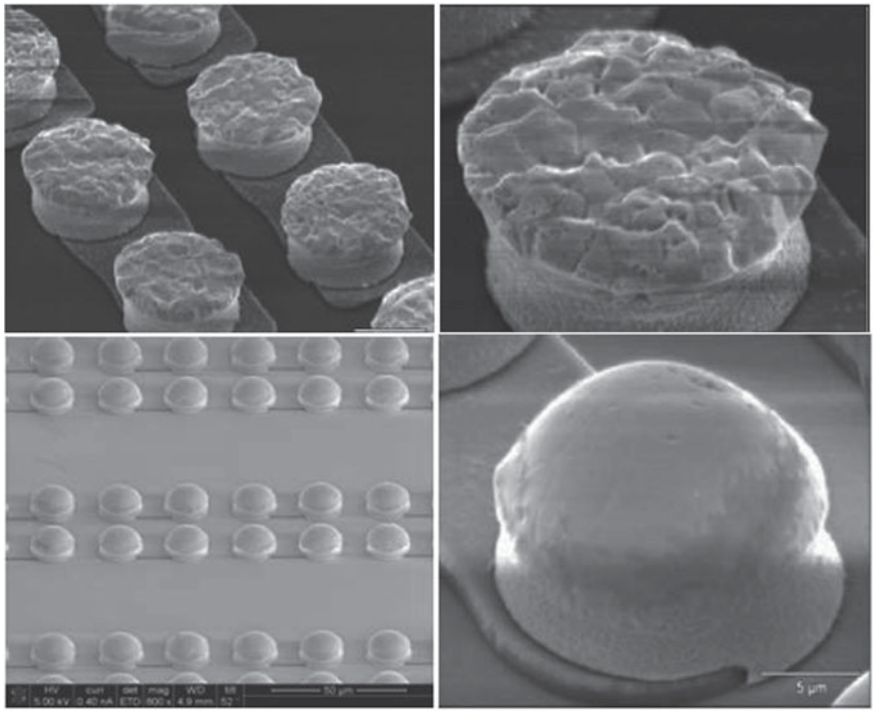


Fig. 9.17 SEM images of CuSn solder microbumps. *Top* Right after plating the CuSn on the memory chip. *Bottom* Right after reflow of the CuSn on the memory chip

9.2.11 Assembly Results

After fabrication of the CuSn solder microbumps on the top chip and the ENIG UBM pads on top of the TSVs on the bottom chip, the top chip and the bottom chip are joined together using the FC150 flip chip bonder. The joining conditions are: pressure of 20 MPa, bottom substrate temperature of 300 °C, arm temperature of 350 °C, and joining time of 60 s. The assembly process is a flux-less process because after joining, the gap between the top chip and the bottom chip is only about 10 µm. Therefore if flux is used, it is very difficult to clean it and then after underfill process, a lot of voids are formed inside the gaps. After joining, underfills with fine filler size, such as underfills of T693/R3434iHx-2 from Nagase ChemteX Corp. or U8443-14 from Namics, are used to fill the gap between the two Si chips [2]. Figure 9.19 shows the cross section of the top chip and the bottom chip joined together at selected bonding conditions. It can be seen that successful joining is achieved.

Shear test is performed to evaluate the joint strength of the assembly. The measurements are carried out by a commercially available shear tester (DAGE-SERIES-4000-T, Dage Precision Industries Ltd., Aylesbury, U.K.). The force applied to the

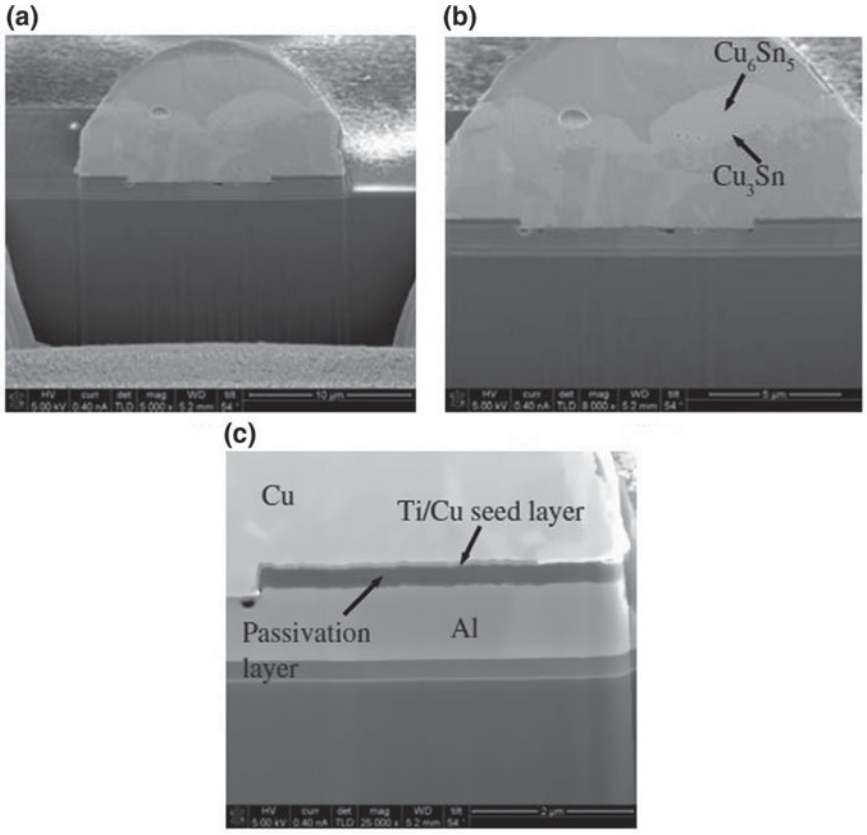


Fig. 9.18 FIB images of Cu pillar + Sn cap after reflow on the top die. **a** Overview. **b** Zoomed-in view of IMC. **c** Zoomed-in view of passivation layer and seed layer

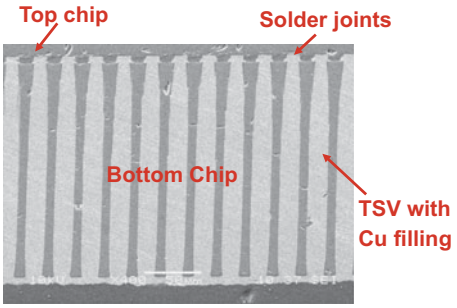


Fig. 9.19 Cross section of the top die and the bottom die joined together

assemblies provides shear in a direction parallel to the surface of the test vehicle by the shear probe. The shear speed for this evaluation is 100 μm/s and the height of the shear probe is 400 μm. The average shear strength of the joints at this bonding condition is 12.1 MPa. Temperature cycling test (−40 ↔ 125 °C, 15 min dwell, ramp at 15 °C/min) of the micro solder joints has been studied and presented in [2]. One sample out of eleven failed at 300 cycles and all the other samples passed 1000 cycles at which point the test is stopped. Reliability of chip bonding with fabricated TSV interposer need to be further studied. Mechanical modeling shows that with underfill between the top chip and the bottom chip, the normal stress at the solder micro-joints is greatly reduced and the substrate core thickness has little effect on the stress at the solder micro-joints [11].

9.2.12 Summary and Recommendations

The developments of heterogeneous integration of chip-to-chip with TSVs have been presented. Some important results and recommendations are summarized as follows [2, 12].

- The face-to-face interconnections of the memory chip and the CPU chip with TSVs achieve the highest bandwidth and electrical performance.
- The bonding of the memory chip and the CPU chip can be performed by wafer-to-wafer bonding to get the maximum throughput. Unfortunately, most to the memory chips are in rectangular shapes and the CPU chips are in square shapes. Also, their sizes are very different. Thus, these post challenges to wafer-to-wafer bonding. Memory-chip to CPU-wafer bonding could be an alternative. Unfortunately, it will occupy the bonder too long. The other way is by memory-chip to CPU-chip bonding. However, this yields the minimum throughput.
- Solder microbumps with 25 μm in pitch and 15 μm in pad diameter have been developed successfully. The ultrafine pitch and high-density bump array can be used for heterogeneous integration with high-density interconnections.
- TSVs with aspect ratio larger than 10 have been fabricated in the bottom chip (wafer) with DRIE method. During the DRIE process, it is found that when the etching cycle time is 80% longer than the passivation cycle time, the undercut is larger than 2 μm and an apparent bow shape appears.
- After Cu plating, there are a few voids that exist on top of the TSV, which can be removed by further thinning of the wafer. The Cu filling process still needs to be optimized to achieve more uniform Cu plating in the TSVs.
- At optimized bonding conditions, good joining with shear strength of 12.1 MPa can be achieved between the Cu/Sn solder microbumps and the ENIG pads on top of the TSVs.

9.3 Heterogeneous Integration of Chip-to-Chip Without TSVs

9.3.1 Test Vehicle and Fabrication

The packaging structure shown in Fig. 9.20 could be a very low cost package for high-performance, high-density, low-power-consumption, and possibly for wide-bandwidth applications. The heat spreader/sink is optional. The chip-to-chip interconnects are face-to-face (the shortest distance), and the signals, powers, grounds, etc. easily can go to the next layer of interconnect through solder bumps. This heterogeneous integration is the most cost-effective package (memory as the daughter chip and logic as the mother chip). It should be emphasized that there are no TSVs in both chips.

The test vehicle is a silicon-stacked module, as shown in Fig. 9.21 [13]. The assembled stacked module consisted of a top silicon chip known as the *daughter chip* and a bottom silicon chip known as the *mother chip*, which are fabricated in wafers. On the daughter chip, there are bumps made of Cu stud (pillar) coated with the AuSn solder. On the mother chip, there are electroless NiAu UBM for the bumps from the daughter chip and AuSn solder bumps for the next level of interconnect, such as substrates. For both chips used in this test, the pads are interconnected in an alternating pattern so as to provide a daisy-chain connection when they are soldered together. There are 20 pads on the daughter chip, and they are arranged in two rows, as shown in Fig. 9.21. The materials and dimensions of the key elements of the Si-stacked module are listed in Table 9.2. This package module eventually is attached to either a rigid or flexible substrate, as shown in Fig. 9.20.

AuSn solders are especially suited for optoelectronics and medical packaging. Most medical and optoelectronic devices have to be soldered in a fluxless process, which is possible using AuSn solders, as shown in the phase diagram in Fig. 9.22. Also, 80 wt%Au20 wt%Sn solder is used widely because of its advantages: (1) high strength, (2) high corrosion resistance, and (3) high fatigue resistance. Thus the

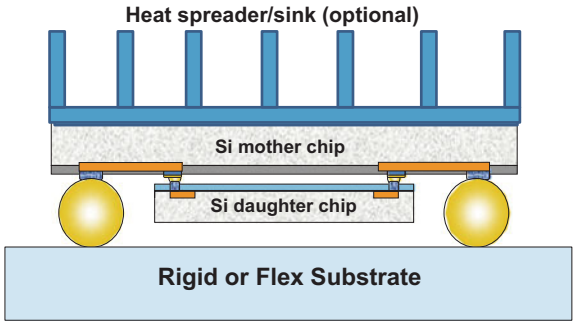


Fig. 9.20 Heterogeneous integration of chip-to-chip without TSVs

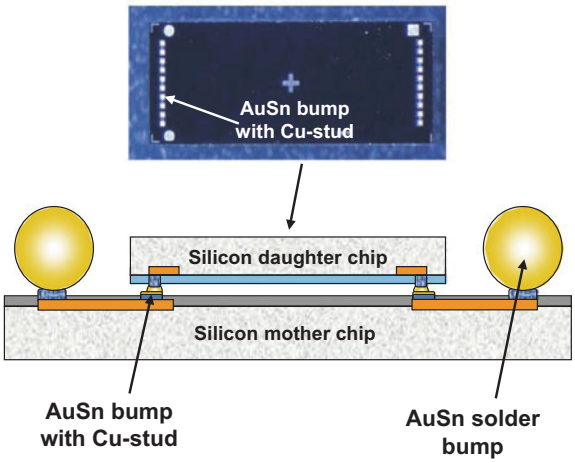


Fig. 9.21 Stacked silicon module (daughter chip and mother chip) and a close look at the daughter chip

Table 9.2 Materials and geometry of key elements of the chip-to-chip module

Package type	Silicon stacked module	
Test die	Daughter	Mother
Die size (mm)	3.405 × 1.34 × 0.06	4.793 × 1.34 × 0.13
Pad opening	FC pad 30 μm	FC pad 30 μm
Pad pitch	100 μm	100 μm
Bump type, height	Au80Sn20 on Cu pillar, 23.5 μm	Au80Sn20, 125 μm
Under pump	Al	Electroless NiAu

Au20Sn solder system usually is selected as the interconnect material for fluxless flip-chip applications. Besides AuSn solder, SnAg is also considered.

AuSn solder can be manufactured by various methods, such as electron-beam evaporation, electron deposition, and paste and solder perform. Among these methods, evaporated solder allows more accurate control of dimensions and positions. Therefore, after UBM patterning, a sequence of alternating layers of Au and Sn are deposited to form an AuSn layered structure. Some of the advantages of using the electron-beam evaporation process for AuSn deposition include: (a) the amount of oxide formed after deposition will be reduced, (b) the thickness and position of the solder can be controlled precisely, (c) the Au deposition rate is high, and (d) uniform AuSn thickness can be achieved across a 200 mm wafer.

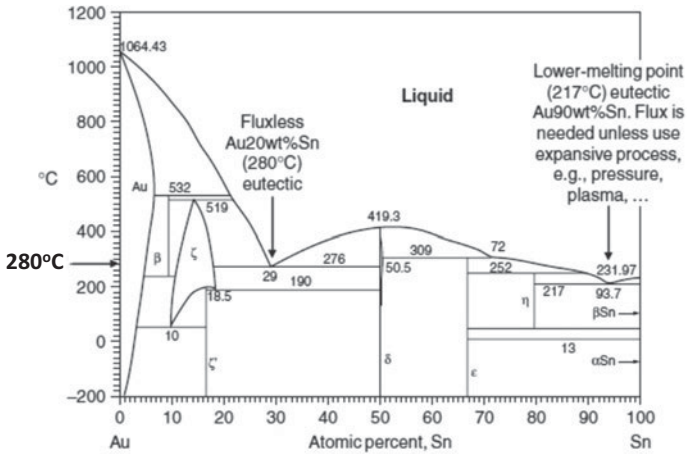


Fig. 9.22 AuSn solder phase diagram

9.3.2 Test Vehicle Fabrication

p-Type silicon (100) wafers of 200 mm diameter with a thin electrical insulating film of 5000 Å of SiO_2 are used for fabricating the test vehicle. Figure 9.23 provides a schematic of the process for making the AuSn solder bumps on the daughter die. The first step is to deposit an AlCu layer on the Si wafer and then pattern the metal pads with daisy chains and etch the AlCu layer. Second, passivation layers of 5000 Å of SiO_2/5000 Å of SiN are deposited, and then the passivation layer is patterned using dry etching to open the metal pad. The Ti/Cu seed layer is sputtered as a conductive layer for a further mini-Cu-stud electroplating process. Then a 20 μm-thick dry-film photoresist is laminated using a hot-roll laminator and ultraviolet (UV) light employing an EVG 640 contact-mask aligner followed by developing the photoresist to define the UBM pads. These patterned vias are filled with copper up to 18–20 μm using the RENA 200 mm wafer electroplating tool, which is a fountain-type (cup-type) tool in which Sperolyte CuSO4-based solution (Atotech Pte, Ltd.) is used as the electrolyte solution. Then layers 2200 Å thick of Au and 2000 Å thick of Sn are deposited alternatively using the electron-beam evaporator. A total of 16 layers are deposited to achieve a 3.5 μm-thick AuSn bump on the mini-Cu stud. These AuSn layers are deposited on the whole wafer surface, but the AuSn on the dry-film layer could be removed using the lift-off process during dry-film stripping, and the AuSn remained only on the Cu stud owing to the adhesion of these layers with the Cu.

After the dry-film stripping, the Ti/Cu seed layers are etched off one by one using a selective wet-etching chemical to complete the AuSn solder-bump fabrication, as shown in Fig. 9.23. These AuSn layers melt and form homogeneous Au20Sn solder joints during reflow in the assembly process. Figure 9.24 shows the AuSn solder bump, where a 3.5 μm thickness of AuSn is deposited on a 20 μm-thick Cu stud by

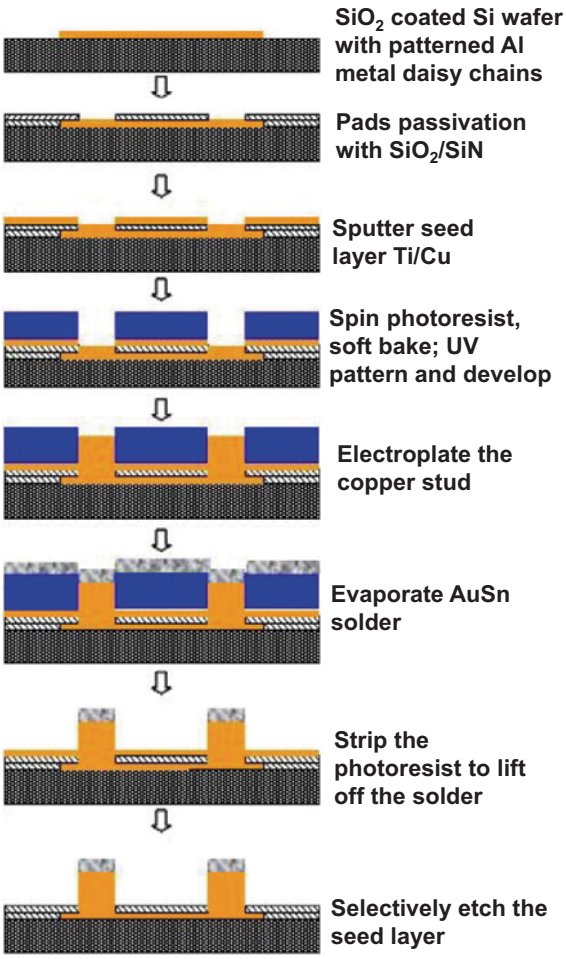


Fig. 9.23 Fabrication process of the AuSn solder bump on the daughter-die wafer

the evaporation process. The AuSn solder bumps are distributed at a 100 μm pitch along the two sides of the daughter die, and they are quite uniform, as the figure shows.

Figure 9.25 shows the bumps on the mother die—namely, the AuSn solder bump (which will not be discussed in this section) and the electroless NiAu UBM. The fabrication process for the mother die is the same as for the daughter die up to the AlCu metal pads being patterned for the daisy chain and metal pads' passivation opening. Then the electroless NiAu layers are deposited as the UBM, as shown in Fig. 9.25.

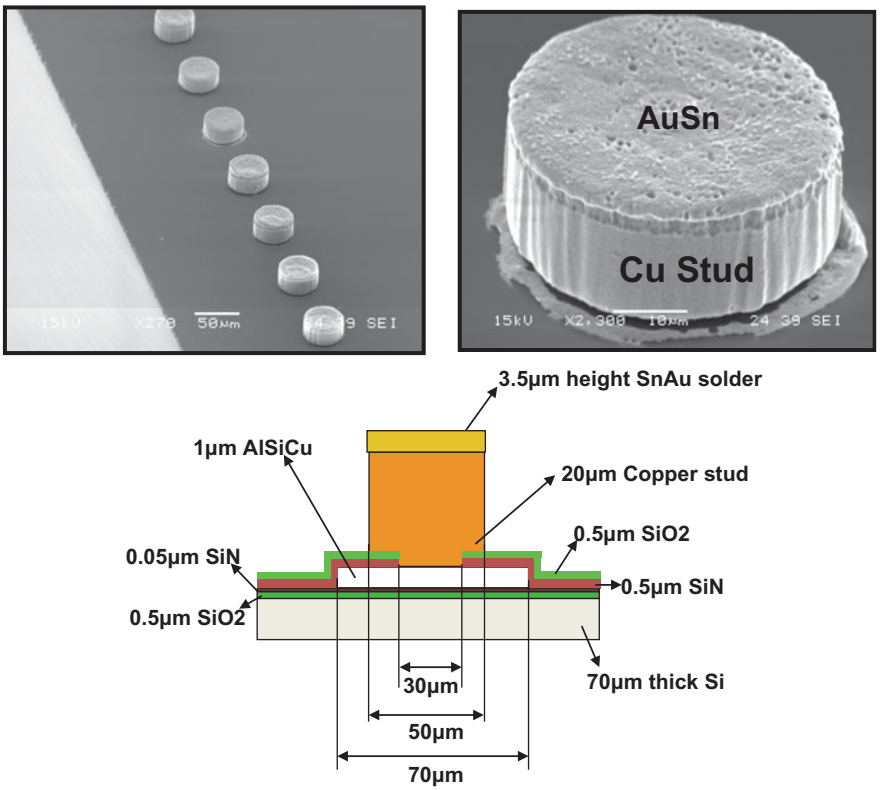


Fig. 9.24 Dimensions and uniformity of the AuSn solder bump on the daughter-chip wafer by the electron-beam evaporation process

9.3.3 Chip-to-Wafer Assembly

The overall assembly process of the AuSn solder-bumped daughter die on the mother die is by a chip-to-wafer (C2W) bonding method; that is, first dice the daughter-die wafer into individual dies and then pick up the good daughter dies and bond them on good mother dies of the mother-die wafer, as shown in Fig. 9.26.

The bonding process is done with the flip-chip bonder FC150 from Karl Suss, as shown in Fig. 9.27. The assembly is carried out using non-reflowed bumps with N2 purging during bonding. Argon sputter cleaning was performed on the daughter die and mother die (on a wafer) prior to the bonding process. The main challenge in AuSn flip-chip bonding is to achieve a good AuSn wetting on the electronless NiAu UBM bond pad with minimum AuSn solder squeezed between the bump and the UBM after bonding. In addition to bump-height coplanarity, the assembly process optimization in terms of alignment accuracy, bond force, bond temperature, and bond time on contact resistance, AuSn wetting, and AuSn solder-joint shape is investigated.

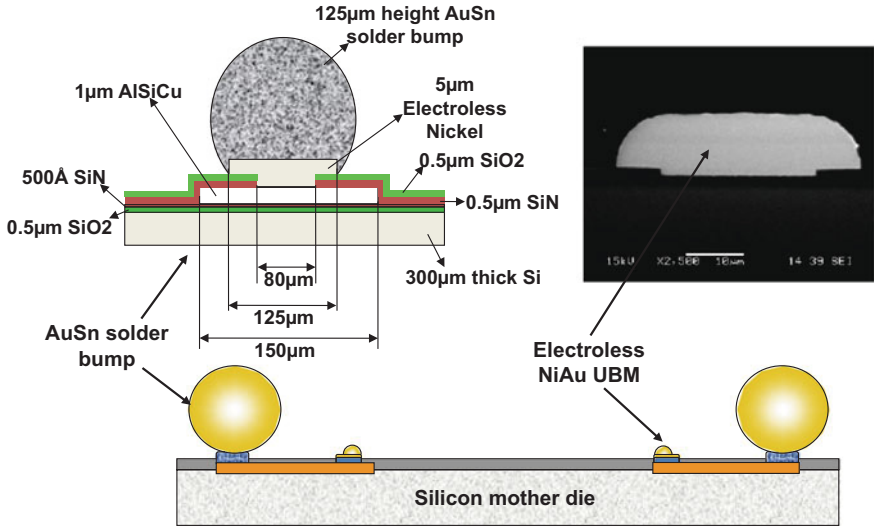


Fig. 9.25 Dimensions of and close-up look at the electronless NiAu UBM on the mother chip

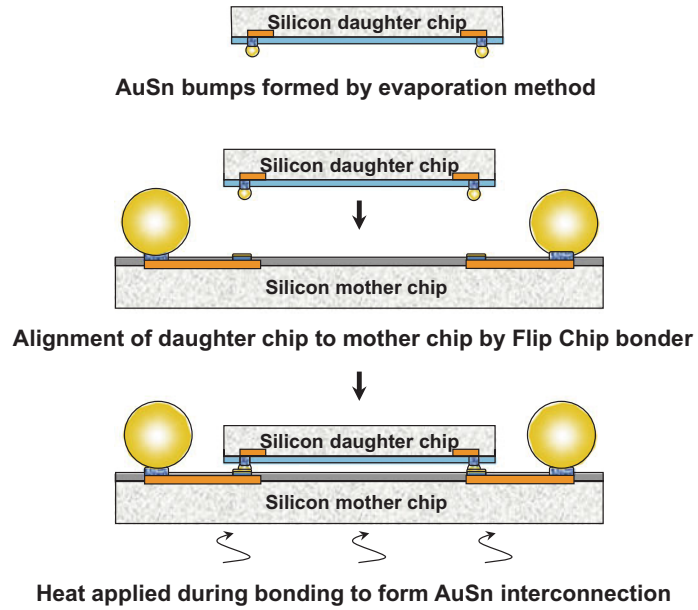


Fig. 9.26 Overall chip-to-chip module assembly process

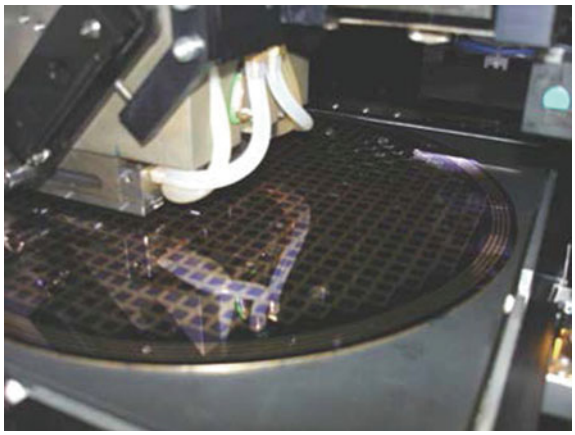


Fig. 9.27 FC150 chip-to-wafer (C2W) bonder

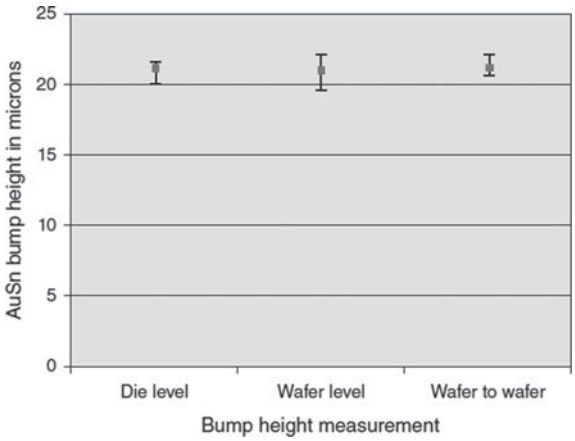


Fig. 9.28 AuSn bump-height measurement on various wafers

9.3.4 Bump-Height Coplanarity

It is important to characterize the Au bump height before the flip chip attachment process because a non-uniform bump height will result in weak joints and even open continuity. Figure 9.28 shows the bump-height measurements in an acceptable range of a maximum 2.5 μm at the die level and 1.5 μm at the wafer-to-wafer level.

9.3.5 Alignment Accuracy

In the flip-chip conventional soldering process, solder bumps are dipped into flux and attached onto the substrate pads before being subjected to the reflow process. During the oven reflow process, the solder bump on the die is able to self-align to the

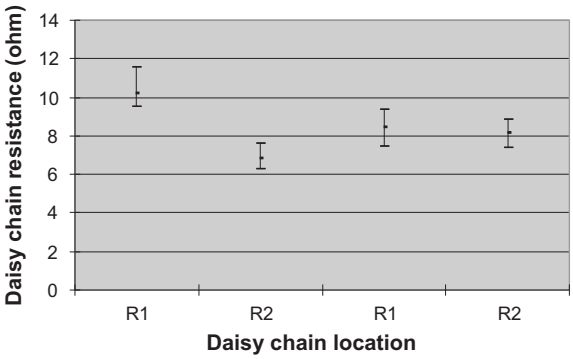


Fig. 9.29 C2W bonding-alignment accuracy versus contact-resistance measurements

substrate pads and form good solder interconnections. However, with thermocompression bonding, the solder is unable to self-align during assembly. Hence bonding alignment accuracy becomes critical, especially when using large dies with solder bumps. Precise bonding equipment with good alignment and bonding accuracy is required to form a good AuSn interconnect with stable contact resistance and good AuSn wetting on the substrate pad.

The contact resistance of the interconnects is characterized at different bonding alignment accuracies, as shown in Fig. 9.29. A bond force of 0.8 kg is applied during the flip-chip bonding process. There is a significant difference in the contact resistance and the AuSn wetting on the electroless NiAu bond pads on misaligned AuSn bumps to electroless NiAu pads, compared with 100% aligned AuSn bumps to electroless NiAu pads, as shown in Fig. 9.30. This mode of joint configuration results in poor AuSn wetting on the bond pad and higher resistance readings. One of the reasons for this is that there is no self-alignment of the AuSn solder bumps to the electroless NiAu UBM after bonding. The AuSn solder is unable to wet the electroless NiAu UBM if there is a great difference in the misalignment offset. On the other hand, for the 100% aligned bonding, stable contact resistance and good AuSn wetting are observed on the electroless NiAu UBM. The contact resistances on the two daisy chains measured are lower and more consistent than the resistance measured on misaligned bonding. The cross section of a good alignment interconnect is shown in Fig. 9.31.

9.3.6 C2W Design of Experiments (DoE)

(a) **Three-Factor DoE**

With the different assembly process issues addressed, actual assembly of the test vehicle is carried out without underfill according to the three-factor DoE (Table 9.3). Three different bond forces—two bond temperatures and time—are evaluated to

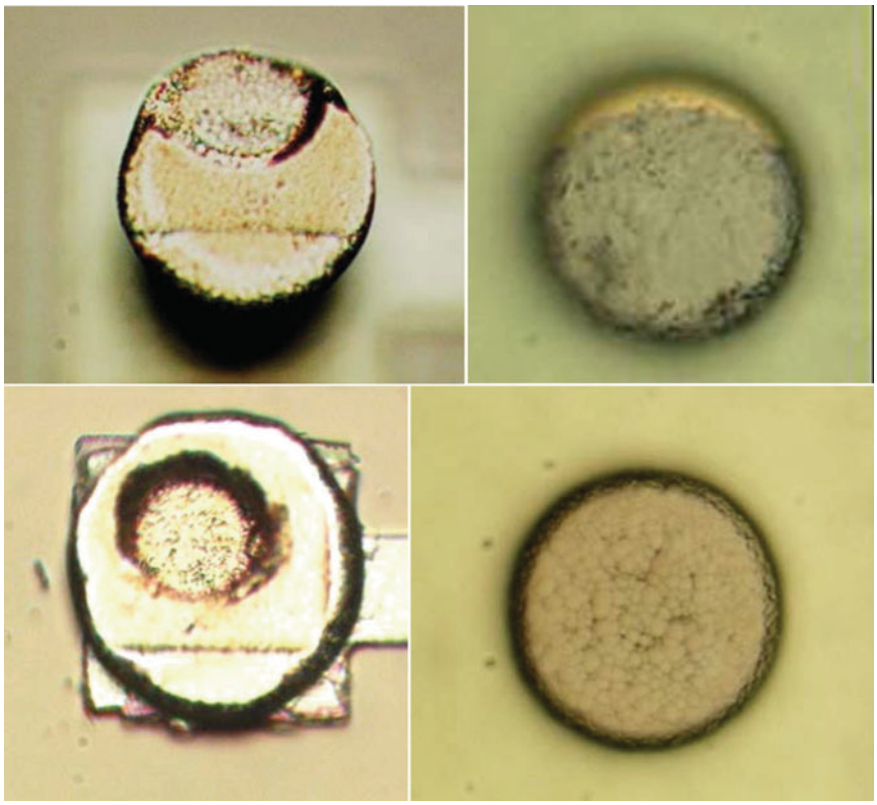


Fig. 9.30 AuSn wetting failure modes. (Top) Misaligned bonding; (Bottom) 100% bonding alignment. Also, (Left) daughter Chips; (Right) mother chips

Fig. 9.31 Cross section of a good AuSn solder joint

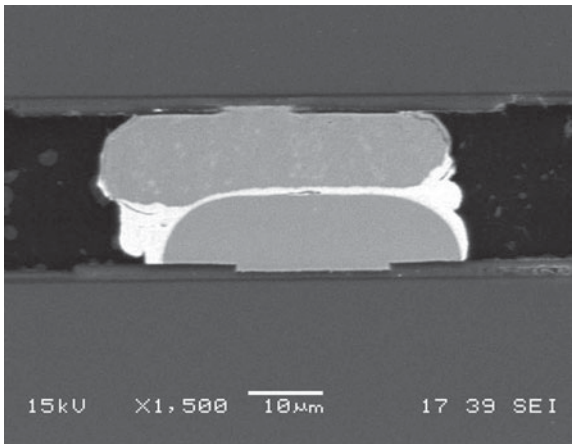


Table 9.3 Three-factor DoE of C2W bonding evaluation

Batch	Bond force (kg)	Bond temperature (°C)	Bond time (s)
A	0.4	290	15
B		315	15
C	0.8	290	15
D		315	15
E	0.1	290	15
F		315	15

Table 9.4 C2W bonding with various combinations of force, temperature, and speed

Factors	Variations	Response
Bond force (kg)	0.4, 0.8, 1	Contact resistance AuSn joint shape AuSn wetting
Bond temperature (°C)	290, 315	
Bond time (s)	15	

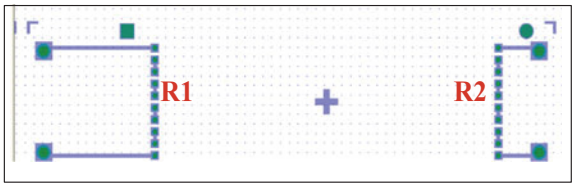


Fig. 9.32 Resistance measurements through the chain on the mother chip

determine the suitable bond force and bond temperature required to achieve consistent resistance measurements, good AuSn wetting, and AuSn joint formation. The three selected bond forces ranged from 0.4 to 1 kg (Table 9.4). The assembly yields are characterized, and the contact resistances are monitored via a daisy-chain network, as shown in Fig. 9.32.

(b) **DoE Results**

The bond force has a significant influence on the interconnection resistance and AuSn joint formation. Figure 9.33 shows that stable contact resistance can be achieved at 0.8 and 1 kg of bond forces. However, 1 kg is undesirable because it results in chip passivation cracking at the Al pad–UBM interface, as shown in Fig. 9.34. Furthermore, a high bonding force tends to squeeze out the AuSn eutectic solder between the bump and bond pad and results in poor AuSn wetting on the bond pad. Figure 9.35 shows a cross-sectional view of the AuSn assembly at 1 kg of bond force. The findings also suggested that the contact resistance is more sensitive to bond force than to bond temperature and bond time.

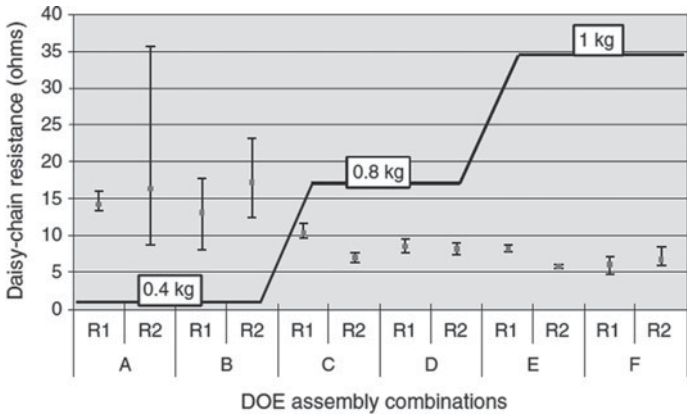


Fig. 9.33 Contact-resistance measurements from the DoE assemblies

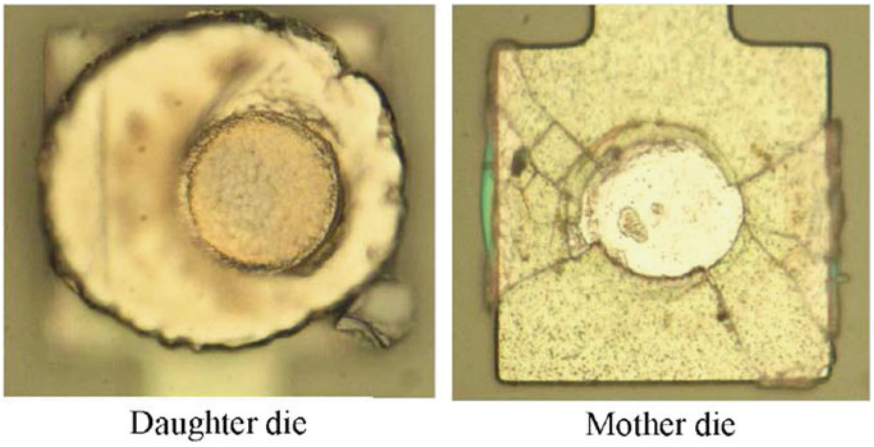


Fig. 9.34 Passivation crack at high bonding force (1 kg)

9.3.7 Reliability Tests and Results

A set (batch D) of test-vehicle assemblies (without underfill) is subjected to temperature cycle testing ($-40 \leftrightarrow 125$ °C) to access the thermal fatigue characteristics of the AuSn interconnects [12]. The electrical contact resistance is measured prior to reliability testing and at every 25 cycles during the testing for 100 cycles. The criteria for failure would be an open continuity in the resistance value (∞) of the daisy chain. This set of samples passed the TC test without open continuity up to 100 cycles, as shown in Fig. 9.36. A minimum change of less than 10 percent in the contact resistance is observed for bond force at 0.8 kg. This suggests that the interconnect configuration of a homogeneous AuSn eutectic solder with direct con-

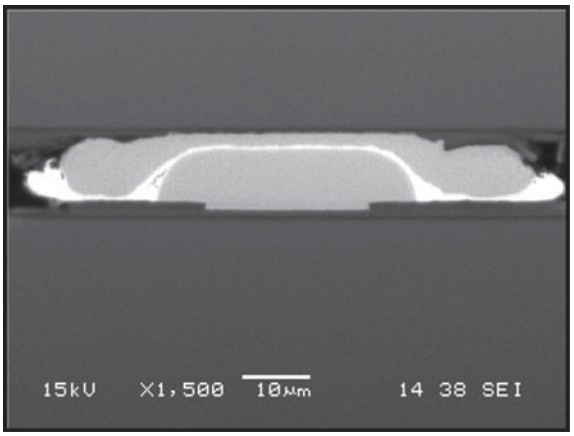


Fig. 9.35 Cross section of an AuSn assembly made by high bonding force (1 kg)

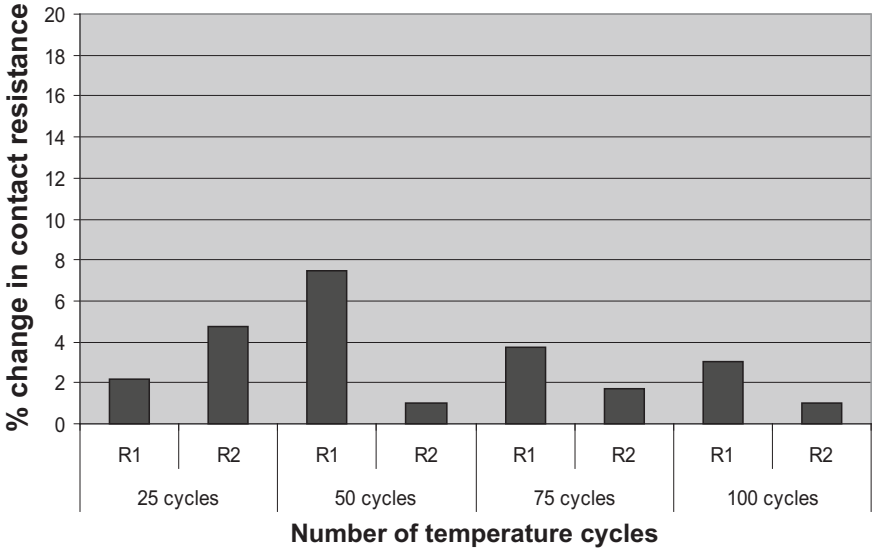


Fig. 9.36 Percentage changes in contact resistance during temperature cycles ($-40 \leftrightarrow +125$ °C)

tact to the electroless NiAu UBM bond pad is robust and able to withstand the TC conditions. The results indicate that stability in contact resistances and good reliability performance can be achieved in combination D (bonding temperature = 315 °C; bonding time = 15 s) at 0.8 kg of bond force.

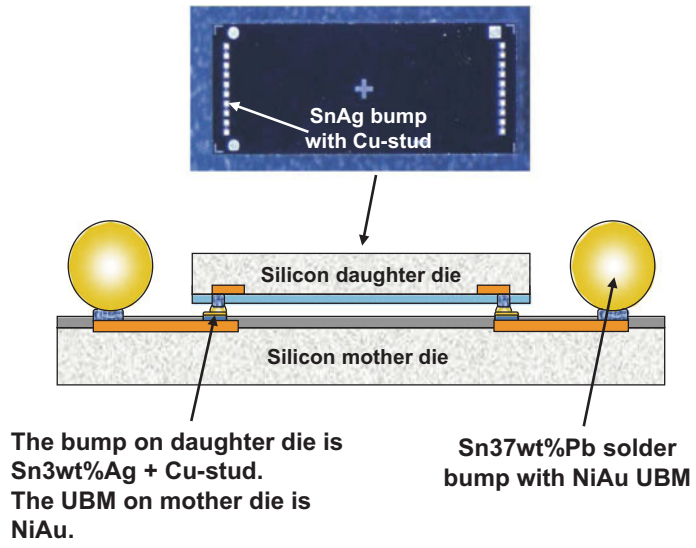


Fig. 9.37 Stacked silicon module (daughter chip and mother chip) with SnAg lead-free solder

9.3.7.1 3D IC Packaging with SnAg Interconnects

Figure 9.37 shows the same daughter chip and mother chip but with a different solder system. Instead of the AuSn solder, the Sn3 wt%Ag + Cu stud is considered on the daughter chip, as shown in Fig. 9.38. Also, the solder ball of the chip-scale package (CSP) on the mother chip is replaced by Sn37 wt%Pb. The focus, of course, is on the reliability of the SnAg solder joints between the daughter chip and mother chip [13]. Prior to assembly, the daughter chip wafer with a 40 μm height of SnAg + Cu-stud microbumps is thinned down to 70 μm, and the mother chip wafer with a 200 μm height of CSP SnPb + UBM microbumps is thinned down to 300 μm, as shown in Fig. 9.39. Figure 9.40 shows a cross section of the assembly where the underfill is applied. It should be pointed out that the solder joints are under natural reflow, and because of the surface tension of the molten solder, the shape of the solder joints is nice and smooth, which is very different from the C2W bonding of AuSn solder joints.

After assembly, the samples are subjected to unbiased highly accelerated stress testing (uHAST): +130 °C, 85% relative humidity (RH), 96 h; MST L3: 30 °C, 60%RH, 192 h, three reflows at 260 °C; MST L1: 85 °C, 85%RH, 168 h, three reflows at 260 °C; HTS: +125 °C, 1000 h; and TC: +125 ↔ −55 °C, 15-min dwell, 15 °C/min ramp, 1000 cycles. A typical image of failed samples after 1000 cycles is shown in Fig. 9.41. The crack initiates near the corner of the interface between the intermetallic compounds (IMCs; Cu_6Sn_5) and the bulk solder and then propagates through the solder joint.

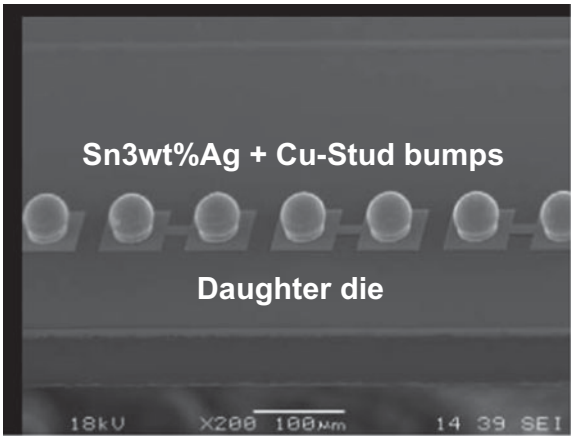


Fig. 9.38 Lead-free Sn3 wt%Ag + Cu-stud (~40 μm) bumps on daughter chip

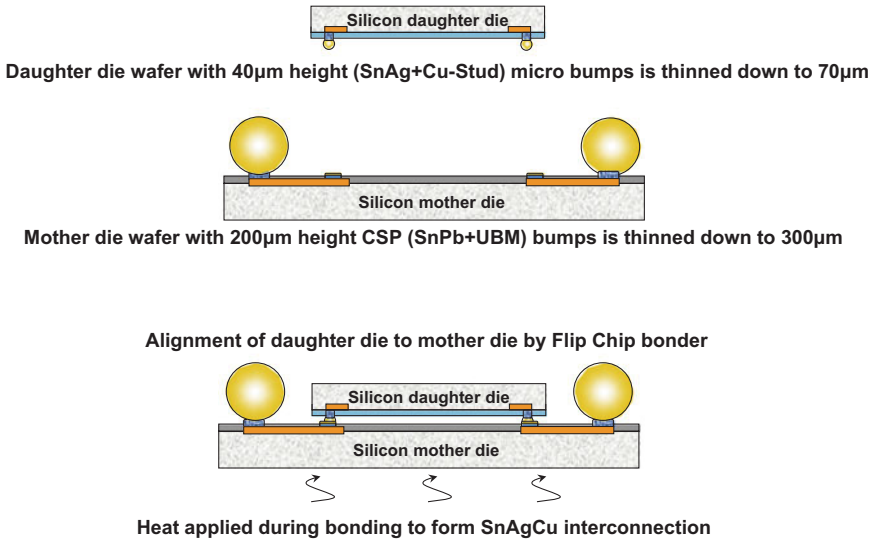


Fig. 9.39 Overall chip-to-chip module assembly process with SnAg solder

9.3.8 Summary and Recommendations

Some important results and recommendations are summarized as follows [13, 14]:

- The face-to-face interconnections of the daughter chip and the mother chip without TSVs but with solder bumps achieve the low-cost solutions. These kinds of interconnects are suitable for mobile and portable products such as medical devices.

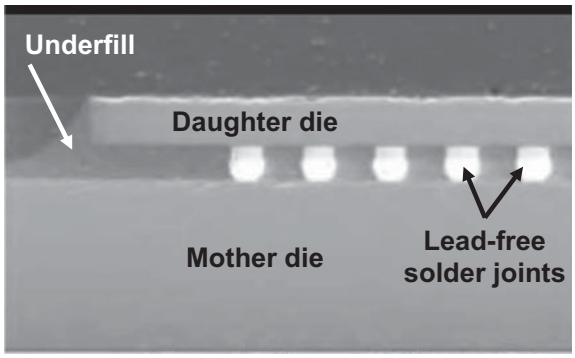


Fig. 9.40 Daughter die assembled on mother die with SnAg solder joints

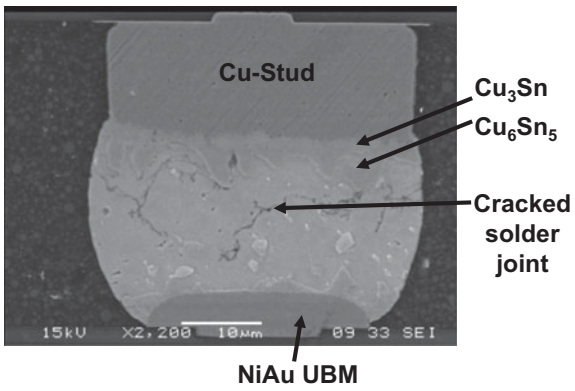


Fig. 9.41 Failed sample after high-temperature storage test, moisture sensitivity test levels 1 and 3, and 1000-thermal-cycles test

- Uniform bump coplanarity at the die level (± 3.5 µm) is required to ensure that uniform pressure can be applied on the test chip and form good AuSn interconnects.
- Stable contact resistance ($\pm 2\ \Omega$) and good AuSn wetting on the electroless NiAu pads are achieved on 100% aligned bonding at 0.8 kg of bond force.
- Assembly results show that samples assembled at high bonding force (1 kg) are undesirable because this force results in chip passivation cracking at the Al pad-UBM interface. Furthermore, a high bonding force tends to squeeze out the AuSn eutectic solder between the bump and bond pad and results in poor AuSn wetting on the bond pad.
- Temperature-cycling results show that stable contact resistances ($\pm 9\ \Omega$) and good reliability performance (>100 temperature cycles) can be achieved without underfill at 0.8 kg of bond force.
- More important, the results of this work will serve as a reference for industries establishing flip-chip assemblies using AuSn fluxless solder-bump technology.

- Chip-to-wafer flip chip natural reflow assembly process was demonstrated (with good alignments) for SnAg micro bumps of 40 μm height at 100 μm pitch. Underfill process also was demonstrated (without voids) for micro bumps at 100 μm pitch. The stacked packages have passed the JEDEC standard package level reliability tests, in terms of thermal cycling, high temperature storage, moisture sensitivity level 1 and level 3, and uHAST.

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Chapter 10
Heterogeneous Integration of CIS, LED, MEMS, and VCSEL



10.1 Introduction

In this chapter, the heterogeneous integration of CIS (CMOS image sensor), heterogeneous integration of LED (light-emitting diode), heterogeneous integration of MEMS (microelectromechanical *s*ystems), and heterogeneous integration of VCSEL (vertical cavity surface emitted laser) and PD (photodiode) detector will be presented. Emphasis is placed on providing some examples of each of these heterogeneous integrations.

10.2 Heterogeneous Integration of CIS

The basic function of CMOS (complementary metal-oxide semiconductor) image sensor (CIS) is to convert light (photons) into electronic signals (electrons). CIS has a huge market with portable, mobile, wearable, and automotive products and is a key element of the IoTs (Internet of Things). For example, smartphones and tablets use CISs for their cameras, and automobiles use CISs for their machine visions. In general, a CIS consists of a matrix of micro lens, transistors and metal wiring, and PD (photodiode) [1–7]. In this section, 3D CIS and IC heterogeneous integration is presented. Emphasis is placed on a 3D CIS and IC stacking [3, 4] and a 3D heterogeneous integration of CIS and processor IC [5].

10.2.1 Front-Illuminated-CIS and Back-Illuminated-CIS

There are two different kinds of CIS, namely FI (front-illuminated) CIS and BI (back-illuminated) CIS. For FI-CIS, the matrix of micro lens is at the front, transistors and metal wiring at the middle, and PD (photodiode) detector at the deep bottom (back)

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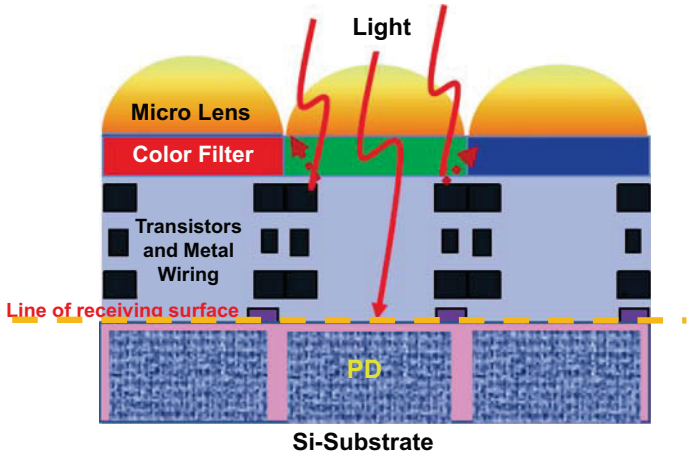


Fig. 10.1 Front-illuminated CIS. Some of the lights are blocked (reflected) by the transistors and metal wirings

of the wafer surface, as shown in Fig. 10.1. The transistors and metal wirings at the surface of the Si substrate reflect some of the light and thus the PD can only receive the remainder of the incoming light.

A BI-CIS contains the same elements, but orients the transistors and metal wiring behind the PD layer by flipping the silicon wafer during manufacturing and then thinning its reverse side so that light can strike the PD layer without passing through the transistors and metal wiring layer as shown schematically in the top of Fig. 10.2. Compared to FI-CIS, BI-CIS can improve the chance of an input photon captured from about 60% to over 90% [7]. However, BI-CIS leads to problems such as cross-talk, which causes noise, dark current, and color mixture between adjacent pixels that yield to image degradation. To overcome this issue, Sony has developed a unique PD structure [2]. Above the illuminated side, a metal light shield (as shown in the bottom of Fig. 10.2) that is formed among the photodiodes to reduce crosstalk in the pixel array achieves good color separation [2].

10.2.2 3D CIS and IC Heterogeneous Integration

The BI-CISs [1, 2] shown in Fig. 10.2 combine the pixel part and logic circuit part into a single chip, which is supported by a Si-substrate, Fig. 10.3a. Sony separates the CIS pixel chip and the logic circuit chip (i.e., the Si-substrate is replaced by the logic circuit chip) and stacks them in a 3D manner [3], Fig. 10.3b.

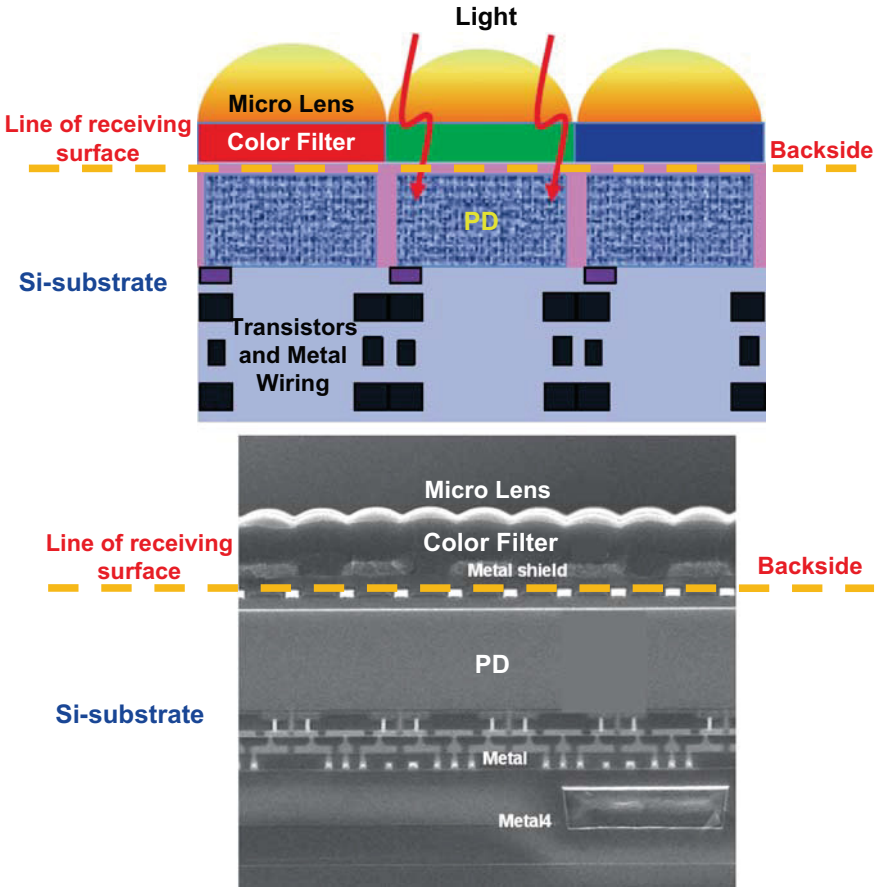


Fig. 10.2 (Top) Schematic of back-illuminated CIS. (Bottom) Cross-section SEM image of a BI-CIS

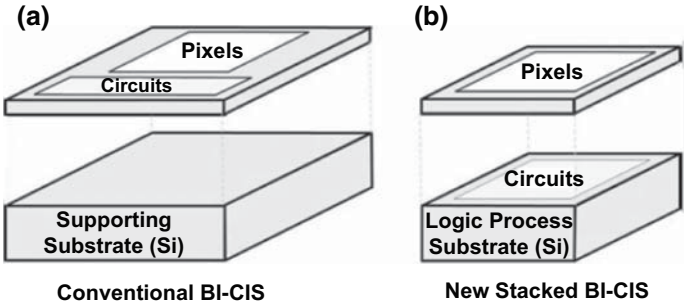


Fig. 10.3 BI-CIS: **a** conventional versus **b** new 3D stacking

(a) **The Structure**

Figure 10.3a shows the conventional BI-CIS [1, 2] and Fig. 10.3b shows the new 3D stacked BI-CIS [3]. It can be seen that the new BI-CIS consists of two chips, the CIS pixel chip and the logic circuit chip and they are vertically connected through TSVs (through-silicon vias) around their edges as shown in Fig. 10.4. The advantages of this new design are that (a) more pixels can be placed on the same CIS pixel chip size (or smaller chip size can be used for the same amount of pixels) and (b) the CIS pixel chip and logic chip can be fabricated separately with different process technologies. As a result, the CIS chip size is reduced by 30% and the scaling of the logic circuit chip is increased from 500 k gates to 2400 k gates [3].

The number of TSVs is in the order of thousands, including signals, power supplies, and grounds. There is no TSV in the pixel array area. The column TSVs are placed in between the comparators on the pixel CIS chip and the counters of the logic circuits chip. The row TSVs are placed in between the row drivers of the CIS chip and the row decoders of the logic chip (Fig. 10.4). These arrangements of the TSVs can reduce the influence of noise and make it easy to manufacture the CIS chip. For example, to reduce the influence of noise, comparators are arranged on the pixel CIS chip, which can be manufactured by using Sony's matured process technology, rather than on the logic circuit chip.

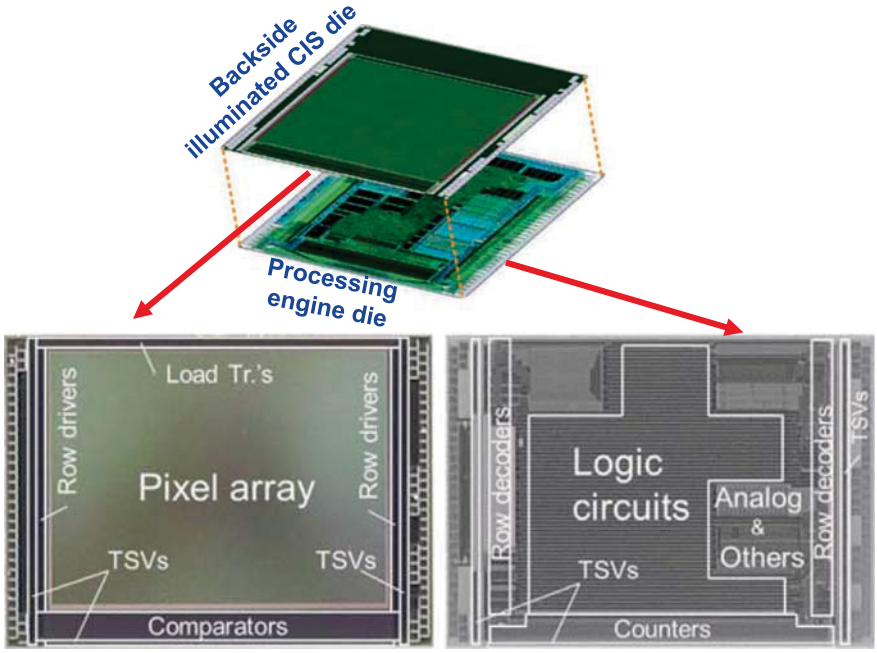


Fig. 10.4 3D CIS pixel chip and logic IC integration

(b) **Fabrication of the CIS Pixel Wafer and Logic IC Wafer**

The CIS pixel chip is fabricated by the Sony conventional 1P4M BI-CIS (90 nm) process technology. The logic chip is fabricated by the matured 65 nm 1P7M logic process technology. The size of the pixel chip and the logic chip is about the same. Sony didn't disclose the TSV and assembly technologies. It is assumed herein that the CIS Si-insulator of the CIS wafer is bonded to the logic Si-insulator of the logic wafer (very similar to the SiO_2-to-SiO_2 wafer-to-wafer bonding). The TSVs are then formed and Cu filled after the bonding of the wafers. Figures 10.5 and 10.6 show the cross-section SEM (scanning electron microscopy) images of the 3D CIS pixel chip and logic IC chip integration. It can be seen that (a) the top part is the BI-CIS chip, (b) the bottom part is the logic chip, (c) the BI-CIS wafer and the logic wafer are insulator-to-insulator (wafer-to-wafer) bonding (Fig. 10.5), and (d) the CIS chip is connected to the logic chip through TSVs (Fig. 10.6).

(c) **Hybrid Bonding**

It is worthwhile to mention that there is another kind of wafer-to-wafer bonding, namely hybrid bonding which bonds the metal pads and dielectric layer on both sides of the wafers at the same time. Sony is the first to use Cu–Cu direct hybrid bonding in HVM [4]. Sony produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results showed that their robust Cu–Cu direct hybrid bonding achieved remarkable

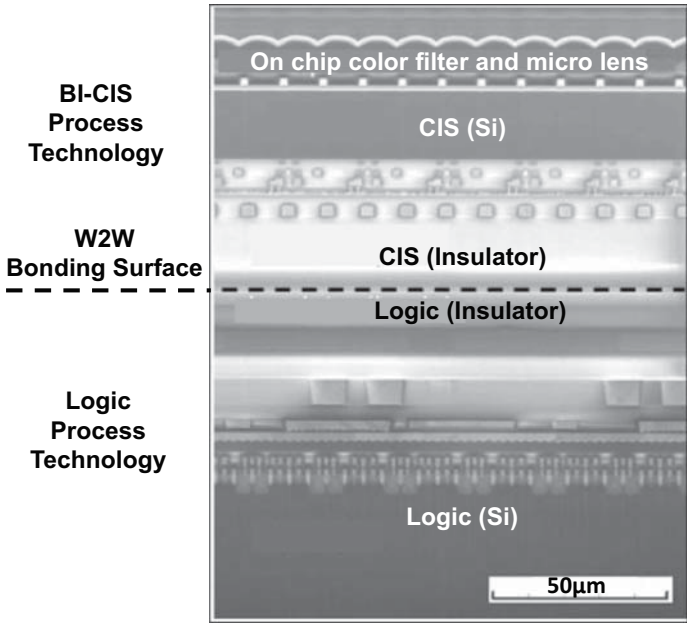


Fig. 10.5 CIS (insulator) wafer to logic (insulator) wafer bonding

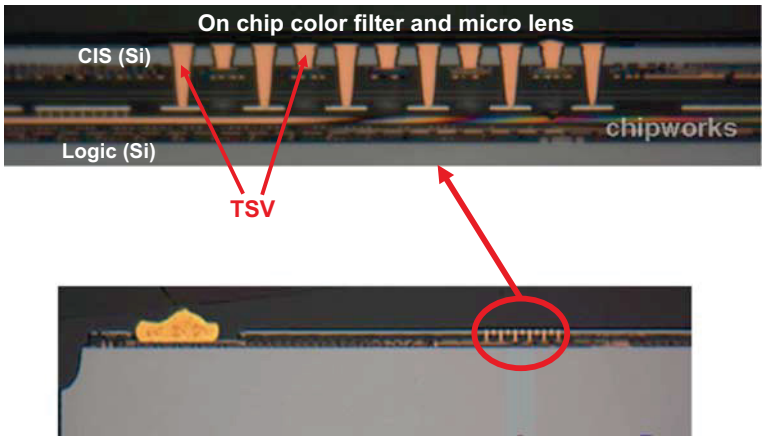


Fig. 10.6 TSVs connecting the CIS pixel chip and the logic circuit chip

connectivity and reliability. The performance of the image sensor was also super. A cross section of the IMX260 BI-CIS is shown in Fig. 10.7. It can be seen that, unlike in [3] for Sony's ISX014 stacked camera sensor, the TSVs are eliminated and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu–Cu direct bonding. The signals are coming from the package substrate with wire bonds to the edges of the processor chip.

The assembly process of Cu–Cu direct hybrid bonding starts off with surface cleaning, metal oxide removal, and activation of SiO_2 or SiN (by wet cleaning and plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a typical cleanroom atmosphere. The first thermal annealing (100–150 °C) is designed to strengthen the bond between the SiO_2 or SiN surfaces of the wafers while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO_2 or SiN. Then, apply higher temperature and pressure (300 °C, 25 kN, 10^{-3} Torr, N2 atm) for 30 min to introduce the Cu diffusion at the interface and grain growth across the bond interface. The post-bond annealing is 300 °C under N2 atm for 60 min. This process leads to the seam-less bonds (Fig. 10.7) formed for both Cu and SiO_2 or SiN at the same time.

10.2.3 3D IC and CIS Heterogeneous Integration

(a) **The Structure**

Figure 10.8 shows the 3D CIS and IC integration presented in [5]. It consists of the CIS, coprocessor IC, and glass carrier. The I/O count of the CIS is 80 and that of the

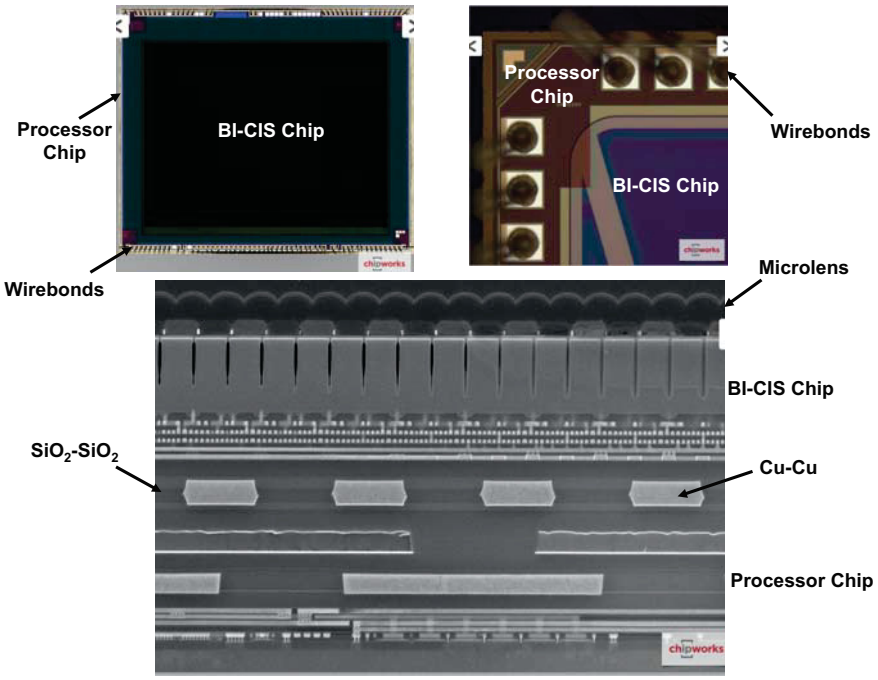


Fig. 10.7 Cross section images of Sony's CIS by Cu–Cu hybrid bonding

IC is 164. The size of the CIS and the coprocessor is not the same. The dimensions of the CIS are 5 mm × 4.4 mm and of the IC are 3.4 mm × 3.5 mm. The IC and the CIS are shown, respectively, in Fig. 10.9a, b and bonded face-to-back, as shown in Fig. 10.8. The interconnects of the CIS and IC are Cu-pillar with SnAg solder cap. The TSVs are in the CIS, which are connected to the substrate with solder bump RDLs (redistribution layers) are in both CIS and coprocessor IC.

(b) **Fabrication Process Flow of the Coprocessor Wafer**

The fabrication process flow of the coprocessor wafer is shown in Fig. 10.10. After the BEOL (back-end-of-line), sputter the barrier/seed layer (Ti/Cu) by PVD (physical vapor deposition). It is followed by making the RDLs by using a BOT (bond-on-trace) lithography and then ECD (electrochemical deposition) SiN (500 nm) and a low stress SiO_2 (600 nm) passivation is deposited by chemical vapor deposition (CVD). The diameter of the Cu-pillar is 20 μm and the Cu-pillars (12 μm) are fabricated by electroplating on a Ti (100 nm) barrier layer and a Cu (400 nm) seed layer. Then, it is followed by electroplating the Ni (2 μm) and SnAg (2 μm). Finally, it is reflowed at 260 °C. Figure 10.11 shows the SEM images of the RDLs and Cu μ-pillars on RDLs.

(c) Fabrication Process Flow of the CIS Wafer

The fabrication process flow of the CIS wafer is shown in Fig. 10.12. After the BEOL, bond the front side of the CIS wafer to a glass carrier wafer. This glass wafer will act as a mechanical (supporting) carrier as well as an optical part of the package. The bonding is performed with a 7 μm-thick SiNRTM adhesive provided by Shin-Etsu MicroSi, patterned in a lace around the pixel array as shown in Fig. 10.13. Then thin down the back side of the CIS wafer to 90 μm. Form the TSVs (60 μm in diameter) from the back side of the CIS wafer and RDLs. It is followed by electroplating the 25 μm-diameter Cu μ-pillars (12 μm) and solder caps (2 μm of Ni and 2 μm of SnAg), and reflowing at 260 °C. Figure 10.14 shows the SEM image of the Cu μ-pillars with solder (Ni/SnAg) caps and RDLs. (These Cu-pillars with solder caps are for the future connection with their counterparts on the top dies.)

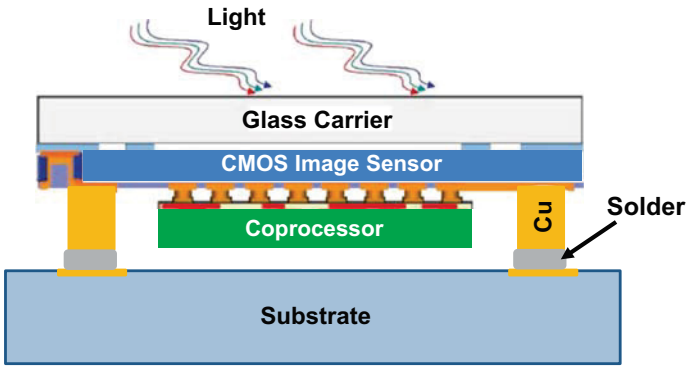


Fig. 10.8 3D CIS and processor heterogeneous integration

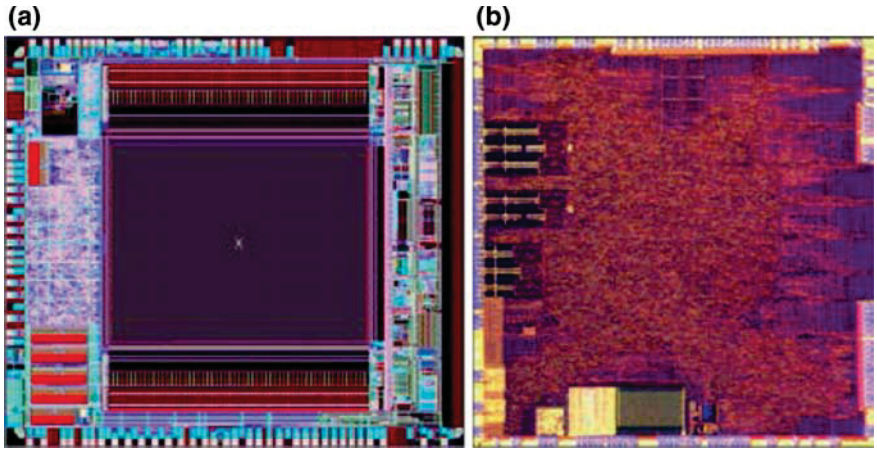


Fig. 10.9 **a** CIS pixel chip. **b** Processor chip

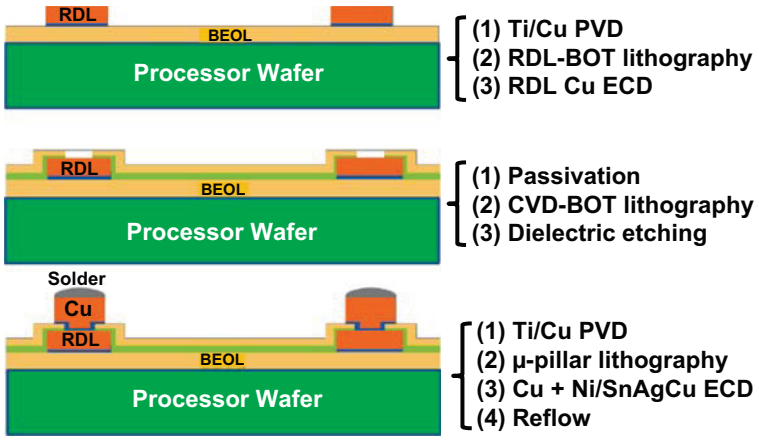


Fig. 10.10 Fabrication process flow of the processor wafer

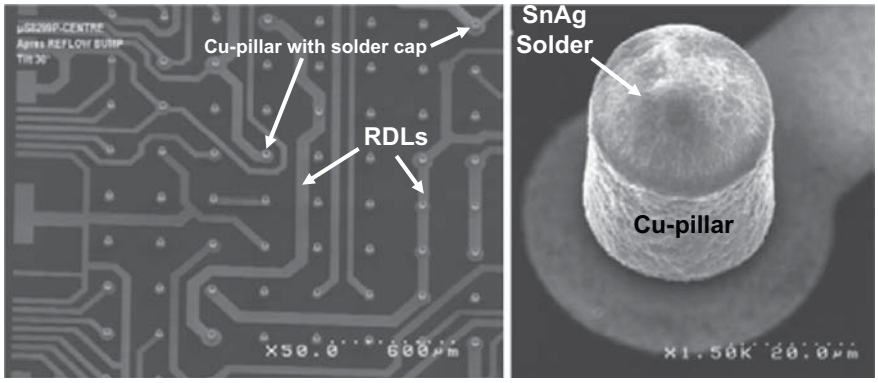


Fig. 10.11 SEM images of the RDLs and Cu μ-pillar with solder cap on the processor wafer

(d) **Final Assembly**

There are at least two ways to perform the final assembly. One is to stack up the coprocessor IC chip to the CIS wafer (chip-to-wafer or C2W) first and then do the ball mounting of the CIS wafer. The other is to perform the ball mounting on the CIS first and then do the IC chip to CIS wafer (C2W) bonding (Table 10.1). Figure 10.15 shows the 3D prototypes during the assembly process (balling first): mounted IC coprocessors and untreated sites.

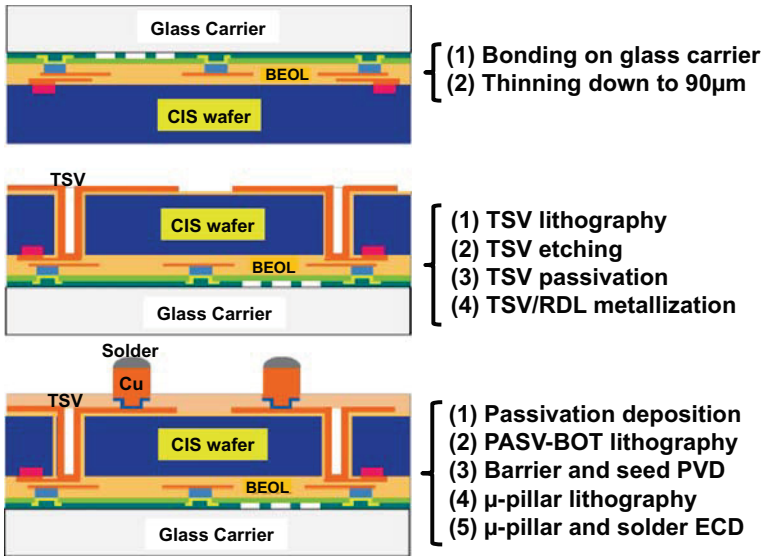


Fig. 10.12 Fabrication process flow of the CIS wafer

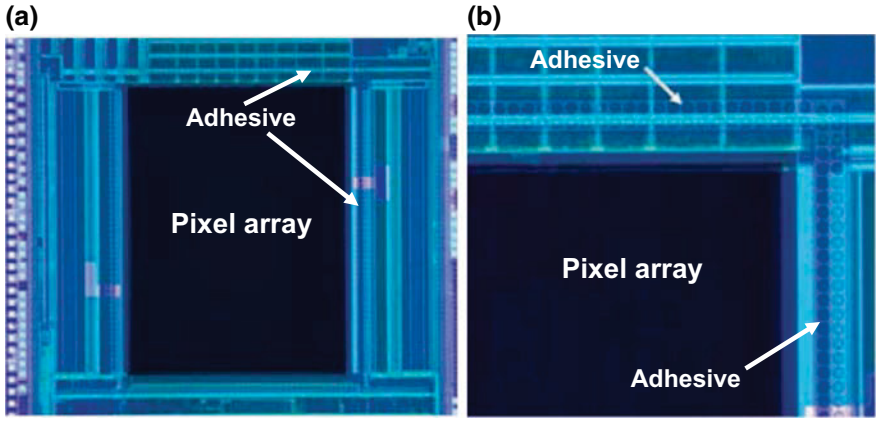


Fig. 10.13 **a** CIS wafer with adhesive. **b** Zoom-in view

10.2.4 Summary and Recommendations

Some important results and recommendations are summarized as follows:

- A couple of real 3D CIS and IC heterogeneous integration examples have been presented.
- Hopefully, more examples in this area will be published in the near future.

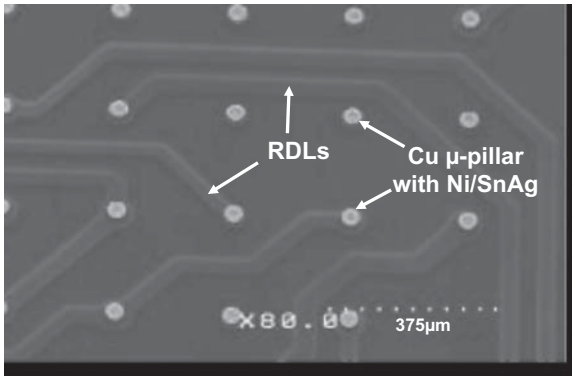


Fig. 10.14 SEM image of RDLs and Cu µ-pillar with solder cap on the CIS wafer

Table 10.1 Assembly processes of the CIS and processor IC: stacking first versus balling first

Stacking first	Balling first
Coprocessor wafer thinning	CIS flux dispense
Coprocessor wafer dicing	CIS balling
Coprocessor die flux dipping	CIS wafer reflow
Coprocessor die to CIS wafer bonding	Coprocessor wafer thinning
Reflow and cleaning	Coprocessor wafer dicing
CIS flux dispense	Coprocessor die flux dipping
CIS ball jetting	Coprocessor die to CIS wafer bonding
CIS wafer reflow	CIS wafer reflow
Capillary underfill	Capillary underfill
CIS singulation	CIS wafer singulation

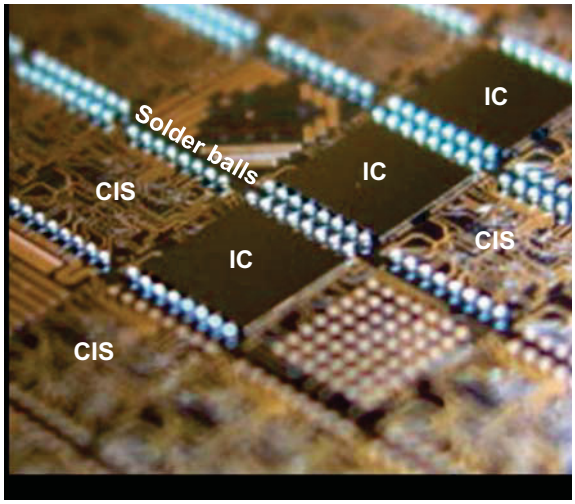


Fig. 10.15 3D prototypes (balling first) during the assembly process: mounted processor ICs and untreated sites

- Hybrid W2W bonding (Cu-to-Cu and SiO_2-to-SiO_2 happen at the same time), Fig. 10.7 is most suitable for 3D CIS and IC heterogeneous integration because the size of the processor chip and the size of the pixel chip are not very much different.

10.3 Heterogeneous Introduction of LED

Due to the rapid progress of the white LED (light-emitting diode) and the pressure of environmental initiatives, the amount of light generated per LED package has increased by a factor of >30 in the past 10 years. 3D LED and IC heterogeneous integration packages such as [8–12] are discussed in this section. These packages consist of the single- or multi-LEDs and either active IC (integrated circuit) chip such as the ASIC (application-specific IC), LED driver, processor, memory, RF (radio frequency) sensor, and power controller in a 3D manner or passive interposer in a 2.5D manner. The assembly processes of these packages are also presented and discussed. Specifically, 2.5D IC and LED integrations, such as (a) LED packaging using silicon substrate with cavities for phosphor printing and copper-filled TSVs for interconnection, and (b) LED on silicon substrate with cavity and TSVs, are discussed.

10.3.1 LED Packaging Using Si-Substrate with Cavities and Cu-Filled TSVs

(a) **The Structure**

Figure 10.16 shows the schematic of the cross-section of a Si-substrate with cavity for phosphor printing and Cu-filled TSVs for interconnection [9, 10]. It can be seen that the Si-substrate is about 400 μm thick with 3 μm-thick low-temperature oxide on both sides. The dimensions of the cavity are 1.3 mm × 1.3 mm × 0.22 mm. The diameter of the TSV is 100 μm and is filled with Cu. The exposed tip of the Cu TSV is 30 μm and plated with solder.

(b) **Key Process Steps**

The key assembly process flow of the LED package is shown in Fig. 10.17. First, deep reactive ion etch (DRIE) is applied to make the blind vias from the back side and the cavity on the front side, Fig. 10.17a. It is followed by dielectric layer, barrier layer, and seed layer deposition and Cu plating to fill the vias, Fig. 10.17b. Then apply the KOH (the formula of potassium hydroxide inorganic compound) and BOE (buffered oxide etch) to further etch the cavity on the front side in order to expose the tip of the Cu-filled TSV, Fig. 10.17c. Solder plating on the tip of the TSV and then electroplating the electrode on the back side, Fig. 10.17d. Solder reflow and

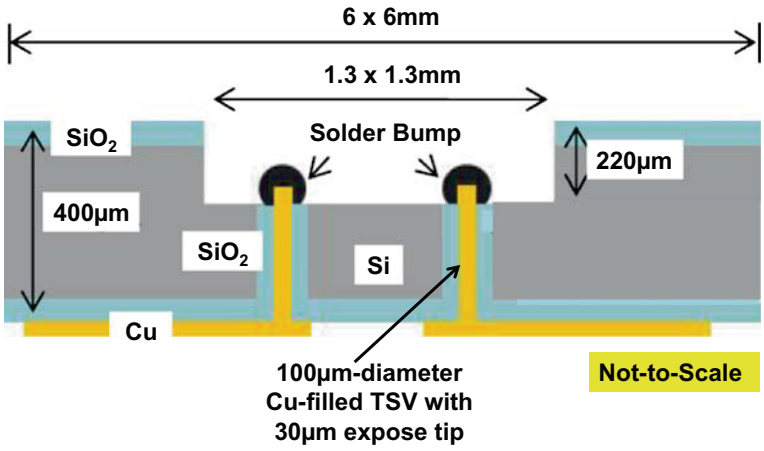


Fig. 10.16 Si-substrate with a cavity and TSVs

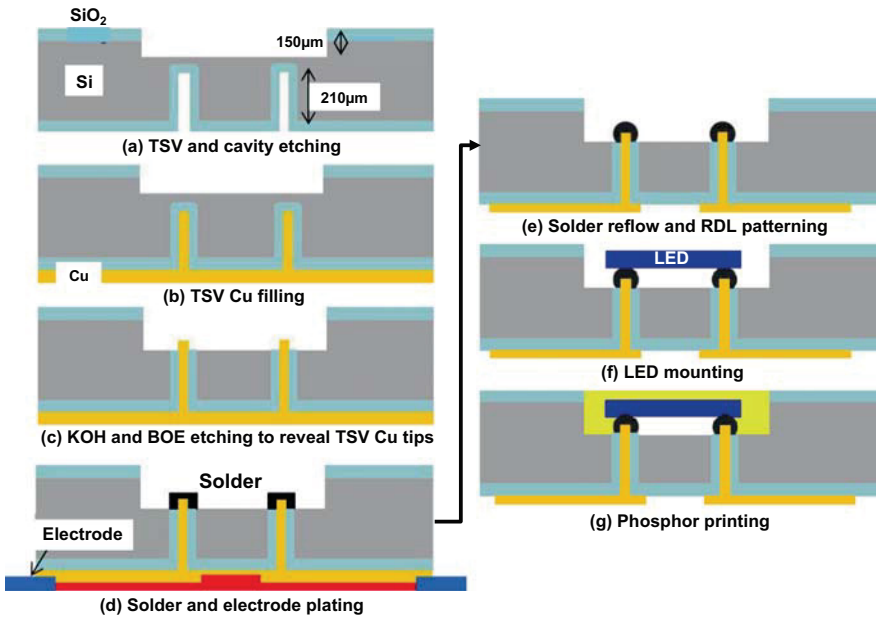


Fig. 10.17 Fabrication process flow of LED package with Si-substrate

then RDL patterning and plating on the back side, Fig. 10.17e. It is followed by pick and place the flip chip (1 mm × 1 mm × 0.07 mm) blue LED device on the solder and reflow to form the solder joints, Fig. 10.17f. Finally, phosphor is printed to fill the cavity as shown in Fig. 10.17g.

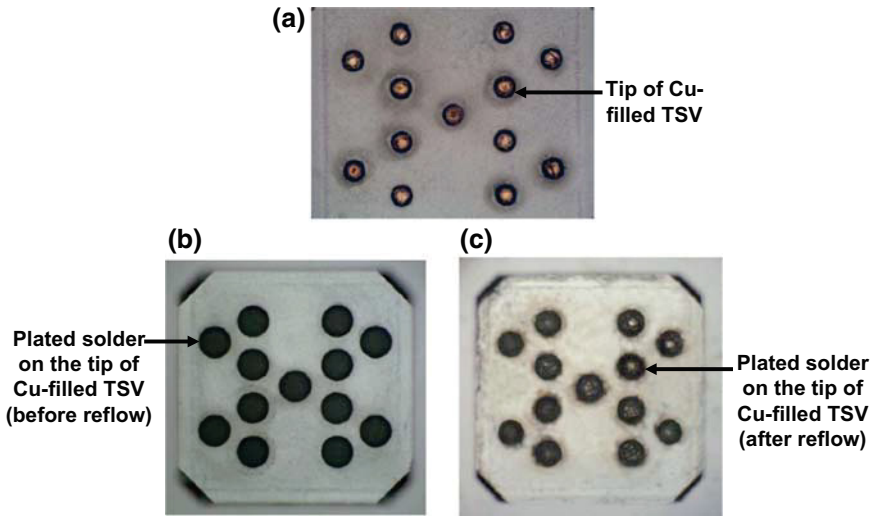


Fig. 10.18 **a** Tips of Cu-filled TSVs. **b** Plated solder on the tip of Cu-filled TSV (before reflow). **c** Plated solder on the tip of Cu-filled TSV (after reflow)

Figure 10.18a shows the image of the tips of Cu-filled TSVs. Figure 10.18b shows the image of the plated solder on the tip of the Cu-filled TSVs (before solder reflow) and Fig. 10.18c shows the image of the plated solder on the tip of the Cu-filled TSV (after solder reflow). It can be seen that they are properly done. Figure 10.19a, b show the images, respectively, of the top view and cross-sectional view of the LED package. The Si-substrate, the RDL, the cavity, and the TSV tips with solder bumps (before LED mounting) can be clearly seen.

Figure 10.20a schematically shows the squeegee printing of the dry YAG:Ce yellow phosphor powders to encapsulate the LED and fill the cavity. First, a small amount (1 μL) of UV-curable epoxy is dispensed into the cavity and then pre-cured for 10s by a UV lamp with a power density of 75 mW/cm^2. The phosphor powder is spread on top of the Si-substrate and printed to fill the cavity by a squeegee blade. Finally, the epoxy is fully cured for 6 min to bind the phosphor and to encapsulate the LED device. Figure 10.20b, c, respectively, show the images of the cavity before phosphor printing and after.

Figures 10.21a and 10.22b show, respectively, the top view and cross-section view of the final LED package. It can be seen that the LED device is embedded in the cavity and encapsulated by the yellow phosphor. The encapsulation is formed within the cavity and achieves a flat profile.

Figure 10.22a, b show, respectively, the lit-up blue LED without the phosphor and with the yellow phosphor. It can be seen that the yellow phosphor does convert the blue LED into white LED.

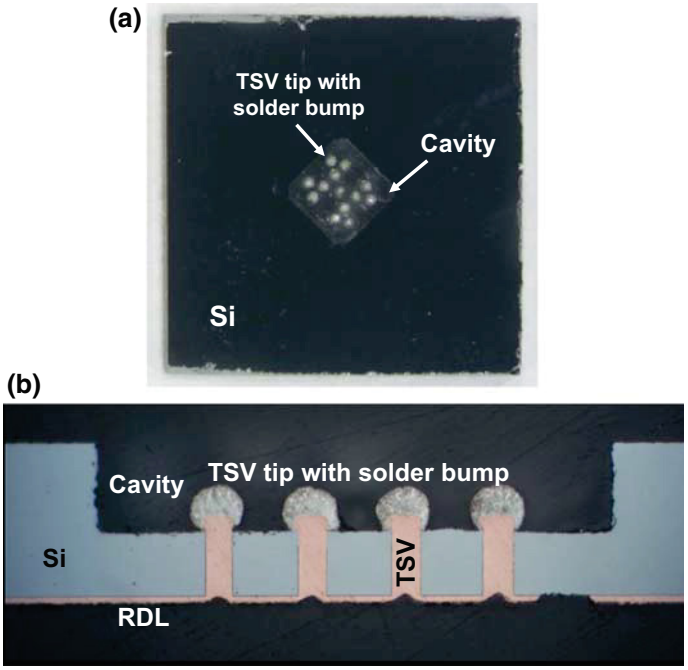


Fig. 10.19 **a** Top view of the Si-substrate with cavity and TSV tips with solder bumps. **b** Cross sectional view of the Si-substrate with cavity and TSV tips with solder bumps

10.3.2 LED Wafer-Level Packaging with TSVs

(a) **The Structure**

Figure 10.23 schematically shows a wafer level packaging with LED devices in the cavities of a Si substrate [11, 12]. It can be seen that the Si-substrate has cavities on its top side to house the LED devices and TSVs to connect the LEDs to the RDLs on its bottom side. The Si-substrate is covered by a glass with yellow phosphor. For the test vehicle used in [11, 12], the 1 W LED chip is shown in Fig. 10.24. It can be seen that the size of the LED is 885 μm $\times$ 885 μm and the size of the P-pad and N-pad is, respectively, 100 μm $\times$ 200 μm and 100 μm $\times$ 100 μm.

(b) **Key Process Steps**

The assembly process flow of the proposed LED package is shown in Fig. 10.25. First, DRIE is applied to form the cavity of the top side of the Si-substrate, Fig. 10.25a. It is followed by sputtering the reflective metal, Fig. 10.25b. Then, attach the LED to the bottom of the Si-substrate cavity with polymer adhesive, Fig. 10.25c. Optical glass with phosphor wafer is bonded to Si-substrate with LED wafer (wafer-to-wafer), Fig. 10.25d. Then, backgrind the bottom side of the Si-substrate, Fig. 10.25e. It is

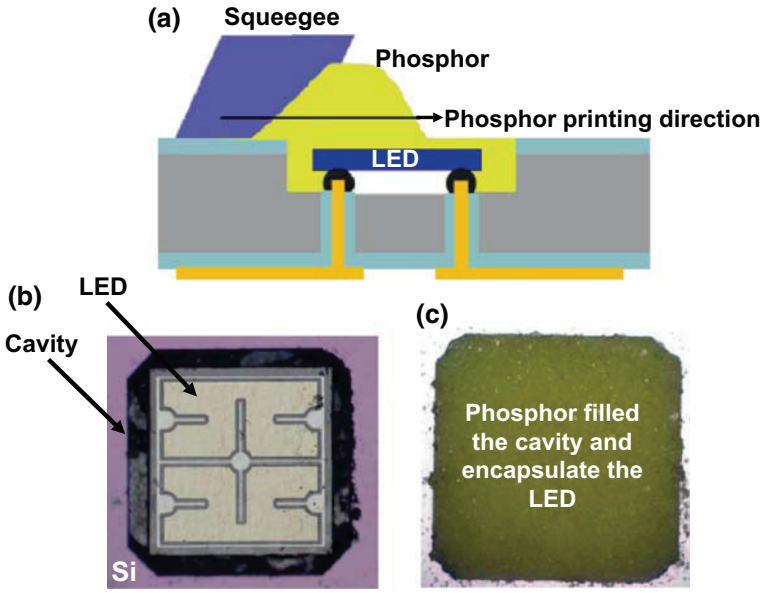
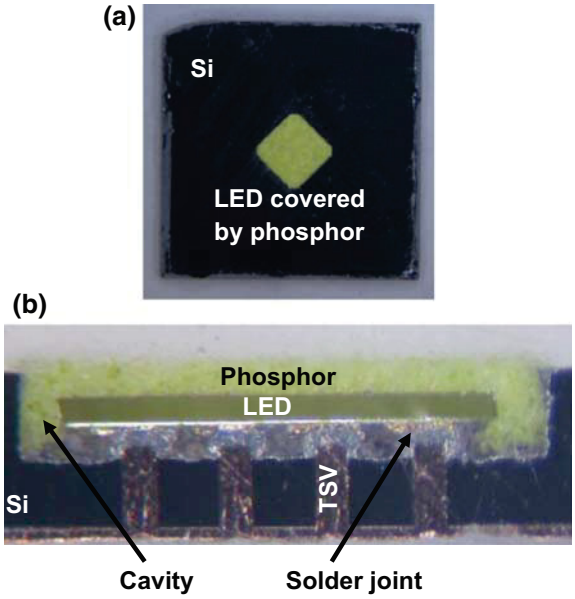


Fig. 10.20 **a** Schematic of the phosphor printing. **b** Top view of the Si substrate with cavity and LED device. **c** Top view of the LED and cavity covered by yellow phosphor

Fig. 10.21 **a** Top view of the Si-substrate with cavity and LED covered by phosphor. **b** Cross sectional view of the Si-substrate with cavity and LED covered by phosphor



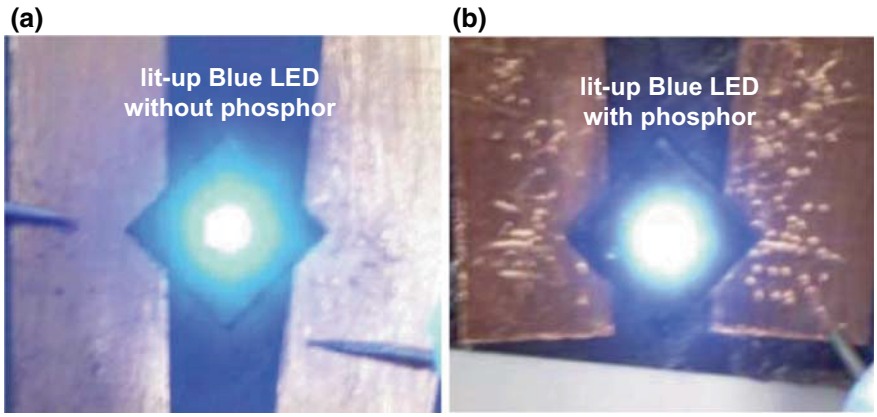


Fig. 10.22 **a** Lit-up blue LED without phosphor. **b** Lit-up blue LED with phosphor (white light)

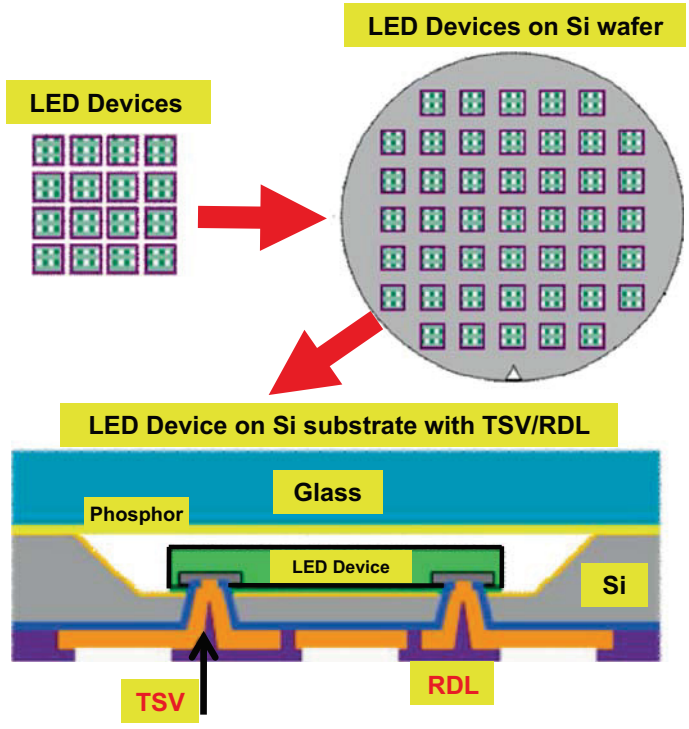


Fig. 10.23 Si-substrate with cavity and TSVs for LED packaging

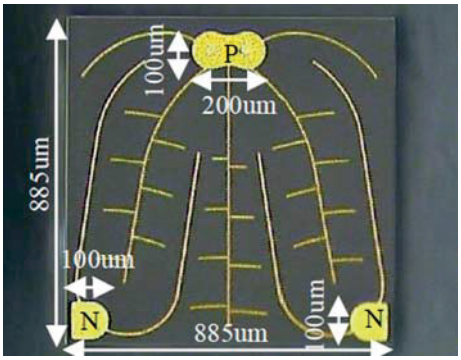


Fig. 10.24 LED device for the test vehicle

followed by photoresist, mask, lithographing, patterning, and DRIE to form the TSVs, Fig. 10.25f. Encapsulation layer and opening are formed by spin coating and then laser drilling, Fig. 10.25g. It is followed by sputtering the seed layer, lithographing, and then plating the RDL, Fig. 10.25h. Finally, the solder resist layer is formed by photo lithography, Fig. 10.25i. The photo images are shown in Fig. 10.26.

The packaged wafer is singulated into individual LED package (2000 μm × 2000 μm). Figure 10.27 shows the SEM images of the cross-section of the LED package without phosphor. It can be seen that (a) the LED device is attached on the bottom of the cavity of the Si-substrate, (b) the glass is bonded on the top of the Si-substrate, (c) the LED pads are connected to the RDL through the TSV with contactor size of about 20 μm, and (d) the encapsulation separates the Si-substrate from the RDL, which prevents electrical shortage between the cathode and the anode.

(c) **Performances**

Figure 10.28a shows the LED package with phosphor on an MCPCB (metal-core printed circuit board). The back side of the MCPCB is attached to a heat spreader with a TIM (thermal interface material), Fig. 10.28b, c. Figure 10.28d shows the lit-up LED with phosphor. It can be seen that the light is of mixed white and blue color, which means the phosphor volume/process needs to be optimized.

Figure 10.29 shows the Labsphere integrating sphere test results with different electricity currents: 50, 200, and 350 mA of the LED package with phosphor. It can be seen that (a) the light power increases with the input electrical current, (b) the light power is 189.98 mW at 350 mA, which is about 85% of the raw LED device (this means valid electrical connection has been formed through wafer-level packaging), and (c) the light power efficacy decreases with the input electrical current (this means the junction temperature of the LED device increases with the input current). Thus, the thermal management of the present LED packaging system needs to be optimized.

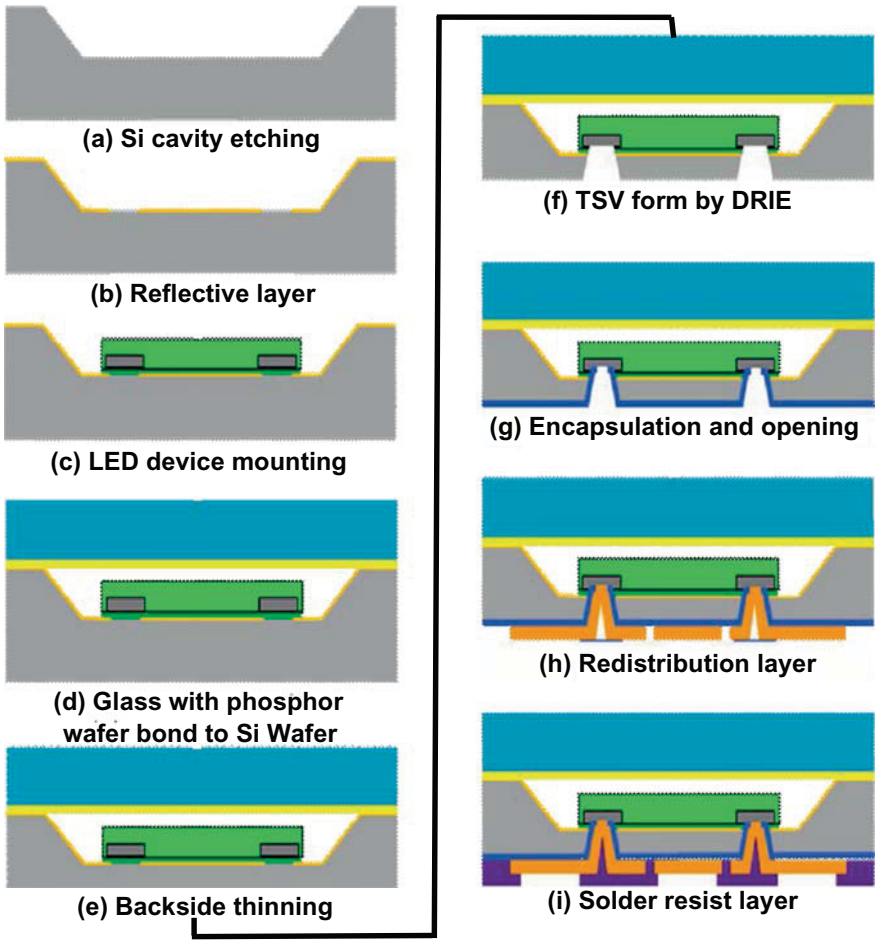


Fig. 10.25 Fabrication process flow for the Si-substrate with cavity and TSVs for LED packaging

10.3.3 Summary and Recommendation

Some important results and recommendations are summarized as follows [9–12]:

- A couple 2.5D IC and LED integration examples have been provided and discussed. Basically, they consist of a Si-substrate (-interposer) with cavity to house the LED and TSVs to connect the LED to the next level of interconnections.
- A lot of work still remains to be done; however, the feasibilities of using Si-interposers to support the LEDs have been demonstrated.
- The next step is to replace the Si-substrate (-interposer) by active device chip with TSVs; a true 3D IC and LED integration.

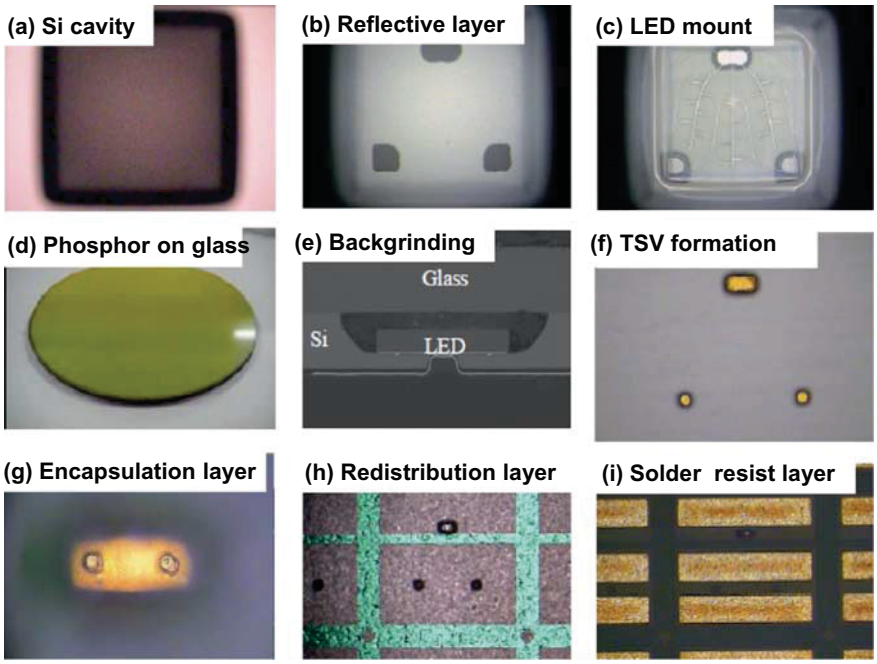


Fig. 10.26 Photo images of the fabrication processes of the LED package

10.4 Heterogeneous Integration of MEMS

MEMS stands for microelectromechanical *s*ystems, which is the integration of mechanical elements such as sensors and actuators and electronics on a common silicon substrate through the use of microfabrication technology [13–21]. The same basic technology and process steps, such as etching, patterning, doping, and connecting, employed for making conventional electronic ICs (integrated circuits), such as CMOS, can be used to fabricate (micromachining) micromechanical elements by selectively etching away parts of a silicon wafer or adding new structural layers to form MEMS devices. However, there is a fundamental difference between MEMS and IC devices—namely, MEMS devices must remain physically movable. MEMS devices use electronics to move their mechanical elements (parts)!

Most people consider the next big thing after smartphones is the IoTs (Internet of Things). IoTs are sometimes called the M2M (machine-to-machine) revolution, and MEMS is one of the important groups of machines which will play an essential role in expansion of the boom of the IoTs. For example, MEMS sensors allow equipment to gather and digitize real-world data that then can be shared on the Internet. The IoTs promote a major new growth opportunity for the MEMS market.

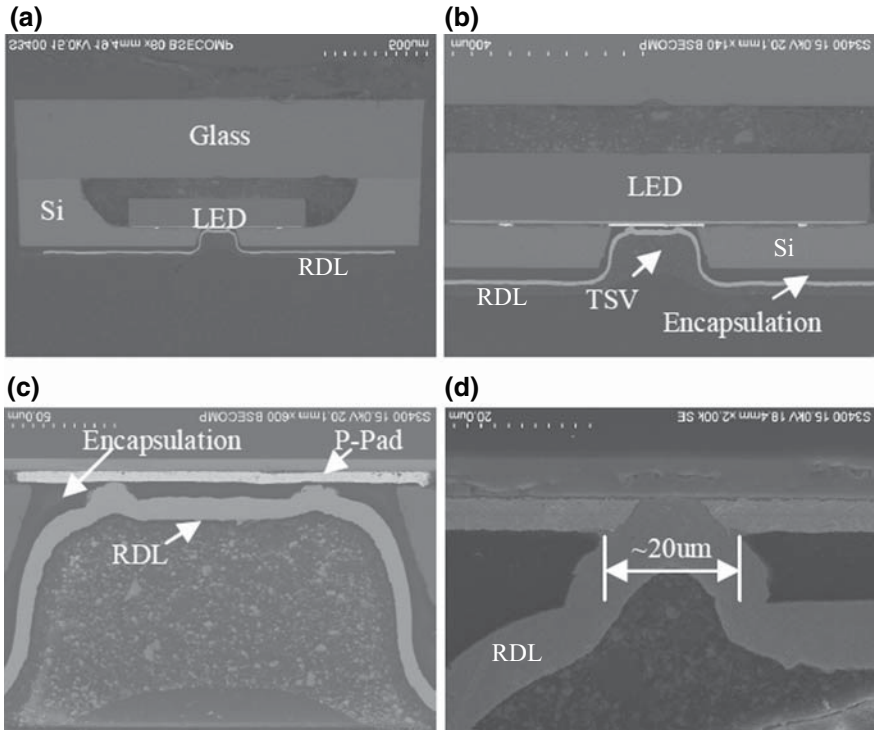


Fig. 10.27 SEM images of the cross-sectional view of the LED package. **a** The Si-substrate with a cavity to house the LED and TSV to connect to the RDL. **b** Zoom-in view of (**a**). **c** Zoom-in view of (**b**). **d** Zoom-in view of (**c**)

In this section, (a) TSVs for wafer-level packaging of RF MEMS devices, (b) wafer-scale packaging for FBAR-based oscillators, and (c) a 3D IC MEMS heterogeneous integration with low-temperature bonding are presented.

10.4.1 TSVs for Wafer-Level Packaging of RF MEMS Devices

(a) **The Structure**

Figure 10.30 schematically shows the cross-section and bird-view of the wafer-level packaging of a RF MEMS device [15, 16]. It consists of the MEMS wafer (RF MEMS device, high resistivity silicon (HR-Si) substrate with RDLs, and AuSn solder for sealing ring and bonding pads) and the cap wafer (cap with a cavity, TSVs, and RDLs, and the solder bump). It is a 2.25D MEMS and IC integration. Main objective of [15, 16] is to study the insertion loss of RF-MEMS wafer during packaging with

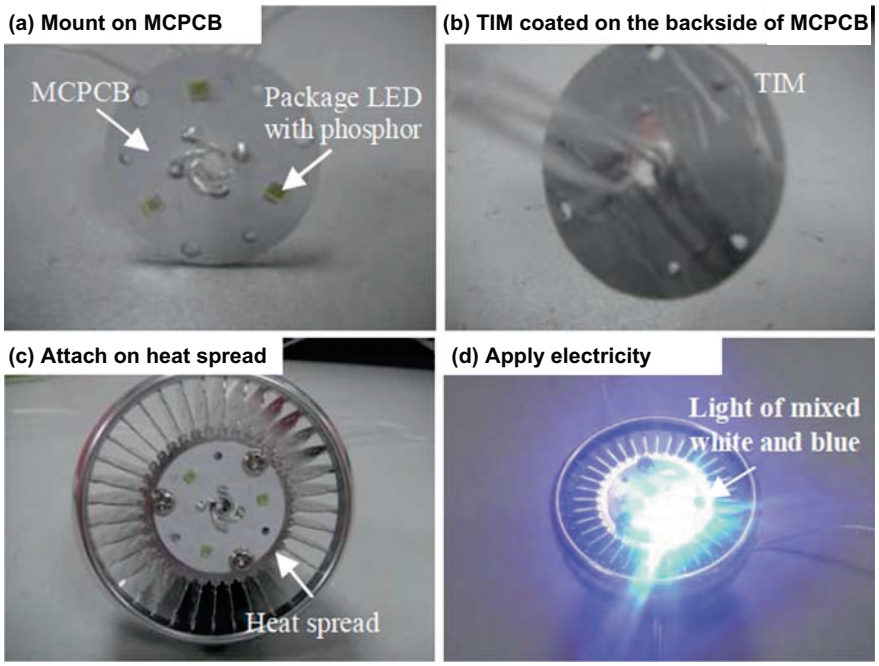


Fig. 10.28 **a** Attach the LED package with phosphor on MCPCB. **b** Coat the TIM at the back side of the MCPCB. **c** Attach the heat spreader to the back side of the MCPCB. **d** Lit-up the LED

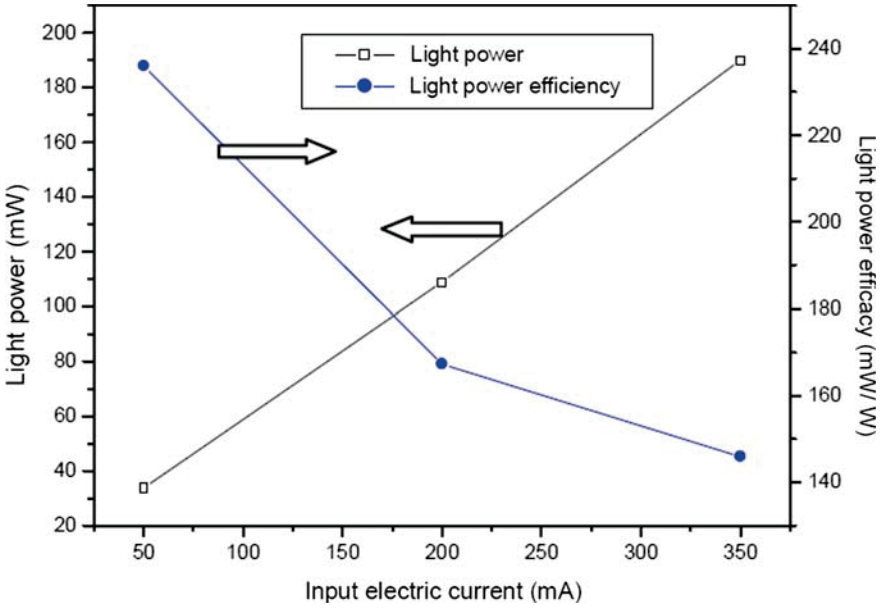


Fig. 10.29 Light power and light power efficacy versus input electrical current of the test vehicle

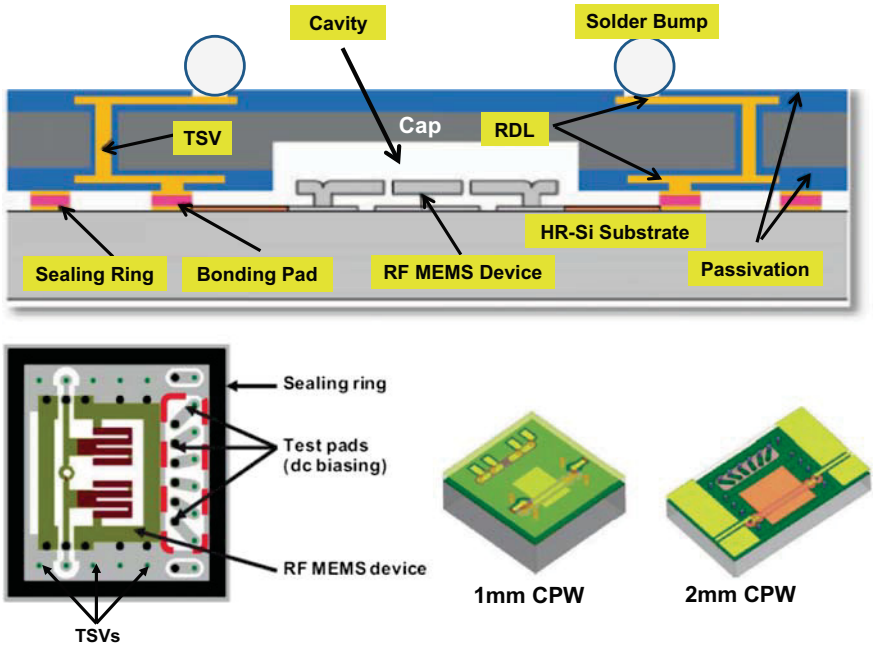


Fig. 10.30 Schematic of the MEMS wafer-level package. Design layout of a typical RF-MEMS package with TSVs. Different length CPW structures

TSV cap wafer. Two different types of CPW (coplanar waveguide) structures (1 mm CPW and 2 mm CPW), as shown in Fig. 10.30, are designed and fabricated.

The CPW lines are fabricated with Al (1.5 μm in thickness). Three passivation schemes are considered: 3 kA Poly Si, 2 μm of low stress oxide, and 1 kA SiN. The UBM on the sealing ring and bonding pads is 0.1 μmTi/0.2 μmPt/2 μmAu/2.15 μmSn/500 ÅAu.

(b) **Key Process Steps**

The fabrication process flow of the cap wafer is shown in Fig. 10.31. First, TSV (60 μm in diameter and 200 μm in depth) forming with DRIE, Fig. 10.31a. Then, TSV filling and RDLs by Cu plating, Fig. 10.31b. It is followed by backgrinding the cap wafer to 200 μm to expose the tip of the TSV and then passivation, Fig. 10.31c. Cu plating of the RDLs on the back side of the cap wafer, Fig. 10.31d. DRIE the cavity to 100 μm, Fig. 10.31e. UBM and AuSn solder deposition, Fig. 10.31f. Thin wafer handling is necessary. Right before the backgrinding to expose the TSV, the front side of the cap wafer is temporary bonded to a supporting wafer (carrier) with BSI HT10.10 adhesive. Right after the solder deposition, the wafers are debonded (separated) by thermal slide-off method.

Figure 10.31g schematically shows the MEMS wafer to cap wafer (W2W) bonding and the bonding condition is shown in Fig. 10.32. It can be seen that the bonding

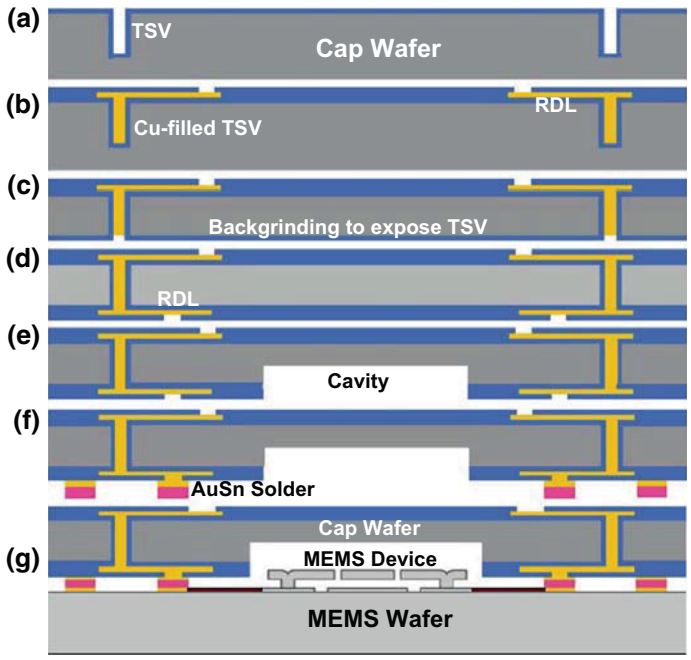


Fig. 10.31 Schematic of TSV cap wafer fabrication process flow and W2W bonding. **a** TSV by DRIE. **b** Cu-plating to fill the TSV. **c** Backgrinding and then passivation. **d** Cu-plating the RDLs on the back side of the cap wafer. **e** DRIE the cavity. **f** UBM and AuSn solder deposition. **g** MEMS wafer to cap wafer bonding

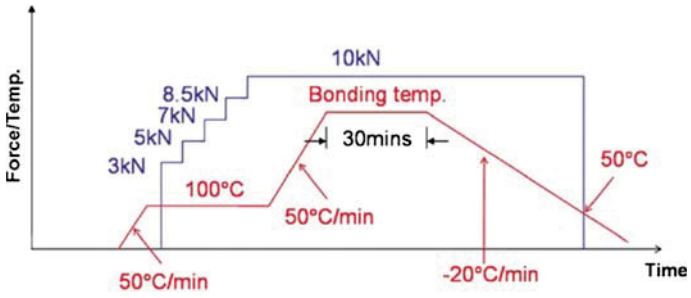


Fig. 10.32 W2W (AuSn) bonding condition

temperature for the AuSn solder is 280 °C for 30 min and the bonding force is 10 kN. Figure 10.33 shows the optical image of the bonded wafer (cap wafer is on top and the MEMS wafer is at the bottom) and the X-ray images. It can be seen that there is nothing unusual. Figure 10.34 shows the X-ray and SEM images of the bonded package. It can be seen that there is no void and delamination of the sealing ring. Figure 10.35 shows the images of the bonded MEMS package. It can be seen that (a) there is no void in the TSV, and (b) there is no delamination of the dielectric, barrier, and seed layer of the TSV.

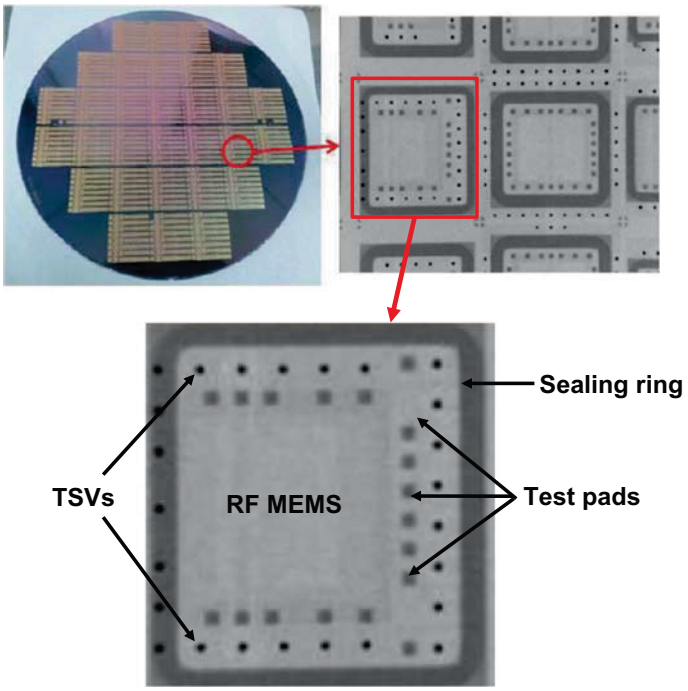


Fig. 10.33 Bonded wafers. X-ray image showing the TSVs and sealing ring

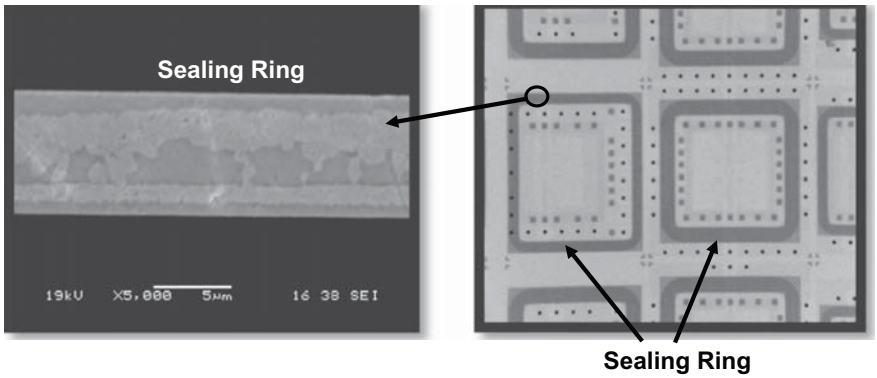


Fig. 10.34 SEM and X-ray images showing the sealing ring

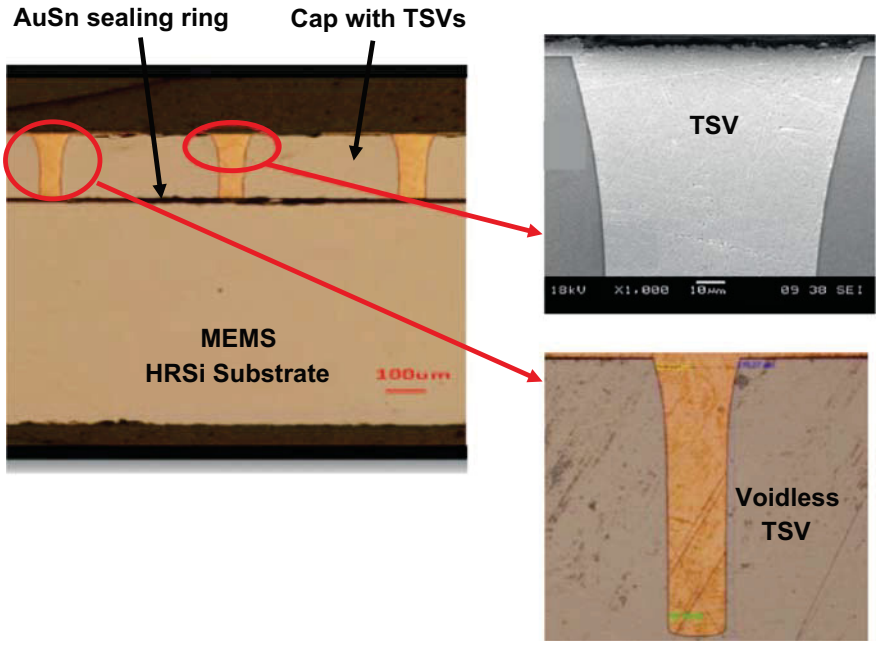


Fig. 10.35 Cross-sectional view of the bonded cap and MEMS wafers showing the AuSn sealing ring and voidless TSV

(c) **Performances**

Packaging loss of the 1 mm CPW lines is measured at different frequencies before the onset of resonance at 19 GHz (Fig. 10.36). This insertion loss ranges from 0.12 to 0.2 dB over 5 to 20 GHz, and 1 dB cut-off frequency is 22.7 GHz. Insertion loss of 2 mm CPW lines ranges from 0.14 to 0.3 dB over 5 to 25 GHz, and 1 dB cut-off frequency is 27.4 GHz (Fig. 10.37). Since the acceptable packaging loss is <0.2 dB for <20 GHz range and 1 dB packaging cut-off frequency is >20 Hz; thus, the 1 mm CPW design is OK.

10.4.2 Wafer-Scale Packaging for FBAR-Based Oscillators

(a) **The Structure**

Figure 10.38 show the wafer-scale packaging for FBAR (film bulk acoustic resonator)-based oscillators [17, 18]. Figure 10.38a shows the cap wafer (upper part) of the package. It can be seen that there is an IC device (330 μm × 285 μm), six TSVs for external connection, two internal connections (ICP), and a small cavity for the FBAR. Figure 10.38b shows the FBAR wafer (lower part) of the package. It can

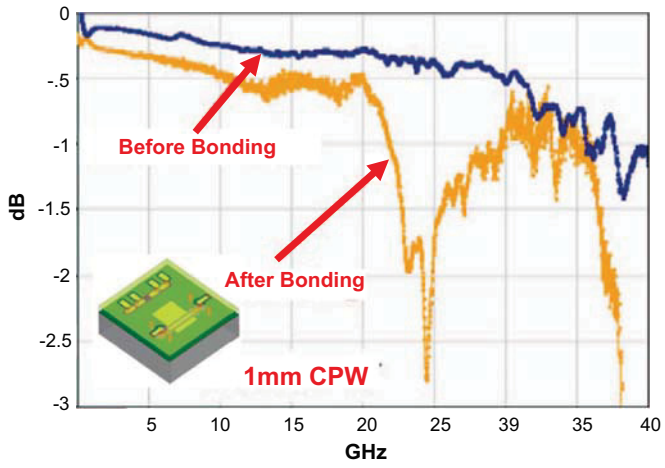


Fig. 10.36 MEMS packaging insertion loss with 1 mm CPW design

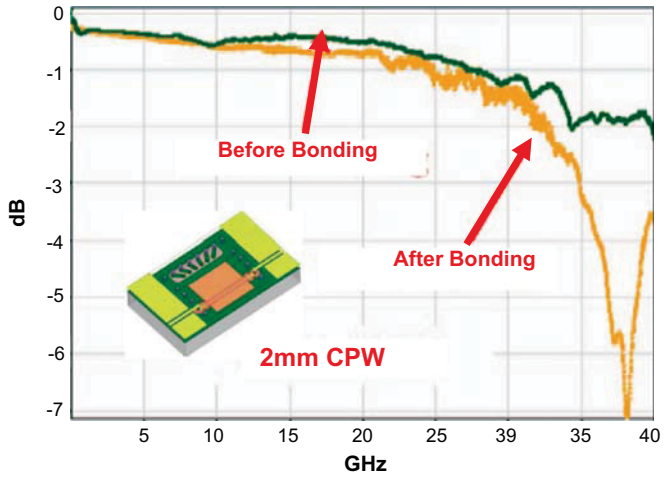


Fig. 10.37 MEMS packaging insertion loss with 2 mm CPW design

be seen that there is an FBAR, six external pads (for those six TSVs), two internal connections (from the cap electronics to the FBAR), and a cavity (for the IC device). This is a real 3D MEMS and IC heterogeneous integration. Both the FBAR and cap wafers are high-impedance Si to minimize cross-talk and capacitive losses.

(b) **Key Process Steps**

The fabrication process flow of the FBAR package without the IC device is shown in Fig. 10.39. For the FBAR wafer, first, define and form the cavity and then fill it with a sacrificial oxide, Fig. 10.39a. Form the FBAR/ZDR (zero drift resonators),

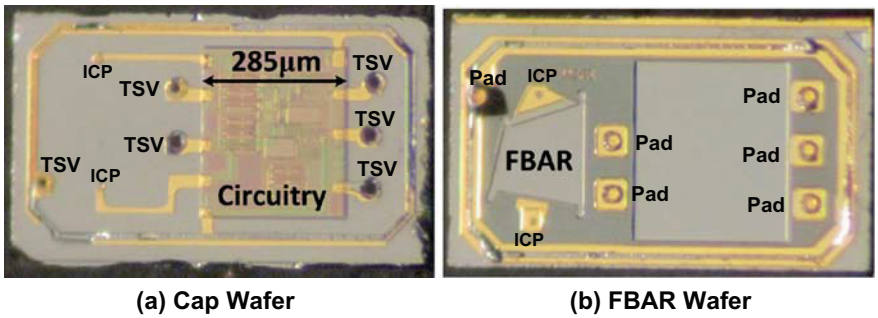


Fig. 10.38 Photo images of the FBAR hermetic package. **a** Cap wafer with IC device, TSVs, internal connections, and cavity for the FBAR. **b** FBAR wafer with FBAR, pads, internal connections, and cavity for IC device

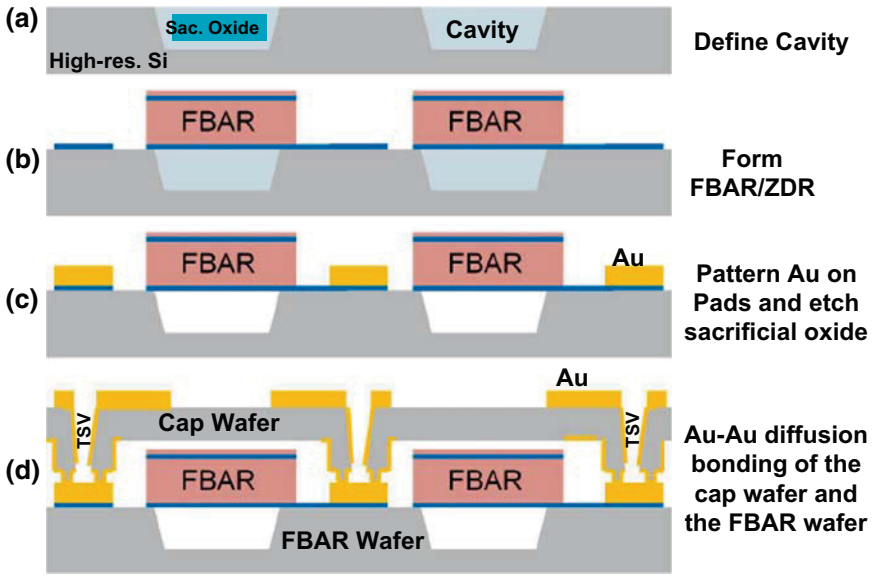


Fig. 10.39 Fabrication process flow of the FBAR wafer and cap wafer to FBAR wafer bonding

Fig. 10.39b. Pattern the Au on pads and sealing ring and then remove the sacrificial oxide, Fig. 10.39c. For the cap wafer, standard micromachining process is applied to make the cavity and DRIE is used to make the TSVs. Electroplate Au on external pads, internal pads, sealing ring, and the side walls of the TSVs. Finally, Au–Au diffusion bonding of the cap wafer and the FBAR wafer, Fig. 10.39d.

The fabrication process flow of the cap wafer with IC device of the FBAR package is shown in Fig. 10.40. The devices are fabricated by a standard bipolar process, except that the interlayer dielectric is left in the field until the devices are complete, Fig. 10.40a. Then remove the field dielectric down to Si, Fig. 10.40b. Apply the

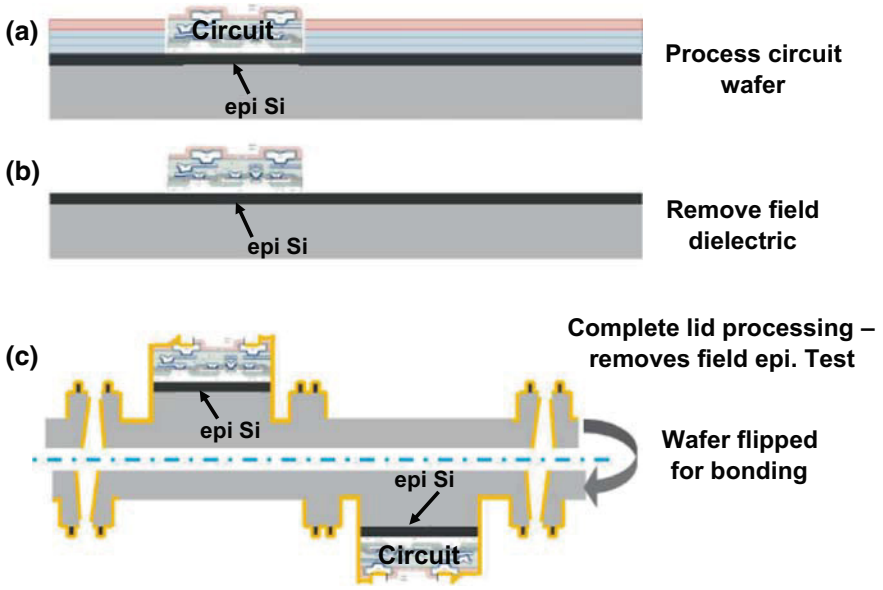


Fig. 10.40 Fabrication process flow of the FBAR cap wafer

standard micromachining process to make the cavity and DRIE to make the TSVs. It is followed by Au plating the pads and side walls of TSVs, and then flipping the wafer for bonding, Fig. 10.40c. The TSVs are not filled.

The Au–Au diffusion bonding of the cap wafer with the IC device and TSVs and the FBAR wafer is schematically shown in the top of Fig. 10.41. The cross-sectional SEM image of the bonded package is shown in the bottom of Fig. 10.41. It can be seen that all the key elements such as the FBAR, IC device TSVs, cap, sealing ring, and pad are in proper position. For detailed characterization and mechanical and electrical performances, please read [17, 18].

10.4.3 Low-Temperature Bonding of 3D MEMS Packaging with Solders

Most current chip-to-wafer and wafer-to-wafer bonding methods use temperatures higher than 300 °C. During bonding, however, the MEMS devices are already released (there are free-standing microstructures, e.g., membranes, beams, and cantilevers), and low-temperature bonding is desired to reduce damage to the microstructure owing to the thermal-expansion mismatch of the bonding structure (less bow). Fusion (e.g., Cu-to-Cu) bonding at room temperature works; however, the bonding surfaces must be very flat and clean (class 1 cleanroom), which does not permit high-volume production. On the other hand, with proper designs of bonding pads and UBM (under bump metallurgy) and selections of solder materials, 180 °C or

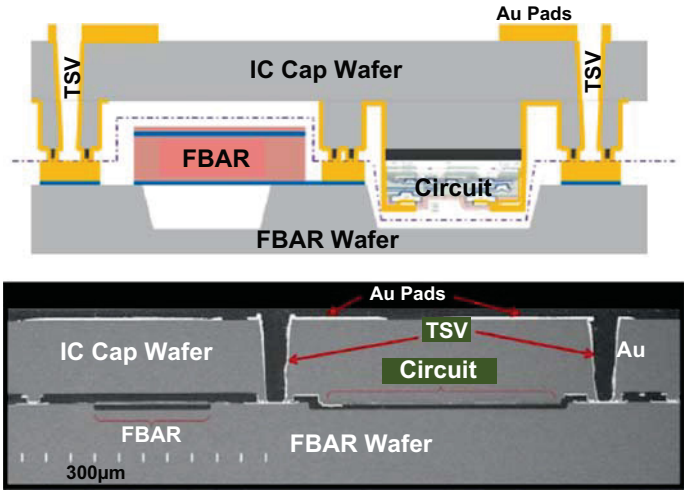


Fig. 10.41 (Top) IC cap wafer to FBAR wafer Au–Au bonding. (Bottom) Cross-section SEM image of the bonded FBAR MEMS package with IC cap

lower bonding temperatures are possible [19–21]. During/after bonding, the solders will be reacted within themselves and the UBM, and become an IMC (intermetallic compound) with a melting point much higher than that of the solders.

This feature is welcome by 3D MEMS and IC heterogeneous integration. For example, after the bonding of a MEMS device with an ASIC wafer with a low melting solder, all the bonding (solder interconnect) areas become the IMC with a very high re-melting temperature. When a cap wafer is bonded to the ASIC wafer (already bonded with the MEMS device), the interconnect between the ASIC and the MEMS devices will not be reflowed. Furthermore, when the whole 3D MEMS and IC heterogeneous integration module is attached to the PCB with SMT (surface-mount technology) lead-free soldering (260 °C), the solder interconnects between the ASIC and MEMS, and cap and ASIC will not be reflowed. In this section, the feasibility of using low-temperature solder for bonding a nonfunctional 3D MEMS and IC heterogeneous integration package (Fig. 10.42) is demonstrated.

(a) **3D IC and MEMS Integration with Different Chip Sizes**

Figure 10.43 shows the dimensions and materials of the nonfunctional MEMS and ASIC, and cap. It can be seen that (a) the MEMS dimensions are 3 mm × 3 mm × 200 μm and has nine pads (200 μm × 200 μm) as shown in Figs. 10.43 and 10.44; (b) the ASIC dimensions are 5.5 mm × 5.5 mm with a sealing ring which is 300 μm width and 5.1 mm on each side of the ASIC as shown in Figs. 10.43, 10.45, and 10.46; and (c) both the bonding pads (for the MEMS device) and seal ring (for the cap wafer) are coated with low-temperature solders.

As in this case, usually the chip size between MEMS and ASIC for 3D MEMS and IC heterogeneous integration is not the same. Thus, wafer-to-wafer bonding of these two devices may not be a good idea, and the interconnections generally are

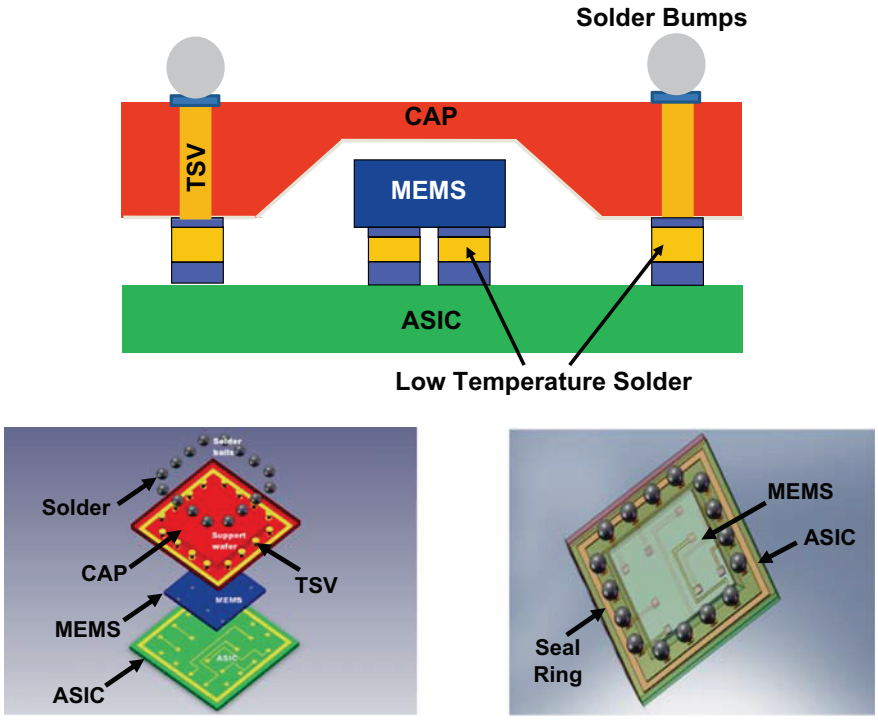


Fig. 10.42 3D MEMS and ASIC heterogeneous integration test vehicle

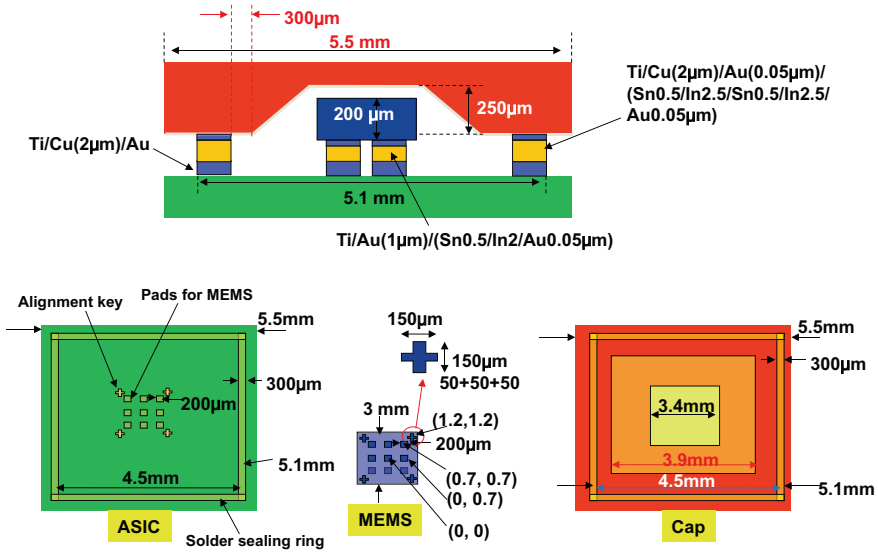


Fig. 10.43 Geometry and dimensions of the test vehicle

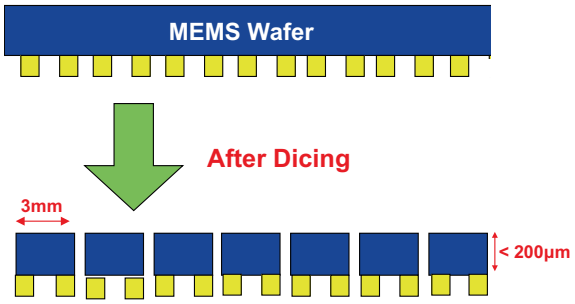


Fig. 10.44 Individual MEMS devices after dicing

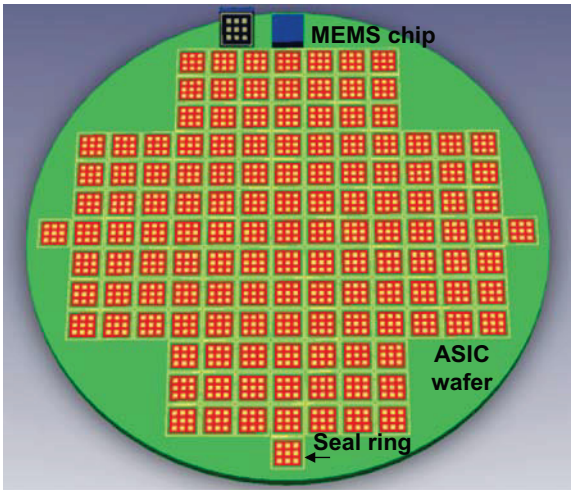


Fig. 10.45 Schematic of ASIC wafer showing the sites for MEMS devices

performed by either chip-to-chip or chip-to-wafer bonding. This section discusses a MEMS chip with only the (Ti/Cu/Au) UBM bonded to an ASIC wafer with the low-temperature solders (AuInSn) as shown in Fig. 10.43.

(b) **Cavity and TSVs in Cap Wafer**

Figures 10.47 and 10.48 show a 200 mm cap wafer with cavities fabricated by the KOH wet etch process and its typical cross-section. It can be seen that KOH etch yields a very smooth wall condition. The TSVs for the cap wafer are fabricated by DRIE (deep reactive-ion etching). The cavity and TSVs can also be made by laser machining and are shown in Fig. 10.49. Even its quality is not as good as that obtained by KOH etching; however, it is adequate for most of the applications. The surface conditions of the TSV made by laser machining are very rough and these may affect the electrical performance. Thus, in general, the TSVs for the cap wafer are made by DRIE process.

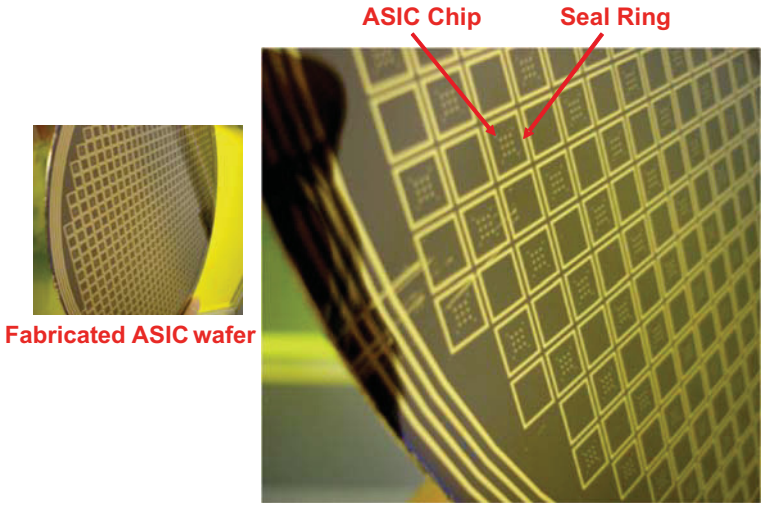


Fig. 10.46 ASIC wafer with the sites for MEMS devices and sealing rings

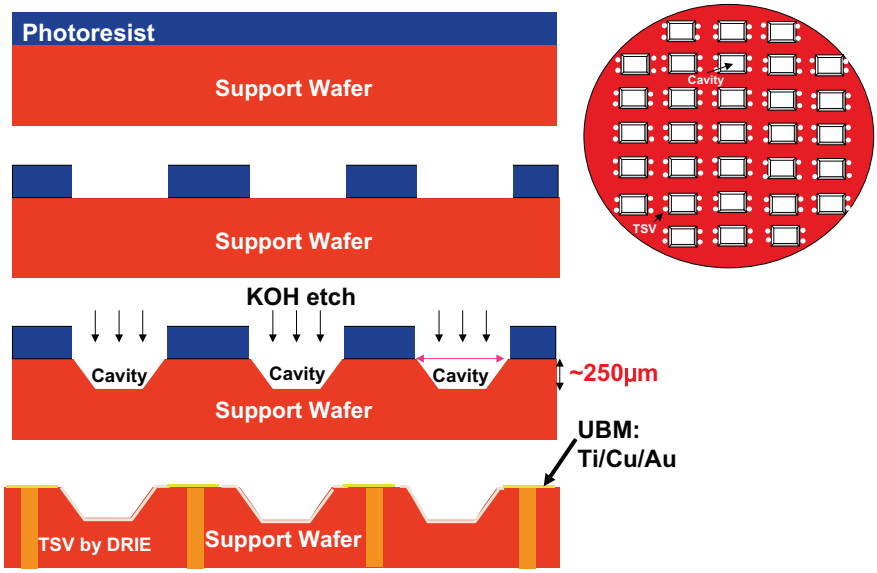


Fig. 10.47 Cap wafer with cavities fabricated by KOH wet etching

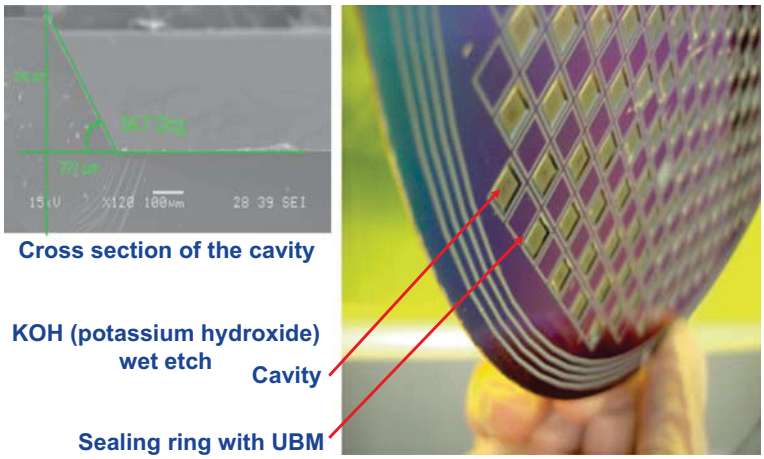


Fig. 10.48 The result of cap wafer fabrication (by KOH) wet process

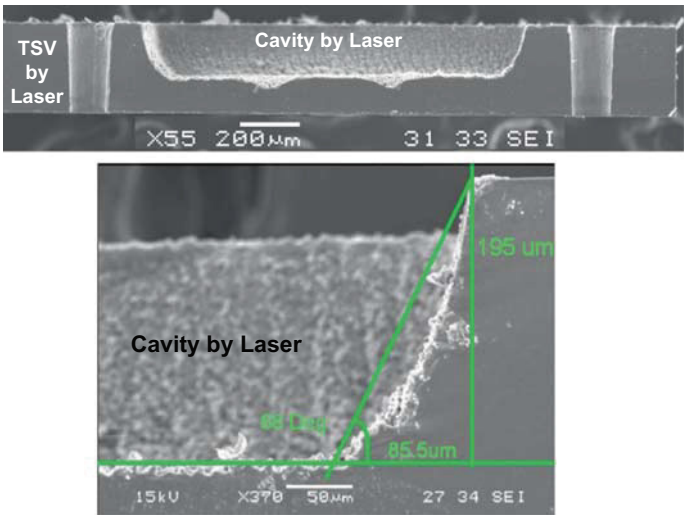


Fig. 10.49 Cap wafer with cavity and TSV fabricated by laser machining

(c) MEMS Chip to ASIC Wafer (C2W) Bonding

Figure 10.50 shows the assembly process of the nonfunctional 3D IC and MEMS heterogeneous integration. It can be seen that the ASIC wafer is fabricated with the sealing ring and pads that are coated with UBM and solder. Figures 10.50 and 10.51 show the MEMS chip picked up and placed on the ASIC wafer in an FC150 bonder. The bonding parameters are 6 MPa of bonding pressure at 200 °C on the bonding tool (MEMS) and 90 °C on the ASIC wafer, lasting for 40 s. The operation is

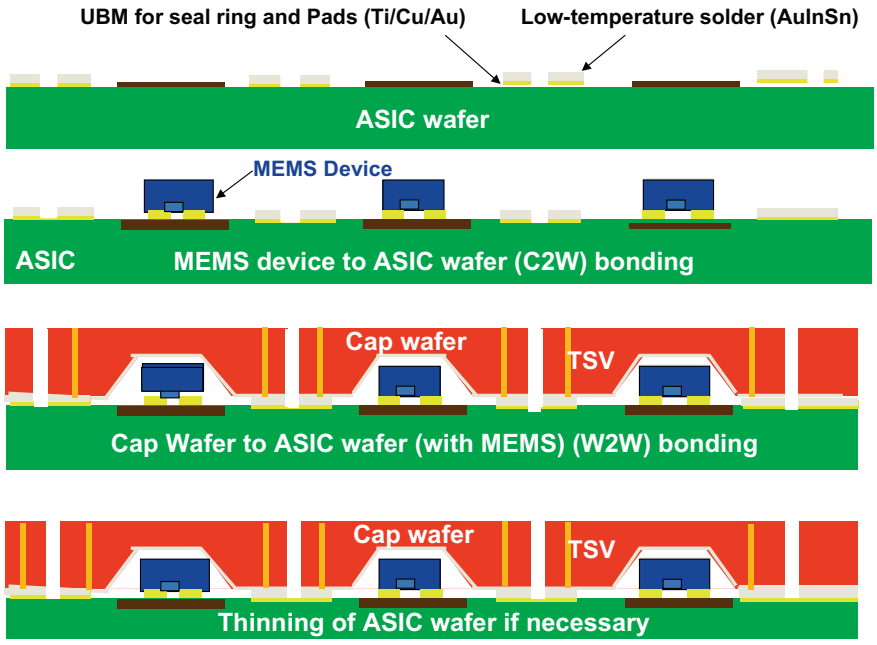
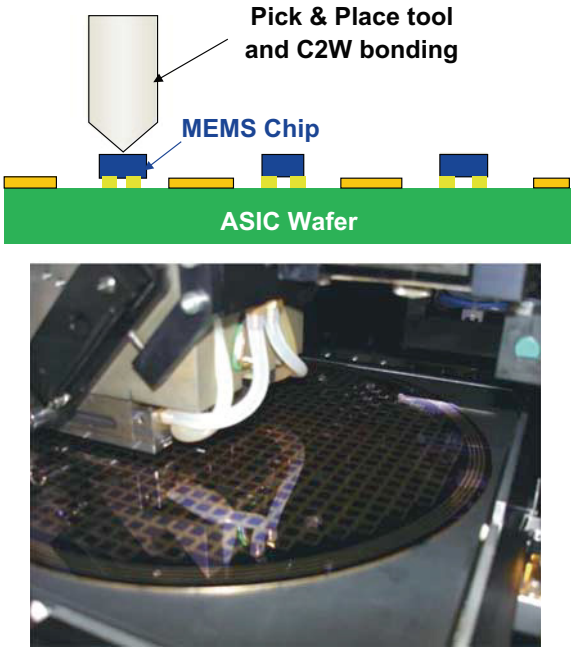


Fig. 10.50 Summary of the process steps of the 3D MEMS and ASIC integration

Fig. 10.51 C2W bonding of the MEMS device on the ASIC wafer



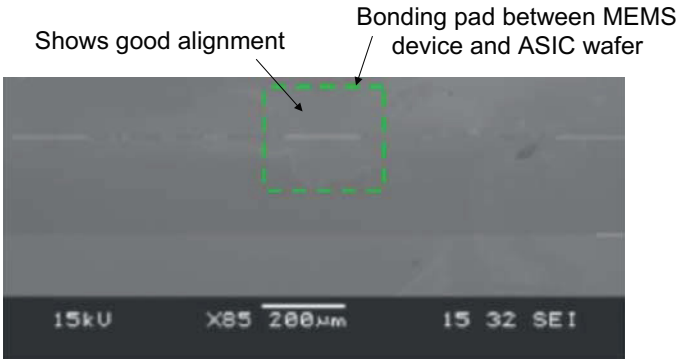


Fig. 10.52 SEM image of the cross-section of the MEMS/ASIC bonding

performed in an enclosed nitrogen environment. Figure 10.52 shows a cross-section of the bonding. There is no misalignment.

(d) **ASIC Wafer with MEMS Chips to Cap Wafer (W2W) Bonding**

As mentioned earlier, the cavity on the 200 mm cap wafer is fabricated by the KOH etch process. The seal ring on the cap wafer is coated only with the UBM. Figure 10.53 shows a schematic of the cap wafer bonding to an ASIC wafer with the MEMS device, which is accomplished in an EVG bonder with a pressure of 9 kN, temperature of 200 °C, and bonding time of 20 min. Figure 10.54 shows an X-ray photograph and SEM images of cross-sections of the wafer-to-wafer bonding of the ASIC wafer with the MEMS device and the cap wafer. It can be seen that (1) bond pads between the MEMS chip and the ASIC chip are in good alignment, and (2) there is no void in the solder sealing ring. Figure 10.55 shows the shear strength test results. All the chips meet the specifications. After solder bumping and dicing, one of the individual packages is also shown in Fig. 10.55.

10.4.4 Summary and Recommendations

Some important results and recommendations are summarized as follows [13–21]:

- The use of heterogeneous integrations of IC chips, MEMS devices, and TSV interposers are increasing.
- Most research papers have the TSVs in the cap without any devices (2.25 MEMS and IC integration).
- Some papers are with the TSV interposer supporting the MEMS device (2.5D MEMS and IC integration).
- There are a few papers such as the FBAR MEMS device bonded with a cap with IC device and TSVs and the use of low-temperature solder for bonding a 3D MEMS and ASIC heterogeneous integration.

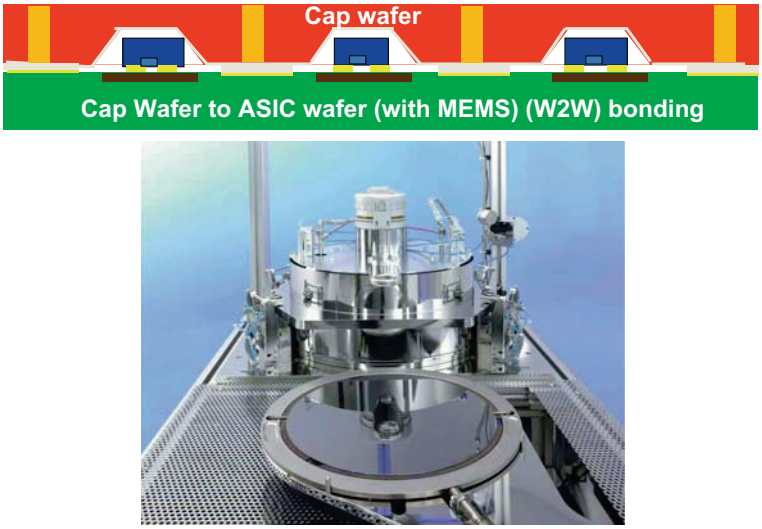


Fig. 10.53 W2W bonding of the cap wafer to the ASIC wafer already with the MEMS devices on

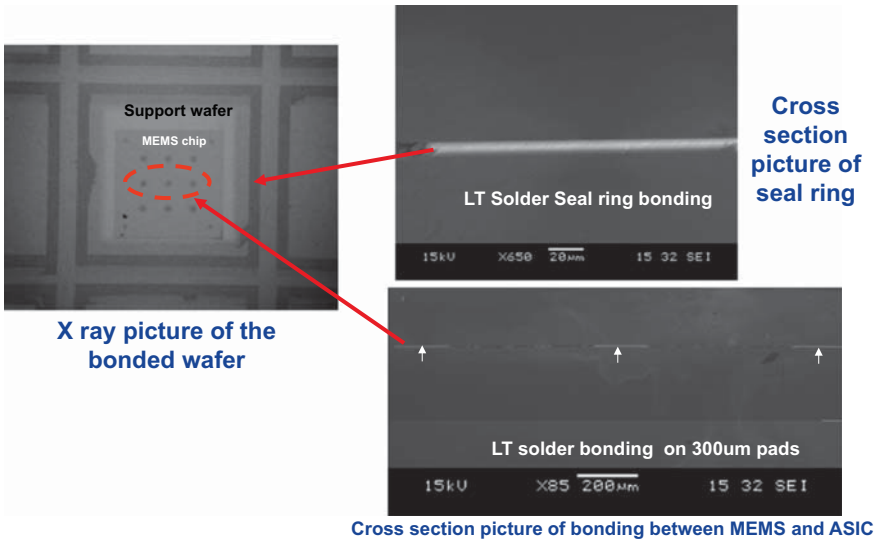
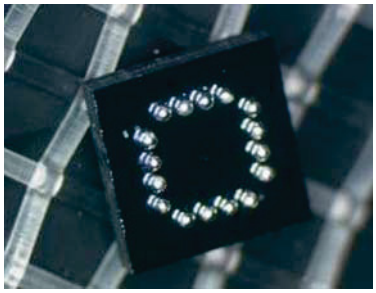


Fig. 10.54 X-ray and SEM images showing the sealing ring between the cap and the ASIC

Bond Force	Temperature	Time	Shear strength (Cap-ASIC)	Shear strength (MEMS – ASIC)
9KN	200°C	20m	71.6MPa	9.2MPa



Completed package with solder ball attached

Fig. 10.55 The complete 3D MEMS and ASIC integration package subjected to the characterization test

10.5 Heterogeneous Integration of VCSEL and PD

Low-cost (with bare chips) and high-performance (optical, electrical, thermal, and mechanical) optoelectronic systems embedded into a PCB (printed circuit board) or an organic laminated substrate are designed and described in this section [22–31]. These systems consist of a rigid PCB (or a substrate) with an embedded optical polymer waveguide, an embedded VCSEL (vertical cavity surface emitted laser), an embedded driver chip, an embedded serializer, an embedded PD (photodiode) detector, an embedded TIA (transimpedance amplifier), an embedded deserializer, embedded heat slugs, and a heat spreader. The design and fabrication of a simpler system will be presented first.

10.5.1 Embedded Board-Level Optical Interconnects

(a) **The Structure**

Figure 10.56 shows a single-channel OECB (opto-electronic circuit board) with embedded waveguide using traditional PCB manufacturing process. The OECB is made up of four electrical layers and one optical layer embedded below a 60 μm-thick substrate. Two optical vias with 100 μm diameter are formed to guide the optical beam from VCSEL to the 45° mirror coupler. Likewise, optical beam exiting the waveguide is diverted from the 45° mirror coupler through the optical via and received by the photodetector.

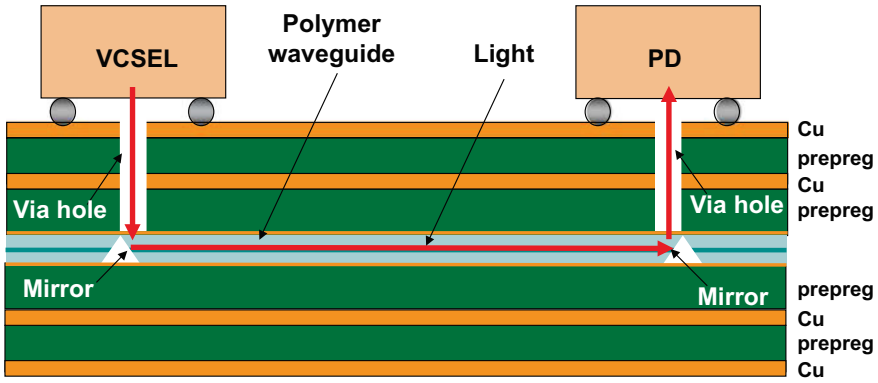


Fig. 10.56 Schematic of fully embedded board-level optical interconnect system

A 10 cm-long embedded polymer waveguide consists of a 70 μm core and a 15 μm-thick top and bottom cladding. Two 45° mirror couplers are formed at both corners of the waveguide by using 90° diamond dicing blade. These mirrors convert optical beam emitted from VCSEL in the vertical path to the planar direction and into the waveguide.

(b) **Fabrication of Polymer Waveguide**

Various fabrication processes are used to fabricate the flexible polymer waveguide, such as photolithography [32, 33], RIE (reactive ion etching), hot embossing, and soft molding [34]. In this section the soft-molding method is discussed, as it is cost effective and convenient to fabricate micro and nanostructures [32–36]. Soft molding is suitable for replicating 3D structures in single-step and for mass production or small quantity in prototyping.

The fabrication process of the waveguide using the UV-curable fluorinated acrylate material is divided into four steps, as shown in Fig. 10.57. First, a layer of bottom cladding material (WIR30-RI) is spin coated on top of the copper polyimide film with a supporting substrate. Second, the PDMS (poly dimethylsiloxane) mold is placed on top of the bottom cladding material. It is then filled up with the core material and is UV cured inside a nitrogen environment. The polymer waveguide is 10 cm long with a 70 μm core cross section. Third, the soft mold is removed from the polymer substrate. Finally, it is spin coated with another layer of cladding material as top cladding and then it is UV cured.

(c) **Fabrication of the 45° Micro-Mirror**

To construct a 3D optical interconnection between waveguides and active optical devices, integrated micro-mirrors are often introduced to assist in deflecting the optical light into/out of the waveguide. Hence, the micro-mirror is an essential basic component for 3D optical interconnections [37]. Till now, the fabrication processes of the micro-mirror have been done by laser ablation [24, 38], grayscale lithography

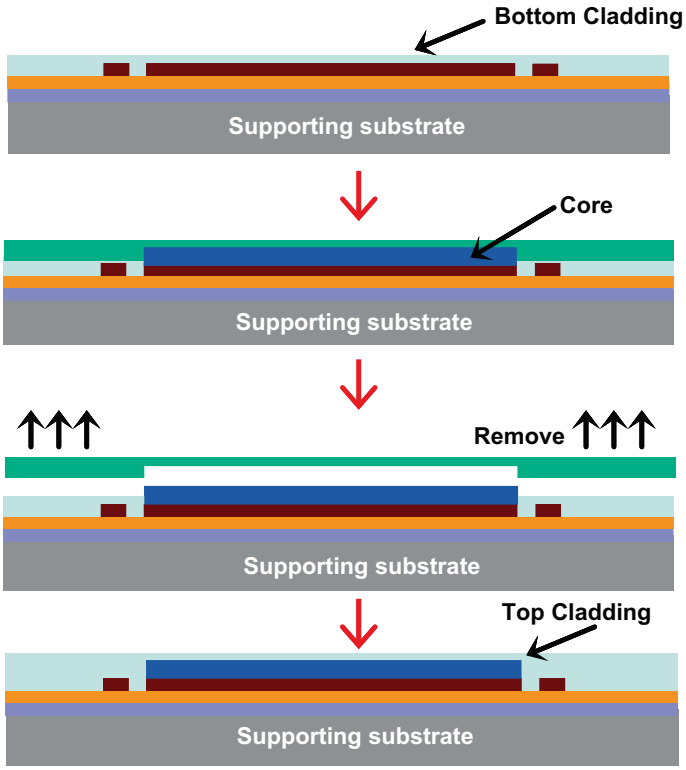


Fig. 10.57 Steps in fabricating the polymer waveguide

[39], dicing [40], x-ray lithography [41], reactive ion etching [42], and molding [43]. The dicing method is discussed in this section.

After the waveguide is fabricated, the next process fabricates the 45° micro-mirror by mechanical dicing using 90° diamond dicing blade. A few key design issues including the positioning of the mirror, the tilting of the mirror, the angle of the mirror, and the mirror surface roughness should be noted when fabricating the micro-mirror because these issues affect the coupling efficiency. Therefore, a set of different dicing parameters are selected for the fabrication of the 45° micro-mirror (Table 10.2). This table provides the spindle speed and the feed rate, which affect the

Table 10.2 Dicing parameters for dicing mirror

Samples	Spindle speed (rpm)	Feed rate (mm/s)
X1	35,000	1
X2	35,000	5
X3	45,000	1
X4	45,000	5

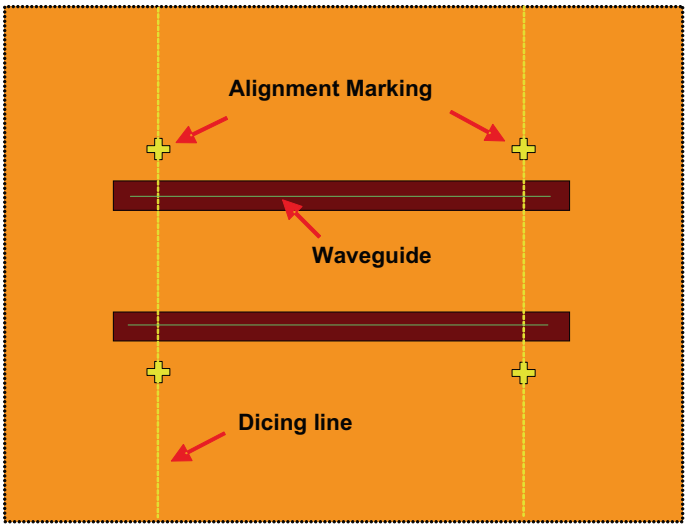


Fig. 10.58 Top view of the optical waveguides and alignment marks

roughness and the angle of the micro-mirror. The result will determine which set of dicing parameter is able to achieve the expected requirement.

The optical waveguide supported by the substrate is mounted on the dicing machine. It is then aligned using the alignment marking, as seen in Fig. 10.58. The micro-mirror is diced at the dicing line position and the 45° micro-mirror is formed. Figure 10.59 shows the side view of the optical waveguide with the micro-mirror.

After the 45° micro-mirror is formed, the next step is to ensure that the angle of the micro-mirror is within the range. To obtain the angle of the micro-mirror, the optical waveguide is cross-sectioned and is determined using SEM. When the image is captured using the SEM, 3D graphical software is used to measure the angle of the micro-mirror, as seen in Fig. 10.60. The following steps explain how the angle is measured:

[1] A baseline is drawn parallel to the plane.
[2] Mirror line is drawn along the edge of the mirror. Two mirrors are drawn, which intersect at a point.
[3] A dividing line perpendicular to the baseline is drawn through the intersect point of the mirror lines, which forms 90°.
[4] Using the 3D graphical software measuring tool, the angle from mirror line 1 to the dividing line is measured, which creates Angle 1, as shown in Fig. 10.60. For Angle 2, the angle from mirror line 2 to the dividing line is measured.

Finally, the angle measurement results (Angle 1 and Angle 2) are tabulated according to the set of dicing parameters as determined earlier on.

There is no perfect 45° micro-mirror. The defect will affect the coupling efficiency. Due to the defect form, the mirror area becomes smaller and the coupling light

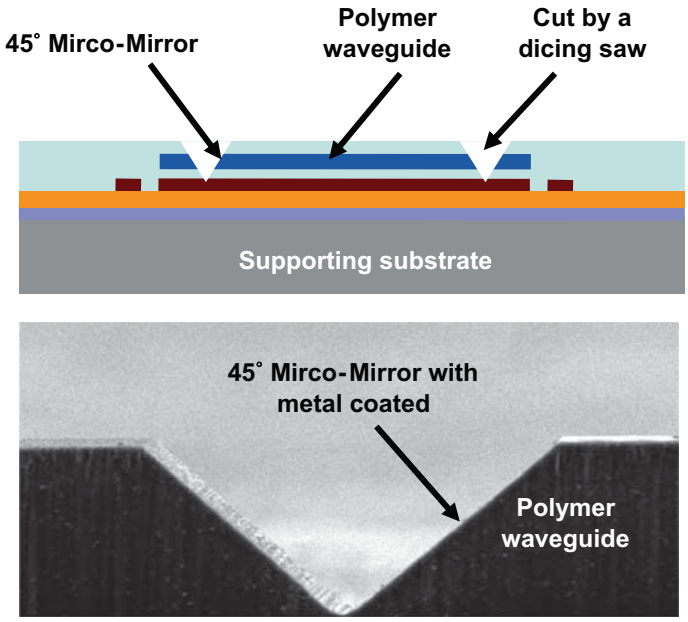


Fig. 10.59 (Top) Schematic of the 45° micro-mirror. (Bottom) Side view of the 45° micro-mirror

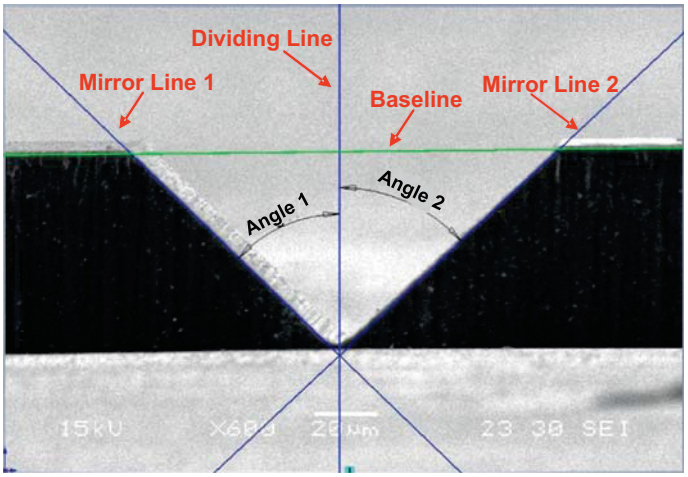


Fig. 10.60 Measurement of the 45° micro-mirror

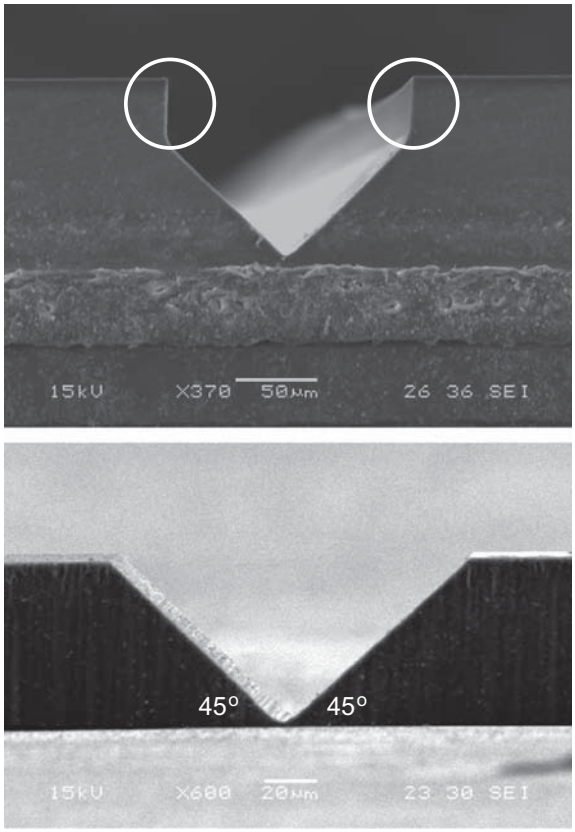


Fig. 10.61 (Top) Side view of the 45° micro-mirror (half cured). (Bottom) Side view of the 45° micro-mirror (fully cured)

source is unable to deflect accurately into the waveguide core and coupling out to the receiver, which increases the optical loss. Due to this, the analysis of the waveguide is carried out. To ensure that the curing condition of the waveguide causes the defect, a comparison test is carried out. Both waveguides are fabricated with different curing conditions, one is fully cured and the other is partially (half) cured. After this the waveguides are diced to form the micro-mirrors. The partially cured waveguide has the defect form, as shown in the top of Fig. 10.61, and the fully cured waveguide has a perfect 45° micro-mirror shape without defect, as shown in the bottom of Fig. 10.61. Therefore, the waveguide must be fully cured, and the optimizing curing condition for the waveguide is UV intensity of 15 to 18 mW/cm^2 for 1.5 h in a nitrogen environment.

The reason that causes the defect is that the aspect ratio of the spin rate and feeding speed provides sufficient removal rate to remove the waveguide materials at the tip of the V-groove. However, due to the increase in the removal volume at the top surface, the aspect ratio is no longer sufficient for the removal rate. Therefore, during the dicing process, the dicing blade pushes aside the waveguide material instead

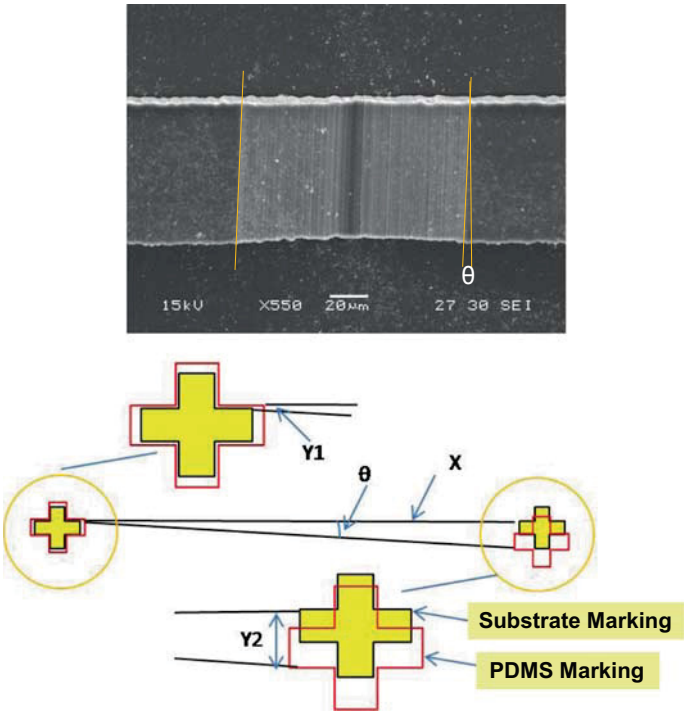


Fig. 10.62 (Top) Mirror titling (without alignment). (Bottom) Measurement of the position of waveguide

of removing the waveguide materials. Then, it recovers after the blade loading is removed, which results in the defects as shown in the top of Fig. 10.61. This shows that the waveguide materials experience the elastic deformation during the dicing process. This does not happen for cured waveguide materials, as shown in the bottom of Fig. 10.61. Therefore, it is believed to be due to the uncured waveguide material that is still in soft and elastic state.

Under the SEM, another issue is found. From the top view of the waveguide, as seen in the top of Fig. 10.62, a slight tilting of the mirror is observed. The positioning and the tilting of the angle of the mirror affect the optical coupling efficiency, as a result there is an increase in optical loss. In order to correct the displacement error in placing of the core of the waveguide, precision alignment bonder is used to minimize the waveguide tilting; the bottom of Fig. 10.62 shows how the measurement was carried out.

A set of alignment marks, as seen in Fig. 10.58 (top view of the waveguide substrate), is used to align the PDMS soft mold, which is used to fabricate the core of the waveguide. On the PDMS mold, there is a set of alignment marks similar to the marking on the waveguide substrate. The two sets of marking are placed on top of each other; this is the perfect scenario for a perfect alignment without errors. But error

always occurs and alignment system is implemented to minimize the misalignment. For normal placement of PDMS mold, there will be misalignments that will cause tilting of the waveguide. Table 10.3 shows the different sample misalignments of the placement of PDMS mold by manual alignment; the angle of tilting causes the tilting of the mirror angle.

As the dicing machine moves in the straight line, normal to the waveguide materials with reference to the alignment marks, the angle is formed by the placement of the core that causes the tilting of the mirror. That is why placement of the core is crucial, and therefore, high accuracy alignment machine is used to place the core so that the slanting is minimized. Because of the tilted angle of the mirror, the coupling light will not completely couple to the core. Small amount of the coupling light will be lost due to the angle error.

Using the alignment system provides a huge improvement in alignment issue. Table 10.3 shows a few sets of measurement by alignment system. According to the result in Table 10.3, the average angle of the tilting for alignment system is 0.006. This minimizes the tilting angle and improves the mirror angle, reducing the coupling loss; the average angle of the tilting for manual alignment is 0.36 (Table 10.4).

Different spindle speed and feed rate affect the angle of the mirror and the roughness of the mirror. After dicing using a set of dicing parameters given in Table 10.2, an optimized dicing parameter is chosen. Table 10.5 lists the results of the angles of micro-mirrors of different sets of dicing parameters, which are measured using SEM and 3D graphical software as mentioned earlier. From Table 10.5, the angle that meets the requirement is obtained for the dicing parameter: spindle speed of 35,000 rpm and feed rate of 1 mm/s. For this micro-mirror Angle 1 is 45.23° and Angle 2 is 45.85°, which are within the range of 45 $\pm$ 1°. For dicing parameter of spindle speed of 45,000 rpm and feed rate of 1 and 5 mm/s, the angle of the micro-mirror is out of the range, and affects the coupling efficiency. The angle is

Table 10.3 Results of the alignment difference in *y*-Axis (alignment system)

Samples	Y1 (μm)	Y2 (μm)	Θ (°)
1	0	3	0.008
2	1	3	0.006
3	1	4	0.008
4	0	1	0.003
Average			0.006

Table 10.4 Results of the alignment difference in *y*-Axis (manual placement)

Samples	Y1 (μm)	Y2 (μm)	Θ (°)
1	10	123	0.32
2	15	44	0.30
3	8	54	0.45
Average			0.36

Table 10.5 Result of the angle of the micro-mirror

Samples	Spindle speed (rpm)	Feed rate (mm/s)	Angle 1 (°)	Angle 2 (°)
X1	35,000	1	45.23	45.85
X2	35,000	5	46.79	45.73
X3	45,000	1	39.93	46.58
X4	45,000	5	43.98	42.39

Table 10.6 Result of the roughness of the micro-mirror

Samples	Spindle speed (rpm)	Feed rate (mm/s)	Roughness (nm)
X1	35,000	1	316
X2	35,000	5	355
X3	45,000	1	340
X4	45,000	5	389

Table 10.7 Roughness Result for spindle rate (35,000 rpm) and feed rate (1 mm/s)

	Roughness (nm)
1	0.313
2	0.307
3	0.312
4	0.309
5	0.312
6	0.315
7	0.317
8	0.322
9	0.325
10	0.324
Average	0.316
Std. dev.	0.006

either smaller or bigger than 45°, which affects the optical loss as the coupling light is unable to accurately deflect into the core of the waveguide.

Next, the roughness of the mirror surface is measured, taking 10 different areas of the surface of the mirror for measurement and getting the mean of the roughness of the surface. Table 10.6 provides the result of the roughness in these 10 different areas of the mirror surface. The average of these values is 316 nm with standard deviation of 0.006. Table 10.7 shows that the best roughness result is for spindle speed of 35,000 rpm and feed rate of 1 mm/s as compared to the rest. The remaining dicing parameters, even though their roughness is close to 316 nm, are not able to achieve the angle requirement. Therefore, the spindle speed of 35,000 rpm and feed rate of 1 mm/s is the preferred dicing parameter.

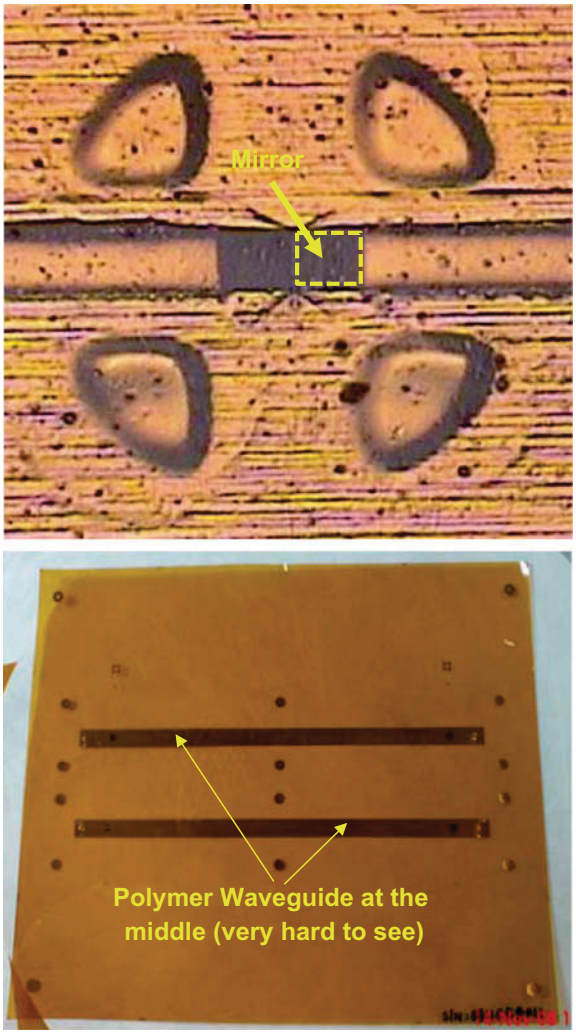


Fig. 10.63 Optical images of the micro-mirror and polymer waveguide on a polyimide film

(d) **Assembly Process of the OECB**

Figure 10.63 shows the optical images of the micro-mirror and polymer waveguide on a polyimide film. Two critical challenges are needed to be resolved in assembling the OECB: (a) adhesion of lamination between waveguide and prepreg material, and (b) precision of layer-to-layer alignment between waveguide mirror, PCB vertical-optical channel, and optical devices packaging. In consideration of these two points, the fabrication process is designed and developed [28] and shown in Figs. 10.64 and 10.65.

Before laminating, surface pretreatment, such as plasma, micro-etching, or pumice, is conducted on the surface of waveguide layer. This pretreatment can

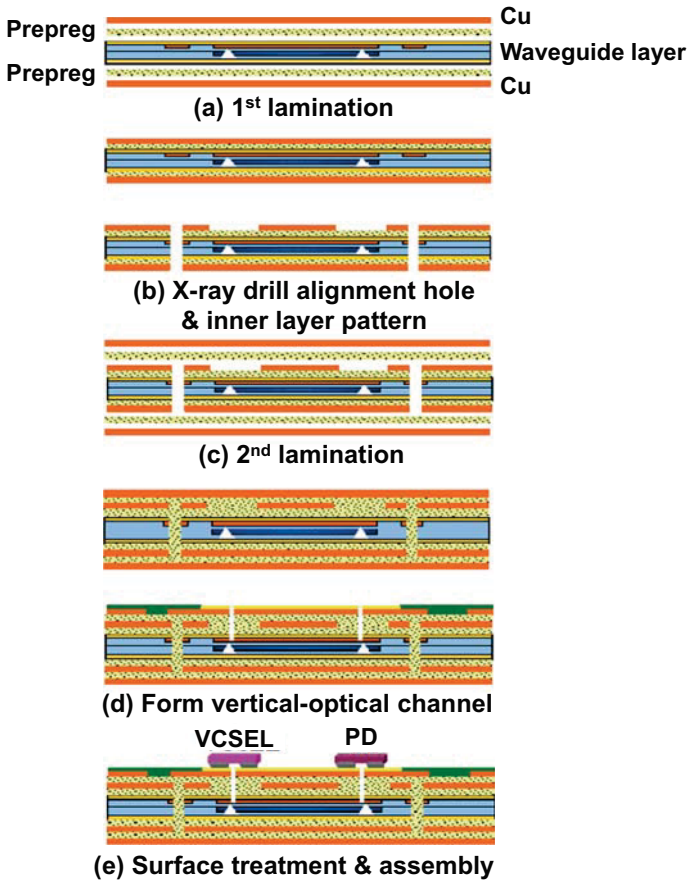


Fig. 10.64 Fabrication process of the OECB

increase the surface roughness; therefore, adhesion between waveguide layer and prepreg can be increased as well. Then, stack up with waveguide layer located in the center between two pieces of prepreg and copper foils, perform the laminating process, and form the sandwich structure of copper–prepreg–waveguide–prepreg—copper, which is called L2/L3, as shown in Fig. 10.64. The laminating condition is 200 °C for 100 min. After laminating, X-ray is used to detect alignment marks and to drill out alignment holes used for L2/L3 patterning, and the same method is used for L1/L4 laminating. Also, use X-ray to drill out alignment holes, and proceed drilling through the holes and copper plating. Then form vertical-optical channel to make the mirror exposed. Finally, outer layer patterning, surface finishing, and a 4 + 1 layer OECB are completed.

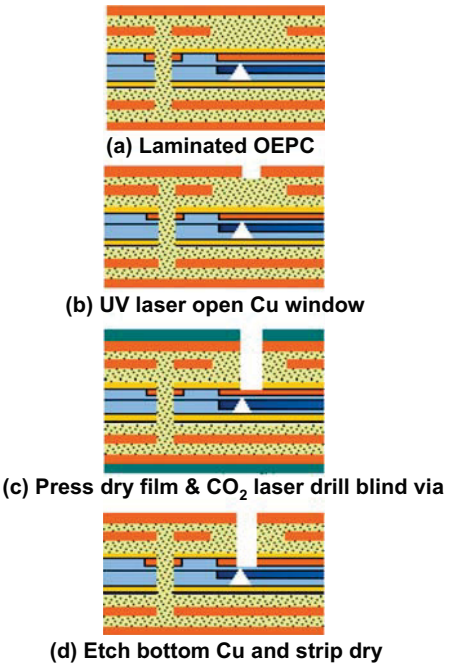


Fig. 10.65 Fabrication process of the vertical-optical channel

(e) Fabrication Process of Vertical-Optical Channel

Fabrication of vertical-optical channel is the most important step of the whole process. A special process is designed and discussed as follows. Three key points are discussed in this section. The first is how to align with mirror in the inner layer of PCB from the top layer; the second is how to control the roughness of the channel wall; the third is how to control the shape of the channel. The special fabrication process is shown in Fig. 10.65.

First, use UV laser to open a copper conformal mask on the desired location of vertical-optical channel, and press the dry film on the surface. The UV laser can precisely find the location and drill directly. Use CO_2 laser to ablate prepreg and form a blind via; the roughness of the wall can be optimized by adjusting laser parameter. Then, remove bottom copper by flash etching, strip the dry film, and form the vertical-optical channel. Finally, use the conventional HDI (high density interconnect) process and finish the OECB.

(f) Final Assembly

After OECB is completed, SMT (surface mount technology) is used to do the final assembly. Solder paste SAC305 is used, and the maximum temperature is 240 °C. The solder pad size of VCSEL and PD is only 80 μm, so micro-lens is used for soldering. The selected VCSEL can emit laser beam with 850 nm wave length, frequency can reach 5 Gbps, diameter of emitter opening is 13 μm, and light dissipation angle is

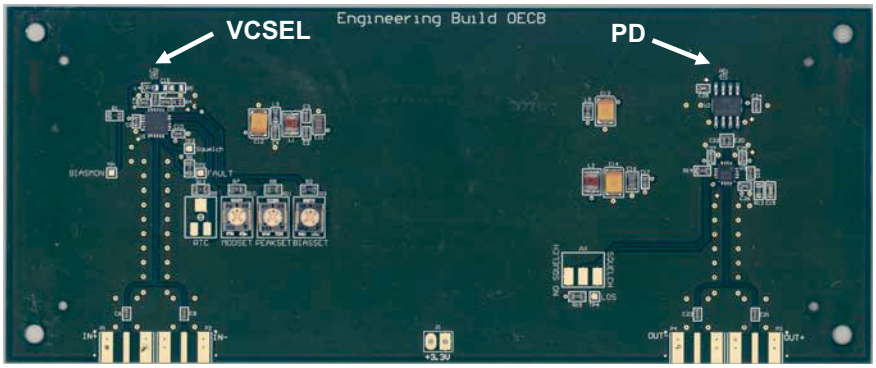


Fig. 10.66 Top view of the assembled OECB

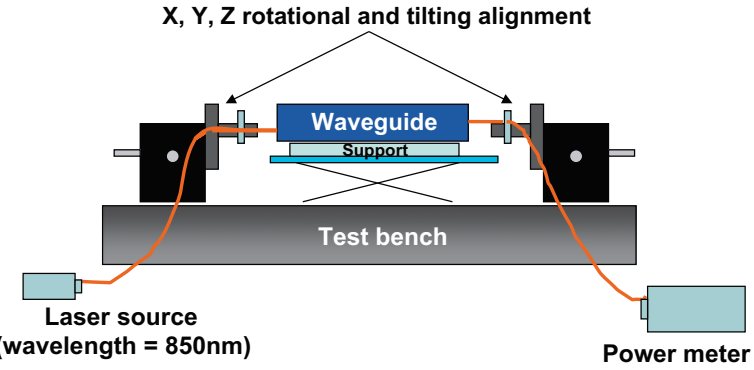


Fig. 10.67 Measurement setup for propagation loss and insertion loss

about 17°. The assembled sample is shown in Fig. 10.66 and the size is 12 cm × 5 cm. The test setup is shown in Fig. 10.67 and some of the measurement results can be found in [26, 28, 44].

10.5.2 3D Heterogeneous Integration of Embedded OECB

(a) **The Structure**

A 3D hybrid optoelectronic system with electrical and photonics ICs for super-thin, super-light, high-performance, and low-cost applications, as shown in Fig. 10.68, is proposed [29–31]. The entire system consists of a rigid PCB made of FR4 material (or an organic substrate) with an embedded optical polymer waveguide, an embedded VCSEL, an embedded LD (laser driver), an embedded serializer, an embedded photodiode detector, an embedded TIA, an embedded deserializer, and heat slugs

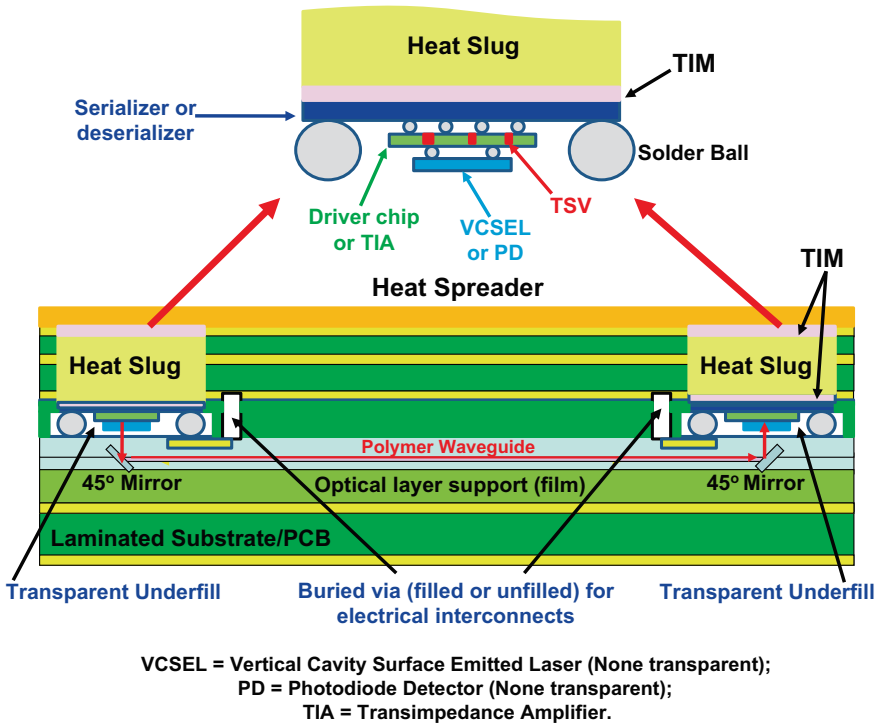


Fig. 10.68 Embedded hybrid 3D heterogeneous integration of opto-electronic interconnects

with or without heat spreader. The bare VCSEL, LD, and serializer chips are stacked and then attached on one end of the embedded optical polymer waveguide in the PCB. It is noted that since the VCSEL is so close to the mirror of the optical polymer waveguide, an optical lens is optional. Similarly, the bare photodiode detector, TIA, and deserializer chips are stacked and then attached on the other end of the embedded optical polymer waveguide in PCB. Both the 3D stacked chip sets are encapsulated by special underfills, e.g., transparent polymer.

(b) **Assembly Process**

As shown in Fig. 10.68, the VCSEL (with light emitting from the backside of the chip) is flip chip bumped with any materials on the VCSEL driver chip with TSV, which is solder bumped flip chip on the serializer chip. Larger bumps with any materials are mounted on the serializer chip while it is in a wafer format.

After dicing the 3D hybrid IC chip set, it is placed on the PCB (or substrate) on top of the polymer waveguide. Special encapsulants such as the transparent polymer may be needed to protect the chip set. If it is needed, a heat slug or any conductive material can be attached to the back side of the serializer chip by a TIM (thermal

interface material). Again, if it is needed, a heat spreader can be attached to the top side of the heat slug with a TIM.

Similarly, the photodetector chip is solder bumped flip chip on the TIA chip, which is then solder bumped flip chip on the deserializer chip. The thermal management techniques are the same as those of the VCSEL chip set. In this case, underfills may be needed between the VCSEL chip and VCSEL driver chip; the VCSEL driver chip and serializer chip; the PD chip and TIA chip; and the TIA chip and deserializer chip.

(c) **An Example**

A low-cost embedded 3D hybrid optoelectronic system with electrical and photonics ICs for board-level applications, as shown in Fig. 10.68, is designed and analyzed [29–31]. The entire system consists of a rigid PCB made of FR4 material with an embedded optical polymer waveguide, a 10 Gbps VCSEL (0.31 mm × 0.4 mm × 0.2 mm, 2.2 V, 33mW, 16 W/cm^2), a 10.7 Gbps LD (2 mm × 2 mm × 0.3 mm, 3.3 V, 0.35 W, 6.35 W/cm^2), a 10 Gbps 16:1 serializer or multiplexer (4.5 mm × 4.5 mm × 0.8 mm, 3.3 V, 2.5 W, 2.5–6.7 W/cm^2), a 10 Gbps photodiode detector (0.31 mm × 0.4 mm × 0.23 mm), a 10.7 Gbps transimpedance amplifier or TIA (2 mm × 2 mm × 0.3 mm), a 10 Gbps 1:16 deserializer or demultiplexer (4.5 mm × 4.5 mm × 0.8 mm, 3.3 V, 2.5 W, 2.5–6.7 W/cm^2), and heat spreaders. The optical, thermal, and mechanical design philosophy and their metrics of the proposed 3D optoelectronic system are given and the analysis results are discussed.

(d) **Optical Design Philosophy, Simulation, and Results**

Besides the heat slug/spreader, Fig. 10.68 shows that the top most layer of the 3D system contains a parallel to serial electrical converter called serializer. The serializer converts the 16-bit 622 Mbps parallel signals into a 10 Gbps serial signal which is fed to the next layer (the VCSEL LD) in the 3D system. The signal inputs to the serializer and VCSEL LD are re-routed using wafer level RDL (redistribution layer) deposition techniques. The VCSEL itself is solder bumped on the LD, which converts the incoming signal into an electrical driving signal for the VCSEL.

Again, Fig. 10.68 shows that the receiver schematic is similar to that of the transmitter except that the internal ICs are the receiving elements. The 3D stacked transmitter and receiver can be used for board-level optical interconnects with the transmitter output coupling to one end of the polymer waveguide, and the output on the other end of the polymer waveguide coupling to the receiver elements, as shown in Fig. 10.68.

For cost reduction, direct coupling (without lens) is used for optical coupling design in this study. The optical signal is coupled from the VCSEL directly into the waveguide through its mirror on one end, and from the waveguide directly to the photodiode through the mirror on its other end. For direct coupling, due to the divergence nature of the optical signal, it is critical to maintain the optical propagating distance as short as possible in order to achieve the desired coupling efficiency.

Based on a given structure, this minimum distance is determined by the assembly design of the optoelectronic components. For wirebonding component, the minimum

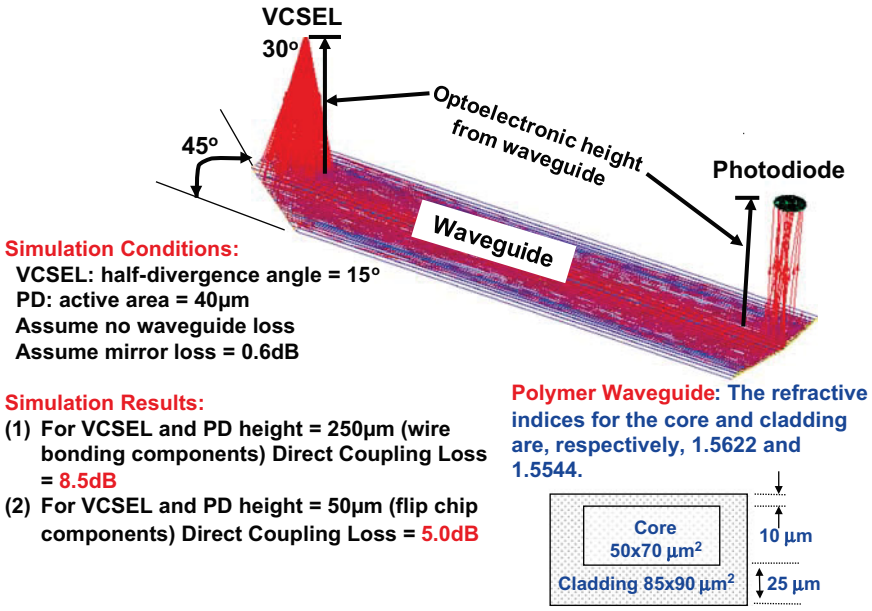


Fig. 10.69 Simulated model showing the direct coupling of the optical signal

distance or height is determined by the bonding wire loop, which is typically approximately 200 μm. On the other hand, for flip chip back illuminated optoelectronics components, the minimum height can be as close as possible (~100 μm for conventional solder bumps and ~25 μm for microbumps [29, 30]) without damaging the active area of the optoelectronic components.

The design of the optical waveguide is shown in Fig. 10.69. The waveguide is embedded in the FR4 PCB to give a complete planar design. The cross-sectional design of the waveguide is shown in Fig. 10.69 and the refractive indices for the core and cladding are, respectively, 1.5622 and 1.5544. At both ends of the waveguide, there is an out-of-plane reflector or mirror, which reflects the optical signal at 90°.

The optical simulation is done using the commercial software, ASAP, and Fig. 10.69 shows the layout used in the simulation. The VCSEL used in the simulation has a beam divergence of 30°, and the photodiode has an active area of 40 μm. The mirror on both sides of the waveguide is simulated with a loss of 0.6 dB, and the waveguide loss is not simulated. Using the above parameters, the coupling losses are 8.5 and 5 dB, respectively, for 250 and 50 μm heights (distances of the VCSEL and photodiode from the waveguide). Figure 10.70 shows the coupling losses for other heights. As expected, the greater the height, the larger the coupling loss.

The typical optical power from the VCSEL is 3 dBm and the responsitivity for the GaAs photodiode at 850 μm is 0.6 A/W. Assuming the waveguide loss is 0.1 dB/cm, the optical loss of a 10 cm long waveguide will be 1 dB. Also assuming that the minimum input optical power required for a 10 Gbps receiver is −13 dBm, then the

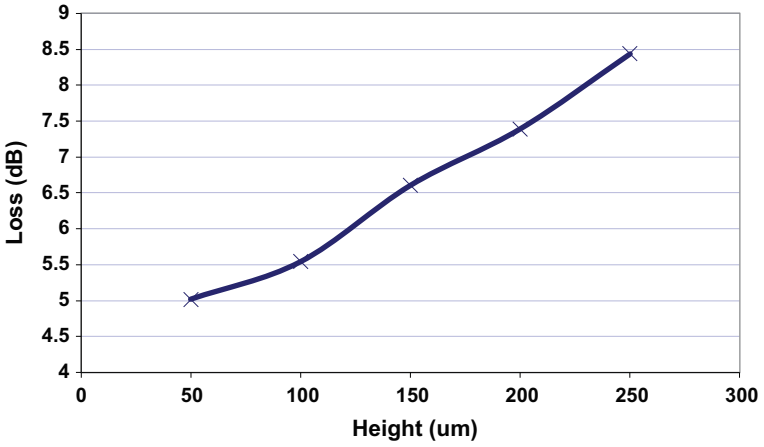


Fig. 10.70 Coupling loss versus the height of VCSEL

maximum optical acceptable coupling loss is approximately 15 dB. Therefore, the direct coupling schemes are feasible for the 10 Gbps OECB design.

(e) **Thermal Design Philosophy, Analysis, and Results**

The choice of a photonic package configuration requires recognition not only of critical cost issues and optical performances but also those of thermal performance and mechanical reliability. Since low-cost bare (VCSEL, PIN, LD, TIA, serializer, and deserializer) chips are used to stack up the optoelectronic structure, as shown in Fig. 10.68, thermal management is a critical issue. This is compounded with the high power dissipation of the 10 Gbps laser (2.2 V, 33 mW, and 16 W/cm^2), the 10.7 Gbps LD and TIA chips (3.3 V, 0.35 W, and 6–35 W/cm^2), and the 10 Gbps 1:16 serializer and the 10 Gpbs 16:1 deserializer (3.3 V, 2.5 W, and 2.5–6.7 W/cm^2); thus, how to take the heat out from these chips before they burn themselves is a challenge. In particular, a stable thermal environment is required for the VCSEL. Excursions from the desired operating temperature may alter the wavelength of the emitted light, consequently degrading the VCSEL's performance. In this study, the target temperature at the laser of the 10 Gpbs VCSEL is 85 °C.

Figure 10.71 shows the model for detailed analyses of a 3D hybrid IC heterogeneous integration for opto-electronic interconnects in organic substrates. It consists of the VCSEL, LD, and serializer on one side and the PIN, TIA, and deserializer on the other side (their dimensions are mentioned earlier). Since the transmitter and the receiver are similar, only half of the structure is modeled. It can be seen that there are three copper layers, four FR4 epoxy layers, one polymer waveguide, one optical layer support film, and a copper heat slug. The thickness of copper layers is 0.3 mm; of FR4 is 1.72 mm; of polymer waveguide is 0.085 mm; and of optical layer support film is 0.5 mm. The length of the polymer waveguide is 50 mm and the total

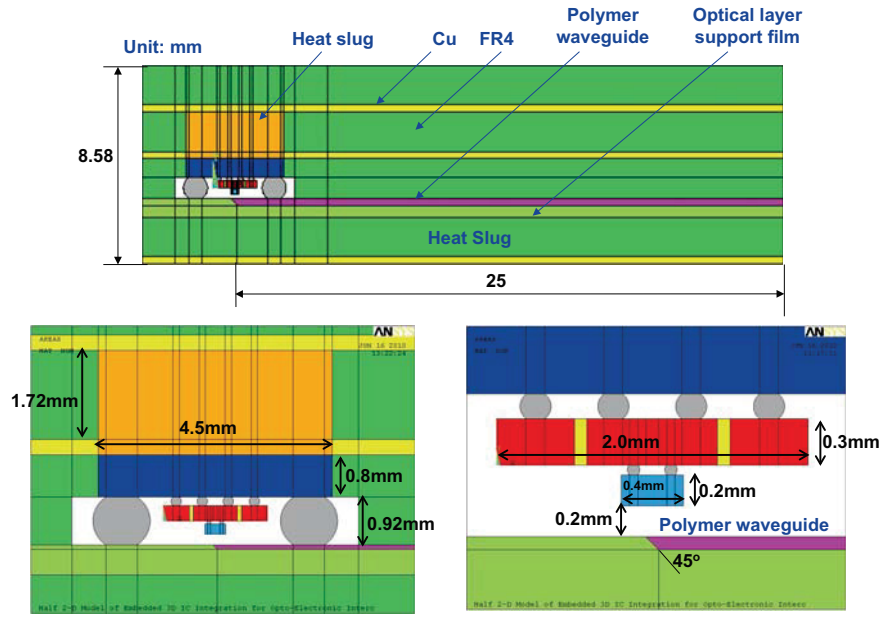


Fig. 10.71 Finite element modeling of the embedded 3D heterogeneous integration of opto-electronic interconnects in organic substrate

thickness of the OECB is 8.37 mm. The material properties of the structure are given in Table 10.8.

The thermal boundary condition is that 1 W of heat is applied to the VCSEL chip and the environmental temperature is 25 °C, as shown in Fig. 10.72. In service, most VCSEL will be switched on and off at a frequency of millions (or more) of cycles per second. Since the thermal time constant of the VCSEL structure is significantly greater than the period of the power-on/power-off cycling, the structure will equilibrate to a near-uniform operating temperature. We conservatively presume that the VCSEL has continuous power generation of 1 W that is uniformly distributed within the VCSEL. Also, since it is a linear heat-transfer analysis, one unit (1 W) is applied. In real application, most VCSEL is much less than 1 W. There is heat transfer between the package and the air. The heat convection conditions are applied on all the external package surfaces, where the environmental temperature is 25 °C and convection coefficient is 0.3 W/m^{2}K. For the embedded portion, there is no heat transfer between VCSEL chip and the air, since it is embedded in the PCB.

Figure 10.73 shows the temperature distribution in half of the OECB and at the critical area of the transmitter. It can be seen that the maximum temperature location is at the VCSEL and the magnitude is 64 °C, which is below the allowable specification (85 °C). Thus, the VCSEL should perform as expected.

Table 10.8 Material properties for modeling of the 3D hybrid integration

Component	PCB	Heat Spreader	Multi-Plexer	Laser Driver	VCSEL	Copper Layer	Solder Bump	Polymer Wave giude
Material	FR4	Cu	Si	Si	GaAs	Cu	63Sn-37Pb	Polymer Wave giude
Thermal Conductivity (W/m-K)	0.8	390	150	150	68	390	50.9	1.5
TCE (ppm/K)	15	17	2.7	2.7	5.6	17	24.5	251
Modulus (MPa)	21000	110000	131000	131000	85000	110000	25000	50
Poisson Ratio	0.18	0.34	0.28	0.28	0.3	0.34	0.35	0.3

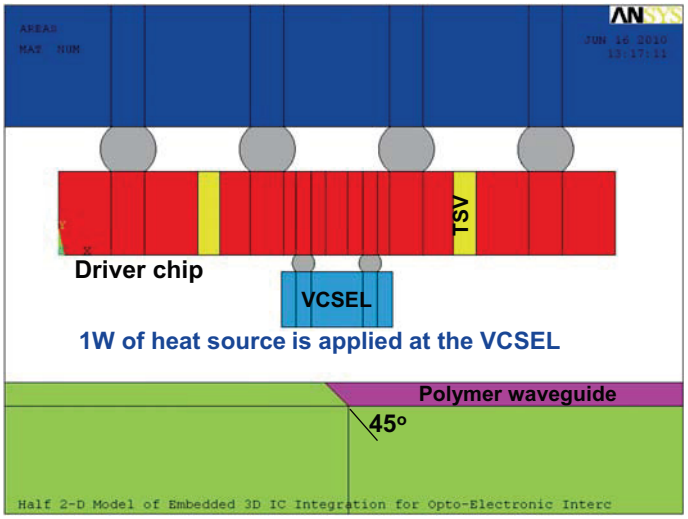


Fig. 10.72 Thermal boundary condition

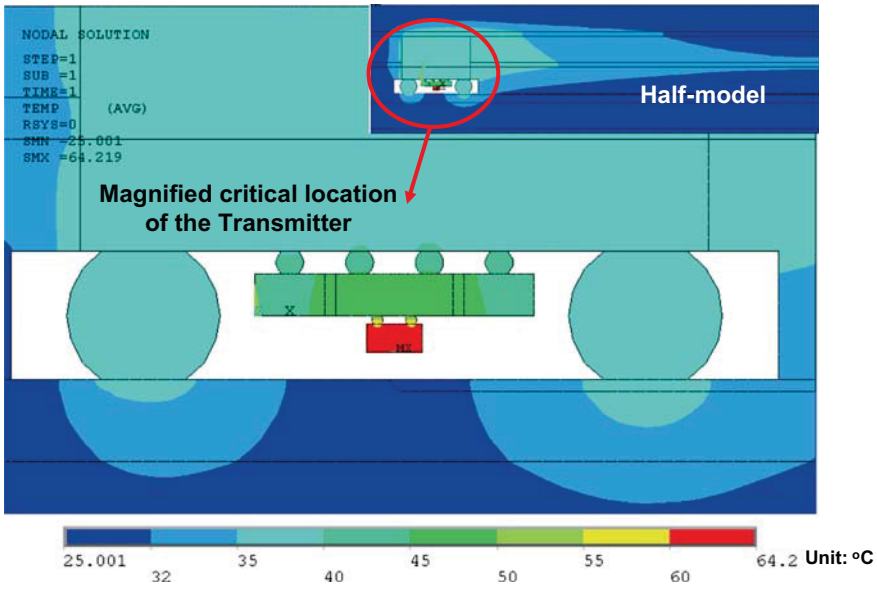


Fig. 10.73 Temperature distribution at the critical location of the 3D hybrid IC SiP

(f) Mechanical Design Philosophy, Analysis, and Results

As mentioned earlier, the choice of a photonic package configuration requires recognition not only of critical cost issues and optical and thermal performances but also those of mechanical reliability. Since low-cost bare chips with different material

properties (e.g., CTE) are used to stack up the optoelectronic structure, as shown in Fig. 10.68, the mechanical deflections of the VCSEL with respect to the mirror of the polymer waveguide, and stresses and strains of the solder joints of the OECB, which are caused by the global and local thermal expansion mismatches of the structure under the environmental stress condition (e.g., temperature cycling with $-25\ ^\circ\text{C} \leftrightarrow +140\ ^\circ\text{C}$, one hour per cycle), are critical issues. The main concern is the mismatch between the VCSEL and the mirror on the polymer waveguide. In this study, the allowable mismatch is 2 μm.

One of the functions of solder ball is to increase the stand-off height of the 3D stacked system and thus to relax the stress and strain acting on the solder joints. However, based on the optical performance of the laser of the VCSEL without lens, the stand-off height should be as small as possible. Thus, it is necessary to design a height of the solder ball such that the structure has enough compliance (for the solder-joint reliability) and still remain within the optical performance target. In this study, the target for the strain and stress per temperature cycle is, respectively, 2% and 45 MPa.

The simulation model is exactly the same as that for thermal simulation, except the symmetric boundary conditions that are applied at the center line. The thermal cycling boundary condition is shown in Fig. 10.74. It can be seen that the whole OECB is subjected to $-25\ ^\circ\text{C}$ for 15 min and ramp up to 140 °C for 15 min, then ramp down to $-25\ ^\circ\text{C}$. The ramp up and ramp down times are 15 min. The reference temperature is 25 °C, i.e., the stress-free condition. The residual stress is not considered, because the thermal expansion effect is the focus of this section.

Figure 10.75 shows the undeformed shape (left) and deformed shape (right) of the critical area of the transmitter of the OECB due to temperature cycling and the definition of mismatch between the VCSEL and the mirror on the polymer waveguide. Figure 10.76 shows the simulation results of the mismatch for various polymer waveguide lengths (25, 50, and 100 μm). It can be seen that the longer the polymer waveguide the larger the mismatch. However, they all are within the allowable specifications (2 μm).

Figure 10.77 shows the distribution of von Mises strain (upper) and stress (lower) acting on the solder joint. Again, their maximum values (0.14% and 35 MPa) are within the allowable specifications, and should be reliable under most of the operating conditions.

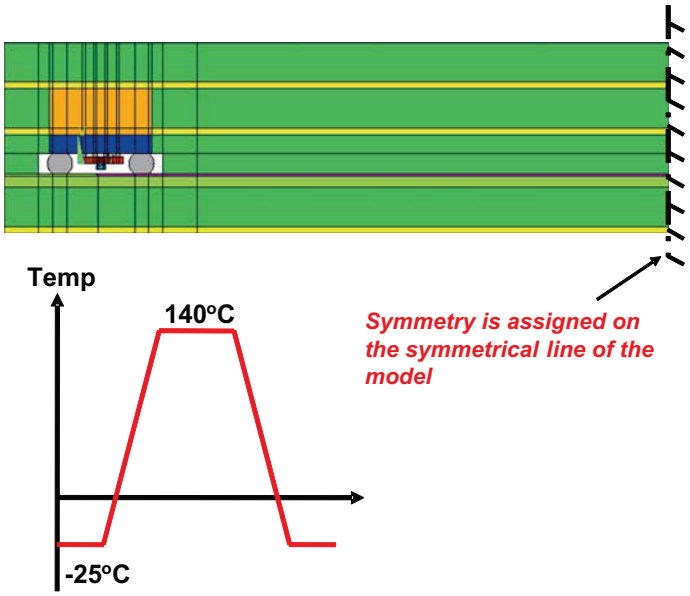


Fig. 10.74 Geometry and temperature loading boundary conditions for mechanical analyses

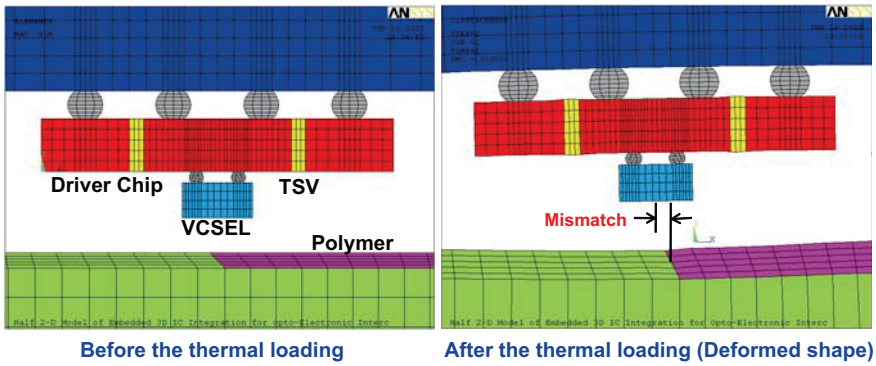


Fig. 10.75 Undeformed (left) and deformed (right) shapes of the transmitter (100x)

10.5.3 Summary and Recommendations

A generic lost-cost and high (optical, electrical, thermal, and mechanical) performance 3D hybrid IC optoelectronic heterogeneous integration system embedded into a PCB or an organic laminated substrate with an optical polymer waveguide is proposed. In addition, a special design is provided for demonstration through simulations. Some important results and recommendations are summarized as follows [29, 30]:

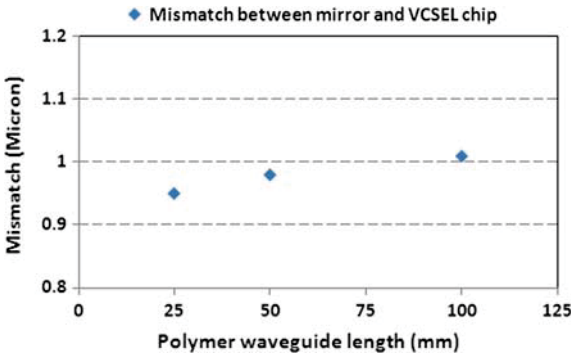


Fig. 10.76 Mismatch between the VCSEL and the mirror on the polymer waveguide as a function of waveguide length

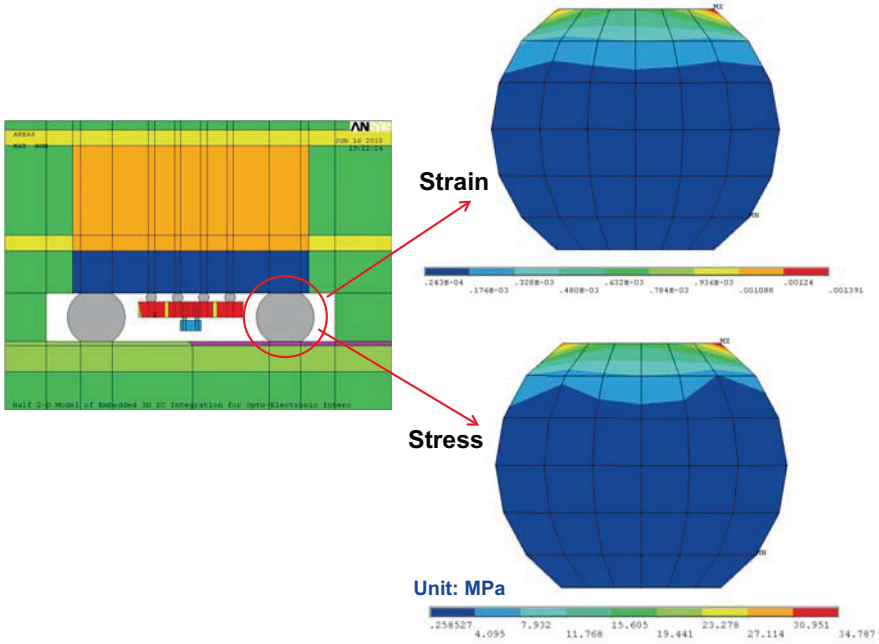


Fig. 10.77 von Mises strain and stress at the critical solder joint of the transmitter

- Heterogeneous integration of VCSEL and PD on OECB is finding its way into volume productions, especially for back panel applications.
- Optical analyses show that the current design of the cross-section of the optical polymer waveguide meets the optical acceptable coupling loss (15 dB). Therefore, the direct coupling schemes (without lens) are feasible for the 10 Gbps optical board-level interconnect.
- Thermal analyses show that when 1 W of heat is applied to the 10 Gbps VCSEL, with the current design, the maximum temperature at the VCSEL is only 65 °C, which is smaller than the specification (85 °C).
- Mechanical analyses show that when the whole embedded 3D hybrid IC heterogeneous integration is subjected to an environmental temperature cycling loading (−25 °C ↔ 140 °C), with the current design, the maximum mismatch (1 μm) between the VCSEL and the mirror of the polymer waveguide with different lengths is within the allowable specification (2 μm). The longer the length of the waveguide the larger the mismatch.
- Mechanical analyses show that when the whole embedded 3D hybrid IC SiP is subjected to an environmental temperature cycling loading (−25 °C ↔ 140 °C), with the current design, the maximum effective strain (0.14%) and stress (35 MPa) at the critical solder joint are less than the allowable specifications (2% and 45 MPa).

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Chapter 11
Trends in Heterogeneous Integrations



11.1 Introduction

Semiconductor industry has identified five main growth engines (applications), namely (1) mobile, (2) high-performance computing (HPC), (3) automotive (especially self-driving car), (4) internet of things (IoTs), and (5) big data (especially for cloud computing).

The system-technology drivers such as (1) 5G, (2) artificial intelligence (AI), and (3) machine learning (ML) are boosting the growths of these 5 semiconductor applications.

The packaging people are using various packaging methods such as wirebonding, flip chip, build-up substrate, PoP (package-on-package), WLCSP (wafer-level chip scale package), FOW/PLP (fan-out wafer/panel-level packaging), TSV (through-silicon via), 2.5D/3D IC integration, HBM (high bandwidth memory), multichip module/system-in-package (SiP)/heterogeneous integration, chiplets, and EMIB (embedded multi-die interconnect bridge) to house (package) the semiconductor devices for those 5 main applications. Because of the drive of 5G, AI, and ML, the semiconductors' density increases, pad-pitch decreases, and chip-size increases. All these provide challenges (opportunities) to packaging people.

11.2 Trends in Heterogeneous Integration

One of the packaging technologies is heterogeneous integration, which uses various packaging technologies to integrate dissimilar chips/components with different materials and functions, and designs from different fabless houses, foundries, wafer sizes, and feature sizes into a system or subsystem, rather than integrating most of the functions into a single chip and going for a finer feature size such as system-on-chip. For the next few years, we will see more of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption,

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signal integrity, and/or cost. How should these dissimilar chips/components talk to each other, however? The answer is: RDLs (redistribution-layers) [1, 2].

11.2.1 Heterogeneous Integration on Organic Substrates

In general, for high-volume manufacturing (HVM), 70% of the RDLs of heterogeneous integrations should be on organic substrates and the metal line width and spacing are $\geq$10 μm. (Most of these heterogeneous integrations are actually SiPs.) No more than 5% of the RDLs of heterogeneous integrations should be on organic substrates, and the metal line width and spacing are <10 μm.

Most of the heterogeneous integrations on organic substrates are assembled with SMT (surface mount technology) equipment. The use of wire bonding chips on board, solder bumped flip chips on board mass-reflow with other SMT components, embedded IPDs (integrated passive devices), coreless substrates, bump-on-leads, embedded-trace substrates, and substrate-like PCBs (printed circuit boards) will be increased. The organic substrates can be rigid or flexible and they are ranging from ordinary to high-density PCBs.

The build-up organic package substrates have been used extensively and the fabrication process is mainly SAP (semi-additive process). Currently, two core layers and 12 build-up layers (6-2-6) with 10 μm metal line width and spacing RDLs are in HVM. The organic interposer such as that proposed by Cisco [3] is finding its way to get into HVM. The i-THOP substrate with thin-film layer on top of the build-up layer proposed by Shinko (with 2 μm metal line width and spacing) [4, 5] is working to reduce yield losses.

11.2.2 Heterogeneous Integration on Non-organic Substrates

In general, for HVM, 25% of the RDLs of heterogeneous integrations would be on other (non-organic) substrates such as the silicon substrates (either passive TSV-interposers or active TSV-interposers or both), silicon substrate (bridges), fan-out RDL substrate, and ceramic substrate (which has not been discussed in this book). The metal line width and spacing of the RDLs are usually very small and can go down to submicron values.

(a) **Heterogeneous Integrations on Silicon Substrates (TSV-Interposers)**

The fabrication process of RDLs for heterogeneous integrations on silicon substrates (either passive TSV-interposers or active TSV-interposers) is by PECVD

(plasma enhanced chemical vapor deposition) and Cu-damascene + CMP (chemical-mechanical polishing). Currently, there are at least four RDLs and their minimum pitch is 0.4 μm. The metal line width and spacing can go down to submicron values. This is called 2.5D IC integration technology [6, 7]. Among all the packaging technologies discussed in this book, this is the most expensive. However, this technology can be applied to very fine pitches, very high density, very high I/Os, very large chips, and for very high performance applications.

(b) **Heterogeneous Integrations on Silicon Substrates (Bridges)**

The fabrication process of RDLs for heterogeneous integration on silicon substrates (bridges) depends on the metal line width and spacing. If the line width and spacing are ≥2 μm, then polymer and ECD (electrochemical deposition) + etching are adequate. On the other hand, if the line width and spacing are <2 μm, then PECVD and Cu-damascene + CMP are needed. The objective of the heterogeneous integrations on silicon substrates (bridges) is to eliminate the TSV-interposer. The metal line width and spacing of the RDLs can be very small.

(c) **Heterogeneous Integration on RDL Fan-Out (Chip-First) Substrates**

The fabrication process of RDLs for heterogeneous integration on fan-out (chip-first) substrates is by polymer and ECD + etching on a reconstituted wafer with embedded chips in the EMC (epoxy molding compound). These RDLs will replace (eliminate) the μbumps, chip-to-wafer bonding, cleaning, underfill dispensing and curing, and the TSV-interposer. However, the metal line width and spacing cannot go down to <2 μm and definitely not to a submicron value.

(d) **Heterogeneous Integration on RDL Fan-Out (Chip-Last) Substrates**

The fabrication process of RDLs for heterogeneous integration on fan-out (chip-last or RDL-first) substrates is by polymer and ECD + etching on a temporary bare glass (wafer or panel) carrier. Those steps are followed by wafer bumping, fluxing, chip-to-wafer or chip-to-panel bonding, cleaning, underfilling, EMC compression molding, etc. These RDLs will replace (eliminate) the TSV-interposer. However, the metal line width and spacing cannot go down to <2 μm. The advantages of fan-out chip-last over fan-out chip-first are: (a) there is not a die shift problem, and therefore a higher packaging assembly yield can be obtained, and (b) one does not have to throw out the known good dies (KGDs). The disadvantages are: (a) higher cost, and (b) more process steps, which lead to more chances to have packaging assembly yield loss.

11.2.3 Applications of Various Heterogeneous Integrations

How to select different heterogeneous integrations? It depends on applications. The most important indicator (selection criterion) is the metal line width and spacing of

the RDLs of the heterogeneous integrations. For example, semiconductors driven by AI for HPC applications, the metal line width and spacing of the RDLs of the heterogeneous integrations must be ultra-fine (<2 μm or down to submicron). In this case, silicon substrate such as the TSV-interposer is needed. The silicon substrate with a bridge made by PECVD and Cu-damascene + CMP can also do the job.

On the other hand, semiconductors driven by 5G for mobile applications, the metal line width and spacing of the RDLs of the heterogeneous integrations are in the 10 μm range. In this case, a build-up organic substrate for connecting the RF-chip and the modem-chip is adequate, but on fan-out substrate is even better.

11.2.4 Application Ranges of Various Heterogeneous Integrations

Figure 11.1 shows the application ranges (size and pin-count) of heterogeneous integrations on various substrates. It can be seen that: (1) the heterogeneous integrations on silicon substrates (TSV-interposers) can have the largest number of pin-counts (>100,000) but the largest substrate size is = 1200 mm^2, (2) the heterogeneous integrations on silicon substrates (bridges) can have the number of pin-count of 4000 and the substrate size ≤ 1200 mm^2, (3) the heterogeneous integrations on fan-out (chip-first) substrates can have the number of pin-count of 2500 and the substrate size ≤ 625 mm^2, (4) the heterogeneous integrations on fan-out (chip-last) substrates can have the number of pin-count of 5000 and the substrate size ≤ 1400 mm^2, and (5) the heterogeneous integrations on organic substrates can have the number of pin-count up to 6000 and the substrate size as large as 3000 mm^2.

11.2.5 Summary and Recommendations

Some important results and recommendations are summarized as follows.

- RDLs are the most integral part of heterogeneous integrations.
- The selection of various heterogeneous integrations depends on the applications. The most important selection criterion is the metal line width and spacing of the RDLs.
- 75% of the heterogeneous integrations will be on organic substrates. (Actually most are SiPs). 25% of the heterogeneous integration will be on other substrates such as silicon (TSV-interposers), silicon (bridges), fan-out RDLs, and ceramic.
- In order to promote/popular the heterogeneous integrations, standards are necessary! The Defense Advanced Research Projects Agency (DARPA) program called

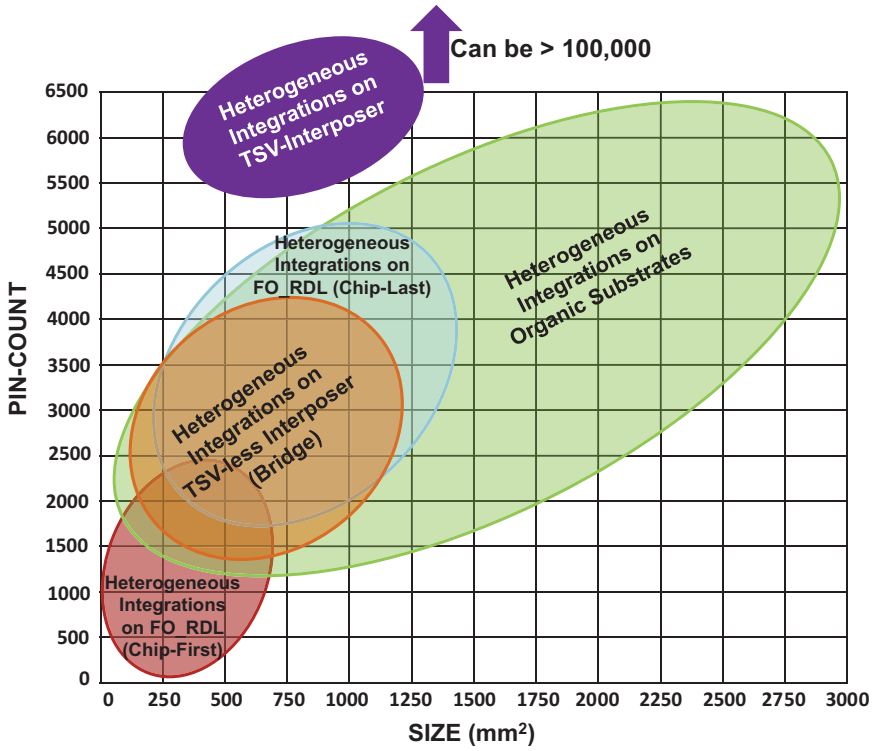


Fig. 11.1 Substrate size and pin-count for RDLs of heterogeneous integrations on organic substrates, silicon substrate (TSV-interposer), silicon substrate (bridges), fan-out RDL substrate (chip-first), and fan-out RDL substrate (chip-last)

Common Heterogeneous Integration and Intellectual Property Reuse Strategies (CHIPS) is heading into the right direction.

- EDA (electronic design automation) tools for automating system partitioning and design are desperately needed for complex heterogeneous integration systems. For example, by using an EDA tool, UCSB and AMD [8] proposed a future very high-performance system shown in Fig. 11.2. This system comprises a central processor unit (CPU) chiplet and several GPU (graph processor unit) chiplets, as well as HBMs (high bandwidth memories) on a passive TSV-interposer and/or on an active TSV-interposer with RDLs.

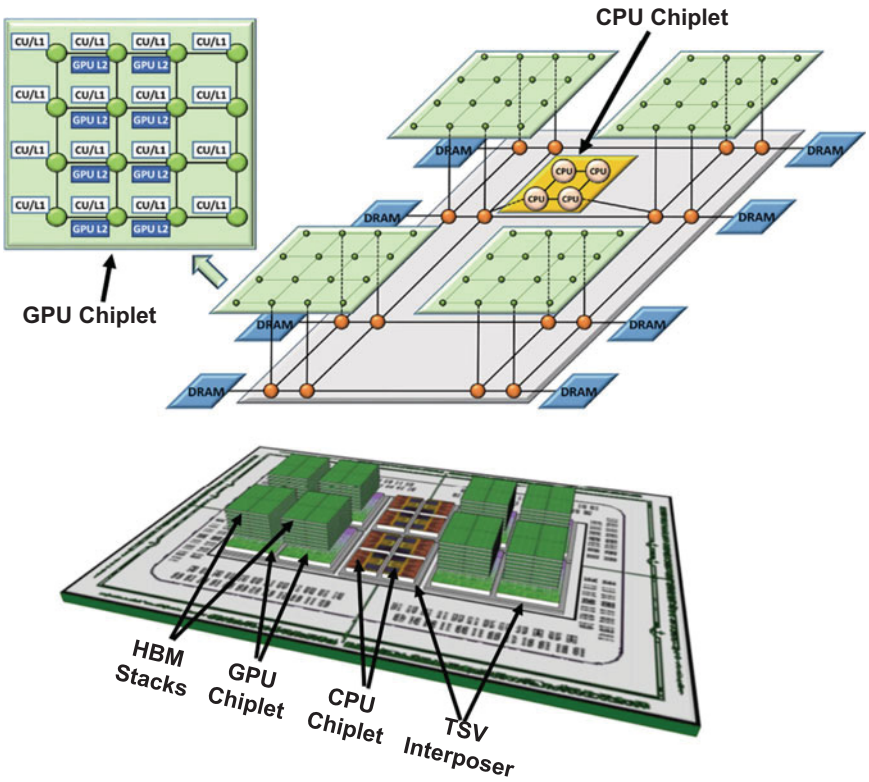


Fig. 11.2 UCSB/AMD GPU chiplets, CPU chiplet, and HBMs on TSV-interposers

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