

2.5D System Integration: A Design Driven System Implementation Schema

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Abstract - This paper investigates a 3D die-stacking based VLSI integration strategy, so-called 2.5D integration, which can potentially overcome many problems stumbling the development of monolithic System-on-Chip (SoC). In this paper, we review available fabrication technologies and testing solutions for the new integration strategy. We also propose a design driven system implementation schema for this new integration strategy. A layout synthesis framework is under development by us to analyze typical "what if" questions and resolve major physical attributes for a 2.5D system according to the design specification and constraints.

Categories and Subject Descriptors

B.7 [Integrated Circuits]: B.7.1 Types and Design Styles -VLSI

General Terms

Performance, Design

Keywords

2.5D System Integration, 3D stacking, 3D-IC

1 Introduction

Functionality increase has been and will continue to be the major driving force for the semiconductor industry. As a matter of fact, the spectacular success of IC industry in the past 30 years depends on the ability to continuously shrink the feature size of IC fabrication process and at the same time pack more devices on a single silicon die. However, when the mainstream fabrication technology are now moving to the 130nm and 90nm nodes, the feasibility of the monolithic integration paradigm is severely stumbled by the following factors:

- Historically, functionality to be integrated in a single chip at every technology generation always exceeds the capacity provided by pure scaling. To accommodate the extra transistors, chip size has always been increasing since the invention of the first integrated circuit [1]. The problem is, interconnection length, especially worst-case interconnection length, has to increase as long as IC chip size is expanding. Starting from the 0.25 μ m generation, the interconnection delay of long on-chip wires has become the dominant part determining system performance [2]. Unfortunately, interconnection delay is very hard to predict before the circuit is actually laid out. Thus current synthesis-based VLSI design methodology often has difficulty to achieve timing closure. The inability

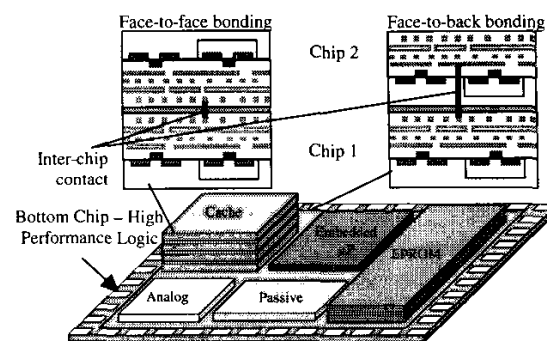


Fig. 1. Potential 2.5D system

to predict physical parameters in advance typically leads to excessive number of design iterations between logic and physical design.

- Memory bandwidth has already become the limiting factor impeding the performance of general-purpose microprocessors and multimedia as well as other data-intensive applications. It has been reported that the processor performance has been improving by 35% annually from 1980 to 1986 and by 55% annually thereafter [3]. In the same period, the access latency of DRAM has been improving by only 7% per year [3]. The traditional solution to this problem is to introduce a multi-level cache hierarchy and integrate memories with the logic on the same chip. For most current processors, at least 50% of the die area is occupied by cache. Besides SRAM cache, a PDA-type phone could use as much as 128Mb flash and 128Mb DRAM [4]. Large volume of embedded memory calls for a merged memory/logic process, which is more expensive and often cannot guarantee satisfactory performance/cost for both logic and memory at the same time. Moreover, interconnect lengths of memory buses and decoders can also become intractable when more embedded memories are monolithically integrated.

- Modern SoCs, especially those designed for wireless applications, typically integrates heterogeneous components like microprocessor, analog/RF circuit, high performance/lower power logic, and so on. These components are originally targeted for different fabrication processes with very diverse configurations and manufacturing steps. This further complicates the merged process and raises fabrication cost. For example, in a

RF-CMOS process, the price of a finished wafer is higher than that of pure CMOS by at least 15% [6]. Meanwhile, for RF circuits, it is difficult to achieve further performance improvement and cost reduction by using a scaled technology. For instance, some analog transistors and passive components have to occupy a rather constant die area to meet performance requirements no matter at which technology node they are fabricated [6].

The above problems are inherent in the monolithic scheme and can hardly be overcome within this 2D regime. In this paper we consider a 3D chip-stacking integration scheme, so-called 2.5D integration strategy [7], to address the above problems. To implement a system (given e.g. in the form of a system-level or RTL description) using the 2.5D system integration schema, one partitions the system into a number of clusters, each containing components that are going to be fabricated in a specific optimum technology. Logic synthesis and layout design for every cluster of components are performed such that each of them can be fabricated as an unpackaged die, optimized for performance and/or cost. Finally these chips can be stacked together in the manner, for instance, illustrated in Figure 1. In this particular implementation the inter-die communication and power distribution might be accomplished through “vertical” interconnects between stacked dies. We refer to the vertical interconnect as “inter-chip contact”.

Intuitively, many benefits can be expected through the adoption of 2.5D integration scheme:

- **Smaller System Footprint** By removing intermediate packaging levels, the 2.5D integrated system allows a system to be constructed with a much smaller volume and weight. This advantage has a significant implication on the portable appliances, which are extremely sensitive to volume/weight. Meanwhile, Smaller chip area also implies higher fabrication yield.
- **Reduced Interconnection Length** Generally speaking, VLSI circuits are not planar and so packing them into a monolithic surface will lead to overhead in the interconnection length. On the other hand, 2.5D/3D integration enables designers or CAD tools to find more efficient packing of circuits according to their inherent topology. This way a systematic reduction in the on-chip wirelength can be expected, which can be translated into speed gain and power saving.
- **Decoupling between functionality increase and technology selection** With the 2.5D integration scheme, chips in a system can be separately designed and fabricated. This way it is possible for every component to be manufactured in a process optimized for performance and/or cost.
- **New reuse opportunity** The 2.5D integration scheme enables reusing verified components at die level. IP cores can be delivered as pre-fabricated, fully characterized, dies with standard interfaces. As a result, systems for different

applications can be realized as different combinations of standard IP dies. This new paradigm of mask reuse promises that VLSI systems be designed and implemented in significantly reduced time with significantly reduced system cost.

Of course, the new integration strategy also has its own limitations. One problem is the extra yield loss introduced by the final assembling process to stack dies together may. An incremental testing and assembling methodology can partially solve this issue. Moreover, it suggests that the 2.5D integration schema will not be a replacement of SoC and the choice between these two schemes should be determined by many factors such as system architecture, performance, yield, and so on. Another important concern for stacked system is the heat dissipation problem. One possible solution is to assign power hungry modules such as communication and clock distribution circuits to the bottom chip, which has the best heat dissipation characteristic. Only low power devices like caches and EPROMs can be stacked with more than 2 levels.

The success of a true 3D stacking scheme depends on the innovations from the three fields: fabrication, testing and design. This paper will review current developments of the first two technology components and then propose a design framework for the new integration schema. The research reported in this paper actually revisits one approach proposed in the past [7] but with a new element: Design Driven System Implementation Schema (DD SIS), which is used to determine system partitioning and components allocations and dictates all major physical attributes of the designed system.

II. Fabrication Technology

Developments of 3D integration technologies can be dated back to as early as 1980s [8, 9]. However, this concept is limited as a research effort largely due to the fact that IC systems were device-limited at that time. Recently, the 3D integration concept is re-gaining popularity as it provides an alternative integration scheme which can potentially overcome the excessive interconnection delay and thus continue the momentum of functionality integration.

Current 3D integration technologies can be classified into two categories: 3D fabrication [9] and 3D stacking [e.g. 7, 10]. In the 3D fabrication approach, each new layer of silicon substrate is grown on the top of a fabricated wafer. The silicon growing technologies include beam recrystallization [11], silicon epitaxial growth [12], and solid phase crystallization [13]. The problem is, however, high temperature processing is inevitable during the formation of circuit structure in upper layers. The high temperature will impair the quality of transistors in bottom level.

Table 1. Candidate technologies for 2.5D Interconnection

Research Group	Stacking Style	Bonding Interface ¹	Inter-chip Contact		
			Alignment Accuracy (μm)	Footprint (μm^2)	Height (μm)
IBM [14, 15]	Face-to-back	Adhesive	N/A	Variable	25–60
Tohoku Univ. [16, 17]	Face-to-face or face-to-back	Adhesive	± 1	3×3	~ 30
NEU [18]	Face-to-face	Adhesive	$\sim \pm 3$	~ 10	< 5
MIT [19]	Face-to-back	Cu-Cu interface	± 3	$3 \sim 5 \times 3 \sim 5$	< 10
RPI/UALbany [20]	Face-to-face or face-to-back	Low-k dielectric glue	$\pm 1 \sim 2$	3×3	~ 30

¹ By bonding interface we indicate the manner in which two chips are attached.

On the other hand, in the 3D stacking approach, a complete VLSI system is an assembly of fabricated, unpackaged dies/wafers [7]. Under such a context [e.g. 7, 14–20], wafers can be built with traditional processes. The upper layer of wafer is first grinded from back to a thickness of less than 10 microns and then bonded with the lower layer of wafer. Finally through-wafer vias are etched from the top. The stacking technology does not involve high-temperature processing. Moreover, it allows wafers built with different processes to be assembled. A problem of this approach is that the wafer thinning process may introduce extra yield loss. In Table 1, we list recent progresses in the 3D stacking technology.

Alignment accuracy determines the lower limit of the size of inter-chip contacts. In the processes listed in Table 1, alignment accuracy is within the range of $\pm 3 \mu\text{m}$. Thus, the footprint of inter-chip contact could be as small as $\sim 10 \text{ mm}^2$. An alternative to the prohibitive alignment technology is to utilize a passive, high-precision self-alignment methodology, e.g. a laterally compliant cantilever with a contact clamp, to facilitate the alignment and engagement of inter-contacts on two adjacent chips. Compliant contacts are desirable for their tolerance to mismatches such as the coefficients of thermal expansion (CTE) of the chips. The alignment process can be organized into multiple stages with increasing accuracies. The refined alignment stage can potentially have very high precision since the alignment features are fabricated in the same process step as the top metallization layer in CMOS technology.

III. Testing Solutions and Fault Tolerance

A stacked system has to be assembled in an incremental manner with a hierarchical and incremental testing methodology so that typical Known Good Dies (KGD) problems could be overcome). Such a methodology actually has been developed when the idea of 2.5D integration was first proposed [7, 24]. Under such a context, each die in the system is isolated with the remaining part of the system by a dedicated boundary-scan chain and can be selectively powered. These features make it possible to separately and incrementally test every die in a fully or partially assembled system.

From the testing perspective, testing an embedded IP core is quite similar to testing a die in a 2.5D system. Consequently, recently developed testing methods for core-based designs [25] provide another set of testing solutions for the 2.5D system:

- Core isolation techniques such as partial boundary

scan chain [26] and test wrapper techniques (e.g. [27]);

- Test data propagation to and from a specific core by set other cores into a transparent mode [28];
- Reuse of system resource like system bus [25] for test purpose;
- Utilization of in-system microprocessor to perform self-testing [29].

The essence of the above techniques is to enable separate access each embedded IP core in a system while trying to reuse existing functionality as much as possible. Accordingly, these testing solutions can be straightforwardly adapted to test 2.5D systems.

Another technique to overcome the difficulty of test access in a 2.5D system is to exploit fault tolerance techniques. For a 3D stacked system, silicon area is not a major concern and thus redundant components can be extensively deployed at different granularity levels to compensate the testing access difficulty introduced by the stacking process. Historically, the fine-grained techniques, such as employing redundant rows or columns of cells in array-styled circuits, have been very successful [30]. On the other hand, coarse-grained techniques (e.g. replicating chip-level functional blocks) have not become popular due to the fact that global failure will impact all modules (including redundant modules) simultaneously [30]. For instance, a short between power and ground in a functional block will lead to the failure of the whole system no matter how many redundant blocks are installed. However, coarse-grained techniques may prove to be very useful in a 2.5D system since different layers can be fully decoupled.

IV. Design Framework for 2.5D System

The 3D stacking and interconnection technologies introduces significant opportunities to realize future electronic systems as well as unprecedented challenges.

Complexity Design of a 2.5D system involves many factors like the huge number of transistors, the number of layers (1, 2, or even more), the choice of process technology (low leakage vs. high performance, standard CMOS vs. embedded DRAM, RF-CMOS vs. SiGe), the heterogeneous use of design technology (digital, analog, optical, MEMS), the necessity for reusing IP components (IP cores/dies, standard buses, memory), and the wide range of communication protocols available for inter-core transactions (buses, on-chip networks, global asynchronous local synchronous).

Manufacturability Even for monolithic VLSI systems, nanometer-scale effects have manifested themselves at almost every design step. Microscopic effects are caused

by device/interconnect parameter variations coupled with transistor leakage and other reliability issues. Macroscopic effects include on-chip temperature variations, voltage drop, and clock skew. All the above factors will be exaggerated in a 2.5D integrated system. In addition, though a 2.5D system can exploit an optimum combination of technologies, the stacking procedure may introduce extra yield loss and suggests complicated yield tradeoffs.

Heat Dissipation Excessive power consumption and resultant heat generation have been major concerns for today's SoC design team. Heat generation on a VLSI chip come from two sources: cell power consumption located inside the substrate, and self-heating effects of interconnections above the substrate. Both heat sources are strongly dependent on the current density and physical parameters of the layout structure and the underlying field oxide thickness. In a 3D stacked VLSI system, heat generation will be a even more serious concern because upper layers of chip may not have good access to heat sinks.

In the following, we introduce our design framework for 2.5D system as a first step to address the above issues. The framework consists of both 2.5D layout synthesis tools and a design exploration engine.

A. Layout Synthesis

We have extended traditional floorplanning, placement and routing algorithms to automatically design 3D stacked VLSI system [23]. These new 2.5D-aware tools could determine the geometric features of a designed system in a stacked space and determine how to assign inter-chip contacts into design hierarchy.

1. 2.5D Floorplanning

Our 2.5D floorplanner is to place macro blocks in a multi-layered space with each layer corresponding to a chip in the 3D stack. Some blocks may be simultaneously assigned to multiple layers. Our floorplanner is based on a multi-layer Bounded Slice-line Grid (BSG) structure [31]. Each layer of chip is represented by a BSG. Then we use a simulated engine to optimize system area and interconnection length. For the largest three MCNC benchmark circuits, total wire length results of the 2.5D implementations are around 30% shorter than those of the monolithic implementations. Meanwhile, worst-case wirelengths in the 2.5D floorplans are up to 39% shorter. As the wires handled at the floorplanning level are global ones. Thus they tend to be in the critical path and have a significant impact on the system delay, the reductions imply potential for significant performance improvement. With the flexibility provided by an inter-chip contact, its length is greatly reduced in 2.5D floorplan.

2. 2.5D Placement

The 2.5D placement framework we build can be used for two popular layout styles, pure standard cell layout and mixed macro/standard cell layout. The targeted layout domain is a face-to-face bonded chip stack and it can be readily adapted to handle stacking of more than 2 levels of

chips. Based on a leading-edge standard cell placer [32], we develop new techniques to support multi-level placements and hierarchical assignment of inter-level interconnections. We also enhance our placer with an efficient procedure to handle mixed macro and standard cell layout in the partition based placement framework. We conduct extensive experiments on more than 60 designs, which have very diverse complexity (2K to 200K place-able objects) and functionality (sub-systems of various ASICs and processor). A consistent wire length reduction of around 28% is observed. Meanwhile, worst-case wirelengths are reduced by around 30%.

Besides traditional design objectives, effective and efficient removal of heat produced by the active devices is essential to guarantee that a chip functions correctly. It is better to avoid putting too many active devices in a region where heat dissipation is difficult. Thermal-aware placement capability is of key importance to avoid hot-spot during layout synthesis process or to migrate a layout to achieve desirable heat map.

3. 2.5D Routing

The 2.5D routing problem is an extension of the classical routing problem by allowing terminals placed on more than one levels. Our 2.5D global router is based on [33], which is a tile based one with a maze routing engine enhanced with congestion control. Iterative rip-up and re-route techniques are also applied to improve solution quality. In our experiments, we found that current routing techniques can well handle the 2.5D routing problems.

B. Design Planning and Exploration

The introduction of 2.5D integration scheme further complicates the solution space. Besides traditional design variables, now designers have to take into account crucial factors such as inter-chip contact density, technology selection for each layer, heat dissipation, redundancy level, and so on. All these factors need to be resolved during the design process to achieve optimized performance and/or cost. For instance, density of inter-chip contacts not only has a major effect on inter-chip communication bandwidth but also directly affects yield and cost of the system assembling process. Thus the key is to find a balanced choice to meet the requirements for both the bandwidth and fabrication yield. An ongoing research project in our group is to develop an exploration framework which navigates a solution space including both the 2D and 2.5D solutions. By combining a set of analytical and constructive models, this framework is targeted to answer the "what if" questions during the design process. Fig. 2 illustrates the flow of the design planning process.

The first step of design exploration is technology selection, which is to resolve system configurations including the number of chips/levels to be stacked, fabrication process for each chip, density of inter-chip contacts, etc. Initially, the solution of this step can be generated manually according to design experience. When design analysis results are available, the technology selection step will be automatically revisited to refine the

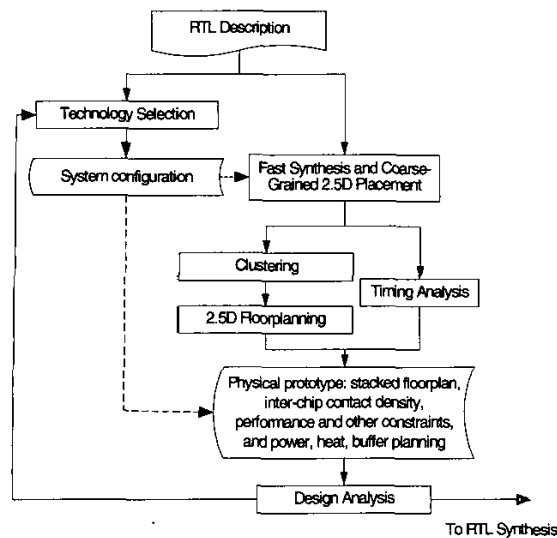


Fig. 2. Design flow for 2.5D system

current system configuration solution.

Given a system configuration, the whole design planning stage is centered on a physical prototype [36], which can be built through a fast synthesis followed by a coarse-grained 2.5D placement. The placement should be performed on a "flattened" netlist, which means all standard cells and macros are handled simultaneously. The placement result must respect the current inter-chip contact density chosen during the technology selection step. To save CPU time, the placement process doesn't need to be completely finished as long as it can provide relatively accurate physical information. Based on the coarse-grained placement, a clustering process taking into account both geometrical closeness and logic hierarchy can be conducted to generate a design hierarchy that is proper for the actual RTL synthesis. The top level blocks in the new hierarchy can then be feed to a 2.5D floorplanning engine. The floorplanning process provides another chance to optimize block positions. This step also performs other design tasks such as pin assignment, buffer insertion and power planning. At the same time, wire load data can also be derived from the placement. The floorplan together with other information that can be directly measured from it constitute a physical prototype for the designed system. Many parameters can then be extracted from the physical prototype. For example, system delay can be computed through a fast event driven simulation or simply a static timing analysis procedure. System power consumption can be estimated by considering gate size, interconnection length and average switching factor [34]. In addition, a cost estimation can be derived according to cost models like the one developed by Nag [35]. The design planning stage need to automatically iterate between technology selection and design analysis steps for several times before such design variables as inter-chip contact density and fabrication processes can be fixed.

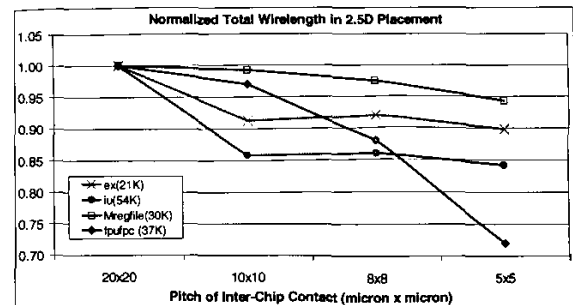


Fig. 3. Normalized wirelength in 2.5D placement vs. pitch of inter-chip contact pitch

Here we'll give a simplified example of analyzing the tradeoff between inter-chip contact pitch and wirelength (which can be a measure of performance). The four benchmark circuits in Fig. 4 are microprocessor subsystems (e.g. integer unit, float point unit and its controller, etc.) of Sun Micro's PicoJAVA and SPARC benchmark suites [21]. The benchmarks are distributed as RTL Verilog code. They are synthesized targeting to a $0.18\mu\text{m}$ CMOS library by Synopsys Design Compiler [37] and then placed by our 2.5D placer [22, 23] into two stacked chips. Fig. 3 shows the normalized wirelengths of the benchmark circuits in their 2.5D implementations (For each circuit, assuming its wirelength is 1 when the pitch of inter-chip contact is $20\times 20\mu\text{m}^2$). Clearly, a general trend shown in Fig. 3 is that the wirelength becomes shorter when the pitch of inter-chip contacts is smaller. On the other hand, different designs have varied sensitivity on the pitch value. For benchmark fpufpc, when pitch size is reduced from $8\times 8\mu\text{m}^2$ to $5\times 5\mu\text{m}^2$, total wirelength can be reduced by $\sim 20\%$. On the other hand, for the remaining three benchmark circuits, it does not gain much to make the pitch smaller than $10\times 10\mu\text{m}^2$. The lesson learned is that major technology parameters of a 2.5D system should be determined according to the system's internal architecture to achieve an optimum configuration.

V. Conclusions and Future Work

Integration of more functionality is continuing to be the major momentum driving the semiconductor industry. However, rapid increasing interconnection length and fabrication cost have become the stumbling blocks for monolithic System-on-Chip. 3D stacked VLSI system, so called 2.5D system, provides an alternative solution to resolve many of the problems inherent to the SoC approach. To enable this new integration strategy, three key technologies are required: fabrication, testing and design. In this paper, we survey the available fabrication technologies and testing solutions for the 2.5D integration strategy. Moreover, this paper proposes a design driven system implementation schema for this new integration strategy. The design framework under development provides a unified background to analyze typical "what if" questions and synthesize final solution.

In the future, we'll further this research in several directions: 1) 2.5D integration design advisor which provides fast estimation on manufacturability, performance, temperature profile, etc.; 2) 2.5D placement tools with routability improvement and hot-spot removal capabilities; 3) efficient 3D integrated microprocessor/DRAM architectures; 4) memory partitioning problem under 3D integration context.

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