

Design and Direct Assembly of 2.5D/3D Rigid Silicon Interposer on PCB

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Abstract

Silicon interposer is emerging as a vehicle for integrating dies with sub 50um bump pitch in 2.5D/3D configuration. Benefits of 2.5D/3D integration are well explained in the literature, however, cost and reliability is a major concern especially with the increase in interposer size. Among the challenges, reliability issues such as warpage, cracks and thermal-stresses must be managed, in addition, multi-layer build-up flip chip substrate cost and its impact on the overall yield must be considered. Because of these challenges, 2.5D/3D silicon interposer has developed a reputation as a costly process.

To overcome the reliability challenges and cost associated with typical thin interposer manufacturing and assembly, a rigid silicon interposer type structure is disclosed. In this study, interposer with thickness of greater than 300um is referred to as rigid interposer. Rigid silicon interposer is directly assembled on PCB without the need for intermediary substrate. This eliminates the need for an intermediary substrate, thin wafer handling, wafer bonding/debonding procedures and Through Silicon Via (TSV) reveal processes, thus, substantially reducing the cost of 2.5D/3D integrated products while improving reliability.

A 10X10mm² rigid silicon interposer test vehicle with 310um thickness was designed and fabricated. BGA side of the interposer with 1mm ball pitch was bumped with eutectic solder balls through a reflow process. Interposer was then assembled on a 50X50mm² FR-4 PCB. We present design and direct assembly of the rigid silicon interposer on PCB followed by temperature cycle results using CSAM images at 250, 500, 750 and 1000 cycles. It is shown that all samples successfully passed the temperature cycle stress test.

Key words

2.5D/3D, Assembly, Cost, Design, Flip Chip, Integration, Package, Reliability, Silicon Interposer, Substrate, Thermal Stress, TSV, Warpage, Yield.

I. Introduction

Known as 2.5D integration, Silicon interposers are becoming a critical component of 2.5D/3D homogeneous or heterogeneous structures. As 2.5D/3D silicon interposer type approach gains momentum, reliability and cost are becoming a major concern. Choice of integration technology used to interconnect dies has profound impact on performance, reliability, yield and finally total cost [1], [2]. Among the challenges, wafer warpage is one of the key parameters that impacts the overall yield and success of 2.5D integration. There are two types of warpages that must be mitigated, first, wafer level warpage and second, interposer die level warpage. Wafer warpage impacts the yield during processing and production, whereas, interposer

die warpage impacts the yield during packaging and assembly [3].

Much studies have been done to investigate and mitigate the impact of wafer warpage. Most recently, Detalle, *et al.* [4] proposed an analytical model for predicting the wafer warpage, the model is used to provide guidelines and recommendations to mitigate the warpage. In high performance applications and in a typical setting with 10:100 aspect ratios (10um TSV diameter and 100um interposer thickness) and thick BEOL leads to warpage at both wafer level and die level.

In 2.5D/3D approach, interposers with 10:100 aspect ratio are assembled on a multi-layer build-up organic substrate followed by board level assembly. In this communication a

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novel rigid silicon interposer substrate is introduced. In this study, interposers with thickness of greater than 300um are referred to as rigid interposer. Aside from being reliable, rigid interposer introduced in this study eliminates the need for thin wafer handling and via-reveal process. In addition, it eliminates the need for multi-layer organic build-up substrate; furthermore, it eliminates or reduces the warpage at both wafer processing level as well as individual die level, thus, substantially reducing the cost [5], [6].

Aside from cost and performance enhancement challenges, 2.5D/3D Path-Finding and design methodology has emerged as an area of expertise due to ultra-dense connectivity among the devices with direct impact on total product cost. Numerous studies [7], [8], [9] have proposed and demonstrated path-finding and co-design optimization methodology for integrating 2.5D/3D devices in the context of multiple PCBs. Such methodology leads to an optimized interconnect which results in lower cost and higher performance products.

II. Cost Impact

Among the cost culprit in manufacturing silicon interposer, 40% is attributed to wafer thinning and backside via-reveal according to Beyne [10]. Other studies [11] investigating a 31X31mm², 100um thick silicon interposer with 12um TSV, 3 copper damascene layers with 65nm design rule for routing on top layer breaks out the manufacturing cost as shown in Table-I.

Table-I: Manufacturing Cost of 100um thick interposer.

Processes	Cost Contribution (%)
Via Etching	13
Via Filling	19
TSV Layers	6
RDL	18
Bonding / Debonding	20
Thinning / TSV reveal	19
Bumping	5

The rigid interposer disclosed in this communication aims at eliminating the time and costs associated with the bonding/debonding steps as well as wafer thinning and TSV reveal processes resulting in a lower cost interposer. Furthermore, eliminating the intermediary substrate that normally sits between the interposer and PCB should result in a cost effective 2.5D/3D integrated product.

The other contributor to the total cost is the yield. In general, the proposed rigid interposer can provide larger size substrate with higher yield by minimizing warpage at the wafer level as well as during the assembly process.

III. TSV Structure

The TSV structure used in this study consists of a front-side via and a back-side via. TSVs were realized on low resistivity silicon with 310um thickness. TSVs were designed to have back-side diameter of 200um and front-side diameter of 18um. TSVs were fabricated with SiO₂ insulation layer of 1um (+/-0.5um) and inner wall copper metallization of ~10-15um thickness [6], [12].

IV. Methodology

Two different 10X10mm² test vehicle structures were designed and fabricated on 200mm wafer. First structure was designed with 50um pitch solder mask defined bump pads on the die side and 1mm pitch solder mask defined landing pads on the BGA side with a fully populated regular BGA pattern. Second structure was designed for signal integrity characterization purposes and had some of the BGA balls removed randomly in an irregular uneven pattern. Routing was achieved on one RDL on both sides of the wafer with ~5-10um front-side and ~15-20um back-side copper metallization thicknesses.

After manufacturing, wafers were diced and individual interposers were placed in a Gel-Box (Fig. 1). BGA side of the interposers were bumped with eutectic solder balls through a reflow process. Bumped interposers were then assembled on a 50X50mm², 2-layer FR-4 board through a reflow process. Series of x-ray images were taken to visually inspect and detect any solder joint anomalies.

Assembled units were then prepared for under-fill process. Before applying under-fill, an ultrasonic cleaning procedure was performed. The units were then baked at 150C for 1 hour followed by a plasma clean procedure. Standard flip chip under-fill (8439-1) was applied and then the units were cured at 150C for 90 minutes (Fig. 2).

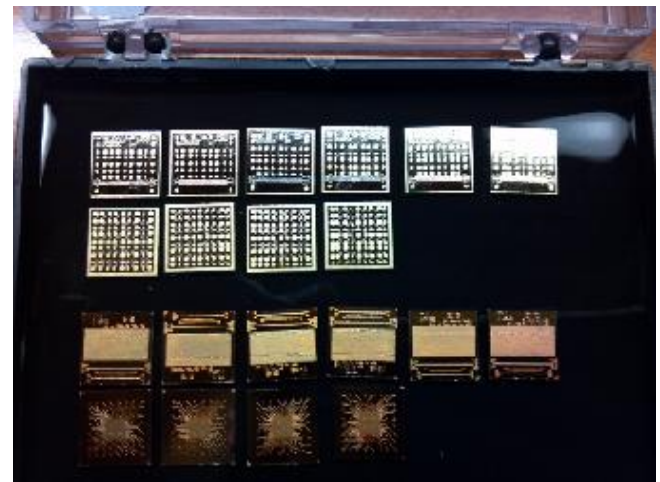


Figure 1: Diced silicon interposers

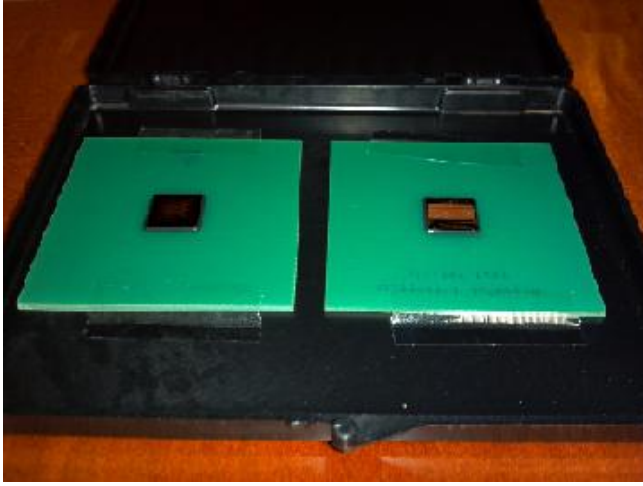


Figure 2: Fully assembled rigid silicon interposer on PBC with under-fill applied.

Samples were then put through JEDEC specified temperature cycle stress test as outlined in Table-II. CSAM images were taken and analyzed at 250 (Fig. 3), 500 (Fig. 4), 750 (Fig. 5) and 1000 cycles (Fig. 6). No anomalies were observed during temperature cycle CSAM inspection. All samples successfully passed the temp cycle stress test post 1000 cycles.

Table-II: Temperature cycle standard and specifications.

Standards-conditions	Specifications
JEDEC Spec	JESD22-A104
Condition B	Temperature -55C to 125C
Temperature Cycle	2 times / hour
Duration	1000 Cycles
CSAM Inspections at	250, 500, 750 and 1000 cycles

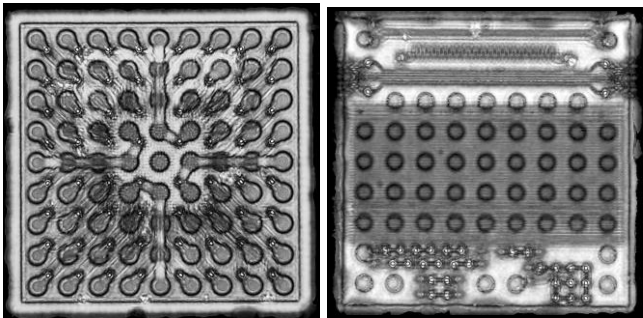


Figure 3: Scanning Acoustic Microscopy post 250 cycles

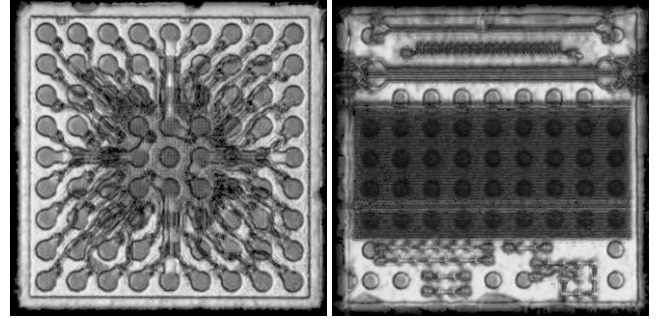


Figure 4: Scanning Acoustic Microscopy post 500 cycles

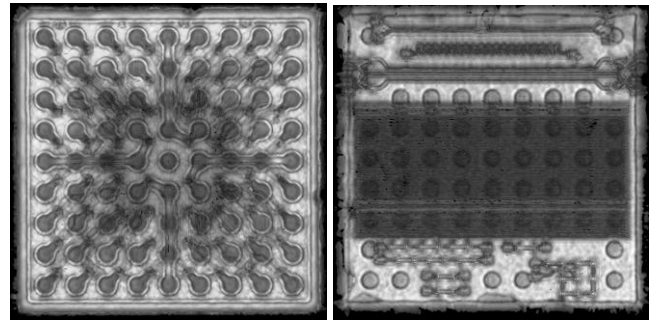


Figure 5: Scanning Acoustic Microscopy post 750 cycles

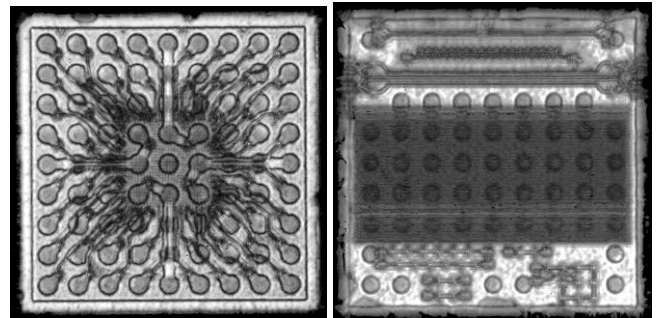


Figure 6: Scanning Acoustic Microscopy post 1000 cycles

IV. Conclusion

To mitigate the cost and common reliability challenges such as warpage that are encountered in thin silicon interposer manufacturing and assembly processes, a novel low cost, reliable and production worthy rigid silicon interposer was introduced. It was shown that the rigid silicon interposer can be directly assembled on PCB eliminating the need for organic build-up substrate. Various samples illustrating both even and uneven BGA ball patterns were manufactured and were directly assembled on PCBs.

Samples were put through standard JEDEC temperature cycle stress test, CSAM images were taken at 250, 500, 750 and 1000 cycles. No anomalies were observed during temperature cycle CSAM inspection. All samples successfully passed the temp cycle stress test post 1000 cycles.

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