**UNITED STATES INTERNATIONAL TRADE COMMISSION**
**WASHINGTON, D.C.**

**Before The Honorable Monica Bhattacharyya**
**Administrative Law Judge**

| | |
|---|---|
| In the Matter of<br>CERTAIN INTEGRATED CIRCUITS, ELECTRONIC DEVICES CONTAINING THE SAME, AND COMPONENTS THEREOF | Investigation No. 337-TA-1450 |

# AMENDED JOINT PROPOSED CLAIM CONSTRUCTION CHART

Pursuant to the Procedural Schedule (Order No. 7), Complainant Onesta IP, LLC ("Onesta" or "Complainant"), Respondents NVIDIA Corporation ("NVIDIA"), Qualcomm Incorporated ("Qualcomm"), OnePlus Technology (Shenzhen) Co., Ltd. ("OnePlus"), and Nothing Technology Limited ("Nothing Tech" or "NTL") (collectively, "Respondents"), and the Commission Investigative Staff ("Staff") respectfully submit the following Amended Joint Proposed Claim Construction Chart.

Table 1 identifies the terms and the corresponding constructions agreed upon by the parties. Table 2 identifies the disputed term the parties will brief for the *Markman* hearing. Table 3 identifies the disputed terms the parties have agreed not to brief for the *Markman* hearing. In the Tables, U.S. Patent No. 9,519,943 is referred to as the "'943 Patent"; U.S. Patent No. 7,717,350 is referred to as the "'350 Patent"; U.S. Patent No. 11,741,019 is referred to as the "'019 Patent"; U.S. Patent No. 11,841,803 is referred to as the "'803 Patent"; and U.S. Patent No. 9,116,809 is referred to as the "'809 Patent."

Pursuant to G.R. 6.1, all parties have agreed on the constructions for the terms listed in Table 1 and that the disputed term listed in Table 2 is amenable for resolution in the *Markman* hearing process.



NVIDIA 1043

**TABLE 1: AGREED-UPON CONSTRUCTIONS[1]**

| Claim Term | Agreed-Upon Construction |
|---|---|
| "chiplet"<br>'803 Patent, Claims 1-3, 7-10 | "a device that includes the following characteristics: 1) a chiplet includes an active silicon die containing part of the computational logic used to solve a full problem (i.e., the computational workload is distributed across multiples of these active silicon dies); 2) chiplets are packaged together as a monolithic unit on the same substrate; and 3) the programming model preserves the concept that these separate computational dies are a single monolithic unit (*i.e.*, each chiplet is not exposed as a separate device to an application that uses the chiplets for processing computational workloads)" |
| "a shared memory address (SMA) in [a/the] shared memory [address space]"<br>'809 Patent, Claims 1-11, 13, 14, 16, 20, 22-25 | "a single unique virtual address in [a/the] shared virtual address space" |
| "an address in [a/the] shared memory"<br>'019 Patent, Claims 1-20 | "an address in [a/the] shared virtual address space" |
| "a shared memory address"<br>'019 Patent, Claims 4 and 14 | "a single unique virtual address" |
| "memory heap[s]"<br>'809 Patent, Claims 1-8, 12-14, 16, 20, 22, 25 | "virtual memory pool[s]" |
| "mapping result"<br>'809 Patent, Claims 1-11, 20, 22-25;<br>'019 Patent, Claims 1-20 | '809 Patent: result of mapping the memory operation to a memory heap<br>'019 Patent: result of mapping the memory operation to a virtual memory pool |

[1] The parties had originally identified agreed-upon terms from claims 5-8 and 19-20 of U.S. Patent No. 8,854,381 (the "'381 Patent"). Those claims, however, have been terminated from this Investigation, pending Commission Review. *See* Order No. 11 (Sept. 25, 2025). In view of that Order, the parties have not included herein any terms from any terminated claim, including claims 5-8 and 19-20 of the '381 Patent.

| Claim Term | Agreed-Upon Construction |
|---|---|
| "a memory operation"[2]<br>'809 Patent, Claims 1-14, 16-20, 22-25;<br>'019 Patent, Claims 1-20 | a command or instruction to access memory, *e.g.,* to load, store, read, write, or copy to or from memory |
| "virtual device(s)"<br>'943 Patent, Claims 1-24 | "virtual devices": software-based processes running on the CPU that appear to the CPU to be GPUs, each of which is used for a different priority of command;<br>"virtual device": one of the "virtual devices." |

[2] The parties and Staff agree that memory allocation is not the claimed "memory operation."

**TABLE 2: DISPUTED CONSTRUCTIONS REQUIRING BRIEFING[3]**

| No. | Claim Term | Exemplary Claim(s) | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|---|
| 1 | "dedicated for inter-chiplet communication" | '803 Patent, Claims 1-3, 7-10 | configured to provide communication only between GPU chiplets | used for transmission of only chiplet-to-chiplet signals | used for transmission of only chiplet-to-chiplet signals | N/A |
| | "a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communication" | | "a passive crosslink": a non-active connecting structure<br>*See also* "dedicated for inter-chiplet communication." | a non-active semiconductor die, which die does not include any through silicon vias and which die is used for transmission of only chiplet-to-chiplet signals | a passive crosslink, wherein the passive crosslink is used for transmission of only chiplet-to-chiplet signals | |

[3] The parties had originally identified terms in dispute requiring briefing from claims 5-8 and 19-20 of the '381 Patent. Those claims, however, have been terminated from this Investigation, pending Commission Review. *See* Order No. 11 (Sept. 25, 2025). In view of that Order, the parties have not included herein any terms from any terminated claim, including claims 5-8 and 19-20 of the '381 Patent.

**TABLE 3: OTHER DISPUTED CONSTRUCTIONS[4]**

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| "the first command"/"the received commands"/"the commands" | '943 Patent, Claims 1, 2, 4-7, 10, 11, 14, 16, 19, 22 | Plain and ordinary meaning | Plain and ordinary meaning | "the same command referenced earlier in the claim received by the virtual device in the CPU" [claims 1-10]<br>"the same command referenced earlier in the claim received from the CPU" [claims 11-24] | "the same command referenced earlier in the claim received by the virtual device in the CPU" [claims 1-10]<br>"the same command referenced earlier in the claim received from the CPU" [claims 11-24] |
| "A processing device, comprising:" | '943 Patent, Claim 11 | Not indefinite; plain and ordinary meaning | Limiting preamble language | Limiting preamble language | Limiting preamble language |

[4] The parties had originally identified terms in dispute from claim 13 of the '350 Patent, claims 15 and 21 of the '809 Patent, claims 10 and 13 of the '943 Patent, and claims 5-8 and 19-20 of the '381 Patent (and claims 1 and 15 from which they depend). Those claims, however, have been terminated from this Investigation, pending Commission Review. *See* Order No. 9 (Sept. 3, 2025); Order No. 11 (Sept. 25, 2025). In view of that Order, the parties have not included herein any terms from any terminated claim, including claim 13 of the '350 Patent, claims 15 and 21 of the '809 Patent, claims 10 and 13 of the '943 Patent, or claims 5-8 and 19-20 of the '381 Patent (and claims 1 and 15 from which they depend).

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| "the processing device is configured to executed the received commands" | '943 Patent, Claim 11 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "preempt execution of the processing device" | '943 Patent, Claim 16 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "wherein the processing device is configured to store a head pointer and a tail pointer respective to each queue of the set of queues in a memory." | '943 Patent, Claim 18 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "a command processor configured to retrieve the received commands from the set of queues," | '943 Patent, Claim 19 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "A method of allocating memory | '809 Patent, Claims 1-11 | Preamble language is not limiting; | Limiting preamble language | Limiting preamble language | Limiting preamble language |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| to a memory operation executed by a processor in a computer arrangement having a first processor configured for unified operation with a second processor, comprising:" | | plain and ordinary meaning | | | |
| "a processor" | '809 Patent, Claims 1-14, 16-20, 22-25 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "mapping"/"mapped" | '809 Patent, Claims 1-14, 16-20, 22-25 | Plain and ordinary meaning | Plain and ordinary meaning | establish[ing/ed] a correlation between [two values] | establish[ing/ed] a correlation between |
| "mapping the memory operation" | '809 Patent, Claims 1-14, 16-20, 22-25 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | Indefinite | N/A |
| "APD" | '809 Patent, Claims 11, 19, 25 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| "a first type"/"of the first type"/"a second, different type" | '809 Patent, Claims 9, 10, 17, 18, 23, 24 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite |
| "A system including a first processor memory resource and a second processor memory resource, the system being configured for providing memory to a memory operation executed by a processor, comprising" | '809 Patent, Claims 12-19 | Preamble language is not limiting; plain and ordinary meaning | Limiting preamble language | Limiting preamble language | Limiting preamble language |
| "a mapper configured to: receive an address reference from the memory operation, and mapping the memory operation to one of the plurality of memory heaps based on the | '809 Patent, Claim 12 | Not subject to § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | Subject to § 112 ¶ 6 / (f); Indefinite | Indefinite under 35 U.S.C. § 112 ¶ 6<br>Function: "receive an address reference from the memory operation, and mapping the memory operation to one of the plurality of |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| address reference, wherein different attributes are applied to a mapped memory heap depending upon origination of the memory operation" | | | | | memory heaps based on the address reference, wherein different attributes are applied to a mapped memory heap depending upon origination of the memory operation"<br>Structure: no corresponding disclosed structure rendering the term indefinite |
| "the [first/second] processor" | '809 Patent, Claims 14, 16-19 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "A computer-readable medium having instructions stored thereon that, when executed by a computing device including a first processor | '809 Patent, Claim 20, 22-25 | Preamble language is not limiting; plain and ordinary meaning | Limiting preamble language | Limiting preamble language | Limiting preamble language |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| configured for unified operation with a second processor cause the computing device to perform a method comprising:" | | | | | |
| "A method for allocating memory in a computer system having a plurality of processors, the method comprising" | '019 Patent, Claims 1-10 | Preamble language is not limiting; plain and ordinary meaning | Limiting preamble language | Limiting preamble language | Limiting preamble language |
| "a processor" | '019 Patent, Claims 1-20 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "mapping"/"map" | '019 Patent, Claims 1-20 | Plain and ordinary meaning | Plain and ordinary meaning | establish[ing] a correlation between [two values] | establish[ing] a correlation between |
| "map[ping] the received memory operation" | '019 Patent, Claims 1-20 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | Indefinite | N/A |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| "at least one of the plurality of processors" | '019 Patent, Claims 3, 13 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "one processor of the plurality of processors" | '019 Patent, Claims 8, 18 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "all processors of the plurality of processors" | '019 Patent, Claims 9, 19 | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite | Indefinite |
| "a mapper, wherein the mapper is configured to: receive a memory operation from a processor that references an address in the share memory; map the received memory operation to at least one virtual memory pool to produce a mapping result, wherein the at least one virtual | '019 Patent, Claim 11 | Not subject to § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | Subject to § 112 ¶ 6 / (f); Indefinite | Indefinite under 35 U.S.C. § 112 ¶ 6<br>Function: "receive a memory operation from a processor that references an address in the shared memory; map the received memory operation to at least one virtual memory pool to produce a mapping result, wherein the at |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| memory pool is associated with at least one memory resource; and provide the mapping result to the processor" | | | | | least one virtual memory pool is associated with at least one memory resource; and provide the mapping result to the processor"<br>Structure: no corresponding disclosed structure rendering the term indefinite |
| "a specific type of processor" | '019 Patent, Claims 10, 20 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | Indefinite | Indefinite |
| "a power management unit coupled to the first processor and the second processor and selectably configured to cause one of the first processor and the second processor to | '350 Patent, Claims 18, 20, 23-25 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Indefinite under 35 U.S.C.§ 112 ¶ 6<br>Function: "cause one of the first processor and the second processor to execute the instructions"<br>Structure: no corresponding |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| execute the instructions" | | | | | disclosed structure rendering the term indefinite |
| "wherein the power management unit is further selectably configured to cause the first processor to operate in [a] fully operational state while executing the instructions, and to cause the second processor to operate in the fully operational state while executing different instructions corresponding to different application software" | '350 Patent, Claim 18 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Governed by 35 U.S.C. § 112 ¶ 6<br>Function: "cause the first processor to operate in a fully operational state while executing the instructions, and to cause the second processor to operate in the fully operational state while executing different instructions corresponding to different application software"<br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit 90 may be configured to |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | provide the necessary signals to cause the different components to operate in various power states. For example, depending on selected preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit 90 may generate signals such as interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |
| "wherein the power management unit is | '350 Patent, Claim 23 | Not subject to 35 U.S.C. § 112 ¶ 6; | Not subject to 35 U.S.C. § 112 ¶ 6; | N/A | Governed by 35 U.S.C. § 112 ¶ 6 |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| further selectably configured to cause the first processor to operate in a reduced power state while the second processor executes different instructions corresponding to different application software" | | plain and ordinary meaning | plain and ordinary meaning. | | Function: "cause the first processor to operate in a reduced power state while the second processor executes different instructions corresponding to different application software"<br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit 90 may be configured to provide the necessary signals to cause the different components to operate in various power states. For |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | example, depending on selected preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit 90 may generate signals such as interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |
| "wherein the power management unit is further selectably configured to cause the second processor to | '350 Patent, Claim 24 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Governed by 35 U.S.C. § 112 ¶ 6<br>Function: "cause the second processor to operate in a reduced power state while the first |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| operate in a reduced power state while the first processor executes the instructions" | | | | | processor executes the instructions"<br><br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit 90 may be configured to provide the necessary signals to cause the different components to operate in various power states. For example, depending on selected preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | 90 may generate signals such as interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |
| "wherein the power management unit is further selectably configured to cause the first processor to operate in a reduced power state while the second processor executes the instructions" | '350 Patent, Claim 25 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Governed by 35 U.S.C. § 112 ¶ 6<br>Function: "cause the first processor to operate in a reduced power state while the second processor executes the instructions"<br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | 90 may be configured to provide the necessary signals to cause the different components to operate in various power states. For example, depending on selected preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit 90 may generate signals such as interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| "a power management unit configured to cause the first processor and the second processor to operate in the first mode and the second mode" | '350 Patent, Claim 2 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Governed by 35 U.S.C. § 112 ¶ 6<br>Function: "cause the first processor and the second processor to operate in the first mode and the second mode"<br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit 90 may be configured to provide the necessary signals to cause the different components to operate in various power states. For example, depending on selected |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit 90 may generate signals such as interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |
| "wherein the power management unit is further selectably configured to cause the first processor and the second processor to operate in a reduced power state while the third processor and the digital signal | '350 Patent, Claim 22 | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning | Not subject to 35 U.S.C. § 112 ¶ 6; plain and ordinary meaning. | N/A | Governed by 35 U.S.C. § 112 ¶ 6 Function: "cause the first processor and the second processor to operate in a reduced power state while the third processor and the digital signal processing unit |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| processing unit operate in a fully operational state" | | | | | operate in a fully operational state"<br>Structure: 7:20-28 ("During operation in the various modes, in one embodiment, power management unit 90 may be configured to provide the necessary signals to cause the different components to operate in various power states. For example, depending on selected preferences, power management unit 90 may receive signals indicative of a mode change. In response, power management unit 90 may generate signals such as |

| Claim Term | Exemplary Claim(s) In Which Term(s) Appear | Complainant's Proposed Construction | Staff's Proposed Construction | NVIDIA's Proposed Construction | Qualcomm, OnePlus, and Nothing Construction |
|---|---|---|---|---|---|
| | | | | | interrupt signals and/or other encoded signals that may cause a given component to enter a particular power state.") |
| "fully operational state" | '350 Patent, Claims 5-8, 18, 22 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "reduced power state" | '350 Patent, Claims 5, 7-9, 22-25 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |
| "second memory" | '350 Patent, Claim 16 | Not indefinite; plain and ordinary meaning | Not indefinite; plain and ordinary meaning | N/A | Indefinite |

Dated: September 30, 2025

Respectfully submitted,

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**CERTIFICATE OF SERVICE**

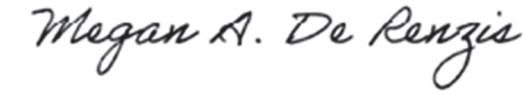
I, Megan De Renzis, hereby certify that on September 30, 2025, true and correct copies of the foregoing was served on the parties as indicated below:

| | |
|---|---|
| The Honorable Lisa R. Barton<br>Secretary to the Commission<br>United States International Trade Commission<br>500 E Street SW, Room 112<br>Washington, DC 20436 | ☒ Via EDIS<br>☐ Via Hand Delivery<br>☐ Via Federal Express (Overnight)<br>☐ Via Electronic Mail |
| The Honorable Monica Bhattacharyya<br>Administrative Law Judge<br>United States International Trade Commission<br>500 E Street SW, Room 317<br>Washington, DC 20436<br>Bhattacharyya337@usitc.gov | ☐ Via Box<br>☐ Via Hand Delivery<br>☐ Via Federal Express (Overnight)<br>☒ Via Electronic Mail |
| Ryan Schmid, Esq<br>Office of Unfair Import Investigations<br>**U.S. International Trade Commission**<br>500 E Street, S.W., Suite 401<br>Washington, D.C. 20436<br>Ryan.Schmid@usitc.gov | ☐ Via Hand Delivery<br>☒ Via Electronic Mail |
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