

Table of Exhibits

Exhibit	Description
1001	U.S. Patent No. 11,841,803 (“’803 patent”)
1002	Declaration of Dr. Vivek Subramanian Regarding U.S. Patent No. 11,841,803 (“Decl.”)
1003	File History for U.S. Patent No. 11,841,803 (“FH”)
1004	U.S. Patent No. 7,598,958 (“Kelleher”)
1005	U.S. Patent No. 11,610,862 (“Collins”)
1006	Coskun et. al, A Cross-Layer Methodology for Design and Optimization of Networks in 2.5D Systems, PROCEEDINGS OF THE INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN (2018) (“Coskun”)
1007	RESERVED
1008	Jerger et al., NoC Architectures for Silicon Interposer Systems, IEEE/ACM INTERNATIONAL SYMPOSIUM ON MICROARCHITECTURE (2015) (“Jerger”)
1009	RESERVED
1010	John Lau, Heterogeneous Integrations, Springer (2019) (“Lau”)
1011	Ajaykumar Kannan, Enabling Interposer-Based Disintegration of Multi-Core Processors, University of Toronto Department of Electrical & Computer Engineering (2015) (“Kannan”)
1012-1013	RESERVED
1014	International Patent Publication No. WO2019132971 (“Elsherbini”)
1015-1019	RESERVED
1020	Dylan Stow, et. al., Cost-Effective Design of Scalable High-Performance Systems Using Active and Passive Interposers, IEEE/ACM INTERNATIONAL CONFERENCE ON COMPUTER-AIDED DESIGN (ICCAD) (2017) (“Stow”)
1021	The Open Domain-Specific Architecture WorkGroup, A Chiplet-Based Open Architecture, Draft v0.9 (2018) (“ODSA”)
1022	Ugljesa Milic et. al., BEYOND THE SOCKET: NUMA-AWARE GPUS, <i>in</i> PROCEEDINGS OF MICRO-50 (2017) (“Milic”)
1023	Complaint, <i>In the Matter of</i> CERTAIN INTEGRATED CIRCUITS, ELECTRONIC DEVICES CONTAINING THE SAME, AND

	COMPONENTS THEREOF, Inv. No. 337-TA-1450 (“ITC-Complaint”)
1024	Complaint, <i>Onesta IP, LLC v. NVIDIA Corp</i> , No. 1:25-cv-00586 (W.D. Tex.) (“District-Court-Complaint”)
1025	ITC Exhibit 50, <i>In the Matter of</i> CERTAIN INTEGRATED CIRCUITS, ELECTRONIC DEVICES CONTAINING THE SAME, AND COMPONENTS THEREOF, Inv. No. 337-TA-1450 (“ITC-Ex50-Infringement”)
1026	ITC Exhibit 19, <i>In the Matter of</i> CERTAIN INTEGRATED CIRCUITS, ELECTRONIC DEVICES CONTAINING THE SAME, AND COMPONENTS THEREOF, Inv. No. 337-TA-1450 (“ITC-Ex19-Domestic-Industry”)
1027	U.S. Patent Publication No. 2019/0123022 (“Teig”)
1028	Paul Enquist, Room Temperature Direct Wafer Bonding for Three Dimensional Integrated Sensors, SENSORS AND MATERIALS, Vol. 17, No. 6 (2005) (“Ziptronix”)
1029	Robert R. Schaller, Moore’s Law: Past, Present, and Future, IEEE SPECTRUM (June 1997) (“Schaller”)
1030	Yangdong (Steven) Deng & Wojciech Maly, 2.5D System Integration: A Design Driven System Implementation Schema, IEEE (2004) (“Deng-&-Maly”)
1031	U.S. Patent No. 10,909,652 (“Koker”)
1032	RESERVED
1033	Akhil Arunkumar et. al, MCM-GPU: Multi-Chip-Module GPUs for Continued Performance Scalability <i>in Proceedings of ISCA ’17</i> (June 2017) (“Arunkumar”)
1034	Dictionary of Computer Science (7th ed.), Oxford University Press (2016) (“Dictionary-of-Computer-Science”)
1035	Dictionary of Multimedia (4th ed.), Franklin, Beedle & Associates Inc. (2005) (“Dictionary-of-Multimedia”)
1036	Joel Mearig & Bill Goers, An Overview of Manufacturing BGA Technology, IEEE/CPMT Int’l Electronics Manufacturing Technology Symposium (1995) (“Mearig-&-Goers”)
1037	U.S. Patent Publication No. 2018/0240778 (“Liu”)
1038	Farhang Yazdani, Design and Direct Assembly of 2.5D/3D Rigid Silicon Interposer on PCB, IMAPS Proceedings (2014) (“Yazdani”)
1039	RESERVED
1040	U.S. Patent Publication No. 2001/0005873 (“Yasuda”)

1041	U.S. Patent No. 10,475,147 (“Price”)
1042	U.S. Patent Publication No. 2007/0273699 (“Sasaki”)
1043	Amended Joint Proposed Claim Construction Chart, <i>In the Matter of</i> CERTAIN INTEGRATED CIRCUITS, ELECTRONIC DEVICES CONTAINING THE SAME, AND COMPONENTS THEREOF, Inv. No. 337-TA-1450 (“Claim-Construction-Chart”)
1044	Chris McClanahan, History and Evolution of GPU Architecture, Georgia Tech. (2010) (“McClanahan”)
1045	Thiruvengadam Vijayaraghavan et.al, Design and Analysis of an APU for Exascale Computing, IEEE International Symposium on High Performance Computer Architecture (2017) (“Vijayaraghavan”)
1046	NVIDIA Tesla P100, Whitepaper, The Most Advanced Datacenter Accelerator Ever Built Featuring Pascal GP100, the World’s Fastest GPU (2016) (“NVIDIA-P100”)
1047	U.S. Patent Publication No. 2009/0037658 (“Sistla”)
1048	Raman Nayyar, “Performance Analysis of a Hierarchical, Cache-Coherent, Shared Memory Based, Multi-processor System” (1993) (“Nayyar”)
1049	Rajeev Balasubramonian et. al, “Multi-Core Cache Hierarchies,” Morgan & Claypool Publishers (2011) (“Balasubramonian”)
1050	Reza Ghaffarian, Book of Knowledge (BOK) for NASA Electronic Packaging Roadmap (2015) (“Ghaffarian”)
1051	Notice of Petitioner’s <i>Sotera</i> Stipulation