

**UNITED STATES INTERNATIONAL TRADE COMMISSION
WASHINGTON, D.C.**

**Before The Honorable Monica Bhattacharyya
Administrative Law Judge**

In the Matter of

**CERTAIN INTEGRATED CIRCUITS,
ELECTRONIC DEVICES CONTAINING
THE SAME, AND COMPONENTS
THEREOF**

Investigation No. 337-TA-1450

**COMPLAINANT ONESTA IP LLC'S PRELIMINARY REBUTTAL
TO NVIDIA'S INVALIDITY CONTENTIONS**

Pursuant to the Procedural Schedule set forth in Order No 7, Complainant Onesta IP, LLC ("Onesta" or "Complainant") submits the following initial disclosures of rebuttals to the Preliminary Invalidity Contentions submitted by Respondent NVIDIA Corporation's ("NVIDIA") on September 5, 2025 ("NVIDIA Invalidity Contentions"), including the cover pleading thereof ("NVIDIA Cover Pleading"), and the exhibits thereto ("NVIDIA Exs."), NVIDIA Exs. 943-A-1 through 943-A-10 and NVIDIA Ex. 943-B; NVIDIA Exs. 803-A-1 through 803-A-12 and NVIDIA Ex. 803-B; NVIDIA Exs. 809-A-1 through 809-A-15 and Ex. 809-B; and Exs. 019-A-1 through 019-A-15 and Ex. 019-B concerning NVIDIA's affirmative defense of invalidity of U.S. Patent No. 9,519,943 ("the '943 Patent"), U.S. Patent No. 11,841,803 ("the '803 Patent"), U.S. Patent No. 11,741,019 ("the '019 Patent"), and U.S. Patent No. 9,116,809 ("the '809 Patent") (collectively, the "NVIDIA Asserted Patents")^{1,2}. Onesta's disclosures herein are hereinafter

¹ The Qualcomm Asserted Patents include all patents asserted against Qualcomm and its customer Respondents in this Investigation.

² Onesta had originally asserted U.S. Patent No. 8,854,381 (the '381 Patent) against NVIDIA. The '381 Patent, however, has been terminated from this Investigation, pending Commission Review. *See* Order No. 11 (Sept. 25, 2025). In view of that Order, Onesta has not included herein any rebuttal contentions related to the '381 Patent.

referred to as Onesta's "Initial Rebuttal Contentions to NVIDIA."³

Onesta's discovery in connection with this Investigation is ongoing. These Initial Rebuttal Contentions to NVIDIA are preliminary and based on information advanced by NVIDIA in its Invalidity Contentions and obtained by Onesta to date. Thus, these Initial Rebuttal Contentions to NVIDIA are subject to further amendment, including identifying, charting, and relying on additional evidence or information about evidence disclosed herein. Further, Onesta reserves the right to revise these Initial Rebuttal Contentions to NVIDIA, including in the event NVIDIA or any other Respondent is permitted to untimely alter and/or expand on the theories disclosed in the NVIDIA Invalidity Contentions during the course of this Investigation. Additionally, Onesta reserves the right to amend these Initial Rebuttal Contentions to NVIDIA in light of construction of the asserted claims adopted by the ALJ and/or positions that Respondents or Respondents' expert witnesses may take concerning claim construction, infringement, domestic industry, invalidity, licensing, or other issues.

I. General Responses and Objections to NVIDIA's Invalidity Contentions

The NVIDIA Invalidity Contentions suffer fatal defects and NVIDIA has not provided Onesta with contentions sufficiently detailed to apprise Onesta of NVIDIA's invalidity theories. *See* NVIDIA Cover Pleading, and NVIDIA Exs. 943-A-1 through 943-A-10 and NVIDIA Ex. 943-B; NVIDIA Exs. 803-A-1 through 803-A-12 and NVIDIA Ex. 803-B; NVIDIA Exs. 809-A-1 through 809-A-15 and Ex. 809-B; and Exs. 019-A-1 through 019-A-15 and Ex. 019-B.

Specifically, the NVIDIA Cover Pleading and the NVIDIA Exhibits are conclusory, unsupported, and lack the necessary mapping of claim elements to disclosures in the prior art such

³ To the extent other Respondents to this Investigation, Qualcomm Incorporated ("Qualcomm"), OnePlus Technology (Shenzhen) Co., Ltd. ("OnePlus"), and Nothing Technology Limited ("Nothing Tech" or "NTL") have attempted to incorporate or adopt the NVIDIA Invalidity Contentions, these Rebuttal Validity Contentions to NVIDIA apply equally to those Respondents and are not limited to NVIDIA.

that one could understand the theories upon which NVIDIA is relying. For example, all of the claim chart appendices provided in the NVIDIA Exhibits fail to match specific claim limitations with disclosures in the alleged prior art. Instead, NVIDIA takes a blunderbuss approach, dumping numerous citations and excerpts from alleged prior art as allegedly disclosing entire claim elements with no explanation or narrative how these excerpts allegedly render the claims anticipated or obvious. Nor does NVIDIA even clearly identify whether it is relying on a reference's disclosures under an anticipation theory (under § 102) or an obviousness theory (under § 103). For example, the NVIDIA Invalidity Contentions assert that "the prior art identified in these contentions anticipates and/or renders obvious all Asserted Claims under 35 U.S.C. § 102 and/or § 103." *See, e.g.,* NVIDIA Cover Pleading at 7. Further, NVIDIA asserts that its identifications are merely "exemplary": "Below and in its attached claim charts, NVIDIA identifies an exemplary list of prior art references and exemplary combinations of prior art references that, at least under Onesta IP's apparent infringement theories, the Asserted Claims obvious." *See, e.g.,* NVIDIA Cover Pleading at 125. Further, the NVIDIA Invalidity Contentions assert that even the "exemplary" combinations, which are excessive and improper are merely "Non-limiting illustrative obviousness combinations," and then proceeds to double the total number of identified combinations by asserting "it should be understood that each listed combination can also include the knowledge of a POSITA." *See, e.g.,* NVIDIA Cover Pleading at 163, 201, 221. The deadline to disclose NVIDIA's invalidity theories was September 5, 2025, but, as of that date, NVIDIA has failed to provide the required clarity. As such, Onesta reserves all rights to seek relief from the ALJ to bar such arguments and evidence from admission into the administrative record. In addition to the above-mentioned shortcomings, Onesta objects to the contentions to the extent that NVIDIA relies on alleged prior art without establishing that the alleged prior art was publicly available in advance of the priority date of the NVIDIA Asserted Patents.

Because of the aforementioned lack of specificity in the NVIDIA Invalidity Contentions with respect to which portions of the references allegedly disclose which portions of the asserted claims, it is impossible for Onesta to put forth tailored arguments as to why each reference lacks disclosure of the inventions claimed by the NVIDIA Asserted Patents. Nor is it possible to put forth tailored arguments as to why each reference lacks a sufficiently enabling disclosure to allow a Person of Ordinary Skill In The Art (“POSITA”) to arrive at the inventions claimed by the NVIDIA Asserted Patents. “A claimed invention cannot be anticipated by a prior art reference if the allegedly anticipatory disclosures cited as prior art are not enabled....a non-enabled disclosure cannot be anticipatory (because it is not truly prior art) if that disclosure fails to ‘enable one of ordinary skill in the art to reduce the disclosed invention to practice.’” *Amgen Inc. v. Hoechst Marion Roussel*, 314 F.3d 1313, 1354 (Fed. Cir. 2003) (citations omitted). Thus, Onesta reserves all rights to address lack of disclosure and lack of enablement in each of the references cited by NVIDIA, should NVIDIA eventually comply with its obligation to provide specific mappings of the prior art to the asserted claim elements.

NVIDIA’s lack of specificity and requisite detail is not limited to the lack of explanation of how the cited references allegedly disclose the claimed inventions. For example, NVIDIA did not identify with the requisite specificity the alleged combinations of references that it intends to rely on at the hearing in this Investigation. Rather than allege specific combinations of references on a limitation-by-limitation basis, NVIDIA merely provided a long but bare list of references for each claim without pointing to any elements (*see e.g.*, NVIDIA Cover Pleading, at 163-171, 201-206, 222-236), inappropriately reserving broad rights to identify more art or utilize art not identified. This approach forces Onesta to sift through the voluminous contentions to identify potential combinations NVIDIA may rely on at a later date. The burden to identify allegedly invalidating combinations of references was with, and always remains with, Respondents. Yet, to

date, NVIDIA has failed in this basic notice requirement. Onesta therefore reserves all rights to bar tardy combination arguments and evidence from admission into the administrative record.

For the references that NVIDIA has identified, NVIDIA has failed to articulate sufficient allegations of motivations to combine these references, and therefore Onesta has not been put on meaningful notice of the arguments and evidence NVIDIA intends to present at the hearing in this Investigation. Rather than articulate specifically how and why a person of skill would combine specific references, NVIDIA provides conclusory assertions that such combinations would have been made because general concepts allegedly disclosed by those references would allegedly be combined. For example, rather than articulate specifically how and why a person of skill would combine the references, NVIDIA asserts that various groups of disparate references would have been combined or some undisclosed subset(s) of those groups of references would have been combined because the references generally relate to graphics processing, inter-chiplet communication, memory operation, or some other technology. These allegations are insufficient, as further explained below. Onesta reserves all rights related to NVIDIA's failure to provide Onesta with meaningful notice of NVIDIA's theories of motivations to combine.

NVIDIA also inappropriately purports to reserve its rights in a number of instances. For example, NVIDIA purports to reserve its rights to revise, amend, and/or supplement its contentions in various improper ways, such as to:

- assert additional references from NVIDIA's further search and analysis;
- change prior art relied upon;
- change the cited portions or rely on uncited portions of prior art references;
- for system art, change its contention for the date "by which the system was known or used, in public use, on sale, and/or invented in the United States";
- rely on other publications;

- for patent references, to interchangeably rely on the issued patent and the application publication;
- assert—for the first time without preserving the rights in its affirmative defense when answering to the Complaint—unenforceability due to alleged inequitable conduct, unclean hands, prosecution laches, ensnarement, and/or reverse doctrine of equivalents, and other unspecified grounds;
- present additional arguments under e.g., 35 U.S.C. §§ 102(f), (g);
- change the use of alleged anticipatory prior art as obviousness prior art;
- identify motivation to combine;
- add written description or enablement arguments;
- add priority date contentions;
- add indefiniteness arguments

See e.g., Invalidity Contentions at Section II, 2-6, 8, 11, 13, 17, 20, 22, 24, 26, 133, and 270. This broad reservation of rights is inappropriate and contrary to the Ground Rules and Procedural Schedule in this Investigation. Indeed, any arguments of invalidity or unpatentability under 35 U.S.C. §§ 101, 102, 103, and/or 112 that NVIDIA failed or elected not to sufficiently allege in its invalidity contentions served on September 5, 2025, are waived, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions.

Onesta's Initial Rebuttal Contentions to NVIDIA are based in whole or in part on Onesta's present understanding of the Asserted Claims, the Parties' proposed claim constructions, and NVIDIA's apparent construction of the NVIDIA Asserted Claims in the NVIDIA Invalidity Contentions. Accordingly, Onesta's Initial Rebuttal Contentions to NVIDIA take into account

alternative and potentially inconsistent positions as to claim construction and scope. By applying any of NVIDIA's apparent or proposed claim constructions herein, Onesta does not concede in any way that those constructions are correct. Rather, Onesta reserves the right to take positions inconsistent with claim construction positions expressed or implied herein. Should a dispute arise at a later date demonstrating that there remains a disagreement regarding the appropriate construction of any claim term that was otherwise not brought to light earlier in the Investigation, Onesta reserves the right to amend these Initial Rebuttal Contentions to NVIDIA in response to any such tardy positions taken by NVIDIA, its officers, directors, employees, agents, experts, or relevant third parties, including named inventors of the NVIDIA Asserted Patents, and corporate or fact witnesses of the alleged prior art, during the course of the Investigation. Nothing contained in these Initial Rebuttal Contentions to NVIDIA should be deemed to be an express or implied admission with respect to the proper construction of the NVIDIA Asserted Claims or with respect to the alleged invalidity or infringement of those claims.

The burden of proof remains at all times with Respondents to prove invalidity through clear and convincing evidence, as patents are presumed valid. This burden never shifts to Onesta. The NVIDIA Invalidity Contentions fail to meet this burden.

II. Person of Ordinary Skill in the Art

Onesta set forth its contentions with respect to the level of skill in the art for each of the Asserted Patents in Third Supplemental Responses And Objections To Respondents' First Set Of Interrogatories To Complainant, served September 5, 2025.

The NVIDIA Invalidity Contentions assert the level of ordinary skill for each of the NVIDIA Asserted Patents

A POSITA for the '943 patent would have had a bachelor's degree in computer science, computer engineering, electrical engineering, or equivalent field, and three to five years of experience with

microprocessor and graphics processor scheduling and execution and/or graphics processor virtualization, or a master's degree or Ph.D. in the same fields, and one to two years of experience with microprocessor and graphics processor scheduling and execution and/or graphics processor virtualization.

NVIDIA Cover Pleading at 6;

A POSITA for the '803 patent would have had a bachelor's degree in computer science, computer engineering, electrical engineering, or equivalent field, and three to five years of experience with semiconductor layout design, or a master's degree or Ph.D. in the same fields, and one to two years of experience with semiconductor layout design.

A POSITA for the '809 and '019 patents would have had a bachelor's degree in computer science, computer engineering, electrical engineering, or equivalent field, and three to five years of experience with memory technology and design, or a master's degree or Ph.D. in the same fields, and one to two years of experience with memory technology and design.

NVIDIA Cover Pleading at 7.

Though the articulations of the level of skill differ slightly between NVIDIA's and Onesta's contentions, as Onesta currently understands NVIDIA's contentions, the differences do not affect the analysis of the Asserted Patents. To the extent that Respondents amend their contentions to provide further articulation of what a POSITA would know/understand or not, Onesta reserves the right to identify the impacts of any differences in the articulations of the level of ordinary skill.

Onesta makes these Initial Rebuttal Validity Contentions to NVIDIA under all proposed definitions for the level of ordinary skill. *See id.*; *see also* Qualcomm Cover Pleading at 14, 41, 62, and 80.

III. Core Concepts Allegedly Known in the Art

The NVIDIA Invalidity Contentions purport to identify "basic concepts, all of which were well known in the prior art." *See* NVIDIA Cover Pleading at 25-121. However, the NVIDIA

Invalidity Contentions fail to demonstrate that the alleged core concepts were known prior to the relevant priority dates of the asserted patents, fail to articulate the relevance of identification of general knowledge in the art, and fail to tie the alleged core concepts to the knowledge or skill of a POSITA.

For example, NVIDIA asserts that “GPUs have been widely available to consumers since the 1990s,” and “GPUs were used to accelerate the execution of instructions that were previously executed by CPUs,” but provides no context related to the asserted claims. NVIDIA Cover Document at 26, 29; *see also id.* at 26-33. For example, none of the asserted patents claim GPUs in and of themselves, or GPUs merely executing any instructions. This approach is improper and fails to meet Respondents’ burden, at least because “Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’” *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)).

NVIDIA also asserts that other concepts were allegedly well known in the art, and provides citations to references that NVIDIA asserts allegedly anticipate or render obvious the asserted claims. *See, e.g.*, NVIDIA Cover Pleading at 64-68 (citing *Doyle*, *Gandhi*, *Gosalia*, *Wyatt*, *Lee*, *Dankin*, and *NVIDIA Tesla* for the proposition that “prioritizing execution of commands on a GPU” was allegedly well known); *see also* NVIDIA Cover Pleading at 68-121. The alleged disclosures of the cited art and the relation they have to the asserted claims are addressed in the appendices attached hereto. *See* Appxs. A-D (addressing the cited references). Moreover, as with the generalized concepts of GPUs existing or performing instructions, NVIDIA’s assertion that individual features were separately known does not satisfy Respondents’ burden, and does not establish that the asserted claims, including the various elements combined in the claimed manner, were anticipated or obvious. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (“A patent composed

of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art.”).

“In making the assessment of differences, section 103 specifically requires consideration of the claimed invention ‘as a whole.’ Inventions typically are new combinations of existing principles or features. The ‘as a whole’ instruction in title 35 prevents evaluation of the invention part by part. Without this important requirement, an obviousness assessment might break an invention into its component parts (A + B + C), then find a prior art reference containing A, another containing B, and another containing C, and on that basis alone declare the invention obvious. This form of hindsight reasoning, using the invention as a roadmap to find its prior art components, would discount the value of combining various existing features or principles in a new way to achieve a new result - often the very definition of invention . . . Section 103 precludes this hindsight discounting of the value of new combinations by requiring assessment of the invention as a whole.” *Ruiz v. A.B. Chance Co.*, 357 F.3d 1270, 1275 (Fed. Cir. 2004).

IV. Anticipation and Obviousness

A. U.S. Patent No. 9,519,943

NVIDIA has failed to meet its burden in setting forth contentions that would support its allegations of anticipation and/or obviousness of the ’943 Patent. NVIDIA asserts 31 devices and systems, patent references, and non-patent literature references in the NVIDIA Cover Pleading (*see e.g.*, pp. 12-19) and NVIDIA Exhibits (*see e.g.*, Exs. 943-A-1 through A-10 and 943-B) as alleged prior art to the ’943 Patent (“ ’943 References”).

First and foremost, the NVIDIA Invalidity Contentions fail to prove that each of the asserted ’943 References qualifies as prior art to the ’943 Patent. The NVIDIA Invalidity Contentions did not identify under which section of law each reference allegedly qualifies as prior art. *See, e.g.*, NVIDIA Cover Pleading at 12-19. Rather, NVIDIA made a blanket citation to “35

U.S.C. §102 and/or § 103. *See, e.g.*, NVIDIA Cover Pleading at 7. It is unclear which specific date NVIDIA asserts is the operative date for each of the '943 References, and under which section of law NVIDIA asserts each of the '943 References qualifies as prior art. For example, the NVIDIA Invalidity Contentions did not identify, *e.g.*, for patent references, whether NVIDIA is relying on the provisional filing date, non-provisional filing date, earliest non-provisional filing date, pre-grant publication date, or patent grant publication date. NVIDIA has also failed to produce multiple references listed in the NVIDIA Invalidity Contentions that are alleged to be prior art (*e.g.*, except for the five alleged Intel documents listed on NVIDIA Ex. 943-A-10 at 1, all other alleged Intel Documents listed in the NVIDIA Cover Pleading at 18 were not produced). The NVIDIA Invalidity Contentions also included numerous errors on the patent numbers, dates, and bates number when listing the references it asserts. *See e.g.*, U.S. "10/763,777" associated with Inventor(s) Gosalia et al., NVIDIA Cover Pleading at 17; "US. Patent Application Publ. No. 2003/0001847 to Gosalia et al.", NVIDIA Ex. 943-A-1 at 1. The NVIDIA Invalidity Contentions fail to satisfy Respondents' burden and have not placed Onesta on notice of any specific allegations based on these references.

Further, the NVIDIA Invalidity Contentions attempt to rely on three alleged systems or devices as prior art in its Invalidity Contentions, including two of NVIDIA's GPU architecture families—Tesla and Fermi, and one Intel "Generation 4 ('GEN4') family of graphics devices." But each of these NVIDIA or Intel product families includes a number of devices released at different dates. By simply citing a code name of a GPU architecture, NVIDIA has failed to meet its burden to show by clear and convincing evidence which specific system or device it alleges as prior art. *E.g.*, "Tesla", *see e.g.*, NVIDIA Cover Pleading at 13-14, 123, 163-171, NVIDIA Ex. 943-A-9; "NVIDIA GeForce 8800 GPU Architecture," *see e.g.*, NVIDIA Ex. 943-A-9; "NVIDIA GeForce GTX 200 GPU Architectural," *see e.g.*, NVIDIA Ex. 943-A-9; "Fermi," *see e.g.*,

NVIDIA Cover Pleading at 15-17, 123, 163-171, NVIDIA Ex. 943-A-3; “Intel GEN4 family of graphics cards” or “Intel Chipset (GEN4)” or “Intel Chipset,” *see e.g.*, NVIDIA Cover Pleading at 13, 123, 163-171, NVIDIA Ex. 943-A-10; “Intel 965 Express Chipset Family,” *see e.g.*, NVIDIA Ex. 943-A-10.

To the extent the NVIDIA Invalidity Contentions rely on any specific product, *e.g.*, NVIDIA GeForce 8800 GTS 640 (*see e.g.*, NVIDIA Cover Pleading at 13), NVIDIA has failed to prove the features relied on from the cited documents were actually implemented in that specific product earlier than the priority date of the ’943 Patent⁴. Nor did NVIDIA show the features or functions cited from the documents were actually implemented in the alleged system or device “known or used by others in this country” or “in public use or on sale in this country, more than one year prior to” the priority date of the ’943 patent. The NVIDIA Invalidity Contentions fail to satisfy Respondents’ burden and have not placed Onesta on notice of any specific allegations based on any system or device.

In addition to failing to prove that the ’943 References qualify as prior art, the NVIDIA Invalidity Contentions fail to prove that the ’943 References anticipate or render obvious the asserted claims of the ’943 Patent. Even considering the teachings of the references, the references and any/all combinations thereof do not invalidate the asserted claims of the ’943 Patent under 35 U.S.C. §§ 102 and/or 103. For example, none of the ’943 References discloses each and every claim element of the asserted ’943 Patent claims. Nor do any of the ’943 references render obvious each and every claim element of the asserted ’943 Patent claims, alone or in combination with any of the other ’943 References. For example, in NVIDIA Ex. 943-B, NVIDIA provides a chart

⁴ The internal technical documents relied on by NVIDIA do not show their disclosure support or being implemented in any specific system or device. In fact, many are not dated and none shows any date of public use, knowledge, or sale.

entitled “Compilation of Disclosures from Additional Prior Art References” excerpting disclosures from nine of the ’943 References (*see e.g.* NVIDIA Ex. 943-B at 1), but these nine references, considered alone or in combination (either in combination with each other or in combination with any other reference), do not render the Asserted Patent Claims anticipated or obvious at least because they do not, under any of the proposed constructions, expressly or inherently disclose all the limitations claimed in the ’943 Patent. The NVIDIA Invalidity Contentions do not provide any explanation or reasoning as to how any asserted references would be combined to arrive at the claimed invention. “Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’” *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). The NVIDIA Invalidity Contentions also fail to prove that the ’943 patent is invalid as obvious because they fail to provide contentions regarding the analysis of the *Graham* factors, such as the differences between the prior art and the claimed invention. *See Graham v. John Deere Co.*, 383 U.S. 1 (1966).

The NVIDIA Invalidity Contentions also fail to prove that any of the ’943 References would be combined with any of the other references, for example by failing to prove that a POSITA would have been motivated to combine the references to arrive at the claimed invention. “[T]here must exist a motivation to combine various prior art references in order for a skilled artisan to make the claimed invention.” *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024). “Obviousness is an issue of law decided based on numerous factual findings, including the scope and content of the prior art, the level of ordinary skill, and whether a relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 956 (Fed. Cir. 2023). “The ultimate conclusion of obviousness is a legal determination based on underlying factual findings,

including whether or not a relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Volvo Penta of the Americas v. Brunswick Corp.*, 81 F.4th 1202, 1209 (Fed. Cir. 2023); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (there must be “a reason” for a skilled artisan “to combine the elements in the way the claimed new invention does”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”).

Although NVIDIA purports to present “exemplary” motivations to combine in Section VI B.2 of the NVIDIA Cover Pleading, NVIDIA’s Invalidity Contentions extract in a piecemeal fashion individual technical features, without reference to the claim language as a whole, and oversimplify the technical aspects of those features to allege that such features would have been obvious. NVIDIA merely contends that prior art references allegedly describing certain concepts could be combined with prior art references allegedly describing certain other concepts. *See* NVIDIA Cover Pleading at 171-201. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

“The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue”). “Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’” *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). Rather than

articulate specifically how and why a person of skill would combine the references, the NVIDIA Cover Pleading provides swiping, over-simplified, and conclusory assertions that such combinations would have been made simply because general concepts allegedly would have been combined. The NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertions that there would have been a motivation to combine any of the cited references, and therefore fail to satisfy Respondents' burden. For example, by making its motivation to combine arguments based on overgeneralized concepts, NVIDIA does not assert, let alone explain or demonstrate that a POSITA would have been motivated to combine any particular references with any others (or in the case of combinations with three or more references with any other combinations of references), let alone to arrive at the claimed subject matter.

By failing or electing to not include any substantive assertions regarding the motivation to combine specific references, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would be within the skill of a POSITA or would yield predictable results, or would result in the claimed invention. In addition, as explained below, NVIDIA fails to show that a POSITA would have been

motivated to combine any of the proposed combinations of concepts.

Additionally, by addressing motivation to combine on a concept-by-concept basis, NVIDIA does not analyze whether a POSITA would have been motivated to combine the “specific references” as required. *See ActiveVideo Networks, Inc. v. Verizon Communs., Inc.* 694 F.3d 1312, 1327 (Fed. Cir. 2012) (holding the reasoning must “explain why a person of ordinary skill in the art would have combined elements *from specific references* in the way the claimed invention does” (emphasis added)). NVIDIA has “failed to explain how *specific references* could be combined, which combination(s) of *elements in specific references* would yield a predictable result, or how any *specific combination* would operate or read on the asserted claims.” *Id.* (emphases added); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (“A patent composed of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art.”); *Arctic Cat v. Bombardier Rec. Prods.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (“the prior art could contain one reference suggesting a combination and others critiquing or otherwise discouraging the same. Even a single reference can include both types of statements, and we have held that it is error to fail to consider the entirety of the art”). “[T]he Supreme Court has long held that ‘known disadvantages in old devices which would naturally discourage the search for new inventions may be taken into account in determining obviousness.’” *Arctic Cat*, 876 F.3d at 1360 (quoting *United States v. Adams*, 383 U.S. 39, 52, 86 S.Ct. 708, 15 L.Ed.2d 572 (1966)).

Additional rebuttal contentions regarding the allegations of invalidity under 35 U.S.C. §§ 102 and 103 for the ’943 Patent are provided below and in the attached Appendix A, incorporated herein by reference.

1. No Motivation to Combine “virtual devices on a CPU” with “a set of queues and command processor on a GPU”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 171. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... discloses virtual devices on a CPU (e.g., Gosalia, Dror, Margulis, Gupta, Alben, Hensley, and/or Blythe) with the teachings of prior art that, ... discloses GPUs with a set of queues and a command processor (e.g., Wyatt, Doyle, Gandhi, Meinert, Intel Chipset, Danskin, Garlick, Tesla, and/or Fermi).” NVIDIA Cover Pleading at 171-172. NVIDIA also contends that “A person of ordinary skill in the art also would have been motivated to combine Dror, Margulis, Gupta, Alben, Hensley, and/or Blythe (which disclose virtual devices ...) with Gosalia (which discloses a GPU with a set of queues and a command processor ...).” NVIDIA Cover Pleading at 172. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “virtual devices on a CPU” and “a set of queues and command

**processor on a GPU” Relate to Specific Asserted Claims of the
'943 Patent**

NVIDIA has not demonstrated how the alleged concepts of “virtual devices on a CPU” and “a set of queues and command processor on a GPU” relate to specific claims of the '943 Patent. For example, NVIDIA is overgeneralizing concepts from the '943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

**b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA
Would Be Motivated to Combine the Concepts of “virtual
devices on a CPU” and “a set of queues and command
processor on a GPU”**

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “virtual devices on a CPU” and “a set of queues and command processor on a GPU.”

The NVIDIA Invalidity Contentions assert that “the references are in the same field (graphics processing) and are directed at the same problem or objective—using a GPU to offload

graphics tasks from a CPU.” NVIDIA Cover Pleading at 172. However, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “using a GPU to offload graphics tasks from a CPU” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. A POSITA would have understood that “graphics processing” and “using a GPU to offload graphics tasks from a CPU” are directed to different focuses, and “graphics processing” can be done *without* “using a GPU to offload graphics tasks from a CPU.” Similarly, references focusing on “virtual devices on the CPU” may have nothing to do with “sending commands from the virtual devices to a GPU.” In fact, “graphics processing” or “virtual devices on the CPU” each encompasses a very broad subject matter. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that “The references themselves provide further motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 173. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of virtual devices on a CPU” and “a set of queues and command processor on a GPU,” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved, or the description sections describing the alleged solution to the problem. *See, e.g.*, NVIDIA Cover Pleading at 173-174 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a

motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA also asserts that a “person of ordinary skill in the art reading [a first group of references] would have known to look to references such as [a second group of references] that, ... describe how GPUs execute received commands once they are received from a virtual device on the CPU, including using a set of queues and command processor on the GPU,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 175. Rather than disclosing any contentions for why a POSITA would have known to look to the other references, NVIDIA provides only bare citation to *Wyatt 369*, *Doyle*, *Gosalia*, *Gandhi*, and *Meinerth*, and does not demonstrate that the references support the proposition that a POSITA would have known to look to the other references. Nor does NVIDIA explain how this relates to the alleged generalized concepts of “virtual devices on a CPU” and “a set of queues and command processor on a GPU.”

NVIDIA also asserts that a “person of skill in the art would have understood that virtual devices, like those that are described ... by [a first group of references] are intended to be used with a GPU, like those described ... by [a second group of references].” NVIDIA Cover Pleading at 177. However, NVIDIA does not provide any explanation or reasoning why that relates to the alleged combination of the generalized concepts of “virtual devices on a CPU” and “a set of queues and command processor on a GPU.” For example, not all GPUs require a set of queues and a command processor on a GPU; merely because using CPUs (even with virtual devices) with a GPU was allegedly known, that does not identify a motivation for a POSITA to combine references allegedly describing the use of virtual devices on a CPU with a set of queues and command processor on a GPU.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed

invention. For example, NVIDIA’s allegations that the implementing each combination “would have been a combination of known prior art elements ... according to known methods ... to yield predictable results” is wholly conclusory. NVIDIA Cover Pleading at 178. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

2. No Motivation to Combine “virtual devices on a CPU” with “prioritized execution of commands”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 181. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... discloses virtual devices on a CPU (e.g., Gosalia, Dror, Margulis, Gupta, Alben, Hensley, and/or Blythe) with the teachings of prior art that, ... discloses prioritized execution of commands (e.g., Danish and Gupta).” NVIDIA Cover Pleading at 181. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would

be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “virtual devices on a CPU” with “prioritized execution of commands” Relate to Specific Asserted Claims of the ’943 Patent

NVIDIA has not demonstrated how the alleged concepts of “virtual devices on a CPU” with “prioritized execution of commands” relate to specific claims of the ’943 Patent. For example, NVIDIA is overgeneralizing concepts from the ’943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA would be Motivated to Combine the Concepts of “virtual devices on a CPU” with “prioritized execution of commands”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “virtual devices on a CPU” with “prioritized execution of commands.”

The NVIDIA Invalidity Contentions assert that “the references are in the same field

(virtualization of computational resources...) and are directed at the same problem or objective—using virtualization to schedule commands for execution.” NVIDIA Cover Pleading at 182. However, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “using virtualization to schedule commands for execution” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. A POSITA would have understood that “virtualization of computational resources” and “using virtualization to schedule commands for execution” are directed to different focuses. NVIDIA has not provided any rationale or a special need for a POSITA to look into combining references allegedly disclosing “virtualization of computational resources” and “using virtualization to schedule commands for execution.” Similarly, NVIDIA has provided no basis or evidence to show why a POSITA “would have understood that systems that include virtual devices” “are intended to be used with scheduling techniques.” In fact, a POSITA would have understood that “systems that include virtual devices” have many other functions than “ “using virtualization to schedule commands for execution.” Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that the “references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 184. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “virtual devices on a CPU” with “prioritized execution of commands” or the actual requirements of the asserted claims. Moreover, the citations to the identified references

merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved, or the description sections describing the alleged solution to the problem. *See, e.g.*, NVIDIA Cover Pleading at 184-186 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA also asserts that a “person of ordinary skill in the art reading [a first group of references] would have known to look to references such as [a second group of references] that, ... describe prioritization of commands on the GPU,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 186. Rather than disclosing any contentions for why a POSITA would have known to look to the other references, NVIDIA provides only bare citation to *Danish* and *Gupta*, and does not demonstrate that the references support the proposition that a POSITA would have known to look to the other references. Nor does NVIDIA explain how this relates to the alleged generalized concepts of “virtual devices on a CPU” with “prioritized execution of commands.”

NVIDIA also asserts that a “person of skill in the art would have understood that virtual devices, like those that are described ... by [a first group of references] are intended to be used with a scheduling techniques, like those described ... by [a second group of references].” NVIDIA Cover Pleading at 187. However, NVIDIA does not provide any explanation or reasoning why that relates to the alleged combination of the generalized concepts of “virtual devices on a CPU” with “prioritized execution of commands.” For example, not all scheduling techniques require prioritized execution of commands; that does not identify a motivation for a POSITA to combine references allegedly describing the use of virtual devices on a CPU with a references allegedly

disclosing prioritized execution of commands.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegations that implementing each combination “would have been a combination of known prior art elements ... according to known methods ... to yield predictable results” is wholly conclusory. NVIDIA Cover Pleading at 189. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

3. No Motivation To Combine “discloses scheduling commands from virtual devices” with “scheduling commands from virtual devices in a round-robin manner”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 189. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... discloses scheduling commands from virtual devices (e.g., Gosalia, Dror, Margulis, Blythe, Hensley, and/or Blythe) with the teachings of prior art that, ... discloses scheduling commands in a round-robin manner (e.g., Gupta and Alben).” NVIDIA

Cover Pleading at 189-190. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “discloses scheduling commands from virtual devices” with “scheduling commands from virtual devices in a round-robin manner” Relate to specific Asserted Claims of the ’943 Patent

NVIDIA has not demonstrated how the alleged concepts of “discloses scheduling commands from virtual devices” with “scheduling commands from virtual devices in a round-robin manner” relate to specific claims of the ’943 Patent. For example, NVIDIA is overgeneralizing concepts from the ’943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA Would Be Motivated to Combine the Concepts of “discloses

**scheduling commands from virtual devices” with “scheduling
commands from virtual devices in a round-robin manner”**

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “discloses scheduling commands from virtual devices” with “scheduling commands from virtual devices in a round-robin manner.”

The NVIDIA Invalidity Contentions assert that “[a]s explained above, a person of ordinary skill in the art would have been motivated to combine these references because they are in the same field and are directed at the same problem or objective.” NVIDIA Cover Pleading at 190 (citing “Section V.B.2.a.”). First, the referenced section (“explained above”) does not relate to these references, what they are directed to (or whether they are directed to the same field or endeavor) or the motivation to combine analysis. *See, e.g.*, NVIDIA Cover Pleading at 190 (citing “Section V.B.2.a.”); *id.* at Section V.B.2 (asserting that “Shader cores in the GPU that execute tasks based on state data” was a “core concept[] well known in the prior art,” and not having a subsection “a”). Second, even assuming NVIDIA mis-cited the section to which it intended to refer—and it meant Section VI.B.2.a—that section does not identify the same references or the same asserted combination of generalized concepts. For example, Section VI.B.2.a identifies references that NVIDIA asserts “disclose[] GPUs with a set of queues and a command processor.” NVIDIA Cover Pleading at 171-172. Further, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “GPUs with a set of queues and a command processor” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that the “references themselves provide a motivation to combine,”

but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 190. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “discloses scheduling commands from virtual devices” with “scheduling commands from virtual devices in a round-robin manner” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved, or the description sections describing the alleged solution to the problem. *See, e.g.*, NVIDIA Cover Pleading at 190-191 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA also asserts that a “round-robin scheduling was among a finite number of well-known scheduling techniques that existed before the alleged invention of the ’943 patent, and as such would have been obvious to try.” NVIDIA Cover Pleading at 191-192. However, NVIDIA does not disclose any contentions for what the finite number of allegedly well-known scheduling techniques were, or any benefits or drawbacks for any over the others such that picking one “would have been obvious to try.” *Id.* By failing or electing to not include any identification of the allegedly finite number of solutions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity

Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA's allegations that implementing each combination "would have been a combination of known prior art elements ... according to known methods ... to yield predictable results" is wholly conclusory. NVIDIA Cover Pleading at 192. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

4. No Motivation to Combine "executing commands on a GPU" with "sending a result of the command from the GPU to the CPU"

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 192. "The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims' actual limitations." *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) ("The inquiry is not whether a relevant artisan would combine a first reference's feature with a second reference's feature to meet requirements of the first reference that are not requirements of the claims at issue.").

NVIDIA contends that "[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... executing a command on a GPU (e.g., Gosalia, Dror,

Margulis, Gupta, Blythe, Alben, Hensley, Blythe, Wyatt, Doyle, Gandhi, Meinerth, Intel Chipset, Danskin, Garlick, Tesla, and/or Fermi) with the teachings of prior art that ... discloses sending the result to the CPU (e.g., Buck).” NVIDIA Cover Pleading at 192-193. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU” Relate to Specific Asserted Claims of the ’943 Patent

NVIDIA has not demonstrated how the alleged concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU” relate to specific claims of the ’943 Patent. For example, NVIDIA is overgeneralizing concepts from the ’943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement

its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA Would be Motivated to Combine the Concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU”

The NVIDIA Invalidity Contentions assert that “the references are in the same field (graphics processing) and are directed at the same problem or objective—using a GPU to offload graphics tasks from a CPU.” NVIDIA Cover Pleading at 194. However, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “using a GPU to offload graphics tasks from a CPU” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that the “references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 195. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU” or the actual requirements of the asserted claims. For example, NVIDIA asserts that “Buck asserts that sending commands from the GPU to the CPU... allows GPUs ... to

be used as a general purpose parallel processor for applications such as machine learning algorithms that ‘run an order of magnitude faster on a GPU than on a CPU,’” but does not explain how this provides a motivation with respect to the identified generalized concepts, nor how it affects the motivation to combine other references. NVIDIA Cover Pleading at 195. In fact, as quoted by NVIDIA, *Buck* is directed to a “machine learning GPU” and “[t]he results of the computation are transferred from the machine learning GPU execution engine 200 to the CPU 120 for use in interactive use applications, such as speech recognition.” See NVIDIA Cover Pleading at 193. NVIDIA has not explained why a POSITA would look to *Buck* for combining references in the fields of “**graphics processing**” and “using a GPU to **offload graphics tasks** from a CPU.” NVIDIA has not met its burden of showing a motivation to combine any of its alleged references. Further, that, *e.g.*, *Buck* purports to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to *Buck*’s disclosures.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegations that implementing each combination “would have been a combination of known prior art elements ... according to known methods ... to yield predictable results” or would only require “straightforward modifications to software running on the CPU” is wholly conclusory. NVIDIA Cover Pleading at 192. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only straightforward modifications to software running on the CPU, or would result in the claimed invention.

5. No Motivation to Combine “controlling a command processor” with “using a run list controller to control a command processor on the GPU”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 196. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... discloses controlling a command processor (e.g., Margulis, Gupta, Blythe, Alben, Hensley, Blythe, Wyatt, Doyle, Gandhi, Meinerth, Intel Chipset, Danskin, Garlick, Tesla, and/or Fermi) with the teachings of prior art that ... discloses using a run list controller (e.g., Gosalia and Dror).” NVIDIA Cover Pleading at 197. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “controlling a command processor” with “using a run list controller to control a command processor on the GPU” Relate to Specific Asserted Claims of the ’943 Patent

NVIDIA has not demonstrated how the alleged concepts of “controlling a command

processor” with “using a run list controller to control a command processor on the GPU” relate to specific claims of the ’943 Patent. For example, NVIDIA is overgeneralizing concepts from the ’943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA would be Motivated to Combine the Concepts of “controlling a command processor” with “using a run list controller to control a command processor on the GPU”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “controlling a command processor” with “using a run list controller to control a command processor on the GPU.”

The NVIDIA Invalidity Contentions assert that “[a]s explained above, a person of ordinary skill in the art would have been motivated to combine these references because they are in the same field and are directed at the same problem or objective.” NVIDIA Cover Pleading at 197 (citing “Section V.B.2.a.”). First, the referenced section (“explained above”) does not relate to

these references, what they are directed to (or whether they are directed to the same field or endeavor) or the motivation to combine analysis. *See, e.g.*, NVIDIA Cover Pleading at 197 (citing “Section V.B.2.a”); *id.* at Section V.B.2 (asserting that “Shader cores in the GPU that execute tasks based on state data” was a “core concept[] well known in the prior art,” and not having a subsection “a”). Second, even assuming NVIDIA mis-cited the section to which it intended to refer—and it meant Section VI.B.2.a—that section does not identify the same references or the same asserted combination of generalized concepts. For example, Section VI.B.2.a identifies references that NVIDIA asserts “disclose[] GPUs with a set of queues and a command processor.” NVIDIA Cover Pleading at 171-172. Further, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “GPUs with a set of queues and a command processor” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that the “references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 197. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “executing commands on a GPU” with “sending a result of the command from the GPU to the CPU” or the actual requirements of the asserted claims. For example, NVIDIA states that “Gosalia asserts that using a run list controller ... is a ‘convenient’ way to execute commands on a GPU ‘without CPU intervention,’” but does not explain how this provides a motivation with respect to the identified generalized concepts, nor how it affects the motivation to

combine other references. NVIDIA Cover Pleading at 197.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA's allegations that implementing each combination "would have been a combination of known prior art elements ... according to known methods ... to yield predictable results" is wholly conclusory. NVIDIA Cover Pleading at 198. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only straightforward modifications to software running on the CPU, or would result in the claimed invention.

6. No Motivation to Combine "virtual devices on a CPU" with "generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver"

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 198. "The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims' actual limitations." *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) ("The inquiry is not whether a relevant artisan would combine a first reference's feature with a second reference's feature to meet requirements of the first reference that are not requirements of the claims at issue.").

NVIDIA contends that "[a] person of ordinary skill in the art would have been motivated to combine the teachings of prior art that, ... discloses virtual devices (e.g., Margulis, Gupta, Blythe, Alben, Hensley, and/or Blythe) with the teachings of prior art that, ... discloses generating commands from a user mode driver instance and fetching the commands from the virtual devices

using a kernel mode driver (e.g., Gosalia and/or Dror).” NVIDIA Cover Pleading at 198-199. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver” Relate To Specific Asserted Claims of the ’943 Patent

NVIDIA has not demonstrated how the alleged concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver” relate to specific claims of the ’943 Patent. For example, NVIDIA is overgeneralizing concepts from the ’943 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA would be Motivated to Combine the Concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver.”

The NVIDIA Invalidity Contentions assert that “[a]s explained above, a person of ordinary skill in the art would have been motivated to combine these references because they are in the same field and are directed at the same problem or objective.” NVIDIA Cover Pleading at 199 (citing “Section V.B.2.a.”). First, the referenced section (“explained above”) does not relate to these references, what they are directed to (or whether they are directed to the same field or endeavor) or the motivation to combine analysis. *See, e.g.*, NVIDIA Cover Pleading at 199 (citing “Section V.B.2.a.”); *id.* at Section V.B.2 (asserting that “Shader cores in the GPU that execute tasks based on state data” was a “core concept[] well known in the prior art,” and not having a subsection “a”). Second, even assuming NVIDIA mis-cited the section to which it intended to refer—and it meant Section VI.B.2.a—that section does not identify the same references or the same asserted combination of generalized concepts. For example, Section VI.B.2.a identifies references that NVIDIA asserts “disclose[] GPUs with a set of queues and a command processor.” NVIDIA Cover Pleading at 171-172. Further, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “GPUs with a set of queues and a command processor” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA also asserts that the “references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 199. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver” or the actual requirements of the asserted claims. NVIDIA states that “Gosalia asserts that using user mode and kernel mode drivers ... provides system security.” NVIDIA Cover Document at 199. However NVIDIA does not explain how or why that is the case, or why that provides the alleged motivation to combine the concepts of “virtual devices on a CPU” with “generating commands from a user mode driver instance and fetching commands from virtual devices using a kernel mode driver,” or the identified references, let alone to arrive at the claimed invention.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegations that implementing each combination “would have been a combination of known prior art elements ... according to known methods ... to yield predictable results” is wholly conclusory. NVIDIA Cover Pleading at 200. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

B. U.S. Patent No. 11,841,803

NVIDIA has failed to meet its burden in setting forth contentions that would support its allegations of anticipation and/or obviousness of the ’803 Patent. NVIDIA asserts 25 devices and

systems, patent references, and non-patent literature references in the NVIDIA Cover Pleading (*see e.g.*, pp. 19-24) and NVIDIA Exhibits (*see e.g.*, Exs. 803-A-1 through A-12 and 803-B) as alleged prior art to the '803 Patent (" '803 References").

First and foremost, the NVIDIA Invalidity Contentions fail to prove that each of the asserted '803 References is eligible as a prior art to the '803 Patent. The NVIDIA Invalidity Contentions did not identify under which section of law each reference allegedly qualifies as prior art. Rather, NVIDIA made a blanket citation to "35 U.S.C. §102 and/or § 103. *See, e.g.*, NVIDIA Cover Pleading at 7. It is unclear which specific date NVIDIA asserts is the operative date for each of the '803 References, and under which section of law NVIDIA asserts each of the '803 References qualifies as prior art. For example, the NVIDIA Invalidity Contentions did not identify, *e.g.*, for patent references, whether NVIDIA is relying on the provisional filing date, non-provisional filing date, earliest non-provisional filing date, pre-grant publication date, or patent grant publication date. The NVIDIA Invalidity Contentions also included numerous errors on the patent numbers, dates, and bates number when listing the references it asserts. The NVIDIA Invalidity Contentions fail to satisfy Respondents' burden and have not placed Onesta on notice of any specific allegations based on these references.

Further, the NVIDIA Invalidity Contentions attempt to rely on six alleged systems or devices as prior art in its Invalidity Contentions, including "AMD products implementing High Bandwidth Memory (HBM)," "AMD products implementing High Bandwidth Memory (HBM) and Infinity Fabric," "Products implementing MoChi and FLC Architectures," "Products implementing EMIB, including Stratix 10," "Fan-out Mediatek Innovation Package," and "NVIDIA Tesla P100." NVIDIA Cover Pleading at 19-21. But each of these alleged systems includes a number of devices released at different dates. By simply citing a code name or family name of a series of products, NVIDIA has failed to meet its burden to show by clear and convincing

evidence which specific system or device it alleges as prior art. *See e.g.*, “AMD Products implementing High Bandwidth Memory (HBM) and Infinity Fabric,” NVIDIA Cover Pleading at 20, NVIDIA Ex. 803-A-07; “Marvell Products implementing MoChi and FLC Architectures,” NVIDIA Cover Pleading at 20, NVIDIA Ex. 803-A-08; “Intel Products implementing EMIB in Stratix 10,” NVIDIA Cover Pleading at 20-21, NVIDIA Ex. 803-A-09; “NVIDIA Tesla P100,” NVIDIA Cover Pleading at 21, NVIDIA Ex. 803-A-10; and MediaTek Fan-out Innovation Package,” NVIDIA Cover Pleading at 21, NVIDIA Ex. 803-A-11.

To the extent the NVIDIA Invalidity Contentions rely on any specific product, NVIDIA has failed to prove the features relied on from the cited documents were actually implemented in that specific product earlier than the priority date of the ’803 Patent.⁵ Nor did NVIDIA show the features or functions cited from the documents were actually implemented in the alleged system or device “known or used by others in this country” or “in public use or on sale in this country, more than one year prior to” the priority date of the ’803 Patent. The NVIDIA Invalidity Contentions fail to satisfy Respondents’ burden and have not placed Onesta on notice of any specific allegations based on any system or device.

In addition to failing to prove that the ’803 References qualify as prior art, the NVIDIA Invalidity Contentions fail to prove that the ’803 References anticipate or render obvious the asserted claims of the ’803 Patent. Even considering the teachings of the references, the references and any/all combinations thereof do not invalidate the asserted claims of the ’803 Patent under 35 U.S.C. §§ 102 and/or 103. For example, none of the ’803 References discloses each and every

⁵ Multiple documents cited by NVIDIA are clearly dated after the priority date of the ’803 Patent. *See, e.g.*, “Stratix® 10 GX/SX Device Overview,” NVIDITC-000134348-4386, dated June 28, 2024; “Stratix® 10 Device Overview,” NVIDITC-000134387- 4425, dated September 7, 2023; “Marvell® ARMADA® with Marvell MoChi, Product brief,” NVIDITC-000134546-4548, indicated “Revised: 11/20” with copyright mark in 2020; a Marvell article “Chiplets Turn 10: Here are Ten Things to Know,” NVIDITC-000134549-4554.

claim element of the asserted '803 Patent claims. Nor do any of the '803 references render obvious each and every claim element of the asserted '803 Patent claims, alone or in combination with any of the other '803 References. For example, in NVIDIA Ex. 803-B, NVIDIA provides a chart entitled "Compilation of Disclosures from Additional Prior Art References" excerpting disclosures from twelve of the '803 References (*see e.g.*, NVIDIA Ex. 803-B at 1), but these twelve references, considered alone or in combination (either in combination with each other or in combination with any other reference), do not render the '803 Patent claims anticipated or obvious at least because they do not, under any of the proposed constructions, expressly or inherently disclose all the limitations claimed in the '803 Patent. The NVIDIA Invalidity Contentions do not provide any explanation or reasoning as to how any asserted references would be combined to arrive at the claimed invention. "Obviousness 'cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.'" *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). The NVIDIA Invalidity Contentions also fail to prove that the '803 Patent is invalid as obvious because they fail to provide contentions regarding the analysis of the *Graham* factors, such as the differences between the prior art and the claimed invention. *See Graham v. John Deere Co.*, 383 U.S. 1 (1966).

The NVIDIA Invalidity Contentions also fail to prove that any of the '803 References would be combined with any of the other references, for example by failing to prove that a POSITA would have been motivated to combine the references to arrive at the claimed invention. "[T]here must exist a motivation to combine various prior art references in order for a skilled artisan to make the claimed invention." *Virtek Vision Int'l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024). "Obviousness is an issue of law decided based on numerous factual findings, including the scope and content of the prior art, the level of ordinary skill, and whether a

relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 956 (Fed. Cir. 2023). “The ultimate conclusion of obviousness is a legal determination based on underlying factual findings, including whether or not a relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Volvo Penta of the Americas v. Brunswick Corp.*, 81 F.4th 1202, 1209 (Fed. Cir. 2023); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (there must be “a reason” for a skilled artisan “to combine the elements in the way the claimed new invention does”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”).

Although NVIDIA purports to present “exemplary” motivations to combine in Section VI B.3 of the NVIDIA Cover Pleading, NVIDIA’s Invalidity Contentions extract in a piecemeal fashion individual technical features, without reference to the claim language as a whole, and oversimplify the technical aspects of those features to allege that such features would have been obvious. NVIDIA merely contends that prior art references allegedly describing certain concepts could be combined with prior art references allegedly describing certain other concepts. *See* NVIDIA Cover Pleading at 206-221. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

“The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”). “Obviousness ‘cannot be based on the hindsight

combination of components selectively culled from the prior art to fit the parameters of the patented invention.”” *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). Rather than articulate specifically how and why a person of skill would combine the references, the NVIDIA Cover Pleading provides sweeping, over-simplified, and conclusory assertions that such combinations would have been made simply because general concepts allegedly would have been combined. The NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertions that there would have been a motivation to combine any of the cited references, and therefore fail to satisfy Respondents’ burden. For example, by making its motivation to combine arguments based on overgeneralized concepts, NVIDIA does not assert, let alone explain or demonstrate that a POSITA would have been motivated to combine any particular references with any others (or in the case of combinations with three or more references with any other combinations of references), let alone to arrive at the claimed subject matter. By failing or electing to not include any substantive assertions regarding the motivation to combine specific references, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would be

within the skill of a POSITA or would yield predictable results, or would result in the claimed invention. In addition, as explained below, NVIDIA fails to show that a POSITA would have been motivated to combine any of the proposed combinations of concepts.

Additionally, by addressing motivation to combine on a concept-by-concept basis, NVIDIA does not analyze whether a POSITA would have been motivated to combine the “specific references” as required. *See ActiveVideo Networks, Inc. v. Verizon Communs., Inc.*, 694 F.3d 1312, 1327 (Fed. Cir. 2012) (holding the reasoning must “explain why a person of ordinary skill in the art would have combined elements *from specific references* in the way the claimed invention does” (emphasis added)). NVIDIA has “failed to explain how *specific references* could be combined, which combination(s) of *elements in specific references* would yield a predictable result, or how any *specific combination* would operate or read on the asserted claims.” *Id.* (emphasis added); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (“A patent composed of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art.”); *Arctic Cat v. Bombardier Rec. Prods.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (“the prior art could contain one reference suggesting a combination and others critiquing or otherwise discouraging the same. Even a single reference can include both types of statements, and we have held that it is error to fail to consider the entirety of the art”). “[T]he Supreme Court has long held that ‘known disadvantages in old devices which would naturally discourage the search for new inventions may be taken into account in determining obviousness.’” *Arctic Cat*, 876 F.3d at 1360 (quoting *United States v. Adams*, 383 U.S. 39, 52, 86 S.Ct. 708, 15 L.Ed.2d 572 (1966)).

Additional rebuttal contentions regarding the allegations of invalidity under 35 U.S.C. §§ 102 and 103 for the ’803 Patent are provided below and in the attached Appendix D, incorporated herein by reference.

1. No Motivation To Combine “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 206. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine (1) the teachings of any of the prior art references cited in these invalidity contentions that ... describe GPU chiplets and (2) the teachings of any of the cited prior art references that ... describe passive interconnects dedicated for inter-chiplet communication.” NVIDIA Cover Pleading at 206. NVIDIA does not even identify which references it asserts disclose each of these generalized concepts, and therefore fails to assert any motivation to combine with respect to any references at all. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated how the Alleged Concepts of “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication” relate to Specific Asserted Claims of the ’803 Patent

NVIDIA has not demonstrated how the alleged concepts of “GPU chiplets” with “passive

interconnects dedicated for inter-chiplet communication” relate to specific claims of the ’803 Patent. For example, NVIDIA is overgeneralizing concepts from the ’803 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated any Reason why a POSITA Would Be Motivated to Combine the Concepts of “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication.”

The NVIDIA Invalidity Contentions assert that “the references are in the same field (integrating multiple dies or chiplets onto one substrate) and are directed at the same solution—enabling high-performance communication between chiplets.” NVIDIA Cover Pleading at 207. However, contrary to NVIDIA’s assertions, the references are not all “directed at the same

solution” at least because “communication between chiplets” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

NVIDIA asserts that “Long before 2019, the semiconductor industry had already begun transitioning away from monolithic system-on-chip (SoC) designs toward chiplet-based systems, to improve manufacturing yield, reduce cost, and enable heterogeneous integration,” but does not explain how this relates to the alleged motivation to combine the generalized concepts of “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication.” *See* NVIDIA Cover Pleading at 208.

NVIDIA also asserts that “The references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 209. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “GPU chiplets” with “passive interconnects dedicated for inter-chiplet communication” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved, or the description sections describing the alleged solution to the problem. *See, e.g.,* NVIDIA Cover Pleading at 209-210 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no

longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA also asserts that a “[t]hese systems used known and conventional interconnect technologies to link the chiplets together,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 210. For example, NVIDIA does not identify which references it is referring to as “these systems,” or provide any support for the assertion that they “used known and conventional interconnect technologies.” *Id.*

NVIDIA asserts that a POSITA “would have recognized that these interconnect solutions had limitations and were ready for improvement.” NVIDIA Cover Pleading at 211. NVIDIA also asserts that a POSITA “would have recognized that several passive interconnect structures offered an improvement.” NVIDIA Cover Pleading at 212. However, NVIDIA’s Invalidity Contentions ignore the realities facing a POSITA and the difficulties of implementing a GPU chiplet design. For example, prior to the ’803 Patent, most use of chiplets in processor design was limited to CPUs, which have a very different architecture and intended use compared to GPUs. Those skilled in the art regarded it as challenging to bring chiplet designs to GPU architectures due to the way GPUs process data, including using a very high level of parallelism, and the perceived requirement for synchronous ordering.

The ’803 Patent implemented a novel and non-obvious solution for structuring GPUs. For example, in some embodiments, a CPU is included in the system and is communicably coupled to a GPU chiplet of the GPU chiplet array. From the CPU’s or a programmer’s view, the application appears to be addressing a single GPU, despite there being multiple GPU chiplets in the GPU chiplet array. This enables the use of a large-capacity, multi-chiplet GPU that appears as a single device to the application. Prior solutions did not offer such an interface or the performance that is achievable with the use of such an arrangement. The architecture also used a unified, coherent last-level cache across all GPU chiplets. This means a processing core on one chiplet can seamlessly

access data stored in the L3 cache of another chiplet without complex coherency protocols.

Even years later, in 2024, industry insiders were still commenting that “Building a multi-chiplet GPU is no small feat. One of the critical challenges Intel faces in making disaggregated GPUs a reality is developing robust interconnect technology.” Onesta-ITC1450_0074031 (<https://techovedas.com/intels-disaggregated-gpu-patent-marks-a-shift-to-chiplet-architecture-boosting-efficiency-and-sparking-competition-with-amd/>). “Manufacturing a GPU with multiple chiplets requires advanced techniques and technology.” *Id.* “[E]fficient interconnect solutions ... can add complexity and cost.” *Id.* “The challenges of manufacturing and interconnect technology will require significant innovation,” even as of 2024.

Moreover, as of 2018, the industry identified issues with using a chiplet design: “as the number of modules in a given chip increase, so does complexity of signal processing and routing.” Onesta-ITC1450_0074265 (<https://www.techpowerup.com/245521/on-the-coming-chiplet-revolution-and-amds-mcm-promise>).

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegations that the implementing each combination “would have amounted to applying a known technique—interconnecting chiplets via a passive interconnect—to a known system—multi-chip module—to solve a known problem—limited bandwidth and excessive heat” or that it would merely involve “routine engineering practices” is wholly conclusory. NVIDIA Cover Pleading at 215. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

2. No Motivation To Combine “GPU chiplets connected by passive interconnects dedicated for inter-chiplet communication” with “cache memory hierarchies at each chiplet”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 216. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine (1) the teachings of any of the prior art references cited in these invalidity contentions that ... describe GPU chiplets connected by passive interconnects dedicated for inter-chiplet communication and (2) the teachings of any of the cited prior art references that ... describe cache memory hierarchies at each chiplet.” NVIDIA Cover Pleading at 216. NVIDIA does not even identify which references it asserts disclose each of these generalized concepts, and therefore fails to assert any motivation to combine with respect to any references at all. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “GPU chiplets connected by passive interconnects dedicated for inter-chiplet communication” with “cache memory

**hierarchies at each chiplet” relate to Specific Asserted Claims
of the ’803 Patent**

NVIDIA has not demonstrated how the alleged concepts of “GPU chiplets connected by passive interconnects dedicated for inter-chiplet communication” with “cache memory hierarchies at each chiplet” relate to specific claims of the ’803 Patent. For example, NVIDIA is overgeneralizing concepts from the ’803 Patent, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

**b. NVIDIA Has Not Demonstrated any Reason why a POSITA
Would Be Motivated to Combine the Concepts of “GPU
chiplets connected by passive interconnects dedicated for inter-
chiplet communication” with “cache memory hierarchies at
each chiplet”**

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “GPU chiplets connected by passive interconnects dedicated for inter-chiplet communication” with “cache memory hierarchies at each chiplet.”

The NVIDIA Invalidity Contentions assert that “the references are in the same field (integrating multiple dies or chiplets onto one substrate) and are directed at the same solution (enabling high-performance communication and coordination between chiplets and/or reducing manufacturing costs).” NVIDIA Cover Pleading at 216. However, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “communication and coordination between chiplets and/or reducing manufacturing costs” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegations that the implementing each combination “would have amounted to applying a known technique—interconnecting chiplets via a passive interconnect—to a known system—multi-chip module—to solve a known problem—limited bandwidth and excessive heat” or that it would merely be a “routine design choice” is wholly conclusory. NVIDIA Cover Pleading at 220-221. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention.

C. U.S. Patent Nos. 9,116,809 and 11,741,019

NVIDIA has failed to meet its burden in setting forth contentions that would support its

allegations of anticipation⁶ and/or obviousness of the '809 Patent and '019 Patent. NVIDIA asserts 28 devices and systems, patent references, and non-patent literature references in the NVIDIA Cover Pleading (*see e.g.*, pp. 24-25) and NVIDIA Exhibits (*see e.g.*, Exs. 809-A-1 through A-15 and 809-B) as alleged prior art to the '809 Patent and '019 Patent (“ '809/'019 References”).

First and foremost, the NVIDIA Invalidity Contentions fail to prove that each of the asserted '809/'019 References is eligible as a prior art to the '809 Patent and '019 Patent. The NVIDIA Invalidity Contentions did not identify under which section of law each reference allegedly qualifies as prior art. Rather, NVIDIA made a blanket citation to “35 U.S.C. §102 and/or § 103.” *See, e.g.*, NVIDIA Cover Pleading at 7. It is unclear which specific date NVIDIA asserts is the operative date for each of the '809/'019 References, and under which section of law NVIDIA asserts each of the '809/'019 References qualifies as prior art. For example, the NVIDIA Invalidity Contentions did not identify, *e.g.*, for patent references, whether NVIDIA is relying on the provisional filing date, non-provisional filing date, earliest non-provisional filing date, pre-grant publication date, or patent grant publication date. The NVIDIA Invalidity Contentions also included numerous errors on the patent numbers, dates, and bates number when listing the references it asserts. The NVIDIA Invalidity Contentions fail to satisfy Respondents' burden and have not placed Onesta on notice of any specific allegations based on these references.

In addition to failing to prove that the '809/'019 References qualify as prior art, the NVIDIA Invalidity Contentions fail to prove that the '809/'019 References anticipate or render obvious the asserted claims of the '809 Patent and '019 Patent. Even considering the teachings of

⁶ NVIDIA does not allege that any of the primary references identified in Exs. 019-A-01 through 019A-15 or 809-A-01 through 809-A-15 anticipate the '019 and '809 Patents' Asserted Claims under 35 U.S.C. §102. *See* NVIDIA Cover Pleading, 121-123 (asserting anticipation, but not including '019 or '809 Patents).

the references, the references and any/all combinations thereof do not invalidate the asserted claims of the '809 Patent and '019 Patent under 35 U.S.C. §§ 102 and/or 103. For example, none of the '809/'019 References discloses each and every claim element of the asserted '809 Patent and '019 Patent claims. Nor do any of the '809/'019 references render obvious each and every claim element of the asserted '809 Patent and '019 Patent claims, alone or in combination with any of the other '809/'019 References. For example, in NVIDIA Ex. 809-B and NVIDIA Ex. 019-B, NVIDIA provides charts entitled "Compilation of Disclosures from Additional Prior Art References" excerpting disclosures from fourteen references for the '809 Patent (*see e.g.*, NVIDIA Ex. 809-B at 1) and the '019 Patent (*see e.g.*, NVIDIA Ex. 019-B at 1), but these references, considered alone or in combination (either in combination with each other or in combination with any other reference), do not render the '809 Patent and '019 Patent claims anticipated or obvious at least because they do not, under any of the proposed constructions, expressly or inherently disclose all the limitations claimed in the '809 Patent and '019 Patent. The NVIDIA Invalidity Contentions do not provide any explanation or reasoning as to how any asserted references would be combined to arrive at the claimed invention. "Obviousness 'cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.'" *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). The NVIDIA Invalidity Contentions also fail to prove that the '809 Patent and '019 Patent are invalid as obvious because they fail to provide contentions regarding the analysis of the *Graham* factors, such as the differences between the prior art and the claimed invention. *See Graham v. John Deere Co.*, 383 U.S. 1 (1966).

The NVIDIA Invalidity Contentions also fail to prove that any of the '809/'019 References would be combined with any of the other references, for example by failing to prove that a POSITA

would have been motivated to combine the references to arrive at the claimed invention. “[T]here must exist a motivation to combine various prior art references in order for a skilled artisan to make the claimed invention.” *Virtek Vision Int’l ULC v. Assembly Guidance Sys., Inc.*, 97 F.4th 882, 887 (Fed. Cir. 2024). “Obviousness is an issue of law decided based on numerous factual findings, including the scope and content of the prior art, the level of ordinary skill, and whether a relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 956 (Fed. Cir. 2023). “The ultimate conclusion of obviousness is a legal determination based on underlying factual findings, including whether or not a relevant artisan would have had a motivation to combine references in the way required to achieve the claimed invention.” *Volvo Penta of the Americas v. Brunswick Corp.*, 81 F.4th 1202, 1209 (Fed. Cir. 2023); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (there must be “a reason” for a skilled artisan “to combine the elements in the way the claimed new invention does”); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) (“[O]bviousness concerns whether a skilled artisan not only could have made but would have been motivated to make the combinations or modifications of prior art to arrive at the claimed invention.”).

Although NVIDIA purports to present “exemplary” motivations to combine in Section VI B.4 of the NVIDIA Cover Pleading, NVIDIA’s Invalidity Contentions extract in a piecemeal fashion individual technical features, without reference to the claim language as a whole, and oversimplify the technical aspects of those features to allege that such features would have been obvious. NVIDIA merely contends that prior art references allegedly describing certain concepts could be combined with prior art references allegedly describing certain other concepts. *See* NVIDIA Cover Pleading at 236-248. For each of these combinations, NVIDIA offers the same rationale: that “the references are in the same field (memory management) and are directed at the

same solution (effective allocation and mapping of memory).” *Id.* at 236, 241, 245 However, contrary to NVIDIA’s assertions, the references are not all “directed at the same solution” at least because “effective allocation and mapping of memory” may be brought about in numerous different ways which will differ depending on the specific characteristics of a particular computing arrangement. Moreover, being in the same field of endeavor is a prerequisite, it does not provide a motivation to combine references. This does not satisfy Respondents’ burden of proving invalidity by clear and convincing evidence.

“The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”). “Obviousness ‘cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.’” *Cheese Sys. v. Tetra Pak Cheese & Powder Sys.*, 725 F.3d 1341, 1352 (Fed. Cir. 2013) (quoting *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998)). Rather than articulate specifically how and why a person of skill would combine the references, the NVIDIA Cover Pleading provides sweeping, over-simplified, and conclusory assertions that such combinations would have been made simply because general concepts allegedly would have been combined. The NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertions that there would have been a motivation to combine any of the cited references, and therefore fail to satisfy Respondents’ burden. For example, by making its motivation to combine arguments based on overgeneralized concepts, NVIDIA does not assert, let alone explain or demonstrate that a POSITA would have been motivated to combine any particular references with any others (or in the case of combinations with three or more references with any other

combinations of references), let alone to arrive at the claimed subject matter. By failing or electing to not include any substantive assertions regarding the motivation to combine specific references, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would be within the skill of a POSITA or would yield predictable results, or would result in the claimed invention. In addition, as explained below, NVIDIA fails to show that a POSITA would have been motivated to combine any of the proposed combinations of concepts.

Additionally, by addressing motivation to combine on a concept-by-concept basis, NVIDIA does not analyze whether a POSITA would have been motivated to combine the “specific references” as required. *See ActiveVideo Networks, Inc. v. Verizon Communs., Inc.* 694 F.3d 1312, 1327 (Fed. Cir. 2012) (holding the reasoning must “explain why a person of ordinary skill in the art would have combined elements *from specific references* in the way the claimed invention does” (emphasis added)). NVIDIA has “failed to explain how *specific references* could be combined, which combination(s) of *elements in specific references* would yield a predictable result, or how any *specific combination* would operate or read on the asserted claims.” *Id.* (emphasis added); *see also KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (“A patent composed

of several elements is not proved obvious by merely demonstrating that each of its elements was, independently, known in the prior art.”); *Arctic Cat v. Bombardier Rec. Prods.*, 876 F.3d 1350, 1360 (Fed. Cir. 2017) (“the prior art could contain one reference suggesting a combination and others critiquing or otherwise discouraging the same. Even a single reference can include both types of statements, and we have held that it is error to fail to consider the entirety of the art”). “[T]he Supreme Court has long held that ‘known disadvantages in old devices which would naturally discourage the search for new inventions may be taken into account in determining obviousness.’” *Arctic Cat*, 876 F.3d at 1360 (quoting *United States v. Adams*, 383 U.S. 39, 52, 86 S.Ct. 708, 15 L.Ed.2d 572 (1966)).

Additional rebuttal contentions regarding the allegations of invalidity under 35 U.S.C. § 102 and 103 for the ’809 Patent and ’019 Patent are provided below and in the attached Appendices D and C, incorporated herein by reference.

1. No Motivation To Combine “a method of allocating memory to a memory operation” with “mapping the memory operation to one of a plurality of memory heaps”

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 236. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated

to combine (1) the teachings of any of the prior art references cited in these invalidity contentions (e.g., Sollich, Motohashi, Madhavarao, and/or Milos) that... describe a method of allocating memory to a memory operation... and (2) the teachings of any of the cited prior art references (e.g., Tong, Motohashi, Shebanaw, Blinzer, Minkin, Case, Wilt, Ni, AMD-IOMMU, Kegel, Mohideen, Rogers, Freimuth, and/or Intel ATS Art) that... describe mapping the memory operation to one of a plurality of memory heaps/virtual memory pool.” NVIDIA Cover Pleading at 236. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated how the Alleged Concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps” relate to Specific Asserted Claims of the ’809 and ’019 Patents

NVIDIA has not demonstrated how the alleged concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps” relate to specific claims of the ’809 and ’019 Patents. For example, NVIDIA is overgeneralizing concepts from the ’809 and ’019 Patents, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations

since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA Would be Motivated to Combine the Concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps.”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps.”

For example, NVIDIA asserts first that “computer engineers had understood that when allocating memory for memory operations it may be beneficial to map virtual memory to physical memory,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 237. Rather than disclosing any contentions for why this was allegedly well known, NVIDIA provides only bare citation to *Tong* and *Shebanow*, and does not demonstrate that the references disclose or render obvious this supposed well known understanding, let alone how or why that provides motivation to combine references describing the generalized concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps,” or the actual requirements of the asserted claims. *See* NVIDIA Cover Pleading at 237 (citing *Tong* and *Shebanow*). For example, the cited portion of *Tong* describes only that “a translation between the virtual addresses used by the GPU and the physical addresses used by the system memory is performed,” which *Tong* describes as being done using “page mapping.” *See* NVIDIA Cover Pleading at 236-237 (citing *Tong*); *see also* *Tong* at Title, ¶ [0043].

Similarly, *Shebanow* discloses “set of page table entries (PTEs) used to map a virtual address to a physical address of a tile.” *See* NVIDIA Cover Pleading at 236-237 (citing *Shebanow*).

NVIDIA next asserts that “The references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 238. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “a method of allocating memory to a memory operation” and “mapping the memory operation to one of a plurality of memory heaps,” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved. *See, e.g.*, NVIDIA Cover Pleading at 238-239 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA next asserts that a POSITA “reading [the first group of references] would have known to look to references such as [the second group of references] that describe well-known techniques for mapping virtual memory to physical memory in computer systems,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 239-240. Rather than disclosing any contentions for why a POSITA would have known to look to the other references, NVIDIA provides only bare citation to *Motohashi* and *Case*, and does not demonstrate that the references support the proposition that a POSITA would have known to look to the other references.

Moreover, NVIDIA is incorrect that a POSITA would have been motivated to combine any reference that describes memory allocation with any reference that generally describes memory mapping. A POSITA would have understood that allocating memory can be done without the use of mapping virtual memory to physical memory, let alone without resulting at the claimed invention. Indeed, implementing memory mapping in a computer system can result in significant drawbacks, such as potential performance decreases, increased complexity of memory operations, and increased hardware requirements. As such, and particularly absent an analysis of the specific details of any specific references, NVIDIA has not met its burden of showing a motivation to combine any two of the identified references.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA's allegation that the implementing each combination would only require "routine engineering practices" is wholly conclusory. NVIDIA Cover Pleading at 240. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention. In addition, as explained below, NVIDIA fails to show that a POSITA would have been motivated to combine any of the proposed combinations of concepts.

2. No Motivation to Combine "a method of allocating memory to a memory operation" with "having the memory operation reference a shared memory address (SMA) in a shared memory"

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550 U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive

at the claimed subject matter. *See* NVIDIA Cover Pleading at 241. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art would have been motivated to combine (1) the teachings of any of the prior art references cited in these invalidity contentions (e.g., Sollich, Motohashi, Madhavarao, and/or Milos) that... describe a method of allocating memory to a memory operation... and (2) the teachings of any of the cited prior art references (e.g., Motohashi, Shebanow, Chen, Madhavarao, Vick, Wilt, Ni, Mohideen, Rogers, and/or Wallach) that... memory operations that reference a shared memory address (SMA) in a shared memory.” NVIDIA Cover Pleading at 241. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

a. NVIDIA Has Not Demonstrated How the Alleged Concepts of “a method of allocating memory to a memory operation” and “having the memory operation reference a shared memory address (SMA) in a shared memory” Relate to Specific Asserted Claims of the ’809 and ’019 Patents

NVIDIA has not demonstrated how the alleged concepts of “a method of allocating memory to a memory operation” and “having the memory operation reference a shared memory address (SMA) in a shared memory” relate to specific claims of the ’809 and ’019 Patents. For example, NVIDIA is overgeneralizing concepts from the ’809 and ’019 Patents, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual

requirements, and fails to meet Respondents' burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA's September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA Would be Motivated to Combine the Concepts of “a method of allocating memory to a memory operation” and “having the memory operation reference a shared memory address (SMA) in a shared memory”

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “a method of allocating memory to a memory operation” and “having the memory operation reference a shared memory address (SMA) in a shared memory.”

For example, NVIDIA asserts first that “computer engineers had understood that when allocating memory in multiprocessor computer systems that it is beneficial to have shared memory between the processors,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 242. Rather than disclosing any contentions for why this was allegedly well known, NVIDIA provides only bare citation to *Motohasi*, *Shebanow*, and *Wilt*, and does not demonstrate that the references disclose or render obvious this supposed well known understanding, let alone how or why that provides motivation to combine references describing the generalized concepts of “a method of allocating memory to a memory operation” and “having the memory operation

reference a shared memory address (SMA) in a shared memory,” or the actual requirements of the asserted claims. *See* NVIDIA Cover Pleading at 242.

NVIDIA next asserts that “The references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 243. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “a method of allocating memory to a memory operation” and “having the memory operation reference a shared memory address (SMA) in a shared memory,” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved. *See, e.g.*, NVIDIA Cover Pleading at 243-244 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA next asserts that a POSITA “reading [the first group of references] would have known to look to references such as [the second group of references] that describe memory shared between processors in a multiprocessor computer system,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 244. Rather than disclosing any contentions for why a POSITA would have known to look to the other references, NVIDIA provides only bare citation to *Mahdavar* and *Sollich*, and does not demonstrate that the references support the proposition that a POSITA would have known to look to the other references.

Moreover, NVIDIA is incorrect that a POSITA would have been motivated to combine

any reference that describes memory allocation with any reference that generally describes memory mapping. A POSITA would have understood that allocating memory can be done without having the memory operation reference a shared memory address (SMA) in a shared memory, let alone without resulting at the claimed invention. Indeed, implementing a shared memory model in a computer system can result in significant drawbacks, such as significant problems with memory allocation, including increased complexity and overhead in keeping data coherent and preventing multiple actors from accessing and modifying the same data simultaneously, as well as limited scalability, increased hardware requirements, and security vulnerabilities. As such, and particularly absent an analysis of the specific details of any specific references, NVIDIA has not met its burden of showing a motivation to combine any two of the identified references.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA's allegation that the implementing each combination would only require "routine engineering practices" is wholly conclusory. NVIDIA Cover Pleading at 244. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention. In addition, as explained below, NVIDIA fails to show that a POSITA would have been motivated to combine any of the proposed combinations of concepts.

3. No Motivation to Combine "mapping the memory operation to one of a plurality of memory heaps" with "applying different attributes to a mapped memory heap depending on the origination of the memory operation"

Even setting aside the impropriety of conducting the motivation to combine analysis on a generalized basis (*see, e.g., Axonics*, 73 F.4th at 957; *Volvo Penta*, 81 F.4th at 1209; *KSR*, 550

U.S. at 418; *Belden*, 805 F.3d at 1073), the NVIDIA Invalidity Contentions fail to prove that a POSITA would have been motivated to combine the identified references in such a way as to arrive at the claimed subject matter. *See* NVIDIA Cover Pleading at 245. “The proper inquiry is whether the relevant artisan would be motivated to make the combination to arrive at the claims’ actual limitations.” *Axonics, Inc. v. Medtronic, Inc.*, 73 F.4th 950, 957 (Fed. Cir. 2023) (“The inquiry is not whether a relevant artisan would combine a first reference’s feature with a second reference’s feature to meet requirements of the first reference that are not requirements of the claims at issue.”).

NVIDIA contends that “[a] person of ordinary skill in the art motivated to combine (1) the teachings of any of the prior art references cited in these invalidity contentions (e.g., Tong, Motohashi, Shebanaw, Blinzer, Minkin, Case, Wilt, Ni, AMD-IOMMU, Kegel, Mohideen, Rogers, Freimuth, and/or Intel ATS Art) that... describe mapping the memory operation to one of a plurality of memory heaps/virtual memory pools and (2) the teachings of any of the cited prior art references (e.g., Tong, Chen, AMD-IOMMU, Schuster, Rogers, Chinya, Wallach, Wyatt, and/or Ginzburg) that... describe applying/imparting different attributes to a mapped memory heap depending on the origination of the memory operation, such as the type of processor from which the memory operation originates.” NVIDIA Cover Pleading at 245. NVIDIA has not met its burden of showing a motivation to combine these references. For example, NVIDIA has not shown why those concepts are disclosed by the identified references, or (a) how those concepts relate to specific asserted claims, (b) any reason why a POSITA would be motivated to make that combination of concepts.

- a. **NVIDIA Has not Demonstrated How the Alleged Concepts of “mapping the memory operation to one of a plurality of memory heaps” and “applying different attributes to a mapped memory heap depending on the origination of the**

**memory operation” Relate to Specific Asserted Claims of the
'809 and '019 Patents**

NVIDIA has not demonstrated how the alleged concepts of “mapping the memory operation to one of a plurality of memory heaps” and “applying different attributes to a mapped memory heap depending on the origination of the memory operation relate to specific claims of the '809 and '019 Patents. For example, NVIDIA is overgeneralizing concepts from the '809 and '019 Patents, rewriting relevant claim language, and ignoring the claim requirements as a whole by conducting its analysis in this way. NVIDIA’s motivation to combine analysis is therefore untethered from the claims’ actual requirements, and fails to meet Respondents’ burden. By failing or electing to not include any mapping between the generalized concepts and specific claim language or claims, NVIDIA has failed to provide sufficient substantive assertions regarding the alleged motivation to combine. Because such mapping was not included in NVIDIA’s September 5 contentions, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

**b. NVIDIA Has Not Demonstrated Any Reason Why a POSITA
would be Motivated to Combine the Concepts of “mapping the
memory operation to one of a plurality of memory heaps” and
“applying different attributes to a mapped memory heap
depending on the origination of the memory operation”**

NVIDIA has not demonstrated any reason why a POSITA would be motivated to combine the concepts of “mapping the memory operation to one of a plurality of memory heaps” and “applying different attributes to a mapped memory heap depending on the origination of the

memory operation.”

NVIDIA asserts that “The references themselves provide a motivation to combine,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 246. For example, rather than disclosing any contentions for why the references allegedly provide the requisite motivation, NVIDIA provides only bare citation to the identified references, and does not demonstrate that how or why that provides motivation to combine references describing the generalized concepts of “mapping the memory operation to one of a plurality of memory heaps” and “applying different attributes to a mapped memory heap depending on the origination of the memory operation,” or the actual requirements of the asserted claims. Moreover, the citations to the identified references merely quote from the background sections of the respective references, which identify the problems that the references themselves purport to have solved. *See, e.g.*, NVIDIA Cover Pleading at 246-247 (citing references with parenthetical quotations). That the references purport to have solved these problems indicates that the problems are resolved, and does not provide a motivation to combine, but rather suggests that the problem (and therefore alleged motivation) no longer exist thanks to the disclosures of the references as individuals, rather than in combination.

NVIDIA next asserts that a POSITA “reading [the first group of references] would have known to look to references such as [the second group of references] that describe applying different attributes to a mapped memory heap depending on the origination of the memory operation,” but provides no analysis or explanation of that assertion. NVIDIA Cover Pleading at 247. Rather than disclosing any contentions for why a POSITA would have known to look to the other references, NVIDIA provides only bare citation to *Wyatt* and *Schuster*, and does not demonstrate that the references support the proposition that a POSITA would have known to look to the other references.

Moreover, NVIDIA is incorrect that a POSITA would have been motivated to combine any reference that generally describes memory mapping with any that describes applying different attributes to a mapped memory heap depending on the origination of the memory operation. A POSITA would have understood that a computer system may implement memory mapping techniques even if all memory operations originate from the same place. Thus, even if a reference described mapping a memory operation, that alone would not be a sufficient rationale to combine with another reference allegedly describing “applying different attributes to a mapped memory heap depending on the origination of the memory operation.” Indeed, implementing a memory model that performs mapping of memory operations to memory heaps and applies different attributes to a mapped memory heap depending on the origination of the memory operation can result in significant drawbacks, such as significant problems with memory allocation, including increased complexity and overhead in tracking the origination of the memory operation and the attributes to apply as a result, keeping data coherent and preventing multiple actors from accessing the same memory heap simultaneously, as well as limited scalability and increased hardware requirements. As such, and particularly absent an analysis of the specific details of any specific references, NVIDIA has not met its burden of showing a motivation to combine any two of the identified references.

The NVIDIA Invalidity Contentions also fail to demonstrate that a POSITA would have had a reasonable expectation of success in combining the references to arrive at the claimed invention. For example, NVIDIA’s allegation that the implementing each combination would only require “routine engineering practices” is wholly conclusory. NVIDIA Cover Pleading at 248. NVIDIA provides no explanation for how any particular combination of references (or combination of concepts) could be implemented, much less that such implementation would require only routine engineering practices, or would result in the claimed invention. In addition,

as explained below, NVIDIA fails to show that a POSITA would have been motivated to combine any of the proposed combinations of concepts.

V. Objective Indicia of Non-Obviousness

In addition to the presumption of validity, and the NVIDIA Invalidity Contentions' failure to prove that the NVIDIA Asserted Patents are obvious, objective indicia of non-obviousness (sometimes referred to as secondary considerations) demonstrate that the NVIDIA Asserted Patents are not obvious. *See e.g., Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1354-55 (Fed. Cir. 2013) ("As a safeguard against slipping into use of hindsight and to resist the temptation to read into the prior art the teachings of the invention in issue, we have required courts to consider evidence of the objective indicia of nonobviousness prior to making the ultimate determination of whether an invention is obvious" and "all evidence pertaining to the objective indicia of nonobviousness must be considered before reaching an obviousness conclusion."). "Objective evidence of nonobviousness includes: (1) commercial success, (2) copying, (3) industry praise, (4) skepticism, (5) long-felt but unsolved need, and (6) failure of others." *Volvo Penta of the Ams., LLC v. Brunswick Corp.*, 81 F.4th 1202, 1212 (Fed. Cir. 2023); *see also Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 17 (1966). "Indeed, evidence of secondary considerations may often be the most probative and cogent evidence in the record. It may often establish that an invention appearing to have been obvious in light of the prior art was not. It is to be considered as part of all the evidence, not just when the decisionmaker remains in doubt after reviewing the art." *Stratoflex, Inc. v. Aeroquip Corp.*, 713 F.2d 1530, 1538-39 (Fed. Cir. 1983).

A. Nexus

Objective indicia demonstrate that the NVIDIA Asserted Patents are nonobvious, and there is a nexus between the claims of each NVIDIA Asserted Patent.

A showing of nexus can be made in two ways: (1) via a presumption of nexus, or (2) via a showing that the evidence is a direct result of the unique characteristics of the claimed invention. A patent owner is entitled to a presumption of nexus when it shows that the asserted objective evidence is tied to a specific product that embodies the claimed features, and is coextensive with them. When a nexus is presumed, the burden shifts to the party asserting obviousness to present evidence to rebut the presumed nexus. The inclusion of noncritical features does not defeat a finding of a presumption of nexus. However, even absent a presumption of nexus, the patent owner is still afforded an opportunity to prove nexus by showing that the evidence of secondary considerations is the 'direct result of the unique characteristics of the claimed invention.

Volvo Penta of the Ams., LLC v. Brunswick Corp., 81 F.4th 1202, 1210 (Fed. Cir. 2023).

1. The '943 Patent Has a Nexus to the Objective Indicia

Onesta is entitled to a presumption of nexus between the objective indicia and the '943 Patent, because the Accused Products and Domestic Industry Products, as defined in Onesta's Initial Infringement Contentions, embody the claimed features and are coextensive with them. Additionally, as set forth below with respect to each of the objective indicia, the evidence is a direct result of the unique characteristics of the claimed invention, and therefore, even absent a presumption of nexus, a nexus still exists.

'943 Patent Claim 1 and claims depending therefrom. For example, the Accused Products and Domestic Industry Products are designed for use in and/or are used in a system with a CPU. *See e.g.*, Complainant Onesta IP, LLC's Initial Infringement And Domestic Industry Technical Prong Contentions; *id.* at Ex. 05, at 1-9. Further, the Accused Products and Domestic Industry Products perform (literally and under the Doctrine of Equivalents) a method comprising "creating, at a central processing unit (CPU), a plurality of virtual devices, each of the virtual devices abstracting a graphics processing unit (GPU) to create a virtual GPU within the CPU, wherein each of the plurality of virtual devices is associated with a respective." *Id.* at 10-34. Additionally, the Accused Products and Domestic Industry Products perform (literally and under the Doctrine of

Equivalents) the method comprising “receiving a first command in a queue of a first virtual device of the plurality of virtual devices, wherein a priority associated with the first command matches a priority associated with the first virtual device.” *Id.* at 35-52. Further, the Accused Products and Domestic Industry Products perform (literally and under the Doctrine of Equivalents) the method comprising “sending the first command from the first virtual device in the CPU to a GPU.” *Id.* at 53-65. The Accused Products and Domestic Industry Products also perform (literally and under the Doctrine of Equivalents) the method comprising “executing, at the GPU, the first command.” *Id.* at 66-96. Thus, there is a nexus between, *e.g.*, claim 1 of the ’943 Patent and the Accused products and Domestic Industry Products. There is also a nexus between claims 2-9 and the Accused products and Domestic Industry Products, as outlined in Onesta’s Initial Invalidity Contentions. *Id.* at 97-179.

’943 Patent Claim 11 and claims depending therefrom. For example, the Accused Products and Domestic Industry Products are “a processing device.” *See e.g.*, Complainant Onesta IP, LLC’s Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 05, at 180-194. Further, the Accused Products include (literally and under the Doctrine of Equivalents), “a set of queues, each queue of the set of queues being configured to hold commands received from a central processing unit (CPU), wherein each command is sent from a virtual device in the CPU.” *Id.* at 195-257. Further, the Accused Products include (literally and under the Doctrine of Equivalents), “a command processor configure[d] to retrieve the received commands from the set of queues, wherein the set of queues includes a high priority queue that holds high priority commands, wherein the command processor is configured to retrieve a high priority command held in the high priority queue before retrieving commands held in other queues of the set of queues, and wherein the processing device is configured to execute[] the received commands.” *Id.* at 258-315. The Accused Products also include (literally

and under the Doctrine of Equivalents), “a processing core configured to execute the received command, wherein the command processor is configured to retrieve commands from the set of queues and send the retrieved commands to the processing core for execution.” *Id.* at 316-352. There is also a nexus between claims 12 and 14-18 and the Accused Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 353-416. There is further a nexus between claims 19-24 of the ’943 Patent and the Accused Products and Domestic Industry Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 417-469.

Onesta is therefore entitled to a presumption of a nexus between the objective indicia and the ’943 Patent.

2. The ’803 Patent Has a Nexus to the Objective Indicia

For example, Onesta is entitled to a presumption of nexus between the objective indicia and the ’803 Patent, because the Accused Products and Domestic Industry Products, as defined in Onesta’s Initial Infringement Contentions, embody the claimed features and are coextensive with them. Additionally, as set forth below with respect to each of the objective indicia, the evidence is a direct result of the unique characteristics of the claimed invention, and therefore, even absent a presumption of nexus, a nexus still exists.

’803 Patent Claim 1 and claims depending therefrom. For example, the Accused Products and Domestic Industry Products, as defined in Complainants’ Initial Infringement Contentions, include (literally and under the Doctrine of Equivalents), “a system.” *See e.g.*, Complainant Onesta IP, LLC’s Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 08, at 1-4. Further, the Accused Products and Domestic Industry Products include (literally and under the Doctrine of Equivalents), “a central processing unit (CPU) communicably coupled to a first graphics processing unit (GPU) chiplet of a GPU chiplet array, wherein the GPU chiplet array includes: the first GPU chiplet communicably coupled

to the CPU via a bus.” *Id.* at 5-19. The Accused Products and Domestic Industry Products further include (literally and under the Doctrine of Equivalents), “a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink, wherein the passive crosslink is dedicated for inter-chiplet communications.” *Id.* at 20-48. There is also a nexus between claims 2-3 and 7-10 and the Accused Products and Domestic Industry Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 49-82.

3. The ’809 Patent and ’019 Patent Have a Nexus to the Objective Indicia

Onesta is entitled to a presumption of nexus between the objective indicia and the ’809 Patent, because the Accused Products and Domestic Industry Products, as defined in Onesta’s Initial Infringement Contentions, embody the claimed features and are coextensive with them. Additionally, as set forth below with respect to each of the objective indicia, the evidence is a direct result of the unique characteristics of the claimed invention, and therefore, even absent a presumption of nexus, a nexus still exists.

’809 Patent Claim 1 and claims depending therefrom. For example, the Accused Products and Domestic Industry Products, as defined in Complainants’ Initial Infringement Contentions, perform (literally and under the Doctrine of Equivalents), “a method of allocating memory to a memory operation executed by a processor in a computer arrangement having a first processor configured for unified operation with a second processor.” *See e.g.*, Complainant Onesta IP, LLC’s Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 12, at 1-7. Further, the Accused Products and Domestic Industry Products perform (literally and under the Doctrine of Equivalents) the method comprising “receiving a memory operation from a processor.” *Id.* at 8-18. Additionally, the Accused Products and Domestic Industry Products perform (literally and under the Doctrine of Equivalents) the method

comprising “mapping the memory operation to one of a plurality of memory heaps, wherein the memory operation references a shared memory address (SMA) in a shared memory, and wherein the mapping includes mapping the memory operation to one of a plurality of memory heaps based on the SMA, wherein the mapping produces a mapping result.” *Id.* at 19-60. The Accused Products and Domestic Industry Products also perform (literally and under the Doctrine of Equivalents) the method comprising “providing the mapping result to the processor.” *Id.* at 61-67. There is also a nexus between claims 2-11 and the Accused Products and Domestic Industry Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 68-86.

’809 Patent Claim 12 and claims dependent therefrom. With respect to the ’809 Patent, the Accused Products, as defined in Onesta’s Initial Infringement Contentions, include (literally or under the Doctrine of Equivalents), “A system including a first processor memory resource and a second processor memory resource, the system being configured for providing memory to a memory operation executed by a processor.” *See e.g.*, Complainant Onesta IP, LLC’s Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 12, at 87-95. Further, the Accused Products include (literally or under the Doctrine of Equivalents), “a plurality of memory heaps, each being configured to access one of the memory resources.” *Id.* at 96-105. Further, the Accused Products include (literally or under the Doctrine of Equivalents), “a mapper configured to: receive an address reference from the memory operation, and mapping the memory operation to one of the plurality of memory heaps based on the address reference, wherein different attributes are applied to a mapped memory heap depending upon origination of the memory operation.” *Id.* at 106-145. There is also a nexus between claims 13-14 and 16-19 and the Accused Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 156-146.

’809 Patent Claim 20 and claims dependent therefrom. With respect to the ’809 Patent,

the Accused Products, as defined in Onesta's Initial Infringement Contentions, include (literally or under the Doctrine of Equivalents), "A computer-readable medium having instructions stored thereon that, when executed by a computing device including a first processor configured for unified operation with a second processor cause the computing device to perform a method." Further, the Accused Products include (literally or under the Doctrine of Equivalents), "receiving a memory operation from a processor, wherein the memory operation references a shared memory address (SMA) in a shared memory." Further, the Accused Products include (literally or under the Doctrine of Equivalents), "mapping the memory operation to one of a plurality of memory heaps, wherein the mapping includes mapping the memory operation to one of a plurality of memory heaps based on the SMA, and wherein the mapping produces a mapping result." Further, the Accused Products include (literally or under the Doctrine of Equivalents), "providing the mapping result to the processor."

There is further a nexus between claims 22-25 of the '809 Patent and the Accused Products, as outlined in Onesta's Initial Infringement Contentions. *Id.* at 157-171.

'019 Patent Claim 1 and claims dependent therefrom. With respect to the '019 Patent, the Accused Products, as defined in Onesta's Initial Infringement Contentions, include (literally or under the Doctrine of Equivalents), "a method for allocating memory in a computer system having a plurality of processors." *See e.g.*, Complainant Onesta IP, LLC's Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 15, at 1-7. Further, the Accused Products perform (literally or under the Doctrine of Equivalents) the method comprising "receiving a memory operation from a processor that references an address in a shared memory." *Id.* at 8-18. Additionally, the Accused Products perform (literally or under the Doctrine of Equivalents) the method comprising "mapping the received memory operation to at least one virtual memory pool to produce a mapping result, wherein the at least one virtual memory

pool is associated with at least one memory resource.” *Id.* at 19-58. The Accused Products also perform (literally or under the Doctrine of Equivalents) the method comprising “providing the mapping result to the processor.” *Id.* at 59-62. Thus, there is a nexus between claim 1 of the ’019 Patent and the Accused Products. There is also a nexus between claims 2-10 and the Accused Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 66-82.

’019 Patent Claim 11 and claims dependent therefrom. With respect to the ’019 Patent, the Accused Products, as defined in Onesta’s Initial Infringement Contentions, include (literally or under the Doctrine of Equivalents), “a computer system.” *See e.g.*, Complainant Onesta IP, LLC’s Initial Infringement And Domestic Industry Technical Prong Contentions Cover Document and the associated Exhibit 15, at 83-89. Further, the Accused Products include (literally or under the Doctrine of Equivalents), “a plurality of processors.” *Id.* at 90-95. Further, the Accused Products include (literally or under the Doctrine of Equivalents), “a shared memory.” *Id.* at 96-101. The Accused Products also include (literally or under the Doctrine of Equivalents), “a mapper, wherein the mapper is configured to: receive a memory operation from a processor that references an address in the shared memory; map the received memory operation to at least one virtual memory pool to produce a mapping result, wherein the at least one virtual memory pool is associated with at least one memory resource; and provide the mapping result to the processor.” *Id.* at 96-134. Thus, there is a nexus between claim 11 of the ’019 Patent and the Accused Products. There is also a nexus between claims 12-20 and the Accused Products, as outlined in Onesta’s Initial Infringement Contentions. *Id.* at 135-143.

B. Copying

As outlined in the Complaint and Onesta’s Initial Infringement Contentions, the Accused Products copy the inventions claimed by the NVIDIA Asserted Patents and embodied by the Domestic Industry Products. *See* Complaint; *see also* Onesta’s Initial Infringement Contentions at

Exhibits 02, 05, 08, 12, and 15. The copying is a direct result of the unique characteristics of the inventions claimed by the NVIDIA Asserted Patents.

For example, the '803 Patent is directed to computer systems and methods of using the same including a GPU chiplet array in which, *inter alia*, a passive crosslink dedicated for inter-chiplet communications communicably couples a first GPU chiplet with a second GPU chiplet. This “improve[d] system performance by using GPU chiplets while preserving the current programming model,” because the recited “systems and methods []utilize high bandwidth passive crosslinks for coupling GPU chiplets.” '803 Patent at 2:1-4.

The NVIDIA products accused of infringing the '803 Patent copied the claimed GPU chiplet array as embodied in the AMD Domestic Industry Products, and did so as a direct result of the unique characteristics of the claimed invention. For example, although “AMD and Nvidia have pursued divergent chip design strategies for many years,” following the Domestic Industry products’ use of the claimed invention, NVIDIA suddenly “switched tactics and adopt a chiplet design.” Onesta-ITC1450_0074250 (<https://www.extremetech.com/computing/nvidia-is-allegedly-planning-to-use-chiplets-for-next-gen-blackwell-gpus>.) “AMD is already using chiplets for AI acceleration with its upcoming MI300 super chip, so [] Nvidia could be taking a page from its rival.” *Id.* NVIDIA’s switch to using the claimed invention was the “most radical shakeup in Nvidia’s product line in recent memory,” and “mean[s] Nvidia [wa]s about to embark on a wildly different course.” *Id.* As reported, NVIDIA’s GPUs were large in physical size, “which can reduce yields and is also pushing the boundaries of what's reasonable to manufacture without defects,” but AMD’s products embodying the invention of the '803 Patent were less than “half that size.” *Id.* The use of “a chiplet design, ... [was] quickly becoming a necessary [strategy]” because of its clear benefits. *Id.* Commenters noted that NVIDIA’s switch to GPU chiplet use was beneficial “so long as [interconnect] speeds between chiplets are sufficiently fast,” one of the benefits of the

claimed invention. *Id.* “Nvidia’s adoption of chiplet technology follows a broader industry trend where leading semiconductor companies, including AMD and Intel, have already integrated similar designs into their processors.” <https://www.digitaltrends.com/computing/tsmc-to-make-chips-for-nvidia-rubin/>. Even in 2020, it was reported that although AMD was moving toward its GPU chiplet design, “Does NVIDIA have this tech? Not yet.” Onesta-ITC1450_0074008 (<https://www.tweaktown.com/news/74274/amds-next-gen-rdna-3-revolutionary-chiplet-design-could-crush-nvidia/index.html>).

Other products also copied the AMD Domestic Industry products, which embody the claimed invention. For example, Intel took a “bold step forward in the world of graphics processing” with “a disaggregated GPU design,” which “fuels an ongoing rivalry with AMD, which has been a strong proponent of chiplet designs.” Onesta-ITC1450_0074031 (<https://techovedas.com/intels-disaggregated-gpu-patent-marks-a-shift-to-chiplet-architecture-boosting-efficiency-and-sparking-competition-with-amd/>). Intel’s design was referred to as “potentially incorporating learnings from AMD’s experience.” *Id.* For example, “[b]uilding a multi-chiplet GPU requires advanced manufacturing techniques and efficient interconnect solutions,” one of the main features of the claimed invention of the ’803 Patent. *Id.* “Building a multi-chiplet GPU is no small feat. One of the critical challenges Intel faces in making disaggregated GPUs a reality is developing robust interconnect technology.” *Id.* “AMD’s EPYC processors, which use chiplet architecture, demonstrate the importance of advanced interconnect technology. For AMD, technologies like Infinity Fabric provide the necessary bandwidth and data-sharing capabilities between chiplets.” *Id.*

C. Industry Praise

The inventions claimed by the NVIDIA Asserted Patents received industry praise when they became available.

'803 Patent

One of the technologies at the heart of the '803 Patent, the use of GPU chiplets with passive interconnects, was the subject of significant industry praise when it was announced. For example, it was reported in 2020 that “AMD is currently in the early design phase of the RDNA 3 architecture, and it could represent the most radical change of GPU design ever. AMD could shift towards using a chiplet design for its RDNA 3 architecture.” Onesta-ITC1450_0074008 (<https://www.tweaktown.com/news/74274/amds-next-gen-rdna-3-revolutionary-chiplet-design-could-crush-nvidia/index.html>). As a result of incorporating AMD's chiplet technology (the same as the '803 Patent), the industry had “the following answer to the question is Big Navi an NVIDIA Killer: f*ck yeah.” <https://www.tweaktown.com/news/74274/amds-next-gen-rdna-3-revolutionary-chiplet-design-could-crush-nvidia/index.html>.

'809 and '109 Patents

As set forth in Onesta's Initial Infringement Contentions, OpenCL 2.0 implements shared virtual memory that meets the claims of the '809 and '019 Patents. Khronos, an industry consortium of over 180 entities, including, e.g., Qualcomm, NVIDIA, AMD, and more, announced OpenCL 2.0 in 2013. Onesta-ITC1450_0074281 (<https://www.khronos.org/about/>); Onesta-ITC1450_0074248 (<https://www.techpowerup.com/187620/khronos-releases-opencl-2-0-specification>). In the OpenCL 2.0 specification, Khronos (and therefore by extension all 170 composite entities, including, e.g., Qualcomm, NVIDIA, AMD, and more) explained that “SVM allows the host and kernels executing on devices to directly share complex, pointer-containing data structures such as trees and linked lists. It also eliminates the need to marshal data between the host and devices. As a result, SVM substantially simplifies OpenCL programming and may improve performance.” Onesta-ITC1450_0074043 (<https://registry.khronos.org/OpenCL/specs/opencl-2.0.pdf>).

D. Long Felt But Unsolved Need

The NVIDIA Asserted Patents solved long-felt but unresolved needs in the fields of computer graphics, inter-chiplets integration and communication, and unified memory operation.

For example, the inventors of the '943 Patent recognized that conventional systems do not allow non-graphics commands, such as computational/AI commands, to be sent to the GPU for execution because the CPU needs results from these commands relatively quickly but the latency incurred by sending computational commands to the GPU may be too high. '943 Patent at 1:27-35. But keeping the computational commands at the CPU for execution adds to the processing burden of the CPU and can hamper the system performance. *Id.* at 1:36-40. Therefore, allowing different types of commands to be executed in a desired order to reduce the latency of processing the relatively high priority commands was a long felt and unresolved need in the industry. *Id.* at 40-44; *see also Id.* at 1:48-53. The '943 Patent addressed this problem by disclosing a method and system as recited in claims 1-9, 11-12, and 14-24 of the '943 Patent. *Id.* at 10:23-12:43. For example, the '943 Patent allows virtual devices with queues taking commands with different priorities from the user mode driver so that higher priority commands wait a shorter time before being sent to GPU for execution. *Id.* at 4:14-5:8; 8:12-54. Further, different types of commands are received at the GPU by priority-based command queues so that the command processor can prioritize retrieving commands from the high priority queue and send them to the processing core for execution. *Id.* at 5:21-6:32; 8:49-9:37. Thus, the solving of a long felt but unmet need was a direct result of the unique characteristics of the inventions claimed by the '943 Patent.

Further, the inventors of the '803 Patent recognized that it is conventionally difficult and expensive to integrate GPU chiplets due to the requirements of synchronized communication of parallel work on multiple threads and coherence view of the memory of shared resources throughout the system. '803 Patent at 1:45-61. Further, different applications are written with the

view that the system only has a single GPU. *Id.* at 1:62-67. Therefore, it was a long felt and unresolved need in the industry to integrate GPU chiplets with CPUs using efficient inter-chiplet communication, addressing the GPU chiplets as a single device from the CPU's point of view. The '803 Patent disclosed a system comprising a CPU communicably coupled to a first GPU chiplet of a GPU chiplet array via a bus, and a second GPU chiplet communicably coupled to the first GPU chiplet via a passive crosslink dedicated for inter-chiplet communications. *Id.* at 2:1-17. For example, a passive die interposer deploys multiple inter-connected GPU chiplets to make the multiple GPU chiplets array appear as a monolithic GPU device from a programmer model/developer perspective. *Id.* at 8:38-42. The GPU chiplets can also maintain cache coherency using the scalable data fabric of one GPU chiplet to access the lower level cache(s) on other GPU chiplets in nearly the same time as to access the lower level cache on its same chiplet. *Id.* at 8:42-48. This low-latency, inter-chiplet cache coherency in turn enables the chiplet-based system to operate as a monolithic GPU from the software developer's perspective, and thus avoids chiplet-specific considerations on the part of a programmer or developer. *Id.* at 8:48-52. Thus, the solving of a long felt but unmet need was a direct result of the unique characteristics of the inventions claimed by the '803 Patent.

The inventors of the '809 Patent and '019 Patent recognized that in conventional systems, memory is separated between distinct address spaces, and heterogeneous processors do not share unified access to a single address space. '809 Patent at 1:58-62; '019 Patent at 2:6-10. Therefore, it was a long felt and unresolved need in the industry for a memory configured to operate in a multi-processor computing system environment that frees the programmer from these constraints, *e.g.*, by providing a region of memory allocated from a single memory space with common access and storage properties. '809 Patent at 1:66-2:4; '019 Patent at 2:15-20. The '809 and '019 Patents introduce a way of mapping multiple heterogeneous components to a single, shared virtual address

space, freeing the programmer to implement faster methods of data transfer, more efficient use of memory, and other performance benefits. '809 Patent at 10:35-48, FIGs. 2, 4A-4E; '019 Patent at 10:61-11:7, FIGs. 2, 4A-4E. Thus, the solving of a long felt but unmet need was a direct result of the unique characteristics of the inventions claimed by the '809 Patent. For example, the problem addressed by the '809 and '019 Patents was well known and long felt: "The problem of data migration between GPU and CPU memory spaces is well-recognized by the developers of CUDA-like frameworks. CUDA, for example, supports mechanisms such as asynchronous buffer copy, CUDA streams (a generalization of the latter), pinning and memory mapping of memory buffers to help tolerate latency by overlapping computation and communication." Onesta-ITC1450_0074276 (https://www.usenix.org/legacy/event/hotos/tech/final_files/Rossbach.pdf) (Published May 9, 2011, *see* Onesta-ITC1450_0074272 (<https://dl.acm.org/doi/10.5555/1991596.1991639>)). The identified problem of memory allocation between CPUs and GPUs was unsolved:

AMD's Fusion integrates the CPU and GPU onto a single die, however, it leaves CPU and GPU memory partitioned. Intel's Sandy Bridge, another CPU/GPU combination, indicates that the coming years will see various forms of integrated CPU/GPU hardware coming to market. New hybrid systems, e.g., NVIDIA Optimus, with both power-efficient on-die and high-performance discrete graphics cards, make data management explicit even with combined CPU/GPU chips. But even a completely integrated virtual memory system requires system support for minimizing data copies.

Id. (https://www.usenix.org/legacy/event/hotos/tech/final_files/Rossbach.pdf). The technology claimed by the '809 and '019 Patents was revolutionary: "Your pointers will address the same memory, so you don't need to do a ton of copying over the bus like you do now to send any kind of instructions to the GPU." *See* Onesta-ITC1450_0074028. The technology allowed the CPU and GPU to operate on more equal terms, which allows software to access more performance.

Id.

Accordingly, the NVIDIA Asserted Patents each addressed long felt needs that were unresolved, and there is objective evidence of non-obviousness of the claims of the NVIDIA Asserted Patents.

E. Commercial Success

The products embodying the inventions claimed by the NVIDIA Asserted Patents (including the Accused Products, Domestic Industry Products, and more) have experienced immense commercial success. For example, the Accused Products and Domestic Industry Products which all incorporate the Asserted Claims of the NVIDIA Asserted Patents have resulted in billions of dollars in sales in the United States alone. Respondent NVIDIA manufactures and sells the computer devices and systems which are incorporated into all of the Accused Products. As another example, according to Qualcomm's 10-K, in 2024, over \$24 billion revenue came from "handsets." *See* Complaint Exhibit 30 (Qualcomm 2024 10-K), Report of Independent Registered Public Accounting Firm at 16. Qualcomm's handset chips are products that embody the inventions claimed by the '943 Patent and the '809 Patent, as set forth in Onesta's infringement contentions. As another example, as set forth in Onesta's contentions with respect to the domestic industry economic prong, AMD's revenue associated with the domestic industry products is significant. AMD's Domestic Industry Products embody the inventions claimed by the '943 Patent, the '803 Patent, and the '809 Patent, as set forth in Onesta's Domestic Industry Contentions. The commercial success of these products is a direct result of the unique characteristics of the inventions claimed by the NVIDIA Asserted Patents, for example as set forth in Onesta's Initial Infringement Contentions.

VI. Other Invalidity Grounds

The NVIDIA Invalidity Contentions have not met Respondents burden of proving invalidity of any claim under 35 U.S.C. § 112. Each of the asserted NVIDIA Asserted Patent claims

contains sufficient written description and enablement under 35 U.S.C. § 112 ¶ 1 and definiteness under 35 U.S.C. § 112 ¶ 2.

As a threshold matter, for *each* identified term in the claims of the NVIDIA Asserted Patents, the NVIDIA Invalidity Contentions improperly recite unfounded enablement and written description allegations by repeating boilerplate statements that “the claims are invalid for lack of enablement and lack of written description: the patent fails to teach those skilled in the art how to make and use the full scope of the claimed features and fails to disclose an invention understandable to a skilled artisan or show that the inventor actually invented the alleged invention claimed.” *See* NVIDIA Cover Pleading at Section IX (“INVALIDITY BASED ON 35 U.S.C. § 112”), Subsections D.2. (“The ’803 Patent”) and Subsection D.3. (“The ’809 and ’019 Patents”), at 266-270. Additionally, such boilerplate language fails to satisfy Respondents’ burden and does not place Onesta on notice of any specific allegations. For example, the NVIDIA Invalidity Contentions do not provide any specific allegations in connection with at least alleged undue experimentation or any of the *Wands* factors. Nor have NVIDIA’s Invalidity Contentions provided any rationale as to why or how the written descriptions of the NVIDIA Asserted Patents are inadequate for a POSITA to understand the invention. Rather, NVIDIA’s Invalidity contentions amount to nothing more than conclusory, baseless, and repetitive statements for *each* identified term. At least for this reason and the additional reasons set forth below, each of these contentions lack merit.

A. Enablement Under 35 U.S.C. § 112 ¶ 1

NVIDIA’s allegations that the asserted claims are invalid for lack of enablement under 35 U.S.C. § 112 ¶ 1 are baseless and do not establish the required clear and convincing evidence of lack of enablement for any of the challenged claims. “[T]o be enabling, the specification of a patent must teach those skilled in the art how to make and use the full scope of the claimed invention

without ‘undue experimentation.’” *In re Wright*, 999 F.2d 1557, 1561 (Fed. Cir. 1993). However, “a patent need not disclose what is well known in the art.” *In re Wands*, 858 F.2d 731, 735 (Fed. Cir. 1988). “Enablement is not precluded by the necessity for some experimentation such as routing screening.” *Id.* at 737.

“The determination of what constitutes undue experimentation in a given case requires the application of a standard of reasonableness, having due regard for the nature of the invention and the state of the art. *In re Wands*, 858 F.2d at 737 (citing *Ansul Co. v. Uniroyal, Inc.*, 448 F.2d 872, 878-79 (2d. Cir. 1971), cert. denied, 404 U.S. 1018 (1972)). The Federal Circuit applies the following factors in determining whether a disclosure requires undue experimentation: (1) the quantity of experimentation necessary, (2) the amount of direction or guidance presented, (3) the presence or absence of working examples, (4) the nature of the invention, (5) the state of the prior art, (6) the relative skill of those in the art, (7) the predictability or unpredictability of the art, and (8) the breadth of the claims. *Id.* at 737 (citing *In re Forman*, 230 USPQ 546 (BPAI 1986)).

NVIDIA’s Invalidity Contentions have failed to satisfy their burden and have not placed Onesta on notice of any specific allegations in connection with undue experimentation or any of the *Wands* factors. Rather, NVIDIA’s Invalidity contentions amount to nothing more than conclusory statements that the claims are not enabled.

B. Written Description Under 35 U.S.C. § 112 ¶ 1

NVIDIA’s allegations that the asserted claims are invalid for lack of written description under 35 U.S.C. § 112 ¶ 1 are baseless and do not establish the required clear and convincing evidence of lack of written description. A patent must include a specification containing “a written description of the invention, and of the manner and process of making and using it.” 35 U.S.C. § 112 ¶ 1. “To fulfill the written description requirement, a patent specification must describe an invention and do so in sufficient detail that one skilled in the art can clearly conclude that ‘the

inventor invented the claimed invention.” *Regents of the Univ. of Cal. v. Eli Lilly & Co.*, 119 F.3d 1559, 1566 (Fed. Cir. 1997) (citing *Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572 (1997)). “[A]n applicant complies with the written description requirement ‘by describing the invention, with all its claimed limitations, not that which makes it obvious,’ and by using ‘such descriptive means as words, structures, figures, diagrams, formulas, etc., that set forth the claimed invention.” *Regents of the Univ. of Cal.*, 119 F.3d at 1566 (quoting *Lockwood*, 107 F.3d at 1572). “[T]he test for sufficiency is whether the disclosure of the application relied upon reasonably conveys to those skilled in the art that the inventor had possession of the claimed subject matter as of the filing date.” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010).

“When determining whether a specification contains adequate written description, one must make an ‘objective inquiry into the four corners of the specification from the perspective of a person of ordinary skill in the art.’” *Ariad Pharms., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010) (en banc). “Because the specification is viewed from the perspective of one of skill, in some circumstances, a patentee may rely on information that is ‘well-known in the art’ for purposes of meeting the written description requirement.” *See Bos. Sci. Cor. v. Johnson & Johnson*, 647 F.3d 1353, 1366 (Fed. Cir. 2011) (citing *Falko Gunter Falkner v. Inglis*, 448 F.3d 1357, 1366-68 (Fed. Cir. 2006)). “What is required to meet the written description requirement ‘varies with the nature and scope of the invention at issue, and with the scientific and technologic knowledge already in existence.’” *Bos. Sci. Cor.*, 647 F.3d at 1363 (citing *Capon v. Eshhar*, 418 F.3d 1349, 1357 (Fed. Cir. 2005)).

C. Definiteness Under 35 U.S.C. § 112 ¶ 2 and ¶ 6

The Asserted Claims of the NVIDIA Asserted Patents are definite in accordance with 35 U.S.C. §§ 112 ¶ 2 and ¶ 6. Patents must include claims “particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.” 35

U.S.C. § 112 ¶ 2. A “patent is invalid for indefiniteness if its claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention.” *Nautilus, Inc. v. Biosig Instruments, Inc.*, 572 U.S. 898 (2014). However, to satisfy the definiteness requirement, “numerical precision is not always required.” *Ironburg Inventions Ltd. v. Valve Corp.*, 64 F.4th 1274, 1285 (Fed. Cir. 2023).

Onesta reserves the right to respond to any supplemental invalidity contentions on the grounds of invalidity based upon indefiniteness put forward by NVIDIA.

D. Rebuttals to NVIDIA’s Section 112 Contentions

1. The ’803 Patent

The NVIDIA Invalidity Contentions baldly allege that claims 8 and 9 of the ’803 Patent “are invalid for lack of written description support and lack of enablement” because they recite “a first level of the first cache memory hierarchy is coherent within the first GPU chiplet,” and “a first level of the second cache memory hierarchy is coherent within the second GPU chiplet.” NVIDIA Cover Pleading at 265-266. NVIDIA’s arguments fail, including because they are unfounded and highly conclusory. The NVIDIA Invalidity Contentions assert the ’803 Patent allegedly “fails to describe or enable a ‘first level’ cache that is coherent within each chiplet.” NVIDIA Cover Pleading at 265-266. However, other than merely conclusorily asserting that “[t]he patent fails to” meet NVIDIA’s (incorrect) reading of the standards for enablement and written description, the NVIDIA Invalidity Contentions do not provide any explanation or justification for its contention. The NVIDIA Invalidity Contentions do not even attempt to explain why the disclosures individually, or as a whole, do or do not demonstrate that the inventors were in possession of “a first level of the first cache memory hierarchy is coherent within the first GPU chiplet,” and “a first level of the second cache memory hierarchy is coherent within the second

GPU chiplet.” Nor does NVIDIA attempt to explain why the disclosure of the ’809 Patent would not be sufficient to inform a POSITA how to make or use the claimed invention. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts invalidity of claims 8 and 9 of the ’803 Patent for lack of written description and enablement, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

Additionally, contrary to NVIDIA’s bald assertion that the claims lack written description support and/or are not enabled, and to the extent that NVIDIA’s invalidity theories can be understood, the ’803 Patent demonstrates its validity.

The claim terms identified by NVIDIA are fully set forth in the patent specification, including as-filed in the original application, and the specification demonstrates that the inventors of the ’803 Patent were in possession of the claimed subject matter as of the filing date. For example, even NVIDIA acknowledges that the ’803 Patent “describes a cache memory hierarchy at the chiplets, including an L1, L2, and L3 (or other last level) cache,” and “further indicates that ‘[t]he L2 level of cache is coherent within a single chiplet.” NVIDIA Cover Pleading at 266. Further, the patent specification describes that “[e]ach of the GPU chiplets 106-1, 106-2 include [sic] a plurality of workgroup processors 302 (WGP) and a plurality of fixed function blocks 304 (GFX) that communicate with a given channel’s L1 cache memory 306,” and “[a] graphics data fabric 314 (GDF) of each GPU chiplet 106 connects all of the L1 cache memories 306 to each of the channels of the L2 cache memory 308, thereby allowing each of the workgroup processors 302

and fixed function blocks 304 to access data stored in any bank of the L2 cache memory 308.” *See* ’803 Patent, 5:5-10, 5:19-24. “The scalable data fabric of one GPU chiplet is able to access the lower level cache(s) on other GPU chiplets in nearly the same time as to access the lower level cache on its same chiplet, and thus allows the GPU chiplets to maintain cache coherency.” *See* also *e.g.*, ’803 Patent, 8:42-48. As such, these terms have adequate written description in the specification. *See Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 969 (Fed. Cir. 2002) (“The written description requirement is satisfied by the patentee’s disclosure of ‘such descriptive means as words, structures, figures, diagrams, formulas, etc., that fully set forth the claimed invention.’”).

The ’803 Patent’s specification also teaches those skilled in the art how to make and use the full scope of the claimed invention without undue experimentation. For example, a POSITA reading the specification of the ’803 Patent would understand how to practice the subject matter claimed by claims 8 and 9 of the ’803 Patent because, *e.g.*, the ’803 Patent explains that “[t]he GPU chiplet 106-1 [] includes a hierarchical cache memory 402 (*e.g.*, L1 cache memory 306, L2 cache memory 308, and L3 cache memory 310 of FIG.3).” *See e.g.*, ’803 Patent, 5:49-52. “A graphics data fabric 314 (GDF) of each GPU chiplet 106 connects all of the L1 cache memories 306 to each of the channels of the L2 cache memory 308,” and “is able to access the lower level cache(s) on other GPU chiplets in nearly the same time as to access the lower level cache on its same chiplet, and thus allows the GPU chiplets to maintain cache coherency” *See e.g.*, ’803 Patent, 5:19-21, 8:42-48. Thus, the ’803 Patent’s specification enables claims 8 and 9. *Hynix Semiconductor Inc. v. Rambus Inc.*, 645 F.3d 1336, 1345 (Fed. Cir. 2011) (“[T]he patent specification is written for a person of skill in the art, and such a person comes to the patent with the knowledge of what has come before. Placed in that context, it is unnecessary to spell out every detail of the invention in the specification; only enough must be included to . . . enable such a person to make and use the invention without undue experimentation.”).

2. The '809 And '019 Patents

The terms of the Asserted Claims in the '809 and '019 Patents are definite, enabled, and supported by sufficient written description.

a. “mapping the memory operation to ...” of the '809 and '019 Patents

The NVIDIA Invalidity Contentions allege that “Claims 1, 12, 13, and 20 of the '809 patent (as well as asserted dependent claims), and claims 1 and 11 of the '019 patent (as well as asserted dependent claims) are invalid as indefinite” because “[c]laims 1, 12, 13, and 20 of the '809 patent require ‘mapping the memory operation to’ virtual memory” and “claims 1 and 11 of the '019 patent require ‘map[ping] the received memory operation’ to virtual memory.” NVIDIA Cover Pleading at 266.

NVIDIA has failed to provide specific rationale as to how or why claims 1, 12, 13, and 20 of the '809 Patent and claims 1 and 11 of the '019 patent, read in light of the specification and the prosecution history fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. For example, the NVIDIA Invalidity Contentions merely assert that the claims are “nonsensical” without explanation, and conclude (incorrectly) that they are indefinite as a result. Moreover, the only statements made regarding these claim terms contained in NVIDIA’s Invalidity Contentions depend on NVIDIA’s own interpretation of a “memory operation” as “an operation that is *executed* by a processor” (emphasis in original). But the NVIDIA Invalidity Contentions provide no reasoning or evidence supporting this interpretation of a “memory operation,” and therefore amount to nothing more than baseless and unexplained assertions that provide no justification or support for the baseless assertions of indefiniteness. *See e.g.*, NVIDIA Cover Pleading at 266. As such, NVIDIA has failed to carry its burden to provide any specific contentions regarding indefiniteness of these terms.

In fact, contrary to NVIDIA's allegations, there is no reason the claims of the '809 and '019 Patents are "nonsensical" as alleged. There is neither any reason to construe "memory operation" as the NVIDIA Invalidity Contentions assert, nor is there reason that the claims would be "nonsensical" even if they were. For example, the specification of the '809 and '019 Patents states that "a unified computing system (USC) memory model broadly describes the permissible interactions of memory operations, e.g., load and store operations, from multiple threads operating in computing system 100 using CPU 102 and APD 104." '809 Patent at 10:35-39. The specification further explains:

Generally speaking, in an embodiment, a method of providing memory to a memory operation operating in a computer arrangement having an APD 104 and CPU 102 processor is provided. A memory operation, for example from application 211, is received from a processor and the memory operation is mapped using mapper 245 to one of a plurality of memory heaps 250. The result of the mapping is provided to the processor. The processor uses the mapping result to perform the memory operation using memory resources.

'809 Patent at 12:5-13; *see also, e.g.*, '809 Patent, 13:49-53, 14:60-63, 18:3-10. A POSITA reading the '809 and '019 Patents would easily understand these terms and the invention so these terms are definite. Nothing further is required by 35 U.S.C. § 112 ¶ 1. Thus, the specification, particularly read in light of the prosecution history, informs a POSITA with reasonable certainty about the scope of the invention.

The NVIDIA Invalidity Contentions also assert that "For the same reasons, the claims are invalid for lack of enablement and lack of written description," followed by its rewording of the relevant legal standards. NVIDIA Cover Pleading at 266-267. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description,

NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

Further, these terms are subject to upcoming claim construction briefing, and Onesta incorporates by reference its upcoming Initial Claim Construction Brief and Rebuttal Claim Construction Brief for the above identified limitations.

b. Antecedent basis for claim 8 of the '809 Patent

NVIDIA alleges that claim 8 of the '809 Patent “is invalid as indefinite” because allegedly “there is no antecedent basis for “the memory heap[]” in the claims from which claim 8 depends.” NVIDIA Cover Pleading at 267.

NVIDIA has failed to provide specific rationale as to how or why claim 8 of the '809 Patent, read in light of the specification and the prosecution history fails to inform, with reasonable certainty, those skilled in the art about the scope of the invention. For example, the NVIDIA Invalidity Contentions merely assert that there is no antecedent basis for “the memory heap[]” without explanation, and conclude (incorrectly) that the claim is indefinite as a result. But the NVIDIA Invalidity Contentions provide no reasoning or evidence supporting this conclusion, and as such, NVIDIA has failed to carry its burden to provide any specific contentions regarding indefiniteness of claim 8.

In fact, contrary to NVIDIA’s allegations, there is antecedent basis for “the memory heap” as recited in claim 8. Claim 8 depends from claim 1, which recites, *inter alia*, “a plurality of memory heaps.” This provides the antecedent basis for claim 8’s recitation of “at least one of the

memory heaps,” (“wherein at least one of the memory heaps (i) is accessible by both the first processor and the second processor”) which in turn provides the antecedent basis for “the memory heap” (“and (ii) the memory heap is mapped to a physical memory resource associated with the second processor using a page table associated with the second processor”).

The NVIDIA Invalidity Contentions also assert that “For the same reasons, the claims are invalid for lack of enablement and lack of written description,” followed by its rewording of the relevant legal standards. NVIDIA Cover Pleading at 267. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

c. “mapper” of the ’809 and ’019 Patents

NVIDIA alleges that “Claim 12 of the ’809 patent and claim 11 of the ’019 patent are invalid as indefinite” because the terms “a mapper” “configured to...” in claim 12 of the ’809 Patent (“a mapper configured to: receive an address reference from the memory operation, and mapping the memory operation to one of the plurality of memory heaps based on the address reference, wherein different attributes are applied to a mapped memory heap depending upon origination of the memory operation”) and claim 11 of the ’019 Patent (“a mapper, wherein the mapper is configured to: receive a memory operation from a processor that references an address

in the shared memory; map the received memory operation to at least one virtual memory pool to produce a mapping result, wherein the at least one virtual memory pool is associated with at least one memory resource [sic]”) are governed by 35 U.S.C. § 112(f), “yet the patent does not disclose sufficient corresponding structure for the limitations” to inform a POSITA “about the scope of the alleged invention.” *See e.g.*, NVIDIA Cover Pleading at 267-268.

However, the NVIDIA Invalidity Contentions provide no explanation or justification for the assumption that term “a mapper configured to” in the ’809 and ’019 Patents is a means-plus-function term. Thus, the NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertion that the claims are unclear, and therefore fail to satisfy Respondents’ burden. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts invalidity of claim 12 of the ’809 Patent or claim 11 of the ’019 Patent for indefiniteness, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to Qualcomm accordingly.

Moreover, the term “a mapper” is not a so-called “nonce word,” and does not include the word “means.” *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1347 (Fed. Cir. 2015) (“the failure to use the word ‘means’ also creates a rebuttable presumption—this time that § 112, para. 6 does not apply”). For example, a POSITA would understand the term “a mapper” to have a sufficiently definite meaning as the name for structure. Therefore, the term “a mapper configured to” in claim 12 of the ’809 Patent and claim 11 of the ’019 Patent is not a means-plus-function term, and is not indefinite.

d. Antecedent basis for claims 14-19 of the '809 Patent

NVIDIA alleges that claims 14 and 16-19 of the '809 Patent are invalid as indefinite because “[c]laims 14-19 require ‘the first processor’ and ‘the second processor,’ yet there is no antecedent basis for ‘the first processor’ or ‘the second processor.’” NVIDIA Cover Pleading at 268. However, the NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertion that the claims are unclear, and therefore fail to satisfy Respondents’ burden. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts invalidity of claims 14 and 16-19 of the '809 Patent for indefiniteness, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

Additionally, the terms are not indefinite. For example, “obvious minor typographical and clerical errors in patents” can be corrected and do not render the claims indefinite. *See, e.g., Pavo Sols. LLC v. Kingston Tech. Co.*, 35 F.4th 1367, 1373 (Fed. Cir. 2022). For example, that claims 14 and 16-19 refer to a “first processor” and a “second processor” is not subject to reasonable debate based on consideration of the claim language and the specification, and the prosecution history does not suggest a different interpretation of the claims. A POSITA would understand that the '809 Patent claims 14-19 reference to “the first processor” and “the second processor” refer to processors associated with the “first processor memory resource” and the “second processor memory resource” previously recited.

The NVIDIA Invalidity Contentions also assert that “For the same reasons, the claims are

invalid for lack of enablement and lack of written description,” followed by its rewording of the relevant legal standards. NVIDIA Cover Pleading at 268. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

e. “a processor,” “a second processor, and “a processor” in claims 1 and 20 of the ’809 Patent and claims 1 and 11 of the ’019 Patent

The NVIDIA Invalidity Contentions allege that “claims 1 and 20 of the ’809 Patent and claims 1 and 11 of the ’019 Patent are invalid as indefinite” because “[c]laims 1 and 20 of the ’809 patent recite ‘a first processor’ and ‘a second processor,’ but then separately recite ‘a processor,’ making it unclear whether ‘a processor’ is one of the ‘first’ or ‘second’ processors, or a third processor.” However, the NVIDIA Invalidity Contentions provide no explanation or justification for the assumption that the preambles of the claims are limiting, which would be required for there to be a requirement for the “first processor” or “second processor” to which NVIDIA refers. Thus, the NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertion that the claims are unclear, and therefore fail to satisfy Respondents’ burden. For example, NVIDIA does not assert, let alone explain or demonstrate that the claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable

certainty, those skilled in the art about the scope of the invention. By failing or electing to not include any substantive assertions regarding the reason why Qualcomm asserts invalidity of claims 1 and 20 of the '809 Patent and claims 1 and 11 of the '019 Patent for indefiniteness, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also assert that “For the same reasons, the claims are invalid for lack of enablement and lack of written description,” followed by its rewording of the relevant legal standards. NVIDIA Cover Pleading at 269. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

f. “APD” in claims 11, 19, and 25 of the '809 Patent

The NVIDIA Invalidity Contentions allege that meaning of the term “APD” in claims 11, 19, and 25 of the '809 Patent is indefinite. NVIDIA Cover Pleading at 269. The NVIDIA Invalidity

Contentions assert that the '809 Patent “fails to disclose or define how to distinguish the claimed “APD” from “conventional” components/software.” *Id.* However, the NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertion that the claims are unclear, and therefore fail to satisfy Respondents’ burden. For example, NVIDIA does not assert, let alone explain or demonstrate that the claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts invalidity of claims 11, 19, and 25 of the '809 Patent for indefiniteness, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

For example, contrary to Qualcomm’s assertions, the specification explains:

Although GPUs, accelerated processing units (APUs), and general purpose use of the graphics processing unit (GPGPU) are commonly used terms in this field, the expression “accelerated processing device (APD)” is considered to be a broader expression. For example, APD refers to any cooperating collection of hardware and/or software that performs those functions and computations associated with accelerating graphics processing tasks, data parallel tasks, or nested data parallel tasks in an accelerated manner compared to conventional CPUs, conventional GPUs, software and/or combinations thereof.

'809 Patent at 2:5-16.

The NVIDIA Invalidity Contentions also assert that “For the same reasons, the claims are invalid for lack of enablement and lack of written description,” followed by its rewording of the

relevant legal standards. NVIDIA Cover Pleading at 269. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

g. Claims 3, 8, 9, 13, 18, and 19 of the '019 Patent

The NVIDIA Contentions assert that “Claims 3, 8, 9, 13, 18, and 19 of the '019 patent are invalid as indefinite” because these claims recite “at least one of the plurality of processors” in claims 3 and 13; “one processor of the plurality of processors” claims 8 and 18; and “all processors of the plurality of processors” in claims 9 and 19. NVIDIA’s Invalidity Contentions at 270. However, the NVIDIA Invalidity Contentions do not provide any explanation or justification for the assertion that the claims are unclear, and therefore fail to satisfy Respondents’ burden. For example, NVIDIA does not assert, let alone explain or demonstrate that the claims, read in light of the specification delineating the patent, and the prosecution history, fail to inform, with reasonable certainty, those skilled in the art about the scope of the invention. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts invalidity of claims 11, 19, and 25 of the '809 Patent for indefiniteness, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its

contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

The NVIDIA Invalidity Contentions also assert that “For the same reasons, the claims are invalid for lack of enablement and lack of written description,” followed by its rewording of the relevant legal standards. NVIDIA Cover Pleading at 269. However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

h. Claims 1 and 20 of the '809 Patent and Claims 1 and 11 of the '019 Patent

The NVIDIA Invalidity Contentions assert that “Claims 1 and 20 of the '809 patent, and claims 1 and 11 of the '019 patent are invalid for lack of written description support and lack of enablement” because the “require ‘provid[ing] the mapping result to the processor.’” NVIDIA Cover Pleading at 270. alleges that the terms “provid[ing] the mapping result to the processor” in claims 1 and 20 of the '809 Patent and claims 1 and 11 of the '019 Patent are “invalid for lack of written description support and lack of enablement.” NVIDIA’s Invalidity Contentions at 270.

However, this bald assertion provides no explanation or allegations as to why the claims allegedly lack written description or are not enabled. By failing or electing to not include any substantive assertions regarding the reason why NVIDIA asserts the claims are invalid for lack of enablement and lack of written description, NVIDIA has waived the ability to do so, as NVIDIA has had all the information and evidence necessary to make such allegations since the beginning of the Investigation, and has no excuse for not including such allegations in its contentions. To the extent any Respondent attempts to expand upon the allegations made in the NVIDIA Invalidity Contentions, Onesta reserves all rights to bar tardy arguments and evidence from admission into the administrative record, and to supplement its Initial Rebuttal Contentions to NVIDIA accordingly.

Moreover, these claim terms cited by NVIDIA in the '809 and '019 Patents are expressly disclosed within the corresponding as-filed U.S. Patent Application Serial Nos. 13/724,879 and US17/471,552– in most cases, used extensively throughout the specification – and used in the same manner as in the as-granted claims. As such, these terms have adequate written description in the specification. *See Enzo Biochem, Inc. v. Gen-Probe Inc.*, 323 F.3d 956, 969 (Fed. Cir. 2002) (“The written description requirement is satisfied by the patentee’s disclosure of ‘such descriptive means as words, structures, figures, diagrams, formulas, etc., that fully set forth the claimed invention.’”). Additionally, the specifications of the '809 and '019 Patents sufficiently describe the invention such that a POSITA could make and use the invention without undue experimentation. For example, the specification describes “[a]t stage **520**, the received memory operation is mapped to a one of a plurality of memory heaps, such mapping resulting in a mapping result.” The specification goes on to describe “[a]t stage **530**, the mapping result is provided to the processor, and the processor uses the mapping result to perform the memory operation. For example, in an embodiment, mapper **245** provides a mapping result to a processor, for example

CPU **102**. In another example, the mapping result is provided to APD **104**.” *See e.g.*, ’809 Patent, 18:3-16; *see also, e.g.*, ’019 Patent, 18:38-52.

VII. Reservation of Rights

Onesta reserves the right to supplement this response, and its arguments and evidence, should Respondents attempt to further support their invalidity contentions.

Onesta further states that fact discovery is ongoing, including at least because productions are ongoing, contention disclosures are ongoing, depositions have not taken place, the Commission’s claim construction ruling has not issued, and more. Accordingly, Onesta reserves the right to further supplement and/or amend this response as Onesta continues to review and receive documents and other relevant information, as Onesta’s understanding of the issues in this Investigation progresses, and in accordance with Commission Rule 210.27(f).

Date: September 29, 2025

Respectfully submitted,

Raymond Lu
MINTZ LEVIN COHN FERRIS
GLOVSKY AND POPEO PC
3580 Carmel Mountain Road, Ste 300
San Diego, CA 92130
Tel: 858-314-1500

Yanyi Liu
MINTZ LEVIN COHN FERRIS
GLOVSKY AND POPEO PC
44 Montgomery Street, 36th Floor
San Francisco, CA 94104
Tel: 415-432-6013

/s/ Michael T. Renaud

Michael T. Renaud
Adam S. Rizk
Samuel F. Davenport
William Meunier
Marguerite McConhie
Matthew A. Karambelas
Catherine Xu
Kumar Ravula
Courtney Herndon
Paul Weinand
Laura Petrasky
Hannah M. Edge
Amanda Metell
Amy LoBue
MINTZ LEVIN COHN FERRIS
GLOVSKY AND POPEO PC
One Financial Center
Boston, MA 02111
Tel: 617-542-6000
Onesta-ITC@mintz.com

*Counsel to Complainant
Onesta IP, LLC*

CERTIFICATE OF SERVICE

I, Megan De Renzis, hereby certify that on September 29, 2025, true and correct copies of the foregoing was served on the parties as indicated below:

Ryan Schmid, Esq Office of Unfair Import Investigations U.S. International Trade Commission 500 E Street, S.W., Suite 401 Washington, D.C. 20436 Ryan.Schmid@usitc.gov	☐ Via Hand Delivery ☒ Via Electronic Mail
<i>Counsel for NVIDIA Corporation:</i> William F. Lee Michael J. Summersgill Jordan Hirsch Harry Hanson Rachel Bier WILMER CUTLER PICKERING HALE AND DORR LLP 60 State Street Boston, MA 02109 Telephone: (617) 526-6000 Todd Zubler Grant Rowan Amanda L. Major Heath Brooks WILMER CUTLER PICKERING HALE AND DORR LLP 2100 Pennsylvania Ave. NW Washington, DC 20037 Telephone: (202) 663-6000 Derek A. Gosma WILMER CUTLER PICKERING HALE AND DORR LLP 350 South Grand Avenue, Suite 2400 Los Angeles, CA 90071 Telephone: (213) 443-5300 WHNvida- Onesta1450Servicelist@wilmerhale.com	☐ Via Hand Delivery ☐ Via Federal Express (Overnight) ☒ Via Electronic Mail
<i>Counsel for Qualcomm, Inc.:</i> Deanna Tanner Okun Daniel F. Smith Lauren E. Peterson	☐ Via Hand Delivery ☐ Via Federal Express (Overnight) ☒ Via Electronic Mail

Sean M. Wesp Polsinelli P.C. 1401 Eye Street N.W., Suite 800 Washington, D.C. 20005 Telephone: (202) 626-8320 qcom-1450-itc@polsinelli.com Jennifer Swize Vishal Khatri Nicholas D’Andrea Derek Walker Yury Kalish Hong Jun-Ha Jones Day 51 Louisiana Avenue, N.W. Washington, D.C. 20001-2113 William Devitt Matthew Hertko Kristina Hendricks James Twieg Marc Blackman Jones Day 110 North Wacker Drive, Suite 4800 Chicago, IL 60606 Dalton Earich Hannah Mehrle David Linden Jones Day 901 Lakeside Avenue Cleveland, OH 44114 Keith Davis Jones Day 2727 North Harwood Street Dallas, TX 75201-1515 Michael Lavine Jones Day 555 California Street, 26th Floor San Francisco, CA 94104 qualcomm-onesta-itc@jonesday.com	
<i>Counsel for OnePlus Technology (Shenzhen) Co., Ltd.:</i>	☐ Via Hand Delivery ☐ Via Federal Express (Overnight)

Jack Ko, Ph.D. Nannan Li PILLSBURY WINTHROP SHAW PITTMAN LLP Suite 3001, 30th Floor, Jing An Kerry Center, Tower 2 1539 Nanjing Road West Shanghai, 200041 86.21.6137.7999 jack.ko@pillsburylaw.com nannan.li@pillsburylaw.com OnePlusTC1450@Pillsburylaw.com Theresa A. Roozen Michael Grosso PILLSBURY WINTHROP SHAW PITTMAN LLP 7900 Tysons One Place, Suite 500 Tysons, VA 22102 (703) 770-7900 theresa.roozen@pillsburylaw.com michael.grosso@pillsburylaw.com	☒ Via Electronic Mail
<i>Counsel for Nothing Technology Limited:</i> Charles S. Barquist MASCHOFF BRENNAN GILMORE ISRAELSEN & MAURIEL 1801 Century Park East, Suite 2400 Los Angeles, California 90067 Jacob O. Israelsen MASCHOFF BRENNAN GILMORE ISRAELSEN & MAURIEL 95 S State Street, Suite 800 Salt Lake City, Utah 84123 MB_NTech_337-TA-1450@mabr.com jisraelsen@mabr.com cbarquist@mabr.com	☐ Via Hand Delivery ☐ Via Federal Express (Overnight) ☒ Via Electronic Mail

Megan A. De Renzis

Megan De Renzis
Legal Specialist
Mintz, Levin, Cohn, Ferris,
Glovsky and Popeo, P.C.
555 12th Street NW, Suite 1100
Washington, DC 20004
202.434.7406
MADeRenzis@mintz.com