IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

NETLIST, INC., Plaintiff, v. MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC, Defendants.	Civil Action No. 6:21-cv-00431 **JURY TRIAL DEMANDED**

NETLIST, INC.'S
COMPLAINT FOR PATENT INFRINGEMENT

Plaintiff Netlist, Inc. ("Netlist") as and for its complaint for patent infringement against Micron Technology, Inc. ("Micron Technology"), Micron Semiconductor Products, Inc. ("Micron Semiconductor"), and Micron Technology Texas LLC ("Micron Texas") (collectively, "Defendants") alleges as follows:

PARTIES

1. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 175 Technology Drive, Suite 150, Irvine, California 92618.

2. Netlist is the owner by assignment of U.S. Patent Nos. 10,489,314 ("the '314 Patent"), 9,824,035 ("the '035 Patent), and 10,268,608 ("the '608 Patent") (together, "the Asserted Patents") (attached as Exhibits 1-3). Netlist has identified the Asserted Patents, among other Netlist patents, as potentially essential to various DDR4 memory module standards promulgated by the Joint Electron Device Engineering Counsel, or "JEDEC," the standard-

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setting body for the microelectronics industry—and has provided RAND Licensing Assurances pursuant to JEDEC's Patent Policy.

3. Micron Technology is a corporation organized and existing under the laws of Delaware, having a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Technology also has a place of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Micron Technology makes dynamic random-access memory (DRAM), NAND Flash, and NOR Flash memory, and other memory products. Micron makes its own products in semiconductor fabrication plants in the United States and other countries throughout the world. On information and belief, Micron sells its products to customers, including customers in this District, in the computer, networking and storage, consumer electronics, solid-state drives, and mobile telecommunications markets.

4. Micron Semiconductor is a corporation organized and existing under the laws of Idaho, having a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Semiconductor also has a place of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Micron Semiconductor is registered with the Texas Secretary of State to do business in Texas. Micron Semiconductor can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

5. Micron Texas is a corporation organized and existing under the laws of Idaho, having a principal place of business at 8000 South Federal Way, Boise, Idaho 83716. Micron Texas also has a place of business at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728. Micron Texas is registered with the Texas Secretary of State to do business in Texas. Micron Texas can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, TX 78701-3218.

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6. Micron Semiconductor and Micron Texas are wholly owned subsidiaries of Micron Technology. Micron Technology does not separately report revenue from Micron Semiconductor or Micron Texas in its filings to the Securities Exchange Commission, but rather reports combined revenue from its various products and subsidiaries.

7. Defendants place, have placed, and contributed to placing infringing products like Load Reduced Dual In-line Memory Modules ("LRDIMMs") into the stream of commerce via an established distribution channel knowing or understanding that such products would be sold and used in the United States, including in the Western District of Texas. On information and belief, Defendants have also derived substantial revenues from infringing acts in this District including from the sale and use of infringing LRDIMM products.

JURISDICTION AND VENUE

8. This is an action for patent infringement arising under the patent laws of the United States, Title 35 of the United States Code § 1, et seq. Accordingly, this Court has subject matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

9. This Court has specific personal jurisdiction over Defendants at least in part because Defendants conduct business in this Judicial District. Netlist's causes of action arise, at least in part, from Defendants' contacts with and activities in the State of Texas and this District. On information and belief, Defendants have committed acts of infringement within the State of Texas and this District by, among other things, directly and/or indirectly using, selling, offering to sell, or importing products that infringe one or more claims of the Asserted Patents.

10. Defendants conduct business in this District and maintain regular and established places of business within this District. For example, Defendants has maintained regular and established places of business with offices and/or other facilities in this District, including at least such offices and/or facilities at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas

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78728. On information and belief, personnel working at this facility in Austin engage in activities directly related to the LDRDIMM products at issue in this case.

11. For example, personnel employed by Defendants working at this location are semiconductor professionals, including design engineers, fabrication engineers, field applications engineers, storage solutions engineers, software engineers, data analysts, customer quality specialists, facilities designers, product line managers, quality assurance managers, program managers, sales directors, marketing directors, and systems architects.

12. Defendants have placed or contributed to placing infringing products including, but not limited to, their LRDIMM products into the stream of commerce knowing or understanding that such products would be sold and used in the United States, including in this District.

13. Defendants have also derived substantial revenues from infringing acts in this District, including from the sale and use of infringing products including, but not limited to, Defendants' LRDIMM products.

14. Defendants have committed acts within this District giving rise to this action, and have established sufficient minimum contacts with the State of Texas such that the exercise of jurisdiction would not offend traditional notions of fair play and substantial justice.

15. Venue is proper in this District as to Defendants pursuant to 28 U.S.C. § 1391(b), (c), and 1400(b) because Defendants (1) have committed and continue to commit acts of patent infringement in this District by, among other things, directly and/or indirectly making, using, selling, offering to sell, or importing products that infringe one or more claims of the Asserted Patents, and (2) have done and continue to do business in this District by maintaining regular and established places of business, including at least at 101 West Louis Henna Boulevard, Suite 210, Austin, Texas 78728.

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FACTUAL BACKGROUND

A. NETLIST

16. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase.

17. Netlist has a long history of being the first to market with disruptive new products based on Netlist's distributed buffer architecture later adopted by the industry.

18. Netlist's innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory modules.

19. The inventors of the Asserted Patents were critical in the development of these pioneering technologies. Indeed, Jay Bhakta, one of the co-founders of Netlist, had more than two decades of electronic design experience and was a well-known engineer who has served as a long-time member of the Joint Electron Device Engineering Council ("JEDEC") Board of Directors prior to his passing.

B. NETLIST'S LRDIMM TECHNOLOGY AND ITS ROLE IN JEDEC

20. The technologies disclosed and claimed in the Asserted Patents relate generally to memory modules. Memory modules are typically printed circuit boards that contain, among other important components, DRAM (Dynamic Random-Access Memory) integrated circuits.

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Memory modules are often installed into memory slots on computer motherboards and serve as memory for computer systems.

21. Certain structures, functions, and operations of server memory modules (such as those used in Defendants' infringing devices) are defined, specified, and standardized by JEDEC—the standard-setting organization that develops and adopts standards for the microelectronics industry.

22. LRDIMM is shorthand for "load-reduced dual inline memory module." An LRDIMM is a particular dual inline memory module ("DIMM") architecture that Netlist first introduced in its HyperCloud product. Netlist's—and the industry's—first LRDIMM product demonstrated what was previously thought to be impossible: that a server could be fully loaded with memory and still operate at the highest system speeds available at the time.

23. Netlist's innovative LRDIMM technology has since been adopted by JEDEC in its DDR4 LRDIMM standard that is used by companies throughout the industry.

24. In August of 2019, JEDEC released the second version of the standard for one of the critical memory module components of LRDIMMs—the DDR4[1] register control device.

25. Netlist has supplied its memory modules in high volume to computer storage customers for many years.

C. NETLIST'S EFFORTS TO LICENSE ITS STANDARD-ESSENTIAL PATENTS PURSUANT TO JEDEC'S PATENT POLICY

26. Netlist is a member of JEDEC. Netlist "committed" the Asserted Patents to various JEDEC standards pursuant to the JEDEC Patent Policy, which sets certain obligations for owners of patents (like the Asserted Patents) that it reasonably believes are essential to one or more

[1] DDR4 refers to the latest generation of DRAM memory. Older, slower generations of memory modules used DDR3 DRAM; even older memory modules used DDR2 DRAM.

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JEDEC standards. Netlist has in all respects and at all times acted in a manner consistent with the JEDEC Patent Policy, as set forth in the JEDEC Manual of Organization and Procedure, which states in relevant part that "[a] license will be offered, to applicants desiring to utilize the license for the purpose of implementing the JEDEC Standard under reasonable terms and conditions that are free of any unfair discrimination . . .."

27. Netlist contacted Defendants by letter dated April 28, 2021 and notified them of their infringement of the Asserted Patents and offered Defendants a license for their RDIMM and LRDIMM products. Netlist's offer complies with JEDEC's patent policy, as the offer was made to license Micron's infringing products under reasonable terms and conditions free of any unfair discrimination. By service of this Complaint, the Defendants either refused to negotiate in good faith in response to Netlist's RAND offer, and/or have refused to pay for a license to the Asserted Patents.

THE ASSERTED PATENTS

A. The '314 Patent

28. Netlist owns the '314 Patent by assignment from the listed inventors Jeffery C. Solomon and Jayesh R. Bhakta. The '314 Patent was filed as Application No. 15/857,519 on December 28, 2017, issued as a patent on November 26, 2019, and claims priority through a series of continuation applications to five provisional applications, filed on January 19, 2005 (No. 60/645,087); July 15, 2004 (No. 60/588,244); March 5, 2004 (No. 60/550,668); May 28, 2004 (No. 60/575,595); and July 21, 2004 (No. 60/590,038).

29. The '314 Patent is entitled "Memory Module with Data Buffering," and relates generally to a memory module operable to communicate data with a memory controller via a data bus that includes a plurality of memory integrated circuits with a data buffer coupled

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between them, as well as logic that is configured to respond to memory commands through the use of the data buffer. As summarized in the Abstract, "[t]he logic is configured to respond to a first memory command by providing first control signals to the data buffer to enable communication of at least one first data signal between the first memory integrated circuits and the memory controller through the data buffer, and is further configured to respond to a second memory command by providing second control signals to the data buffer to enable communication of at least one second data signal between the second memory integrated circuit and the memory controller through the data buffer."

30. The invention of the '314 Patent enables the effective operation of DDR4 LRDIMMs, which are characterized by the use of a buffer approach to accomplish memory bandwidth efficiencies when scaling to higher capacities and speed. The '314 Patent includes embodiments directed to modifying latency to achieve more efficient data transfers.

B. The '035 Patent

31. Netlist owns the '035 Patent by assignment from the listed inventors Hyun Lee and Jayesh Bhakta. The '035 Patent was filed as Application No. 15/426,064 on February 7, 2017, issued as a patent on November 21, 2017, and claims priority through a series of continuation applications to provisional application No. 61/676,883 filed on July 27, 2012.

32. The '035 Patent is entitled "Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers," and relates generally to module control devices that receive command signals from a memory controller and output module command signals and module control signals, as well as a plurality of buffer circuits that include logic configured to obtain timing information from the module control signals and to control timing of the data and strobe signals with the timing information.

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33. The invention of the ’035 Patent is directed to improving DDR4 performance in LRDIMMs by ensuring proper timing of control and data signals received and transmitted by a memory module through the distribution of buffer circuits across the memory module. In this way, during high speed operations, each module control signal may arrive at different buffer circuits at different points of time across more than one clock cycle of the system clock.

C. The ’608 Patent

34. Netlist owns the ’608 patent by assignment from the listed inventors Hyun Lee and Jayesh Bhakta. The ’608 Patent was filed as Application No. 15/820,076 on November 21, 2017, as a continuation of the ’035 Patent, issued as a patent on April 23, 2019, and claims priority through a series of continuation applications to provisional application No. 61/676,883 filed on July 27, 2012.

35. The ’608 Patent is entitled “Memory Module with Timing-Controlled Data Paths in Distributed Data Buffers” and generally discloses memory devices organized in groups, a module control device, and data buffers. The memory module is operable to perform memory operations in response to memory commands, each of which is represented by a set of signals transmitted by the memory controller to the memory module.

36. As a continuation of the ’035 Patent, the ’608 Patent is similarly directed to improving DDR4 performance in LRDIMMs by ensuring proper timing of control and data signals received and transmitted by a memory module through the distribution of buffer circuits across the memory module. The ’608 Patent includes a command processing circuit that is configured to decode module control signals, as well as a delay circuit that is configured to delay signals by a predetermined amount.

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OVERVIEW OF DEFENDANTS' INFRINGING TECHNOLOGY

37. Defendants are worldwide semiconductor solution providers that primarily manufacture semiconductor memory products such as DRAM, NAND Flash and MCP (Multi-Chip Package).

38. Defendants' infringing DDR4 LRDIMM memory modules are designed for use in servers, such as those supporting cloud-based computing and other data-intensive applications. The infringed memory modules are JEDEC-standard compliant memory modules.

39. Defendants make, use, sell, offer to sell, and/or import within this District and elsewhere in the United States, infringing DDR4 LRDIMMS (the "LRDIMM Infringing Products").

40. The LRDIMM Infringing Products include, without limitation, the following exemplary DDR4 LRDIMM modules[2] -- as well as comparable models that operate in the same or similar manner as described in the Infringement Counts:

+ Filters	Density	Technology	Part Status	Depth	Width	Voltage
Part No. (8)						
MTA144ASQ16G72LSZ-2S6	128GB	DDR4 SDRAM	Production	16Gb	x72	1.2V
MTA144ASQ16G72LSZ-2S9	128GB	DDR4 SDRAM	Production	16Gb	x72	1.2V
MTA36ASF4G72LZ-2G6	32GB	DDR4 SDRAM	Production	4Gb	x72	1.2V
MTA36ASF8G72LZ-2G9	64GB	DDR4 SDRAM	Production	8Gb	x72	1.2V
MTA36ASF8G72LZ-3G2	64GB	DDR4 SDRAM	Production	8Gb	x72	1.2V
MTA72ASS16G72LZ-3G2	128GB	DDR4 SDRAM	Production	16Gb	x72	1.2V
MTA72ASS8G72LZ-2G6	64GB	DDR4 SDRAM	Production	8Gb	x72	1.2V
MTA72ASS8G72LZ-2G9	64GB	DDR4 SDRAM	Production	8Gb	x72	1.2V

[2] *See* Micron LRDIMM Product catalog, available at https://www.micron.com/products/dram-modules/lrdimm/part-catalog.

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COUNT 1

(Willful Infringement of U.S. Patent No. 10,489,314)

41. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

42. Plaintiff is informed and believes, and on that basis alleges, that Defendants have infringed and are currently infringing one or more claims (e.g., claim 15) of the ’314 Patent, in violation of 35 U.S.C. § 271.

43. Defendants have infringed and are currently infringing literally and/or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing within this judicial district and elsewhere in the United States, without license or authority, Infringing Products, including without limitation their DDR4 LRDIMM memory modules and related products and/or processes falling within the scope of one or more claims of the ’314 Patent, including claim 15:

> A memory module operable in a computer system to communicate data with a memory controller of the computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller, the memory module comprising:
>
> > a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;
> >
> > logic coupled to the printed circuit board and configured to receive a first set of input address and control signals associated with a first read or write memory command and to output a first set of registered address and control signals in response to the first set of input address and control signals, the first set of input address and control signals including a first plurality of input chip select signals, the first set of registered address and control signals including a first plurality of registered chip select signals corresponding to respective ones of the first plurality of input chip select signals, the first plurality of registered chip select signals including a first registered chip select signal having an active signal value and one or more other registered chip select signals each having a non-active signal value;
> >
> > memory devices mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, wherein the plurality of N-bit wide ranks are configured to receive respective ones of the first plurality of registered chip select signals, wherein a first N-bit wide rank in the plurality of N-bit wide ranks receiving the first registered chip select signal having the active signal value is configured to receive or output a first burst of N-bit wide data signals and a first burst of data strobes associated with the first read or write command;

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circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks; and

wherein the logic is further configured to, in response to the first read or write memory command, output first control signals to the circuitry, and wherein the circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the first control signals so that respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module; and

wherein the data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices.

44. Defendants' acts of making, using, offering for sale, selling, and/or importing Infringing Products, including but not limited to DDR4 LRDIMM memory modules and related products and/or processes satisfy, literally or under the doctrine of equivalents, each and every claim limitation, including but not limited to limitations of claim 15.[3]

45. For example, the Defendants' Infringing Product 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 meets each and every limitation of claim 15.

46. Defendants' 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 is a memory module operable to communicate data with a memory controller of a computer system via a N-bit wide memory bus in response to read or write memory commands received from the memory controller.

[3] Plaintiff expressly reserves the right to identify additional asserted claims in its infringement contentions in accordance with this Court's Order Governing Procedures ("OGP") and other Standing Orders. Claim 15 is provided for notice pleading only and is not presented as an "exemplary" claim of all other claims in the '314 patent.

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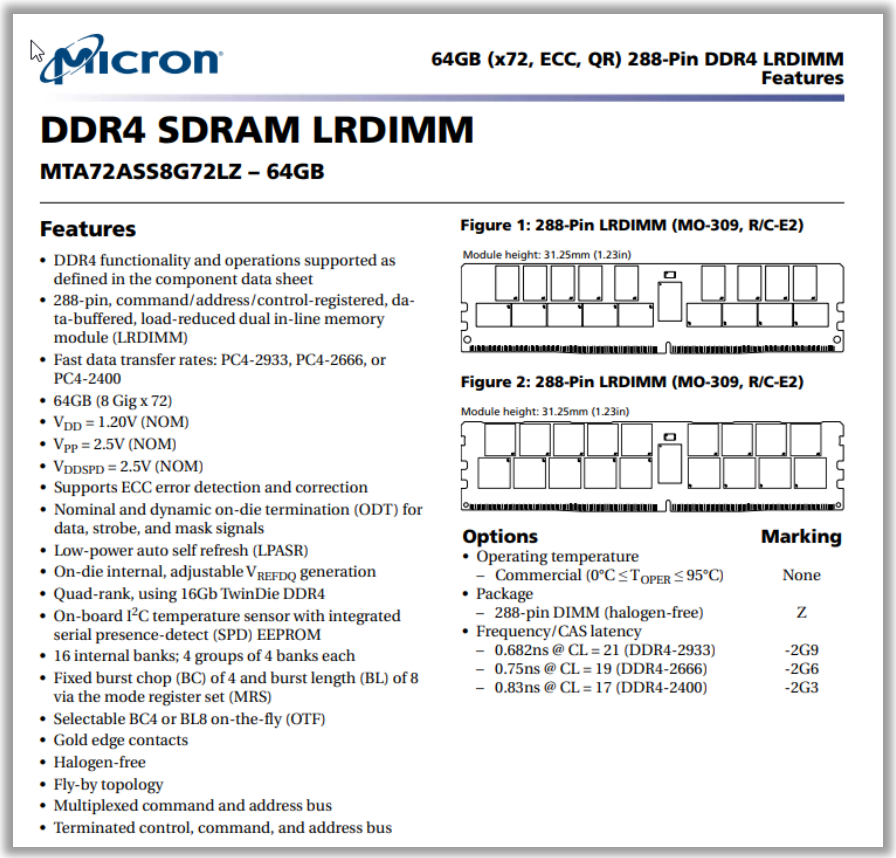


Micron

64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM
Features

DDR4 SDRAM LRDIMM

MTA72ASS8G72LZ – 64GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, command/address/control-registered, data-buffered, load-reduced dual in-line memory module (LRDIMM)
- Fast data transfer rates: PC4-2933, PC4-2666, or PC4-2400
- 64GB (8 Gig x 72)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.5V (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die internal, adjustable V_{REFDQ} generation
- Quad-rank, using 16Gb TwinDie DDR4
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Figure 1: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Figure 2: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	None
• Package	
– 288-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.682ns @ CL = 21 (DDR4-2933)	-2G9
– 0.75ns @ CL = 19 (DDR4-2666)	-2G6
– 0.83ns @ CL = 17 (DDR4-2400)	-2G3

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet ("Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet"), Page 1 (https://media-www.micron.com/-/media/client/global/documents/products/data-sheet/modules/lrdimm/ddr4/ass72c8gx72lz.pdf?rev=9cd25a3a18c84a98bf57e0ba5c691cec).

47. As an LRDIMM, Defendants' 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 complies with the DDR4 SDRAM Load Reduced DIMM Design Specification promulgated by the JEDEC:

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

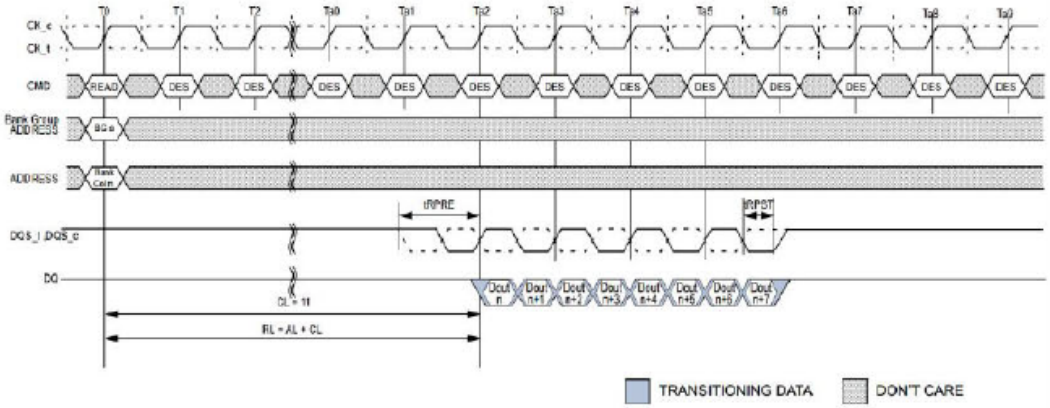
See JEDEC Standard No. 21C (Aug. 2015), Page 4.20.27-5.

48. The JEDEC standard specifies READ and WRITE operations. By way of example only, the following excerpts show operations according to the standard:

JEDEC Standard No. 79-4B
Page 98

4.24.2 READ Burst Operation

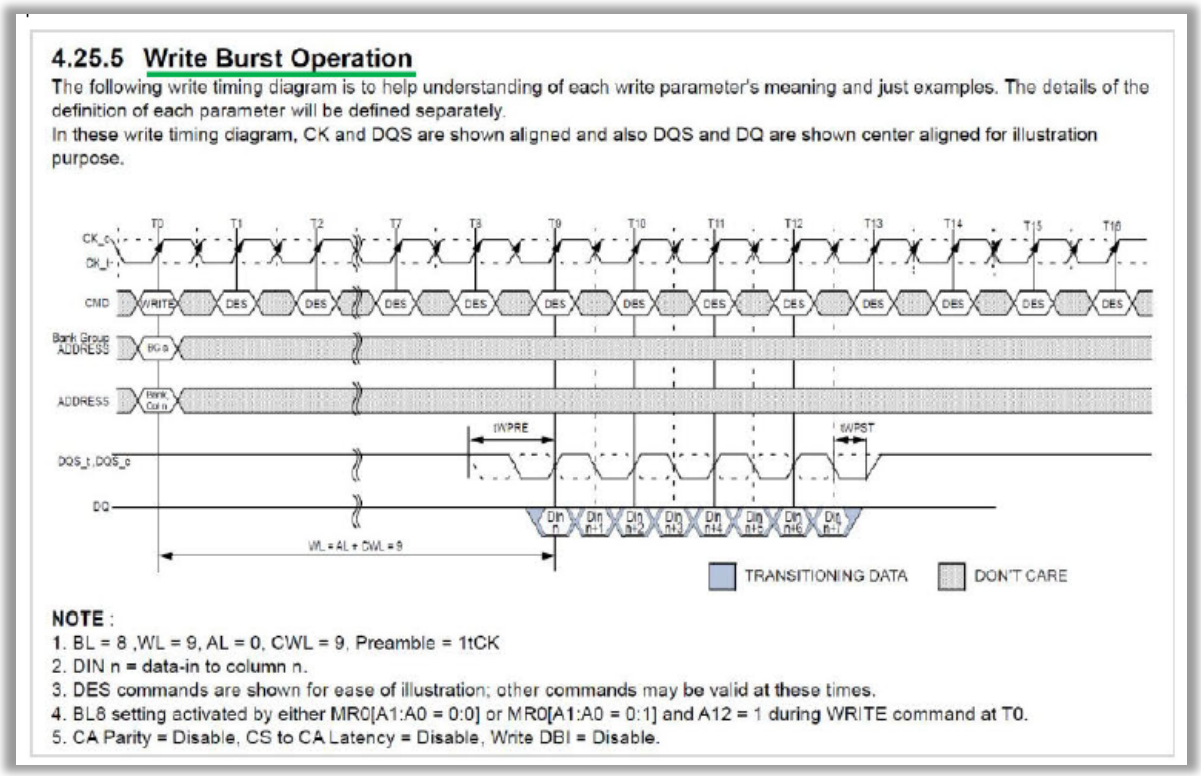
During a READ or WRITE command, DDR4 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).
A12 = 0 : BC4 (BC4 = burst chop)
A12 = 1 : BL8
A12 is used only for burst length control, not as a column address.



NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 76 — READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)

See JEDEC Standard No. 79-4B (June 2017), Page 98.



4.25.5 Write Burst Operation

The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.

NOTE :

1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

See JEDEC Standard No. 79-4B (June 2017), Page 119.

49. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 incorporates a Montage Gen2 DDR4 data buffer ("DB") and a Montage Gen2 DDR4 Registering Clock Driver ("RCD").

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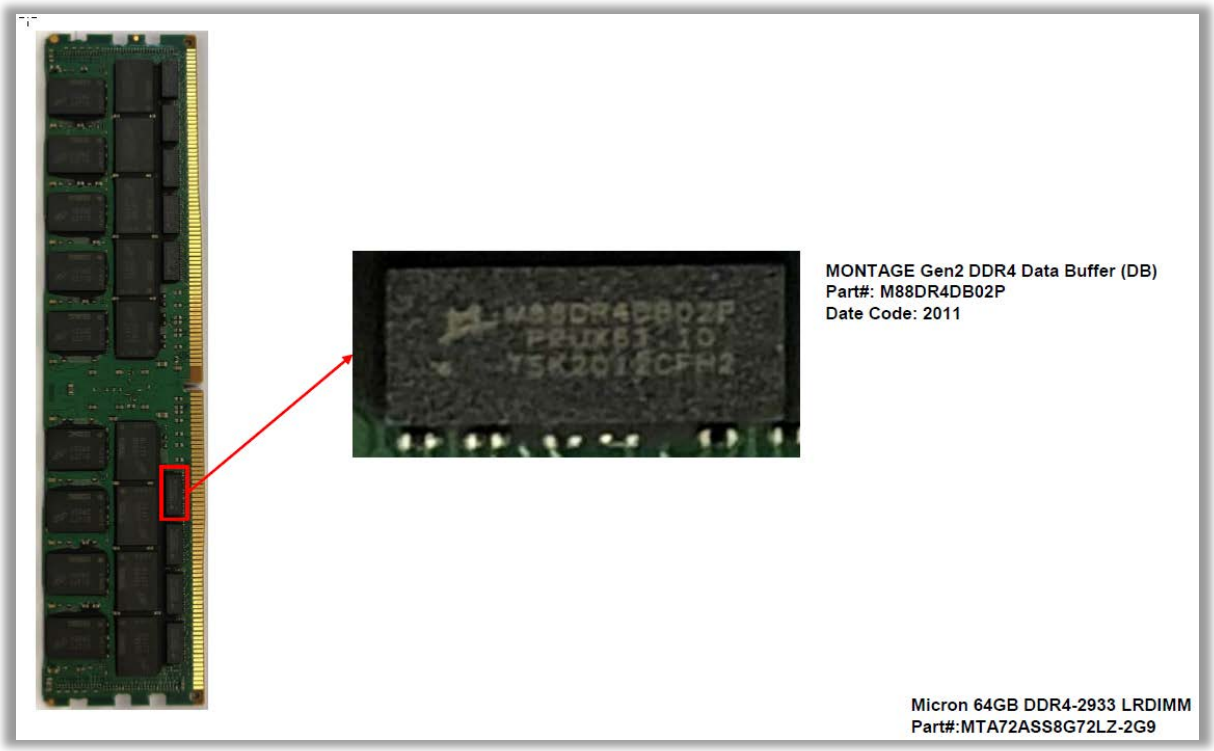
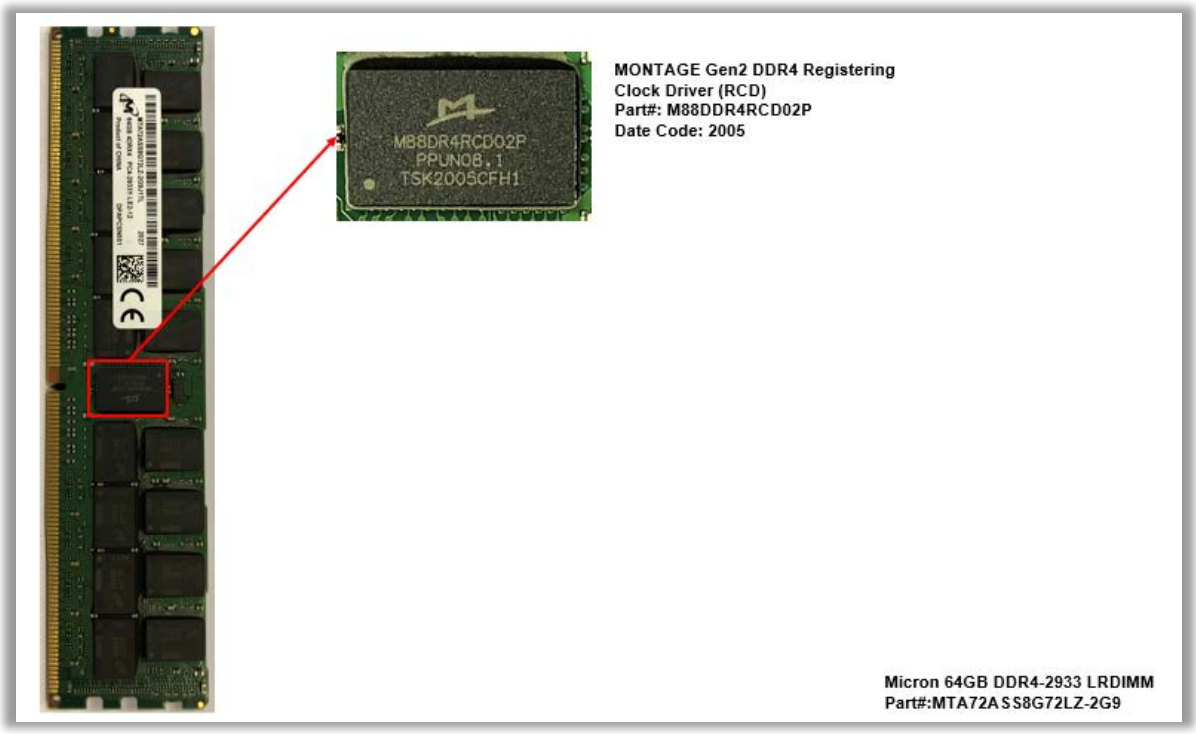

MONTAGE Gen2 DDR4 Data Buffer (DB)
Part#: M88DR4DB02P
Date Code: 2011
Micron 64GB DDR4-2933 LRDIMM
Part#:MTA72ASS8G72LZ-2G9


M88DR4RCD02P
PPUN08.1
TSK2005CFH1
MONTAGE Gen2 DDR4 Registering
Clock Driver (RCD)
Part#: M88DDR4RCD02P
Date Code: 2005
Micron 64GB DDR4-2933 LRDIMM
Part#:MTA72ASS8G72LZ-2G9

50. The Montage DB is compliant with the JEDEC DDR4DB02 specification. (*See* M88DDR4DB02 Product Description, https://www.montage-tech.com/Memory_Interface/DDR4/M88DDR4DB02.) The Montage RCD is compliant with the JEDEC DDR4RCD02 specification. (*See* M88DDR4RCD02 Product Description, https://www.montage-tech.com/Memory_Interface/DDR4/M88DDR4RCD02.)

51. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a printed circuit board ("PCB," see images of front and back below) with edge connections configured to be electrically coupled to corresponding contacts of a module slot of the computer system (see excerpt of pin descriptions below).

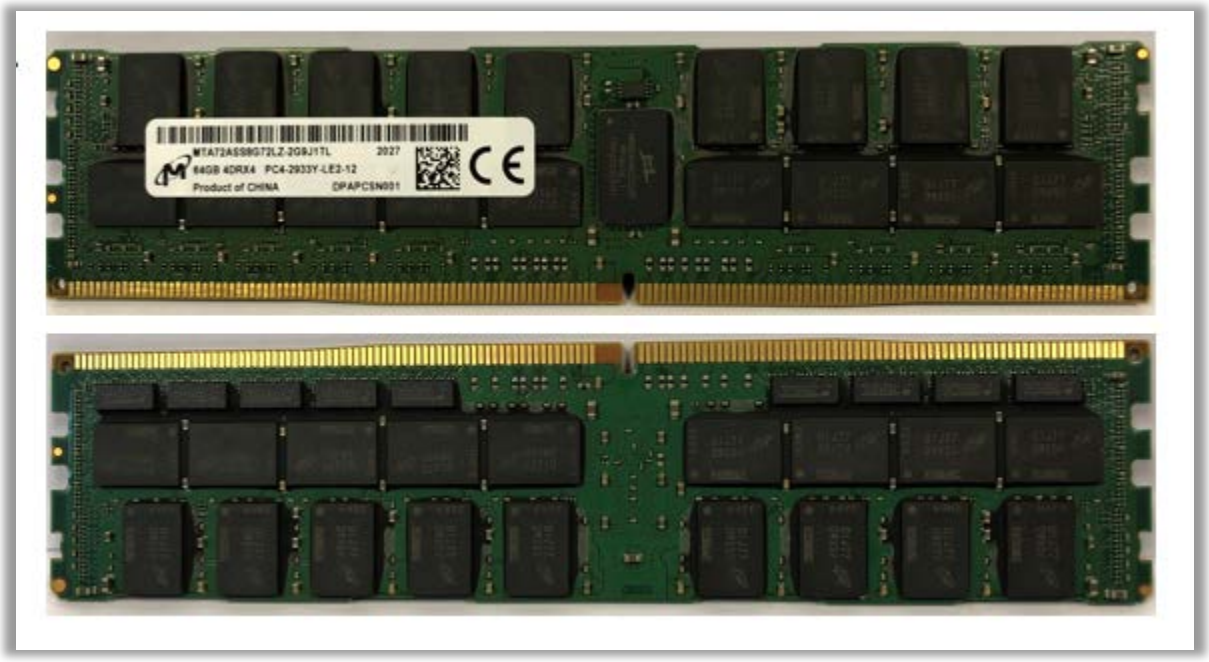
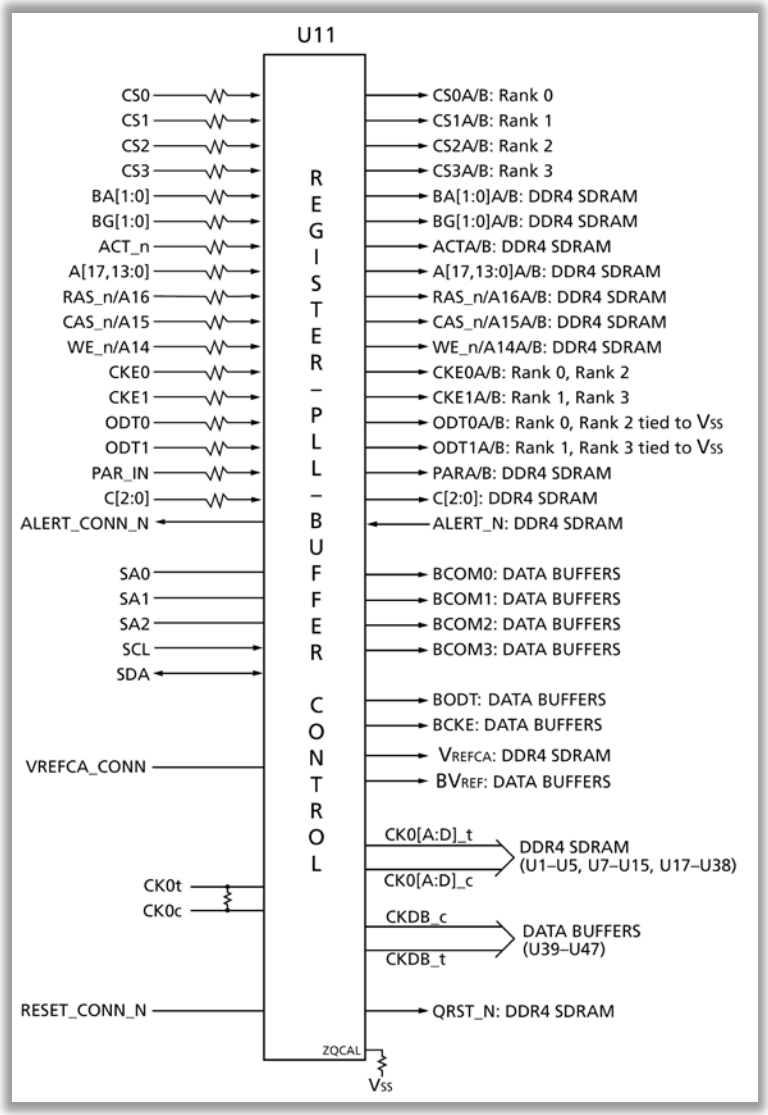


Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 5.

52. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 includes logic coupled to the PCB and configured to receive input address and control signals associated with a read or write memory command and to output registered address and control signals in response. Specifically, that functionality is supported by the RCD.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

53. The DDR4 Registering Clock Drive Definition (DDR4RCD002) of the JEDEC standard, with which the RCD complies, further shows a logic diagram specifying this configuration:

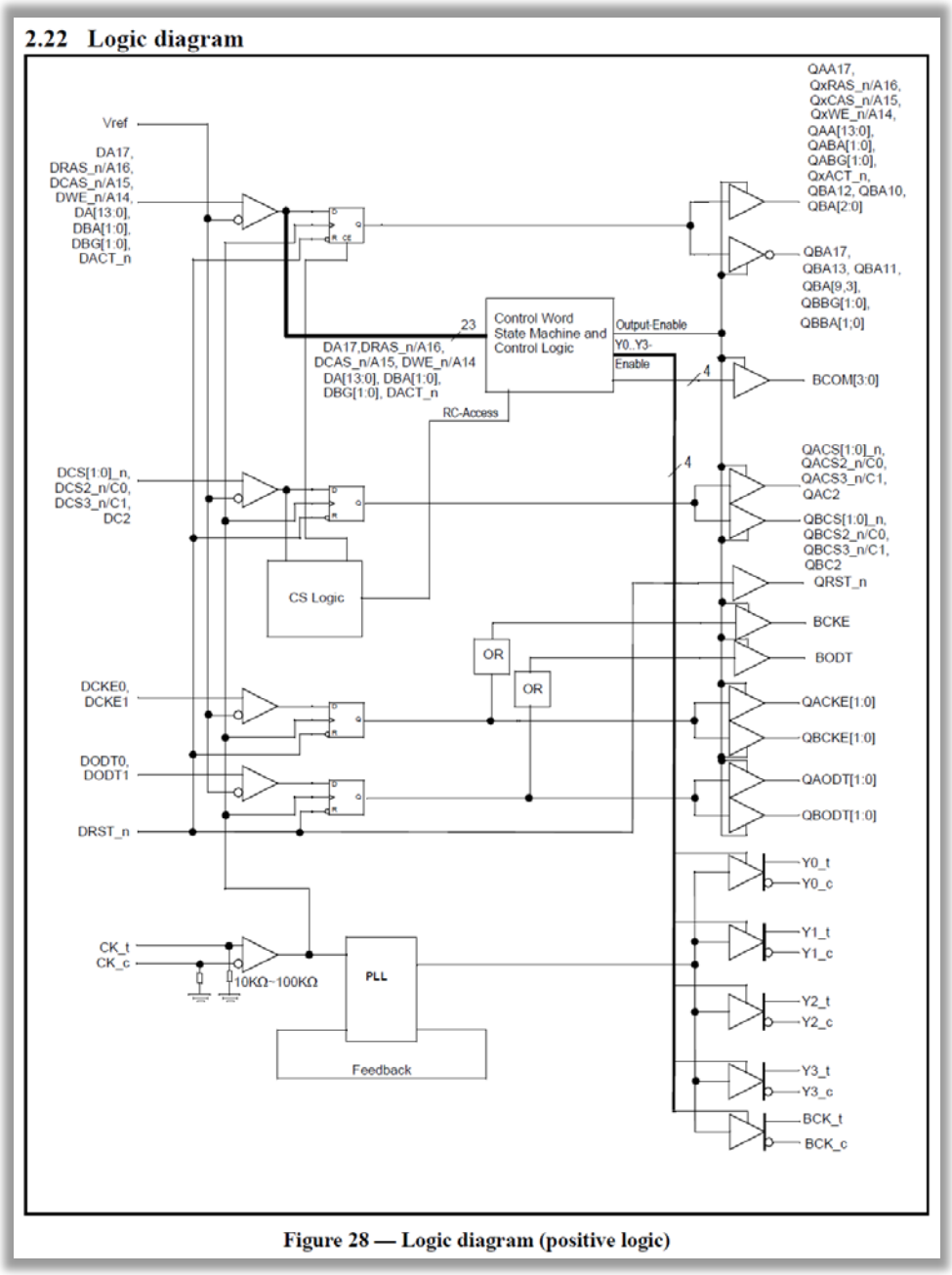
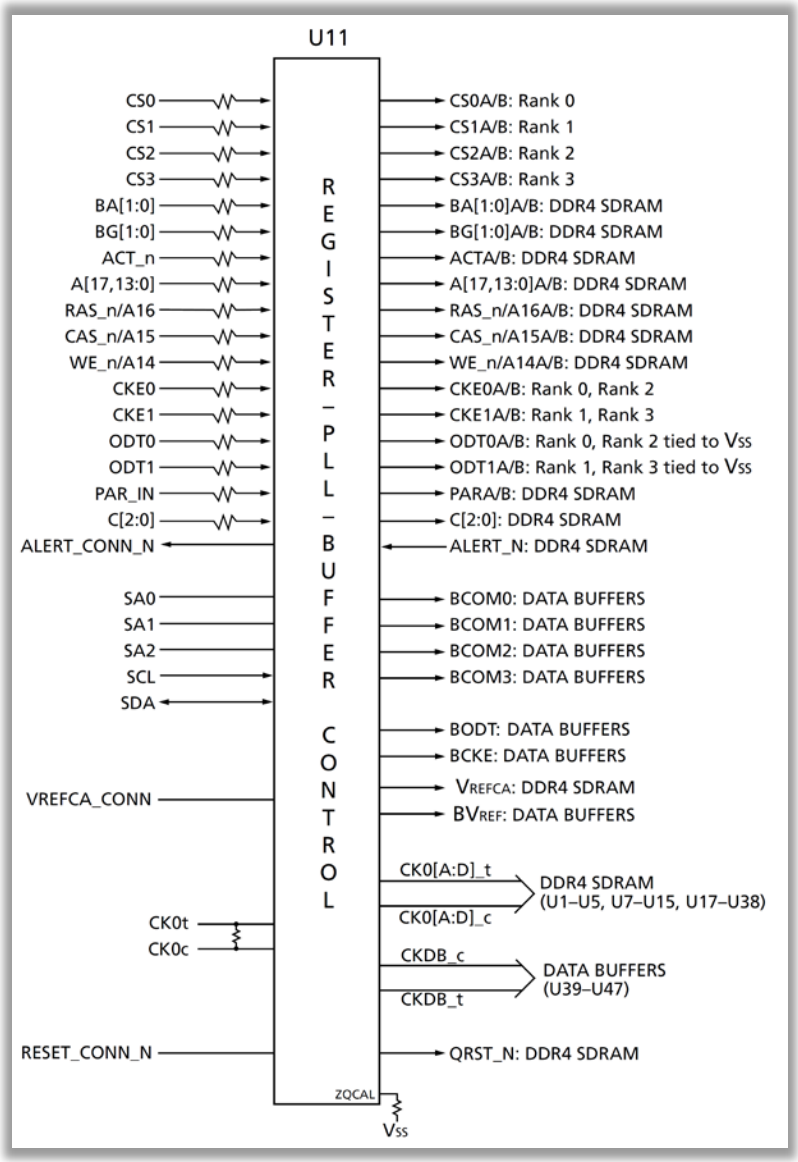


Figure 28 — Logic diagram (positive logic)

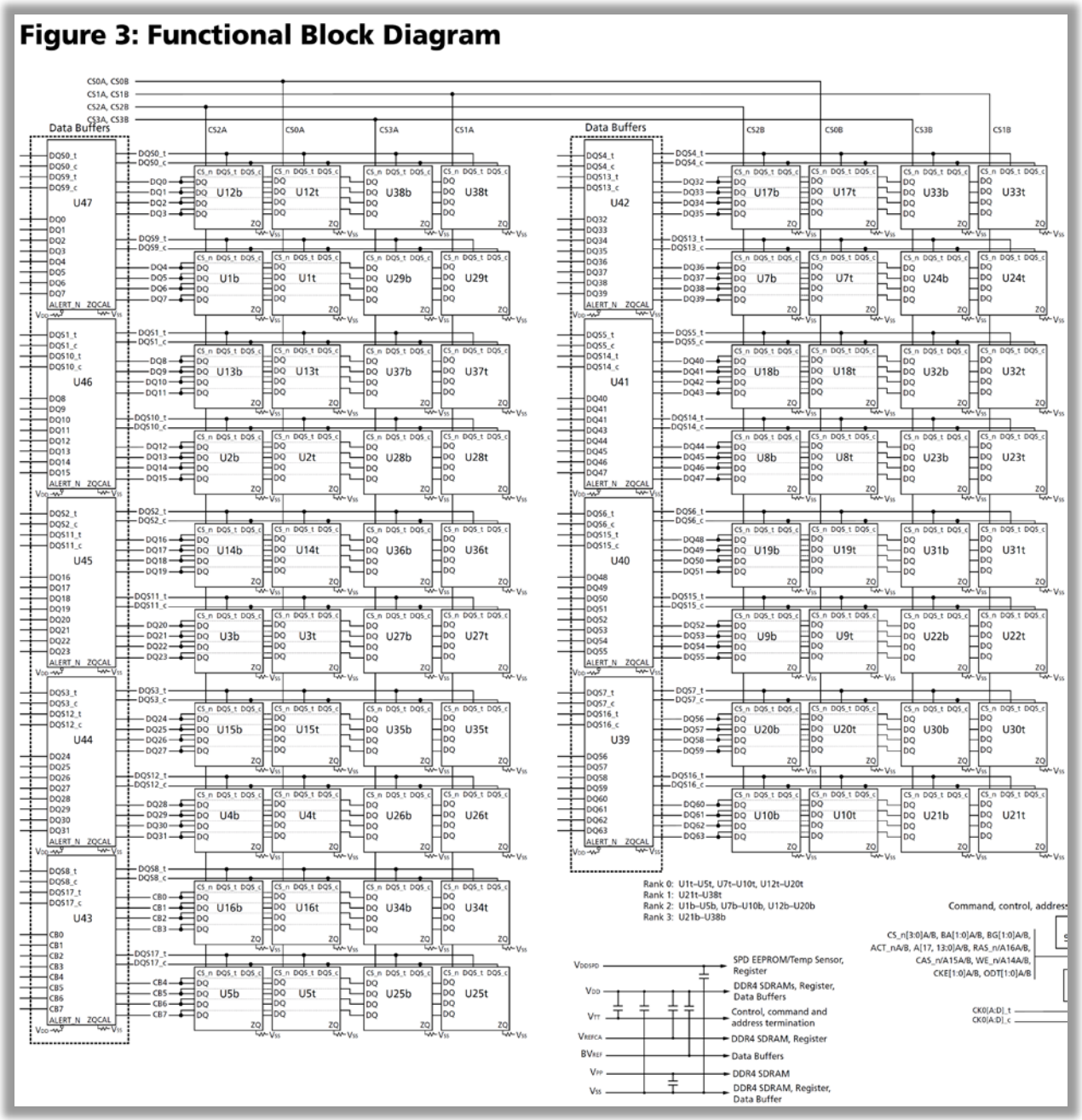
See JEDEC Standard No. 82-31A (Aug. 2019), Page 66.

54. The input address and control signals include input chip select signals and the registered address and control signals include corresponding registered chip select signals. The registered chip select signals, in turn, include a registered chip select signal having an active

signal value and one or more other registered chip select signals each having a non-active signal value.

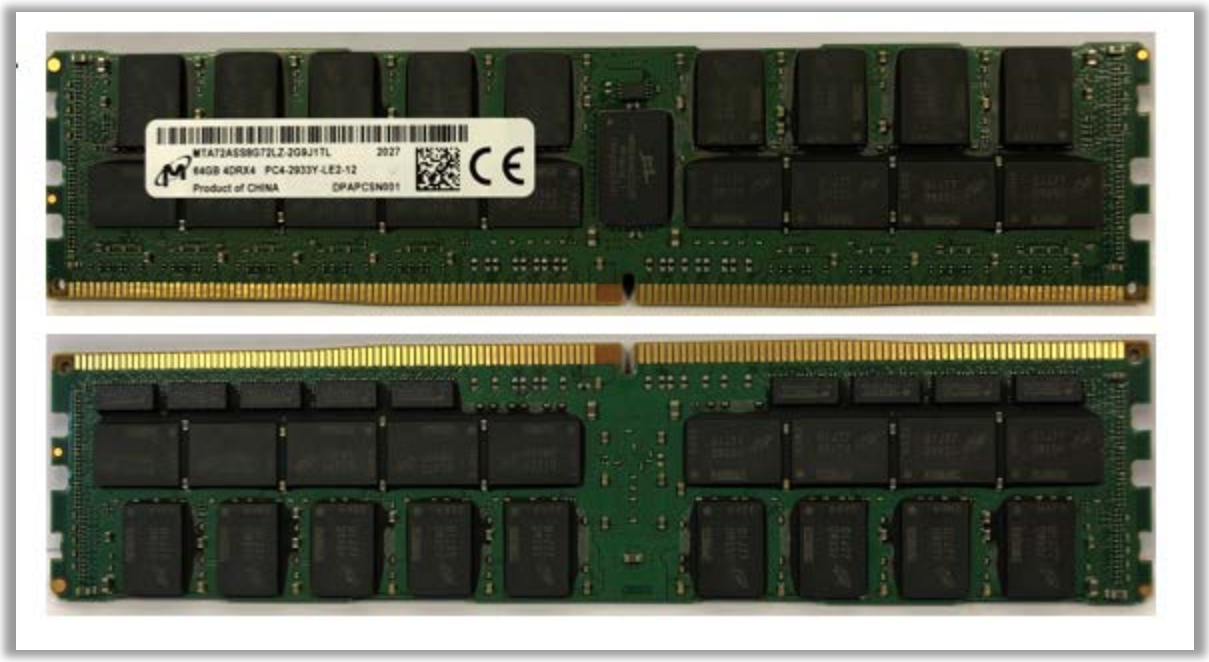


See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

55. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 includes memory devices mounted on the PCB and arranged in a plurality of N-bit wide ranks, which are configured to receive registered chip select signals.



56. An N-bit wide rank receives the registered chip select signal having the active signal value and is configured to receive or output a burst of N-bit wide data signals and a burst of data strobes associated with a read or write command. For example, the module data sheet shows:

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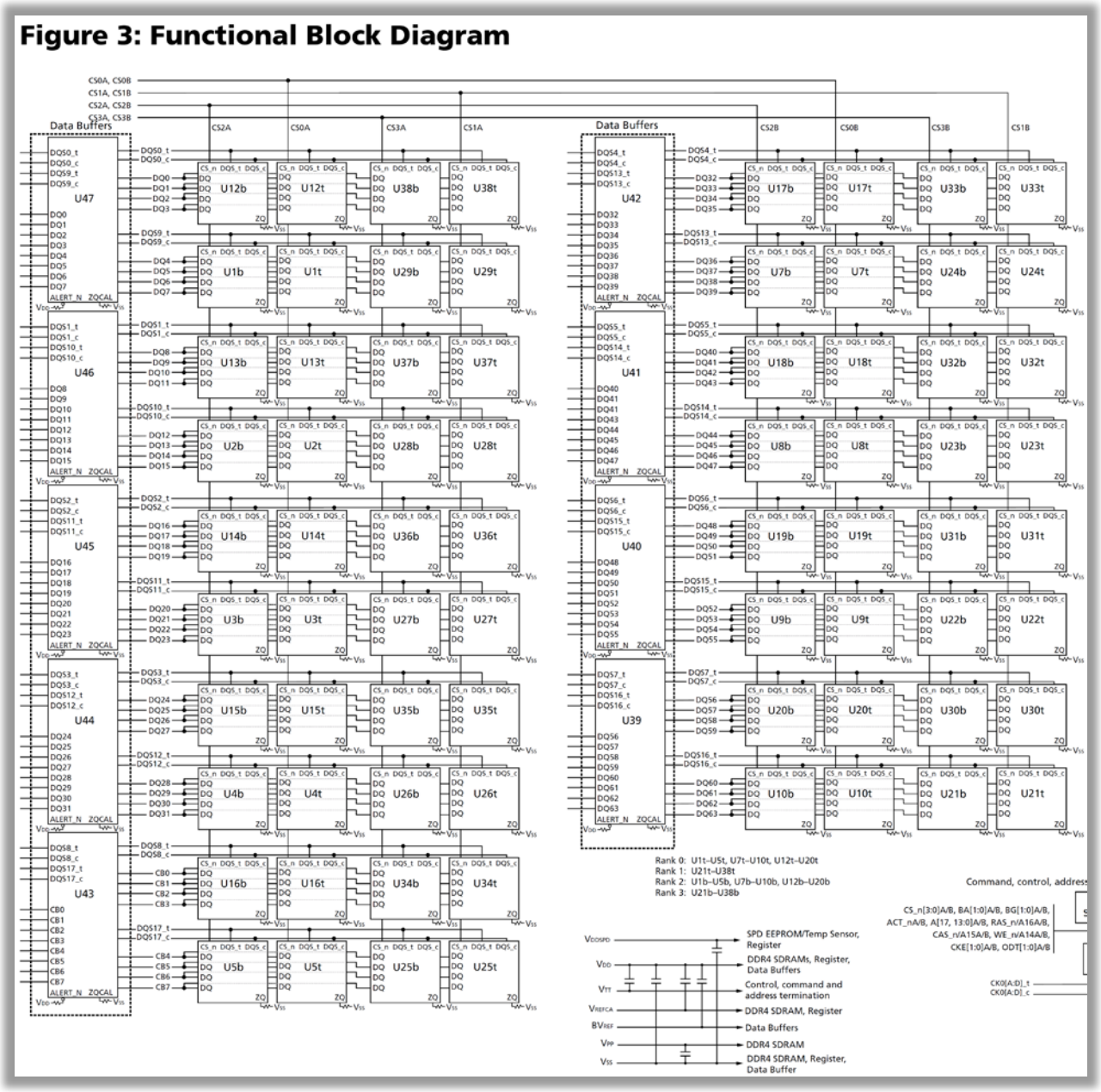
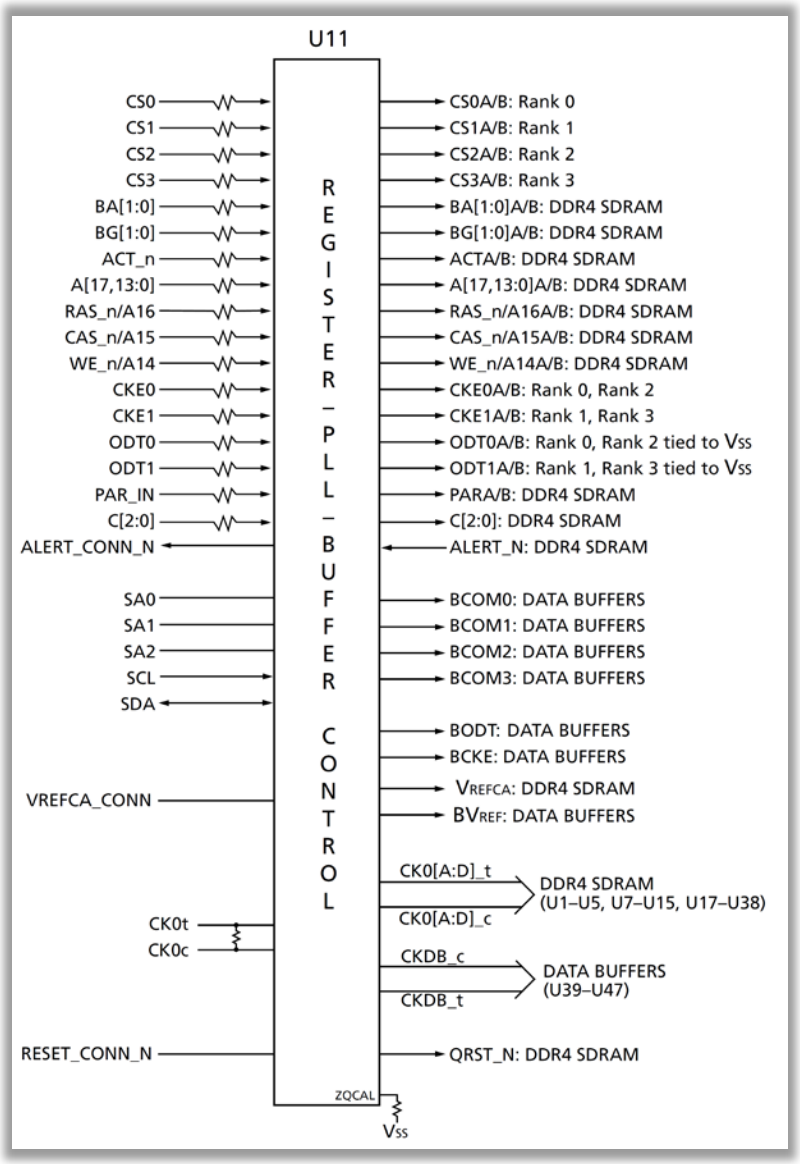


See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

57. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 includes circuitry coupled between data and strobe signal lines in the N-bit wide memory bus and corresponding data and strobe pins of memory devices in each of the plurality of N-bit wide ranks. *See id.*

58. The infringing 64GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 further includes logic configured to, in response to the read or write memory command, output control signals to the circuitry.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

59. The circuitry is configured to enable data transfers between the first rank and the memory bus through the circuitry in response to the control signals so that respective N-bit wide data signals of the burst of N-bit wide data signals and respective data strobes of the burst of data

strobes are transferred through the circuitry in accordance with an overall CAS latency of the memory module.

60. The data transfers between the first rank and the memory bus through the circuitry are registered data transfers and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry such that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the memory devices. By way of example, the following timing diagrams from the JEDEC standard from READ and WRITE operations show a predetermined amount of time delay for registered data transfers.

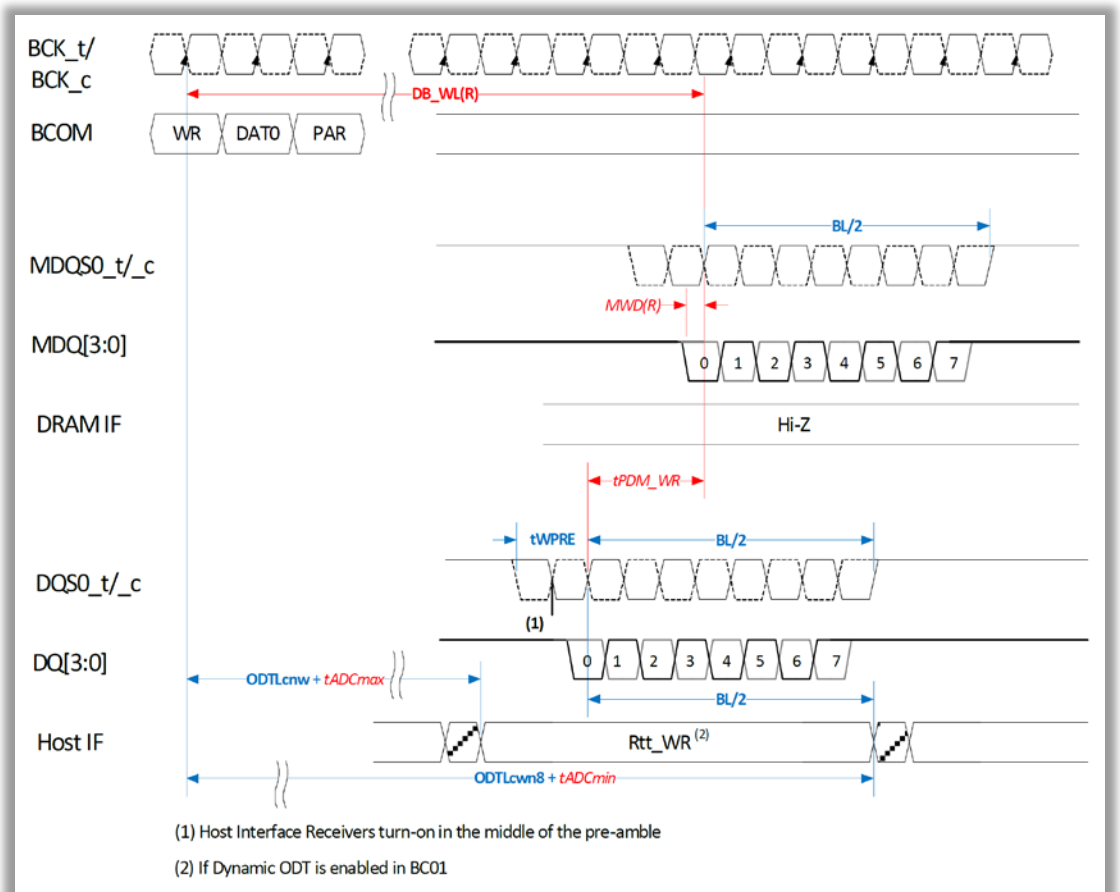


Figure 2 — WRITE Timing

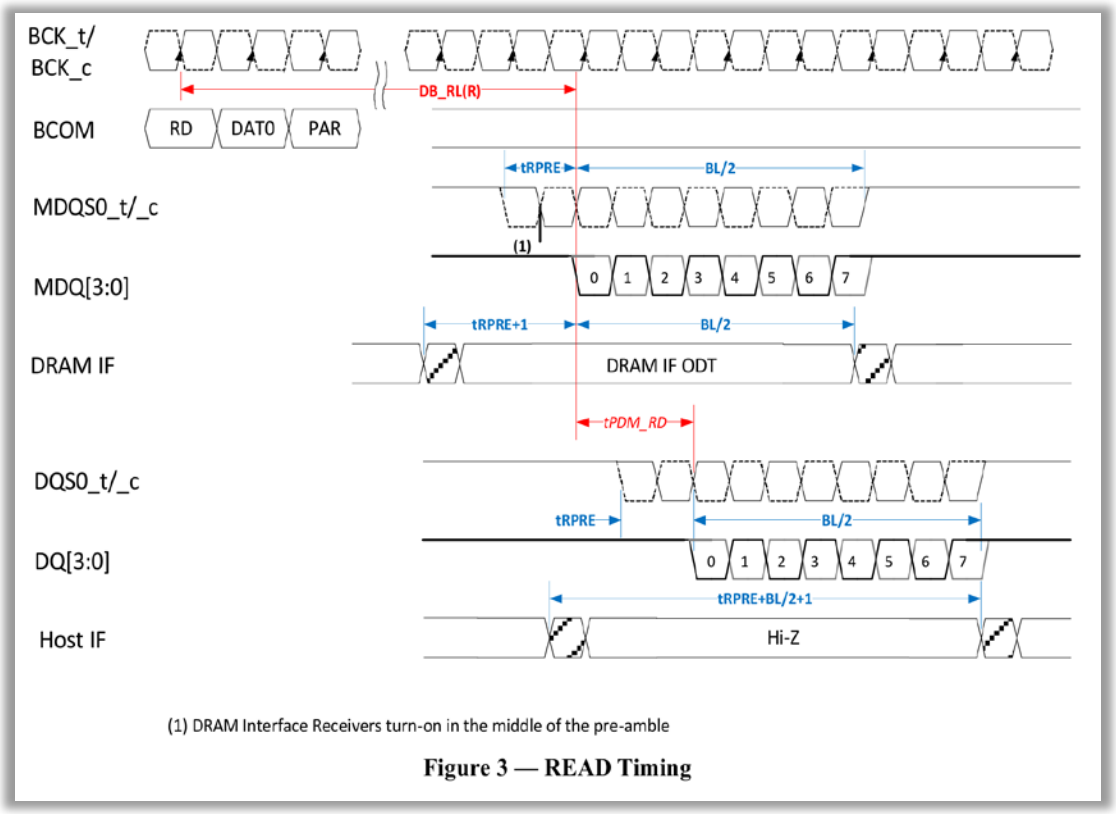


Figure 3 — READ Timing

See JEDEC Standard No. 82-32A (August 2019), Pages 13-14.

61. By infringing claim 15 and other claims of the ’314 Patent, Defendants’ Infringing Products allow for systems configured with greater memory capacity than other types of memory modules.

62. Defendants have also infringed indirectly and continue to infringe indirectly the ’314 Patent by active inducement under 35 U.S.C. § 271(b).

63. Defendants have been aware of the ’314 Patent and their infringement since no later than April 28, 2021, when Netlist informed Defendants of their infringement and offered to license the Infringing Products. By service of this Complaint, Defendants have either refused to negotiate in good faith in response to Netlist’s RAND offer, and/or have refused to pay for a license to the ’314 Patent.

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64. On information and belief, Defendants have intended, and continue to intend, to induce patent infringement by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties, incorporating their DDR4 LRDIMM memory modules and have had knowledge that the inducing acts would cause infringement or have been willfully blind to the possibility that the inducing acts would cause infringement.

65. For example, Defendants advertise and market their Load Reduced DDR4 SDRAM DIMMS by telling customers that:

> Implementing load-reduced DIMMs (LRDIMMs) enables you to add more DIMMs per channel and increase the memory capacity and speed of your systems. Our LRDIMMs use a specially designed buffer to reduce the data load to a single load (up to an 8-rank DIMM), whereas standard RDIMMs present multiple loads for dual-rank and quad-rank versions and limit the amount of data you can load to the data bus.

See Micron, Solutions, Server, LRDIMM (https://www.micron.com/solutions/server).

66. Defendants have also infringed indirectly and continue to infringe indirectly the ’314 Patent by contributory infringement under 35 U.S.C. § 271(c).

67. Defendants have and continue to intentionally commit contributory infringement by selling, offering to sell, or importing the infringing products, which include configurations that have no substantial non-infringing use, including but not limited to their DDR4 LRDIMM memory modules, with the knowledge that they will be used by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties, to directly infringe claims of the ’314 Patent.

68. Defendants have had actual knowledge of the ’314 Patent since at least April 28, 2021, when Netlist informed Defendants of their infringement of the ’314 Patent. By service of

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this Complaint, despite having actual knowledge of their infringement of the ’314 Patent, Defendants have continued to willfully, wantonly, and deliberately infringe the ’314 Patent. Defendants have either failed to negotiate in good faith, and/or refused to pay for a license to the ’314 Patent under reasonable terms. Accordingly, Plaintiff seeks enhanced damages pursuant to 35 U.S.C. § 284 and a finding that this is an exceptional case within the meaning of 35 U.S.C. § 285, entitling Plaintiff to its attorneys’ fees and expenses.

69. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’314 Patent.

70. As a result of Defendants’ infringement of the ’314 Patent and refusal to take a license to it, Plaintiff has been injured by Defendants’ unauthorized use of Plaintiff’s intellectual property.

71. Plaintiff seeks monetary damages in an amount adequate to compensate for Defendants’ infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

COUNT 2

(Willful Infringement of U.S. Patent No. 9,824,035)

72. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

73. Plaintiff is informed and believes, and on that basis alleges, that Defendants have infringed and are currently infringing one or more claims (e.g., claim 1) of the ’035 Patent, in violation of 35 U.S.C. § 271.

74. Defendants have infringed and are currently infringing literally and/or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or

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importing within this judicial district and elsewhere in the United States, without license or authority, Infringing products, including but not limited to their 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module and related products and/or processes falling within the scope of one or more claims of the ’035 Patent, including claim 1:

> A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> > a module board having edge connections for coupling to respective signal lines in the memory bus;
> >
> > a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and
> >
> > memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
> >
> > a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

75. Defendants’ acts of making, using, offering for sale, selling, and/or importing infringing products, including but not limited to their 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module and related products and/or processes satisfy,

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literally or under the doctrine of equivalents, each and every claim limitation, including but not limited to limitations of claim 1.[4]

76. For example, on information and belief, the Defendants' 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module meets each and every limitation of claim 1.

77. Defendants' 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 is a memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines.

[4] Plaintiff expressly reserves the right to identify additional asserted claims in its infringement contentions in accordance with this Court's Order Governing Procedures ("OGP") and other Standing Orders. Claim 1 is provided for notice pleading only and is not presented as an "exemplary" claim of all other claims in the '035 patent.

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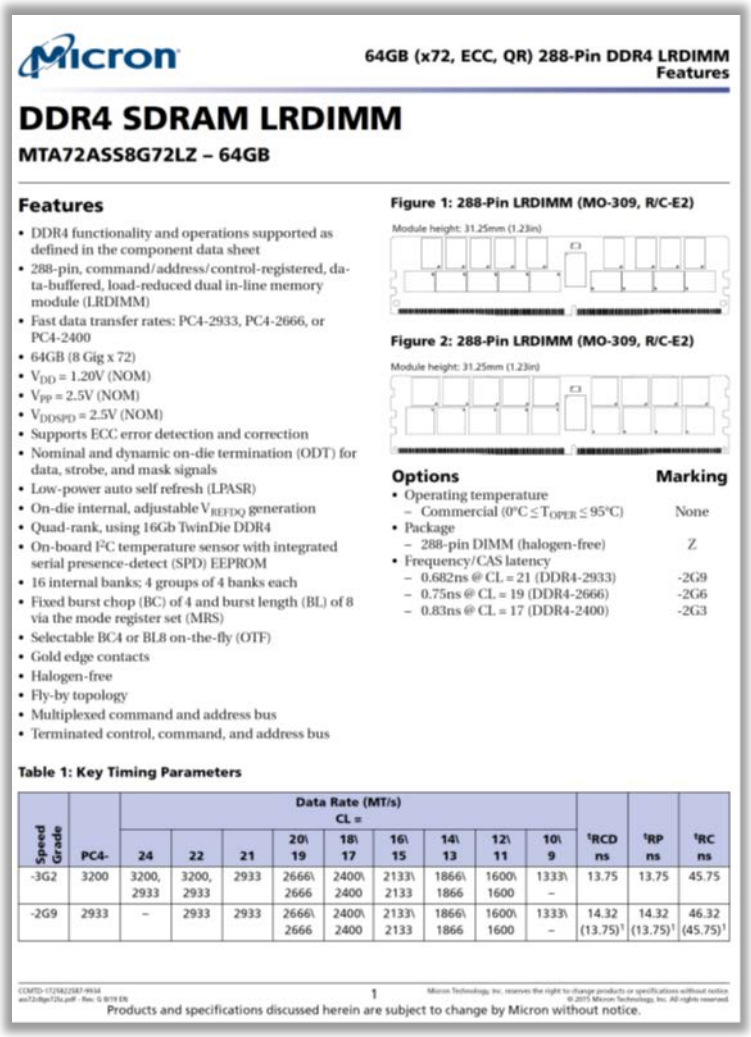


Micron

64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM
Features

DDR4 SDRAM LRDIMM

MTA72ASS8G72LZ – 64GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, command/address/control-registered, data-buffered, load-reduced dual in-line memory module (LRDIMM)
- Fast data transfer rates: PC4-2933, PC4-2666, or PC4-2400
- 64GB (8 Gig x 72)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.5V (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die internal, adjustable V_{REFDQ} generation
- Quad-rank, using 16Gb TwinDie DDR4
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Figure 1: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Figure 2: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	None
• Package	
– 288-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.682ns @ CL = 21 (DDR4-2933)	-2G9
– 0.75ns @ CL = 19 (DDR4-2666)	-2G6
– 0.83ns @ CL = 17 (DDR4-2400)	-2G3

Table 1: Key Timing Parameters

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22	21	20\19	18\17	16\15	14\13	12\11	10\9	tRCD ns	tRP ns	tRC ns
-3G2	3200	3200, 2933	3200, 2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	13.75	13.75	45.75
-2G9	2933	–	2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	14.32 (13.75)[1]	14.32 (13.75)[1]	46.32 (45.75)[1]

1

Products and specifications discussed herein are subject to change by Micron without notice.

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet (August 2019) ("Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet"), Page 1 (https://www.micron.com/products/dram-modules/lrdimm/part-catalog/mta72ass8g72lz-2g9).

78. As an LRDIMM, the 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 complies with the DDR4 SDRAM Load Reduced DIMM Design Specification promulgated by the JEDEC:

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

See JEDEC Standard No. 21C, (Aug. 2015), Page 4.20.27-5.

79. The JEDEC standard specifies a memory module operable to communicate with a memory controller via a memory bus.

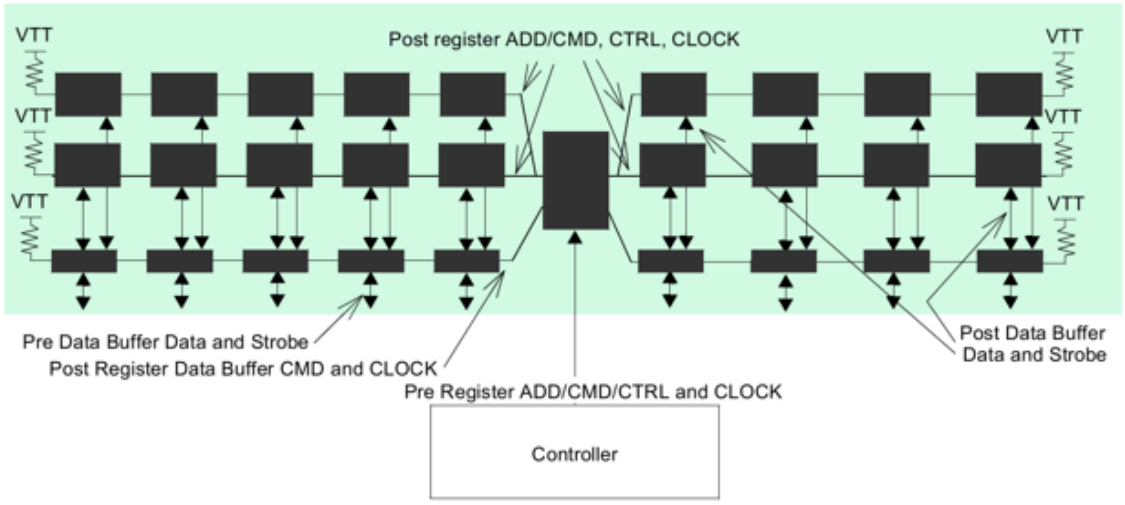
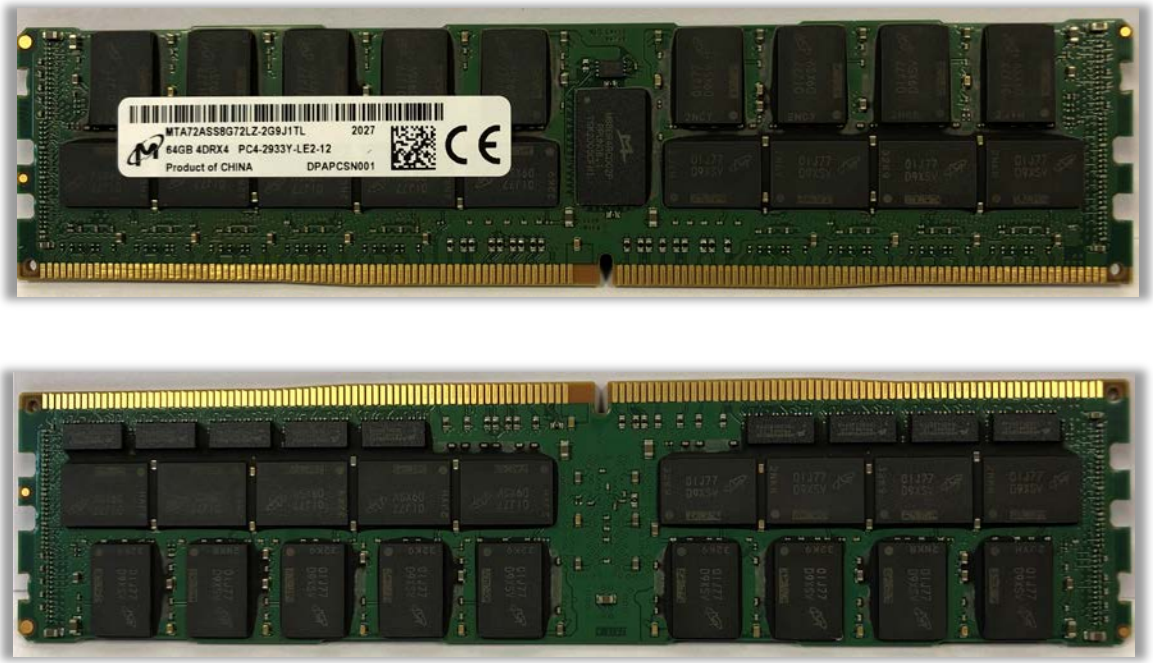


Figure 3 — LRDIMM Topologies

See JEDEC Standard No. 21C, (Aug 2015), Page 4.20.27-17.



80. The memory bus incorporated in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 includes signal lines, which include a set of control/address signal lines and a plurality of sets of data/strobe signal lines.

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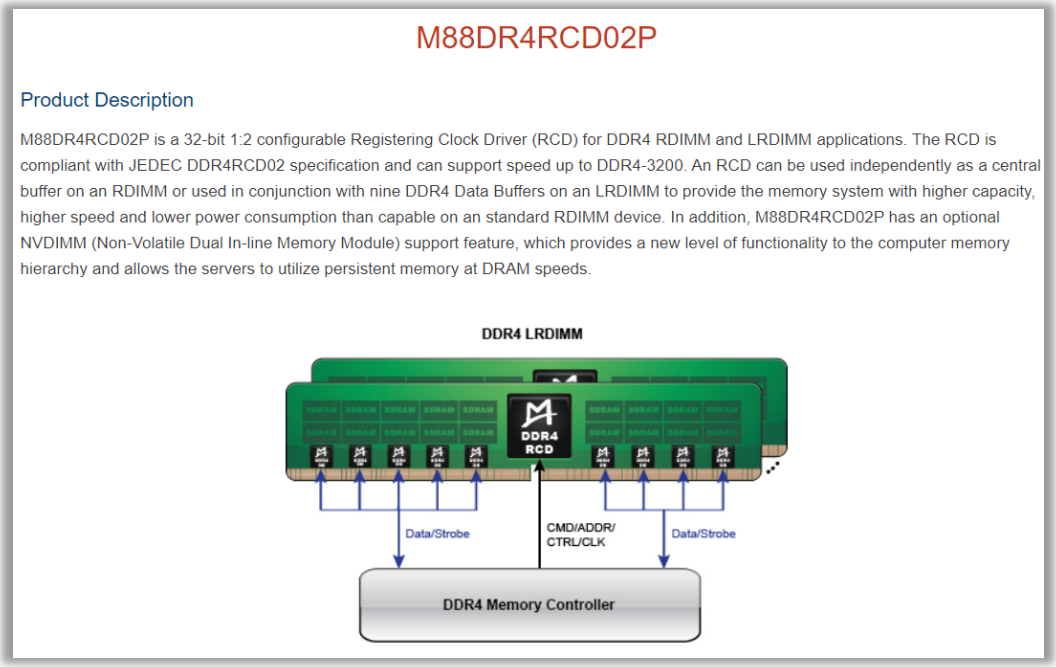
Table 4: Pin Assignments

288-Pin DDR4 LRDIMM Front								288-Pin DDR4 LRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V_{SS}	73	V_{DD}	109	V_{ss}	145	NC	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DQS14_t	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	DQS14_c	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DQS12_t	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	DQS12-c	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DQS9_t	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	DQS09_c	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	V_{SS}	225	A10_AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n/ A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	NC	263	V_{SS}
12	DQ2	48	V_{SS}	84	S0_n	120	V_{SS}	156	V_{SS}	192	CB5	228	WE_n/ A14	264	DQ49
13	V_{SS}	49	CB0	85	V_{DD}	121	DQS15_t	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n/ A15	122	DQS15_c	158	V_{SS}	194	CB1	230	NC	266	DQS6_c
15	V_{SS}	51	DQS17_t	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	DQS17_c	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	S1_n	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DQS10_t	54	CB6	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	A17	270	V_{SS}
19	DQS10_c	55	V_{SS}	91	ODT1	127	V_{SS}	163	DQS1_c	199	CB7	235	NF	271	DQ51
20	V_{SS}	56	CB2	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	S2_n	129	V_{SS}	165	V_{SS}	201	CB3	237	S3_n	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DQS16_t	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}
25	DQ20	61	V_{DD}	97	DQ32	133	DQS16_c	169	V_{SS}	205	NC	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DQS13_t	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	V_{DD}	100	DQS13_c	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DQS11_t	65	A12	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	DQS11_c	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{ss}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	NC	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 4.

81. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a module board having edge connections for coupling to respective signal lines in the memory bus.

82. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a module control device mounted on the module board and configured to receive memory command signals.



M88DR4RCD02P

Product Description

M88DR4RCD02P is a 32-bit 1:2 configurable Registering Clock Driver (RCD) for DDR4 RDIMM and LRDIMM applications. The RCD is compliant with JEDEC DDR4RCD02 specification and can support speed up to DDR4-3200. An RCD can be used independently as a central buffer on an RDIMM or used in conjunction with nine DDR4 Data Buffers on an LRDIMM to provide the memory system with higher capacity, higher speed and lower power consumption than capable on an standard RDIMM device. In addition, M88DR4RCD02P has an optional NVDIMM (Non-Volatile Dual In-line Memory Module) support feature, which provides a new level of functionality to the computer memory hierarchy and allows the servers to utilize persistent memory at DRAM speeds.

See https://www.montage-tech.com/Memory_Interface/DDR4/M88DR4RCD02P.

83. The module control device in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 is configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals.

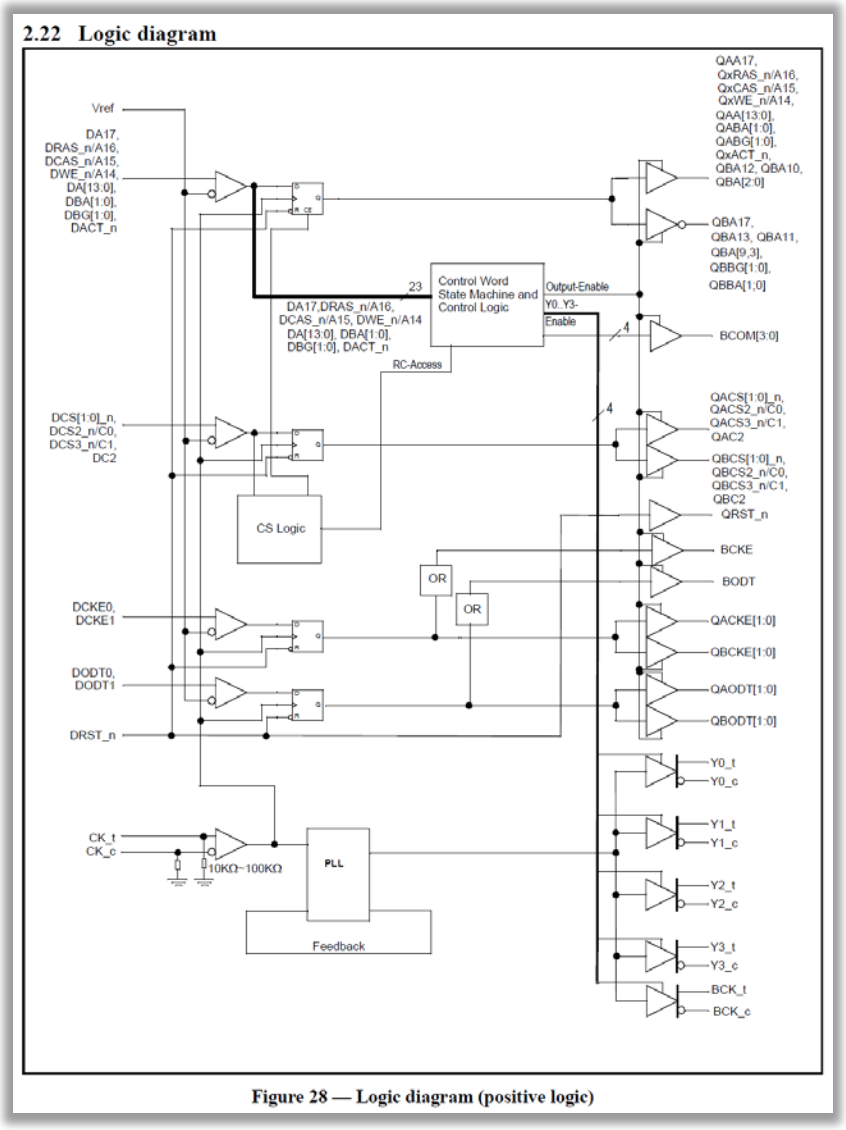


Figure 28 — Logic diagram (positive logic)

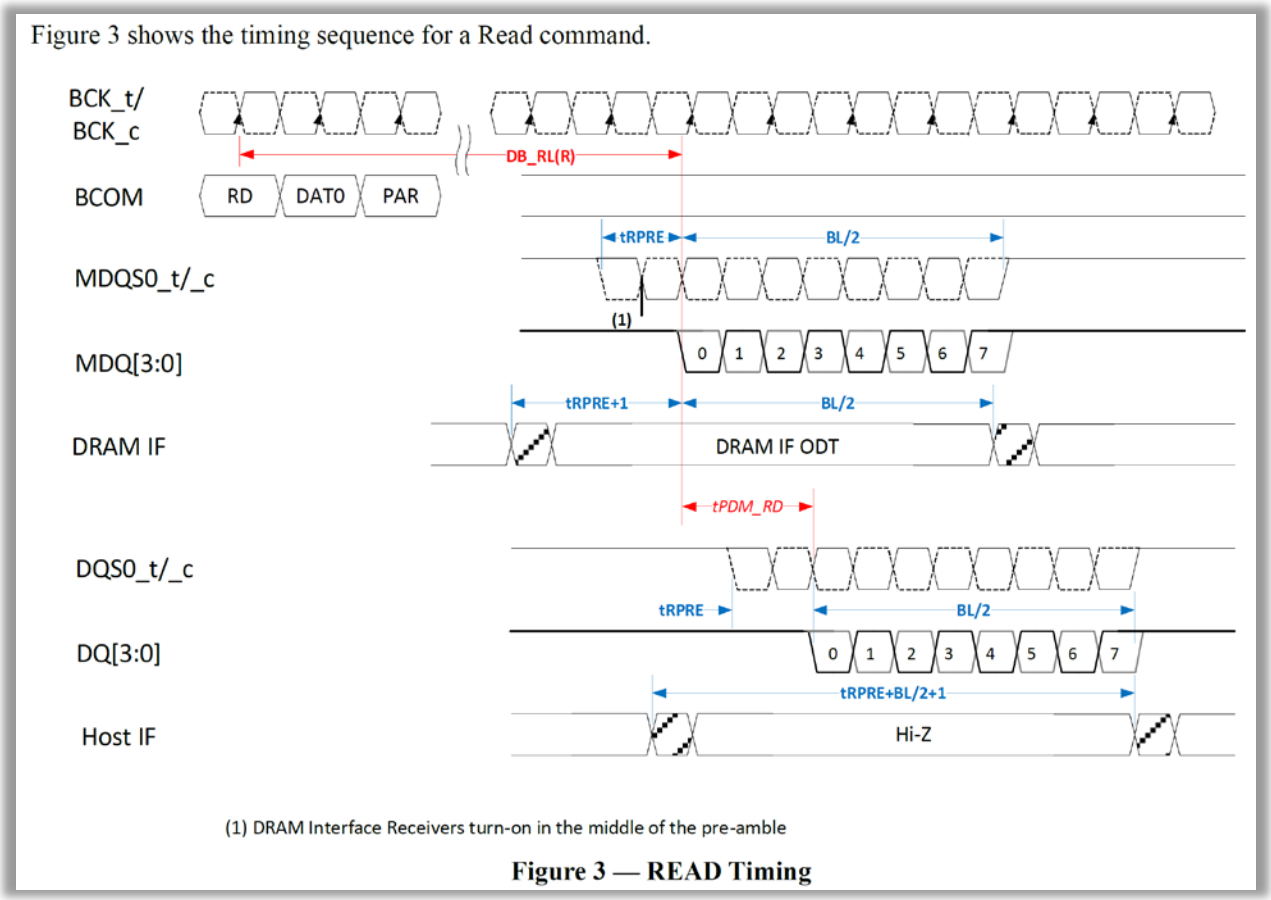
See JEDEC Standard No. 82-31A, (August 2019), Page 66.

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

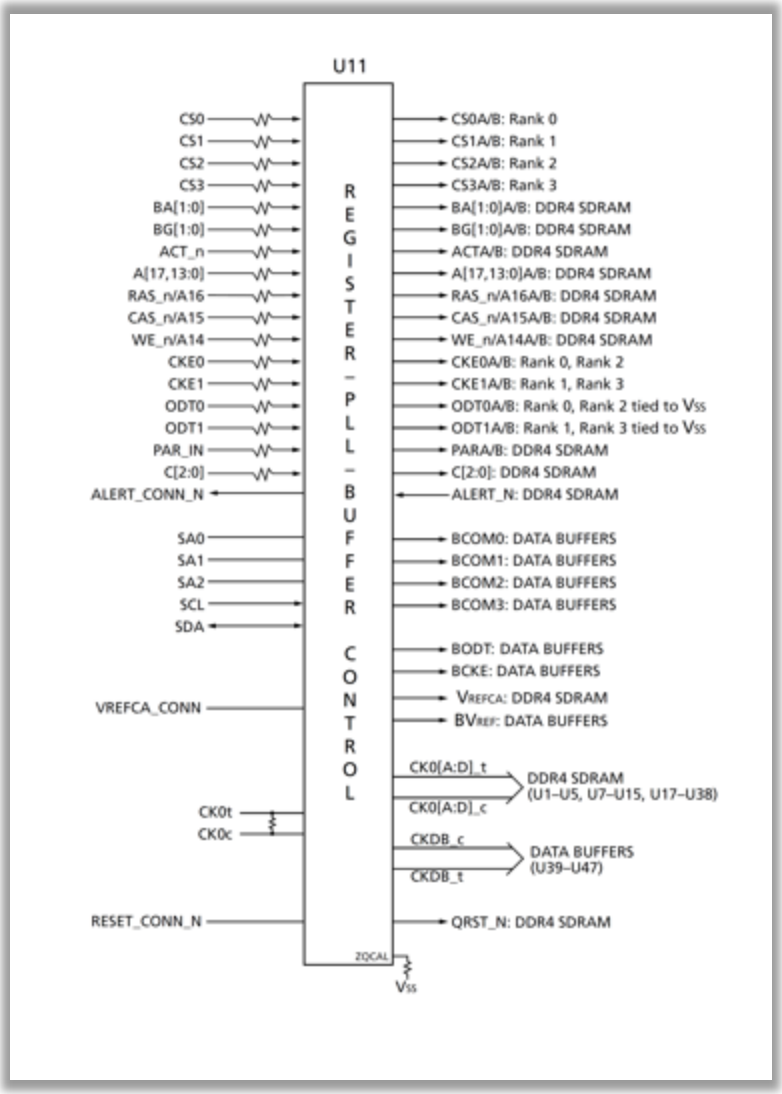
1. RFU commands are treated as NOP commands for command sequence error detection

See JEDEC Standard No. 82-31A (August 2019), Page 14.



See JEDEC Standard No. 82-32A (August 2019), Page 14.

84. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101

See JEDEC Standard No. 82-32A (August 2019), Page 4.

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

See JEDEC Standard No. 82-31A (August 2019), Page 14.

Figure 3 shows the timing sequence for a Read command.

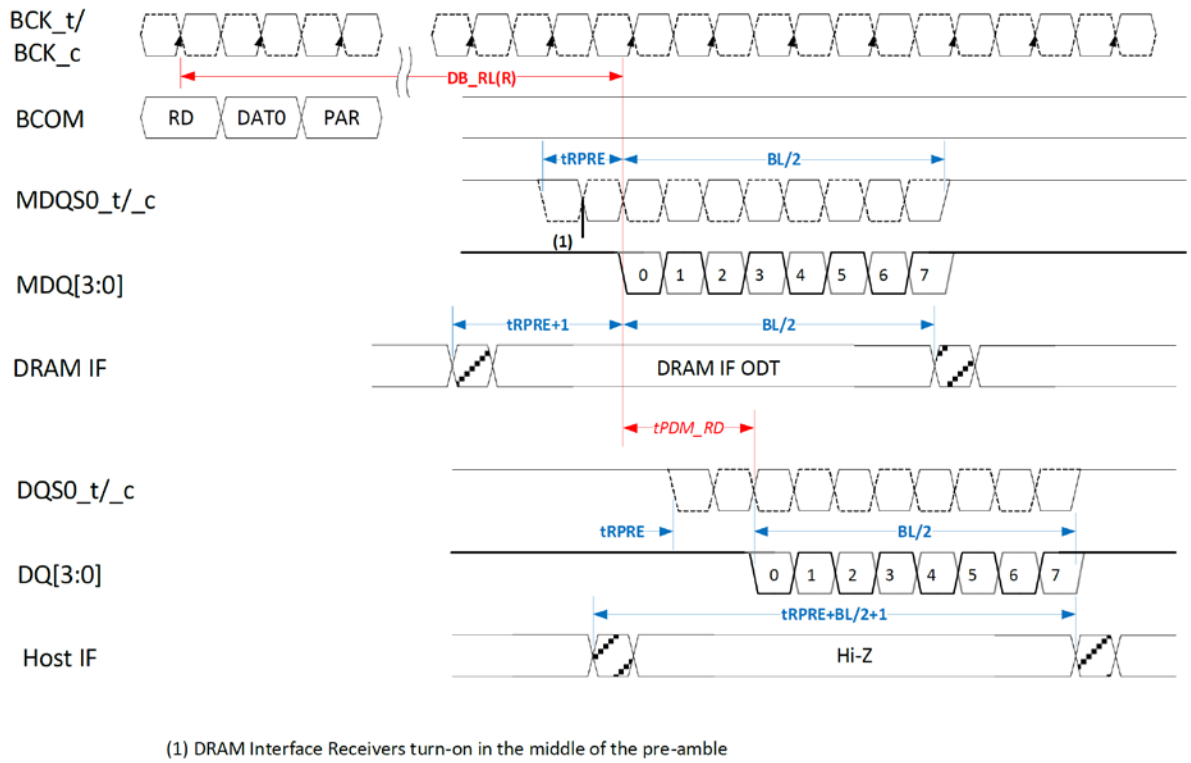


Figure 3 — READ Timing

See JEDEC Standard No. 82-32A (August 2019), Page 14.

85. The memory devices in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 include a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines.

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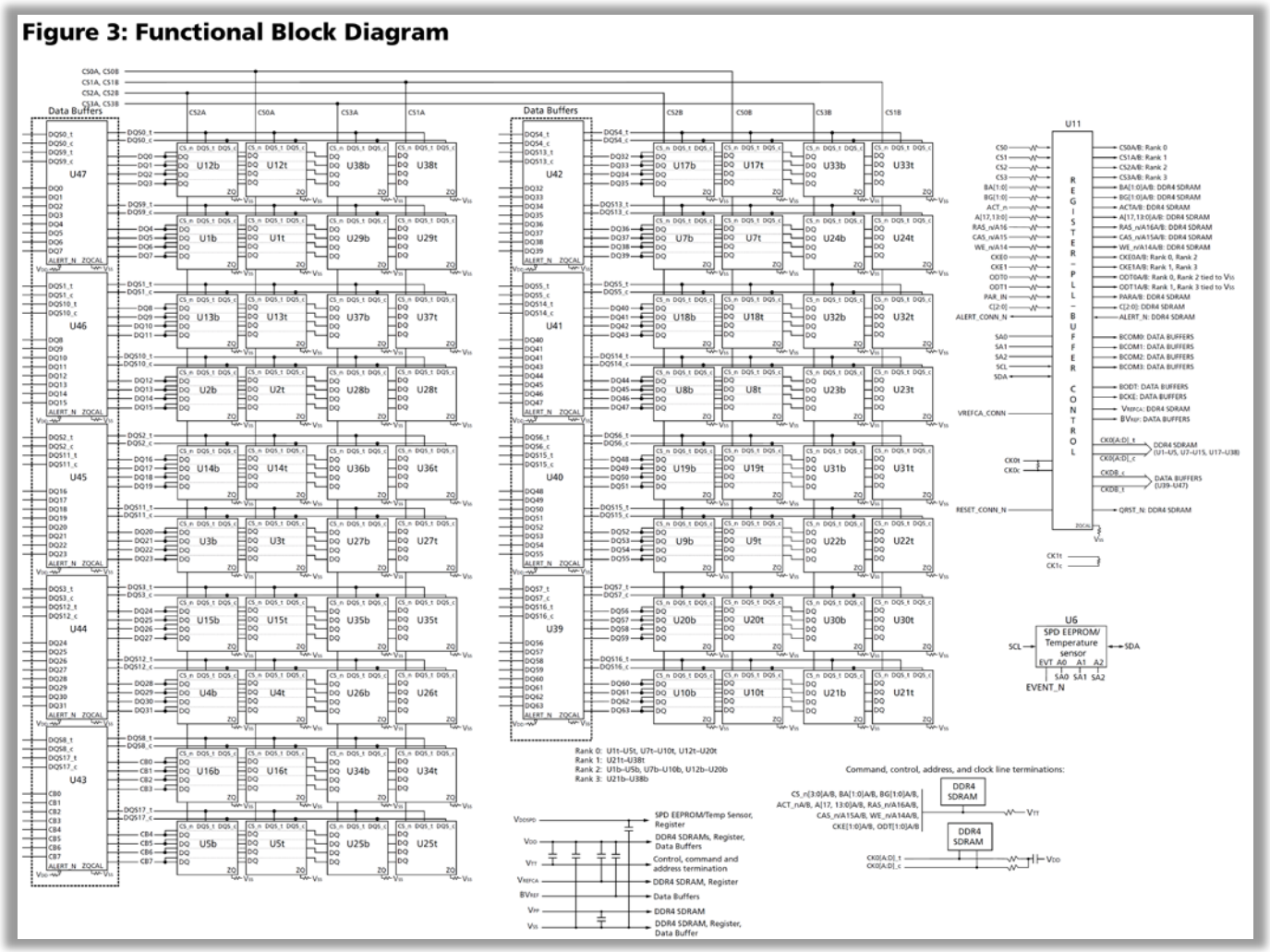
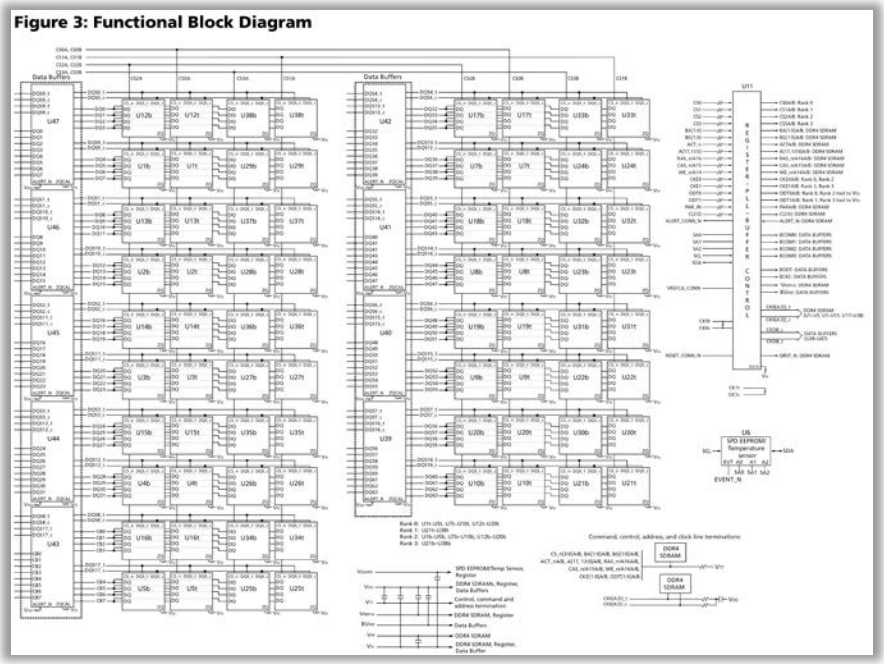


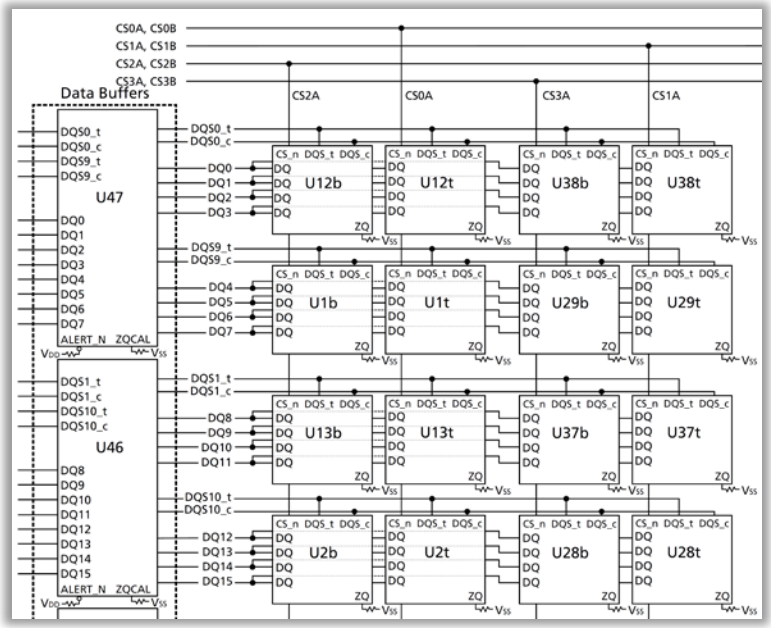
See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

86. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

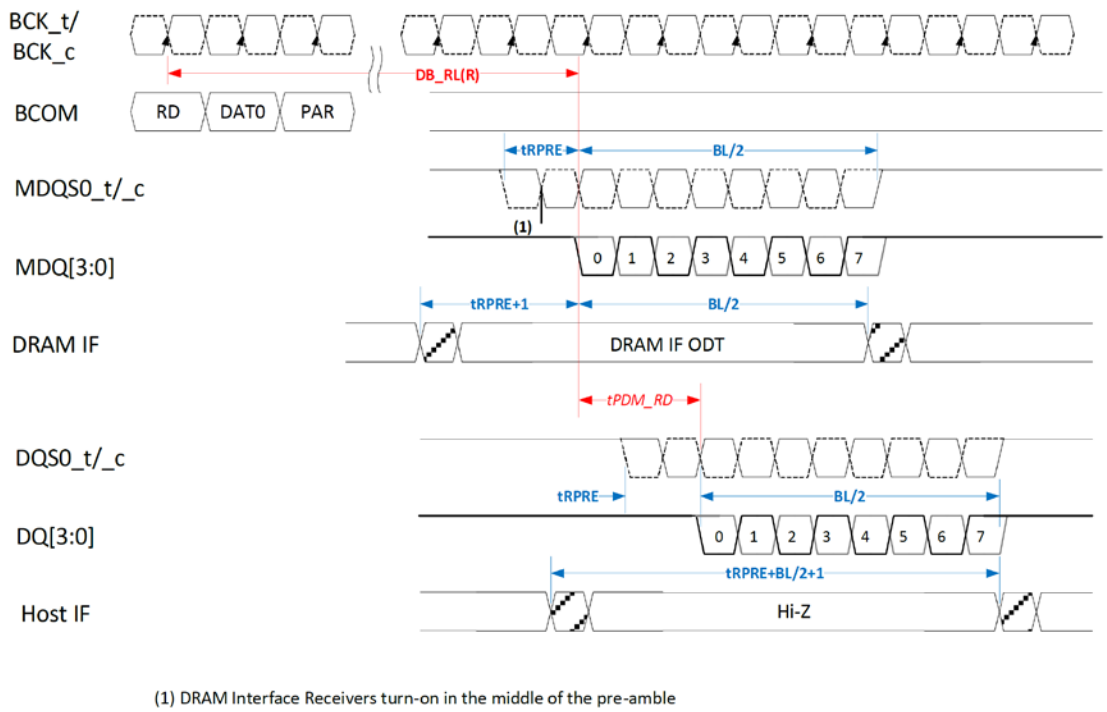
87. In the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9, each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

88. In the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9, each respective buffer circuit includes data paths for transmitting respective data and strobe signals associated with the first memory operation.

Figure 3 shows the timing sequence for a Read command.



(1) DRAM Interface Receivers turn-on in the middle of the pre-amble

Figure 3 — READ Timing

See JEDEC Standard No. 82-32A (August 2019), Page 14.

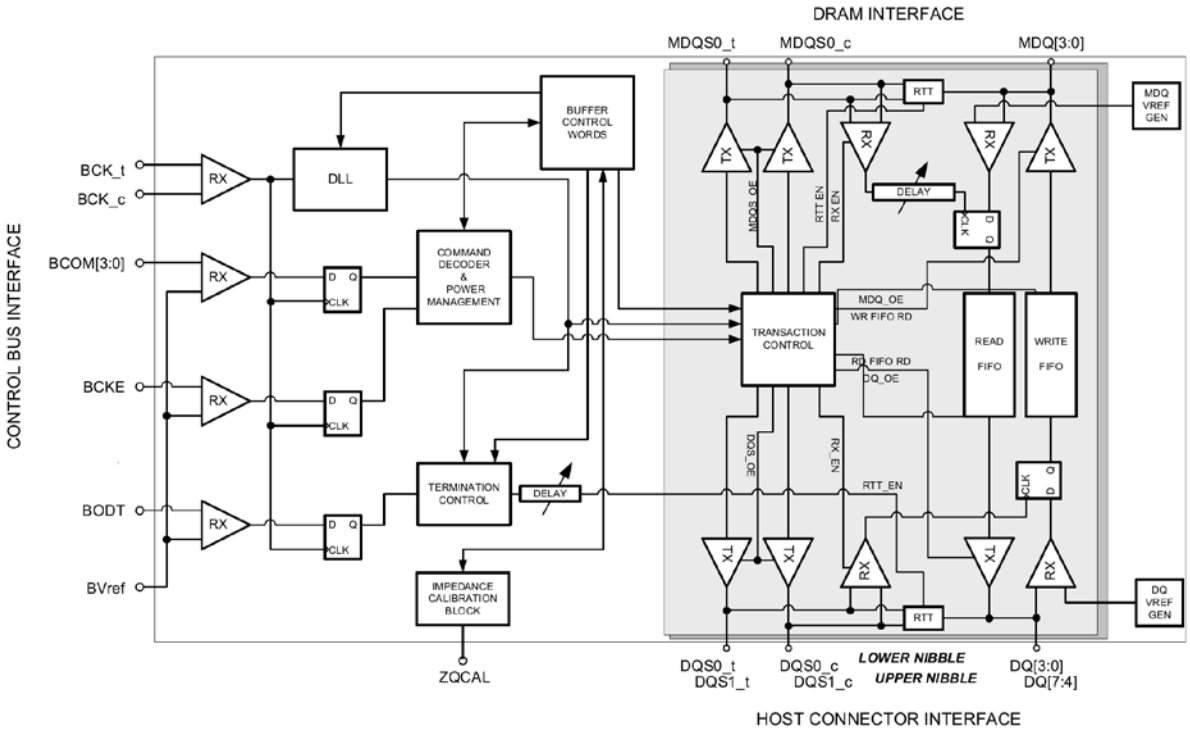


Figure 15 — Logic Diagram

See JEDEC Standard No. 82-32A (August 2019), Page 95.

89. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 incorporates logic configured to respond to the module control signals by enabling the data paths. *See id.*

90. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 incorporates logic that is further configured to obtain timing information based on one or more signals received by each respective buffer circuit during a second memory operation prior to the first memory operation.

Table 16 below provides an overview of the buffer control words (BCW) that are involved in the timing control and timing training features of the DDR4DB02.

Table 16 — Timing and Training Control Words

Address	Description	Scope
BC0C	Training control word	Training mode enable
F0BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 0	Additional cycles of DRAM Interface Receive Enable Delay and Write Leveling Delay per rank and per nibble
F0BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 0	
F0BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 2	
F0BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 2	
F1BCCx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 1	
F1BCDx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 1	
F1BCEx	Lower/Upper Nibble Additional Cycles of DRAM Interface Receive Enable Control Word for Rank 3	
F1BCFx	Lower/Upper Nibble Additional Cycles of DRAM Interface Write Leveling Control Word for Rank 3	
F[3:0]BC2x	Lower nibble DRAM interface receive enable training control	DRAM Interface Receive Enable phase and cycle control per rank
F[3:0]BC3x	Upper nibble DRAM interface receive enable training control	
F[3:0]BC4x	Lower nibble MDQS read delay control	Input MDQS delay control per rank
F[3:0]BC5x	Upper nibble MDQS read delay control	
F[3:0]BC8x	Lower nibble MDQ-MDQS write delay control	Output MDQ signal phase control per rank
F[3:0]BC9x	Upper nibble MDQ-MDQS write delay control	
F[3:0]BCAx	Lower nibble host interface write leveling control	Host Interface write leveling phase and cycle control per rank
F[3:0]BCBx	Upper nibble host interface write leveling training control	
F5BC0x - F5BC3x F6BC0x - F6BC3x	Lower and upper nibble Multi Purpose Registers[7:0]	Store read/write data patterns for receive enable, read and write delay and host interface write training as well as MPR override mode.
F6BC4x	Buffer training configuration control word	Configuration control for certain training modes
F6BC5x	Buffer training status word	Status for certain training modes
F[7:4]BC8x	MDQ0/4-Read delay control	Input MDQS delay control per rank and per lane
F[7:4]BC9x	MDQ1/5-Read delay control	
F[7:4]BCAx	MDQ2/6-Read delay control	
F[7:4]BCBx	MDQ3/7-Read delay control	
F[7:4]BCCx	MDQ0/4-MDQS write delay control	Output MDQ signal phase control per rank and per lane
F[7:4]BCDx	MDQ1/5-MDQS write delay control	
F[7:4]BCEx	MDQ2/6-MDQS write delay control	
F[7:4]BCFx	MDQ3/7-MDQS write delay control	

See JEDEC Standard No. 82-32A (August 2019), Page 27.

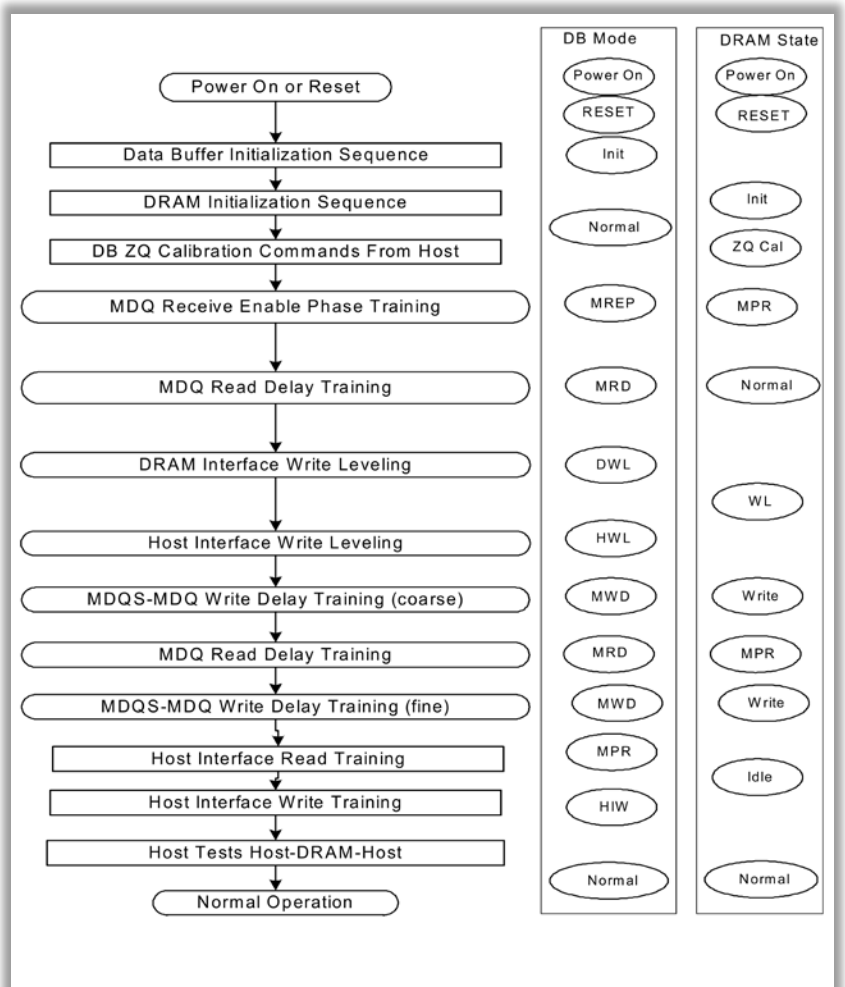


Figure 10 — Example of Training Sequence Flow Diagram

See JEDEC Standard No. 82-32A (August 2019), Page 29.

2.20.4 DRAM-to-DB Read Delay (MRD) Training Mode

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM (either from its internal array or from the MPRs for data-preserving read training). The data buffer provides data pattern control words that are programmed with the expected read data from the DRAM and the results of the comparison is provided on the data buffers host interface.

To perform DRAM-to-DB read training, the host will first enable the MDQS read delay training mode in the Training Mode Control Word (BC0C).

The delay of the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) during read transactions is selected by buffer control word F[3:0]BC4x and F[3:0]BC5x for lower and upper nibble respectively. The nominal setting for F[3:0]BC4x/F[3:0]BC5x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into F[3:0]BC4x/F[3:0]BC5x. Since the DDR4DB02 uses the RANK ID fields in the BCOM Read Command sequences to select the correct DRAM interface receive enable timings for the reads from the DRAMs, the content of BC08 DA[1:0] is don't care while in this training mode.

In this training mode, the data buffer uses a data pattern comparator to determine if the read data arriving from the DRAMs after a Read command match an expected result. There is one data comparator per data buffer. The output of the data comparator is driven onto the eight host connector interface DQ pins corresponding. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. Bit 0 of the Buffer Training Configuration control word F6BC4x selects whether all four DQ bits within a nibble are driven to '0' if there is any mismatch in any of the 32 bits associated with that nibble or whether only the DQ bit(s) of the particular lane(s) (i.e. the series of 8 bits arriving on the same DQ bit) that had one or more mismatches are driven to '0'. The expected data pattern values are stored in the MPR control words F5BC0x through F5BC3x and F6BC0x through F6BC3x.

MPR0[7:0] will contain the expected first UI (UI0) for MDQ[7:0] and MPR7[7:0] will contain the expected last UI(UI7) for MDQ[7:0], or in a general sense: MPRx[7:0] should match UIx for MDQ[7:0].

The 64 bits contained in these data registers can support arbitrary data patterns in a single BL8 data transaction. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The DDR4DB02 is required to support fine adjustment of the phase of individual bit lanes relative to the baseline MDQS for DDR4 data rates above 2400 MT/s-. For this purpose the host controller can utilize the per lane MDQS-MDQ read delay control words F[7:4]BC8x through F[7:4]BCBx. F4BC8x controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BC9x controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS

See JEDEC Standard No. 82-32A (August 2019), Page 32.

91. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 incorporates logic that is further configured to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.

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Ex. 1016, p. 51

2.20.4 DRAM-to-DB Read Delay (MRD) Training Mode

For the DRAM-to-DB read training, the MDQS delay adjustments are performed in the data buffer so that it can correctly sample the data driven by the DRAM (either from its internal array or from the MPRs for data-preserving read training). The data buffer provides data pattern control words that are programmed with the expected read data from the DRAM and the results of the comparison is provided on the data buffers host interface.

To perform DRAM-to-DB read training, the host will first enable the MDQS read delay training mode in the Training Mode Control Word (BC0C).

The delay of the DRAM interface data strobe signals (MDQSx_t/MDQSx_c) during read transactions is selected by buffer control word F[3:0]BC4x and F[3:0]BC5x for lower and upper nibble respectively. The nominal setting for F[3:0]BC4x/F[3:0]BC5x is one quarter of a cycle delay. The host controller may need to perform additional iterations of the training procedures, including Host Interface Read Training, when non-default settings are written into F[3:0]BC4x/F[3:0]BC5x. Since the DDR4DB02 uses the RANK ID fields in the BCOM Read Command sequences to select the correct DRAM interface receive enable timings for the reads from the DRAMs, the content of BC08 DA[1:0] is don't care while in this training mode.

In this training mode, the data buffer uses a data pattern comparator to determine if the read data arriving from the DRAMs after a Read command match an expected result. There is one data comparator per data buffer. The output of the data comparator is driven onto the eight host connector interface DQ pins corresponding. If the data pattern is matched, the DQ pins are driven to '1' until the next comparison takes place or until the training mode is disabled. If the data pattern is not matched, the DQ pins are driven to '0'. Bit 0 of the Buffer Training Configuration control word F6BC4x selects whether all four DQ bits within a nibble are driven to '0' if there is any mismatch in any of the 32 bits associated with that nibble or whether only the DQ bit(s) of the particular lane(s) (i.e. the series of 8 bits arriving on the same DQ bit) that had one or more mismatches are driven to '0'. The expected data pattern values are stored in the MPR control words F5BC0x through F5BC3x and F6BC0x through F6BC3x.

MPR0[7:0] will contain the expected first UI (UI0) for MDQ[7:0] and MPR7[7:0] will contain the expected last UI(UI7) for MDQ[7:0], or in a general sense: MPRx[7:0] should match UIx for MDQ[7:0].

The 64 bits contained in these data registers can support arbitrary data patterns in a single BL8 data transaction. In addition to driving the DQ pins, status for the MRD training mode is also provided in the Buffer Training Status word (F6BC5x). The status provided in F6BC5x can be modified by the Buffer Training Configuration control word (F6BC4x).

The DDR4DB02 is required to support fine adjustment of the phase of individual bit lanes relative to the baseline MDQS for DDR4 data rates above 2400 MT/s-. For this purpose the host controller can utilize the per lane MDQS-MDQ read delay control words F[7:4]BC8x through F[7:4]BCBx. F4BC8x controls the phase of bits MDQ0 and MDQ4 within the lower and upper nibble respectively for Rank 0, F5BC9x controls the phase bits MDQ1 and MDQ5 for Rank 1, and so on. Since all bits within a nibble a generally aligned by routing, only a small range of +/- 3 * 1/64 * t_{CK} is provided for fine-grained adjustment of individual bit lane delay differences. A negative delay in these control words means that the particular data lane requires slightly less delay than the previously established MDQS

See JEDEC Standard No. 82-32A (August 2019), Page 32.

delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble. A positive delay in these control words means that the particular data lane requires slightly more delay than the previously established MDQS delay in F[3:0]BC4x or F[3:0]BC5x for the entire nibble.

To exit this training mode, the host controller can go back to resume normal operation or enable other training modes with a BCW to BC0C.

See JEDEC Standard No. 82-32A (August 2019), Page 33.

92. By infringing claim 1 and other claims of the '035 Patent, Defendants' infringing Products allow for systems configured with greater memory capacity than other types of memory modules.

93. Defendants have also infringed indirectly and continue to infringe indirectly the ’035 Patent by active inducement under 35 U.S.C. § 271(b).

94. Defendants have been aware of the ’035 Patent and their infringement since no later than April 28, 2021, when Netlist informed Defendants of their infringement and offered to license the Infringing Products. By service of this Complaint, Defendants have either refused to negotiate in good faith in response to Netlist’s RAND offer, and/or have refused to pay for a license to the ’035 Patent.

95. On information and belief, Defendants have intended, and continue to intend, to induce patent infringement by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties, incorporating their DDR4 LRDIMM memory modules and have had knowledge that the inducing acts would cause infringement or have been willfully blind to the possibility that the inducing acts would cause infringement.

96. For example, Defendants advertise and market their Load Reduced DDR4 SDRAM DIMMS by telling customers that:

> Implementing load-reduced DIMMs (LRDIMMs) enables you to add more DIMMs per channel and increase the memory capacity and speed of your systems. Our LRDIMMs use a specially designed buffer to reduce the data load to a single load (up to an 8-rank DIMM), whereas standard RDIMMs present multiple loads for dual-rank and quad-rank versions and limit the amount of data you can load to the data bus.

See Micron, Solutions, Server, LRDIMM (https://www.micron.com/solutions/server).

97. Defendants have also infringed indirectly and continue to infringe indirectly the ’035 Patent by contributory infringement under 35 U.S.C. § 271(c).

98. Defendants have and continue to intentionally commit contributory infringement by selling, offering to sell, or importing the infringing products, which include configurations that

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have no substantial non-infringing use, including but not limited to their DDR4 LRDIMM memory modules, with the knowledge that they will be used by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties to directly infringe claims of the ’035 Patent.

99. Defendants have had actual knowledge of the ’035 Patent since at least April 28, 2021, when Netlist informed Defendants of their infringement of the ’035 Patent. By service of this Complaint, despite having actual knowledge of their infringement of the ’035 Patent, Defendants have continued to willfully, wantonly, and deliberately infringe the ’035 Patent. Defendants have either failed to negotiate in good faith, and/or refused to pay for a license to the ’035 Patent under reasonable terms. Accordingly, Plaintiff seeks enhanced damages pursuant to 35 U.S.C. § 284 and a finding that this is an exceptional case within the meaning of 35 U.S.C. § 285, entitling Plaintiff to its attorneys’ fees and expenses.

100. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’035 Patent.

101. As a result of Defendants’ infringement of the ’035 Patent and refusal to take a license to it, Plaintiff has been injured by Defendants’ unauthorized use of Plaintiff’s intellectual property.

102. Plaintiff seeks monetary damages in an amount adequate to compensate for Defendants’ infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

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COUNT 3

(Willful Infringement of U.S. Patent No. 10,268,608)

103. Plaintiff re-alleges and incorporates by reference the allegations in the foregoing paragraphs as if fully set forth herein.

104. Plaintiff is informed and believes, and on that basis alleges, that Defendants have infringed and are currently infringing one or more claims (e.g., claim 1) of the ’608 Patent, in violation of 35 U.S.C. § 271.

105. Defendants have infringed and are currently infringing literally and/or under the doctrine of equivalents, by, among other things, making, using, offering for sale, selling, and/or importing within this judicial district and elsewhere in the United States, without license or authority, Infringing products, including but not limited to their 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module and related products and/or processes falling within the scope of one or more claims of the ’608 Patent, including claim 1:

> A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
>
> > a module board having edge connections for coupling to respective signal lines in the memory bus;
> >
> > a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
> >
> > memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

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> a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

106. Defendants' acts of making, using, offering for sale, selling, and/or importing infringing products, including but not limited to their 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module and related products and/or processes satisfy, literally or under the doctrine of equivalents, each and every claim limitation, including but not limited to limitations of claim 1.[5]

107. For example, on information and belief, the Defendants' 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 memory module meets each and every limitation of claim 1.

108. Defendants' 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 is a memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines.

[5] Plaintiff expressly reserves the right to identify additional asserted claims in its infringement contentions in accordance with this Court's Order Governing Procedures ("OGP") and other Standing Orders. Claim 1 is provided for notice pleading only and is not presented as an "exemplary" claim of all other claims in the '608 patent.

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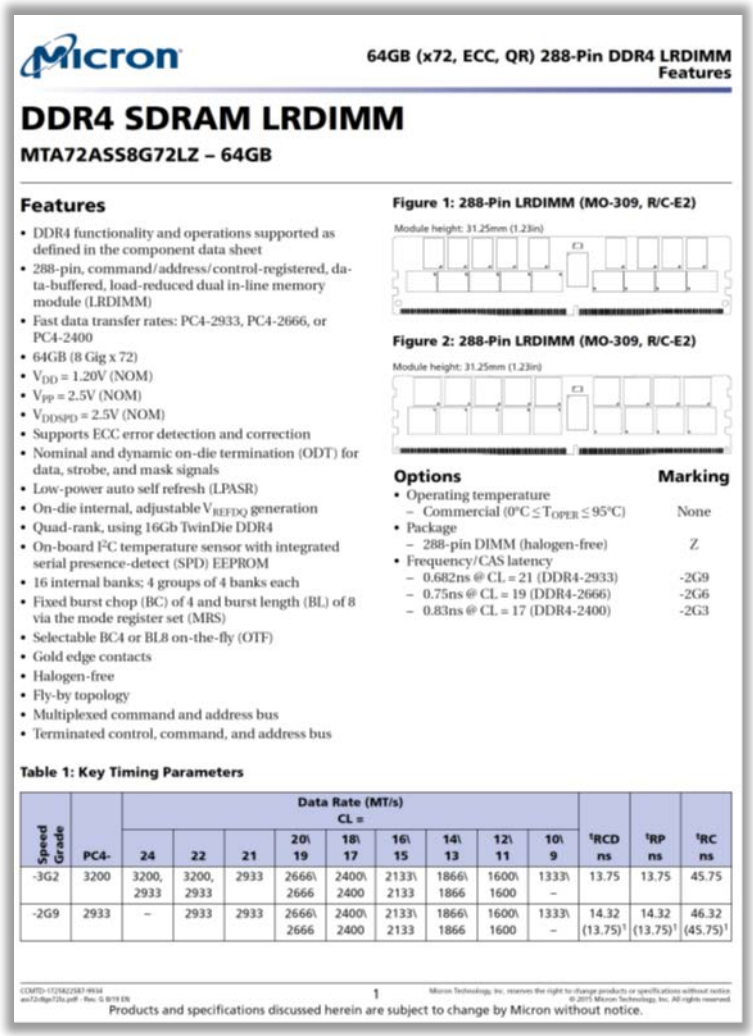

Micron

64GB (x72, ECC, QR) 288-Pin DDR4 LRDIMM
Features

DDR4 SDRAM LRDIMM

MTA72ASS8G72LZ – 64GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, command/address/control-registered, data-buffered, load-reduced dual in-line memory module (LRDIMM)
- Fast data transfer rates: PC4-2933, PC4-2666, or PC4-2400
- 64GB (8 Gig x 72)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.5V (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die internal, adjustable V_{REFDQ} generation
- Quad-rank, using 16Gb TwinDie DDR4
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Multiplexed command and address bus
- Terminated control, command, and address bus

Figure 1: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Figure 2: 288-Pin LRDIMM (MO-309, R/C-E2)

Module height: 31.25mm (1.23in)

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	None
• Package	
– 288-pin DIMM (halogen-free)	Z
• Frequency/CAS latency	
– 0.682ns @ CL = 21 (DDR4-2933)	-2G9
– 0.75ns @ CL = 19 (DDR4-2666)	-2G6
– 0.83ns @ CL = 17 (DDR4-2400)	-2G3

Table 1: Key Timing Parameters

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22	21	20\19	18\17	16\15	14\13	12\11	10\9	^tRCD ns	^tRP ns	^tRC ns
-3G2	3200	3200, 2933	3200, 2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	13.75	13.75	45.75
-2G9	2933	–	2933	2933	2666\2666	2400\2400	2133\2133	1866\1866	1600\1600	1333\–	14.32 (13.75)[1]	14.32 (13.75)[1]	46.32 (45.75)[1]

1

Products and specifications discussed herein are subject to change by Micron without notice.

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 1.

109. As an LRDIMM, the 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 complies with the DDR4 SDRAM Load Reduced DIMM Design Specification promulgated by the JEDEC:

1 Product Description

This specification defines the electrical and mechanical requirements for 288-pin, 1.2 Volt (VDD), Load Reduced, Double Data Rate, Synchronous DRAM Dual In-Line Memory Modules (DDR4 SDRAM LRDIMMs). These DDR4 Load Reduced DIMMs (LRDIMMs) are intended for use as main memory when installed in PCs.

Reference design examples are included that provide an initial basis for DDR4 LRDIMM designs. Modifications to these reference designs may be required to meet all system timing, signal integrity, and thermal requirements for PC4-1600, PC4-1866, PC4-2133, PC4-2400, PC4-2666, and PC4-3200 support. All DDR4 LRDIMM implementations must use simulations and lab verification to ensure proper timing requirements and signal integrity in the design.

An additional lower voltage of TBD is defined. PC4L is used to reference DIMMs capable of operation at this voltage level. The annex for each raw card will have specific entries to indicate DIMM operation at PC4 and PC4L voltage levels.

This specification follows the JEDEC standard DDR4 component specification (refer to JEDEC standard JESD79-4, at www.jedec.org).

See JEDEC Standard No. 21C (Aug. 2015), Page 4.20.27-5.

110. The JEDEC standard specifies a memory module operable to communicate with a memory controller via a memory bus.

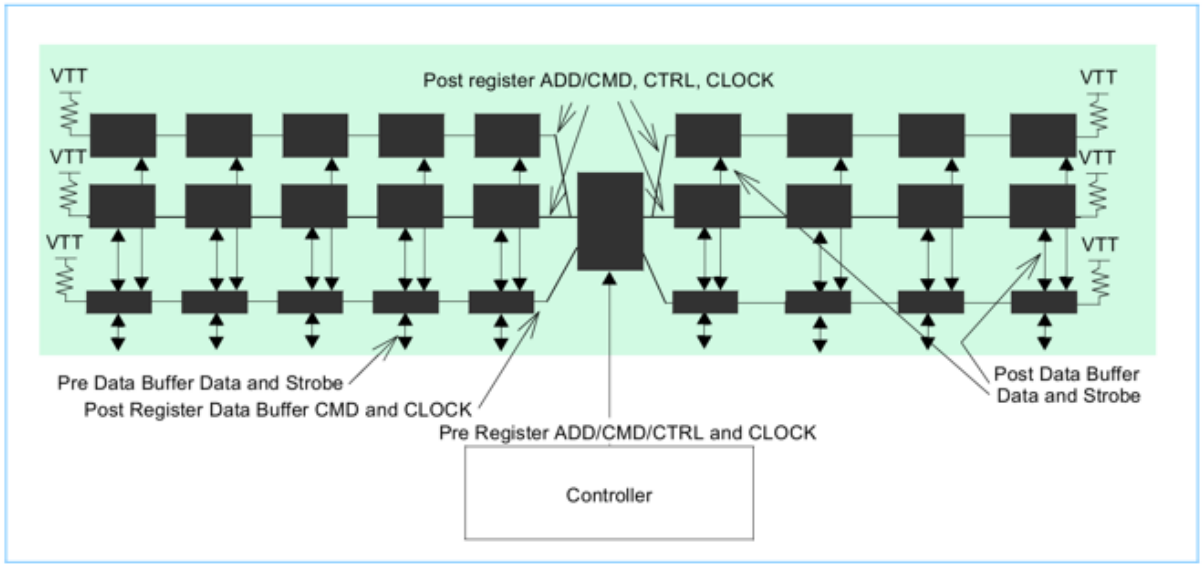

Figure 3 — LRDIMM Topologies

See JEDEC Standard No. 21C (Aug. 2015), Page 4.20.27-17.

111. The memory bus incorporated in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 includes signal lines, which include a set of control/address signal lines and a plurality of sets of data/strobe signal lines.

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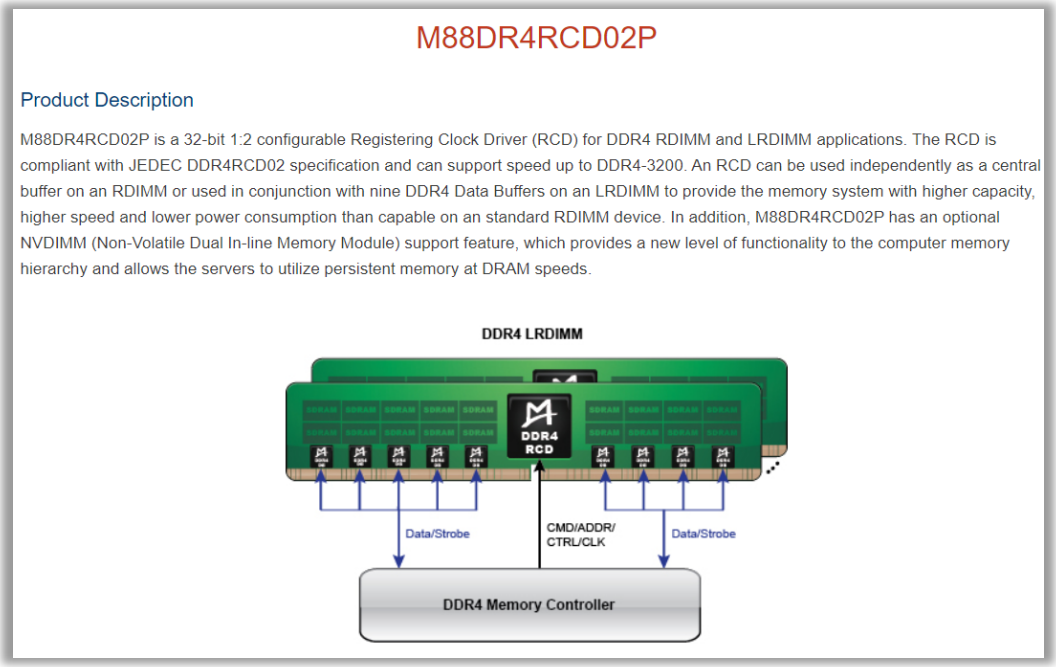
Table 4: Pin Assignments

288-Pin DDR4 LRDIMM Front								288-Pin DDR4 LRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V_{SS}	73	V_{DD}	109	V_{ss}	145	NC	181	DQ29	217	V_{DD}	253	DQ41
2	V_{SS}	38	DQ24	74	CK0_t	110	DQS14_t	146	V_{REFCA}	182	V_{SS}	218	CK1_t	254	V_{SS}
3	DQ4	39	V_{SS}	75	CK0_c	111	DQS14_c	147	V_{SS}	183	DQ25	219	CK1_c	255	DQS5_c
4	V_{SS}	40	DQS12_t	76	V_{DD}	112	V_{SS}	148	DQ5	184	V_{SS}	220	V_{DD}	256	DQS5_t
5	DQ0	41	DQS12-c	77	V_{TT}	113	DQ46	149	V_{SS}	185	DQS3_c	221	V_{TT}	257	V_{SS}
6	V_{SS}	42	V_{SS}	78	EVENT_n	114	V_{SS}	150	DQ1	186	DQS3_t	222	PARITY	258	DQ47
7	DQS9_t	43	DQ30	79	A0	115	DQ42	151	V_{SS}	187	V_{SS}	223	V_{DD}	259	V_{SS}
8	DQS09_c	44	V_{SS}	80	V_{DD}	116	V_{SS}	152	DQS0_c	188	DQ31	224	BA1	260	DQ43
9	V_{SS}	45	DQ26	81	BA0	117	DQ52	153	DQS0_t	189	V_{SS}	225	A10_AP	261	V_{SS}
10	DQ6	46	V_{SS}	82	RAS_n/ A16	118	V_{SS}	154	V_{SS}	190	DQ27	226	V_{DD}	262	DQ53
11	V_{SS}	47	CB4	83	V_{DD}	119	DQ48	155	DQ7	191	V_{SS}	227	NC	263	V_{SS}
12	DQ2	48	V_{SS}	84	S0_n	120	V_{SS}	156	V_{SS}	192	CB5	228	WE_n/ A14	264	DQ49
13	V_{SS}	49	CB0	85	V_{DD}	121	DQS15_t	157	DQ3	193	V_{SS}	229	V_{DD}	265	V_{SS}
14	DQ12	50	V_{SS}	86	CAS_n/ A15	122	DQS15_c	158	V_{SS}	194	CB1	230	NC	266	DQS6_c
15	V_{SS}	51	DQS17_t	87	ODT0	123	V_{SS}	159	DQ13	195	V_{SS}	231	V_{DD}	267	DQS6_t
16	DQ8	52	DQS17_c	88	V_{DD}	124	DQ54	160	V_{SS}	196	DQS8_c	232	A13	268	V_{SS}
17	V_{SS}	53	V_{SS}	89	S1_n	125	V_{SS}	161	DQ9	197	DQS8_t	233	V_{DD}	269	DQ55
18	DQS10_t	54	CB6	90	V_{DD}	126	DQ50	162	V_{SS}	198	V_{SS}	234	A17	270	V_{SS}
19	DQS10_c	55	V_{SS}	91	ODT1	127	V_{SS}	163	DQS1_c	199	CB7	235	NF	271	DQ51
20	V_{SS}	56	CB2	92	V_{DD}	128	DQ60	164	DQS1_t	200	V_{SS}	236	V_{DD}	272	V_{SS}
21	DQ14	57	V_{SS}	93	S2_n	129	V_{SS}	165	V_{SS}	201	CB3	237	S3_n	273	DQ61
22	V_{SS}	58	RESET_n	94	V_{SS}	130	DQ56	166	DQ15	202	V_{SS}	238	SA2	274	V_{SS}
23	DQ10	59	V_{DD}	95	DQ36	131	V_{SS}	167	V_{SS}	203	CKE1	239	V_{SS}	275	DQ57
24	V_{SS}	60	CKE0	96	V_{SS}	132	DQS16_t	168	DQ11	204	V_{DD}	240	DQ37	276	V_{SS}
25	DQ20	61	V_{DD}	97	DQ32	133	DQS16_c	169	V_{SS}	205	NC	241	V_{SS}	277	DQS7_c
26	V_{SS}	62	ACT_n	98	V_{SS}	134	V_{SS}	170	DQ21	206	V_{DD}	242	DQ33	278	DQS7_t
27	DQ16	63	BG0	99	DQS13_t	135	DQ62	171	V_{SS}	207	BG1	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	V_{DD}	100	DQS13_c	136	V_{SS}	172	DQ17	208	ALERT_n	244	DQS4_c	280	DQ63
29	DQS11_t	65	A12	101	V_{SS}	137	DQ58	173	V_{SS}	209	V_{DD}	245	DQS4_t	281	V_{SS}
30	DQS11_c	66	A9	102	DQ38	138	V_{SS}	174	DQS2_c	210	A11	246	V_{SS}	282	DQ59
31	V_{SS}	67	V_{DD}	103	V_{ss}	139	SA0	175	DQS2_t	211	A7	247	DQ39	283	V_{SS}
32	DQ22	68	A8	104	DQ34	140	SA1	176	V_{SS}	212	V_{DD}	248	V_{SS}	284	V_{DDSPD}
33	V_{SS}	69	A6	105	V_{SS}	141	SCL	177	DQ23	213	A5	249	DQ35	285	SDA
34	DQ18	70	V_{DD}	106	DQ44	142	V_{PP}	178	V_{SS}	214	A4	250	V_{SS}	286	V_{PP}
35	V_{SS}	71	A3	107	V_{SS}	143	V_{PP}	179	DQ19	215	V_{DD}	251	DQ45	287	V_{PP}
36	DQ28	72	A1	108	DQ40	144	NC	180	V_{SS}	216	A2	252	V_{SS}	288	V_{PP}

See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 4.

112. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a module board having edge connections for coupling to respective signal lines in the memory bus.

113. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a module control device mounted on the module board and configured to receive system command signals for memory operations.



M88DR4RCD02P

Product Description

M88DR4RCD02P is a 32-bit 1:2 configurable Registering Clock Driver (RCD) for DDR4 RDIMM and LRDIMM applications. The RCD is compliant with JEDEC DDR4RCD02 specification and can support speed up to DDR4-3200. An RCD can be used independently as a central buffer on an RDIMM or used in conjunction with nine DDR4 Data Buffers on an LRDIMM to provide the memory system with higher capacity, higher speed and lower power consumption than capable on an standard RDIMM device. In addition, M88DR4RCD02P has an optional NVDIMM (Non-Volatile Dual In-line Memory Module) support feature, which provides a new level of functionality to the computer memory hierarchy and allows the servers to utilize persistent memory at DRAM speeds.

See https://www.montage-tech.com/Memory_Interface/DDR4/M88DR4RCD02P.

Table 3 — DDR4 Data Buffer Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101

See JEDEC Standard No. 82-32A (August 2019), Page 4.

Table 6 — Data Buffer Control Bus Command Table

Command	Description	BCOM[3:0] Encoding
WR	Write BC4 or BC8 (fixed or on the fly) or BC10 (with CRC enabled) and send accessed rank ID and BL information in the next command time slot, followed by parity in the last command time slot.	1000
RD	Read BC4 or BC8 (fixed or on the fly) and send accessed rank ID and BL information for regular reads or MPR number for MPR override reads in the next command time slot, followed by parity in the last command time slot.	1001
MRS Write	Send MRS Write bits snooped by DDR4 Register and the MRS ID in the following six command time slots, followed by parity in the last command time slot.	1011
BCW Write	Write buffer control word data in the next five command slots, followed by parity in the last command time slot.	1100
BCW Read	Read buffer control word address in the four command slots, followed by parity in the last command time slot.	1101
RFU[1]	Reserved for future use	1110
RFU[1]	Reserved for future use	1111
NOP	Idle, do nothing	1010

1. RFU commands are treated as NOP commands for command sequence error detection

See JEDEC Standard No. 82-31A (August 2019), Page 14.

Figure 3 shows the timing sequence for a Read command.

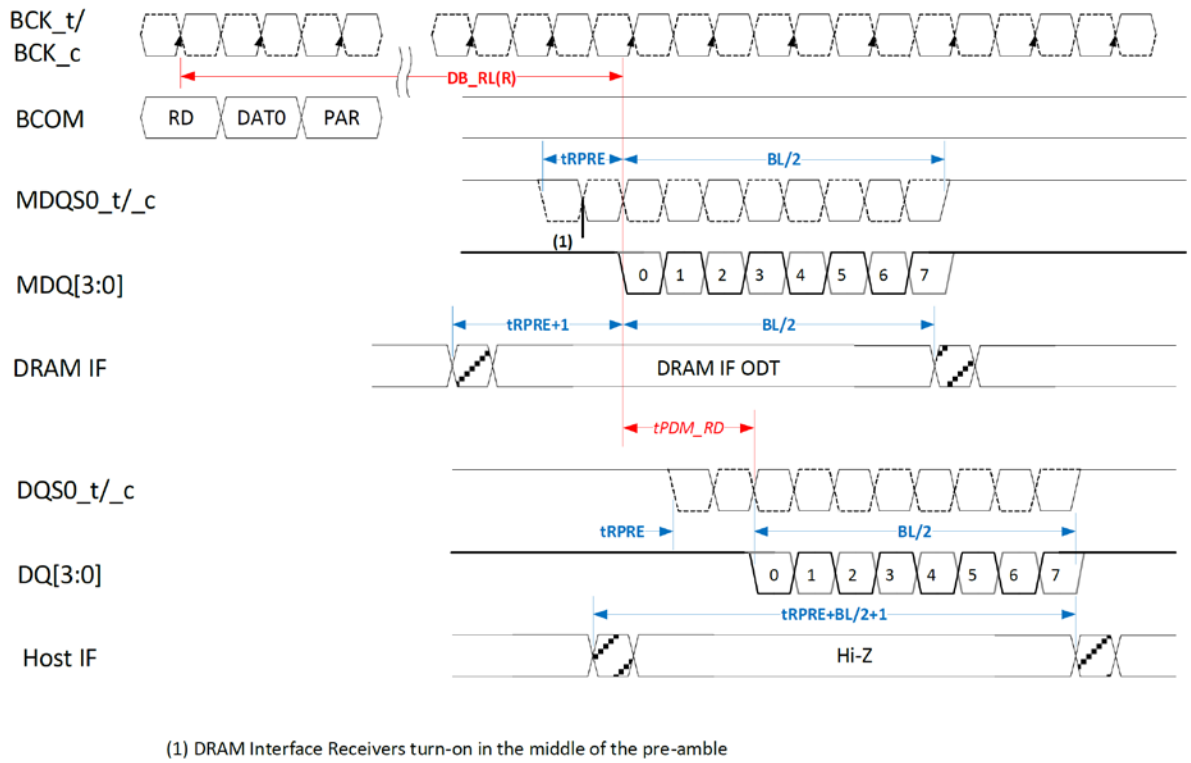
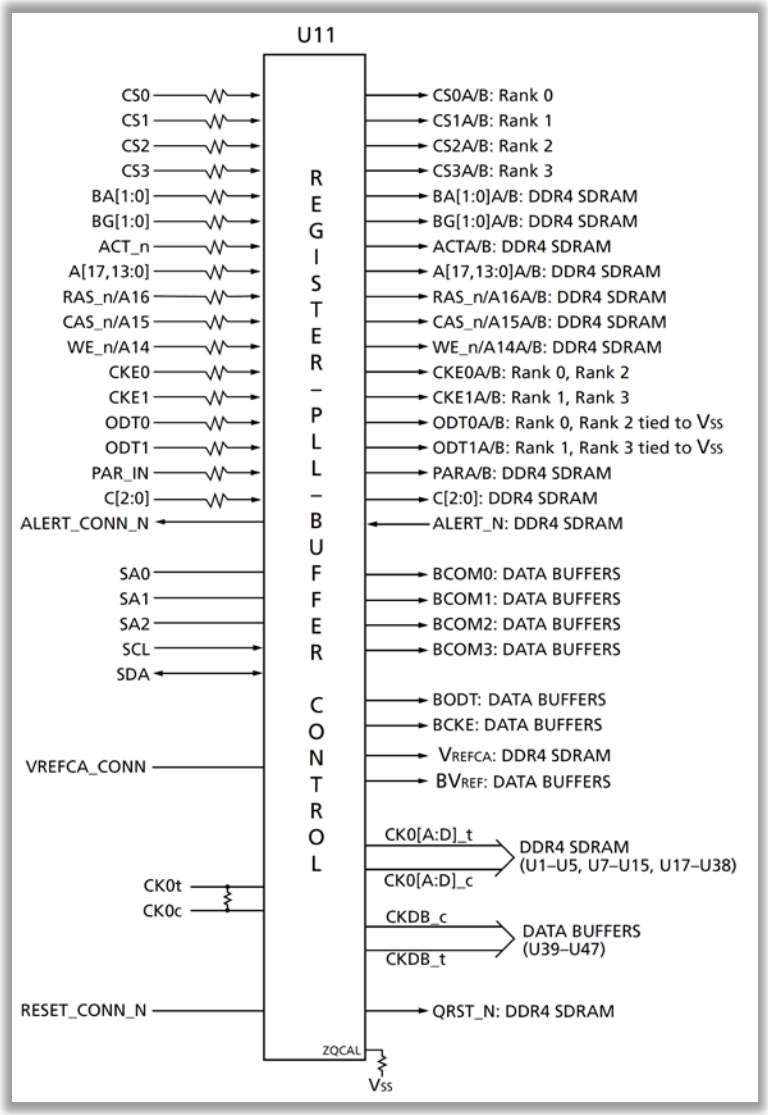


Figure 3 — READ Timing

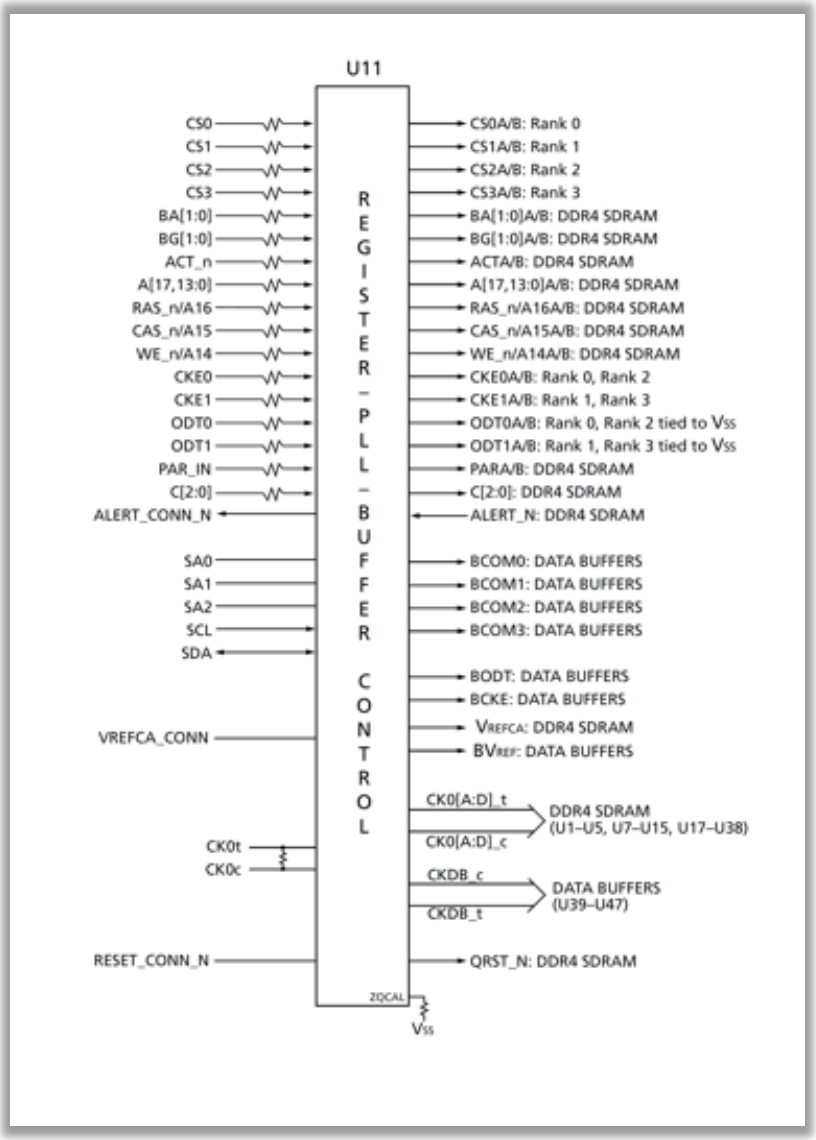
See JEDEC Standard No. 82-32A (August 2019), Page 14.

114. The module control device in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 is configured to receive system command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal.

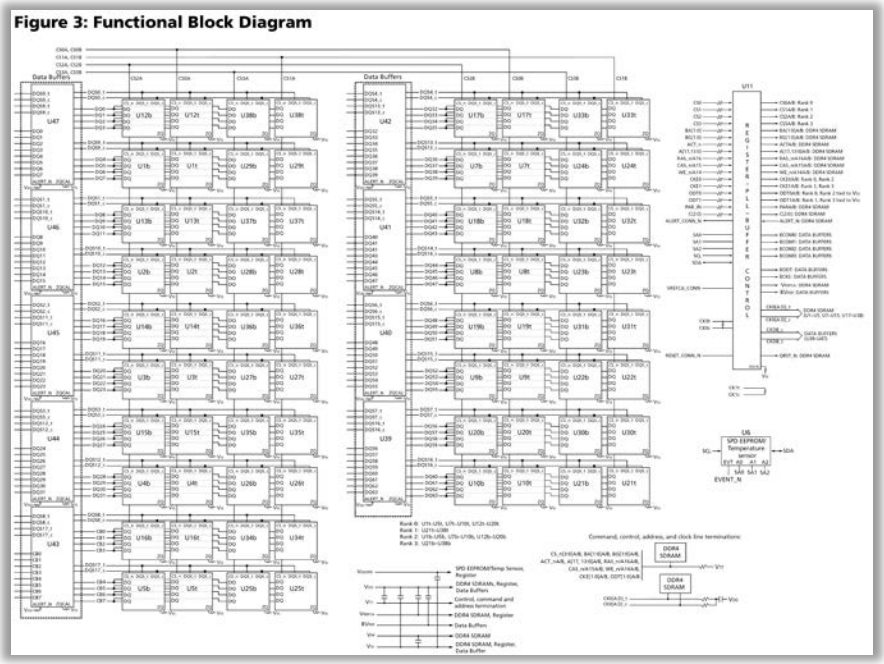


See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

115. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals.

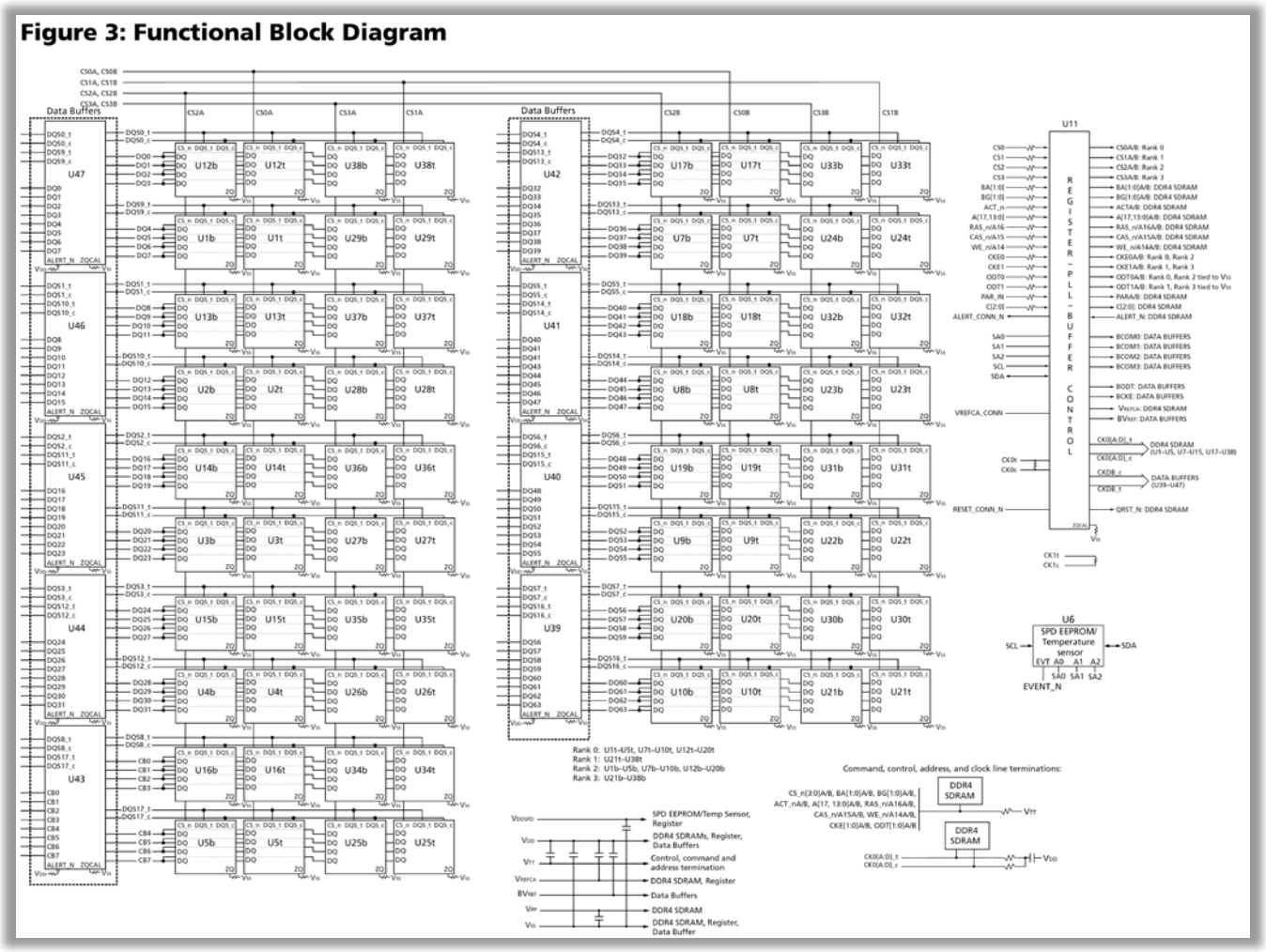


See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

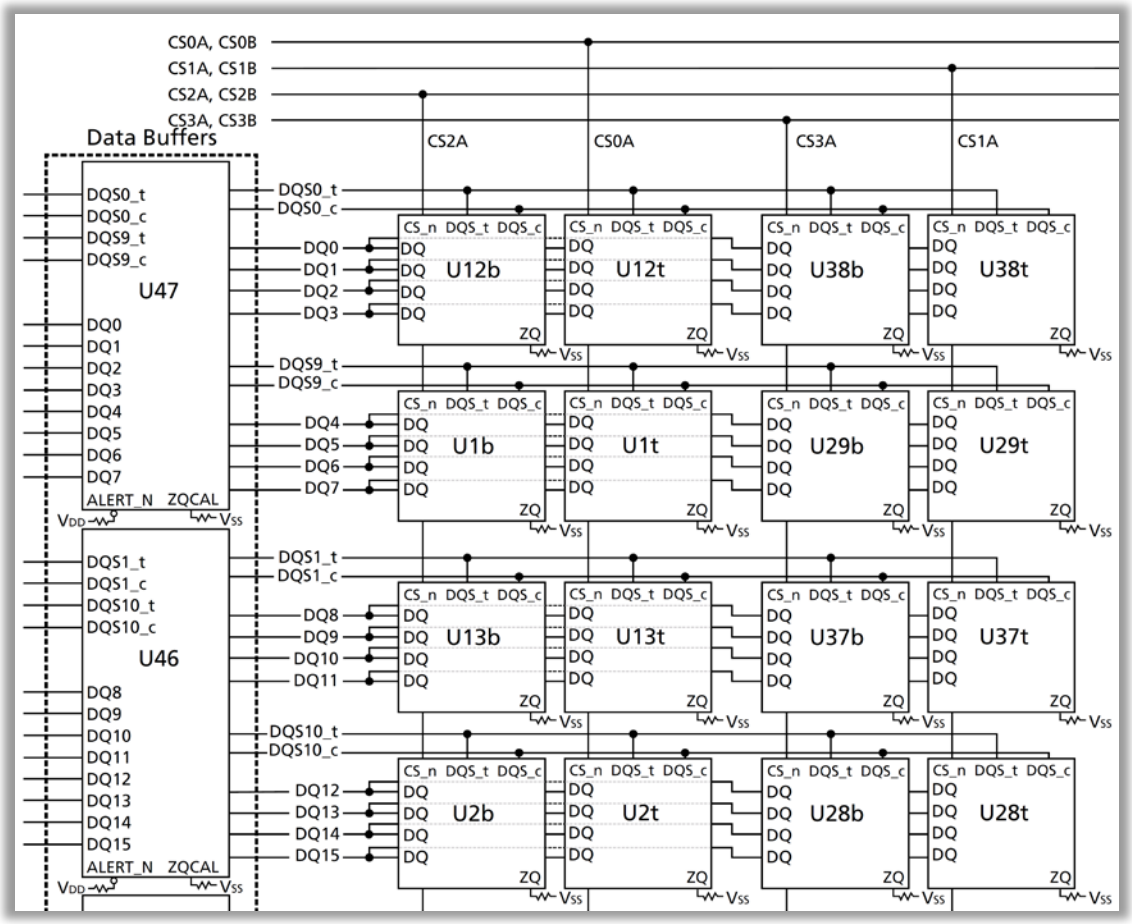
116. The memory devices in the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 include a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines.



See Micron 64GB DDR4 LRDIMM MTA72ASS8G72LZ Data Sheet, Page 10.

117. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 comprises a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines. *See id.*

118. In the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9, each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal.



See Micron 64GB DDR4 LRDIMM Data Sheet (August 2019), Page 10.

119. In the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9, each buffer circuit includes a data path corresponding to each data signal line in the respective set of data/strobe signal lines.

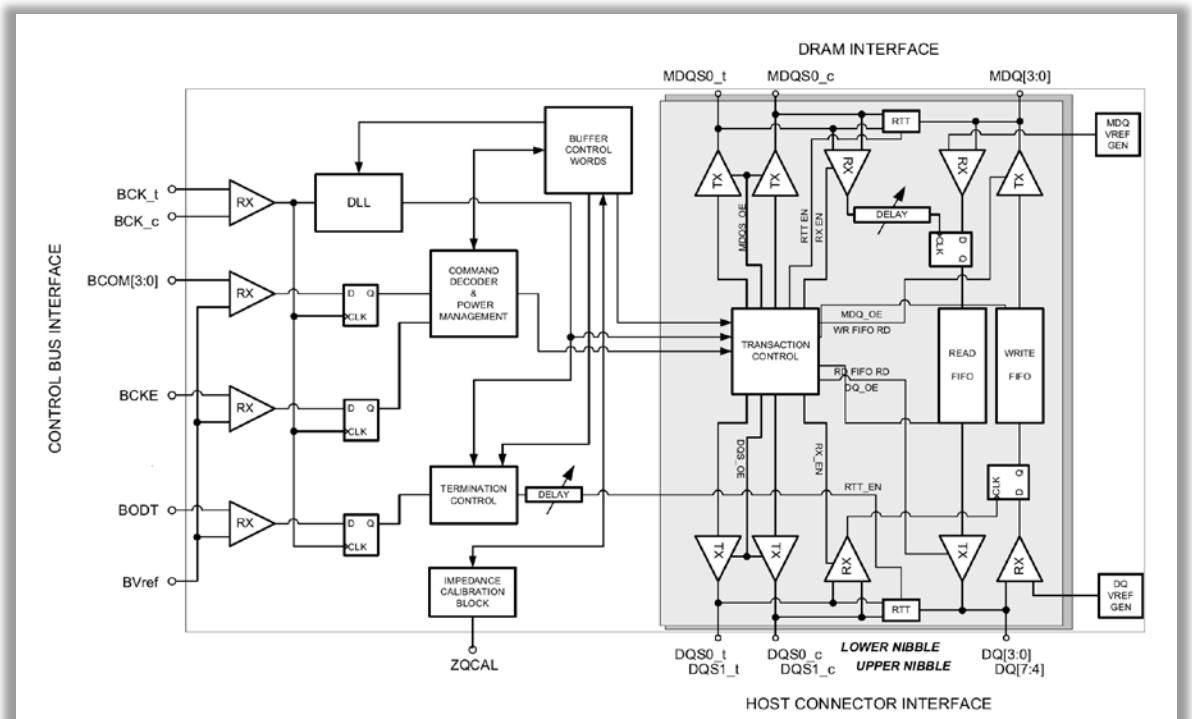


Figure 15 — Logic Diagram

See JEDEC Standard No. 82-32A (August 2019), Page 95.

120. The infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9 incorporates a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal. *See id.*

121. In the infringing 64 GB DDR4 LRDIMM MTA72ASS8G72LZ-2G9, the data path corresponding to each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. *See id.*

122. By infringing claim 1 and other claims of the ’608 Patent, Defendants’ infringing Products allow for systems configured with greater memory capacity than other types of memory modules.

123. Defendants have also infringed indirectly and continue to infringe indirectly the ’608 Patent by active inducement under 35 U.S.C. § 271(b).

124. Defendants have been aware of the ’608 Patent and their infringement since no later than April 28, 2021, when Netlist informed Defendants of their infringement and offered to license the Infringing Products. By service of this Complaint, Defendants have either refused to negotiate in good faith in response to Netlist’s RAND offer, and/or have refused to pay for a license to the ’608 Patent.

125. On information and belief, Defendants have intended, and continue to intend, to induce patent infringement by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties, incorporating their DDR4 LRDIMM memory modules and have had knowledge that the inducing acts would cause infringement or have been willfully blind to the possibility that the inducing acts would cause infringement.

126. For example, Defendants advertise and market their Load Reduced DDR4 SDRAM DIMMS by telling customers that:

> Implementing load-reduced DIMMs (LRDIMMs) enables you to add more DIMMs per channel and increase the memory capacity and speed of your systems. Our LRDIMMs use a specially designed buffer to reduce the data load to a single load (up to an 8-rank DIMM), whereas standard RDIMMs present multiple loads for dual-rank and quad-rank versions and limit the amount of data you can load to the data bus.

See Micron, Solutions, Server, LRDIMM (https://www.micron.com/solutions/server).

127. Defendants have also infringed indirectly and continue to infringe indirectly the ’608 Patent by contributory infringement under 35 U.S.C. § 271(c).

128. Defendants have and continue to intentionally commit contributory infringement by selling, offering to sell, or importing the infringing products, which include configurations that

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have no substantial non-infringing use, including but not limited to their DDR4 LRDIMM memory modules, with the knowledge that they will be used by others, including system designers, software providers, distributors, customers, end-users, and/or other third parties, to directly infringe claims of the ’608 Patent.

129. Defendants have had actual knowledge of the ’608 Patent since at least April 28, 2021, when Netlist informed Defendants of their infringement of the ’608 Patent. By service of this Complaint, despite having actual knowledge of their infringement of the ’608 Patent, Defendants have continued to willfully, wantonly, and deliberately infringe the ’608 Patent. Defendants have either failed to negotiate in good faith, and/or refused to pay for a license to the ’608 Patent under reasonable terms. Accordingly, Plaintiff seeks enhanced damages pursuant to 35 U.S.C. § 284 and a finding that this is an exceptional case within the meaning of 35 U.S.C. § 285, entitling Plaintiff to its attorneys’ fees and expenses.

130. To the extent applicable, the requirements of 35 U.S.C. § 287(a) have been met with respect to the ’608 Patent.

131. As a result of Defendants’ infringement of the ’608 Patent and refusal to take a license to it, Plaintiff has been injured by Defendants’ unauthorized use of Plaintiff’s intellectual property.

132. Plaintiff seeks monetary damages in an amount adequate to compensate for Defendants’ infringement, but in no event less than a reasonable royalty for the use made of the invention by Defendants, together with interest and costs as fixed by the Court.

PRAYER FOR RELIEF

Plaintiff prays for the following relief:

A. A judgment that Defendants have infringed one or more claims of the Asserted

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Patents;

B. An award of damages resulting from Defendants' acts of infringement in accordance with 35 U.S.C. § 284;

C. A judgment and order finding that Defendants' acts of infringement were egregious and willful and trebling damages under 35 U.S.C. § 284;

D. A judgment and order finding that this is an exceptional case within the meaning of 35 U.S.C. § 285 and awarding to Plaintiff its reasonable attorneys' fees against Defendants.

E. A judgment and order requiring Defendants to provide accountings and to pay supplemental damages to Plaintiff, including, without limitation, prejudgment and post-judgment interest; and

F. Any and all other relief to which Plaintiff may show itself to be entitled.

JURY TRIAL DEMANDED

Plaintiff hereby demands a jury trial for all issues so triable.

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Dated: April 28, 2021

/s/ *Paul J. Skiermont*

Paul J. Skiermont (TX Bar No. 24033073)
Steven Hartsell (TX Bar No. 24040199)
Jaime Olin (TX Bar No. 24070363)
Ryan A. Hargrave (TX Bar No. 24071516)
Sheetal S. Patel (TX Bar No. 24070390)
SKIERMONT DERBY LLP
1601 Elm St., Ste. 4400
Dallas, TX 75201
Phone: (214) 978-6600
Fax: (214) 978-6601
pskiermont@skiermontderby.com
shartsell@skiermontderby.com
jolin@skiermontderby.com
rhargrave@skiermontderby.com
spatel@skiermontderby.com

Rex Hwang (CA Bar No. 221079)
SKIERMONT DERBY LLP
800 Wilshire Blvd., Ste. 1450
Los Angeles, CA 90017
Phone: (213) 788-4500
Fax: (213) 788-4545
rhwang@skiermontderby.com

J. Stephen Ravel (TX Bar No. 16584975)
KELLY HART & HALLMAN LLP
303 Colorado, Suite 2000
Austin, Texas 78701
Tel: (512) 495-6429
steve.ravel@kellyhart.com

Attorneys for Plaintiff
Netlist, Inc.

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