

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 10,860,506

Issued: December 8, 2020

Filed: April 22, 2019

Inventors: Hyun Lee and Jayesh R. Bhakta

Title: MEMORY MODULE WITH TIMING-CONTROLLED DATA
BUFFERING

Inter Partes Review No. IPR2022-00711

**DECLARATION OF DR. ROBERT WEDIG
REGARDING U.S. PATENT NO. 10,860,506**

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for Samsung Electronics Co., Ltd. as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 10,860,506 (“the ’506 Patent”) (EX1001) and on the patentability of claims 1-20 of this patent.

B. Background and Qualifications

2. I received a Bachelor of Electrical Engineering degree from the University of Dayton in 1977. I received a Master of Science degree in Electrical Engineering from the University of Southern California in 1979, and received a Ph.D. in Electrical Engineering from Stanford University in 1982.

3. From 1977 through 1979, I worked as a processor design engineer at Hughes Aircraft Company in Fullerton, California. In this capacity, I designed computer systems which interface with memory integrated circuits. As one example, I was responsible for the design of an Input/Output processor which directly interfaced to a memory controller for a military mainframe computer system. From 1979 through June 1982, I was a Research Assistant, Instructor, and Teaching Assistant in the Computer Systems Laboratory at Stanford University. From 1982 through December 1985, I was an Assistant Professor of Electrical and Computer Engineering at Carnegie-Mellon University. My research, both as a PhD

student and as an assistant professor, involved the research and design of concurrent computer systems which interface with memory integrated circuits. As a professor, I taught courses in computer design which included memory design issues involving DRAM and SDRAM. Since January 1986, I have worked as an independent consultant, doing business as Wedig Consulting, Inc. As a consultant, I have designed digital circuits, analyzed computer systems and designed software for computer based electronic systems. I have also analyzed high-speed backplane design issues including crosstalk, signal reflection and signal trace timing and impedance.

C. Compensation and Prior Testimony

4. I am being compensated at a rate of \$700.00 per hour for work on this matter. I am also being reimbursed for reasonable and customary expenses associated with my work on this matter. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

5. Previously, I have testified either by deposition or at trial in a number of litigation matters. My curriculum vitae, including a list of all of my publications, and cases in which I have previously testified as an expert is attached as Exhibit 1004.

D. Information Considered

6. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in Attachment B.

7. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

8. My analysis of the materials produced in this matter is ongoing and I will continue to review any new material as it is provided.

II. LEGAL STANDARDS FOR PATENTABILITY

9. In expressing my opinions and considering the subject matter of the claims of the '506 Patent, I am relying upon certain basic legal principles that have been explained to me.

10. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

11. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and

generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, etc.).

12. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the '506 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

13. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims, after being construed in this manner, are then to be compared to the information in the prior art.

14. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

15. I understand that there are two ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. My understanding of the two legal standards is set forth below.

A. Anticipation

16. I understand that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art.

17. I understand that the “prior art” includes patents and printed publications that existed before the earliest filing date (the “effective filing date”) of the claim in the patent. I also understand that a patent will be considered prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be considered prior art if it was publicly available before that date.

18. I understand that, for a patent claim to be “anticipated” by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are “inherent” to the thing or process being described in the prior art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

19. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

20. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

21. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

22. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

23. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the '506 Patent would have been considered obvious as of the priority date of the patent.

24. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

25. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

26. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; satisfying a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected

results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors” suggesting the claimed inventions are not obvious, and reserve my right to address any such evidence if it is identified in the future.

27. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

28. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one

device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

29. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

30. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

31. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements

of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

32. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor as of the priority date of the patent and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

33. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or

more prior art references discourage or lead away from the line of inquiry disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

34. I understand that a person of ordinary skill is also a person of ordinary creativity.

35. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance, the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE '506 PATENT

A. Effective Filing Date

36. The application that resulted in the '506 Patent (EX1001) is U.S. Patent Application Serial No. 16/391,151 (EX1002), filed April 22, 2019. The '506 Patent claims priority to U.S. Provisional Application No. 61/676,883 (EX1025), filed July 27, 2012. All of the prior art that I rely upon below predates July 27, 2012, and thus, for now, I assume that the claims of the '506 Patent have an effective filing date of **July 27, 2012**, regardless of whether there is actually support in the provisional application for all of the claim limitations.

B. Person of Ordinary Skill in the Art

37. Based upon my experience in the field and the information discussed below, I believe a person of ordinary skill in the art ("Skilled Artisan" or "POSITA") in the field of the '506 Patent in July 2012 would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field. Such a person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with

various standards, and how they interact with other components of a computer system, such as memory controllers. He or she would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers.

C. Overview of the Patent

38. The '506 Patent discloses a memory module with a module control circuit, memory devices, and data buffers. EX1001 at Abstract. As illustrated in annotated Figure 2C below, the memory module (110) includes memory devices (112, green) organized in groups, each group with an associated data buffer (isolation device 118, blue) and one module control device (116, red) located in the center of the module. *Id.*, 3:25-27, Fig. 2C (reproduced below with annotations). The groups of memory devices (green) and associated data buffers (blue) are distributed length-wise across the memory module. *Id.*, 3:51-54, Fig. 2C (reproduced below with annotations).

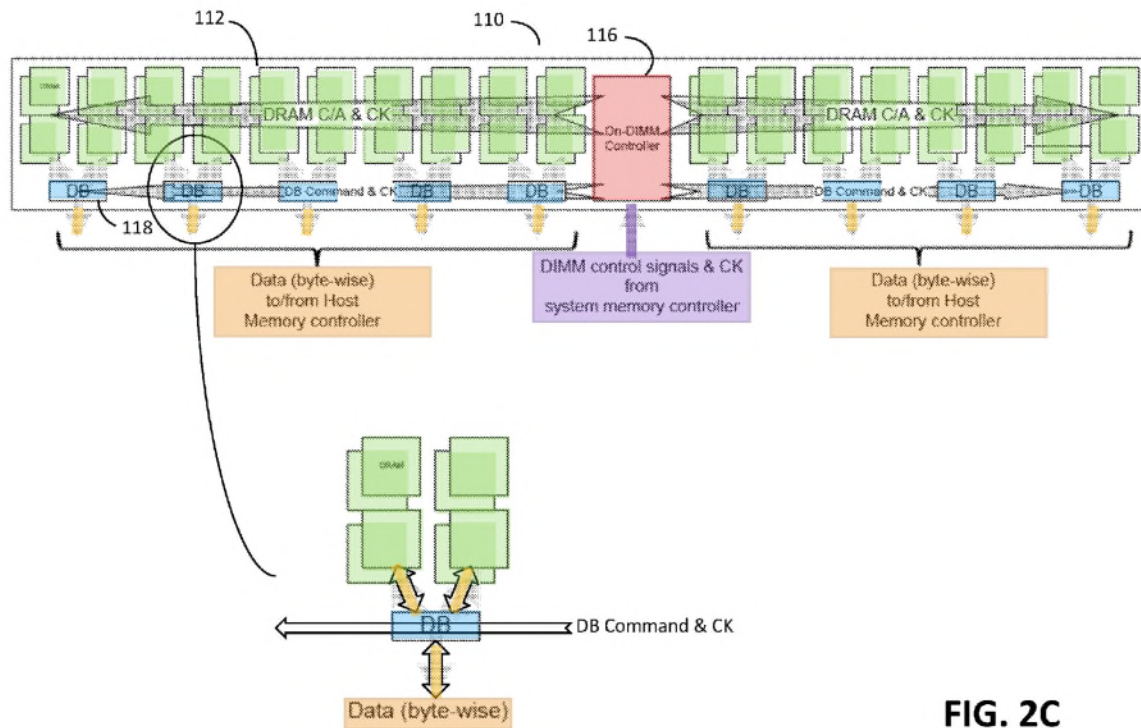


FIG. 2C

39. As shown in annotated Figure 1 below, the memory module (110) is connected to a memory controller (MCH) (101). *Id.*, 3:29-34, 4:20-23, FIG. 1 (reproduced below with annotations).

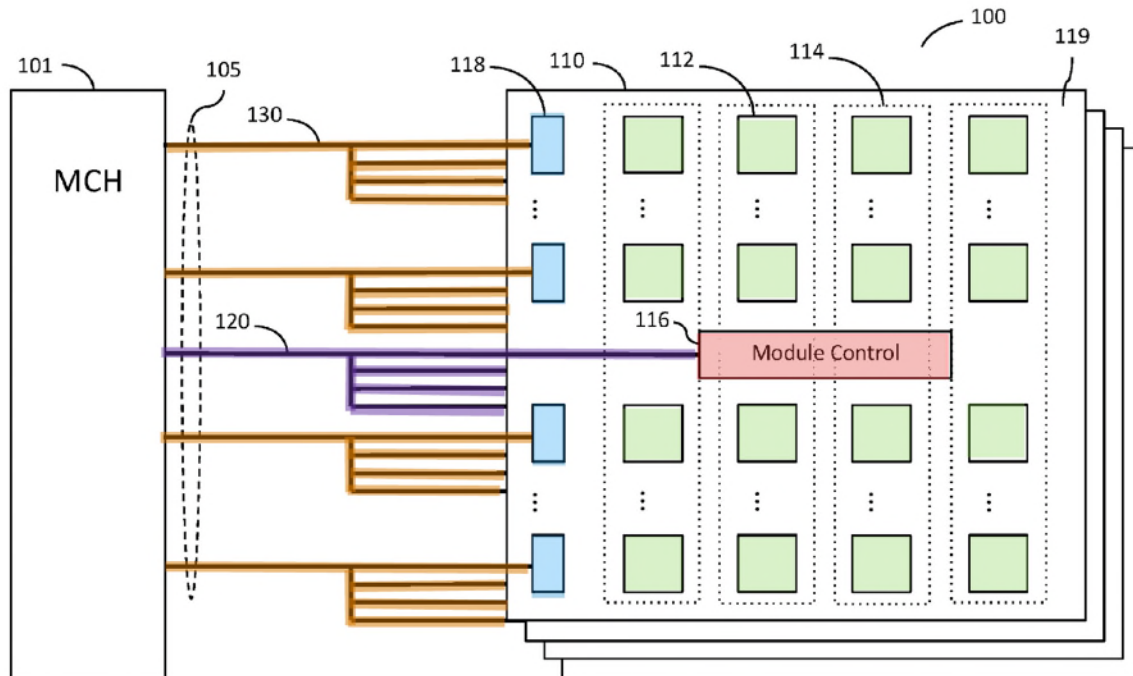


FIG. 1

40. As shown in annotated Figures 1 and 2C above, a memory bus (105) connects the memory controller (MCH) (101) and the memory module (110) with control/address (C/A) signal lines (120, purple) between the memory controller (101) and the module control device (116, red), and data/strobe signal lines (130, orange) between the memory controller and each memory device (112, green) via each data buffer (118, blue). *Id.*, 4:20-32. The memory controller (MCH) (101) issues C/A signals (on lines 120, purple) to the memory module (110) via the module control device (116, red), and sends and receives data/strobe signals (on lines 130, orange) to/from the memory devices (112, green) via the data buffers (118, blue). *Id.*

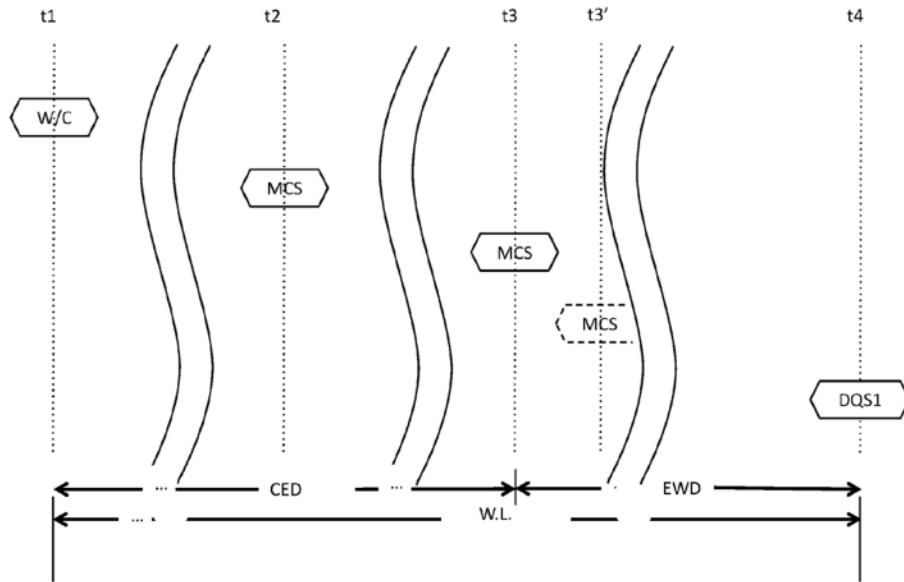
41. In an exemplary embodiment, the module control device (red) receives the system memory commands represented by a set of system C/A signals from the memory controller (MCH) and generates module command signals and module control signals based on memory commands from the system. *Id.*, 4:65-5:7. The module control device (red) transmits the module command signals to the memory devices (green) via signal lines and the module control signals to the data buffers (blue) via other signal lines. *Id.*, 5:57-66; *see also* FIGS. 2A and 2B (showing connections between the module controller 116, the memory devices 112, and data buffers 118).

42. As shown in annotated Figure 1 above, each group of memory devices can include, for example, four memory devices (green), *id.*, 6:12-16, each consisting of a dynamic random access memory (DRAM), *id.*, 4:60-64. All four of the memory devices (green) can connect in parallel to the memory controller data/strobe signal lines (orange) through their associated data buffer (blue), which isolate the memory devices (green) from the memory controller (MCH). *Id.*, 3:27-29, 6:17-29.

43. The '506 Patent notes that because the data buffers (blue) and their associated memory devices (green) are distributed across the memory module in various positions, "a same set of module control signals may reach different [data buffers (blue)] at different times across more than one clock cycle of the system

clock.” *Id.*, 9:52-10:6. Each data buffer (blue) thus may include signal alignment circuits that determine time intervals to use to adjust for the signals received at different times. *Id.*, 10:7-21.

44. As shown in Figures 12A below, the data buffer determines a time interval based upon the reception of signals to the data buffer during a write operation. *Id.*, 15:27-50. In particular, the module control circuit receives **a write command** (W/C) at time t1, and outputs a corresponding module control signal (MCS) at time t2. *Id.*, 15:27-32. The module control signal (MCS) is received by one data buffer at time t3 and by another data buffer, farther away from the module control circuit, at time t3’ which “can be in a different cycle of the system clock MCK from the cycle which t3 is in.” *Id.*, 15:33-38. Both of those data buffers receive the corresponding data strobe signal (DQS1) of the write data at time t4, in accordance with a known write latency (W.L.) after the write command at t1 (W/C). *Id.*, 15:38-42. Thus, each data buffer can measure the difference (EWD) between time t3, the reception of the module control signal (MCS), and time t4, the reception of the corresponding data strobe (DQS1). *Id.*, 15:42-45. The time interval EWD and the known write latency (W.L.) can then be used to adjust signal timing during memory read operations so that the signals are released or processed at the proper times. *Id.*, 15:45-50.



In particular, “[w]ith knowledge of the time interval between t7 and t5, which should be about the same as the time interval between t3 and t1, i.e., the command-to-enable delay CED, in certain embodiments, the isolation device can ***add a proper amount of delay to the read data*** signals and the one or more DQS signal such that the read data signals and the one or more DQS signal are transmitted at time t9 by the isolation device to the MCH 101” *Id.*, 15:66-16:6, FIG. 12B (red annotations added).

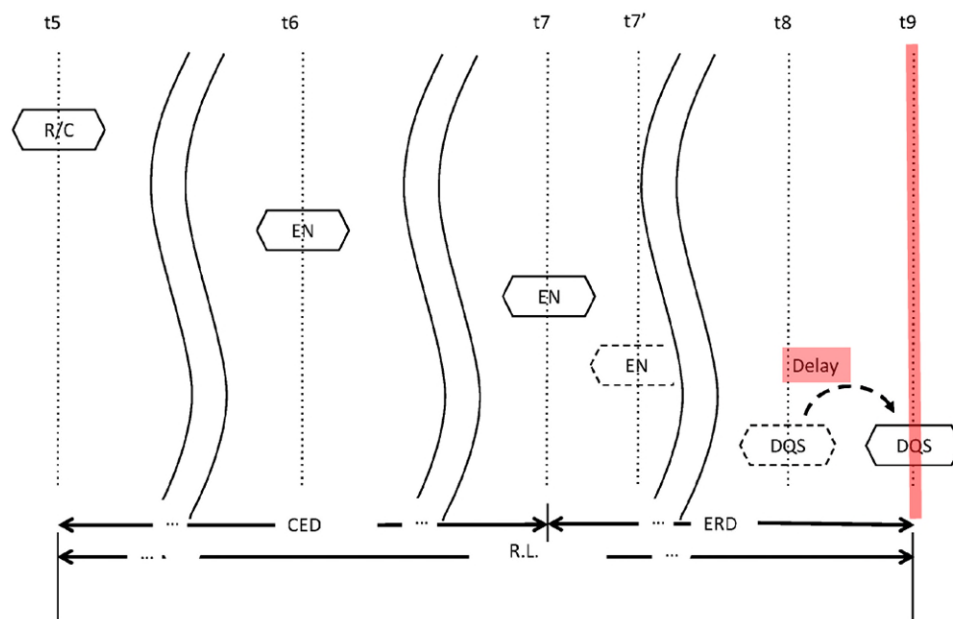


FIG. 12B

D. The Prosecution History

1. The 599 Application (The '632 Patent)

45. U.S. Patent No. 9,128,632 (“the ‘632 Patent”) is related to the ‘506 Patent. Both the ‘632 Patent and the ‘506 Patent claim priority to the filing date of the same provisional application, EX1025, which was filed on July 27, 2012. The ‘632 Patent issued from Application No. 13/952,599 (“the 599 Application”). EX1010 (‘632 File History). The 599 Application presented 20 claims, claims 1-20. *Id.* at 36-39.

46. The Examiner rejected all the claims of the 599 Application as anticipated by the Manohararajah ‘033 patent, EX1026. *Id.* at 99-108. In response,

the applicant substantially amended the claims, including the final clause of claim 1 to read:

wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

EX1010 (632 File History) at 134-135. Among other things, the applicant argued that “[n]owhere in Manohararajah it is described the transmission of read data signal from each respective buffer is timed in accordance with a time interval determined based signals received by the each respective buffer. Thus, Manohararajah does not anticipate claim 1 as amended.” *Id.*, 140-141.

47. In response, the Examiner accepted the applicant’s amendments and arguments and issued a Notice of Allowance, stating:

the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an operation to configure the timing of transmission of signals to the

memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims.

Id., 1078.

2. The 993 Application (The '587 Patent)

48. U.S. Patent No. 9,563,587 (“the '587 Patent”) is related to the '506 Patent. Both the '587 Patent and the '506 Patent claim priority to the filing date of the same provisional application, which was filed on July 27, 2012. The '587 Patent issued from Application No. 14/846,993 (“the '993 Application”). EX1011 ('587 File History). The '993 Application presented 20 claims, claims 1-20. *Id.* at 37-41.

49. The Examiner issued a Notice of Allowance, stating:

the prior art does not fairly teach or suggest, individually or in combination, a memory module system with a buffer for implementing delayed transmission of signals from a memory controller to each group of memory devices of the module, wherein the buffer circuits are used to determine a respective time interval based on signals received by each buffer circuit during an

operation to configure the timing of transmission of signals to the memory devices, wherein the buffers are located in such a way that they receive control signals at differing points in time, hence the determination of the time interval is based on the receiving of a first signal from the controller and receiving a second signal with for each buffer, i.e. each buffer determines its own respective time interval used for transmitting read / write signals to their respective groups of memory devices as claimed in the independent claims.

Id., 113.

3. IPR2017-00730 by SK hynix against the '632 Patent

50. On January 20, 2017, SK hynix filed a petition for *inter partes* review of the '632 Patent. *See generally* EX1012 (IPR2017-00730, i.e., 632 IPR Petition); EX1013 (Netlist's Patent Owner Preliminary Response).

51. Claim 1 of the '632 Patent contains the following limitation, which is not expressly found in the claims of the '506 Patent:

wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation

EX1014 at 10.

52. Based on the claim limitation above, the Board denied institution in IPR2017-00730 on July 21, 2017, stating that “Petitioner argues that [the re-timing in the cited prior art] is related to the time interval determined during the read leveling operation by read leveling circuit 323, but that operation determines a ‘time A’ that is used to adjust timing of ‘the *input buffer circuit INB* and the like.’ [The cited prior art] does not teach time A being used to adjust timing of data *output* by data buffer circuit 300 to the system controller (i.e., to ‘time transmission of a respective set of read data signals,’) as recited in the claim [of the ’632 Patent].” EX1014 (632 Decision) at 12-13 (citation omitted).

53. Neither the Board’s decision in IPR2017-00730, nor the prior art raised in that IPR, was provided to the examiner of the ’506 Patent, despite the fact that IPR2017-00730 concluded in 2017 before the application for the ’506 Patent was filed in 2019. *See generally* EX1002 (’506 prosecution history).

4. The 064 Application (The ’035 Patent)

54. U.S. Patent No. 9,824,035 (“the ’035 Patent”), EX1031, is related to the ’506 Patent. Both the ’035 Patent and the ’506 Patent claim priority to the filing date of the same provisional application, which was filed on July 27, 2012. The ’035 Patent issued from Application No. 15/426,064 (“the 064 Application”). EX1032 (’035 File History). The 064 Application originally presented 20 claims, claims 1-20. *Id.* at 46-49. The Examiner rejected the claims for obvious-type

double patenting over U.S. Patent No. 9,128,632 (“the ’632 Patent”). *Id.* at 89-95.

In response, the applicant submitted a terminal disclaimer and substantially amended the claims:

A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

a module board having edge connections for coupling to respective ~~data/strobe~~ signal lines in the memory bus;

a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to ~~produce~~ output module command signals and module control signals in response to the memory command signals; and

memory devices mounted on the module board and configured to perform thea first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines ~~each respective set of memory devices corresponding to a respective set of the data/strobe signal lines~~; and

a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit ~~providing data paths~~ of the plurality of buffer circuits is coupled between a respective set of ~~the~~ data/strobe signal lines and a respective set ~~of the plurality of sets~~ of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic that responds configured to respond to the module control signals by enabling ~~a subset of the data paths for transmitting data and strobe signals corresponding to the first memory operation between the respective set of the data/strobe signal lines and the corresponding set of the plurality of sets of memory devices~~, wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on ~~the subset of the data paths~~ in accordance with the timing information.

Id. at 105-11. The applicant also presented two new claims, claims 21-22. *Id.*, 110.

55. The Examiner subsequently issued a Notice of Allowance. *Id.*, 123-130. The applicant filed an Amendment after Notice of Allowance to amend (i) dependent claims 6 and 8 to “correct antecedent basis issues and a minor error,” (ii) dependent claims 10 and 12 to change dependency from dependent claim 9 to

independent claim 1, and (iii) dependent claims 13 and 20 to “correct minor errors.” *Id.*, 142-47.

5. The 076 Application (The '608 Patent)

56. U.S. Patent No. 10,268,608 (“the '608 Patent”), EX1033, is related to the '506 Patent. Both the '608 Patent and the '506 Patent claim priority to the filing date of the same provisional application, which was filed on July 27, 2012. The '608 Patent issued from Application No. 15/820,076 (“the 076 Application”). EX1034 (608 File History). The 076 Application originally presented 1 claim. *Id.* at 72. The Examiner rejected the claim for obvious-type double patenting over U.S. Patent No. 9,824,035 and U.S. Patent No. 9,128,632. *Id.*, 83-91. In response, the applicant submitted terminal disclaimers and amended claim 1 to include “memory operations a first operation” and “at least one a tristate buffer.” *Id.* at 102, 116-18. The applicant also presented new dependent claims 2-12. *Id.*, 119-20.

57. The Examiner subsequently issued a Notice of Allowance. *Id.*, 122-29; *see also id.*, 92, 204-06. The Examiner provided the following reasons for allowance:

The following is an examiner’s statement of reasons for allowance:

Prior art teaches memory module systems arranged into respective groups of memory devices, memory module systems with buffered memory modules, and memory module systems that implement delays for transmitting signals to the memory devices of each module, however, the prior art does not fairly teach or suggest, individually or in combination, a memory module

system with a plurality of buffers mounted in positions corresponding to the respective sets of data / strobe signal lines, each buffer providing data paths between the data / strobe signal lines and a set of memory devices and including logic that responds to control signals by enabling the data paths corresponding to memory operations between the data / strobe signal lines and the memory devices, wherein the logic is configured to obtain timing information based on signals received by the buffers during a second memory operation prior to the first memory operation and to control timing of the data and strobe signals on the data paths in accordance with the obtained timing information as claimed. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Id., 127-28 (citing *id.*, 46-71 (“Description of the Embodiments”)).

58. The applicant filed an Amendment after Notice of Allowance to amend claims 1 and 10 to “correct antecedent basis issues.” *Id.*, 266-269, 277.

6. The 151 Application (The '506 Patent)

59. The '506 Patent issued from Application No, 16/391,151 (“the 151 Application”). EX1002 (506 File History). The 151 Application originally presented 1 claim. *Id.* at 45. The Examiner rejected the claim for obvious-type double patenting over the '608 Patent, the '035 Patent, the '587 Patent, and the '632 Patent. *Id.*, 140-151. The Examiner also rejected the original claim 1 as anticipated by U.S. Patent No. 8,565,033 to Manohararajah (EX1026). *Id.*, 151-

153. In response, the applicant submitted terminal disclaimers, canceled the original claim 1, and introduced twenty new claims. *Id.*, 173-184.

60. The Examiner subsequently issued a Notice of Allowance. *Id.*, 195. In that Notice, the Examiner provided the following reasons for allowance:

Prior art teaches memory controller systems with memory arranged into memory ranks and memory modules including a buffer provided for buffering signals / data to and from memory chips on the memory modules; and memory systems that implement delays for transmitting signals to and from memory devices of a memory module including delaying strobe signals, however, the prior art does not fairly teach or suggest, individually or in combination, a memory controller system with memory modules having control and address signal lines implemented to be used corresponding to memory read operations to and from memory devices of the memory module that are arranged in multiple ranks with data buffers coupled to the memory devices, where memory read operations output read data and read strobes associated with the memory read operations, and where the data buffer implemented delaying of a first read strobe by a predetermined amount, i.e. generating a delayed read strobe, sampling the first section of read data using the delayed read strobe, and transmitting the section of read data to a data bus, where the predetermined amount of delay is determined based at least on signals received by the data buffer before the memory read operation as claimed. Applicant argues these limitations on Pages 11-13 of Applicant's Remarks filed 4/10/2020. These limitations find support in Applicant's Specification on Pages 5-30. The prior art of record neither anticipates nor renders obvious the above recited combination.

Id., 201-202 (citing *id.*, 19-44).

61. During prosecution of the '506 Patent, the applicant did not disclose to the Examiner U.S. Patent Publication No. 2010/0312956 to Hiraishi (EX1005), U.S. Patent Publication No. 2007/0008791 to Butt (EX1029), U.S. Patent No. 8,020,022 to Tokuhiro (EX1006), or U.S. Patent No. 6,184,701 to Kim (EX1008), and I am not aware of any evidence that the Examiner considered these references during prosecution. *See* EX1001; EX1002.

E. Challenged Claims

62. This declaration relates to claims 1-20 of the '506 Patent. Those claims as listed in **Appendix A**.

F. Construction of Terms Used in the Patent Claims

63. I understand that claim terms should be given their ordinary and customary meaning as understood by one of ordinary skill in the art in view of the patent and its file history. As detailed in my analysis and set forth below, I have used what I believe to be the ordinary and customary meaning of the claim terms as understood by one of ordinary skill in the art in view of the '506 Patent and its file history.

64. I also understand that where a patent applicant provides an explicit definition of a claim term in the specification, that definition may control the interpretation of that term in the claim.

65. I also understand that if no explicit definition is given to a term in the patent specification, the claim terms must be evaluated using the ordinary meaning of the words being used in those claims, evaluated from the perspective of a person of ordinary skill in the art.

66. I understand that in litigation between Micron and Netlist involving the parent and grandparent to the '506 Patent, there is a claim construction dispute where Micron asserts that certain terms are subject to § 112, ¶ 6 and indefinite for failure to disclose an adequate structure or algorithm, EX1041 at 9-11, while Netlist asserts that those terms are not subject to § 112, ¶ 6 and should be given their plain and ordinary meaning, EX1042 at 4-5. I am not aware of any claim construction ruling resolving this claim construction dispute, so for now I am assuming that those claim terms (and the corresponding claim terms in the '506 Patent) are not invalid, and as discussed below, the prior art discloses the examples provided in the '506 Patent, and thus it is not necessary for purposes of my analysis to determine whether any terms of the '506 Patent are governed by § 112, ¶ 6.

67. I understand that, in IPR2017-00730, Petitioner proposed constructions for certain terms under the broadest reasonable interpretation; Patent Owner asserted that those terms have the ordinary meaning as understood by a Skilled Artisan; and the Board found that no express construction was necessary

for any of those terms. EX1014 (632 Decision) at 8. Below, I address some claim terms in the '506 Patent, including some terms that were also discussed in IPR2017-00730, and I show how the specification uses those terms. As I further discuss below, the prior art discloses these terms in the same sense as used in the '506 Patent. Accordingly, I do not expect that an express construction is necessary for these terms to resolve the validity issues discussed in this declaration.

1. “*memory module*”

68. In light of the '506 Patent specification, a Skilled Artisan would have understood that the claim term “*memory module*” includes a printed circuit board or other removable carrier that contains multiple RAM memory chips.

69. For instance, the '506 Patent discloses that a “memory module usually includes multiple memory devices, such as dynamic random access memory devices (DRAM) or synchronous dynamic random access memory devices (SDRAM), packaged individually or in groups, and/or mounted on a printed circuit board (PCB).” EX1001 at 1:50-55; *see also* Microsoft Computer Dictionary 334 (5th ed. 2002) (EX1023) (defining a “memory module” as a “removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips.”).

2. “*memory controller*”

70. In light of the '506 Patent specification, a Skilled Artisan would have understood that the claim term “*memory controller*” includes “any device capable

of sending instructions or commands, or otherwise controlling memory devices.”

EX1001 at 4:46-49.

3. “*memory bus*”

71. In light of the ’506 Patent specification, a Skilled Artisan would have understood that the claim term “*memory bus*” includes “any component, connection, or groups of components and/or connections, used to provide electrical communication between a memory module and a memory controller.” EX1001 at 4:50-53. “For example, in various embodiments, the memory bus 105 may include printed circuit board (PCB) transmission lines, module connectors, component packages, sockets, and/or any other components or connections that provide connections for signal transmission.” *Id.* at 4:53-58.

4. “*module control signals*”

72. In light of the ’506 Patent specification, a Skilled Artisan would have understood that the claim term “*module control signals*” includes signals that the module controller (i) derived in response to memory command signals from the memory controller and (ii) provided to the data buffers to control their operations.

73. For example, the ’506 Patent states that “the module control device ... generates ... a set of module control signals in response to each memory command from the memory controller and the module control signals . . . are transmitted by the module control device to the [data] buffer circuits via module control signal

lines.” EX1001 at 3:41-50; *id.*, 5:43-51 (“Examples of module control signals include, but are not limited to a mode signal (MODE), which specifies a mode of operation (*e.g.*, test mode or operating mode) for the isolation devices 118; one or more enable signals, which are used by an isolation device to select one or more subgroups of memory devices to communicate data with the memory controller; and one or more ODT signals, which are used by the isolation devices to set up on-die termination for the data/strobe signals.”).

5. “*metastability*”

74. In light of the ’506 Patent specification, a Skilled Artisan would have understood that the claim term “*metastability*” includes a condition when a signal has a misalignment with the relevant clock signal resulting in an output signal with a temporary indeterminate binary value.

75. For example, the ’506 Patent states that, “[a]s the module control signals travel over such a distance, they can become misaligned with the module clock signal, resulting in metastability in the received module control signals.” EX1001 at 9:42-45 (emphasis added);² *see also* EX1022 (Stone textbook) at 107 (explaining “metastable” state is when “the output lies about midway between a logic 0 and logic 1. The output stays in this condition for a variable and

² All emphasis in this declaration has been added unless otherwise indicated.

unpredictable amount of time, then relaxes unpredictably to either a logic 0 or logic 1.”).

IV. OVERVIEW OF THE PRIOR ART

A. U.S. Publication No. 2010/0312956 to Hiraishi (EX1005)

76. United States Published Patent Application No. US 2010/0312956 to Hiraishi (“Hiraishi”) was filed in the United States on June 3, 2010 and published on December 9, 2010. EX1005. I therefore understand that Hiraishi is prior art to the ’506 Patent pursuant to at least 35 U.S.C. §§ 102(a), (b) & (e). Hiraishi was not cited or discussed during prosecution of the ’506 Patent. *See* EX1002.

77. Hiraishi discloses an information processing system 10 including a memory system (20) with a memory module (100) and a memory controller (“memory control hub,” MCH 12) for controlling the memory module. EX1005 (Hiraishi), FIG. 2, [0063-65].

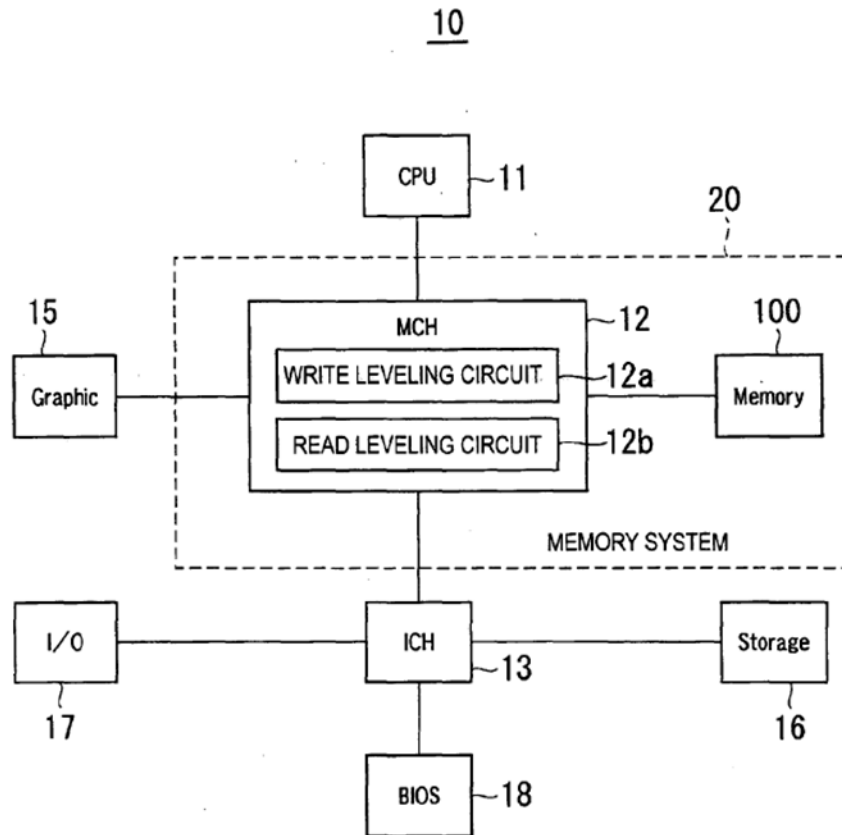


FIG.2

Hiraishi also discloses a perspective view that includes the memory system 20. *Id.*

[0067-68], FIG. 3 (reproduced below).

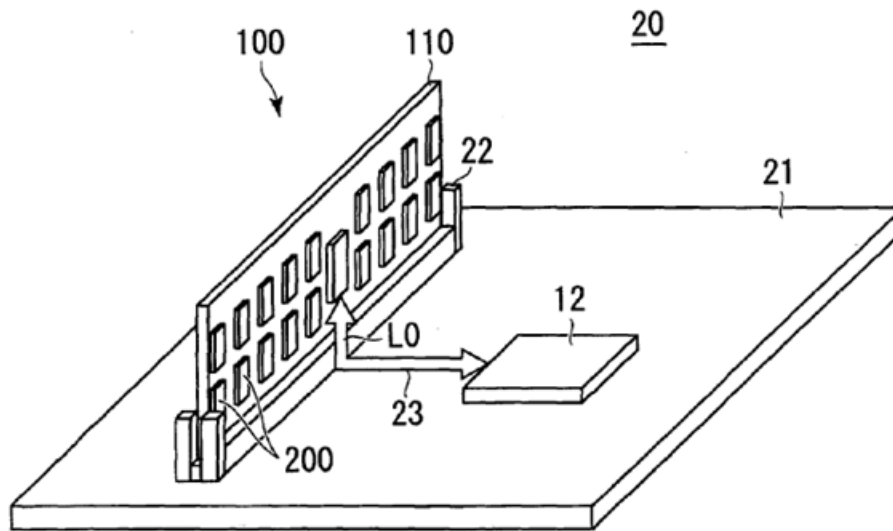
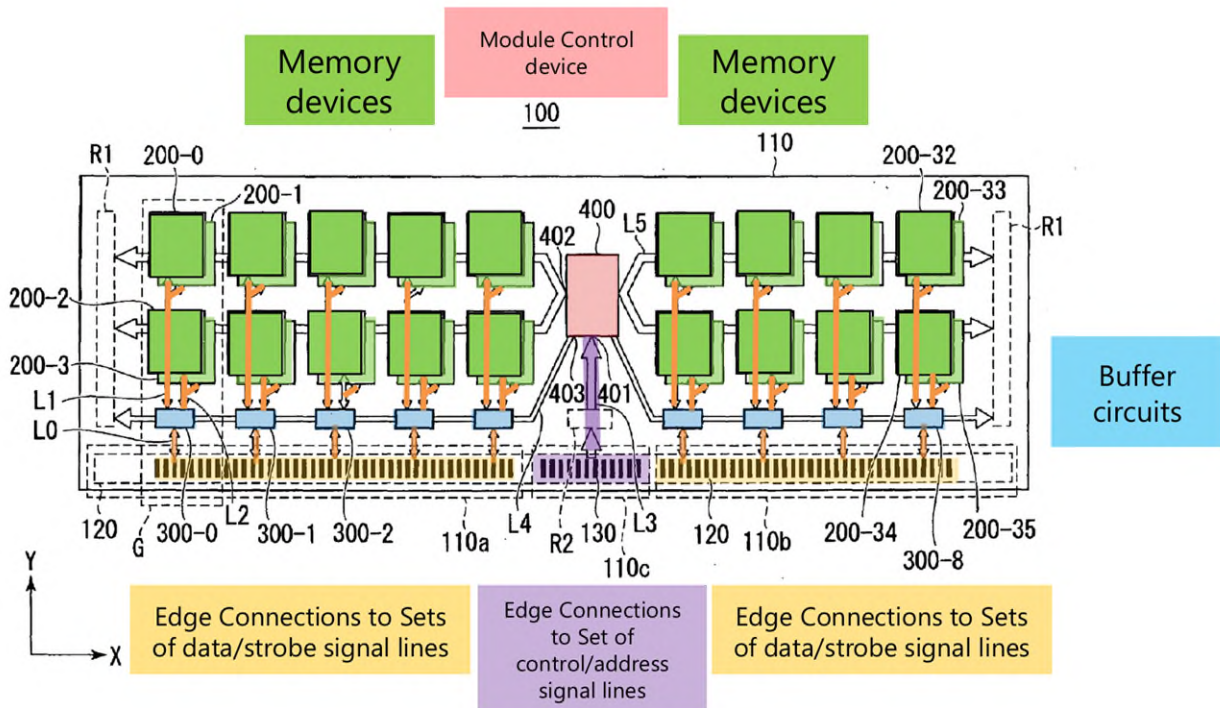


FIG.3

“As shown in FIG. 3, a memory slot 22 is provided on the motherboard 21, so that the memory module 100 is inserted in the memory slot 22. On the other hand, a memory controller 12 is directly mounted on the motherboard 21.” *Id.*

78. Annotated Figure 1 of Hiraishi, reproduced below, illustrates an implementation of the memory module 100. The memory module 100 includes a “command/address/control register buffer” (400, red), EX1005 at ¶¶[0045], [0059], [0060], “memory chips” (200, green), *id.*, and “data register buffers” (300, blue), *id.*, ¶¶[0046], [0055]. The memory module also includes “data connectors” (120, yellow), *id.*, ¶[0048], and “command/address/control connectors” (130, purple), *id.*, at ¶[0049], to couple the corresponding data/strobe lines and control/address signal lines of a system memory bus.



A connection diagram of the memory module 100 is illustrated in FIG. 7 of Hiraishi, showing the connections in the middle and one (left) side of the module 100, including the bus L0 between the data connectors 120 and the data register buffer, the busses L1 and L2 between the data register buffer (300) and the memory devices (200), the bus L3 between the command/address/control connectors 130 and the command/address/control register buffer 400, the bus L4 between the command/address/control register buffer 400 and the data register buffer (300), and the bus L5 between the command/address/control register buffer 400 and the memory devices (200). *Id.* [0103], [0107] and FIG. 7 (reproduced below with annotations).

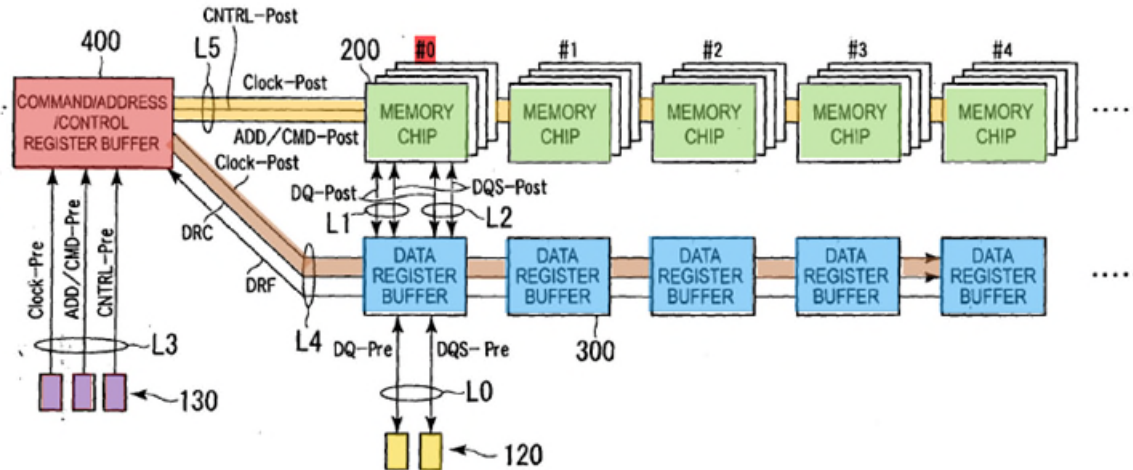


FIG. 7

79. The memory module can include “thirty-six memory chips,” (200, green), EX1005, ¶[0046], which are mounted on “a printed circuit board that includes a multilayer wiring. The planar shape of the module substrate 110 is substantially rectangle.” *Id.*, ¶[0047]. A plurality of data connectors (120, yellow) and a plurality of command/address/control connectors (130, purple) are located along one of the long sides, and are provided “for making an electrical connection with a memory controller via a memory slot.” *Id.*

80. The 36 memory chips are in a “4-rank configuration.” *Id.*, ¶[0051]. “[F]our memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other.” *Id.*, ¶[0052]. The memory module includes “nine data register buffers”

(300, blue), each of which is associated with one of the nine groups of four memory chips. *Id.*, ¶[0046], [0055]. The data connectors (120, yellow) “exchange write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller.” *Id.*, ¶[0048]. The data connectors are located “substantially right below the memory chips,” with the corresponding data register buffers in between the memory chips and the connectors. *Id.* ¶[0048], [0056] & Fig.1.

81. The “command/address/control register buffer” (400, red) is centrally located on the memory module. *Id.*, ¶[0059]. The “command/address/control connectors” (130, purple) are centrally located below the “command/address/control register buffer” (400, red), and are “connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400.” *Id.*, ¶[0049] & Fig.1.

82. The “command/address/control register buffer” (400, red) “receives the command signal, the address signal, the control signal, and the clock signal” from the memory controller at an input terminal 401 (purple), “buffers the signals, and supplies the signals” at an output terminal 402 (orange) to the memory chips (200, green). *Id.*, ¶[0060], [0061]. Simultaneously, the “command/address/control register buffer” (400, red) “generates a control signal” and supplies it at the output

terminal 403 (brown) to the data register buffers (300, blue). *Id.*, ¶[0060], [0096-97], FIG. 6 (reproduced below with annotations).

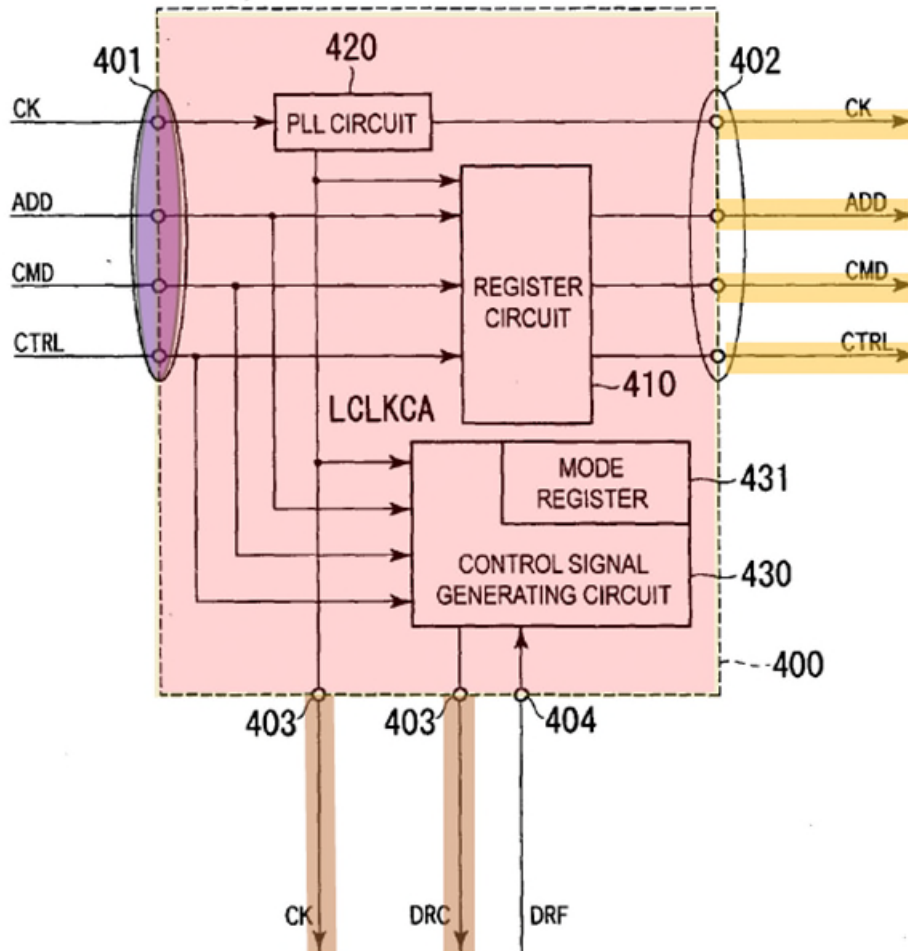


FIG.6

83. Because of high speed operation and differing locations of “memory chips” (200, green) and “data register buffers” (300, blue) relative to the “command/address/control register buffer” (400, red), Hiraishi recognizes that there may be signal timing discrepancies. *Id.*, ¶[0090], [0104]. Accordingly, the memory module makes “timing adjustments” to account for the signal timing

discrepancies during initialization by performing write leveling and read leveling operations. *Id.*, ¶[0140]-[0141]. Each group of memory chips/data register buffer performs two sets of write and read leveling operations, one “between the data register buffer 300 and the memory chip 200” referred to as “Step S4,” *id.*, ¶[0140], and one “between the memory controller and the data register buffer 300” referred to as “Step S5,” *id.*, ¶[0141].

84. An implementation of Hiraishi’s data register buffer 300 is illustrated in FIG. 5 (reproduced below with annotations). As shown here, the data register buffer 300 (blue) includes a data register control circuit 320 (upper right) with a write leveling circuit 322 and a read leveling circuit 323 to perform the “S4” leveling operations between the data buffer and the memory chips. *Id.* ¶[0142], [0147], and FIG. 5 (reproduced below with annotations).

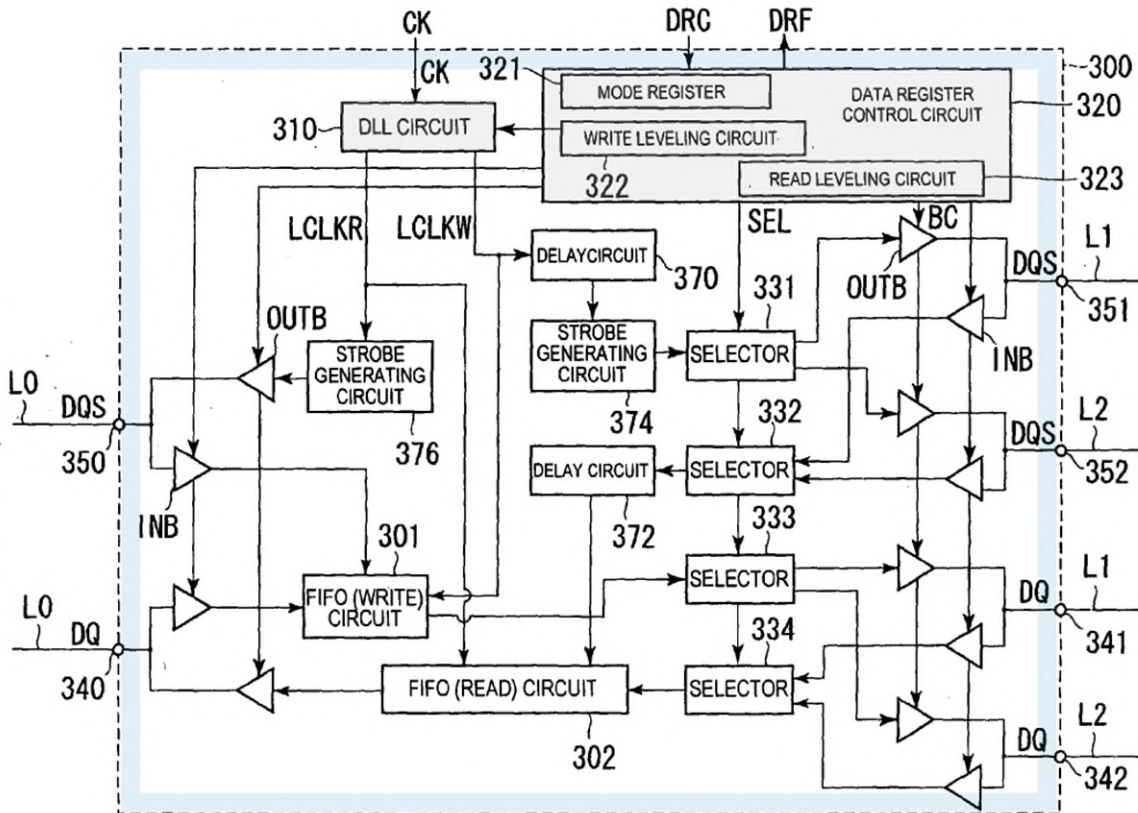


FIG.5

The “data register buffer” (300, blue) also includes a “DLL circuit” (310). *Id.*, ¶[0084]. “The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400.” *Id.*, ¶[0087]. For example, “[a]n output operation timing of the FIFO (Write) circuit 301 is defined by the internal clock LCLKW that is generated by the DLL circuit 310[, and a]n output operation timing of the FIFO (Read) circuit 302 is defined by the internal clock LCLKR that is generated by the DLL circuit 310.” *Id.*

B. U.S. Patent Publication No. 2007/0008791 to Butt (EX1029)

85. U.S. Patent Publication No. 2007/0008791 to Butt (EX1029) was filed on July 7, 2005, and published on January 11, 2007. I understand that Butt is prior art to the '506 Patent pursuant to at least 35 U.S.C. §§ 102(a), (b), & (e). Butt was not cited or discussed during the prosecution of the '506 Patent. See EX1002.

86. Butt discloses a method for calibrating a data valid window for memory devices. EX1029 at [0005]. According to Butt, previous approaches “relie[d] heavily on the pre-silicon, system-level, SPICE timing analysis,” and there was thus a need for calibrations that could calibrate the actual data valid window in the silicon. *Id.*, [0003]-[0004]. Butt describes the method as follows:

(A) setting a base delay of one or more datapaths to a predetermined value, (B) determining an optimum offset delay value for each of the one or more datapaths based upon actual memory accesses and (C) delaying a read data strobe signal based upon the base delay and the optimum offset delay value for each of the one or more datapaths.

Id., [0005].

87. Butt further describes an exemplary circuit for implementing this method, with a block diagram of illustration in FIG. 2 (reproduced below). As shown here, physical read datapaths 114 (red) can be configured to receive both the read data signals (DQ) (orange) and the read data strobe (DQS) (orange,

dashed) from the DDR memory (green), and to communicate with asynchronous first-in, first-out buffers 112 (olive). *Id.*, [0017].

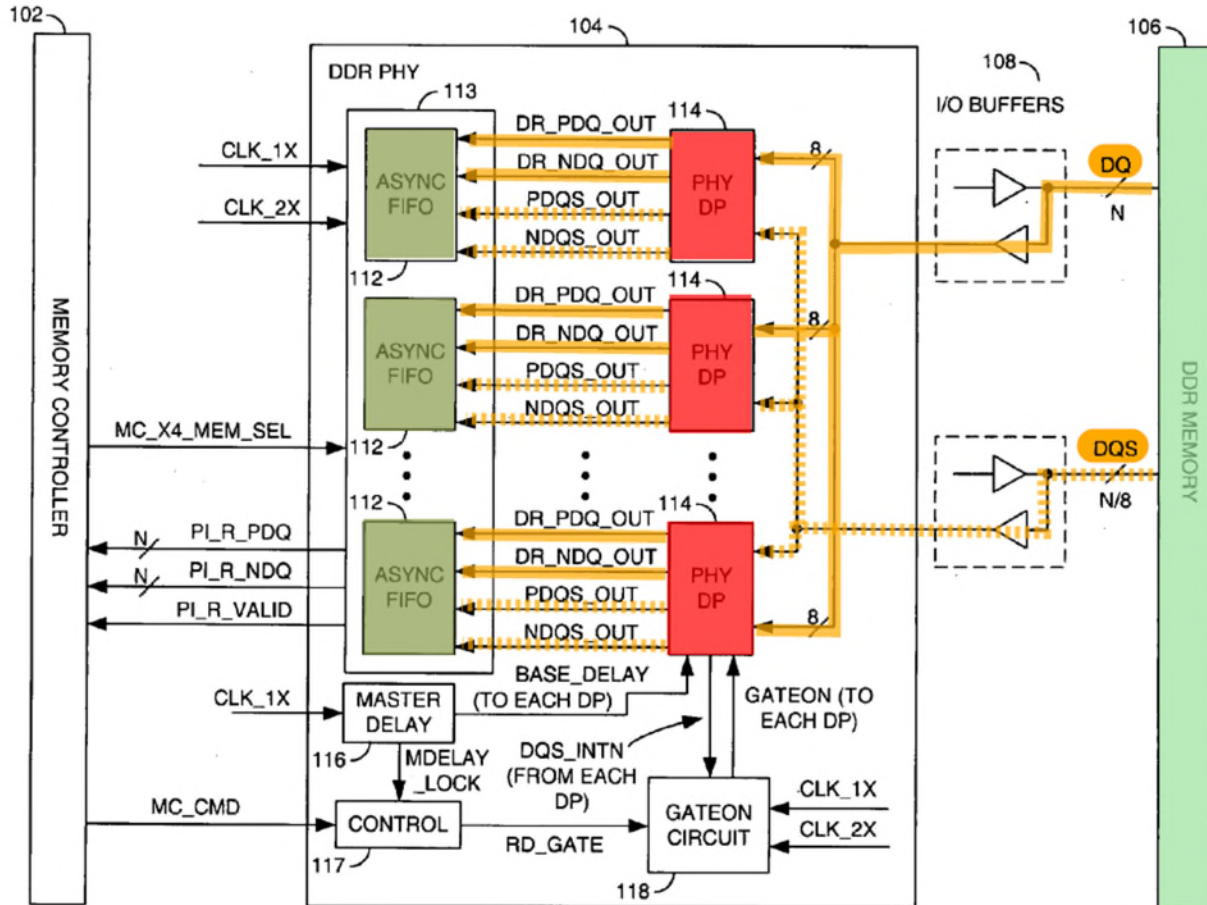


FIG. 2

Id., Fig. 2.

88. Butt further teaches that the datapaths 114 (red) sample the data signal DQ (orange) based on a delayed read strobe signal DQS (orange dashed):

The DPs may be configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116. Each of the DPs 114 may be configured to present the DQ data to a respective asynchronous

FIFO 112 via the signals DR_PDQ_OUT and DR_NDQ_OUT, after the data is sampled using the delayed read data strobe signals DQS.

Id., [0018]. The master delay (“MDELAY”) circuit 116 in Butt can set a base delay for the datapaths 114. *Id.*, [0014], [0022].

89. Butt further describes additional training by which the datapath 114 can achieve an optimum offset for centering the read strobe DQS data eye in the valid data window:

The present invention generally provides for adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window. For example, when the delay is too short, the read data strobe signal DQS is generally earlier than a minimum boundary of the valid data eye window (e.g., trace 140). When the delay is too great, the read data strobe signal DQS is generally later than a maximum boundary of the valid data eye window (e.g., trace 142). In general, a correctly set delay places the read data strobe signal DQS within the valid data eye window (e.g., trace 144).

Id., [0035]. As illustrated below in Fig. 5, the optimum offset for each datapath 114 is determined by iteratively checking the validity of test data at different offsets until a maximum and minimum offset are identified. *Id.*, [0045], Figs. 6 and 7. These minimum and maximum values can then be used to determine the optimal offset for the data eye. *Id.*, [0046].

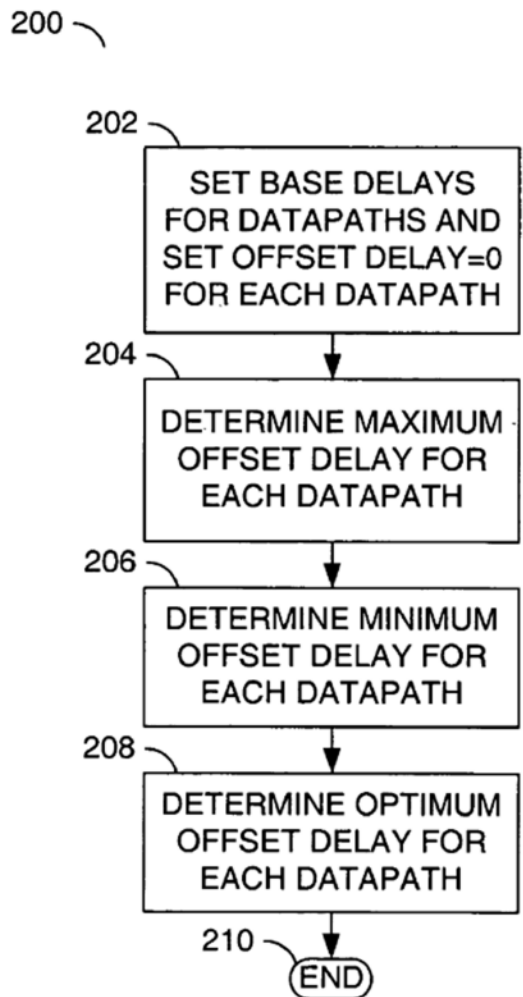


FIG. 5

Id., Fig. 5. The optimum offset values can then be programmed into each datapath 114, which is the end of the training. *Id.*, [0046].

C. U.S. Patent No. 8,020,022 to Tokuhiko (EX1006)

90. U.S. Patent No. 8,020,022 to Tokuhiko (EX1006) was filed on September 12, 2008 and issued on September 13, 2011. I understand that Tokuhiko

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

is prior art to the '506 Patent pursuant to at least 35 U.S.C. §§ 102(a) & (e).

Tokuhiro was not cited or discussed during the prosecution of the '506 Patent. See EX1002.

91. Tokuhiro discloses a memory module that includes a plurality of SDRAMs connected to a memory controller by signal lines. EX1006 at 1:38-47. Tokuhiro recognizes the problems of fly-by delays, for example, in DDR3 memory systems. Tokuhiro explains:

[I]n the DDR3 memory interface, because the clock signal line for the clock signal CK is wired to the plurality of SDRAMs 92-1 to 92-n through the daisy chain connection and a propagation delay is generated, ***the clock signal CK output from the memory controller 90 cannot reach all the SDRAMs 92-1 to 92-n at the same time.*** According to the JEDEC standards, for example, a length L1 of outer dimension of the DIMM module 91 is determined to be 133 mm. Assuming a data transmission speed to be 7 ps/mm, therefore, a difference of about 1 ns is generated in arrival time of the clock signal CK between the SDRAM 92-1 disposed at one end and the SDRAM 92-n disposed at the other end of the DIMM module 91 in the lengthwise direction thereof (namely, $7 \text{ ps/mm} \times 133 \text{ mm} = 931 \text{ ps}$).

EX1006 at 1:63-2:9. Tokuhiro further notes that, for this reason, the JEDEC standards specify employing write leveling in the DDR3 memory interface. *Id.*, 2:10-12.

92. However, Tokuhiro notes that although “the DDR3 memory interface compensates the arrival time when the data strobe signals DQS-1 to DQS-n arrive at the SDRAMs 92-1 to 92-n in the write operations according to the JEDEC standards as described above, ***compensations of the signal arrival time in read operations are not provided with the JEDEC standards.***” *Id.*, 2:54-59. Tokuhiro explains that in connection with conventional DDR3 memory interfaces, “the data signal DQ-n and the data strobe signal DQS-n output from the SDRAM 92-n to which the clock signal CK is input lastly arrives at the memory controller 90 approximately 1 ns after the data signal DQ-1 and the data strobe signal DQS-1 output from the SDRAM 92-1 to which the clock signal CK is input firstly where the data transmission speed is 7 ps/mm as the case described above. $7 \text{ ps/mm} \times 133 \text{ mm} = 931 \text{ ps}$.” *Id.*, 3:1-8.

93. Tokuhiro further identifies a specific problem that happens when this fly-by delay becomes greater than one clock cycle:

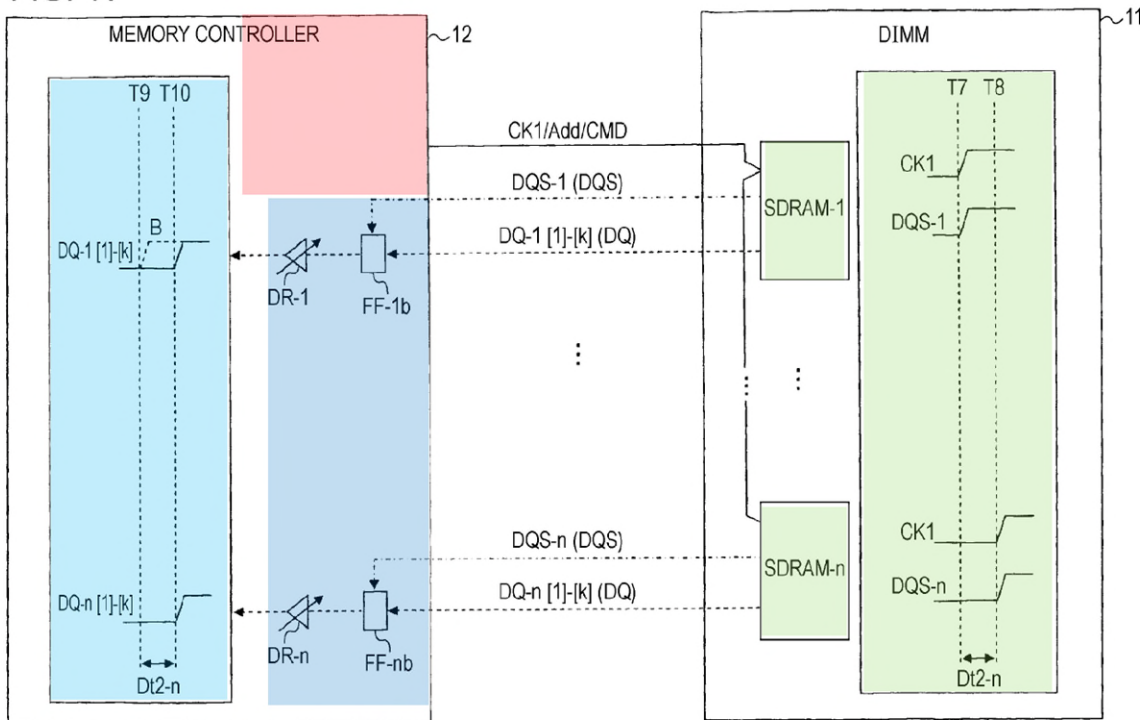
The delay on the order of 1 ns will become ***greater than a typical data period*** of the DDR3 memory interface, at minimum 0.625 ns, so that ***the delay may affect in reading data*** from the SDRAM 92.

Id., 3:9-12.

94. As a solution to this problem, Tokuhiro proposes determining a first delay time utilizing the ***write*** leveling function, *i.e.*, a mechanism for determining timing for write operations, and using this delay time not just for write operations

but also to delay the transmission of data during **read** operations. *See, e.g., id.*, 3:16-26 (“a first variable delay unit for delaying, in the write operation, a data strobe signal output to the memory by **a first delay time that is set by utilizing the write leveling function** and **a second variable delay unit for delaying, in the read operation, a data signal input from the memory by a second delay time that is set based on the first delay time**”); Fig. 11 (annotated, showing compensations to fly-by delays of memory devices SDRAM-1 to SDRAM-n (green) by respective read delay elements DR-1 to DR-n in a data-handling part (blue) interfacing with the memory devices during a memory read operation):

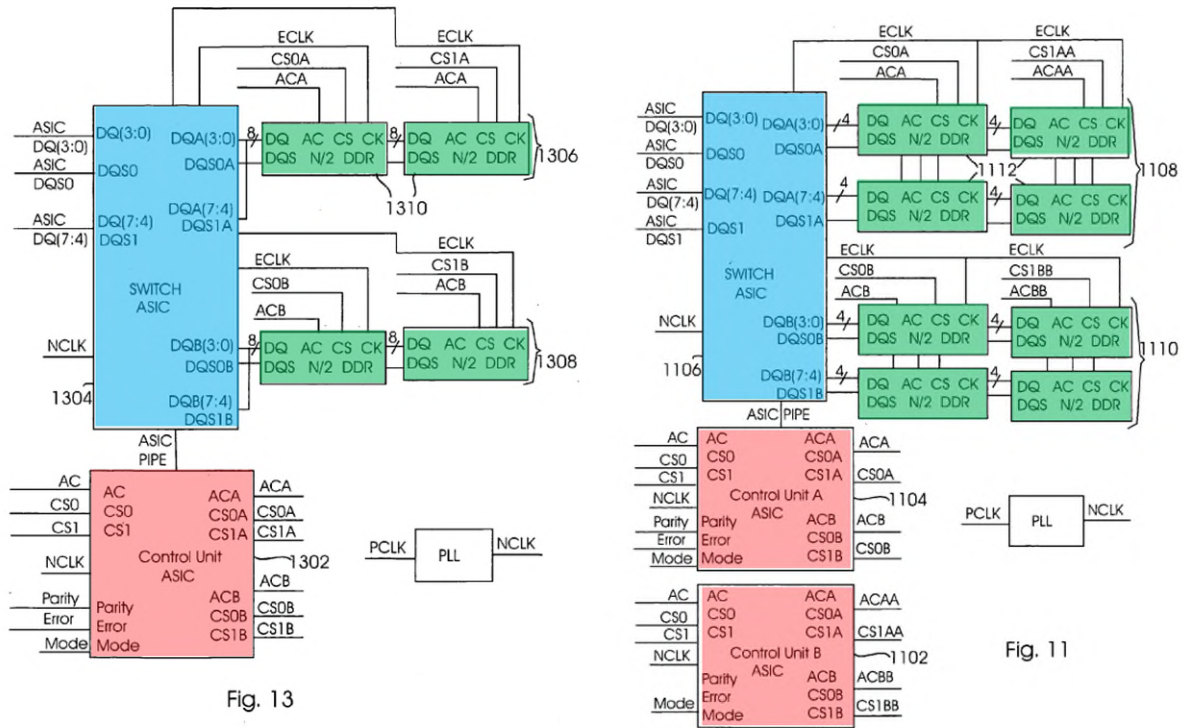
FIG. 11



D. U.S. Patent Publication No. 2006/0277355 to Ellsberry (EX1007)

95. U.S. Patent Application Publication No. 2006/0277355 to Ellsberry (“Ellsberry”) (EX1007) was filed on June 1, 2005 and published on December 7, 2006. I understand that Ellsberry is prior art to the ’506 Patent pursuant to at least 35 U.S.C. §§ 102(a) & (b). Although Ellsberry was cited in the ’506 Patent (among hundreds of other references, *see* EX1002 at 116, 216, 261), it was not discussed during prosecution. *See* EX1002.

96. Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi and additionally expressly describes modules with 8-bit wide data buffers and with either 8-bit wide chips or pairs of 4-bit wide chips. For example, Ellsberry’s FIGS. 2, 5, and 13 correspond to an embodiment of Ellsberry utilizing 8-bit memory devices, EX1007 at ¶[0056], FIGS. 2, 5, 13 (FIG. 13 reproduced below), while FIGS. 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit memory devices, EX1007 at FIGS. 2, 6, 11 (FIG. 11 reproduced below); *see also* EX1015 (’907 Decision) at 57, 60, 66, 68, 77, 81 (Board concluding that Ellsberry discloses 8-bit memory devices, and also pairs of 4-bit memory devices).



E. U.S. Patent No. 6,184,701 to Kim (EX1008)

97. United States Patent No. 6,184,701 to Kim (“Kim”) (EX1008) was filed on May 27, 1999 and issued on February 6, 2001. I therefore understand that Kim is prior art to the ’506 Patent pursuant to at least 35 U.S.C. §§ 102(a) & (b).

98. Kim teaches that, when a circuit “receives input signals at similar analog levels [it] may be prone to generating an output signal in a metastable state (i.e., where the potential of the output signal is greater than a maximum logic 0 level (VJL) and less than a minimum logic 1 level (VJH)). Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output

generation.” EX1008 at 1:21-31. To solve that problem, Kim discloses “a metastability detection/prevention circuit 20” to be incorporated with any “main active circuit 10” in need thereof. EX1008 at 2:23-24. For example, Kim teaches that the “the circuit 10 may comprise a data input buffer.” *Id.*, 2:30-31. “[T]he metastability detection/prevention circuit 20 preferably performs the function of detecting whether the output POUT of the main active circuit 10 has been disposed in a metastable state for a duration in excess of a transition duration.” *Id.*, 2:33-37.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS

A. Claims 1, 2, 4, 6, 7, 11, 13-15, 17 and 18 are Obvious Over Hiraishi Alone or Further in View of Butt.

99. I understand that in related litigation, Netlist has suggested that claim 1 of the '506 Patent is satisfied by read training between the memory chips and the data buffers, followed by a read command. *See* EX1038 (Netlist Texas Complaint against Samsung) at ¶¶46, 48; EX1039 (JESD82-32A DDR4DB02 standard) at pp.26,28-29,32-33 (“DRAM-to-DB Read Delay (MRD) Training Mode” for DQ/DQS alignment including the ability to make “fine adjustment of the phase of individual bit lanes relative to the baseline MDQS”). Netlist’s apparent interpretation of the claims differs from the teaching of the '506 Patent, which discloses the use of two different operations, where the “*previous operation*” is a memory operation (*e.g.*, write) that transfers data in a different direction than the later read operation. *See supra* ¶¶43-44. During read leveling — the operation that

Netlist suggests satisfies this limitation — the memory provides read data from a register in response to a read command. After read leveling, the memory also performs a read operation addressed to the memory array in response to a read command. The '506 Patent, however, focuses on signal timing between circuits, and there is no difference in timing between how the memory provides read data during read leveling vs. a read operation. Although read leveling and a read operation differ in terms of the place from which the information is read from (a register during read leveling vs. a memory array location according to an address during a read operation), a Skilled Artisan would have understood at the time that the memory would operate the same way in terms of timing during read leveling and subsequent read operations, since the optimal timing the buffer found during read leveling is for the very purpose of using that optimal timing during the subsequent read operations.

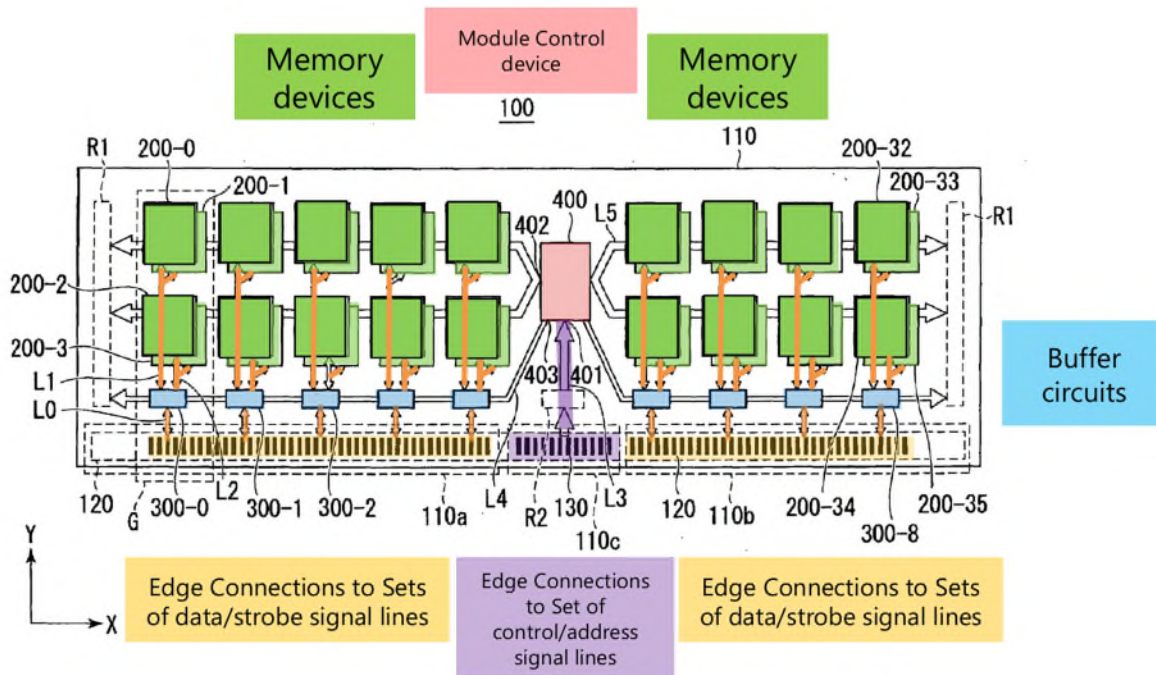
100. Netlist's apparent interpretation also conflicts with the specification of the '506 Patent, which states that the conventional "leveling mechanisms for write and/or read operations for unbalanced wire length ... [are] insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules." EX1001 at 2:28-36. As discussed below in detail, the Skilled Artisan would have understood that, during a conventional read leveling operation, the memory provides read data in response to a read command with the same

timing as used for normal read operations, and the memory controller detects timing information for subsequent read operations assuming that the memory performs all read operations using the same timing. Thus, the '506 Patent teaches to a Skilled Artisan that a traditional leveling operation (e.g., read leveling) followed by a memory operation in the same direction (e.g., read operation) is not directed to two different operations, since read leveling finds timing for a read operation and this read timing is subsequently used for the same type of read operations. Instead, the '506 Patent is directed to different operations of the memory, namely to a “signal alignment mechanism to time the transmission of **read** data signals based on timing information derived from a prior **write** operation.” *Id.* 15:23-26 (emphasis added). In my analysis below, I show that the claims of the '506 Patent are invalid under both the broader interpretation for this limitation asserted by Netlist, *infra* § I.A–C, and under the narrower interpretation that is consistent with the claim language, the specification, and the file history, *infra* § I.D.

1. Claim 1

a) 1[pre]: “A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising”

101. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 of Hiraishi below, Hiraishi discloses “*a memory module [such as memory module 100] operable in a computer to communicate with a memory controller [MCH 12 (Fig. 2)] of the computer system via a memory bus [line 23 (Fig. 3)] including control and address (C/A) signal lines [to couple to command/address/control line L3 on the module, purple] and a data bus [to couple to data line L0 on the module, orange].*”



EX1005 (Hiraishi), Fig. 1 (annotated and color added; “command/address/control register buffer” in red, “memory chips” in green, “data register buffers” in blue, “data connectors” in orange, “command/address/control connectors” in purple).

102. Hiraishi discloses that the memory module 100 is connected to memory control hub (MCH) 12 such that the MCH 12 functions as a memory controller for memory module 100:

The memory module 100 shown in FIG. 1 and a graphic controller 15 are **connected to the MCH 12**. As shown in FIG. 2, the memory module 100 and the MCH 12 constitute a memory system 20, where the MCH 12 has a controller function for the memory module 100. That is, **the MCH 12 functions as a memory controller for the memory module 100**.

Id., ¶[0065]. Hiraishi discloses that memory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) that is coupled to data line L0 and the command/address/control line L3 on the memory module 100. *Id.*, [0069] and FIGS. 2 and 3 (reproduced below).

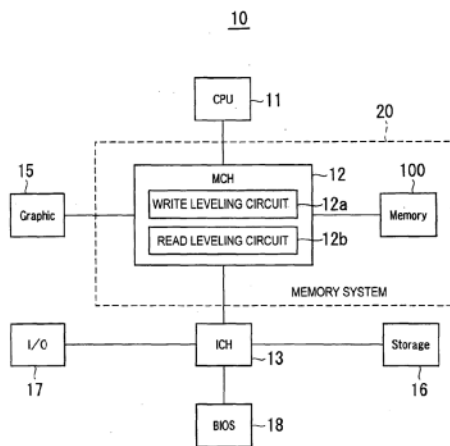


FIG.2

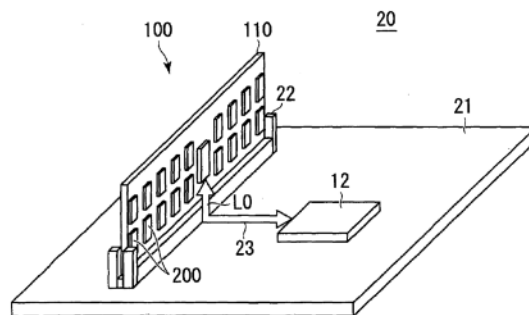


FIG.3

Id., FIGS. 2 and 3. Thus, a Skilled Artisan would have understood that memory module 100 is operable to communicate with the memory controller (MCH 12) via a memory bus (line 23) as recited in the preamble.

103. Hiraishi further discloses that the memory bus (line 23) includes signal lines, the signal lines including a set of control/address signal lines coupling, through command/address/control connectors 130 (purple), to command/address/control line L3, and a plurality of sets of data/strobe signal lines, each set coupling, through data connectors 120 (orange), to data line L0. *See id.*,



As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the ***data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, ***a plurality of data transferred through the data line L0*** is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, ***a data strobe signal transferred through the data line L0*** is represented by a data strobe signal DQS-Pre, and a data

strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

Id., [0103]. Hiraishi also explains that the memory bus includes a set of control/address signal lines:

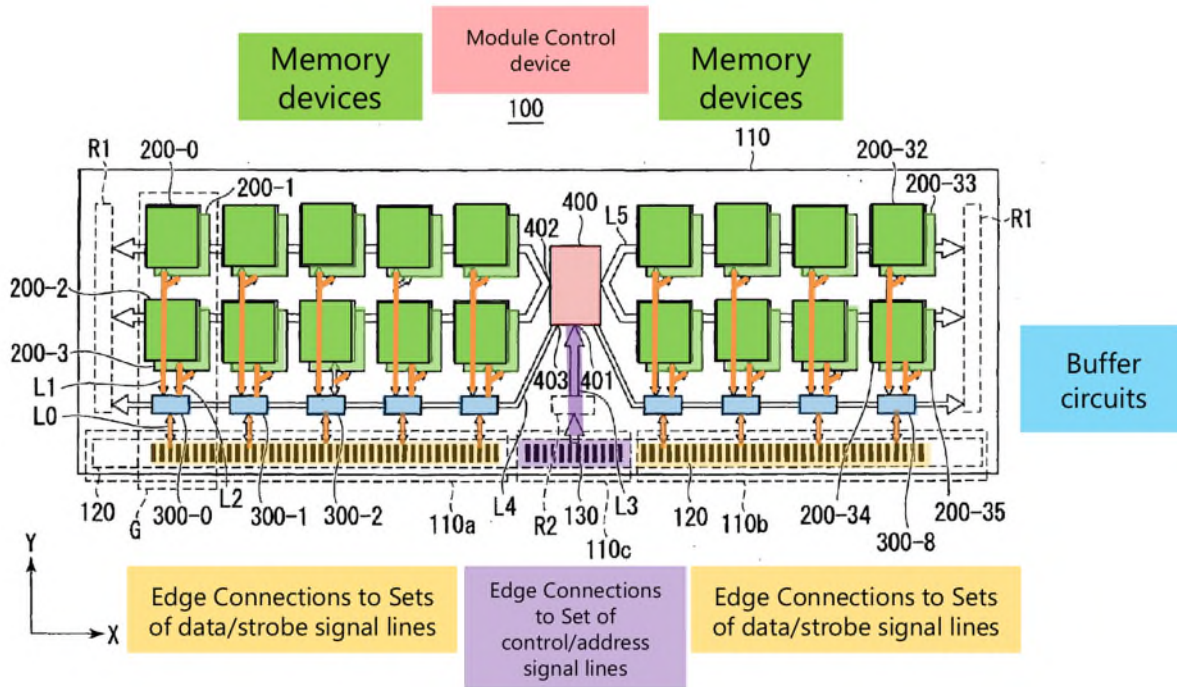
The data connectors 120 and the ***command/address/control connectors 130*** are terminals ***for making an electrical connection with a memory controller*** via a memory slot ... The ***command/address/control connectors 130 are connectors for supplying a command signal, an address signal, a control signal,*** and a clock signal to be supplied to the command/address/control register buffer 400.

Id., [0047], [0049]; *see also* [0060], [0069] (explaining that the signal path between the memory controller 12 and memory chips 200 includes line 23 on the motherboard and the data line L0 and the command/address/control line L3 on the module 100). Thus, a Skilled Artisan would have understood that the memory bus includes signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines as recited in the preamble.

b) 1[a]: “a module board having edge connections to be coupled to respective signal lines in the memory bus”

104. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 of Hiraishi below, Hiraishi discloses “*a module board [module substrate 110] having edge connections [including command/address/control*

connectors 130 (purple) and data connectors 120 (orange)] *to be coupled to respective signal lines in the memory bus [line 23, shown above in Fig. 3].*”



Id., Fig. 1 (annotations and color added showing command/address/control connectors 130 (purple) and data connectors 120 (orange)).

105. Hiraishi discloses that the memory module 100 shown in Figure 1 includes a module substrate:

As shown in FIG. 1, the memory module 100 according to the present embodiment includes **a module** substrate **110**, a plurality of memory chips 200 mounted on the module substrate 110, a plurality of data register buffers 300, and a command/address/control register buffer 400.

Id., [0045].

106. Hiraishi discloses that the module's substrate has connectors 120 and connectors 130 that are arranged at the edge of the substrate:

The ***module substrate 110 is a printed circuit board*** that includes a multilayer wiring. The planar shape of the module PCB 110 is substantially rectangle, as shown in FIG. 1, with a long side in the X direction and a short side in the Y direction. ***On one side of the module substrate 110 along the X direction, which is the long side, a plurality of data connectors 120 and a plurality of command/address/control connectors 130 are provided.***

Id., [0047]. Thus, a Skilled Artisan would have understood that data connectors 120 and command/address/control connectors 130 are “*edge connections*” as recited in the claim. Indeed, the '506 Patent does not even mention the term “*edge connections*,” and its figures provide less detail about connections at the edge of the module than Hiraishi does. Compare, e.g., EX1005, Hiraishi's Fig. 1 (above), to EX1001, Fig. 2C of the '506 Patent (reproduced below with similar coloring annotations).

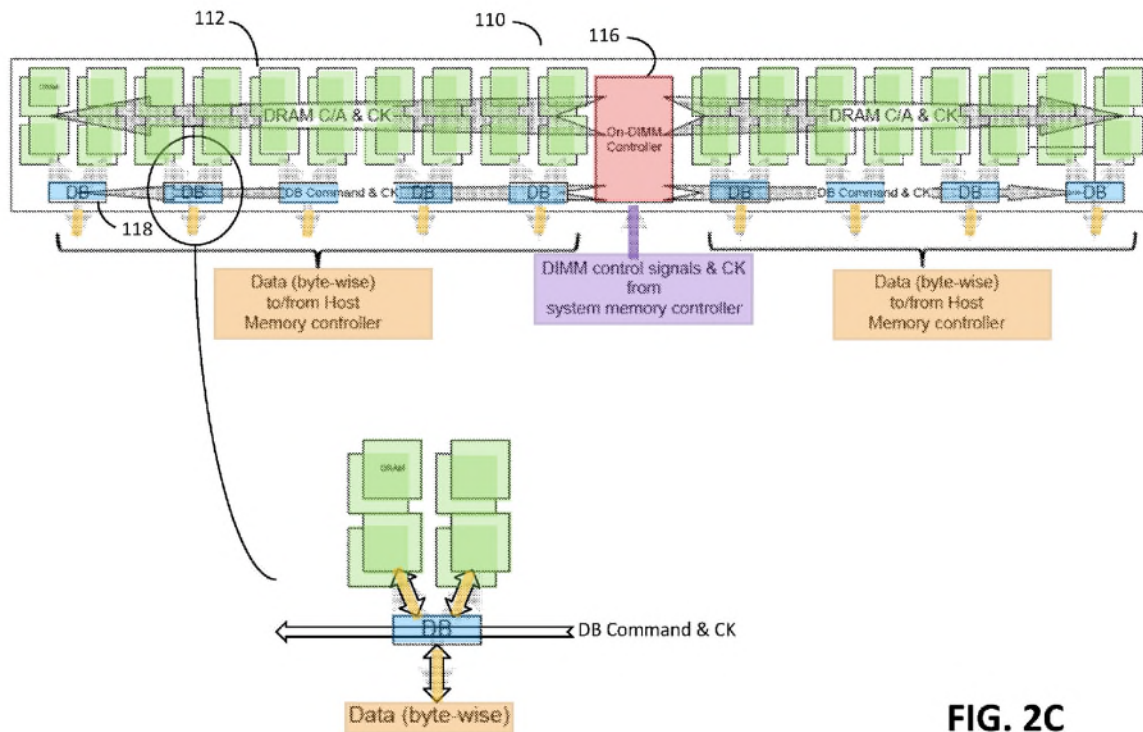


FIG. 2C

107. Hiraishi also discloses that the connectors 120 and 130 are “terminals for making an electrical connection with a memory controller” and that they are used, respectively, for exchanging write and read data with the memory controller, and for supplying command, address, control, and clock signals to the register buffer:

The data connectors 120 and the command/address/control connectors 130 are ***terminals for making an electrical connection with a memory controller*** via a memory slot, which will be described later.

EX1005 (Hiraishi), [0047];

The ***data connectors 120*** are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller.

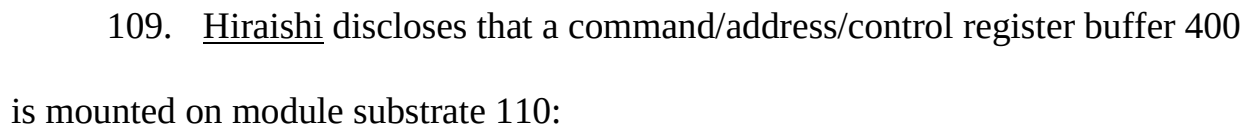
Id., [0048];

The ***command/address/control connectors 130*** are connectors for supplying a command signal, an address signal, a control signal, and a clock signal to be supplied to the command/address/control register buffer 400.

Id., [0049]. Thus, a Skilled Artisan would have understood that the “terminals for making an electrical connection” are edge connections to be coupled to respective signal lines in the memory bus.

c) 1[b]: “a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals”

108. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 1 below, Hiraishi discloses “*a module control device [command/address/control register buffer 400, red] on the module board [substrate 110].*”



Id., [0059].

Samsung Electronics Co., Ltd.
Ex. 1045, p. 64

buffer 400, red) is “configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines [through command/address/control connectors 130 and command/address/control line L3 (Fig. 7) at input terminal 401 (Fig. 6, purple)] and to output registered C/A signals [module command/address/control line L5 (Fig. 7) at output terminal 402 (Fig. 6, orange)] in response to the input C/A signals and to output module control signals [DRC and Clock-Post (brown) on control line L4 (Fig. 7) at output terminal 403 (Fig. 6)].”

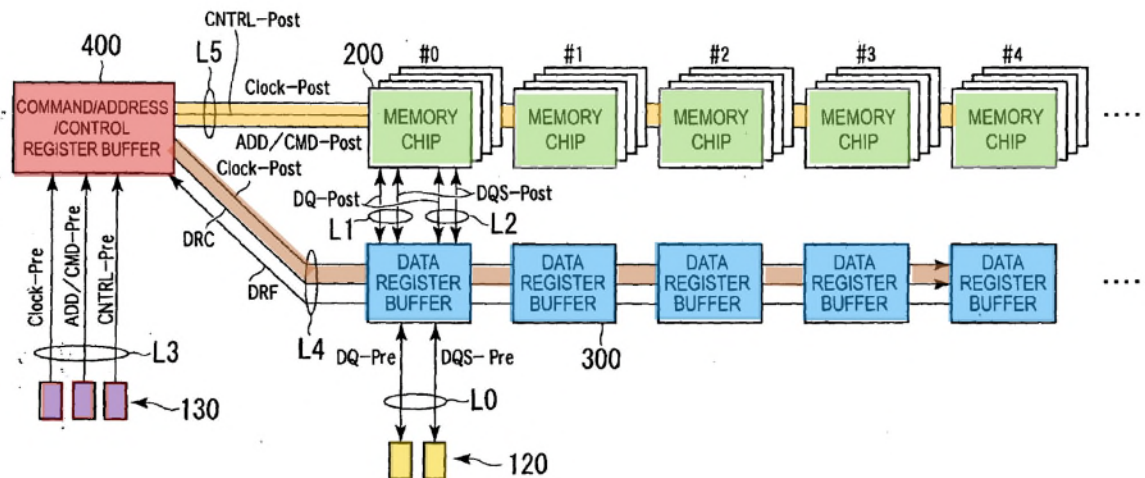


FIG. 7

Id., Fig. 7 (color added); see also [0019] (“Fig. 7 is a connection diagram of memory module 100”);

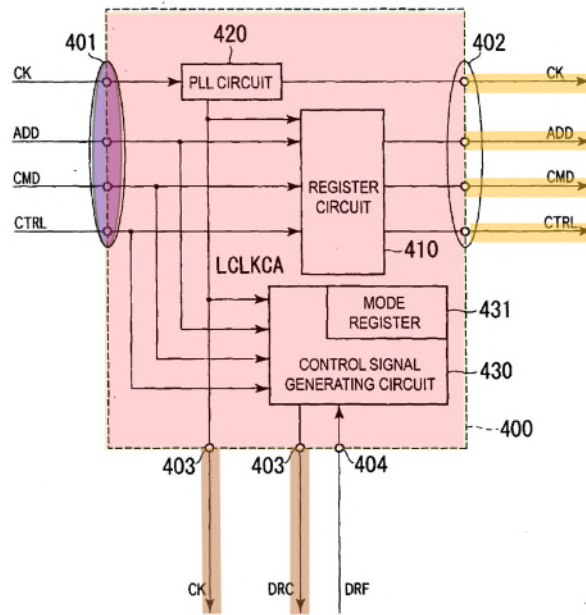


FIG.6

Id., Fig. 6 (color added); *see also id.*, [0018] (“FIG. 6 is a block diagram of the configuration of the command/address/control register buffer 400”).

111. For example, Hiraishi discloses that “the command/address/control **connectors 130** are terminals for making an electrical **connection with a memory controller** via a memory slot” (*Id.*, [0047]) and that “[t]he **command/address/control register buffer 400** receives the command signal, the address signal, the control signal, and the clock signal ... that are supplied **from the command/address/control connectors 130** through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200.” *Id.*, [0060]; *see also id.*, [0097] (“[t]he command/address/control signal that is supplied from the memory controller 12 is input from the input terminal 401.”). Thus, a Skilled

Artisan would have understood that Hiraishi discloses that the module control device (*i.e.*, command/address/control register buffer 400) is configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines.

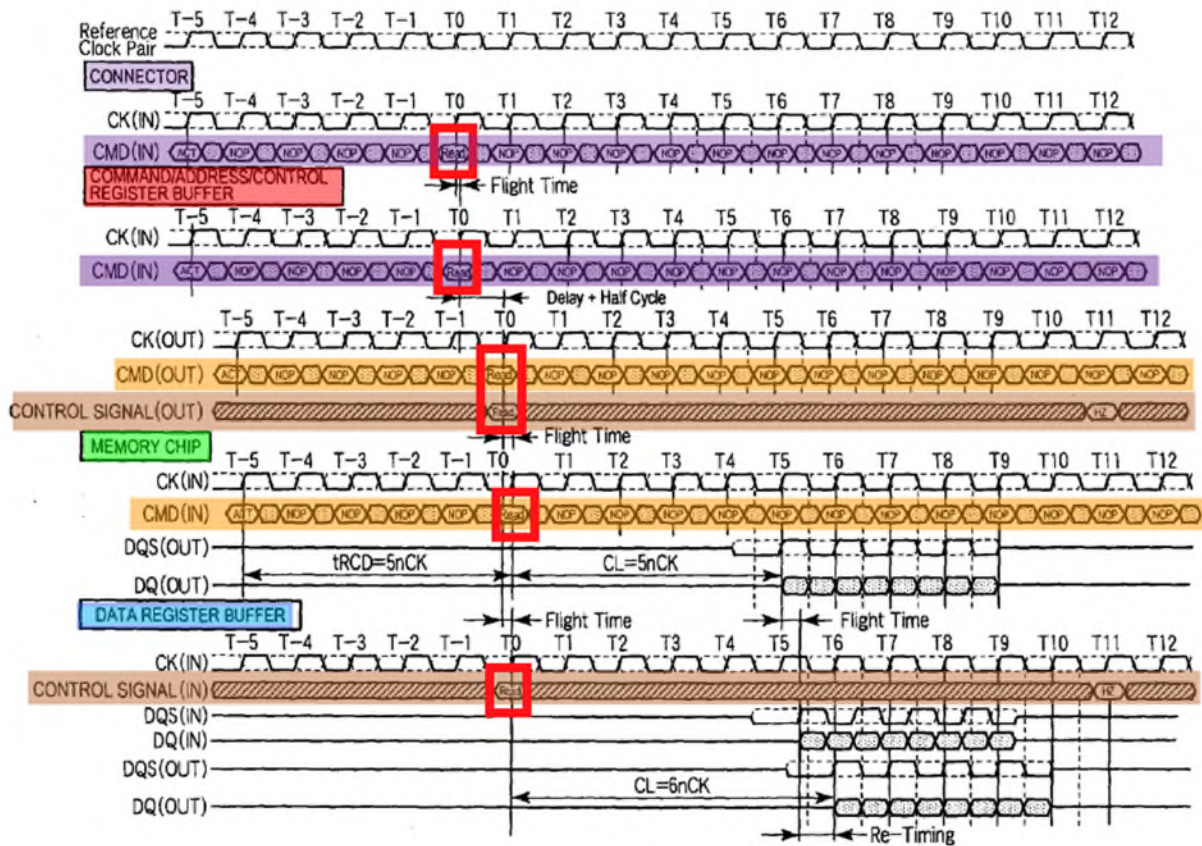
112. Hiraishi further discloses that the “command/address/control register buffer 400 receives the **command signal**, [and] **the address signal** ... supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and **supplies the signals to the memory chips 200.**” *Id.*, [0060]; *see also id.*, [0097] (“[t]he register circuit 410 is a circuit that buffers the command signal CMD, [and] the address signal ADD, ... and the **buffered command signal CMD**, [and] **address signal ADD**... are supplied to the memory chip 200 via the output terminal 402.”). Hiraishi also discloses that “[a]t the same time, the command/address/control register buffer 400 generates a **control signal.**” Hiraishi, [0060]. Hiraishi explains that the control signal generating circuit 430 (which is part of the command/address/control register buffer 400), generates control signals (e.g., DRC) based on the command/address/control signal supplied by input terminal 401:

The control signal generating circuit 430 is a circuit that **generates the control signal DRC** to be supplied to the data register buffer 300 **based on the command/address/control signal supplied via the input terminal 401**, of which an operation is performed in

synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404.

Id., [0099]. Thus, a Skilled Artisan would have understood that Hiraishi discloses that the module control device (*i.e.*, command/address/control register buffer 400) is configurable to output registered C/A signals and module control signals in response to the input C/A signals.

113. Hiraishi discloses that the signals input and output by the command/address/control register buffer 400 can correspond to a memory read operation. *See, e.g., id.*, [0122]-[0131]. Figure 11 (annotated below) shows the timing of a read operation, including receiving a read command (red box at “T0”) on line CMD(IN) (purple) by the Command/Address/Control Register Buffer (red), and outputting corresponding signals on line CMD(OUT) (orange) to the memory chips (green) and on line CONTROL SIGNAL(OUT) (brown) to the Data Register Buffer (blue):

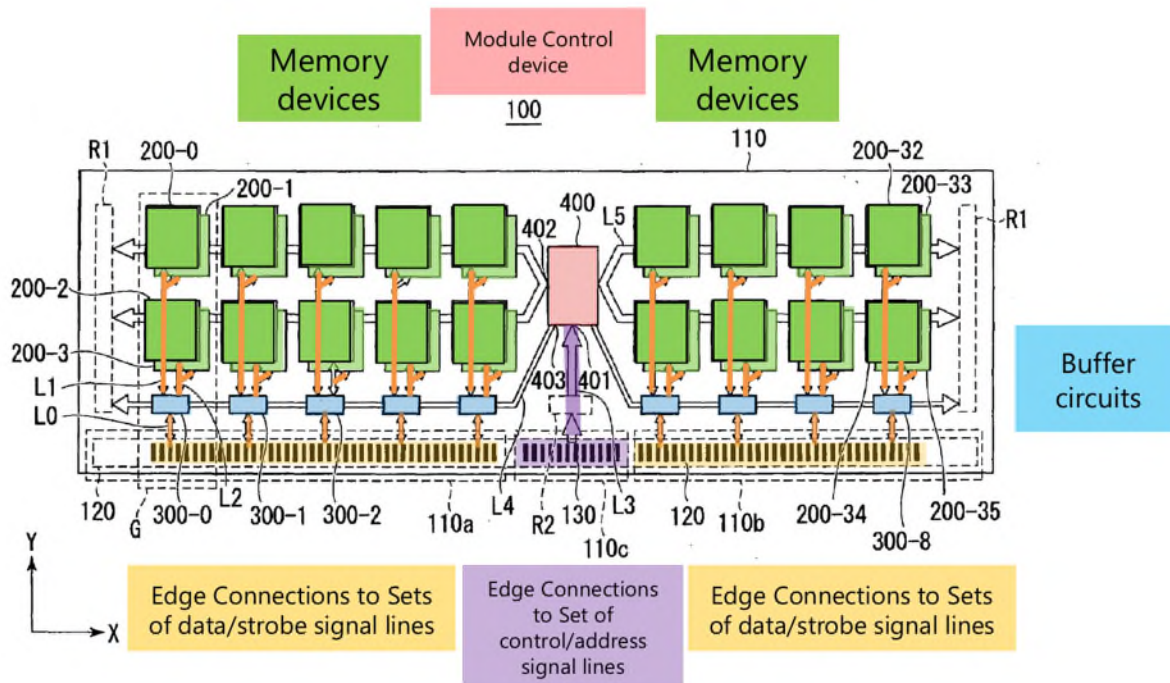


Id., Fig. 11 (annotated). Thus, a Skilled Artisan would have understood that Hiraishi discloses this limitation.

d) 1[c1]: “memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals”

114. Hiraishi discloses this limitation. For example, as illustrated by annotated figures 1 and 7 below, Hiraishi discloses “memory devices [200-0 to 200-35 (green)] arranged in multiple ranks [e.g., 200-0, 200-1, 200-2, and 200-3 in four different ranks] on the module board and coupled to the module control

device via module C/A signal lines [module command/address/control line L5] that conduct the registered C/A signals [such as ADD/CMD-Post on L5 (Fig. 7)].”



EX1005 (Hiraishi), Fig. 1 (annotated, “memory chips” in green);

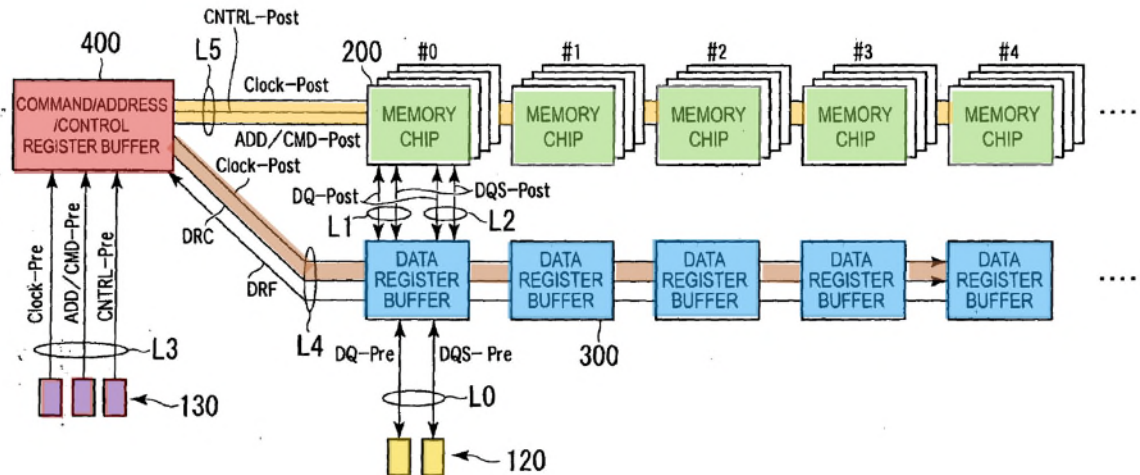


FIG. 7

Id., Fig. 7 (annotated, “memory chips” in green).³

115. Hiraishi discloses that memory module 100 includes a plurality of memory chips 200 mounted on the module substrate 110:

³ In Fig. 1 and Fig. 7 of Hiraishi, the groups of memory devices and the corresponding data buffers are numbered differently in relation to the module controller. In Fig. 1, the group numbers start at the left side (as group “0”) of the module, the farthest away from the module controller in the center. In Fig. 7, the group numbers start to the right of the module controller with group #0 closest to the module controller.

As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, ***a plurality of memory chips 200 mounted on the module substrate 110***, a plurality of data register buffers 300, and a command/address/control register buffer 400.

Id., [0045]. Hiraishi also expressly discloses a “four-Rank configuration” with four memory devices in a group, and each memory device in the group part of a different rank.

The memory module 100 according to the present embodiment has a so-called 4-Rank configuration. The number of Ranks indicates the number of memory spaces that can be selected in an exclusive manner.

Id., ¶[0051]; *see also id.* ¶[0050],[0052].

116. Hiraishi further discloses that command/address/control register buffer 400 transfers command/address signals (e.g., “ADD/CMD-Post”) via line L5 to the memory chips 200. *Id.*, ¶[0107], Fig.7 (annotated above). A Skilled Artisan would understand that these are registered C/A signals.

e) 1[c2]: “ wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and”

117. Hiraishi discloses this limitation. For example, as illustrated by annotated figures 1 and 7 above, Hiraishi discloses “*wherein the registered C/A signals [on module command/address/control line L5 (Fig. 7)] cause a selected rank of the multiple ranks [e.g., 4-Rank configuration (Id., ¶[0051])] to perform the memory read operation by outputting read data and read strobes associated with the memory read operation [e.g., using input/output circuits 213 and 214 (Id., ¶¶ [0079-80] and Fig. 4)], and wherein a first memory device [memory device 200-0] in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe [on DQ/DQS-Post lines L1 (Fig. 7)].*”

118. Hiraishi further discloses that the memory chips 200 are configured to perform memory operations in response to the registered C/A signals. For example, Hiraishi discloses:

An operation of the memory chip 200 is ***controlled based on the command signal, the address signal, the control signal, and the clock signal*** supplied from the command/address/control register buffer 400.

Id., [0054]. The memory operation can be a read operation or a write operation.

See, e.g., id., [0120]-[0129]. In this regard, Hiraishi discloses:

The command/address/control register buffer 400 registers the received commands ACT and Read with an input clock signal in the register circuit 410 shown in FIG. 6, and ***then outputs them to the memory chip 200***. ... The memory chip 200 ***receives the commands ACT and Read, and starts an actual read operation***.

Id., [0126]-[0127]. Thus, a Skilled Artisan would have understood that each rank of memory chips 200 are configured to perform a read operation in response to registered C/A signals from command/address/control register buffer 400. *See also* EX1005 at [0079], [0080], and Fig. 4 (showing that a memory device outputs data from 213, and the strobe from 214, for a read command); *id.* at [0163] and [0170] (disclosing that the memory chips can be DDR3 memory chips), and EX1020 (JESD79-3C, JEDEC standard for DDR3 SDRAM) at 33, 56-67 (describing read operations).

119. Hiraishi discloses that the memory devices include a plurality of sets of memory devices (*e.g.*, a set including memory devices 200-0 to 200-3 called a group) corresponding to respective sets of the plurality of sets of data/strobe signal lines (*e.g.*, L0). For example, Hiraishi discloses:

As shown in FIG. 1, the ***four memory chips 200 constituting a single group*** are connected to one of the data register buffers 300.

For example, the ***group of the memory chips 200-0 to 200-3 is***

connected to the data register buffer 300-0. Among the memory chips 200-0 to 200-3, the memory chips 200-0 and 200-1 that are ***mounted on the upper side of the module substrate 110*** are connected to the data register buffer 300-0 ***via a data line L1***, and the memory chips 200-2 and 200-3 that are ***mounted on the lower side of the module substrate 110*** are connected to the data register buffer 300-0 ***via a data line L2***. An arrow of each of the data lines L1 and L2 shown in FIG. 1 indicates a line of 1 byte (8 bits). Both the data lines L1 and L2 are formed inside the module substrate 110.

EX1005, [0053]; *see also id.*, [0056] (describing group G in FIG. 1). That is, Hiraishi discloses that one set of memory devices (200-0 to 200-3) are connected to data register buffer 300-0. In particular, memory devices 200-0 and 200-1 are connected to the buffer 300-0 by data line L1, and memory devices 200-2 and 200-3 are connected to the buffer 300-0 by data line L2. The read data and corresponding strobe signals output by a selected one of the group of memory devices (200-0 through 200-3) include “*a first section of the read data and at least a first read strobe*” of the selected rank, and correspond to the read data and corresponding strobe signals of the respective section of data bus L0. Indeed, Hiraishi explains that data buffer 300-0 is associated with a respective section of data bus L0, which comprises a set of data/strobe signal lines:

As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the

memory chips 200. The ***data connectors 120 and the data register buffer 300 are connected to each other with the data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of ***data transferred through the data line L0 is represented by data DQ-Pre***, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, ***a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre***, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

Id., [0103].

120. Hiraishi also discloses that the module command signals include chip select signals that select one of the four Ranks:

Although the same address is assigned to each of the Ranks, one of the Ranks is selected by exclusively activating a chip select (CS) signal or a clock enable (CKE) signal. In the present embodiment, four memory chips 200 constitute a single group (a single set), and the four memory chips 200 constituting the single group belong to different Ranks from each other. For example, the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other.

EX1005 (Hiraishi), [0051]-[0052]; *see also* EX1021 (Jacobs) at 319, 413; EX1018 (JEDEC 21-C) at p. 4.20.4-6 (“chip select lines”), pp. 4.20.4-10 to -16 (showing one chip select line for each rank of memory devices). Hiraishi also discloses that the chip select signals are part of the command signals:

By the chip select (CS) signal, a DRAM for which a command is to be issued is switched, and an activation of a clock system and a control of an on die termination in the DRAM are performed.

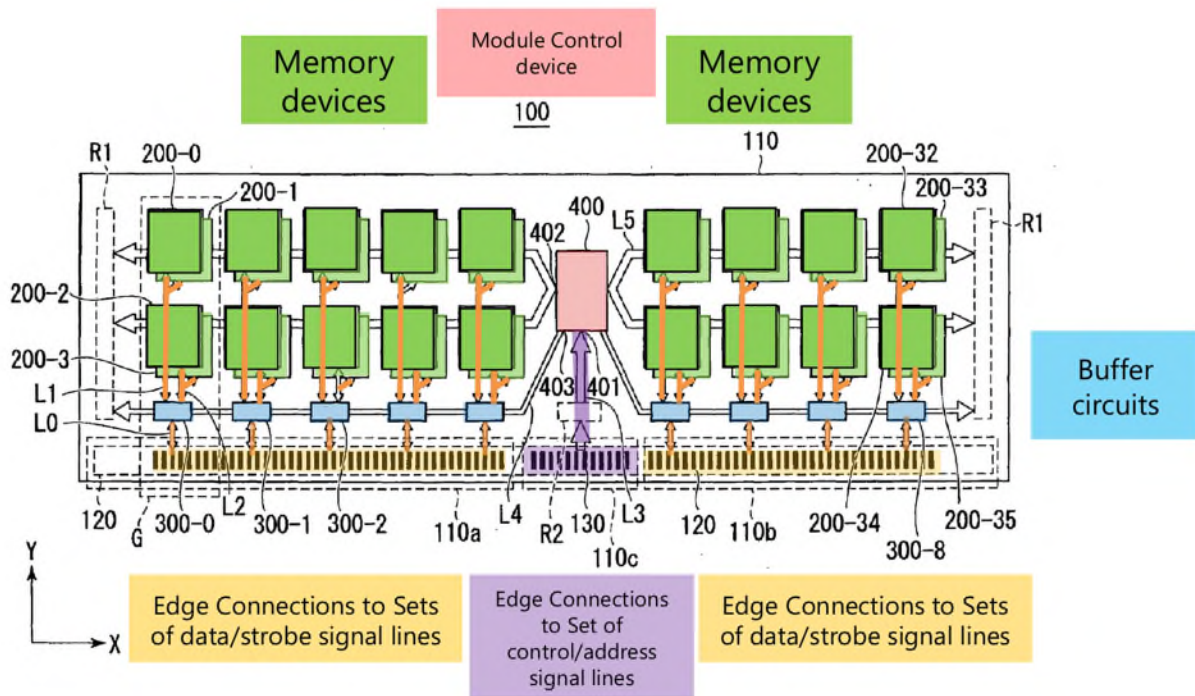
Id., [0076]. This is consistent with the understanding of a Skilled Artisan. *See, e.g.*, EX1020 (JESD79-3C) at 33 (Command Table identifying chip select signals as being part of command signals); *id.* at 13, 34 n.1 (same). Therefore, a Skilled Artisan would understand that Hiraishi teaches “...*the registered C/A signals [including the chip select signals] cause a selected rank of the multiple ranks to perform the memory read operation...*”

121. Because the multiple memory devices in a given Rank are read together, a Skilled Artisan would thus have understood that each memory device in a given Rank would output a section of the full read data. Similarly, because Hiraishi teaches each memory device in the Rank would correspond to its own set of data/strobe lines (*e.g.*, as illustrated in Fig. 1, a set for each buffer 300-0 through 300-8), a Skilled Artisan would understand that each memory device in the Rank sends its own data strobe signal DQS with the section of the read data being transmitted. Thus, from this arrangement a Skilled Artisan would understand that

the data/strobe signal sent by a first memory device 200-0 on the corresponding set of data/strobe lines (L1) would represent a first strobe and a first section of the complete data read by the entire Rank.

f) 1[d]: “data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device”

122. Hiraishi discloses this limitation. For example, as illustrated by annotated Figures 1 and 7 below, Hiraishi discloses “*data buffers [data register buffer circuits 300-0 to 300-8 (blue)] on the module board between the edge connections and the memory devices [e.g., buffer circuit 300-0 (blue) is positioned between the set of memory devices 200-0 to 200-3 (green) and the connectors 120 (yellow) connecting to the data line L0 (Fig. 1)] wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks [e.g., buffer circuit 300-0 (blue) is coupled to at least memory devices 200-0 to 200-3 (green) in four different ranks] and is configurable to receive the module control signals from the module control device [e.g., buffer circuit 300-0 (blue) receives module command/address/control line L4 (Fig. 7) from command/address/control register buffer 400 (including DRC, brown, Fig. 7)].*



EX1005 (Hiraishi), Fig. 1 (annotated and color added, showing buffer circuits in blue);

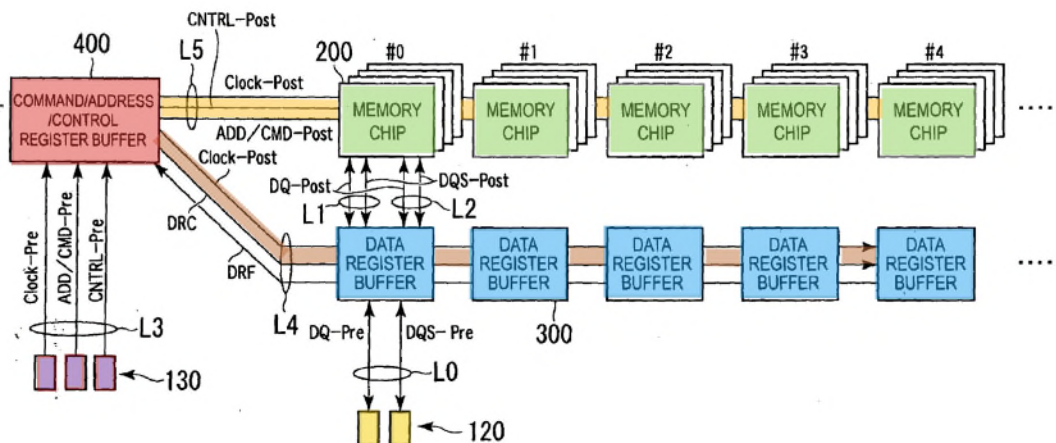


FIG. 7

Id., Fig. 7 (annotated and color added, showing buffer circuits in blue and data line L0 comprising DQ and DQS signals).

123. Hiraishi discloses that the memory module includes a plurality of data register buffers (shown in blue in the annotated figures above):

As shown in FIG. 1, the memory module 100 according to the present embodiment includes a module substrate 110, a plurality of memory chips 200 mounted on the module substrate 110, **a plurality of data register buffers 300**, and a command/address/control register buffer 400.

Id., [0045]. Each data register buffer 300 inputs and outputs 1 byte of data (8 bits).

Id., [0085]. Hiraishi explains that each of nine buffers is allocated to four memory chips, such that each data register buffer buffers read and write data that is transferred via line L0 to data lines L1 and L2 and *vice versa*:

A single data register buffer 300 is allocated for every four memory chips 200, as described above, so that ***nine data register buffers 300 are arranged along the X direction***, which is the long side. The data register buffer 300 is a chip for buffering write data that is transferred via a data line L0 and outputting the write data to either one of the data lines L1 and L2, and at the same time, buffering read data that is transferred via either one of the data lines L1 and L2 and outputting the read data to the data line L0. The data line L0 is also formed inside the module substrate 110.

Id., [0055]. Hiraishi further explains that a single data register buffer, data connectors 120, and the four memory chips corresponding thereto constitute a group (G, shown in Figure 1), such that a relative position relationship between each of the buffers and corresponding four memory chips is constant in all groups:

[T]he *single data register buffer 300, the data connectors 120 and the four memory chips 200 corresponding to the data register buffer 300 constitute a group G*. The memory chips 200, the data register buffer 300, and the data connectors 120 included in the same group are arranged along the Y direction, which is the short side, and a plurality of groups G formed in the above manner are arranged along the X direction, which is the long side. Therefore, *a relative positional relationship between each of the data register buffers 300 and corresponding four memory chips 200 becomes constant in all the groups G*.

Id., [0056]. Hiraishi further explains that “the memory chips 200-0 to 200-3 constitute a single group, and the memory chips 200-0 to 200-3 belong to different Ranks from each other.” *Id.*, [0052].

124. Figure 5 of Hiraishi is a schematic block diagram of a data register buffer 300. *Id.*, [0017].

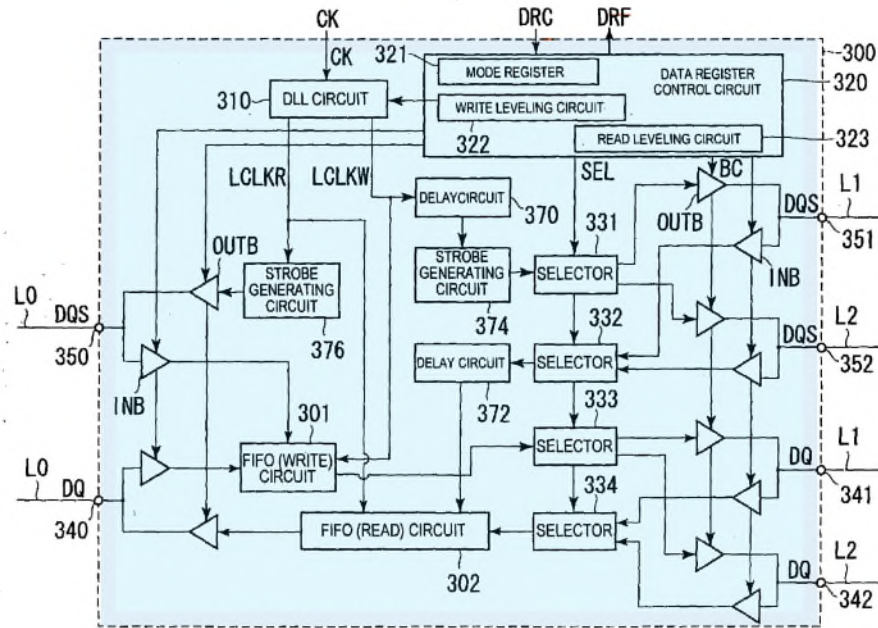


FIG.5

Id., Fig. 5. Hiraishi explains, with reference to Fig. 5, that the data register buffer 300 is positioned between respective sets of data/strobe signal lines:

As shown in FIG. 5, the data register buffer 300 includes a FIFO (Write) circuit 301 and a FIFO (Read) circuit 302. The FIFO (Write) circuit 301 **buffers data DQ that is supplied via an input/output terminal 340 with a data strobe signal DQS that is supplied via an input/output terminal 350**. The FIFO (Read) circuit 302 **buffers data DQ that is supplied via an input/output terminal 341 or 342 with a data strobe signal DQS that is supplied via an input/output terminal 351 or 352**. A strobe generating circuit 376 **generates a data strobe signal DQS to be supplied to the data connectors 120**, in synchronization with an internal clock LCLKR that is generated by a DLL circuit 310. A strobe generating circuit 374 **generates a data strobe signal DQS**

to be supplied to the memory chip 200, in synchronization with an internal clock LCLKW that is generated by the DLL circuit 310.

Id., [0084].

125. Hiraishi further discloses, with reference to Fig. 7, that the buffer circuits intervene between the data connectors 120 and the memory chips 200, such that the data connectors 120 are connected to the buffer via data line L0 (which comprises data and strobe signals DQ-pre and DQS-pre), and the buffer is connected to the memory chips via data lines L1 or L2 (which each comprise data and strobe signals DQ-post and DQS-post):

As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the ***data line L0***, and the data register buffer 300 and the memory chips 200 are connected to each other with the ***data line L1 or L2***. In FIG. 7, ***a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post***. Similarly, ***a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post***.

Id., [0103]. Accordingly, a Skilled Artisan would have understood that Hiraishi's buffer circuits are in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines coupled between the data connectors 120 and the memory chips 200.

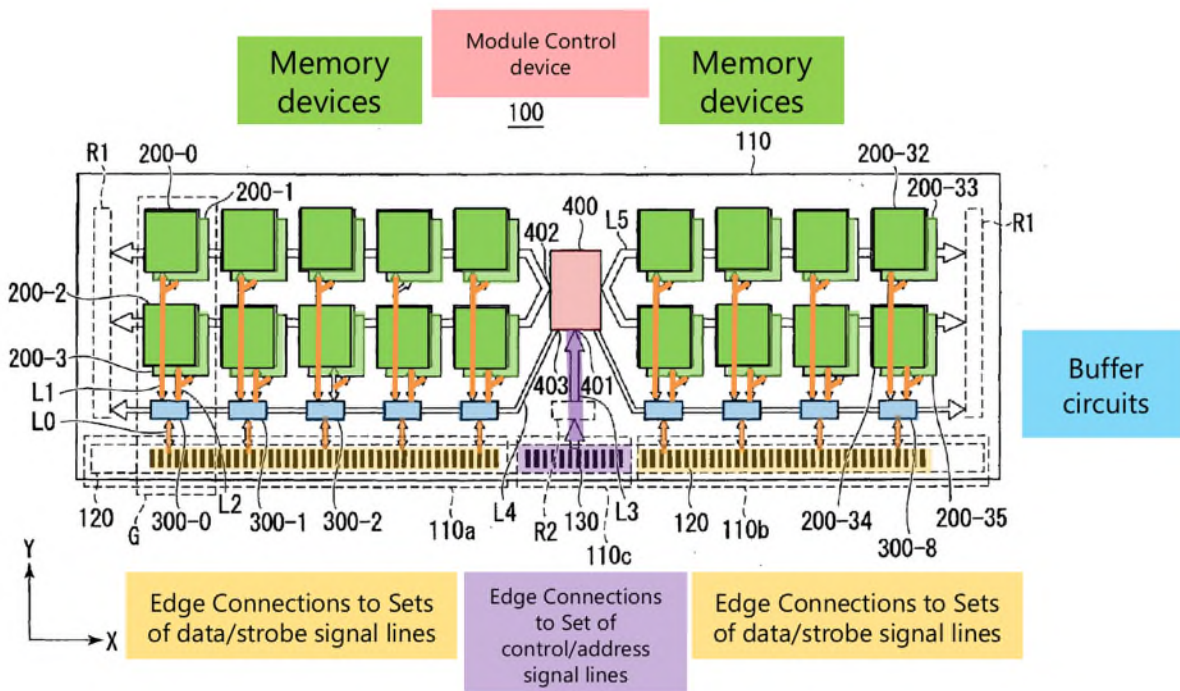
126. Hiraishi discloses that the data register buffer 300 also receives module command/address/control (line L4) from command/address/control register buffer 400. Specifically, Hiraishi explains that the control signal generating circuit 430 (which is part of the command/address/control register buffer 400), generates control signals based on the command/address/control signal supplied by input terminal 401:

The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. ***The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403.*** The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404.

Id., [0099]. Thus, a Skilled Artisan would understand that Hiraishi's data buffers receive control signals from the command/address/control register buffer 400.

g) 1[e]: “wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:”

127. Hiraishi discloses this limitation. For example, as illustrated by annotated Figures 1 and 7 below, Hiraishi discloses that “a first data buffer of the data buffer buffers is coupled to the first memory device [data register buffer circuits 300-0, blue, is coupled to memory device 200-0, green], and is configurable to, in response to one or more of the module control signals [signals on line L4 from command/address/control register buffer 400 (including DRC, brown, Fig. 7)].”



EX1005 (Hiraishi), Fig. 1 (annotated and color added, showing buffer circuits in blue and memory devices in green).

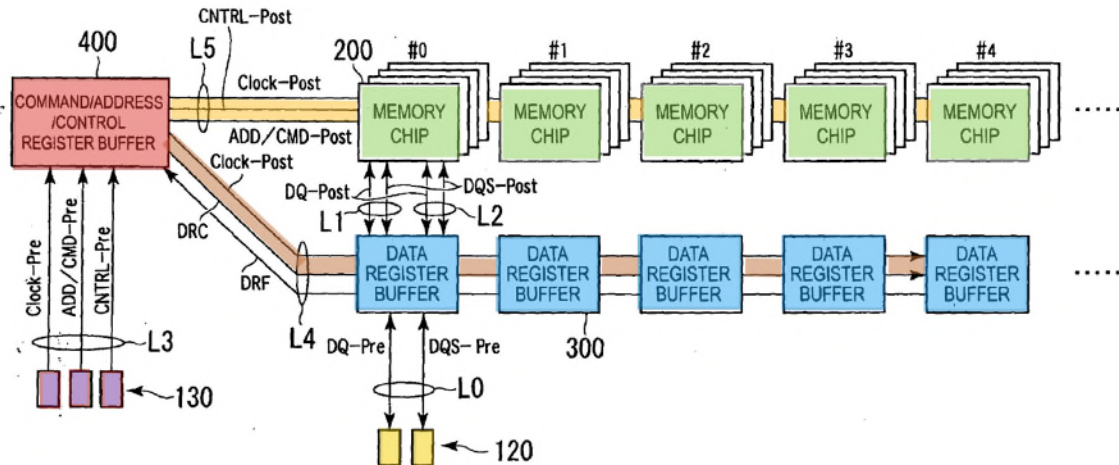


FIG. 7

Id., Fig. 7 (annotated and color added, showing buffer circuits in blue, memory devices in green, and data lines L0, L1, and L2 comprising DQ and DQS signals).

128. For example, as explained above in connection with limitation 1[d], Hiraishi discloses that each buffer circuit is mounted on the module board and coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and is configured to receive control signals from command/address/control register buffer 400. *See supra* ¶¶ 122-126 (limitation 1[d]); EX1005 (Hiraishi), [0045], [0055]-[0056], [0084], [0099], [0103].

h) 1[f]: “delay the first read strobe by a first predetermined amount to generate a first delayed read strobe;”

129. Hiraishi discloses this limitation. For example, as illustrated by annotated Figure 5 of Hiraishi below, Hiraishi discloses that data register buffers (300), including delay circuit 372, can “delay the first read strobe [orange dashed line, e.g., on 351] by a first predetermined amount [e.g., “about 90 degrees” (EX1005, [0091])] to generate a first delayed read strobe [e.g., the DQS signal supplied to FIFO (Read) circuit 302].”

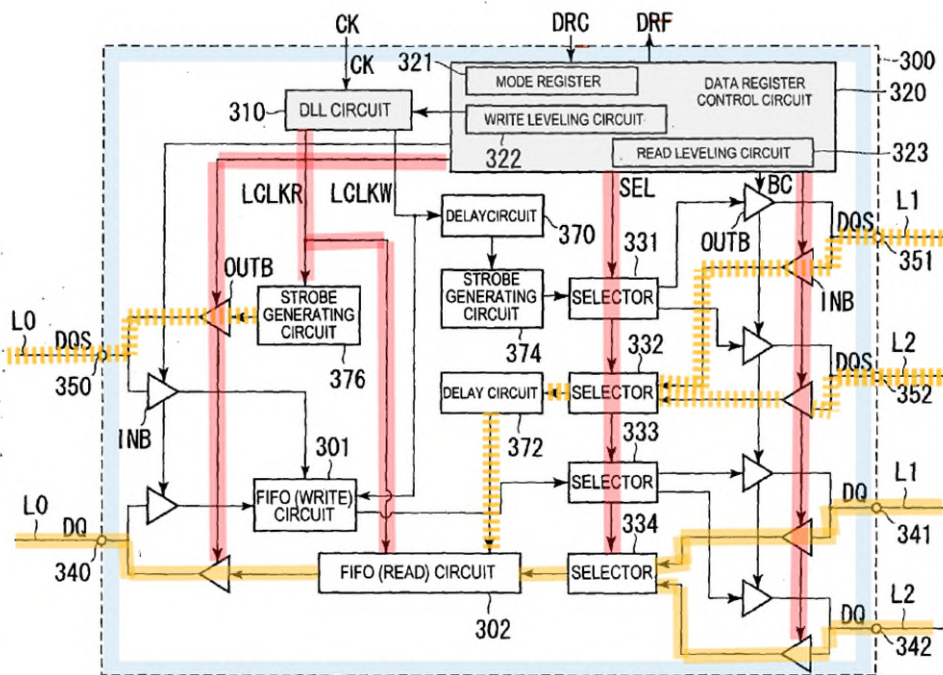


FIG.5

EX1005 (Hiraishi), Fig. 5 (annotated).

130. Hiraishi describes the operations of components of data register buffer 300 receiving the data signal DQ and data strobe signal DQS for a read operation as follows:

The selector 334 is a circuit that selects data DQ input from either one of the input/output terminals 341 and 342 and supplies the selected data DQ to the FIFO (Read) circuit 302. The selectors 331 and 332 perform the similar functions as those of the selectors 333 and 334, respectively. Specifically, the selector 332 selects a data strobe signal DQS input from either one of the input/output terminals 351 and 352.

A phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal.

Id., [0091]. As such, under Netlist's interpretation of the claim, *supra* ¶¶99-100, a Skilled Artisan would thus understand that the delay circuit 372 in Hiraishi's data register buffer 300 “*delay[s] the first read strobe by a first predetermined amount to generate a first delayed read strobe*” that is provided to FIFO (Read) circuit 302.

i) 1[g]: “sample the first section of the read data using the first delayed read strobe; and”

131. Hiraishi discloses or renders obvious this limitation. For example, a Skilled Artisan would understand that FIFO (Read) circuit 302 in data register

buffer 300 would “sample the first section of the read data [DQ, orange line, e.g., on 341] using the first delayed read strobe [DQS, orange dashed line, from delay circuit 372].”

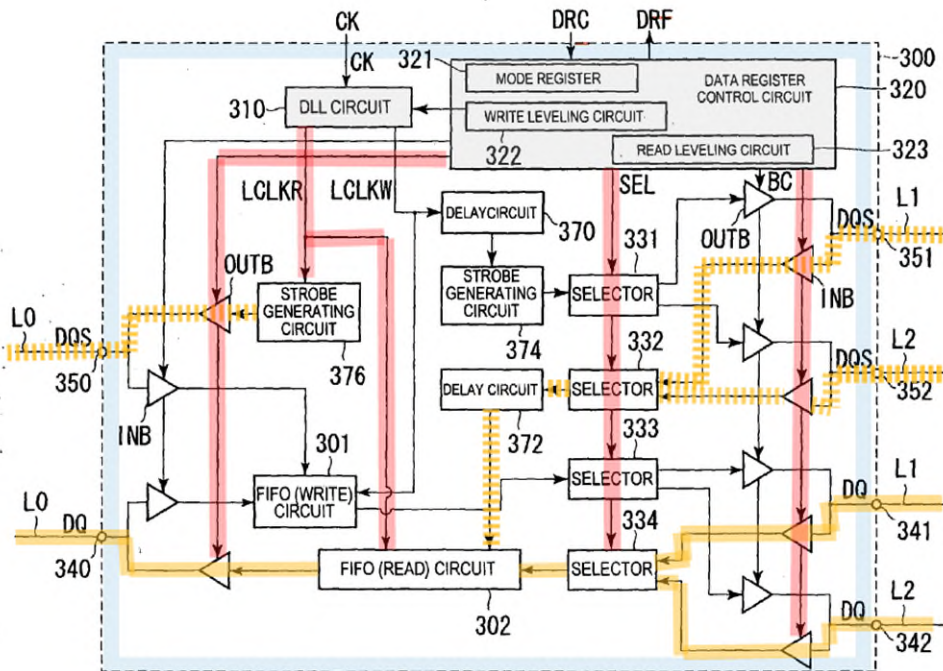


FIG. 5

EX1005 (Hiraishi), FIG. 5 (annotated). A Skilled Artisan would have understood that FIFO (Read) circuit 302 would sample the data signal DQ in accordance with the delayed strobe signal, DQS, similar to the sampling disclosed in the '506 Patent. See, e.g., EX1001 at 13:27-29 (disclosing that “a sampler or register circuit ... samples the ... signal ... according to the clock signal”); *id.*, 17:15-18 (“The selected read strobe signal is delayed in a delay circuit 1560 by an amount controlled by the delay signal DS, and sampled by a sampler circuit 1570 according to the buffered module clock signal CK0.”).

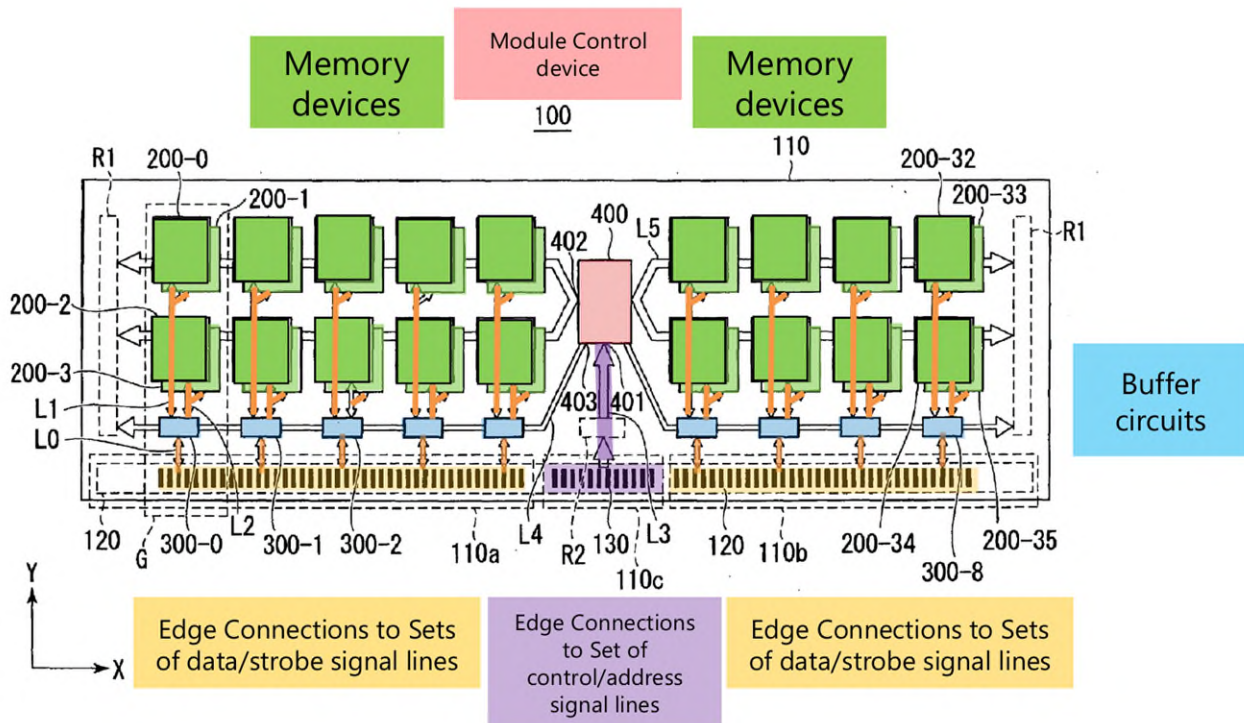
132. As explained above, Hiraishi discloses in connection with a read operation that “[a] phase of the selected data strobe signal DQS is delayed by about 90 degrees by a delay circuit 372, and ***then the data strobe signal DQS is supplied to the FIFO (Read) circuit 302 as an input trigger signal.***” EX1005 (Hiraishi), [0091]. A Skilled Artisan would therefore have understood that FIFO (Read) circuit 302 samples the DQ signal based at least in part on the delayed DQS signal received from delay circuit 372. In particular, a Skilled Artisan would have understood that, when the data signal is latched in the FIFO, it necessarily is sampled (registered). Further, because the delayed DQS signal acts “as an input trigger signal” to latch the data in the FIFO (Read) circuit 302, a Skilled Artisan would understand the data signal is necessarily sampled in accordance with the delayed strobe signal received from delay circuit 372. Thus, a Skilled Artisan would have understood that Hiraishi’s FIFO (Read) circuit 302 “*sample[s] the first section of the read data [DQ] using the first delayed read strobe.*”

133. To the extent one might argue that Hiraishi does not “sample” the first section of the read data using the first delayed read strobe, this claim is rendered obvious by Hiraishi in further view of Butt. For example, Butt discloses a method for calibrating a delayed read strobe DQS “to approximately center the read data strobe signal DQS in the valid data eye window.” EX1029, [0035]. Butt further states that “data is ***sampled*** using the delayed read data strobe signals DQS.” *Id.*,

[0018] (emphasis added). Indeed, the operation that Butt describes as “sampling” is equivalent to the use of the DQS signal in Hiraishi to trigger the FIFO (Read) circuit 302. See EX1029, [0019] (“The read data DR_PDQ_OUT and DR_NDQ_OUT are generally written to the FIFOs 112 in response to (e.g., clocked by) the signals PDQS_OUT and NDQS_OUT, respectively.”). Accordingly, it would have been obvious to a Skilled Artisan at the time of the ’506 Patent to configure the data register buffer 300 in Hiraishi to “sample” the read data using the delayed read strobe signal as disclosed in Butt. Additional motivations to combine Hiraishi and Butt are described in connection with claim 1[i]. *Infra* ¶¶ 144-151.

j) 1[h]: “transmit the first section of the read data to a first section of the data bus;”

134. Hiraishi discloses this limitation. For example, as illustrated by annotated Figures 1, 5, and 13 of Hiraishi below, Hiraishi discloses that the first data register buffer (300-0) can, “transmit the first section of the read data [e.g., DQ on L0 via 340 (Fig. 5)] to a first section of the data bus [e.g., from buffer circuit 300-0 (blue) to the connectors 120 (yellow) connecting to the data line L0 (Fig. 1)].”



EX1005 (Hiraishi), Fig. 1 (annotated)

135. As discussed above with reference to claim element [1c2], each data buffer (blue) receives “the first section of the read data” (and the corresponding strobe) from one of the coupled memory devices and, in turn, transmits that first section (and the corresponding strobe) on the respective section of data bus L0. *Supra* at ¶¶117-121. As further illustrated by the annotated version of Fig. 5 of Hiraishi, below, the data paths for read operations include a first data path for transmitting read data, such as the data path coupled to the line L1 at the input terminal 341 and the line L0 at the output terminal 340 for transmitting data signals (DQ, orange line).

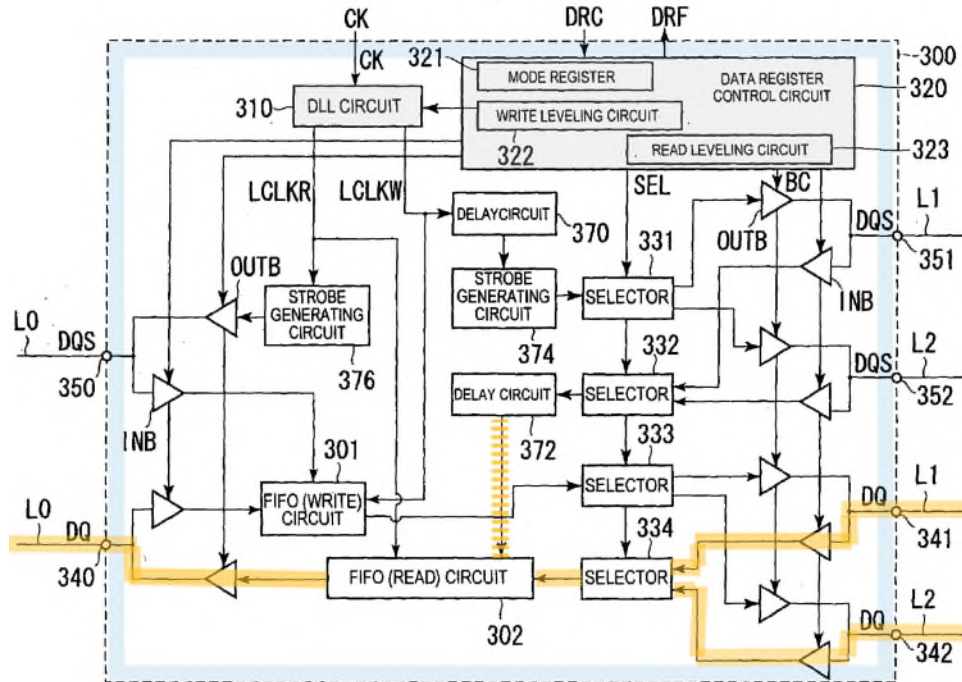


FIG. 5

EX1005 (Hiraishi), FIG. 5 (annotated). As also shown in FIG. 5 of Hiraishi, data paths for read operations include routing data from either one (L1, 341) or the other (L2, 342) branch to the same output (terminal 340, coupled to line L0) during read operations.

k) 1[i]: “wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.”

136. Hiraishi discloses this limitation (under Netlist’s apparent interpretation). For example, as illustrated by annotated Figures 5 and 13 of Hiraishi below, “the first predetermined amount [e.g., applied by delay circuit 372] is determined based at least on signals [e.g., dummy data or strobe signals] received

by the first data buffer during one or more previous operations [e.g., the S4 read leveling operation].”

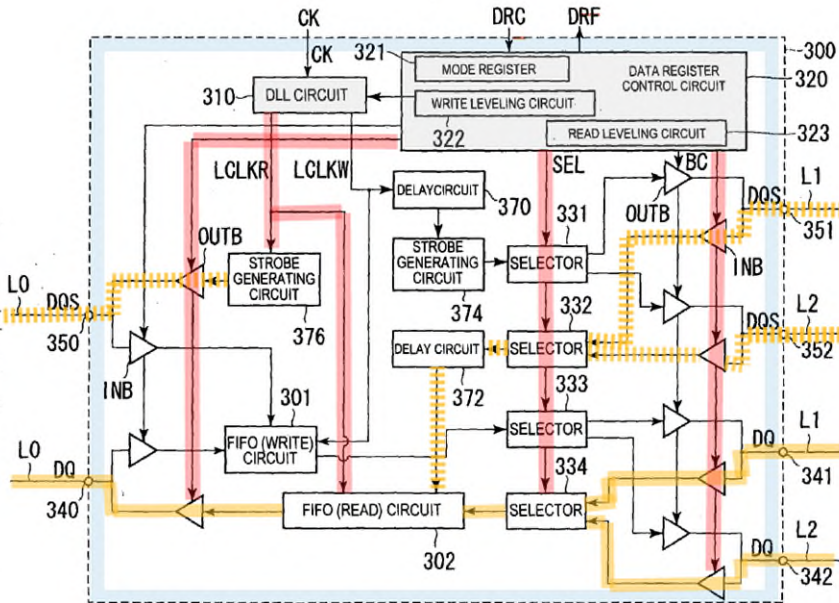


FIG. 5

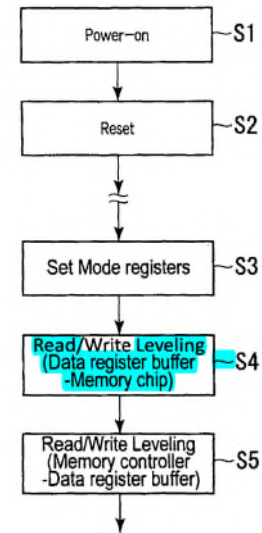


FIG. 13

EX1005 (Hiraishi), Figs. 5 and 13 (annotated).

137. Hiraishi expressly states that delay circuit 372 delays the DQS “by about 90 degrees.” *Id.*, [0091]. A Skilled Artisan would have understood from the disclosure of Hiraishi that the “about” qualifier here refers to fine timing adjustments to the DQS signals calculated, e.g., by read leveling circuit 323, through a read leveling operation, *e.g.*, step S4 in Fig. 13 above.

138. For example, a Skilled Artisan would have understood from the JEDEC standards that the read data strobe signal is edge aligned with the read data. EX1020 (JESD79-3C) at pp.56-65. A Skilled Artisan would have also understood that, to capture the data values reliably and optimally, the strobe signal needs to be

delayed so that the data is sampled in the middle of the “data eye.” *See, e.g.*, EX1030 (Zumkehr) at Abstract (“A method for optimizing a source synchronous clock reference signal timing to capture data from a memory device (e.g., DDR SDRAM) includes conducting an iterative two-dimensional data eye search for optimizing the delay of the source synchronous clock reference signal (e.g., DQS).”) and Fig. 2B (reproduced below).

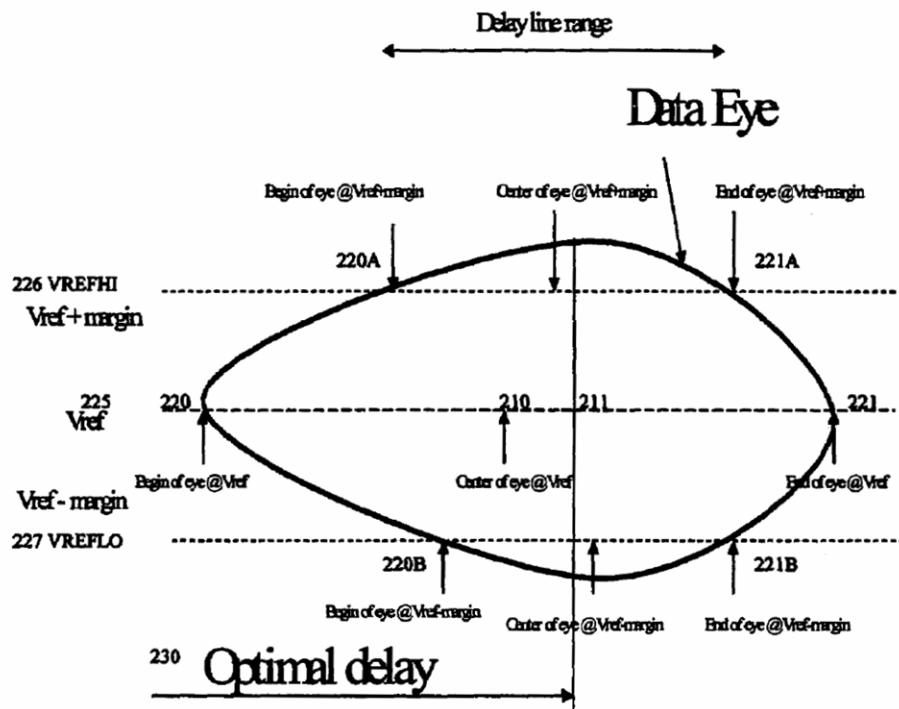


FIG. 2B: Data Eye for DDR

As illustrated here, the optimal delay is “about 90 degrees,” but its exact location depends on the shape of the data eye. *Id.* A Skilled Artisan would have also understood that the shape of the data eye can be found by adjusting the delay, for example, by: applying less and less delay until the captured data becomes

erroneous, thus finding the minimum delay; applying more and more delay until the captured data becomes erroneous, thus finding the maximum delay; and determining an optimum delay between the minimum and maximum delays. *See, e.g.,* EX1029 (Butt) at Figs. 4 and 5 (reproduced below).

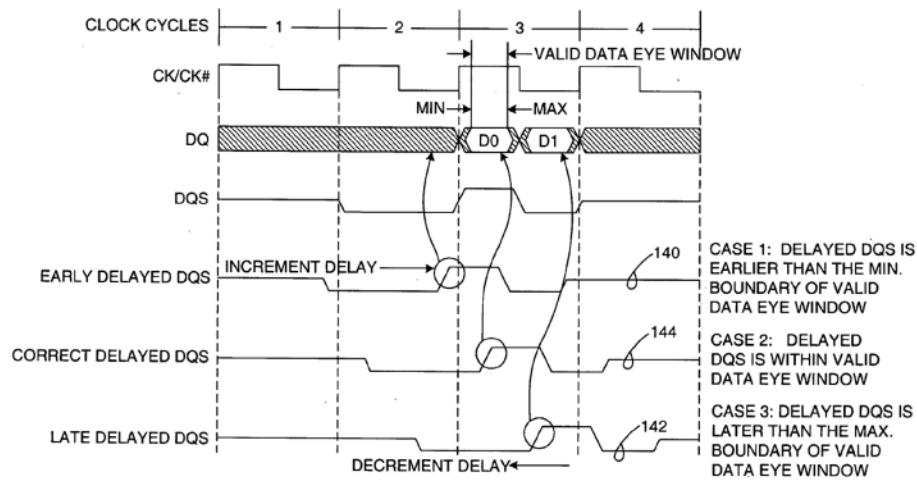


FIG. 4

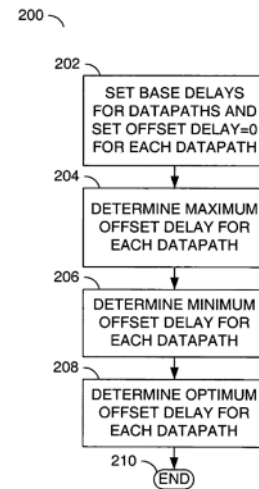


FIG. 5

A Skilled Artisan would have further understood that whether the captured data is erroneous or not can be determined using a known data pattern. *Id.* at [0044]. In fact, providing such a known data pattern for the very purpose of read data synchronization has been already standardized at the time. EX1020 (JESD-79-3C) at p.31 (describing a “Multi Purpose Register (MPR) function [which] is used to Read out a predefined system timing calibration bit sequence,” including a “Predefined pattern” that is “used for read synchronization,” *see id.* p.31 Note 2), *see also id.* at pp.48-54 (same, described in detail); *see also* EX1005 (Hiraishi) at [0150], [0160] (describing the use of predefined data during read leveling);

EX1006 (Tokuhiro) at Figs. 5 and 6 (showing adjustable delay elements on the DQS strobe lines for latching the DQ values in flip-flops FF5 and FF7). Since a Skilled Artisan would have been familiar with the JEDEC standards, *see supra* at ¶137, she would have understood this function of using the MPR for read leveling.

139. Hiraishi also discloses that the S4 read leveling operation is controlled by read leveling circuit 323 “to adjust ... a read timing in consideration of a propagation time of a signal.” *Id.*, [0090], [0140]. Because the data and strobe signals are buffered by the data register buffer 300, the timing is off between the DQ-pre/DQS-pre and DQ-post/DQS-post (where DQ-pre and DQS-pre are the data/strobe signals between memory controller and buffer, and DQ-post and DQS-post are the data/strobe signals between the buffer and the memory device):

Although the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post.

Id., [0104]. Accordingly, Hiraishi discloses that it is necessary to separately perform a timing adjustment between the memory chips 200 and the data register buffer 300 (step S-4 in Fig. 13) and between the data register buffer 300 and the memory controller (step S-5 in Fig. 13):

Therefore, in the present embodiment, it is ***required to perform a timing adjustment*** between the memory chips 200 and the data register buffer 300 and a timing adjustment between the data register buffer 300 and the memory controller in a separate manner. Details on the timing adjustments will be described later.

Id.

140. Step S-4 in Figure 13 of Hiraishi includes both read and write leveling between the data register buffer and the memory chips 200. *See id.*, [0090] (“Furthermore, the data register control circuit 320 includes a write leveling circuit 322 and a read leveling circuit 323. The write leveling circuit 322 is a circuit for ***performing a write leveling operation***, and the read leveling circuit 323 is a circuit for ***performing a read leveling operation***. Details on the write leveling operation and the read leveling operation will be described later.”); [0140] (“Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The ***leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal***. The ***adjustment of the write timing is performed by a write leveling operation***, and the ***adjustment of the read timing is performed by a read leveling operation***”).

141. A Skilled Artisan would have also understood at the time that during read leveling, a predetermined data pattern (also called “dummy data” in Hiraishi)

is transmitted from the memory, so the Read Leveling circuit can compare the received (latched) data with that predetermined data pattern to identify any mismatches and adjust the phases and timing to achieve a better match. *See id.*, [0150] (“The read data DQ at the time of the read leveling is, for example, a signal in which a High level and a Low level are repeated in an alternate manner.”); *see also id.* [0160] (describing the role of “dummy data” for the read leveling operation between the data register buffer and the system memory controller), and FIGS. 5, 13. Indeed, Hiraishi expressly teaches the importance of the function of DLL circuits (phase matching) for DDR3 DRAM devices. *Id.*, [0163] (“In a recent high speed memory such as a DDR3 DRAM, a use of the DLL circuit is substantially essential.”). A Skilled Artisan would have also understood at the time that DDR3 memories follow the JESD79-3 standard which describes that, during the read leveling operation, the DDR3 memories output a pre-defined data pattern from a Multi-Purpose Register, and this data pattern can be used to verify whether the read data has been properly captured. *Id.*, [0148]-[0150]; EX1020 (JESD79-3C) at Section 3.4.5 (p. 31, *2, “The predefined pattern will be used for read synchronization”), and Section 4.10 (p. 48, “The Multi Purpose Register (MPR) function is used to Read out a predefined system timing calibration bit sequence.”), Fig. 21 (p. 51, “Memory controller repeats these calibration reads until read data capture at memory controller is optimized.”). Thus, a Skilled Artisan would have

understood that Hiraishi's read leveling can also use the standard read leveling techniques of the time.

142. Figure 15 in Hiraishi (below) is a timing diagram for the read leveling in Hiraishi. EX1005, [0028].

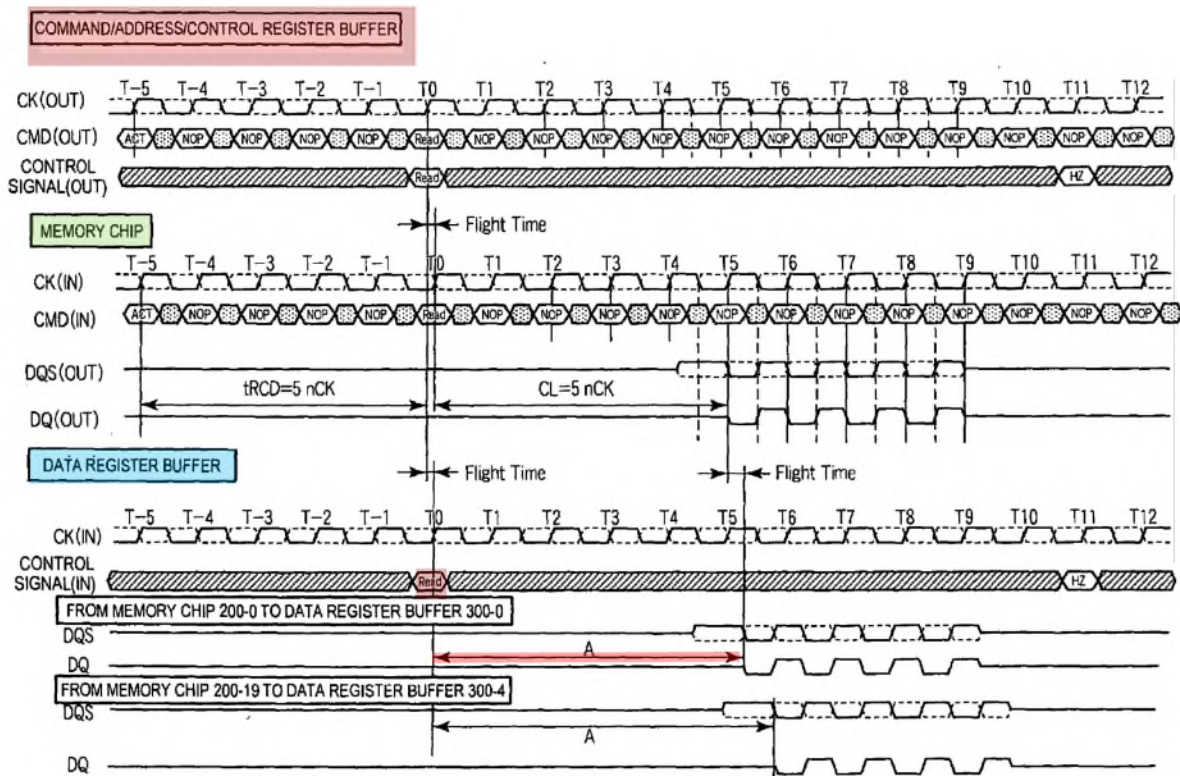


FIG.15

Id., Fig. 15. As shown in Figure 15, during read leveling, “[t]he memory chip 200 receives the read command Read and performs an actual read operation.” *Id.*, [0150]. Because memory chip 200 is performing an actual read operation, a Skilled Artisan would understand that the data register buffer 300 would receive a DQS signal from the memory device 200 as part of the read leveling—as shown in

Figure 15 (e.g., “FROM MEMORY CHIP 200-0 TO DATA REGISTER BUFFER 300-0” at the bottom).

143. For all the reasons explained above, a Skilled Artisan would therefore have understood from this disclosure of Hiraishi and her knowledge of common read leveling techniques that the amount of delay applied to the data strobe signal DQS by delay circuit 372 would be based at least on signals received by the data buffer 300 during S4 read leveling (e.g., the DQS from memory device 200, and the “dummy data” used in S4 read leveling), thus satisfying Netlist’s interpretation of the claim, *supra* ¶¶99-100.

144. To the extent one might argue that Hiraishi does not sufficiently disclose determining the amount of delay based at least on signals received during S4 read leveling, this claim is rendered obvious by Hiraishi in further view of Butt (EX1029). For example, Butt discloses “*wherein the first predetermined amount [e.g., the delay applied by datapaths 114 to the data strobe signal DQS] is determined based at least on signals [e.g., data strobes during read training] received by the first data buffer during one or more previous operations [e.g., read training process 200].*”

145. Figure 2 in Butt, below, depicts a circuit 104 between a memory controller (left) and a DDR memory (right, green):

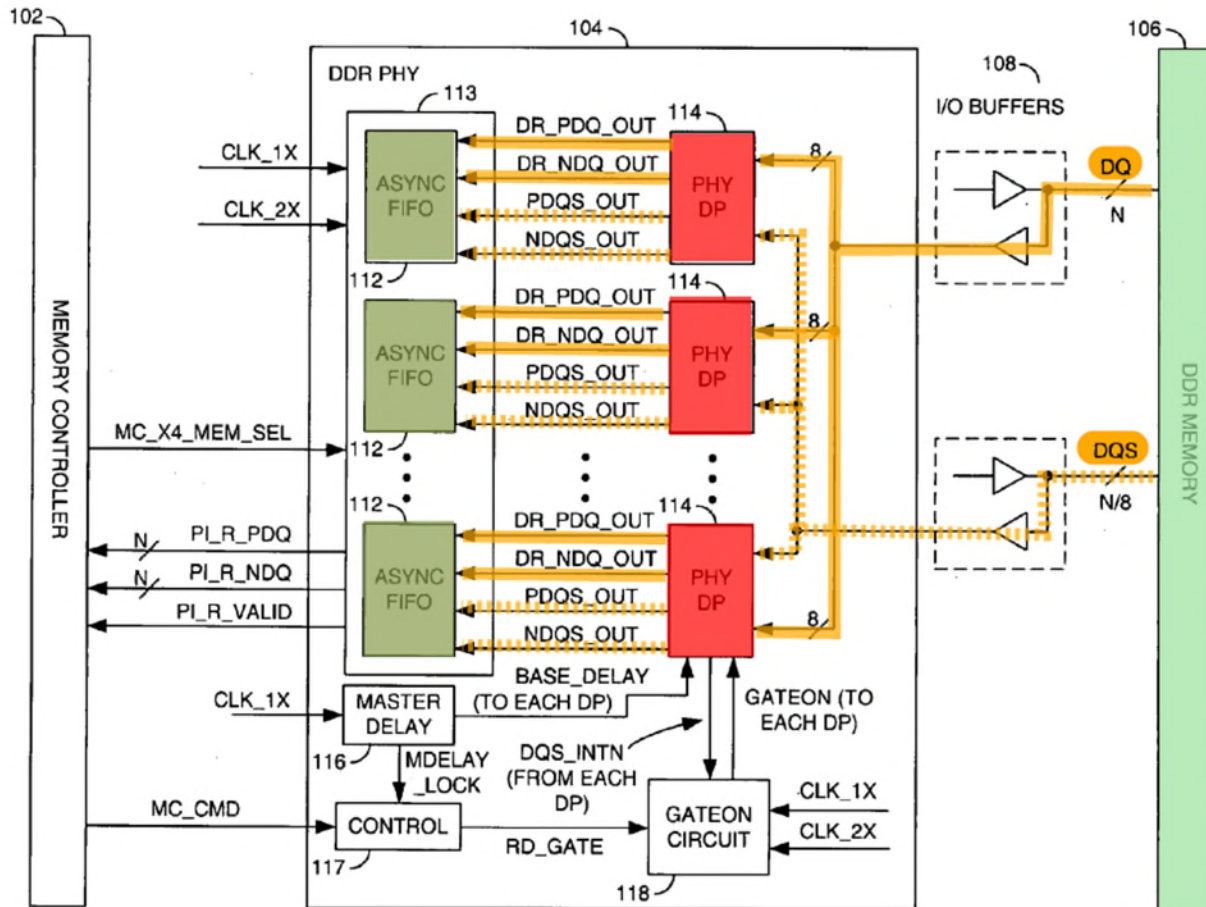


FIG. 2

EX1029, Fig. 2. Circuit 104 includes physical datapaths 114 (red) that receive DQ (orange) and DQS (orange dashed) from the DDR memory, and these datapaths 114 pass the signals to asynchronous first in, first out buffers 112 (olive). *Id.*, [0017]. Moreover, Butt discloses that datapaths 114 can delay the read strobe signal DQS that is used to read the data signal DQ. *Id.*, [0018].

146. Butt further discloses a specific structure for the datapaths 114, explaining that the DQS signals (dashed orange lines) are delayed by a predetermined amount (“Stored Slave Delay Adjustment,” red) to be optimally

positioned relative to the data DQ (solid orange lines). EX1029 at [0033] (“The circuits 124a, 124b, 128a and 128b within the datapath (DP) hardmacro are generally configured to shift the DQS strobe to be optimally positioned relative to DQ (valid read data).”) and Fig. 3A (reproduced below, annotated).

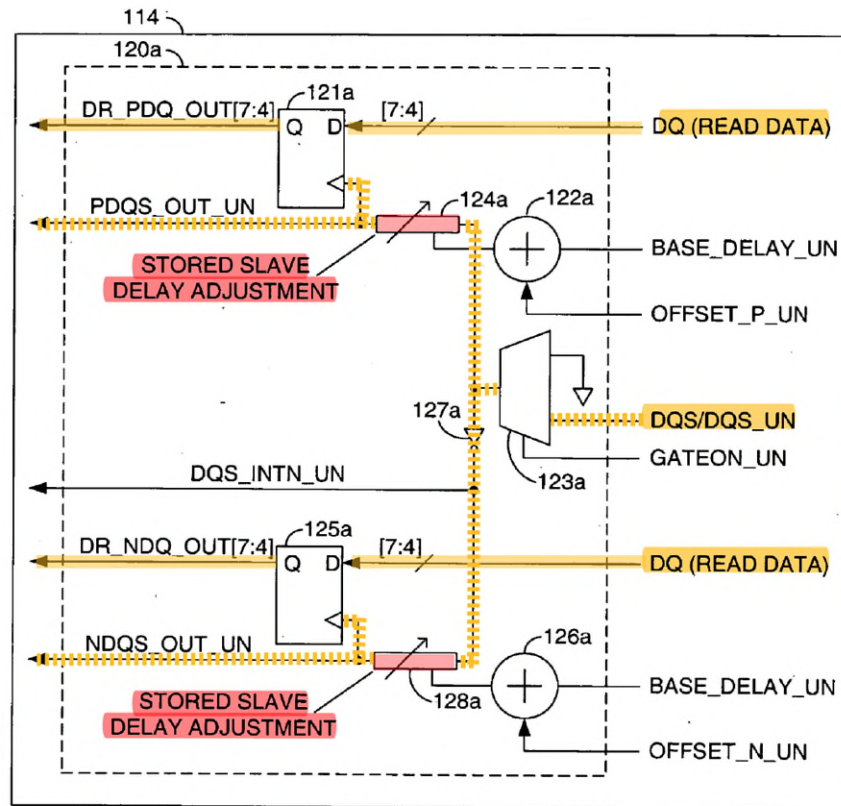


FIG. 3A

147. Butt describes a method of “read training” that can “establish optimum DQS strobe settings.” EX1029, [0033] The invention described in Butt “provides for adjusting a delay of the read data strobe signal DQS to approximately center the read data strobe signal DQS in the valid data eye window.” *Id.*, [0035].

Figure 5, below, illustrates the overall process, with more details for specific steps shown in Figures 6 and 7:

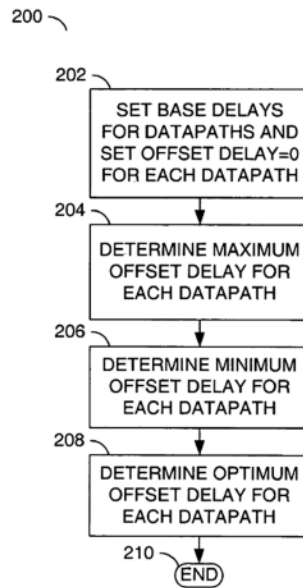


FIG. 5

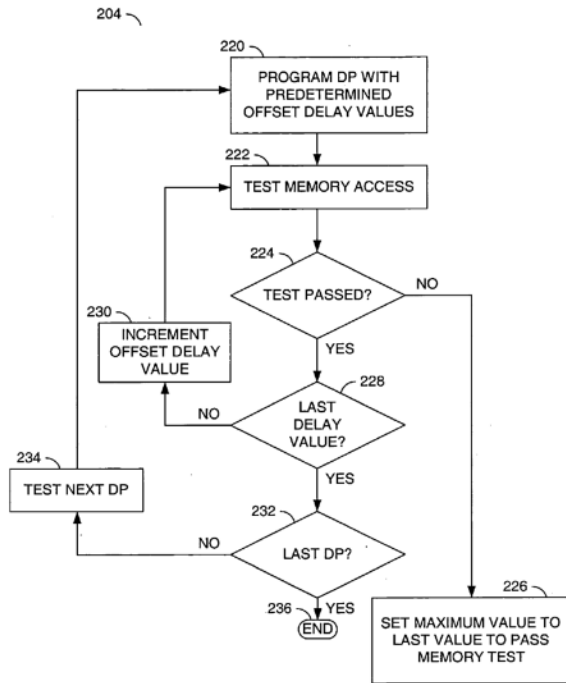


FIG. 6

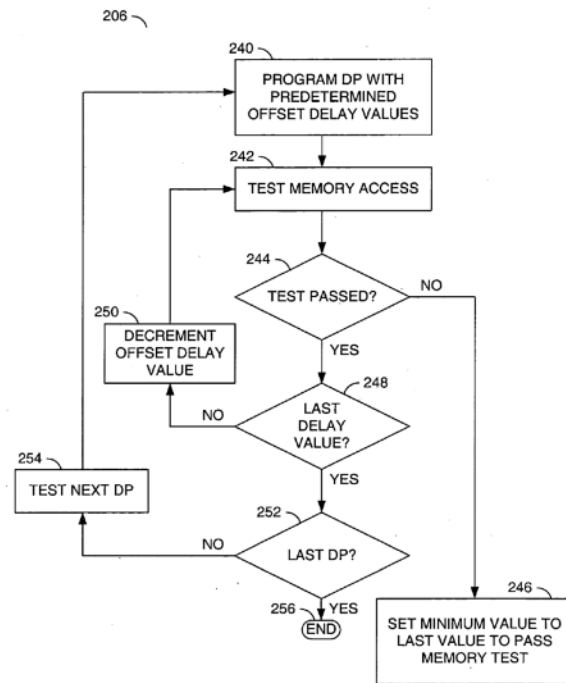


FIG. 7

Id., Figs. 5-7. Butt explains that each datapath iteratively tests different offsets from a base delay to determine a minimum and maximum acceptable offset. *Id.*, [0037], [0045]. As indicated in Figures 6 and 7 above, the process for determining the minimum and maximum will involve repeatedly testing for valid memory access at different offset values. *Id.*, [0048]-[0061].

148. A Skilled Artisan would understand from Butt that in order to test each offset, the datapath 114 would receive predefined read data (DQ) and corresponding data strobe (DQS) signals and apply the offset to be tested to the data strobe signal. In particular, Butt discloses test memory access operations (222, 224, 242, 244) with different delays of the data strobe (DQS) to find the boundary

of the data eye where the memory access fails to recover the predefined read data. EX1029 at Figs 6 and 7 (reproduced above), [0054] (“The process 204 may perform a test access on the memory 106 (e.g., blocks 222 and 224). When the memory test access fails, the process 204 may set the maximum offset delay value for the corresponding datapath 114 to the last value that passed the test (e.g., block 226).”) and [0061] (“The process 206 may perform a test access on the memory 106 (e.g., blocks 242 and 244). When the memory test access fails, the process 206 may set the minimum offset delay value for the corresponding datapath 114 to the last value that passed the test (e.g., block 246).”). These minimum and maximum offsets are then used to determine an optimum offset for the datapath, which is programmed into the datapath for use during later read operations. *Id.* [0046]; *see also id.*, [0022] (“The DPs 114 may also be programmed with offset delay values corresponding to each nibble (e.g., OFFSET_P_UN, OFFSET_N_UN, OFFSET_P_LN and OFFSET_N_LN).”). A Skilled Artisan would thus understand that datapaths 114 in Butt delay the data strobe signal DQS in an amount based on signals received during a previous operation—e.g., the test memory data and data strobe signals received during read training in process 200 (shown in Figures 5-7 above).

149. It would have been obvious to a Skilled Artisan at the time of the ’506 Patent to apply the teaching of Butt to Hiraishi and implement the functionality of

determining the amount of delay for the delay circuit 372, e.g., by read leveling circuit 323 in Figure 5 of Hiraishi, based on signals received during a prior read training, and a Skilled Artisan would have had a reasonable expectation of success in making such a combination. Hiraishi explicitly calls for “read leveling,” e.g., EX1005, ¶¶[0090], [0140], [0147], Fig.5(323), Fig.13(step S4), Fig.15, and as explained above Butt teaches the details for performing read leveling. A Skilled Artisan would have recognized that the calibration provided by the read training in Butt would facilitate more accurate and rapid exchanges of data by centering the data strobe signal in a valid data eye. Indeed, Butt expressly teaches this motivation: “The present invention generally enables a reliable data read operation for high speed applications.” EX1029, [0036]. Moreover, application of the techniques in Butt to set the delay in the delay circuit 372 of Hiraishi, e.g., by the read leveling circuit 323, would be a simple application of known techniques to improve similar technology. The delay circuit 372 is serving an analogous function in Hiraishi: sending a delayed data strobe signal to trigger sampling of the corresponding data signal in a register or FIFO circuit. Accordingly, the calibration process 200 from Butt would offer the same benefit for delay circuit 372 in Hiraishi, as achieved in Butt.

150. In this combination, a Skilled Artisan would calibrate Hiraishi’s delay circuit 372 in the manner that Butt teaches to calibrate datapaths 114. Like the

datapaths 114 in Butt, the read leveling circuit 323 and delay circuit 372 would iteratively test memory access using different offsets to a received data strobe signal DQS, in order to find the maximum, minimum, and optimum offsets. The optimum offset would then be used in later memory read operations; the read leveling circuit 323 would adjust the base delay of the delay circuit 372 in the amount of the optimum offset (e.g., “about 90 degrees”). Thus, a Skilled Artisan would have understood that, when combined with Butt, Hiraishi’s read leveling circuit 323 determines the delay by which delay circuit 372 delays the data strobe signal DQS based at least on signals received by the first data buffer (including a known data pattern and the corresponding data strobe signal DQS) during one or more previous operations (the calibration process).

151. Accordingly, under Netlist’s apparent claim interpretation, claim 1 is at least rendered obvious by Hiraishi in light of the knowledge of a Skilled Artisan at the time, and/or Butt.

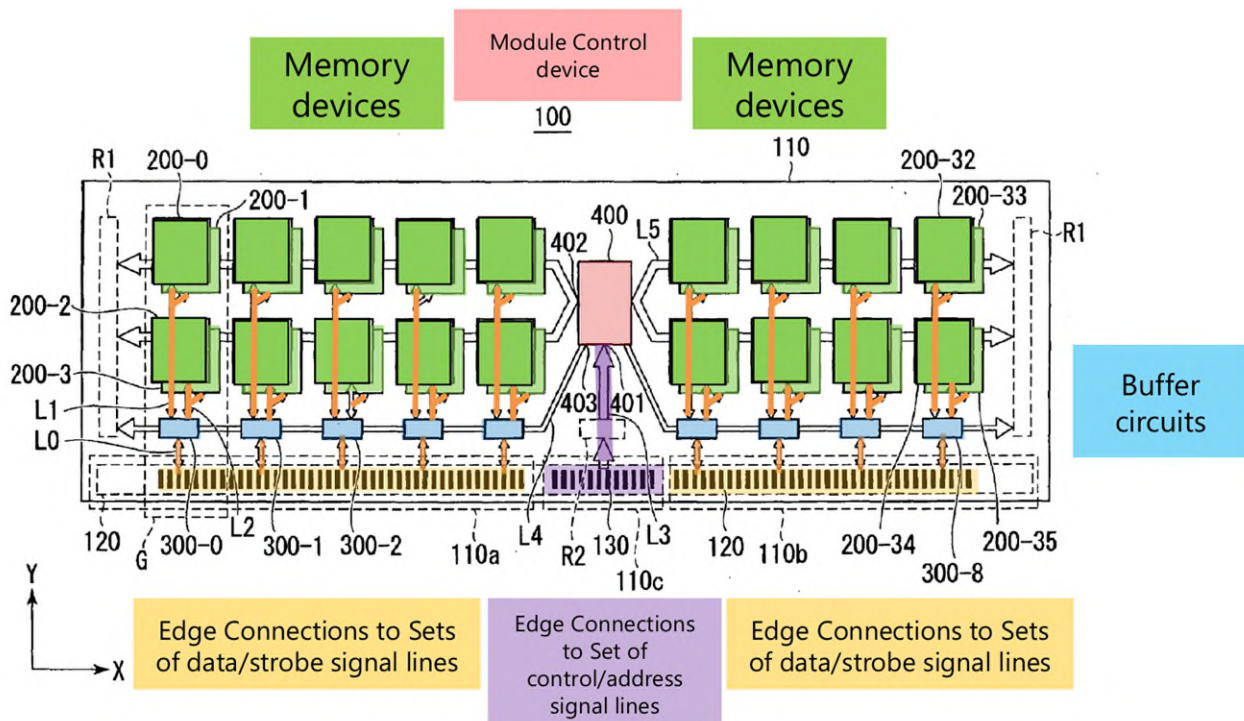
2. Claim 2

a) 2[a]: “The memory module of claim 1, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and”

152. As explained above, Hiraishi and/or Butt discloses each and every limitation of claim 1. Hiraishi further discloses this limitation as well. For example, “a second memory device in the selected rank [e.g., memory device 200-32 (Fig.

1)] is configurable to output at least a second section of the read data and at least a second read strobe.”

153. As explained above in connection with claim 1 and as shown in the annotated Figure 1 below, Hiraishi discloses ranks comprising multiple memory devices 200 each with data and strobe lines connecting the device to a respective data buffer 300. *See supra* ¶¶ 117-120.



EX1005 (Hiraishi), Fig. 1 (annotated). A Skilled Artisan would understand a read strobe signal sent from memory device 200-32 to data buffer 300-8 is a second read strobe signal, relative to the read strobe signal sent from memory device 200-0 to data buffer 300-0 (on data/strobe lines L1).

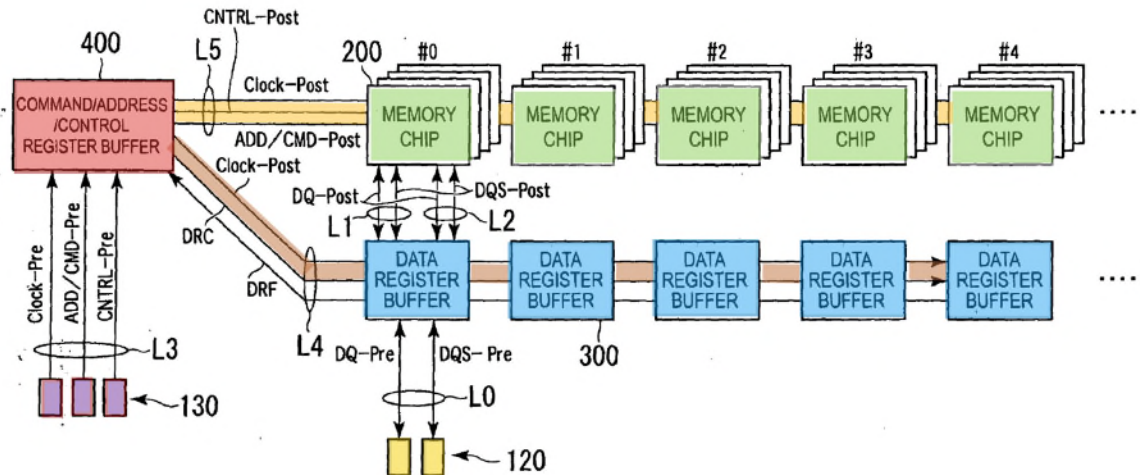


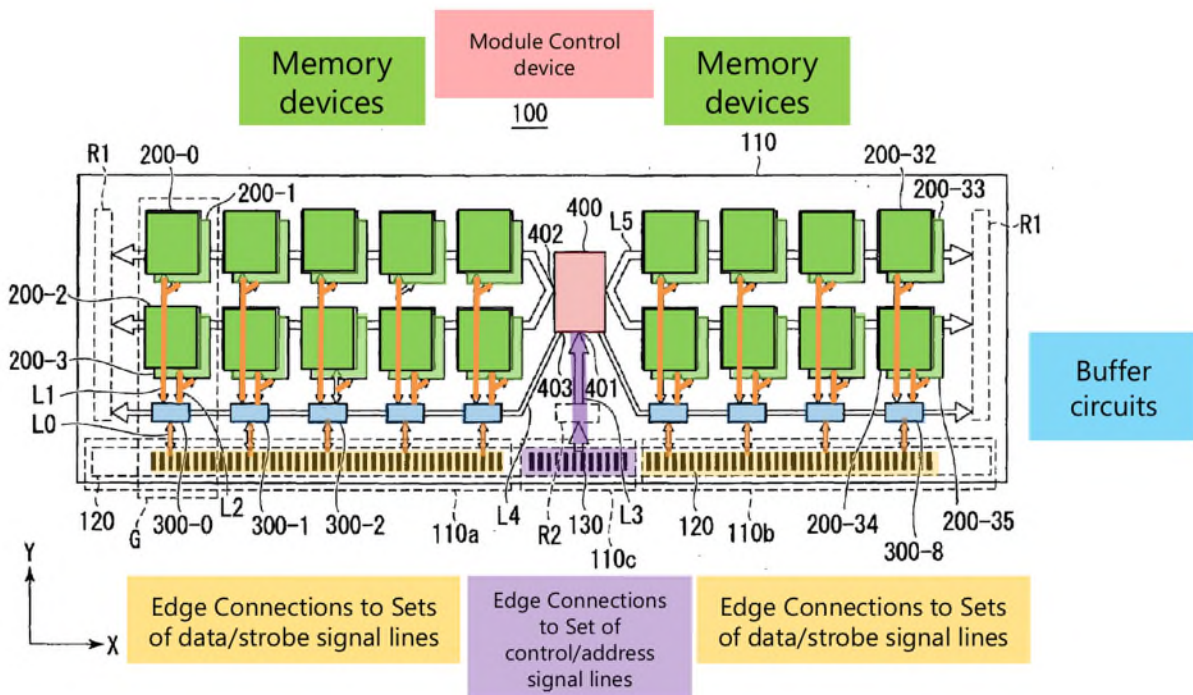
FIG. 7

Id., Fig. 7

154. As also explained above with respect to claim 1 (*supra* ¶¶ 117-120), a Skilled Artisan would further understand that in a read operation, each memory device 200 in the selected rank would output a corresponding section of the read data and its own read strobe signal on the corresponding data/strobe lines. Thus, a Skilled Artisan would understand that where memory device 200-0 outputs a “first” section of the read data and a “first” strobe signal, then memory device 200-32 would output a “second” section of the read data and second read strobe, on its own corresponding data/strobe lines (lines not labeled in Fig. 1).

b) 2[b]: “wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals,”

155. Hiraishi discloses this limitation. For example, “the data buffers [data register buffer circuits 300] further include a second data buffer [e.g., data register buffer circuit 300-8 (Fig.1)] configurable to, in response to the one or more of the module control signals” [e.g., buffer circuit 300-8 (blue) receives module command/address/control line L4 (Fig. 7) from command/address/control register buffer 400 (including DRC, brown, Fig. 7)].



EX1005 (Hiraishi), Fig. 1 (annotated and color added, showing buffer circuits in blue).

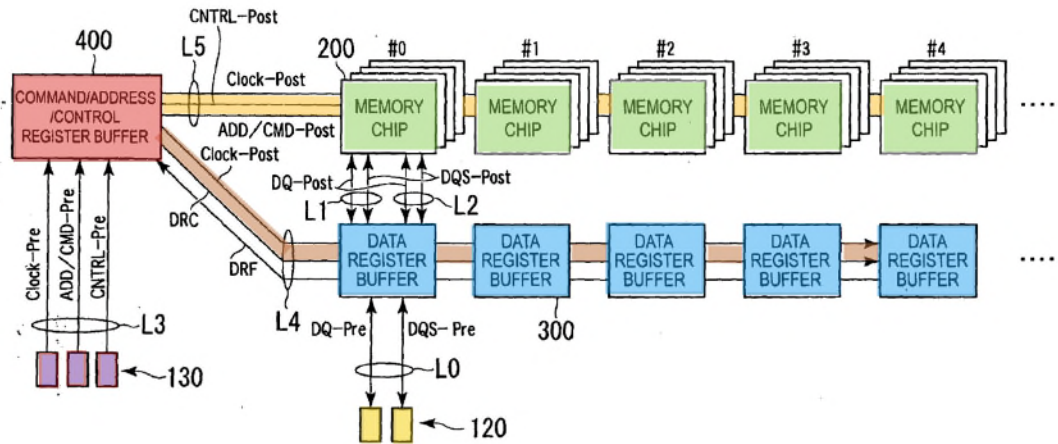


FIG. 7

Id., Fig. 7 (annotated).

c) 2[c]: “delay the second read strobe by a second predetermined amount to generate a second delayed read strobe,”

156. Hiraishi discloses this limitation. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim 1[f]. See *supra* ¶¶ 129-130. The “*second data buffer*” [e.g., data register buffer circuit 300-8] would “*delay the second read strobe by a second predetermined amount to generate a second delayed read strobe*” in the same manner as described for the *first data buffer* above.

d) 2[d]: “sample the second section of the read data using the second delayed read strobe; and,”

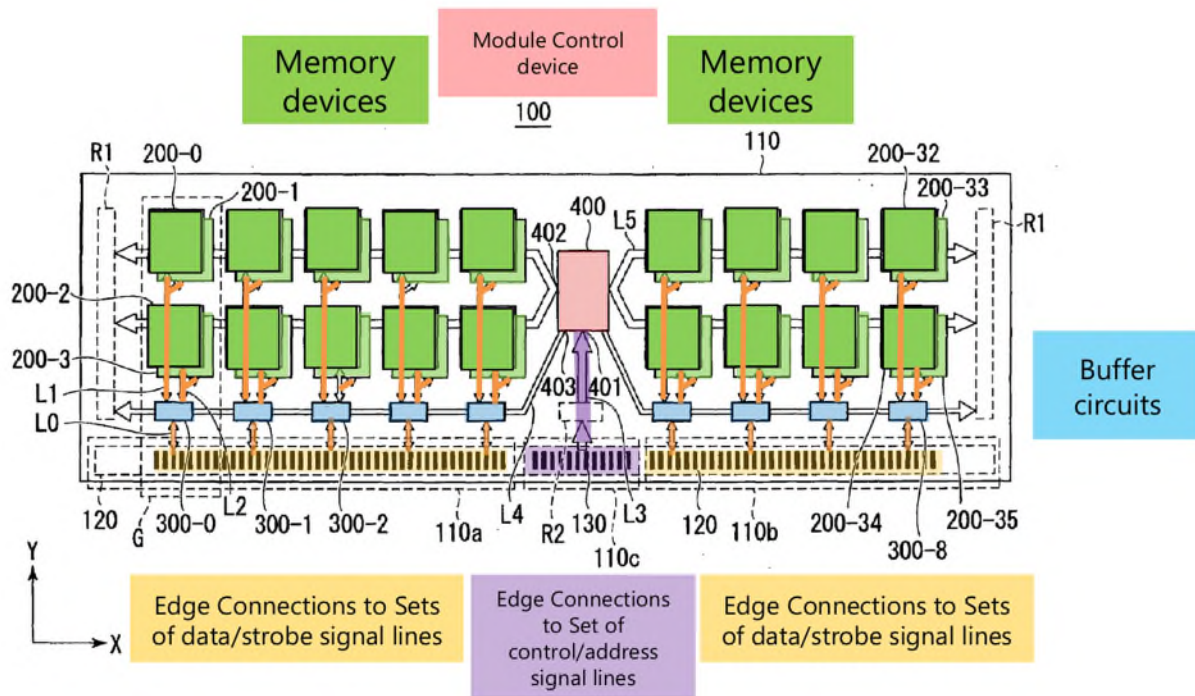
157. Hiraishi discloses this limitation. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim

1[g]. See *supra* ¶¶ 131-133. The “*second data buffer*” [e.g., data register buffer circuit 300-8] would “*sample the second section of the read data using the second delayed read strobe*” in the same manner as described for the *first data buffer* above.

158. To the extent one might argue that Hiraishi does not sample the read data using the delayed read strobe, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above in 1[g] for the “*first data buffer*,” it would have been obvious to a Skilled Artisan to utilize the sampling in Butt with the “*second data buffer*” [e.g., data register buffer circuit 300-8]. See *supra* ¶133.

e) 2[e]: “transmit the second section of the read data to a second section of the data bus;”

159. Hiraishi discloses this limitation. For example, “*the second data buffer*” [e.g., data register buffer circuit 300-8] can “*transmit the second section of the read data* [e.g., data received from 200-32] *to a second section of the data bus* [line 23, shown in Fig. 3].”



EX1005, Fig. 1 (annotated and color added, showing buffer circuits in blue)

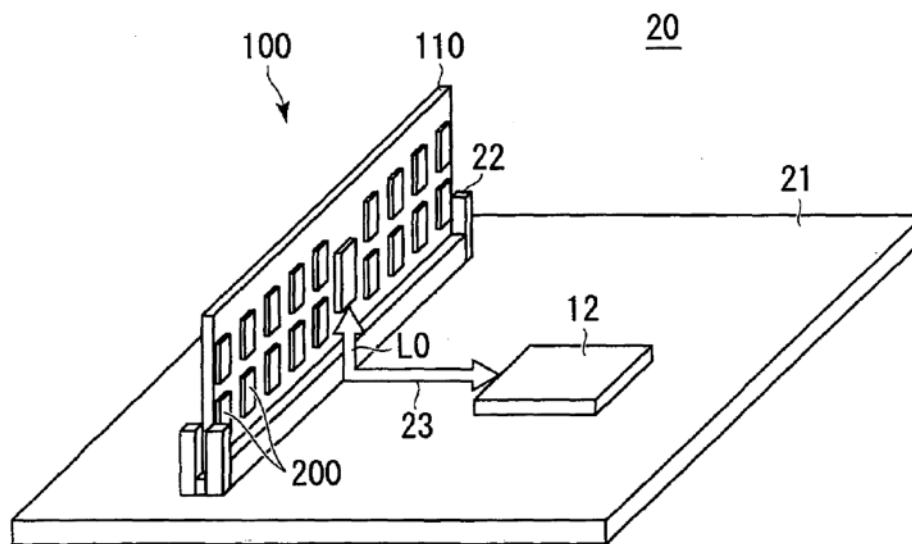


FIG.3

Id., Fig. 3. Hiraishi discloses that the data connectors 120 correspond to different memory devices 200:

The data connectors 120 are connectors for exchanging write data to be written in the memory chip 200 and read data read from the memory chip 200 between the memory module 100 and the memory controller. Although it is not particularly limited, the number of pins of the data connectors 120 is seventy two in the present embodiment. As shown in FIG. 1, among the seventy-two data connectors 120, data connectors corresponding to the memory chips 200-0 to 200-19 are arranged in an area 110a that is located substantially right below the memory chips 200-0 to 200-19, and data connectors corresponding to the memory chips 200-20 to 200-35 are arranged in an area 110 b that is located substantially right below the memory chips 200-20 to 200-35.

160. *Id.*, [0048]. Thus, a Skilled Artisan would understand that data register buffer circuit 300-8 would transmit the second section of the read data from 200-32 to a second section of the data bus via connectors 120, different from the first section corresponding to data received from 200-0.

f) 2[f]: “wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.”

161. Hiraishi discloses this limitation. An analogous determination for the “*first predetermined amount*” [e.g., the amount of delay imposed by data register

buffer circuit 300-0] is described above for claim 1[i]. *See supra* ¶¶ 136-151. The “*second predetermined amount*” [e.g., the amount of delay imposed by data register buffer circuit 300-8] can be determined in a manner similar to the “*first predetermined amount*” addressed above. Thus, for the same reasons, Hiraishi discloses this limitation.

162. To the extent one might argue that Hiraishi does not determine the predetermined amount of delay based on signals received during one or more previous operations, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above in 1[i] for the “*first predetermined amount*,” it would have been obvious to a Skilled Artisan to combine Butt with Hiraishi to determine the “*second predetermined amount*.” *See supra* ¶¶ 144-151.

3. Claim 4

a) 4[a]: “*The memory module of claim 2, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and*”

163. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 2. For example, as explained above for claim 1[i], “*the signals received by the first data buffer during one or more previous operations* [e.g., signals received during Hiraishi’s S4 leveling] *include at least a strobe signal associated with a previous operation* [e.g., a DQS signal from memory device 200 to data register buffer 300].” *Supra* ¶ 142.

164. To the extent one might argue that Hiraishi does not determine the predetermined amount of delay based on signals received during one or more previous operations, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above for claim 1[i], “*the signals received by the first data buffer during one or more previous operations [e.g., signals received by datapaths 114 during process 200] include at least a strobe signal associated with a previous operation [e.g., a DQS signal on which each offset is tested].*” It would have been obvious to a Skilled Artisan to combine Butt with Hiraishi such that delay circuit 372 in Figure 5 of Hiraishi similarly determines an optimum offset by testing for valid memory operations at different offsets of a DQS signals. See *supra* ¶¶144-151. Thus, a Skilled Artisan would find this limitation obvious based on the combination of Butt and Hiraishi.

b) 4[b]: “wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.”

165. Hiraishi discloses this limitation. An analogous determination for the “*first data buffer*” is described above for claim 4[a]. *Supra* ¶¶ 163-164. The “*second data buffer* [data register buffer 300-8]” would receive a strobe signal from memory device 200-32 during read leveling in the same manner as described above for how the “*first data buffer* [data register buffer 300-0]” would receive a strobe signal from memory device 200-0. The “*second data buffer* [data register

buffer 300-8]” would receive another DQS signal from the corresponding memory device 200-32. Thus, for the same reasons described for claim 4[a], Hiraishi discloses this limitation.

166. To the extent one might argue that Hiraishi does not determine the predetermined amount of delay based on signals received during one or more previous operations, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above in 4[a] for the “*first data buffer*,” it would have been obvious to a Skilled Artisan to combine Butt with Hiraishi such that the “*second data buffer*” determines an amount of delay based on calibrating an optimum DQS offset. *Supra* ¶ 164. Thus, for the same reasons described for claim 4[a], Hiraishi in combination with Butt renders this limitation obvious.

4. Claim 6: “*The memory module of claim 1, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation.*”

167. As explained above, Hiraishi and/or Butt discloses each and every limitation of claim 1. For the same reasons stated for claim 4[a], Hiraishi further discloses or renders obvious claim 6, either alone or in further view of Butt. *Supra* ¶¶ 163-164.

5. Claim 7

a) 7[a]: “The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and”

168. As explained above, Hiraishi and/or Butt disclose each and every limitation of claim 1. Hiraishi further discloses this limitation as well. For example, “the module control device [e.g., command/address/control register buffer 400 (red in annotated Fig. 7 below)] is further configurable to receive a system clock signal [CK/Clock-Pre, purple] and output a module clock signal [CK/Clock-Post, brown].”

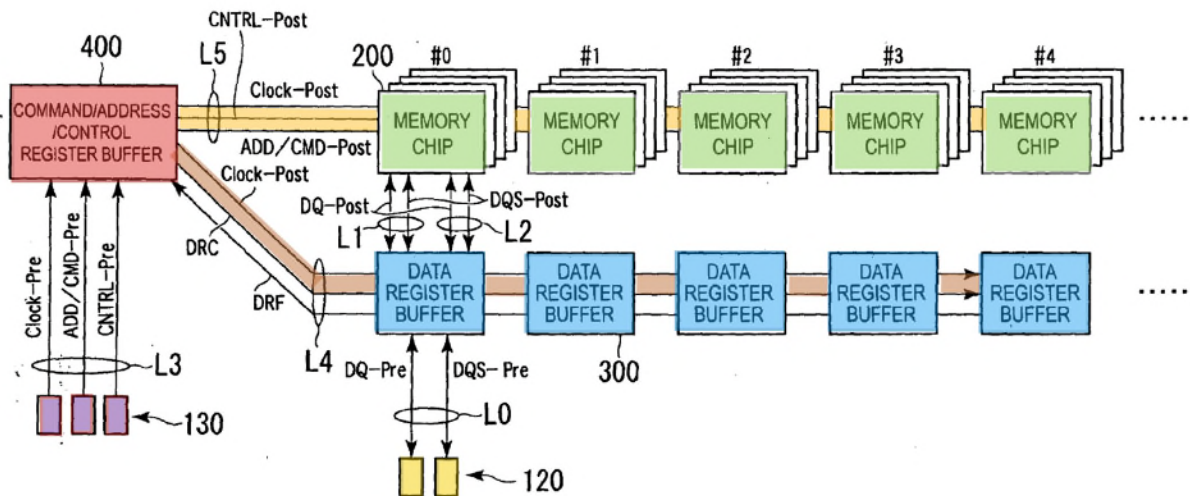


FIG.7

EX1005, Fig.7 (color added); see also *id.* Fig. 6 (showing system clock signal CK at 401, and module clock signal CK at 403). Hiraishi further states:

The clock signal CK to be supplied to the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400. ***In FIG. 7, a clock signal transferred through the command/address/control line L3 is represented by a clock signal Clock-Pre, and a clock signal transferred through the command/address/control line L5 is represented by a clock signal Clock-Post.***

Id., [0108]; *see also id.*, [0060]. A Skilled Artisan would thus understand that Hiraishi's command/address/control register buffer 400 "receive[s] a system clock signal [Clock-Pre] and output[s] a module clock signal [Clock-Post]."

b) 7[b]: "wherein the first data buffer is further configurable to: [7b1] receive the module clock signal;"

169. Hiraishi discloses this limitation. For example, "the first data buffer [e.g., data register buffer 300] is further configurable to receive the module clock signal [CK (Figs. 5 and 6), also shown as Clock-Post (Fig. 7)]." As shown in Figure 7 above and in Figure 5 below, Hiraishi discloses that data register buffer 300 receives the module clock signal (CK or Clock-Post):

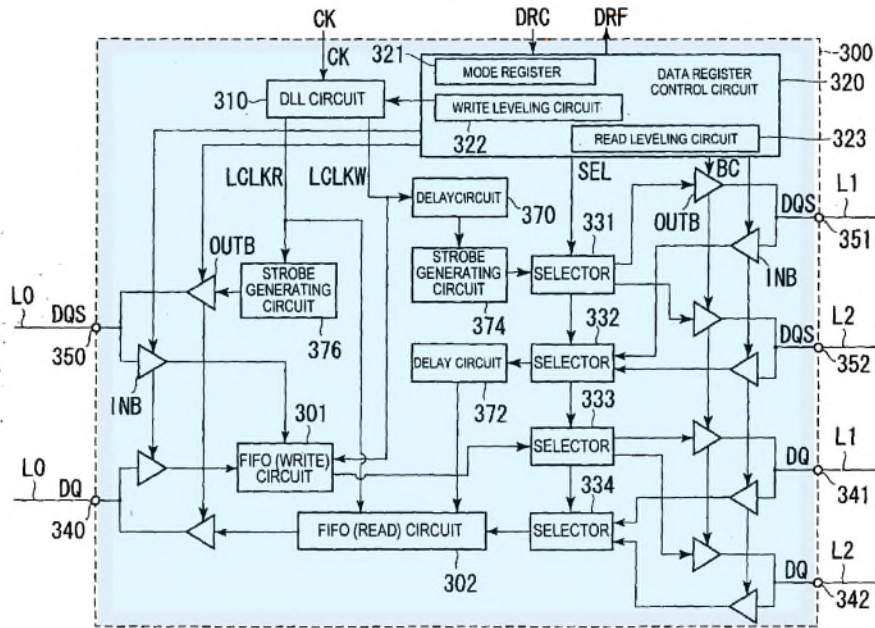


FIG. 5

Id., Fig. 5; *see also id.*, [0087] (“The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR **based on the clock signal CK that is supplied from the command/address/control register buffer 400 . . .**”).

c) 7[b]: “wherein the first data buffer is further configurable to: ... [7b2] generate a local clock signal having a programmable phase relationship with the module clock signal;

170. Hiraishi discloses this limitation. For example, “the first data buffer [e.g., data register buffer 300 including DLL circuit 310] is further configurable to ... generate a local clock signal [e.g., LCLKW and LCLKR (Fig. 5)] having a programmable phase relationship with the module clock signal.” Hiraishi expressly explains that the DLL circuit 310 generates local clock signals LCLKR and LCLKW based on the module clock signal CK:

An output operation timing of the FIFO (Write) circuit 301 is defined by the ***internal clock LCLKW that is generated by the DLL circuit 310***. An output operation timing of the FIFO (Read) circuit 302 is defined by the ***internal clock LCLKR that is generated by the DLL circuit 310***. The DLL circuit 310 is a circuit that ***generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400***, having the ***same circuit configuration and function as that of the DLL circuit 212*** provided in the memory chip 200. It is selected based on a set content in a data register control circuit 320 whether to use the DLL circuit 310.

Id., [0087]. Hiraishi also discloses that the generated clock signals have a “programmable phase relationship.” For example, Hiraishi discloses that its read and write leveling operations are adjusting the timing of the read and write operations, respectively. *Id.* at [0140] (“The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.”). A Skilled Artisan would have understood from this disclosure that this time adjustment includes programming the phase relationships of the local clocks used for the read and write operations. Indeed, Hirashi expressly discloses that the write leveling circuit 322 displaces the LCLKW clock’s phase as required by the write

leveling operation, and a Skilled Artisan would understand that read leveling circuit 323 would similarly program the phase relationship for LCLKR. *Id.*, [0145] (“The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift.”). Furthermore, as also explained by Hiraishi, the DLL circuit 310 in the data buffer has the same function as DLL circuit 212 in the memory chip. *Id.* at [0087]. With respect to the DLL circuit 212 in the memory chip 200, Hiraishi further explains that this functionality includes generating a local clock with a phase matching the phases of the read data and data strobe signals:

The DLL circuit 212 takes a role of generating an internal clock LCLK and supplying the internal clock LCLK to a data input/output circuit 213 and a data strobe signal input/output circuit 214. The internal clock LCLK is a signal that is phase-controlled with respect to the clock signal CK, of which a phase is slightly advanced with respect to the clock signal CK such that phases of read data DQ and a data strobe signal DQS match with a phase of the clock signal CK.

Id., [0074]. Hiraishi also discloses that:

As described above, the DLL circuit is a circuit that generates an internal clock signal of which a phase is controlled with respect to an external clock signal, which is used for matching the phases of

the read data DQ and the data strobe signal DQS with the phase of the clock signal CK.

Id., [0163]. A Skilled Artisan would have understood from this disclosure that Hiraishi's DLL circuit 310 in data register buffer 300 is likewise configured to generate local clock signals with a programmable phase relationship relative to the module clock signal CK.

d) 7[b]: “wherein the first data buffer is further configurable to: ... [7b3] output the local clock signal;”

171. Hiraishi discloses and/or renders obvious this limitation, in view of the knowledge of a Skilled Artisan. For example, Hiraishi discloses an embodiment where “*the first data buffer* [e.g., data register buffer 300 including DLL circuit 310] *is further configurable to output the local clock signal* [to the memory device 200].”

172. Although Hiraishi discloses embodiments in which the buffer circuits 300 and memory devices 200 each have their own DLL circuits (and thus generate their own local clock signal, such that the local clock of the buffer circuits is not output to the memory devices), Hiraishi also discloses that:

[W]hile the above embodiment has described a memory chip that includes a DLL circuit therein as the memory chip 200, ***a memory chip that does not include a DLL circuit therein can be alternatively used.*** In this case, ***the DLL circuit included in the***

data register buffer 300 is used to adjust the input/output timing.”

Id., [0200]. A Skilled Artisan would thus have understood from this disclosure that, when the memory chips do not include a DLL circuit, it is the DLL circuit in the buffer circuit 300 which is used to adjust the input/output timing in the memory chips as well, and a local clock signal of the buffer circuits would be output to the respective set of memory devices in order to synchronize the operations of those memory devices with the buffer circuit.

173. Indeed, a Skilled Artisan would have known that sharing circuitry between buffer circuits and memory devices, including circuits that generate a local clock, was a well-known design choice at the time of the invention, and that one common technique is to output the local clock of the buffer circuit to the memory devices. For example, U.S. Patent No. 8,566,516 to Schakel (“Schakel,” filed October 30, 2007 and claiming priority to July 31, 2006) discloses several configurations of memory modules, one of which involves a plurality of memory devices (DRAM modules) electrically interconnected to each other and a single buffer circuit (“intelligent buffer 133”), which includes the functionality of an interface circuit (“interface circuit 102”). *See, e.g.*, EX1009 (Schakel) at 4:5-14 (“In some embodiments, the any of the memory devices 104A-N may itself be a group of memory devices, or may be a group in the physical orientation of a stack.

For example, FIG. 1B shows a memory device 130 which is comprised of a group of DRAM memory devices 132A-132N all electrically interconnected to each other and an intelligent buffer 133. In alternative embodiments, the intelligent buffer 133 may include the functionality of interface circuit 102. Further, the memory device 130 may be included in a DIMM (dual in-line memory module) or other type of memory module.”); FIG. 1B:

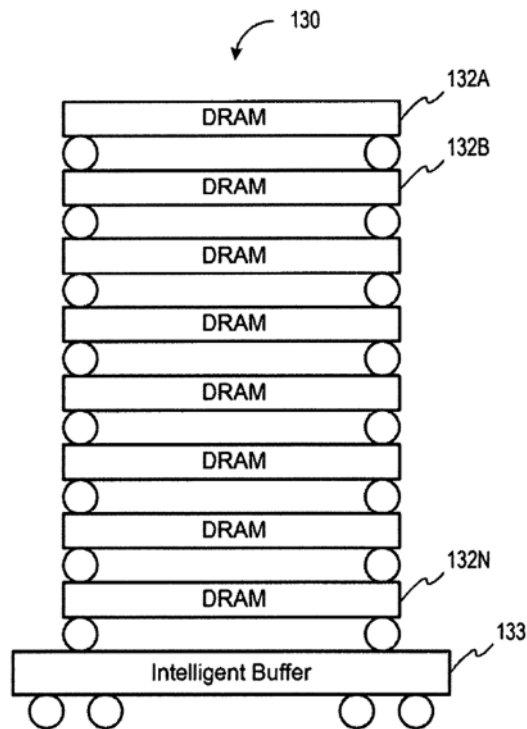


FIG. 1B

174. Schakel teaches that, in such an arrangement, “[t]he interface circuit 102 interfaces a plurality of signals 108 between the system device 106 and the memory devices 104A-N. The signals 108 may include, for example, data signals, address signals, control signals, **clock signals**, and the like. In some embodiments,

all of the signals 108 communicated between the system device 106 and the memory devices 104A-N are communicated via the interface circuit 102.” *Id.*, 4:31-41, Fig. 1A (reproduced below, annotated).

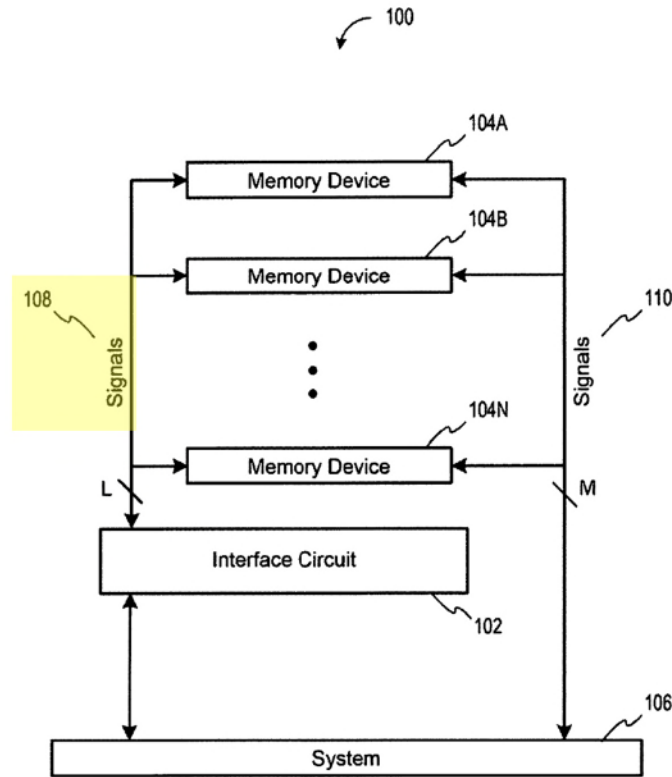


FIG. 1A

In other words, Schakel discloses that, as an alternative to each DRAM module having its own clock generating circuitry, they can be associated with a single buffer circuit which outputs a clock signal thereto. This disclosure is consistent with the knowledge of a Skilled Artisan at the time—including that it would have been obvious to output the local clock signal of the buffer circuit to the memory devices. *See also* EX1007 (Ellsberry) at Figs. 10-13 (showing data buffer transmitting clock signal ECLK to the memory devices).

e) 7[c]: “wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.”

175. Hiraishi discloses and/or renders obvious this limitation, in view of the knowledge of a Skilled Artisan. For example, as explained above for 7[b3], Hiraishi discloses that “*the first data buffer [e.g., data register buffer 300 including DLL circuit 310] is further configurable to output the local clock signal [to the memory device 200].*” *Supra* ¶¶ 171-174. Hiraishi expressly states that in such embodiments that instead of a circuit on the memory device generating a local clock signal “the DLL circuit included in the data register buffer 300 is used to adjust the input/output timing.” *Id.*, [0200]. Thus, a Skilled Artisan would understand that where the output of DLL circuit 310 [e.g., LCLKR and/or LCLKW] are “used to adjust the input/output timing” of the memory device 200, that means that Hiraishi teaches: “*wherein the first memory device [200-0] is configurable to receive the local clock signal [e.g., LCLKR and/or LCLKW from DLL circuit 310] and to output the first section of the read data and first read strobe in accordance with the local clock signal.*”

6. Claim 11: “*The memory module of claim 1, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.*”

176. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 1. Hiraishi alone further discloses this limitation as well. For example, as explained above for claim 1[i], Hiraishi discloses the “*first predetermined amount*” [e.g., the amount of delay imposed by data register buffer circuit 300-0] is determined based at least on the signals received by the first data buffer during one or more previous operations.” See *supra* ¶¶136-151. As such, a Skilled Artisan would understand that at least the circuitry shown in Figure 5 for data register buffer circuit 300 includes “*circuitry [including read leveling circuit 323 and delay circuit 372] that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.*”

177. To the extent one might argue that Hiraishi does not sufficiently disclose determining the predetermined amount of delay based on signals received during one or more previous operations, this claim is rendered obvious by Hiraishi in further view of Butt. Butt discloses that the delay of the read data strobe signal is determined based on the shape of the data eye that is measured by using predetermined read data signals from the memory device. EX1029, e.g., at [0044] (“Verifying that valid DDR data may be read with the delay offset values set to

zero. For example, a routine may be executed that writes to, reads from, and compares a selected data pattern to a selected range of the DDR memory 106. If valid data cannot be read with the delay offset values set to zero, the initial settings may not be sufficient.”); *see also id.* at Figs. 6 and 7 (performing test access in blocks 222 and 242 to determine the maximum and minimum delays for the data eye). For the same reasons explained above with reference to claim element 1[i], it would have been obvious to a Skilled Artisan to combine Butt with Hiraishi to determine the “*first predetermined amount.*” *See supra* ¶¶144-151. As described above, in such a combination the read leveling circuit 323 and delay circuit 372 of Hiraishi would iteratively determine an optimum offset, as taught for the datapaths 114 in Butt. Thus, a Skilled Artisan would have understood that at least the modified delay circuit 372 and the read leveling circuit 323 are part of the “circuitry that determines first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.”

7. Claim 13: “*The memory module of claim 1, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.*”

178. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 1. For example, Hiraishi states that “[t]he memory chips 200 are, for example, DRAMs,” EX1005, [0050], and can be, in particular, “DDR3 DRAM,” *id.* [0163], [0170], which a Skilled Artisan would understand is a

type of “*double-data-rate dynamic random-access memory*” standardized by JEDEC, *see* EX1021, pp.465, 471-72, 476-77; EX1020 (JESD79-3C), e.g., at 56, 59, 69 (showing double data rate).

8. Claim 14

a) 14[pre]: “A method, comprising:

179. To the extent the preamble is limiting, Hiraishi (EX1005) discloses methods involving a memory module, including for example the read/write leveling steps S4 and S5 shown in Figure 13 and the timing diagrams for memory operations depicted in Figures 11 and 15.

b) 14[a]: “at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including”

180. For the same reasons stated for claim 1[pre], Hiraishi further discloses this element. *Supra* ¶¶ 101-103.

c) 14[b]: “a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board,”

181. For the same reasons stated for claims 1[a] and 1[b], Hiraishi further discloses this element. *Supra* ¶¶ 104-113.

d) 14[c1]: “memory devices arranged in multiple ranks on the module board and coupled to the module control device, and”

182. For the same reasons stated for claim 1[c1], Hiraishi further discloses this element. *Supra* ¶¶ 114-116.

e) 14[c2]: “data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer,”

183. For the same reasons stated for claim 1[d], Hiraishi further discloses this element. *Supra* ¶¶ 122-126.

f) 14[d]: “wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;”

184. As explained for claim 1[d], Hiraishi discloses a “each respective data buffer [e.g., data register buffer 300] is coupled to one respective memory device [e.g., memory devices 200].” *Supra* ¶¶ 122-126. Hiraishi further discloses that the data register buffer 300 “inputs and outputs 1-byte data[.]” EX1005, [0085].

Accordingly, a Skilled Artisan would understand that “each respective data buffer [e.g., data register buffer 300] is coupled to one respective memory device [e.g., memory device 200] having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks.” Indeed, a Skilled Artisan would have understood that 8-bit-wide (“x8”) memory devices, and pairs of 4-bit-wide (“x4”) memory devices, were standard at the time. *See, e.g.*, EX1020

(JESD79-3C) at 1; EX1018 (JEDEC 21-C) at 4.20.4-12 (module with x8 memory devices); *id.* at 4.20.4-16 (module with pairs of x4 memory devices).

g) 14[e]: “receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;”

185. For the same reasons stated for claim 1[b], Hiraishi further discloses this element. *Supra* ¶¶ 108-113.

h) 14[f1]: “outputting, at the module control device, registered C/A signals in response to the input C/A signals,”

186. For the same reasons stated for claim 1[b], Hiraishi further discloses this element. *Supra* ¶¶ 108-113.

i) 14[f2]: “wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;”

187. For the same reasons stated for claim 1[c2], Hiraishi further discloses this element. *Supra* ¶¶ 117-121.

j) 14[g]: “outputting, at the module control device, module control signals;”

188. For the same reasons stated for claim 1[b], Hiraishi further discloses this element. *Supra* ¶¶ 108-113.

k) 14[h]: “receiving, at each of the data buffers, the module control signals from the module control device;”

189. For the same reasons stated for claim 1[d], Hiraishi further discloses this element. *Supra* ¶¶ 122-126.

l) 14[i]: “the method further comprising, at the first data buffer, in response to one of more of the module control signals:”

190. For the same reasons stated for claim 1[e], Hiraishi further discloses this element. *Supra* ¶¶ 127-128.

m) 14[j]: “delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;”

191. For the same reasons stated for claim 1[f], Hiraishi further discloses this element. *Supra* ¶¶ 129-130.

n) 14[k]: “sampling the first section of the read data using the first delayed read strobe; and”

192. For the same reasons stated for claim 1[g], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶ 131-133.

o) 14[l]: “transmitting the first section of the read data to a first section of the data bus; and”

193. For the same reasons stated for claim 1[h], Hiraishi further discloses this element. *Supra* ¶¶ 134-135.

p) 14[m]: “the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.”

194. For the same reasons stated for claim 1[i], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶ 136-151.

9. Claim 15

a) 15[a]: “The method of claim 14, wherein the data buffers further include a second data buffer, and”

195. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 14. For the same reasons stated for claim 2[b], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 155.

b) 15[b]: “wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe,”

196. For the same reasons stated for claim 2[a], Hiraishi further discloses or renders obvious this element. *Supra* ¶¶ 152-154.

c) 15[c]: “the method further comprising, at the second data buffer, in response to the one or more of the module control signals:”

197. For the same reasons stated for claim 2[b], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 155.

d) 15[d]: “delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;”

198. For the same reasons stated for claim 2[c], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 156.

e) 15[e]: “sampling the second section of the read data using the second delayed read strobe; and”

199. For the same reasons stated for claim 2[d], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶157-158.

f) 15[f]: “transmitting the second section of the read data to a second section of the data bus;”

200. For the same reasons stated for claim 2[e], Hiraishi further discloses or renders obvious this element. *Supra* ¶¶ 159-160.

g) 15[g]: “wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations.”

201. For the same reasons stated for claim 2[f], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶ 161-162.

10. Claim 17

a) 17[a]: “The method of claim 15, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and”

202. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 15. For the same reasons stated for claim 4[a], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶ 163-164.

b) 17[b]: “the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.”

203. For the same reasons stated for claim 4[b], Hiraishi alone and/or in combination with Butt further disclose or render obvious this element. *Supra* ¶¶ 165-166.

11. Claim 18

a) 18[a]: “The method of claim 14, further comprising:”

204. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 14.

b) 18[b]: “receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;”

205. For the same reasons stated for claim 7[a], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 168. As shown in Figures 6-7 (below),

Hirashi discloses that the “*system clock signal*” [CK/Clock-Pre, purple] is received at the “*module control device*” [400] “*concurrently with receiving the input C/A signals*” [CNTRL-Pre, ADD/CMD-Pre] at terminal 401. EX1005, [0060], Figs. 6, 7.

c) 18[c]: “*outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;*”

206. For at least the same reasons stated for claim 7[a], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 168. Hiraishi further discloses, as shown in Figure 7, that the “*module control device [command/address/control register buffer 400, red]*” outputs both the “*module clock signal [e.g., Clock-Post]*” and the “*module control signal [e.g., DRC]*” on control line L4.

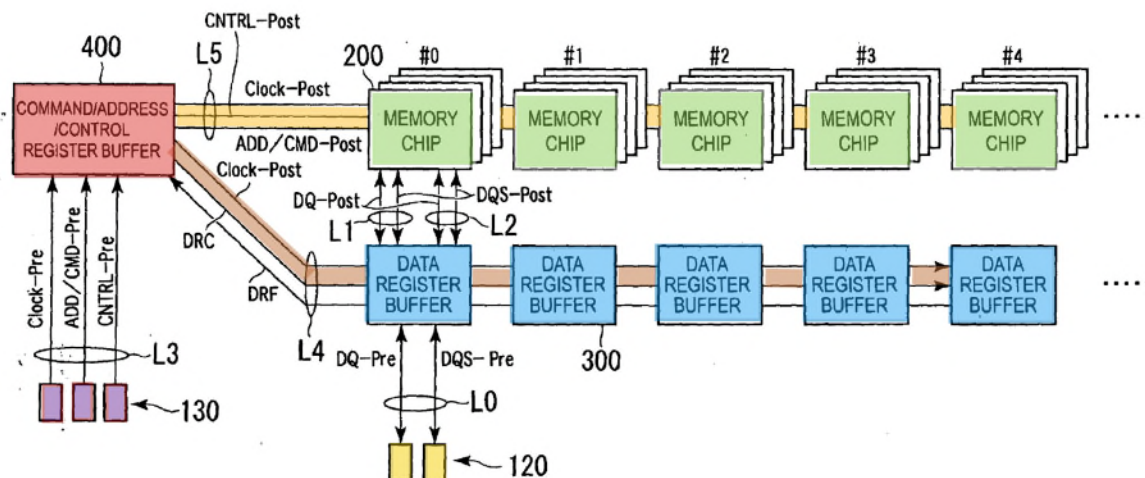


FIG.7

EX1005, Fig. 7 (color added); *see also* [0019] (“Fig. 7 is a connection diagram of memory module 100”). A Skilled Artisan would thus understand that Hiraishi discloses “*outputting at the module control device* [command/address/control register buffer 400, red], *a module clock signal* [e.g., Clock-Post] *concurrently with outputting the module control signal* [e.g., DRC].” *See also id.* at Fig. 6 (showing details of the command/address/control register 400, including a PLL circuit 420 for outputting a module clock signal, brown, together with the module control signal DRC through output terminal 403) and [0098] (“The PLL circuit 420 is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller 12 having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200.”). Hiraishi also explains that the operation of the circuit that generates the module control signals DRC is synchronized with the same clock (LCLKA) which is output to the data register buffers. *Id.* at [0099] (“The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403.”).

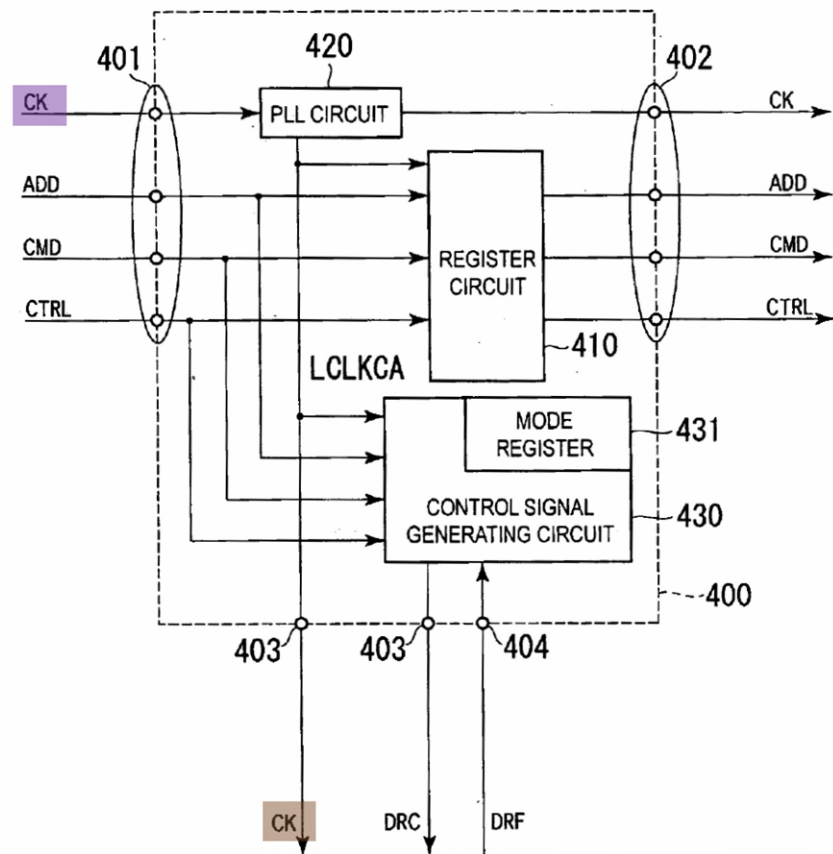


FIG.6

A Skilled Artisan would have understood that “*module clock signal*” is output “*concurrently with outputting the module control signals*” because they are output at the output terminal 403 and the generation of the module control signals is synchronized by the same clock signal (LCLKCA).

d) 18[d]: “receiving, at the first data buffer, the module clock signal;”

207. For the same reasons stated for claim 7[b1], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 169.

e) 18[e]: “generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and”

208. For the same reasons stated for claim 7[b2], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 170.

f) 18[f]: “outputting, at the first data buffer, the local clock signal;”

209. For the same reasons stated for claim 7[b3], Hiraishi further discloses or renders obvious this element. *Supra* ¶¶ 171-174.

g) 18[g]: “receiving, at the first memory device, the local clock signal; and”

210. For the same reasons stated for claim 7[c], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 175.

h) 18[h]: “outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.”

211. For the same reasons stated for claim 7[c], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 175.

B. Claims 3, 5, 12, and 16 are Obvious Over Hiraishi alone or in view of Butt and further in view of Ellsberry

212. Claims 3, 5, 12, and 16 of the '506 Patent are all obvious over Hiraishi alone or in view of Butt, and further in view of Ellsberry. In particular, it would have been obvious to a Skilled Artisan to modify Hiraishi to use a pair of 4-

bit wide memory devices in place of each individual 8-bit wide memory device 200.

213. Although Hiraishi discloses that each of the memory devices has a data width of 1 byte, Hiraishi does not limit his invention to that particular data width, *see, e.g.*, EX1005 (Hiraishi) [0073] (stating “memory chip 200 is a DRAM” without limiting the data width of the DRAM) and thus a Skilled Artisan would have understood that a data width of 1 byte is just one implementation, and other implementations can use memory devices with different bit widths. *See, e.g.*, EX1020 (JESD79-3C) at 1, 3-12 (describing standard DDR3 SDRAM devices with x4, x8, and x16 data widths), and EX1018 (JESD21-C) at 4.20.4-25 to -27 (describing DDR SDRAM Module Configurations for Registered DIMM, including x8 and pairs of x4 DDR SDRAM devices); *see also* EX1021 (Jacobs) at 370-71 and Table 8.1 (showing x4, x8, and x16 memory devices as known alternatives). Thus, using a pair of 4-bit wide memory devices instead of one 8-bit wide memory device would have been obvious in view of the knowledge of a person of ordinary skill in the art since using either 4-bit or 8-bit wide memory devices on a module was well known at the time.

214. For example, Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Hiraishi and expressly describes modules with 8-bit wide data buffers (SWITCH ASIC, blue,

with DQ[3:0] called lower nibble, and DQ [7:4] called upper nibble) coupled to either 8-bit wide memory chips (below right, green) or pairs of 4-bit wide memory chips (below left, green). *See, e.g., EX1007 (Ellsberry) at Fig. 11 (pairs of 4-bit wide memories) and Fig. 13 (8-bit wide memories):*

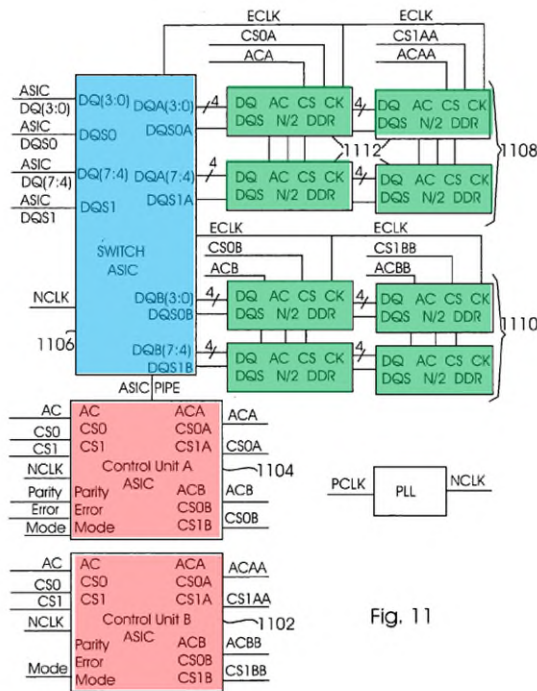


Fig. 11

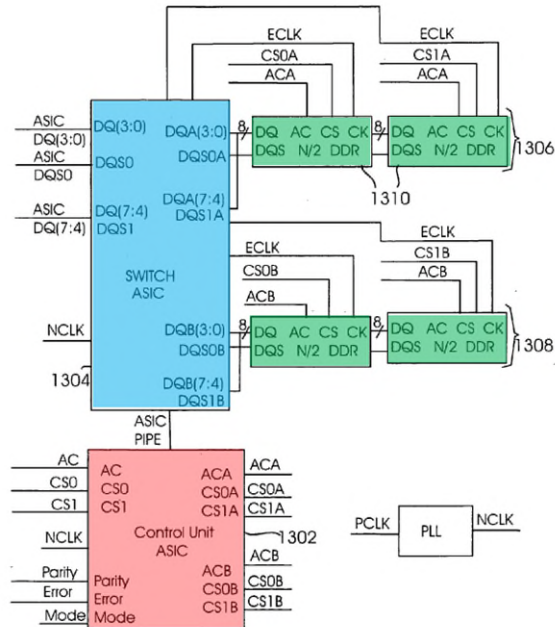


Fig. 13

215. A Skilled Artisan would understand that FIGS. 2, 5, and 13 correspond to an embodiment of Ellsberry utilizing 8-bit memory devices, and FIGS. 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit memory devices. EX1015 (FWD of IPR2018-00362) at 77-78 (PTAB agreeing that Ellsberry discloses embodiments with both 4-bit-wide and 8-bit-wide memory devices). With respect to the 4-bit embodiment, Ellsberry explains that the memory module of FIG. 6 “uses a dual stack configuration (similar to that illustrated in

FIG. 11) in which two control units 604 are employed, one control unit 604 on each side of the module.” EX1007 (Ellsberry), [0051]. A Skilled Artisan would understand from this disclosure that, in this case, two 4-bit wide memory devices are stacked in each “CSP” package shown in FIG. 6. *See, e.g.*, EX1020 (JESD79-3C) at 6 (showing “Stacked” x4 memory devices with two chip-select signals, one for each memory device in a different rank). Thus, in FIG. 11 of Ellsberry, four pairs of 4-bit memory devices are used rather than four 8-bit wide memory devices as shown in FIG. 13. In FIG. 11, two 4-bit wide memory devices are coupled to Port A, bits [3:0] and [7:4], respectively, and receive the same chip select signal. For example, a pair of 4-bit memory devices coupled to bits [7:0] of Port A for this arrangement receive the CS0A chip select signal generated by Control Unit A ASIC as shown in Fig. 11, above. *See also* EX1007 (Ellsberry), [0051], [0054]. Also, another control unit ASIC (B) is mounted to the other side of the module in FIG. 6, but otherwise the module operates as before. *Id.*, [0051].

216. A Skilled Artisan trying to select the available bit width of the memory devices and the corresponding buffers for Hiraishi’s memory module would have been motivated to look at Ellsberry’s disclosure, and would have had a reasonable expectation of success in making such a combination, because Ellsberry discloses a memory module with the same distributed buffer architecture and four

ranks of memories as Hiraishi and expressly describes modules with 8-bit wide data buffers and with 8-bit and 4-bit wide chips.

1. Claim 3

a) 3[a]: “The memory module of claim 2, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe,”

217. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 2. *Supra* ¶¶152-162. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry (discussed above, ¶¶213-216). For example, when modified in view of the knowledge of a Skilled Artisan and/or Ellsberry to use pairs of 4-bit memory devices instead of an 8-bit memory device, the “*first memory device*” described above in 1[c2] (e.g., in rank 0 at the location of 200-0) would be a 4-bit memory device handling, say, a lower nibble of a data byte, and paired with that memory device would be a second 4-bit memory device for handling the other, upper nibble of that data byte (i.e., “*a third memory device in the selected rank*,” here rank 0), together making a pair of 4-bit memory devices connected to the same data buffer (e.g., 300-0). *Supra* ¶¶213-216. In this example, the 4-bit memory for the upper nibble is “*a third memory device in the selected rank*” (here rank 0), and would be “*configurable to output a third section of the read data and a third read strobe*,” i.e., the upper nibble for the data byte connected to the data buffer (e.g., 300-0). This example is

consistent with Ellsberry, which expressly shows that each 4-bit wide memory device (green, below) is coupled to four data lines (“/4”), and a corresponding strobe signal line (connected to “DQS”) coupled to the respective data buffer (blue), where each pair of 4-bit memory devices (e.g., lower nibble connected to DQA(3:0) and upper nibble connected to DQA(7:4)) shares the same chip-select signal (e.g., CS0A). EX1007 (Ellsberry) at Fig. 11 (reproduced below, annotated).

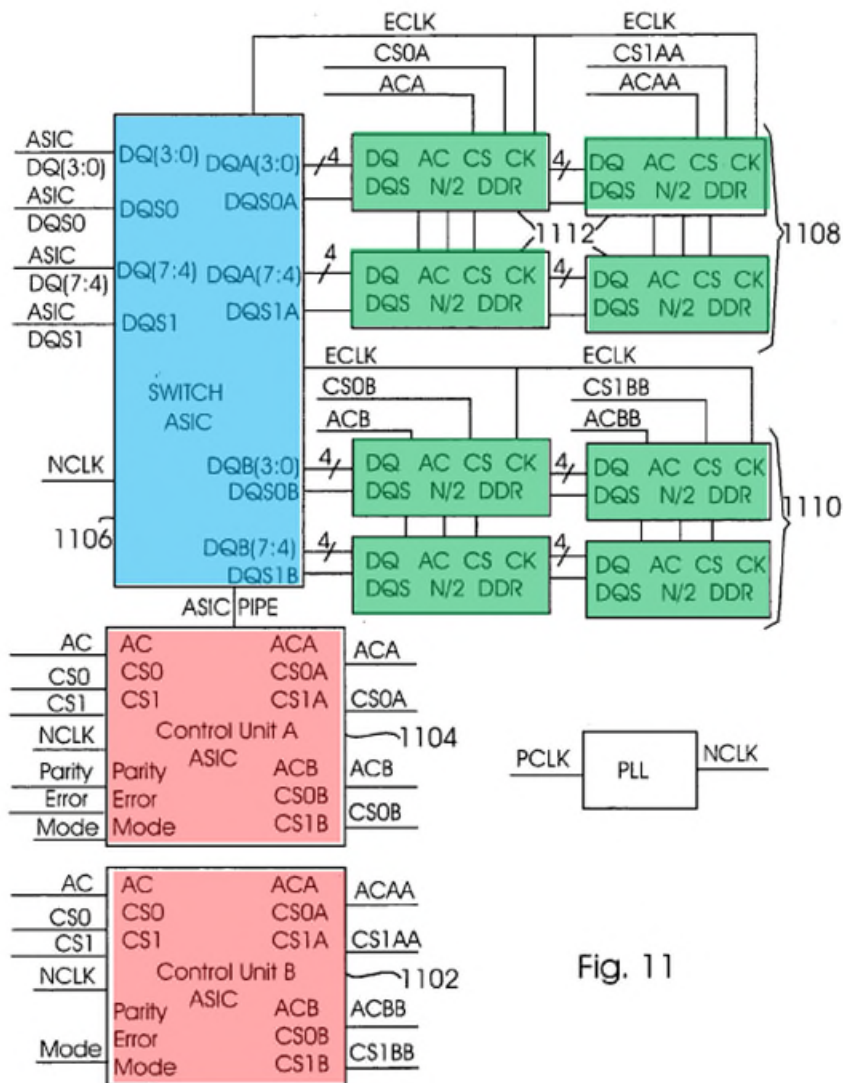
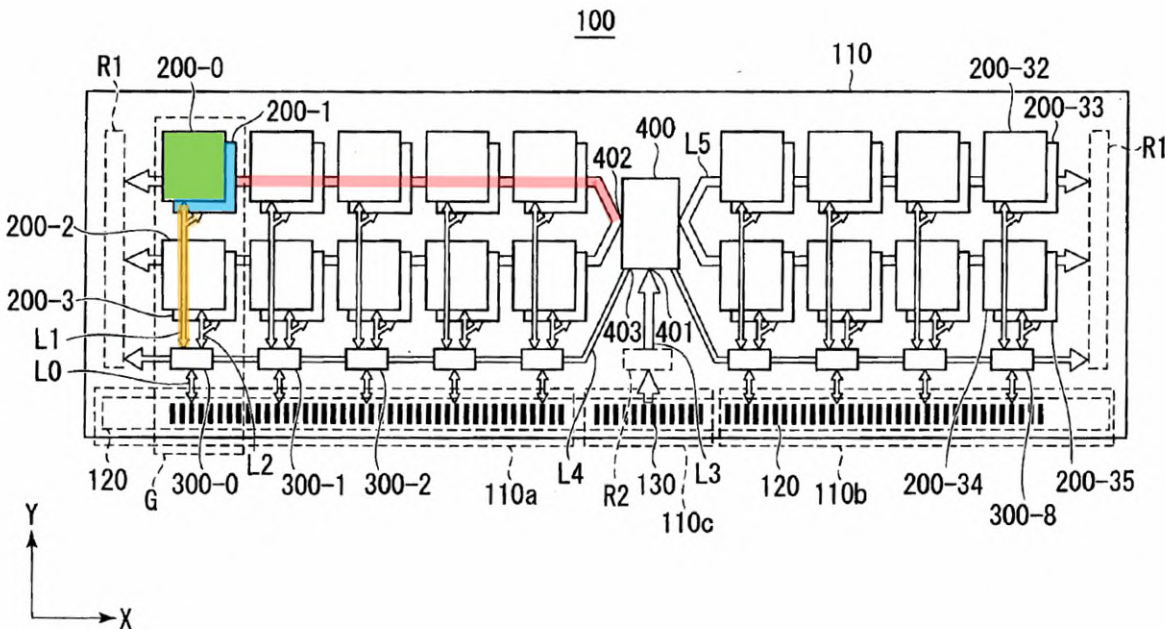


Fig. 11

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

The '506 Patent does not disclose any details about the physical arrangement of 4-bit memory devices on a memory module (e.g., the relative placement of lower and upper nibbles in a given rank), *see, e.g.*, EX1001 at Figs.2C and 2D, but a Skilled Artisan would know that different arrangements of 4-bit wide (i.e., “x4”) memory devices were possible. For example, the lower nibble of a given rank (e.g., DQ0-DQ3) could be placed on one side of the module, while the upper nibble of that rank (e.g., DQ4-DQ7) could be placed at the same location on the other side of the module. *See, e.g.*, EX1018 (JEDEC 21-C) at 4.20.4-8, -14, -31. A Skilled Artisan would also understand that 4-bit wide memory devices can be stacked on each other to reduce the amount of space taken on the printed circuit board of the memory module, and that different stacking arrangements would be possible. *See, e.g.*, EX1020 (JESD79-3C) at 6 (showing “Stacked” x4 memory devices). For example, instead of a single x8 memory device, a Skilled Artisan would understand it would be possible to stack two x4 memory devices that provide the lower and upper nibble of a given byte in a given rank, similar to a single x8 memory device. Alternatively, it would be possible to stack the lower nibbles of two ranks (e.g., ranks 0 and 1) on one side of the printed circuit board (e.g., at the location of the green box below) and to stack the upper nibbles of those two ranks (e.g., ranks 0 and 1) on the other side of the printed circuit board at the same horizontal and vertical location (e.g., at the location of the blue box below), with

the lower and upper nibble in a given rank (e.g., rank 0) receiving one chip-select signal, and the lower and upper nibble in the other rank (e.g., rank 1) receiving a different chip-select signal. *See, e.g.*, EX1020 (JESD79-3C) at 6; EX1018 (JEDEC 21-C) at 4.20.4-8, -9, -15, -21, -35; EX1007 (Ellsberry), [0051] & Figs. 6, 11. Either way, the result would be a pair of x4 memory devices, instead a single x8 memory device, in a given rank (e.g., rank 0) connected to the same data buffer (e.g., 300-0).



b) 3[b]: “wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and”

218. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. As explained above, when modified in view of the knowledge of a Skilled Artisan and/or Ellsberry to use pairs of 4-bit memory

devices instead of an 8-bit memory device, all of the memory devices 200 would be 4-bit memory devices, which would read 4-bit wide sections of data. *Supra* ¶¶ 213-216. A Skilled Artisan would thus understand that as modified “*each of the first section* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-0], *the second section* [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-8], *and the third section of the read data* [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] *is 4-bit wide.*”

c) 3[c] “wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:”

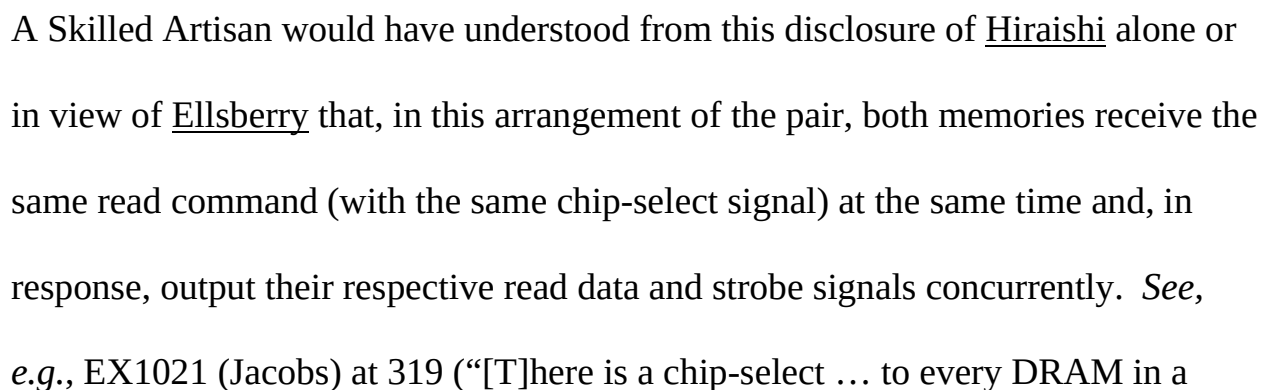
219. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. As explained above, when modified in view of the knowledge of a Skilled Artisan and/or Ellsberry to use pairs of 4-bit memory devices instead of an 8-bit memory device, the pair of 4-bit memory devices would connect to the same corresponding buffer as the prior 8-bit memory device (e.g., 300-0). *Supra* ¶¶ 213-216. Thus, a Skilled Artisan would understand that data register buffer 300-0 is the “*first data buffer ... coupled to the third memory device.*” As explained above for claim 1[e], the “*first data buffer* [e.g., data register buffer 300-0] ... *respon[ds] to the one or more of the module control signals.*” *Supra* ¶¶ 127-128.

d) 3[d]: “delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;”

220. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim 1[f]. See *supra* ¶¶ 129-130. The “*first data buffer*” [e.g., data register buffer circuit 300-0] would “*delay the third read strobe by a third predetermined amount to generate a third delayed read strobe*” in the same manner as described for the “*first read strobe*” above.

e) 3[e]: “sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and”

221. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim 1[g]. See *supra* ¶¶ 131-133. The “*first data buffer*” [e.g., data register buffer circuit 300-0] would “*sample the third section of the read data using the third delayed read strobe*” in the same manner as described for the “*first section of the read data*” above. Further and as illustrated by Ellsberry, a Skilled Artisan would understand that when a pair of 4-bit memory devices are used instead of an 8-bit memory device, the read data from the two 4-bit memory devices in the pair would be



rank (a separately addressable set of DRAMs.”), 413 (“[A] *rank* of memory is ... one or more DRAM devices that operate in lockstep in response to a given command.”); EX1007 (Ellsberry) Fig.11 (below, showing lower nibble (e.g., DQA(3:0)) and upper nibble (e.g., DQA(7:4)) receiving the same signals at the same time (e.g., ACA and CS0A)). Accordingly, the read data and strobe signals would arrive concurrently at the data buffer (blue) which would process the read data and strobe signals from the pair of memory devices concurrently, including “sampling” the respective section of the read data using the respective delayed strobe.

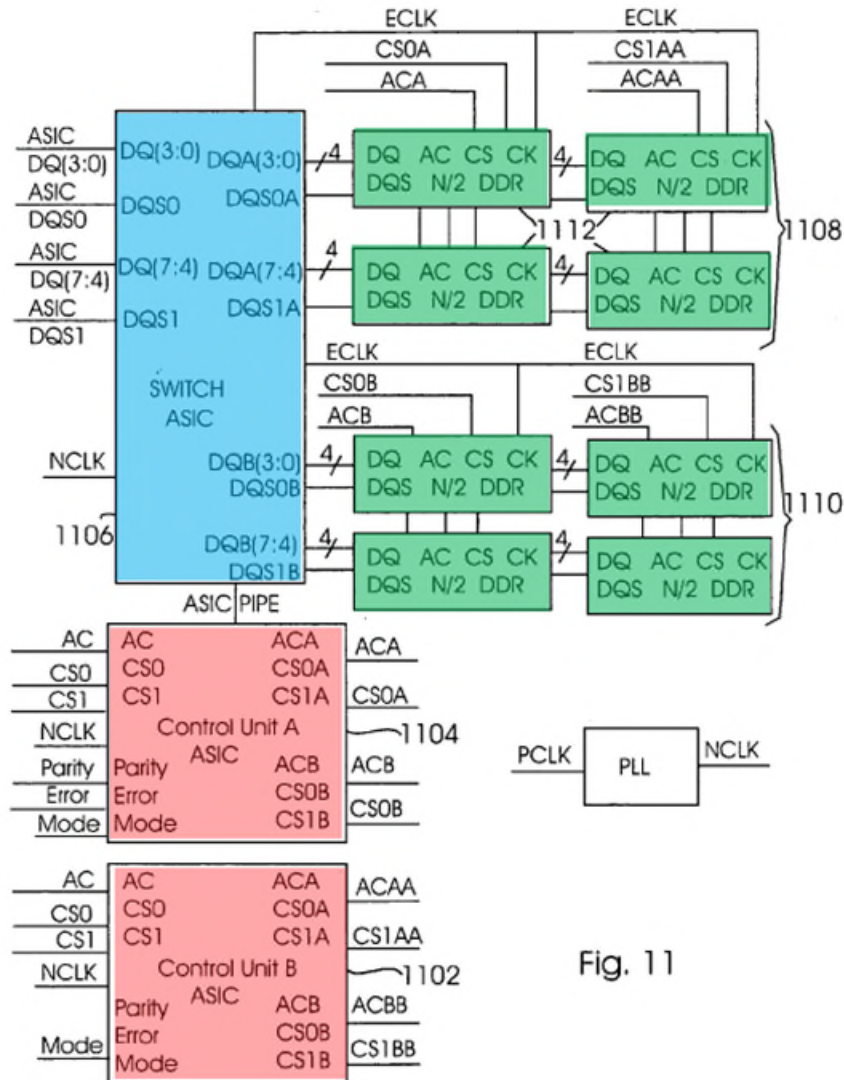


Fig. 11

222. Thus, Hiraishi alone or in view of Ellsberry would disclose that the “first data buffer” [e.g., data register buffer circuit 300-0] is configured to “sample the third section of the read data [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] using the third delayed read strobe concurrently with sampling the first section of the read data [e.g., lower nibble of the byte in rank 0 connected to data buffer 300-0] using the first delayed read strobe.”

223. To the extent one might argue that Hiraishi does not sample the read data using the delayed read strobe, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above in 1[g] for the “*first section of the read data*” it would have been obvious to a Skilled Artisan to utilize the sampling in Butt to sample the “*third section of the read data*” [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0]. See *supra* ¶¶133.

f) 3[f]: “transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;”

224. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. As explained for claim 1[h], Hiraishi discloses that the first data register buffer (300-0) can, “*transmit the first section of the read data to a first section of the data bus* [e.g., from buffer circuit 300-0 (blue) to the connectors 120 (yellow) connecting to the data line L0 (Fig. 1)].” *Supra* ¶¶ 134-135. For the same reasons, when Hiraishi is modified to use a pair of 4-bit memory devices instead of a single 8-bit memory device, the first data register buffer (300-0) can “*transmit the third section of the read data* [e.g., upper nibble of the byte in rank 0 connected to data buffer 300-0] *to a third section of the data bus* [e.g., the upper nibble from buffer circuit 300-0 (blue) to the connectors 120 (yellow) connecting to the data line L0 (Fig. 1)] *concurrently with transmitting the first section of the read data* [e.g., lower nibble of the byte in rank 0 connected to data

buffer 300-0] *to the first section of the data bus*” for the lower nibble of the data line L0. In particular, and as explained above and illustrated in Ellsberry, a Skilled Artisan would understand that data read in a single read operation from the two 4-bit memory devices would be transmitted to respective sections on the data bus concurrently.

g) 3[g]: “wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.”

225. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. An analogous determination for the “*first predetermined amount*” [e.g., the amount of delay imposed by data register buffer circuit 300-0] is described above for claim 1[i]. *See supra* ¶¶136-151. The “*third predetermined amount*” [e.g., the amount of delay for the upper nibble of the byte in rank 0 connected to data buffer 300-0] can be determined in a manner similar to the “*first predetermined amount*” [e.g., the amount of delay for the lower nibble of the byte in rank 0 connected to data buffer 300-0] addressed above. Thus, for the same reasons, Hiraishi discloses this limitation.

226. To the extent one might argue that Hiraishi does not determine the predetermined amount of delay based on signals received during one or more previous operations, this claim is rendered obvious by Hiraishi in further view of Butt. For the same reasons explained above in 1[i] for the “*first predetermined*

amount,” it would have been obvious to a Skilled Artisan to combine Butt with Hiraishi to determine the “third predetermined amount.” See supra ¶¶144-151.

2. Claim 5: “The memory module claim 2, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.”

227. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 2. Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. For example, as explained above, it would have been obvious to modify Hiraishi such that “*at least one respective memory device [200] in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.*” *Supra* ¶¶ 212-216. Further, where Hiraishi is modified to use pairs of 4-bit memory devices in place of single 8-bit devices—as illustrated by Ellsberry above—a Skilled Artisan would understand that “*each of the first section and the second section of the read data is 4-bit wide*” at least because this data would be output by 4-bit memory devices.

3. Claim 12: “The memory module of claim 1, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.”

228. Claim 12 overlaps with the requirements of claim 5 (*supra* ¶ 227). As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 1. For the same reasons explained above for Claim 5 (*supra* ¶ 227), Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry.

4. Claim 16

a) 16[a]: “The method of claim 15, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe,”

229. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 15. For the same reasons stated for claim 3[a], Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶ 217.

b) 16[b]: “the method further comprising, at the first data buffer, in response to the one or more of the module control signals:”

230. For the same reasons stated for claim 3[c], Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶ 219.

c) 16[c]: “delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;”

231. For the same reasons stated for claim 3[d], Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶ 220.

d) 16[d]: “sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and”

232. For the same reasons stated for claim 3[e], Hiraishi alone or in view of Butt further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶¶ 221-223.

e) 16[e]: “transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;”

233. For the same reasons stated for claim 3[f], Hiraishi further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶ 224.

f) 16[f]: “wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations.”

234. For the same reasons stated for claim 3[g], Hiraishi alone or in view of Butt further discloses or renders obvious this element, either alone or in further view of Ellsberry. *Supra* ¶¶ 225-226.

C. **Claims 8, 9, 10, 19, and 20 are Obvious Over Hiraishi alone or in view of Butt and further in view of Kim**

1. **Claim 8**

a) 8[a]: *“The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and”*

235. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 1 to a Skilled Artisan (under Patent Owner’s apparent claim interpretation). *Supra* ¶¶101-151. Hiraishi also discloses that “*the module control device [(command/address/control register 400)] is further configurable to receive a system clock signal [(CK/Clock-Pre in L3, purple)].*” EX1005 (Hiraishi) at [0108] (“In FIG. 7, a clock signal transferred through the command/address/control line L3 is represented by a clock signal Clock-Pre ...”), Fig. 7 (reproduced below, annotated, showing that the command/address/control register 400 is configurable to receive the system clock signal Clock-Pre through connectors 130).

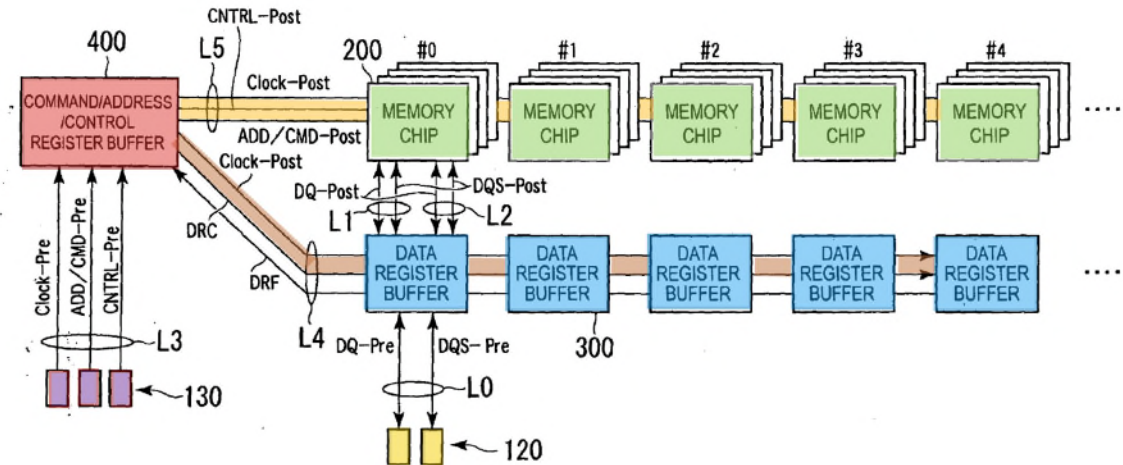


FIG. 7

See also *id.* at Fig. 6 (showing details of the command/address/control register 400, including a PLL circuit 420 for receiving the system clock, purple, through input terminal 401) and [0098] (“The PLL circuit 420 is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller 12 having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200.”).

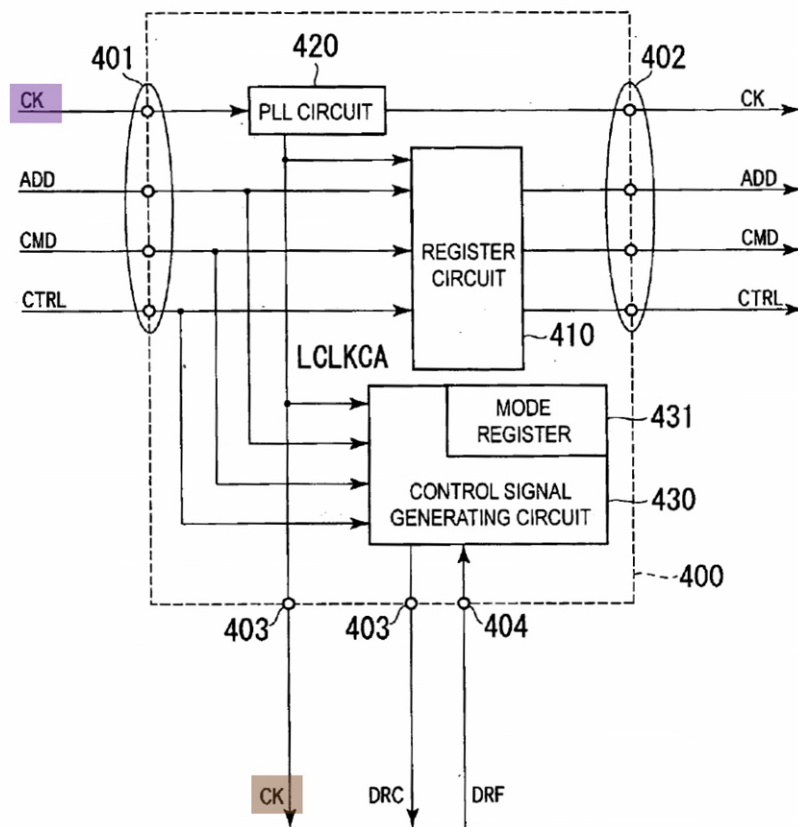


FIG.6

236. Therefore, Hiraishi discloses that “the module control device is further configurable to receive a system clock signal,”

b) 8[b]: “output a module clock signal together with the module control signals to the data buffers, and”

237. Hiraishi also discloses that “the module control device [(command/address/control register 400)] is further configurable to ... output a module clock signal [(CK/Clock-Post in L4, brown)] together with the module control signals [(DRC in L4, brown)] to the data buffers [(Data Register Buffers 300, blue)].” EX1005 (Hiraishi) at [0108] (“The clock signal CK to be supplied to

the memory chip 200 and the data register buffer 300 is supplied from the command/address/control register buffer 400.”), Fig. 7 (reproduced below, annotated, showing that the command/address/control register 400 is configurable to output a module clock signal Clock-Post together with the module control signal DRC in bus L4).

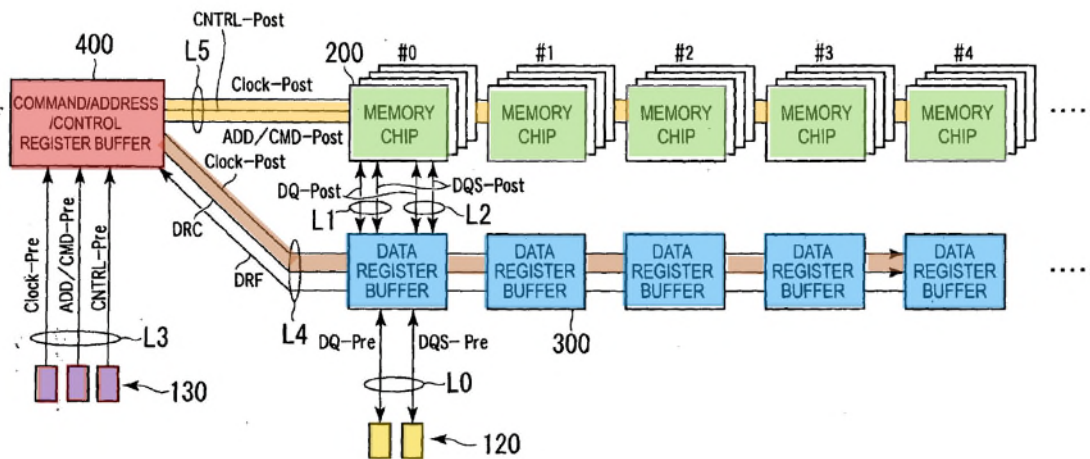


FIG. 7

See also *id.* at Fig. 6 (showing details of the command/address/control register 400, including a PLL circuit 420 for outputting a module clock signal, brown, together with the module control signal DRC through output terminal 403) and [0098] (“The PLL circuit 420 is a circuit that generates the internal clock LCLKCA based on the clock signal CK supplied from the memory controller 12 having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200.”). Hiraishi also explains that the operation of the circuit that

generates the module control signals DRC is synchronized with the same clock (LCLKA) which is output to the data register buffers. *Id.* at [0099] (“The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403.”).

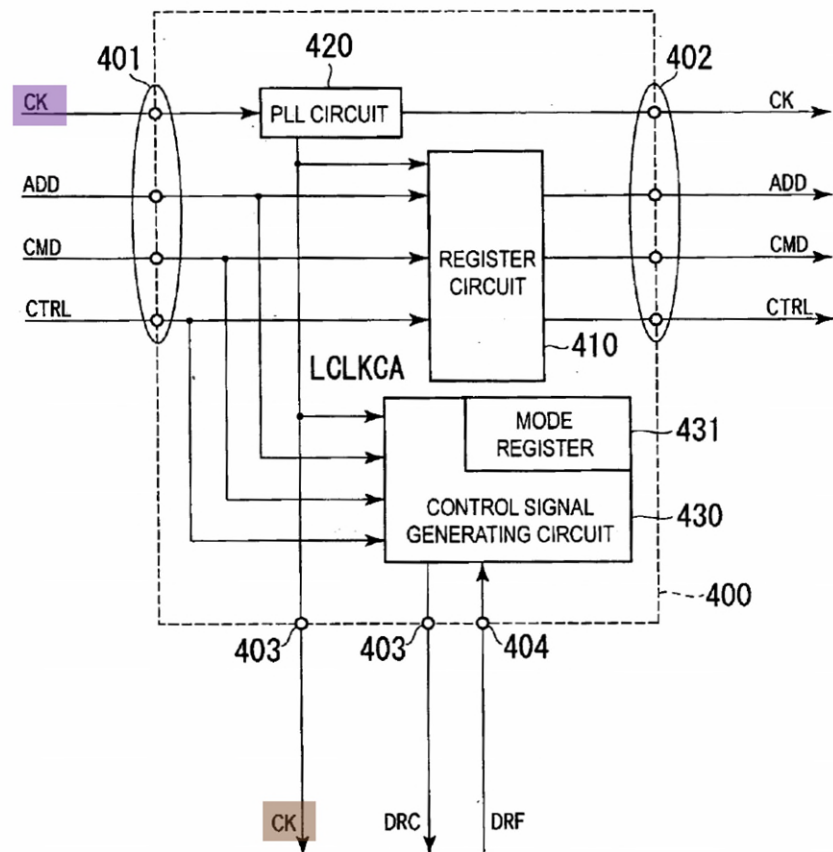


FIG.6

A Skilled Artisan would have understood that “*module clock signal*” is output “*together with the module control signals*” because they are output at the output terminal 403 and the generation of the module control signals is synchronized by the same clock signal (LCLKCA).

238. Therefore, Hiraishi discloses that “*the module control device is further configurable to ... output a module clock signal together with the module control signals to the data buffers.*”

c) 8[c]: “wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.”

239. Hiraishi discloses or renders obvious this element, either alone or in view of Butt and/or in further view of Kim. For example, as illustrated by annotated Figure 5 of Hiraishi below, Hiraishi discloses that “*the first data buffer further includes receiver circuits [in DLL circuit 310 and Data Register Control circuit 320] corresponding to respective ones of the module control signals [e.g., the signals in control signal DRC],*” and at least renders obvious “*a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition [such as a metastability condition in capturing*

signal values] in the respective module control signals [e.g., the signals in control signal DRC] with respect to the module clock signal [CK].”

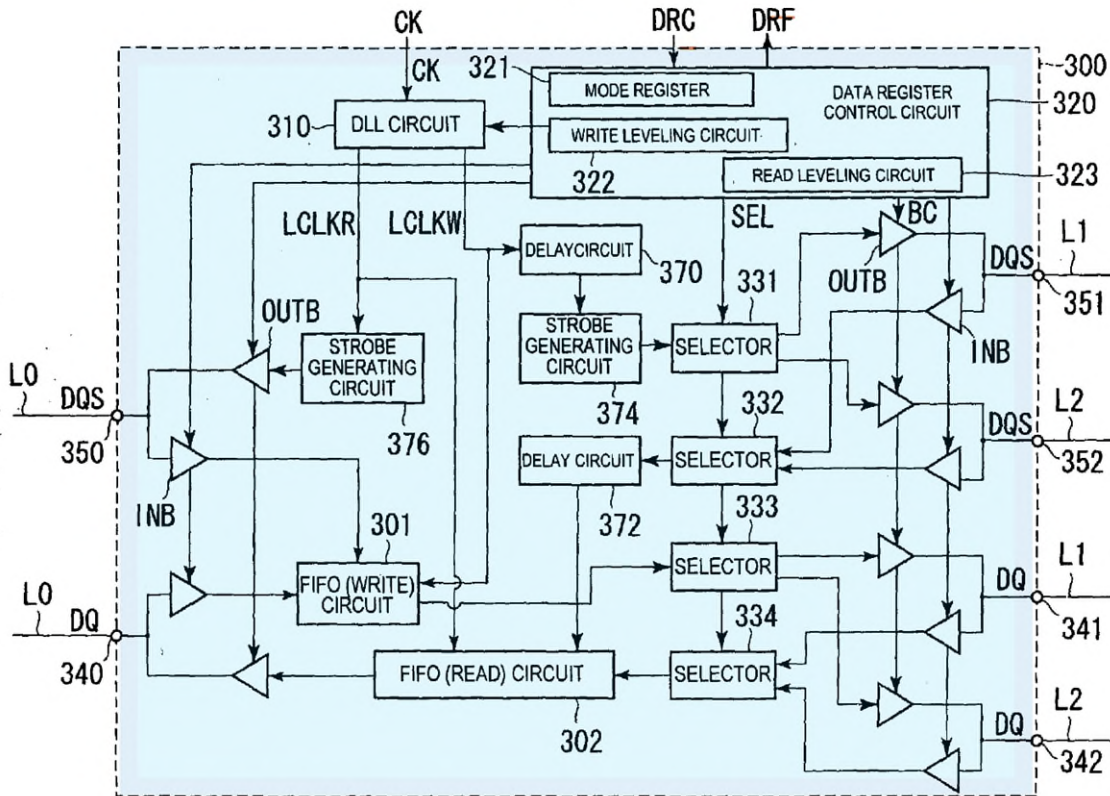


FIG. 5

EX1005 (Hiraishi), Fig. 5 (annotated).

240. As discussed above with reference to claim elements 8[a] and 8[b], Hiraishi discloses that the control signal DRC and the corresponding clock CK are transmitted on control line L4 to multiple Data Register Buffers. *Id.* Fig. 7 (reproduced above), ¶¶ 235-238. Hiraishi also discloses that the DLL circuit 310 in the data buffer receives the module clock signal CK and generates from the received clock signal CK a number of internal clocks, including LCLKR and

LCLKW, with fine phase adjustments that are used for the internal operation of the data buffer. *See, e.g.*, EX1005 (Hiraishi) at [0087] (“The DLL circuit 310 is a circuit that generates the internal clocks LCLKW and LCLKR based on the clock signal CK that is supplied from the command/address/control register buffer 400, having the same circuit configuration and function as that of the DLL circuit 212 provided in the memory chip 200.”), FIG. 5 (reproduced above); *see also id.* at [0074] (“The DLL circuit 212 takes a role of generating an internal clock LCLK and supplying the internal clock LCLK to a data input/output circuit 213 and a data strobe signal input/output circuit 214. The internal clock LCLK is a signal that is phase-controlled with respect to the clock signal CK, of which a phase is slightly advanced with respect to the clock signal CK such that phases of read data DQ and a data strobe signal DQS match with a phase of the clock signal CK.”). Hiraishi further discloses that the DRC signal is captured by the Data Register Control Circuit 320. *Id.* at [0088] (“The data register control circuit 320 is a circuit that controls the operation of the data register buffer 300 based on a control signal DRC that is supplied from the command/address/control register buffer 400.”)

241. A Skilled Artisan would have understood from this disclosure that DLL circuit 310 generates the internal clock that is used to capture the DRC signal based on the received clock signal CK. A Skilled Artisan would have also understood, and at least would have been motivated, to use the DLL circuit of

Hiraishi to generate that internal clock from the received module clock signal CK with a specific phase relative to the DRC signals to avoid metastability. For example, a Skilled Artisan would have understood the importance of the control information conveyed by the DRC signal which may not be correctly captured (thus causing malfunction) if there is a metastability condition at the reception of the DRC and CK signals. EX1008 (Kim) at 1:21-31 (“Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output generation.”). A Skilled Artisan would have understood that such metastability may happen in Hiraishi when the received clock and DRC signals are captured by the DLL and register control circuit with an incorrect alignment in time. *See, e.g.*, EX1027 (US 5,036,221, “Brucculeri”) at 2:53-56 (“In FIG. 2, active edge 26 of system clock signal 20 is shown to occur during the setup time t_{su} associated with data signal 18. When this occurs, the output signal along output line 16 may be metastable or invalid.”); EX1028 (US 6,906,555, “Ma”) at 1:36-46 (“... FIG. 2 illustrates the D flip flop setup and hold times. If the data input is not stable during the setup and hold time, a condition known as a setup and hold violation, the flip flop may go into a metastable state and the data output will not be a 1 or a 0 as desired.”). Indeed, due to the high speed at which the memory devices operated at

the time, a Skilled Artisan would have understood that the “use of the DLL circuit is substantially essential.” EX1005 (Hiraishi), [0163].

242. In light of the possibility of erroneous DRC signal reading, it would have been at least obvious to a Skilled Artisan to have the DLL circuit 310 and Data Register Control Circuit 320 include the functionality of a known metastability condition detector (such as taught by Kim, EX1008) and implement the DLL circuit 310 and Data Register Control Circuit 320 to avoid such potential metastability, including adjusting the phase of the internal clock signal and/or the phase of the DRC signal (similar to how Hiraishi’s DLL circuit adjusts the LCLKW signal’s phase). A Skilled Artisan would have understood that such a metastability condition detector can be used, e.g., during initialization, to indicate the presence of a metastability condition so that the phases of the internal clock and the DRC signals can be adjusted to avoid the metastability condition (and corresponding malfunction).

243. To the extent one might argue that Hiraishi’s disclosure alone does not sufficiently disclose or render obvious a metastability detection circuit as claimed, U.S. Patent No. 6,184,701 to Kim (“Kim”) (EX1008) discloses such circuitry. Kim is analogous art to Hiraishi, since each is directed to solving the problem of reliable communication between integrated circuits, including between Hiraishi’s command/address/control register buffer 400 and data buffers 300. *See*,

e.g., EX1008 at 1:12-14 (“The present invention relates to integrated circuit devices, and more particularly to integrated circuit devices which may be prone to generating metastable output signals.”). For example, Kim teaches that, when a circuit “receives input signals at similar analog levels [it] may be prone to generating an output signal in a metastable state (*i.e.*, where the potential of the output signal is greater than a maximum logic 0 level (VJL) and less than a minimum logic 1 level (VJH)). Such generation of metastable outputs may result in device failure if devices that are responsive to the output signal interpret the state of the output signal incorrectly. Accordingly, there is a need to develop circuits having less susceptibility to metastable output generation.” EX1008 at 1:21-31. To solve that metastability problem, Kim discloses “a metastability detection/prevention circuit 20” to be incorporated with any “main active circuit 10” in need thereof, including “a data input buffer.” EX1008 at 2:23-37.

244. It would have been obvious to a Skilled Artisan to combine the functionality of Kim’s metastability detection circuitry with the DRC inputs in Hiraishi’s data register buffers. A Skilled Artisan would have been motivated to make the combination in order to obtain more reliable communication by avoiding metastability at the input of the clock and DRC signals. Indeed, a Skilled Artisan would have understood that the DRC signals carry important control information. EX1005 (Hiraishi), [0100] (“The control signal DRC includes signals such as a

signal indicating a direction of transmitting and receiving data, a signal for controlling an ODT timing at the data line L0 side of the data register buffer 300, a signal for controlling an ODT timing at the data lines L1 and L2 side, a signal for controlling on and off of the DLL circuit, a signal for controlling enable and disable of the data register buffer 300, and a signal for performing a mode switching of the data register buffer 300 and a mode register set and the like.”).

245. In particular, as discussed above, a Skilled Artisan would have understood that metastability can be avoided by adjusting the phases of the internal clock and the DRC signal to properly latch the control signal value in the input buffer. *See, e.g.*, EX1030 (Zumkehr) at Fig. 2A and 1:33-35 (“The DQS signal 110 must be delayed relative to the DQ signal 120 to capture the data DQ 120 when it is valid and stable.”). Furthermore, Hiraishi already teaches that its DLL circuit 310 can perform fine phase adjustments, such as those used for the LCLKW internal clock signal. EX1005 at [0087]. In addition, a Skilled Artisan would have understood that either or both of the clock and DRC signals can be delayed as required for the proper capture of the data values. EX1016 (Nimaiyar) at [0021-22] (“The clock and data signals 410 and 420 may optionally be delayed via the delay lines 312 and 372 of FIG. 3, respectively. The settings of the delay lines 312 and 372 may be such that the active transitions in a delayed clock signal 430 occur within a valid data time, such as approximately in the center of the eye of, a

delayed data signal 440.”). Accordingly, making the combination of implementing Kim’s metastability detection functionality in Hiraishi’s data register buffer would have been well within the level of skill at the time and provided nothing more than expected from the prior art: detecting metastability at the clock and DRC inputs and removing the metastability, including adjusting the phase of the clock and DRC signals.

246. Furthermore, a Skilled Artisan would have understood that, in order to detect a metastability condition and make a corresponding adjustment, the metastability detection circuit “*generate[s] one or more metastability indicators.*” For example, Kim discloses that, “[i]f the output signal has been in a metastable state for a duration in excess of the transition duration, then the metastability detection/prevention circuit will generate a control signal at a designated logic level.” EX1008 at Abstract; *see also* EX1028 (Ma) at Fig. 8 and 8:25-27 (“The “Clock” and “Clock_Invert” signals overlap the “Change_Detected” pulse to generate the “Bad_News” pulse.”). A Skilled Artisan would have understood that such an output indicates the presence of a metastable states, thus it includes “*one or more metastability indicators.*”

247. Accordingly, Hiraishi alone or in combination with Kim discloses to a Skilled Artisan that “*the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective*

receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.”

2. Claim 9

a) 9[a]: “The memory module of claim 8, where-in the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and”

248. As explained above, Hiraishi alone or in view of Butt and/or Kim discloses to a Skilled Artisan each and every limitation of claim 8. Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. For example, Hiraishi discloses that “*the metastability detection circuit [including DLL circuit 310 and Data Register Control Circuit 320] is further configurable to generate at least one delayed version of the module clock signal [an internal clock phase delayed to lag relative to the received clock], and at least one delayed version of the respective module control signal [a delayed DRC, so that the phase of clock signal CK moves forward relative to the delayed DRC].”*

249. As discussed above, a Skilled Artisan would have understood that Hiraishi’s DLL circuit 310 and data register control circuit 320 adjust the relative phase of the internal clock signal and the DRC signal to correctly capture the DRC

signal values. A Skilled Artisan would have also understood that the phase of the received clock signal CK can be early or late relative to the phase of the received DRC signal, so that either the clock signal (CK, dashed orange, below) or the DRC signal (solid orange, below) can be delayed (with delay lines, red, below) in order to avoid metastability. EX1016 (Nimaiyar) at Fig. 3 (reproduced below in part, annotated, showing optional delay lines 372 and 312 for data and clock signals, respectively), *see also id.* at [0022] (“The settings of the delay lines 312 and 372 may be such that the active transitions in a delayed clock signal 430 occur within a valid data time, such as approximately in the center of the eye of, a delayed data signal 440.”).

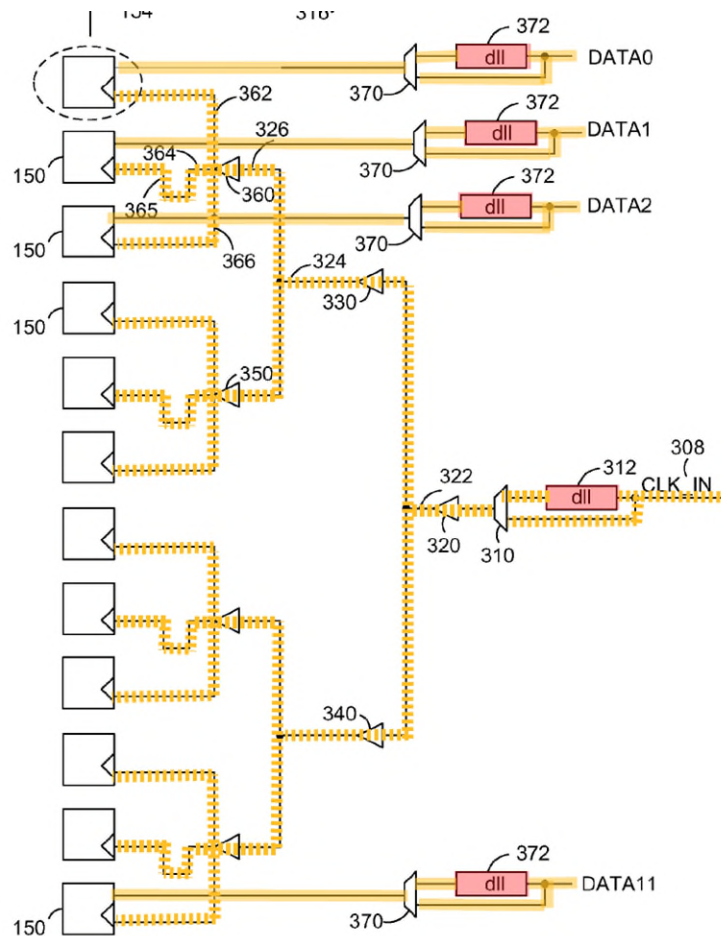


FIG. 3

250. Accordingly, a Skilled Artisan would have understood that if the clock signal is early, the phase of the clock signal can be delayed in order to capture the data properly (similar to delaying the strobe signal to capture the eye of the read data, *see, e.g., Zumkehr* (EX1030) at Figs. 2A and 2B). Conversely, if the clock signal is late, a Skilled Artisan would have understood that the phase of the DRC signal can be delayed to capture the data properly with the phase of the clock signal CK. *See, e.g., EX1016 (Nimaiyar)* at Fig. 3 (reproduced above in part, annotated, showing optional delays 372 and 312, red, for data, solid orange, and

clock, dashed orange, signals, respectively), & [0021-22] (“The clock and data signals 410 and 420 may optionally be delayed via the delay lines 312 and 372 of FIG. 3, respectively. The settings of the delay lines 312 and 372 may be such that the active transitions in a delayed clock signal 430 occur within a valid data time, such as approximately in the center of the eye of, a delayed data signal 440.”).

Since a Skilled Artisan would have understood that both of these possibilities may happen depending on the circumstances, she would have been motivated to generate both a delayed clock signal (in case the clock is early) and a delayed control signal DRC (in case the clock is late) and select the one which removes the metastability condition. *Id.* at Fig. 3 (reproduced above in part, annotated, showing multiplexers 370 and 310 to select the data and clock signals with or without delays) and [0018] (“A multiplexer 310 may be used to programmably direct reception by the driver 320 of one of the clock signal 308 or a replicated version of the clock signal 308, perhaps delayed via a delay line 312.”); *see also* EX1028 (Ma) at Fig. 4 (reproduced below, showing specific metastability detection circuitry including delay elements to delay both the clock and data signals).

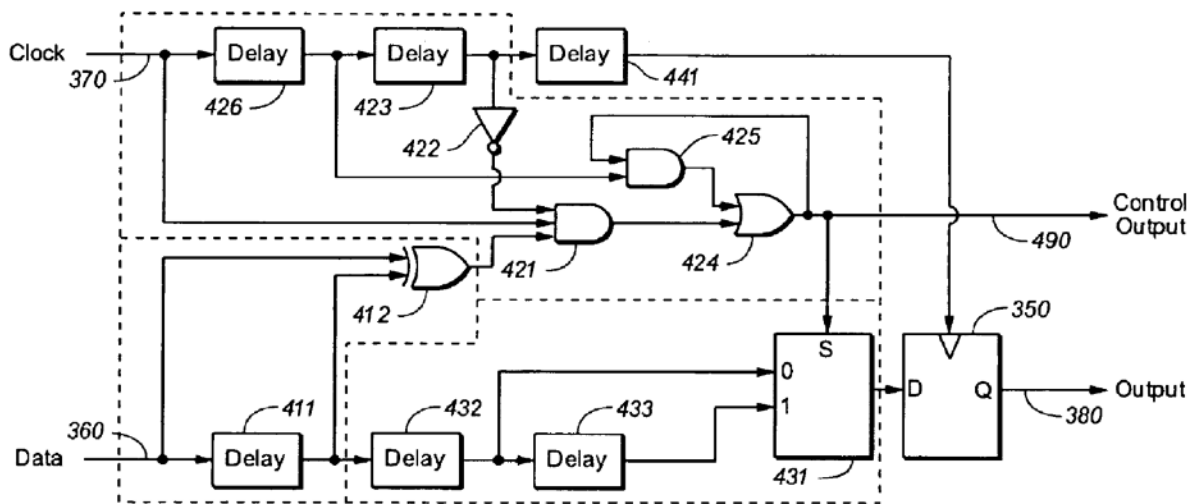


FIG. 4

251. Delaying the clock signal and the DRC control signal was well within the level of skill at the time as evidenced by Hiraishi (generating phase adjusted internal clocks), as well as Butt and Zumkehr (describing delaying strobe signals), and Nimaiyar (using delay lines 312 and 372 to delay clock and data signals) and Ma (delaying data and clock signals in metastability preventing circuitry).

Therefore, a Skilled Artisan would have been motivated to implement the functionality of Kim's metastability detection together with delaying elements for both the clock and DRC signals in order to avoid metastability and to capture the DRC signal values properly, as evidenced, e.g., by Nimaiyar (EX1016) and Ma (EX1028). Thus, it would have been obvious to a Skilled artisan *"to generate at least one delayed version of the module clock signal, and at least one delayed*

version of the respective module control signal” in order to detect metastability and prepare for the cases when the clock signal is early or late.

252. Accordingly, it would have been at least obvious to a Skilled Artisan that *“the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal.”*

b) 9[b]: “wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and”

253. Hiraishi discloses or renders obvious this element to a Skilled Artisan, either alone or in further view of Kim. For example, as discussed above with reference to claim element 9[a], it would have been obvious to a Skilled Artisan to detect and prepare for both an early and a late clock signal CK relative to the data eye. *Supra* at ¶¶248-252. A Skilled Artisan would have also understood that an early clock CK can be properly delayed to latch the DRC signal, and a late clock CK can be used to latch a properly delayed DRC signal. *Id.* And, of course, there is a possibility that both the clock signal and the DRC signal are received with the proper phase, so the received clock signal can be used to properly sample the received DRC signal without any delay. Accordingly, a Skilled Artisan would have been motivated to use a signal selection circuit to select either the received clock signal CK (in case it was late or on time) or the delayed clock (in case the received

clock was early). EX1016 (Nimaiyar) at Fig. 3 (reproduced above in part, annotated, showing multiplexers 310 and 370 to select delayed or non-delayed clock and data signals to capture the proper data values) & [0020-22], [0018] (“A multiplexer 310 may be used to programmably direct reception by the driver 320 of one of the clock signal 308 or a replicated version of the clock signal 308, perhaps delayed via a delay line 312.”).

254. Therefore, it would have been at least obvious to a Skilled Artisan that *“the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal.”*

c) [9c] to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

255. Hiraishi discloses or renders obvious this element to a Skilled Artisan, either alone or in further view of Kim for the reasons discussed above with reference to claim elements [9a] and [9b]. *Supra* ¶¶248-254. For example, a Skilled Artisan would have understood that, if the one or more metastability indicators, like those in Kim and/or Ma, indicate no metastability when receiving the module clock signal and its phase is such that it can be used to capture the DRC signal values, the selection circuit would select the module clock signal to capture the

DRC signal values. *See, e.g.,* Nimaiyar (EX1016) at [0018] & Fig. 3 (explaining the optional delays 312 of clock signals and their selection by multiplexers 310). And if the one or more metastability indicators, like those in Kim and/or Ma, indicate no metastability when the *delayed* module clock signal is used to capture the DRC signal values, the selection circuit would select the delayed module clock signal to capture the DRC signal values. *Id.*

256. Therefore, it would have been at least obvious to a Skilled Artisan “to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.”

3. Claim 10

a) 10[a]: “The memory module of claim 9, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and”

257. As explained above, Hiraishi alone or in view of Butt and/or Kim discloses to a Skilled Artisan each and every limitation of claim 9. Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. For the reasons discussed above with reference to claims 8 and 9, a Skilled Artisan would have been motivated to implement the metastability detection functionality of Kim in the DLL and data register control circuits 310 and 320 of Hirashi. *See*

supra ¶¶ 243-256. As also discussed above, a Skilled Artisan would have understood that, in order to properly capture the DRC signal values, e.g., in case the clock signal is late, the DRC signal may be optionally delayed. *See, e.g.*, EX1016 (Nimaiyar) at [0021-22] & Fig. 3 (reproduced above in part, *supra* ¶249, annotated with optional delays 372 of data signals and their selection by multiplexers 370); *see also* EX1028 (Ma) at Fig. 4 (reproduced above, *supra* ¶ 250, showing multiplexer 431 selecting data with and without delay 433 to avoid metastability) & 7:35-39 (“Delay element 433 needs to provide, at a minimum, sufficient delay to equal the setup plus the hold time of the flip flop 350. This will ensure that any changes in the data signal 360 which caused the selection of an alternate signal will be displaced by the delay amount.”). Therefore, a Skilled Artisan would have been motivated to have a selection circuit to receive the DRC signal and a delayed version of the DRC signal and select the one which can avoid the metastability. *Id.*

258. Therefore, it would have been at least obvious to a Skilled Artisan that *“the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal.”*

b) 10[b]: “to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and”

259. Hiraishi discloses or renders obvious this element, either alone or in further view of Kim. For the reasons discussed above with reference to claim element 10[a], a Skilled Artisan would have been motivated to select either the DRC signal or the delayed DRC signal in order to properly capture the DRC signal values. *See supra* ¶ 257. As discussed above, a Skilled Artisan would have been motivated to implement the *functionality* of Kim’s metastability detection circuit in Hiraishi’s data register controller 320 to detect metastability in the received DRC signal, and to use such a metastability detection to delay the DRC signal such that its value can be safely captured. Kim (EX1008) at Abstract (“The metastability detection/prevention circuit performs the function of detecting whether an output of the main active circuit has been disposed in a metastable state for a duration in excess of a transition duration.”). A Skilled Artisan would have understood that the details of implementing the metastability circuitry can vary, and can include delay elements for both the data and the clock signals. *See, e.g.*, EX1028 (Ma) at Fig. 4 (reproduced above, *supra* ¶ 250). As further discussed above, a Skilled Artisan would have understood that the received clock signal can be early or late and, accordingly, the clock or the DRC signal can be delayed. *See, e.g.*, EX1016

(Nimaiyer) at Fig. 3 (reproduced above in part, annotated, *supra* ¶249). Thus, a Skilled Artisan would have understood, and have been motivated, to use a metastability detection circuitry which provides both a “*first metastability indicator*” to detect whether the clock needs to be delayed and “*a second metastability indicator*” to detect whether the data needs to be delayed, and make the selection of delaying the clock or the data based on these metastability indicators. *Id.* For example, as also discussed above with respect to Hirashi and Butt, a Skilled Artisan would have understood that latching predefined data with different relative phases can be used to identify which combination of delayed clocks and/or data captures the data properly. *Supra* at ¶¶136-151. Thus, a “*first metastability indicator*” would indicate whether the predefined data is correctly captured with delayed clock (“*to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator*”), and “*a second metastability indicator*” would indicate whether the data is correctly captured with delayed data (“*select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator*”). See, e.g., EX1016 (Nimaiyer) at Fig. 3 (reproduced above in part, *supra* ¶249 showing separate multiplexers 370 and 310 to select, optionally, delayed data or delayed clock and corresponding data buffers

150 to capture the corresponding data in accordance with the selected clock signal).

260. Therefore, it would have been at least obvious to a Skilled Artisan “to select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators.”

c) 10[c]: “wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.”

261. Hiraishi discloses or renders obvious this element to a Skilled Artisan, either alone or in further view of Kim. As discussed above with reference to claims 8 and 9 and claim elements 10[a] and 10[b], a Skilled Artisan would have been motivated to implement Kim’s metastability detection functionality in Hirashi’s data register to detect metastability when inputting the DRC signal and the corresponding CK clock signal. As also discussed above, a Skilled Artisan would have understood that, to avoid the metastability and properly capture the DRC signal values, the clock signal CK and/or the control signal DRC can be delayed. See, e.g., EX1016 (Nimaiyar) at Fig. 3 (reproduced above in part, annotated, *supra* ¶249, showing optional delay circuits 312 and 372 and corresponding multiplexers

310 and 370 to select the clock and data signals or their delayed versions) & [0021-22] (“The settings of the delay lines 312 and 372 may be such that the active transitions in a delayed clock signal 430 occur within a valid data time, such as approximately in the center of the eye of, a delayed data signal 440.”). A Skilled Artisan would have also understood that, after the proper selection, the DRC signal values can be captured by circuitry, such as a register, that samples the selected version of the DRC signal according to the selected version of the clock signal. *Id.* (e.g., Fig. 3 showing that the clock signal selected by multiplexer 310 is used to clock the data signal selected by multiplexer 370 into registers 150). A Skilled Artisan would have further understood how to properly select the versions of the DRC and CK signals as inputs to the register so that the register outputs the correct values of the DRC signal. *See, e.g.,* EX1030 (Zumkehr) at Figs 2A and 2B (disclosing how to sample the data signal with appropriate delays to avoid registering incorrect data values).

262. Therefore, it would have been at least obvious to a Skilled Artisan that *“the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.”*

4. Claim 19

a) 19[a]: “The method of claim 14, further comprising: receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;”

263. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 14. *Supra* ¶¶ 179-194. For the same reasons stated for claim 18[b], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 205.

b) 19[b] “outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;”

264. For the same reasons stated for claim 18[c], Hiraishi further discloses or renders obvious this element. *Supra* ¶ 206.

c) 19[c] “generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.”

265. For the same reasons stated for claim 8[c], Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. *Supra* ¶¶ 239-247.

5. Claim 20

a) 20[a] “The method of claim 19, further comprising, at the first data buffer: generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;”

266. As explained above, Hiraishi alone or in view of Butt discloses each and every limitation of claim 19, either alone or in further view of Kim. For the same reasons stated for claim 9[a], Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. *Supra* ¶¶ 248-252.

b) 20[b] “selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;”

267. For the same reasons stated for claim 9[c], Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. *Supra* ¶¶ 255-256.

c) 20[c] “selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and”

268. For the same reasons stated for claim 10[b], Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. *Supra* ¶¶ 259-260.

d) 20[d] “sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.”

269. For the same reasons stated for claim 10[c], Hiraishi further discloses or renders obvious this element, either alone or in further view of Kim. *Supra* ¶¶ 261-262.

D. Claims 1-20 are Obvious Over Hiraishi and Butt in view of Tokuhiko and/or in further view of Ellsberry and/or Kim

270. As explained above, the '506 Patent discloses a “*previous operation*” (e.g., write) that is in a different direction than the later “*operation*” (e.g., read). *See supra* ¶¶ 43-44, 99-100. Under this claim interpretation, which is narrower than Netlist’s interpretation addressed in the sections above, claims 1-20 are obvious in light of Hiraishi alone or with Butt in view of Tokuhiko (or in further view of Ellsberry and/or Kim) as explained below.

1. Tokuhiko’s teaching

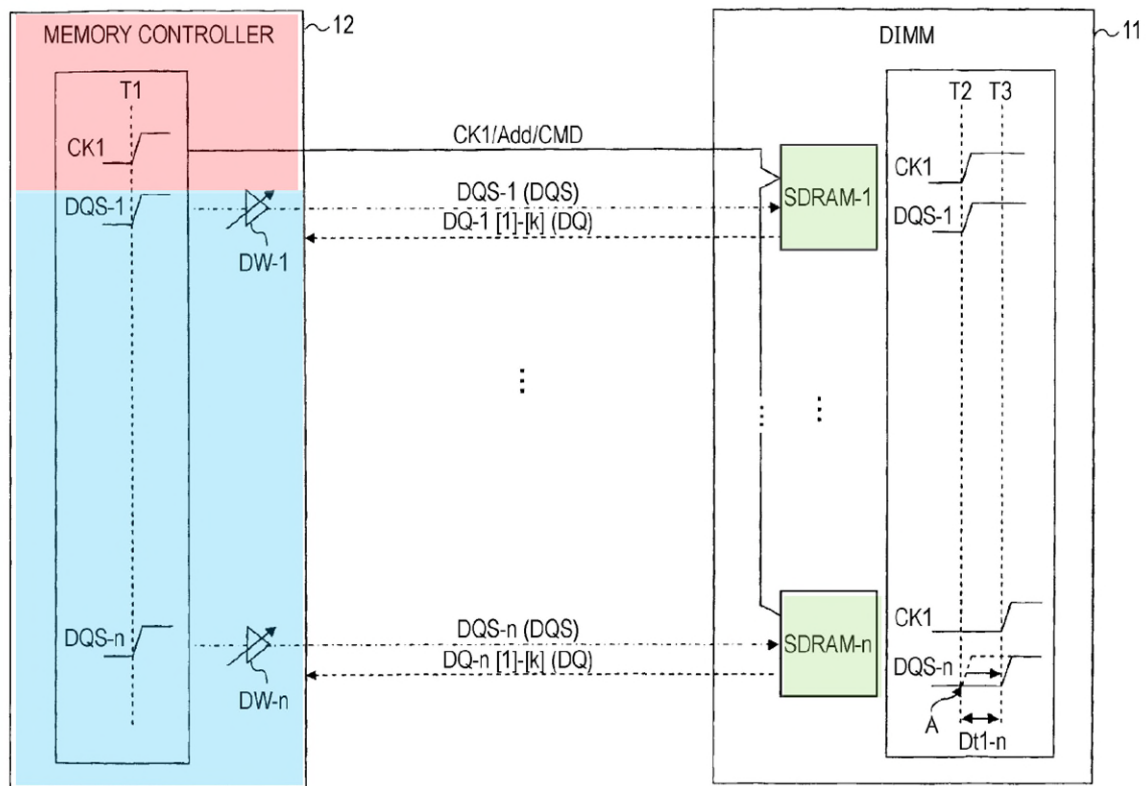
271. Tokuhiko teaches that a DDR3 memory interface employs fly-by topology for connection between a memory controller and a DIMM (Dual Inline Memory Module). EX1006 (Tokuhiko), 1:22-33. The JEDEC standards specify how to adjust timing in the fly-by configuration for write data, but do not specify a mechanism to adjust the fly-by delays of the read data. *See* EX1006 (Tokuhiko), 2:54-59 (“Although, the DDR3 memory interface compensates the arrival time when the data strobe signals DQS-1 to DQS-n arrive at the SDRAMs 92-1 to 92-n

in the write operations according to the JEDEC standards as described above, compensations of the signal arrival time in read operations are not provided with the JEDEC standards.”). Tokuhiro further explains that, with increasing speed of memories, such fly-by delays of the read data “will become greater than a typical data period of the DDR3 memory interface ... so that the delay may affect in reading data.” *Id.*, 3:9-12. Thus, Tokuhiro teaches to a Skilled Artisan that fly-by delays need to be compensated for read data and not just for write data, and problems arise if the fly-by delay in read operations exceeds the clock period. Tokuhiro teaches techniques to solve this problem of inputting read data with large fly-by delays in a simple way using read delay units “without providing a special mechanism, such as an FIFO,” where the read delays are obtained from the timing for write operations. *See, e.g., id.*, 3:16-26, 18:66-19:7 (“Also, with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.”).

272. In particular, Tokuhiro proposes delaying the transmission of the read data to compensate for those fly-by delays before the read data enters the common clock domain of the receiver. To implement these delays, Tokuhiro discloses “a ***second variable delay unit*** for delaying, in the ***read operation***, a data signal input from the memory ***by a second delay time***.” *Id.*, 3:16-26. Tokuhiro also teaches that, for the read operation, the “***second delay time ... is set based on the first delay time***” which is determined using “a ***first variable delay unit for delaying***, in the ***write operation***, a data strobe signal output to the memory ***by a first delay time*** that is set by utilizing the write leveling function.” *Id.*

273. Tokuhiro’s embodiments are described in connection with unbuffered DIMMS where the memory controller (12) directly interfaces with the memory devices. *See, e.g.*, EX1006 (Tokuhiro), Fig. 7. For example, as illustrated in Tokuhiro’s Fig. 7, the memory controller 12 directly controls the write leveling operation between the memory controller and the memory chips:

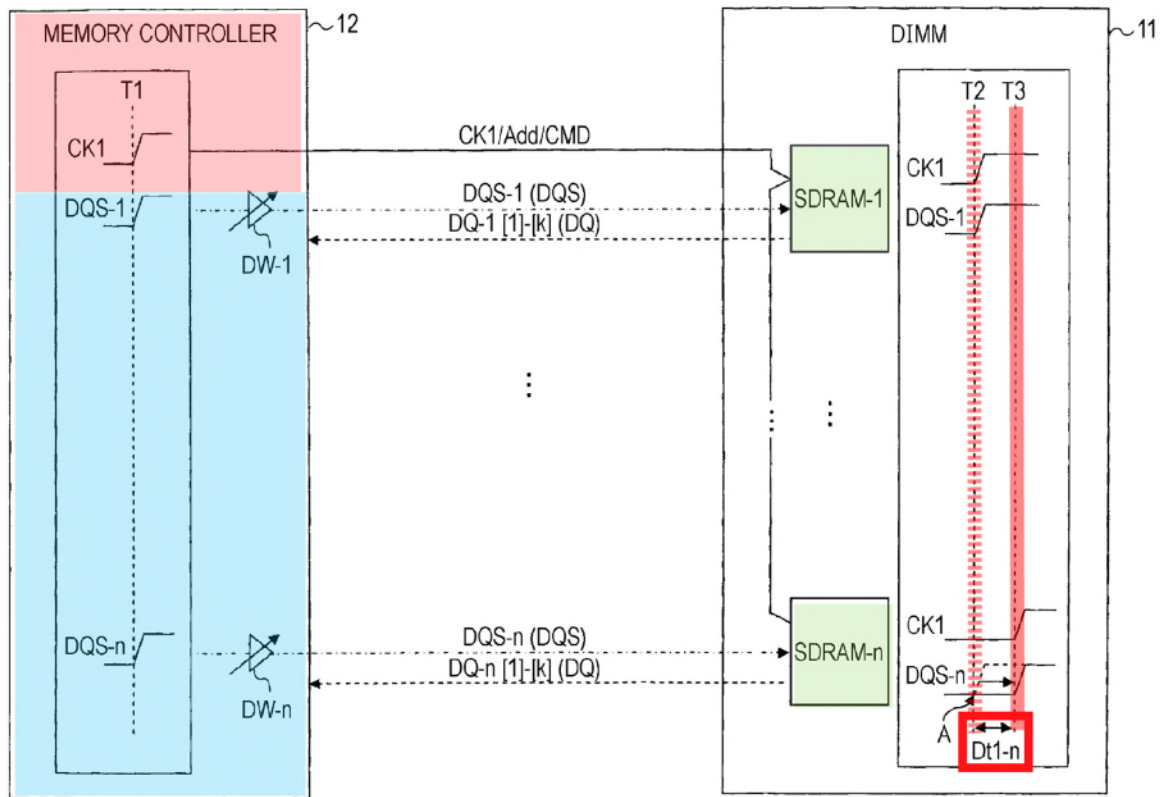
FIG. 7



274. Tokuhiro's FIG. 7 shows that, inside the memory controller (on the left side of the figure), the clock (CK1) and strobe (DQS-1, ..., DQS-n) signals are all initially in sync, i.e., transitioning at the same time (T1). *Id.* at 13:23-29 & FIG.7. Accordingly, before write leveling (no delay applied by DW-1, ... DW-n), the strobe signals arrive substantially at the same time (T2) to the DIMM (on the right side of the figure). *Id.* at 13:30-37. The clock signal CK1 (and the corresponding address and command signals) arrives with different delays to the different memory devices (SDRAM-1, ..., SDRAM-n; green) due to the delay caused by the "fly-by" arrangement of those memories. As an example, Tokuhiro

illustrates that the clock CK1 arrives in sync with the DQS-1 signal at time T2 (dashed red line) in SDRAM-1, but there is a delay Dt1-n (red box) when the clock signal arrives at the last device SDRAM-n in the fly-by arrangement at time T3 (solid red line). *Id.* & FIG. 7 (reproduced below with annotations).

FIG. 7

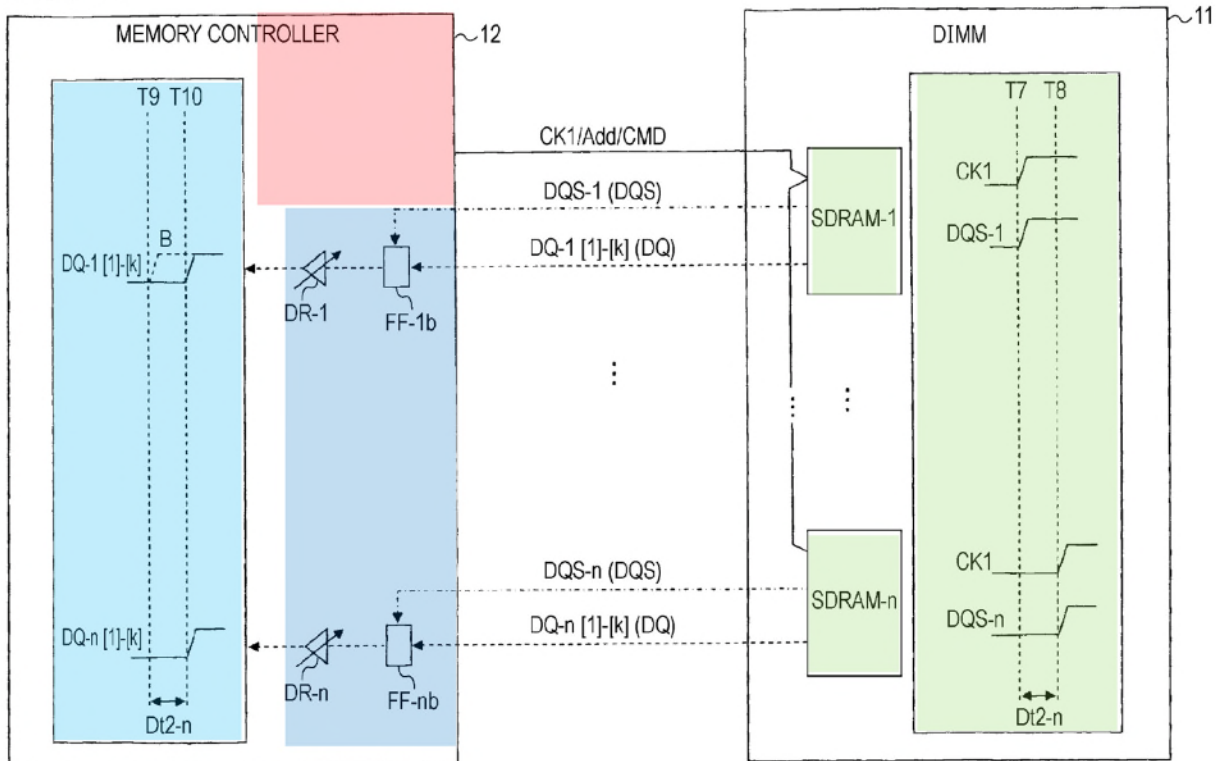


During write leveling, the memory controller adjusts the delay unit DW-n to delay DQS-n by Dt1-n, allowing DQS-n to arrive at the same time (T3, solid red line) as the delayed clock signal CK1 at the n-th device SDRAM-n. *Id.* at 13:47-14:2.

275. Tokuhiro teaches that the write delay Dt1 can also be used to determine delays for **read** data transmissions in order to compensate for large fly-by delays before the read data enters the clock domain of the memory controller.

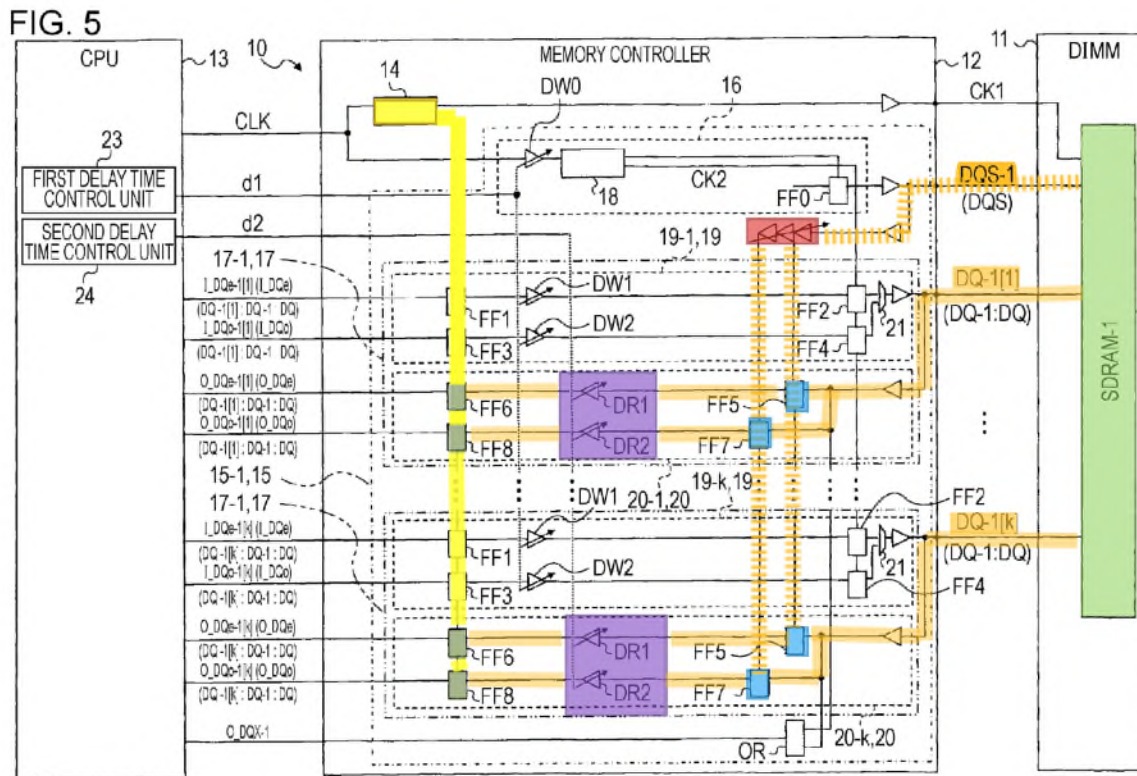
Id. at 3:16-26. For example, Tokuhiro at FIG. 11 shows a read operation where data DQ-1 is transmitted from SDRAM-1 at T7 and data DQ-n is transmitted from SDRAM-n at T8 with a delay of $Dt2-n$. *Id.* at 18:26-35 & FIG. 11 (reproduced below with annotations). Tokuhiro teaches that, after the read data is clocked into respective flip-flops FF-1b to FF-nb using the corresponding strobe signals, delay elements DR-1 and DR-n delay their respective read data such that, at T10, all corresponding data bits can be captured with the memory controller local clock. *Id.* at 18:36-52.

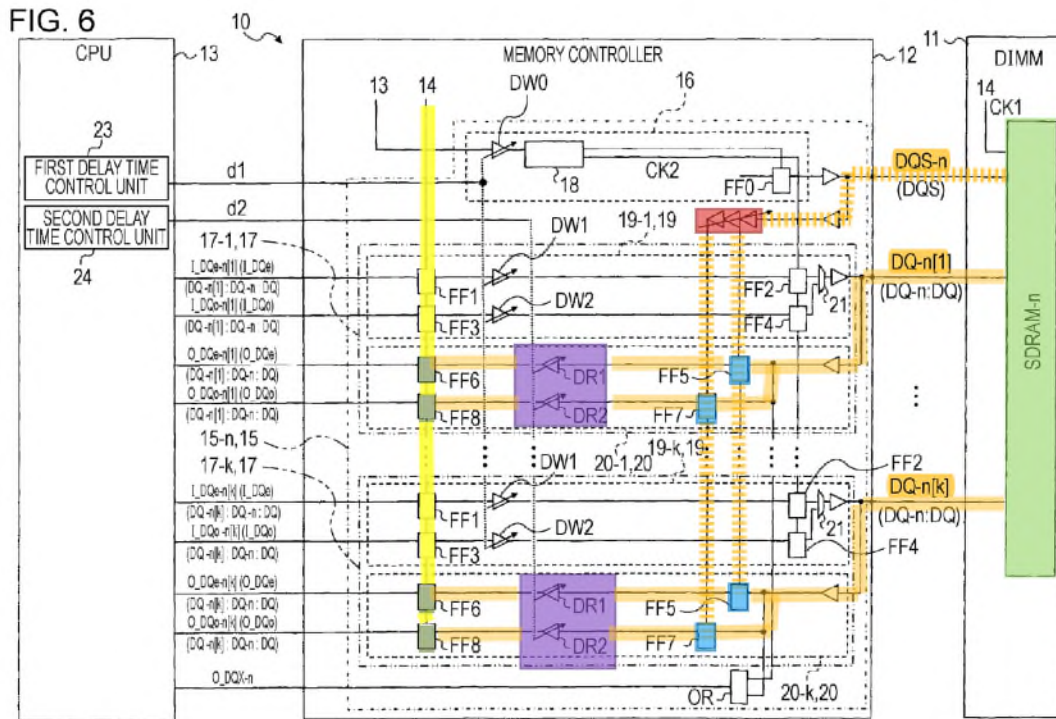
FIG. 11



EX1006 (Tokuhiro), Fig. 11 (annotated).

276. As shown below, the details of delaying the data signals (solid orange) by the delay elements DR1 and DR2 (purple) before the values of those signals are captured by the flip-flops FF6 and FF8 (olive green) that use the clock domain (yellow) of the memory controller are illustrated by Tokuhiro's FIG. 5 (for SDRAM-1) and FIG. 6 (for SDRAM-n) (both reproduced below with annotations).
Id. at 10:63-12:5.





277. Tokuhiro explains that, “with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt_2 based on the first delay time Dt_1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.” EX1006 (Tokuhiro), 18:66-19:7. A Skilled Artisan would have understood from Tokuhiro’s teaching that the delay elements DR1 and DR2 (purple) can compensate for fly-by delays of read data in a simple way using the delays for write operations without

special circuitry (such as FIFOs), even if the fly-by delay between two memory devices, such as between SDRAM-1 in FIG. 5 and SDRAM-n in FIG. 6, is larger than a clock cycle. EX1006 (Tokuhiro), 3:9-26, FIGS. 5 and 6.

2. Motivations to Combine Tokuhiro and Hiraishi

278. Tokuhiro and Hiraishi are analogous art since each is directed to improving memory systems using memory modules in which the memory chips are arranged in a fly-by configuration, such as modules using DDR3 memory chips. A person of ordinary skill would have been motivated to combine Tokuhiro and Hiraishi for at least three reasons, discussed below.

a) First motivation: Tokuhiro teaches calculating read delays based on the delays for write operations, which is more efficient than Hiraishi's technique of performing read leveling independent of the write delays

279. As shown below, Hiraishi discloses that the data register buffers on the module (blue) buffer the data (DQ) and strobe (DQS) signals and, “[a]lthough the data DQ-Pre and the data DQ-Post have the same content, because the data DQ is buffered by the data register buffer 300, the timing is off between the data DQ-Pre and the data DQ-Post. The same is true for a relationship between the data strobe signal DQS-Pre and the data strobe signal DQS-Post. Therefore, in the present embodiment, it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300 and a timing adjustment

between the data register buffer 300 and the memory controller in a separate manner.” EX1005 (Hiraishi) at [0104], FIG. 7.

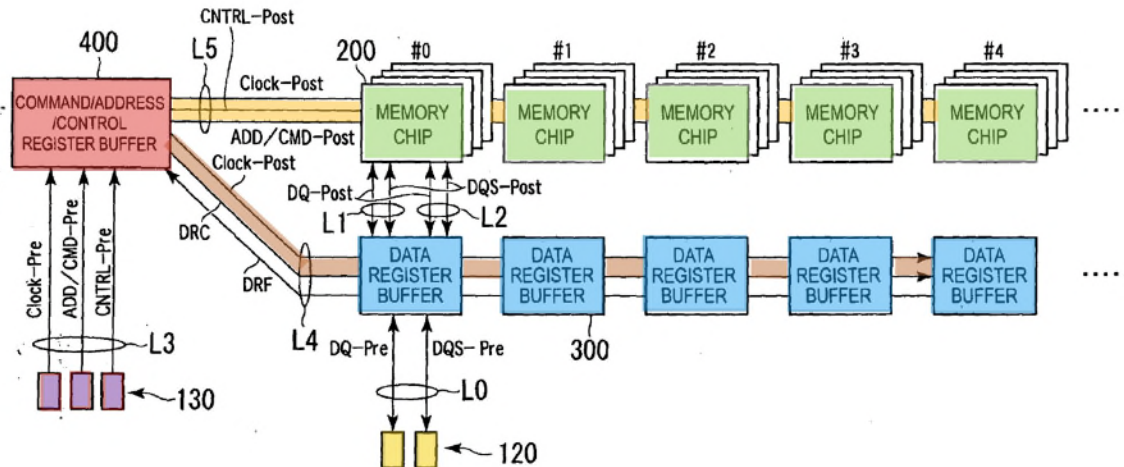


FIG.7

280. In Hiraishi, these timing adjustments include write and read leveling operations that are performed independent from each other. EX1005 (Hiraishi) at [0140] (“The leveling operation is to adjust a write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.”); *see also id.*, FIGS. 14A and 14B (explaining the write leveling operation between the data register buffer 300 and the memory chip 200), FIG. 15 (explaining the read leveling operation between the data register buffer 300 and the memory chip 200), FIGS. 16A and 16B (explaining the write leveling operation between the memory controller 12 and the

data register buffer 300), FIG. 17 (explaining the read leveling operation between the memory controller 12 and the data register buffer 300).

281. For example, during Hiraishi's "S4" read leveling between the data register buffer and the memory devices, "the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like." EX1005 (Hiraishi) at [0151], FIG. 15.

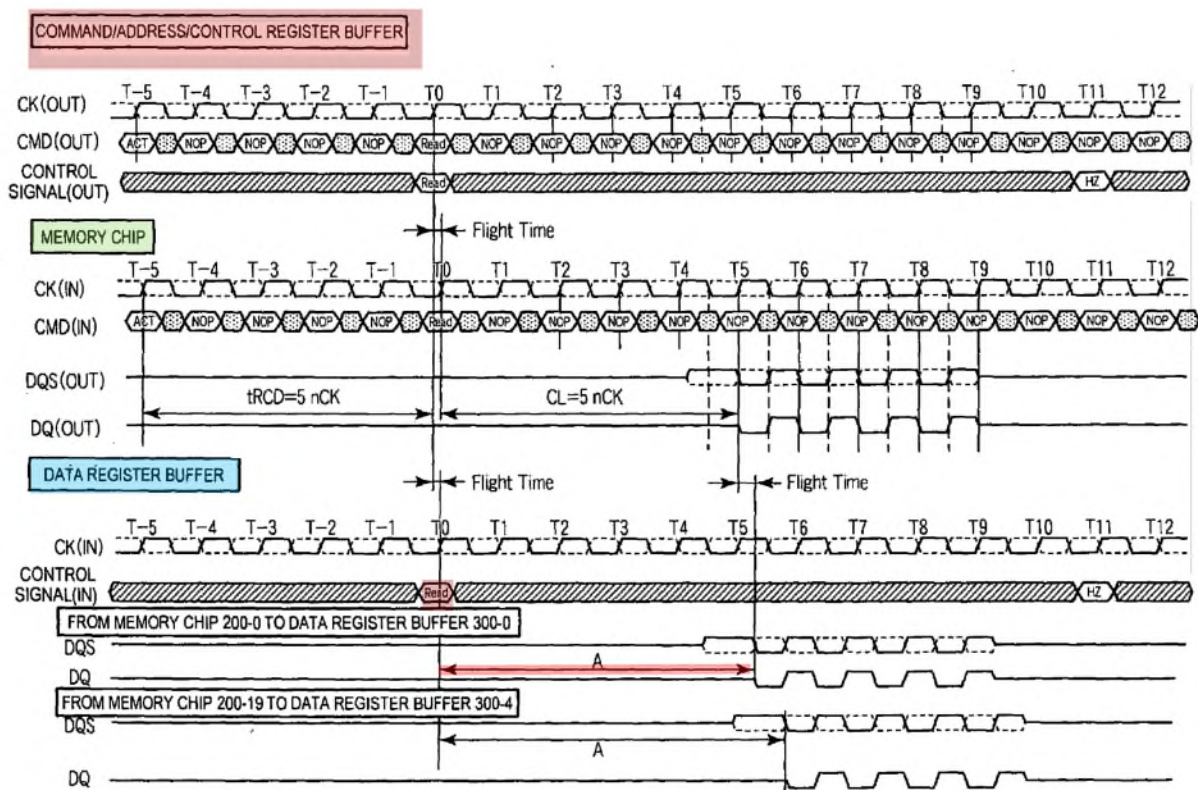
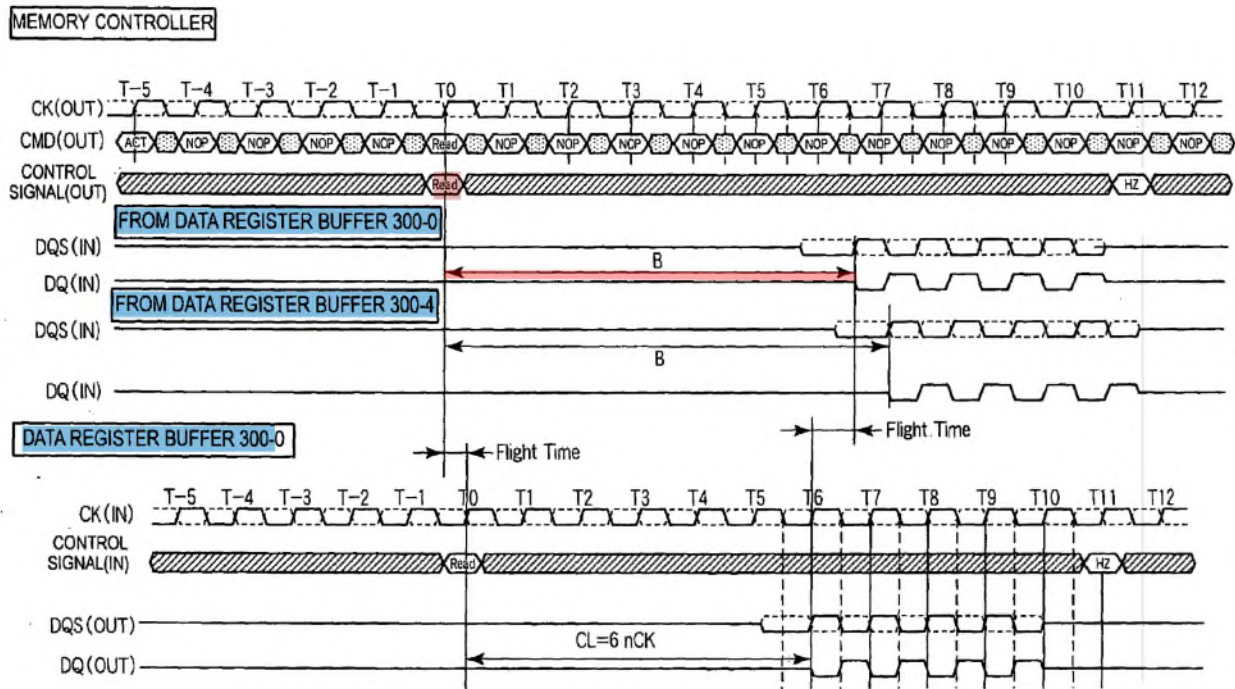


FIG.15

282. Similarly, during Hiraishi's "S5" read leveling between the data register buffer and the memory controller, "the memory controller 12 can find a time B from an issuance timing of the read command Read until the read data DQ is input. The time is measured for each of the data register buffers 300, stored in the internal circuit of the memory controller 12, and used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like." EX1005 (Hiraishi) at [0161] and FIG. 17.



283. A Skilled Artisan would have understood that performing these write and read leveling operations independently as disclosed by Hiraishi would require time and corresponding circuitry in both the data register buffers and in the

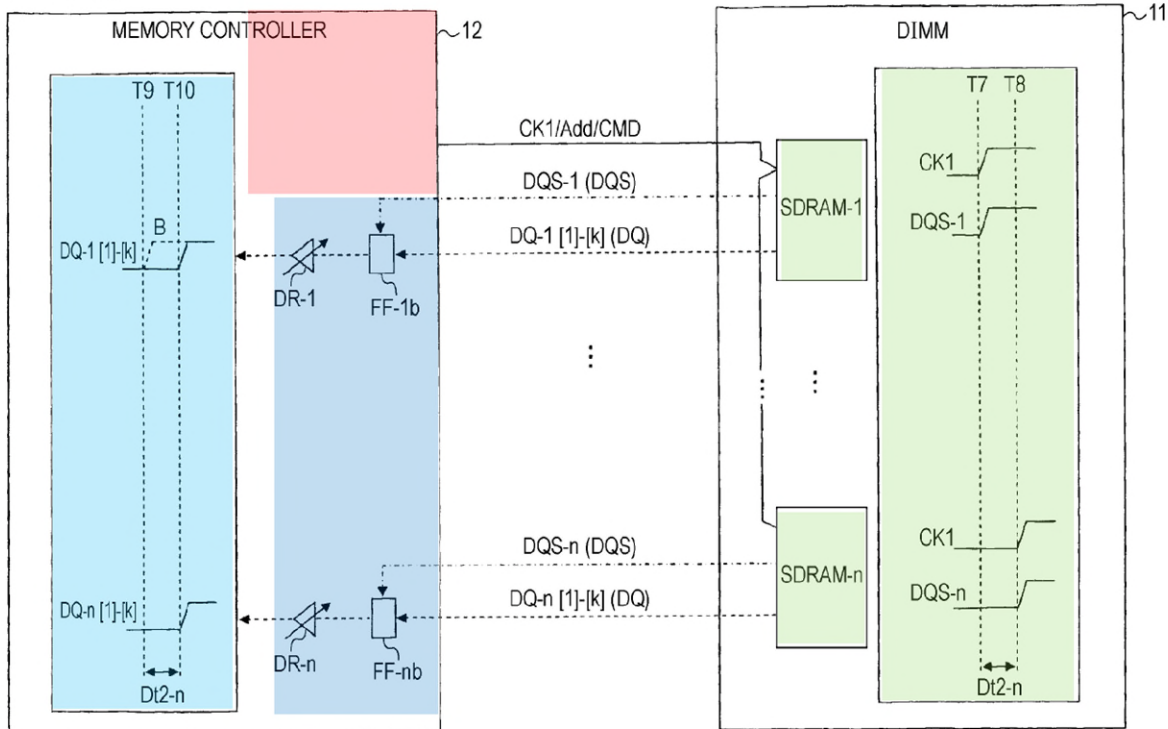
memory controller. Thus, a Skilled Artisan would have been motivated to simplify these write and read leveling operations and the corresponding circuitry.

284. For example, a Skilled Artisan would have understood that Tokuhiro discloses using the time delays found for write operations to determine the delays for read operations. EX1006 (Tokuhiro) at Abstract (“For each of the plurality of memories, a first variable delay unit delays, in a write operation, a data strobe signal output to the memory by a first delay time that is set by utilizing the write leveling function and a second variable delay unit delays, in a read operation, a data signal input from the memory by a second delay time that is set based on the first delay time.”). Tokuhiro further explains that “with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.” EX1006 (Tokuhiro) at 18:66-19:7.

285. In particular, as first presented above and explained in more detail below, Tokuhiro’s FIG. 11 illustrates its technique of handling large fly-by delays of the memory devices (green) during a memory read operation where the memory

controller's data handling part (blue), which interfaces with the memory devices, includes the read delay elements DR-1 to DR-n (reproduced below with annotations).

FIG. 11

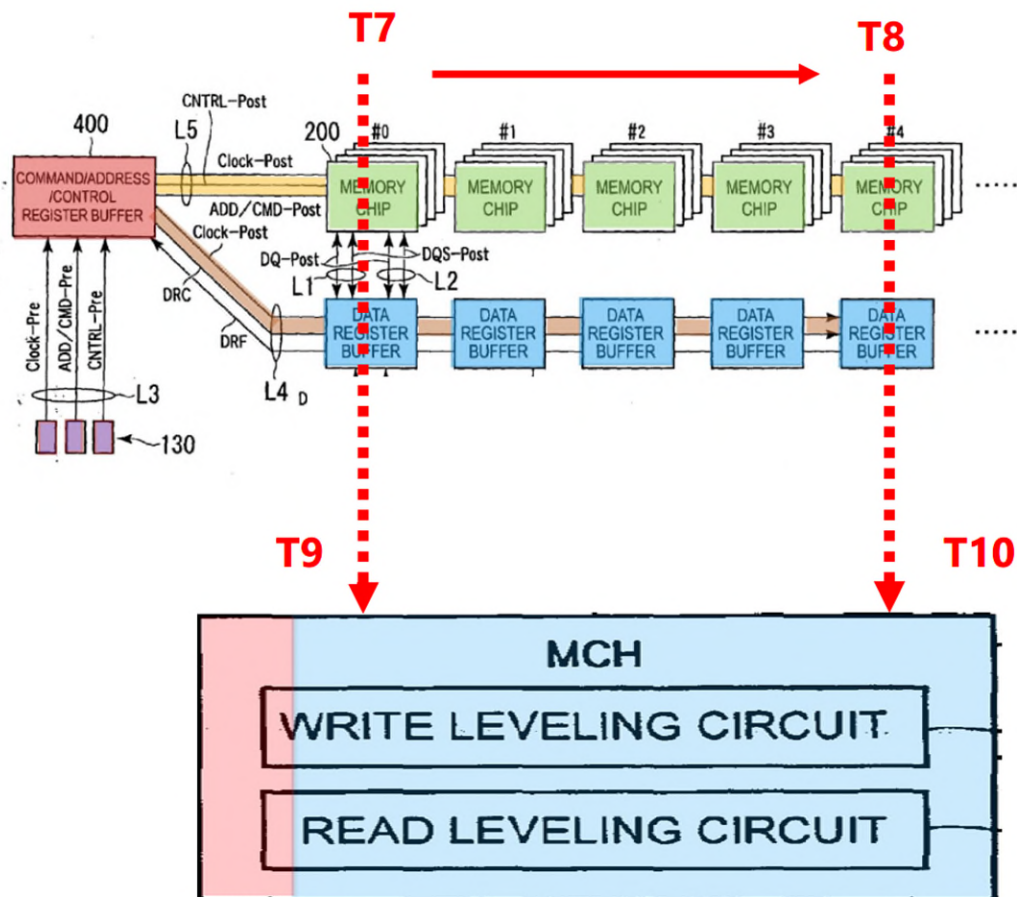


During the read operation, the first memory in the chain (SDRAM-1) (upper right) sends the data strobe DQS (and the corresponding data signal) at T7, but the last SDRAM-n (bottom right) sends its data and strobe signals at T8, after a delay Dt2-n. Accordingly, the data arrives at the memory controller from SDRAM-1 at T9 (upper left), but from SDRAM-n only at T10, after the delay Dt2-n (bottom left).

Tokuhiro's solution is that those delays are compensated by the read delay

elements DR-1 to DR-n such that the data arrives from all the memories substantially at the same time T10 (light blue timing diagram), thus the properly delayed data can be captured in a single clock cycle of the memory controller.

286. The corresponding timing delays in Hiraishi's system are illustrated below in an annotated version of Hiraishi's FIG. 7 (with the MCH and timing added).



As shown by the added timing annotations, the memory devices in Hiraishi have similar fly-by arrangements, and thus similar fly-by delays, as in Tokuhiro. That is,

if the first memory device (in group #0) starts sending the read data at time T7, the last memory in the chain (in group #4) will start sending its read data at a later time T8 due to the fly-by delay (solid red arrow). The data register buffers (dark blue) of Hiraishi have a fly-by arrangement similar to that of the memory devices, and thus they transmit the read data to the memory controller (MCH) with similar fly-by delays. In particular, the data register buffers transmit the read data with a pre-set latency from the time of receiving the read command which also arrives with those fly-by delays (on bus L4, horizontal in FIG. 7). EX1005, [0129]-[0130] & Fig.11. A Skilled Artisan would have also understood that the transmission delays from the data register buffers to the memory controller are substantially the same for each of the data-buffer-to-controller data paths since those data paths are substantially the same length. Accordingly, the read data from the first memory (in group #0) will arrive at time T9 at the memory controller, and the read data from the last memory (in group #4) would arrive at time T10 at the memory controller with a large fly-by delay which is substantially the same as the fly-by delay considered by Tokuhiro (EX1006) in its FIG. 11. *Supra* ¶285. Thus, the same problem of large fly-by delays happens in Hiraishi when the clock speeds of the memory devices increases.

287. Furthermore, techniques for read and write leveling were known at the time, *see, e.g.*, EX1020 (JESD79-3C) at 26-27, 33, 42-45 (write leveling); *id.*, 31,

33, 48-54 (multi-purpose register for read calibration), and Netlist has suggested that read and write leveling are memory operations in the sense of the '506 Patent, *see* EX1038 ¶ 48.

288. Therefore, a Skilled Artisan would have been motivated to implement Tokuhiro's technique of setting the read delays based on the write delays in the memory system of Hiraishi in order to simplify the read leveling operations and the corresponding circuitry. Such a combination would have been well within the level of skill at the time, since Tokuhiro teaches in detail how to calculate the read delays based on the delays for write operations, and the combination would have provided what is expected from the combination: a memory system where the read leveling operation is simplified by using the write delays.

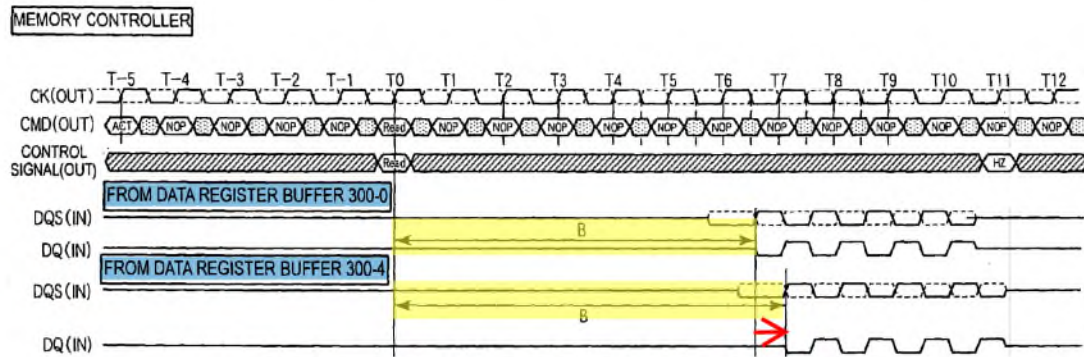
b) *Second motivation: Tokuhiro provides simple techniques for removing fly-by delays, while Hiraishi does not disclose how its memory controller re-times read data received with fly-by delays*

289. As discussed above, Hiraishi discloses that, during the "S4" read leveling operation, its data buffer determines, for each memory device, a "time A" between the Read command and the arrival of the corresponding read data, and uses that time A for the "adjustment of an activation timing of the input buffer circuit INB and the like." EX1005 (Hiraishi) at [0151], FIG. 15. Hiraishi further discloses using a Read FIFO 302 for re-timing the read data and outputting the read data in sync with the local clock signal. *Id.*, [0130] ("Thereafter, the data

register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS.”). As also discussed above, Hiraishi discloses that, during the “S5” read leveling operation, its memory controller determines, for each data buffer, a “time B” between the Read command and the arrival of the read data, and uses that time B for “an adjustment of an activation timing of an input buffer circuit (not shown) and the like.” EX1005 (Hiraishi) at [0161], FIG. 17.

290. However, Hiraishi’s Figure 17 shows that the read data still arrives at the memory controller from different data buffers with ***different*** “time B.” *Id.*, FIG. 17 (reproduced below in part with annotations).⁴ That is, the memory controller in Hiraishi still has to remove the fly-by delay (red arrow) between the different data buffers. *Id.*

⁴ I note that, in Fig. 17 of Hiraishi, the numbering of the data register buffers starts from the module controller, just like in Fig. 7, with data register buffer 300-0 being in group #0, i.e., closest to the module controller, and data register buffer 300-4 being in group #4, i.e., farthest from the module controller. This is similar to the issue discussed above in footnote 3 on page 73.



291. Tokuhiro, however, teaches that, “with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt_2 based on the first delay time Dt_1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.”

EX1006 (Tokuhiro) at 18:66-19:7. A Skilled Artisan would have understood from this disclosure of Tokuhiro that the delay circuits of Tokuhiro can be used in the memory module of Hiraishi to compensate for the fly-by delays between the different data buffers during a read operation so that the read data arrives at the memory controller from the different data buffers at substantially the same time. A Skilled Artisan would have also understood that, as a result of such a fly-by delay compensation in the memory module, the memory controller of Hiraishi would not have to manage large fly-by delays of read data, and could be implemented without

“a special mechanism, such as an FIFO.” EX1006 (Tokuhiro) at 18:66-19:7. A Skilled Artisan would have also understood that implementing such a fly-by delay compensation in the memory module would simplify the read leveling in the memory controller of Hiraishi and make the system’s operation more reliable since the large fly-by delays of read data would be removed at an early stage so that the rest of the system does not have to manage such large fly-by delays.

292. Therefore, a Skilled Artisan would have been motivated to use Tokuhiro’s technique of using delay circuits DR in the system of Hiraishi in order to match the input times of the respective read data signals in a simple way without using a special mechanism, such as FIFO based techniques.

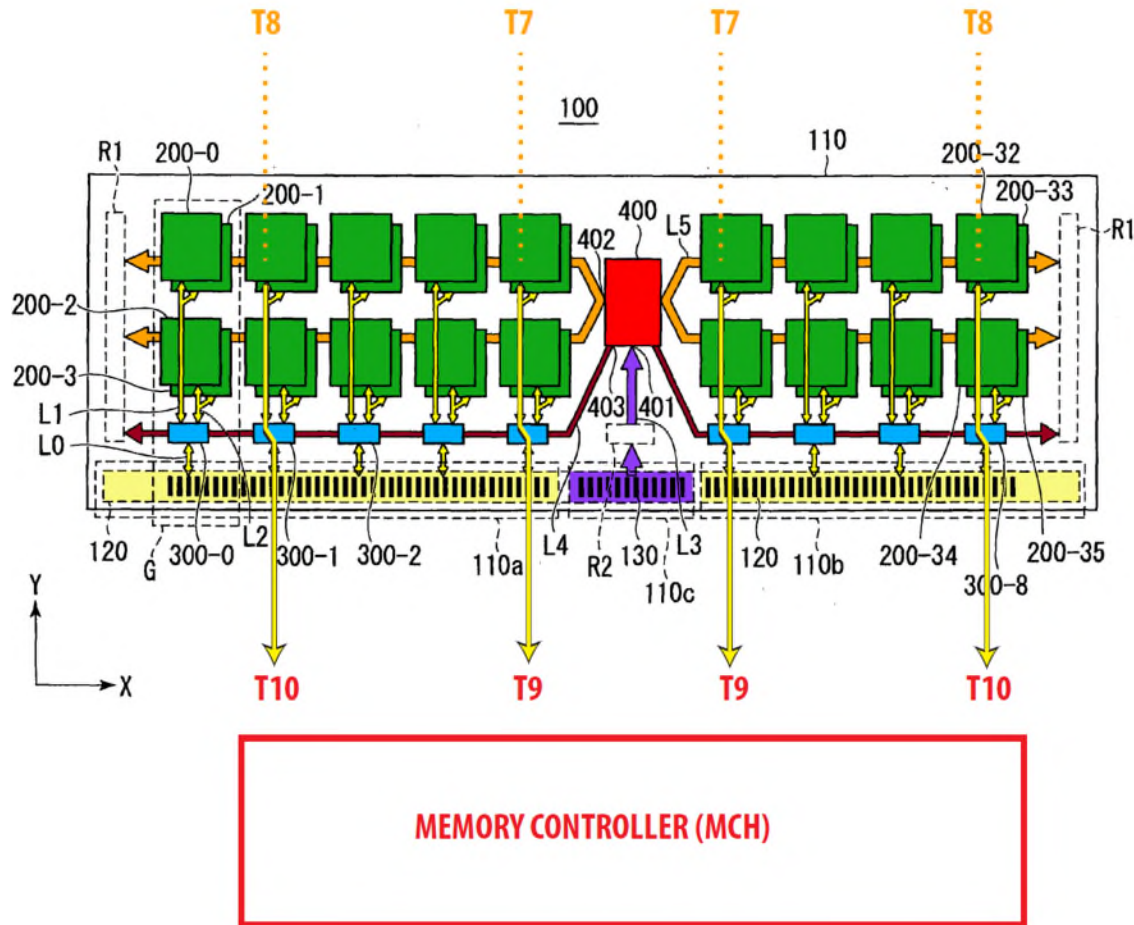
c) Third motivation: Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Hiraishi does not

293. Tokuhiro teaches that compensating for the fly-by delays of the read data is not specified by the JEDEC standards even though such delays can be larger than a clock cycle, which can cause problems at the receiver. See EX1006 (Tokuhiro), 2:54-59 (“compensations of the signal arrival time in read operations are not provided with the JEDEC standards”), 3:9-12 (“The delay on the order of 1 ns will become ***greater than a typical data period*** of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92.”). Thus, Tokuhiro teaches to a Skilled Artisan that problems arise if

the fly-by delay on read operations are not compensated, in particular if such delay exceeds the clock period, and teaches simple techniques to solve this problem of large fly-by delays at the arrival of read data based on timing for the write operations. *Id.*, *e.g.*, 3:16-26.

294. Moreover, fly-by delays greater than a clock cycle was a known problem for persons of ordinary skill in the art. For example, U.S. Patent No. 9,263,103 to Giovannini (“Giovannini”), which was filed March 17, 2008, around the same time as Tokuhiro, also explains that a “‘fly-by delay separation’ which results from a difference in delay between the clock signal on the fly-by path and the data-strobe signal on a direct path ***can exceed one clock period.***” EX1024 (Giovannini) at 2:17-20. “[I]f the fly-by delay separation between the clock signal and the data-strobe signal exceeds one clock period, the above-described timing adjustment process will adjust the phase relationship properly, but ***the timing adjustment may be off by a multiple of a clock period.***” *Id.*, 5:26-31. To solve this known problem of fly-by delays that are larger than a clock cycle, Giovannini discloses a special, FIFO-based circuitry in the memory controller. *Id.*, 6:56-7:2.

295. The following annotated version of Hiraishi’s Fig. 1 shows that Hiraishi suffers from the same potential problem identified by Tokuhiro of fly-by delays that can be greater than a clock cycle:



EX1005 (Hiraishi), Fig. 1 (annotated); *see also supra* ¶ 286 (similar annotation of Hiraishi Fig. 7). Here, times T7 to T10 correspond to the times shown in Fig. 11 of Tokuhiro. *See* EX1006 (Tokuhiro), 18:15-48. Tokuhiro teaches that due to fly-by delays, the memory devices nearer to the center of the module will execute the read command at T7 (and the memory controller will receive the data at T9), while the memory devices further from the center will execute the read command at T8 (and the memory controller will receive the data at T10). *Id.* Tokuhiro teaches that there will be a problem when the difference between T9 and T10 is greater than one

[illegible]

Samsung Electronics Co., Ltd.
Ex. 1045, p. 209

dimensions of the module stay the same, if the clock cycle is shortened to allow for faster memory operations. In Hiraishi's system, the data buffers have separate local clocks having similar fly-by delays as the memory devices. In contrast, the system memory controller is a single device with its own local clock. As a result of the large fly-by delays in the modified version of Figure 17 above, Hiraishi's memory controller cannot simply capture, in the same clock cycle, both the first byte of read data from data register buffer 300-0 (left dashed red line) and the first byte of read data from the data register buffer 300-4 (right dashed red line), and instead would require circuitry and logic to re-align the read data that arrives with more than a clock cycle of fly-by delay. *See, e.g.,* EX1024 (Giovannini) at 6:56-7:2 (“‘Read-alignment’ (also referred to as ‘read-data-alignment’) involves synchronizing the read data to the same clock signal as the read data comes out of, for example a first in, first out buffer (‘FIFO’) in the memory controller and is provided to the core of the memory controller.”). Thus, a Skilled Artisan would have understood that large fly-by delays (in the “horizontal” direction between the module controller and the data buffers) cause problems, in particular with reception of the read data in the system memory controller. (Hiraishi's data buffer and its S4 training handle much smaller delays in the “vertical” direction on the data lines between a data buffer and the coupled memory devices.)

297. Further, a Skilled Artisan would have understood that the fact that Hiraishi teaches read leveling in the memory controller (*see, e.g.*, EX1005 (Hiraishi), Fig. 2) does **not** necessarily solve the problem of larger-than-clock-cycle fly-by delays. Indeed, Hiraishi describes the read leveling operation between the memory controller and the data register buffer with reference to FIG. 17, including the memory controller measuring a time B, which is “used in an adjustment of an activation timing of an input buffer circuit (not shown) and the like.” EX1005, [0161] & FIG. 17. Adjusting the activation timing of the input buffer circuit, however, does not align the read data with the local clock of the memory controller. Thus, without any further processing, read data with larger than clock cycle delays at the end of the fly-by chain would be latched at different cycles. Hiraishi, however, is silent about any solution in the memory controller for fly-by delays *greater* than one clock cycle, and instead only shows fly-by delays *less* than one clock cycle. *See, e.g.*, EX1005 (Hiraishi) at FIG. 17 (annotated above at ¶290 showing a fly-by delay (red arrow) which is less than a clock cycle). Therefore, Hiraishi is silent about the details of its read leveling operation in the memory controller, in particular, about larger-than-clock-cycle delays or how to handle the problems caused by those delays. A Skilled Artisan would have known about these problems, motivating her to look for solutions.

298. Tokuhiro, for example, discloses that, “with the provision of the second variable delay circuit DR for delaying the data signal by the second delay time Dt2 based on the first delay time Dt1 that has been set by utilizing the write leveling function, a memory interface capable of matching the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n with one another, to which the clock signal line is wired through the daisy chain connection, can be simply realized without providing a special mechanism, such as an FIFO.” EX1006 (Tokuhiro) at 18:66-19:7.

299. Thus, a Skilled Artisan would have been motivated to use Tokuhiro’s technique of using delay circuits DR to get rid of the fly-by delays of the read data before that data is input to the local clock domain of the memory controller, so that the memory controller does not need special FIFO-based circuitry for re-timing the read data.

3. The combination of Hiraishi in view of Tokuhiro relied upon here

a) It would have been obvious to implement Tokuhiro’s delay elements in Hiraishi’s data register buffers

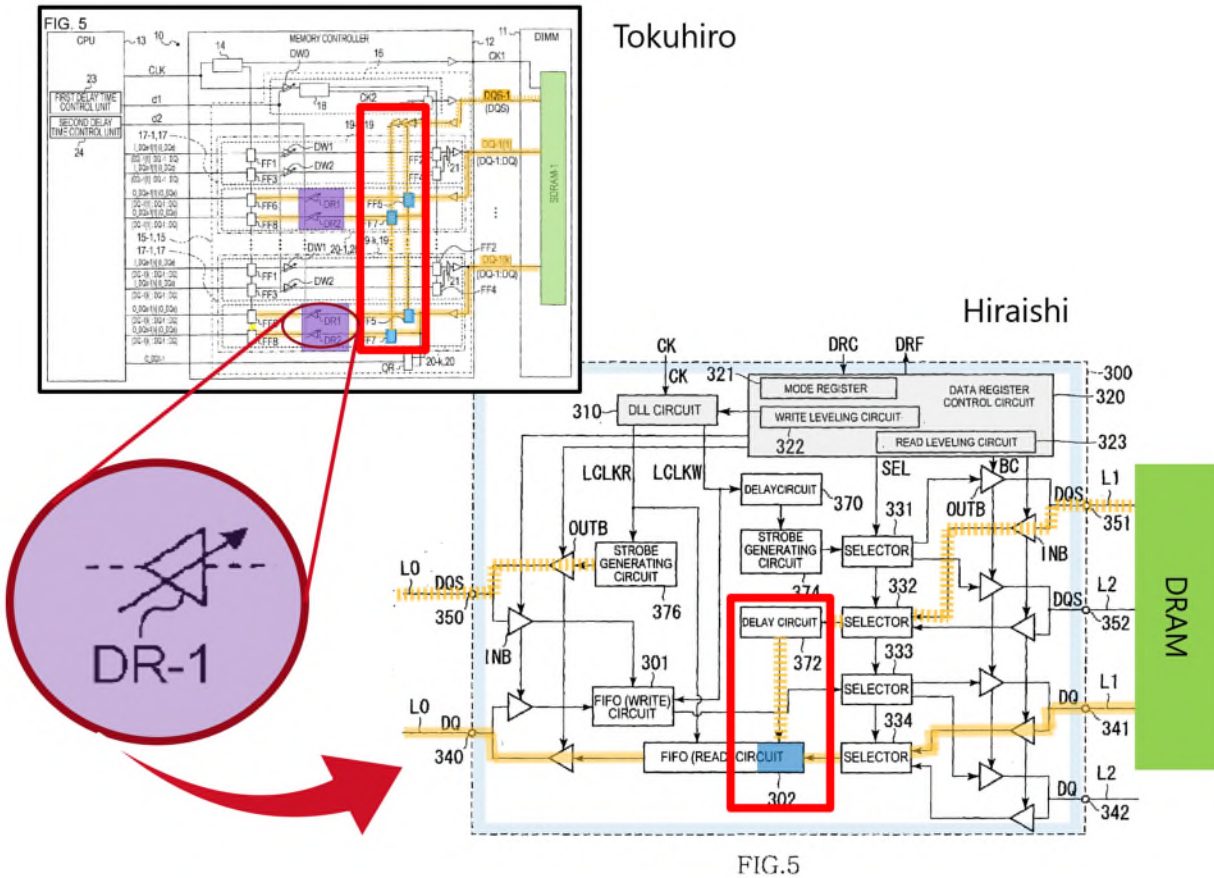
300. As discussed above, a Skilled Artisan would have been motivated to implement Tokuhiro’s technique of delaying read data based on delays for write operations so that the read data from all the memory devices arrive at substantially the same time in the clock domain of the memory controller. A Skilled Artisan

would have also understood from Tokuhiro's disclosure that it was advantageous to implement Tokuhiro's delays in the data buffers of Hiraishi.

301. For example, a Skilled Artisan would have understood that, if Tokuhiro's delays of the read data are implemented in the data buffers of Hiraishi and those delays are determined from the delays for write operations, the memory controller does not have to manage large fly-by delays of read data and the memory controller does not require any extra circuitry (e.g., FIFOs) to handle those large delays. Accordingly, a Skilled Artisan would have been motivated to implement Tokuhiro's read data delaying technique in the data register buffers of Hiraishi, including determining delays for write operations and using those write delays to determine read delays for read operations.

302. In particular, it would have been obvious to a person of ordinary skill to implement Tokuhiro's delay elements in Hiraishi's data register buffers (rather than in the memory controller), and such a person would have had a reasonable expectation of success in making such a combination. For example, Tokuhiro teaches to apply the read delay (e.g., DR-1, purple) immediately after the corresponding read data from the memory (SDRAM-1, green) has been latched (e.g., by flip-flop FF5, blue, in red box), as illustrated in an annotated version of Tokuhiro's Figure 5 below (upper left). Hiraishi teaches that the read data from the memory (DRAM, green added) is latched into FIFO (Read) Circuit 302 (blue, in

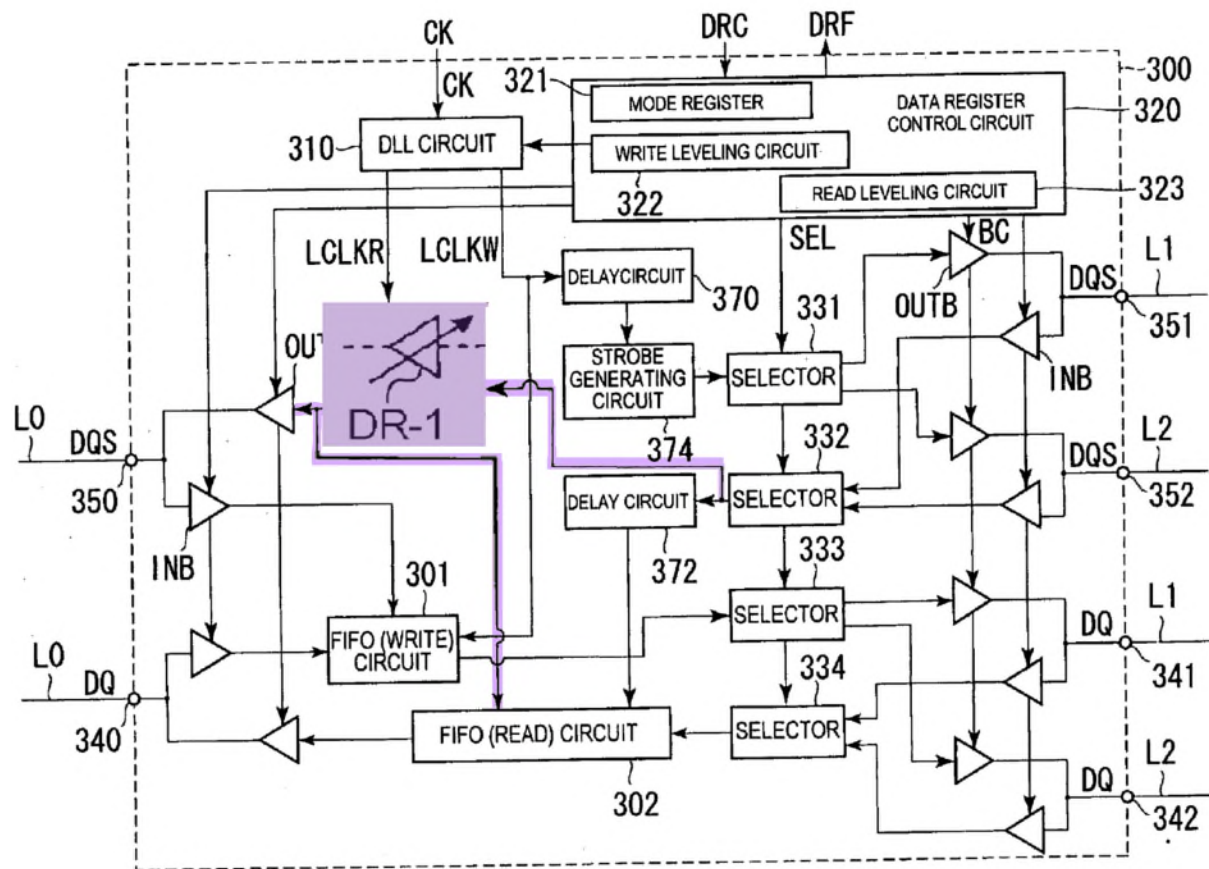
red box). EX1005 (Hiraishi), FIG. 5 (reproduced below, lower right, with annotations). Accordingly, a Skilled Artisan would have been motivated to add Tokuhiro's read delay elements (e.g., DR-1) to Hiraishi's data register buffer immediately after the read data from the memory is latched.



Annotated version of Tokuhiro Fig. 5 and Hiraishi Fig. 5

303. A Skilled Artisan would have understood that, in a read operation, the data signal (DQ) is transmitted from the data buffer to the memory controller with a corresponding strobe signal (DQS) which is in sync with the data signal. EX1005 (Hiraishi), FIG. 5. Thus, a Skilled Artisan would have understood that the strobe

(DQS) and data signals (DQ) have to be in sync after Tokuhiro's read delay has been added to Hiraishi's data buffer. Delaying both data and strobe signals were well known in the art, and one such implementation is disclosed even by Tokuhiro for the write operations. *See, e.g.*, EX1006 (Tokuhiro) at FIGS. 5-6 (showing delay element DW0 for a strobe signal and delay elements DW1 and DW2 for data signals) & 9:33-40 ("More specifically, a first delay time Dt1-1 is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-1 shown in FIG. 5. Likewise, a first delay time Dt1-n is set for the three first variable delay circuits DW0, DW1 and DW2 which are included in the control circuit unit 15-n shown in FIG. 6."). A Skilled Artisan would have understood that the same functionality can be implemented in the data buffer of Hiraishi to delay the transmission of read data along with its strobe signal to the memory controller. An example of such an implementation is illustrated in a modified FIG. 5 of Hiraishi below.

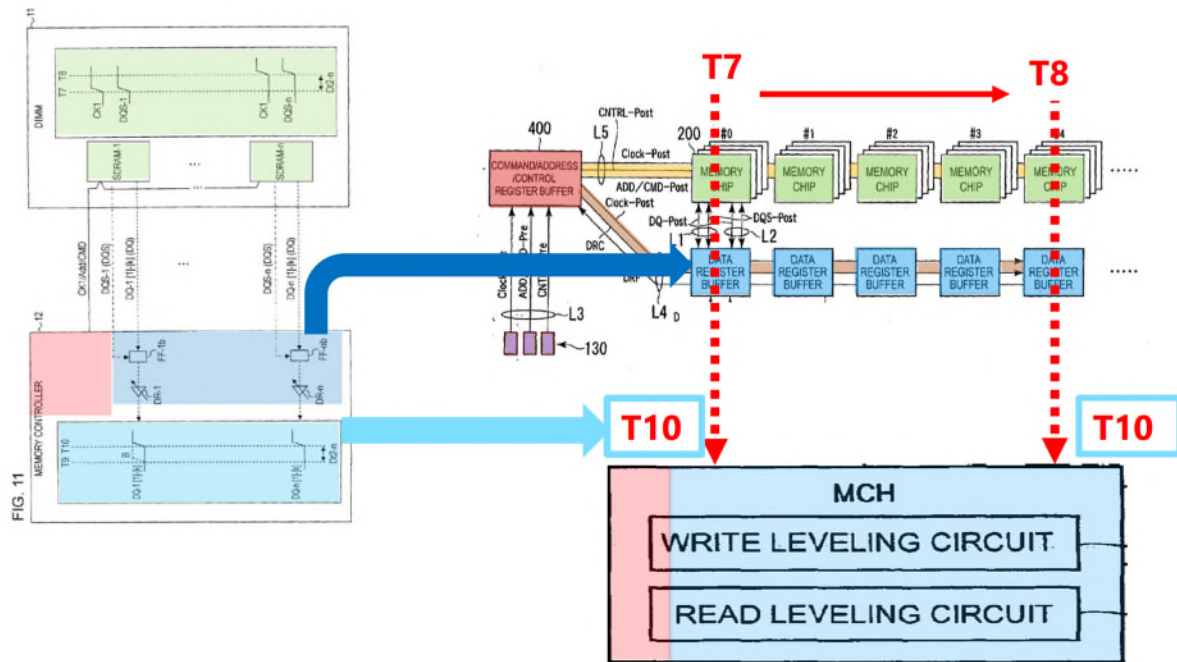


304. In this exemplary implementation, Tokuhiro's read delay circuit (DR-1, purple) is added to Hiraishi's data buffer to remove the large fly-by delays, while the existing delay circuit 372 continues to make fine timing adjustments to the phase of the incoming strobe DQS as before to properly latch the incoming data DQ. Based on the principles in Tokuhiro, including setting the read delays based on delays in a write operation, the added read delay circuit DR-1 is configured to delay the read data strobe signal DQS (purple, received from selector 332, purple) and to use the delayed strobe to clock out data from FIFO (Read) Circuit 302 so that the delayed data DQ from the Read FIFO is in sync with the

delayed strobe. A Skilled Artisan would have understood that the above modifications, including the additional read delay DR-1, would synchronize the read data output from the multiple data register buffers 300 across the memory module. See EX1006 (Tokuhiro) 18:53-64 (“Thus [...], for the plurality of SDRAMs of SDRAM-1 to SDRAM-n to which the clock signal line is wired through the daisy chain connection, the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n, to which the clock signal line is wired through the daisy chain connection, can be easily matched with one another . . .”); *see also, e.g.*, EX1020 (JESD79-3C), p. 56 (Fig. 25 showing read data output in synchronization with the corresponding strobe). I note that, in this implementation, Hiraishi’s existing read FIFO circuit is adapted to delay the read data, so there is no need to add delay circuits to the data line (DQ). A Skilled Artisan would have also understood that, in alternative implementations, delay elements similar to Tokuhiro’s DR elements can be used instead of or in addition to Hiraishi’s FIFO circuit for delaying the read data.

305. In Hiraishi, as illustrated in the annotated FIG. 5 of Hiraishi above, the memory devices interface with the data register buffers, not directly with the memory controller (MCH). Hiraishi also expressly teaches a Skilled Artisan to implement read and write leveling circuitry in each data buffer as part of the functionality of interfacing with the memory devices, and this functionality is in

addition to write and read leveling circuitry in the memory controller. *See, e.g.*, EX1005 (Hiraishi) at FIG. 5 (illustrating write and read leveling circuits 322 and 323 in the data buffer) and FIG. 2 (illustrating write and read leveling circuits in the MCH); Fig. 13 (identifying S4 read and write leveling, which takes place between buffers and memory devices, as a separate step from S5 read and write leveling, which takes place between buffers and memory controller). Since Hiraishi already teaches read (and write) leveling circuitry in the data register buffers, a Skilled Artisan would have been motivated to implement the functionality of the delay elements (DR) of Tokuhiro in the data buffers of Hiraishi to delay transmission of read data in order to compensate for the fly-by delays of the data register buffers of Hiraishi.



306. As illustrated above in the annotated FIG. 11 of Tokuhiro (on the left above) and FIG. 7 of Hiraishi (on the right above), the combination implements the functionality of the additional read delay of Tokuhiro in the data register buffers of Hiraishi (as illustrated by the dark blue arrow). As a result of these additional read delays, the read data arrives to the memory controller (MCH) at substantially the same time (T10) despite the fly-by delay (from T7 to T8) on the memory module. In the annotated figures above, the light blue arrow illustrates that the additional read delays compensate for the fly-by delays in accordance with Tokuhiro's teaching by delaying the read data so that it all arrives from each data buffer at substantially the same time. As a result, the memory controller can capture the

corresponding read data from all the memories in a single clock cycle even if the fly-by delays on the module are larger than a clock cycle. In particular, as a result of the additional delays implemented in the data register buffers of Hiraishi, the data from all of the data registers would arrive to the MCH without fly-by delays, at substantially the same time (T10).

307. A Skilled Artisan would have understood that an important advantage of this combination is that the memory controller (MCH) receives all read data at substantially the same time, so it does not need to manage large fly-by delays of read data either during the training or during normal operation as it tries to capture the correct value of the read data. Accordingly, the memory controller can be implemented with less circuitry and functionality. For example, the memory controller does not need extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles due to the larger than clock cycle fly-by delays on the module.

308. Furthermore, a Skilled Artisan would have also understood that the advantages of implementing Tokuhiro's read delays in the data buffers of Hiraishi include that it would remove the large fly-by delays on the module at the first practically available location, so that the rest of the system does not have to manage those large fly-by delays. Indeed, as Tokuhiro explains, the JEDEC standards did not provide a solution for the read leveling in the memory devices,

thus JEDEC-compliant memory devices do not have Tokuhiro's read delay elements. EX1006 (Tokuhiro) at 2:54-59. A Skilled Artisan, however, would have understood that Hiraishi's data buffer can include delay elements like those of Tokuhiro, since it already includes both read and write leveling functionality. Accordingly, a Skilled Artisan would have been motivated to implement Tokuhiro's read delays in the data buffers of Hiraishi.

309. In addition, I understand that, when there is a design need to solve a problem, and there are a finite number of identified predictable solutions to the problem, all of those solutions likely are obvious. Here, a Skilled Artisan would have understood that, in the combination of Hiraishi and Tokuhiro, the delay elements of Tokuhiro can be implemented either in the data buffers or in the memory controller of Hiraishi, rendering both of those solutions obvious.

b) It would have been obvious for either of Hiraishi's memory controller and module controller to program Tokuhiro's delay elements in Hiraishi's data buffers

310. A Skilled Artisan would have understood that there are two potential ways to implement Tokuhiro's technique of adding read delay elements to Hiraishi's data register buffer to solve the problem of large fly-by delays: (1) the **system memory controller** can determine the read delays based on the timing for a write operation and, in turn, program the read delay elements in the data register buffers on the module accordingly, or (2) the **module controller** can determine the

read delays based on the delays measured by the data register buffers during a write operation and, in turn, program the read delay elements in the data register buffers accordingly. *See, e.g.*, EX1006 (Tokuhiro), 16:18 (Formula 3-6 for calculating the read delays from the write delays, including the maximum of those write delays).

311. As discussed above, a Skilled Artisan would have been motivated to implement the teaching of Tokuhiro to determine the specific delays for the read delay elements in the data buffers of Hiraishi based on the delays for the write operations. *Supra* ¶¶ 279-288. A Skilled Artisan would have also understood that using delays of the write operations to determine the fly-by delays for read operations would have worked for its intended purpose as taught by Tokuhiro because, as discussed below, either the **memory controller** can determine the fly-by delays *during* write leveling or, alternatively, the **data buffers** can detect the fly-by delays *Dt1 before* write leveling, when the memory controller issues a write command to the memory module. In either case, the result is that the memory controller does not have to manage large fly-by delays when trying to capture the read data.

312. **As to the first method** of utilizing the teachings of Tokuhiro in the memory system of Hiraishi, the system memory controller in Hiraishi can determine the fly-by delays on the module during write leveling as taught by

Tokuhiro. See *supra* ¶¶ 273-274; EX1006 (Tokuhiro), Fig. 7 (annotated). Tokuhiro further explains that these Dt1 delay times obtained from write leveling are used to set the delays Dt2 for the read data. *Supra* ¶¶ 275-277. For example, “the second delay times Dt2-1 to Dt2-n corresponding respectively to the SDRAM-1 to the SDRAM-n are set so as to become shorter gradually in the order from the 1-channel SDRAM-1 toward the n-channel SDRAM-n.” EX1006 (Tokuhiro) at 16:43-46.

313. Thus, in this first implementation of the combination of Hiraishi and Tokuhiro, a Skilled Artisan would implement Tokuhiro’s calculation of the fly-by delays based on write leveling in Hiraishi’s memory controller and, based on these fly-by delays, the memory controller would program the additional read delay elements in the data buffers. In particular, a Skilled Artisan would have implemented Hiraishi’s leveling operations between the memory controller and the data buffers (Step S5 of Fig. 13) by the memory controller performing write leveling first, programming the read delay elements in the data buffers based on the write delays next, and performing the simplified read leveling last. EX1005, Fig. 13 (reproduced below with annotations in accordance with the first implementation of the Hiraishi-Tokuhiro combination). As taught by Tokuhiro, the result of this combination is that the read data arrives to the memory controller without substantial fly-by delays, thus simplifying the memory controller’s job and

circuitry for properly capturing the read data. For example, the memory controller does not have to compensate for fly-by delays in the read data, although it may still require read training to activate the input buffers in time and, if necessary, to adjust the phase of a local clock “for matching the phases of the read data DQ and the data strobe signal DQS” (similar to Hiraishi’s existing delay circuit 372 making fine timing adjustments to the phase of the incoming strobe DQS to properly latch the incoming data DQ). EX1005, [0091], [0141], [0161], [0163].

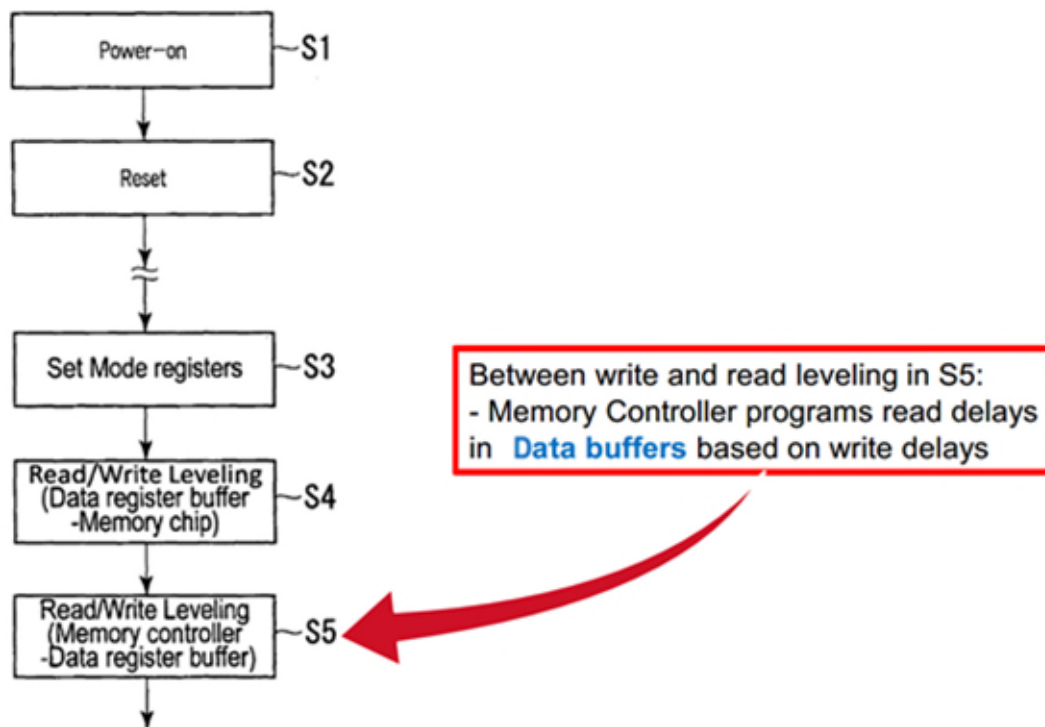


FIG.13

EX1005 (Hiraishi) Fig. 13 (annotated).

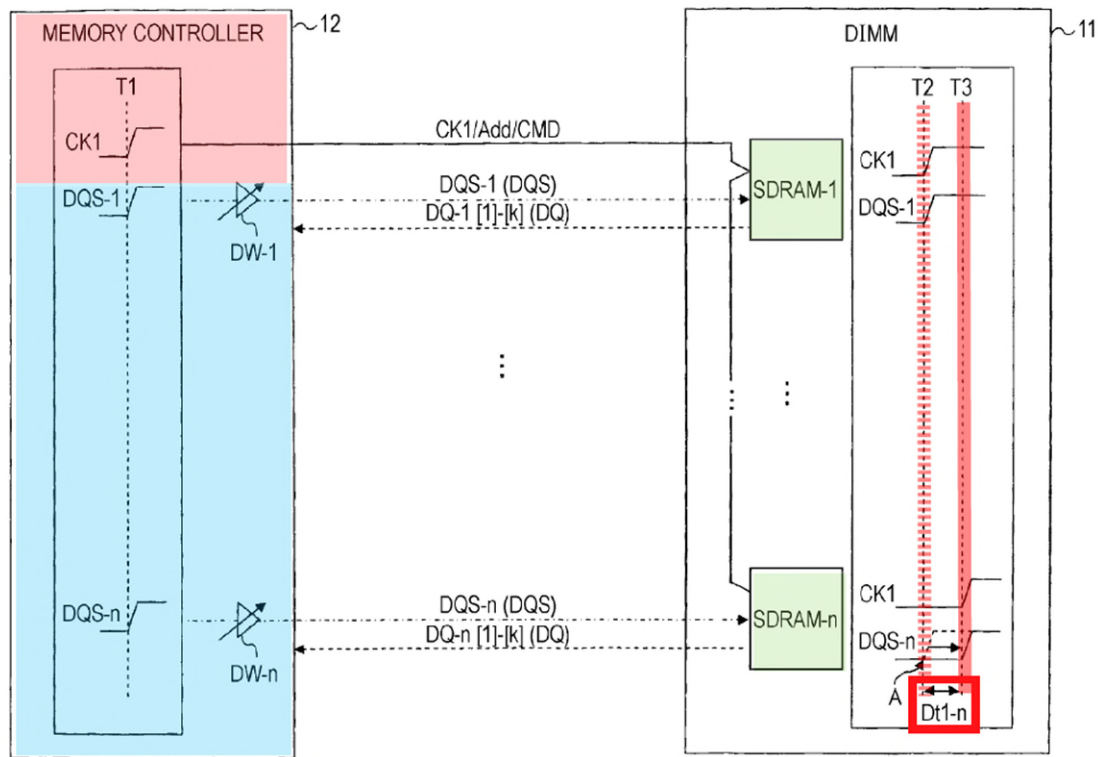
314. This implementation was well within the level of ordinary skill and provided nothing more than what was expected from the combination. For example, implementing Tokuhiro's read delay functionality in Hiraishi's data register buffers required adding a known function (delaying the read data as taught by Tokuhiro) to a known data register buffer of Hiraishi, where the data register buffer already had similar functionalities, including read and write leveling functions. Similarly, since Tokuhiro already taught how to calculate and set those read delays, a Skilled Artisan would have understood how to modify Hiraishi's memory controller to add the same functionalities. The result of the combination is as expected: a memory system in which the memory controller does not have to manage large delays, in particular larger than a clock cycle, when trying to capture the correct values of read data.

315. **As to the second method** of utilizing the teachings of Tokuhiro in the memory system of Hiraishi, a Skilled Artisan would have understood that Tokuhiro's technique can also be implemented in Hiraishi's memory module such that the ***data buffer circuits*** measure timing information to determine the fly-by delays during a write operation, and Hiraishi's ***module controller*** can be implemented to program the corresponding read delays in the data buffers with a reasonable expectation of success.

316. A Skilled Artisan would have been motivated to implement Tokuhiro's technique in Hiraishi's module, as opposed to the memory controller, because Hiraishi already teaches that functionalities of the memory controller, including interfacing with the memory chips and performing read and write leveling, can be performed by the module controller and data register buffers of the memory module. See, e.g., EX1005 (Hiraishi) at FIG. 5 (showing write and read leveling circuits 322 and 323). For example, Hiraishi expressly teaches that "the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input." EX1005 (Hiraishi) at [0151]. In addition, Tokuhiro explains that, before the write leveling, the write strobe signals arrive to the module at substantially the same time (T2), but the corresponding clock/address/command signals have respective fly-by delays in the chain (such as a delay Dt1-n for the n-th device). EX1006 (Tokuhiro), FIG. 7 (reproduced below with annotations); see also FIG. 10, 13:30-37 ("For example, **before the first delay time Dt1 is adjusted based on the write leveling function**, as shown in FIG. 7, the clock signal CK1 and the data strobe signal DQS-1 are input to the 1-channel SDRAM-1 substantially at the same time (see a time 'T2' in FIG. 7), while the clock signal CK1 is input (see a time 'T3' in FIG. 7) to **the n-channel SDRAM-n with a delay of the time Dt1-n**

after the input of the data strobe signal DQS-n (see the time 'T2' and a point 'A' in FIG. 7).”).

FIG. 7



Accordingly, a Skilled Artisan would have been motivated to use Hiraishi's time measuring technique in the data buffer to determine the fly-by delays during a *write* operation and set the *read* delays accordingly as taught by Tokuhiro.

317. For example, when Hiraishi's memory controller issues a ***write command***, say at time T1, the module controller forwards the write command on the DRC lines to the data buffers, and each of the data buffers will receive that write command with a corresponding fly-by delay: the data buffer closest to the module controller receives the write command at T2, and the n-th buffer receives

yet applied by the memory controller. As such, each data buffer can measure the time difference between the time of receiving the write command (between T2 and T3, depending on the buffer) and the time of the arrival of the data (T5). For the data buffer closest to the module controller, that time difference is the difference between T5 and T2, and for the data buffer furthest from the module controller, that time difference is the difference between T5 and T3.

319. A Skilled Artisan would have understood that those time differences for a write operation can be measured using the same technique that Hiraishi's data buffer is already using to determine a time delay between receiving a read command and the arrival of the corresponding read data. EX1005 (Hiraishi) [0151] ("The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200..."); *see also id.*, Fig. 15. Thus, a Skilled Artisan would have understood that the functionality of measuring the difference between the time of receiving a read command and the time of the arrival of the corresponding read data can also be implemented to measure the difference between the time of receiving a write command and the time of the arrival of the corresponding write data. Accordingly, a Skilled Artisan would have been motivated to use Hiraishi's time measuring

technique to measure a time interval between the arrival of a write command (e.g., T3) and the respective strobe signal (DQS) travelling with the corresponding write data (DQ) (e.g., T5) in order to determine the corresponding fly-by delays (e.g., Dt1-n).

320. A Skilled Artisan would have then understood that Hiraishi's memory buffers can use the feed-back channel DRF to communicate the measured time intervals to the module controller which, in turn, can use those time intervals to determine the corresponding fly-by delays for a read operation as taught by Tokuhiro, and program the read delay elements in the data buffers for transmitting the read data accordingly. See EX1005 (Hiraishi), [0089] ("the data register control circuit 320 generates a feedback signal DRF and supplies it to the command/address/control register buffer 400. The feedback signal DRF is a signal indicating a current status of the data register buffer 300."); [0099] ("The feedback signal DRF is supplied to the control signal generating circuit 430 from the data register buffer 300 via the input terminal 404.").

321. In this implementation of the Hiraishi-Tokuhiro combination, Tokuhiro's read delay functionality is added to the data register buffers of Hiraishi's module such that, advantageously, no changes to the circuitry of the memory controller are necessary. Furthermore, Tokuhiro's functionality of determining the fly-by delays from delays for the write operations and setting the

additional read delays accordingly is also implemented in Hiraishi's memory module. Thus, as illustrated by modified Fig. 13 of Hiraishi below, the system memory controller's operation in this combination changes in that it issues one (or more, if necessary) write commands and subsequently sends corresponding (dummy) write data *without* applying the write leveling delays, *e.g., before* write leveling in step S5, so that the memory module then can set the read delay elements as taught by Tokuhiro. That is, the data buffers receive the write command from the module controller with fly-by delays and the subsequent write data without those fly-by delays from the memory controller; the data buffers measure the time difference between the write command and the write data, and report it to the module controller; the module controller calculates the additional read delays for each data buffer and programs them accordingly. After the additional read delays have been set in the data register buffers, Hiraishi's memory controller can perform its write leveling function. Since the read data now arrives to the memory controller without substantial fly-by delays, the memory controller's training to capture the proper values of read data has been advantageously simplified.

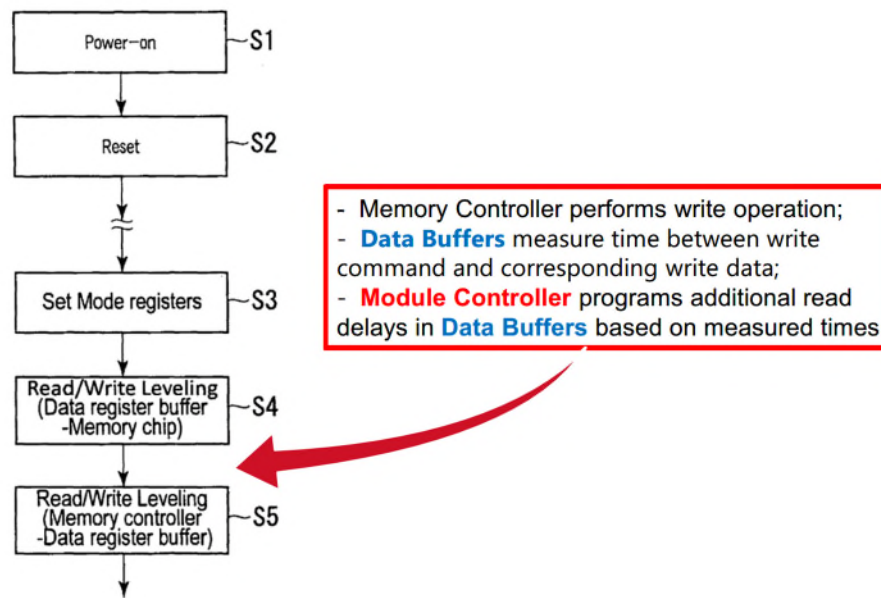


FIG.13

EX1005 (Hiraishi), Fig. 13 (annotated according to the second implementation of the Hiraishi and Tokuhiro combination). A Skilled Artisan would have understood that adding such write commands to the boot-up sequence of the system memory controller is a simple software change that can be easily implemented even in systems that use traditional system memory controllers. Thus, the memory module of the Hiraishi-Tokuhiro combination can also be advantageously used in traditional memory systems.

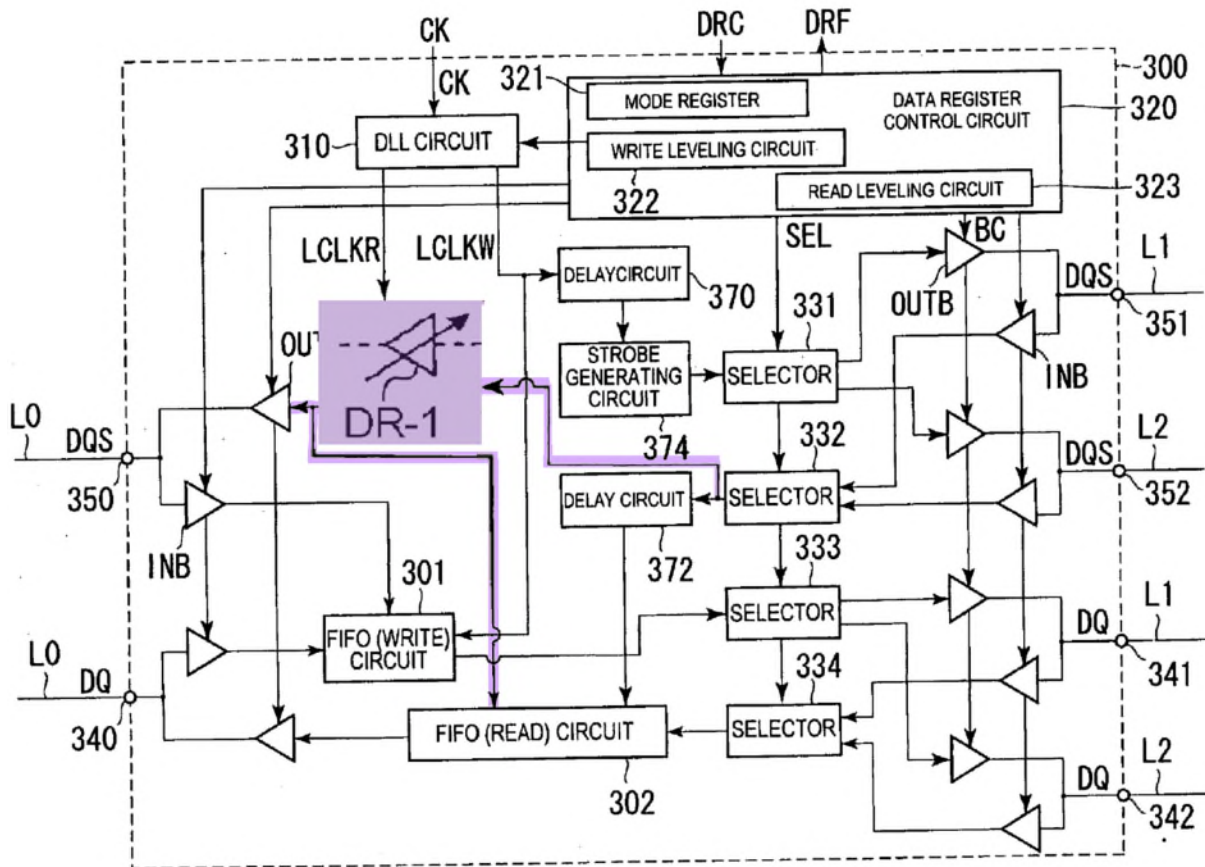
4. Claim 1

322. The combination of Hiraishi and Tokuhiro explained above, *supra* ¶¶271-321, discloses and renders obvious claim 1. Claim limitations 1[pre] through 1[e], 1[g], and 1[h] are disclosed by Hiraishi alone or with Butt as explained

previously, *supra* ¶¶ 101-128, 131-135. Claim limitations 1[f] and 1[i] are satisfied by the combination of Hiraishi and Tokuhiro, *supra* ¶¶ 271-321, as explained below in more detail.

a) 1[f]: “delay the first read strobe by a first predetermined amount to generate a first delayed read strobe”

323. Hiraishi as modified in combination with Tokuhiro discloses this limitation. For example, as explained above, the combination of Hiraishi and Tokuhiro includes a delay element DR-1 added to Hiraishi’s buffer circuits, which would delay the strobe signal from selector 332 and provide that delayed strobe signal to FIFO (Read) Circuit 302 (and to the output 350). See *supra* ¶¶ 300-321.



Thus, as modified in this combination, the modified data register buffer 300-0 would be configured to “*delay the first read strobe* [e.g., DQS from selector 332 to purple delay element DR-1, as taught by Tokuhiro] *a first predetermined amount* [e.g., the amount calculated as taught by Tokuhiro to remove fly-by delays] *to generate a first delayed read strobe* [e.g., sent to FIFO (Read) Circuit 302].”

b) 1[i]: “wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.”

324. Hiraishi as modified in combination with Tokuhiro (*supra* ¶¶ 300-321) discloses this limitation. For example, as explained above, Tokuhiro teaches that the delay introduced by DR-1 for the read operation would be based on a write operation:

Thus, with the information processing apparatus 10 according to the first embodiment, for the plurality of SDRAMs of SDRAM-1 to SDRAM-n to which the clock signal line is wired through the daisy chain connection, the input times of the respective data signals DQ output from the SDRAM-1 to the SDRAM-n, to which the clock signal line is wired through the daisy chain connection, can be easily matched with one another by ***setting***, based on the first delay time Dt1 set by ***utilizing the write leveling function, the second delay time*** Dt2 for each data signal DQ input from the SDRAM ***in the read operation***.

EX1006 (Tokuhiro), 18:53-63. Tokuhiro further teaches, for example, that the write operation used to set the delay time can include receiving signals, such as data strobe signals:

The term "write leveling function" refers to the function of sampling the clock signal CK by ***using the data strobe signal DQS*** output from the memory controller 90, detecting the phase relationship between the data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.

Id., 2:13-18.

325. As explained above, there are two different obvious ways that the combination of Hiraishi and Tokuhiro could be implemented to use the delay from write operations to determine the delays for subsequent read operations depending on whether the system memory controller or the module controller programs the read delays into the data buffers. *See supra* ¶¶ 310-321. Either way, in the combination of Hiraishi and Tokuhiro, the modified data register buffer 300-0 would thus disclose “*wherein the first predetermined amount [e.g., applied by added delay elements DR-1] is determined based at least on signals [e.g., data strobe signal DQS from the earlier write operation] received by the first data buffer during one or more previous operations [e.g., the earlier write operation as discussed above, ¶¶ 300-321].*”

5. Claim 2

326. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 2. Claim limitations 2[a], 2[b], 2[d], and 2[e] are disclosed by Hiraishi as previously explained, *supra* ¶¶ 152-155, 157-160. Claim limitations 2[c] and 2[f] are satisfied by the combination of Hiraishi and Tokuhiro, *supra* ¶¶ 271-321, as explained below in more detail.

a) 2[c]: “*delay the second read strobe by a second predetermined amount to generate a second delayed read strobe,*”

327. Hiraishi as modified in combination with Tokuhiro discloses this limitation. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim 1[f]. See *supra* ¶ 323. The “*second data buffer*” [e.g., data register buffer circuit 300-8] as modified in the combination with Tokuhiro would “*delay the second read strobe by a second predetermined amount to generate a second delayed read strobe*” in the same manner as described for the *first data buffer* above.

b) 2[f]: “*wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.*”

328. Hiraishi as modified in combination with Tokuhiro discloses this limitation. An analogous determination for the “*first predetermined amount*” [e.g., the amount of delay imposed by data register buffer circuit 300-0] is described

above for claim 1[i]. *See supra* ¶¶ 324-325. The “*second predetermined amount*” [e.g., the amount of delay imposed by data register buffer circuit 300-8] can be determined in a manner similar to the “*first predetermined amount*” addressed above. Thus, for the same reasons, Hiraishi as modified in combination with Tokuhiro discloses this limitation.

6. Claim 3

329. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321), further in view of Ellsberry, discloses and renders obvious claim 3. Claim limitations 3[a], 3[b], 3[c], 3[e], and 3[f] are disclosed by Hiraishi in view of Ellsberry as previously explained, *supra* ¶¶ 212-219, 221-224. Claim limitations 3[d] and 3[g] are satisfied by the combination of Hiraishi and Tokuhiro, *supra* ¶¶ 271-321, as explained below in more detail.

a) 3[d]: “delay the third read strobe by a third predetermined amount to generate a third delayed read strobe,”

330. Hiraishi as modified in combination with Tokuhiro and further in view of Ellsberry discloses this limitation. An analogous operation for the “*first data buffer*” [e.g., data register buffer circuit 300-0] is described above for claim 1[f]. *See supra* ¶ 323. The “*first data buffer*” [e.g., data register buffer circuit 300-0] as modified in the combination with Tokuhiro can “*delay the third read strobe*

by a third predetermined amount to generate a third delayed read strobe” in the same manner as described for the “first read strobe” above.

b) 3[g]: “wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.”

331. Hiraishi as modified in combination with Tokuhiro and further in view of Ellsberry discloses this limitation. An analogous determination for the “first predetermined amount” [e.g., the amount of delay imposed by data register buffer circuit 300-0] is described above for claim 1[i]. See *supra* ¶¶ 324-325. The “third predetermined amount” [e.g., the amount of delay for the second 4-bit memory device at location 200-0] can be determined in a manner similar to the “first predetermined amount” [e.g., the amount of delay for the 8-bit memory device at location 200-0] as addressed above. Thus, for the same reasons, the combination discloses this limitation.

7. Claim 4

332. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 4, as explained below.

a) 4[a]: “The memory module of claim 2, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and”

333. As explained above, Hiraishi and Tokuhiro discloses each and every limitation of claim 2. Hiraishi in combination with Tokuhiro further disclose this

limitation as well. For example, as explained above for claim 1[i], “*the signals received by the first data buffer during one or more previous operations* [e.g., the earlier write operation as discussed above, ¶¶ 300-321] *include at least a strobe signal associated with a previous operation* [e.g., data strobe signal DQS].” *Supra* ¶¶ 324-325.

b) 4[b]: “wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.”

334. Hiraishi in combination with Tokuhiro discloses this limitation. An analogous determination for the “*first data buffer*” is described above for claim 4[a]. *Supra* ¶ 333. The “*second data buffer* [data register buffer 300-8]” would receive a strobe signal corresponding to memory device 200-32 in the same manner as described above for how the “*first data buffer* [data register buffer 300-0]” would receive a strobe signal corresponding to memory device 200-0. Thus, for the same reasons described for claim 4[a], Hiraishi in combination with Tokuhiro discloses this limitation.

8. Claim 6

335. Claim 6 recites “*The memory module of claim 1, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation.*” The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders

obvious claim 6. As explained above, Hiraishi and/or Tokuhiro discloses each and every limitation of claim 1. For the same reasons stated for claim 4[a], Hiraishi in combination with Tokuhiro further discloses or renders obvious this element.

Supra ¶ 333 .

9. Claim 11

336. Claim 11 recites “*The memory module of claim 1, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.*” The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 11. As explained above, it would have been obvious to a Skilled Artisan to implement the calculation of the amount of delay (as taught by Tokuhiro) in the data register buffer 300 of Hiraishi. See *supra* ¶¶ 315-321 (discussing the second method of utilizing the teachings of Tokuhiro). Thus, in such an implementation, “*the first data buffer [e.g., data register buffer 300-0] includes circuitry [e.g., in data register control circuit 320] that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.*”

10. Claim 14

337. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 14. Claim limitations 14[pre]

through 14[i], 14[k], and 14[l] are disclosed by Hiraishi as previously explained, *supra* ¶¶ 179-190, 192-193. Claim limitations 14[j] and 14[m] are also met by the combination of Hiraishi and Tokuhiro, for the same reasons stated above for claims 1[f] and 1[i], respectively. *Supra* ¶¶ 323-325.

11. Claim 15

338. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 15. Claim limitations 15[a] through 15[c], 15[e], and 15[f] are disclosed by Hiraishi as previously explained, *supra* ¶¶ 195-197, 199-200. Claim limitations 15[d] and 15[g] are also met by the combination of Hiraishi and Tokuhiro, for the same reasons stated above for claims 2[c] and 2[f], respectively. *Supra* ¶¶ 327-328.

12. Claim 16

339. The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321), further in view of Ellsberry, discloses and renders obvious claim 16. Claim limitations 16[a], 16[b], 16[d] and 16[e] are disclosed by Hiraishi as previously explained, *supra* ¶¶ 229, 230, 232, 233. Claim limitations 16[c] and 16[f] are also met by the combination of Hiraishi and Tokuhiro, further in view of Ellsberry, for the same reasons stated above for claims 3[d] and 3[g], respectively. *Supra* ¶¶ 330-331.

13. Claim 17

The combination of Hiraishi and Tokuhiro explained above (*supra* ¶¶ 271-321) discloses and renders obvious claim 17, as explained below.

c) 17[a]: “The method of claim 15, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and”

340. As explained above, Hiraishi and Tokuhiro discloses each and every limitation of claim 15. For the same reasons stated for claim 4[a], Hiraishi alone and/or in combination with Tokuhiro further disclose or render obvious this element. *Supra* ¶ 333.

d) 17[b]: “the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.”

341. For the same reasons stated for claim 4[b], Hiraishi alone and/or in combination with Tokuhiro further disclose or render obvious this element. *Supra* ¶ 334.

14. Claims 5, 7-10, 12, 13, 18-20

342. As previously explained, claims 5, 7-10, 12, 13, 18-20 are rendered obvious by Hiraishi, alone or further in view of Butt, Ellsberry, and/or Kim. See *supra* ¶¶ 168-175, 178, 204-211, 227, 228, and 235-269. Thus, the combination of Hiraishi in view of Tokuhiro described above renders obvious these claims alone or further in view of Ellsberry and/or Kim for the same reasons.

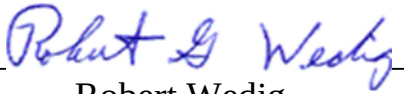
Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

* * *

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

I, Robert Wedig, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: March 14, 2022


Robert Wedig

APPENDIX A

Listing of Challenged Claims

Ref. #	Listing of Challenged Claims
1[pre]	1. A memory module operable in a computer system to communicate with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module comprising:
1[a]	a module board having edge connections to be coupled to respective signal lines in the memory bus;
1[b]	a module control device on the module board configurable to receive input C/A signals corresponding to a memory read operation via the C/A signal lines and to output registered C/A signals in response to the input C/A signals and to output module control signals;
1[c1]	memory devices arranged in multiple ranks on the module board and coupled to the module control device via module C/A signal lines that conduct the registered C/A signals
1[c2]	wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is configurable to output at least a first section of the read data and at least a first read strobe; and
1[d]	data buffers on the module board and coupled between the edge connections and the memory devices, wherein a respective data buffer of the data buffers is coupled to at least one respective memory device in each of the multiple ranks and is configurable to receive the module control signals from the module control device, and
1[e]	wherein a first data buffer of the data buffers is coupled to the first memory device and is configurable to, in response to one or more of the module control signals:
1[f]	delay the first read strobe by a first predetermined amount to generate a first delayed read strobe.
1[g]	sample the first section of the read data using the first delayed read strobe; and

Ref. #	Listing of Challenged Claims
1[h]	transmit the first section of the read data to a first section of the data bus;
1[i]	wherein the first predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.
2[a]	2. The memory module of claim 1, wherein a second memory device in the selected rank is configurable to output at least a second section of the read data and at least a second read strobe, and
2[b]	wherein the data buffers further include a second data buffer configurable to, in response to the one or more of the module control signals:
2[c]	delay the second read strobe by a second predetermined amount to generate a second delayed read strobe;
2[d]	sample the second section of the read data using the second delayed read strobe; and
2[e]	transmit the second section of the read data to a second section of the data bus;
2[f]	wherein the second predetermined amount is determined based at least on signals received by the second data buffer during one or more previous operations.
3[a]	3. The memory module of claim 2, wherein a third memory device in the selected rank is configurable to output a third section of the read data and a third read strobe,
3[b]	wherein each of the first section, the second section, and the third section of the read data is 4-bit wide, and
3[c]	wherein the first data buffer is further coupled to the third memory device and is further configurable to, in response to the one or more of the module control signals:

Ref. #	Listing of Challenged Claims
3[d]	delay the third read strobe by a third predetermined amount to generate a third delayed read strobe;
3[e]	sample the third section of the read data using the third delayed read strobe concurrently with sampling the first section of the read data using the first delayed read strobe; and
3[f]	transmit the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;
3[g]	wherein the third predetermined amount is determined based at least on signals received by the first data buffer during one or more previous operations.
4[a]	4. The memory module of claim 2, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and
4[b]	wherein the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation
5	5. The memory module claim 2, wherein each of the first section and the second section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.
6	6. The memory module of claim 1, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation.
7[a]	7. The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and output a module clock signal, and
7[b1]	wherein the first data buffer is further configurable to: receive the module clock signal;

Ref. #	Listing of Challenged Claims
7[b2]	generate a local clock signal having a programmable phase relationship with the module clock signal; and
7[b3]	output the local clock signal;
7[c]	wherein the first memory device is configurable to receive the local clock signal and to output the first section of the read data and first read strobe in accordance with the local clock signal.
8[a]	8. The memory module of claim 1, wherein the module control device is further configurable to receive a system clock signal and
8[b]	output a module clock signal together with the module control signals to the data buffers, and
8[c]	wherein the first data buffer further includes receiver circuits corresponding to respective ones of the module control signals, a respective receiver circuit for a respective module control signal including a metastability detection circuit configurable to generate one or more metastability indicators indicating a metastability condition in the respective module control signals with respect to the module clock signal.
9[a]	9. The memory module of claim 8, where-in the metastability detection circuit is further configurable to generate at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal, and
9[b]	wherein the respective receiver circuit further includes a signal selection circuit configurable to receive the module clock signal and the at least one delayed version of the module clock signal, and
9[c]	to select a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least a first metastability indicator of the one or more metastability indicators.

Ref. #	Listing of Challenged Claims
10[a]	10. The memory module of claim 9, wherein the signal selection circuit is further configurable to receive the respective module control signal and the at least one delayed version of the respective module control signal, and to
10[b]	select a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on a second metastability indicator of the one or more metastability indicators; and
10[c]	wherein the respective receiver circuit further includes a sampler that samples a selected module control signal according to a selected module clock signal and outputs received respective module control signal.
11	11. The memory module of claim 1, wherein the first data buffer includes circuitry that determines the first predetermined amount based at least on the signals received by the first data buffer during one or more previous operations.
12	12. The memory module of claim 1, wherein the first section of the read data is 4-bit wide, and wherein the at least one respective memory device in each of the multiple ranks includes one memory device having a bit width of 8 or two memory devices each having a bit width of 4.
13	13. The memory module of claim 1, wherein the memory devices are selected from the group consisting of dynamic random-access memory, synchronous dynamic random-access memory, and double-data-rate dynamic random-access memory.
14[pre]	14. A method, comprising:
14[a]	at a memory module in a computer system and operable to communicate data with a memory controller of the computer system via a memory bus including control and address (C/A) signal lines and a data bus, the memory module including

Ref. #	Listing of Challenged Claims
14[b]	a module board having edge connections to be coupled to respective signal lines in the memory bus, a module control device on the module board,
14[c1]	memory devices arranged in multiple ranks on the module board and coupled to the module control device, and
14[c2]	data buffers on the module board and coupled between the edge connections and the memory devices, the data buffers including a first data buffer,
14[d]	wherein each respective data buffer is coupled to one respective memory device having a bit width of 8 or two respective memory devices each having a bit width of 4 in each of the multiple ranks;
14[e]	receiving, at the module control device, input C/A signals corresponding to a memory read operation via the C/A signal lines;
14[f1]	outputting, at the module control device, registered C/A signals in response to the input C/A signals,
14[f2]	wherein the registered C/A signals cause a selected rank of the multiple ranks to perform the memory read operation by outputting read data and read strobes associated with the memory read operation, and wherein a first memory device in the selected rank is coupled to the first data buffer and is configurable to output at least a first section of the read data and at least a first read strobe;
14[g]	outputting, at the module control device, module control signals;
14[h]	receiving, at each of the data buffers, the module control signals from the module control device;
14[i]	the method further comprising, at the first data buffer, in response to one of more of the module control signals:
14[j]	delaying the first read strobe by a first predetermined amount to generate a first delayed read strobe;

Ref. #	Listing of Challenged Claims
14[k]	sampling the first section of the read data using the first delayed read strobe; and
14[l]	transmitting the first section of the read data to a first section of the data bus; and
14[m]	the method further comprising, before receiving the input C/A signals corresponding to the memory read operation at the module control device, determining the first predetermined amount based at least on signals received by the first data buffer.
15[a]	15. The method of claim 14, wherein the data buffers further include a second data buffer, and
15[b]	wherein a second memory device in the selected rank is coupled to the second data buffer and is configurable to output at least a second section of the read data and at least a second read strobe,
15[c]	the method further comprising, at the second data buffer, in response to the one or more of the module control signals:
15[d]	delaying the second read strobe by a second predetermined amount to generate a second delayed read strobe;
15[e]	sampling the second section of the read data using the second delayed read strobe; and
15[f]	transmitting the second section of the read data to a second section of the data bus;
15[g]	wherein the second predetermined amount is determined based on signals received by the second data buffer during one or more previous operations.
16[a]	16. The method of claim 15, wherein a third memory device in the selected rank is coupled to the first data buffer and is configurable to output a third section of the read data and a third read strobe,
16[b]	the method further comprising, at the first data buffer, in response to the one or more of the module control signals:

Ref. #	Listing of Challenged Claims
16[c]	delaying the third read strobe by a third predetermined amount to generate a third delayed read strobe;
16[d]	sampling the third section of the read data using the third delayed read strobe concurrently with receiving the first section of the read data using the first delayed read strobe; and
16[e]	transmitting the third section of the read data to a third section of the data bus concurrently with transmitting the first section of the read data to the first section of the data bus;
16[f]	wherein the third predetermined amount is determined based on the signals received by the first data buffer during one or more previous operations.
17[a]	17. The method of claim 15, wherein the signals received by the first data buffer during one or more previous operations include at least a strobe signal associated with a previous operation, and
17[b]	the signals received by the second data buffer during one or more previous operations include at least another strobe signal associated with the previous operation.
18[a]	18. The method of claim 14, further comprising:
18[b]	receiving, at the module control device, a system clock signal concurrently with receiving the input C/A signals;
18[c]	outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
18[d]	receiving, at the first data buffer, the module clock signal;
18[e]	generating, at the first data buffer, a local clock signal having a programmable phase relationship with the module clock signal; and
18[f]	outputting, at the first data buffer, the local clock signal;
18[g]	receiving, at the first memory device, the local clock signal; and

Ref. #	Listing of Challenged Claims
18[h]	outputting, at the first memory device, the first section of the read data and first read strobe in accordance with the local clock signal.
19[a]	19. The method of claim 14, further comprising: receiving, at the module control device, a system clock signal concurrently with receiving the input control and address signal;
19[b]	outputting, at the module control device, a module clock signal concurrently with outputting the module control signal;
19[c]	generating, at the first data buffer, one or more metastability indicators indicating a metastability condition in a respective module control signal of the module control signals with respect to the module clock signal.
20[a]	20. The method of claim 19, further comprising, at the first data buffer: generating at least one delayed version of the module clock signal, and at least one delayed version of the respective module control signal;
20[b]	selecting a clock signal from among the module clock signal and the at least one delayed version of the module clock signal based on at least one of the metastability indicators;
20[c]	selecting a module control signal from among the respective module control signal and the at least one delayed version of the respective module control signal based at least on another metastability indicator; and
20[d]	sampling the selected module control signal according to the selected module clock signal to output received respective module control signal.

APPENDIX B

Listing of Materials Considered

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

Exhibit #	Reference Name
1001	U.S. Patent No. 10,860,506
1002	File History of U.S. Patent No. 10,860,506
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. 2010/0309706 to Hiraishi
1006	U.S. Patent No. 8,020,022 to Tokuhiro
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry
1008	U.S. Patent No. 6,184,701 to Kim
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	U.S. Patent Pub. No. 2011/0062999 to Nimaiyar
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

Exhibit #	Reference Name
1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., Memory Systems: Cache, DRAM, Disk (2008) (excerpts)
1022	Harold S. Stone, Microcomputer Interfacing (1982)
1023	Microsoft Computer Dictionary 334 (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to '632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 5,036,221 to Brucculeri
1028	U.S. Patent No. 6,906,555 to Ma
1029	U.S. Patent Pub. No. 2007/0008791 to Butt
1030	U.S. Patent No. 7,036,053 to Zumkehr
1031	U.S. Patent No. 9,824,035
1032	File History of U.S. Patent No. 9,824,035
1033	U.S. Patent No. 10,268,608
1034	File History of U.S. Patent No. 10,268,608
1035	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1036	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, <i>Samsung</i>

Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506

Exhibit #	Reference Name
	<i>Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1037	Netlist’s motion to dismiss the First Amended Complaint, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1038	Complaint in <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1039	JEDEC DDR4DB02 Data Buffer Definition Standard, JESD82-32A (Aug. 2019)
1040	Order extending response to complaint to April 12, 2022, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. filed Dec. 29, 2021)
1041	Micron’s proposed claim constructions, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 6:21-cv-00431 (W.D. Tex. Dec. 23, 2021)
1042	Netlist’s proposed claim constructions, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 6:21-cv-00431 (W.D. Tex. Dec. 23, 2021)