JEDEC STANDARD

DDR4 SDRAM

JESD79-4

SEPTEMBER 2012

JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the JEDEC legal counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby a JEDEC standard or publication may be further processed and ultimately become an ANSI standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC at the address below, or refer to www.jedec.org under Standards and Documents for alternative contact information.

Published by

©JEDEC Solid State Technology Association 2012

3103 North 10th Street

Suite 240 South

Arlington, VA 22201-2107

This document may be downloaded free of charge; however JEDEC retains the copyright on this material. By downloading this file the individual agrees not to charge for or resell the resulting material.

PRICE: Contact JEDEC

Printed in the U.S.A.

All rights reserved

PLEASE!

DON'T VIOLATE
THE
LAW!

This document is copyrighted by JEDECand may not be
reproduced without permission.

For information, contact:

JEDEC Solid State Technology Association
3103 North 10th Street, Suite 240 South
Arlington, Virginia 22201-2107
or call (703) 907-7559

DDR4 SDRAM STANDARD

(From JEDEC Board Ballot JCB-12-40, formulated under the cognizance of the JC-42.3 Subcommittee on DRAM Memories.)

Contents

1. Scope 1
2. DDR4 SDRAM Package Pinout and Addressing 2
  2.1 DDR4 SDRAM Row for X4,X8 and X16 2
  2.2 DDR4 SDRAM Ball Pitch 2
  2.3 DDR4 SDRAM Columns for X4,X8 and X16 2
  2.4 DDR4 SDRAM X4/8 Ballout using MO-207 2
  2.5 DDR4 SDRAM X16 Ballout using MO-207 3
  2.6 Pinout Description 5
  2.7 DDR4 SDRAM Addressing 7
3. Functional Description 8
  3.1 Simplified State Diagram 8
  3.2 Basic Functionality 9
  3.3 RESET and Initialization Procedure 10
    3.3.1 Power-up Initialization Sequence 10
    3.3.2 Reset Initialization with Stable Power 11
  3.4 Register Definition 12
    3.4.1 Programming the mode registers 12
  3.5 Mode Register 13
4. DDR4 SDRAM Command Description and Operation 24
  4.1 Command Truth Table 24
  4.2 CKE Truth Table 25
  4.3 Burst Length, Type and Order 26
    4.3.1 BL8 Burst order with CRC Enabled 26
  4.4 DLL-off Mode & DLL on/off Switching procedure 27
    4.4.1 DLL on/off switching procedure 27
    4.4.2 DLL “on” to DLL “off” Procedure 27
    4.4.3 DLL “off” to DLL “on” Procedure 28
  4.5 DLL-off Mode 29
  4.6 Input Clock Frequency Change 30
  4.7 Write Leveling 31
    4.7.1 DRAM setting for write leveling & DRAM termination function in that mode 32
    4.7.2 Procedure Description 33
    4.7.3 Write Leveling Mode Exit 34
  4.8 Temperature controlled Refresh modes 34
    4.8.1 Normal temperature mode 34
    4.8.2 Extended temperature mode 34
  4.9 Fine Granularity Refresh Mode 35
    4.9.1 Mode Register and Command Truth Table 35
    4.9.2 tREFI and tRFC parameters 35
    4.9.3 Changing Refresh Rate 36
    4.9.4 Usage with Temperature Controlled Refresh mode 36
    4.9.5 Self Refresh entry and exit 37
  4.10 Multi Purpose Register 37
    4.10.1 DQ Training with MPR 37
    4.10.2 MR3 definition 37
    4.10.3 MPR Reads 38
    4.10.4 MPR Writes 40
    4.10.5 MPR Read Data format 43
  4.11 Data Mask(DM), Data Bus Inversion (DBI) and TDQS 48
  4.12 ZQ Calibration Commands 50

Samsung Electronics Co., Ltd.
Ex. 1054, p. i

4.12.1 ZQ Calibration Description 50
4.13 DQ Vref Training 51
4.14 Per DRAM Addressability 56
4.15 CAL Mode (CS_n to Command Address Latency) 59
4.15.1 CAL Mode Description 59
4.16 CRC 61
4.16.1 CRC Polynomial and logic equation 61
4.16.2 CRC data bit mapping for x8 devices 63
4.16.3 CRC data bit mapping for x4 devices 63
4.16.4 CRC data bit mapping for x16 devices 63
4.16.5 Write CRC for x4, x8 and x16 devices 64
4.16.6 CRC Error Handling 64
4.16.7 CRC Frame format with BC4 65
4.16.8 Simultaneous DM and CRC Functionality 68
4.17 Command Address Parity(CA Parity) 68
4.17.1 CA Parity Error Log Readout 74
4.18 Control Gear Down Mode 74
4.19 DDR4 Key Core Timing 77
4.20 Programmable Preamble 80
4.20.1 Write Preamble 80
4.20.2 Read Preamble 81
4.20.3 Read Preamble Training 82
4.21 Postamble 82
4.21.1 Read Postamble 82
4.21.2 Write Postamble 82
4.22 ACTIVATE Command 82
4.23 Precharge Command 83
4.24 Read Operation 83
4.24.1 READ Timing Definitions 83
4.24.1.1 READ Timing; Clock to Data Strobe relationship 85
4.24.1.2 READ Timing; Data Strobe to Data relationship 86
4.24.1.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation 87
4.24.1.4 tRPRE Calculation 88
4.24.1.5 tRPST Calculation 89
4.24.2 READ Burst Operation 90
4.24.3 Burst Read Operation followed by a Precharge 101
4.24.4 Burst Read Operation with Read DBI (Data Bus Inversion) 103
4.24.5 Burst Read Operation with Command/Address Parity 104
4.24.6 Read to Write with Write CRC 105
4.24.7 Read to Read with CS to CA Latency 106
4.25 Write Operation 107
4.25.1 Write Burst Operation 107
4.26 Refresh Command 123
4.27 Self refresh Operation 124
4.27.1 Low Power Auto Self Refresh 126
4.28 Power down Mode 127
4.28.1 Power-Down Entry and Exit 127
4.28.2 Power-Down clarifications 132
4.29 Maximum Power Saving Mode 132
4.29.1 Maximum power saving mode 132
4.29.2 Mode entry 132
4.29.3 CKE transition during the mode 133
4.29.4 Mode exit 134
4.29.5 Timing parameter bin of Maximum Power Saving Mode for DDR4-1600/1866/2133/2400/2666/3200 134
4.30 Connectivity Test Mode 135
4.30.1 Introduction 135
4.30.2 Pin Mapping 135
4.30.3 Logic Equations 136
4.30.3.1 Min Term Equations 136

Samsung Electronics Co., Ltd.
Ex. 1054, p. ii

4.30.3.2 Output equations for x16 devices 136
4.30.3.3 Output equations for x8 devices 136
4.30.3.4 Output equations for x4 devices 136
4.30.4 Timing Requirement 137
4.31 CLK to Read DQS timing parameters 137
5. On-Die Termination 139
5.1 ODT Mode Register and ODT State Table 139
5.2 Synchronous ODT Mode 141
5.2.1 ODT Latency and Posted ODT 142
5.2.2 Timing Parameters 142
5.2.3 ODT during Reads: 143
5.3 Dynamic ODT 144
5.3.1 Functional Description 144
5.3.2 ODT Timing Diagrams 145
5.4 Asynchronous ODT mode 146
5.5 ODT buffer disabled mode for Power down 147
5.6 ODT Timing Definitions 148
5.6.1 Test Load for ODT Timings 148
5.6.2 ODT Timing Definitions 148
6. Absolute Maximum Ratings 150
7. AC & DC Operating Conditions 151
7.1 AC and DC Input Measurement Levels: VREF Tolerances 151
7.2 AC and DC Logic Input Levels for Differential Signals 152
7.2.1 Differential signal definition 152
7.2.2 Differential swing requirements for clock (CK_t - CK_c) 152
7.2.3 Single-ended requirements for differential signals 153
7.2.4 Address and Control Overshoot and Undershoot specifications 153
7.2.5 Clock Overshoot and Undershoot Specifications 154
7.2.6 Data, Strobe and Mask Overshoot and Undershoot Specifications 154
7.3 Slew Rate Definitions for Differential Input Signals (CK) 155
7.4 Differential Input Cross Point Voltage 156
7.5 CMOS rail to rail Input Levels 158
7.5.1 CMOS rail to rail Input Levels for RESET_n 158
8. AC and DC output Measurement levels 159
8.1 Output Driver DC Electrical Characteristics 159
8.1.1 Alert_n output Drive Characteristic 160
8.2 Single-ended AC & DC Output Levels 161
8.3 Differential AC & DC Output Levels 161
8.4 Single-ended Output Slew Rate 161
8.5 Differential Output Slew Rate 162
9. Speed Bin 163
9.0.1 Speed Bin Table Note 167
10. IDD and IDDQ Specification Parameters and Test conditions 168
10.1 IDD, IPP and IDDQ Measurement Conditions 168
10.2 IDD Specifications 183
11. Input/Output Capacitance 185
12. Electrical Characteristics & AC Timing 187
12.1 Reference Load for AC Timing and Output Slew Rate 187
12.2 tREFI 187
12.3 Timing Parameters by Speed Grade 188
12.4 The DQ input receiver compliance mask for voltage and timing is shown in the figure below 198
12.5 DDR4 Function Matrix 203

Samsung Electronics Co., Ltd.
Ex. 1054, p. iii

Samsung Electronics Co., Ltd.
Ex. 1054, p. iv

1 Scope

This document defines the DDR4 SDRAM specification, including features, functionalities, AC and DC characteristics, packages, and ball/signal assignments. The purpose of this Standard is to define the minimum set of requirements for JEDEC compliant 2 Gb through 16 Gb for x4, x8, and x16 DDR4 SDRAM devices. This standard was created based on the DDR3 standardn (JESD79-3) and some aspects of the DDR and DDR2 standards (JESD79, JESD79-2).

Each aspect of the changes for DDR4 SDRAM operation were considered and approved by committee ballot(s). The accumulation of these ballots were then incorporated to prepare this JESD79-4 specifications, replacing whole sections and incorporating the changes into Functional Description and Operation.

2 DDR4 SDRAM Package Pinout and Addressing

2.1 DDR4 SDRAM Row for X4, X8 and X16

The DDR4 SDRAM x4/x8 component will have 13 electrical rows of balls. Electrical is defined as rows that contain signal ball or power/ground balls. There may be additional rows of inactive balls for mechanical support.

The DDR4 SDRAM x16 component will have 16 electrical rows of balls. There may be additional rows of inactive balls for mechanical support.

2.2 DDR4 SDRAM Ball Pitch

The DDR4 SDRAM component will use a ball pitch of 0.8 mm by 0.8 mm.
The number of depopulated columns is 3.

2.3 .DDR4 SDRAM Columns for X4,X8 and X16

The DDR4 SDRAM x4/x8 and x16 component will have 6 electrical columns of balls in 2 sets of 3 columns.
There will be coulmns between the electrical columns where there are no balls populated. The number of these columns is 3.
Electrical is defined as columns that contain signal ball or power/ground balls. There may be additional columns of inactive balls for mechanical support.

2.4 DDR4 SDRAM X4/8 Ballout using MO-207

	1	2	3	4	5	6	7	8	9	
A	VDD	VSSQ	TDQS_c[3]				DM_n, DBI_n TDQS_t[2], (NC)[1]	VSSQ	VSS	A
B	VPP	VDDQ	DQS_c				DQ1	VDDQ	ZQ	B
C	VDDQ	DQ0	DQS_t				VDD	VSS	VDDQ	C
D	VSSQ	DQ4 (NC)[1]	DQ2				DQ3	DQ5 (NC)[1]	VSSQ	D
E	VSS	VDDQ	DQ6 (NC)[1]				DQ7 (NC)[1]	VDDQ	VSS	E
F	VDD	(C2)[5] ODT1[6]	ODT				CK_t	CK_c	VDD	F
G	VSS	(C0)[5] CKE1[6]	CKE				CS_n	(C1)[5] (CS1_n)[6]	TEN (NC)[7]	G
H	VDD	WE_n A14	ACT_n				CAS_n A15	RAS_n A16	VSS	H
J	VREFCA	BG0	A10 AP				A12 BC_n	BG1	VDD	J
K	VSS	BA0	A4				A3	BA1	VSS	K
L	RESET_n	A6	A0				A1	A5	ALERT_n	L
M	VDD	A8	A2				A9	A7	VPP	M
N	VSS	A11	PAR				A17 (NC)[4]	A13	VDD	N

NOTE 1 These pins are not connected for the X4 configuration.

NOTE 2 TDQS_t is not valid for the x4 configuration.

NOTE 3 TDQS_c is not valid for the x4 configuration.

NOTE 4 A17 is only defined for the x4 configuration.

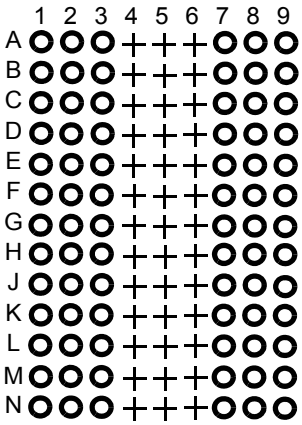
NOTE 5 These pins are for stacked component such as 3DS. For mono package, these pins are NC.

NOTE 6 ODT1 / CKE1 /CS1_n are used together only for DDP.

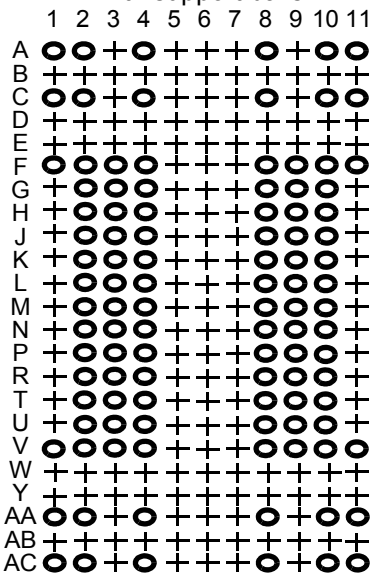
NOTE 7 TEN is optional for 8Gb and above. This pin is not connected if TEN is not supported.

Figure 1 — DDR4 Ball Assignments for the x4/8 component

MO-207 Variation DT-z (x4)



MO-207 Variation DW-z (x4)
with support balls



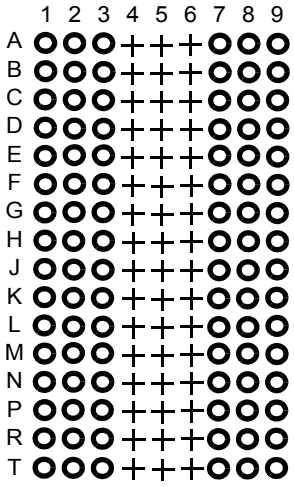
Populated ball
Ball not populated

2.5 DDR4 SDRAM X16 Ballout using MO-207

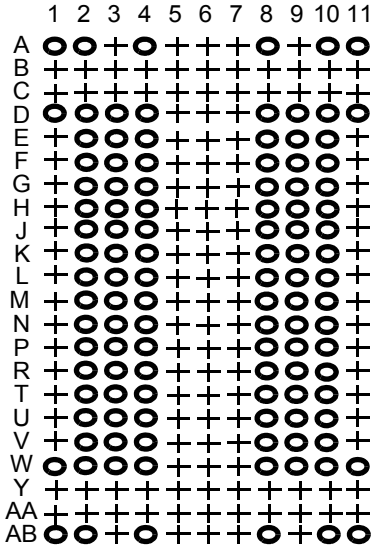
	1	2	3	4	5	6	7	8	9	
A	VDDQ	VSSQ	DQU0				DQSU_c	VSSQ	VDDQ	A
B	VPP	VSS	VDD				DQSU_t	DQU1	VDD	B
C	VDDQ	DQU4	DQU2				DQU3	DQU5	VSSQ	C
D	VDD	VSSQ	DQU6				DQU7	VSSQ	VDDQ	D
E	VSS	DMU_n/ DBIU_n	VSSQ				DML_n DBIL_n	VSSQ	VSS	E
F	VSSQ	VDDQ	DQSL_c				DQL1	VDDQ	ZQ	F
G	VDDQ	DQL0	DQSL_t				VDD	VSS	VDDQ	G
H	VSSQ	DQL4	DQL2				DQL3	DQL5	VSSQ	H
J	VDD	VDDQ	DQL6				DQL7	VDDQ	VDD	J
K	VSS	CKE	ODT				CK_t	CK_c	VSS	K
L	VDD	WE_n/ A14	ACT_n				CS_n	RAS_n/ A16	VDD	L
M	VREFCA	BG0	A10/ AP				A12/ BC_n	CAS_n/ A15	VSS	M
N	VSS	BA0	A4				A3	BA1	TEN	N
P	RESET_n	A6	A0				A1	A5	ALERT_n	P
R	VDD	A8	A2				A9	A7	VPP	R
T	VSS	A11	PAR				NC	A13	VDD	T

Figure 2 — DDR4 Ball Assignments for the x16 component

MO - 207 Variation DU-z (x16)



MO-207 Variation DY-z (x16)
with support balls



O Populated ball
+ Ball not populated

2.6 Pinout Description

Symbol	Type	Function
CK_t, CK_c	Input	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CKE, (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t,CK_c, ODT and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
CS_n, (CS1_n)	Input	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code.
C0,C1,C2	Input	Chip ID : Chip ID is only used for 3DS for 2,4,8high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code
ODT, (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c and DM_n/DBI_n/TDQS_t, NU/TDQS_c (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x8 configurations. For x16 configuration ODT is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n, and DML_n signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM.
ACT_n	Input	Activation Command Input : ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14
RAS_n/A16. CAS_n/ A15. WE_n/A14	Input	Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, those are Addressing like A16,A15 and A14 but for non-activation command with ACT_n High, those are Command pins for Read, Write and other command defined in command truth table
DM_n/DBI_n/ TDQS_t, (DMU_n/ DBIU_n), (DML_n/ DBIL_n)	Input/Output	Input Data Mask and Data Bus Inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. DM is muxed with DBI function by Mode Register A10,A11,A12 setting in MR5. For x8 device, the function of DM or TDQS is enabled by Mode Register A11 setting in MR1. DBI_n is an input/output identifing whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 SDRAM and not inverted if DBI_n is HIGH. TDQS is only supported in X8
BG0 - BG1	Input	Bank Group Inputs : BG0 - BG1 define to which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. X4/8 have BG0 and BG1 but X16 has only BG0
BA0 - BA1	Input	Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle.
A0 - A17	Input	Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions, see other rows.The address inputs also provide the op-code during Mode Register Set commands.A17 is only defined for the x4 configuration.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge).A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / BC_n	Input	Burst Chop: A12 / BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.
RESET_n	Input	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of V_{DD},

Symbol	Type	Function
DQ	Input / Output	Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0~DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific datasheets to determine which DQ is used.
DQS_t, DQS_c, DQSU_t, DQSU_c, DQSL_t, DQSL_c	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQL0-DQL7; DQSU corresponds to the data on DQU0-DQU7. The data strobe DQS_t, DQSL_t and DQSU_t are paired with differential signals DQS_c, DQSL_c, and DQSU_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended.
TDQS_t, TDQS_c	Output	Termination Data Strobe: TDQS_t/TDQS_c is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS_t/TDQS_c that is applied to DQS_t/DQS_c. When disabled via mode register A11 = 0 in MR1, DM/DBI/TDQS will provide the data mask function or Data Bus Inversion depending on MR5; A11,12,10and TDQS_c is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
PAR	Input	Command and Address Parity Input : DDR4 Supports Even Parity check in DRAMs with MR setting. Once it's enabled via Register in MR5, then DRAM calculates Parity with ACT_n,RAS_n/A16,CAS_n/A15,WE_n/A14,BG0-BG1,BA0-BA1,A17-A0. Input parity should maintain at the rising edge of the clock and at the same time with command & address with CS_n LOW
ALERT_n	Input/Output	Alert : It has multi functions such as CRC error flag , Command and Address Parity error flag as Output signa . If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then Alert_n goes LOW for relatively long period until on going DRAM internal recovery transaction to complete. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDD on board.
TEN	Input	Connectivity Test Mode Enable : Required on X16 devices and optional input on x4/x8 with densities equal to or greater than 8Gb.HIGH in this pin will enable Connectivity Test Mode operation along with other pins. It is a CMOS rail to rail signal with AC high and low at 80% and 20% of VDD. Using this signal or not is dependent on System. This pin may be DRAM internally pulled low through a weak pull-down resistor to VSS.
NC		No Connect: No internal electrical connection is present.
VDDQ	Supply	DQ Power Supply: 1.2 V +/- 0.06 V
VSSQ	Supply	DQ Ground
VDD	Supply	Power Supply: 1.2 V +/- 0.06 V
VSS	Supply	Ground
VPP	Supply	DRAM Activating Power Supply: 2.5V (2.375V min , 2.75V max)
VREFCA	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration
NOTE Input only pins (BG0-BG1,BA0-BA1, A0-A17, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, CS_n, CKE, ODT, and RESET_n) do not supply termination.		

2.7 DDR4 SDRAM Addressing

2 Gb Addressing Table

Configuration		512 Mb x4	256 Mb x8	128 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A14	A0~A13	A0~A13
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

4 Gb Addressing Table

Configuration		1 Gb x4	512 Mb x8	256 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A15	A0~A14	A0~A14
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

8 Gb Addressing Table

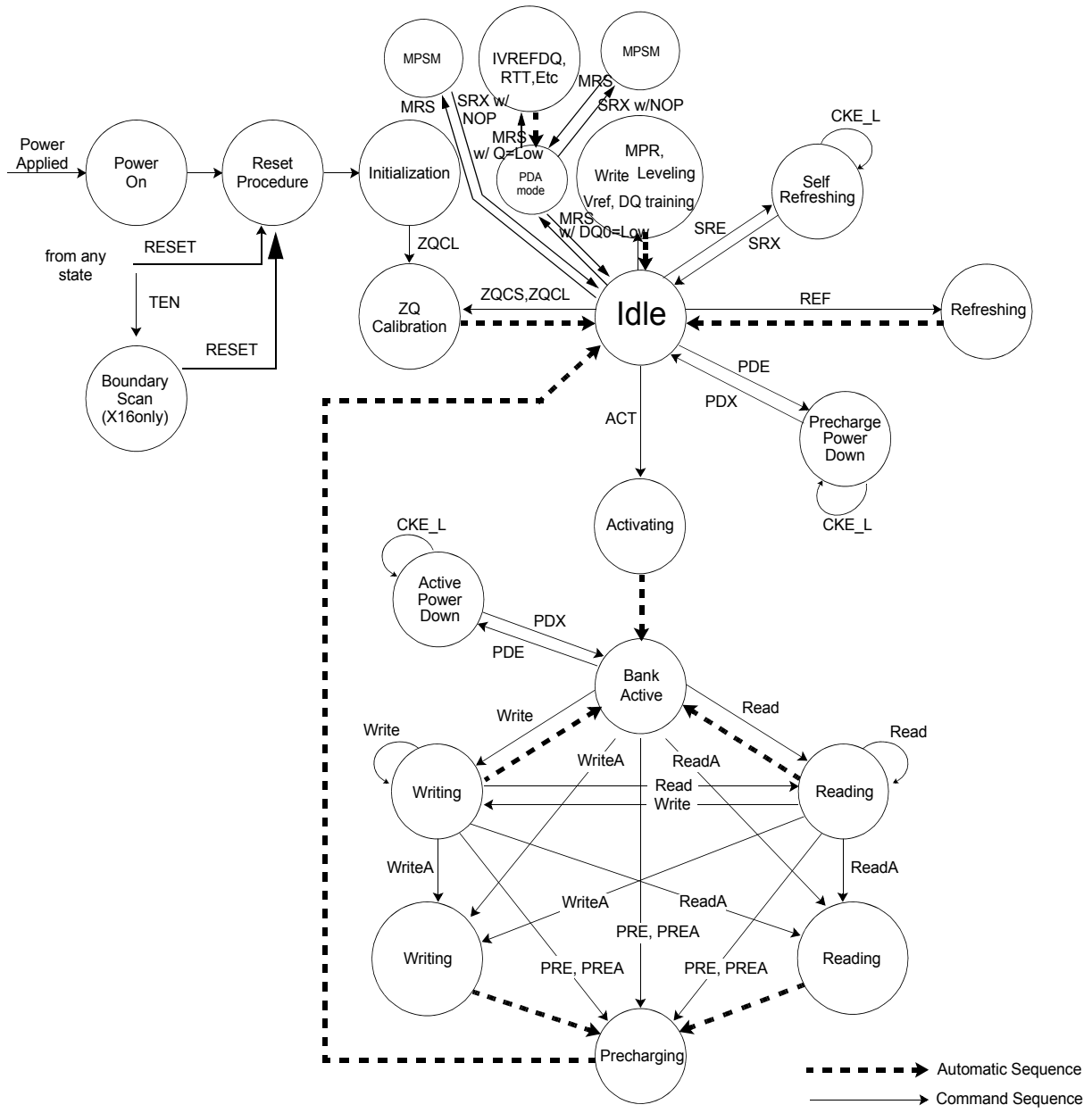
Configuration		2 Gb x4	1 Gb x8	512 Mb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A16	A0~A15	A0~A15
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

16 Gb Addressing Table

Configuration		4 Gb x4	2 Gb x8	1 Gb x16
Bank Address	# of Bank Groups	4	4	2
	BG Address	BG0~BG1	BG0~BG1	BG0
	Bank Address in a BG	BA0~BA1	BA0~BA1	BA0~BA1
Row Address		A0~A17	A0~A16	A0~A16
Column Address		A0~A9	A0~A9	A0~A9
Page size		512B	1KB	2KB

3 Functional Description

3.1 Simplified State Diagram



Abbreviation	Function	Abbreviation	Function	Abbreviation	Function
ACT	Activate	Read	RD,RDS4, RDS8	PDE	Enter Power-down
PRE	Precharge	Read A	RDA, RDAS4, RDAS8	PDX	Exit Power-down
PREA	PRECHARGE All	Write	WR, WRS4, WRS8 with/without CRC	SRE	Self-Refresh entry
MRS	Mode Register Set	Write A	WRA,WRAS4, WRAS8 with/without CRC	SRX	Self-Refresh exit
REF	Refresh, Fine granularity Refresh	RESET_n	Start RESET procedure	MPR	Multi Purpose Register
TEN	Boundary Scan Mode Enable				

NOTE This simplified State Diagram is intended to provide an overview of the possible state transitions and the commands to control them. In particular, situations involving more than on bank, the enabling or disabling of on-die termination, and some other events are not captured in full detail.

3.2 Basic Functionality

The DDR4 SDRAM is a high-speed dynamic random-access memory internally configured as sixteen-banks, 4 bank group with 4 banks for each bank group for x4/x8 and eight-banks, 2 bank group with 4 banks for each bankgroup for x16 DRAM.
The DDR4 SDRAM uses a 8n prefetch architecture to achieve high-speed operation. The 8n prefetch architecture is combined with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write operation for the DDR4 SDRAM consists of a single 8n-bit wide, four clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half clock cycle data transfers at the I/O pins.

Read and write operation to the DDR4 SDRAM are burst oriented, start at a selected location, and continue for a burst length of eight or a 'chopped' burst of four in a programmed sequence. Operation begins with the registration of an ACTIVATE Command, which is then followed by a Read or Write command. The address bits registered coincident with the ACTIVATE Command are used to select the bank and row to be activated (BG0-BG1 in x4/8 and BG0 in x16 select the bankgroup; BA0-BA1 select the bank; A0-A17 select the row; refer to "DDR4 SDRAM Addressing" on Section 2.7 for specific requirements). The address bits registered coincident with the Read or Write command are used to select the starting column location for the burst operation, determine if the auto precharge command is to be issued (via A10), and select BC4 or BL8 mode 'on the fly' (via A12) if enabled in the mode register.

Prior to normal operation, the DDR4 SDRAM must be powered up and initialized in a predefined manner.

The following sections provide detailed information covering device reset and initialization, register definition, command descriptions, and device operation.

3.3 RESET and Initialization Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly default values for the following MR settings need to be defined.

Gear down mode (MR3 A[3]) : 0 = 1/2 Rate

Per DRAM Addressability (MR3 A[4]) : 0 = Disable

Max Power Saving Mode (MR4 A[1]) : 0 = Disable

CS to Command/Address Latency (MR4 A[8:6]) : 000 = Disable

CA Parity Latency Mode (MR5 A[2:0]) : 000 = Disable

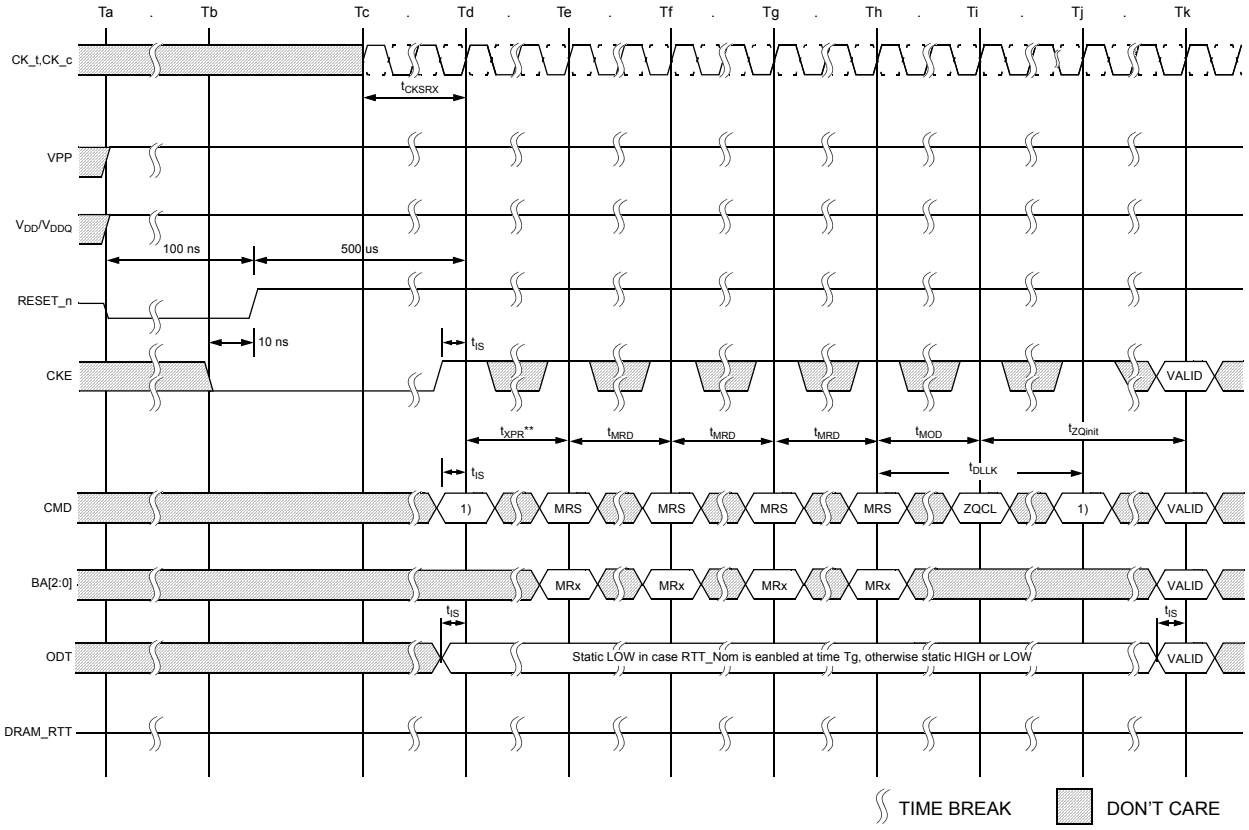
3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization and is shown in Figure 3.

1. Apply power (RESET_n is recommended to be maintained below 0.2 x VDD; all other inputs may be undefined). RESET_n needs to be maintained for minimum 200us with stable power. CKE is pulled " Low" anytime before RESET_n being de-asserted (min. time 10ns) . The power voltage ramp time between 300mV to V_{DD} min must be no greater than 200ms; and during the ramp, $V_{DD} \geq V_{DDQ}$ and $(V_{DD}-V_{DDQ}) < 0.3$volts. VPP must ramp at the same time or earlier than VDD and VPP must be equal to or higher than VDD at all times.
   - V_{DD} and V_{DDQ} are driven from a single power converter output, AND
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side. In addition, V_{TT} is limited to TBDV max once power ramp is finished, AND
   - VrefCA tracks TBD.

     or
   - Apply V_{DD} without any slope reversal before or at the same time as V_{DDQ}
   - Apply V_{DDQ} without any slope reversal before or at the same time as V_{TT} & VrefCA.
   - Apply VPP without any slope reversal before or at the same time as VDD.
   - The voltage levels on all pins other than V_{DD},V_{DDQ},V_{SS},V_{SSQ} must be less than or equal to V_{DDQ} and V_{DD} on one side and must be larger than or equal to V_{SSQ} and V_{SS} on the other side.
2. After RESET_n is de-asserted, wait for another 500us until CKE becomes active. During this time, the DRAM will start internal initialization; this will be done independently of external clocks.
3. Clocks (CK_t,CK_c) need to be started and stabilized for at least 10ns or 5tCK (which is larger) before CKE goes active. Since CKE is a synchronous signal, the corresponding setup time to clock (tIS) must be met. Also a Deselect command must be registered (with tIS set up time to clock) at clock edge Td. Once the CKE registered "High" after Reset, CKE needs to be continuously registered "High" until the initialization sequence is finished, including expiration of tDLLK and tZQinit
4. The DDR4 SDRAM keeps its on-die termination in high-impedance state as long as RESET_n is asserted. Further, the SDRAM keeps its on-die termination in high impedance state after RESET_n deassertion until CKE is registered HIGH. The ODT input signal may be in undefined state until tIS before CKE is registered HIGH. When CKE is registered HIGH, the ODT input signal may be statically held at either LOW or HIGH. If RTT_NOM is to be enabled in MR1 the ODT input signal must be statically held LOW. In all cases, the ODT input signal remains static until the power up initialization sequence is finished, including the expiration of tDLLK and tZQinit.

5. After CKE is being registered high, wait minimum of Reset CKE Exit time, tXPR, before issuing the first MRS command to load mode register. (tXPR=Max(tXS, 5nCK)]
6. Issue MRS Command to to load MR3 with all application settings(To issue MRS command to MR3, provide " Low" to BG0, "High" to BA1, BA0)
7. Issue MRS command to load MR6 with all application settings (To issue MRS command to MR6, provide "Low" to BA0, "High" to BG0, BA1)
8. Issue MRS command to load MR5 with all application settings (To issue MRS command to MR5, provide "Low" to BA1, "High" to BG0, BA0)
9. Issue MRS command to load MR4 with all application settings (To issue MRS command to MR4, provide "Low" to BA1, BA0, "High" to BG0)
10. Issue MRS command to load MR2 with all application settings (To issue MRS command to MR2, provide "Low" to BG0, BA0, "High" to BA1)
11. Issue MRS command to load MR1 with all application settings (To issue MRS command to MR1, provide "Low" to BG0, BA1, "High" to BA0)
12. Issue MRS command to load MR0 with all application settings (To issue MRS command to MR0, provide "Low" to BG0, BA1, BA0)
13. Issue ZQCL command to starting ZQ calibration
14. Wait for both tDLLK and tZQ init completed
15. The DDR4 SDRAM is now ready for read/Write training (include Vref training and Write leveling).



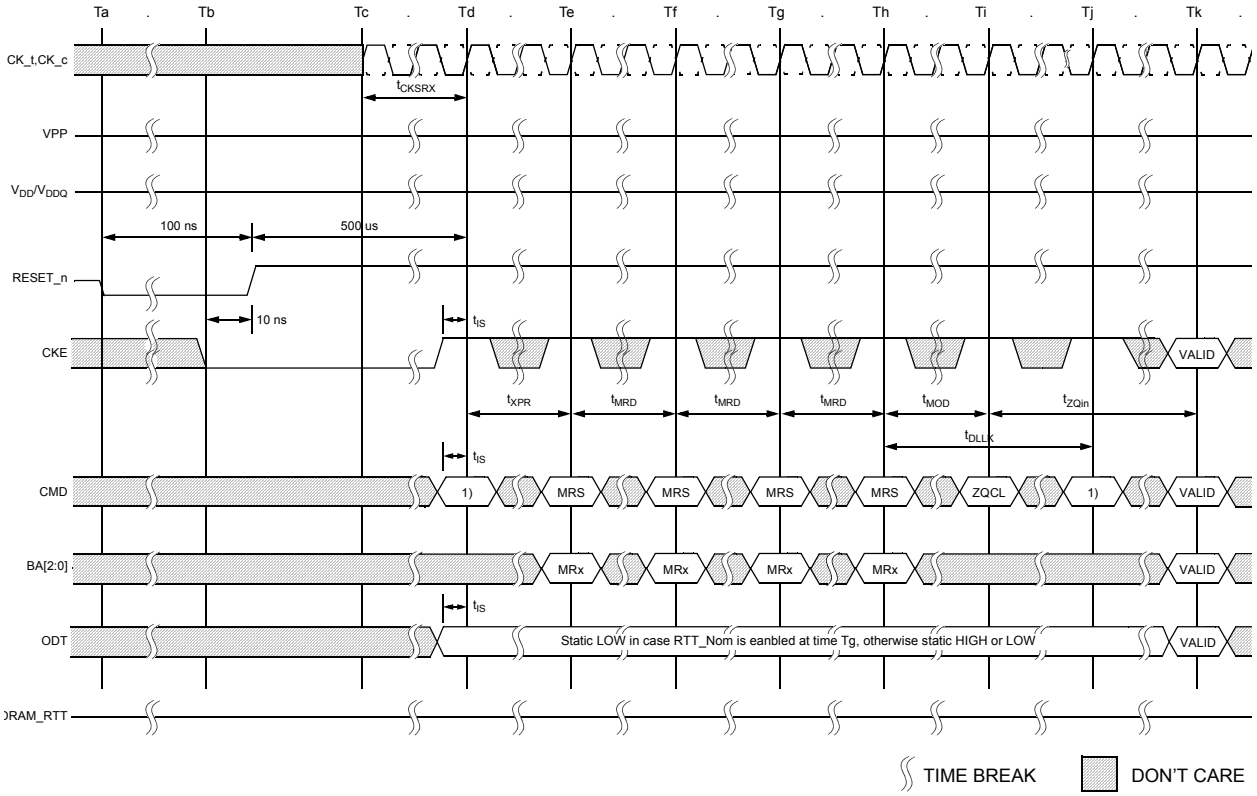
NOTE 1 From time point 'Td' until 'Tk', DES commands must be applied between MRS and ZQCL commands.
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.

Figure 3 — RESET_n and Initialization Sequence at Power-on Ramping

3.3.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization as shown in Figure 4.

1. Asserted RESET_n below 0.2 * V_{DD} anytime when reset is needed (all other inputs may be undefined). RESET_n needs to be maintained for minimum tPW_RESET. CKE is pulled "LOW" before RESET_n being de-asserted (min. time 10 ns).
2. Follow steps 2 to 10 in “Power-up Initialization Sequence” on page 13.
3. The Reset sequence is now completed, DDR4 SDRAM is ready for Read/Write training (include Vref training and Write leveling)



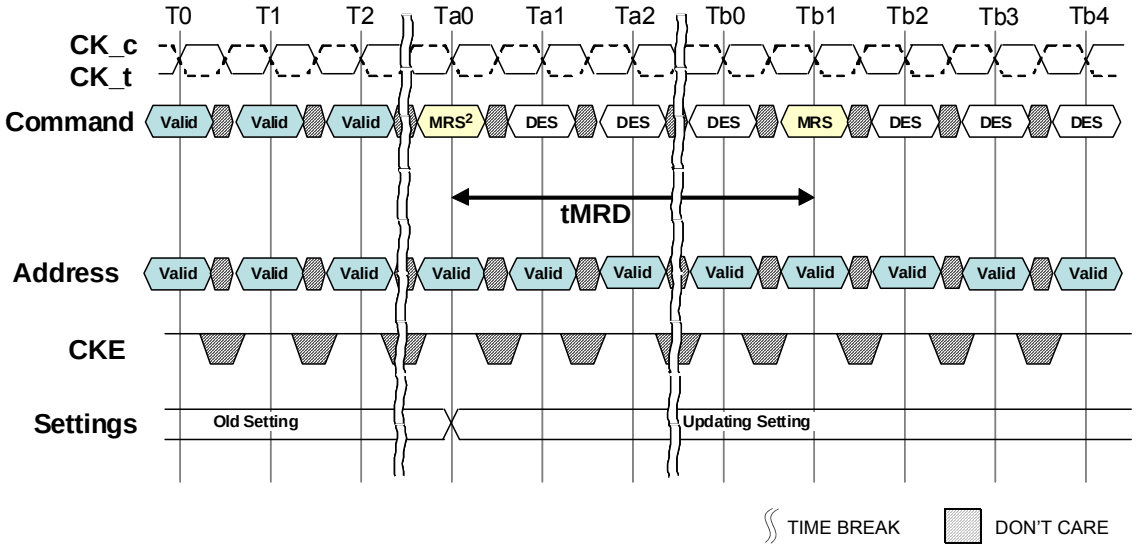
NOTE 1 From time point ‘Td’ until ‘Tk’, DES commands must be applied between MRS and ZQCL commands
NOTE 2 MRS Commands must be issued to all Mode Registers that have defined settings.

Figure 4 — Reset Procedure at Power Stable

3.4 Register Definition

3.4.1 Programming the mode registers

For application flexibility, various functions, features, and modes are programmable in seven Mode Registers, provided by the DDR4 SDRAM, as user defined variables and they must be programmed via a Mode Register Set (MRS) command. The mode registers are divided into various fields depending on the functionality and/or modes. As not all the Mode Registers (MR#) have default values defined, contents of Mode Registers must be initialized and/or re-initialized, i. e. written, after power up and/or reset for proper operation. Also the contents of the Mode Registers can be altered by re-executing the MRS command during normal operation. When programming the mode registers, even if the user chooses to modify only a sub-set of the MRS fields, all address fields within the accessed mode register must be redefined when the MRS command is issued. MRS command and DLL Reset do not affect array contents, which means these commands can be executed any time after power-up without affecting the array contents. The mode register set command cycle time, tMRD is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 5.



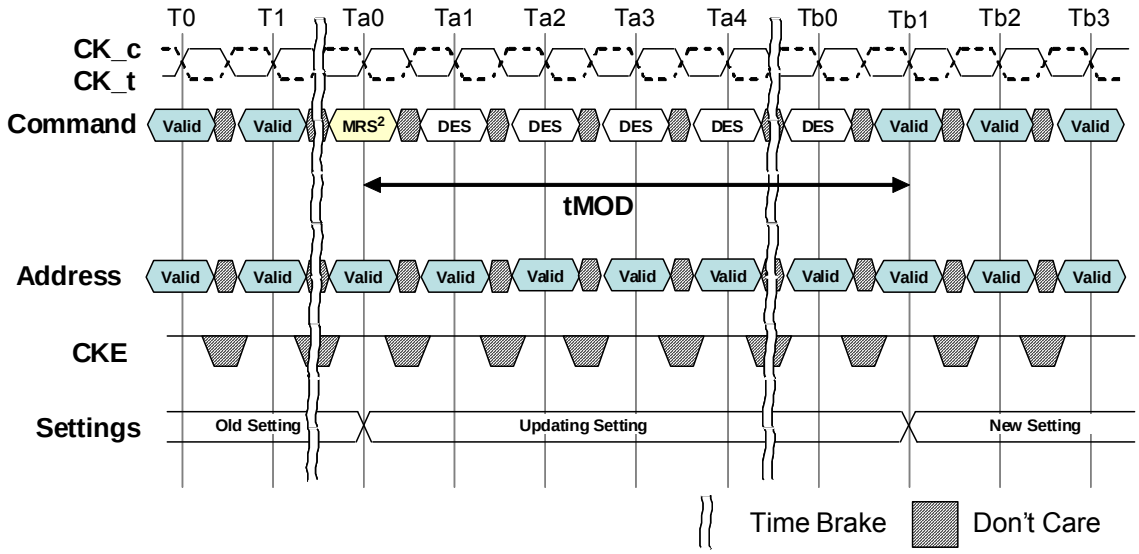
NOTE 1 This timing diagram shows C/A Parity Latency mode is "Disable" case.
NOTE 2 List of MRS commands exception that do not apply to tMRD
- Gear down mode
- C/A Parity Latency mode
- CS to Command/Address Latency mode
- Per DRAM Addressability mode
- VrefDQ training Value, VrefDQ Training mode and VrefDQ training Range

Figure 5 — tMRD Timing

Some of the Mode Register setting affect to address/command/control input functionality. These case, next MRS command can be allowed when the function updating by current MRS command completed.

This type of MRS command does not apply tMRD timing to next MRS command is listed in Note 2 of Figure 5. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

The most MRS command to Non-MRS command delay, tMOD, is required for the DRAM to update the features, and is the minimum time required from an MRS command to a non-MRS command excluding DES shown in Figure 6.



NOTE 1 This timing diagram shows CA Parity Latency mode is "Disable" case.
NOTE 2 List of MRS commands exception that do not apply to tMOD
- DLL Enable, DLL Reset
- VrefDQ training Value, internal Vref Monitor, VrefDQ Training mode and VrefDQ training Range
- Gear down mode
- Per DRAM addressability mode
- Maximum power saving mode
- CA Parity mode

Figure 6 — tMOD Timing

The mode register contents can be changed using the same command and timing requirements during normal operation as long as the DRAM is in idle state, i.e., all banks are in the precharged state with tRP satisfied, all data bursts are completed and CKE is high prior to writing into the mode register. For MRS command, If RTT_Nom function is intended to change (enable to disable and vice versa) or already enabled in DRAM MR, ODT signal must be registered Low ensuring RTT_NOM is in an off state prior to MRS command affecting RTT_NOM turn-on and off timing. Refer to note2 of Figure 6 for this type of MRS. The ODT signal may be registered high after tMOD has expired. ODT signal is a don't care during MRS command if DRAM RTT_Nom function is disabled in the mode register prior and after an MRS command.

Some of the mode register setting cases, function updating takes longer than tMOD. This type of MRS does not apply tMOD timing to next valid command excluding DES is listed in note 2 of Figure 6. These MRS command input cases have unique MR setting procedure, so refer to individual function description.

3.5 Mode Register

MR0

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	RFU	0 = must be programmed to 0 during MRS
A11:A9	WR and RTP[2, 3]	Write Recovery and Read to Precharge for auto precharge(see Table 1)
A8	DLL Reset	0 = NO 1 = Yes
A7	TM	0 = Normal 1 = Test
A6:A4,A2	CAS Latency[4]	(see Table 2)

Address	Operating Mode	Description
A3	Read Burst Type	0 = Sequential 1 = Interleave
A1:A0	Burst Length	00 = 8 (Fixed) 01 = BC4 or 8 (on the fly) 10 = BC4 (Fixed) 11 = Reserved

NOTE :

1. Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.
2. WR (write recovery for autoprecharge)min in clock cycles is calculated by dividing tWR(in ns) by tCK(in ns) and rounding up to the next integer:WRmin[cycles] = Roundup(tWR[ns] / tCK[ns]). The WR value in the mode register must be programmed to be equal or larger than WRmin. The programmed WR value is used with tRP to determine tDAL.
3. The table shows the encodings for Write Recovery and internal Read command to Precharge command delay. For actual Write recovery timing, please refer to AC timing table.
4. The table only shows the encodings for a given Cas Latency. For actual supported Cas Latency, please refer to speedbin tables for each frequency.

Table 1 — Write Recovery and Read to Precharge (cycles)

A11	A10	A9	WR	RTP	WR_CRC_DM
0	0	0	10	5	TBD
0	0	1	12	6	TBD
0	1	0	14	7	TBD
0	1	1	16	8	TBD
1	0	0	18	9	TBD
1	0	1	20	10	TBD
1	1	0	24	12	TBD
1	1	1	Reserved	Reserved	Reserved

Table 2 — CAS Latency

A6	A5	A4	A2	CAS Latency
0	0	0	0	9
0	0	0	1	10
0	0	1	0	11
0	0	1	1	12
0	1	0	0	13
0	1	0	1	14
0	1	1	0	15
0	1	1	1	16
1	0	0	0	18
1	0	0	1	20
1	0	1	0	22
1	0	1	1	24
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Reserved

MR1

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[3]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Qoff[1]	0 = Output buffer enabled 1 = Output buffer disabled
A11	TDQS enable	0 = Disable 1 = Enable
A10, A9, A8	RTT_NOM	(see Table 3)
A7	Write Leveling Enable	0 = Disable 1 = Enable
A6, A5	RFU	0 = must be programmed to 0 during MRS
A4, A3	Additive Latency	00 = 0(AL disabled) 10 = CL-2 01 = CL-1 11 = Resrved
A2, A1	Output Driver Impedance Control	(see Table 4)
A0	DLL Enable	0 = Disable[2] 1 = Enable

NOTE 1 Outputs disabled - DQs, DQS_ts, DQS_cs.
NOTE 2 States reversed to “0 as Disable” with respect to DDR4.
NOTE 3 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn’t respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 3 — RTT_NOM

A10	A9	A8	RTT_NOM
0	0	0	RTT_NOM Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 4 — Output Driver Impedance Control

A2	A1	Output Driver Impedance Control
0	0	RZQ/7
0	1	RZQ/5
1	0	Reserved
1	1	Reserved

MR2

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Write CRC	0 = Disable 1 = Enable
A11	RFU	0 = must be programmed to 0 during MRS
A10:A9	RTT_WR	(see Table 5)
A8	RFU	0 = must be programmed to 0 during MRS
A7:A6	Low Power Array Self Refresh (LP ASR)	00 = Manual Mode (Normal Operaing Temperature Range) 01 = Manual Mode (Reduced Operating Temperature Range) 10 = Manual Mode (Extended Operating Temperature Range) 11 = ASR Mode (Auto Self Refresh)
A5:A3	CAS Write Latency(CWL)	(see Table 6)
A2:A0	RFU	0 = must be programmed to 0 during MRS

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 5 — RTT_WR

A10	A9	RTT_WR
0	0	Dynamic ODT Off
0	1	RZQ/2
1	0	RZQ/1
1	1	Hi-Z

Table 6 — CWL (CAS Write Latency)

A5	A4	A3	CWL	Speed bin in MT/s
0	0	0	9	1600
0	0	1	10	1866
0	1	0	11	2133,1600
0	1	1	12	2400,1866
1	0	0	14	2133
1	0	1	16	2400
1	1	0	18	
1	1	1	Reserved	

MR3

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12:A11	MPR Read Format	00 = Serial 01 = Parallel	10 = Staggered 11 = ReservedTemperature
A10:A9	Write CMD Latency when CRC and DM are enabled	(see Table 8)	
A8:A6	Fine Granularity Refresh Mode	(see Table 7)	
A5	Temperature sensor readout	0 : disabled	1: enabled
A4	Per DRAM Addressability	0 = Disable	1 = Enable
A3	Geardown Mode	0 = 1/2 Rate	1 = 1/4 Rate
A2	MPR Operation	0 = Normal	1 = Dataflow from/to MPR
A1:A0	MPR page Selection	00 = Page0 01 = Page1 (see Table.8)	10 = Page2 11 = Page3

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 7 — Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

Table 8 — MR3 A<10:9> Write Command Latency when CRC and DM are both enabled

A10	A9	CRC+DM Write Command Latency	Speed Bin
0	0	4nCK	1600
0	1	5nCK	1866,2133,2400
1	0	6nCK	TBD
1	1	RFU	RFU

Table 9 — MPR Data Format

MPR page0 (Training Pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/ Write (default value)
	01 = MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

MPR page1 (CA Parity Error Log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE 1 MPR used for C/A parity error log readout is enabled by setting A[2] in MR3

NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.

NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

NOTE 4 MPR3 bit 0~2 (CA parity latency) reflects the latest programmed CA parity latency values.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	RFU	RFU	RFU	Temperature Sensor Status(Table1)		CRC Write Enable	Rtt_WR		read-only
		-	-	-	-	-	MR2	MR2		
		-	-	-	-	-	A12	A10	A9	
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable	
		MR6	MR6							
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency				RFU	CAS Write Latency			
		MR0				-	MR2			
		A6	A5	A4	A2	-	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A6	A8	A7	A6	A2	A1	

MR bit for Temperature
MR3 bit A5=1 : DRAM updates the temperature sensor status to MPR Page 2 (MPR0 bits A4:A3). Temperature data is guaranteed by the DRAM to be no more than 32ms old at the time of MPR Read of the Temperature Sensor Status bits.
MR3 bit A5=0: DRAM disables updates to the temperature sensor status in MPR Page 2(MPR0-bit A4:A3)

MPR0 bit A4	MPR0 bit A3	Refresh Rate Range
0	0	Sub 1X refresh (> tREFI)
0	1	1X refresh rate(= tREFI)
1	0	2X refresh rate(1/2* tREFI)
1	1	rsvd

MPR page3 (Vendor use only)[1]

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	Read-only
	01 = MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	

NOTE 1 MPR page3 is specifically assigned to DRAM. Actual encoding method is vendor specific.

MR4

Address	Operating Mode	Description	
BG1	RFU	0 = must be programmed to 0 during MRS	
BG0, BA1:BA0	MR Select	000 = MR0 001 = MR1 010 = MR2 011 = MR3	100 = MR4 101 = MR5 110 = MR6 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS	
A13	RFU	0 = must be programmed to 0 during MRS	
A12	Write Preamble	0 = 1 nCK	1 = 2 nCK
A11	Read Preamble	0 = 1 nCK	1 = 2 nCK
A10	Read Preamble Training Mode	0 = Disable	1 = Enable
A9	Self Refresh Abort	0 = Disable	1 = Enable
A8:A6	CS to CMD/ADDR Latency Mode (cycles)	000 = Disable 001 = 3 010 = 4 011 = 5 (See Table 10)	100 = 6 101 = 8 110 = Reserved 111 = Reserved
A5	RFU	0 = must be programmed to 0 during MRS	
A4	Internal Vref Monitor	0 = Disable	1 = Enable
A3	Temperature Controlled Refresh Mode	0 = Disable	1 = Enable
A2	Temperature Controlled Refresh Range	0 = Normal	1 = Extended
A1	Maximum Power Down Mode	0 = Disable	1 = Enable
A0	RFU	0 = must be programmed to 0 during MRS	

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

Table 10 — CS to CMD / ADDR Latency Mode Setting

A8	A7	A6	CAL
0	0	0	Disable
0	0	1	3
0	1	0	4
0	1	1	5
1	0	0	6
1	0	1	8
1	1	0	Reserved
1	1	1	Reserved

MR5

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12	Read DBI	0 = Disable 1 = Enable
A11	Write DBI	0 = Disable 1 = Enable
A10	Data Mask	0 = Disable 1 = Enable
A9	CA parity Persistent Error	0 = Disable1 = Enable
A8:A6	RTT_PARK	(see Table 11)
A5	ODT Input Buffer during Power Down mode	0 = ODT input buffer is activated 1 = ODT input buffer is deactivated
A4	C/A Parity Error Status	0 = Clear 1 = Error
A3	CRC Error Clear	0 = Clear 1 = Error
A2:A0	C/A Parity Latency Mode	(see Table 12)

NOTE 1 Reserved for Register control word setting .DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond. When RFU MR code setting is inputted, DRAM operation is not defined.

NOTE 2 When RTT_NOM Disable is set in MR1, A5 of MR5 will be ignored.

Table 11 — RTT_PARK

A8	A7	A6	RTT_PARK
0	0	0	RTT_PARK Disable
0	0	1	RZQ/4
0	1	0	RZQ/2
0	1	1	RZQ/6
1	0	0	RZQ/1
1	0	1	RZQ/5
1	1	0	RZQ/3
1	1	1	RZQ/7

Table 12 — C/A Parity Latency Mode

A2	A1	A0	PL	Speed Bin
0	0	0	Disable	
0	0	1	4	1600,1866,2133
0	1	0	5	2400
0	1	1	6	RFU
1	0	0	8	RFU
1	0	1	Reserved	
1	1	0	Reserved	
1	1	1	Reserved	

NOTE 1 Parity latency must be programmed according to timing parameters by speed grade table

MR6

Address	Operating Mode	Description
BG1	RFU	0 = must be programmed to 0 during MRS
BG0, BA1:BA0	MR Select	000 = MR0 100 = MR4 001 = MR1 101 = MR5 010 = MR2 110 = MR6 011 = MR3 111 = RCW[1]
A17	RFU	0 = must be programmed to 0 during MRS
A13	RFU	0 = must be programmed to 0 during MRS
A12:A10	tCCD_L	(see Table 13)
A9, A8	RFU	0 = must be programmed to 0 during MRS
A7	VrefDQ Training Enable	0 = Disable(Normal operation Mode) 1 = Enable(Training Mode)
A6	VrefDQ Training Range	(see Table 14)
A5:A0	VrefDQ Training Value	(see Table 15)

NOTE 1 Reserved for Register control word setting . DRAM ignores MR command with BG0,BA1;BA0=111 and doesn't respond.

Table 13 — tCCD_L

A12	A11	A10	tCCD_L.min (nCK)[1]	tDLLKmin (nCK)[1]	Note
0	0	0	4	597	≤ 1333Mbps
0	0	1	5		≤ 1866Mbps (1600/1866Mbps)
0	1	0	6	768	≤ 2400Mbps (2133/2400Mbps)
0	1	1	7	1024	≤ TBD
1	0	0	8		≤ TBD
1	0	1	Reserved		
1	1	0			
1	1	1			

NOTE 1 tCCD_L/tDLLK should be programmed according to the value defined in AC parameter table per operating frequency

Table 14 — VrefDQ Training : Range

A6	VrefDQ Range
0	Range 1
1	Range 2

Table 15 — VrefDQ Training: Values

A5:A0	Range1	Range2	A5:A0	Range1	Range2
00 0000	60.00%	45.00%	01 1010	76.90%	61.90%
00 0001	60.65%	45.65%	01 1011	77.55%	62.55%
00 0010	61.30%	46.30%	01 1100	78.20%	63.20%
00 0011	61.95%	46.95%	01 1101	78.85%	63.85%
00 0100	62.60%	47.60%	01 1110	79.50%	64.50%
00 0101	63.25%	48.25%	01 1111	80.15%	65.15%
00 0110	63.90%	48.90%	10 0000	80.80%	65.80%
00 0111	64.55%	49.55%	10 0001	81.45%	66.45%
00 1000	65.20%	50.20%	10 0010	82.10%	67.10%
00 1001	65.85%	50.85%	10 0011	82.75%	67.75%
00 1010	66.50%	51.50%	10 0100	83.40%	68.40%
00 1011	67.15%	52.15%	10 0101	84.05%	69.05%
00 1100	67.80%	52.80%	10 0110	84.70%	69.70%
00 1101	68.45%	53.45%	10 0111	85.35%	70.35%
00 1110	69.10%	54.10%	10 1000	86.00%	71.00%
00 1111	69.75%	54.75%	10 1001	86.65%	71.65%
01 0000	70.40%	55.40%	10 1010	87.30%	72.30%
01 0001	71.05%	56.05%	10 1011	87.95%	72.95%
01 0010	71.70%	56.70%	10 1100	88.60%	73.60%
01 0011	72.35%	57.35%	10 1101	89.25%	74.25%
01 0100	73.00%	58.00%	10 1110	89.90%	74.90%
01 0101	73.65%	58.65%	10 1111	90.55%	75.55%
01 0110	74.30%	59.30%	11 0000	91.20%	76.20%
01 0111	74.95%	59.95%	11 0001	91.85%	76.85%
01 1000	-75.60%	60.60%	11 0010	92.50%	77.50%
01 1001	76.25%	61.25%	11 0011 to 11 1111	Reserved	Reserved

DRAM MR7 Ignore

The DDR4 SDRAM shall ignore any access to MR7 for all DDR4 SDRAM.Any bit setting within MR7 may not take any effect in the DDR4 SDRAM.

4 DDR4 SDRAM Command Description and Operation

4.1 Command Truth Table

(a) Note 1,2,3 and 4 apply to the entire Command truth table
(b) Note 5 applies to all Read/Write commands.
[BG=Bank Group Address, BA=Bank Address, RA=Row Address, CA=Column Address, BC_n=Burst Chop, X=Don't Care, V=Valid].

Table 16 — Command Truth Table

Function	Abbreviation	CKE		CS_n	ACT_n	RAS_n /A16	CAS_n /A15	WE_n/ A14	BG0-BG1	BA0-BA1	C2-C0	A12/ BC_n	A17, A13, A11	A10/ AP	A0-A9	NOTE
		Previous Cycle	Current Cycle													
Mode Register Set	MRS	H	H	L	H	L	L	L	BG	BA	V	OP Code				12
Refresh	REF	H	H	L	H	L	L	H	V	V	V	V	V	V	V	
Self Refresh Entry	SRE	H	L	L	H	L	L	H	V	V	V	V	V	V	V	7,9
Self Refresh Exit	SRX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	7,8,9, 10
				L	H	H	H	H	V	V	V	V	V	V	V	
Single Bank Precharge	PRE	H	H	L	H	L	H	L	BG	BA	V	V	V	L	V	
Precharge all Banks	PREA	H	H	L	H	L	H	L	V	V	V	V	V	H	V	
RFU	RFU	H	H	L	H	L	H	H	RFU							
Bank Activate	ACT	H	H	L	L	Row Address(RA)			BG	BA	V	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	H	L	L	BG	BA	V	V	V	L	CA	
Write (BC4, on the Fly)	WRS4	H	H	L	H	H	L	L	BG	BA	V	L	V	L	CA	
Write (BL8, on the Fly)	WRS8	H	H	L	H	H	L	L	BG	BA	V	H	V	L	CA	
Write with Auto Precharge (Fixed BL8 or BC4)	WRA	H	H	L	H	H	L	L	BG	BA	V	V	V	H	CA	
Write with Auto Precharge (BC4, on the Fly)	WRAS4	H	H	L	H	H	L	L	BG	BA	V	L	V	H	CA	
Write with Auto Precharge (BL8, on the Fly)	WRAS8	H	H	L	H	H	L	L	BG	BA	V	H	V	H	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	H	L	H	BG	BA	V	V	V	L	CA	
Read (BC4, on the Fly)	RDS4	H	H	L	H	H	L	H	BG	BA	V	L	V	L	CA	
Read (BL8, on the Fly)	RDS8	H	H	L	H	H	L	H	BG	BA	V	H	V	L	CA	
Read with Auto Precharge (Fixed BL8 or BC4)	RDA	H	H	L	H	H	L	H	BG	BA	V	V	V	H	CA	
Read with Auto Precharge (BC4, on the Fly)	RDAS4	H	H	L	H	H	L	H	BG	BA	V	L	V	H	CA	
Read with Auto Precharge (BL8, on the Fly)	RDAS8	H	H	L	H	H	L	H	BG	BA	V	H	V	H	CA	
No Operation	NOP	H	H	L	H	H	H	H	V	V	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	X	X	X	
Power Down Entry	PDE	H	L	H	X	X	X	X	X	X	X	X	X	X	X	6
Power Down Exit	PDX	L	H	H	X	X	X	X	X	X	X	X	X	X	X	6
ZQ calibration Long	ZQCL	H	H	L	H	H	H	L	V	V	V	V	V	H	V	
ZQ calibration Short	ZQCS	H	H	L	H	H	H	L	V	V	V	V	V	L	V	

NOTE 1 All DDR4 SDRAM commands are defined by states of CS_n, ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14 and CKE at the rising edge of the clock. The MSB of BG, BA, RA and CA are device density and configuration dependant. When ACT_n = H; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as command pins RAS_n, CAS_n, and WE_n respectively. When ACT_n = L; pins RAS_n/A16, CAS_n/A15, and WE_n/A14 are used as address pins A16, A15, and A14 respectively
NOTE 2 RESET_n is Low enable command which will be used only for asynchronous reset so must be maintained HIGH during any function.
NOTE 3 Bank Group addresses (BG) and Bank addresses (BA) determine which bank within a bank group to be operated upon. For MRS commands the BG and BA selects the specific Mode Register location.
NOTE 4 "V" means "H or L (but a defined logic level)" and "X" means either "defined or undefined (like floating) logic level".
NOTE 5 Burst reads or writes cannot be terminated or interrupted and Fixed/on-the-Fly BL will be defined by MRS.
NOTE 6 The Power Down Mode does not perform any refresh operation.
NOTE 7 The state of ODT does not affect the states described in this table. The ODT function is not available during Self Refresh.
NOTE 8 Controller guarantees self refresh exit to be synchronous.
NOTE 9 VREF(VrefCA) must be maintained during Self Refresh operation. The first Write Leveling Activity may not occur earlier than TBD nCK after exit from Self Refresh.
NOTE 10 The No Operation command should be used in cases when the DDR4 SDRAM is in Gear Down Mode and Max Power Saving Mode Exit
NOTE 11 Refer to the CKE Truth Table for more detail with CKE transition.
NOTE 12 During a MRS command A17 is Reserved for Future Use and is device density and configuration dependent.

4.2 CKE Truth Table

Table 17 — CKE Truth Table

Current State[2]	CKE		Command (N)[3] RAS_n, CAS_n, WE_n, CS_n	Action (N)[3]	NOTE
	Previous Cycle[1] (N-1)	Current Cycle[1] (N)			
Power Down	L	L	X	Maintain Power-Down	14, 15
	L	H	DESELECT	Power Down Exit	11, 14
Self Refresh	L	L	X	Maintain Self Refresh	15, 16
	L	H	DESELECT	Self Refresh Exit	8, 12, 16
Bank(s) Active	H	L	DESELECT	Active Power Down Entry	11, 13, 14
Reading	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Writing	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Precharging	H	L	DESELECT	Power Down Entry	11, 13, 14, 17
Refreshing	H	L	DESELECT	Precharge Power Down Entry	11
All Banks Idle	H	L	DESELECT	Precharge Power Down Entry	11,13, 14, 18
	H	L	REFRESH	Self Refresh Entry	9, 13, 18
For more details with all signals See “Command Truth Table”.					10

NOTE 1 CKE (N) is the logic state of CKE at clock edge N; CKE (N-1) was the state of CKE at the previous clock edge.

NOTE 2 Current state is defined as the state of the DDR4 SDRAM immediately prior to clock edge N.

NOTE 3 COMMAND (N) is the command registered at clock edge N, and ACTION (N) is a result of COMMAND (N),ODT is not included here.

NOTE 4 All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.

NOTE 5 The state of ODT does not affect the states described in this table. The ODT function is not available during Self-Refresh.

NOTE 6 During any CKE transition (registration of CKE H->L or CKE L->H), the CKE level must be maintained until 1nCK prior to tCKEmin being satisfied (at which time CKE may transition again).

NOTE 7 DESELECT and NOP are defined in the Command Truth Table.

NOTE 8 On Self-Refresh Exit DESELECT commands must be issued on every clock edge occurring during the tXS period. Read or ODT commands may be issued only after tXSDLL is satisfied.

NOTE 9 Self-Refresh mode can only be entered from the All Banks Idle state.

NOTE 10 Must be a legal command as defined in the Command Truth Table.

NOTE 11 Valid commands for Power-Down Entry and Exit are DESELECT only.

NOTE 12 Valid commands for Self-Refresh Exit are DESELECT only except for Gear Down mode and Max Power Saving exit. NOP is allowed for these 2 modes.

NOTE 13 Self-Refresh can not be entered during Read or Write operations. For a detailed list of restrictions See “Self-Refresh Operation” on Section 4.27 and See “Power-Down Modes” on Section 4.28.

NOTE 14 The Power-Down does not perform any refresh operations.

NOTE 15 “X” means “don’t care“ (including floating around VREF) in Self-Refresh and Power-Down. It also applies to Address pins.

NOTE 16 VPP and VREFCA must be maintained during Self-Refresh operation. The first Write operation or first Write Leveling Activity may not occur earlier than TBD nCK after exit from Self Refresh.

NOTE 17 If all banks are closed at the conclusion of the read, write or precharge command, then Precharge Power-Down is entered, otherwise Active Power-Down is entered.

NOTE 18 ‘Idle state’ is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD, tRFC, tZQinit, tZQoper, tZQCS, etc.) as well as all Self-Refresh exit and Power-Down Exit parameters are satisfied (tXS, tXP,etc)

4.3 Burst Length, Type and Order

Accesses within a given burst may be programmed to sequential or interleaved order. The burst type is selected via bit A3 of Mode Register MR0. The ordering of accesses within a burst is determined by the burst length, burst type, and the starting column address as shown in Table 17. The burst length is defined by bits A0-A1 of Mode Register MR0. Burst length options include fixed BC4, fixed BL8, and 'on the fly' which allows BC4 or BL8 to be selected coincident with the registration of a Read or Write command via A12/BC_n.

Table 18 — Burst Type and Burst Order

Burst Length	Read/ Write	Starting Column Address (A2,A1,A0)	burst type = Sequential (decimal) A3=0	burst type = Interleaved (decimal) A3=1	NOTE
4 Chop	READ	0 0 0	0,1,2,3,T,T,T,T	0,1,2,3,T,T,T,T	1,2,3
		0 0 1	1,2,3,0,T,T,T,T	1,0,3,2,T,T,T,T	1,2,3
		0 1 0	2,3,0,1,T,T,T,T	2,3,0,1,T,T,T,T	1,2,3
		0 1 1	3,0,1,2,T,T,T,T	3,2,1,0,T,T,T,T	1,2,3
		1 0 0	4,5,6,7,T,T,T,T	4,5,6,7,T,T,T,T	1,2,3
		1 0 1	5,6,7,4,T,T,T,T	5,4,7,6,T,T,T,T	1,2,3
		1 1 0	6,7,4,5,T,T,T,T	6,7,4,5,T,T,T,T	1,2,3
		1 1 1	7,4,5,6,T,T,T,T	7,6,5,4,T,T,T,T	1,2,3
	WRITE	0, V, V	0,1,2,3,X,X,X,X	0,1,2,3,X,X,X,X	1,2,4,5
		1, V, V	4,5,6,7,X,X,X,X	4,5,6,7,X,X,X,X	1,2,4,5
8	READ	0 0 0	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2
		0 0 1	1,2,3,0,5,6,7,4	1,0,3,2,5,4,7,6	2
		0 1 0	2,3,0,1,6,7,4,5	2,3,0,1,6,7,4,5	2
		0 1 1	3,0,1,2,7,4,5,6	3,2,1,0,7,6,5,4	2
		1 0 0	4,5,6,7,0,1,2,3	4,5,6,7,0,1,2,3	2
		1 0 1	5,6,7,4,1,2,3,0	5,4,7,6,1,0,3,2	2
		1 1 0	6,7,4,5,2,3,0,1	6,7,4,5,2,3,0,1	2
		1 1 1	7,4,5,6,3,0,1,2	7,6,5,4,3,2,1,0	2
	WRITE	V, V, V	0,1,2,3,4,5,6,7	0,1,2,3,4,5,6,7	2,4

NOTE 1 In case of burst length being fixed to 4 by MR0 setting, the internal write operation starts two clock cycles earlier than for the BL8 mode. This means that the starting point for tWR and tWTR will be pulled in by two clocks. In case of burst length being selected on-the-fly via A12/BC_n, the internal write operation starts at the same point in time like a burst of 8 write operation. This means that during on-the-fly control, the starting point for tWR and tWTR will not be pulled in by two clocks.

NOTE 2 0...7 bit number is value of CA[2:0] that causes this bit to be the first read during a burst.

NOTE 3 Output driver for data and strobes are in high impedance.

NOTE 4 V : A valid logic level (0 or 1), but respective buffer input ignores level on input pins.

NOTE 5 X : Don't Care.

4.3.1 BL8 Burst order with CRC Enabled

DDR4 SDRAM supports fixed write burst ordering [A2:A1:A0=0:0:0] when write CRC is enabled in BL8 (fixed).

4.4 DLL-off Mode & DLL on/off Switching procedure

4.4.1 DLL on/off switching procedure

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to “0”; this will disable the DLL for subsequent operations until A0 bit is set back to “1”.

4.4.2 DLL “on” to DLL “off” Procedure

To switch from DLL “on” to DLL “off” requires the frequency to be changed during Self-Refresh, as outlined in the following procedure:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled, and DRAMs On-die Termination resistors, RTT_NOM, must be in high impedance state before MRS to MR1 to disable the DLL.)

2. Set MR1 bit A0 to “0” to disable the DLL.

3. Wait tMOD.

4. Enter Self Refresh Mode; wait until (tCKSRE) is satisfied.

5. Change frequency, in guidance with “Input clock frequency change” on Section 4.6.

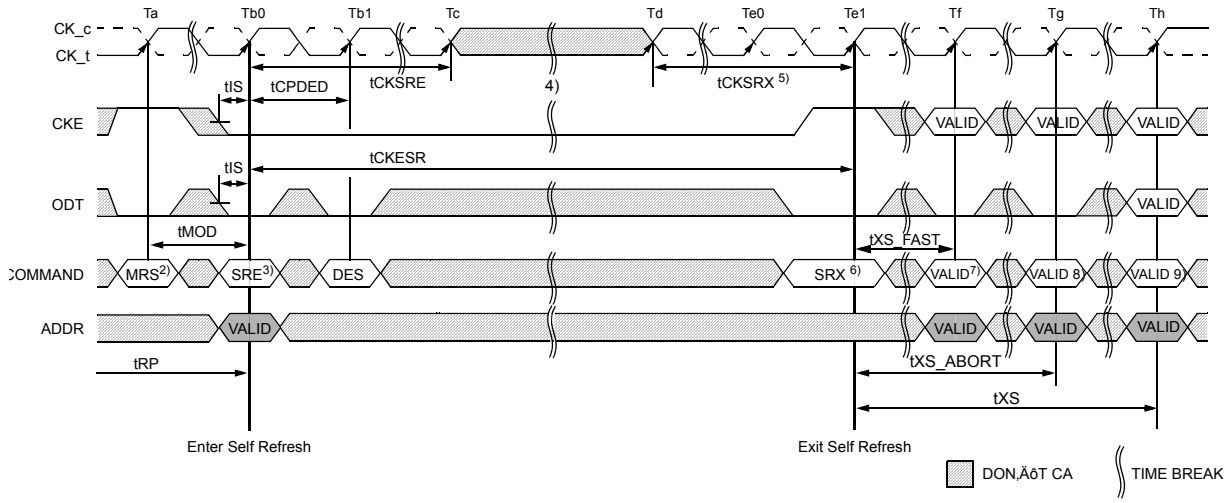
6. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

7. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until all tMOD timings from any MRS command are satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until all tMOD timings from any MRS command are satisfied. If RTT_NOM features were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t Care.

8. Wait tXS_Fast or tXS_Abort or tXS, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. A ZQCL command may also be issued after tXS_Fast).

- tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, RD, RDS4, RDS8, RDA, RDAS4, RDAS8
- tXS_Fast - ZQCL, ZQCS, MRS commands. For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressibility mode. Access to other DRAM mode registers must satisfy tXS timing.
- tXS_Abort - If the MR4 bit A9 is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command after a delay of tXS_abort. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.

9. Wait for tMOD, then DRAM is ready for next command.



1. Starting with Idle State, RTT in Stable
2. Disable DLL by setting MR1 Bit A0 to 0
3. Enter SR
4. Change Frequency
5. Clock must be stable tCKSRX
6. Exit SR
7.8.9. Update Mode registers allowed with DLL off parameters setting

Figure 7 — DLL Switch Sequence from DLL ON to DLL OFF

4.4.3 DLL “off” to DLL “on” Procedure

To switch from DLL “off” to DLL “on” (with required frequency change) during Self-Refresh:

1. Starting from Idle state (All banks pre-charged, all timings fulfilled and DRAMs On-die Termination resistors (RTT_NOM) must be in high impedance state before Self-Refresh mode is entered.)

2. Enter Self Refresh Mode, wait until tCKSRE satisfied.

3. Change frequency, in guidance with "Input clock frequency change" on Section 4.6.

4. Wait until a stable clock is available for at least (tCKSRX) at DRAM inputs.

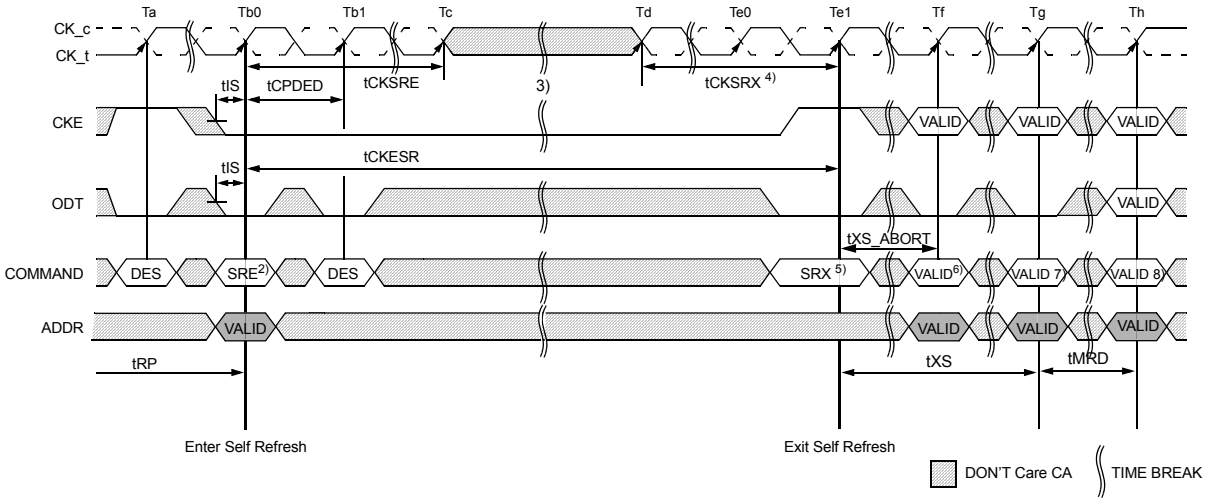
5. Starting with the Self Refresh Exit command, CKE must continuously be registered HIGH until tDLLK timing from subsequent DLL Reset command is satisfied. In addition, if any ODT features were enabled in the mode registers when Self Refresh mode was entered, the ODT signal must continuously be registered LOW until tDLLK timings from subsequent DLL Reset command is satisfied. If RTT_NOM were disabled in the mode registers when Self Refresh mode was entered, ODT signal is Don’t care.

6. Wait tXS or tXS_ABORT depending on Bit A9 in MR4, then set MR1 bit A0 to “1” to enable the DLL.

7. Wait tMRD, then set MR0 bit A8 to “1” to start DLL Reset.

8. Wait tMRD, then set Mode Registers with appropriate values (especially an update of CL, CWL and WR may be necessary. After tMOD satisfied from any proceeding MRS command, a ZQCL command may also be issued during or after tDLLK.)

9. Wait for tMOD, then DRAM is ready for next command (Remember to wait tDLLK after DLL Reset before applying command requiring a locked DLL!). In addition, wait also for tZQoper in case a ZQCL command was issued.



1. Starting with Idle State
2. Enter SR
3. Change Frequency
4. Clock must be stable tCKSRX
5. Exit SR
6.7. Set DLL-on by MR1 A0='1'
8. Start DLLReset
9. Update rest MR register values after tDLLK (not shown in the diagram)
10. Ready for valid command after tDLLK (not shown in the diagram)

Figure 8 — DLL Switch Sequence from DLL OFF to DLL ON

4.5 DLL-off Mode

DDR4 SDRAM DLL-off mode is entered by setting MR1 bit A0 to "0"; this will disable the DLL for subsequent operations until A0 bit is set back to "1". The MR1 A0 bit for DLL control can be switched either during initialization or later. Refer to "Input clock frequency change" on Section 4.6.

The DLL-off Mode operations listed below are an optional feature for DDR4 SDRAM. The maximum clock frequency for DLL-off Mode is specified by the parameter tCKDLL_OFF. There is no minimum frequency limit besides the need to satisfy the refresh interval, tREFI.

Due to latency counter and timing restrictions, only one value of CAS Latency (CL) in MR0 and CAS Write Latency (CWL) in MR2 are supported. The DLL-off mode is only required to support setting of both CL=10 and CWL=9. When DLL-off Mode is enabled, use of CA Parity Mode is not allowed.

DLL-off mode will affect the Read data Clock to Data Strobe relationship (tDQSCK), but not the Data Strobe to Data relationship (tDQSQ, tQH). Special attention is needed to line up Read data to controller time domain.

Comparing with DLL-on mode, where tDQSCK starts from the rising clock edge (AL+CL) cycles after the Read command, the DLL-off mode tDQSCK starts (AL+CL - 1) cycles after the read command.
Another difference is that tDQSCK may not be small compared to tCK (it might even be larger than tCK) and the difference between tDQSCKmin and tDQSCKmax is significantly larger than in DLL-on mode.
tDQSCK(DLL_off) values are vendor specific.
The timing relations on DLL-off mode READ operation are shown in the following Timing Diagram
(CL=10, BL=8, PL=0):

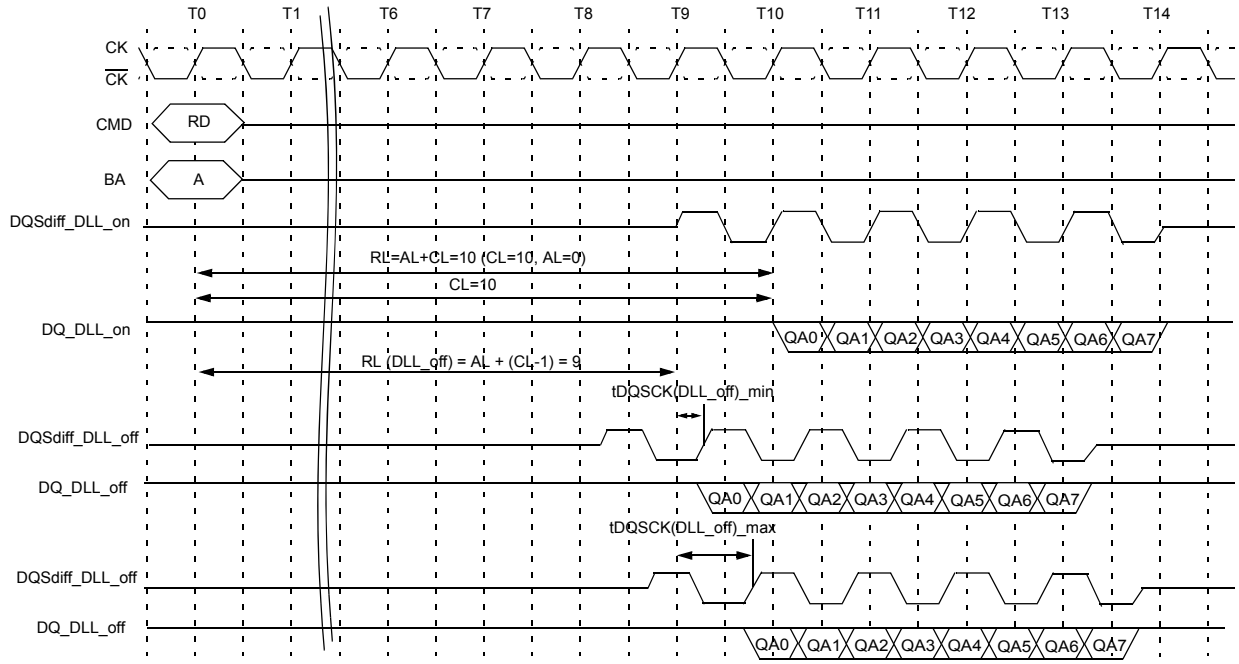


Figure 9 — READ operation at DLL-off mode

4.6 Input Clock Frequency Change

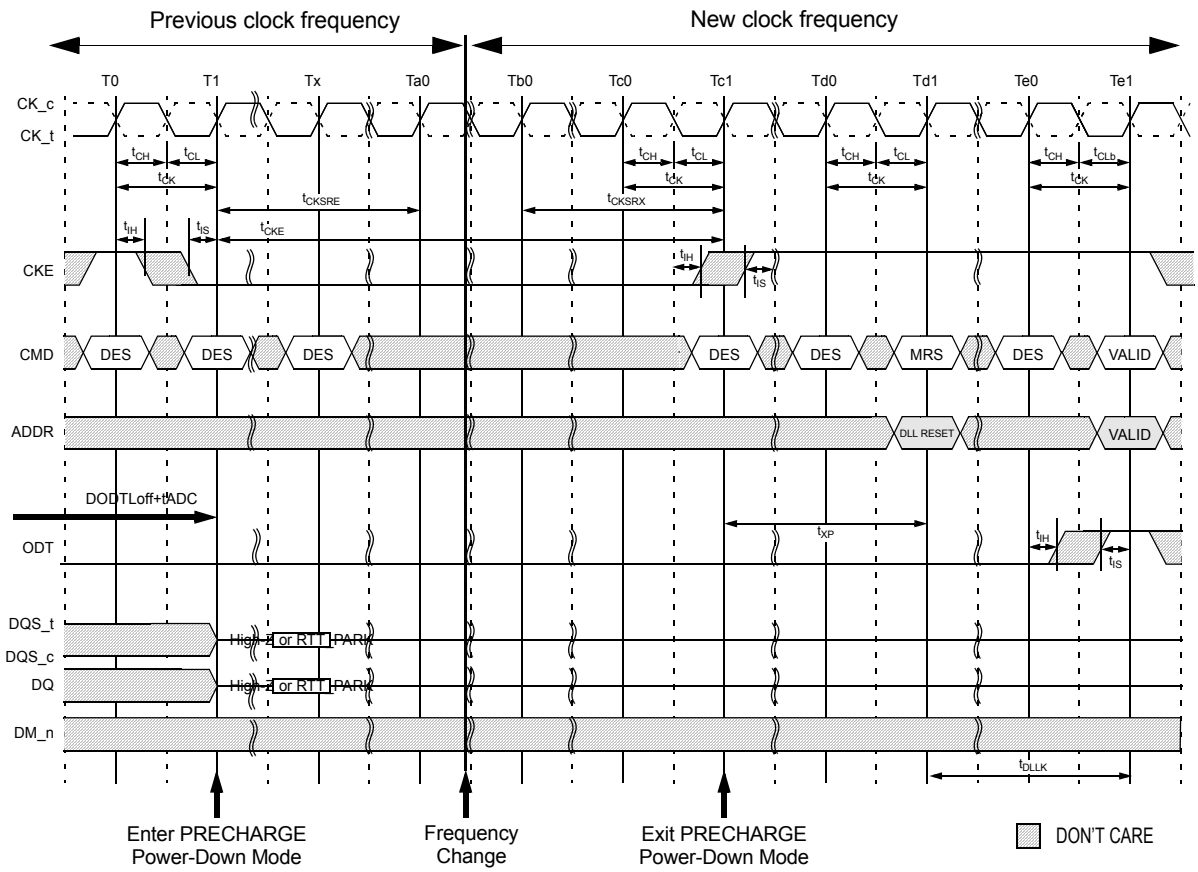
Once the DDR4 SDRAM is initialized, the DDR4 SDRAM requires the clock to be “stable” during almost all states of normal operation. This means that, once the clock frequency has been set and is to be in the “stable state”, the clock period is not allowed to deviate except for what is allowed for by the clock jitter and SSC (spread spectrum clocking) specifications.

The input clock frequency can be changed from one stable clock rate to another stable clock rate under twoconditions: (1) Self-Refresh mode and (2) Precharge Power-down mode. Outside of these two modes, it is illegal to change the clock frequency.
For the first condition, once the DDR4 SDRAM has been successfully placed in to Self-Refresh mode and tCKSRE has been satisfied, the state of the clock becomes a don’t care. Once a don’t care, changing the clock frequency is permissible, provided the new clock frequency is stable prior to tCKSRX. When entering and exiting Self-Refresh mode for the sole purpose of changing the clock frequency, the Self-Refresh entry and exit specifications must still be met as outlined in Section 4.27 “Self-Refresh Operation”. However, because DDR4 DLL lock time ranges from 597nCK at 1333MT/s to 1024nCK at 3200MT/s, additional MRS commands need to be issued for the new clock frequency. If DLL is enabled, tDLLK must be programmed according to the value defined in AC parameter tables, and the DLL must be RESET by an explicit MRS command (MR0 bit A8=’1’b) when the input clock frequency is different before and after self refresh.The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. Any frequency change below the minimum operating frequency would require the use of DLL_on- mode -> DLL_off -mode transition sequence, refer to Section 4.4, DLL on/off switching procedure

The second condition is when the DDR4 SDRAM is in Precharge Power-down mode. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW during this sequence until DLL re-lock to complete.

If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode, ODT signal is allowed to be floating and DRAM does not provide RTT_NOM termination. A minimum of tCKSRE must occur after CKE goes LOW before the clock frequency may change.

The DDR4 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed grade. During the input clock frequency change, CKE must be held at stable LOW levels. Once the input clock frequency is changed, stable new clocks must be provided to the DRAM tCKSRX before Precharge Power-down may be exited; after Precharge Power-down is exited and tXP has expired, tDLLK MRS command followed by DLL reset must be issued. Depending on the new clock frequency, additional MRS commands may need to be issued to appropriately set the WR/RTP, CL, and CWL with CKE continuously registered high. During DLL re-lock period, CKE must remain HIGH. After the DLL lock time, the DRAM is ready to operate with new clock frequency., see Figure 10.



NOTE :

1. tCKSRE and tCKSRX are Self-Refresh mode specifications but the value they represent are applicable here.
2. If the RTT_NOM feature was enabled in the mode register prior to entering Precharge power down mode, the ODT signal must continuously be registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering Precharge power down mode or DRAM ODT input deactivation is enabled, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.
3. If RTT_PARK is disabled and ODT input buffer is not deactivated.

Figure 10 — Change Frequency during Precharge Power-down

4.7 Write Leveling

For better signal integrity, the DDR4 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and their length, but it also causes flight time skew between clock and strobe at every DRAM on the DIMM. This makes it difficult for the Controller to maintain tDQSS, tDSS, and tDSH specification. Therefore, the DDR4 SDRAM supports a 'write leveling' feature to allow the controller to compensate for skew. This feature may not be required under some system conditions provided the host can maintain the tDQSS, tDSS and tDSH specifications.

The memory controller can use the 'write leveling' feature and feedback from the DDR4 SDRAM to adjust the DQS_t - DQS_c to CK_t - CK_c relationship. The memory controller involved in the leveling must have adjustable delay setting on DQS_t - DQS_c to align the rising edge of DQS_t - DQS_c with that of the clock at the DRAM pin. The DRAM asynchronously feeds back CK_t - CK_c, sampled with the rising edge of DQS_t - DQS_c, through the DQ bus. The controller repeatedly delays DQS_t - DQS_c until a transition from 0 to 1 is detected. The DQS_t - DQS_c delay established through this exercise would ensure tDQSS specification. Besides tDQSS, tDSS and tDSH specification also needs to be fulfilled. One way to achieve this is to combine the actual tDQSS in the application with an appropriate duty cycle and jitter on the DQS_t - DQS_c signals. Depending on the actual tDQSS in the application, the actual values for tDQSL and tDQSH may have to be better than the absolute limits provided in the chapter "AC Timing Parameters" in order to satisfy tDSS and tDSH specification. A conceptual timing of this scheme is shown in Figure 11.

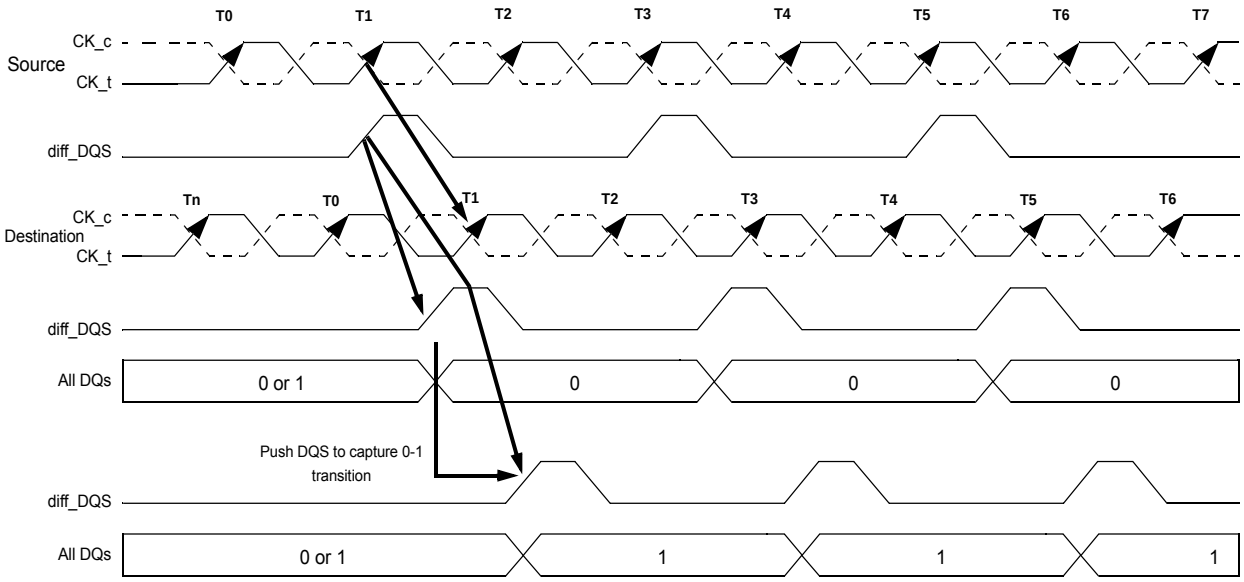


Figure 11 — Write Leveling Concept

DQS_t - DQS_c driven by the controller during leveling mode must be terminated by the DRAM based on ranks populated. Similarly, the DQ bus driven by the DRAM must also be terminated at the controller.

All data bits should carry the leveling feedback to the controller across the DRAM configurations X4, X8, and X16. On a X16 device, both byte lanes should be leveled independently. Therefore, a separate feedback mechanism should be available for each byte lane. The upper data bits should provide the feedback of the upper diff_DQS(diff_UDQS) to clock relationship whereas the lower data bits would indicate the lower diff_DQS(diff_LDQS) to clock relationship.

4.7.1 RAM setting for write leveling & DRAM termination function in that mode

DRAM enters into Write leveling mode if A7 in MR1 set 'High' and after finishing leveling, DRAM exits from write leveling mode if A7 in MR1 set 'Low' (Table 19). Note that in write leveling mode, only DQS_t/DQS_c terminations are activated and deactivated via ODT pin, unlike normal operation (Table 20).

Table 19 — MR setting involved in the leveling procedure

Function	MR1	Enable	Disable
Write leveling enable	A7	1	0
Output buffer mode (Qoff)	A12	0	1

Table 20 — DRAM termination function in the leveling mode

ODT pin @DRAM if RTT_NOM/PARK Value is set via MRS	DQS_t/DQS_c termination	DQs termination
RTT_NOM with ODT High	On	Off
RTT_PARK with ODT LOW	On	Off

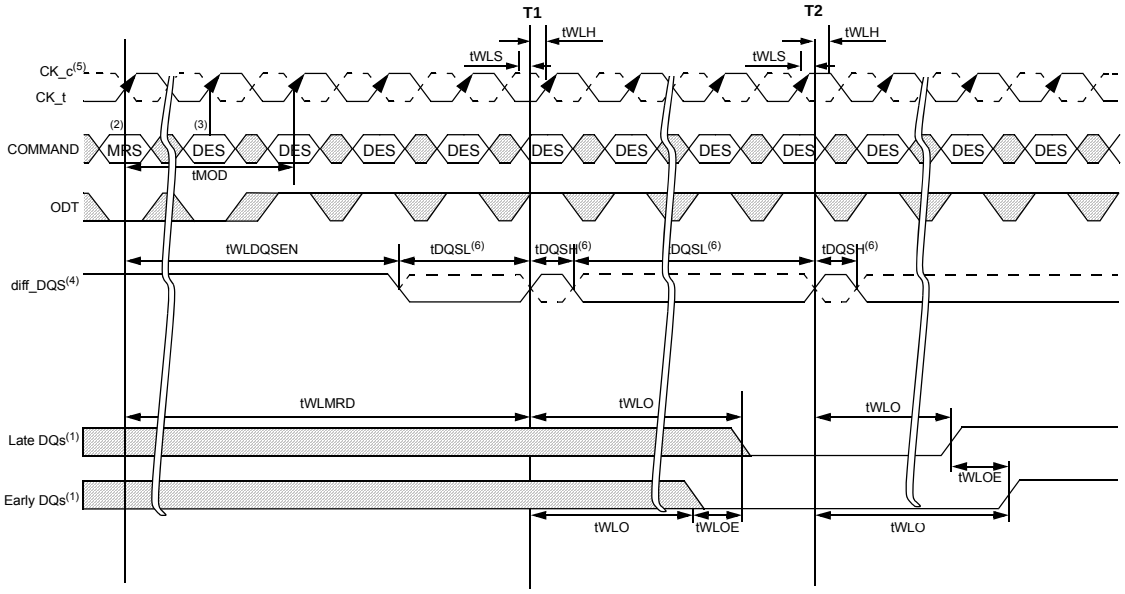
NOTE 1 In Write Leveling Mode with its output buffer disabled (MR1[bit A7] = 1 with MR1[bit A12] = 1) all RTT_NOM and RTT_PARK settings are allowed; in Write Leveling Mode with its output buffer enabled (MR1[bit A7] = 1 with MR1[bit A12] = 0) only RTT_NOM and RTT_PARK settings of TBD are allowed

4.7.2 Procedure Description

The Memory controller initiates Leveling mode of all DRAMs by setting bit A7 of MR1 to 1. When entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only DESELECT commands are allowed, as well as an MRS command to change Qoff bit (MR1[A12]) and an MRS command to exit write leveling (MR1[A7]). Upon exiting write leveling mode, the MRS command performing the exit (MR1[A7]=0) may also change MR1 bits of A12-A8 ,A2-A1. Since the controller levels one rank at a time, the output of other ranks must be disabled by setting MR1 bit A12 to 1. The Controller may assert ODT after tMOD, at which time the DRAM is ready to accept the ODT signal.

The Controller may drive DQS_t low and DQS_c high after a delay of tWLDQSEN, at which time the DRAM has applied on-die termination on these signals. After tDQSL and tWLMRD, the controller provides a single DQS_t, DQS_c edge which is used by the DRAM to sample CK_t - CK_c driven from controller. tWLMRD(max) timing is controller dependent.

DRAM samples CK_t - CK_c status with rising edge of DQS_t - DQS_c and provides feedback on all the DQ bits asynchronously after tWLO timing. There is a DQ output uncertainty of tWLOE defined to allow mismatch on DQ bits. The tWLOE period is defined from the transition of the earliest DQ bit to the corresponding transition of the latest DQ bit. There are no read strobes (DQS_t/ DQS_c) needed for these DQs. Controller samples incoming DQs and decides to increment or decrement DQS_t - DQS_c delay setting and launches the next DQS_t/DQS_c pulse after some time, which is controller dependent. Once a 0 to 1 transition is detected, the controller locks DQS_t - DQS_c delay setting and write leveling is achieved for the device. Figure 12 describes the timing diagram and parameters for the overall Write Leveling procedure.



NOTE 1 DDR4 SDRAM drives leveling feedback on all DQs
NOTE 2 MRS : Load MR1 to enter write leveling mode
NOTE 3 DES : Deselect
NOTE 4 diff_DQS is the differential data strobe (DQS_t-DQS_c). Timing reference points are the zero crossings. DQS is shown with solid line, DQS_c is shown with dotted line
NOTE 5 CK_t/CK_c : CK is shown with solid dark line, where as CK_c is drawn with dotted line.
NOTE 6 DQS_t, DQS_c needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent

Figure 12 — Timing details of Write leveling sequence [DQS_t - DQS_c is capturing CK_t - CK_c low at T1 and CK_t - CK_c high at T2

4.7.3 Write Leveling Mode Exit

The following sequence describes how the Write Leveling Mode should be exited:

1. After the last rising strobe edge (see ~T0), stop driving the strobe signals (see ~Tc0). Note: From now on, DQ pins are in undefined driving mode, and will remain undefined, until tMOD after the respective MRS command (Te1).
2. Drive ODT pin low (tIS must be satisfied) and continue registering low. (see Tb0).
3. After the RTT is switched off, disable Write Level Mode via MRS command (see Tc2).
4. After tMOD is satisfied (Te1), any valid command may be registered. (MRS commands may be issued after tMRD (Td1).

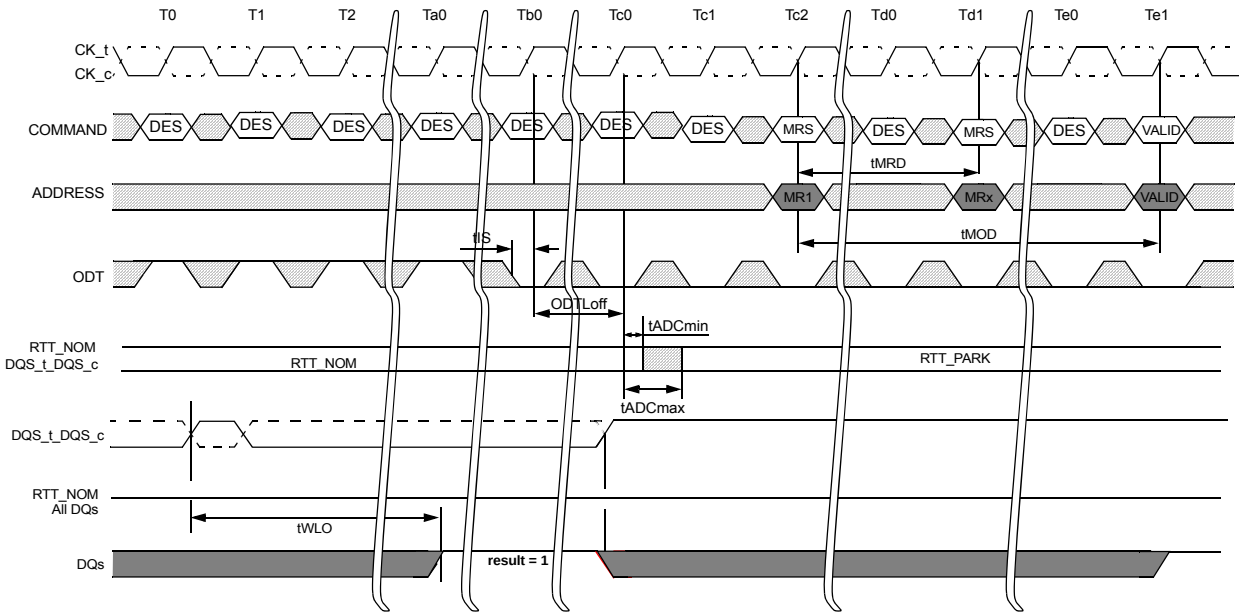


Figure 13 — Timing details of Write leveling exit

4.8 Temperature controlled Refresh modes

This mode is enabled and disabled by setting bit A3 in MR4. Two modes are supported that are selected by bit A2 setting in MR4.

4.8.1 Normal temperature mode

Once this mode is enabled by setting bit A3=1 and A2=0 in MR4, Refresh commands should be issued to DDR4 SDRAM with the refresh period equal to or shorter than tREFI of normal temperature range (0°C - 85°C). In this mode, the system guarantees that the DRAM temperature does not exceed 85°C.

Below 45°C, DDR4 SDRAM may adjust internal refresh period to be longer than tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. The internal refresh period adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

4.8.2 Extended temperature mode

Once this mode is enabled by setting bit A3=1 and A2=1 in MR4, Refresh commands should be issued to DDR4 SDRAM with the refresh period equal to or shorter than tREFI of extended temperature range (85°C - 95°C).

In the normal temperature range (0°C - 85°C), DDR4 SDRAM adjusts its internal refresh period to tREFI of the normal temperature range by skipping external refresh commands with proper gear ratio. Below 45°C, DDR4 SDRAM may further adjust internal refresh period to be longer than tREFI of the normal temperature range. The internal refresh period adjustment is automatically done inside the DRAM and user does not need to provide any additional control.

4.9 Fine Granularity Refresh Mode

4.9.1 Mode Register and Command Truth Table

The Refresh cycle time (tRFC) and the average Refresh interval (tREFI) of DDR4 SDRAM can be programmed by MRS command. The appropriate setting in the mode register will set a single set of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device (fixed mode), or allow the dynamic selection of one of two sets of Refresh cycle time and average Refresh interval for the DDR4 SDRAM device(on-the-fly mode). The on-the-fly mode must be enabled by MRS as shown in Table 21 before any on-the-fly- Refresh command can be issued.

Table 21 — MR3 definition for Fine Granularity Refresh Mode

A8	A7	A6	Fine Granularity Refresh
0	0	0	Normal mode (Fixed 1x)
0	0	1	Fixed 2x
0	1	0	Fixed 4x
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Enable on the fly 2x
1	1	0	Enable on the fly 4x
1	1	1	Reserved

There are two types of on-the-fly modes (1x/2x and 1x/4x modes) that are selectable by programming the appropriate values into the mode register. When either of the two on-the-fly modes is selected (‘A8=1’), DDR4 SDRAM evaluates BG0 bit when a Refresh command is issued, and depending on the status of BG0, it dynamically switches its internal Refresh configuration between 1x and 2x (or 1x and 4x) modes, and executes the corresponding Refresh operation. The command truth table is as shown in Table 22.

Table 22 — Refresh command truth table

Function	CS_n	ACT_n	RAS_n /A15	CAS_n /A14	WE_n /A13	BG1	BG0	BA0-1	A10/ AP	A0-9, A11-12, A16-20	MR3 Setting
Refresh (Fixed rate)	L	H	L	L	H	V	V	V	V	V	A8 = ‘0’
Refresh (on-the-fly 1x)	L	H	L	L	H	V	L	V	V	V	A8 = ‘1’
Refresh (on-the-fly 2x)	L	H	L	L	H	V	H	V	V	V	A8:A7:A6=‘1 01’
Refresh (on-the-fly 4x)											A8:A7:A6=‘1 10’

4.9.2 tREFI and tRFC parameters

The default Refresh rate mode is fixed 1x mode where Refresh commands should be issued with the normal rate, i.e., tREFI1 = tREFI(base) (for Tcase<=85°C), and the duration of each refresh command is the normal refresh cycle time (tRFC1). In 2x mode (either fixed 2x or on-the-fly 2x mode), Refresh commands should be issued to the DRAM at the double frequency (tREFI2 = tREFI(base)/2) of the normal Refresh rate. In 4x mode, Refresh command rate should be quadrupled (tREFI4 = tREFI(base)/4). Per each mode and command type, tRFC parameter has different values as defined in Table 23 .

The refresh command that should be issued at the normal refresh rate and has the normal refresh cycle duration may be referred to as a REF1x command. The refresh command that should be issued at the double frequency (tREFI2 = tREFI(base)/2) may be referred to as a REF2x command. Finally, the refresh command that should be issued at the quadruple rate (tREFI4 = tREFI(base)/4) may be referred to as a REF4x command.

In the Fixed 1x Refresh rate mode, only REF1x commands are permitted. In the Fixed 2x Refresh rate mode, only REF2x commands are permitted. In the Fixed 4x Refresh rate mode, only REF4x commands are permitted. When the on-the-fly 1x/2x Refresh rate mode is enabled, both REF1x and REF2x commands are permitted. When the on-the-fly 1x/4x Refresh rate mode is enabled, both REF1x and REF4x commands are permitted.

Table 23 — tREFI and tRFC parameters

Refresh Mode	Parameter		2Gb	4Gb	8Gb	16Gb	Unit
	tREFI(base)		7.8	7.8	7.8	TBD	us
1X mode	tREFI1	0°C <= TCASE <= 85°C	tREFI(base)	tREFI(base)	tREFI(base)	tREFI(base)	us
		85°C < TCASE <= 95°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
	tRFC1(min)		160	260	350	TBD	ns
2X mode	tREFI2	0°C <= TCASE <= 85°C	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	tREFI(base)/2	us
		85°C < TCASE <= 95°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
	tRFC2(min)		110	160	260	TBD	ns
4X mode	tREFI4	0°C <= TCASE <= 85°C	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	tREFI(base)/4	us
		85°C < TCASE <= 95°C	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	tREFI(base)/8	us
	tRFC4(min)		90	110	160	TBD	ns

4.9.3 Changing Refresh Rate

If Refresh rate is changed by either MRS or on the fly, new tREFI and tRFC parameters would be applied from the moment of the rate change. As shown in Figure 14, when REF1x command is issued to the DRAM, then tREF1 and tRFC1 are applied from the time that the command was issued. And then, when REF2x command is issued, then tREF2 and tRFC2 should be satisfied.

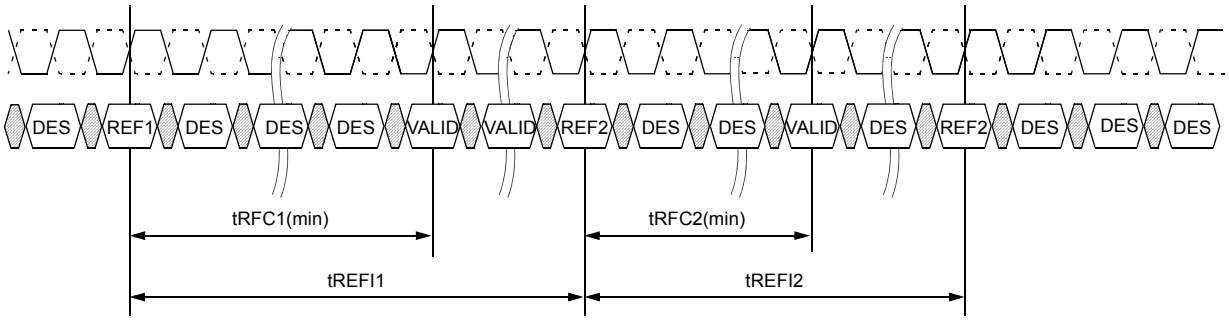


Figure 14 — On-the-fly Refresh Command Timing

The following conditions must be satisfied before the Refresh rate can be changed. Otherwise, data retention of DDR4 SDRAM cannot be guaranteed.

1. In the fixed 2x Refresh rate mode or the on-the-fly 1x/2x Refresh mode, an even number of REF2x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate mode with an MRS command before the Refresh rate can be changed by another MRS command.
2. In the on-the-fly 1x/2x Refresh rate mode, an even number of REF2x commands must be issued between any two REF1x commands.
3. In the fixed 4x Refresh rate mode or the on-the-fly 1x/4x Refresh mode, a multiple of-four number of REF4x commands must be issued to the DDR4 SDRAM since the last change of the Refresh rate with an MRS command before the Refresh rate can be changed by another MRS command.
4. In the on-the-fly 1x/4x Refresh rate mode, a multiple-of-four number of REF4x commands must be issued between any two REF1x commands.

There are no special restrictions for the fixed 1x Refresh rate mode. Switching between fixed and on-the-fly modes keeping the same rate is not regarded as a Refresh rate change.

4.9.4 Usage with Temperature Controlled Refresh mode

If the Temperature Controlled Refresh mode is enabled, then only the normal mode (Fixed 1x mode; A8:A7:A6='000') is allowed. If any other Refresh mode than the normal mode is selected, then the temperature controlled Refresh mode must be disabled.

4.9.5 Self Refresh entry and exit

DDR4 SDRAM can enter Self Refresh mode anytime in 1x, 2x and 4x mode without any restriction on the number of Refresh commands that has been issued during the mode before the Self Refresh entry. However, upon Self Refresh exit, extra Refresh command(s) may be required depending on the condition of the Self Refresh entry. The conditions and requirements for the extra Refresh command(s) are defined as follows

1. There are no special restrictions on the fixed 1x Refresh rate mode.
2. In the fixed 2x Refresh rate mode or the enable-on-the-fly 1x/2x Refresh rate mode, it is recommended that there should be an even number of REF2x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or two extra REF2x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).
3. In the fixed 4x Refresh rate mode or the enable-on-the-fly 1x/4x Refresh rate mode, it is recommended that there should be a multiple-of-four number of REF4x commands before entry into Self Refresh since the last Self Refresh exit or REF1x command or MRS command that set the refresh mode. If this condition is met, no additional refresh commands are required upon Self Refresh exit. In the case that this condition is not met, either one extra REF1x command or four extra REF4x commands are required to be issued to the DDR4 SDRAM upon Self Refresh exit. These extra Refresh commands are not counted toward the computation of the average refresh interval (tREFI).

4.10 Multi Purpose Register

4.10.1 DQ Training with MPR

The DDR4 DRAM contains four 8bit programmable MPR registers used for DQ bit pattern storage. These registers once programmed are activated with MRS read commands to drive the MPR bits on to the DQ bus during link training.

And DDR4 SDRAM only supports following command, MRS, RD, RDA WR, WRA, DES, REF and Reset during MPR enable Mode: MR3 [A2 = 1].

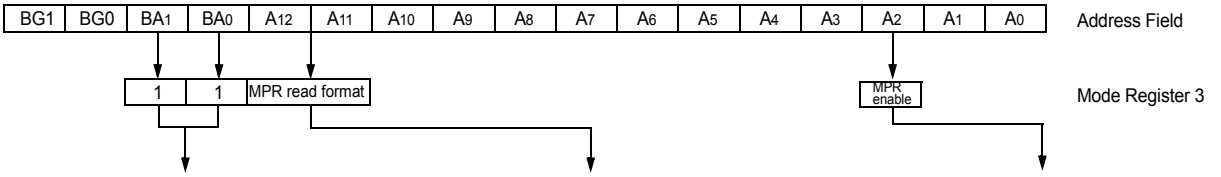
Note that in MPR mode RDA/WRA has the same functionality as a READ/WRITE command which means the auto precharge part of RDA/WRA is ignored. Power-Down mode and Self-Refresh command also is not allowed during MPR enable Mode. No other command can be issued within tRFC after REF command and 1x Refresh is only allowed when MPR mode is Enable. During MPR operations, MPR read or write sequence must be complete prior to a refresh command.

4.10.2 MR3 definition

Mode register MR3 controls the Multi-Purpose Registers (MPR) used for training. MR3 is written by asserting CS_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 low, ACT_n, BA0 and BA1 high and BG1[1] and BG0 low while controlling the states of the address pins according to the table below.

NOTE 1. x4/x8 only

MR3 Programming:



BA1	BA0	MR select
0	0	MR0
0	1	MR1
1	0	MR2
1	1	MR3

A12	A11	MPR read format
0	0	Serial
0	1	Parallel
1	0	Staggered
1	1	RFU

A2	MPR Operation
0	Normal operation
1	Dataflow from/to MPR

Read or Write with MPR LOCATION :

BA1	BA0	MPR Location
0	0	MPR location 0
0	1	MPR location 1
1	0	MPR location 2
1	1	MPR location 3

Default value for MPR0 = 01010101
Default value for MPR1 = 00110011
Default value for MPR2 = 00001111
Default value for MPR3 = 00000000

4.10.3 MPR Reads

MPR reads are supported using BL8 and BC4(Fixed) modes. BC4 on the fly is not supported for MPR reads.

MPR reads using BC4:

BA1 and BA0 indicate the MPR location within the selected page in MPR Mode.

A10 and other address pins are don't care including BG1 and BG0.
Read commands for BC4 are supported with starting column address of A2:A0 of '000' and '100'.

Data Bus Inversion (DBI) is not allowed during MPR Read operation.

DDR4 MPR mode is enabled by programming bit A2=1 and then reads are done from a specific MPR location.
MPR location is specified with the Read command using Bank address bits BA1 and BA0.

Each MPR location is 8 bit wide.

STEPS:
DLL must be locked prior to MPR Reads. If DLL is Enabled : MR1[A0 = 1]
Precharge all
Wait until tRP is satisfied
MRS MR3, Opcode A2='1'b
- Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

Read command
- A[1:0] = '00'b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= '0'b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)

or

- A[2]= 1 (For BL=8 : Not Support)
  (For BC=4, burst order is fixed at 4,5,6,7,T,T,T,T)
- A12/BC= 0 or 1 : Burst length supports only BL8(Fixed) and BC4(Fixed), not supports BC4(OTF).

When MR0 A[1:0] is set "01" , A12/BC must be always '1'b in MPR read commands (BL8 only).
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1and BG0

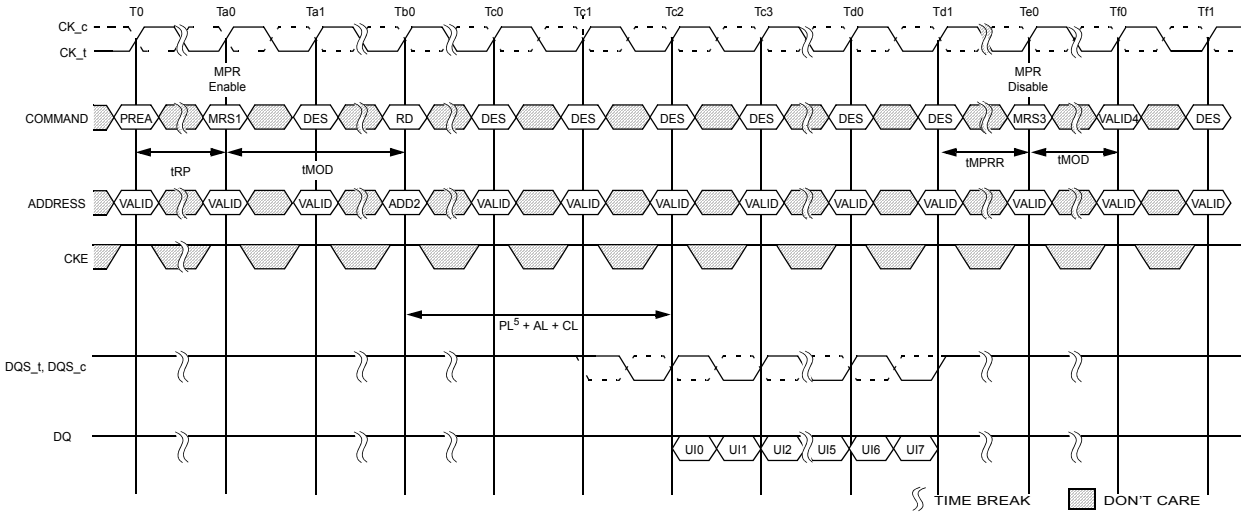
After RL= AL + CL, DRAM bursts out the data from MPR location. The format of data on return is described in a later section and controlled by MR3 bits A0,A1, A11 and A12.

Memory controller repeats these calibration reads until read data capture at memory controller is optimized. Read MPR location can be a different location as specified by the Read command
After end of last MPR read burst, wait until tMPRR is satisfied
MRS MR3, Opcode A2= '0b'
All subsequent reads and writes from DRAM array

Wait until tMRD and tMOD are satisfied

Continue with regular DRAM commands like Activate.

This process is depicted below(PL=0).

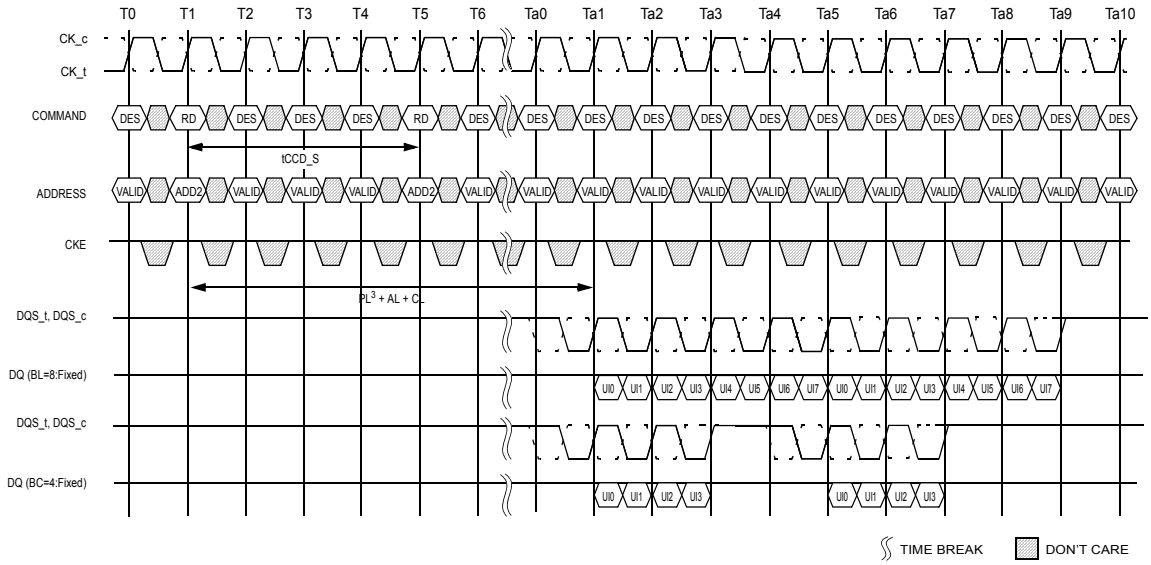


NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations

NOTE 2 Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10” , and must be ‘1’b when MR0 A[1:0] = “01”

NOTE 3 Multi-Purpose Registers Read/Write Disable (MR3 A2 = 0)
NOTE 4 Continue with regular DRAM command.
NOTE 5 PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 15 — MPR Read Timing

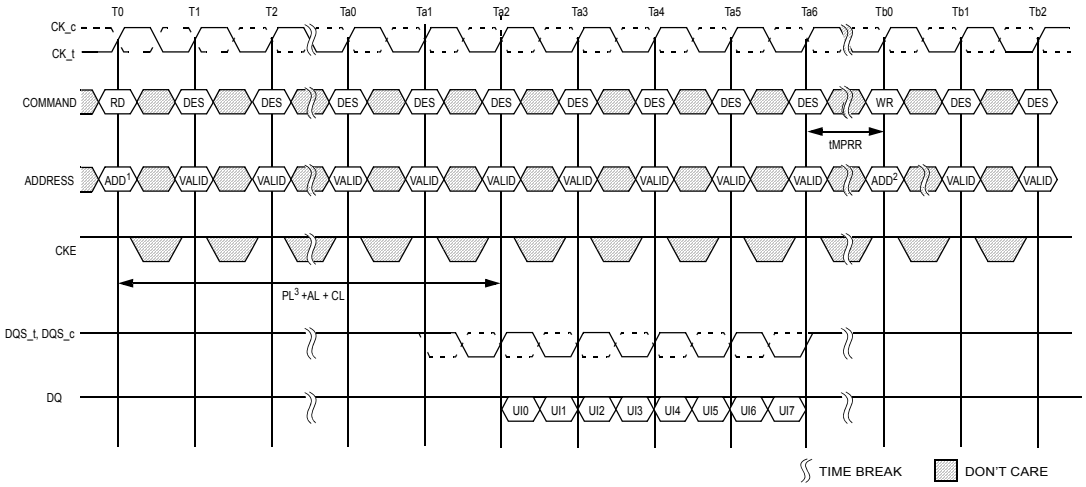


NOTE 1 tCCD_S = 4, Read Preamble = 1tCK

NOTE 2 Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
  (For BC=4, burst order is fixed at 0,1,2,3,T,T,T,T)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10” , and must be ‘1’b when MR0 A[1:0] = “01”

NOTE 3 PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 16 — MPR Back to Back Read Timing



NOTE 1 Address setting
- A[1:0] = "00"b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= "0"b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don't care including BG1 and BG0. A12 is don't care when MR0 A[1:0] = "00", and must be '1'b when MR0 A[1:0] = "01"

NOTE 2 Address setting
- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

NOTE 3 PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 17 — MPR Read to Write Timing

4.10.4 MPR Writes

DDR4 allows 8 bit writes to the MPR location using the address bus A7:A0.

Table 24 — UI and Address Mapping for MPR Location

MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
SDRAM Address	A7	A6	A5	A4	A3	A2	A1	A0
UI	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7

STEPS:
DLL must be locked prior to MPR Writes. If DLL is Enabled : MR1[A0 = 1]
Precharge all
Wait until tRP is satisfied
MRS MR3, Opcode A2='1'b
Redirect all subsequent read and writes to MPR locations

Wait until tMRD and tMOD satisfied.

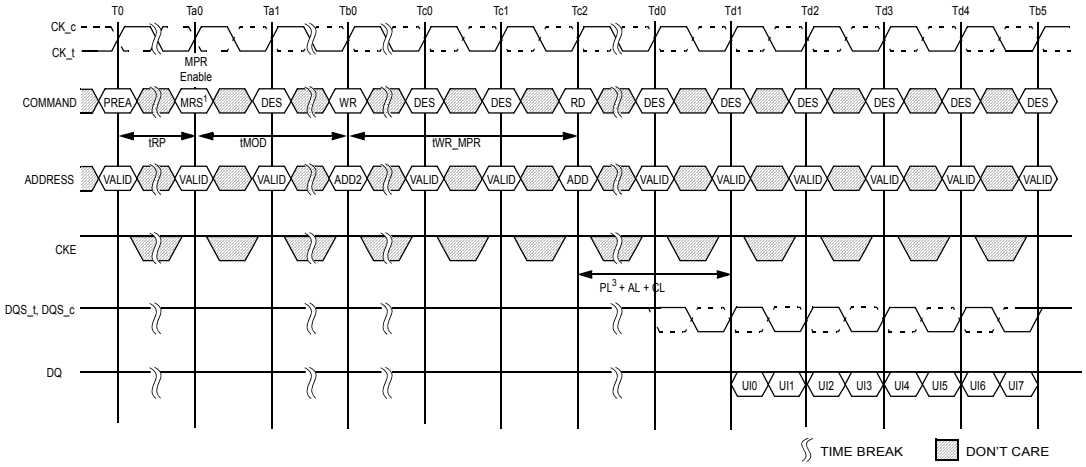
Write command
BA1 and BA0 indicate the MPR location
A [7:0] = data for MPR

Wait until tWR_MPR satisfied, so that DRAM to complete MPR write transaction.

Memory controller repeats these calibration writes and reads until data capture at memory controller is optimized.
After end of last MPR read burst, wait until tMPRR is satisfied
MRS MR3, Opcode A2= '0b'
All subsequent reads and writes from DRAM array

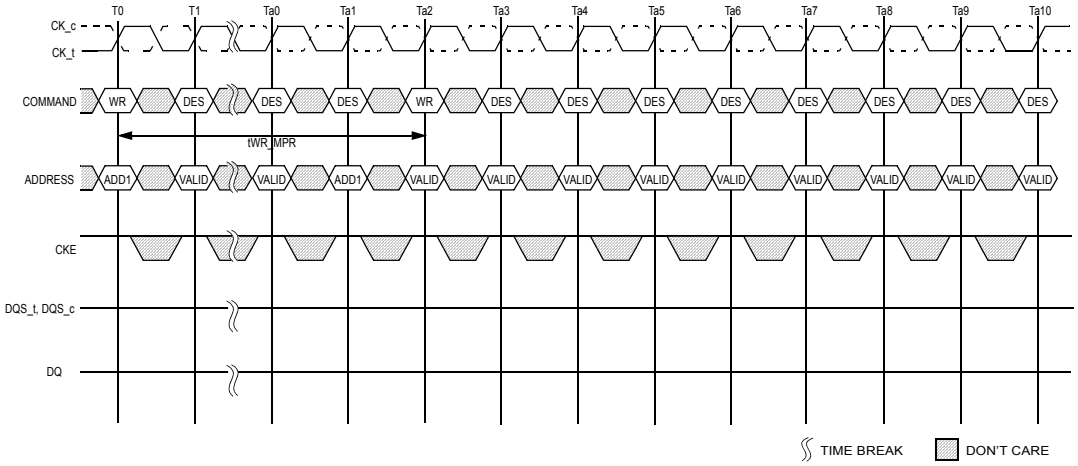
Wait until tMRD and tMOD are satisfied
Continue with regular DRAM commands like Activate.

This process is depicted in Figure 18.



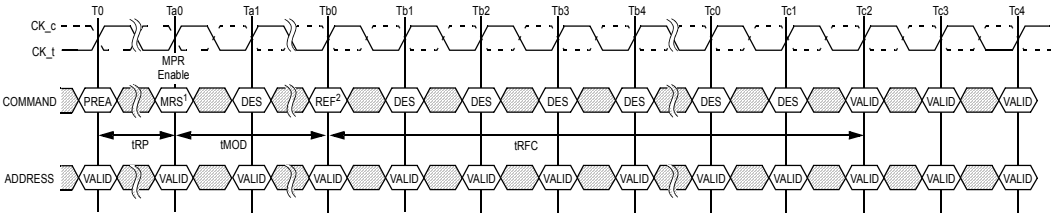
NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
NOTE 2 Address setting - BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.
NOTE 3 PL(Parity latency) is added to Data output delay when C/A parity latency mode is enabled.

Figure 18 — MPR Write Timing and Write to Read Timing



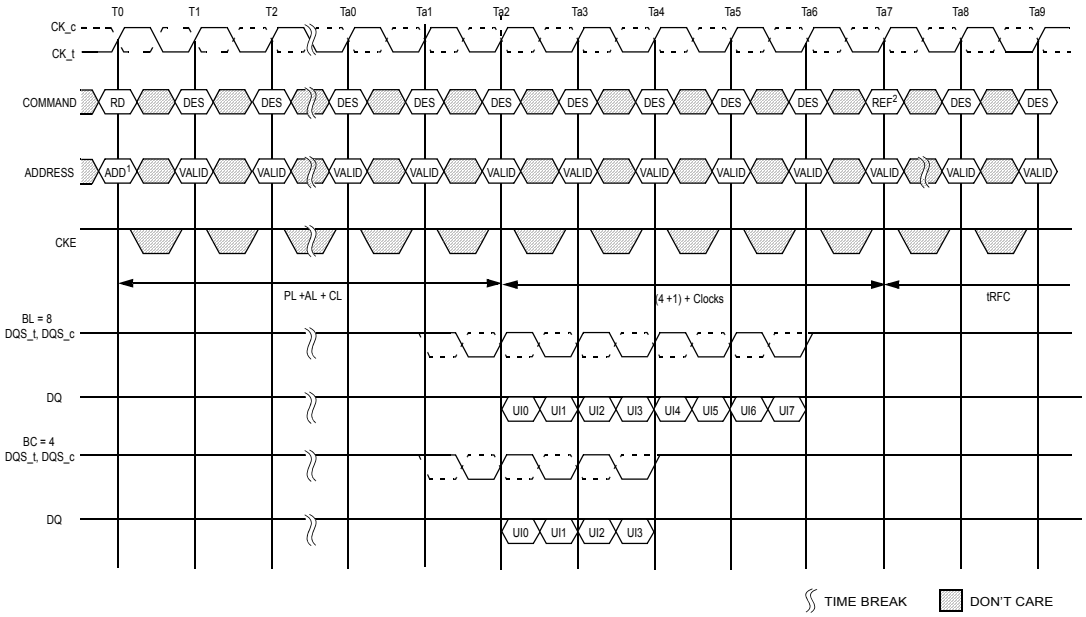
NOTE 1 Address setting
- BA1 and BA0 indicate the MPR location
- A [7:0] = data for MPR
- A10 and other address pins are don't care.

Figure 19 — MPR Back to Back Write Timing



NOTE 1 Multi-Purpose Registers Read/Write Enable (MR3 A2 = 1)
- Redirect all subsequent read and writes to MPR locations
NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

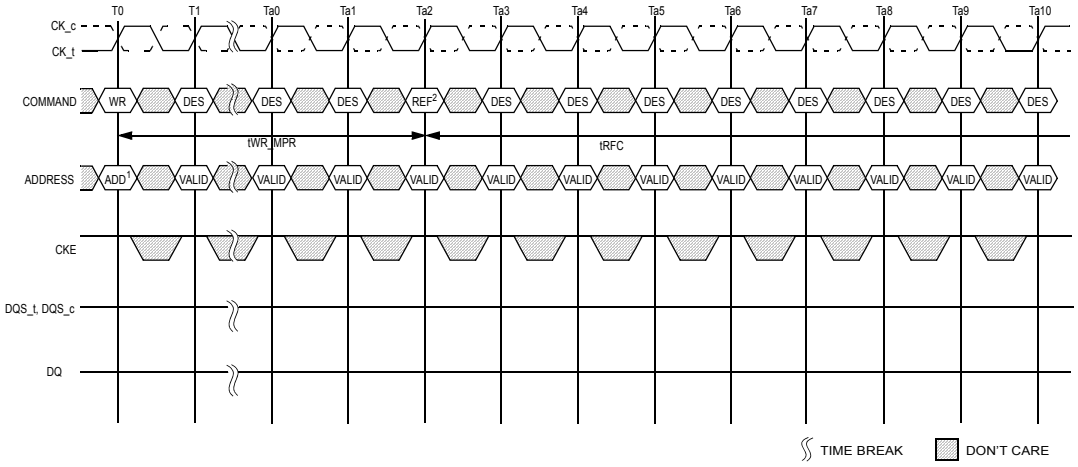
Figure 20 — Refresh Command Timing



NOTE 1 Address setting
- A[1:0] = “00”b (data burst order is fixed starting at nibble, always 00b here)
- A[2]= “0”b (For BL=8, burst order is fixed at 0,1,2,3,4,5,6,7)
- BA1 and BA0 indicate the MPR location
- A10 and other address pins are don’t care including BG1 and BG0. A12 is don’t care when MR0 A[1:0] = “00” or “10” , and must be ‘1’b when MR0 A[1:0] = “01”

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Figure 21 — Read to Refresh Command Timing



NOTE 1 Address setting - BA1 and BA0 indicate the MPR location - A [7:0] = data for MPR
- A10 and other address pins are don’t care.

NOTE 2 1x Refresh is only allowed when MPR mode is Enable.

Figure 22 — Write to Refresh Command Timing

4.10.5 MPR Read Data format

Mode bits in MR3: (A12, A11) are used to select the data return format for MPR reads. The DRAM is required to drive associated strobes with the read data returned for all read data formats.

Serial return implies that the same pattern is returned on all DQ lanes as shown in figure below. Data from the MPR is used on all DQ lanes for the serial return case. Reads from MPR page0, MPR page1 and MPR page3 are alllowed with serial data return mode. In this example the pattern programmed in the MPR register is 0111 111: MPR Location [7:0].

x4 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1

x8 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1

x16 Device

Serial	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	1	1	1	1	1	1	1
DQ1	0	1	1	1	1	1	1	1
DQ2	0	1	1	1	1	1	1	1
DQ3	0	1	1	1	1	1	1	1
DQ4	0	1	1	1	1	1	1	1
DQ5	0	1	1	1	1	1	1	1
DQ6	0	1	1	1	1	1	1	1
DQ7	0	1	1	1	1	1	1	1
DQ8	0	1	1	1	1	1	1	1
DQ9	0	1	1	1	1	1	1	1
DQ10	0	1	1	1	1	1	1	1
DQ11	0	1	1	1	1	1	1	1
DQ12	0	1	1	1	1	1	1	1
DQ13	0	1	1	1	1	1	1	1
DQ14	0	1	1	1	1	1	1	1
DQ15	0	1	1	1	1	1	1	1

Parallel return implies that the MPR data is retuned in the first UI and then repeated in the remaining UI's of the burst as shown in the figure below. Data from Page0 MPR registers can be used for the parallel return case as well. Read from MPR page1, MPR page2 and MPR page3 are not allowed with parallel data return mode. In this example the pattern programmed in the Page 0 MPR register is 0111 1111:MPR Location [7:0] . For the case of x4, only the first four bits are used (0111:MPR Location [7:4] in this example). For the case of x16, the same pattern is repeated on upper and lower bytes.

x4 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1

x8 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1

x16 Device

Parallel	UI0	UI1	UI2	UI3	UI4	UI5	UI6	UI7
DQ0	0	0	0	0	0	0	0	0
DQ1	1	1	1	1	1	1	1	1
DQ2	1	1	1	1	1	1	1	1
DQ3	1	1	1	1	1	1	1	1
DQ4	1	1	1	1	1	1	1	1
DQ5	1	1	1	1	1	1	1	1
DQ6	1	1	1	1	1	1	1	1
DQ7	1	1	1	1	1	1	1	1
DQ8	0	0	0	0	0	0	0	0
DQ9	1	1	1	1	1	1	1	1
DQ10	1	1	1	1	1	1	1	1
DQ11	1	1	1	1	1	1	1	1
DQ12	1	1	1	1	1	1	1	1
DQ13	1	1	1	1	1	1	1	1
DQ14	1	1	1	1	1	1	1	1
DQ15	1	1	1	1	1	1	1	1

The third mode of data return is the staggering of the MPR data across the lanes. In this mode a read command is issued to a specific MPR and then the data is returned on the DQ from different MPR registers. Read from MPR page1, MPR page2, and MPR page3 are not allowed with staggered data return mode.

For a x4 device, a read to MPR0 will result in data from MPR0 being driven on DQ0, data from MPR1 on DQ1 and so forth as shown below.

A read command to MPR1 will result in data from MPR1 being driven on DQ0, data from MPR2 on DQ1 and so forth as shown below. Reads from MPR2 and MPR3 are also shown below.

x4 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3

x4 (Read MPR1 command)

Stagger	UI0-7
DQ0	MPR1
DQ1	MPR2
DQ2	MPR3
DQ3	MPR0

x4 (Read MPR2 command)

Stagger	UI0-7
DQ0	MPR2
DQ1	MPR3
DQ2	MPR0
DQ3	MPR1

x4 (Read MPR3 command)

Stagger	UI0-7
DQ0	MPR3
DQ1	MPR0
DQ2	MPR1
DQ3	MPR2

It is expected that the DRAM can respond to back to back read commands to MPR for all DDR4 frequencies so that a stream as follows can be created on the data bus with no bubbles or clocks between read data. In this case controller issues a sequence of RD MPR0, RD MPR1, RD MPR2, RD MPR3, RD MPR0, RD MPR1, RD MPR2 and RD MPR3.

x4 (Back to Back read commands)

Stagger	UI 0-7	UI 8-15	UI 16-23	UI 24-31	UI 32-39	UI 40-47	UI 48-55	UI 56-63
DQ0	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3
DQ1	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0
DQ2	MPR2	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1
DQ3	MPR3	MPR0	MPR1	MPR2	MPR3	MPR0	MPR1	MPR2

The following figure shows a read command to MPR0 for a x8 device. The same pattern is repeated on the lower nibble as on the upper nibble. Reads to other MPR location follows the same format as for x4 case.

A read example to MPR0 for x8 and x16 device is shown below.

x8 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3
DQ4	MPR0
DQ5	MPR1
DQ6	MPR2
DQ7	MPR3

x16 (Read MPR0 command)

Stagger	UI0-7
DQ0	MPR0
DQ1	MPR1
DQ2	MPR2
DQ3	MPR3
DQ4	MPR0
DQ5	MPR1
DQ6	MPR2
DQ7	MPR3
DQ8	MPR0
DQ9	MPR1
DQ10	MPR2
DQ11	MPR3
DQ12	MPR0
DQ13	MPR1
DQ14	MPR2
DQ15	MPR3

DDR4 MPR mode enable and page selection is done by Mode Register command as shown below.

Table 25 — MPR MR3 Register Definition

Address	Operating Mode	Description
A2	MPR operaion	0 = Normal 1 = Dataflow from/to MPR
A1:A0	MPR selection	00 = page0 01 = page1 10 = page2 11 = page3
A12:A11	MPR Read Format	00 = Serial 01 = Parallel 10 = Staggered 11 = Reserved

Four MPR pages are provided in DDR4 SDRAM. Page 0 is for both read and write, and pages 1,2 and 3 are read-only. Any MPR location (MPR0-3) in page 0 can be readable through any of three readout modes (serial, parallel or staggered), but pages 1, 2 and 3 support only the serial readout mode.

After power up, the content of MPR page 0 should have the default value as defined in the table. MPR page 0 can be writeable only when MPR write command is issued by controller. Unless MPR write command is issued, DRAM must keep the default value permanently, and should never change the content on its own for any purpose.

Table 26 — MPR data format

MPR page0 (Training pattern)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	0	1	0	1	0	1	0	1	Read/Write (default value)
	01= MPR1	0	0	1	1	0	0	1	1	
	10 = MPR2	0	0	0	0	1	1	1	1	
	11 = MPR3	0	0	0	0	0	0	0	0	

NOTE 1 MPRx using A7:A0 that A7 is mapped to location [7] and A0 is mapped to location [0].

MPR page1 (CA parity error log)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	Read-only
	01 = MPR1	CAS_n/ A15	WE_n/ A14	A[13]	A[12]	A[11]	A[10]	A[9]	A[8]	
	10 = MPR2	PAR	ACT_n	BG[1]	BG[0]	BA[1]	BA[0]	A[17]	RAS_n/ A16	
	11 = MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency[4]			C[2]	C[1]	C[0]	
				MR5.A[2]	MR5.A[1]	MR5.A[0]				

NOTE 1 MPR used for C/A parity error log readout is enabled by setting A[2] in MR3
NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

MPR page2 (MRS Readout)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	RFU	RFU	RFU	Temperature Sensor Status(Table1)		CRC Write Enable	Rtt_WR		read-only
		-	-	-	-	-	MR2	MR2		
		-	-	-	-	-	A12	A10	A9	
	01= MPR1	Vref DQ Trng range	Vref DQ training Value						Gear-down Enable	
		MR6	MR6							
		A6	A5	A4	A3	A2	A1	A0	A3	
	10 = MPR2	CAS Latency				RFU	CAS Write Latency			
		MR0				-	MR2			
		A6	A5	A4	A2	-	A5	A4	A3	
	11 = MPR3	Rtt_Nom			Rtt_Park			Driver Impedance		
		MR1			MR5			MR2		
		A10	A9	A6	A8	A7	A6	A2	A1	

MPR page3 (Vendor purpose only)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]	note
BA1:BA0	00 = MPR0	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	read-only
	01= MPR1	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	10 = MPR2	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	
	11 = MPR3	don't care	don't care	don't care	don't care	don't care	don't care	don't care	don't care	

4.11 Data Mask(DM), Data Bus Inversion (DBI) and TDQS

DDR4 SDRAM supports Data Mask (DM) function and Data Bus Inversion (DBI) functionon in x8 and x16 DRAM configuration. x4 DDR4 SDRAM does not support DM and DBI function. x8 DDR4 SDRAM supports TDQS function. x4 and x16 DDR4 SDRAM does not support TDQS function.

DM, DBI & TDQS functions are supported with dedicated one pin labeled as DM_n/DBI_n/TDQS_t. The pin is bi-directional pin for DRAM. The DM_n/DBI _n pin is Active Low as DDR4 supports VDDQ reference termination. TDQS function does not drive actual level on the pin.

DM, DBI & TDQS functions are programmable through DRAM Mode Register (MR). The MR bit location is bit A11 in MR1 and bit A12:A10 in MR5 .

Write operation: Either DM or DBI function can be enabled but both functions cannot be enabled simultanteously. When both DM and DBI functions are disabled, DRAM turns off its input receiver and does not expect any valid logic level.

Read operation: Only DBI function applies. When DBI function is disabled, DRAM turns off its output driver and does not drive any valid logic level.

TDQS function: When TDQS function is enabled, DM & DBI functions are not supported. When TDQS function is disabled, DM and DBI functions are supported as described below in Table 27. When enabled, the same termination resistance function is applied to the TDQS_t/TDQS_c pins that is applied to DQS_t/DQS_c pins.

Table 27 — TDQS Function Matrix

MR1 bit A11	DM (MR5 bit A10)	Write DBI (MR5 bit A11)	Read DBI (MR5 bit A12)
0 (TDQS Disabled)	Enabled	Disabled	Enabled or Disabled
	Disabled	Enabled	Enabled or Disabled
	Disabled	Disabled	Enabled or Disabled
1 (TDQS Enabled)	Disabled	Disabled	Disabled

Table 28 — DRAM Mode Register MR5

A10	DM Enable
0	Disabled
1	Enabled

Table 29 — DRAM Mode Register MR5

A11	Write DBI Enable	A12	Read DBI Enable
0	Disabled	0	Disabled
1	Enabled	1	Enabled

Table 30 — DRAM Mode Register MR1

A11	TDQS Enable
0	Disabled
1	Enabled

DM function during Write operation: DRAM masks the write data received on the DQ inputs if DM_n was sampled Low on a given byte lane. If DM_n was sampled High on a given byte lane, DRAM does not mask the write data and writes into the DRAM core.

DBI function during Write operation: DRAM inverts write data received on the DQ inputs if DBI_n was sampled Low on a given byte lane. If DBI_n was sampled High on a given byte lane, DRAM leaves the data received on the DQ inputs non-inverted.

DBI function during Read operation: DRAM inverts read data on its DQ outputs and drives DBI_n pin Low when the number of ‘0’ data bits within a given byte lane is greater than 4; otherwise DRAM does not invert the read data and drives DBI_n pin High.

Table 31 — x8 DRAM Write DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DM_n or DBI_n	DM0 or DBI0	DM1 or DBI1	DM2 or DBI2	DM3 or DBI3	DM4 or DBI4	DM5 or DBI5	DM6 or DBI6	DM7 or DBI7

Table 32 — x8 DRAM Read DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQ[7:0]	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7
DBI_n	DBI0	DBI1	DBI2	DBI3	DBI4	DBI5	DBI6	DBI7

Table 33 — x16 DRAM Write DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DML_n or DBIL_n	DML0 or DBIL0	DML1 or DBIL1	DML2 or DBIL2	DML3 or DBIL3	DML4 or DBIL4	DML5 or DBIL5	DML6 or DBIL6	DML7 or DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DMU_n or DBIU_n	DMU0 or DBIU0	DMU1 or DBIU1	DMU2 or DBIU2	DMU3 or DBIU3	DMU4 or DBIU4	DMU5 or DBIU5	DMU6 or DBIU6	DMU7 or DBIU7

Table 34 — x16 DRAM Read DQ Frame Format

	Data transfer							
	0	1	2	3	4	5	6	7
DQL[7:0]	LByte 0	LByte 1	LByte 2	LByte 3	LByte 4	LByte 5	LByte 6	LByte 7
DBIL_n	DBIL0	DBIL1	DBIL2	DBIL3	DBIL4	DBIL5	DBIL6	DBIL7
DQU[7:0]	UByte 0	UByte 1	UByte 2	UByte 3	UByte 4	UByte 5	UByte 6	UByte 7
DBIU_n	DBIU0	DBIU1	DBIU2	DBIU3	DBIU4	DBIU5	DBIU6	DBIU7

4.12 ZQ Calibration Commands

4.12.1 ZQ Calibration Description

ZQ Calibration command is used to calibrate DRAM Ron & ODT values. DDR4 SDRAM needs longer time to calibrate output driver and on-die termination circuits at initialization and relatively smaller time to perform periodic calibrations.

ZQCL command is used to perform the initial calibration during power-up initialization sequence. This command may be issued at any time by the controller depending on the system environment. ZQCL command triggers the calibration engine inside the DRAM and, once calibration is achieved, the calibrated values are transferred from the calibration engine to DRAM IO, which gets reflected as updated output driver and on-die termination values.

The first ZQCL command issued after reset is allowed a timing period of tZQinit to perform the full calibration and the transfer of values. All other ZQCL commands except the first ZQCL command issued after RESET are allowed a timing period of tZQoper.

ZQCS command is used to perform periodic calibrations to account for voltage and temperature variations. A shorter timing window is provided to perform the calibration and transfer of values as defined by timing parameter tZQCS. One ZQCS command can effectively correct a minimum of 0.5 % (ZQ Correction) of RON and RTT impedance error within 128 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application-specific parameters. One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\textbf{ZQCorrection}}{\textbf{(TSens x Tdriftrate) + (VSens x Vdriftrate)}}$$

Where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% / oC, VSens = 0.15% / mV, Tdriftrate = 1 oC / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

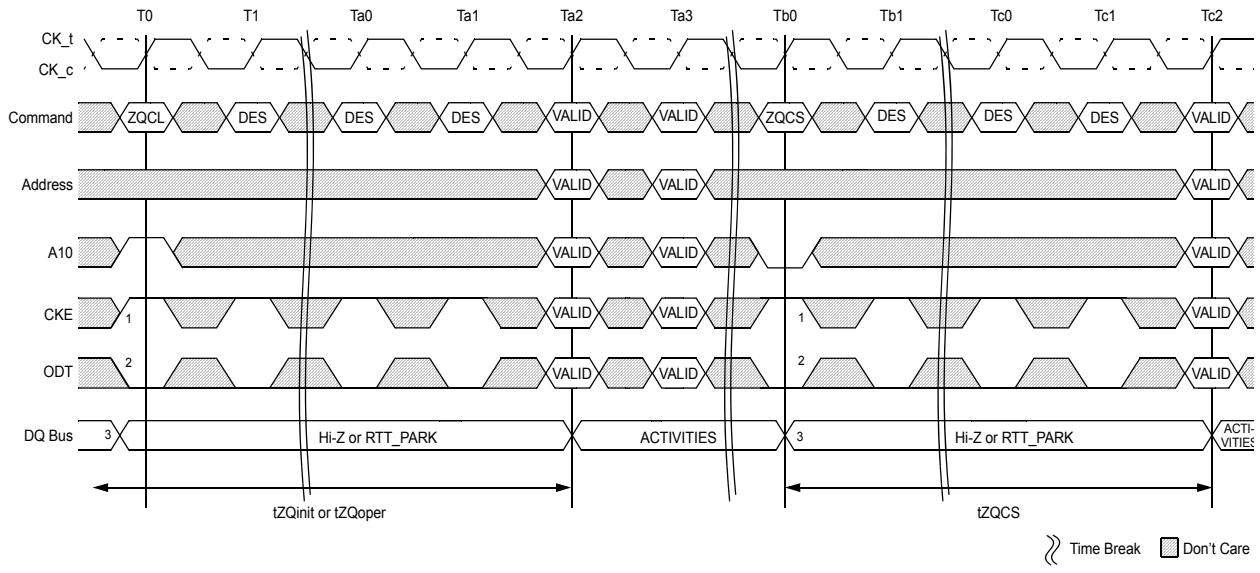
$$\frac{\mathbf{0.5}}{\mathbf{(1.5 \times 1) + (0.15 \times 15)}} = \mathbf{0.133 \approx 128}\boldsymbol{ms}$$

No other activities should be performed on the DRAM channel by the controller for the duration of tZQinit, tZQoper, or tZQCS. The quiet time on the DRAM channel allows accurate calibration of output driver and on-die termination values. Once DRAM calibration is achieved, the DRAM should disable ZQ current consumption path to reduce power.

All banks must be precharged and tRP met before ZQCL or ZQCS commands are issued by the controller. See "Command Truth Table" on Section 4.1 for a description of the ZQCL and ZQCS commands.

ZQ calibration commands can also be issued in parallel to DLL lock time when coming out of self refresh. Upon Self-Refresh exit, DDR4 SDRAM will not perform an IO calibration without an explicit ZQ calibration command. The earliest possible time for ZQ Calibration command (short or long) after self refresh exit is XS, XS_Abort/ XS_FAST depending on operation mode.

In systems that share the ZQ resistor between devices, the controller must not allow any overlap of tZQoper, tZQinit, or tZQCS between the devices.



NOTE 1 CKE must be continuously registered high during the calibration procedure.
NOTE 2 During ZQ Calibration, ODT signal must be held LOW and DRAM continues to provide RTT_PARK.
NOTE 3 All devices connected to the DQ bus should be high impedance or RTT_PARK during the calibration procedure.

Figure 23 — ZQ Calibration Timing

4.13 DQ Vref Training

The DRAM internal DQ Vref specification parameters are operating voltage range, stepsize, Vref step time, Vref full step time and Vref valid level.

The voltage operating range specifies the minimum required Vref setting range for DDR4 DRAM devices. The minimum range is defined by Vrefmax and Vrefmin as depicted in Figure 24 below.

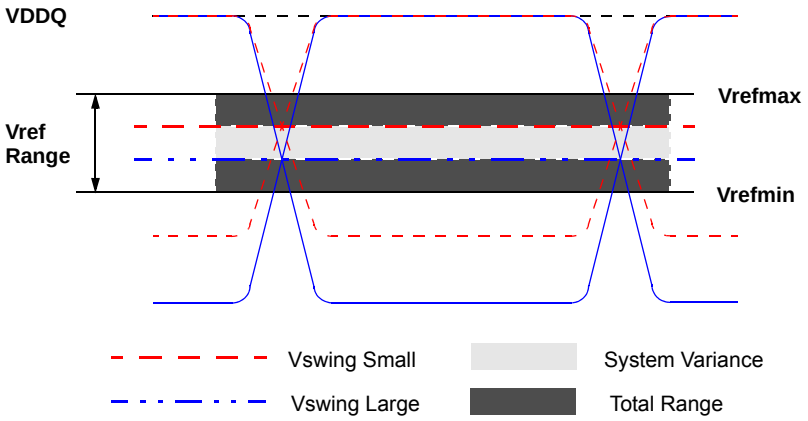


Figure 24 — Vref operating range(Vrefmin, Vrefmax)

The Vref stepsize is defined as the stepsize between adjacent steps. Vref stepsize ranges from 0.5% VDDQ to 0.8% VDDQ. However, for a given design, DRAM has one value for Vref step size that falls within the range.

The Vref set tolerance is the variation in the Vref voltage from the ideal setting. This accounts for accumulated error over multiple steps. There are two ranges for Vref set tolerance uncertainity. The range of Vref set tolerance uncertainty is a function of number of steps n.

The Vref set tolerance is measured with respect to the ideal line which is based on the two endpoints. Where the endpoints are at the min and max Vref values for a specified range. An illustration depicting an example of the stepsize and Vref set tolerance is below.

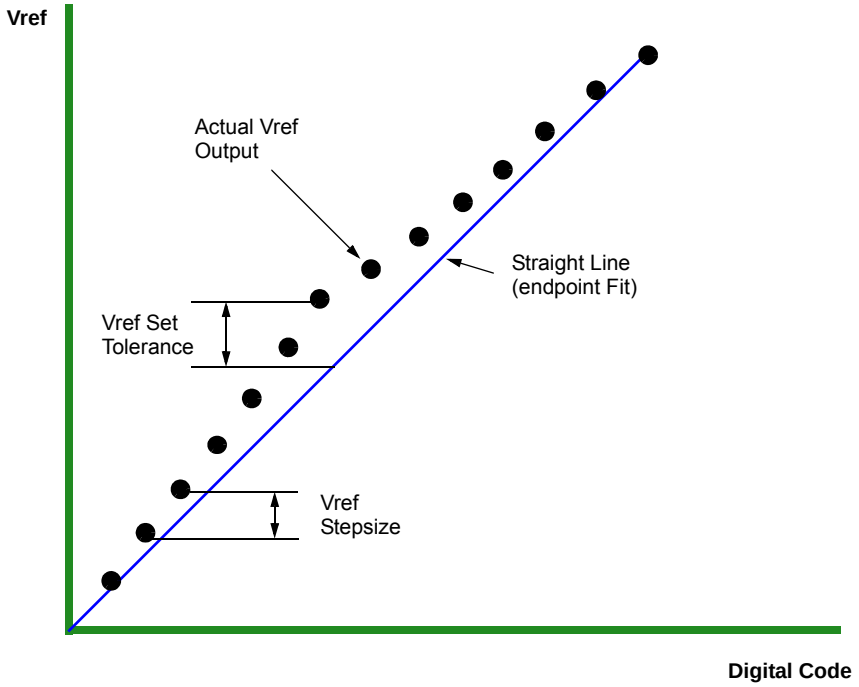


Figure 25 — Example of Vref set tolerance(max case only shown) and stepsize

The Vref increment/decrement step times are define by Vref_time-short and long. The Vref_time-short and long is defined from t0 to t1 as shown in the Figure 26 below where t1 is referenced to when the vref voltage is at the final DC level within the Vref valid tolerance(Vref_val_tol).

The Vref valid level is defined by Vref_val tolerance to qualify the step time t1 as shown in Figure 28 through Figure 31. This parameter is used to insure an adequate RC time constant behavior of the voltage level change after any Vref increment/decrement adjustment. This parameter is only applicable for DRAM component level validation/characterization.

Vref_time-Short is for a single stepsize increment/decrement change in Vref voltage.
Vref_time-Long is the time including up to Vrefmin to Vrefmax or Vrefmax to Vrefmin change in Vref voltage.

t0 - is referenced to MRS command clock
t1 - is referenced to the Vref_val_tol

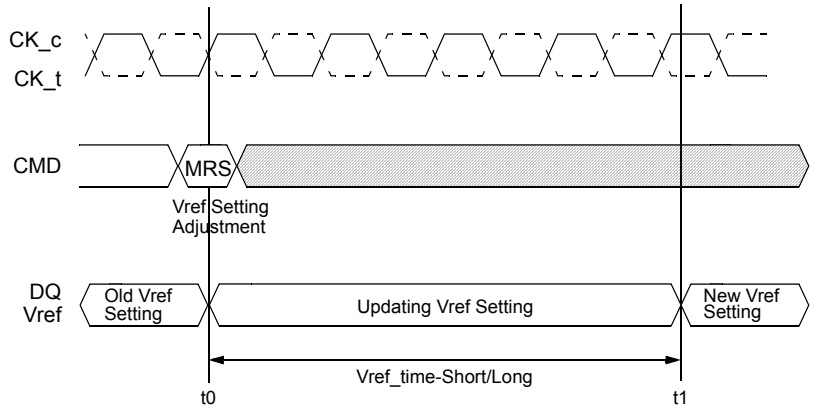
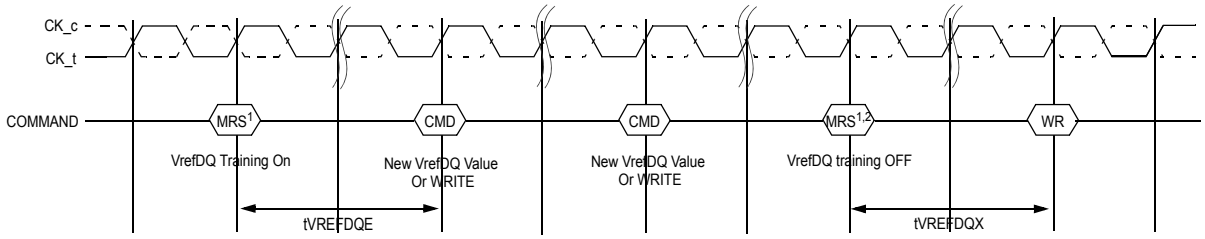


Figure 26 — Vref_time for short and long timing diagram

A MRS command to the mode register bits 5:0 of MR6 are used to program the vref value. VrefDQ training mode is enabled/disabled by A7 of MR6 and training range can be selected by A6 of MR6. When VrefDQ training mode is entered/exited, the following parameter needs to be satisfied to prevent current consumption and also stable operation



NOTE 1 New VrefDQ value is not allowed with MRS commands for training mode exit.
NOTE 2 Depending on the step size of the latest programmed VREF value, Vref_time_short or Vref_time_long must be satisfied before disabling VrefDQ training mode.

Figure 27 — VrefDQ training mode entry and exit timing diagram

Table 35 — AC parameters of DDR4 VrefDQ training

Speed		DDR4-1600,1866,2133,2400,2666,3200		Units	NOTE
Parameter	Symbol	MIN	MAX		
VrefDQ training					
Enter VrefDQ training mode to the first write or VREFDQ MRS command delay	tVREFDQE	150	-	ns	
Exit VrefDQ training mode to the first write command delay	tVREFDQX	150	-	ns	

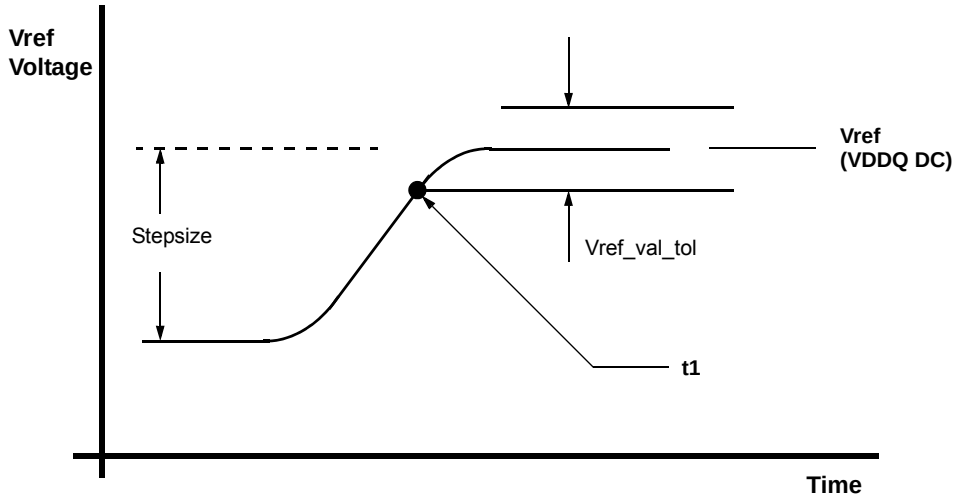


Figure 28 — Vref step single stepsize increment case

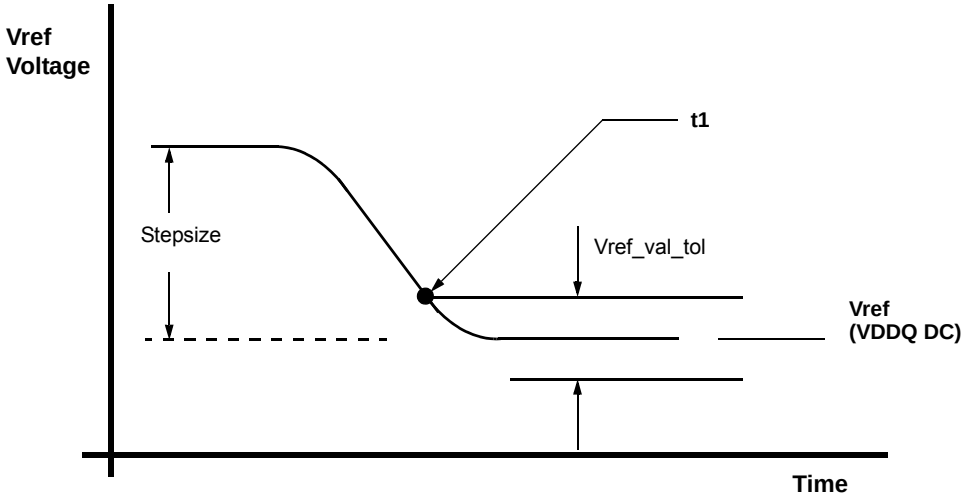


Figure 29 — Vref step single stepsize decrement case

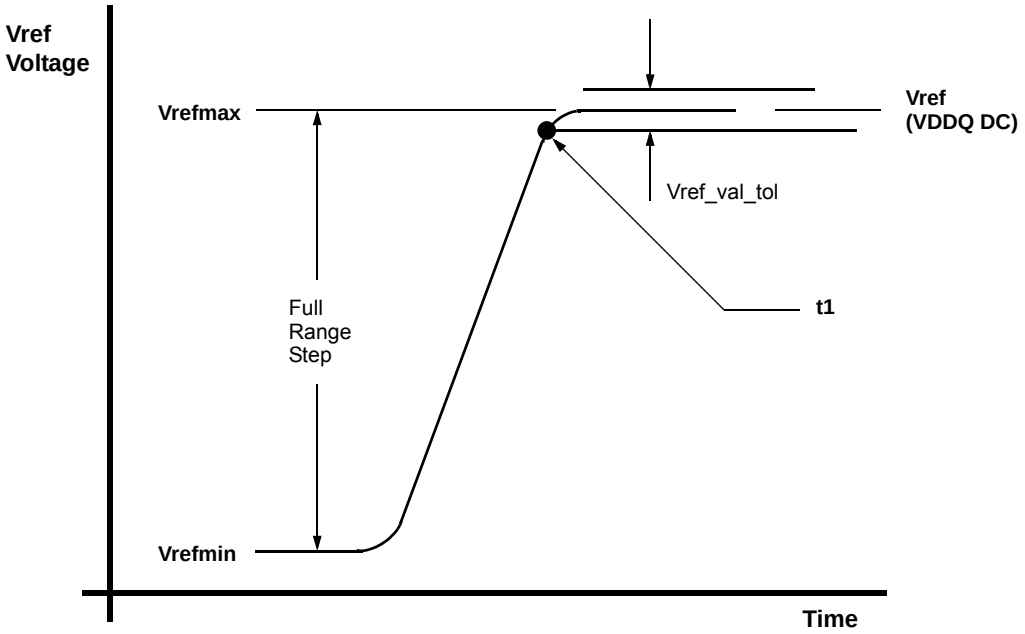


Figure 30 — Vref full step from Vrefmin to Vrefmax case

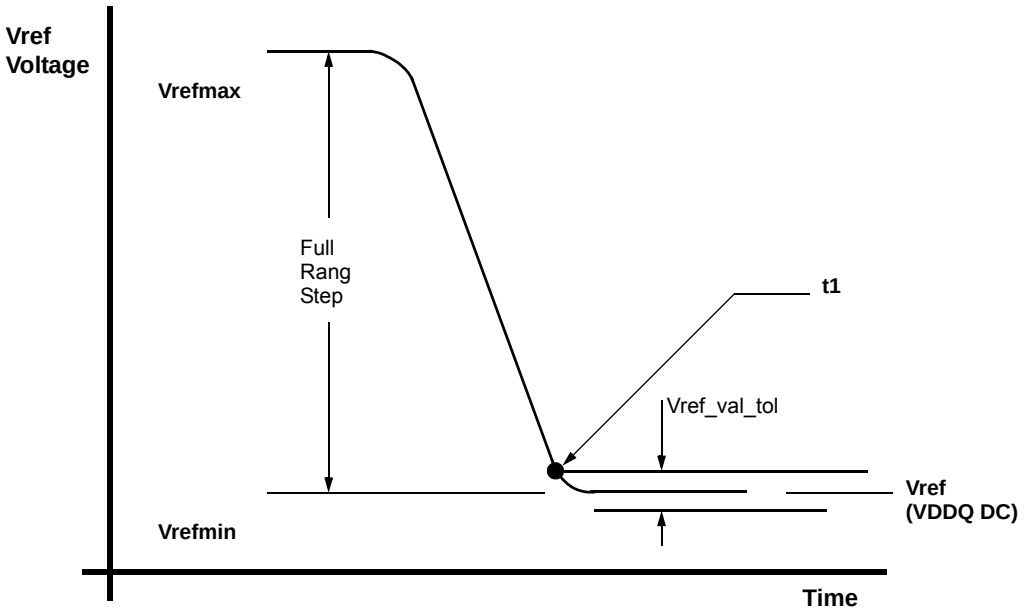


Figure 31 — Vref full step from Vrefmax to Vrefmin case

Table 36 — DQ Internal Vref Specifications

Prarmeter	Symbol	Min	Typ	Max	Unit	NOTE
Vref Max operating point Range1	$V_{ref_max_R1}$	92%	-	-	VDDQ	1, 11
Vref Min operating point Range1	$V_{ref_min_R1}$	-	-	60%	VDDQ	1, 11
Vref Max operating point Range2	$V_{ref_max_R2}$	77%	-	-	VDDQ	1, 11
Vref Min operating point Range2	$V_{ref_min_R2}$	-	-	45%	VDDQ	1, 11
Vref Stepsize	$V_{ref\ step}$	0.50%	0.65%	0.80%	VDDQ	2
Vref Set Tolerance	$V_{ref_set_tol}$	-1.625%	0.00%	1.625%	VDDQ	3,4,6
		-0.15%	0.00%	0.15%	VDDQ	3,5,7
Vref Step Time	$V_{ref_time\text{-}Short}$	-	-	60	ns	8,12
	$V_{ref_time\text{-}Long}$	-	-	150	ns	9,12
Vref Valid tolerance	$V_{ref_val_tol}$	-0.15%	0.00%	0.15%	VDDQ	10

NOTE 1. Vref DC voltage referenced to VDDQ_DC. VDDQ_DC is 1.2V
NOTE 2. Vref stepsize increment/decrement range. Vref at DC level.
NOTE 3. Vref_new = Vref_old+n*Vref_step; n=number of step; if increment use "+"; If decrement use "-"
NOTE 4 The minimum value of Vref setting tolerance=Vref_new-1.625%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+1.625%*VDDQ. For n>4
NOTE 5 The minimum value of Vref setting tolerance=Vref_new-0.15%*VDDQ. The maximum value of Vref setting tolerance=Vref_new+0.15%*VDDQ. For n≤4
NOTE 6 Measured by recording the min and max values of the Vref output over the range, drawing a straight line between those points and comparing all other Vref output settings to that line
NOTE 7 Measured by recording the min and max values of the Vref output across 4 consecutive steps(n=4), drawing a straight line between those points and comparing all other Vref output settings to that line
NOTE 8 Time from MRS command to increment or decrement one step size for Vref
NOTE 9 Time from MRS command to increment or decrement more than one step size up to full range of Vref
NOTE 10 Only applicable for DRAM component level test/characterization purpose. Not applicable for normal mode of operation. Vref valid is to qualify the step times which will be characterized at the component level.
NOTE 11 DRAM range1 or 2 set by MRS bit MR6,A6.
NOTE 12 If the Vref monitor is enabled, Vref_time-long and Vref_time-short must be derated by: +10ns if DQ load is 0pF and an additional +15ns/pF of DQ loading.

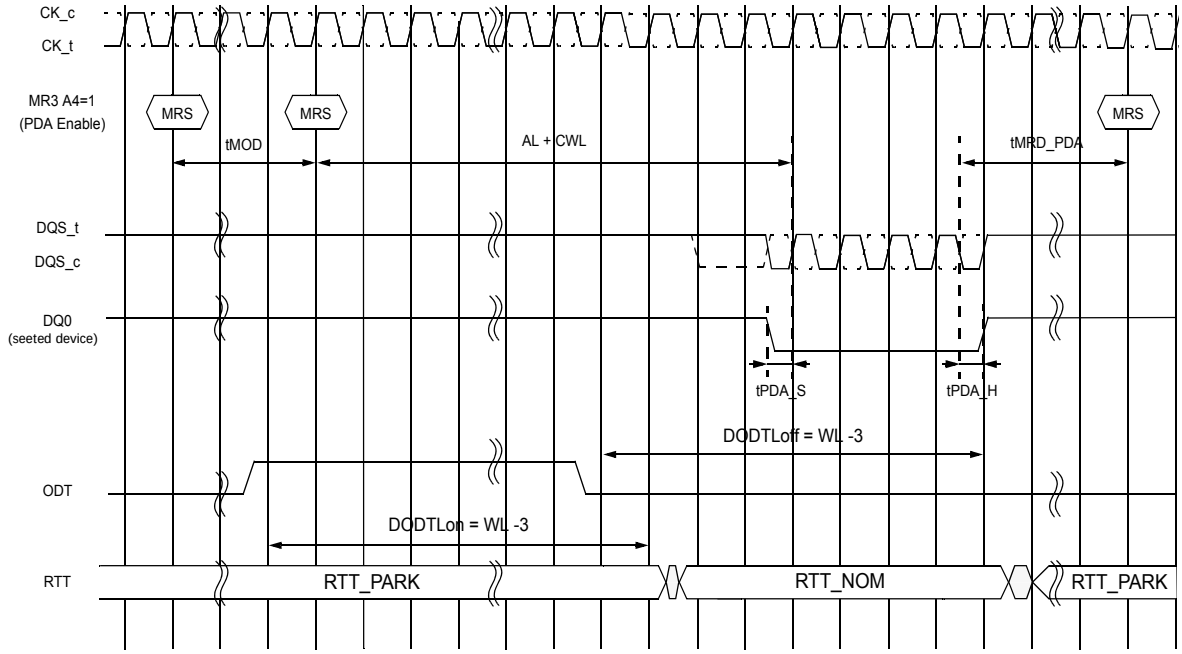
4.14 Per DRAM Addressability

DDR4 allows programmability of a given device on a rank. As an example, this feature can be used to program different ODT or Vref values on DRAM devices on a given rank.

1. Before entering 'per DRAM addressability (PDA)' mode, the write leveling is required.
2. Before entering 'per DRAM addressability (PDA)' mode, the following Mode Register setting is possible.
   -RTT_PARK MR5 {A8:A6} = Enable
   -RTT_NOM MR1 {A10:A9:A8} = Enable
3. Enable 'per DRAM addressability (PDA)' mode using MR3 bit "A4=1".
4. In the 'per DRAM addressability' mode, all MRS command is qualified with DQ0. DRAM captures DQ0 by using DQS_c and DQS_t signals as shown Figure 32 . If the value on DQ0 is 0 then the DRAM executes the MRS command. If the value on DQ0 is 1, then the DRAM ignores the MRS command. The controller can choose to drive all the DQ bits.
5. Program the desired devices and mode registers using MRS command and DQ0.
6. In the 'per DRAM addressability' mode, only MRS commands are allowed.
7. The mode register set command cycle time at PDA mode, AL + CWL + 3.5nCK + tMRD_PDA is required to complete the write operation to the mode register and is the minimum time required between two MRS commands shown in Figure 32.
8. Remove the DRAM from 'per DRAM addressability' mode by setting MR3 bit "A4=0". (This command will require DQ0=0 which shown in Figure 33.
   Note: Removing a DRAM from per DRAM addressability mode will require programming the entire MR3 when the MRS command is issued. This may impact some per DRAM values programmed within a rank as the exit command is sent to the rank. In order to avoid such a case the PDA Enable/Disable Control bit is located in a mode register that does not have any 'per DRAM addressability' mode controls). In per DRAM addressability mode, DRAM captures DQ0 using DQS_t and DQS_c like normal write operation. However, Dynamic ODT is not supported. So extra care required for the ODT setting. If RTT_NOM MR1 {A10:A9:A8} = Enable, DDR4 SDRAM data termination need to be controlled by ODT pin and apply the same timing parameters as defined in Direct ODT function that shown in Table 37.

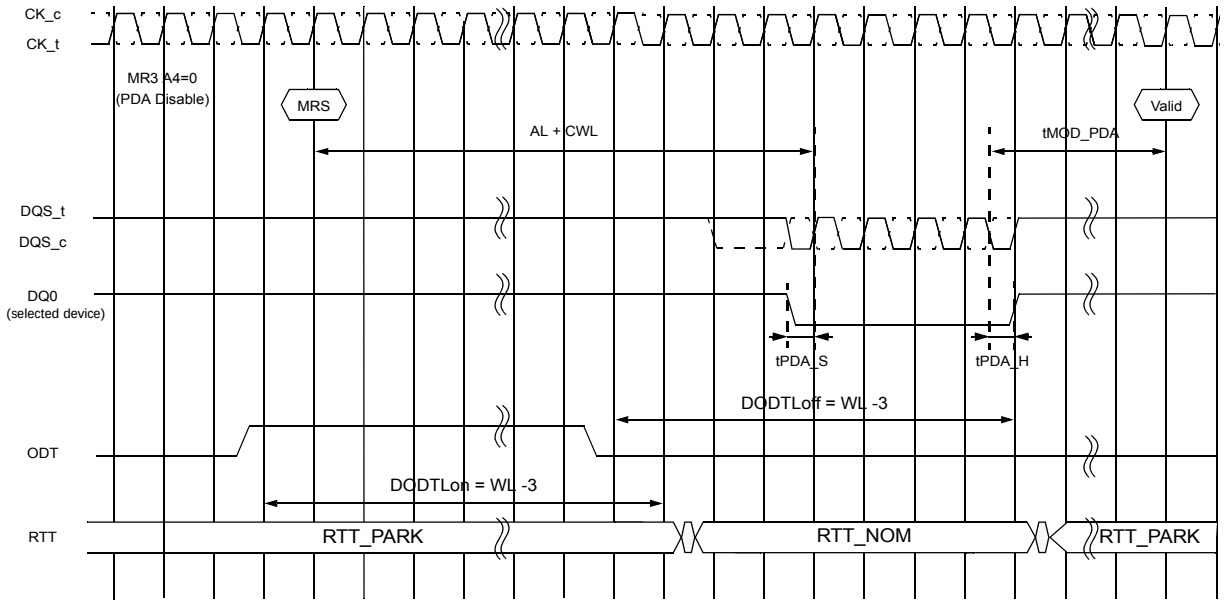
Table 37 — Applied ODT Timing Parameter to PDA Mode

Symbol	Parameter
DODTLon	Direct ODT turn on latency
DODTLoff	Direct ODT turn off latency
tADC	RTT change timing skew
tAONAS	Asynchronous RTT_NOM turn-on delay
tAOFAS	Asynchronous RTT_NOM turn-off delay



NOTE RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON

Figure 32 — MRS w/ per DRAM addressability (PDA) issuing before MRS



NOTE RTT_PARK = Enable, RTT_NOM = Enable, Write Preamble Set = 2tCK and DLL = ON

Figure 33 — MRS w/ per DRAM addressability (PDA) Exit

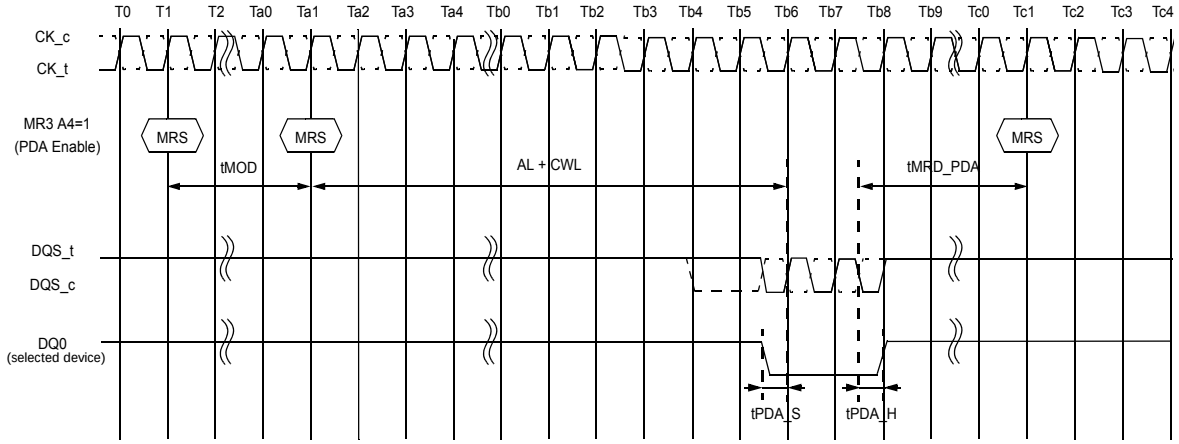


Figure 34 — PDA using Burst Chop 4

tPDA_S = tDS and tPDA_H = tDH for all DDR4 speed bins.

Since PDA mode may be used to program optimal Vref for the DRAM, the DRAM may incorrectly read DQ level at the first DQS edge and the last falling DQS edge. It is recommended that DRAM samples DQ0 on either the first falling or second rising DQS edges. This will enable a common implementation between BC4 and BL8 modes on the DRAM. Controller is required to drive DQ0 to a

'Stable Low or High' during the length of the data transfer for BC4 and BL8 cases.

4.15 CAL Mode (CS_n to Command Address Latency)

4.15.1 CAL Mode Description

DDR4 supports Command Address Latency, CAL, function as a power savings feature. CAL is the delay in clock cycles between CS_n and CMD/ADDR defined by MR4[A8:A6] (See Figure 35).

CAL gives the DRAM time to enable the CMD/ADDR receivers before a command is issued. Once the command and the address are latched,the receivers can be disabled. For consecutive commands, the DRAM will keep the receivers enabled for the duration of the command sequence (See Figure 36)

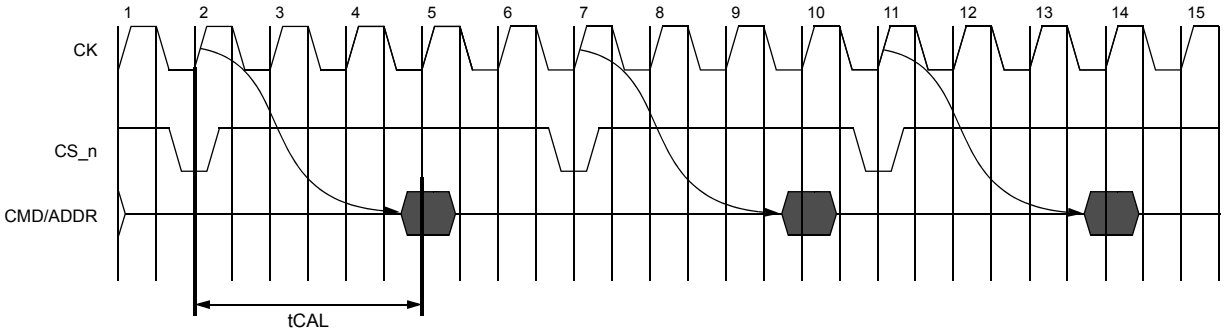


Figure 35 — Definition of CAL

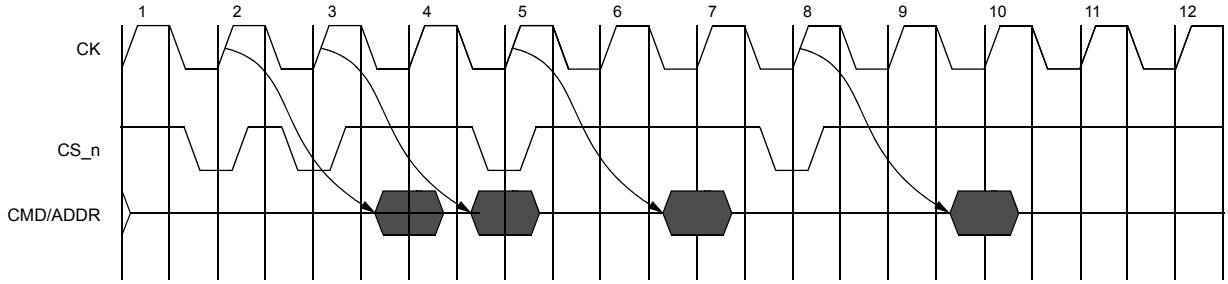


Figure 36 — CAL operational timing for consecutive command issues

The following tables show the timing requirements for tCAL (Table 38) and MRS settings (Table 39) at different data rates.

Table 38 — CS to Command Address Latency

Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
CS to Command Address Latency	CAL	3	4	4	5	nCK

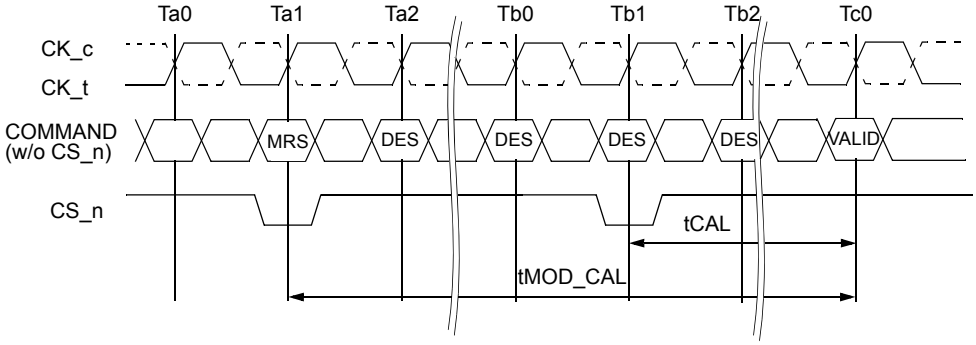
Parameter	Symbol	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	Units
CS to Command Address Latency (Gear down mode even CK)	CAL	4	4	4	6	nCK

Table 39 — MRS settings for CAL

A8:A6 @ MR4	CAL(tCK cycles)
000	default(disable)
001	3
010	4
011	5
100	6
101	8
110	Reserve
111	Reserve

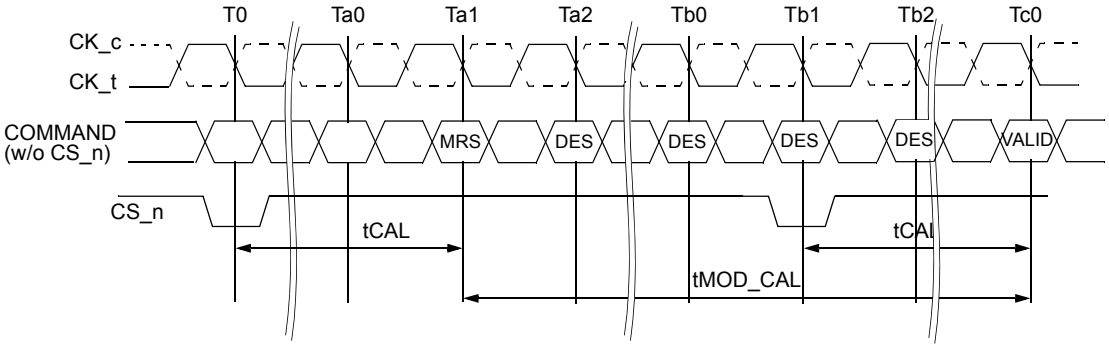
MRS Timings with Command/Address Latency enabled

When Command/Address latency mode is enabled, users must allow more time for MRS commands to take effect. When CAL mode is enabled, or being enabled by an MRS command, the earliest the next valid command can be issued is tMOD_CAL, where tMOD_CAL=tMOD+tCAL.



NOTE 1 MRS command at Ta1 enables CAL mode
NOTE 2 tMOD_CAL=tMOD+tCAL

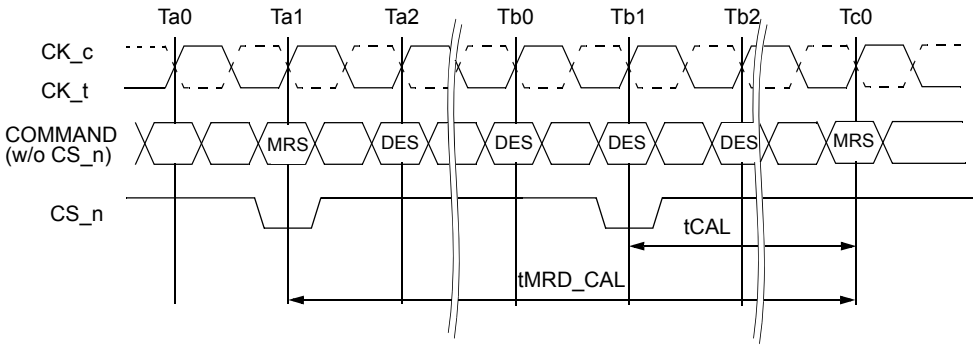
Figure 37 — CAL enable timing - tMOD_CAL



NOTE 1 MRS at Ta1 may or may not modify CAL, tMOD_CAL is computed based on new tCAL setting.
NOTE 2 tMOD_CAL=tMOD+tCAL.

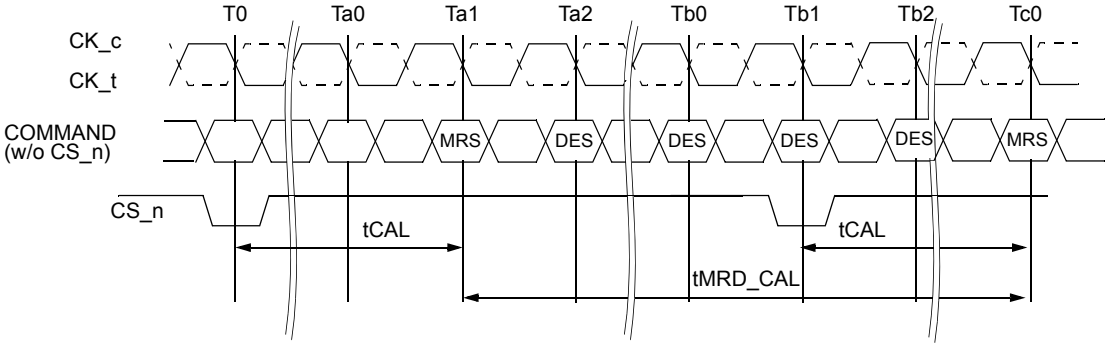
Figure 38 — tMOD_CAL, MRS to valid command timing with CAL enabled

When Command/Address latency is enabled or being entered, users must wait tMRD_CAL until the next MRS command can be issued. tMRD_CAL=tMOD+tCAL.



NOTE 1 MRS command at Ta1 enables CAL mode
NOTE 2 tMRD_CAL=tMOD+tCAL

Figure 39 — CAL enabling MRS to next MRS command, tMRD_CAL



NOTE 1 MRS at Ta1 may or may not modify CAL, tMRD_CAL is computed based on new tCAL setting.
NOTE 2 tMRD_CAL=tMOD+tCAL.

Figure 40 — tMRD_CAL, mode register cycle time with CAL enabled

4.16 CRC

4.16.1 CRC Polynomial and logic equation

DDR4 supports CRC for write operation, and doesn't support CRC for read operation.

The CRC polynomial used by DDR4 is the ATM-8 HEC, X^8+X^2+X^1+1

A combinatorial logic block implementation of this 8-bit CRC for 72-bits of data contains 272 two-input XOR gates contained in eight 6 XOR gate deep trees.

The CRC polynomial and combinatorial logic used by DDR4 is the same as used on GDDR5.

Table 40 — Error Detection Details

ERROR TYPE	DETECTION CAPABILITY
Random Single Bit Error	100%
Random Double Bit Error	100%
Random Odd Count Error	100%
Random one Multi-bit UI vertical column error detection excluding DBI bits	100%

CRC COMBINATORIAL LOGIC EQUATIONS

```
module CRC8_D72;
// polynomial: (0 1 2 8)
// data width: 72
// convention: the first serial data bit is D[71]
// initial condition all 0 implied
function [7:0]
nextCRC8_D72;
input [71:0] Data;
reg [71:0] D;
reg [7:0] NewCRC;
begin
D = Data;

NewCRC[0] = D[69] ^ D[68] ^ D[67] ^ D[66] ^ D[64] ^ D[63] ^ D[60] ^
            D[56] ^ D[54] ^ D[53] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^
            D[45] ^ D[43] ^ D[40] ^ D[39] ^ D[35] ^ D[34] ^ D[31] ^
            D[30] ^ D[28] ^ D[23] ^ D[21] ^ D[19] ^ D[18] ^ D[16] ^
            D[14] ^ D[12] ^ D[8] ^ D[7] ^ D[6] ^ D[0] ;
NewCRC[1] = D[70] ^ D[66] ^ D[65] ^ D[63] ^ D[61] ^ D[60] ^ D[57] ^
            D[56] ^ D[55] ^ D[52] ^ D[51] ^ D[48] ^ D[46] ^ D[45] ^
            D[44] ^ D[43] ^ D[41] ^ D[39] ^ D[36] ^ D[34] ^ D[32] ^
            D[30] ^ D[29] ^ D[28] ^ D[24] ^ D[23] ^ D[22] ^ D[21] ^
            D[20] ^ D[18] ^ D[17] ^ D[16] ^ D[15] ^ D[14] ^ D[13] ^
            D[12] ^ D[9] ^ D[6] ^ D[1] ^ D[0];
NewCRC[2] = D[71] ^ D[69] ^ D[68] ^ D[63] ^ D[62] ^ D[61] ^ D[60] ^
            D[58] ^ D[57] ^ D[54] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
            D[44] ^ D[43] ^ D[42] ^ D[39] ^ D[37] ^ D[34] ^ D[33] ^
            D[29] ^ D[28] ^ D[25] ^ D[24] ^ D[22] ^ D[17] ^ D[15] ^
            D[13] ^ D[12] ^ D[10] ^ D[8] ^ D[6] ^ D[2] ^ D[1] ^ D[0];
NewCRC[3] = D[70] ^ D[69] ^ D[64] ^ D[63] ^ D[62] ^ D[61] ^ D[59] ^
            D[58] ^ D[55] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^ D[45] ^
            D[44] ^ D[43] ^ D[40] ^ D[38] ^ D[35] ^ D[34] ^ D[30] ^
            D[29] ^ D[26] ^ D[25] ^ D[23] ^ D[18] ^ D[16] ^ D[14] ^
            D[13] ^ D[11] ^ D[9] ^ D[7] ^ D[3] ^ D[2] ^ D[1];
NewCRC[4] = D[71] ^ D[70] ^ D[65] ^ D[64] ^ D[63] ^ D[62] ^ D[60] ^
            D[59] ^ D[56] ^ D[52] ^ D[50] ^ D[49] ^ D[48] ^ D[46] ^
            D[45] ^ D[44] ^ D[41] ^ D[39] ^ D[36] ^ D[35] ^ D[31] ^
            D[30] ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15] ^
            D[14] ^ D[12] ^ D[10] ^ D[8] ^ D[4] ^ D[3] ^ D[2];
NewCRC[5] = D[71] ^ D[66] ^ D[65] ^ D[64] ^ D[63] ^ D[61] ^ D[60] ^
            D[57] ^ D[53] ^ D[51] ^ D[50] ^ D[49] ^ D[47] ^ D[46] ^
            D[45] ^ D[42] ^ D[40] ^ D[37] ^ D[36] ^ D[32] ^ D[31] ^
            D[28] ^ D[27] ^ D[25] ^ D[20] ^ D[18] ^ D[16] ^ D[15] ^
            D[13] ^ D[11] ^ D[9] ^ D[5] ^ D[4] ^ D[3];
NewCRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62] ^ D[61] ^ D[58] ^
            D[54] ^ D[52] ^ D[51] ^ D[50] ^ D[48] ^ D[47] ^ D[46] ^
            D[43] ^ D[41] ^ D[38] ^ D[37] ^ D[33] ^ D[32] ^ D[29] ^
            D[28] ^ D[26] ^ D[21] ^ D[19] ^ D[17] ^ D[16] ^ D[14] ^
            D[12] ^ D[10] ^ D[6] ^ D[5] ^ D[4];
NewCRC[7] = D[68] ^ D[67] ^ D[66] ^ D[65] ^ D[63] ^ D[62] ^ D[59] ^
            D[55] ^ D[53] ^ D[52] ^ D[51] ^ D[49] ^ D[48] ^ D[47] ^
            D[44] ^ D[42] ^ D[39] ^ D[38] ^ D[34] ^ D[33] ^ D[30] ^
            D[29] ^ D[27] ^ D[22] ^ D[20] ^ D[18] ^ D[17] ^ D[15] ^
            D[13] ^ D[11] ^ D[7] ^ D[6] ^ D[5];

nextCRC8_D72 = NewCRC;
```

4.16.2 CRC data bit mapping for x8 devices

The following figure shows detailed bit mapping for a x8 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBI_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1

4.16.3 CRC data bit mapping for x4 devices

The following figure shows detailed bit mapping for a x4 device.

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	CRC4
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	CRC5
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	CRC6
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	CRC7

4.16.4 CRC data bit mapping for x16 devices

A x16 device is treated as two x8 devices. x16 device will have two identical CRC trees implemented. CRC(0-7) covers data bits d(0-71). CRC(8-15) covers data bits d(72-143).

	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	d4	d5	d6	d7	CRC0	1
DQ1	d8	d9	d10	d11	d12	d13	d14	d15	CRC1	1
DQ2	d16	d17	d18	d19	d20	d21	d22	d23	CRC2	1
DQ3	d24	d25	d26	d27	d28	d29	d30	d31	CRC3	1
DQ4	d32	d33	d34	d35	d36	d37	d38	d39	CRC4	1
DQ5	d40	d41	d42	d43	d44	d45	d46	d47	CRC5	1
DQ6	d48	d49	d50	d51	d52	d53	d54	d55	CRC6	1
DQ7	d56	d57	d58	d59	d60	d61	d62	d63	CRC7	1
DBIL_n	d64	d65	d66	d67	d68	d69	d70	d71	1	1
DQ8	d72	d73	d74	d75	d76	d77	d78	d79	CRC8	1
DQ9	d80	d81	d82	d83	d84	d85	d86	d87	CRC9	1
DQ10	d88	d89	d90	d91	d92	d93	d94	d95	CRC10	1
DQ11	d96	d97	d98	d99	d100	d101	d102	d103	CRC11	1
DQ12	d104	d105	d106	d107	d108	d109	d110	d111	CRC12	1
DQ13	d112	d113	d114	d115	d116	d117	d118	d119	CRC13	1
DQ14	d120	d121	d122	d123	d124	d125	d126	d127	CRC14	1
DQ15	d128	d129	d130	d131	d132	d133	d134	d135	CRC15	1
DBIU_n	d136	d137	d138	d139	d140	d141	d142	d143	1	1

4.16.5 Write CRC for x4, x8 and x16 devices

The Controller generates the CRC checksum and forms the write data frames as shown in Section 4.16.1 to Section 4.16.4.

For a x8 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBI_n lane if DBI function is enabled.

For a x16 DRAM the controller must send 1's in the transfer 9 if CRC is enabled and must send 1's in transfer 8 and transfer 9 of the DBIL_n and DBIU_n lanes if DBI function is enabled.

The DRAM checks for an error in a received code word D[71:0] by comparing the received checksum against the computed checksum and reports errors using the ALERT_n signal if there is a mis-match.

A x8 device has a CRC tree with 72 input bits. The upper 8 bits are used for DBI inputs if DBI is enabled. If DBI is disabled then the inputs of the upper 8 bits D[71:64] are '1's.

A x16 device has two identical CRC trees with 72 input bits each. The upper 8 bits are used for DBI inputs if DBI is enabled. If DBI is disabled then the input of the upper 8 bits [D(143:136) and D(71:64)] is '1'.

A x4 device has a CRC tree with 32 input bits. The input for the upper 40 bits D[71:32] are '1's.

DRAM can write data to the DRAM core without waiting for CRC check for full writes. If bad data is written to the DRAM core then controller will retry the transaction and overwrite the bad data. Controller is responsible for data coherency.

4.16.6 RC Error Handling

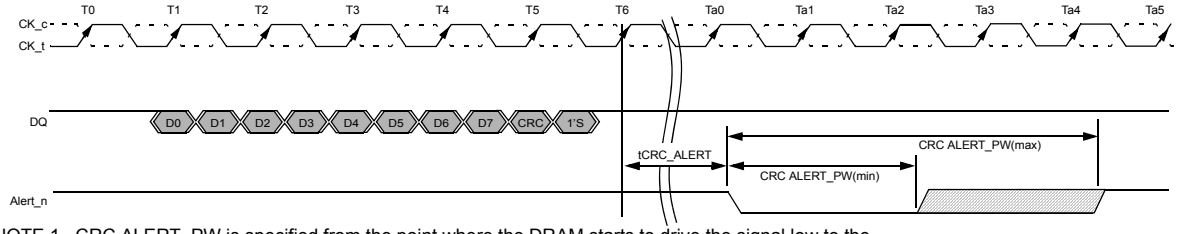
CRC Error mechanism shares the same Alert_n signal for reporting errors on writes to DRAM. The controller has no way to distinguish between CRC errors and Command/Address/Parity errors other than to read the DRAM mode registers. This is a very time consuming process in a multi-rank configuration.

To speed up recovery for CRC errors, CRC errors are only sent back as a pulse. The minimum pulse-width is 2 clocks. The latency to Alert_n signal is defined as tCRC_ALERT in the figure below.

DRAM will set CRC Error Clear bit in A4 of MR5 to '1' and CRC Error Status bit in MPR3 of page1 to '1' upon detecting a CRC error. The CRC Error Clear bit remains set at '1' until the host clears it explicitly using an MRS command.

The controller upon seeing an error as a pulse width will retry the write transactions. The controller understands the worst case delay for Alert_n (during init) and can backup the transactions accordingly or the controller can be made more intelligent and try to correlate the write CRC error to a specific rank or a transaction. The controller is also responsible for opening any pages and ensuring that retrying of writes is done in a coherent fashion.

The pulse width may be seen longer than two clocks at the controller if there are multiple CRC errors as the Alert_n is a daisy chain bus.



NOTE 1 CRC ALERT_PW is specified from the point where the DRAM starts to drive the signal low to the point where the DRAM driver releases and the controller starts to pull the signal up.
NOTE 2 Timing diagram applies to x4, x8, and x16 devices.

TIME BREAK
TRANSITIONING DATA

Figure 41 — CRC Error Reporting

Table 41 — CRC Error Timing Parmeters

		DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		Unit
Parameter	Symbol	min	max	min	max	min	max	min	max	
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	-	13	ns
CRC ALERT_n pulse width	CRC ALERT_PW	6	10	6	10	6	10	6	10	nCK

4.16.7 CRC Frame format with BC4

DDR4 SDRAM supports CRC function for Write operation for Burst Chop 4 (BC4). The CRC function is programmable using DRAM mode register and can be enabled for writes.

When CRC is enabled the data frame length is fixed at 10UI for both BL8 and BC4 operations. DDR4 SDRAM also supports burst length on the fly with CRC enabled. This is enabled using mode register.

CRC data bit mapping for x4 devices (BC4)
The following figure shows detailed bit mapping for a x4 device.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	CRC4
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	CRC5
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	CRC6
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	CRC7

For a x4 SDRAM, the CRC tree input is 16 data bits as shown in the figure above. The input for the remaining bits are “1”.

CRC data bit mapping for x8 devices (BC4)
The following figure shows detailed bit mapping for a x8 device.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DM_n DBI_n	d64	d65	d66	d67	1	1	1	1	1	1

For a x8 SDRAM, the CRC tree inputs are 36 bits as shown in the figure above. The input bits d(64:67) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(64:67) are “1”

CRC data bit mapping for x16 devices (BC4)
The following figure shows detailed bit mapping for a x16 device.

	Tranfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DML_n DBIL_n	d64	d65	d66	d67	1	1	1	1	1	1
DQ8	d72	d73	d74	d75	1	1	1	1	CRC8	1
DQ9	d80	d81	d82	d83	1	1	1	1	CRC9	1
DQ10	d88	d89	d90	d91	1	1	1	1	CRC10	1
DQ11	d96	d97	d98	d99	1	1	1	1	CRC11	1
DQ12	d104	d105	d106	d107	1	1	1	1	CRC12	1
DQ13	d112	d113	d114	d115	1	1	1	1	CRC13	1
DQ14	d120	d121	d122	d123	1	1	1	1	CRC14	1
DQ15	d128	d129	d130	d131	1	1	1	1	CRC15	1
DMU_n DBIU_n	d136	d137	d138	d139	1	1	1	1	1	1

For a x16 SDRAM there are two identical CRC trees.
The lower CRC tree inputs has 36 bits as shown in the figure above. The input bits d(64:67) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(64:67) are “1”.
The upper CRC tree inputs has 36 bits as shown in the figure above. The input bits d(136:139) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(136:139) are “1”.

DBI and CRC clarification
Write operation: The SDRAM computes the CRC for received data d(71:0). Data is not inverted based on DBI before it is used for computing CRC. The data is inverted based on DBI before it is written to the DRAM core.

Burst Ordering with BC4 and CRC enabled
If CRC is enabled then address bit A2 is used to transfer critical data first for BC4 writes.
A x8 SDRAM is used as an example with DBI enabled.

The following figure shows data frame with A2=0.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d0	d1	d2	d3	1	1	1	1	CRC0	1
DQ1	d8	d9	d10	d11	1	1	1	1	CRC1	1
DQ2	d16	d17	d18	d19	1	1	1	1	CRC2	1
DQ3	d24	d25	d26	d27	1	1	1	1	CRC3	1
DQ4	d32	d33	d34	d35	1	1	1	1	CRC4	1
DQ5	d40	d41	d42	d43	1	1	1	1	CRC5	1
DQ6	d48	d49	d50	d51	1	1	1	1	CRC6	1
DQ7	d56	d57	d58	d59	1	1	1	1	CRC7	1
DM_n DBI_n	d64	d65	d66	d67	1	1	1	1	1	1

The following figure shows data frame with A2=1.

	Transfer									
	0	1	2	3	4	5	6	7	8	9
DQ0	d4	d5	d6	d7	1	1	1	1	CRC0	1
DQ1	d12	d13	d14	d15	1	1	1	1	CRC1	1
DQ2	d20	d21	d22	d23	1	1	1	1	CRC2	1
DQ3	d28	d29	d30	d31	1	1	1	1	CRC3	1
DQ4	d36	d37	d38	d39	1	1	1	1	CRC4	1
DQ5	d44	d45	d46	d47	1	1	1	1	CRC5	1
DQ6	d52	d53	d54	d55	1	1	1	1	CRC6	1
DQ7	d60	d61	d62	d63	1	1	1	1	CRC7	1
DM_n DBI_n	d68	d69	d70	d71	1	1	1	1	1	1

If A2=1 then the data input to the CRC tree are 36 bits as shown above. Data bits d(4:7) are used as inputs for d(0:3), d(12:15) are used as inputs to d(8:11) and so forth for the CRC tree.

The input bits d(68:71) are used if DBI or DM functions are enabled. If DBI and DM are disabled then d(68:71) are “1”s. If A2=1 then data bits d(68:71) are used as inputs for d(64:67)

The CRC tree will treat the 36 bits in transfer’s four through seven as 1’s

CRC equations for x8 device in BC4 mode with A2=0 are as follows:

CRC[0] = D[69]=1 ^ D[68]=1 ^ D[67] ^ D[66] ^ D[64] ^ D[63]=1 ^ D[60]=1 ^ D[56] ^ D[54]=1 ^ D[53]=1 ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[45]=1 ^ D[43] ^ D[40] ^ D[39]=1 ^ D[35] ^ D[34] ^ D[31]=1^ D[30]=1 ^ D[28]=1 ^ D[23]=1 ^ D[21]=1 ^ D[19] ^ D[18] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[8] ^ D[7]=1 ^ D[6] =1 ^ D[0] ;

CRC[1] = D[70]=1 ^ D[66] ^ D[65] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^D[56] ^ D[55]=1 ^ D[52]=1 ^ D[51] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[34] ^ D[32] ^ D[30]=1 ^ D[29]=1 ^ D[28]=1 ^ D[24] ^ D[23]=1 ^ D[22]=1 ^ D[21]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[16] ^ D[15]=1 ^ D[14]=1 ^ D[13]=1 ^ D[12]=1 ^ D[9] ^ D[6]=1 ^ D[1] ^ D[0];

CRC[2] = D[71]=1 ^ D[69]=1 ^ D[68]=1 ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[60]=1 ^ D[58] ^ D[57] ^ D[54]=1 ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[44]=1 ^ D[43] ^ D[42] ^ D[39]=1 ^ D[37]=1 ^ D[34] ^ D[33] ^
D[29]=1 ^ D[28]=1 ^ D[25] ^ D[24] ^ D[22]=1 ^ D[17] ^ D[15]=1 ^ D[13]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[6]=1 ^ D[2] ^ D[1] ^ D[0];

CRC[3] = D[70]=1 ^ D[69]=1 ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[61]=1 ^ D[59] ^ D[58] ^ D[55]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[45]=1 ^ D[44]=1 ^ D[43] ^ D[40] ^ D[38]=1 ^ D[35] ^ D[34] ^ D[30]=1 ^ D[29]=1 ^ D[26] ^ D[25] ^ D[23]=1 ^ D[18] ^ D[16] ^ D[14]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[7]=1 ^ D[3] ^ D[2] ^ D[1];

CRC[4] = D[71]=1 ^ D[70]=1 ^ D[65] ^ D[64] ^ D[63]=1 ^ D[62]=1 ^ D[60]=1 ^ D[59] ^ D[56] ^ D[52]=1 ^ D[50] ^ D[49] ^ D[48] ^ D[46]=1 ^ D[45]=1 ^ D[44]=1 ^ D[41] ^ D[39]=1 ^ D[36]=1 ^ D[35] ^ D[31]=1 ^
D[30]=1 ^ D[27] ^ D[26] ^ D[24] ^ D[19] ^ D[17] ^ D[15]=1 ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[8] ^ D[4]=1 ^ D[3] ^ D[2];

CRC[5] = D[71]=1 ^ D[66] ^ D[65] ^ D[64] ^ D[63]=1 ^ D[61]=1 ^ D[60]=1 ^ D[57] ^ D[53]=1 ^ D[51] ^ D[50] ^ D[49] ^ D[47]=1 ^ D[46]=1 ^ D[45]=1 ^ D[42] ^ D[40] ^ D[37]=1 ^ D[36]=1 ^ D[32] ^ D[31]=1 ^ D[28]=1 ^ D[27] ^ D[25] ^ D[20]=1 ^ D[18] ^ D[16] ^ D[15]=1 ^ D[13]=1 ^ D[11] ^ D[9] ^ D[5]=1 ^ D[4]=1 ^ D[3];

CRC[6] = D[67] ^ D[66] ^ D[65] ^ D[64] ^ D[62]=1 ^ D[61]=1 ^ D[58] ^ D[54]=1 ^ D[52]=1 ^ D[51] ^ D[50] ^ D[48] ^ D[47]=1 ^ D[46]=1 ^ D[43] ^ D[41] ^ D[38]=1 ^ D[37]=1 ^ D[33] ^ D[32] ^ D[29]=1 ^ D[28]=1 ^ D[26] ^ D[21]=1 ^ D[19] ^ D[17] ^ D[16] ^ D[14]=1 ^ D[12]=1 ^ D[10] ^ D[6]=1 ^ D[5]=1 ^ D[4]=1;

CRC[7] = D[68]=1 ^ D[67] ^ D[66] ^ D[65] ^ D[63]=1 ^ D[62]=1 ^ D[59] ^ D[55]=1 ^ D[53]=1 ^ D[52]=1 ^ D[51] ^ D[49] ^ D[48] ^ D[47]=1 ^ D[44]=1 ^ D[42] ^ D[39]=1 ^ D[38]=1 ^ D[34] ^ D[33] ^ D[30]=1 ^ D[29]=1 ^ D[27] ^ D[22]=1 ^ D[20]=1 ^ D[18] ^ D[17] ^ D[15] =1^ D[13]=1 ^ D[11] ^ D[7]=1 ^ D[6]=1 ^ D[5]=1;

CRC equations for x8 device in BC4 mode with A2=1 are as follows:

CRC[0] = 1 ^ 1 ^ D[71] ^ D[70] ^ D[68] ^ 1 ^ 1 ^ D[60] ^ 1 ^ 1 ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1^ 1 ^ 1 ^ 1 ^ 1 ^ D[23] ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[12] ^ 1 ^ 1 ^ D[4] ;

CRC[1] = 1 ^ D[70] ^ D[69] ^ 1 ^ 1 ^ 1 ^ D[61] ^ D[60] ^ 1 ^ 1 ^ D[55] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[38] ^ D[36] ^ 1 ^ 1 ^ 1 ^ D[28] ^ 1 ^ 1 ^ 1 ^ 1 ^ D[22] ^ D[21] ^ D[20] ^1 ^ 1 ^1 ^ 1 ^ D[13] ^ 1 ^ D[5] ^ D[4];

CRC[2] = 1 ^ 1 ^ 1 ^1 ^1 ^ 1 ^ 1 ^ D[62] ^ D[61] ^ 1 ^ D[54] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[29] ^ D[28] ^ 1 ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D12] ^1 ^ D[6] ^ D[5] ^ D[4];

CRC[3] = 1 ^ 1 ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[62] ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ 1 ^ D[47] ^ D[44] ^ 1 ^ D[39] ^ D[38] ^ 1 ^ 1 ^ D[30] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ D[7] ^ D[6] ^ D[5];

CRC[4] = 1 ^1 ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[63] ^ D[60] ^ 1 ^ D[54] ^ D[53] ^ D[52] ^ 1 ^1 ^ 1 ^ D[45] ^ 1 ^ 1 ^ D[39] ^1 ^ 1 ^ D[31] ^ D[30] ^ D[28] ^ D[23] ^ D[21] ^ 1 ^ 1 ^ 1 ^ D[14] ^ D[12] ^ 1 ^ D[7] ^ D[6];

CRC[5] = 1 ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ 1 ^ D[61] ^ 1 ^ D[55] ^ D[54] ^ D[53] ^ 1 ^ 1 ^ 1 ^ D[46] ^ D[44] ^ 1 ^ 1 ^ D[36] ^ 1 ^ 1 ^ D[31] ^ D[29] ^ 1 ^ D[22] ^ D[20] ^ 1 ^ 1 ^ D[15] ^ D[13] ^ 1 ^ 1 ^ D[7];

CRC[6] = D[71] ^ D[70] ^ D[69] ^ D[68] ^ 1 ^ 1 ^ D[62] ^ 1 ^ 1 ^ D[55] ^ D[54] ^ D[52] ^ 1 ^1 ^ D[47] ^ D[45] ^ 1 ^ 1 ^ D[37] ^ D[36] ^1 ^ 1 ^ D[30] ^ 1 ^ D[23] ^ D[21] ^ D[20] ^ 1 ^ 1 ^ D[14] ^ 1 ^ 1 ^ 1;

CRC[7] = 1 ^ D[71] ^ D[70] ^ D[69] ^ 1 ^ 1 ^ D[63] ^ 1 ^ 1 ^ 1 ^ D[55] ^ D[53] ^ D[52] ^ 1 ^ 1 ^ D[46] ^ 1 ^ 1 ^ D[38] ^ D[37] ^ 1 ^ 1 ^ D[31] ^ 1 ^ 1 ^ D[22] ^ D[21] ^ 1^ 1 ^ D[15] ^ 1 ^ 1 ^ 1;

4.16.8 Simultaneous DM and CRC Functionality

When both DM and Write CRC are enabled in the DRAM mode register, the DRAM calculates CRC before sending the write data into the array. If there is a CRC error, the DRAM blocks the write operation and discards the data.

4.17 Command Address Parity(CA Parity)

[A2:A0] of MR5 are defined to enable or disable C/A Parity in the DRAM. The default state of the C/A Parity bits is disabled. If C/A parity is enabled by programming a non-zero value to C/A Parity Latency in the mode register (the Parity Error bit must be set to zero when enabling C/A any Parity mode), then the DRAM has to ensure that there is no parity error before executing the command. The additional delay for executing the commands versus a parity disabled mode is programmed in the mode register when C/A Parity is enabled (Parity Latency) and is applied to all commands.When C/A Parity is enabled, only DES is allowed between valid commands to prevent DRAM from any malfunctioning. CA Parity Mode is supported when DLL-on Mode is enabled, use of CA Parity Mode when DLL-off Mode is enabled is not allowed.

C/A Parity signal (PAR) covers ACT_n, RAS_n, CAS_n, WE_n and the address bus including bank address and bank group bits. The control signals CKE, ODT and CS_n are not included. (e.g. for a 4 Gbit x4 monolithic device, parity is computed across BG0, BG1, BA1, BA0, A16/ RAS_n, A15/CAS_n, A14/WE_n, A13-A0 and ACT_n). (DRAM should internally treat any unused address pins as 0's, e.g., if a common die has stacked pins but the device is used in a monolithic application then the address pins used for stacking should internally be treated as 0's)

The convention of parity is even parity i.e. valid parity is defined as an even number of ones across the inputs used for parity computation combined with the parity signal. In other words the parity bit is chosen so that the total number of 1's in the transmitted signal, including the parity bit is even.

If a DRAM detects a C/A parity error in any command as qualified by CS_n then it must perform the following steps:

- Ignore the erroneous command. Commands in max NnCK window (tPAR_UNKNOWN) prior to the erroneous command are not guaranteed to be executed. When a READ command in this NnCK window is not executed, the DRAM does not activate DQS outputs.
- Log the error by storing the erroneous command and address bits in the error log. (MPR page1)
- Set the Parity Error Status bit in the mode register to '1'. The Parity Error Status bit must be set before the ALERT_n signal is released by the DRAM (i.e. tPAR_ALERT_ON + tPAR_ALERT_PW(min)).
- Assert the ALERT_n signal to the host (ALERT_n is active low) within tPAR_ALERT_ON time.
- Wait for all in-progress commands to complete. These commands were received tPAR_UNKOWN before the erroneous command. If a parity error occurs on a command issued between the tXS_Fast and tXS window after self-refresh exit then the DRAM may delay the de-assertion of ALERT_n signal as a result of any internal on going refresh. (See Figure 46)
- Wait for tRAS_min before closing all the open pages. The DRAM is not executing any commands during the window defined by (tPAR_ALERT_ON + tPAR_ALERT_PW).
- After tPAR_ALERT_PW_min has been satisfied, the DRAM may de-assert ALERT_n.
- After the DRAM has returned to a known pre-charged state it may de-assert ALERT_n.
- After (tPAR_ALERT_ON + tPAR_ALERT_PW), the DRAM is ready to accept commands for normal operation. Parity latency will be in effect, however, parity checking will not resume until the memory controller has cleared the Parity Error Status bit by writing a '0'(the DRAM will execute any erroneous commands until the bit is cleared).
- It is possible that the DRAM might have ignored a refresh command during the (tPAR_ALERT_ON + tPAR_ALERT_PW) window or the refresh command is the first erroneous frame so it is recommended that the controller issues extra refresh cycles as needed.
- The Parity Error Status bit may be read anytime after (tPAR_ALERT_ON + tPAR_ALERT_PW) to determine which DRAM had the error. The DRAM maintains the Error Log for the first erroneous command until the Parity Error Status bit is reset to '0'.

Mode Register for C/A Parity Error is defined as follows. C/A Parity Latency bits are write only, Parity Error Status bit is read/write and error logs are read only bits. The controller can only program the Parity Error Status bit to '0'. If the controller illegally attempts to write a '1' to the Parity Error Status bit the DRAM does not guarantee that parity will be checked. The DRAM may opt to block the controller from writing a '1' to the Parity Error Status bit.

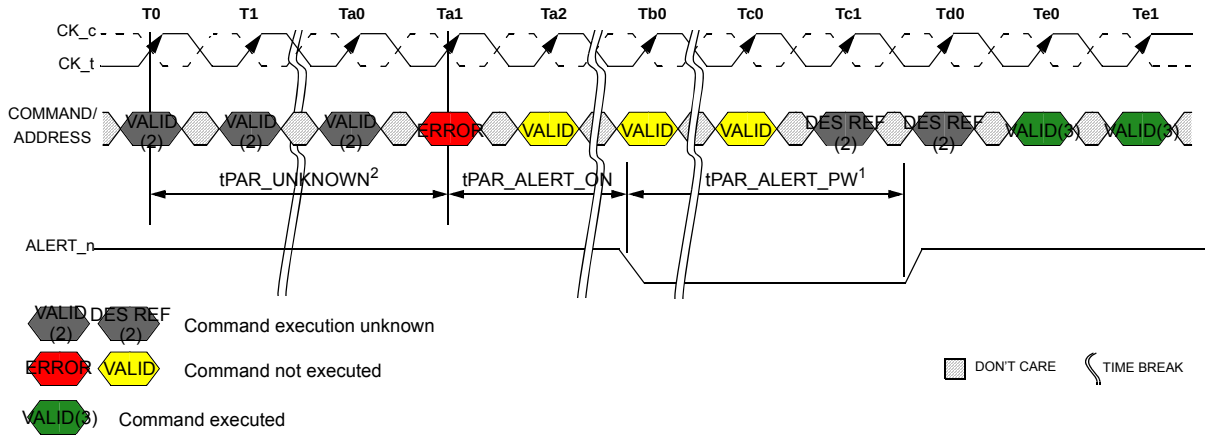
Table 42 — Mode Registers for C/A Parity

C/A Parity Latency MR5[2:0]*	Speed bins	C/A Parity Error Status MR5[4]	Errant C/A Frame
000 = Disabled	-	0=clear	C2-C0, ACT_n, BG1, BG0, BA0, BA1, PAR, A17, A16/RAS_n, A15/CAS_n, A14/WE_n, A13:A0
001= 4 Clocks	1600,1866,2133		
010= 5 Clocks	2400	1=Error	
011= 6 Clocks	RFU		
100= 8 Clocks	RFU		

NOTE1 Parity Latency is applied to all commands.
NOTE 2 Parity Latency can be changed only from a C/A Parity disabled state, i.e. a direct change from PL=3 → PL=4 is not allowed. Correct sequence is PL=3 → Disabled → PL=4
NOTE 3 Parity Latency is applied to write and read latency. Write Latency = AL+CWL+PL. Read Latency = AL+CL+PL.

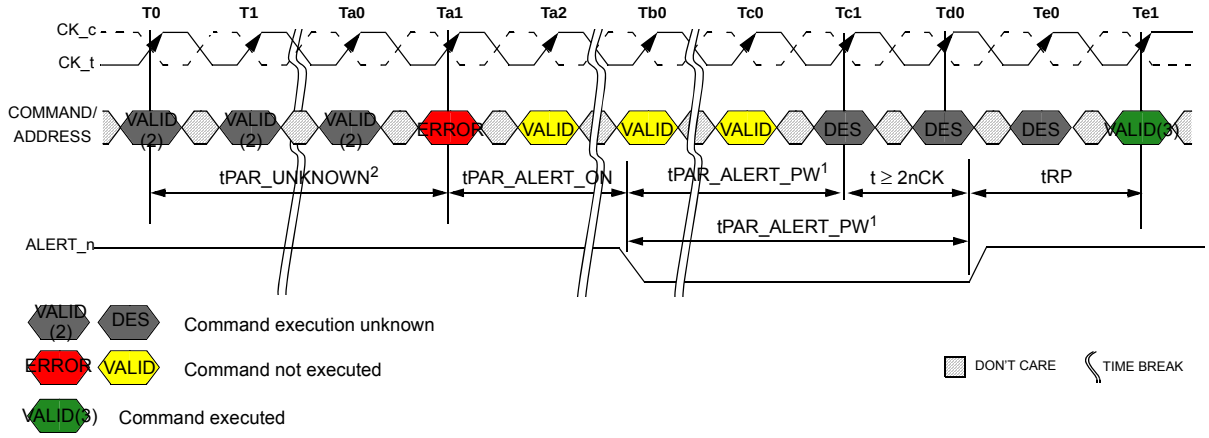
DDR4 SDRAM supports MR bit for 'Persistent Parity Error Mode'. This mode is enabled by setting MR5 A9=High and when it is enabled, DRAM resumes checking CA Parity after the alert_n is deasserted, even if Parity Error Status bit is set as High. If multiple errors occur before the Error Status bit is cleared the Error log in MPR page 1 should be treated as 'Don't Care'. In 'Persistent Parity Error Mode' the Alert_n pulse will be asserted and deasserted by the DRAM as defined with the min. and max. value for tPAR_ALERT_PW. The controller must issue DESELECT com-mands once it detects the Alert_n signal, this response time is defined as tPAR_ALERT_RSP

The following figure captures the flow of events on the C/A bus and the ALERT_n signal.



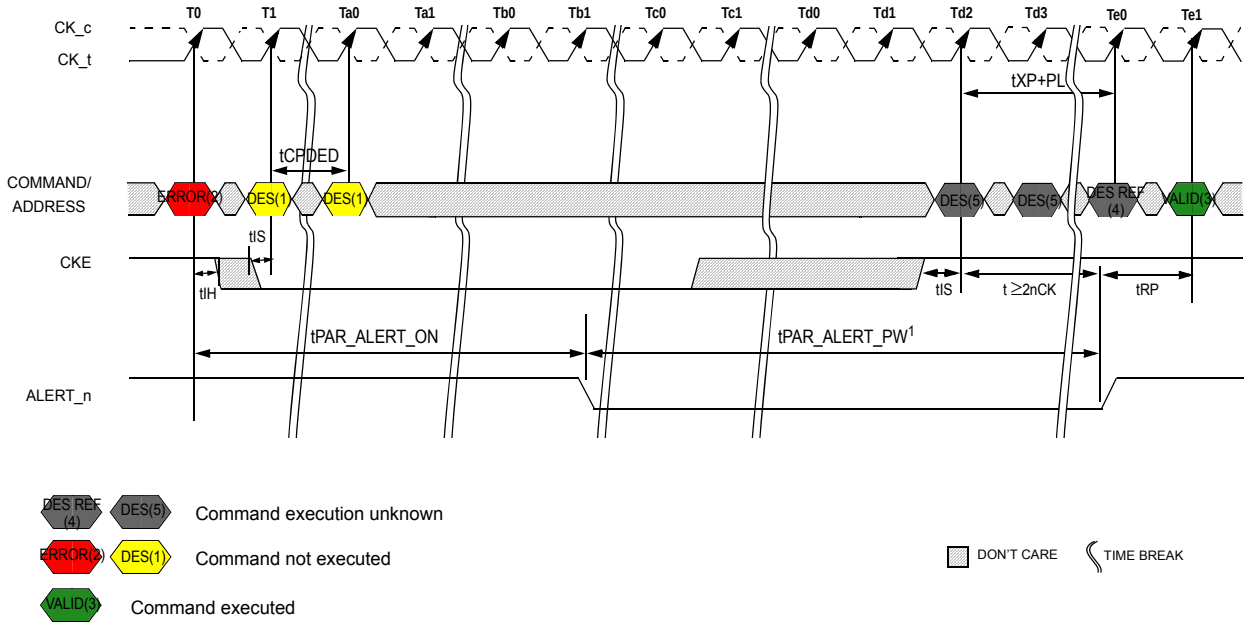
NOTE 1 DRAM is emptying queues, Precharge All and parity checking off until Parity Error Status bit cleared.
NOTE 2 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 3 Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.

Figure 42 — Normal CA Parity Error Checking Operation



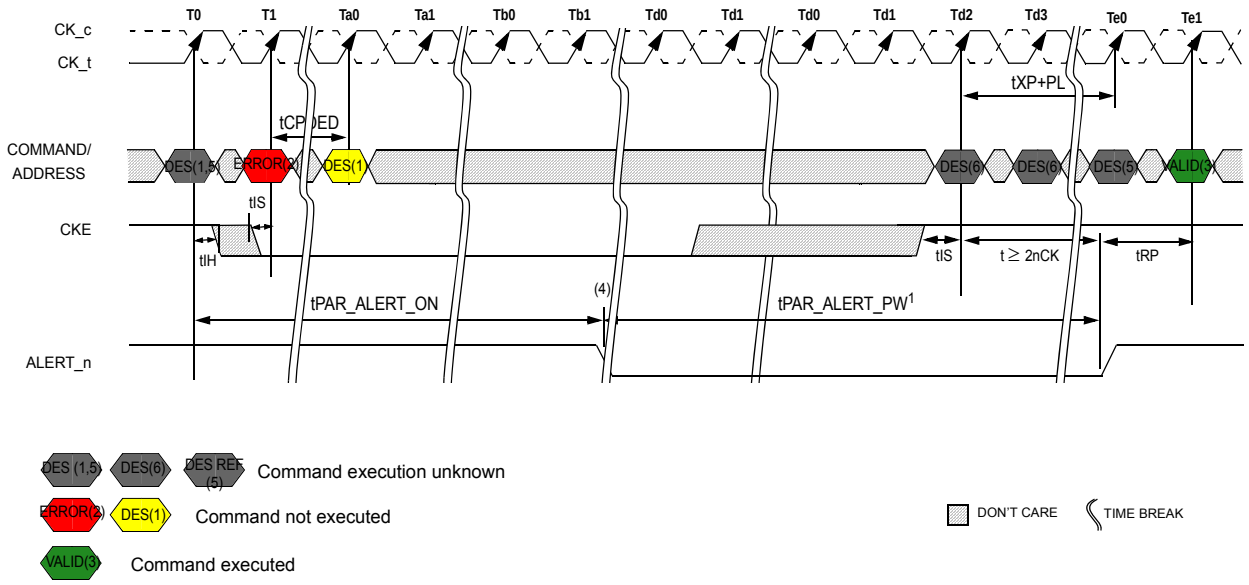
NOTE 1 DRAM is emptying queues, Precharge All and parity check re-enable finished by tPAR_ALERT_PW.
NOTE 2 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 3 Normal operation with parity latency and parity checking (CA Parity Persistent Error Mode enabled).

Figure 43 — Persistent CA Parity Error Checking Operation



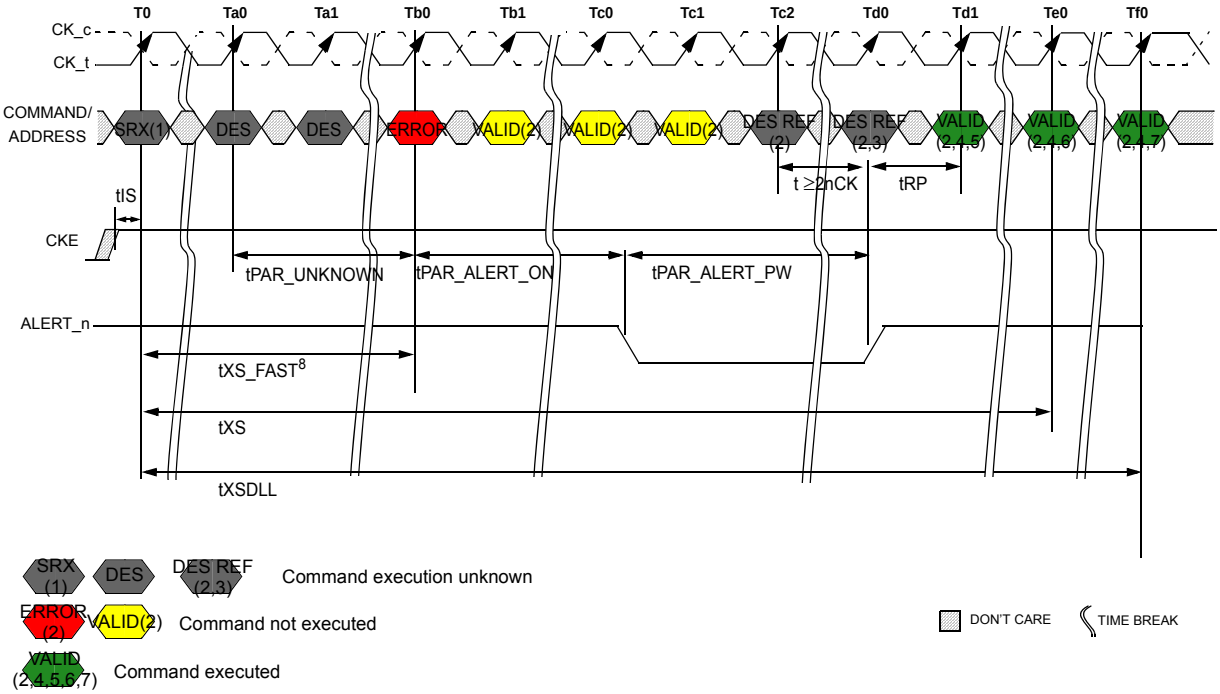
NOTE 1 Deselect command only only allowed.
NOTE 2 Error could be Precharge or Activate.
NOTE 3 Normal operation with parity latency(CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.
NOTE 4 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 5 Deselect command only allowed CKE may go high prior to Td2 as long as DES commands are issued.

Figure 44 — CA Parity Error Checking - PDE/PDX



NOTE 1 Deselect command only only allowed.
NOTE 2 SelfRefresh command error. DRAM masks the intended SRE cammand enters Precharge Down.
NOTE 3 Normal operation with parity latency(CA Parity Persistent Error Mode disable). Parity checking is off until Parity Error Status bit cleared.
NOTE 4 Controller can not disable dock until it has been able to have detected a possible C/A Parity error.
NOTE 5 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 6 Deselect command only allowed CKE may go high prior to Tc2 as long as DES commands are issued.

Figure 45 — CA Parity Error Checking - SRE Attempt



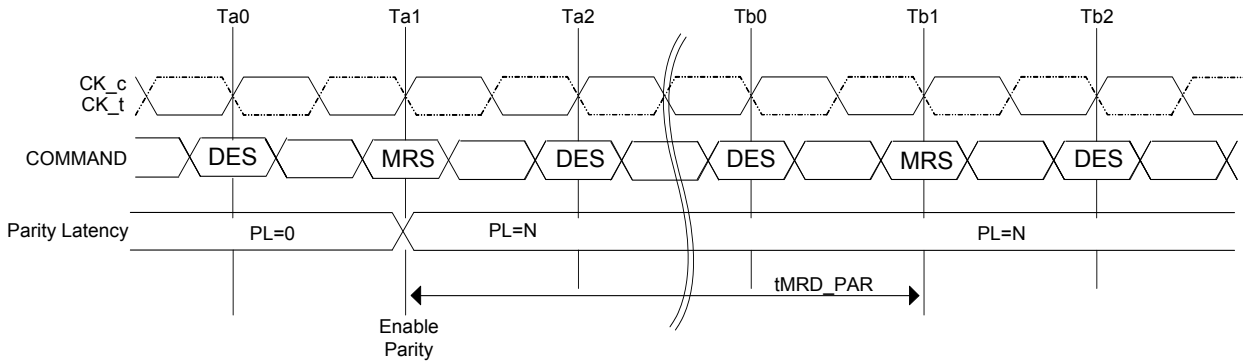
NOTE 1 SelfRefresh Abort = Disable : MR4 [A9=0]
NOTE 2 Input commands are bounded by tXSDLL, tXS, tXS_ABORT and tXS_FAST timing.
NOTE 3 Command execution is unknown the corresponding DRAM internal state change may or may not occur. The DRAM Controller should consider both cases and make sure that the command sequence meets the specifications.
NOTE 4 Normal operation with parity latency(CA Parity Persistent Error Mode disabled). Parity checking off until Parity Error Status bit cleared.
NOTE 5 Only MRS (limited to those described in the Self-Refresh Operation section), ZQCS or ZQCL command allowed.
NOTE 6 Valid commands not requiring a locked DLL
NOTE 7 Valid commands requiring a locked DLL
NOTE 8 This figure shows the case from which the error occurred after tXS FAST_An error also occur after tXS_ABORT and tXS.

Figure 46 — CA Parity Error Checking - SRX

Command/Address parity entry and exit timings

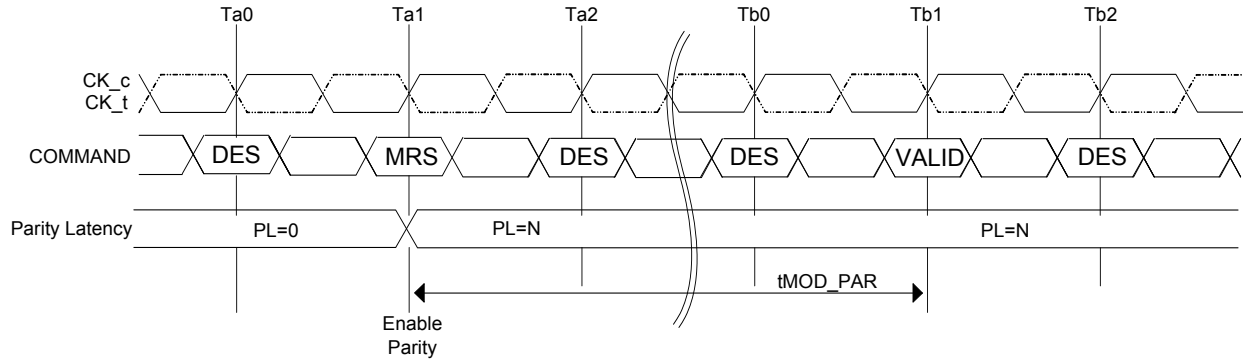
When entering and exiting Parity mode, users must wait tMRD_PAR before issuing another MRS command, and wait tMOD_PAR before any other commands.

tMOD_PAR = tMOD + PL
tMRD_PAR = tMOD + PL
For CA parity entry, PL in the equations above is the parity latency programmed with the MRS command entering CA parity mode.
For CA parity exit, PL in the equations above is the programmed parity latency prior to the MRS command exiting CA parity mode.



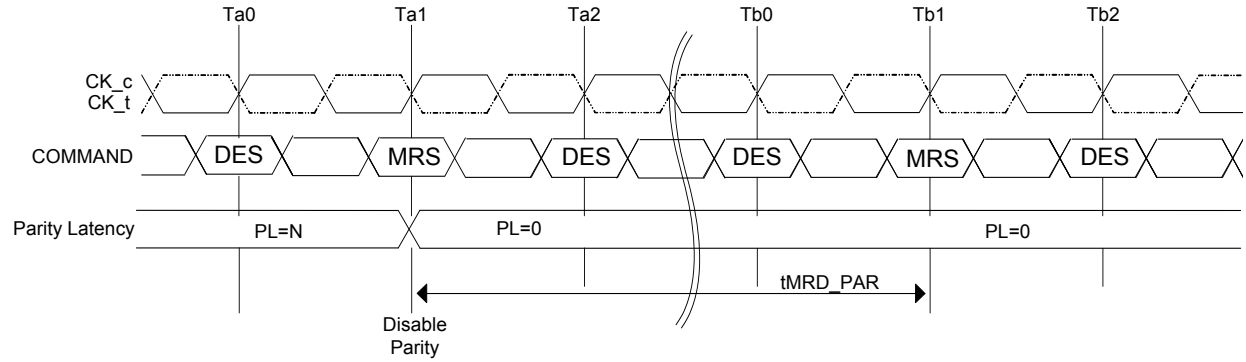
NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 47 — Parity entry timing example - tMRD_PAR



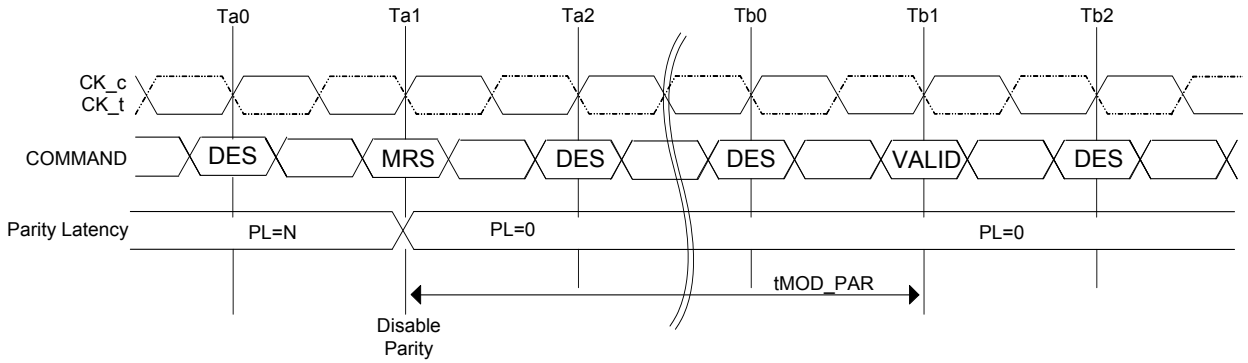
NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 48 — Parity entry timing example - tMOD_PAR



NOTE 1 tMRD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 49 — Parity exit timing example - tMRD_PAR



NOTE 1 tMOD_PAR = tMOD + N; where N is the programmed parity latency.

Figure 50 — Parity exit timing example - tMOD_PAR

4.17.1 CA Parity Error Log Readout

MPR Mapping of CA Parity Error Log[1](Page1)

Address	MPR Location	[7]	[6]	[5]	[4]	[3]	[2]	[1]	[0]
BA1:BA0 = 0:1	00=MPR0	A7	A6	A5	A4	A3	A2	A1	A0
	01=MPR1	CAS_n/ A15	WE_n/A14	A13	A12	A11	A10	A9	A8
	10=MPR2	PAR	ACT_n	BG1	BG0	BA1	BA0	A17	RAS_n/ A16
	11=MPR3	CRC Error Status	CA Parity Error Status	CA Parity Latency			C2	C1	C0

NOTE 1 MPR used for CA parity error log readout is enabled by setting A[2] in MR3
NOTE 2 For higher density of DRAM, where A[17] is not used, MPR2[1] should be treated as don't care.
NOTE 3 If a device is used in monolithic application, where C[2:0] are not used, then MPR3[2:0] should be treated as don't care.

4.18 Control Gear Down Mode

The following ballot represents the sequence for the gear down mode. The DRAM defaults in 1/2 rate(1N) clock mode and utilizes a low frequency MRS command followed by a sync pulse to align the proper clock edge for operating the control lines CS_n, CKE and ODT in 1/4rate(2N) mode. For operation in 1/2 rate mode no MRS command for geardown or sync pulse is required. DRAM defaults in 1/2 rate mode.

General sequence for operation in geardown during initialization
- DRAM defaults to a 1/2 rate(1N mode) internal clock at power up/reset
- Assertion of reset
- Assertion of CKE enables the rank
- MRS is accessed with a low frequency N*tck MRS geardown CMD
  Ntck static MRS command qualified by 1N CS_n
- MC sends 1N sync pulse with a low frequency N*tck NOP CMD
  CK tSYCN_GEAR is an even number of clocks
  Sync pulse on even edge from MRS CMD
- Normal operation in 2N starts tCMD_GEAR clocks later

For the operation of geardown mode in 1/4 rate, the following MR settings should be applied.

CAS Latency (MR0 A[6:4,2]) : Even numbers

Write Recovery and Read to Precharge (MR0 A[11:9]) : Even numbers

Additive Latency (MR1 A[4:3]) : 0, CL -2

CAS Write Latency (MR2 A[5:3]) : Even numbers

CS to Command/Address Latency Mode (MR4 A[8:6]) : Even numbers

CA Parity Latency Mode (MR5 A[2:0]) : Even numbers

The diagram below illustrates the sequence for control operation in 2N mode during power up.

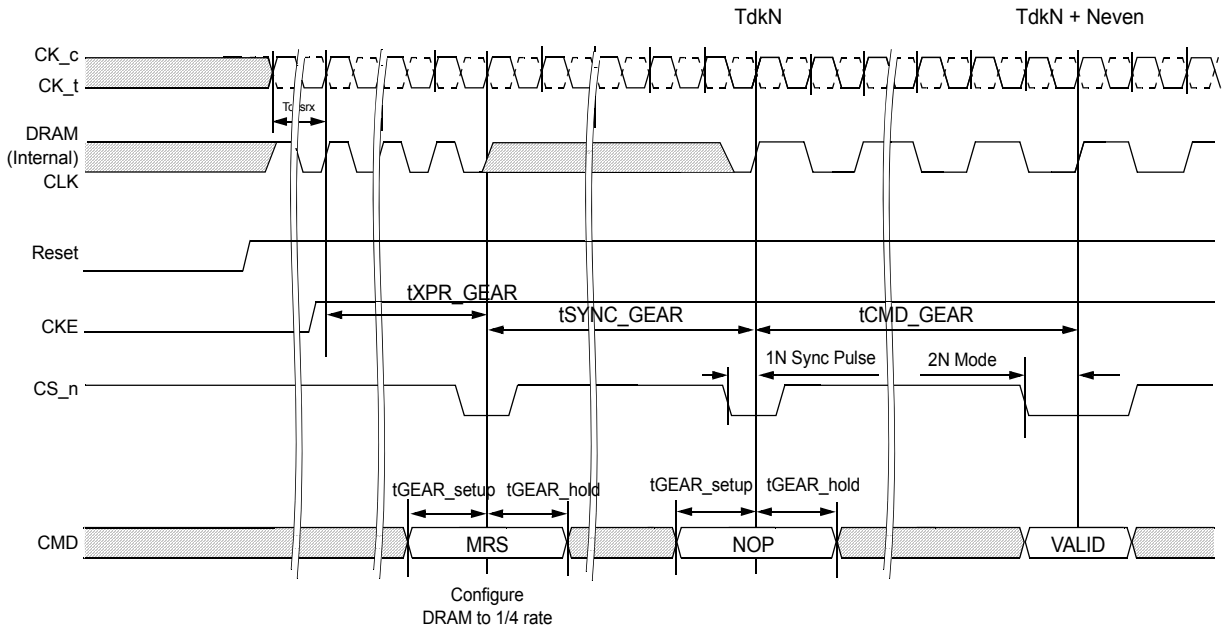


Figure 51 — Gear down (2N) mode entry sequence during initialization

The diagram below represents the operation of geardown(1/2 rate to 1/4 rate)mode during normal operation with CKE and Reset set high.

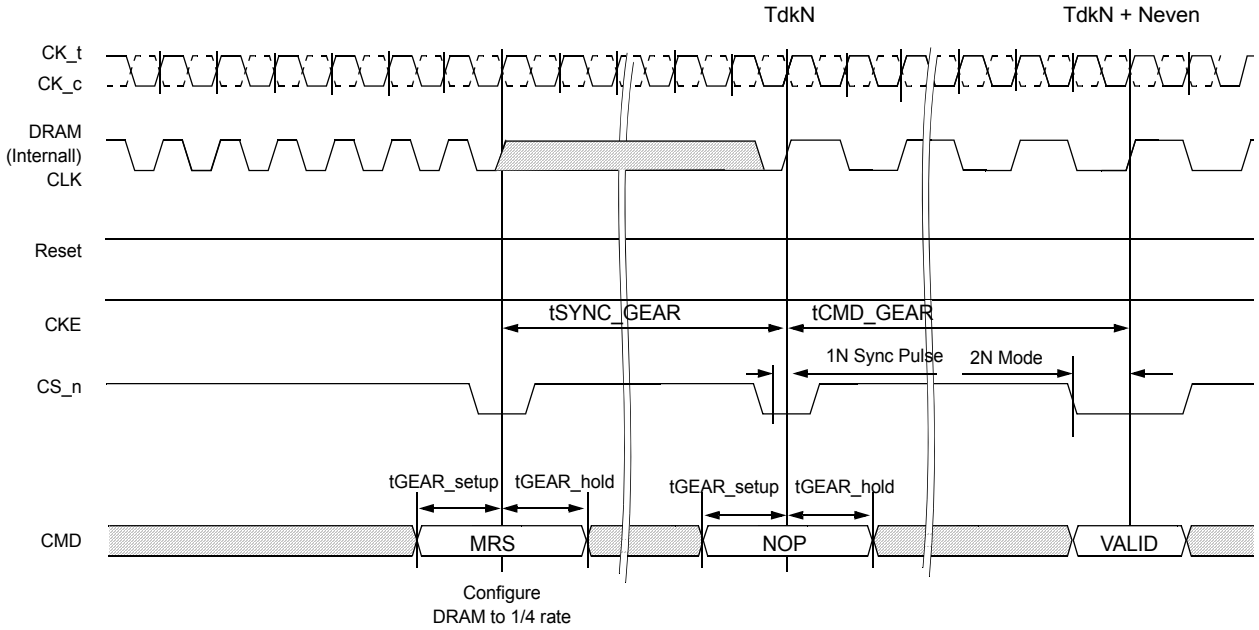
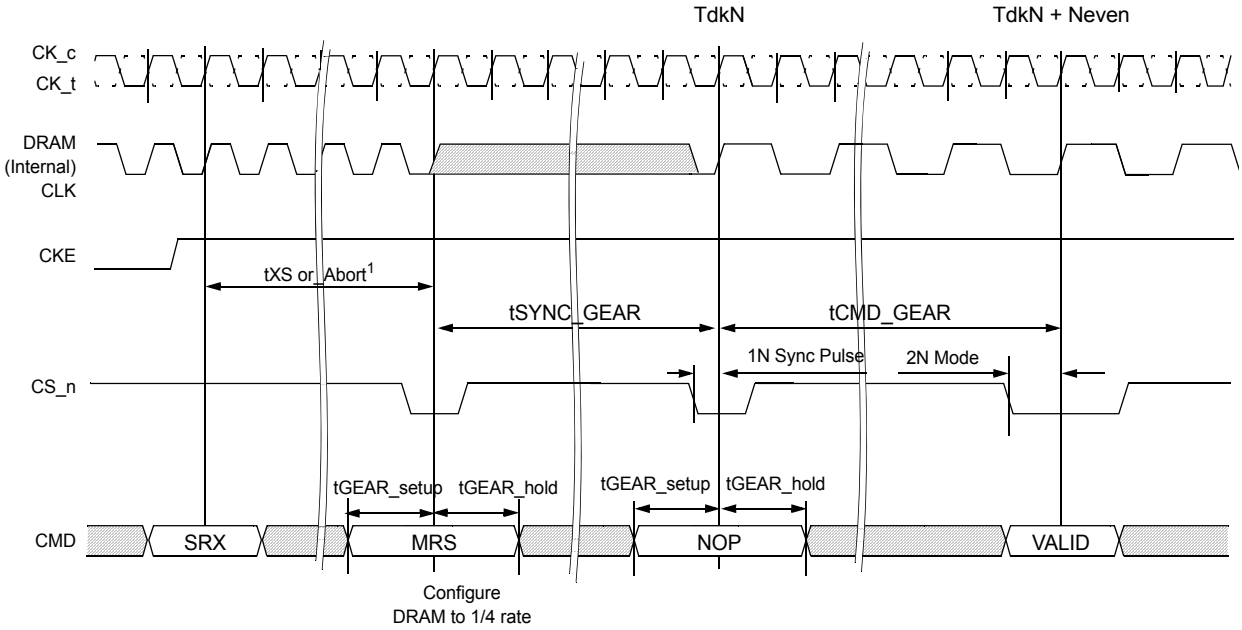


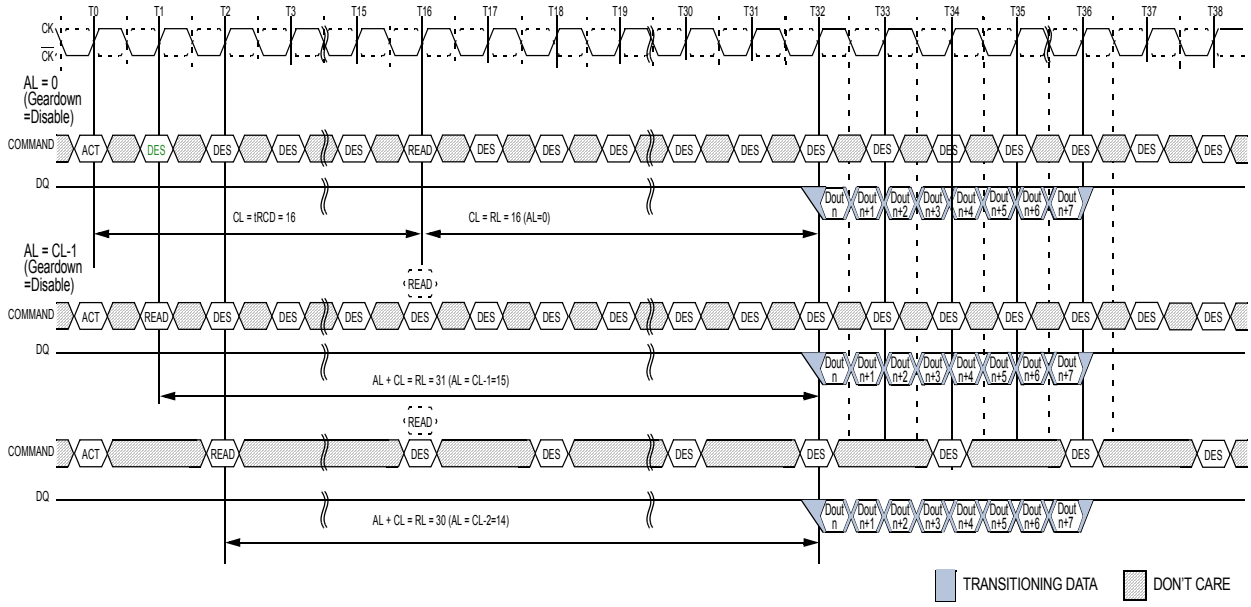
Figure 52 — Gear down (2N) mode entry sequence during normal operation

If operation is 1/2 rate(1N) mode before and after self refresh, no MRS command or sync pulse is required during self refresh exit. The min exit delay is tXS, or tXS_Abort to the first valid command.
If operation is in 1/4 rate mode after self refresh exit, the DRAM requires a MRS command and sync pulse as illustrated in the figure below.
DRAM must internally reset to 1N mode from 2N mode during self Refresh and Max Power Saving Mode to properly align internal clock edge with the sync pulse.Illustration below for the DRAM operating in 1/4 rate mode before and after self refresh entry and exit.



NOTE 1 CKE High Assert to Gear Down Enable Time (tXS, tXS_Abort) depend on MR setting. A correspondence of tXS/tXS_Abort and MR Setting is as follows.
- MR4[A9] = 0 : tXS
- MR4[A9] = 1 : tXS_Abort

Figure 53 — Gear down (2N) mode entry sequence after self refresh exit (SRX)

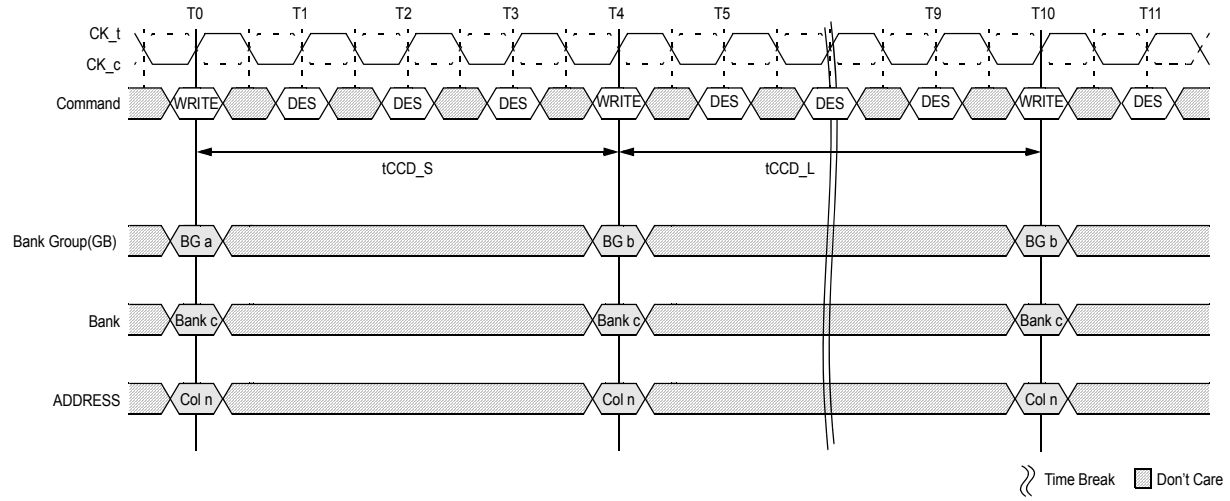


NOTE 1 BL=8, tRCD=CL=16
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 54 — Comparison Timing Diagram Between Geardown Disable and Enable.

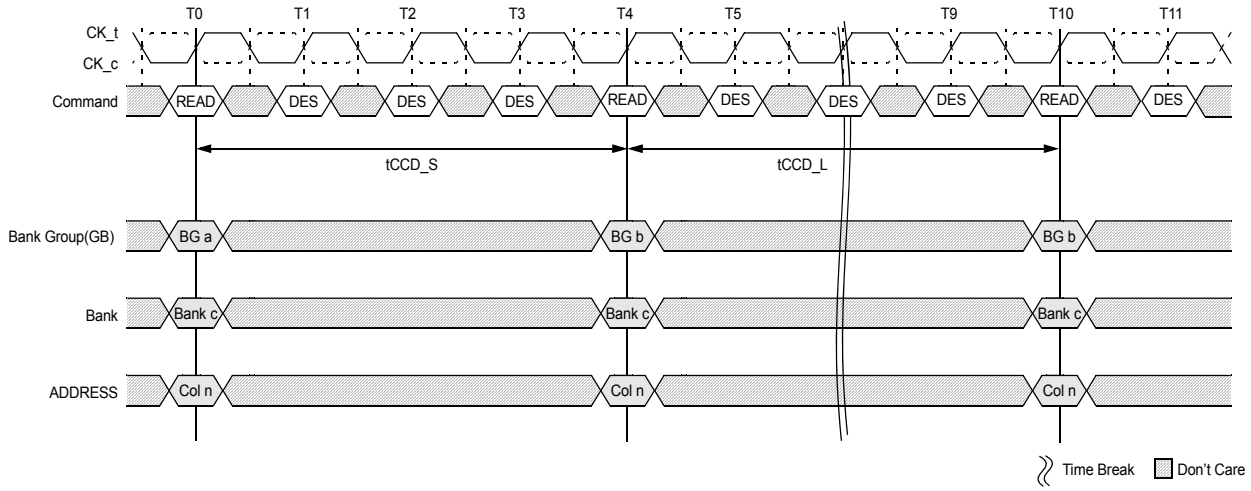
4.19 DDR4 Key Core Timing

DDR4, Core Timing



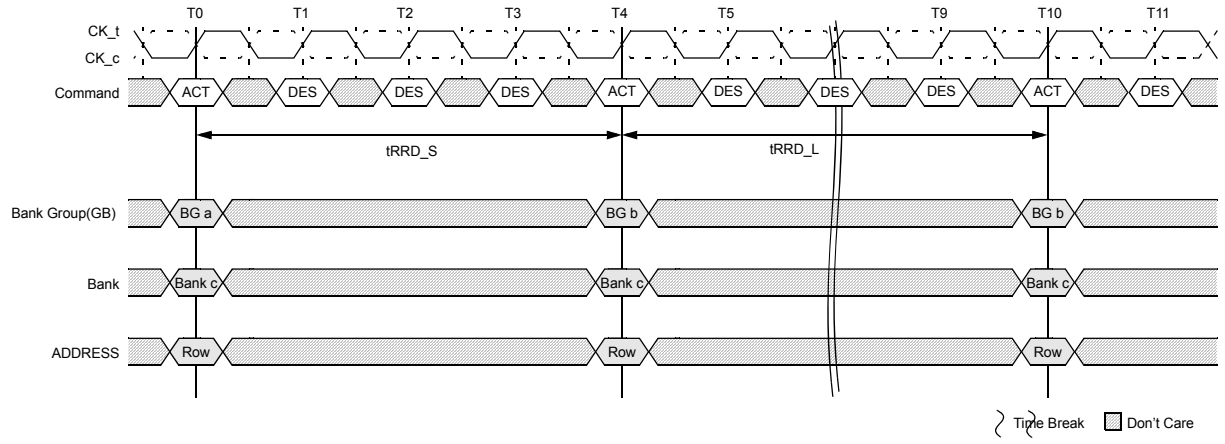
NOTE 1 tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
NOTE 2 tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

Figure 55 — tCCD Timing (WRITE to WRITE Example)



NOTE 1 tCCD_S : CAS_n-to-CAS_n delay (short) : Applies to consecutive CAS_n to different Bank Group (i.e. T0 to T4)
NOTE 2 tCCD_L : CAS_n-to-CAS_n delay (long) : Applies to consecutive CAS_n to the same Bank Group (i.e. T4 to T10)

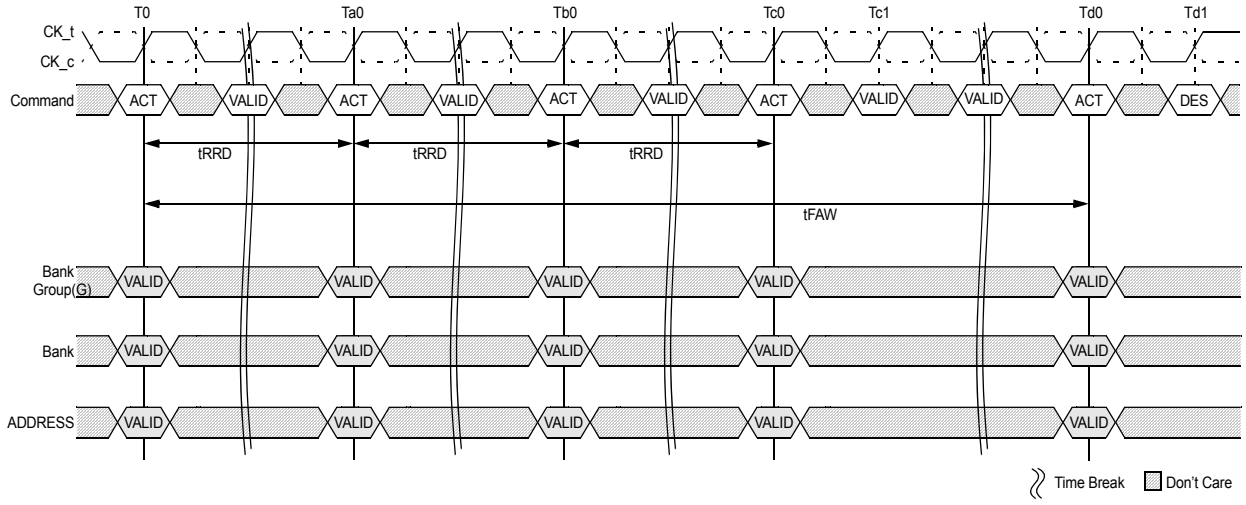
Figure 56 — tCCD Timing (READ to READ Example)



NOTE 1 tRRD_S : ACTIVATE to ACTIVATE Command period (short) : Applies to consecutive ACTIVATE Commands to different Bank Group (i.e. T0 to T4)

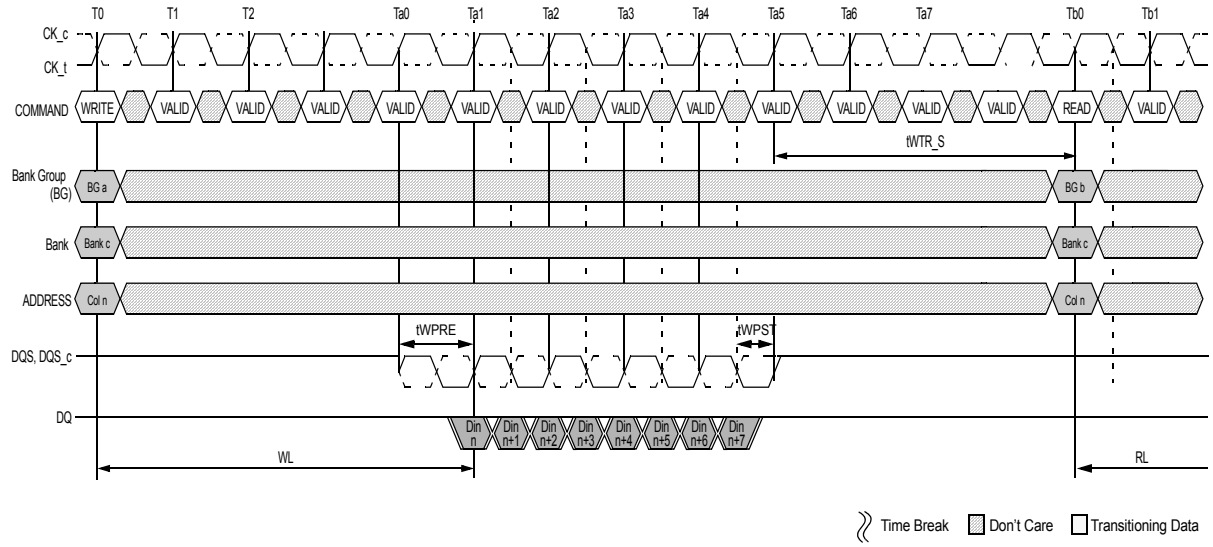
NOTE 2 tRRD_L : ACTIVATE to ACTIVATE Command period (long) : Applies to consecutive ACTIVATE Commands to the different Banks of the same Bank Group (i.e. T4 to T10)

Figure 57 — tRRD Timing



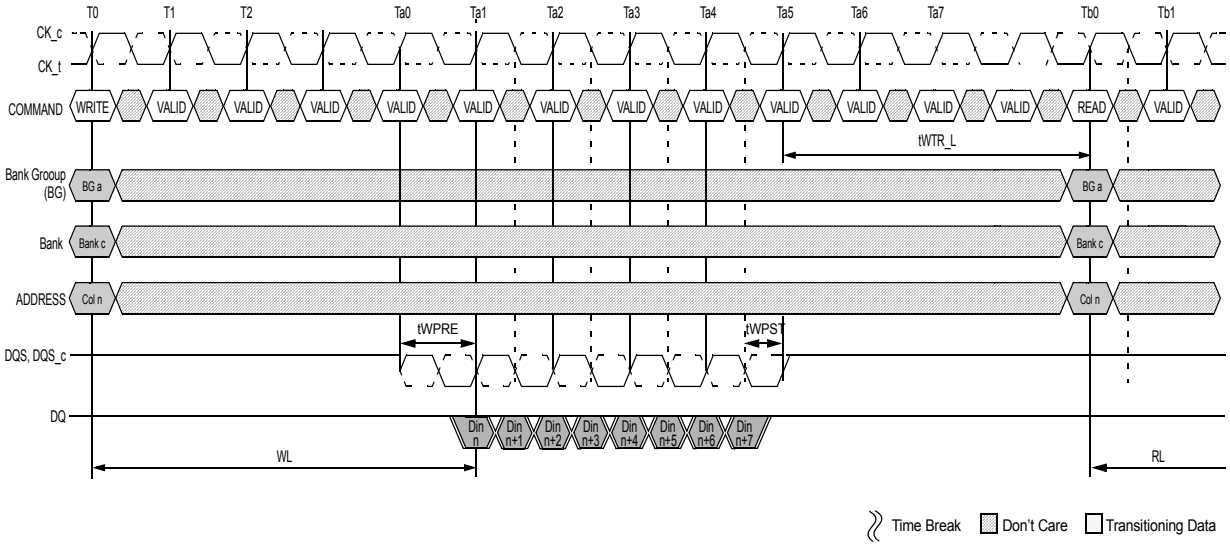
NOTE 1 tFAW : Four activate window :

Figure 58 — tFAW Timing



NOTE 1 tWTR_S : Delay from start of internal write transaction to internal read command to a different Bank Group.

Figure 59 — tWTR_S Timing (WRITE to READ, Different Bank Group, CRC and DM Disabled)



NOTE 1 tWTR_L : Delay from start of internal write transaction to internal read command to the same Bank Group.

Figure 60 — tWTR_L Timing (WRITE to READ, Same Bank Group, CRC and DM Disabled)

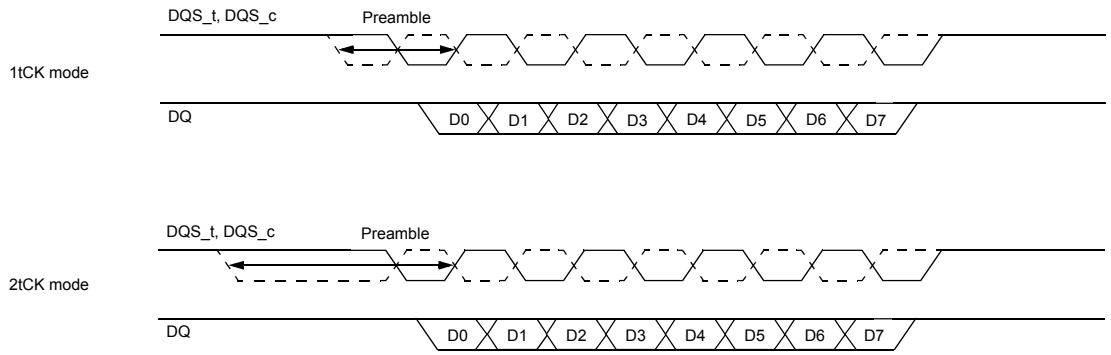
4.20 Programmable Preamble

4.20.1 Write Preamble

DDR4 will support a programmable write preamble.
Write preamble modes of 1 tCK and 2 tCK are shown below.

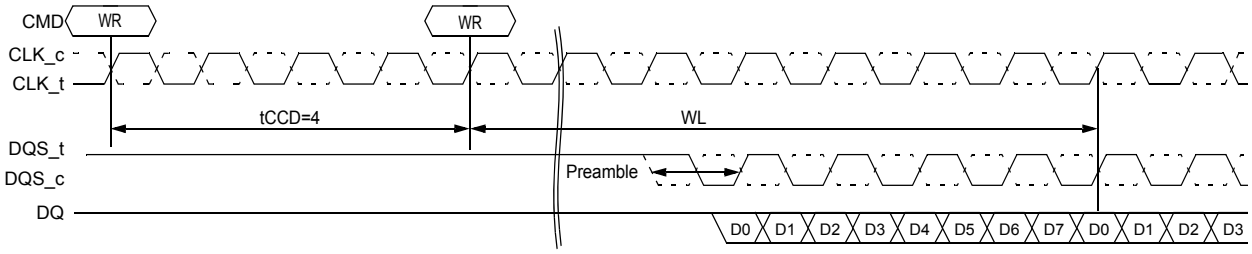
1 tCK and 2 tCK modes are selectable by MRS.
CWL needs to be incremented by 1nCK when 2tCK preamble is enabled.

When operating in 2tCK Write Preamble Mode, tWTR and tWR must be programmed to a value 1 clock greater than the tWTR and tWR setting supported in the applicable speed bin.



The timing diagrams contained in Figure 61, Figure 62 and Figure 63 illustrate 1 and 2 tCK preamble scenarios for consecutive write commands with tCCD timing of 4, 5 and 6 nCK, respectively. Setting tCCD to 5nCK is not allowed in 2 tCK preamble mode

1tCK mode



2tCK mode

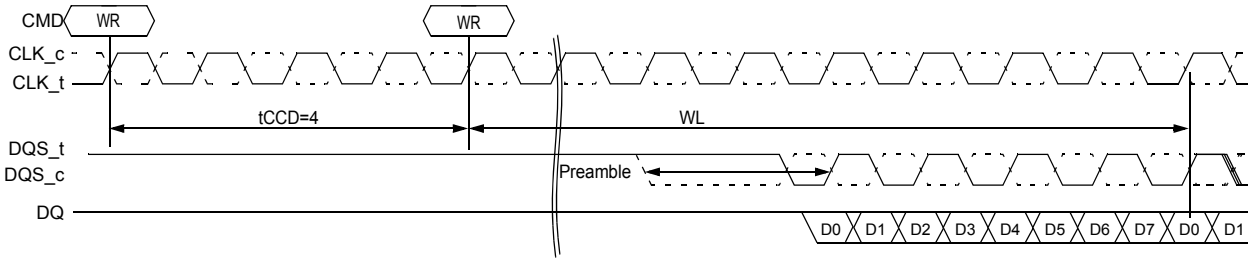
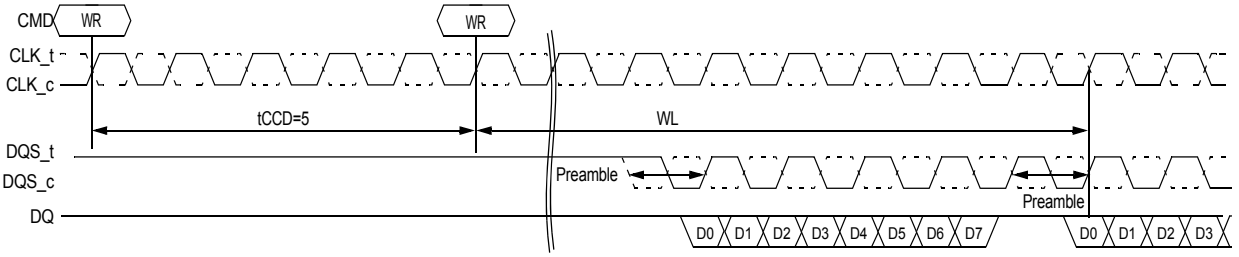


Figure 61 — tCCD=4 (AL=PL=0)

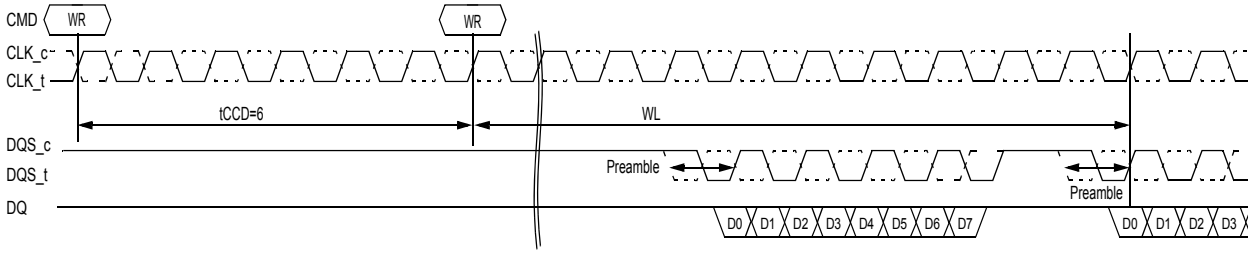
1tCK mode



2tCK mode: **tCCD=5 is not allowed in 2tCK mode**

Figure 62 — tCCD=5 (AL=PL=0)

1tCK mode



2tCK mode

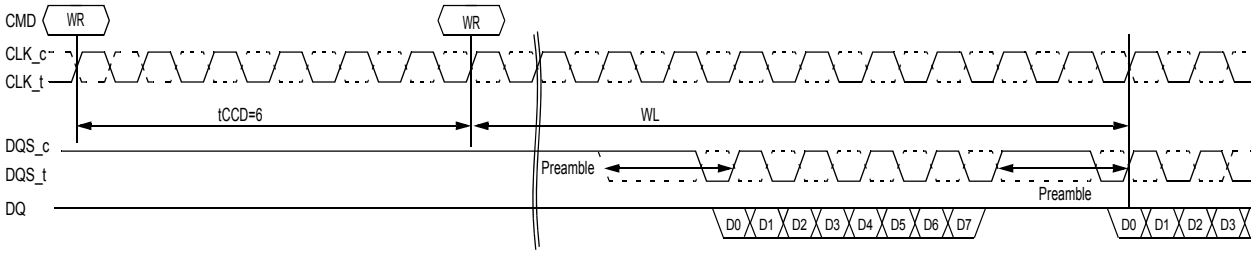
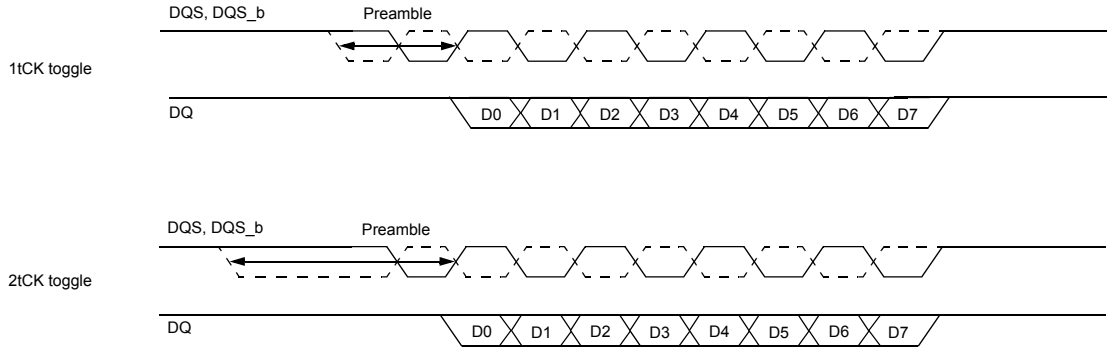


Figure 63 — tCCD=6 (AL=PL=0)

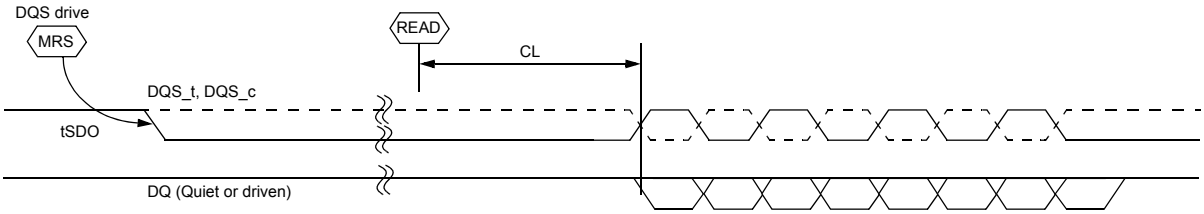
4.20.2 Read Preamble

DDR4 will support a programmable read preamble.
Read preamble modes of 1 tCK and 2 tCK are shown below.



4.20.3 Read Preamble Training

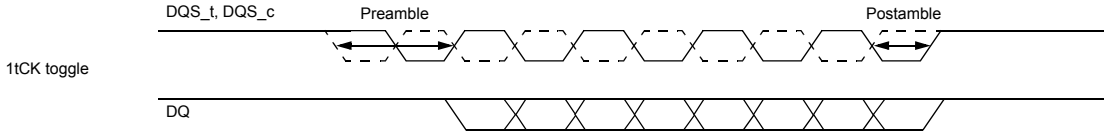
DDR4 will support a programmable read preamble. This requires an additional MRS mode to train the read preamble for read leveling. The MRS mode below will be used for Read preamble training and It is only available in MPR mode.
Illegal READ commands, any command during the READ process or initiating the READS process, are not allowed during Read Preamble Training.

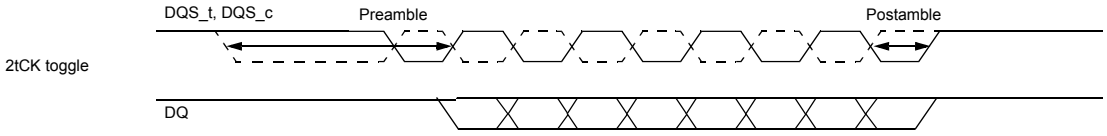


4.21 Postamble

4.21.1 Read Postamble

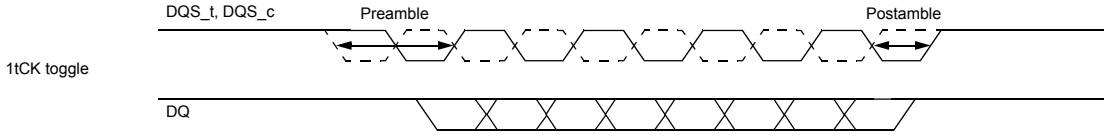
DDR4 will support a fixed read postamble.
Read postamble of nominal 0.5tck for preamble modes 1,2 Tck are shown below:

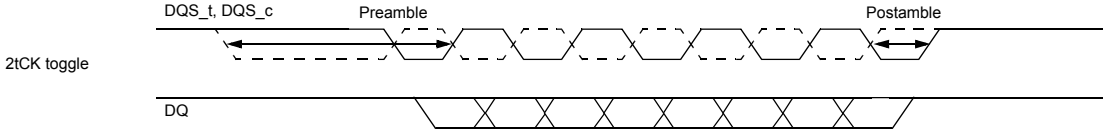




4.21.2 Write Postamble

DDR4 will support a fixed Write postamble.
Write postamble nominal is 0.5tck for preamble modes 1,2 Tck are shown below:





4.22 ACTIVATE Command

The ACTIVATE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BG0-BG1 in X4/8 and BG0 in X16 select the bankgroup; BA0-BA1 inputs selects the bank within the bankgroup, and the address provided on inputs A0-A17 selects the row. This row remains active (or open) for accesses until a precharge command is issued to that bank or a precharge all command is issued. A bank must be precharged before opening a different row in the same bank.

4.23 Precharge Command

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row activation a specified time (tRP) after the PRECHARGE command is issued, except in the case of concurrent auto precharge, where a READ or WRITE command to a different bank is allowed as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is allowed if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

4.24 Read Operation

4.24.1 READ Timing Definitions

Read timing shown in this section is applied when the DLL is enabled and locked.

Rising data strobe edge parameters:

- tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK_t, CK_c.
- tDQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c.
- tQSH describes the DQS_t, DQS_c differential output high time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tQSL describes the DQS_t, DQS_c differential output low time.
- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.

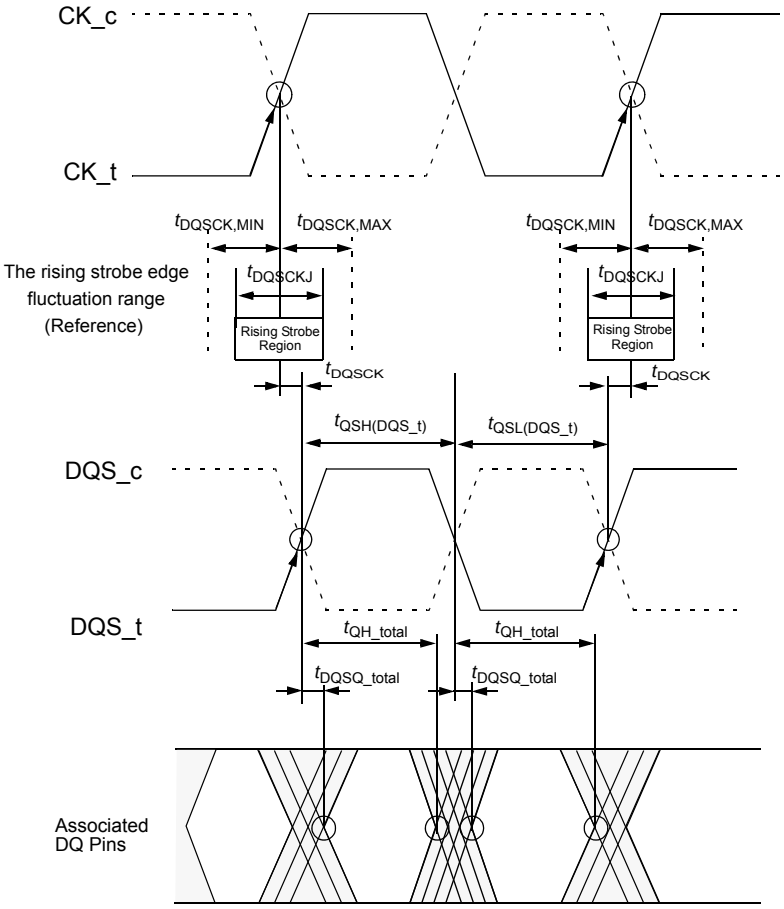


Figure 64 — READ Timing Definition

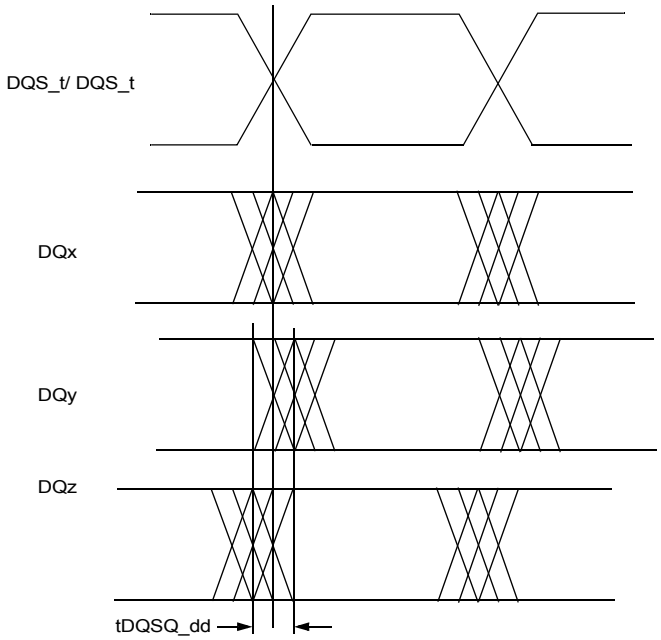


Figure 65 — Read data timing data(DQ) to data(DQ) tDQSQ_dd offset

Table 43 — tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

		DDR4-1600,1866		DDR4-2133,2400			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**	**NOTE**
Data Timing							
DQS_t,DQS_c to DQ Skew total, per group, per access	tDQSQ_total	-	tbd	-	tbd	UI	1,6
DQS_t,DQS_c to DQ Skew deterministic, per group, per access	tDQSQ_dj	-	tbd	-	tbd	UI	2,4,6
DQ output hold time total from DQS_t, DQS_c	tQH_total	tbd	-	tbd	-	UI	1,5,6
DQ output hold time deterministic from DQS_t, DQS_c	tQH_dj	tbd	-	tbd	-	UI	2,4,6
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ_total_dbi _on	-	tbd	-	tbd	UI	1,7
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH_total_dbi_on	tbd	-	tbd	-	UI	1,7
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ_dd	tbd	tbd	tbd	tbd	UI	3,4
Data Strobe Timing							
DQS, DQS# differential output low time	tQSL	tbd	tbd	tbd	tbd	UI	8
DQS, DQS# differential output high time	tQSH	tbd	tbd	tbd	tbd	UI	9

Unit UI = tCK(avg).min/2

NOTE 1 DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are TBD.
NOTE 2 The deterministic component of the total timing. Measurement method TBD.
NOTE 3 DQ to DQ static offset relative to strobe per group. Measurement method TBD.
NOTE 4 This parameter will be characterized and guaranteed by design.
NOTE 5 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example TBD.
NOTE 6 DRAM DBI mode is off.
NOTE 7 DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
NOTE 8 tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge

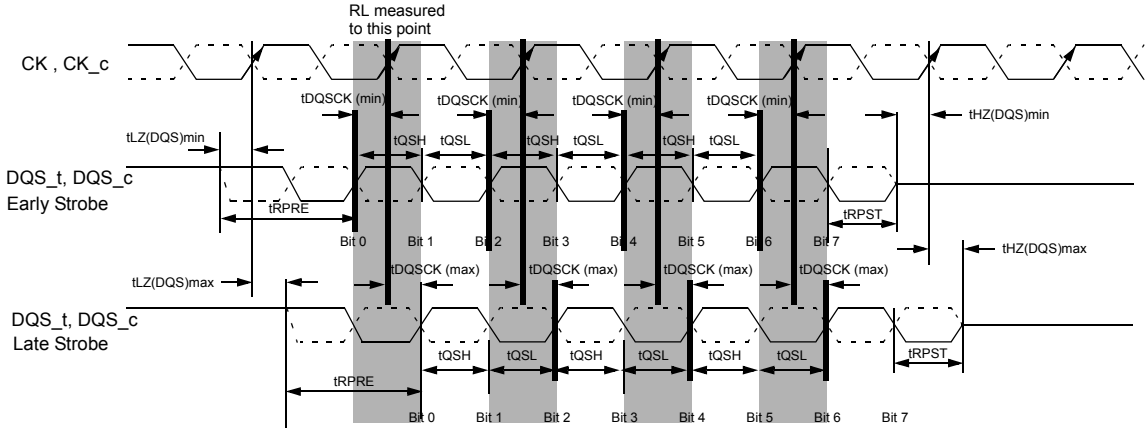
4.24.1.1 READ Timing; Clock to Data Strobe relationship

Clock to Data Strobe relationship is shown in Figure 66 and is applied when the DLL is enabled and locked.
Rising data strobe edge parameters:

- •tDQSCK min/max describes the allowed range for a rising data strobe edge relative to CK_t, CK_c.
- •tDQSCK is the actual position of a rising strobe edge relative to CK_t, CK_c.
- •tQSH describes the data strobe high pulse width.

Falling data strobe edge parameters:

- tQSL describes the data strobe low pulse width.
- tLZ(DQS), tHZ(DQS) for preamble/postamble.



NOTE 1 Within a burst, rising strobe edge will be varied within tDQSCKJ by fixed and constant VDD. However incorporate the device, voltage and temperature variation, rising strobe edge will be varied between tDQSCK(min) and tDQSCK(max).

NOTE 2 Notwithstanding note 1, a rising strobe edge with tDQSCK(max) at T(n) can not be immediately followed by a rising strobe edge with tDQSCK(min) at T(n+1). This is because other timing relationships (tQSH, tQSL) exist:

if tDQSCK(n+1) < 0:
tDQSCK(n) < 1.0 tCK - (tQSHmin + tQSLmin) - |tDQSCK(n+1)|

NOTE 3 The DQS_t, DQS_c differential output high time is defined by tQSH and the DQS_t, DQS_c differential output low time is defined by tQSL.

NOTE 4 Likewise, tLZ(DQS)min and tHZ(DQS)min are not tied to tDQSCKmin (early strobe case) and tLZ(DQS)max and tHZ(DQS)max are not tied to tDQSCKmax (late strobe case).

NOTE 5 The minimum pulse width of read preamble is defined by tRPRE(min).

NOTE 6 The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZDQS(max) on the right side.

NOTE 7 The minimum pulse width of read postamble is defined by tRPST(min).

NOTE 8 The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side.

Figure 66 — Clock to Data Strobe Relationship

4.24.1.2 READ Timing; Data Strobe to Data relationship

The Data Strobe to Data relationship is shown in Figure 67 and is applied when the DLL is enabled and locked.

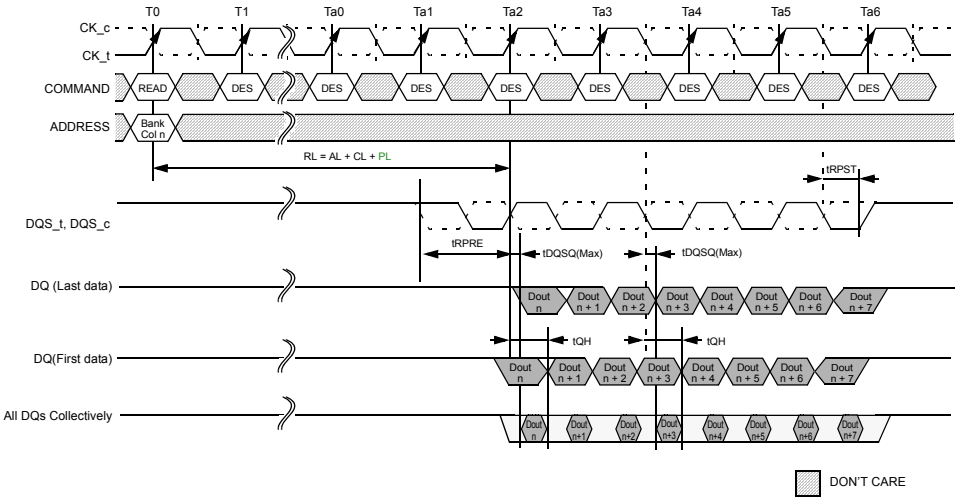
Rising data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

Falling data strobe edge parameters:

- tDQSQ describes the latest valid transition of the associated DQ pins.
- tQH describes the earliest invalid transition of the associated DQ pins.

tDQSQ; both rising/falling edges of DQS, no tAC defined.



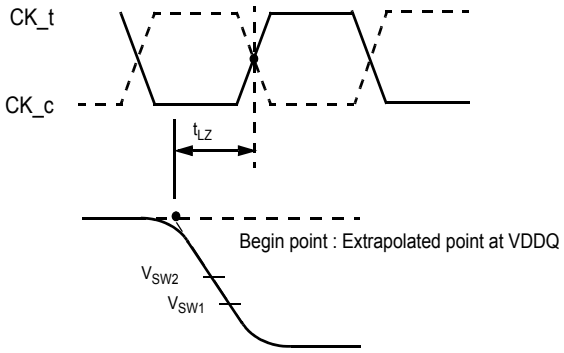
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
NOTE 5 Output timings are referenced to VDDQ, and DLL on for locking.
NOTE 6 tDQSQ defines the skew between DQS_t,DQS_c to Data and does not define DQS_t, DQS_c to Clock.
NOTE 7 Early Data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst

Figure 67 — Data Strobe to Data Relationship

4.24.1.3 tLZ(DQS), tLZ(DQ), tHZ(DQS), tHZ(DQ) Calculation

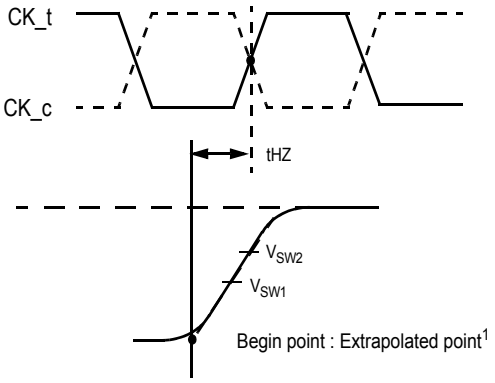
tHZ and tLZ transitions occur in the same time window as valid data transitions. These parameters are referenced to a specific voltage level that specifies when the device output is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ). Figure 68 shows a method to calculate the point when the device is no longer driving tHZ(DQS) and tHZ(DQ), or begins driving tLZ(DQS), tLZ(DQ), by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters tLZ(DQS), tLZ(DQ), tHZ(DQS), and tHZ(DQ) are defined as single ended.

tLZ(DQ): CK_t - CK_c rising crossing at RL



tLZ(DQ) begin point is above-mentioned extrapolated point.

tHZ(DQ) with BL8: CK_t - CK_c rising crossing at RL + 4 nCK
tHZ(DQ) with BC4: CK_t - CK_c rising crossing at RL + 2 nCK



tHZ(DQ) is begin point is above-mentioned extrapolated point.

NOTE 1 Extrapolated point (Low Level) = VDDQ - ((VDDQ/(50+34)) X 34)
- Ron = 34ohm
- Reference Load= 50ohm

Figure 68 — tLZ and tHZ method for calculating transitions and begin points

Table 44 — Reference Voltage for tLZ, tHZ Timing Measurements

Measured Parameter	Vsw1	Vsw2	Figure	Note
tLZ	TBD	TBD	Figure 68	
tHZ	TBD	TBD		

4.24.1.4 tRPRE Calculation

The method for calculating differential pulse widths for tRPRE is shown in Figure 69.

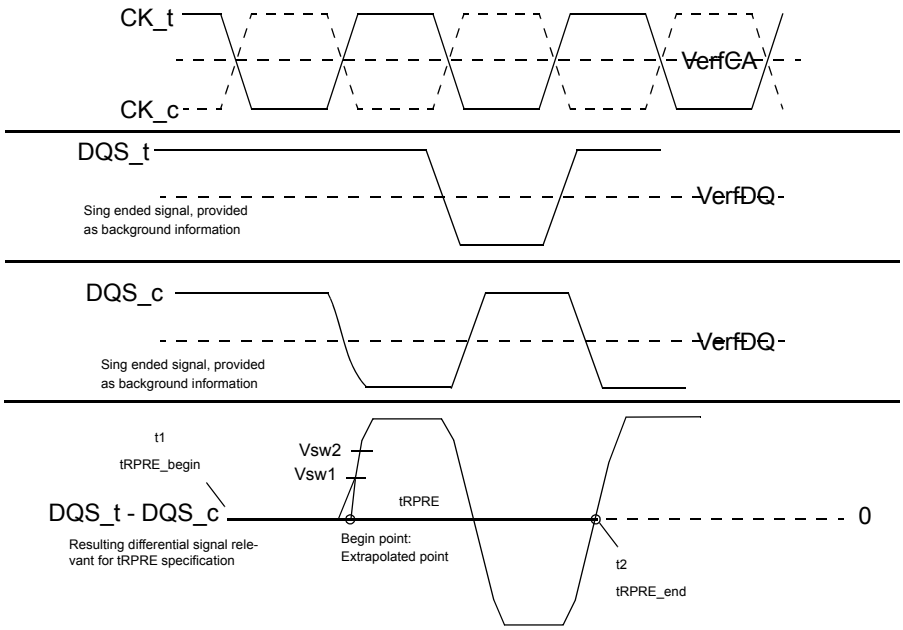


Figure 69 — Method for calculating tRPRE transitions and endpoints

Table 45 — Reference Voltage for tRPRE Timing Measurements

Measured Parameter	Vsw1	Vsw2	Figure	Note
tRPRE	TBD	TBD	Figure 69	

4.24.1.5 tRPST Calculation

The method for calculating differential pulse widths for tRPST is shown in Figure 70.

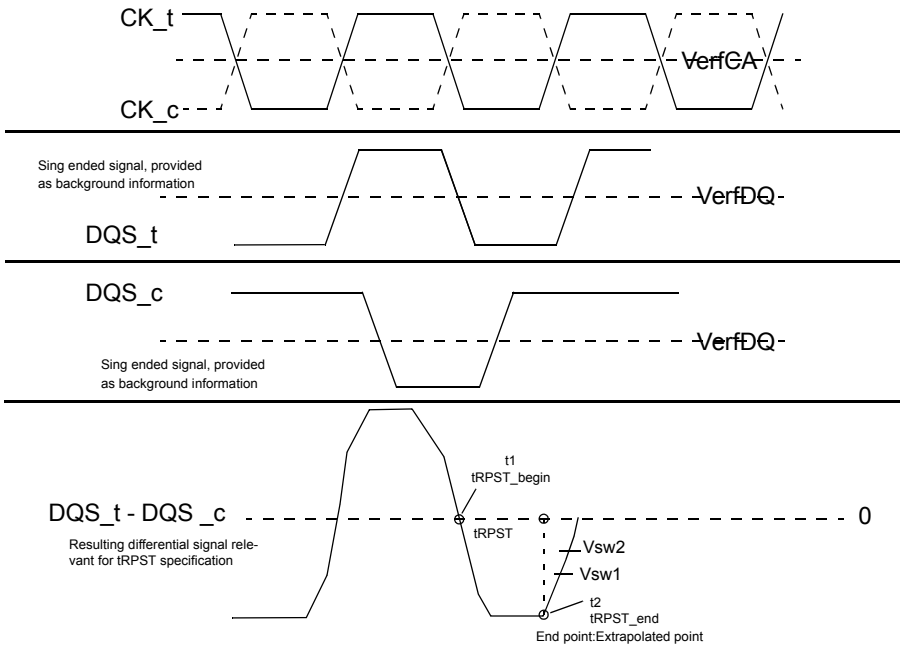


Figure 70 — Method for calculating tRPST transitions and endpoints

Table 46 — Reference Voltage for tRPST Timing Measurements

Measured Parameter	Vsw1	Vsw2	Figure	Note
tRPST	TBD	TBD	Figure 70	

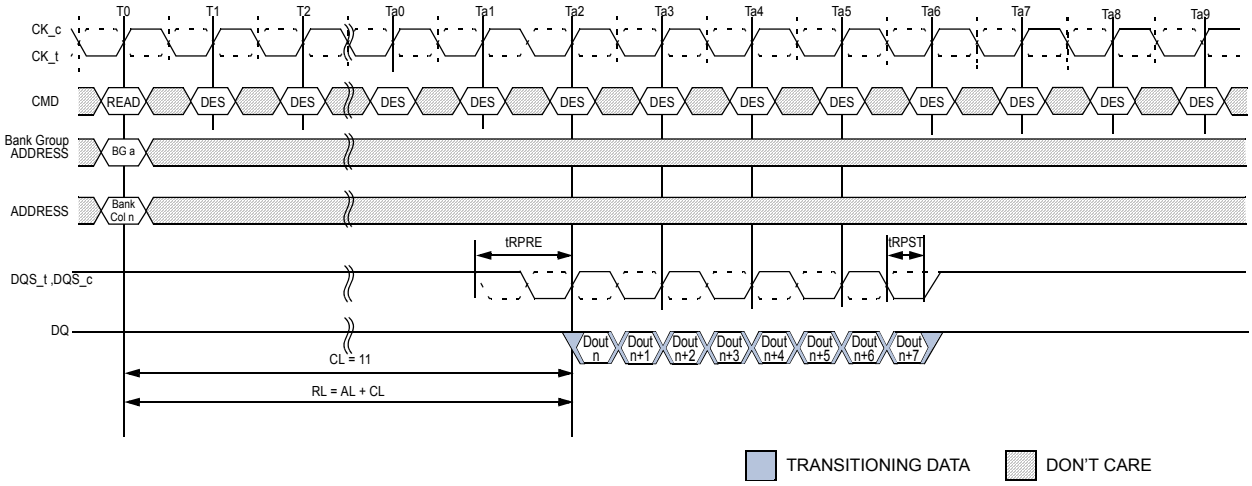
4.24.2 READ Burst Operation

During a READ or WRITE command, DDR4 will support BC4 and BL8 on the fly using address A12 during the READ or WRITE (AUTO PRECHARGE can be enabled or disabled).

A12 = 0 : BC4 (BC4 = burst chop)

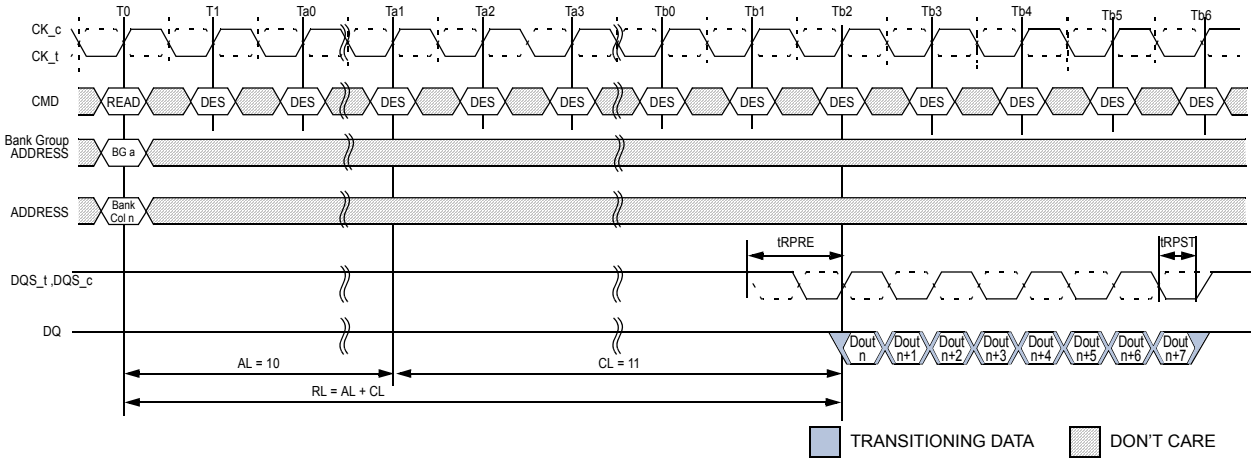
A12 = 1 : BL8

A12 is used only for burst length control, not as a column address.



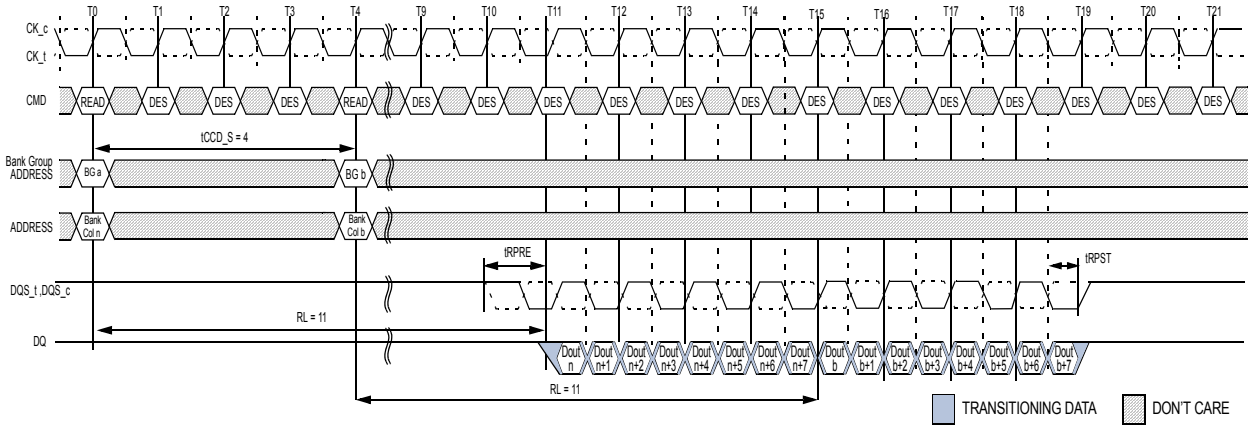
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 71 — READ Burst Operation RL = 11 (AL = 0, CL = 11, BL8)



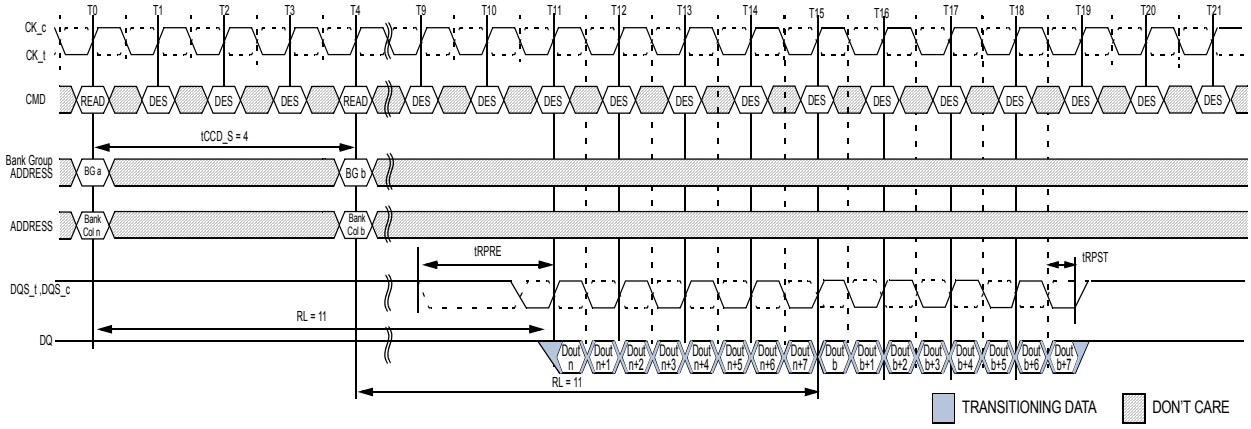
NOTE 1 BL = 8, RL = 21, AL = (CL-1), CL = 11, Preamble = 1tCK
NOTE 2 DOUT n = data-out from column n.
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during READ command at T0.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 72 — READ Burst Operation RL = 21 (AL = 10, CL = 11, BL8)



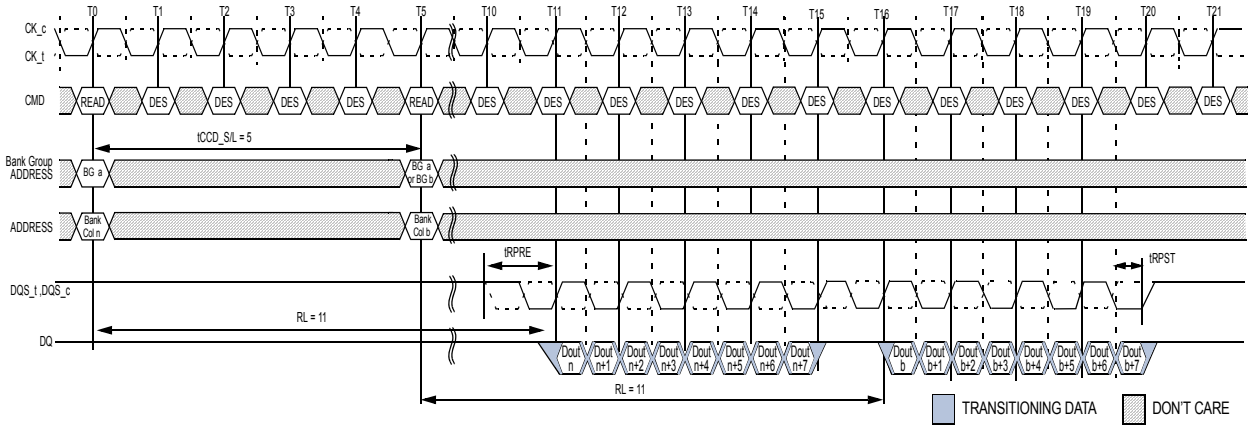
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK
NOTE 2 DOUT n (or b) = data-out from column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 73 — Consecutive READ (BL8) with 1tCK Preamble in Different Bank Group



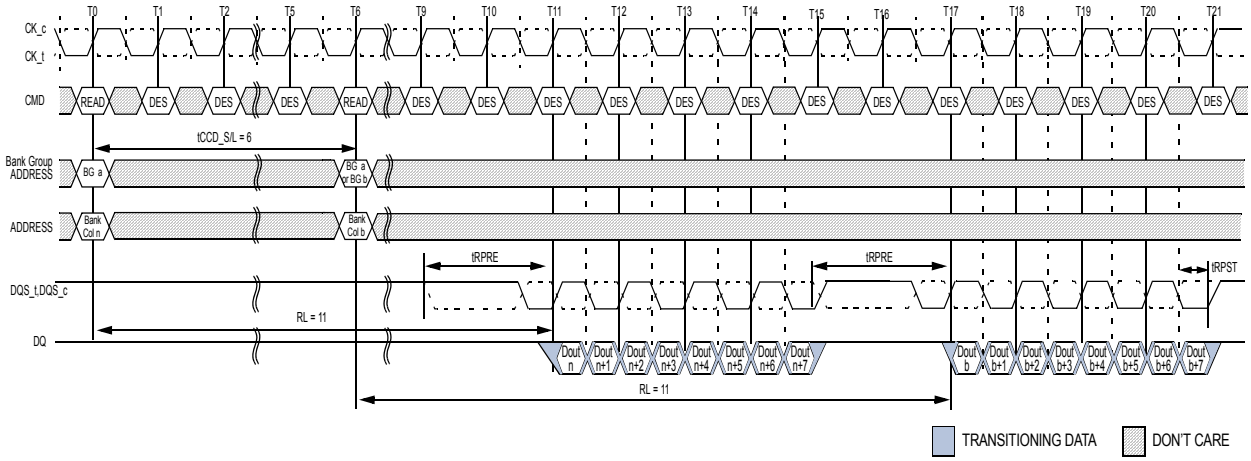
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK
NOTE 2 DOUT n (or b) = data-out from column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A:0 = 0:1] and A12 = 1 during READ command at T0 and T4.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 74 — Consecutive READ (BL8) with 2tCK Preamble in Different Bank Group



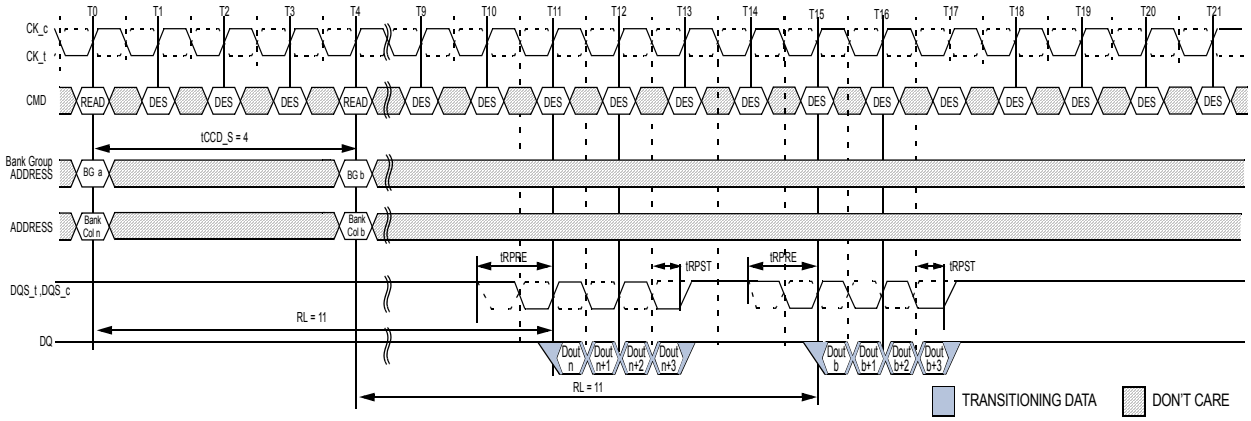
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tCCD_S/L = 5
NOTE 2 DOUT n (or b) = data-out from column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T5.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 75 — Nonconsecutive READ (BL8) with 1tCK Preamble in Same or Different Bank Group



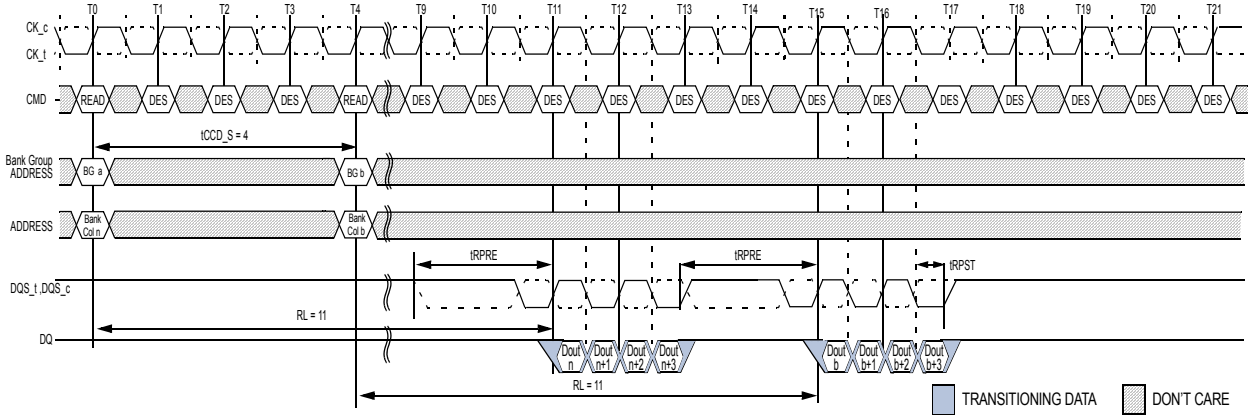
NOTE 1 BL = 8, AL = 0, CL = 11, Preamble = 2tCK, tCCD_S/L = 6
NOTE 2 DOUT n (or b) = data-out from column n (or column b).
NOTE 3 DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 4 BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T6.
NOTE 5 CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable
NOTE 6 tCCD_S/L=5 isn't allowed in 2tCK preamble mode.

Figure 76 — Nonconsecutive READ (BL8) with 2tCK Preamble in Same or Different Bank Group



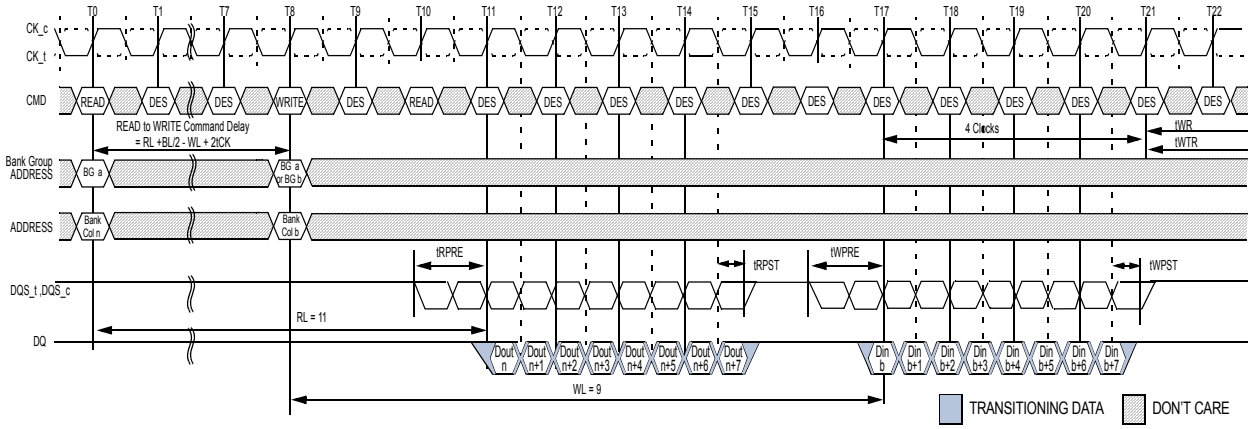
NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

Figure 77 — READ (BC4) to READ (BC4) with 1tCK Preamble in Different Bank Group



NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable

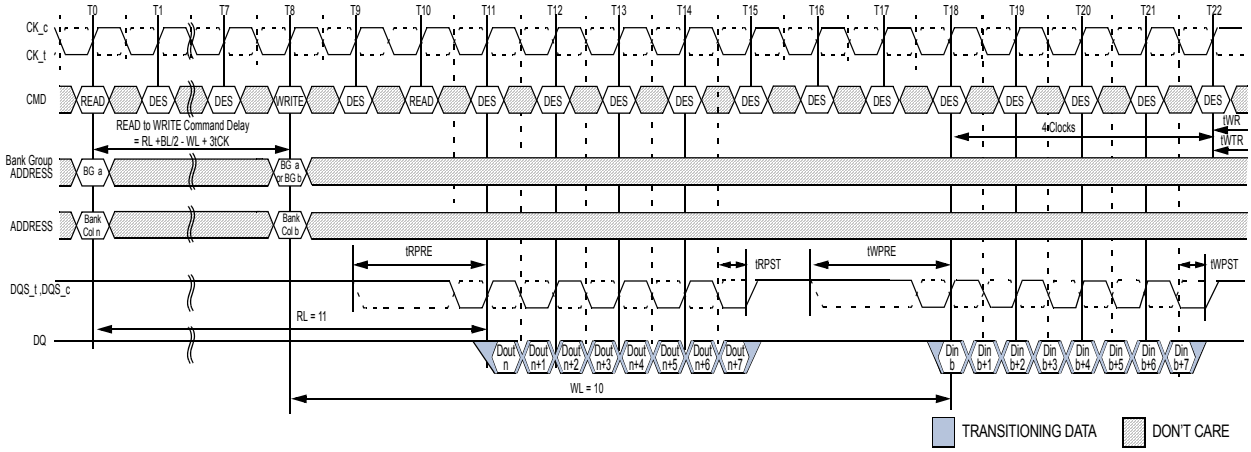
Figure 78 — READ (BC4) to READ (BC4) with 2tCK Preamble in Different Bank Group



NOTE :

1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL =9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

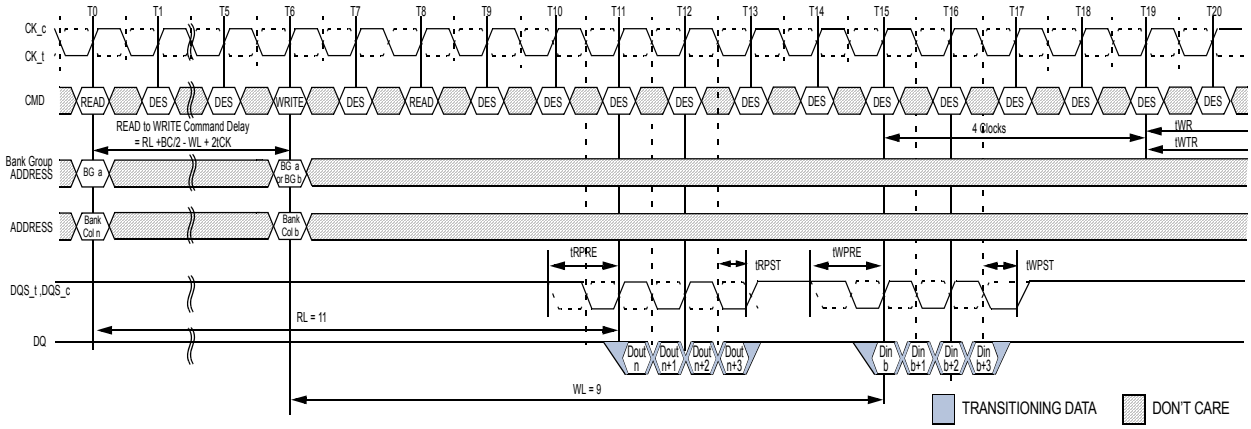
Figure 79 — READ (BL8) to WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE :

1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

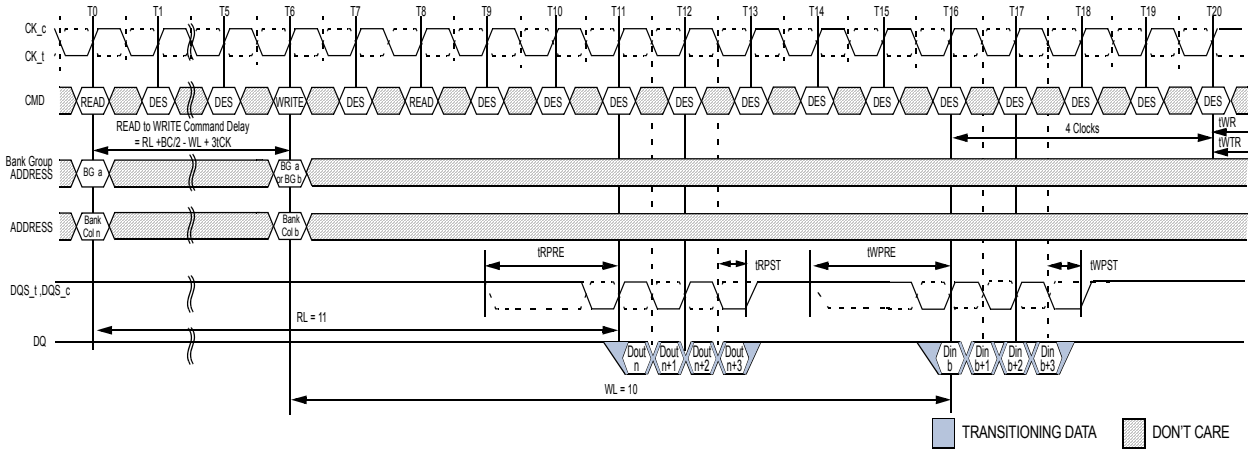
Figure 80 — READ (BL8) to WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE :

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

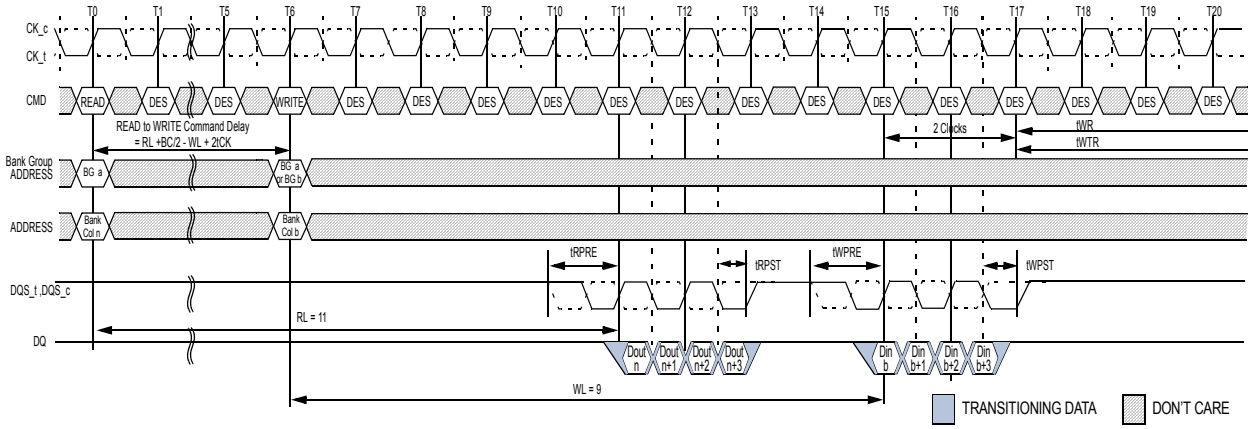
Figure 81 — READ (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE :

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(OTF) setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0 and WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

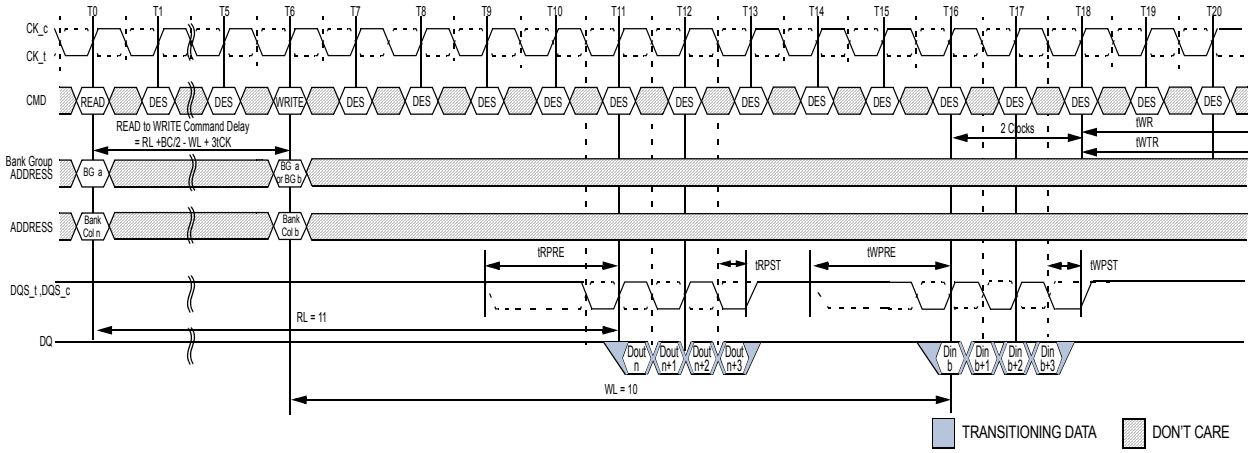
Figure 82 — READ (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE :

1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL = 9 (CWL = 9, AL = 0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

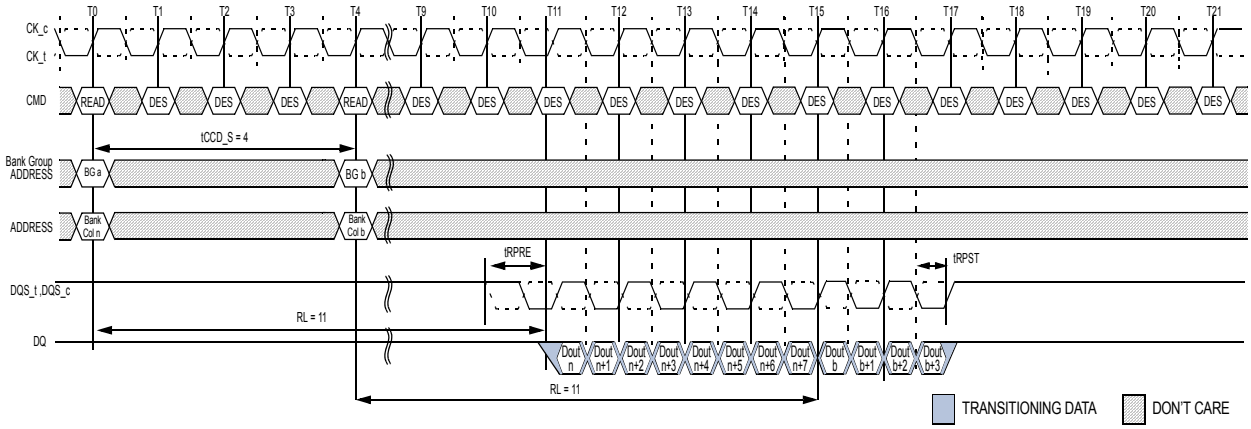
Figure 83 — READ (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Same or Different Bank Group



NOTE :

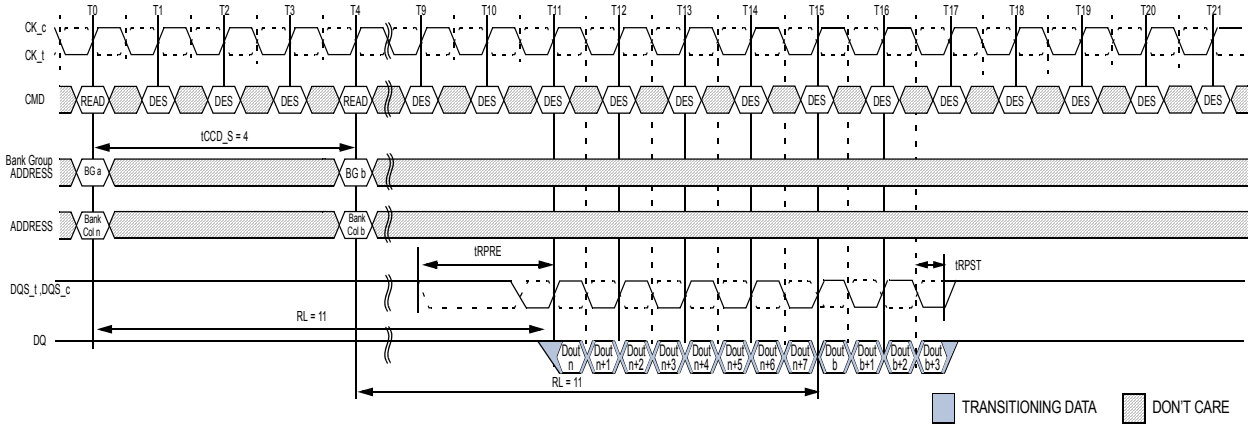
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4(Fixed) setting activated by MR0[A1:A0 = 1:0].
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 84 — READ (BC4) Fixed to WRITE (BC4) Fixed with 2tCK Preamble in Same or Different Bank Group



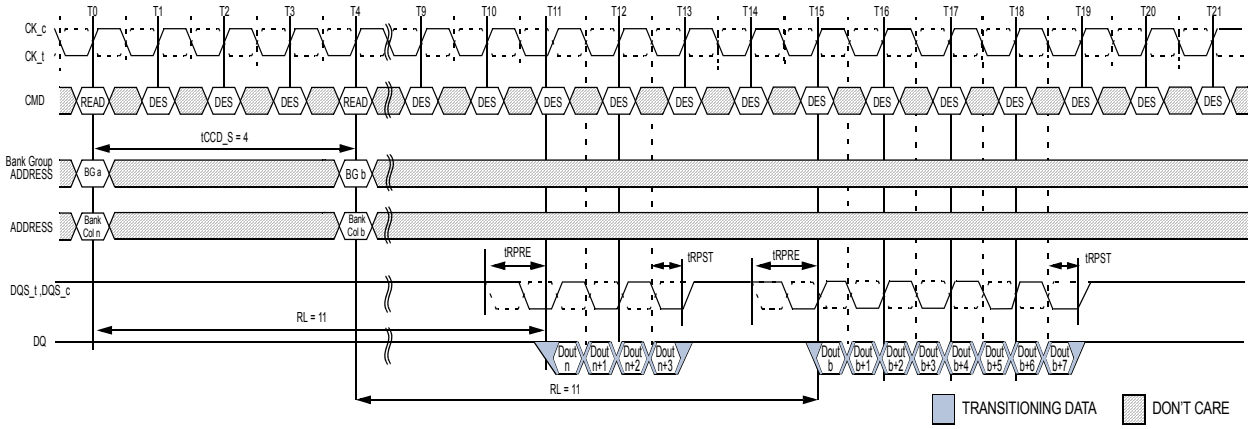
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 85 — READ (BL8) to READ (BC4) OTF with 1tCK Preamble in Different Bank Group



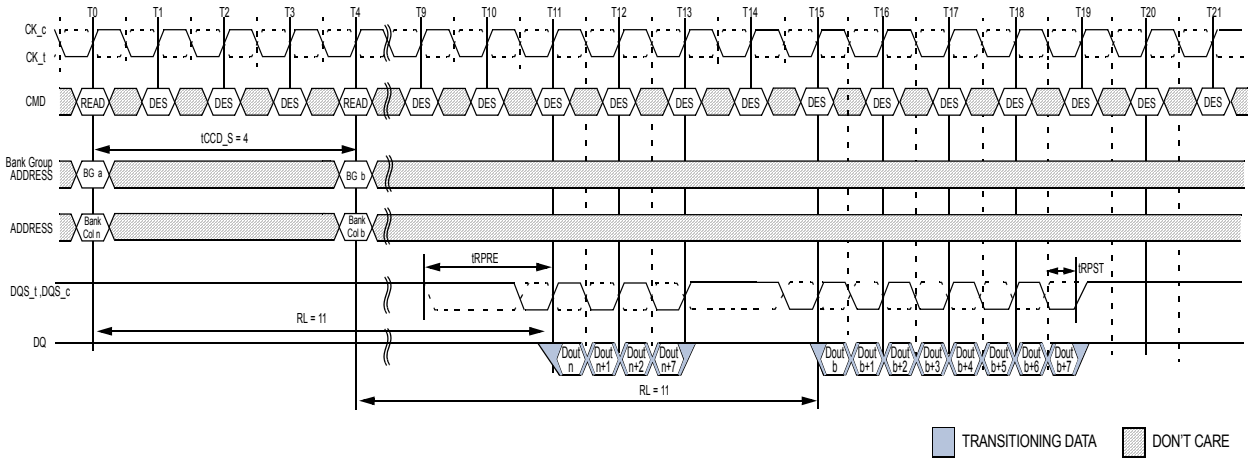
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 86 — READ (BL8) to READ (BC4) OTF with 2tCK Preamble in Different Bank Group



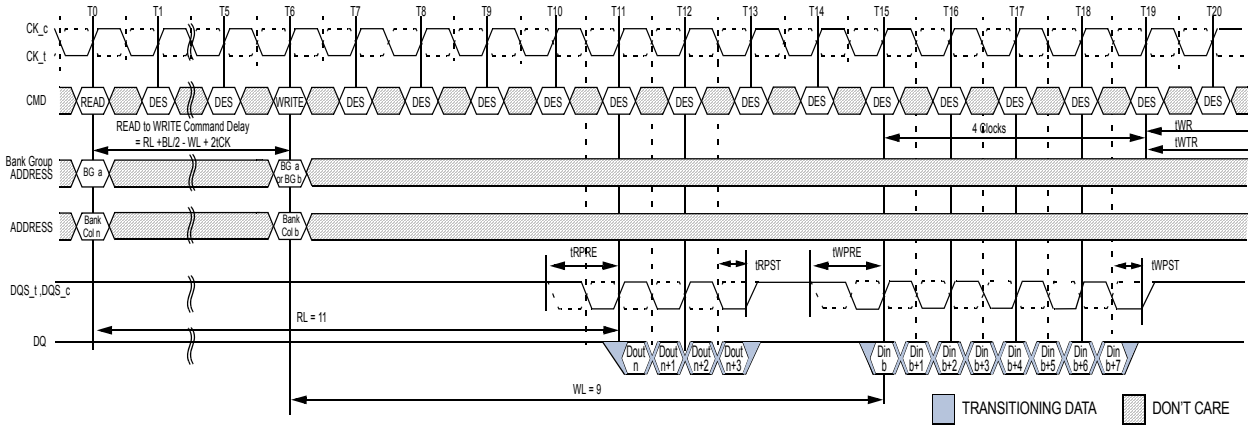
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 87 — READ (BC4) to READ (BL8) OTF with 1tCK Preamble in Different Bank Group



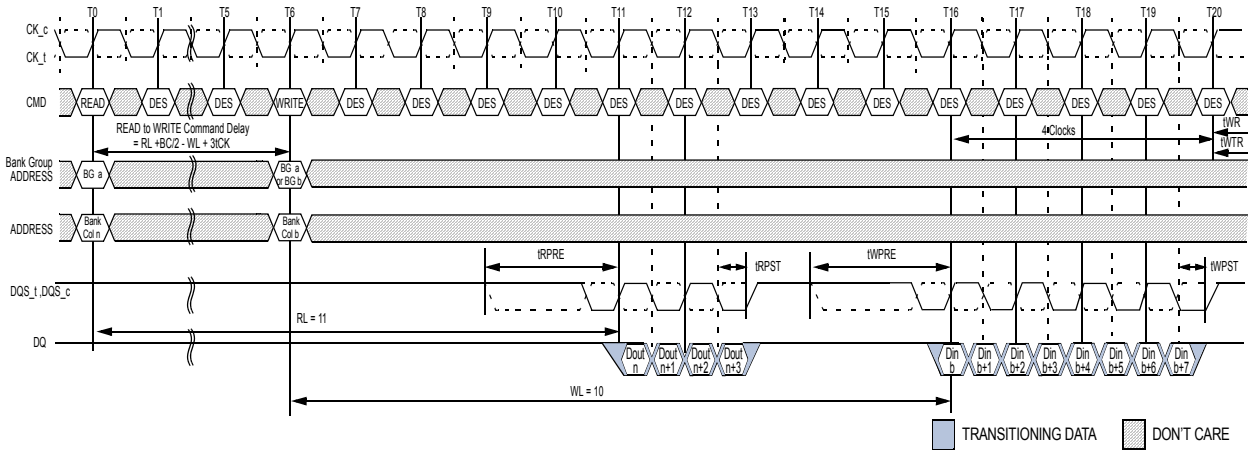
NOTE :
1. BL = 8, AL =0, CL = 11 ,Preamble = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 88 — READ (BC4) to READ (BL8) OTF with 2tCK Preamble in Different Bank Group



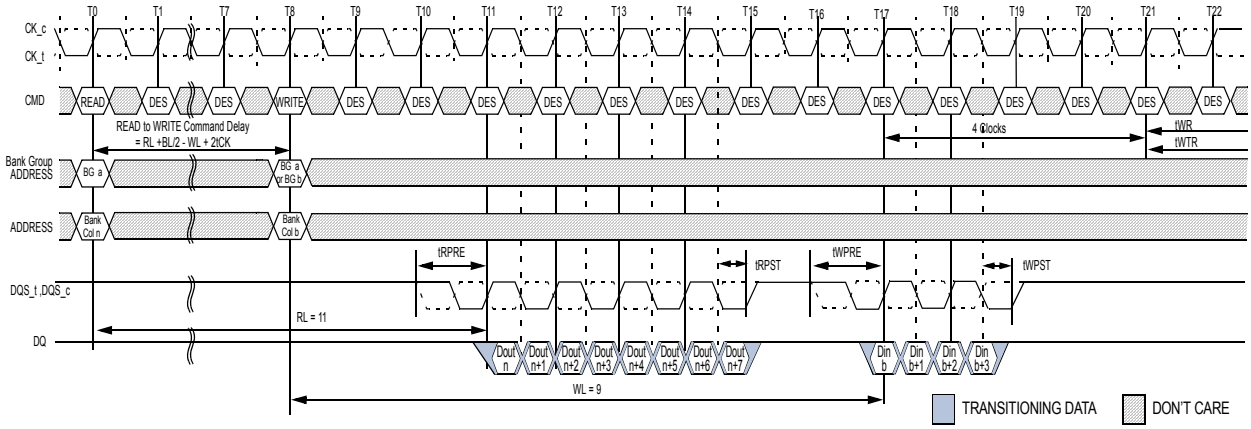
NOTE :
1. BC = 4, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 89 — READ (BC4) to WRITE (BL8) OTF with 1tCK Preamble in Same or Different Bank Group



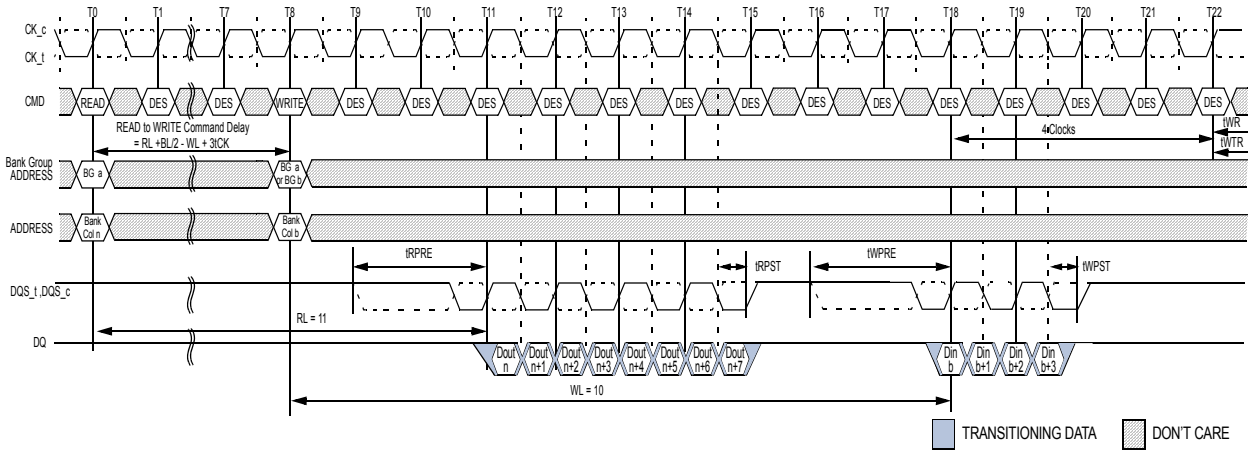
NOTE :
1. BC = 4, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T6.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 90 — READ (BC4) to WRITE (BL8) OTF with 2tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Read Preamble = 1tCK, WL=9(CWL=9,AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

Figure 91 — READ (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Same or Different Bank Group



NOTE :
1. BL = 8, RL = 11 (CL = 11, AL = 0), Read Preamble = 2tCK, WL = 10 (CWL = 9+1[*5], AL = 0), Write Preamble = 2tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T8.
5. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

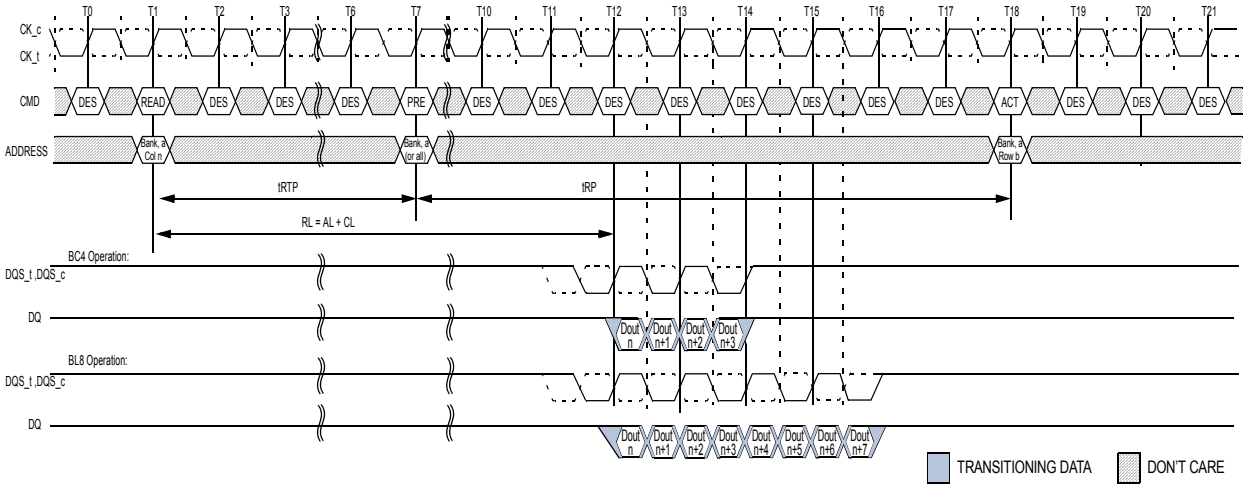
Figure 92 — READ (BL8) to WRITE (BC4) OTF with 2tCK Preamble in Same or Different Bank Group

4.24.3 Burst Read Operation followed by a Precharge

The minimum external Read command to Precharge command spacing to the same bank is equal to AL + tRTP with tRTP being the Internal Read Command to Precharge Command Delay. Note that the minimum ACT to PRE timing, tRAS, must be satisfied as well. The minimum value for the Internal Read Command to Precharge Command Delay is given by tRTP.min, A new bank active command may be issued to the same bank if the following two conditions are satisfied simultaneously:

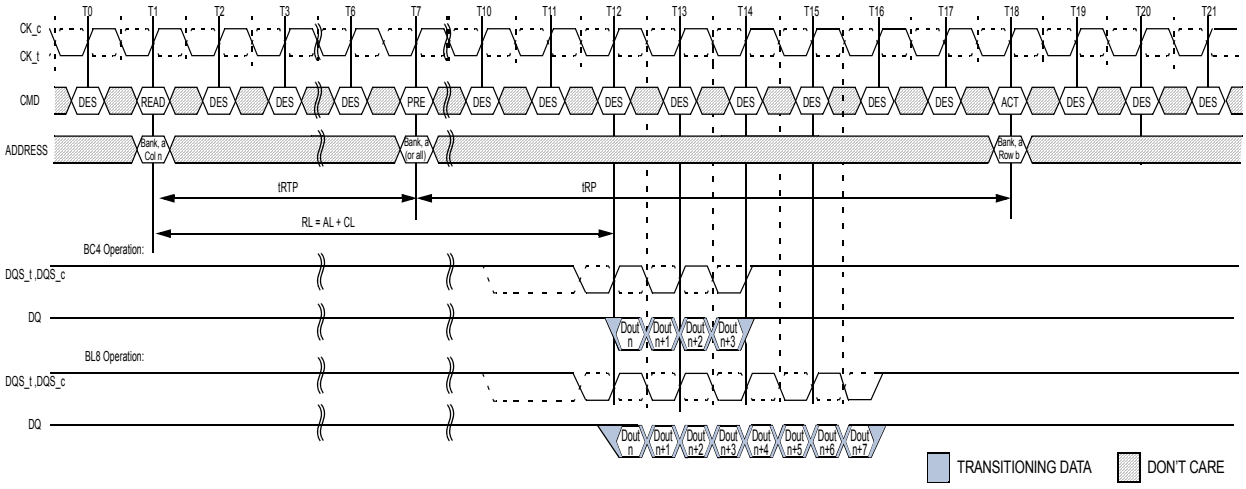
1. The minimum RAS precharge time (tRP.MIN) has been satisfied from the clock at which the precharge begins.
2. The minimum RAS cycle time (tRC.MIN) from the previous bank activation has been satisfied.

Examples of Read commands followed by Precharge are show in Figure 93 to Figure 95.



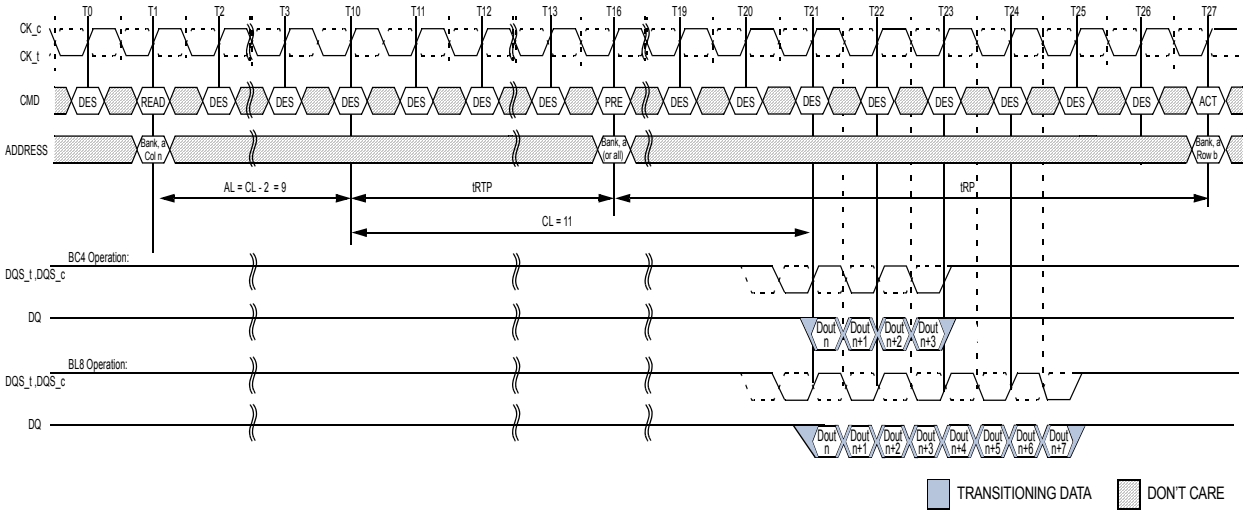
NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 93 — READ to PRECHARGE with 1tCK Preamble



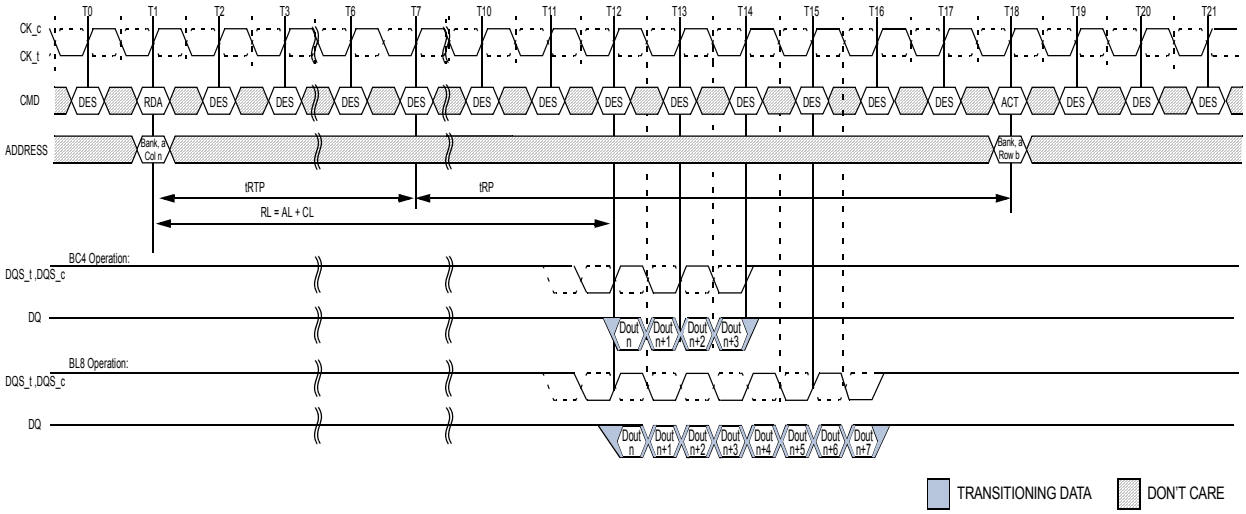
NOTE :
1. BL = 8, RL = 11(CL = 11 , AL = 0), Preamble = 2tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T7) and that tRC. MIN is satisfied at the next Active command time(T18).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 94 — READ to PRECHARGE with 2tCK Preamble



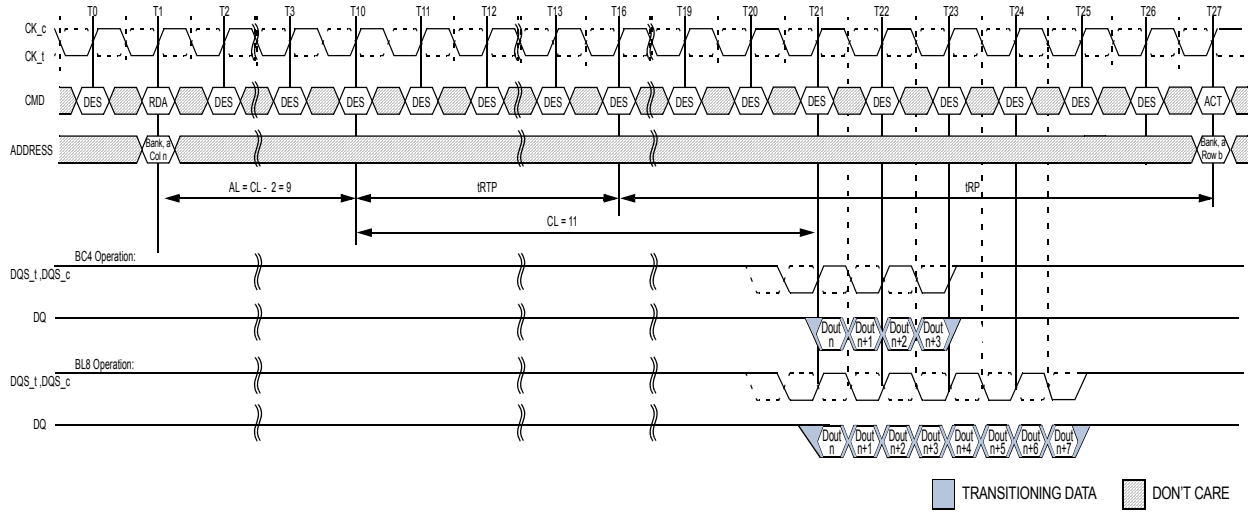
NOTE :
1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. The example assumes tRAS. MIN is satisfied at Precharge command time(T16) and that tRC. MIN is satisfied at the next Active command time(T27).
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 95 — READ to PRECHARGE with Additive Latency and 1tCK Preamble



NOTE :
1. BL = 8, RL = 11 (CL = 11 , AL = 0), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T18).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

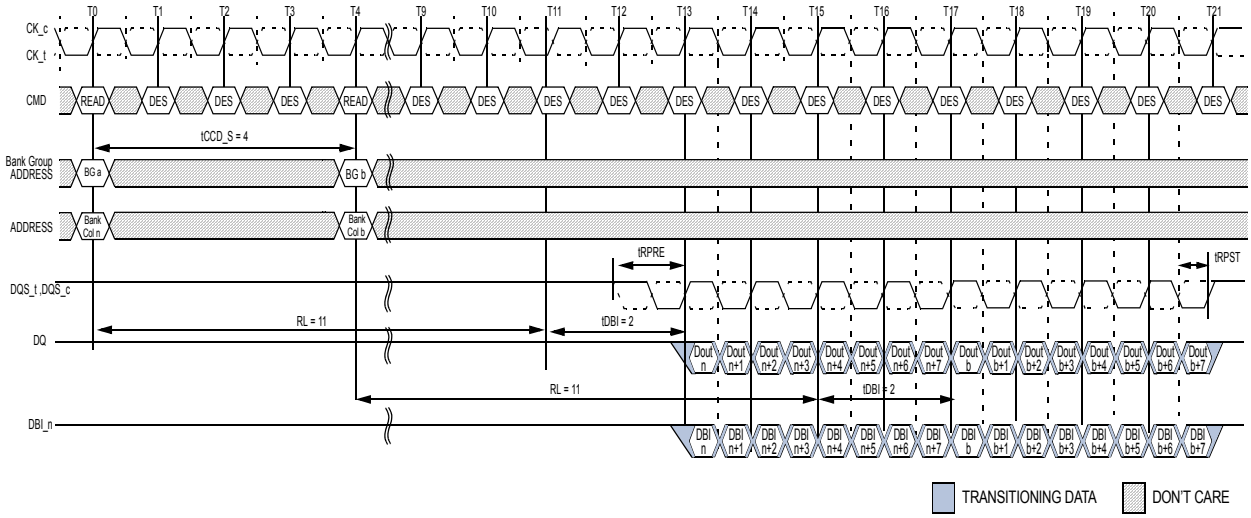
Figure 96 — READ with Auto Precharge and 1tCK Preamble



NOTE :
1. BL = 8, RL = 20 (CL = 11 , AL = CL- 2), Preamble = 1tCK, tRTP = 6, tRP = 11
2. DOUT n = data-out from column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. tRTP = 6 setting activated by MR0[A11:9 = 001]
5. The example assumes tRC. MIN is satisfied at the next Active command time(T27).
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable.

Figure 97 — READ with Auto Precharge, Additive Latency and 1tCK Preamble

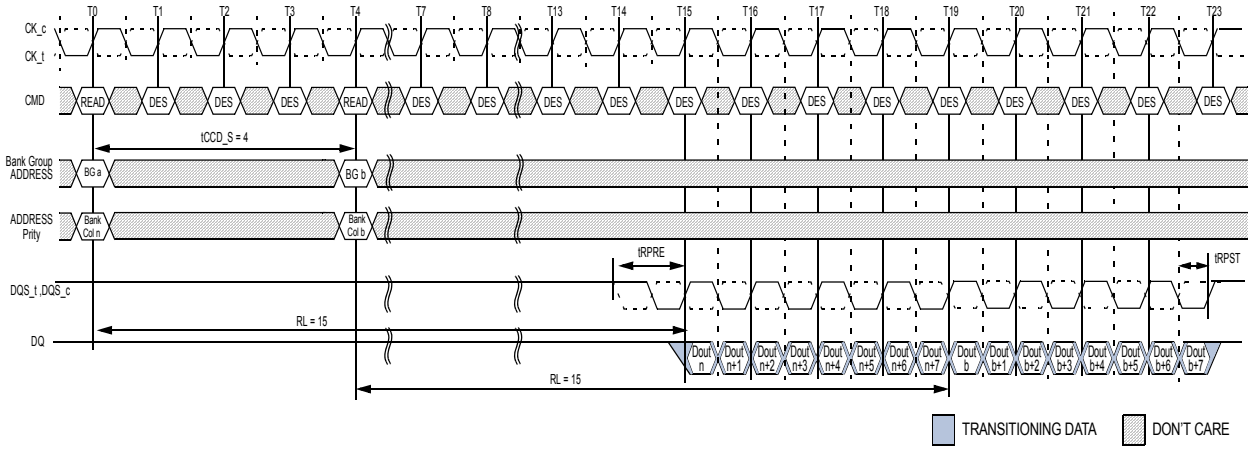
4.24.4 Burst Read Operation with Read DBI (Data Bus Inversion)



NOTE :
1. BL = 8, AL = 0, CL = 11, Preamble = 1tCK, tDBI = 2tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustrat:ion; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 00] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Enable.

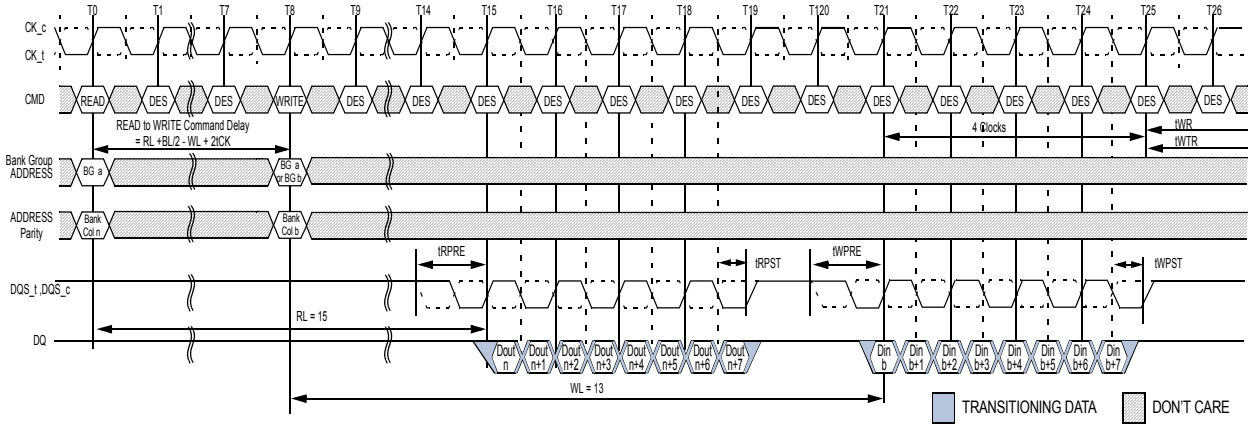
Figure 98 — Consecutive READ (BL8) with 1tCK Preamble and DBI in Different Bank Group

4.24.5 Burst Read Operation with Command/Address Parity



NOTE :
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and T4.
5. CA Parity =Enable, CS to CA Latency = Disable, Read DBI = Disable.

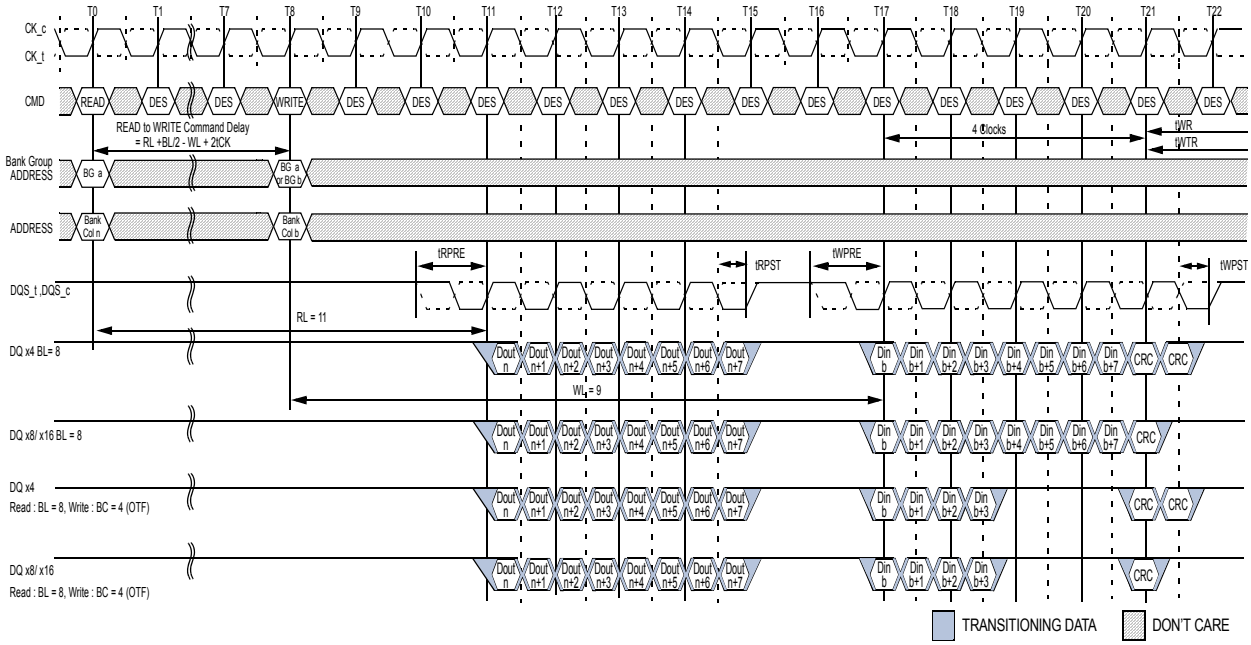
Figure 99 — Consecutive READ (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE :
1. BL = 8, AL = 0, CL = 11, PL = 4, (RL = CL + AL + PL = 15), Read Preamble = 1tCK, CWL=9, AL=0, PL=4, (WL=CL+AL+PL=13), Write Preamble = 1tCK
2. DOUT n = data-out from column n, DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. CA Parity = Enable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Disable.

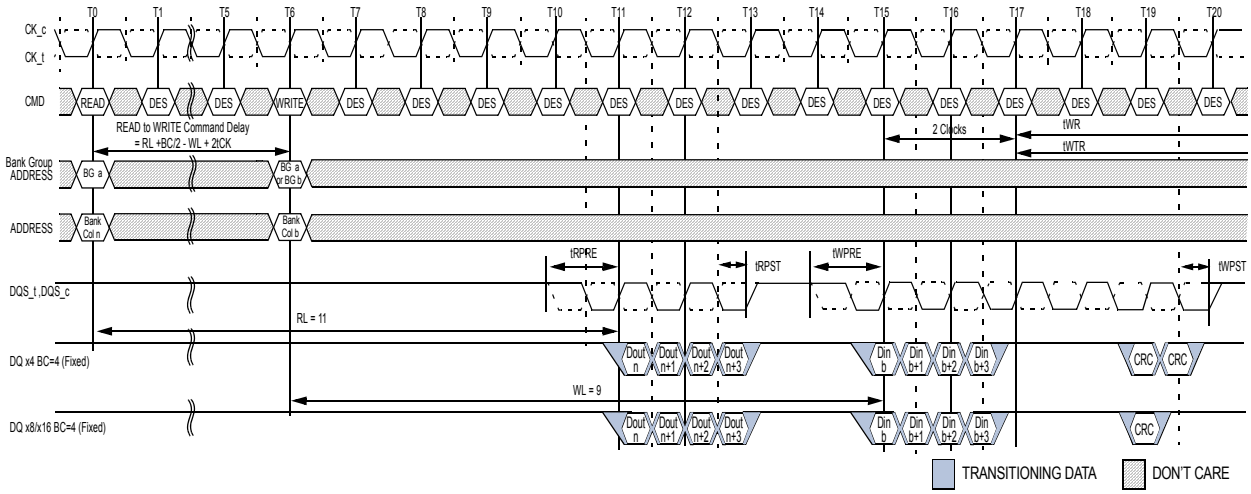
Figure 100 — READ (BL8) to WRITE (BL8) with 1tCK Preamble and CA parity in Same or Different Bank Group

4.24.6 Read to Write with Write CRC



NOTE :
1. BL = 8 (or BC = 4 : OTF for Write), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T0 and Write command at T8.
5. BC4 setting activated by MR0[A1:0 = 01] and A12 = 0 during Write command at T8.
6. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

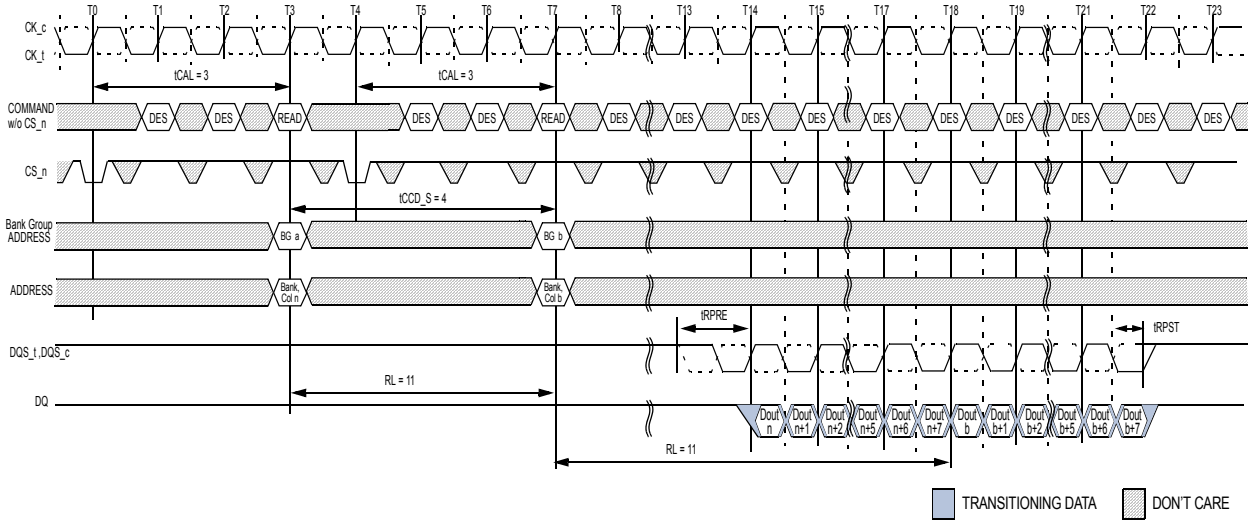
Figure 101 — READ (BL8) to WRITE (BL8 or BC4:OTF) with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE :
1. BC = 4 (Fixed), RL = 11 (CL = 11, AL = 0), Read Preamble = 1tCK, WL=9 (CWL=9, AL=0), Write Preamble = 1tCK
2. DOUT n = data-out from column n . DIN b = data-in to column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Read DBI = Disable, Write DBI = Disable, Write CRC = Enable.

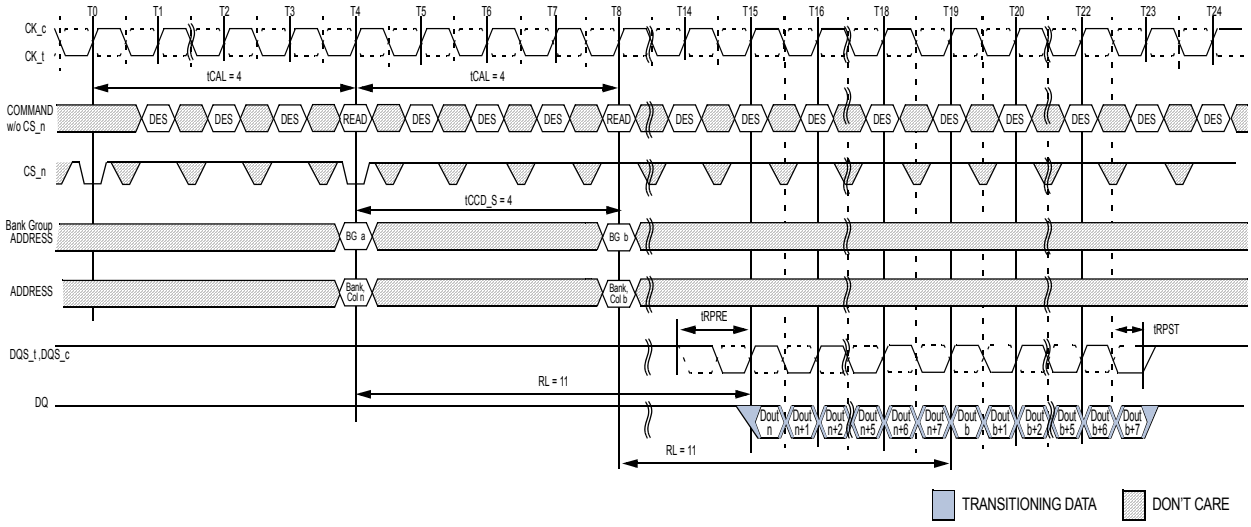
Figure 102 — READ (BC4:Fixed) to WRITE (BC4:Fixed) with 1tCK Preamble and Write CRC in Same or Different Bank Group

4.24.7 Read to Read with CS to CA Latency



NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 3, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T3 and T7.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

Figure 103 — Consecutive READ (BL8) with CAL(3) and 1tCK Preamble in Different Bank Group



NOTE :
1. BL = 8 ,AL = 0, CL = 11, CAL = 4, Preamble = 1tCK
2. DOUT n (or b) = data-out from column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during READ command at T4 and T8.
5. CA Parity = Disable, CS to CA Latency = Enable, Read DBI = Disable.
6. Enabling of CAL mode does not impact ODT control timings. Users should maintain the same timing relationship relative to the command/ address bus as when CAL is disabled.

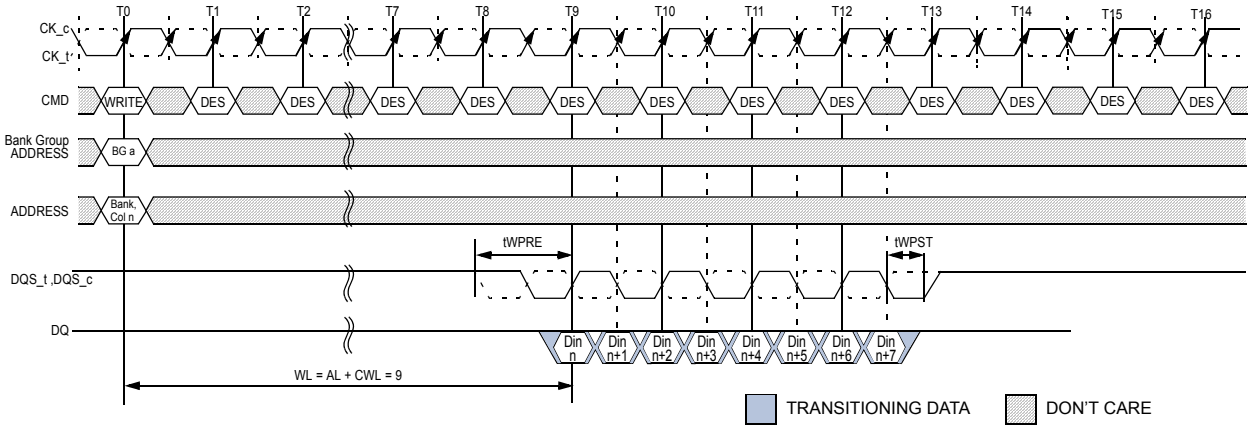
Figure 104 — Consecutive READ (BL8) with CAL(4) and 1tCK Preamble in Different Bank Group

4.25 Write Operation

4.25.1 Write Burst Operation

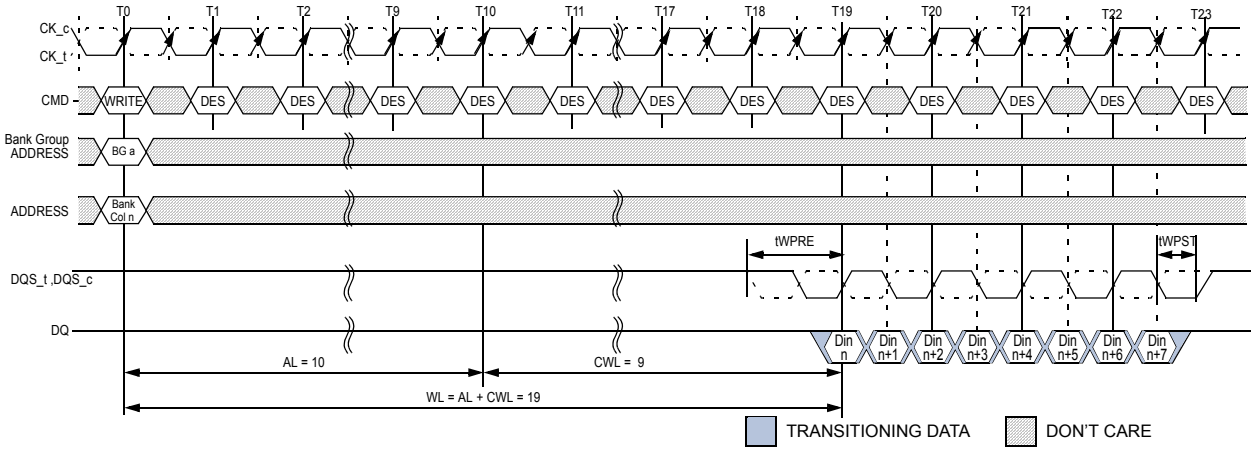
The following write timing diagram is to help understanding of each write parameter's meaning and just examples. The details of the definition of each parameter will be defined separately.

In these write timing diagram, CK and DQS are shown aligned and also DQS and DQ are shown center aligned for illustration purpose.



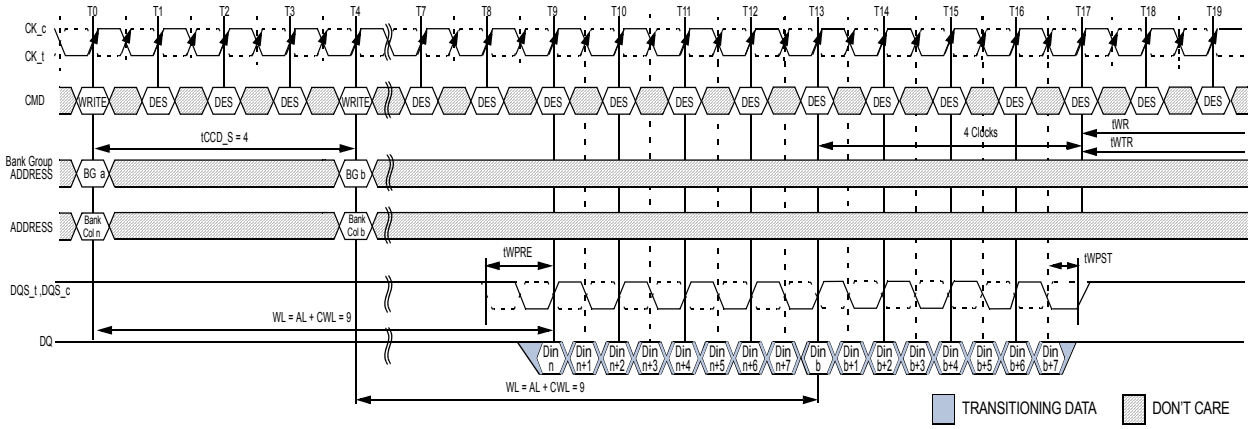
NOTE :
1. BL = 8 ,WL = 9, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

Figure 105 — WRITE Burst Operation WL = 9 (AL = 0, CWL = 9, BL8)



NOTE :
1. BL = 8 ,WL = 19, AL = 10 (CL-1), CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.

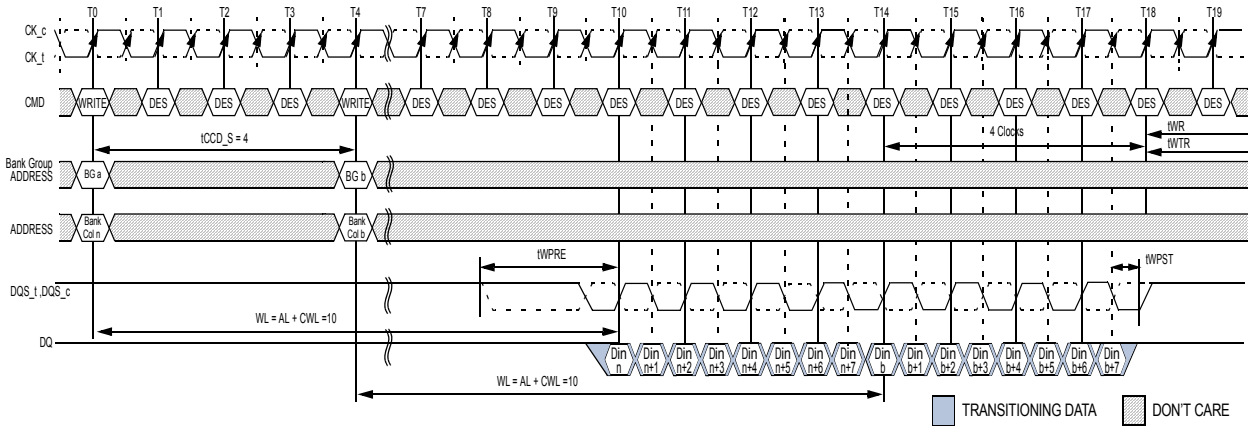
Figure 106 — WRITE Burst Operation WL = 19 (AL = 10, CWL = 9, BL8)



NOTE :

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

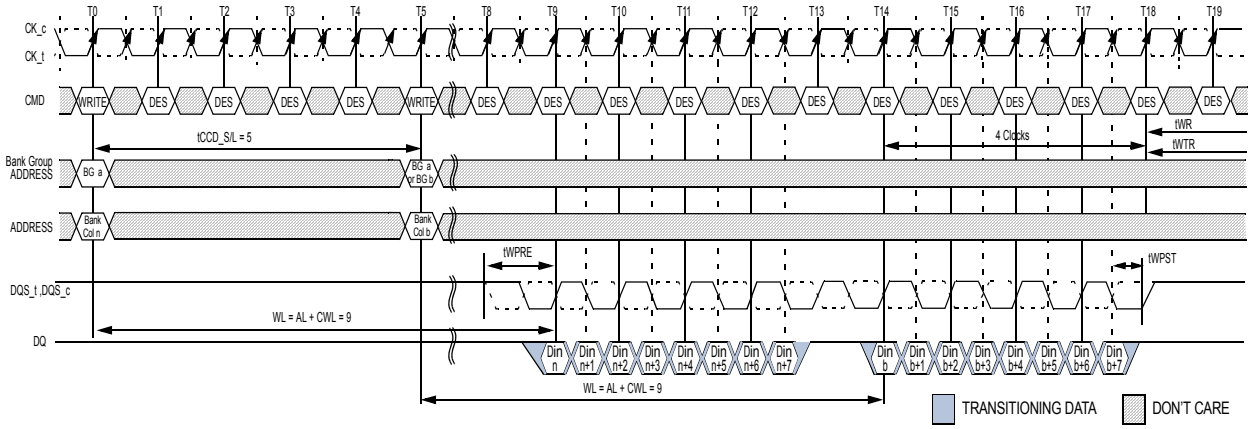
Figure 107 — Consecutive WRITE (BL8) with 1tCK Preamble in Different Bank Group



NOTE :

1. BL = 8 ,AL = 0, CWL = 9 + 1 = 10[7], Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time(tWR) and write timing parameter(tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

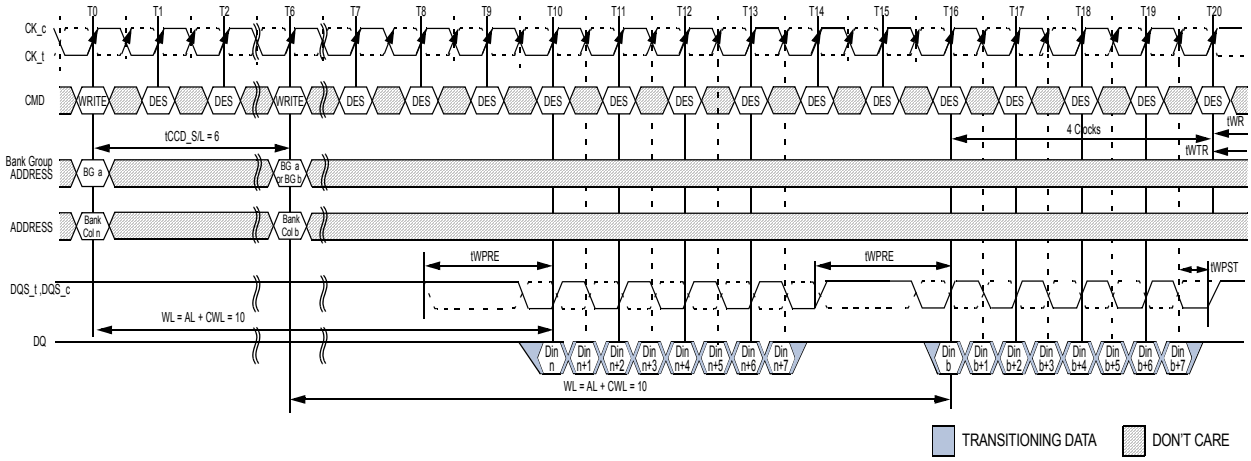
Figure 108 — Consecutive WRITE (BL8) with 2tCK Preamble in Different Bank Group



NOTE:

1. BL = 8 ,AL = 0, CWL = 9 , Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.

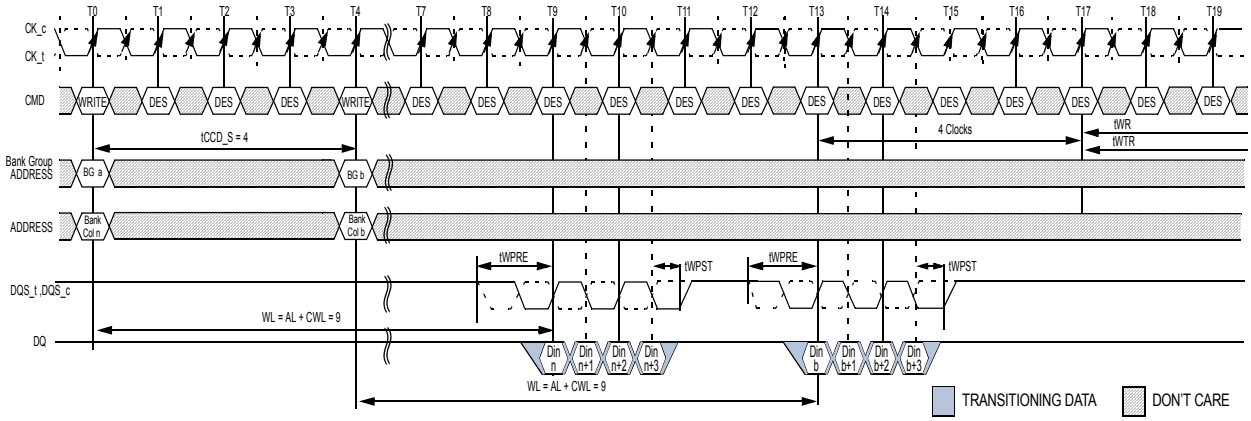
Figure 109 — Nonconsecutive WRITE (BL8) with 1tCK Preamble in Same or Different Bank Group



NOTE:

1. BL = 8 ,AL = 0, CWL = 9 + 1 = 10[8] , Preamble = 2tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and T6.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. tCCD_S/L=5 isn't allowed in 2tCK preamble mode.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T20.
8. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

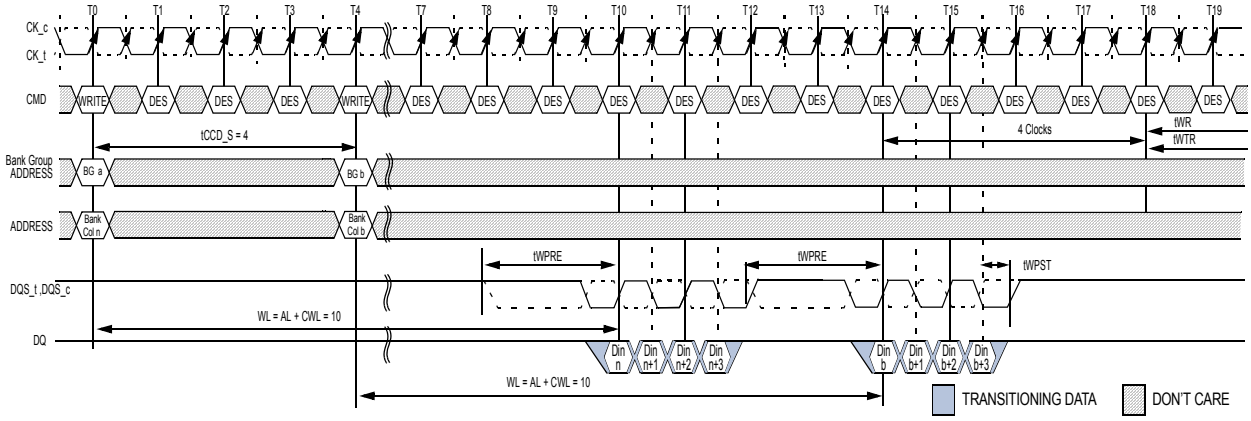
Figure 110 — Nonconsecutive WRITE (BL8) with 2tCK Preamble in Same or Different Bank Group



NOTE:

1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17.

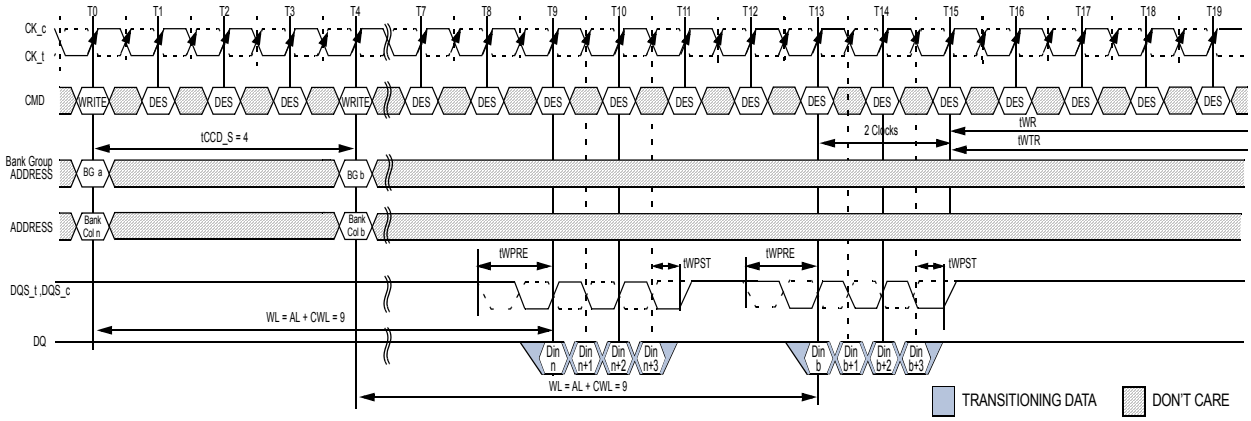
Figure 111 — WRITE (BC4) OTF to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



NOTE:

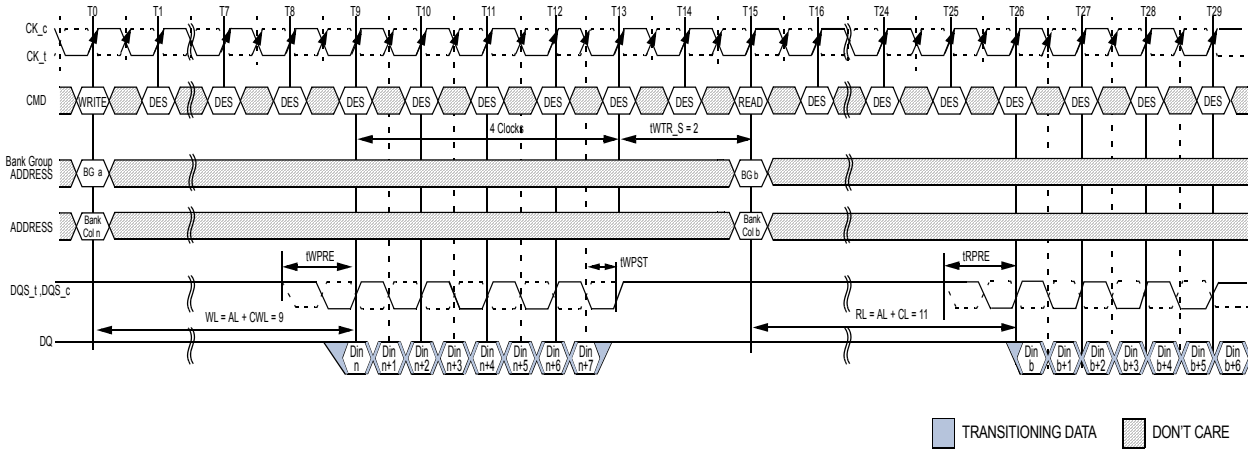
1. BC = 4, AL = 0, CWL = 9 + 1 = 10^7 , Preamble = 2tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18.
7. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range.That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode.

Figure 112 — WRITE (BC4) OTF to WRITE (BC4) OTF with 2tCK Preamble in Different Bank Group



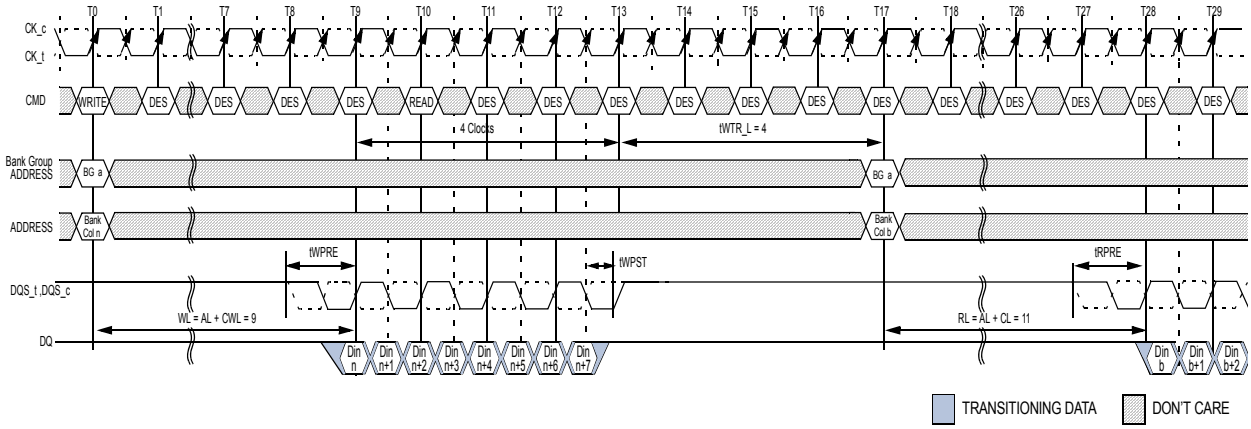
NOTE:
1. BC = 4, AL = 0, CWL = 9 , Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T15.

Figure 113 — WRITE (BC4) Fixed to WRITE (BC4) Fixed with 1tCK Preamble in Different Bank Group



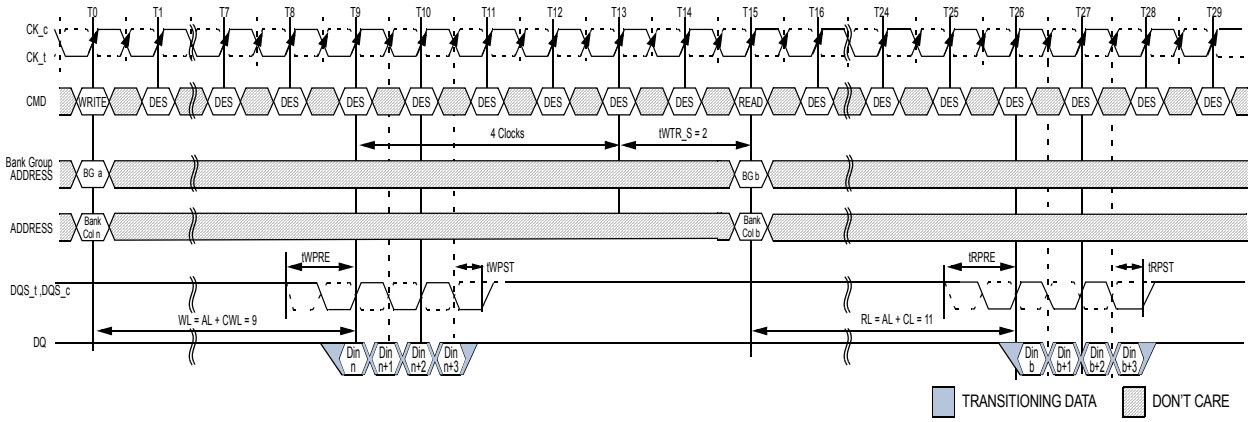
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n(or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 114 — WRITE (BL8) to READ (BL8) with 1tCK Preamble in Different Bank Group



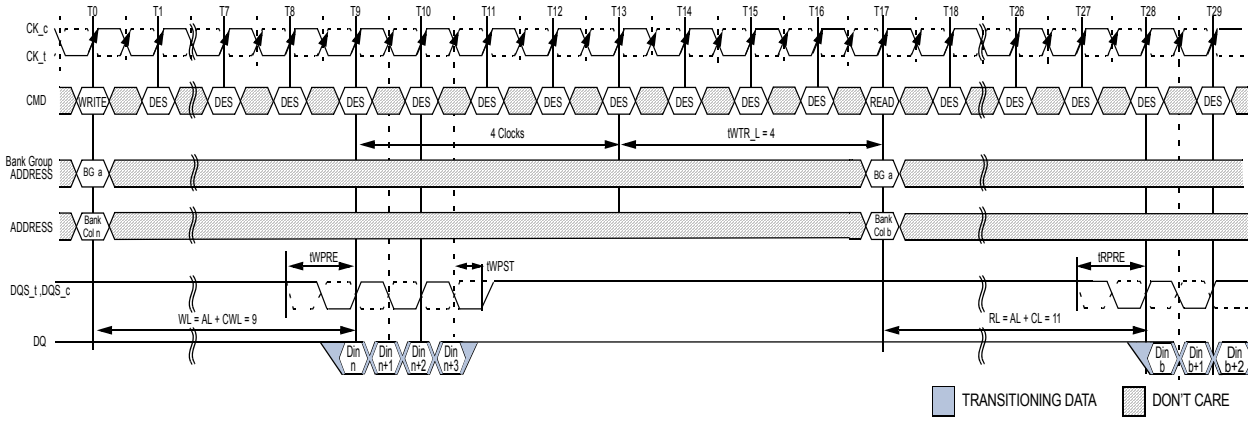
NOTE:
1. BL = 8, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 115 — WRITE (BL8) to READ (BL8) with 1tCK Preamble in Same Bank Group



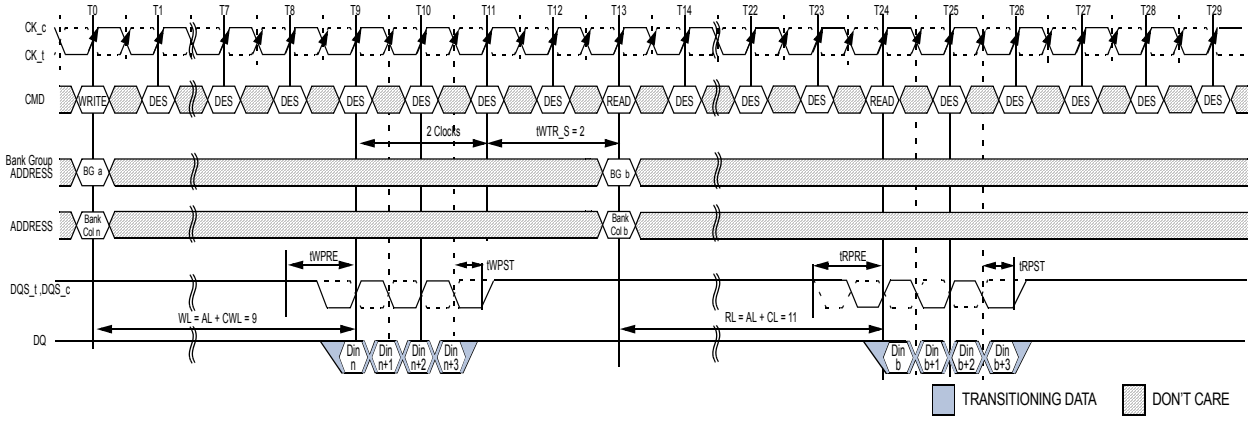
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T15.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 116 — WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Different Bank Group



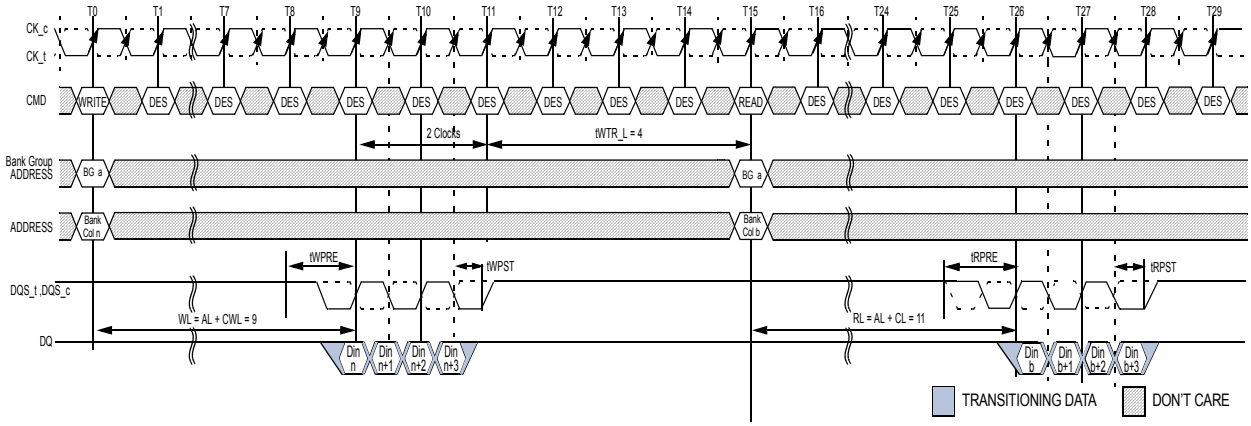
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and READ command at T17.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 117 — WRITE (BC4)OTF to READ (BC4)OTF with 1tCK Preamble in Same Bank Group



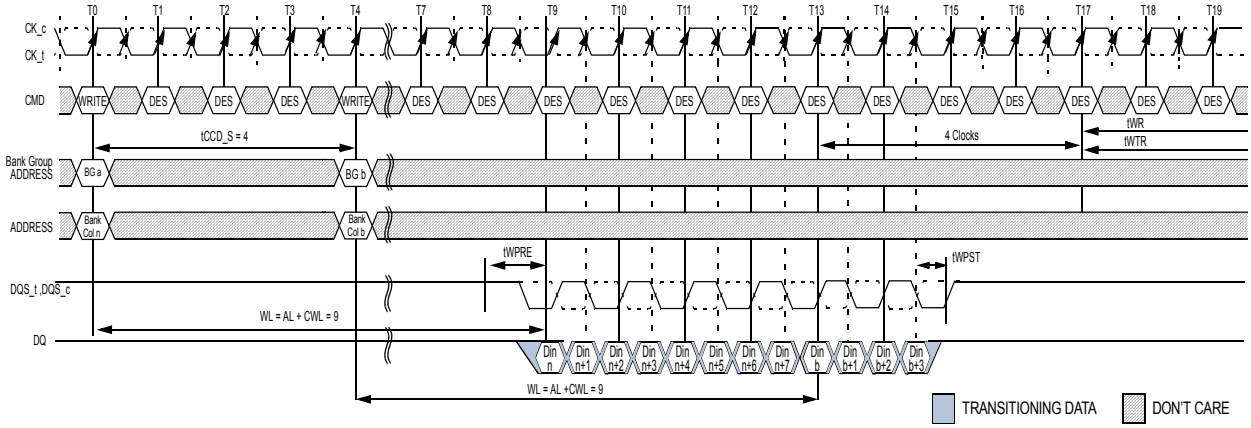
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_S) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 118 — WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Different Bank Group



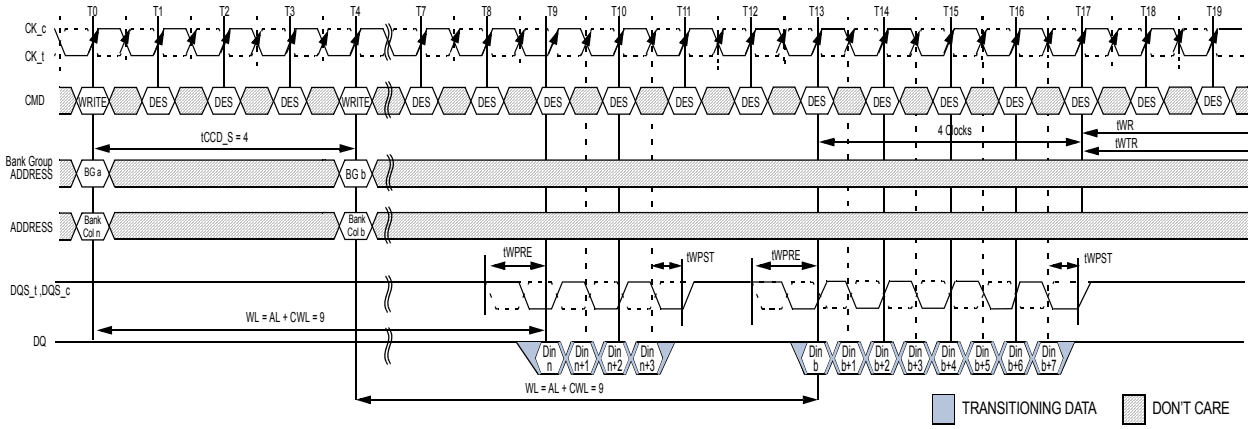
NOTE:
1. BC = 4, AL = 0, CWL = 9, CL = 11, Preamble = 1tCK
2. DIN n = data-in to column n (or column b). DOUT b = data-out from column b.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write timing parameter (tWTR_L) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 119 — WRITE (BC4)Fixed to READ (BC4)Fixed with 1tCK Preamble in Same Bank Group



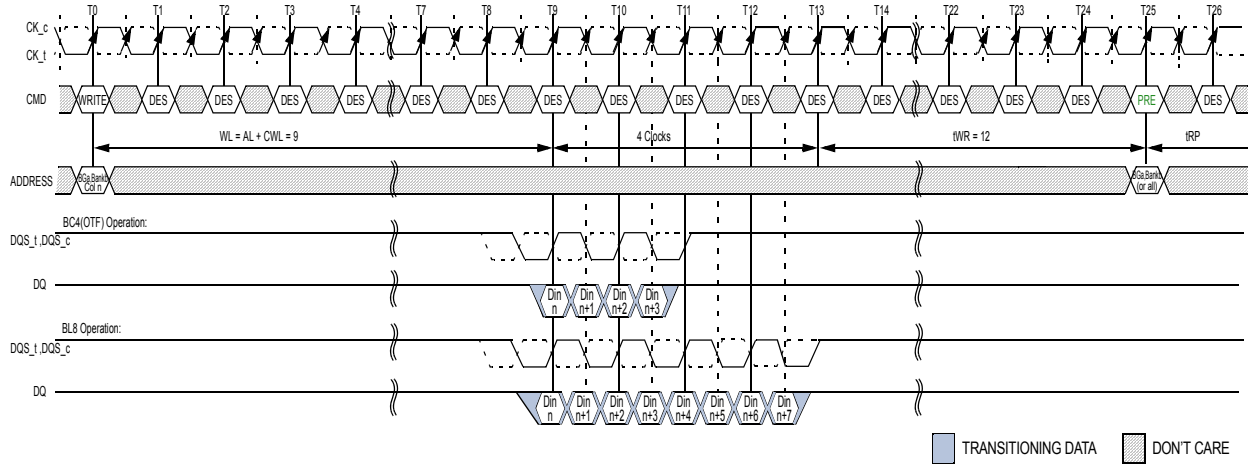
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
   BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

Figure 120 — WRITE (BL8) to WRITE (BC4) OTF with 1tCK Preamble in Different Bank Group



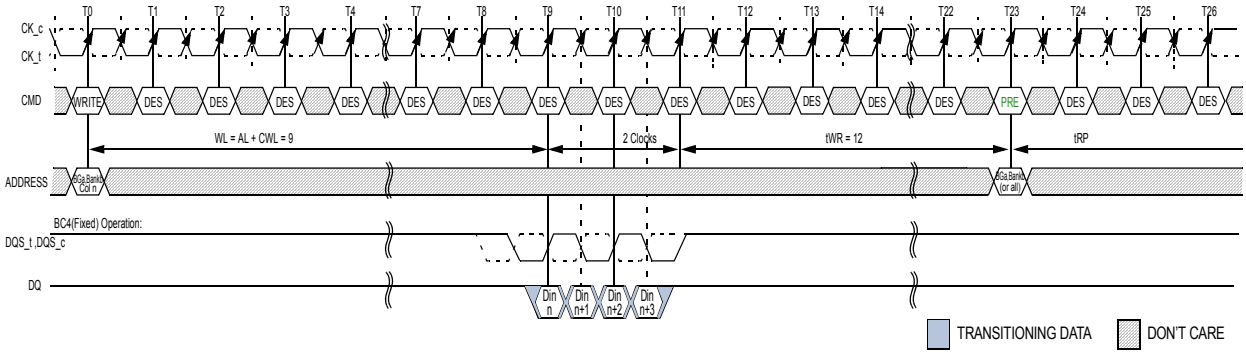
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T4.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T17

Figure 121 — WRITE (BC4)OTF to WRITE (BL8) with 1tCK Preamble in Different Bank Group



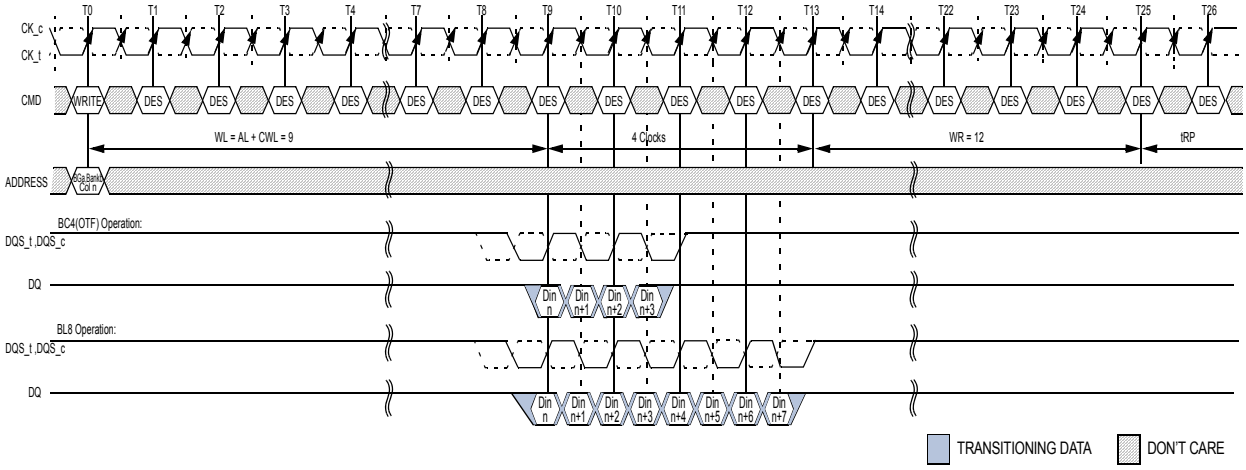
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by MR0[A1:A0 = 0:0] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T13.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 122 — WRITE (BL8/BC4) OTF to PRECHARGE Operation with 1tCK Preamble



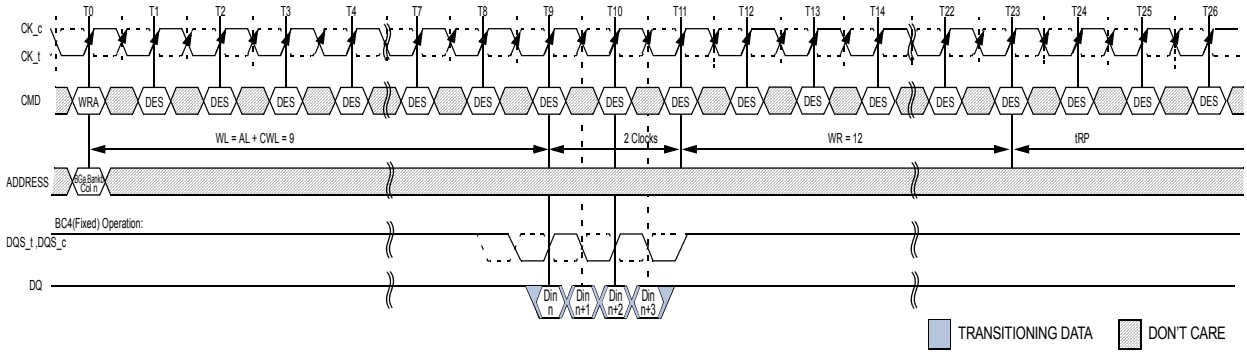
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tWR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   tWR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 123 — WRITE (BC4) Fixed to PRECHARGE Operation with 1tCK Preamble



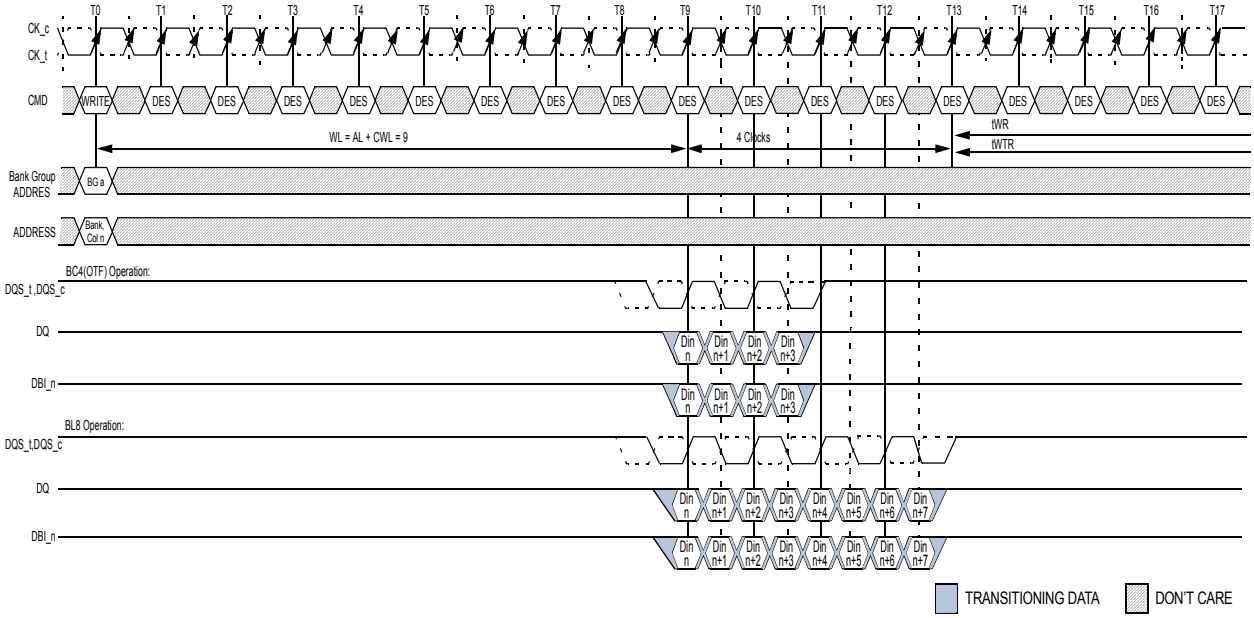
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (WR) is referenced from the first rising clock edge after the last write data shown at T13.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 124 — WRITE (BL8/BC4) OTF with Auto PRECHARGE Operation and 1tCK Preamble



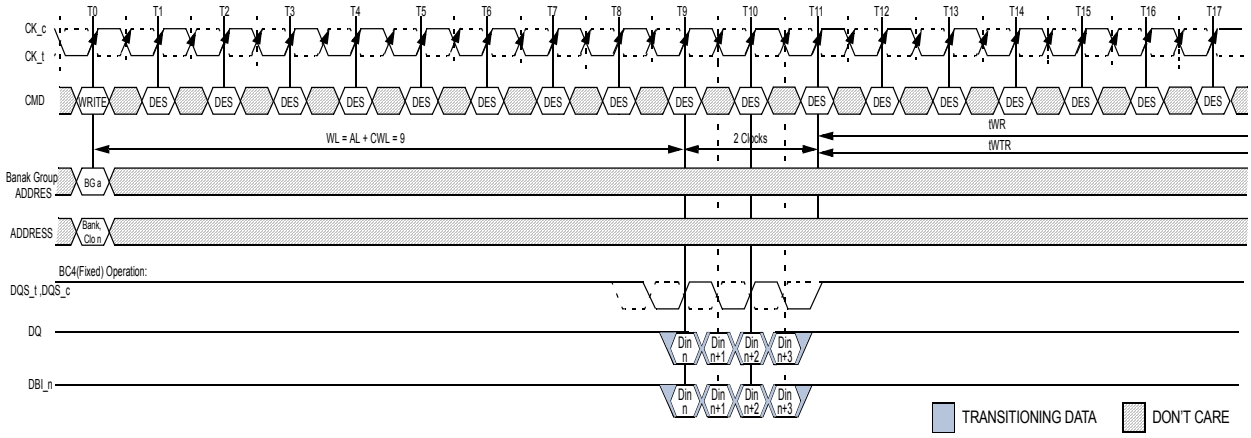
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, WR = 12
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) is referenced from the first rising clock edge after the last write data shown at T11.
   WR specifies the last burst write cycle until the precharge command can be issued to the same bank.

Figure 125 — WRITE (BC4) Fixed with Auto PRECHARGE Operation and 1tCK Preamble



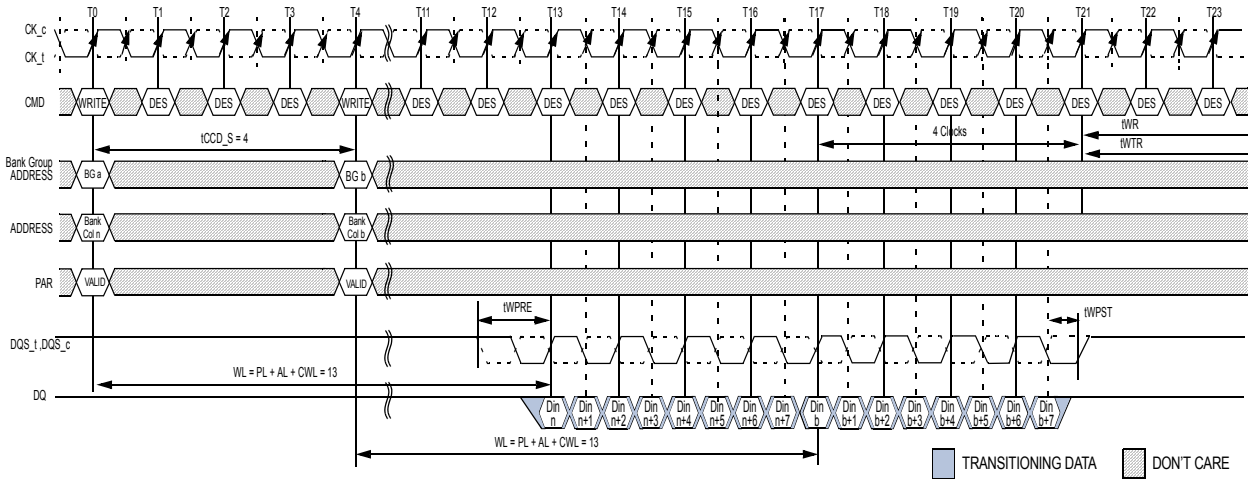
NOTE:
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0.
   BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 126 — WRITE (BL8/BC4) OTF with 1tCK Preamble and DBI



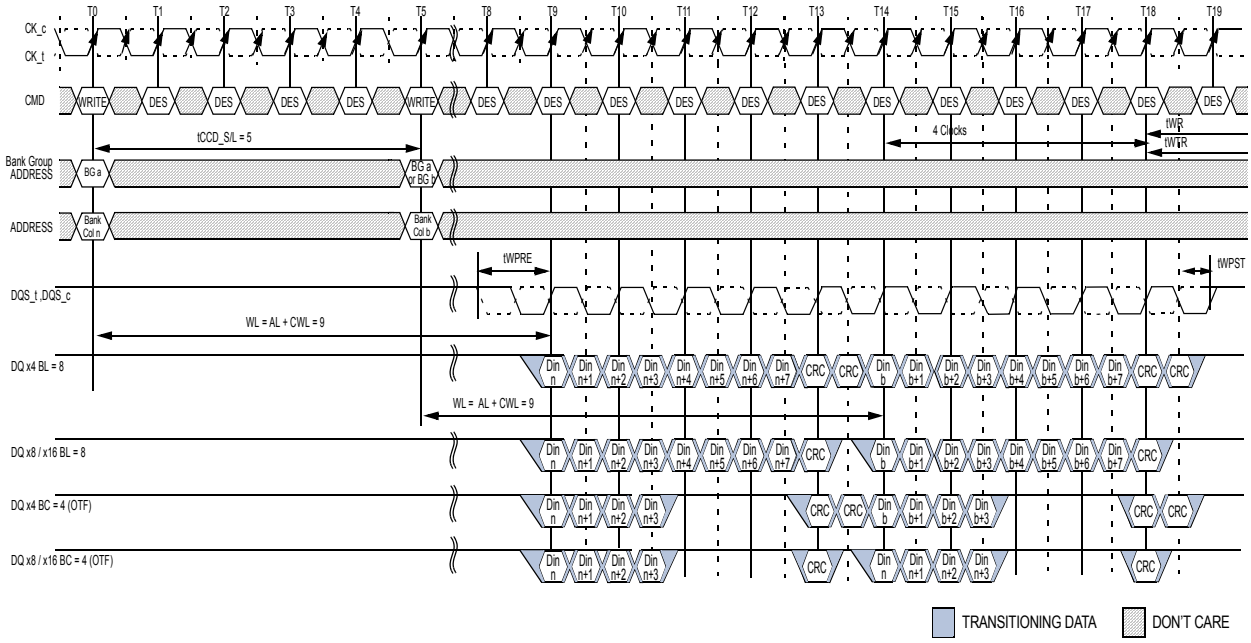
NOTE:
1. BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BC4 setting activated by MR0[A1:A0 = 1:0].
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Enable, CRC = Disable.
6. The write recovery time (tWR_DBI) and write timing parameter (tWTR_DBI) are referenced from the first rising clock edge after the last write data shown at T11.

Figure 127 — WRITE (BC4) Fixed with 1tCK Preamble and DBI



NOTE:
1. BL = 8, AL = 0, CWL = 9, PL = 4, Preamble = 1tCK
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T4.
5. CA Parity = Enable, CS to CA Latency = Disable, Write DBI = Disable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.

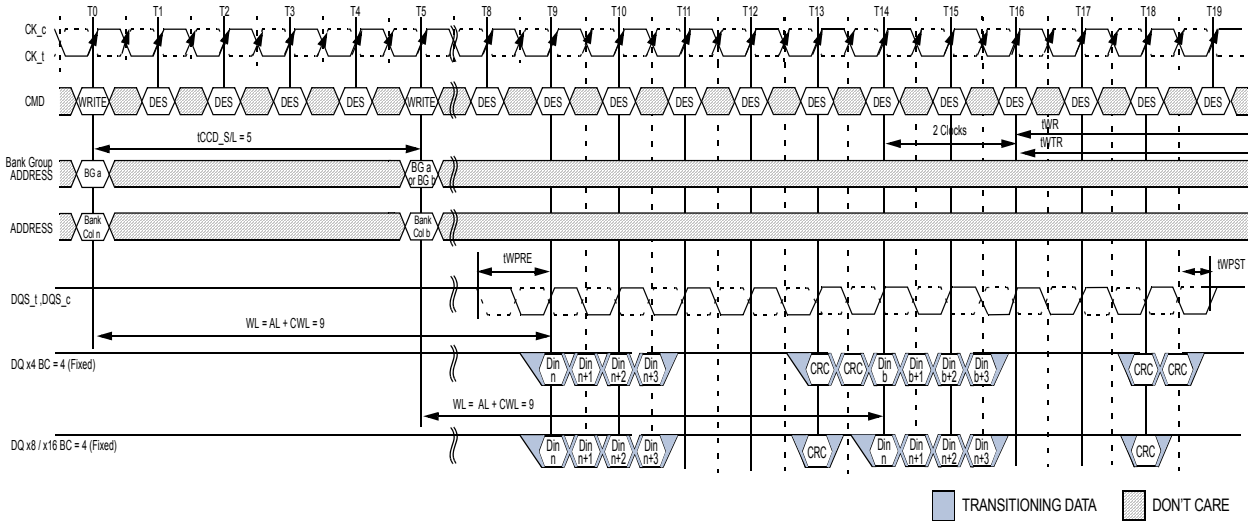
Figure 128 — Consecutive WRITE (BL8) with 1tCK Preamble and CA Parity in Different Bank Group



NOTE:

1. BL = 8/BC = 4, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n (or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:0 = 00] or MR0[A1:0 = 01] and A12 = 1 during WRITE command at T0 and T5.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 = 0 during WRITE command at T0 and T5.
6. C/A Parity = Disable, CS to C/A Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T18

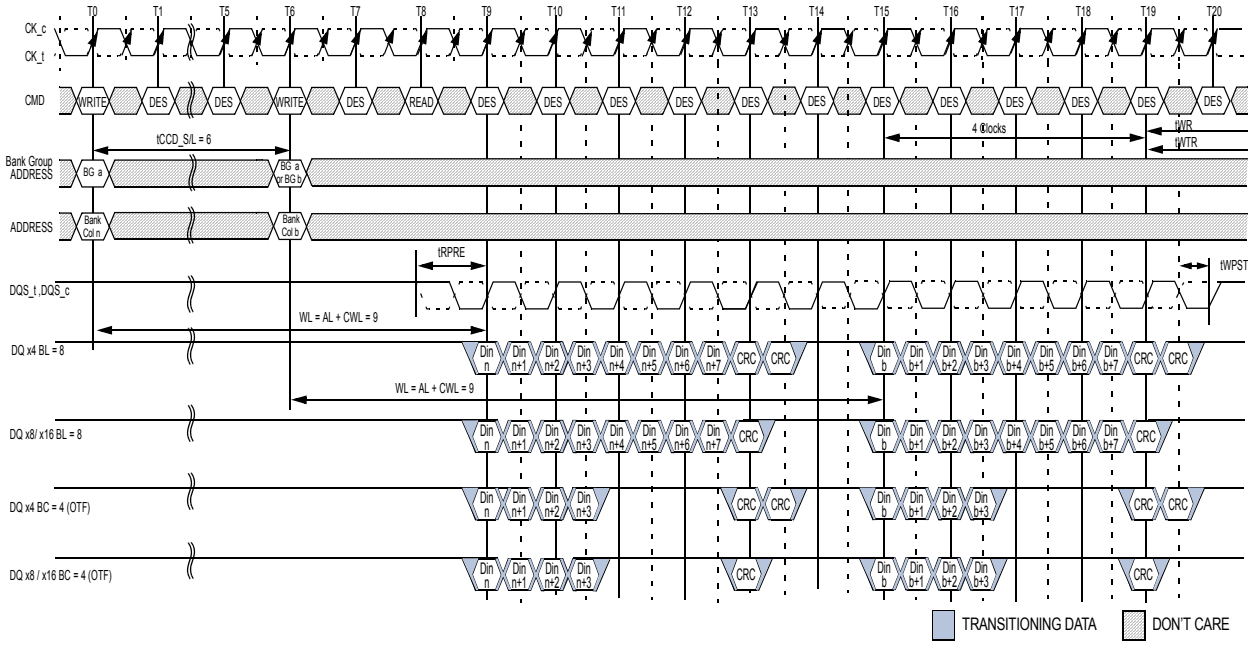
Figure 129 — Consecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 5
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by MR0[A1:A0 = 1:0] at T0 and T5.
5. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, CRC = Enable.
6. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T16.

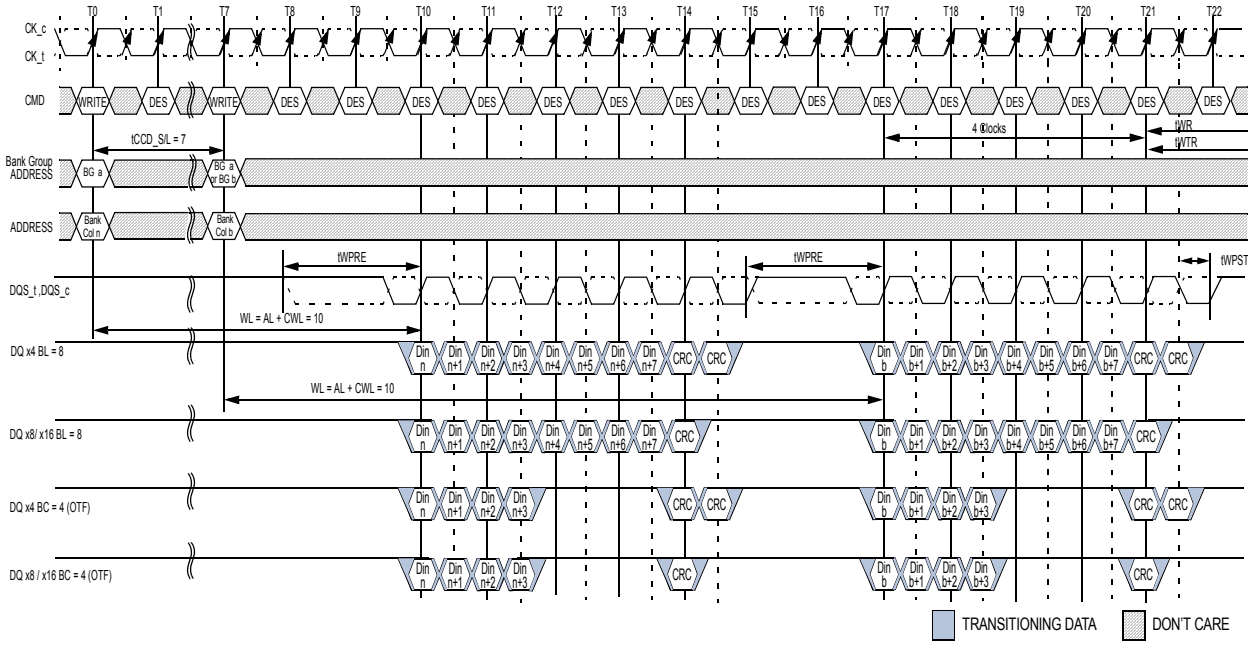
Figure 130 — Consecutive WRITE (BC4)Fixed with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8, AL = 0, CWL = 9, Preamble = 1tCK, tCCD_S/L = 6
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1A:0 = 0:0] or MR0[A1A:0 = 0:1] and A12 =1 during WRITE command at T0 and T6.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T6.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T19.

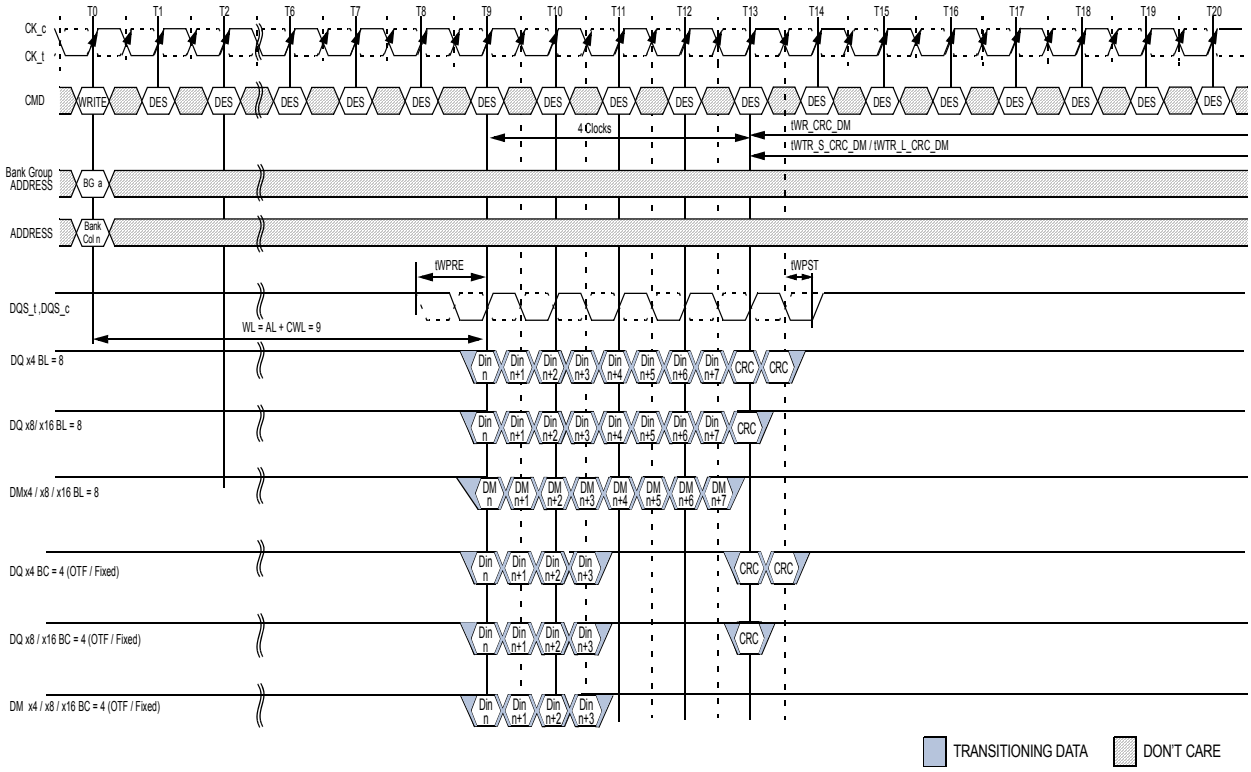
Figure 131 — Nonconsecutive WRITE (BL8/BC4)OTF with 1tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

1. BL = 8, AL = 0, CWL = 9 + 1 = 10[9], Preamble = 2tCK, tCCD_S/L = 7
2. DIN n (or b) = data-in to column n(or column b).
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 =1 during WRITE command at T0 and T7.
5. BC4 setting activated by MR0[A1:A0 = 0:1] and A12 =0 during WRITE command at T0 and T7.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable.
7. tCCD_S/L = 6 isn't allowed in 2tCK preamble mode.
8. The write recovery time (tWR) and write timing parameter (tWTR) are referenced from the first rising clock edge after the last write data shown at T21.
9. When operating in 2tCK Write Preamble Mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable tCK range. That means CWL = 9 is not allowed when operating in 2tCK Write Preamble Mode

Figure 132 — Nonconsecutive WRITE (BL8/BC4)OTF with 2tCK Preamble and Write CRC in Same or Different Bank Group



NOTE:

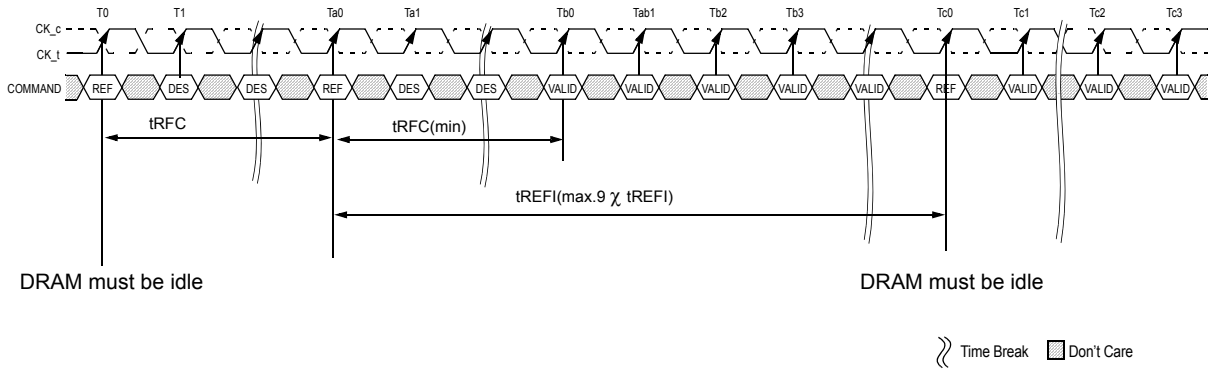
1. BL = 8 / BC = 4, AL = 0, CWL = 9, Preamble = 1tCK
2. DIN n = data-in to column n.
3. DES commands are shown for ease of illustration; other commands may be valid at these times.
4. BL8 setting activated by either MR0[A1:A0 = 0:0] or MR0[A1:A0 = 0:1] and A12 = 1 during WRITE command at T0.
5. BC4 setting activated by either MR0[A1:A0 = 1:0] or MR0[A1:A0 = 0:1] and A12 = 0 during READ command at T0.
6. CA Parity = Disable, CS to CA Latency = Disable, Write DBI = Disable, Write CRC = Enable, DM = Enable.
7. The write recovery time (tWR_CRC_ DM) and write timing parameter (tWR_S_CRC_ DM/tWR_L_CRC_ DM) are referenced from the first rising clock edge after the last write data shown at T13.

Figure 133 — WRITE (BL8/BC4)OTF/Fixed with 1tCK Preamble and Write CRC and DM in Same or Different Bank Group

4.26 Refresh Command

The Refresh command (REF) is used during normal operation of the DDR4 SDRAMs. This command is non persistent, so it must be issued each time a refresh is required. The DDR4 SDRAM requires Refresh cycles at an average periodic interval of tREFI. When CS_n, RAS_n/A16 and CAS_n/A15 are held Low and WE_n/A14 and ACT_n are held High at the rising edge of the clock, the chip enters a Refresh cycle. All banks of the SDRAM must be precharged and idle for a minimum of the precharge time tRP(min) before the Refresh Command can be applied. The refresh addressing is generated by the internal refresh controller. This makes the address bits “Don’t Care” during a Refresh command. An internal address counter supplies the addresses during the refresh cycle. No control of the external address bus is required once this cycle has started. When the refresh cycle has completed, all banks of the SDRAM will be in the precharged (idle) state. A delay between the Refresh Command and the next valid command, except DES, must be greater than or equal to the minimum Refresh cycle time tRFC(min) as shown in Figure X. Note that the tRFC timing parameter depends on memory density.

In general, a Refresh command needs to be issued to the DDR4 SDRAM regularly every tREFI interval. To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided for postponing and pulling-in refresh command. A maximum of 8 Refresh commands can be postponed when DRAM is in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be postponed respectively during operation of the DDR4 SDRAM, meaning that at no point in time more than a total of 8,16,32 Refresh commands are allowed to be postponed for 1X,2X,4X Refresh mode respectively. In case that 8 Refresh commands are postponed in a row, the resulting maximum interval between the surrounding Refresh commands is limited to 9 × tREFI (see Figure 134). In 2X and 4X Refresh mode, it’s limited to 17 x tREFI2 and 33 x tREFI4. A maximum of 8 additional Refresh commands can be issued in advance (“pulled in”) in 1X refresh mode and for 2X/4X refresh mode, 16/32 Refresh commands can be pulled in respectively, with each one reducing the number of regular Refresh commands required later by one. Note that pulling in more than 8/16/32, depending on Refresh mode, Refresh commands in advance does not further reduce the number of regular Refresh commands required later, so that the resulting maximum interval between two surrounding Refresh commands is limited to 9 × tREFI , 17 x tRFEI2 and 33 x tREFI4 respectively. At any given time, a maximum of 16 REF/ 32REF 2/64REF 4 commands can be issued within 2 x tREFI/ 4 x tREFI2/ 8 x tREFI4



NOTE : 1. Only DES commands allowed after Refresh command registered untill tRFC(min) expires.
2. Time interval between two Refresh commands may be extended to a maximum of 9 X tREFI.

Figure 134 — Refresh Command Timing (Example of 1x Refresh mode)

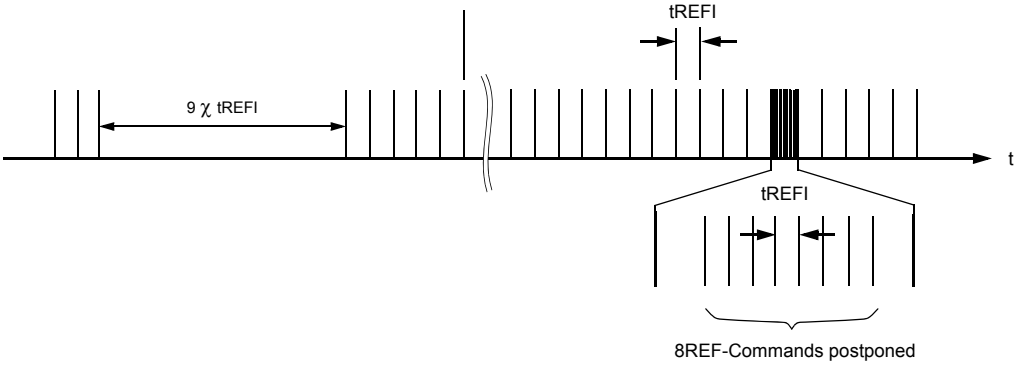


Figure 135 — Postponing Refresh Commands (Example of 1X Refresh mode)

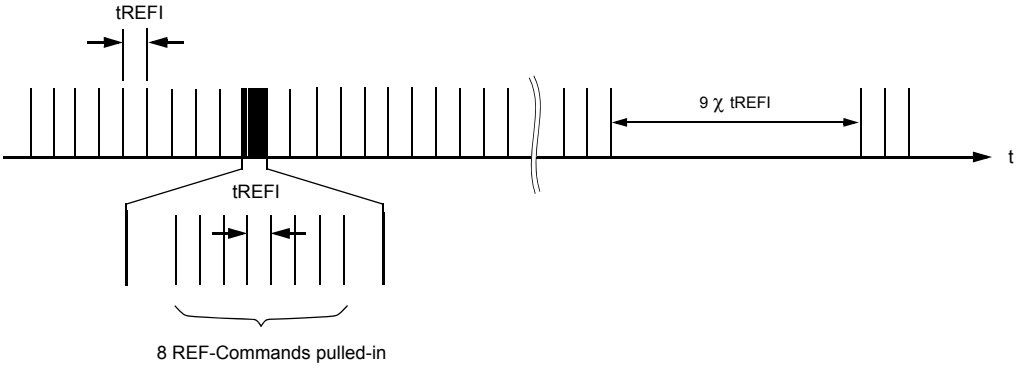


Figure 136 — Pulling-in Refresh Commands (Example of 1X Refresh mode)

4.27 Self refresh Operation

The Self-Refresh command can be used to retain data in the DDR4 SDRAM, even if the rest of the system is powered down. When in the Self-Refresh mode, the DDR4 SDRAM retains data without external clocking.The DDR4 SDRAM device has a built-in timer to accommodate Self-Refresh operation. The Self-Refresh-Entry (SRE) Command is defined by having CS_n, RAS_n/A16, CAS_n/A15, and CKE held low with WE_n/A14 and ACT_n high at the rising edge of the clock.

Before issuing the Self-Refresh-Entry command, the DDR4 SDRAM must be idle with all bank precharge state with tRP satisfied. 'Idle state' is defined as all banks are closed (tRP, tDAL, etc. satisfied), no data bursts are in progress, CKE is high, and all timings from previous operations are satisfied (tMRD, tMOD,tRFC, tZQinit, tZQoper, tZQCS, etc.). Deselect command must be registered on last positive clock edge before issuing Self Refresh Entry command. Once the Self Refresh Entry command is registered, Deselect command must also be registered at the next positive clock edge. Once the Self-Refresh Entry command is registered, CKE must be held low to keep the device in Self-Refresh mode. .DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of ODT pin and RTT_PARK set when it enters in Self-Refresh mode. Upon exiting Self-Refresh, DRAM automatically enables ODT termination and set RTT_PARK asynchronously during tXSDLL when RTT_PARK is enabled. During normal operation (DLL on) the DLL is automatically disabled upon entering Self-Refresh and is automatically enabled (including a DLL-Reset) upon exiting Self-Refresh.

When the DDR4 SDRAM has entered Self-Refresh mode, all of the external control signals, except CKE and RESET_n, are "don't care." For proper Self-Refresh operation, all power supply and reference pins (VDD, VDDQ, VSS, VSSQ, VPP, and VRefCA) must be at valid levels. DRAM internal VrefDQ generator circuitry may remain ON or turned OFF depending on DRAM design. If DRAM internal VrefDQ circuitry is turned OFF in self refresh, when DRAM exits from self refresh state, it ensures that VrefDQ generator circuitry is powered up and stable within tXS period. First Write operation or first Write Leveling Activity may not occur earlier than tXS after exit from Self Refresh. The DRAM initiates a minimum of one Refresh command internally within tCKE period once it enters Self-Refresh mode.

The clock is internally disabled during Self-Refresh Operation to save power. The minimum time that the DDR4 SDRAM must remain in Self-Refresh mode is tCKESR. The user may change the external clock frequency or halt the external clock tCKSRE after Self-Refresh entry is registered, however, the clock must be restarted and stable tCKSRX before the device can exit Self-Refresh operation.

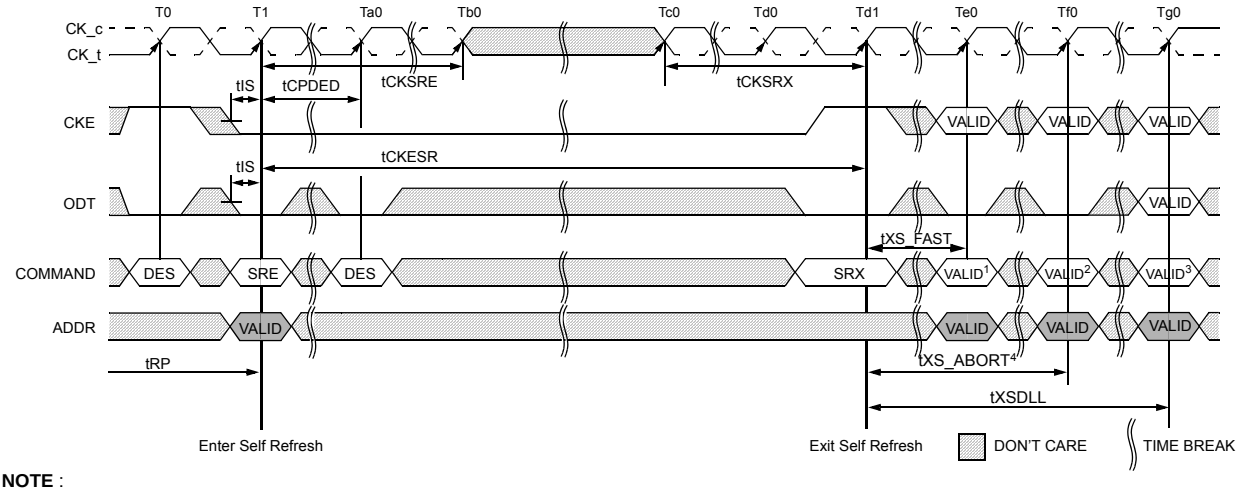
The procedure for exiting Self-Refresh requires a sequence of events. First, the clock must be stable prior to CKE going back HIGH. Once a Self-Refresh Exit command (SRX, combination of CKE going high and Deselect on command bus) is registered, following timing delay must be satisfied:

1. Commands that do not require locked DLL:
tXS - ACT, PRE, PREA, REF, SRE, PDE, WR, WRS4, WRS8, WRA, WRAS4, WRAS8, tXSFast - ZQCL, ZQCS, MRS commands.
For MRS command, only DRAM CL and WR/RTP register in MR0, CWL register in MR2 and geardown mode in MR3 are allowed to be accessed provided DRAM is not in per DRAM addressability mode. Access to other DRAM mode registers must satisfy tXS timing.
Note that synchronous ODT for write commands (WR, WRS4, WRS8, WRA, WRAS4 and WRAS8) and dynamic ODT controlled by write command require locked DLL.

2. Commands that require locked DLL:
tXSDLL - RD, RDS4, RDS8, RDA, RDAS4, RDAS8
Depending on the system environment and the amount of time spent in Self-Refresh, ZQ calibration commands may be required to compensate for the voltage and temperature drift as described in “ZQ Calibration Commands” on Section 4.12. To issue ZQ calibration commands, applicable timing requirements must be satisfied.

CKE must remain HIGH for the entire Self-Refresh exit period tXSDLL for proper operation except for Self-Refresh re-entry. Upon exit from Self-Refresh, the DDR4 SDRAM can be put back into Self-Refresh mode or Power down mode after waiting at least tXS period and issuing one refresh command (refresh period of tRFC). Deselect commands must be registered on each positive clock edge during the Self-Refresh exit interval tXS. Low level of ODT pin must be registered on each positive clock edge during tXSDLL when normal mode (DLL-on) is set. Under DLL-off mode, asynchronous ODT function might be allowed.
The use of Self-Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self-Refresh mode. Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode.

The exit timing from self-refresh exit to first valid command not requiring a locked DLL is tXS.
The value of tXS is (tRFC+10ns). This delay is to allow for any refreshes started by the DRAM to complete. tRFC continues to grow with higher density devices so tXS will grow as well.
A Bit A9 in MR4 is defined to enable the self refresh abort mode. If the bit is disabled then the controller uses tXS timings.
If the bit is enabled then the DRAM aborts any ongoing refresh and does not increment the refresh counter. The controller can issue a valid command not requiring a locked DLL after a delay of tXS_abort.
Upon exit from Self-Refresh, the DDR4 SDRAM requires a minimum of one extra refresh command before it is put back into Self-Refresh Mode. This requirement remains the same irrespective of the setting of the MRS bit for self refresh abort.
.



NOTE :
1. Only MRS (limited to those described in the Self-Refresh Operation section). ZQCS or ZQCL command allowed.
2. Valid commands not requiring a locked DLL
3. Valid commands requiring a locked DLL
4. Only DES is allowed during tXS_ABORT

Figure 137 — Self-Refresh Entry/Exit Timing

4.27.1 Low Power Auto Self Refresh

DDR4 devices support Low Power Auto Self-Refresh (LP ASR) operation at multiple temperatures ranges (See temperature table below). Mode Register MR2 – descriptions

Table 47 — MR2 definitions for Low Power Auto Self-Refresh mode

A6	A7	Self-Refresh Operation Mode
0	0	Manual Mode – Normal operating temperature range
0	1	Manual Mode – Extended operating temperature range
1	0	Manual Mode – Lower power mode at a reduced operating temperature range
1	1	ASR Mode – automatically switching between all modes to optimize power for any of the temperature ranges listed above

Auto Self Refresh (ASR)
DDR4 DRAM provides an Auto Self-Refresh mode (ASR) for application ease. ASR mode is enabled by setting the above MR2 bits A6=1 and A7=1. The DRAM will manage Self Refresh entry through the supported temperature range of the DRAM. In this mode, the DRAM will change self-refresh rate as the DRAM operating temperature changes, lower at low temperatures and higher at high temperatures.

Manual Modes
If ASR mode is not enabled, the LP ASR Mode Register must be manually programmed to one the three self-refresh operating modes listed above. In this mode, the user has the flexibility to select a fixed self-refresh operating mode at the entry of the self-refresh according to their system memory temperature conditions. The user is responsible to maintain the required memory temperature condition for the mode selected during the self-refresh operation. The user may change the selected mode after exiting from self refresh and before the next self-refresh entry. If the temperature condition is exceeded for the mode selected, there is risk to data retention resulting in loss of data.

Table 48 — Self Refresh Function table

MR2-A6	MR2-A7	LP ASR Mode	Self Refresh Operation	Allowed Operating Temperature Range for Self Refresh Mode (all reference to DRAM Tcase)
0	0	Normal	Fixed normal self-Refresh rate to maintain data retention for the normal operating temperature. User is required to ensure 85°C DRAM Tcasemax is not exceeded to avoid any risk of data loss.	(0°C – 85°C)
0	1	Extended Temperature range	Fixed high self-Refresh rate to optimize data retention to support the extended temperature range	(0°C – 95°C)
1	0	Reduced Temperature range	Variable or fixed self-Refresh rate or any other DRAM power consumption reduction control for the reduced temperature range. User is required to ensure 45°C DRAM Tcasemax is not exceeded to avoid any risk of data loss .	(0°C – 45°C)
1	1	Auto Self Refresh	ASR Mode Enabled. Self-Refresh power consumption and data retention are optimized for any given operating temperature conditions	All of the above

4.28 Power down Mode

4.28.1 Power-Down Entry and Exit

Power-down is synchronously entered when CKE is registered low (along with Deselect command). CKE is not allowed to go low while mode register set command, MPR operations, ZQCAL operations, DLL locking or read / write operation are in progress. CKE is allowed to go low while any of other operations such as row activation, precharge or auto-precharge and refresh are in progress, but power-down IDD spec will not be applied until finishing those operations. Timing diagrams are shown in Figure 139 through Figure 147 with details for entry and exit of Power-Down.

The DLL should be in a locked state when power-down is entered for fastest power-down exit timing. If the DLL is not locked during power-down entry, the DLL must be reset after exiting power-down mode for proper read operation and synchronous ODT operation. DRAM design provides all AC and DC timing and voltage specification as well as proper DLL operation with any CKE intensive operations as long as DRAM controller complies with DRAM specifications.

During Power-Down, if all banks are closed after any in-progress commands are completed, the device will be in precharge Power-Down mode; if any bank is open after in-progress commands are completed, the device will be in active Power-Down mode.

Entering power-down deactivates the input and output buffers, excluding CK_t, CK_c, CKE and RESET_n. In power-down mode, DRAM ODT input buffer deactivation is based on MR5 bit A5. If it is configured to 0b, ODT input buffer remains on and ODT input signal must be at valid logic level. If it is configured to 1b, ODT input buffer is deactivated and DRAM ODT input signal may be floating and DRAM does not provide Rtt_Nom termination. Note that DRAM continues to provide Rtt_Park termination if it is enabled in DRAM mode register MR5 bit A8:A6 To protect DRAM internal delay on CKE line to block the input signals, multiple Deselect commands are needed during the CKE switch off and cycle(s) after, this timing period are defined as tCPDED. CKE_low will result in deactivation of command and address receivers after tCPDED has expired.

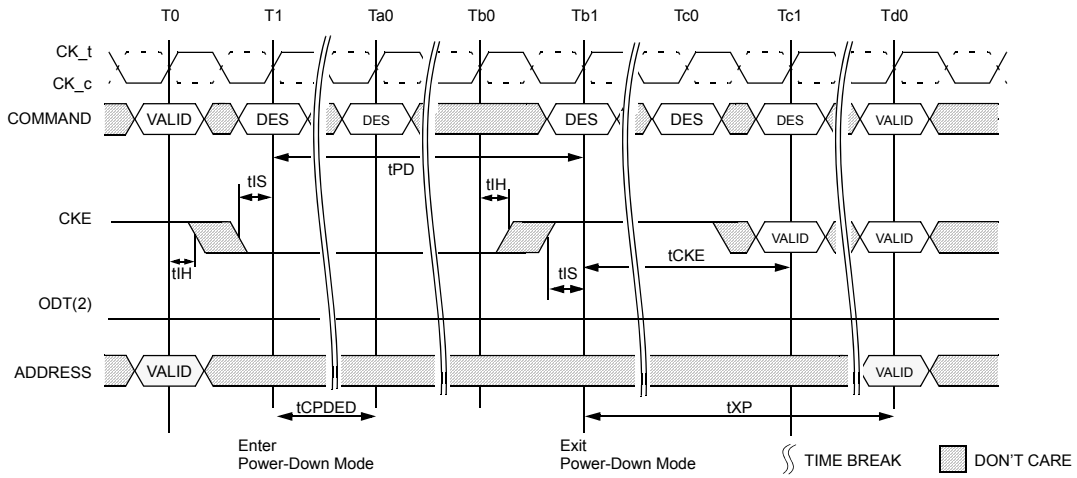
Table 49 — Power-Down Entry Definitions

Status of DRAM	DLL	PD Exit	Relevant Parameters
Active (A bank or more Open)	On	Fast	tXP to any valid command
Precharged (All banks Precharged)	On	Fast	tXP to any valid command.

Also, the DLL is kept enabled during precharge power-down or active power-down. In power-down mode, CKE low, RESET_n high, and a stable clock signal must be maintained at the inputs of the DDR4 SDRAM, and ODT should be in a valid state, but all other input signals are “Don’t Care.” (If RESET_n goes low during Power-Down, the DRAM will be out of PD mode and into reset state.) CKE low must be maintained until tCKE has been satisfied. Power-down duration is limited by 9 times tREFI of the device.

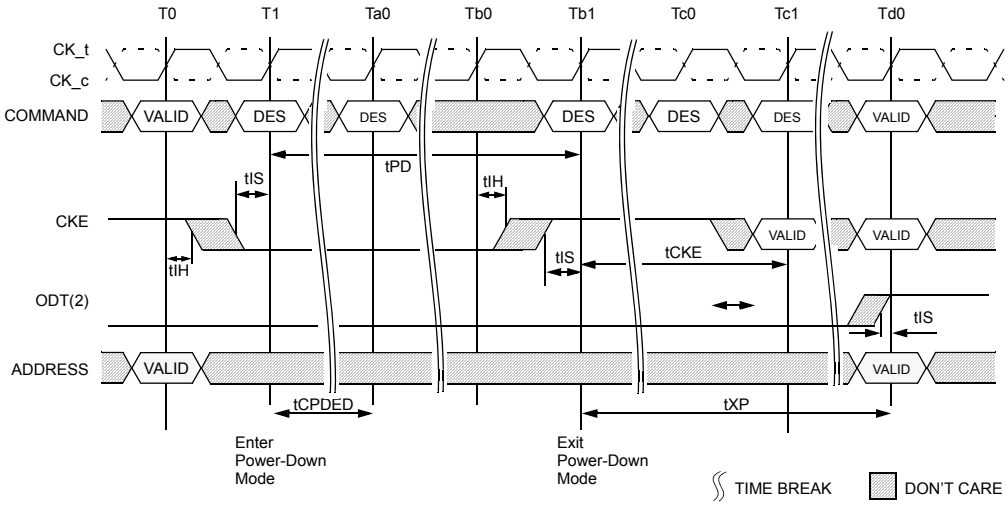
The power-down state is synchronously exited when CKE is registered high (along with a Deselect command). CKE high must be maintained until tCKE has been satisfied. DRAM ODT input signal must be at valid level when DRAM exits from power-down mode independent of MR5 bit A5 if Rtt_Nom is enabled in DRAM mode register. If DRAM Rtt_Nom is disabled then ODT input signal may remain floating. A valid, executable command can be applied with power-down exit latency, tXP after CKE goes high. Power-down exit latency is defined in the AC specifications Table in Section 12.3.

Active Power Down Entry and Exit timing diagram example is shown in Figure 139. Timing Diagrams for CKE with PD Entry, PD Exit with Read and Read with Auto Precharge, Write, Write with Auto Precharge, Activate, Precharge, Refresh, and MRS are shown in Figure 140 through Figure 147. Additional clarification is shown in Figure 148.



NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=0 (default setting) is shown.

Figure 138 — Active Power-Down Entry and Exit Timing Diagram MR5 bit A5 =0



NOTE : 1. VALID command at T0 is ACT, DES or Precharge with still one bank remaining open after completion of the precharge command.
2. ODT pin driven to a valid state. MR5 bit A5=1 is shown.

Figure 139 — Active Power-Down Entry and Exit Timing Diagram MR5 bit A5=1

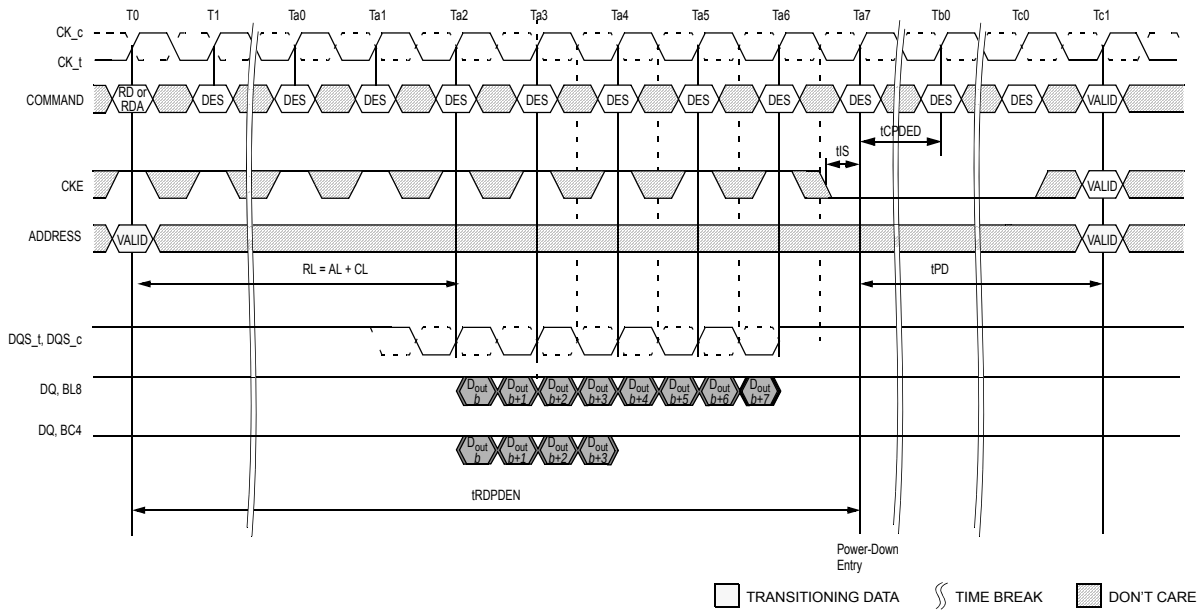
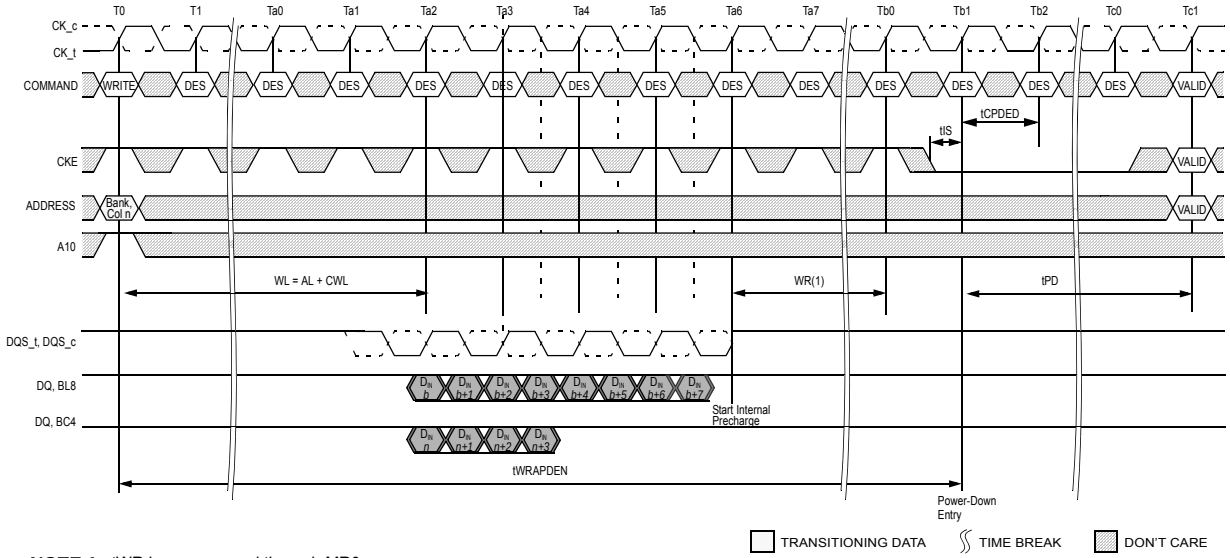


Figure 140 — Power-Down Entry after Read and Read with Auto Precharge



NOTE 1. tWR is programmed through MR0.

Figure 141 — Power-Down Entry After Write with Auto Precharge

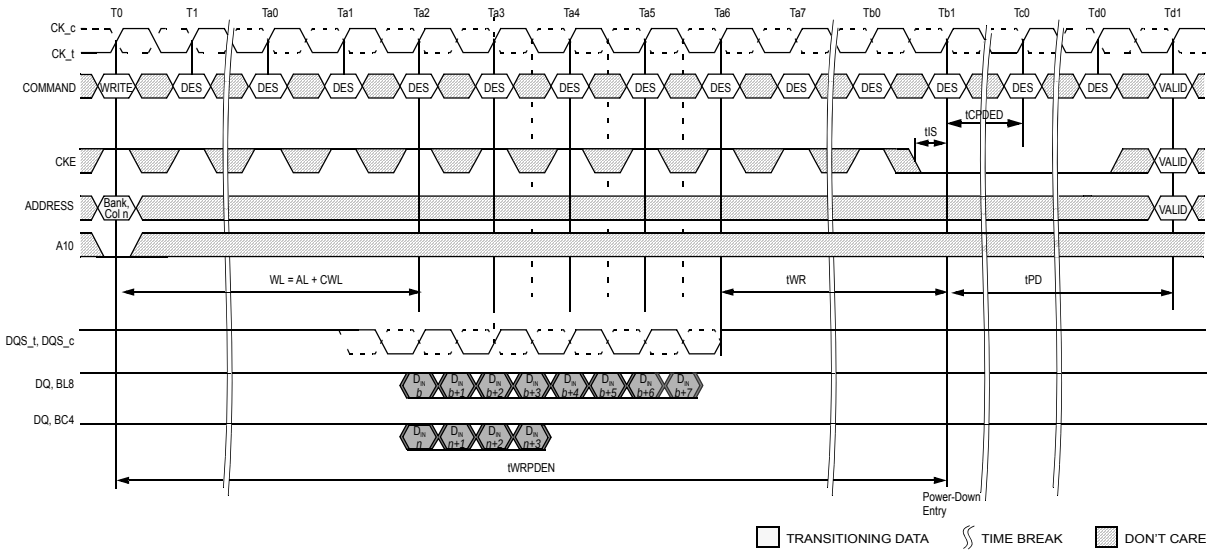


Figure 142 — Power-Down Entry after Write

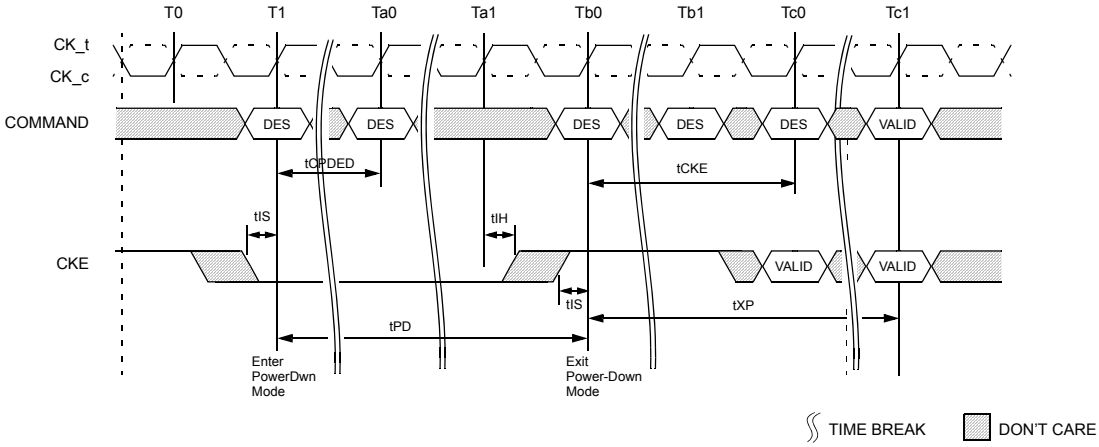


Figure 143 — Precharge Power-Down Entry and Exit

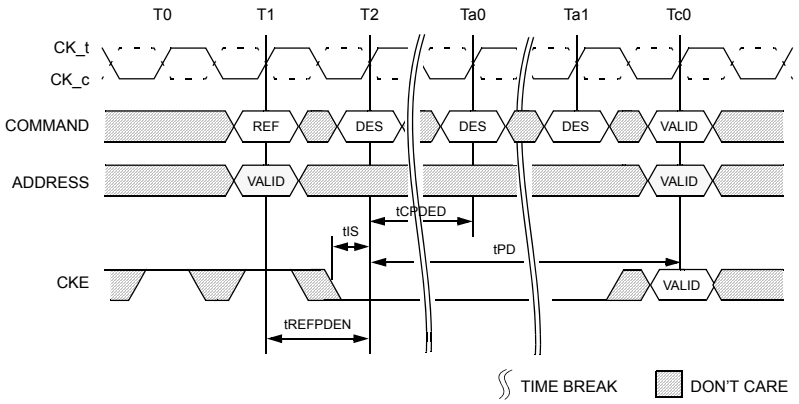


Figure 144 — Refresh Command to Power-Down Entry

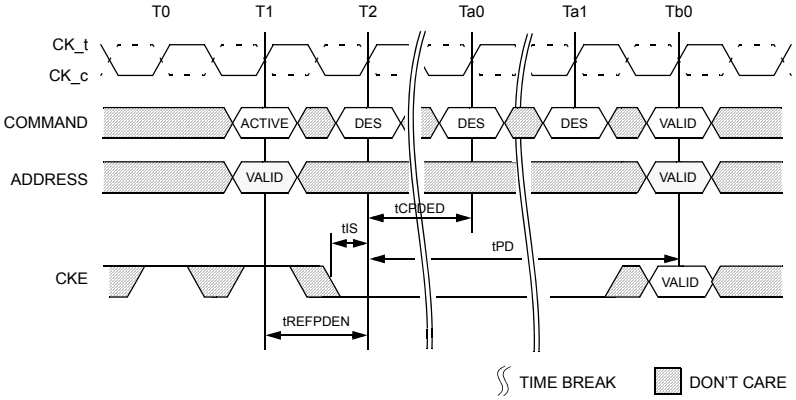


Figure 145 — Activate Command to Power-Down Entry

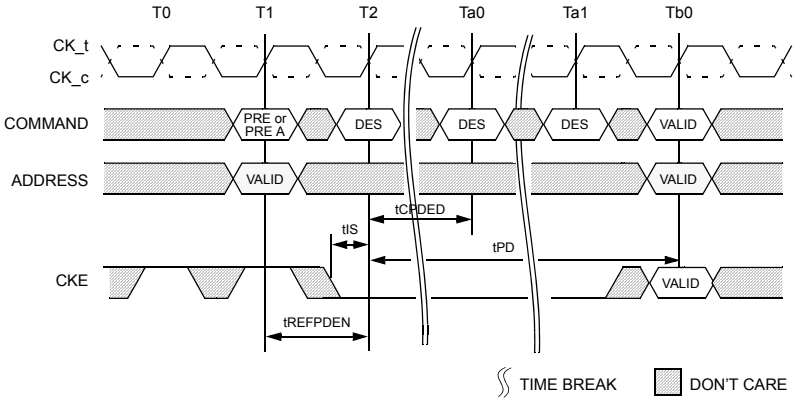


Figure 146 — Precharge/Precharge all Command to Power-Down Entry

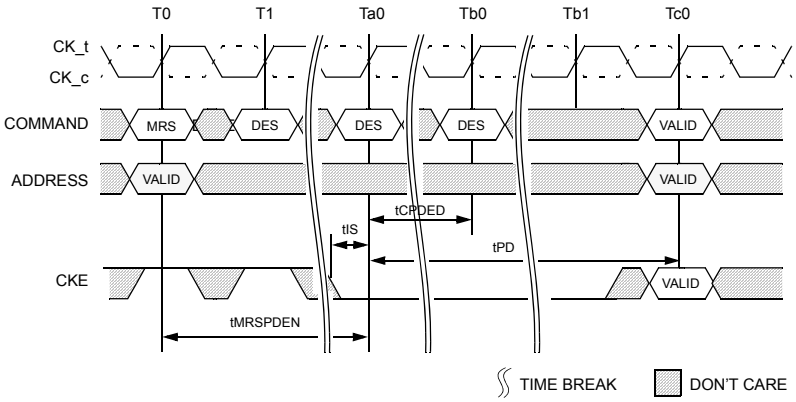


Figure 147 — MRS Command to Power-Down Entry

4.28.2 Power-Down clarifications

When CKE is registered low for power-down entry, tPD(min) must be satisfied before CKE can be registered high for power-down exit. The minimum value of parameter tPD(min) is equal to the minimum value of parameter tCKE(min) as shown in Table "Timing Parameters by Speed Bin". A detailed example of Case1 is shown in Figure 148.

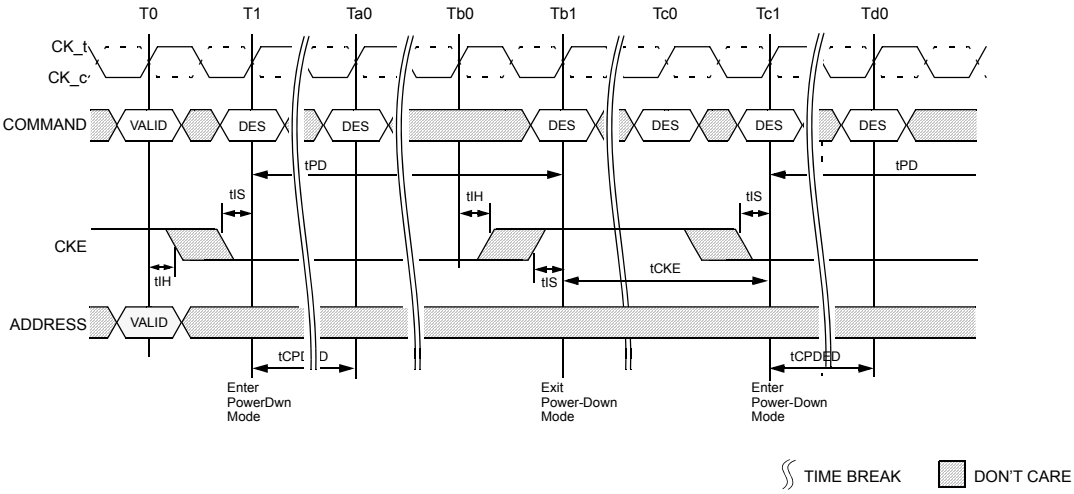


Figure 148 — Power-Down Entry/Exit Clarification

4.29 Maximum Power Saving Mode

4.29.1 Maximum power saving mode

This mode provides lowest power consuming mode which could be similar to the Self-Refresh status with no internal refresh activity. When DDR4 SDRAM is in the maximum power saving mode, it does not need to guarantee data retention nor respond to any external command (except maximum power saving mode exit and asserting RESET_n signal LOW) to minimize the power consumption.

4.29.2 Mode entry

Max power saving mode is entered through an MRS command. For devices with shared control/address signals, a single DRAM device can be entered into the max power saving mode using the per DRAM Addressability MRS command.
Note that large CS_n hold time to CKE upon the mode exit may cause DRAM malfunction, thus it is required that the CA parity, CAL

and Gear Down modes are disabled prior to the max power saving mode entry MRS command.

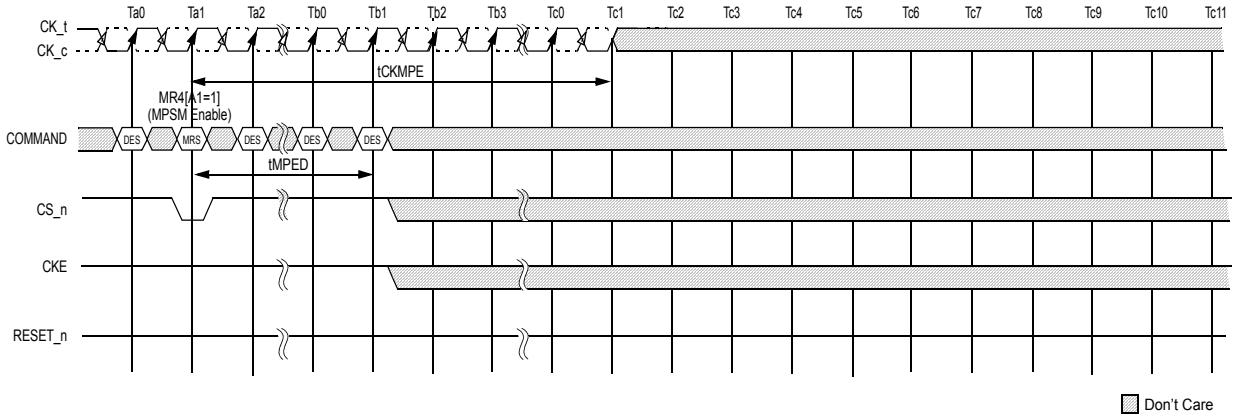


Figure 149 — Maximum Power Saving mode Entry

Figure 150 below illustrates the sequence and timing parameters required for the maximum power saving mode with the per DRAM addressability (PDA).

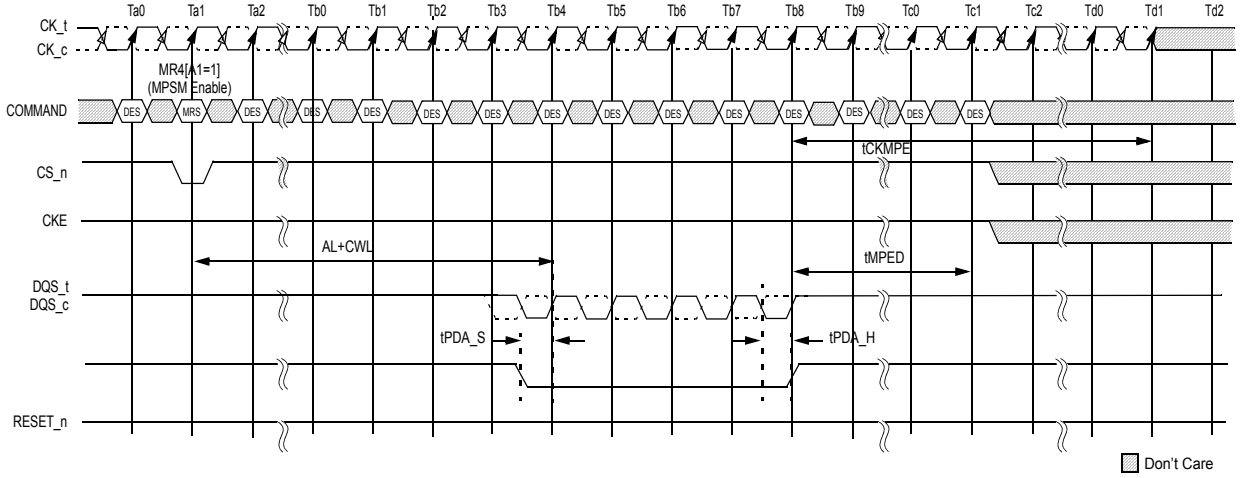


Figure 150 — Maximum Power Saving mode Entry with PDA

When entering Maximum Power Saving mode, only DES commands are allowed until tMPED is satisfied. After tMPED period from the mode entry command, DRAM is not responsive to any input signals except CS_n, CKE and RESET_n signals, and all other input signals can be High-Z. CLK should be valid for tCKMPE period and then can be High-Z.

4.29.3 CKE transition during the mode

CKE toggle is allowed when DRAM is in the maximum power saving mode. To prevent the device from exiting the mode, CS_n should be issued 'High' at CKE 'L' to 'H' edge with appropriate setup tMPX_S and hold tMPX_HH timings.

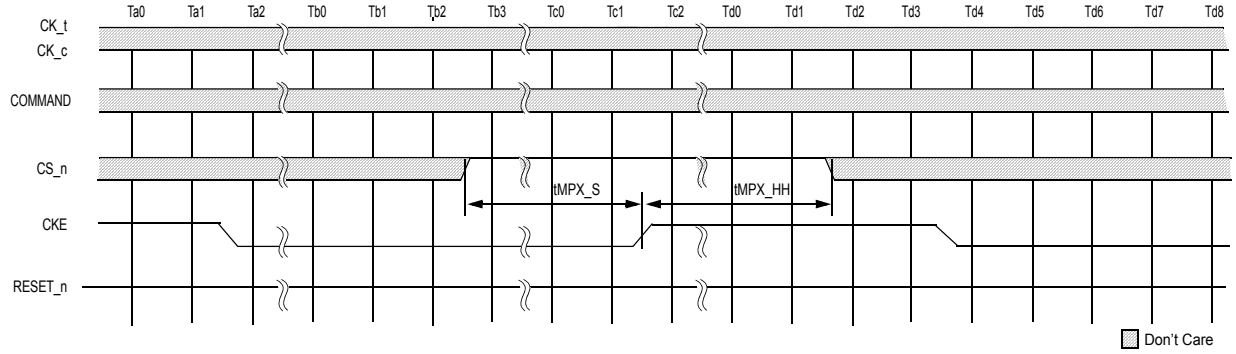


Figure 151 — CKE Transition Limitation to hold Maximum Power Saving Mode

4.29.4 Mode exit

DRAM monitors CS_n signal level and when it detects CKE 'L' to 'H' transition, and either exits from the power saving mode or stay in the mode depending on the CS_n signal level at the CKE transition. Because CK receivers are shut down during this mode, CS_n = 'L' is captured by rising edge of the CKE signal. If CS_n signal level is detected 'L', then the DRAM initiates internal exit procedure from the power saving mode. CK must be restarted and stable tCKMPX period before the device can exit the maximum power saving mode. During the exit time tXMP, any valid commands except DES command is not allowed to DDR4 SDRAM and also tXMP_DLL, any valid commands requiring a locked DLL is not allowed to DDR4 SDRAM.

When recovering from this mode, the DRAM clears the MRS bits of this mode. It means that the setting of MR4 [A1] is move to '0' automatically.

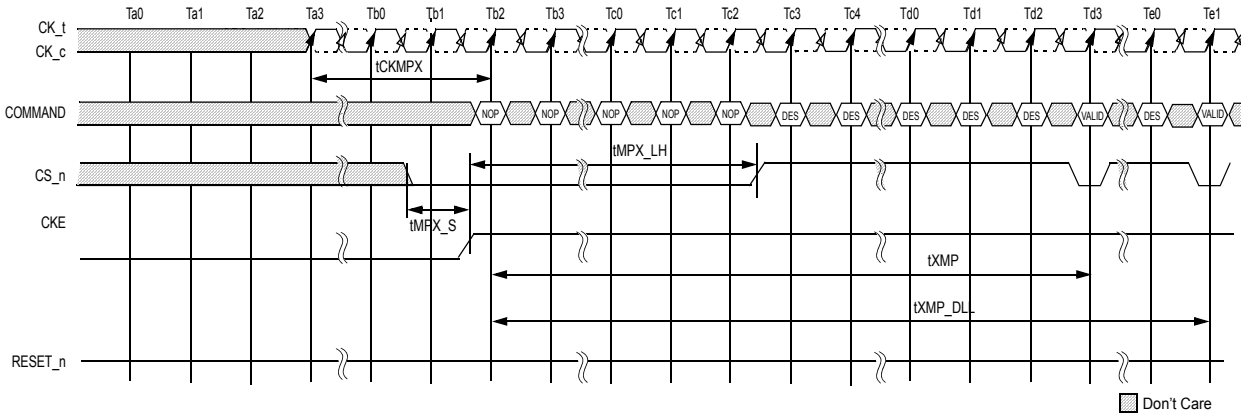


Figure 152 — Maximum Power Saving Mode Exit Sequence

4.29.5 Timing parameter bin of Maximum Power Saving Mode for DDR4-1600/1866/2133/2400/2666/3200

Description	symbol	DDR4-1600/1866/2133/2400		DDR4-2666/3200		Unit	Note
		Min	Max	Min	Max		
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	tXS(min)	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	TBD	-		
CS setup time to CKE	tMPX_S	tISmin + tIH-min	-	TBD	-		
CS_n High hold time to CKE rising edge	tMPX_HH	tXP(min)		TBD	-		
CS_n Low hold time to CKE rising edge	tMPX_LH	12	tXMP-10ns	TBD	TBD	ns	1

NOTE 1 tMPX_LH(max) is defined with respect to actual tXMP in system as opposed to tXMP(min).

4.30 Connectivity Test Mode

4.30.1 Introduction

The DDR4 memory device supports a connectivity test (CT) mode, which is designed to greatly speed up testing of electrical continuity of pin interconnection on the PC boards between the DDR4 memory devices and the memory controller on the SoC. Designed to work seamlessly with any boundary scan devices, the CT mode is required for all x16 width devices independant of density and optional for all x8 and x4 width devices with densities greater than or equal to 8Gb.

Contrary to other conventional shift register based test mode, where test patterns are shifted in and out of the memory devices serially in each clock, DDR4's CT mode allows test patterns to be entered in parallel into the test input pins and the test results extracted in parallel from the test output pins of the DDR4 memory device at the same time, significantly enhancing the speed of the connectivity check. RESET_n is registered to High and VrefCA must be stable prior to entering CT mode. Once put in the CT mode, the DDR4 memory device effectively appears as an asynchronous device to the external controlling agent; after the input test pattern is applied, the connectivity check test results are available for extraction in parallel at the test output pins after a fixed propagation delay. During CT mode, any ODT is turned off.

A reset of the DDR4 memory device is required after exiting the CT mode.

4.30.2 Pin Mapping

Only digital pins can be tested via the CT mode. For the purpose of connectivity check, all pins that are used for the digital logic in the DDR4 memory device are classified as one of the following types:

1. Test Enable (TEN) pin: when asserted high, this pin causes the DDR4 memory device to enter the CT mode. In this mode, the normal memory function inside the DDR4 memory device is bypassed and the IO pins appear as a set of test input and output pins to the external controlling agent. The TEN pin is dedicated to the connectivity check function and will not be used during normal memory operation.
2. Chip Select (CS_n) pin: when asserted low, this pin enables the test output pins in the DDR4 memory device. When de-asserted, the output pins in the DDR4 memory device will be tri-stated. The CS_n pin in the DDR4 memory device serves as the CS_n pin when in CT mode.
3. Test Input: a group of pins that are used during normal DDR4 DRAM operation are designated test input pins. These pins are used to enter the test pattern in CT mode.
4. Test Output: a group of pins that are used during normal DDR4 DRAM operation are designated test output pins. These pins are used for extraction of the connectivity test results in CT mode.
5. RESET_n : Fixed high level is required during CT mode same as normal function.

Table 50 below shows the pin classification of the DDR4 memory device.

Table 50 — Pin Classification of DDR4 Memory Device in Connectivity Test(CT) Mode

Pin Type in CT Mode	Pin Names during Normal Memory Operation
Test Enable	TEN
Chip Select	CS_n
Test Input	BA0-1, BG0-1, A0-A9, A10/AP, A11, A12/BC_n, A13, WE_n/A14, CAS_n/A15, RAS_n/A16, RESET_n, CKE, ACT_n, ODT, CLK_t, CLK_c, DML_n, DBIL_n, DMU_n/DBIU_n, Parity, Alert_n
Test Output	DQ0-DQ15, DQSU_t, DQSU_c, DQSL_t, DQSL_c

Table 51 — Signal Description

Symbol	Type	Function
TEN	Input	Connectivity Test Mode is active when TEN is HIGH and inactive when TEN is LOW. TEN must be LOW during normal operation TEN is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of VDD, i.e, 960mV for DC high and 240mV for DC low.

4.30.3 Logic Equations

4.30.3.1 Min Term Equations

MTx is an inernal signal to be used to generate the signal to drive the output signals.
x16 and x8 signals are internal signal indicating the density of the device.
MT0 = XOR (A1, A6, PAR)
MT1 = XOR (A8, ALERT, A9)
MT2 = XOR (A2, A5, A15)
MT3 = XOR (A0 A7, A11)
MT4 = XOR (CK_c, ODT, CAS_n)
MT5 = XOR (Cke, RAS_n,/A16, A10/AP)
MT6 = XOR (ACT_n, A4, BA1)
MT7 = XOR (((x16 and DMU_n / DBIU_n) or (!x16 and BG1)), ((x8 or x16) and DML_n / DBIL_n), CK_t))
MT8 = XOR (WE_n / A14, A12 / BC, BA0)
MT9 = XOR (BG0, A3, (Reset_n and TEN))

4.30.3.2 Output equations for x16 devices

DQ0 = MT0
DQ1 = !DQ0
DQ2 = MT1
DQ3 = !DQ2
DQ4 = MT2
DQ5 = !DQ4
DQ6 = MT3
DQ7 = !DQ6
DQ8 = MT4
DQ9 = !DQ8
DQ10 = MT5
DQ11 = ! DQ10
DQ12 = MT6
DQ13 = MT7
DQ14 = MT8
DQ15 = !DQ14
DQSL_t = MT9
DQSL_c = !DQ12
DQSU_t = !DQSL_t
DQSU_c = !DQ13

4.30.3.3 Output equations for x8 devices

DQ0 = MT0
DQ1 = MT1
DQ2 = MT2
DQ3 = MT3
DQ4 = MT4
DQ5 = MT5
DQ6 = MT6
DQ7 = MT7
DQS_t = MT8
DQS_c = MT9

4.30.3.4 Output equations for x4 devices

DQ0 = XOR(MT0, MT1)
DQ1 = XOR(MT2, MT3)
DQ2 = XOR(MT4, MT5
DQ3 = XOR(MT6, MT7)
DQS_t = MT8
DQS_c = MT9

4.30.4 Timing Requirement

Prior to the assertion of the TEN pin, all voltage supplies must be valid and stable.

Upon the assertion of the TEN pin, the CK_t and CK_c signals will be ignored and the DDR4 memory device enter into the CT mode after tBSCAN_Enable. In the CT mode, no refresh activities in the memory arrays, initiated either externally (i.e., auto-refresh) or internally (i.e., self-refresh), will be maintained.

The TEN pin may be asserted at anytime during normal memory operation including when the DDR4 memory device is in low power (or self refreshed) mode. During CT Mode, the signaling of all test input pins is CMOS rail-to-rail with DC high and low at 80% and 20% of VDD.

The TEN pin may be de-asserted at any time in the CT mode. Upon exiting the CT mode, the states of the DDR4 memory device are unknown and the integrity of the original content of the memory array is not guaranteed and therefore the reset initialization sequence is required.

All output signals at the test output pins will be stable within tBSCAN_valid after the test inputs have been applied to the test input pins with TEN input and CS_n input maintained High and Low respectively.

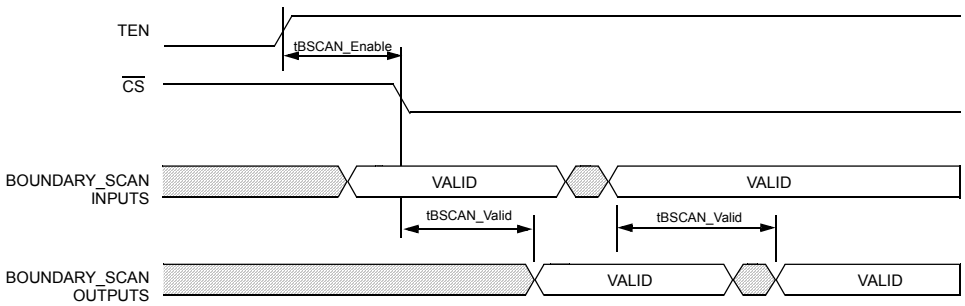


Figure 153 — Timing Diagram for Boundary Scan mode

Table 52 — AC parameters for Boundary scan mode

Symbol	Min	Mix	Unit
tBSCAN_Enable	100	-	ns
tBSCAN_Valid	-	20	ns

NOTE 1 The signaling of all test input pins, TEN and CS_n is CMOS rail-to-rail with DC high and low at 80% and 20% of VDD

4.31 CLK to Read DQS timing parameters

DDR4 supports DLLOFF mode. Following parameters will be defined for CK to read DQS timings.

Table 53 — CLK to Read DQS Timing Parameters

Speed		DDR4-1600/1866/2133/2400/2666/3200			
Parameter	Symbol	Min	Max	Units	NOTE
DQS_t, DQS_c rising edge output access time from rising CK_t, CK_c	tDQSCK (DLL On)	TBD	TBD	ps	1, 3, 8
	tDQSCK (DLL Off)	TBD	TBD	ps	2, 3, 8
Jitter of DQS_t, DQS_c rising edge output access time	tDQSCKJ (DLL On)	-	TBD	ps	1,4,5,6,7,8
	tDQSCKJ (DLL Off)	-	TBD	ps	2,4,5,6,7,8
VDD sensitivity of tDQSCK (DLL Off)	dTDQSCKdV	-	TBD	ps/mV	2, 6
Temperature sensitivity of tDQSCK (DLL Off)	dTDQSCKdT	-	TBD	ps/^{o}C	2, 6

NOTE 1 These parameters are applied when DRAM is in DLLON mode.
NOTE 2 These parameters are applied when DRAM is in DLLOFF mode.
NOTE 3 Measured over full VDD and Temperature spec ranges.
NOTE 4 Measured at fixed and constant VDD and Temperature condition.
NOTE 5 Measured for a given DRAM part, and for each DQS_t/DQS_c pair in case of x16 (part variation is excluded).
NOTE 6 These parameters are verified by design and characterization, and may not be subject to production test.
NOTE 7 For a given part and VDD and Temperature condition, the window of DQS_t/DQS_c rising edge with respect to the clock rising edge is fixed for an indefinite time period.
NOTE 8 Assume no jitter on input clock signals to the DRAM.

tDQSCK,Min
= Min {Min {tDQSCK(j), all VDD and Temperature ranges}, all DQS pairs and parts}
tDQSCK,Max
= Max {Max {tDQSCK(j), all VDD and Temperature ranges}, all DQS pairs and parts}
tDQSCKJ, Max
= Max {tDQSCK(j), fixed VDD and Temperature} - Min {tDQSCK(j), fixed VDD and Temperature}

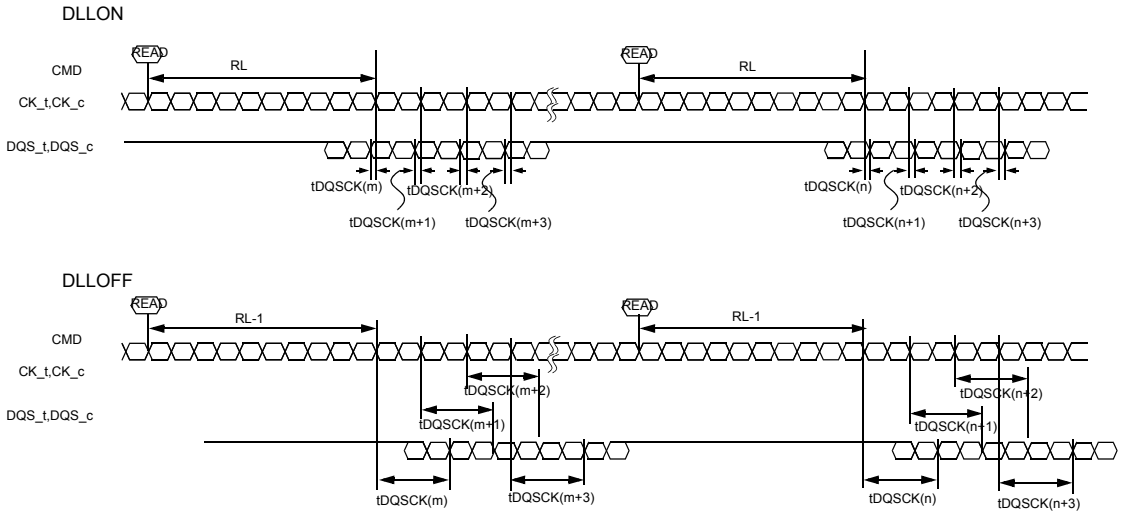
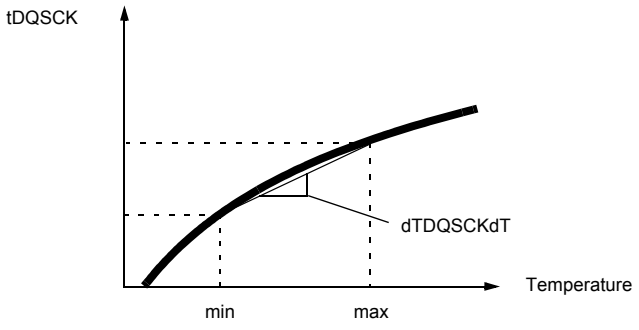
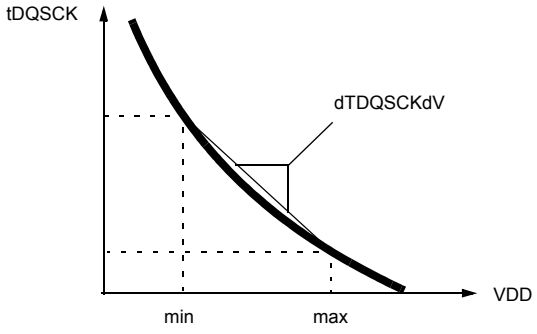


Figure 154 — tDQSCK Definition Difference between DLL ON and DLL OFF



dTDQSCKdT = I tDQSCK(Toper,max) - tDQSCK(Toper,min)I / IToper,max - Toper,minI

Figure 155 — dTDQSCKTdT Definition



dTDQSCKdV = I tDQSCK(VDD,max) - tDQSCK(VDD,min)I / IVDD,max - VDD,minI

Figure 156 — TDQSCKTdV Definition

5 On-Die Termination

ODT (On-Die Termination) is a feature of the DDR4 SDRAM that allows the DRAM to change termination resistance for each DQ, DQS_t, DQS_c and DM_n for x4 and x8 configuration (and TDQS_t, TDQS_c for X8 configuration, when enabled via A11=1 in MR1) via the ODT control pin or Write Command or Default Parking value with MR setting. For x16 configuration, ODT is applied to each DQU, DQL, DQSU_t, DQSU_c, DQSL_t, DQSL_c, DMU_n and DML_n signal. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently change termination resistance for any or all DRAM devices. More details about ODT control modes and ODT timing modes can be found further down in this document :

- The ODT control modes are described in Section 5.1.
- The ODT synchronous mode is described in Section 5.2
- The Dynamic ODT feature is described in Section 5.3
- The ODT asynchronous mode is described in Section 5.4
- The ODT buffer disable mode is described in “ODT buffer disabled mode for Power down” in Section 5.5

The ODT feature is turned off and not supported in Self-Refresh mode. A simple functional representation of the DRAM ODT feature is shown in Figure 157.

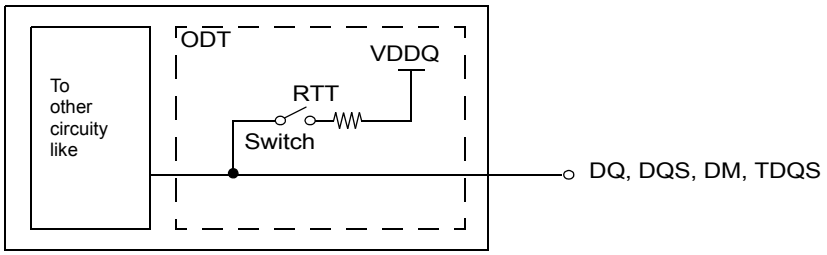


Figure 157 — Functional Representation of ODT

The switch is enabled by the internal ODT control logic, which uses the external ODT pin and Mode Register Setting and other control information, see below. The value of RTT is determined by the settings of Mode Register bits (see Section 3.5). The ODT pin will be ignored if the Mode Registers MR1 is programmed to disable RTT_NOM(MR1{A10,A9,A8}={0,0,0}) and in self-refresh mode.

5.1 ODT Mode Register and ODT State Table

The ODT Mode of DDR4 SDRAM has 4 states, Data Termination Disable, RTT_WR, RTT_NOM and RTT_PARK. And the ODT Mode is enabled if any of MR1{A10,A9,A8} or MR2 {A10:A9} or MR5 {A8:A6} are non zero. In this case, the value of RTT is determined by the settings of those bits.
After entering Self-Refresh mode, DRAM automatically disables ODT termination and set Hi-Z as termination state regardless of these setting.

Application: Controller can control each RTT condition with WR/RD command and ODT pin

- RTT_WR: The rank that is being written to provide termination regardless of ODT pin status (either HIGH or LOW)
- RTT_NOM: DRAM turns ON RTT_NOM if it sees ODT asserted (except ODT is disabled by MR1).
- RTT_PARK: Default parked value set via MR5 to be enabled and ODT pin is driven LOW.
- Data Termination Disable: DRAM driving data upon receiving READ command disables the termination after RL-X and stays off for a duration of BL/2 + X + Y clock cycles.
X is 2 for 1tCK and 3 for 2tCK preamble mode.
Y is 0 when CRC is disabled and 1 when it’s enabled
- The Termination State Table is shown in Table 54.

Those RTT values have priority as following.
1. Data Termination Disable
2. RTT_WR
3. RTT_NOM
4. RTT_PARK
which means if there is WRITE command along with ODT pin HIGH, then DRAM turns on RTT_WR not RTT_NOM, and also if there is READ command, then DRAM disables data termination regardless of ODT pin and goes into Driving mode.

Table 54 — Termination State Table

RTT_PARK MR5{A8:A6}	RTT_NOM MR1 {A10:A9:A8}	ODT pin	DRAM termination state	Note
Enabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	RTT_PARK	1,2
	Disabled	Don't care[3]	RTT_PARK	1,2
Disabled	Enabled	HIGH	RTT_NOM	1,2
		LOW	Hi-Z	1,2
	Disabled	Don't care[3]	Hi-Z	1,2

NOTE 1 When read command is executed, DRAM termination state will be Hi-Z for defined period independent of ODT pin and MR setting of RTT_PARK/RTT_NOM. This is described in section 1.2.3 ODT During Read.

NOTE 2 If RTT_WR is enabled, RTT_WR will be activated by Write command for defined period time independent of ODT pin and MR setting of RTT_PARK /RTT_NOM. This is described in section 1.3 Dynamic ODT.

NOTE 3 If RTT_NOM MRS is disabled, ODT receiver power will be turned off to save power.

On-Die Termination effective resistance RTT is defined by MRS bits.
ODT is applied to the DQ, DM, DQS_T/DQS_C and TDQS_T/TDQS_C (x8 devices only) pins.
A functional representation of the on-die termination is shown in the figure below.

$$RTT = \frac{VDDQ - Vout}{|\ I\ out\ |}$$

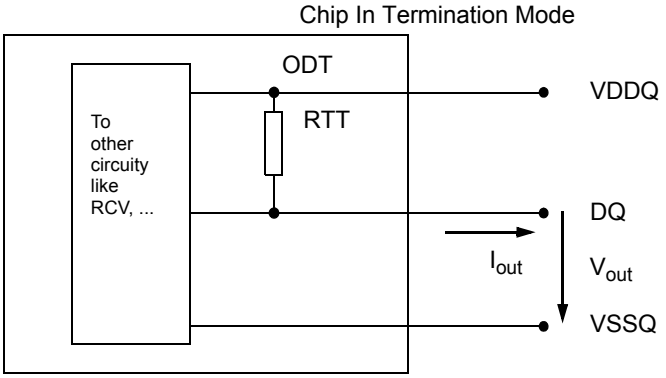


Figure 158 — On Die Termination

On die termination effective Rtt values supported are 240, 120, 80, 60, 48, 40, 34 ohms.

ODT Electrical Characteristics RZQ=240Ω +/-1% entire temperature operation range; after proper ZQ calibration

RTT	Vout	Min	Nom	Max	Unit	NOTE
240Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ	1,2,3
120Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/2	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/2	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/2	1,2,3
80Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/3	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/3	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/3	1,2,3
60Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/4	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/4	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/4	1,2,3
48Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/5	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/5	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/5	1,2,3
40Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/6	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/6	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/6	1,2,3
34Ω	VOLdc= 0.5* VDDQ	0.9	1	1.25	RZQ/7	1,2,3
	VOMdc= 0.8* VDDQ	0.9	1	1.1	RZQ/7	1,2,3
	VOHdc= 1.1* VDDQ	0.8	1	1.1	RZQ/7	1,2,3
DQ-DQ Mismatch within byte	0.8* VDDQ	TBD		TBD	%	1,2,4

NOTE 1 The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity.

NOTE 2 Pull-up ODT resistors are recommended to be calibrated at 0.8*VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5*VDDQ and 1.1*VDDQ.

NOTE 3 Measurement definition for RTT:tbd

NOTE 4 DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C (characterized)

5.2 Synchronous ODT Mode

Synchronous ODT mode is selected whenever the DLL is turned on and locked. Based on the power-down definition, these modes are:

- Any bank active with CKE high
- Refresh with CKE high
- Idle mode with CKE high
- Active power down mode
- Precharge power down mode

In synchronous ODT mode, RTT_NOM will be turned on DODTLon clock cycles after ODT is sampled HIGH by a rising clock edge and turned off DODTLoff clock cycles after ODT is registered LOW by a rising clock edge. The ODT latency is tied to the Write Latency (WL = CWL + AL + PL) by: DODTLon = WL - 2; DODTLoff = WL - 2.
When operating in 2tCK Preamble Mode, The ODT latency must be 1 clock smaller than in 1tCK Preamble Mode; DODTLon =WL - 3; DODTLoff = WL - 3."(WL = CWL+AL+PL)

5.2.1 ODT Latency and Posted ODT

In Synchronous ODT Mode, the Additive Latency (AL) and the Parity Latency (PL) programmed into the Mode Register (MR1) applies to ODT Latencies as shown inTable 55 and Table 56. For details, refer to DDR4 SDRAM latency definitions.

Table 55 — ODT Latency

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Unit
DODTLon	Direct ODT turn on Latency	CWL + AL + PL - 2.0	tCK
DODTLoff	Direct ODT turn off Latency	CWL + AL + PL - 2.0	
RODTLoff	Read command to internal ODT turn off Latency	See detail Table 56	
RODTLon4	Read command to RTT_PARK turn on Latency in BC4	See detail Table 56	
RODTLon8	Read command to RTT_PARK turn on Latency in BC8/BL8	See detail Table 56	

Table 56 — Read command to ODT off/on Latency variation by Preamble and CRC

Symbol	1tck Preamble	2tck Preamble	Unit
	CRC off	CRC off	
RODTLoff	CL+AL+PL-2.0	CL+AL+PL-3.0	tCK
RODTLon4	RODTLoff +4	RODTLoff +5	
RODTLon8	RODTLoff +6	RODTLoff +7	

5.2.2 Timing Parameters

In synchronous ODT mode, the following timing parameters apply:

DODTLon, DODTLoff, RODTLoff, RODTLon4, RODTLon8, tADC,min,max.

tADC,min and tADC,max are minimum and maximum RTT change timing skew between different termination values. Those timing parameters apply to both the Synchronous ODT mode and the Data Termination Disable mode.

When ODT is asserted, it must remain HIGH until minimum ODTH4 (BL=4) or ODTH8 (BL=8) is satisfied. Additionally, depending on CRC or 2tCK preamble setting in MRS, ODTH should be adjusted.

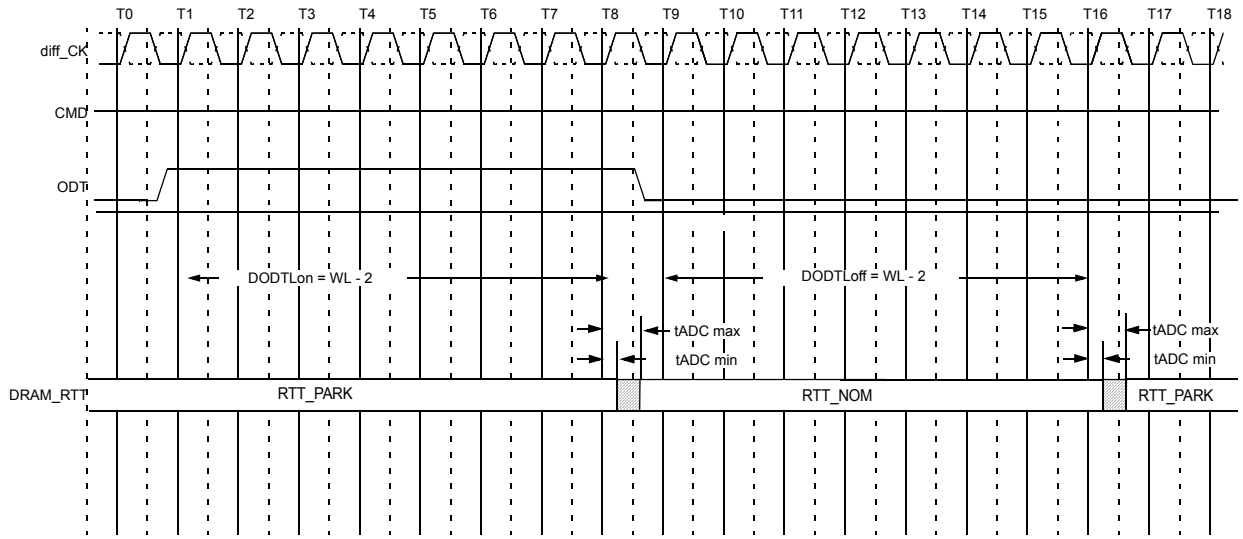


Figure 159 — Synchronous ODT Timing Example for CWL=9, AL=0, PL=0; DODTLon=WL-2=7; DODTLoff=WL-2=7

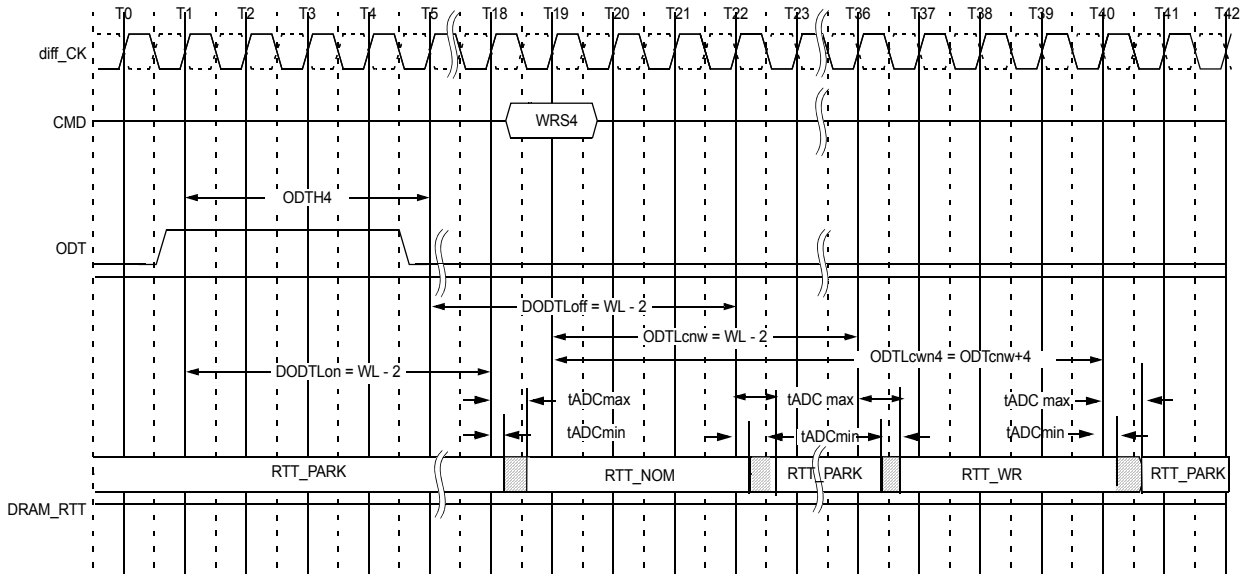


Figure 160 — Synchronous ODT example with BL=4, CWL=9, AL=10, PL=0; DODTLon/off=WL-2=17, ODTcnw=WL-2=17

ODT must be held HIGH for at least ODTH4 after assertion (T1). ODTH is measured from ODT first registered HIGH to ODT first registered LOW, or from registration of Write command. Note that ODTH4 should be adjusted depending on CRC or 2tCK preamble setting

5.2.3 ODT during Reads:

As the DDR4 SDRAM can not terminate and drive at the same time. RTT may nominally not be enabled until the end of the postamble as shown in the example below. As shown in Figure 161 below at cycle T25, DRAM turns on the termination when it stops driving which is determined by tHZ. If DRAM stops driving early (i.e tHZ is early) then tADC,min timing may apply. If DRAM stops driving late (i.e tHZ is late) then DRAM complies with tADC,max timing.

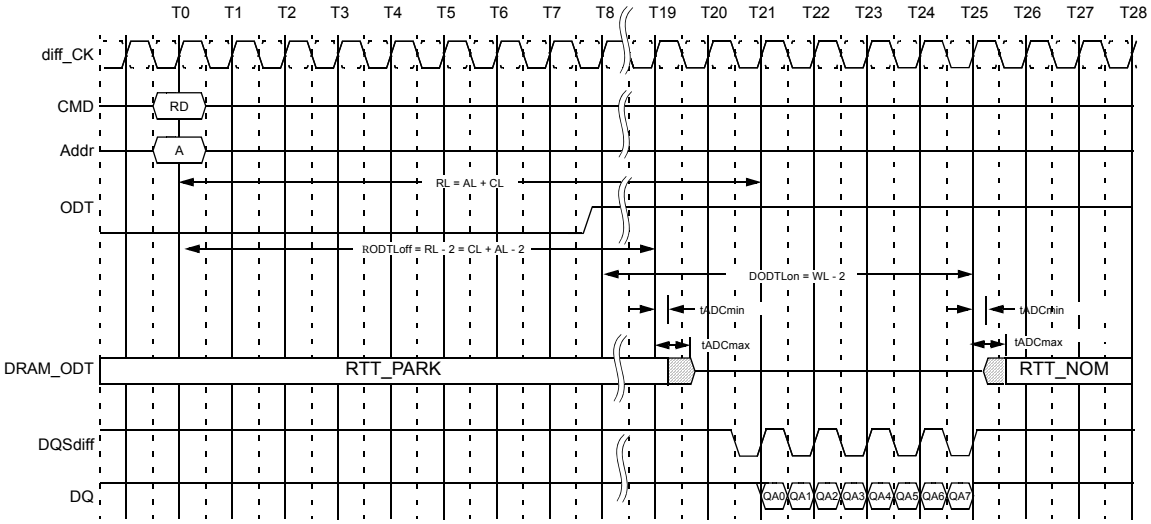


Figure 161 — Example: CL=11, PL=0; AL=CL-1=10; RL=AL+PL+CL=21; CWL=9; DODTLon=AL+CWL-2=17; DODTLoff=AL+CWL-2=17;1tCK preamble)

5.3 Dynamic ODT

In certain application cases and to further enhance signal integrity on the data bus, it is desirable that the termination strength of the DDR4 SDRAM can be changed without issuing an MRS command. This requirement is supported by the "Dynamic ODT" feature as described as follows:

5.3.1 Functional Description

The Dynamic ODT Mode is enabled if bit A[9] or A[10] of MR2 is set to '1'. The function is described as follows:

• Three RTT values are available: RTT_NOM, RTT_PARK and RTT_WR.
- The value for RTT_NOM is preselected via bits A[10:8] in MR1
- The value for RTT_PARK is preselected via bits A[8:6] in MR5
- The value for RTT_WR is preselected via bits A[10:9] in MR2

• During operation without commands, the termination is controlled as follows;
- Nominal termination strength RTT_NOM or RTT_PARK is selected.
- RTT_NOM on/off timing is controlled via ODT pin and latencies DODTLon and DODTLoff and RTT_PARK is on when ODT is LOW.

• When a write command (WR, WRA, WRS4, WRS8, WRAS4, WRAS8) is registered, and if Dynamic ODT is enabled, the termination is controlled as follows:
- A latency ODTLcnw after the write command, termination strength RTT_WR is selected.
- A latency ODTLcwn8 (for BL8, fixed by MRS or selected OTF) or ODTLcwn4 (for BC4, fixed by MRS or selected OTF) after the write command, termination strength RTT_WR is de-selected.
- 1 or 2 clocks will be added or subtracted into/from ODTLcwn8 and ODTLcwn4 depending on CRC and/or 2tCK preamble setting.

Table 57 shows latencies and timing parameters which are relevant for the on-die termination control in Dynamic ODT mode.

The Dynamic ODT feature is not supported at DLL-off mode. User must use MRS command to set Rtt_WR, MR2{A10,A9}={0,0} externally.

Table 57 — Latencies and timing parameters relevant for Dynamic ODT with 1tCK preamble mode and CRC disabled

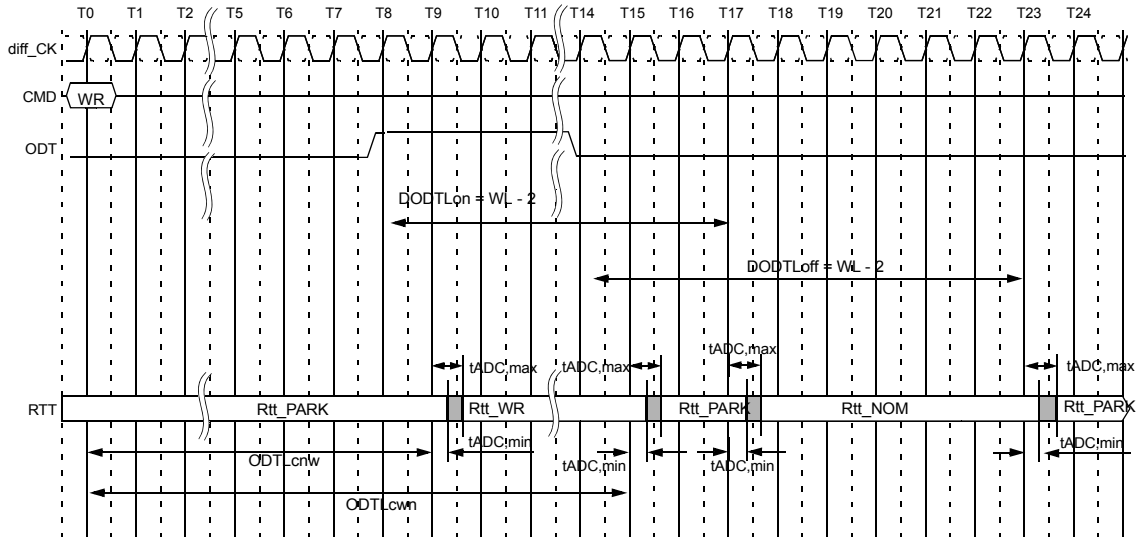
Name and Description	Abbr.	Defined from	Define to	Definition for all DDR4 speed bins	Unit
ODT Latency for changing from RTT_PARK/ RTT_NOM to RTT_WR	ODTLcnw	Registering external write command	Change RTT strength from RTT_PARK/ RTT_Nom to RTT_WR	ODTLcnw = WL - 2	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 4)	ODTLcwn4	Registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn4 = 4 + ODTLcnw	tCK
ODT Latency for change from RTT_WR to RTT_PARK/RTT_Nom (BL = 8)	ODTLcwn8	registering external write command	Change RTT strength from RTT_WR to RTT_PARK/ RTT_Nom	ODTLcwn8 = 6 + ODTLcnw	tCK(avg)
RTT change skew	tADC	ODTLcnw ODTLcwn	RTT valid	tADC(min) = 0.3 tADC(max) = 0.7	tCK(avg)

Table 58 — Latencies and timing parameters relevant for Dynamic ODT with 1 and 2tCK preamble mode and CRC en/disabled

Symbol	1tck Preamble		2tck Preamble		Unit
	CRC off	CRC on	CRC off	CRC on	
ODTLcnw	WL - 2	WL - 2	WL - 3	WL - 3	tCK
ODTLcwn4	ODTLcnw +4	ODTLcnw +7	ODTLcnw +5	ODTLcnw +8	
ODTLcwn8	ODTLcnw +6	ODTLcnw +7	ODTLcnw +7	ODTLcnw +8	

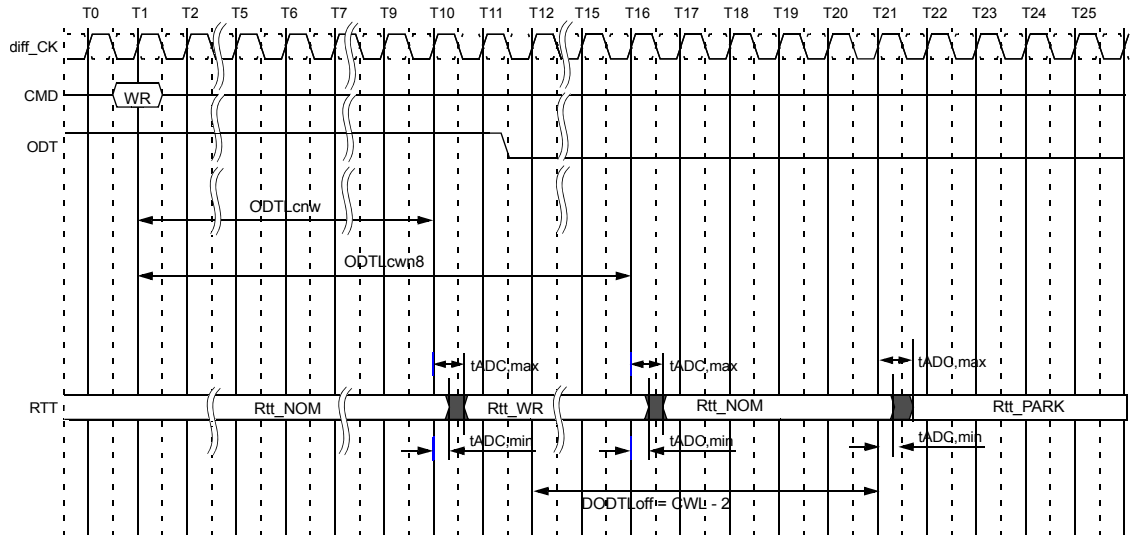
5.3.2 ODT Timing Diagrams

The following pages provide example timing diagrams



ODTLcnw = WL-2 (1tCK preamble), WL-3 (2tCK preamble)
ODTLcwn = WL+2 (BC4), WL+4(BL8) w/o CRC or WL+5,5 (BC4, BL8 respectively) when CRC is enabled.

Figure 162 — ODT timing (Dynamic ODT, 1tCK preamble, CL=14, CWL=11, BL=8, AL=0, CRC Disabled)



Behavior with WR command is issued while ODT being registered high.

Figure 163 — Dynamic ODT overlapped with Rtt_NOM (CL=14, CWL=11, BL=8, AL=0, CRC Disabled)

5.4 Asynchronous ODT mode

Asynchronous ODT mode is selected when DLL is disabled by MR1 bit A0='0'b.
In asynchronous ODT timing mode, internal ODT command is not delayed by either the Additive latency (AL) or relative to the external ODT signal (RTT_NOM).
In asynchronous ODT mode, the following timing parameters apply tAONAS,min, max, tAOFAS,min,max.

Minimum RTT_NOM turn-on time (tAONASmin) is the point in time when the device termination circuit leaves RTT_PARK and ODT resistance begins to change. Maximum RTT_NOM turn on time(tAONASmax) is the point in time when the ODT resistance is reached RTT_NOM.

tAONASmin and tAONASmax are measured from ODT being sampled high.
Minimum RTT_NOM turn-off time (tAOFASmin) is the point in time when the devices termination circuit starts to leave RTT_NOM.
Maximum RTT_NOM turn-off time (tAOFASmax) is the point in time when the on-die termination has reached RTT_PARK.
tAOFASmin and tAOFASmax are measured from ODT being sampled low.

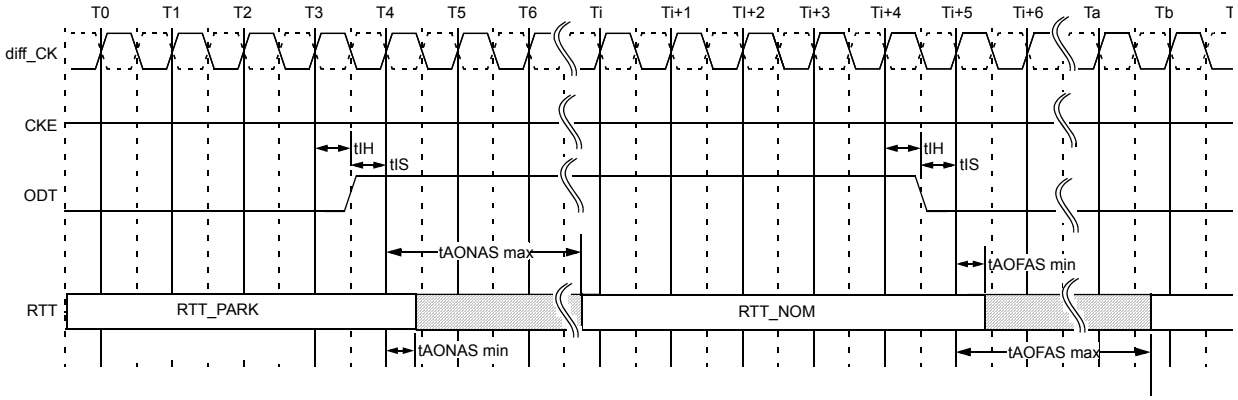


Figure 164 — Asynchronous ODT Timing on DDR4 SDRAM with DLL-off

Table 59 — Asynchronous ODT Timing Parameters for all Speed Bins

Description	Symbol	min	max	Unit
Asynchronous RTT turn-on delay	t_{AONAS}	1.0	9.0	ns
Asynchronous RTT turn-off delay	t_{AOFAS}	1.0	9.0	ns

5.5 ODT buffer disabled mode for Power down

DRAM does not provide Rtt_NOM termination during power down when ODT input buffer deactivation mode is enabled in MR5 bit A5. To account for DRAM internal delay on CKE line to disable the ODT buffer and block the sampled output, the host controller must continuously drive ODT to either low or high when entering power down. The ODT signal may be floating after tCPDEDmin has expired. In this mode, RTT_NOM termination corresponding to sampled ODT at the input after CKE is first registered low (and tANPD before that) may not be provided. tANPD is equal to (WL-1) and is counted backwards from PDE.

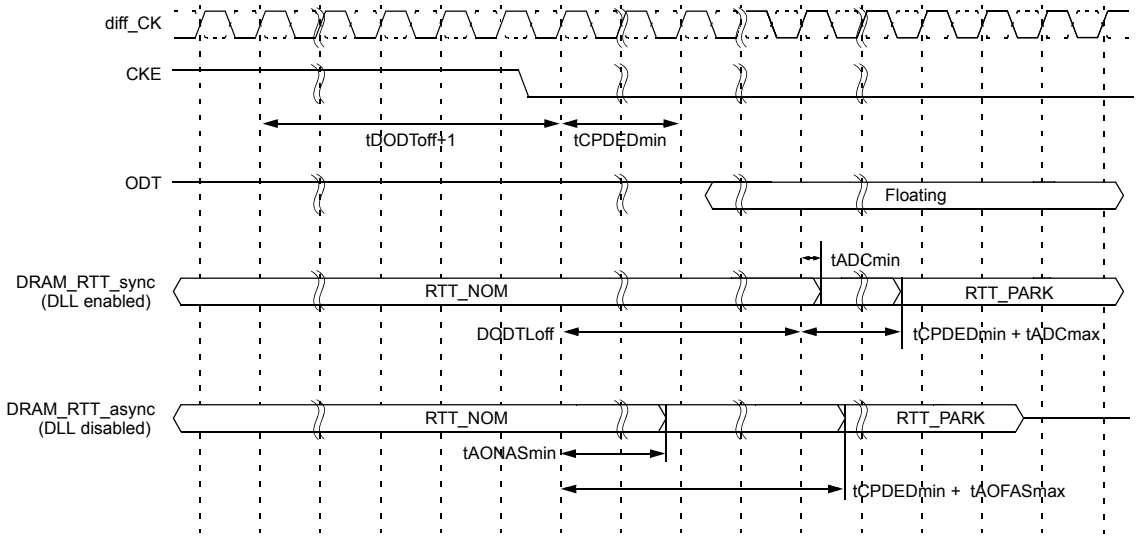


Figure 165 — ODT timing for power down entry with ODT buffer disable mode

When exit from power down, along with CKE being registered high, ODT input signal must be re-driven and maintained low until tXP is met.

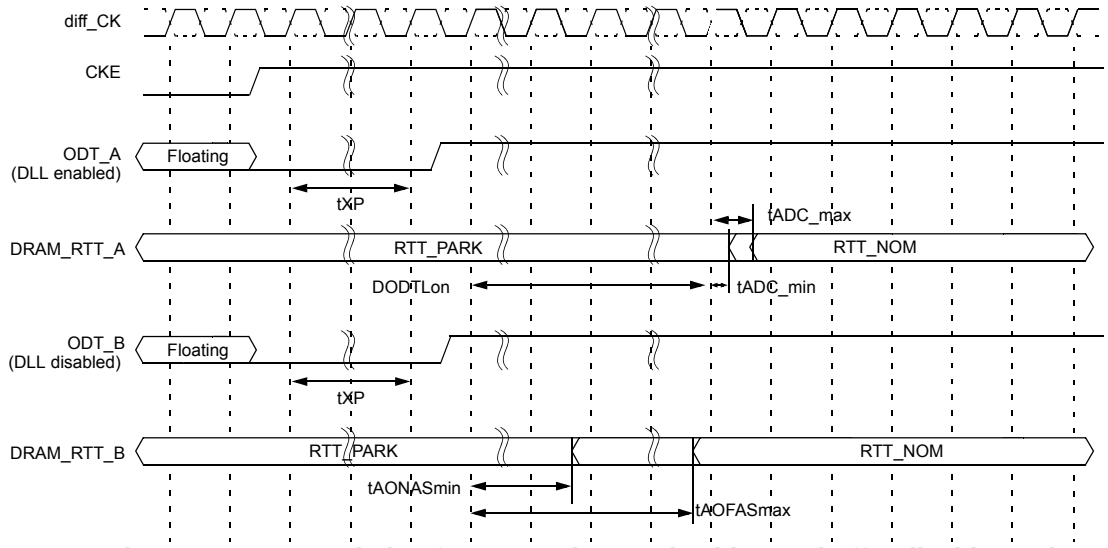


Figure 166 — ODT timing for power down exit with ODT buffer disable mode

5.6 ODT Timing Definitions

5.6.1 Test Load for ODT Timings

Different than for timing measurements, the reference load for ODT timings is defined in Figure 167.

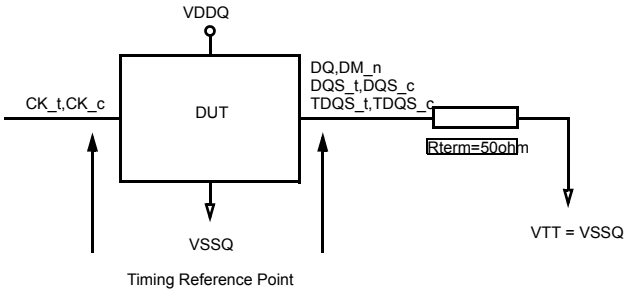


Figure 167 — ODT Timing Reference Load

5.6.2 ODT Timing Definitions

Definitions for tADC, tAONAS and tAOFAS are provided in Table 60 and subsequent figures. Measurement reference settings are provided in Table 61. tADC of Dynamic ODT case and Read Disable ODT case are represented by tADC of Direct ODTControl case.

Table 60 — ODT Timing Definitions

Symbol	Begin Point Definition	End Point Definition	Figure	Note
tADC	Rising edge of CK_t,CK_c defined by the end point of DODTLoff	Extrapolated point at VRTT_NOM	Figure 168	
	Rising edge of CK_t,CK_c defined by the end point of DODTLon	Extrapolated point at VSSQ		
tAONAS	Rising edge of CK_t,CK_c with ODT being first registered high	Extrapolated point at VSSQ	Figure 169	
tAOFAS	Rising edge of CK_t,CK_c with ODT being first registered low	Extrapolated point at VRTT_NOM		

Table 61 — Reference Settings for ODT Timing Measurements

Measured Parameter	RTT_PARK	RTT_NOM	Vsw1	Vsw2	Figure	Note
tADC	Disable	RZQ/7	0.20V	0.40V	Figure 168	1,2
tAONAS	Disable	RZQ/7	0.20V	0.40V	Figure 169	1,2
tAOFAS	Disable	RZQ/7	0.20V	0.40V		

NOTE 1 MR setting is as follows.
- MR1 A10=1, A9=1, A8=1 (RTT_NOM_Setting)
- MR5 A8=0 , A7=0, A6=0 (RTT_PARK Setting)

NOTE 2 ODT state change is controlled by ODT pin.

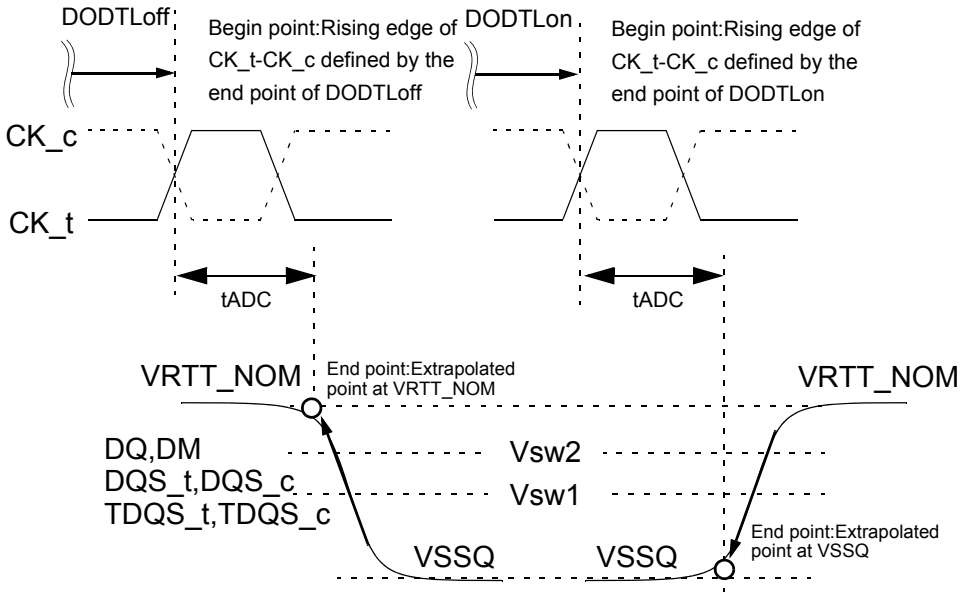


Figure 168 — Definition of tADC

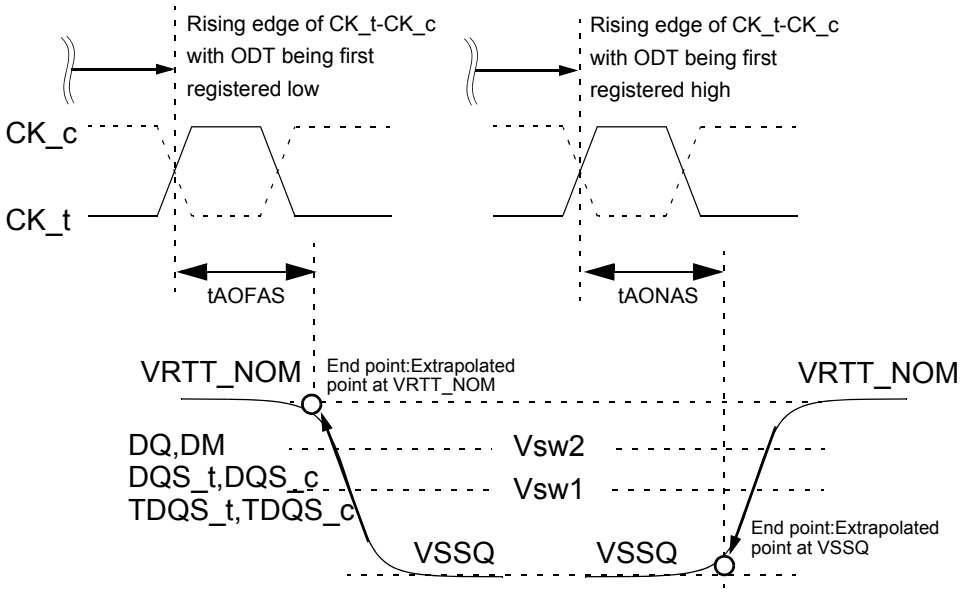


Figure 169 — Definition of tAOFAS and tAONAS

6 Absolute Maximum Ratings

Table 62 — Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	NOTE
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin relative to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	°C	1,2

NOTE 1 Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

NOTE 2 Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

NOTE 3 VDD and VDDQ must be within 300 mV of each other at all times;and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

NOTE 4 VPP must be equal or greater than VDD/VDDQ at all times

7 AC & DC Operating Conditions

Table 63 — Recommended DC Operating Conditions

Symbol	Parameter	Rating			Unit	NOTE
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.14	1.2	1.26	V	1,2,3
VDDQ	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
VPP		2.375	2.5	2.75	V	3

NOTE 1 Under all conditions VDDQ must be less than or equal to VDD.
NOTE 2 VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
NOTE 3 DC bandwidth is limited to 20MHz.

7.1 AC and DC Input Measurement Levels: V_{REF} Tolerances

The DC-tolerance limits and ac-noise limits for the reference voltages V_{REFCA} is illustrated in Figure 170. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. (V_{REF} stands for V_{REFCA}).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirement in Table X. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than ± 1% V_{DD}.

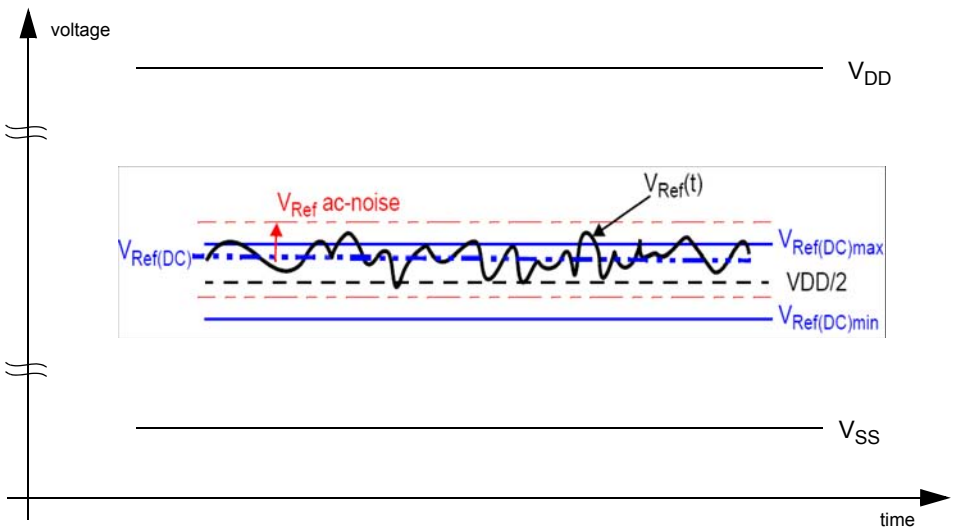


Figure 170 — Illustration of V_{REF}(DC) tolerance and V_{REF} AC-noise limits

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on V_{REF}.

"V_{REF}" shall be understood as $V_{REF}(DC)$, as defined in Figure 170.

This clarifies, that DC-variations of V_{REF} affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with V_{REF} AC-noise. Timing and voltage effects due to AC-noise on V_{REF} up to the specified limit (+/-1% of V_{DD}) are included in DRAM timings and their associated deratings.

7.2 AC and DC Logic Input Levels for Differential Signals

7.2.1 Differential signal definition

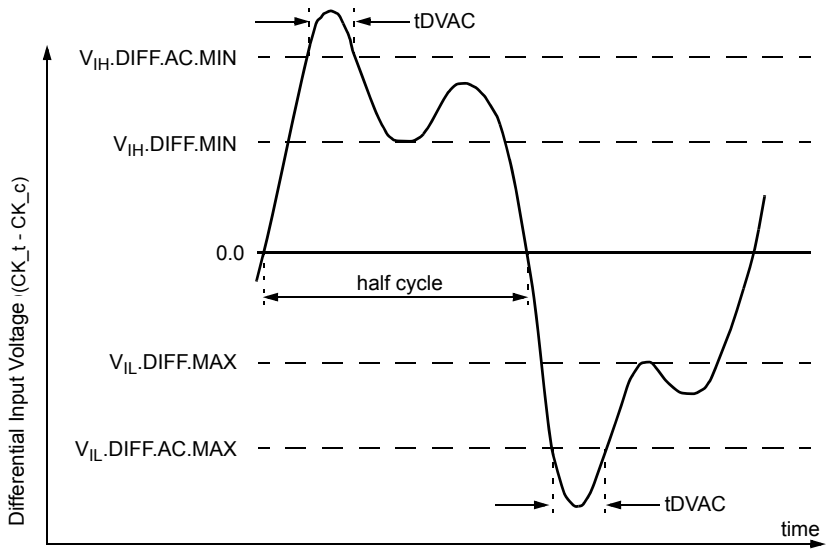


Figure 171 — Definition of differential ac-swing and "time above ac-level" t_{DVAC}

7.2.2 Differential swing requirements for clock (CK_t - CK_c)

Table 64 — Differential AC and DC Input Levels

Symbol	Parameter	DDR4 -1600,1866,2133		DDR4 -2400,2666 & 3200		unit	NOTE
		min	max	min	max		
V_{IHdiff}	differential input high	TBD	NOTE 3	TBD	NOTE 3	V	1
V_{ILdiff}	differential input low	NOTE 3	TBD	NOTE 3	TBD	V	1
$V_{IHdiff}(AC)$	differential input high ac	2 x ($V_{IH}(AC)$ - V_{REF})	NOTE 3	2 x ($V_{IH}(AC)$ - V_{REF})	NOTE 3	V	2
$V_{ILdiff}(AC)$	differential input low ac	NOTE 3	2 x ($V_{IL}(AC)$ - V_{REF})	NOTE 3	2 x ($V_{IL}(AC)$ - V_{REF})	V	2

NOTE 1 Used to define a differential signal slew-rate.
NOTE 2 for CK_t - CK_c use $V_{IH}/V_{IL}(AC)$ of ADD/CMD and V_{REFCA};
NOTE 3 These values are not defined; however, the differential signals CK_t - CK_c, need to be within the respective limits ($V_{IH}(DC)$ max, $V_{IL}(DC)$min) for single-ended signals as well as the limitations for overshoot and undershoot.

Table 65 — Allowed time before ringback (tDVAC) for CK_t - CK_c

Slew Rate [V/ns]	tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = TBDmV		tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = TBDmV	
	min	max	min	max
> 4.0	TBD	-	TBD	-
4.0	TBD	-	TBD	-
3.0	TBD	-	TBD	-
2.0	TBD	-	TBD	-
1.8	TBD	-	TBD	-
1.6	TBD	-	TBD	-
1.4	TBD	-	TBD	-
1.2	TBD	-	TBD	-
1.0	TBD	-	TBD	-
< 1.0	TBD	-	TBD	-

7.2.3 Single-ended requirements for differential signals

Each individual component of a differential signal (CK_t, CK_c) has also to comply with certain requirements for single-ended signals.

CK_t and CK_c have to approximately reach VSEHmin / VSELmax (approximately equal to the ac-levels (VIH(ac) / VIL(ac)) for ADD/CMD signals) in every half-cycle.

Note that the applicable ac-levels for ADD/CMD might be different per speed-bin etc. E.g., if Different value than VIH.CA(AC120)/VIL.CA(AC120) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK_t and CK_c

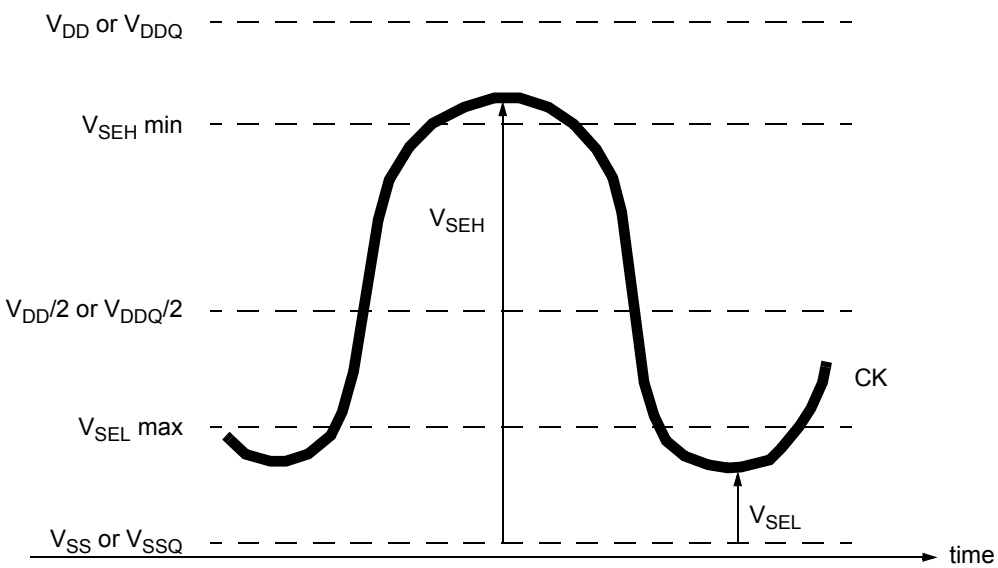


Figure 172 — Single-ended requirement for differential signals.

Note that, while ADD/CMD signal requirements are with respect to VrefCA, the single-ended components of differential signals have a requirement with respect to VDD / 2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach VSELmax, VSEHmin has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

Table 66 — Single-ended levels for CK_t, CK_c

Symbol	Parameter	DDR4-1600/1866/2133		DDR4-2400/2666/3200		Unit	NOTE
		Min	Max	Min	Max		
V_{SEH}	Single-ended high-level for CK_t - CK_c	TBD	NOTE3	TBD	NOTE3	V	1, 2
V_{SEL}	Single-ended low-level for CK_t - CK_c	NOTE3	TBD	NOTE3	TBD	V	1, 2

NOTE 1 For CK_t - CK_c use V_{IH}/V_{IL}(AC) of ADD/CMD;

NOTE 2 V_{IH}(AC)/V_{IL}(AC) for ADD/CMD is based on V_{REFCA};

NOTE 3 These values are not defined, however the single-ended signals CK_t - CK_c need to be within the respective limits (V_{IH}(DC) max, V_{IL}(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot.

7.2.4 Address and Control Overshoot and Undershoot specifications

Table 67 — AC overshoot/undershoot specification for Address and Control pins

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum overshoot area above V_{DD}	0.25	0.25	0.25	TBD	TBD	TBD	V-ns
Maximum undershoot area below V_{SS}	0.25	0.25	0.25	TBD	TBD	TBD	V-ns
(A0-A13,A17,BG1-BG0,BA2-BA0,CS_n,RAS_n / A14,CAS_n / A15,WE_n / A16,CKE,ODT,C2-C0)							

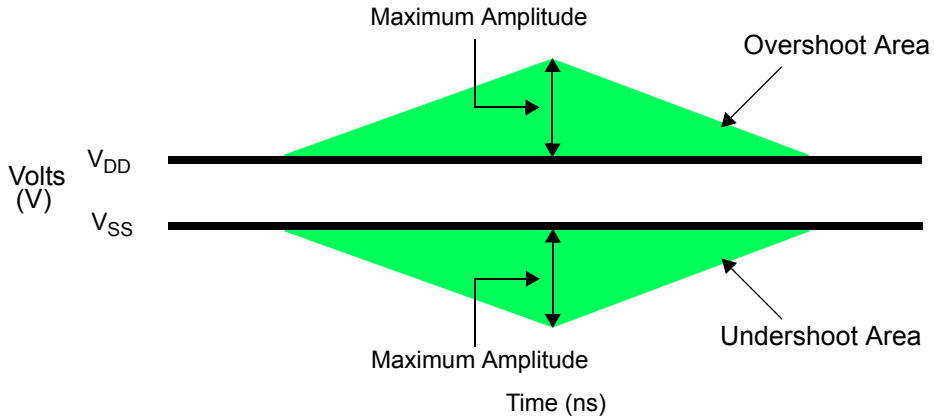


Figure 173 — Address and Control Overshoot and Undershoot Definition

7.2.5 Clock Overshoot and Undershoot Specifications

Table 68 — AC overshoot/undershoot specification for Clock

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	0.3	0.3	0.3	0.3	TBD	TBD	V
Maximum overshoot area above V_{DDQ}	0.10	0.10	0.10	TBD	TBD	TBD	V-ns
Maximum undershoot area below V_{SSQ}	0.10	0.10	0.10	TBD	TBD	TBD	V-ns
(CK_t, Ck_c)							

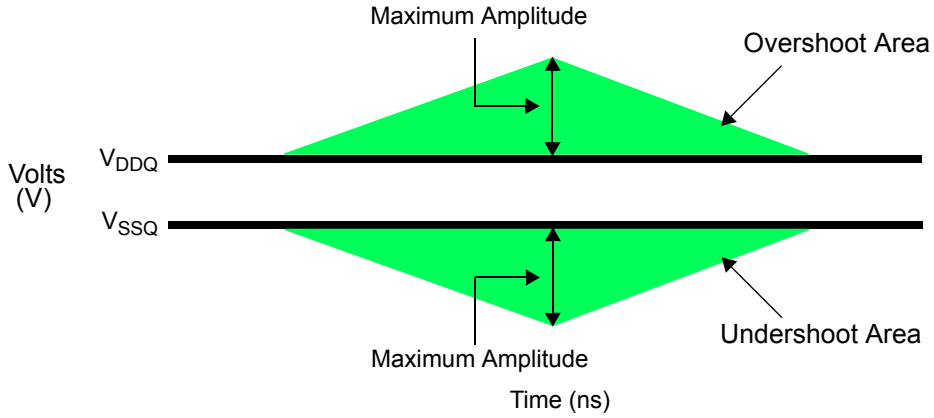


Figure 174 — Clock Overshoot and Undershoot Definition

7.2.6 Data, Strobe and Mask Overshoot and Undershoot Specifications

Table 69 — AC overshoot/undershoot specification for Data, Strobe and Mask

Parameter	Specification						Unit
	DDR4-1600	DDR4-1866	DDR4-2133	DDR4-2400	DDR4-2666	DDR4-3200	
Maximum peak amplitude allowed for overshoot area	0.4	0.4	0.4	0.4	TBD	TBD	V
Maximum peak amplitude allowed for undershoot area	0.32	0.32	0.32	0.32	0	0	V
Maximum overshoot area above V_{DDQ}	0.2	0.2	0.2	0.2	TBD	TBD	V-ns
Maximum undershoot area below V_{SSQ}	0.1	0.1	0.1	0.1	0	0	V-ns
(DQs,DQS_t,DQS_c,DM/DBI)							

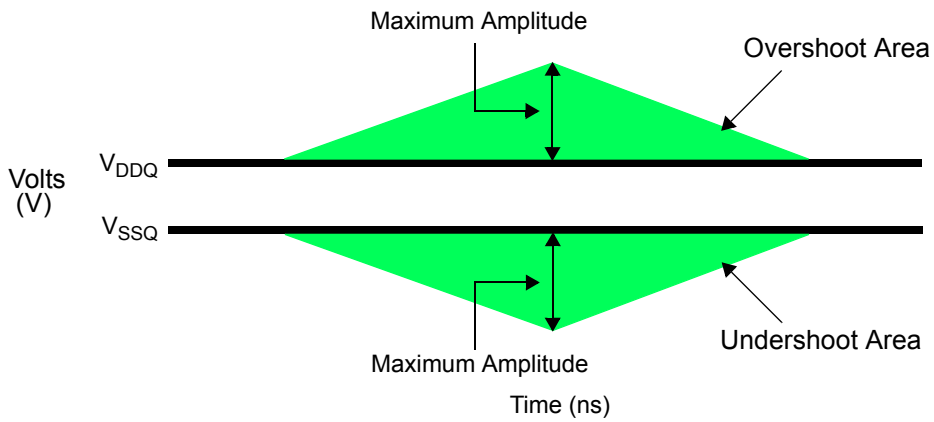


Figure 175 — Data, Strobe and Mask Overshoot and Undershoot Definition

7.3 Slew Rate Definitions for Differential Input Signals (CK)

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Table 70 and Figure 176.

Table 70 — Differential Input Slew Rate Definition

Description			Defined by
	from	to	
Differential input slew rate for rising edge(CK_t - CK_c)	$V_{ILdiffmax}$	$V_{IHdiffmin}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTRdiff$
Differential input slew rate for falling edge(CK_t - CK_c)	$V_{IHdiffmin}$	$V_{ILdiffmax}$	$[V_{IHdiffmin} - V_{ILdiffmax}] / DeltaTFdiff$
NOTE: The differential signal (i,e.,CK_t - CK_c) must be linear between these thresholds.			

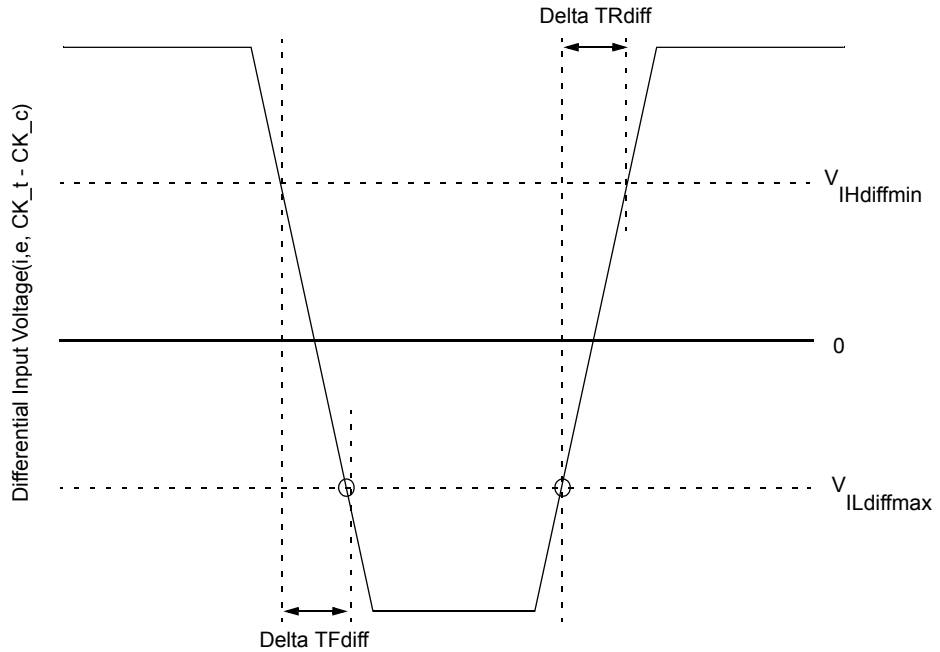


Figure 176 — Differential Input Slew Rate Definition for CK_t, CK_c

7.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock, each cross point voltage of differential input signals (CK_t, CK_c) must meet the requirements in Table 72. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the midlevel between of VDD and VSS.

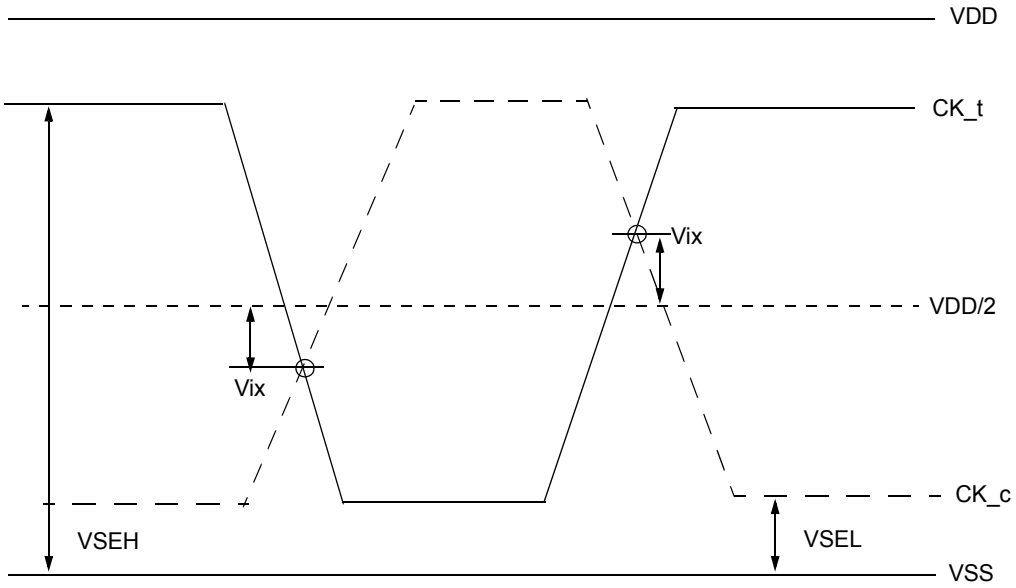


Figure 177 — Vix Definition (CK)

Table 71 — Cross point voltage for differential input signals (CK)

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200		Unit	Note
		min	max		
VIX(CK)	Differential Input Cross Point Voltage relative to VDD/2 for CK_t, CK_c	-120	-120	mV	2
		-TBD	-TBD	mV	1

NOTE 1 Extended range for Vix is only allowed for clock and if single-ended clock input signals CK_t and CK_c are monotonic with a single-ended swing VSEL / VSEH of at least VDD/2 +/- TBD mV, and when the differential slew rate of CK_t - CK_c is larger than 3 V/ns.
Refer to TBD for VSEL and VSEH standard values.

NOTE 2 The relation between Vix Min/Max and VSEL/VSEH should satisfy following.
(VDD/2) + Vix (Min) - VSEL ≥ 25mV
VSEH - ((VDD/2) + Vix (Max)) ≥ 25mV

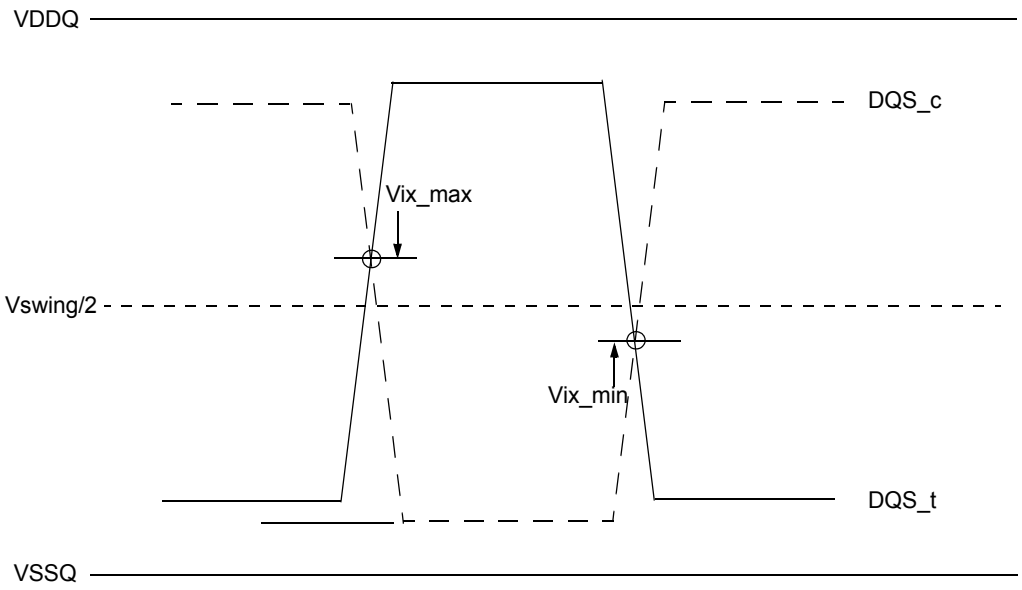


Figure 178 — Vix Definition (DQS)

Table 72 — Cross point voltage for differential input signals (DQS)

Parameter	Symbol	DDR4-1600/1866/2133		DDR4-2400		Unit	Note
		min	max	min	max		
DQS Differential input crosspoint voltage ratio	Vix_DQS_ratio	-	TBD	-	TBD	%	1,2

NOTE 1 Referenced to Vswing/2=avg 0.5(VDQS_t + VDQS_c) where the average is over tbd UI.
NOTE 2 Ratio of the Vix pk voltage divided by Vdiff_DQS : Vix_DQS_Ratio = 100* (Vix_DQS/Vdiff DQS pk-pk) where VdiffDQS pk-pk = 2*|VDQS_t - VDQS_c|

7.5 CMOS rail to rail Input Levels

7.5.1 CMOS rail to rail Input Levels for RESET_n

Table 73 — CMOS rail to rail Input Levels for RESET_n

Parameter	Symbol	Min	Max	Unit	NOTE
AC Input High Voltage	VIH(AC)_RESET	0.8*VDD	VDD	V	6
DC Input High Voltage	VIH(DC)_RESET	0.7*VDD	VDD	V	2
DC Input Low Voltage	VIL(DC)_RESET	VSS	0.3*VDD	V	1
AC Input Low Voltage	VIL(AC)_RESET	VSS	0.2*VDD	V	7
Rising time	TR_RESET	-	1.0	us	4
RESET pulse width	tPW_RESET	1.0	-	us	3,5

NOTE :

1.After RESET_n is registered LOW, RESET_n level shall be maintained below VIL(DC)_RESET during tPW_RESET, otherwise, SDRAM may not be reset.
2. Once RESET_n is registered HIGH, RESET_n level must be maintained above VIH(DC)_RESET, otherwise, SDRAM operation will not be guaranteed until it is reset asserting RESET_n signal LOW.
3. RESET is destructive to data contents.
4. No slope reversal(ringback) requirement during its level transition from Low to High.
5. This definition is applied only “Reset Procedure at Power Stable”.
6. Overshoot might occur. It should be limited by the Absolute Maximum DC Ratings.
7. Undershoot might occur. It should be limited by Absolute Maximum DC Ratings

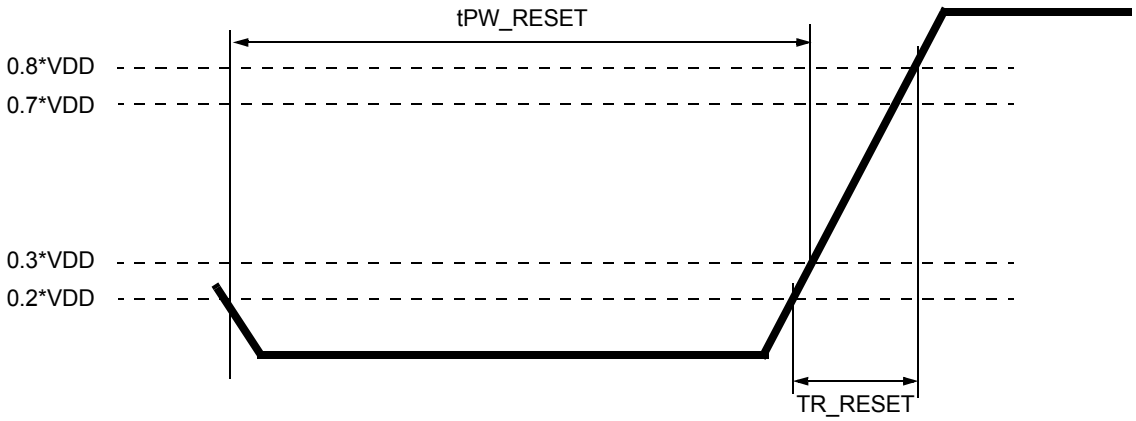


Figure 179 — RESET_n Input Slew Rate Definition

8 AC and DC output Measurement levels

8.1 Output Driver DC Electrical Characteristics

The DDR4 driver supports two different Ron values. These Ron values are referred as strong(low Ron) and weak mode(high Ron). A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

The individual pull-up and pull-down resistors (RON_{Pu} and RON_{Pd}) are defined as follows:

$$RON_{Pu} = \frac{VDDQ - Vout}{|I\,out|}$$ under the condition that RON_{Pd} is off

$$RON_{Pd} = \frac{Vout}{|I\,out|}$$ under the condition that RON_{Pu} is off

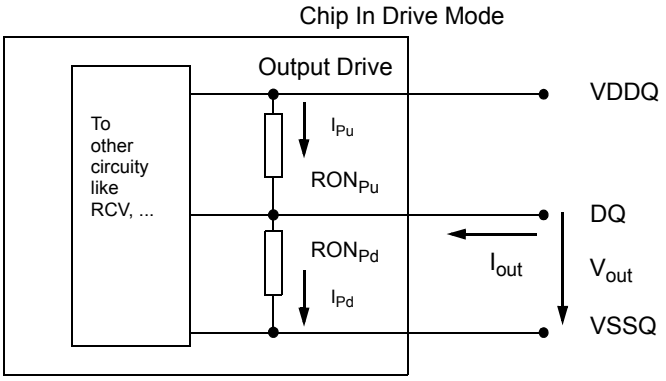


Figure 180 — Output driver

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON34Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	34Ω	1,2
	RON34Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	34Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	34Ω	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	34Ω	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,3
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,3

NOTE :
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C(characterized)
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} *100$$

Figure 181 — Strong Mode (Low Ron) Specifications

RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
48Ω	RON48Pd	VOLdc= 0.5*VDDQ	0.8	1	1.1	48Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	48Ω	1,2
		VOHdc= 1.1* VDDQ	0.9	1	1.25	48Ω	1,2
	RON48Pu	VOLdc= 0.5* VDDQ	0.9	1	1.25	48Ω	1,2
		VOMdc= 0.8* VDDQ	0.9	1	1.1	48Ω	1,2
		VOHdc= 1.1* VDDQ	0.8	1	1.1	48Ω	1,2
Mismatch between pull-up and pull-down, MMPuPd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,4
Mismatch DQ-DQ within byte variation pull-up, MMPudd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,3
Mismatch DQ-DQ within byte variation pull-dn, MMPddd		VOMdc= 0.8* VDDQ	TBD		TBD	%	1,2,3

NOTE :

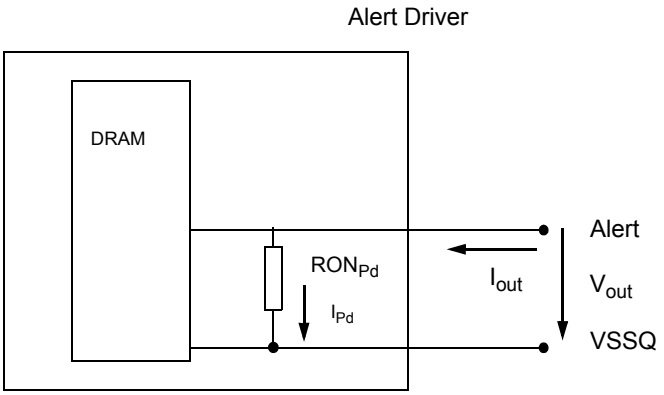
1. The tolerance limits are specified after calibration with stable voltage and temperature. For the behavior of the tolerance limits if temperature or voltage changes after calibration, see following section on voltage and temperature sensitivity(TBD).
2. Pull-up and pull-dn output driver impedances are recommended to be calibrated at 0.8 * VDDQ. Other calibration schemes may be used to achieve the linearity spec shown above, e.g. calibration at 0.5 * VDDQ and 1.1 * VDDQ.
3. DQ to DQ mismatch within byte variation for a given component including DQS_T and DQS_C(characterized)
4. Measurement definition for mismatch between pull-up and pull-down, MMPuPd : Measure RONPu and RONPD both at 0.8*VDD separately; Ronnom is the nominal Ron value

$$MMPuPd = \frac{RONPu - RONPd}{RONNOM} *100$$

8.1.1 Alert_n output Drive Characteristic

A functional representation of the output buffer is shown in the figure below. Output driver impedance RON is defined as follows:

$$RON_{Pd} = \frac{Vout}{|\ Iout\ |}$$ under the condition that RON_{Pu} is off



RON_{NOM}	Resistor	Vout	Min	Nom	Max	Unit	NOTE
34Ω	RON_{34Pd}	VOLdc= 0.1* VDDQ	0.8	1	1.2	34Ω	1
		V_{OMdc} = 0.8* VDDQ	0.8	1	1.2	34Ω	1
		V_{OHdc} = 1.1* VDDQ	0.8	1	1.2	34Ω	1

NOTE 1 VDDQ voltage is at VDDQ DC. VDDQ DC definition is tbd.

8.2 Single-ended AC & DC Output Levels

Table 74 — Single-ended AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
V_{OH}(DC)	DC output high measurement level (for IV curve linearity)	1.1 x V_{DDQ}	V	
V_{OM}(DC)	DC output mid measurement level (for IV curve linearity)	0.8 x V_{DDQ}	V	
V_{OL}(DC)	DC output low measurement level (for IV curve linearity)	0.5 x V_{DDQ}	V	
V_{OH}(AC)	AC output high measurement level (for output SR)	(0.7 + 0.15) x V_{DDQ}	V	1
V_{OL}(AC)	AC output low measurement level (for output SR)	(0.7 - 0.15) x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.15 × V_{DDQ} is based on approximately 50% of the static single-ended output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ}.

8.3 Differential AC & DC Output Levels

Table 75 — Differential AC & DC output levels

Symbol	Parameter	DDR4-1600/1866/2133/2400/2666/3200	Units	NOTE
V_{OHdiff}(AC)	AC differential output high measurement level (for output SR)	+0.3 x V_{DDQ}	V	1
V_{OLdiff}(AC)	AC differential output low measurement level (for output SR)	-0.3 x V_{DDQ}	V	1

NOTE :
1. The swing of ± 0.3 × V_{DDQ} is based on approximately 50% of the static differential output peak-to-peak swing with a driver impedance of RZQ/7Ω and an effective test load of 50Ω to V_{TT} = V_{DDQ} at each of the differential outputs.

8.4 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL(AC)}$ and $V_{OH(AC)}$ for single ended signals as shown in Table 76 and Figure 182.

Table 76 — Single-ended output slew rate definition

Description	Measured		Defined by
	From	To	
Single ended output slew rate for rising edge	V_{OL}(AC)	V_{OH}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TRse
Single ended output slew rate for falling edge	V_{OH}(AC)	V_{OL}(AC)	[V_{OH}(AC)-V_{OL}(AC)] / Delta TFse

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

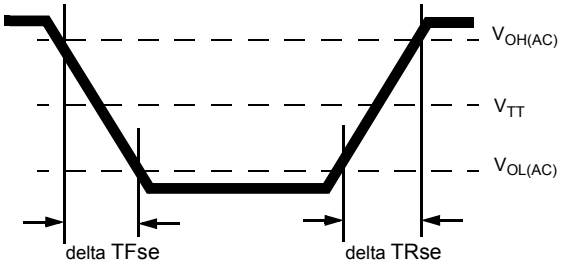


Figure 182 — Single-ended Output Slew Rate Definition

Table 77 — Single-ended output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Single ended output slew rate	SRQse	4	9	4	9	4	9	4	9	TBD	TBD	TBD	TBD	V/ns

Description: SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
se: Single-ended Signals
For Ron = RZQ/7 setting

NOTE 1 In two cases, a maximum slew rate of 12 V/ns applies for a single DQ signal within a byte lane.
-Case 1 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are static (i.e. they stay at either high or low).
-Case 2 is defined for a single DQ signal within a byte lane which is switching into a certain direction (either from high to low or low to high) while all remaining DQ signals in the same byte lane are switching into the opposite direction (i.e. from low to high or high to low respectively). For the remaining DQ signal switching into the opposite direction, the regular maximum limit of 9 V/ns applies

8.5 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between VOLdiff(AC) and VOHdiff(AC) for differential signals as shown in Table 78 and Figure 183.

Table 78 — Differential output slew rate definition

Description	Measured		Defined by
	From	To	
Differential output slew rate for rising edge	$V_{OLdiff}(AC)$	$V_{OHdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TRdiff
Differential output slew rate for falling edge	$V_{OHdiff}(AC)$	$V_{OLdiff}(AC)$	$[V_{OHdiff}(AC)-V_{OLdiff}(AC)]$ / Delta TFdiff

NOTE :
1. Output slew rate is verified by design and characterization, and may not be subject to production test.

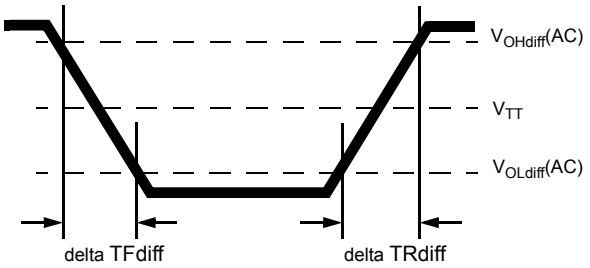


Figure 183 — Differential Output Slew Rate Definition

Table 79 — Differential output slew rate

Parameter	Symbol	DDR4-1600		DDR4-1866		DDR4-2133		DDR4-2400		DDR4-2666		DDR4-3200		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Differential output slew rate	SRQdiff	8	18	8	18	8	18	8	18	TBD	TBD	TBD	TBD	V/ns

Description:
SR: Slew Rate
Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
diff: Differential Signals
For Ron = RZQ/7 setting

9 Speed Bin

Table 80 — DDR4-1600 Speed Bins and Operations

Speed Bin				DDR4-1600J (Optional)		DDR4-1600K		DDR4-1600L		Unit	NOTE
CL-nRCD-nRP				10-10-10		11-11-11		12-12-12			
Parameter			Symbol	min	max	min	max	min	max		
Internal read command to first data			tAA	12.50	18.00	13.75[14] (13.50)[5,12]	18.00	15.00	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	tAA(min) + 2nCK	tAA(max) +2nCK	tAA(min) + 2nCK	tAA(max) +2nCK	ns	
ACT to internal read or write delay time			tRCD	12.50	-	13.75 (13.50)[5,12]	-	15.00	-	ns	
PRE command period			tRP	12.50	-	13.75 (13.50)[5,12]	-	15.00	-	ns	
ACT to PRE command period			tRAS	35	9 x tREFI	35	9 x tREFI	35	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	47.5	-	48.75 (48.50)[5,12]	-	50	-	ns	
	Normal	Read DBI									
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	1.5	1.6	Reserved		ns	1,2,3,4,11,14
				(Optional)[5]		(Optional)[5,12]					
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	Reserved		1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	1.25	<1.5	Reserved		Reserved		ns	1,2,3,4
	CL = 11	CL = 13	tCK(AVG)	1.25	<1.5	1.25	<1.5	Reserved		ns	1,2,3,4
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns	1,2,3
Supported CL Settings				(9),10,11,12		(9),11,12		10,12		nCK	13,14
Supported CL Settings with read DBI				(11),12,13,14		(11),13,14		11,14		nCK	13
Supported CWL Settings				9,11		9,11		9,11		nCK	

Table 81 — DDR4-1866 Speed Bins and Operations

Speed Bin				DDR4-1866L (Optional)		DDR4-1866M		DDR4-1866N		Unit	NOTE
CL-nRCD-nRP				12-12-12		13-13-13		14-14-14			
Parameter			Symbol	min	max	min	max	min	max		
Internal read command to first data			tAA	12.85	18.00	13.92[14] (13.50)[5,12]	18.00	15.00	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	tAA(min) + 2nCK	tAA(max) +2nCK	tAA(min) + 2nCK	tAA(max) +2nCK	tAA(min) + 2nCK	tAA(max) +2nCK	ns	
ACT to internal read or write delay time			tRCD	12.85	-	13.92 (13.50)[5,12]	-	15.00	-	ns	
PRE command period			tRP	12.85	-	13.92 (13.50)[5,12]	-	15.00	-	ns	
ACT to PRE command period			tRAS	34	9 x tREFI	34	9 x tREFI	34	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	46.85	-	47.92 (47.50)[5,12]	-	49.00	-	ns	
	Normal	Read DBI									
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	1.5	1.6	Reserved		ns	1,2,3,4,11,14
			tCK(AVG)	(Optional)[5]		(Optional)[5,12]					
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	Reserved		1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		Reserved		Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	Reserved		1.25	<1.5	Reserved		ns	1,2,3,4,6
						(Optional)[5,12]					
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns	1,2,3,6
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	1.071	<1.25	Reserved		Reserved		ns	1,2,3,4
	CL = 13	CL = 15	tCK(AVG)	1.071	<1.25	1.071	<1.25	Reserved		ns	1,2,3,4
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns	1,2,3
Supported CL Settings				9,10,11,12 ,13,14		9,11,12,13,14		10,12,14		nCK	13,14
Supported CL Settings with read DBI				(11),12,13,14 ,14,16		11,13,14 ,15,16		12,14,16		nCK	13
Supported CWL Settings				9,10,11,12		9,10,11,12		9,10,11,12		nCK	

Table 82 — DDR4-2133 Speed Bins and Operations

Speed Bin				DDR4-2133N (Optional)		DDR4-2133P		DDR4-2133R		Unit	NOTE
CL-nRCD-nRP				14-14-14		15-15-15		16-16-16			
Parameter			Symbol	min	max	min	max	min	max		
Internal read command to first data			tAA	13.13	18.00	14.06[14] (13.50)[5,12]	18.00	15.00	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	TBD	TBD	TBD	TBD	TBD	TBD	ns	
ACT to internal read or write delay time			tRCD	13.13	-	14.06 (13.50)[5,12]	-	15.00	-	ns	
PRE command period			tRP	13.13	-	14.06 (13.50)[5,12]	-	15.00	-	ns	
ACT to PRE command period			tRAS	33	9 x tREFI	33	9 x tREFI	33	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	46.13	-	47.06 (46.50)[5,12]	-	48.00	-	ns	
	Normal	Read DBI									
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	1.5	1.6	Reserved		ns	1,2,3,4,11,14
			tCK(AVG)	(Optional)[5]		(Optional)[5,12]					
	CL = 10	CL = 12	tCK(AVG)	1.5	1.6	Reserved		1.5	1.6	ns	1,2,3,11
CWL = 9,11	CL = 11	CL = 13	tCK(AVG)	Reserved		1.25	<1.5	Reserved		ns	1,2,3,4,7
			tCK(AVG)			(Optional)[5,12]					
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns	1,2,3,7
CWL = 10,12	CL = 13	CL = 15	tCK(AVG)	Reserved		1.071	<1.25	Reserved		ns	1,2,3,4,7
						(Optional)[5,12]					
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns	1,2,3,7
CWL = 11,14	CL = 14	CL = TBD	tCK(AVG)	0.938	<1.071	Reserved		Reserved		ns	1,2,3,4
	CL = 15	CL = TBD	tCK(AVG)	0.938	<1.071	0.938	<1.071	Reserved		ns	1,2,3,4
	CL = 16	CL = TBD	tCK(AVG)	0.938	<1.071	0.938	<1.071	0.938	<1.071	ns	1,2,3
Supported CL Settings				(9),10,12,14,15,16		(9),(11),12,(13),14,15,16		10,12,14,16		nCK	13,14
Supported CL Settings with read DBI				TBD		TBD		TBD		nCK	
Supported CWL Settings				9,10,11,12,14		9,10,11,12,14		9,10,11,12,14		nCK	

Table 83 — DDR4-2400 Speed Bins and Operations

Speed Bin				DDR4-2400P (Optional)		DDR4-2400R		DDR4-2400U		Unit	NOTE
CL-nRCD-nRP				15-15-15		16-16-16		18-18-18			
Parameter			Symbol	min	max	min	max	min	max		
Internal read command to first data			tAA	12.50	18.00	13.32	18.00	15.00	18.00	ns	
Internal read command to first data with read DBI enabled			tAA_DBI	TBD	TBD	TBD	TBD	TBD	TBD	ns	
ACT to internal read or write delay time			tRCD	12.50	-	13.32	-	15.00	-	ns	
PRE command period			tRP	12.50	-	13.32	-	15.00	-	ns	
ACT to PRE command period			tRAS	32	9 x tREFI	32	9 x tREFI	32	9 x tREFI	ns	
ACT to ACT or REF command period			tRC	44.50	-	45.32	-	47.00	-	ns	
	Normal	Read DBI									
CWL = 9	CL = 9	CL = 11 (Optional)[5]	tCK(AVG)	1.5	1.6	1.5	1.6	Reserved		ns	1,2,3,4,11
				(Optional)[5]		(Optional)[5,12]					
	CL = 10	CL = 12		1.5	1.6	Reserved		1.5	1.6	ns	1,2,3,4,11
CWL = 9,11	CL = 10	CL = 12	tCK(AVG)	Reserved		Reserved		Reserved		ns	4
	CL = 11	CL = 13	tCK(AVG)	Reserved		1.25	<1.5	Reserved		ns	1,2,3,4,8
	CL = 12	CL = 14	tCK(AVG)	1.25	<1.5	1.25	<1.5	1.25	<1.5	ns	1,2,3,8
CWL = 10,12	CL = 12	CL = 14	tCK(AVG)	Reserved		Reserved		Reserved		ns	4
	CL = 13	CL = 15	tCK(AVG)	Reserved		1.071	<1.25	Reserved		ns	1,2,3,4,8
	CL = 14	CL = 16	tCK(AVG)	1.071	<1.25	1.071	<1.25	1.071	<1.25	ns	1,2,3,8
CWL = 11,14	CL = 14	CL = TBD	tCK(AVG)	Reserved		Reserved		Reserved		ns	4
	CL = 15	CL = TBD	tCK(AVG)	Reserved		0.938	<1.071	Reserved		ns	1,2,3,4,8
	CL = 16	CL = TBD	tCK(AVG)	0.938	<1.071	0.938	<1.071	0.938	<1.071	ns	1,2,3,8
CWL = 12.16	CL = 15	CL = TBD	tCK(AVG)	0.833	<0.938	Reserved		Reserved		ns	1,2,3,4
	CL = 16	CL = TBD	tCK(AVG)	0.833	<0.938	0.833	<0.938	Reserved		ns	1,2,3,4
	CL = 18	CL = TBD	tCK(AVG)	0.833	<0.938	0.833	<0.938	0.833	<0.938	ns	1,2,3
Supported CL Settings				(9),10,12,14,15,16,18		11,12,13,14,15,16,18		10,12,14,16,18		nCK	13
Supported CL Settings with read DBI				TBD		TBD		TBD		nCK	
Supported CWL Settings				9,10,11,12,14,16		9,10,11,12,14,16		9,10,11,12,14,16		nCK	

9.1 Speed Bin Table Note

Absolute Specification
- VDDQ = VDD = 1.20V +/- 0.06 V
- VPP = 2.5V +0.25/-0.125 V
- The values defined with above-mentioned table are DLL ON case.
- DDR4-1600, 1866, 2133 and 2400 Speed Bin Tables are valid only when Geardown Mode is disabled.

1. The CL setting and CWL setting result in tCK(avg).MIN and tCK(avg).MAX requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (1.5, 1.25, 1.071, 0.938 or 0.833 ns) when calculating CL [nCK] = tAA [ns] / tCK(avg) [ns], rounding up to the next 'Supported CL', where tAA = 12.5ns and tCK(avg) = 1.3 ns should only be used for CL = 10 calculation.
3. tCK(avg).MAX limits: Calculate tCK(avg) = tAA.MAX / CL SELECTED and round the resulting tCK(avg) down to the next valid speed bin (i.e. 1.5ns or 1.25ns or 1.071 ns or 0.938 ns or 0.833 ns). This result is tCK(avg).MAX corresponding to CL SELECTED.
4. 'Reserved' settings are not allowed. User must program a different value.
5. 'Optional' settings allow certain devices in the industry to support this setting, however, it is not a mandatory feature. Refer to supplier's data sheet and/or the DIMM SPD information if and how this setting is supported.
6. Any DDR4-1866 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
7. Any DDR4-2133 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
8. Any DDR4-2400 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/Characterization.
9. Reserved for DDR4-2666 speed bin.
10. Reserved for DDR4-3200 speed bin.
11. DDR4-1600 AC timing apply if DRAM operates at lower than 1600 MT/s data rate.
12 .For devices supporting optional down binning to CL=9, CL=11 and CL=13, tAA/tRCD/tRPmin must be 13.5ns or lower. SPD settings must be programmed to match.For example, DDR4-1600K devices supporting down binning to 1333MT/s should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).DDR4-1866M devices supporting down binning to 1333MT/s or DDR4-1600K should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).DDR4-2133P devices supporting down binning to 1333MT/s or DDR4-1600K or DDR4-1866M should program 13.5ns in SPD bytes for tAAmin (Byte 24), tRCDmin (Byte 25), and tRPmin (Byte 26).tRCmin (Byte 27, 29) also should be programmed accordingly. For example, 48.5ns (tRASmin + tRPmin = 35ns+ 13.5ns) is set to supporting optional down binning CL=9 and CL=11.
13. CL number in parentheses, it means that these numbers are optional.
14. DDR4 SDRAM supports CL=9 as long as a system meets tAA(min).

10 IDD and IDDQ Specification Parameters and Test conditions

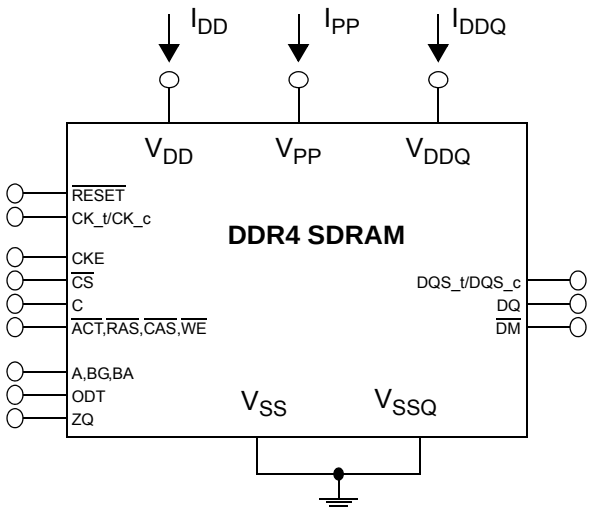
10.1 IDD, IPP and IDDQ Measurement Conditions

In this chapter, IDD, IPP and IDDQ measurement conditions such as test load and patterns are defined. Figure 184 shows the setup and test load for IDD, IPP and IDDQ measurements.

- IDD currents (such as IDD0, IDD0A, IDD1, IDD1A, IDD2N, IDD2NA, IDD2NL, IDD2NT, IDD2P, IDD2Q, IDD3N, IDD3NA, IDD3P, IDD4R, IDD4RA, IDD4W, IDD4WA, IDD5B, IDD5F2, IDD5F4, IDD6N, IDD6E, IDD6R, IDD6A, IDD7 and IDD8) are measured as time-averaged currents with all VDD balls of the DDR4 SDRAM under test tied together. Any IPP or IDDQ current is not included in IDD currents.
- IPP currents have the same definition as IDD except that the current on the VPP supply is measured.
- IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR4 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
  Attention: IDDQ values cannot be directly used to calculate IO power of the DDR4 SDRAM. They can be used to support correlation of simulated IO power to actual IO power as outlined in Figure 185. In DRAM module application, IDDQ cannot be measured separately since VDD and VDDQ are using one merged-power layer in Module PCB.

For IDD, IPP and IDDQ measurements, the following definitions apply:

- “0” and “LOW” is defined as VIN <= VILAC(max).
- “1” and “HIGH” is defined as VIN >= VIHAC(min).
- “MID-LEVEL” is defined as inputs are VREF = VDD / 2.
- Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns are provided in Table 84.
- Basic IDD, IPP and IDDQ Measurement Conditions are described in Table 85.
- Detailed IDD, IPP and IDDQ Measurement-Loop Patterns are described in Table 86 through Table 94.
- IDD Measurements are done after properly initializing the DDR4 SDRAM. This includes but is not limited to setting
  RON = RZQ/7 (34 Ohm in MR1);
  RTT_NOM = RZQ/6 (40 Ohm in MR1);
  RTT_WR = RZQ/2 (120 Ohm in MR2);
  RTT_PARK = Disable;
  Qoff = 0_B (Output Buffer enabled) in MR1;
  TDQS_t disabled in MR1;
  CRC disabled in MR2;
  CA parity feature disabled in MR5;
  Gear down mode disabled in MR3
  Read/Write DBI disabled in MR5;
  DM disabled in MR5
- Attention: The IDD, IPP and IDDQ Measurement-Loop Patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
- Define D = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, LOW, LOW, LOW, LOW}
- Define D# = {CS_n, ACT_n, RAS_n, CAS_n, WE_n } := {HIGH, HIGH, HIGH, HIGH, HIGH}



NOTE:
1. DIMM level Output test load condition may be different from above

Figure 184 — Measurement Setup and Test Load for IDD, IPP and IDDQ Measurements

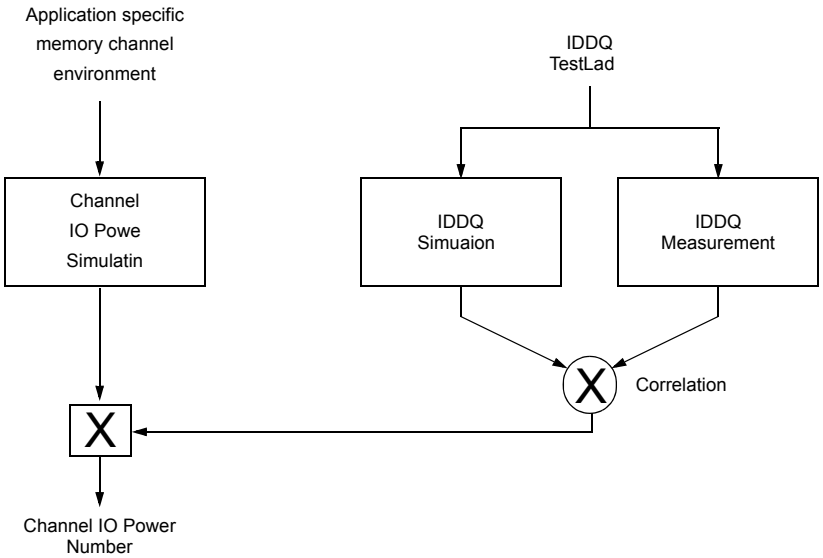


Figure 185 — Correlation from simulated Channel IO Power to actual Channel IO Power supported by IDDQ Measurement.

Table 84 — Timings used for IDD, IPP and IDDQ Measurement-Loop Patterns

Symbol		DDR4-1600			DDR4-1866			DDR4-2133			DDR4-2400			Unit
		10-10-10	11-11-11	12-12-12	12-12-12	13-13-13	14-14-14	14-14-14	15-15-15	16-16-16	15-15-15	16-16-16	18-18-18	
tCK		1.25			1.071			0.938			0.833			ns
CL		10	11	12	12	13	14	14	15	16	15	16	18	nCK
CWL		9	11	11	10	12	12	11	14	14	12	16	16	nCK
nRCD		10	11	12	12	13	14	14	15	16	15	16	18	nCK
nRC		38	39	40	44	45	46	50	51	52	54	55	57	nCK
nRAS		28			32			36			39			nCK
nRP		10	11	12	12	13	14	14	15	16	15	16	18	nCK
nFAW	x4	16			16			16			16			nCK
	x8	20			22			23			26			nCK
	x16	28			28			32			36			
nRRDS	x4	4			4			4			4			nCK
	x8	4			4			4			4			nCK
	x16	5			5			6			7			
nRRDL	x4	5			5			6			6			nCK
	x8	5			5			6			6			nCK
	x16	6			6			7			8			
tCCD_S		4			4			4			4			nCK
tCCD_L		5			5			6			6			nCK
tWTR_S		2			3			3			3			nCK
tWTR_L		6			7			8			9			nCK
nRFC 2Gb		128			150			171			193			nCK
nRFC 4Gb		208			243			278			313			nCK
nRFC 8Gb		280			327			374			421			nCK
nRFC 16Gb		TBD			TBD			TBD			TBD			nCK
TBD														nCK

Table 85 — Basic IDD, IPP and IDDQ Measurement Conditions

Symbol	Description
IDD0	**Operating One Bank Active-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n:** High between ACT and PRE; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 3 on page 9; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 3 on page 9); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 3 on page 9
IDD0A	**Operating One Bank Active-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD0
IPP0	**Operating One Bank Active-Precharge IPP Current** **Same condition with IDD0**
IDD1	**Operating One Bank Active-Read-Precharge Current (AL=0)** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: High between ACT, RD and PRE; **Command, Address, Bank Group Address, Bank Address Inputs, Data IO:** partially toggling according to Table 4 on page 10; **DM_n:** stable at 1; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 4 on page 10); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 4 on page 10
IDD1A	**Operating One Bank Active-Read-Precharge Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD1
IPP1	**Operating One Bank Active-Read-Precharge IPP Current** **Same condition with IDD1**
IDD2N	**Precharge Standby Current (AL=0)** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 5 on page 11; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 5 on page 11
IDD2NA	**Precharge Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD2N
IPP2N	**Precharge Standby IPP Current** **Same condition with IDD2N**
IDD2NT	**Precharge Standby ODT Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 6 on page 11; **Data IO: VSSQ**; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** toggling according to Table 6 on page 11; **Pattern Details:** see Table 6 on page 11
IDDQ2NT (Optional)	**Precharge Standby ODT IDDQ Current** Same definition like for IDD2NT, however measuring IDDQ current instead of IDD current
IDD2NL	**Precharge Standby Current with CAL enabled** Same definition like for IDD2N, CAL enabled[3]
IDD2NG	**Precharge Standby Current with Gear Down mode enabled** Same definition like for IDD2N, Gear Down mode enabled[3]
IDD2ND	**Precharge Standby Current with DLL disabled** Same definition like for IDD2N, DLL disabled[3]
IDD2N_par	**Precharge Standby Current with CA parity enabled** Same definition like for IDD2N, CA parity enabled[3]
IDD2P	**Precharge Power-Down Current CKE:** Low; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP2P	**Precharge Power-Down IPP Current** **Same condition with IDD2P**
IDD2Q	**Precharge Quiet Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0

IDD3N	**Active Standby Current** **CKE**: High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 5 on page 11; **Data IO:** VDDQ; **DM_n:** stable at 1;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 5 on page 11
IDD3NA	**Active Standby Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD3N
IPP3N	**Active Standby IPP Current** **Same condition with IDD3N**
IDD3P	**Active Power-Down Current** **CKE:** Low; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: stable at 1; **Command, Address, Bank Group Address, Bank Address Inputs:** stable at 0; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0
IPP3P	**Active Power-Down IPP Current** **Same condition with IDD3P**
IDD4R	**Operating Burst Read Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[2]; **AL:** 0; **CS_n**: High between RD; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 7 on page 12; **Data IO:** seamless read data burst with different data between one burst and the next one according to Table 7 on page 12; **DM_n**: stable at 1; **Bank Activity:** all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 7 on page 12); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 7 on page 12
IDD4RA	**Operating Burst Read Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4R
IDD4RB	**Operating Burst Read Current with Read DBI** **Read DBI enabled[3], Other conditions:** see IDD4R
IPP4R	**Operating Burst Read IPP Current** **Same condition with IDD4R**
IDDQ4R (Optional)	**Operating Burst Read IDDQ Current** Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
IDDQ4RB (Optional)	**Operating Burst Read IDDQ Current with Read DBI** Same definition like for IDD4RB, however measuring IDDQ current instead of IDD current
IDD4W	**Operating Burst Write Current** **CKE:** High; **External clock:** On; **tCK, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: High between WR; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 8 on page 12; **Data IO:** seamless write data burst with different data between one burst and the next one according to Table 8 on page 12; **DM_n:** stable at 1; **Bank Activity:** all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... (see Table 8 on page 12); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** see Table 8 on page 12
IDD4WA	**Operating Burst Write Current (AL=CL-1)** **AL = CL-1, Other conditions:** see IDD4W
IDD4WB	**Operating Burst Write Current with Write DBI** **Write DBI enabled[3], Other conditions:** see IDD4W
IDD4WC	**Operating Burst Write Current with Write CRC** **Write CRC enabled[3], Other conditions:** see IDD4W
IDD4W_par	**Operating Burst Write Current with CA Parity** **CA Parity enabled[3], Other conditions:** see IDD4W
IPP4W	**Operating Burst Write IPP Current** **Same condition with IDD4W**
IDD5B	**Burst Refresh Current (1X REF)** **CKE:** High; **External clock:** On; **tCK, CL, nRFC**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n**: High between REF; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 9 on page 13; **Data IO:** VDDQ; **DM_n:** stable at 1; **Bank Activity:** REF command every nRFC (see Table 9 on page 13); **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 9 on page 13
IPP5B	**Burst Refresh Write IPP Current (1X REF)** **Same condition with IDD5B**
IDD5F2	**Burst Refresh Current (2X REF)** **tRFC=tRFC_x2, Other conditions:** see IDD5B
IPP5F2	**Burst Refresh Write IPP Current (2X REF)** **Same condition with IDD5F2**

IDD5F4	**Burst Refresh Current (4X REF)** **tRFC=tRFC_x4, Other conditions:** see IDD5B
IPP5F4	**Burst Refresh Write IPP Current (4X REF)** **Same condition with IDD5F4**
IDD6N	**Self Refresh Current: Normal Temperature Range** T_{CASE}**:** 0 - 85°C; **Low Power Array Self Refresh (LP ASR)** : Normal[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n:** stable at 1; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6N	**Self Refresh IPP Current: Normal Temperature Range** **Same condition with IDD6N**
IDD6E	**Self-Refresh Current: Extended Temperature Range**) T_{CASE}**:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Extended[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c: LOW; **CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LE**VEL**
IPP6E	**Self Refresh IPP Current: Extended Temperature Range** **Same condition with IDD6E**
IDD6R	**Self-Refresh Current: Reduced Temperature Range** T_{CASE}**:** 0 - TBD (~35-45)°C; **Low Power Array Self Refresh (LP ASR)** : Reduced[4]; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6R	**Self Refresh IPP Current: Reduced Temperature Range** **Same condition with IDD6R**
IDD6A	**Auto Self-Refresh Current** T_{CASE}**:** 0 - 95°C; **Low Power Array Self Refresh (LP ASR)** : Auto[4];**Partial Array Self-Refresh (PASR)**: Full Array; **CKE:** Low; **External clock:** Off; CK_t and CK_c#: LOW; **CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** 0; **CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO:** High; **DM_n**:stable at 1; **Bank Activity:** Auto Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** MID-LEVEL
IPP6A	**Auto Self-Refresh IPP Current** **Same condition with IDD6A**
IDD7	**Operating Bank Interleave Read Current** **CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL**: see Table 1 on page 4; **BL:** 8[1]; **AL:** CL-1; **CS_n**: High between ACT and RDA; **Command, Address, Bank Group Address, Bank Address Inputs:** partially toggling according to Table 10 on page 14; **Data IO:** read data bursts with different data between one burst and the next one according to Table 10 on page 14; **DM_n:** stable at 1; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing, see Table 10 on page 14; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** see Table 10 on page 14
IPP7	**Operating Bank Interleave Read IPP Current** **Same condition with IDD7**
IDD8	**Maximum Power Down Current** **TBD**
IPP8	**Maximum Power Down IPP Current** **Same condition with IDD8**

NOTE 1 Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
NOTE 2 Output Buffer Enable
- set MR1 [A12 = 0] : Qoff = Output buffer enabled
- set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7

RTT_Nom enable
- set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6

RTT_WR enable
- set MR2 [A10:9 = 01] : RTT_WR = RZQ/2

RTT_PARK disable
- set MR5 [A8:6 = 000]

NOTE 3 CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s
010] : 1866MT/s, 2133MT/s
011] : 2400MT/s
Gear Down mode enabled :set MR3 [A3 = 1] : 1/4 Rate
DLL disabled : set MR1 [A0 = 0]
CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s
010] : 2400MT/s
Read DBI enabled : set MR5 [A12 = 1]
Write DBI enabled : set :MR5 [A11 = 1]

NOTE 4 Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal
01] : Reduced Temperature range
10] : Extended Temperature range
11] : Auto Self Refresh

Table 86 — IDD0, IDD0A and IPP0 Measurement-Loop Pattern[1]

CK_t /CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/ A16	CAS_n/ A15	WE_n/ A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	-
			3,4	D_#, D_#	1	1	1	1	1	0	0	3[2]	3	0	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	PRE	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 1** instead																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		7	7*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
		8	8*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	9*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
		11	11*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
		13	13*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 2** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead																
		15	15*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 DQ signals are VDDQ.

Table 87 — IDD1, IDD1A and IPP1 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			1, 2	D, D	1	0	0	0	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			3, 4	D#, D#	1	1	1	1	1	0	0	3[b]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern 1...4 until nRCD - AL - 1, truncate if necessary																
			nRCD -AL	**RD**	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat pattern 1...4 until nRC - 1, truncate if necessary																
		1	1*nRC + 0	**ACT**	0	0	0	1	1	0	0	1	**1**	**0**	0	0	0	0	0	-
			1*nRC + 1, 2	D, D	1	0	0	0	0	0	**0**	**0**	0	0	0	0	0	0	0	-
			1*nRC + 3, 4	D#, D#	1	1	1	1	1	0	**0**	3[b]	**3**	**0**	0	0	7	F	0	-
			...	repeat pattern nRC + 1...4 until 1*nRC + nRAS - 1, truncate if necessary																
			1*nRC + nRCD - AL	**RD**	0	1	1	0	1	0	**0**	**1**	1	0	0	0	0	**0**	**0**	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 1...4 until nRAS - 1, truncate if necessary																
			1*nRC + nRAS	**PRE**	0	1	0	1	0	0	0	0	**0**	**0**	0	0	0	0	0	-
			...	repeat nRC + 1...4 until 2*nRC - 1, truncate if necessary																
		2	2*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	3*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	4*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	5*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	6*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		8	7*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
		9	9*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																For x4 and x8 only
		10	10*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
		11	11*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
		12	12*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
		13	13*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
		14	14*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 2 instead																
		15	15*nRC	repeat Sub-Loop 1, use **BG[1:0][2] = 2, BA[1:0] =** 3 instead																
		16	16*nRC	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] =** 0 instead																

NOTE 1 DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

Table 88 — IDD2N, IDD2NA, IDD2NL, IDD2NG, IDD2ND, IDD2N_par, IPP2,IDD3N, IDD3NA and IDD3P Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	0
			2	D#, D#	1	1	1	1	1	0	0	**3[2]**	**3**	0	0	0	**7**	**F**	0	0
			3	D#, D#	1	1	1	1	1	0	0	**3[2]**	**3**	0	0	0	**7**	**F**	0	0
		1	4-7	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0][2] = 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, use **BG[1:0][2] = 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 0** instead																
		9	36-39	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0][2] = 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, use **BG[1:0][2] = 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 DQ signals are VDDQ.

Table 89 — IDD2NT and IDDQ2NT Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			1	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4-7	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
		2	8-11	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, but ODT = 0 and **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 0, but ODT = 1 and **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 DQ signals are VDDQ.

Table 90 — IDD4R, IDDR4RA, IDD4RB and IDDQ4R Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**RD**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**RD**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are used according to RD Commands, otherwise VDDQ.
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 Burst Sequence driven on each DQ signal by Read Command.

Table 91 — IDD4W, IDD4WA, IDD4WB and IDD4W_par Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**WR**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2,3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		1	4	**WR**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			5	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			6,7	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	8-11	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	12-15	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	16-19	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	20-23	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	24-27	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	28-31	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	32-35	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	36-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	40-43	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	44-47	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	48-51	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	52-55	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	56-59	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	60-63	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are used according to WR Commands, otherwise VDDQ.
NOTE 2 BG1 is don't care for x16 device
NOTE 3 C[2:0] are used only for 3DS device
NOTE 4 Burst Sequence driven on each DQ signal by Write Command.

Table 92 — IDD4WC Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][c]	BG[1:0][b]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[d]
toggling	Static High	0	0	**WR**	0	1	1	0	1	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF D8=CRC**
			1,2	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3,4	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			5	**WR**	0	1	1	0	1	0	0	**1**	**1**	0	0	0	**7**	**F**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00 D8=CRC**
			6,7	D, D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			8,9	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
		2	10-14	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	15-19	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	20-24	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		5	25-29	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		6	30-34	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		7	35-39	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		8	40-44	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		9	45-49	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		10	50-54	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		11	55-59	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		12	60-64	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		13	65-69	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		14	70-74	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		15	75-79	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device.
NOTE 3 C[2:0] are used only for 3DS device.
NOTE 4 Burst Sequence driven on each DQ signal by Write Command.

Table 93 — IDD5B Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**REF**	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
		1	1	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			4	D#, D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			4-7	repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 1** instead																
			8-11	repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
			12-15	repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
			16-19	repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
			20-23	repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
			24-27	repeat pattern 1...4, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
			28-31	repeat pattern 1...4, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
			32-35	repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
			36-39	repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
			40-43	repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
			44-47	repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
			48-51	repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
			52-55	repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
			56-59	repeat pattern 1...4, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
			60-63	repeat pattern 1...4, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																
		2	64 ... nRFC - 1	repeat Sub-Loop 1, Truncate, if necessary																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device.
NOTE 3 C[2:0] are used only for 3DS device.
NOTE 4 DQ signals are VDDQ.

Table 94 — IDD7 Measurement-Loop Pattern[1]

CK_t, CK_c	CKE	Sub-Loop	Cycle Number	Command	CS_n	ACT_n	RAS_n/A16	CAS_n/A15	WE_n/A14	ODT	C[2:0][3]	BG[1:0][2]	BA[1:0]	A12/BC_n	A[17,13,11]	A[10]/AP	A[9:7]	A[6:3]	A[2:0]	Data[4]
toggling	Static High	0	0	**ACT**	0	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	**-**
			1	**RDA**	0	1	1	0	1	0		**0**	**0**	0	0	1	**0**	**0**	0	**D0=00, D1=FF D2=FF, D3=00 D4=FF, D5=00 D6=00, D7=FF**
			2	D	1	0	0	0	0	0	0	**0**	**0**	0	0	0	**0**	**0**	0	-
			3	D#	1	1	1	1	1	0	0	**3**[2]	**3**	0	0	0	**7**	**F**	0	-
			...	repeat pattern 2...3 until nRRD - 1, if nRCD > 4. Truncate if necessary																
		1	nRRD	**ACT**	0	0	0	0	0	0	0	**1**	**1**	0	0	0	**0**	**0**	0	**-**
			nRRD + 1	**RDA**	0	1	1	0	1	0		**1**	**1**	0	0	1	**0**	**0**	0	**D0=FF, D1=00 D2=00, D3=FF D4=00, D5=FF D6=FF, D7=00**
			...	repeat pattern 2 ... 3 until 2*nRRD - 1, if nRCD > 4. Truncate if necessary																
		2	2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 2** instead																
		3	3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 3** instead																
		4	4*nRRD	repeat pattern 2 ... 3 until nFAW - 1, if nFAW > 4*nRCD. Truncate if necessary																
		5	nFAW	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 1** instead																
		6	nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 2** instead																
		7	nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 0, BA[1:0] = 3** instead																
		8	nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 1, BA[1:0] = 0** instead																
		9	nFAW + 4*nRRD	repeat Sub-Loop 4																
		10	2*nFAW	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 0** instead																For x4 and x8 only
		11	2*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 1** instead																
		12	2*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 2** instead																
		13	2*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 3** instead																
		14	2*nFAW + 4*nRRD	repeat Sub-Loop 4																
		15	3*nFAW	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 1** instead																
		16	3*nFAW + nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 2** instead																
		17	3*nFAW + 2*nRRD	repeat Sub-Loop 0, use **BG[1:0]**[2] **= 2, BA[1:0] = 3** instead																
		18	3*nFAW + 3*nRRD	repeat Sub-Loop 1, use **BG[1:0]**[2] **= 3, BA[1:0] = 0** instead																
		19	3*nFAW + 4*nRRD	repeat Sub-Loop 4																
		20	4*nFAW	repeat pattern 2 ... 3 until nRC - 1, if nRC > 4*nFAW. Truncate if necessary																

NOTE 1 DQS_t, DQS_c are VDDQ.
NOTE 2 BG1 is don't care for x16 device.
NOTE 3 C[2:0] are used only for 3DS device.
NOTE 4 Burst Sequence driven on each DQ signal by Read Command. Outside burst operation, DQ signals are VDDQ.

10.2 IDD Specifications

IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted. IDD and IPP values are for full operating range of voltage and temperature unless otherwise noted.

Table 95 — I_{DD} and I_{DDQ} Specification Example

Speed Grade Bin				
Symbol	**IDD Max.**	**IPP Max.**	**Unit**	**NOTE**
I_{DD0}			mA	
I_{DD0A}			mA	
I_{DD1}			mA	
I_{DD1A}			mA	
I_{DD2N}			mA	
I_{DD2NA}			mA	
I_{DD2NT}			mA	
I_{DDQ2NT}			mA	
I_{DD2NL}			mA	
I_{DD2NG}			mA	
I_{DD2ND}			mA	
I_{DD2N_par}			mA	
I_{DD2P}			mA	
I_{DD2Q}			mA	
I_{DD3N}			mA	
I_{DD3NA}			mA	
I_{DD3P}			mA	
I_{DD4R}			mA	
I_{DD4RA}			mA	
I_{DD4RB}			mA	
I_{DDQ4R}			mA	
I_{DDQ4RB}			mA	
I_{DD4W}			mA	
I_{DD4WA}			mA	
I_{DD4WB}			mA	
I_{DD4WC}			mA	
I_{DD4W_par}			mA	
I_{DD5B}			mA	
I_{DD5F2}			mA	
I_{DD5F4}			mA	
I_{DD6N}			mA	
I_{DD6E}			mA	
I_{DD6N}			mA	
I_{DD6E}[1]			mA	
I_{DD6R}			mA	
I_{DD6A}			mA	
I_{DD7}			mA	
I_{DD8}			mA	

NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

Table 96 — I_{PP} Specification Example

Speed Grade Bin			Unit	NOTE
Symbol	IDD Max.	IPP Max.		
I_{PP0}			mA	
I_{PP1}			mA	
I_{PP2N}			mA	
I_{PP2P}			mA	
I_{PP3N}			mA	
I_{PP3P}			mA	
I_{PP4R}			mA	
I_{PP4W}			mA	
I_{PP5B}			mA	
I_{PP5F2}			mA	
I_{PP5F4}			mA	
I_{PP5TC}			mA	
I_{PP6N}			mA	
I_{PP6E}			mA	
I_{PP6N}			mA	
I_{PP6E}[1]			mA	
I_{PP6R}			mA	
I_{PP6A}			mA	
I_{PP7}			mA	
I_{PP8}			mA	

NOTE 1 Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR4 SDRAM devices support the following options or requirements referred to in this material.

Table 97 — I_{DD6} Specification

Symbol	Temperature Range	Value	Unit	NOTE
I_{DD6N}	0 - 85 ^{o}C		mA	3,4
I_{DD6E}	0 - 95 ^{o}C		mA	4,5,6
I_{DD6R}	0 - 45°C		mA	4,6,9
I_{DD6A}	0 ^{o}C ~ T_a		mA	4,6,7,8
	T_b ~ T_y		mA	4,6,7,8
	T_z ~ $T_{OPERmax}$		mA	4,6,7,8

NOTE 1 Some I_{DD} currents are higher for x16 organization due to larger page-size architecture.
NOTE 2 Max. values for I_{DD} currents considering worst case conditions of process, temperature and voltage.
NOTE 3 Applicable for MR2 settings A6=0 and A7=0.
NOTE 4 Supplier data sheets include a max value for I_{DD6}.
NOTE 5 Applicable for MR2 settings A6=0 and A7=1. I_{DD6ET} is only specified for devices which support the Extended Temperature Range feature.
NOTE 6 Refer to the supplier data sheet for the value specification method (e.g. max, typical) for I_{DD6ET} and I_{DD6TC}
NOTE 7 Applicable for MR2 settings A6=1 and A7=0. I_{DD6TC} is only specified for devices which support the Auto Self Refresh feature.
NOTE 8 The number of discrete temperature ranges supported and the associated Ta - Tz values are supplier/design specific. Temperature ranges are specified for all supported values of T_{OPER}. Refer to supplier data sheet for more information.
NOTE 9 Applicable for MR2 settings TBD. IDD6R is verified by design and characterization, and may not be subject to production test

11 Input/Output Capacitance

Table 98 — Silicon pad I/O Capacitance

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400,2666		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max		
C_{IO}	Input/output capacitance	0.7	1.4	0.7	1.3	TBD	TBD	pF	1,2,3
C_{DIO}	Input/output capacitance delta	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,3,11
C_{DDQS}	Input/output capacitance delta DQS_t and DQS_c		0.05		0.05	TBD	TBD	pF	1,2,3,5
C_{CK}	Input capacitance, CK_t and CK_c	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3
C_{DCK}	Input capacitance delta CK_t and CK_c		0.05		0.05	TBD	TBD	pF	1,3,4
C_{I}	Input capacitance(CTRL, ADD, CMD pins only)	0.2	0.8	0.2	0.7	TBD	TBD	pF	1,3,6
C_{DI_CTRL}	Input capacitance delta(All CTRL pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,3,7,8
$C_{DI_ADD_CMD}$	Input capacitance delta(All ADD/ CMD pins only)	-0.1	0.1	-0.1	0.1	TBD	TBD	pF	1,2,9,10
C_{ALERT}	Input/output capacitance of ALERT	0.5	1.5	0.5	1.5	TBD	TBD	pF	1,3
C_{ZQ}	Input/output capacitance of ZQ	0.5	1.5	0.5	1.5	TBD	TBD	pF	1,3,12

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The silicon only capacitance is validated by de-embedding the package L & C parasitic. The capacitance is measured with VDD, VDDQ, VSS, VSSQ applied with all other signal pins floating. Measurement procedure tbd.

NOTE 2 DQ, DM_n, DQS_T, DQS_C, TDQS_T, TDQS_C. Although the DM, TDQS_T and TDQS_C pins have different functions, the loading matches DQ and DQS

NOTE 3 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 4 Absolute value CK_T-CK_C

NOTE 5 Absolute value of CIO(DQS_T)-CIO(DQS_C)

NOTE 6 CI applies to ODT, CS_n, CKE, A0-A17, BA0-BA1, BG0-BG1, RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

NOTE 7 CDI CTRL applies to ODT, CS_n and CKE

NOTE 8 CDI_CTRL = CI(CTRL)-0.5*(CI(CLK_T)+CI(CLK_C))

NOTE 9 CDI_ADD_ CMD applies to, A0-A17, BA0-BA1, BG0-BG1,RAS_n/A16, CAS_n/A15, WE_n/A14, ACT_n and PAR.

NOTE 10 CDI_ADD_CMD = CI(ADD_CMD)-0.5*(CI(CLK_T)+CI(CLK_C))

NOTE 11 CDIO = CIO(DQ,DM)-0.5*(CIO(DQS_T)+CIO(DQS_C))

NOTE 12 Maximum external load capacitance on ZQ pin: tbd pF.

Table 99 — DRAM package electrical specifications

Symbol	Parameter	DDR4-1600,1866,2133		DDR4-2400,2666		DDR4-3200		Unit	NOTE
		min	max	min	max	min	max		
Z_{IO}	Input/output Zpkg	50	85	50	85	TBD	TBD	Ω	1,2,4,5
T_{dIO}	Input/output Pkg Delay	14	37	14	37	TBD	TBD	ps	1,3,4,5
$DZ_{DIO\ DQS}$	Delta Zpkg DQS_t and DQS_c	-	10	-	10	TBD	TBD	Ω	1,2,5,7
$D_{TdDIO\ DQS}$	Delta Delay DQS_t and DQS_c	-	5	-	5	TBD	TBD	pF	1,3,5,7
$Z_{I\ CTRL}$	Input- CTRL pins Zpkg	TBD	TBD	TBD	TBD	TBD	TBD	Ω	1,2,5,9
$T_{dI_\ CTRL}$	Input- CTRL pins Pkg Delay	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,9
$Z_{IADD\ CMD}$	Input- CMD ADD pins Zpkg	TBD	TBD	TBD	TBD	TBD	TBD	Ω	1,2,5,8
$Td_{IADD_\ CMD}$	Input- CMD ADD pins Pkg Delay	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5,8
Z_{CK}	CK_t and CK_c Zpkg	TBD	TBD	TBD	TBD	TBD	TBD	Ω	1,2,5
Td_{CK}	CK_t and CK_c Pkg Delay	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5
DZ_{DCK}	Delta Zpkg CK_t and CK_c	-	TBD	-	TBD	TBD	TBD	Ω	1,2,5,6
D_{TdCK}	Delta Delay CK_t and CK_c	-	TBD	-	TBD	TBD	TBD	ps	1,3,5,6
Z_{OZQ}	ZQ Zpkg	TBD	TBD	TBD	TBD	TBD	TBD	Ω	1,2,5
$Td_{O\ ZQ}$	ZQ Delay	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5
$Z_{O\ ALERT}$	ALERT Zpkg	TBD	TBD	TBD	TBD	TBD	TBD	Ω	1,2,5
$Td_{O\ ALERT}$	ALERT Delay	TBD	TBD	TBD	TBD	TBD	TBD	ps	1,3,5

NOTE :

NOTE 1 This parameter is not subject to production test. It is verified by design and characterization. The package parasitic(L & C) are validated using package only samples. The capacitance is measured with VDD, VDDQ, VSS, VSSQ shorted with all other signal pins floating. The inductance is measured with VDD, VDDQ, VSS and VSSQ shorted and all other signal pins shorted at the die side(not pin). Measurement procedure tbd

NOTE 2 Package only impedance (Zpkg) is calculated based on the Lpkg and Cpkg total for a given pin where:

$$Zpkg(\text{total per pin}) = \sqrt{Lpkg/Cpkg}$$

NOTE 3 Package only delay(Tpkg) is calculated based on Lpkg and Cpkg total for a given pin where:

$$Tdpkg(\text{total per pin}) = \sqrt{Lpkg * Cpkg}$$

NOTE 4 Z & Td IO applies to DQ, DM, DQS_C, DQS_T, TDQS_T and TDQS_C

NOTE 5 This parameter applies to monolithic devices only; stacked/dual-die devices are not covered here

NOTE 6 Absolute value of ZCK_t-ZCK_c for impedance(Z) or absolute value of TdCK_t-TdCK_c for delay(Td).

NOTE 7 Absolute value of ZIO(DQS_t)-ZIO(DQS_c) for impedance(Z) or absolute value of TdIO(DQS_t)-TdIO(DQS_c) for delay(Td)

NOTE 8 ZI & Td ADD CMD applies to A0-A17, BA0-BA1, BG0-BG1, RAS_n CAS_n, WE_n.

NOTE 9 ZI & Td CTRL applies to ODT, CS_n and CKE

12 Electrical Characteristics & AC Timing

12.1 Reference Load for AC Timing and Output Slew Rate

Figure 186 represents the effective reference load of 50 ohms used in defining the relevant AC timing parameters of the device as well as output slew rate measurements.

It is not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

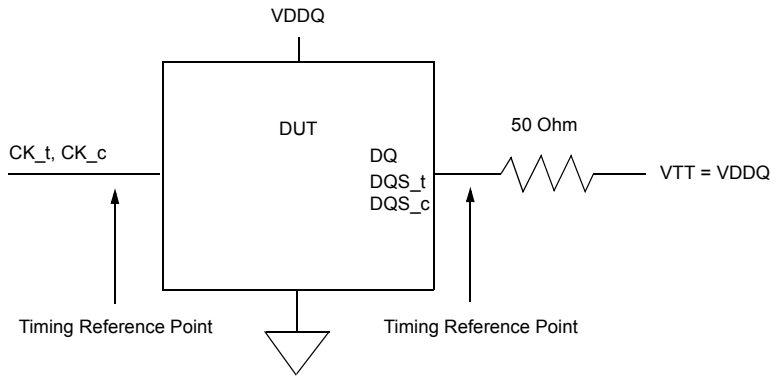


Figure 186 — Reference Load for AC Timing and Output Slew Rate

12.2 tREFI

Average periodic Refresh interval (tREFI) of DDR4 SDRAM is defined as shown in the table.

Table 100 — tREFI by device density

Parameter	Symbol		2Gb	4Gb	8Gb	16Gb	Units
Average periodic refresh interval	tREFI	0°C ≤ TCASE ≤ 85°C	7.8	7.8	7.8	TBD	µs
		85°C < TCASE ≤ 95°C	3.9	3.9	3.9	TBD	µs

12.3 Timing Parameters by Speed Grade

Table 101 — Timing Parameters by Speed Bin for DDR4-1600 to DDR4-2133

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns	22
Average Clock Period	tCK(avg)	tbd –(Definition tbd)						ps	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	UI	23
Clock Period Jitter- deterministic	JIT(per)_dj	TBD	TBD	TBD	TBD	TBD	TBD	UI	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cycle to Cycle Period Jitter	tJIT(cc)_total	0.2		0.2		0.2		UI	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	TBD		TBD		TBD		UI	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	TBD		TBD		TBD		UI	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 2 cycles	tERR(2per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 3 cycles	tERR(3per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 4 cycles	tERR(4per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 5 cycles	tERR(5per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 6 cycles	tERR(6per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 7 cycles	tERR(7per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 8 cycles	tERR(8per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 9 cycles	tERR(9per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 10 cycles	tERR(10per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 11 cycles	tERR(11per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 12 cycles	tERR(12per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	TBD		TBD		TBD		UI	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	5	-	5	-	6	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	4	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Command and Address Timing									
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,5ns)	-	Max(4nCK,4.2ns)	-	Max(4nCK,3.7ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,7.5ns)	-	Max(4nCK,6.4ns)	-	Max(4nCK,6.4ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,6ns)	-	Max(4nCK,5.3ns)	-	Max(4nCK,5.3ns)	-	nCK	
Four activate window for 2KB page size	tFAW_2K	35	-	30	-	30	-	ns	
Four activate window for 1KB page size	tFAW_1K	25	-	23	-	21	-	ns	
Four activate window for 1/2KB page size	tFAW_1/2K	20	-	17	-	15	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-	max(2nCK,2.5ns)	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-		
WRITE recovery time	tWR	15	-	15	-	15	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (4nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	tWR+max (5nCK,3.75ns)	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (4nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	tWTR_S+max (5nCK,3.75ns)	-	ns	2, 29
delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (4nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	tWTR_L+max (5nCK,3.75ns)	-	ns	3,30
DLL locking time	tDLLK	TBD	-	TBD	-	TBD	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	8	-	8	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	max(24nCK,15ns)	-	max(24nCK,15ns)	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min)	-	tMOD (min)	-	tMOD (min)	-	-	
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	3	-	4	-	4	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg)/2	13,18
DQS_t,DQS_c to DQ Skew deterministic, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg)/2	14,16,18
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	tCK(avg)/2	13,17,18
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	TBD	-	TBD	-	UI	14,16.18
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-	TBD	-	TBD	UI	13,19
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	UI	13,19
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	UI	15,16

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Data Strobe Timing									
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	21
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	20
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	tMOD(min) + tCP-DED(min)	-	tMOD(min) + tCPDED(min)	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		tCKSRX(min)		tCKSRX(min)			
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD		TBD		TBD			
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)		tXMP(min) + tXSDLL(min)			
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	1024	-	1024	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	512	-	512	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	128	-	128	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+ 10ns)	-	max (5nCK,tRFC(min) + 10ns)	-	max (5nCK,tRFC(min) + 10ns)	-		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	tRFC(min)+10ns	-	tRFC(min)+10ns	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-	tCKE(min)+1nCK	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-	max (5nCK,10ns)+PL	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-		
Power Down Timing									
Exit Power Down with DLL on to any valid com-mand;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	max (4nCK,6ns)	-	max (4nCK,6ns)	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-	max (3nCK, 5ns)	-		31,32
Command pass disable delay	tCPDED	4	-	4	-	4	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI		6

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Power Down Timing									
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	2	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	2	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	WL+4+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK	5
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	WL+2+(tWR/ tCK(avg))	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	2	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		max(16nCK,10ns)		max(16nCK,10ns)			
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		tMOD		tMOD			
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	1.0	9.0	1.0	9.0	ns	
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	nCK	12
DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write Leveling Timing									
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	0.13	-	0.13	-	tCK(avg)	
Write leveling output delay	tWLO	0	9.5	0	9.5	0	9.5	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)	-	Max(2nCK,3ns)	-	Max(2nCK,3ns)		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	PL+6ns	-	PL+6ns		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	48	96	56	112	64	128	nCK	

Speed		DDR4-1600		DDR4-1866		DDR4-2133		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
CA Parity Timing									
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	43	-	50	-	57	nCK	
Parity Latency	PL	4		4		4		nCK	
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	13	-	13	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	6	10	6	10	nCK	
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	
	4Gb	260	-	260	-	260	-	ns	
	8Gb	350	-	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	
	4Gb	160	-	160	-	160	-	ns	
	8Gb	260	-	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	
	4Gb	110	-	110	-	110	-	ns	
	8Gb	160	-	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	

Table 102 — Timing Parameters by Speed Bin for DDR4-2400 to DDR4-3200

Speed		DDR4-2400		DDR4-2666		DDR4-3200		Units	NOTE
Parameter	Symbol	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing									
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	-	8	-	8	-	ns	22
Average Clock Period	tCK(avg)	tbd –(Definition tbd)						ps	
Average high pulse width	tCH(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Average low pulse width	tCL(avg)	0.48	0.52	0.48	0.52	0.48	0.52	tCK(avg)	
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)min + tJIT(per)min_to t	tCK(avg)m ax + tJIT(per)m ax_tot	tCK(avg)	
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	23
Absolute clock LOW pulse width	tCL(abs)	0.45	-	0.45	-	0.45	-	tCK(avg)	24
Clock Period Jitter- total	JIT(per)_tot	- 0.1	0.1	- 0.1	0.1	- 0.1	0.1	UI	25
Clock Period Jitter- deterministic	JIT(per)_dj	TBD	TBD	TBD	TBD	TBD	TBD	UI	26
Clock Period Jitter during DLL locking period	tJIT(per, lck)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cycle to Cycle Period Jitter	tJIT(cc)_total	0.2		0.2		0.2		UI	25
Cycle to Cycle Period Jitter deterministic	tJIT(cc)_dj	TBD		TBD		TBD		UI	26
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	TBD		TBD		TBD		UI	
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	TBD	TBD	TBD	TBD	UI	

Cumulative error across 2 cycles	tERR(2per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 3 cycles	tERR(3per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 4 cycles	tERR(4per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 5 cycles	tERR(5per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 6 cycles	tERR(6per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 7 cycles	tERR(7per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 8 cycles	tERR(8per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 9 cycles	tERR(9per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 10 cycles	tERR(10per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 11 cycles	tERR(11per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across 12 cycles	tERR(12per)	TBD	TBD	TBD	TBD	TBD	TBD	UI	
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	TBD		TBD		TBD		UI	
Command and Address Timing									
CAS_n to CAS_n command delay for same bank group	tCCD_L	6	-	TBD	-	TBD	-	nCK	
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	4	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	TBD	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3.3ns)	-	TBD	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to different bank group for 1/2KB page size	tRRD_S(1/2K)	Max(4nCK,3.3ns)	-	TBD	-	TBD	-	nCK	
Speed		**DDR4-2400**		**DDR4-2666**		**DDR4-3200**		**Units**	**NOTE**
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Command and Address Timing									
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	TBD	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	TBD	-	TBD	-	nCK	
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/2K)	Max(4nCK,4.9ns)	-	TBD	-	TBD	-	nCK	
Four activate window for 2KB page size	tFAW_2K	30	-	TBD	-	TBD	-	ns	
Four activate window for 1KB page size	tFAW_1K	21	-	TBD	-	TBD	-	ns	
Four activate window for 1/2KB page size	tFAW_1/2K	13	-	TBD	-	TBD	-	ns	
Delay from start of internal write transaction to internal read command for different bank group	tWTR_S	max (2nCK, 2.5ns)	-	TBD	-	TBD	-		1,2,e
Delay from start of internal write transaction to internal read command for same bank group	tWTR_L	max (4nCK,7.5ns)	-	TBD	-	TBD	-		1
Internal READ Command to PRECHARGE Command delay	tRTP	max (4nCK,7.5ns)	-	TBD	-	TBD	-		
WRITE recovery time	tWR	15	-	TBD	-	TBD	-	ns	1
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	TBD	-	TBD	-	ns	1, 28
delay from start of internal write transaction to internal read command for different bank groups with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	TBD	-	TBD	-	ns	2, 29

delay from start of internal write transaction to internal read command for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	TBD	-	TBD	-	ns	3, 30
DLL locking time	tDLLK	TBD	-	TBD	-	TBD	-	nCK	
Mode Register Set command cycle time	tMRD	8	-	TBD	-	TBD	-	nCK	
Mode Register Set command update delay	tMOD	max(24nCK,15ns)	-	TBD	-	TBD	-		
Multi-Purpose Register Recovery Time	tMPRR	1	-	TBD	-	TBD	-	nCK	33
Multi Purpose Register Write Recovery Time	tWR_MPR	tMOD (min)	-	TBD	-	TBD	-		
CS_n to Command Address Latency									
CS_n to Command Address Latency	tCAL	5	-	TBD	-	TBD	-	nCK	
DRAM Data Timing									
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg)/2	13,18
DQS_t,DQS_c to DQ Skew deterministic, per group, per access	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg)/2	14,16,18
DQ output hold time from DQS_t,DQS_c	tQH	TBD	-	TBD	-	TBD	-	tCK(avg)/2	13,17,18
DQ output hold time deterministic from DQS_t, DQS_c	tQH	TBD	-	TBD	-	TBD	-	tCK(avg)/2	14,16,18
DQS_t,DQS_c to DQ Skew total, per group, per access; DBI enabled	tDQSQ	-	TBD	-	TBD	-	TBD	tCK(avg)/2	13,19
DQ output hold time total from DQS_t, DQS_c; DBI enabled	tQH	TBD	-	TBD	-	TBD	-	tCK(avg)/2	13,19
DQ to DQ offset , per group, per access referenced to DQS_t, DQS_c	tDQSQ	TBD	TBD	TBD	TBD	TBD	TBD	tCK(avg)/2	15,16
Data Strobe Timing									
DQS_t,DQS_c differential output high time	tQSH	TBD	TBD	TBD	TBD	TBD	TBD	UI	21
DQS_t,DQS_c differential output low time	tQSL	TBD	TBD	TBD	TBD	TBD	TBD	UI	21
Speed		**DDR4-2400**		**DDR4-2666**		**DDR4-3200**		**Units**	**NOTE**
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
MPSM Timing									
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	TBD	-	TBD	-		
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	TBD	-	TBD	-		
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)	-	TBD	-	TBD	-		
Exit MPSM to commands not requiring a locked DLL	tXMP	TBD	-	TBD	-	TBD	-		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)	-	TBD	-	TBD	-		
CS setup time to CKE	tMPX_S	TBD	-	TBD	-	TBD	-		
CS hold time to CKE	tMPX_H	TBD	-	TBD	-	TBD	-		
Calibration Timing									
Power-up and RESET calibration time	tZQinit	1024	-	TBD	-	TBD	-	nCK	
Normal operation Full calibration time	tZQoper	512	-	TBD	-	TBD	-	nCK	
Normal operation Short calibration time	tZQCS	128	-	TBD	-	TBD	-	nCK	
Reset/Self Refresh Timing									
Exit Reset from CKE HIGH to a valid command	tXPR	max (5nCK,tRFC(min)+10ns)	-	TBD	-	TBD	-		

Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	TBD	-	TBD	-		
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tXS_ABORT(min)	tRFC4(min)+10ns	-	TBD	-	TBD	-		
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-	tRFC4(min)+10ns	-		
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	TBD	-	TBD	-		
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	TBD	-	TBD	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max (5nCK,10ns)	-	TBD	-	TBD	-		
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down when CA Parity is enabled	tCKSRE_PAR	max (5nCK,10ns)+PL	-	TBD	-	TBD	-		
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max (5nCK,10ns)	-	TBD	-	TBD	-		
Power Down Timing									
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (4nCK,6ns)	-	TBD	-	TBD	-		
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	TBD	-	TBD	-		31,32
Command pass disable delay	tCPDED	4	-	TBD	-	TBD	-	nCK	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	TBD	-	TBD	-		6
Timing of ACT command to Power Down entry	tACTPDEN	2	-	TBD	-	TBD	-	nCK	7
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	TBD	-	TBD	-	nCK	7
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	TBD	-	TBD	-	nCK	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	TBD	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	TBD	-	TBD	-	nCK	5
Speed		**DDR4-2400**		**DDR4-2666**		**DDR4-3200**		**Units**	**NOTE**
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
Power Down Timing									
Timing of WR command to Power Down entry (BC4MRS)	tWRPBC4DEN	WL+2+(tWR/ tCK(avg))	-	TBD	-	TBD	-	nCK	4
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPBC4DEN	WL+2+WR+1	-	TBD	-	TBD	-	nCK	5
Timing of REF command to Power Down entry	tREFPDEN	2	-	TBD	-	TBD	-	nCK	7
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	TBD	-	TBD	-		
PDA Timing									
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		TBD	-	TBD	-		
Mode Register Set command update delay in PDA mode	tMOD_PDA	tMOD		TBD	-	TBD	-		
ODT Timing									
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	TBD	TBD	TBD	TBD	ns	
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	TBD	TBD	TBD	TBD	ns	
RTT dynamic change skew	tADC	0.3	0.7	TBD	TBD	TBD	TBD	tCK(avg)	
Write Leveling Timing									
First DQS_t/DQS_n rising edge after write leveling mode is programmed	tWLMRD	40	-	TBD	TBD	TBD	TBD	nCK	12

DQS_t/DQS_n delay after write leveling mode is programmed	tWLDQSEN	25	-	TBD	TBD	TBD	TBD	nCK	12
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	TBD	TBD	TBD	TBD	ps	
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	TBD	TBD	TBD	TBD	ps	
Write leveling output delay	tWLO	0	9.5	TBD	TBD	TBD	TBD	ns	
Write leveling output error	tWLOE							ns	
CA Parity Timing									
Commands not guaranteed to be executed during this time	tPAR_UNKNOWN	-	Max(2nCK,3ns)	-	TBD	-	TBD		
Delay from errant command to ALERT_n assertion	tPAR_ALERT_ON	-	PL+6ns	-	TBD	-	TBD		
Pulse width of ALERT_n signal when asserted	tPAR_ALERT_PW	72	144	TBD	TBD	TBD	TBD	nCK	
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALERT_RSP	-	64					nCK	
Parity Latency	PL	5		TBD		TBD		nCK	
CRC Error Reporting									
CRC error to ALERT_n latency	tCRC_ALERT	-	13	-	TBD	-	TBD	ns	
CRC ALERT_n pulse width	CRC_ALERT_PW	6	10	TBD	TBD	TBD	TBD	nCK	
Geardown timing									
Exit RESET from CKE HIGH to a valid MRS geardown (T2/Reset)	tXPR_GEAR	-		tXPR		tXPR			
CKE High Assert to Gear Down Enable time(T2/CKE)	tXS_GEAR	-		tXS		tXS			
MRS command to Sync pulse time(T3)	tSYNC_GEAR	-	-	tMOD(min)+4nCK	-	tMOD(min)+4nCK	-		27
Sync pulse to First valid command(T4)	tCMD_GEAR	-		tMOD		tMOD			27
Geardown setup time	tGEAR_setup	-	-	2	-	2	-	nCK	
Geardown hold time	tGEAR_hold	-	-	2	-	2	-	nCK	
Speed		**DDR4-2400**		**DDR4-2666**		**DDR4-3200**		**Units**	**NOTE**
Parameter	**Symbol**	**MIN**	**MAX**	**MIN**	**MAX**	**MIN**	**MAX**		
tREFI									
tRFC1 (min)	2Gb	160	-	160	-	160	-	ns	
	4Gb	260	-	260	-	260	-	ns	
	8Gb	350	-	350	-	350	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC2 (min)	2Gb	110	-	110	-	110	-	ns	
	4Gb	160	-	160	-	160	-	ns	
	8Gb	260	-	260	-	260	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	
tRFC4 (min)	2Gb	90	-	90	-	90	-	ns	
	4Gb	110	-	110	-	110	-	ns	
	8Gb	160	-	160	-	160	-	ns	
	16Gb	TBD	-	TBD	-	TBD	-	ns	

NOTE :

1. Start of internal write transaction is defined as follows :
   For BL8 (Fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL.
   For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL.
2. A separate timing parameter will cover the delay from write to read when CRC and DM are simultaneously enabled
3. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
4. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR/tCK to the next integer.
5. WR in clock cycles as programmed in MR0.
6. tREFI depends on TOPER.
7. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
8. For these parameters, the DDR4 SDRAM device supports tnPARAM[nCK]=RU{tPARAM[ns]/tCK(avg)[ns]}, which is in clock cycles assuming all input clock jitter specifications are satisfied
9. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
10. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
11. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
12. The max values are system dependent.
13. DQ to DQS total timing per group where the total includes the sum of deterministic and random timing terms for a specified BER. BER spec and measurement method are tbd.
14. The deterministic component of the total timing. Measurement method tbd.
15. DQ to DQ static offset relative to strobe per group. Measurement method tbd.
16. This parameter will be characterized and guaranteed by design.
17 When the device is operated with the input clock jitter, this parameter needs to be derated by the actual tjit(per)_total of the input clock. (output deratings are relative to the SDRAM input clock). Example tbd.
18. DRAM DBI mode is off.
19. DRAM DBI mode is enabled. Applicable to x8 and x16 DRAM only.
20. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
21. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as measured from on falling edge to the next consecutive rising edge
22. There is no maximum cycle time limit besides the need to satisfy the refresh interval tREFI
23. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge
24. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge
25. Total jitter includes the sum of deterministic and random jitter terms for a specified BER. BER target and measurement method are tbd.
26. The deterministic jitter component out of the total jitter. This parameter is characterized and gauranteed by design.
27. This parameter has to be even number of clocks
28. When CRC and DM are both enabled, tWR_CRC_DM is used in place of tWR.
29. When CRC and DM are both enabled tWTR_S_CRC_DM is used in place of tWTR_S.
30. When CRC and DM are both enabled tWTR_L_CRC_DM is used in place of tWTR_L.
31. After CKE is registered LOW, CKE signal level shall be maintained below VILDC for tCKE specification (Low pulse width).
32. After CKE is registered HIGH, CKE signal level shall be maintained above VIHDC for tCKE specification (HIGH pulse width).
33. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.

UI=tCK(avg).min/2

12.4 The DQ input receiver compliance mask for voltage and timing (see figure)

The DQ input receiver compliance mask for voltage and timing is shown in the figure below. The receiver mask (Rx Mask) defines area the input signal must not encroach in order for the DRAM input receiver to be expected to be able to successfully capture a valid input signal; it is not the valid data-eye.

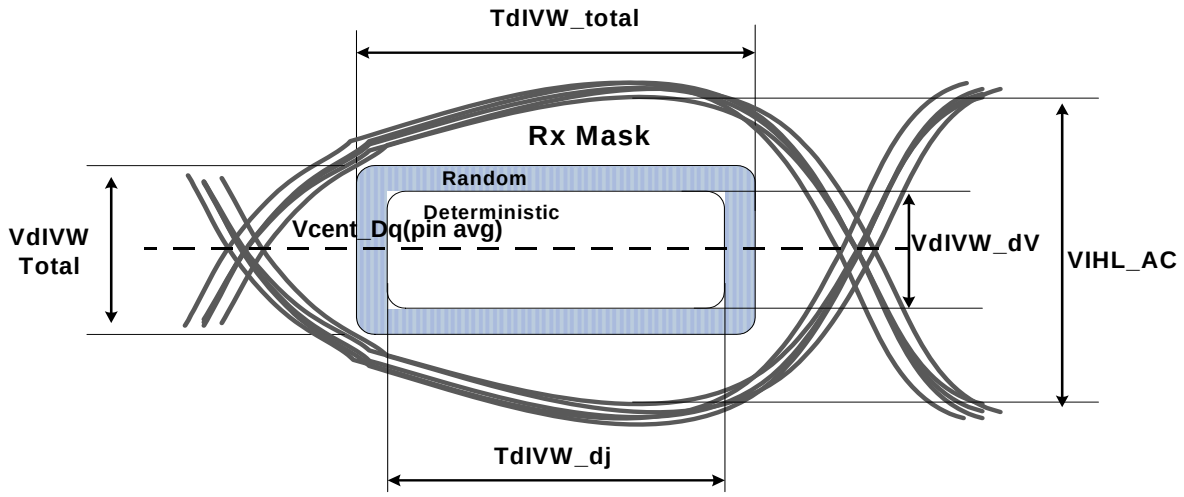


Figure 187 — DQ Receiver(Rx) compliance mask

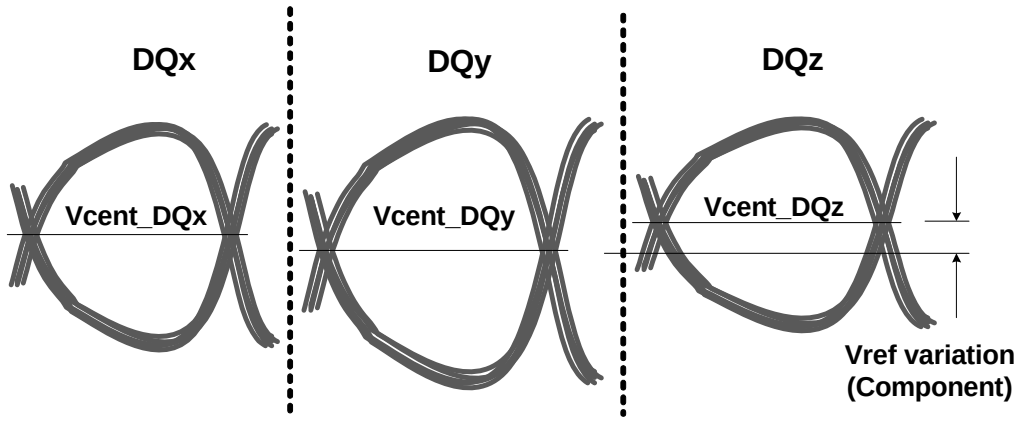
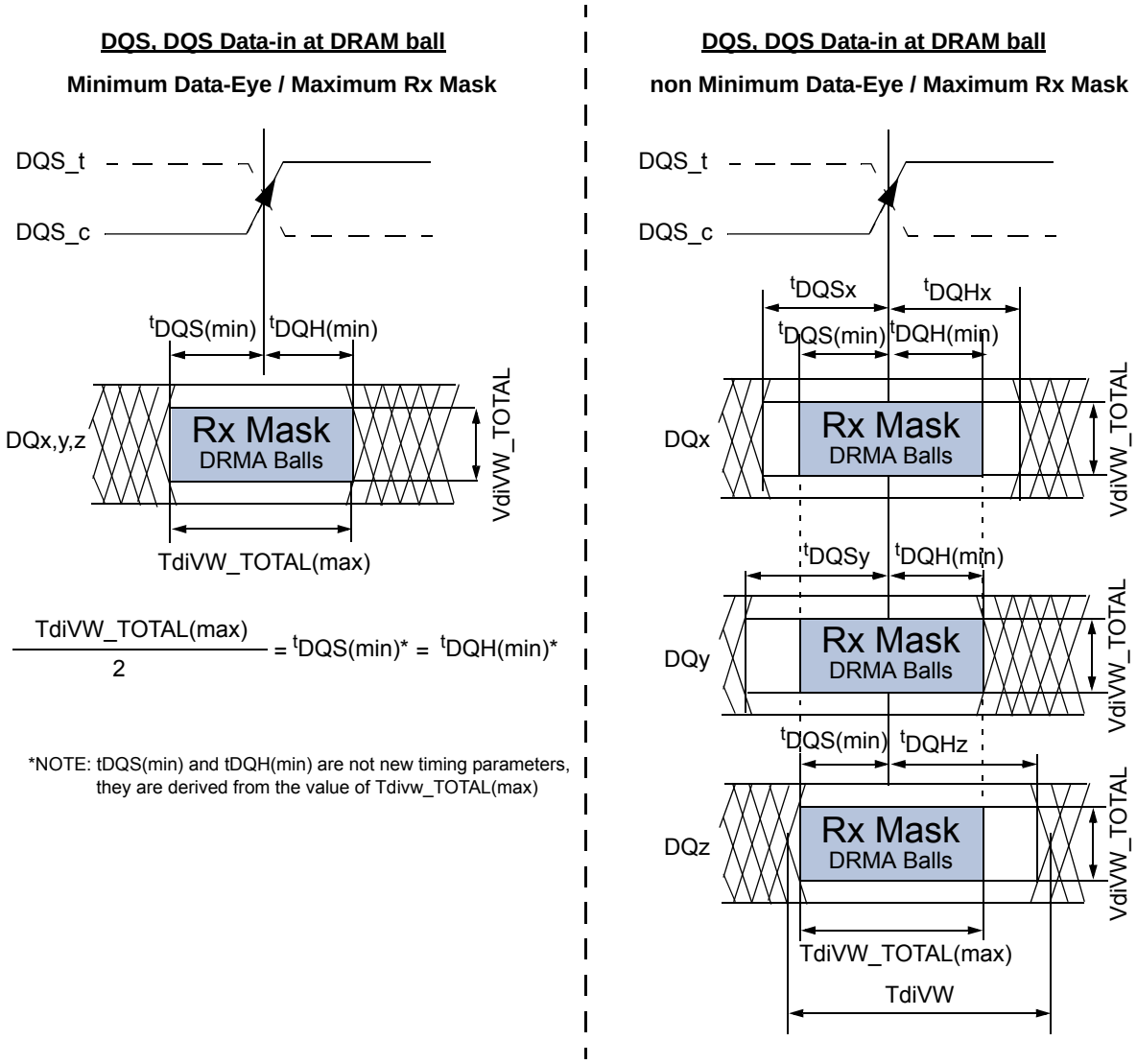


Figure 188 — Across pin Vref DQ voltage variation

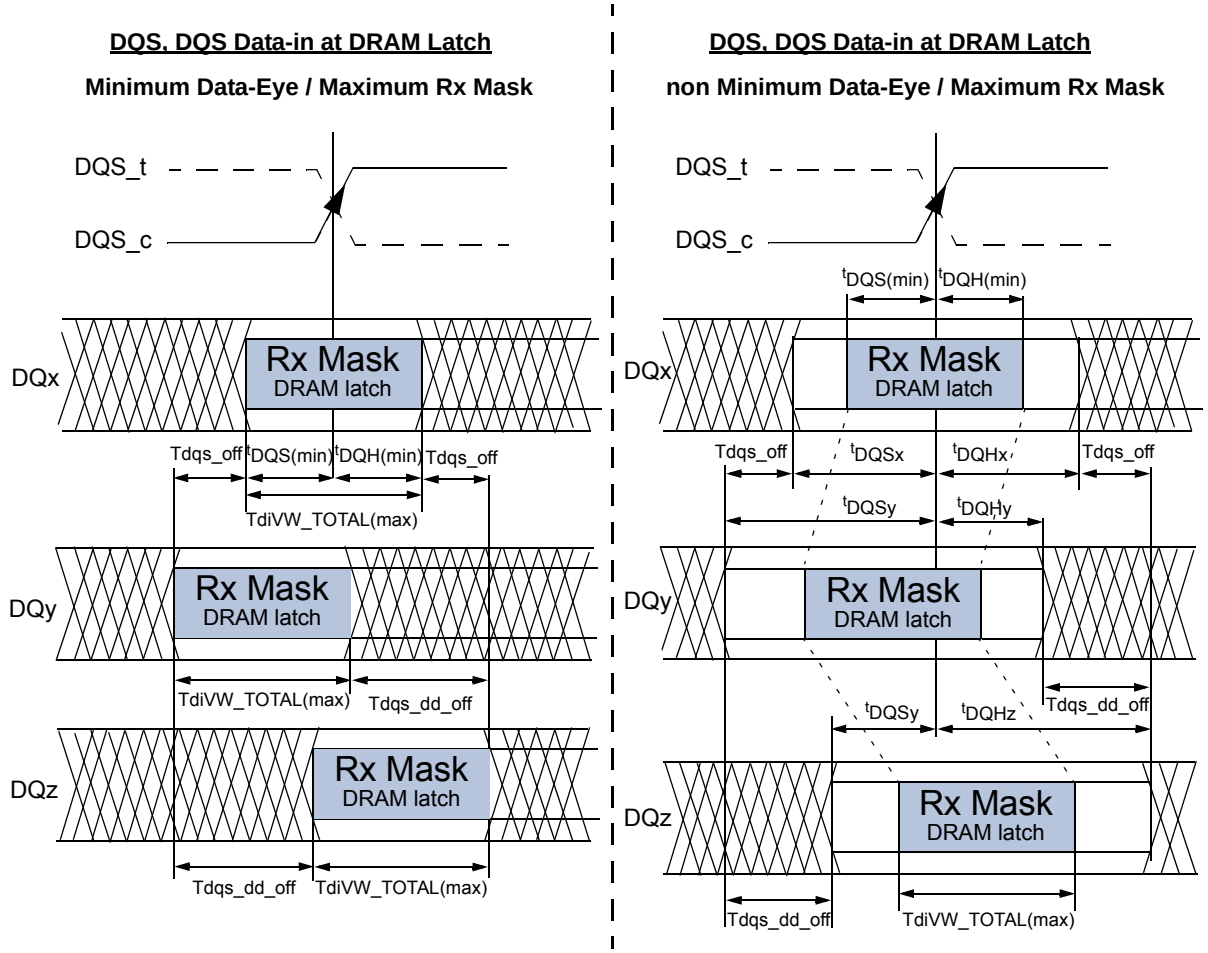
Vcent_DQ(pin avg) is defined as the midpoint between the largest Vref_DQ voltage level and the smallest Vref_DQ voltage level across all DQ pins for a given DRAM component. Each DQ pin Vref level is defined by the center, i.e. widest opening, of the cumulative data input eye as depicted in figure 2.This clarifies that any DRAM component level variation must be accounted for within the DRAM Rx mask.The component level Vref will be set by the system to account for Ron and ODT settings.



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transiining input
DQz represents latest valid transitioning input

Figure 189 — DQ to DQS Timings at DRAM Balls

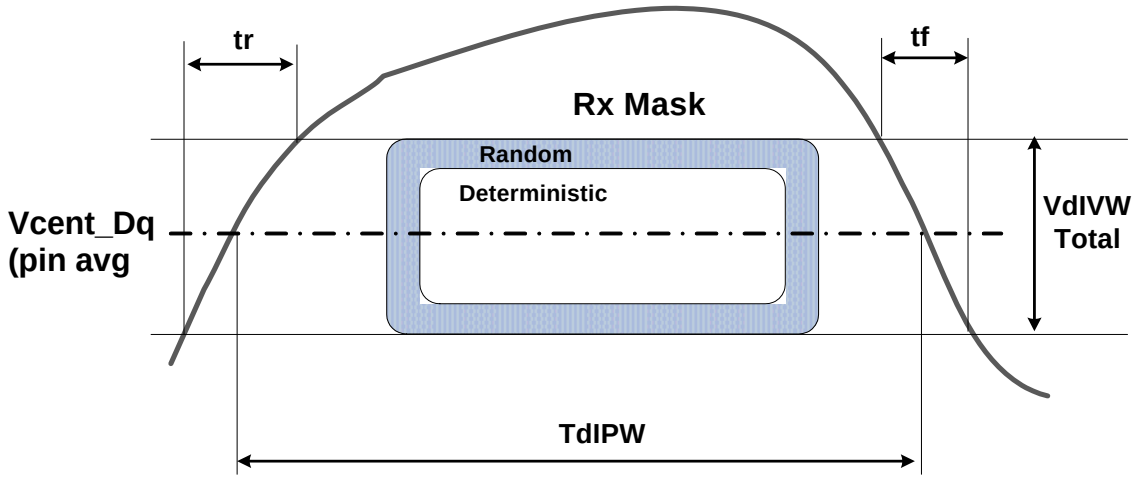
All of the timing terms in Figure 189 are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS_t/DQS_c center aligned to the DQ per pin.



NOTE: DQx represents an optimally centered input
DQy represents earliest valid transiining input
DQz represents latest valid transitioning input

Figure 190 — DQ to DQS Timings at DRAM latch

All of the timing terms in Figure 190 are measured at the VdIVW_total voltage levels centered around Vcent_DQ(pin avg) and are referenced to the DQS_t/DQS_c center aligned. Typical view assumes DQx, DQy, and DQz edges are aligned at DRAM balls.



NOTE 1 SRIN_dIVW=VdIVW_Total/(tr or tf), signal must be monotonic within tr and tf range.

Figure 191 — DQ TdIPW and SRIN_dIVW definition (for each input pulse)

Table 103 — DRAM DQs In Receive Mode; * UI=tck(avg)min/2

Symbol	Parameter	1600,1866,2133		2400		2666,3200		Unit	NOTE
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	136 (note12)	-	tbd	-	tbd	mV	1,2,4,6
VdIVW_dV	Rx Mask voltage - deterministic	-	136	-	tbd	-	tbd	mV	1,5,13
TdIVW_total	Rx timing window total	-	0.2 (note12)	-	tbd	-	tbd	UI*	1,2,4,6
TdIVW_dj	Rx deterministic timing	-	0.2	-	tbd	-	tbd	UI*	1,5, 13
VIHL_AC	DQ AC input swing pk-pk	186	-	tbd	-	tbd	-	mV	7
TdIPW	DQ input pulse width	0.58		tbd		tbd		UI*	8
Tdqs_off	DQ to DQS Setup offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqh_off	DQ to DQS Hold offset	-	tbd	-	tbd	-	tbd	UI*	9
Tdqs_dd_off	DQ to DQ Setup offset	-	tbd	-	tbd	-	tbd	UI*	10
Tdqh_dd_off	DQ to DQ Hold offset	-	tbd	-	tbd	-	tbd	UI*	10
SRIN_dIVW	Input Slew Rate over VdIVW_total	tbd	9	tbd	tbd	tbd	tbd	V/ns	11

NOTE :

1. Data Rx mask voltage and timing total input valid window where VdIVW is centered around Vcent_DQ(pin avg). The data Rx mask is applied per bit and should include voltage and temperature drift terms. The design specification is BER <1e-16 and how this varies for lower BER is tbd. The BER will be characterized and extrapolated if necessary using a dual dirac method from a higher BER(tbd).
2. Rx mask voltage AC swing peak-peak requirement over TdIVW_total with at least half of TdIVW_total(max) above Vcent_DQ(pin avg) and at least half of TdIVW_total(max) below Vcent_DQ(pin avg).
3. Rx differential DQ to DQS jitter total timing window at the VdIVW voltage levels centered around Vcent_DQ(pin avg).
4. Defined over the DQ internal Vref range 1.
5. Deterministic component of the total Rx mask voltage or timing. Parameter will be characterized and guaranteed by design. Measurement method tbd
6. Overshoot and Undershoot Specifications tbd.
7. DQ input pulse signal swing into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin avg)
8. DQ minimum input pulse width defined at the Vcent_DQ(pin avg).
9. DQ to DQS setup or hold offset defined within byte from DRAM ball to DRAM internal latch; ^{t}DQS and ^{t}DQH are the minimum DQ setup and hold per DQ pin; each is equal to one-half of TdIVW_total(max).
10. DQ to DQ setup or hold delta offset within byte. Defined as the static difference in Tdqs_off(max) and Tdqs_off(min) or Tdqh(max) – Tdqh(min) for a given component, from DRAM ball to DRAM internal latch.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin avg). Slowest DQ slew rate to fastest DQ slew rate per transition edge must be within tbd V/ns of each other.
12. The total timing and voltage terms(tdIVW_total & VdIVWtotal) are valid for any BER lower {lower fail rate} than the spec.
13. VdIVW_total - VdIVW_dV and TdIVW_total - TdIVW_dj define the difference between random and deterministic fail mask. When VdIVW_total - VdIVW_dV = 0 and TdIVW_total - TdIVW_dj = 0, random error is assumed to be zero.

12.5 DDR4 Function Matrix

DDR4 SDRAM has several features supported by ORG and also by Speed. The following Table is the summary of the features.

Table 104 — Function Matrix (By ORG. V:Supported, Blank:Not supported)

Functions	x4	x8	x16	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask		V	V	
Data Bus Inversion		V	V	
TDQS		V		
ZQ calibration —	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V		
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC	V	V	V	
CA Parity	V	V	V	
Control Gear Down Mode	V	V	V	
Programmable Preamble	V	V	V	
Maximum Power Down Mode	V	V		
Boundary Scan Mode			V	
Additive Latency	V	V		
3DS	V	V		

Table 105 — Function Matrix (By Speed. V:Supported, Blank:Not supported)

Functions	1600/1866/2133 Mbps	2400Mbps	2666/3200Mbps	NOTE
Write Leveling	V	V	V	
Temperature controlled Refresh	V	V	V	
Low Power Auto Self Refresh	V	V	V	
Fine Granularity Refresh	V	V	V	
Multi Purpose Register	V	V	V	
Data Mask	V	V	V	
Data Bus Inversion	V	V	V	
TDQS	V	V	V	
ZQ calibration	V	V	V	
DQ Vref Training	V	V	V	
Per DRAM Addressability	V	V	V	
Mode Register Readout	V	V	V	
CAL	V	V	V	
WRITE CRC			V	
CA Parity	V	V	V	
Control Gear Down Mode			V	
Programmable Preamble (2tCK)			V	
Maximum Power Down Mode	V	V	V	
Boundary Scan Mode	V	V	V	
3DS	V	V	V	

Standard Improvement Form **JEDEC** _____

The purpose of this form is to provide the Technical Committees of JEDEC with input from the industry regarding usage of the subject standard. Individuals or companies are invited to submit comments to JEDEC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

JEDEC
Attn: Publications Department
3103 North 10th Street
Suite 240 South
Arlington, VA 22201-2107

Fax: 703.907.7583

1. I recommend changes to the following:

☐ Requirement, clause number _____

☐ Test method number _____ Clause number _____

The referenced clause number has proven to be:

☐ Unclear ☐ Too Rigid ☐ In Error

☐ Other _____

2. Recommendations for correction:

_____

_____

_____

_____

3. Other suggestions for document improvement:

_____

_____

_____

_____

Submitted by

Name: _____ Phone: _____

Company: _____ E-mail: _____

Address: _____

City/State/Zip: _____ Date: _____

Rev. 9/02