

Petitioner Samsung Electronics Co., Ltd.'s Oral Argument for PTAB Hearing

***Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00847 (U.S. Patent No. 10,268,608)**

September 5, 2024

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OVERVIEW

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OVERVIEW OF '608 PATENT, INSTITUTED GROUNDS, AND PRIOR ART

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



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'608 PATENT

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



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'608 Patent

(12) **United States Patent**
Lee et al.

(10) **Patent No.:** US 10,268,608 B2
(45) **Date of Patent:** *Apr. 23, 2019

(54) **MEMORY MODULE WITH
TIMING-CONTROLLED DATA PATHS IN
DISTRIBUTED DATA BUFFERS**

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(72) Inventors: **Hyun Lee**, Ladera Ranch, CA (US);
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(73) Assignee: **NETLIST, INC.**, Irvine, CA (US)

Related U.S. Application Data

(63) Continuation of application No. 15/426,064, filed on Feb. 7, 2017, now Pat. No. **9,824,035**, which is a continuation of application No. 14/846,993, filed on Sep. 7, 2015, now Pat. No. 9,563,587, which is a continuation of application No. 13/952,599, filed on Jul. 27, 2013, now Pat. No. 9,128,632.

(60) Provisional application No. 61/676,883, filed on Jul. 27, 2012.

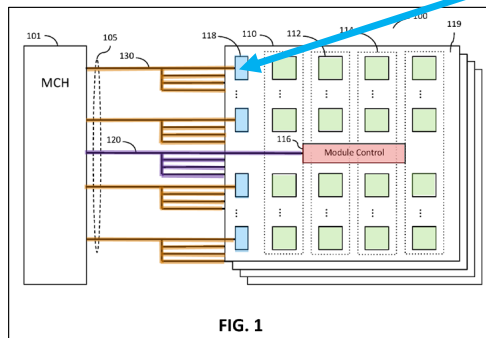


FIG. 1

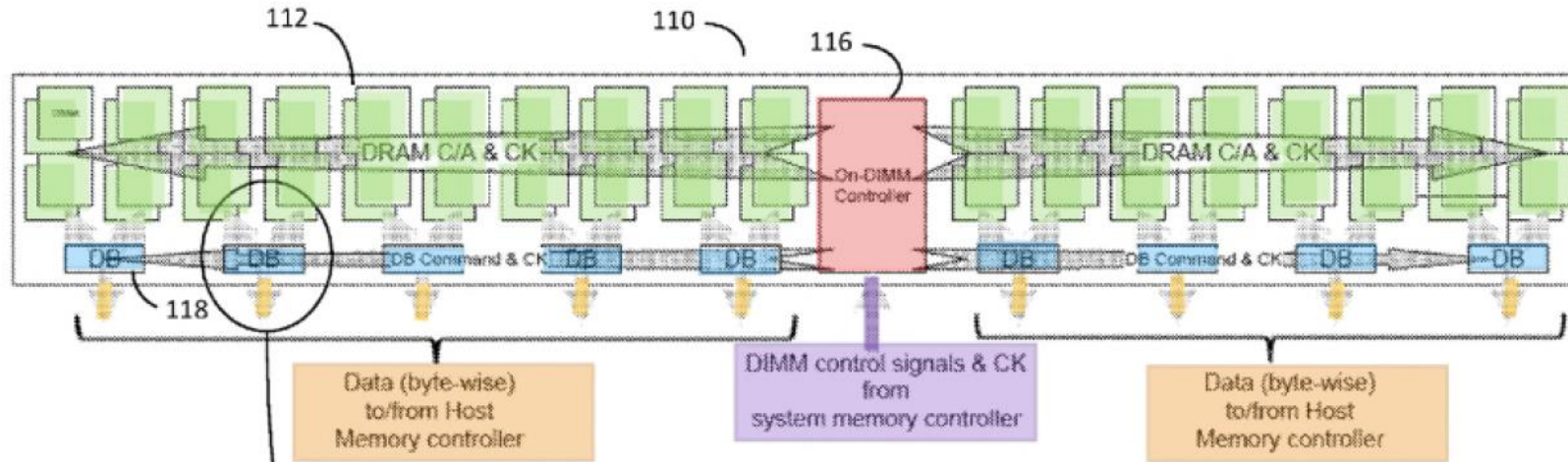
1. A memory module operable to communicate with **a memory controller** via a memory bus, the memory bus including signal lines, the signal lines including **a set of control/address signal lines** and **a plurality of sets of data/strobe signal lines**, the memory module comprising:
a module board having edge connections for coupling to respective signal lines in the memory bus;

a **module control device** mounted on the module board and configured to receive system command signals for memory operations via **the set of control/address signal lines** and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

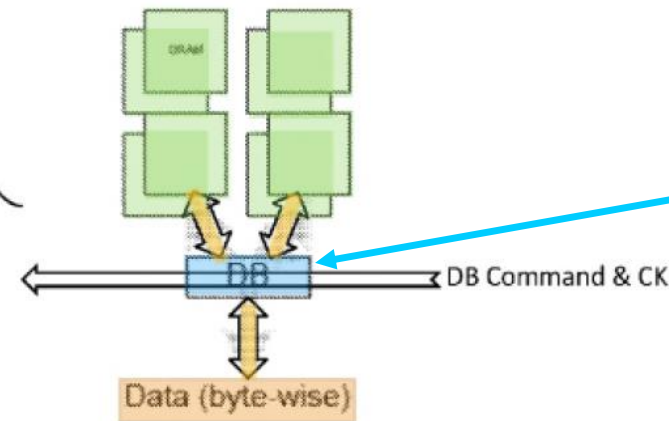
memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, **the memory devices** including a plurality of sets of memory devices corresponding to **respective sets of the plurality of sets of data/strobe signal lines**; and

a plurality of buffer circuits corresponding to **respective sets of the plurality of sets of data/strobe signal lines**, wherein **each respective buffer circuit of the plurality of buffer circuits** is mounted on the module board, coupled between **a respective set of data/strobe signal lines** and **a respective set of memory devices**, and configured to receive the module control signals and the module clock signal, **the each respective buffer circuit** including a **data path** corresponding to **each data signal line in the respective set of data/strobe signal lines**, and a command processing circuit configured to decode the module control signals and to control **the data path** in accordance with the module control signals and the module clock signal, wherein **the data path** corresponding to **the each data signal line** includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

'608 Patent: Disclosed Invention



EX1001 ('608 Patent), Fig. 2C



DESCRIPTION OF EMBODIMENTS

A memory module according to one embodiment includes memory devices organized in groups, a module control device, and data buffers (DB). The data buffers are sometimes referred to herein as buffer circuits, isolation devices (I.D.) or load reduction devices. The memory module is

EX1001 ('608 Patent), 3:22-:29

'608 Patent: Exemplary Claims

1[pre]	A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
1[a]	a module board having edge connections for coupling to respective signal lines in the memory bus;
1[b]	a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and
1[c]	memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and
1[d]	a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,
1[e]	wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,
1[f]	wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.
2	The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation, wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation, wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals, wherein the at least one of the module control signals include at least one of the first set of module control signals, and wherein the signal through the data path is a signal associated with the second memory operation.
9	The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal, wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.
10	The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

INSTITUTED GROUNDS

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Instituted Grounds

Hiraishi is equivalent to Osanai, which invalidated claims 1, 10-13, and 21-22 of the related '035 patent in IPR2022-00236 (June 20, 2023) [EX1066, EX1088] in combination with Tokuhiro

Grounds	Claims	Prior art (§103(a) combination)
1	Claims 1-5	<u>Hiraishi</u> + <u>Butt</u>
2	Claims 1-5	Ground 1 + <u>Tokuhiro</u>
3	Claim 5	(Ground 1 or 2) + <u>Ellsberry</u>
4	~~6-8~~	~~(Ground 1 or 2) + <u>Kim</u>~~
5	~~8~~	~~(Ground 1 or 2) + <u>Kim</u> and <u>Ellsberry</u>~~

Claims 6-12 were disclaimed after the Petition was filed on April 27, 2023. See EX2001.

OVERVIEW OF THE PRIOR ART

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



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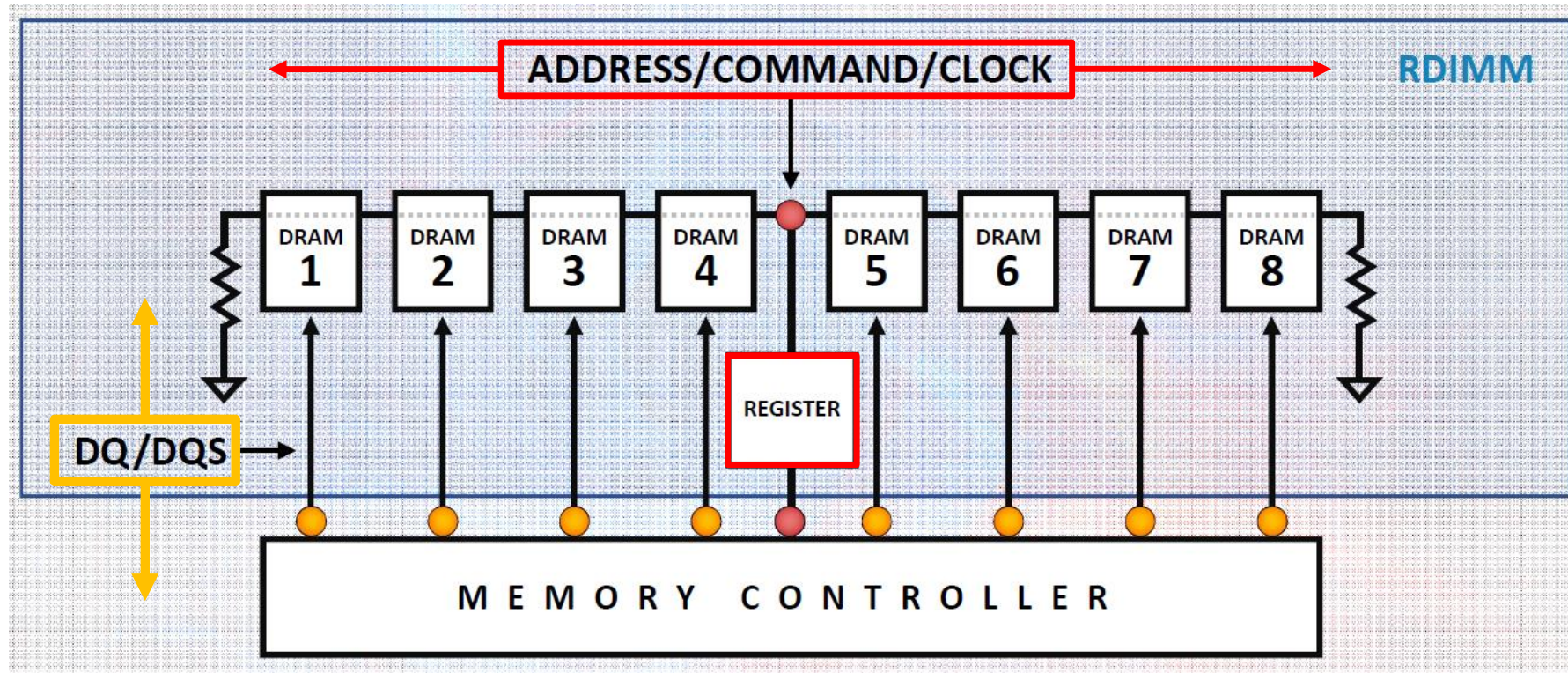
Undisputed: Level of Skill in the Art

B. Person of Ordinary Skill in the Art (“POSITA”)

A POSITA in the field of the '608 Patent in July 2012 would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field. EX1003, ¶37. She would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers. *Id.* She would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers. *Id.*

Paper 1 (Pet.) at 2-3; Paper 13 (ID) at 14-15;
Paper 20 (POR) at 12 ("Patent Owner is applying the level of ordinary skill in the art proposed by Petitioner.")

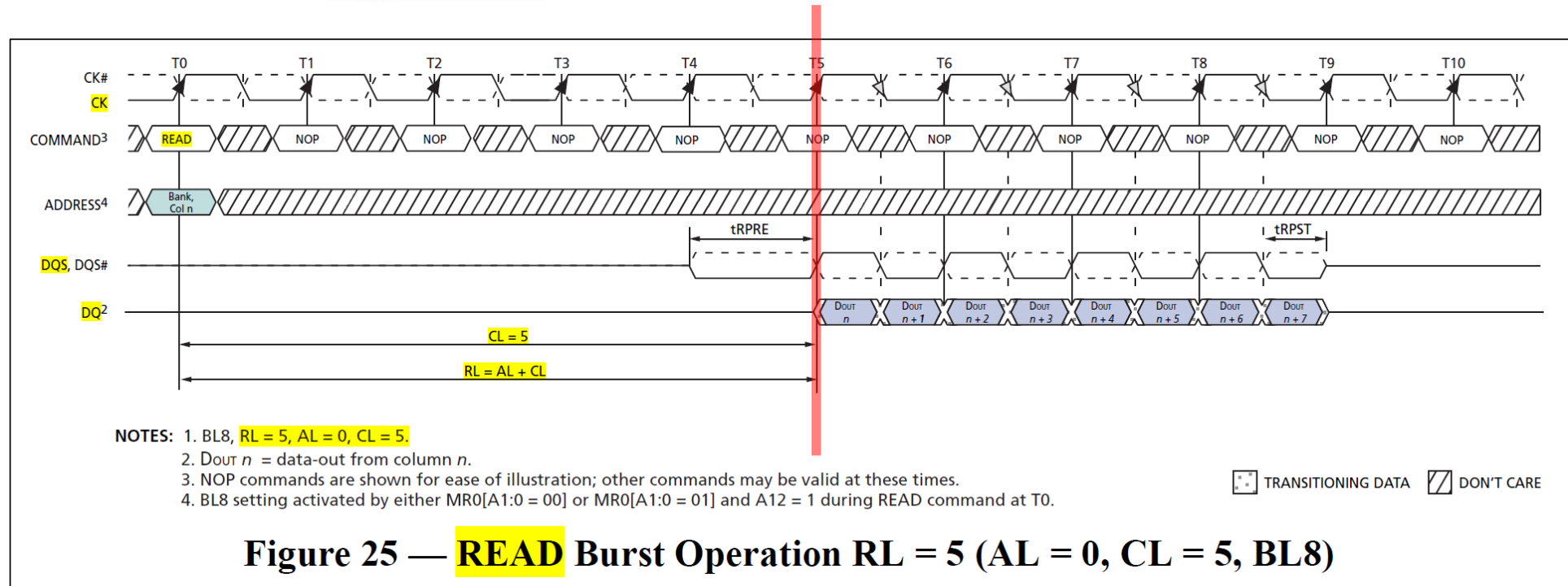
Memory modules transmit address/command and clock (CK) signals in the horizontal direction, and data (DQ) and strobe (DQS) signals in the vertical direction



EX1077, 8

JEDEC DDR3 standard: align clock (CK), strobe (DQS), and data (DQ) signals

JEDEC DDR3 SDRAM STANDARD

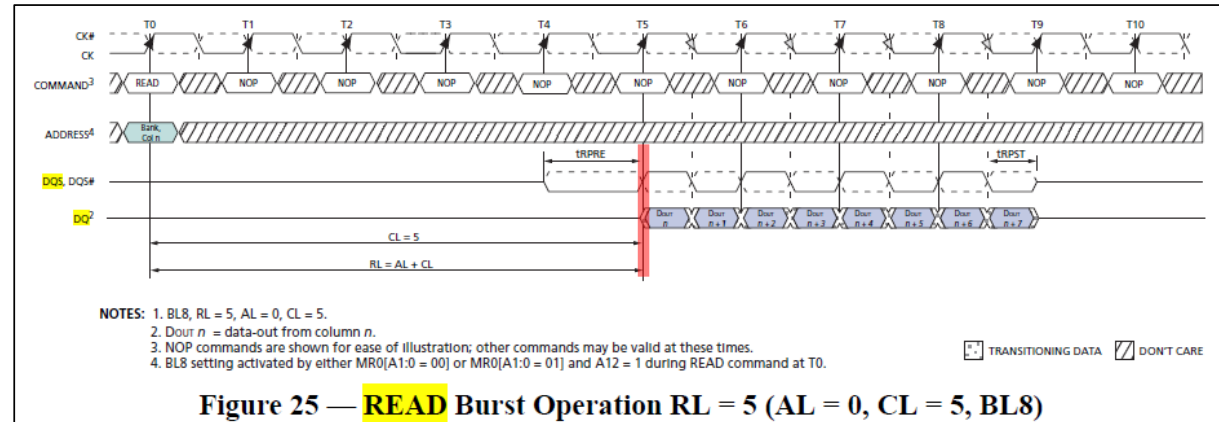


EX1020, 56; see also *id.* at 42, 48, 51, 68

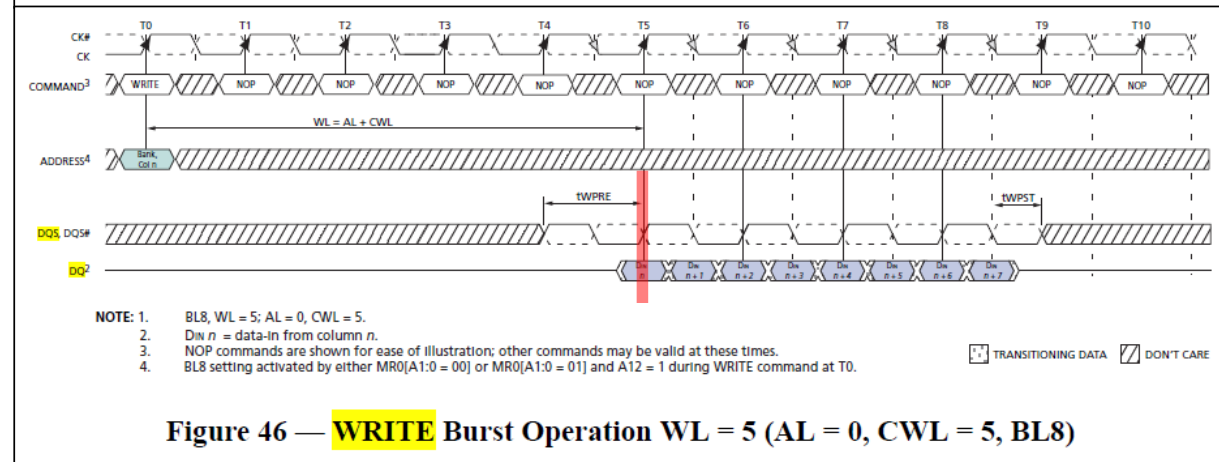
JEDEC DDR3 standard: read data is edge-aligned with DQS; write data is center-aligned

JEDEC DDR3 SDRAM STANDARD

Read is edge aligned:

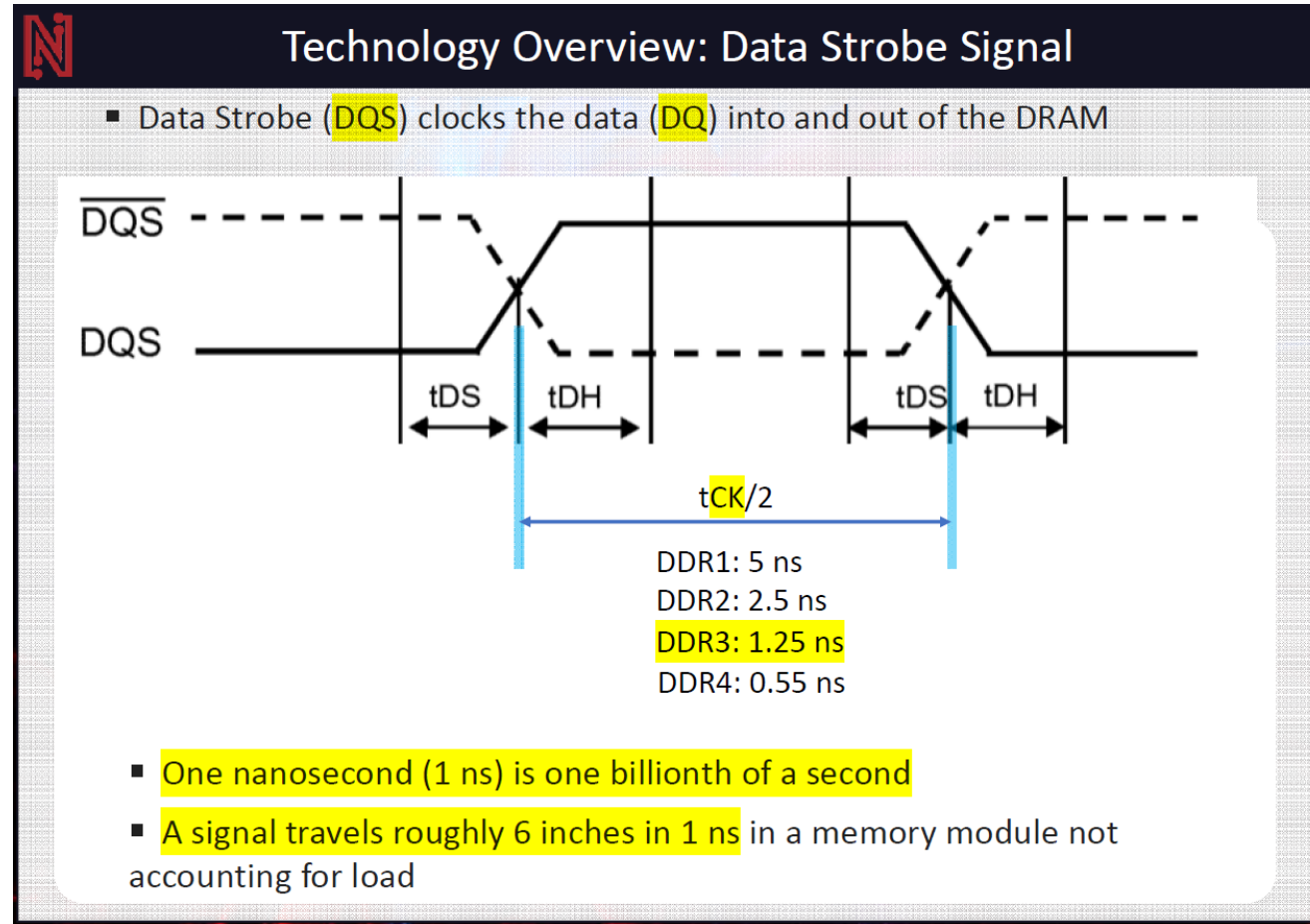


Write is center aligned:



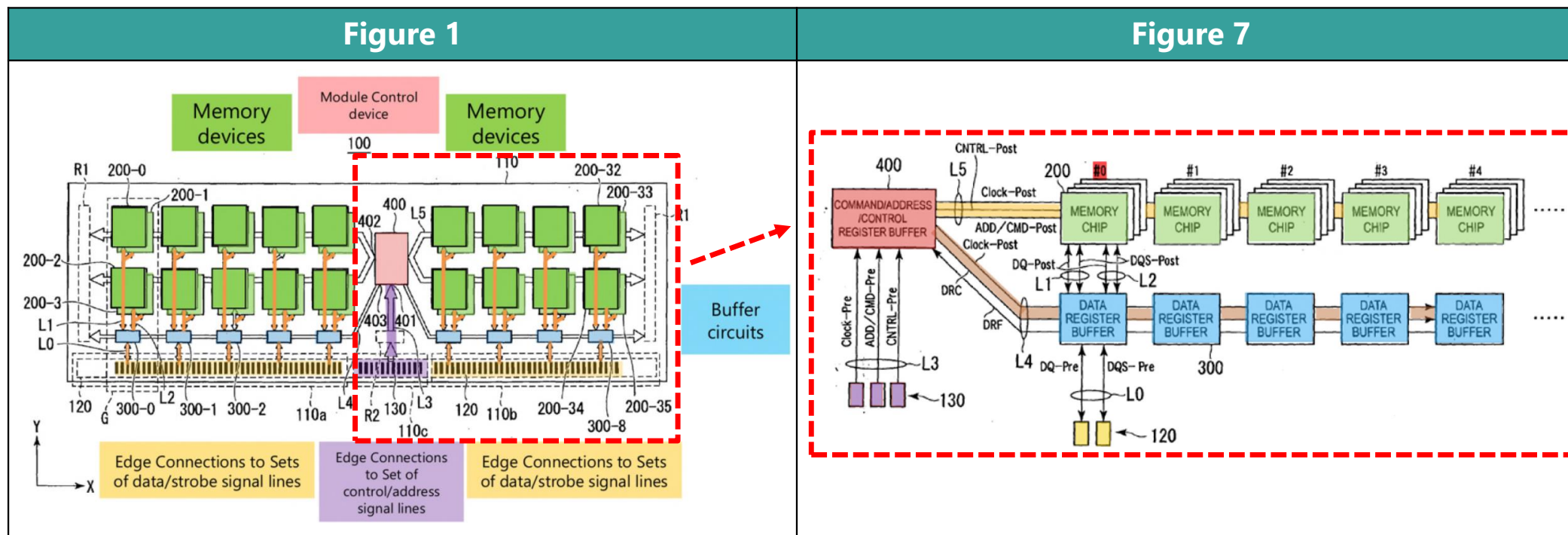
EX1020, 56, 71

By 2012, DDR3 memory devices had clock speeds around one billionth of a second, making it important to keep the strobe (DQS), data (DQ), and clock (CK) signals aligned



EX1077, 6; see also EX2015, 141 ("tCK"); EX1020, 59, 164 ("tDQSQ")

Hiraishi (U.S. Pat. Pub. No. 2010/0312956) [EX1005]



Abstract: A memory module includes a plurality of **memory chips** and a plurality of **data register buffers** mounted on the module substrate. At least two **memory chips** are allocated to each of the **data register buffers**. Each of the **data register buffers** includes M input/output terminals (M is a positive integer equal to or larger than 1) that are connected to the data connectors via a **first data line** and N input/output terminals (N is a positive integer equal to or larger than 2M) that are connected to corresponding **memory chips** via **second and third data lines**, so that the number of the **second and third data lines** is N/M times the number of the **first data lines**. According to the present invention, because the load capacities of the **second and third data lines** are reduced by a considerable amount, it is possible to realize a considerably high data transfer rate.

EX1005, Abstract

Hiraishi (left) is similar to the '608 Patent (right)

Figure 1 of Hiraishi [EX1005]

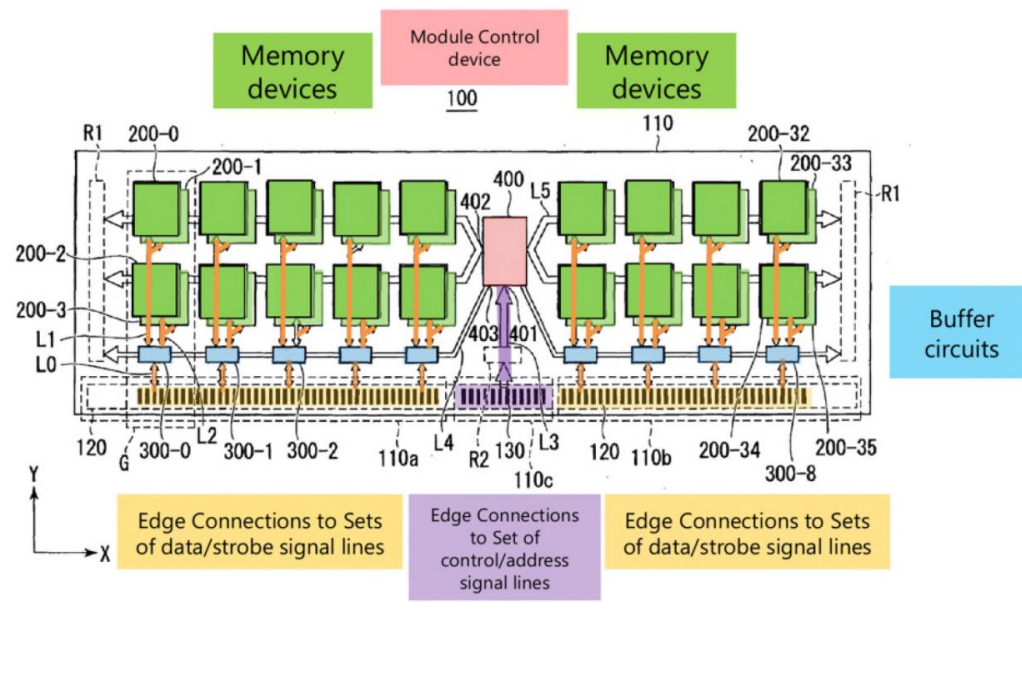


Figure 2C of '608 Patent [EX1001]

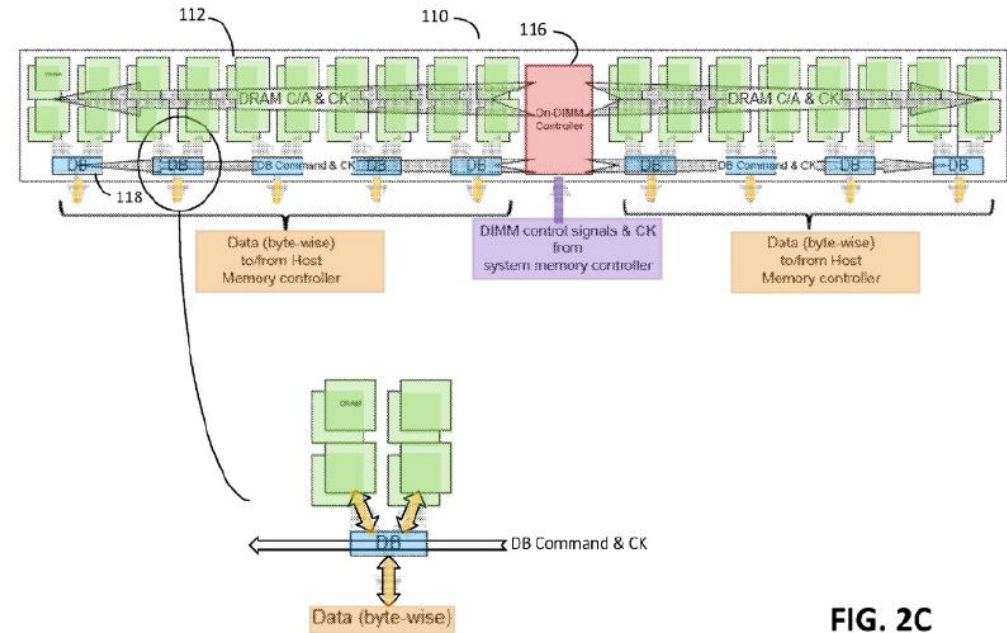
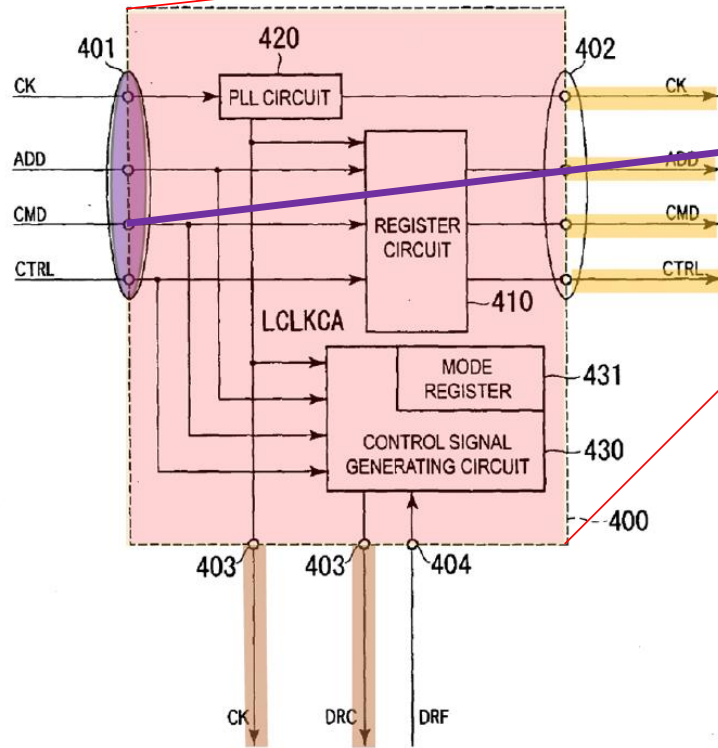


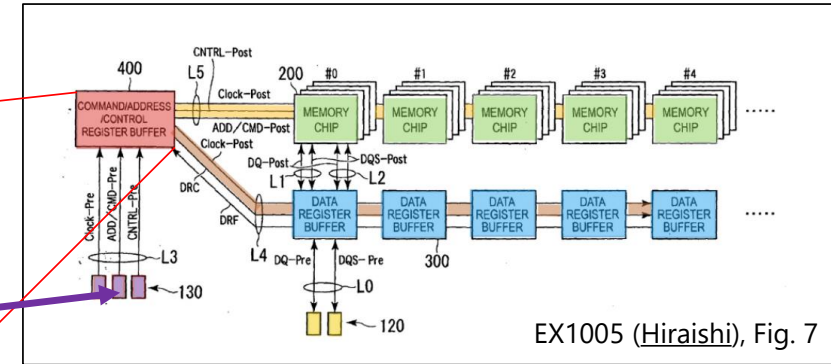
FIG. 2C

Hiraishi's Module Control Device



EX1005 (Hiraishi), Fig. 6

FIG.6

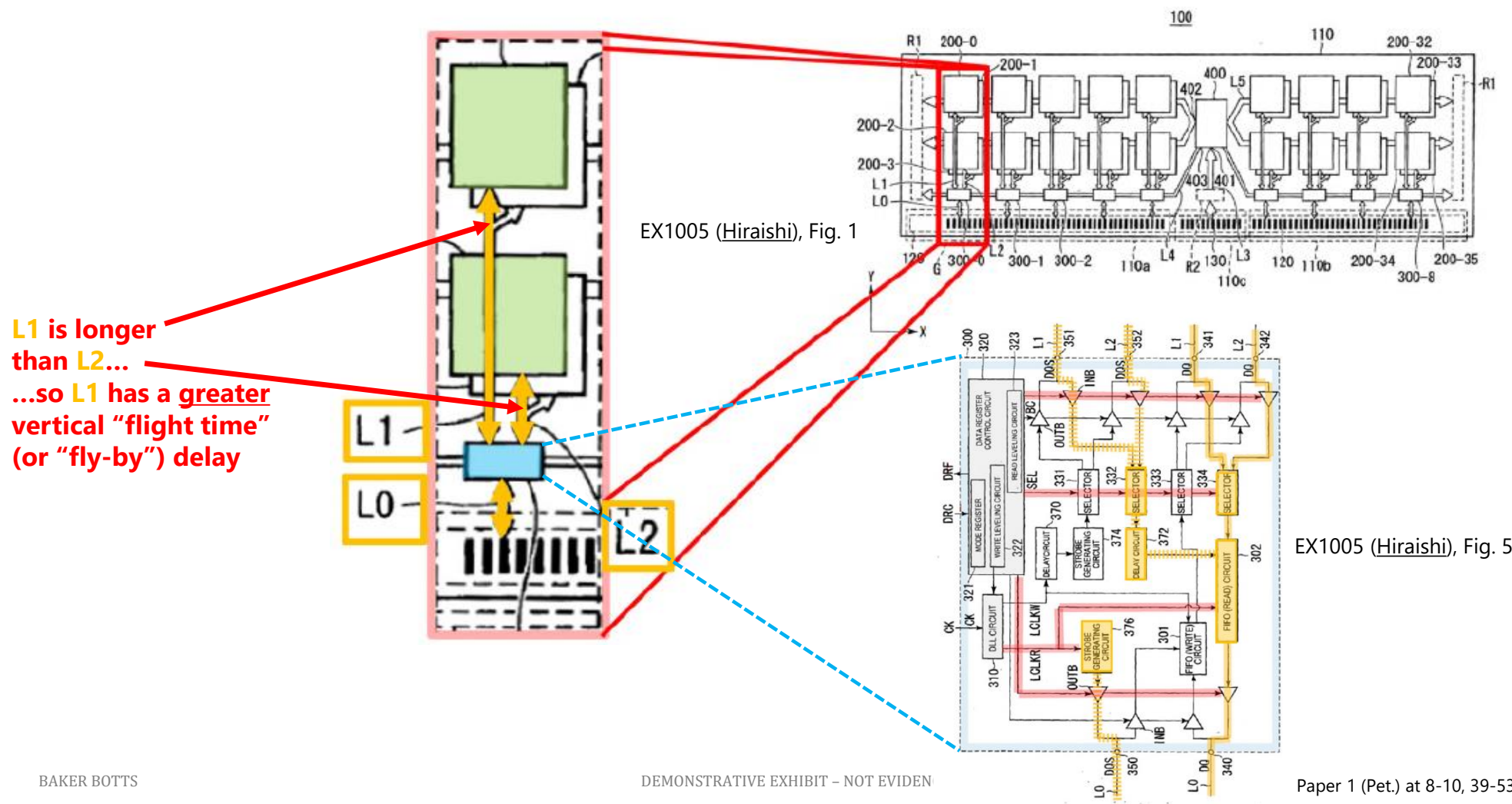


EX1005 (Hiraishi), Fig. 7

[0060] The command/address/control register buffer 400 receives the command signal, the address signal, the control signal, and the clock signal (in some cases, collectively referred to as a command/address/control signal and the like) that are supplied from the command/address/control connectors 130 through an input terminal 401, buffers the signals, and supplies the signals to the memory chips 200. At the same time, the command/address/control register buffer 400 generates a control signal. The command/address/control signal to be supplied to the memory chips 200 are output through an output terminal 402, and the control signal to be supplied to the data register buffers 300 are output through an output terminal 403.

EX1005 (Hiraishi), [0060]

Hiraishi's data buffer makes timing adjustments for DQ data and DQS strobe signals to account for vertical "flight time" delays on L1 and L2



Hiraishi's data buffer uses a two-step process to delay ("re-time") the DQ data and DQS strobe signals

First, during initialization, S4 read/write leveling (Figs. 13-15) measures and stores delays for DQ/DQS



Second, a normal read/write operation (Fig. 11 or 12) delays ("re-times") DQ/DQS based on the stored delays

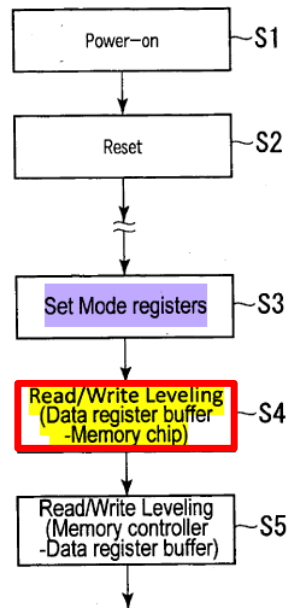


FIG.13

BAKER BOTTS

[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005 (Hiraishi), ¶[0130]

[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above,

EX1005 (Hiraishi), ¶[0135]

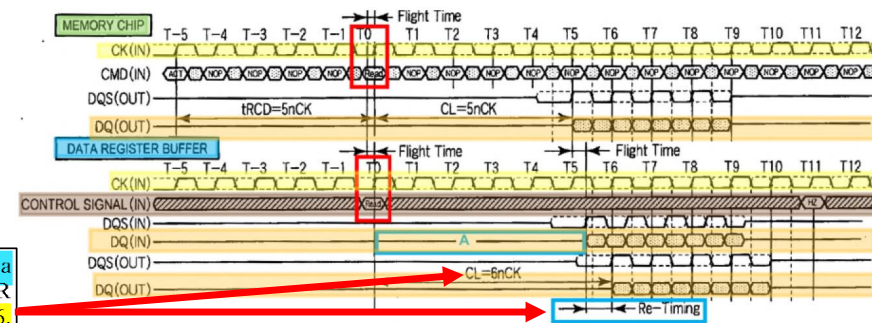


FIG.11

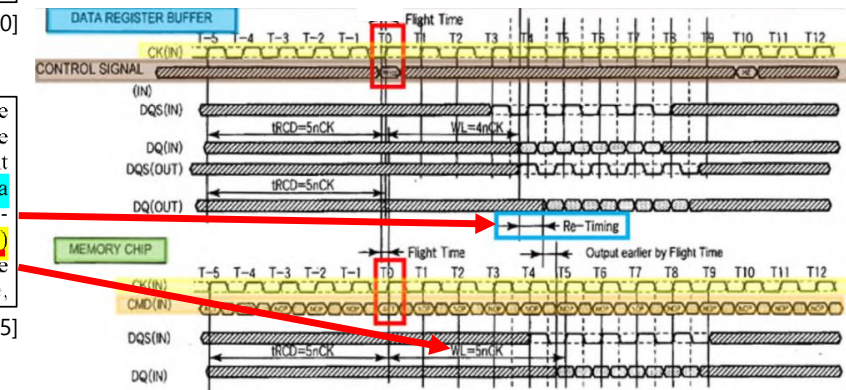


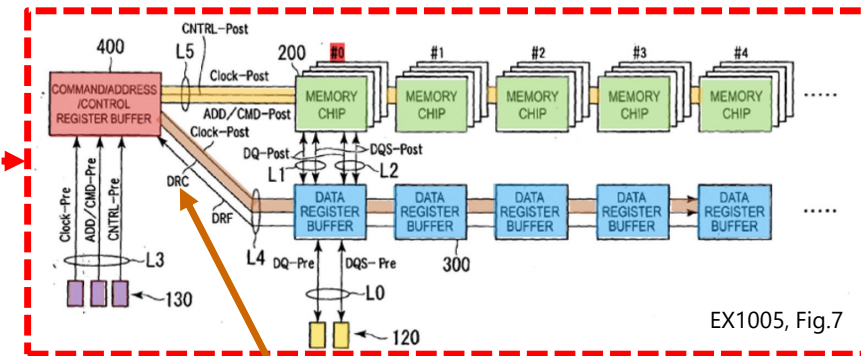
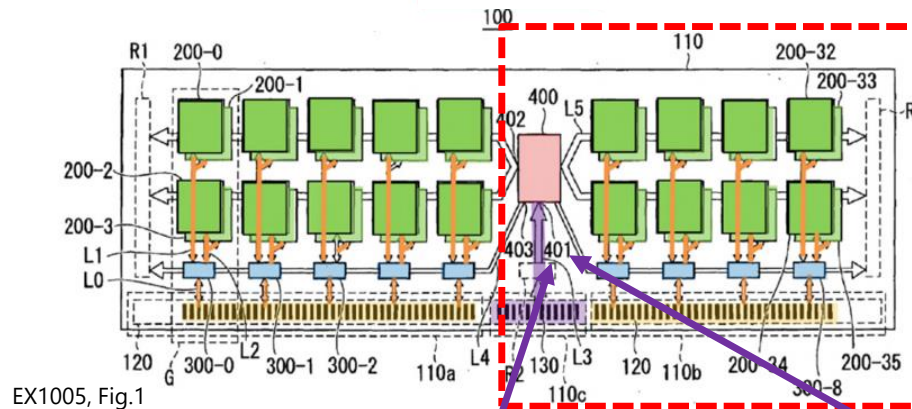
FIG.12

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

Paper 1 (Pet.) at 8-10, 25, 39-53

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First, the host computer's memory controller sends an MRS (mode register set) command, which is conveyed by DRC module control signals to the data buffers, which then perform S4 read/write leveling



ter buffer 400 performs the initializing operation. The initializing operation includes a mode register setting operation by which predetermined mode information is set in the mode registers 215, 321, and 431 that are included in the memory chip 200, the data register buffer 300, and the command/address/control register buffer 400, respectively (Step S3).

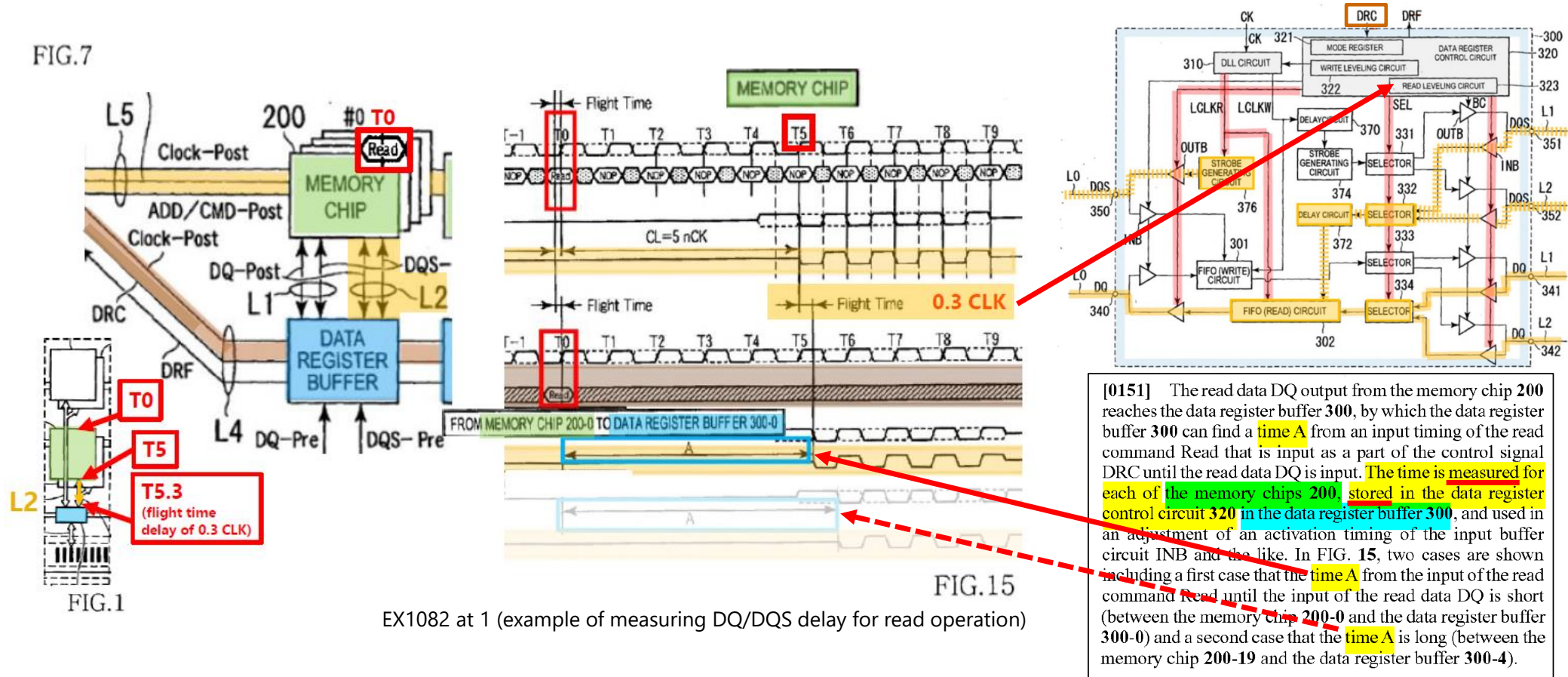
[0140] Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The level-

EX1005 at ¶¶[0139]-[0140]

[0099] The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to

EX1005 at ¶[0099]

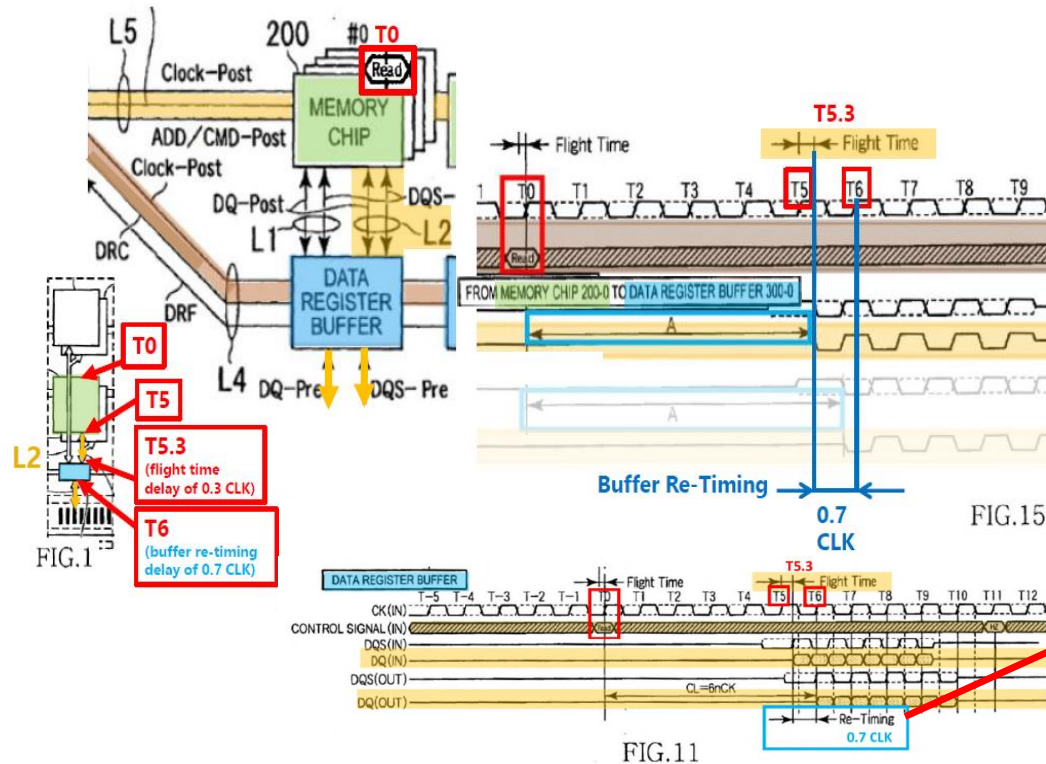
During S4 read/write leveling, the **data buffer** measures and stores vertical “Flight Time” (or “fly-by”) delays (e.g., 0.3 clock cycles for **L2**)



EX1005, ¶[0151] & Fig. 5

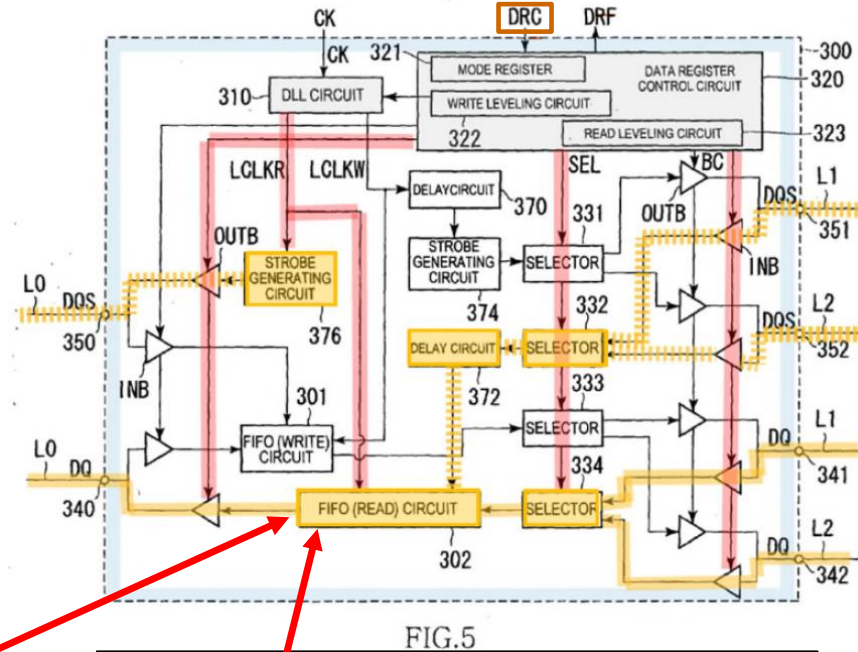
Second, during normal read/write operation, Hiraishi's data buffer uses the FIFO to delay ("re-time") the DQ data signals (e.g., by 0.7 clock cycles for L2)

FIG.7



EX1082 at 2 (example of measuring and applying DQ delay for read operation);

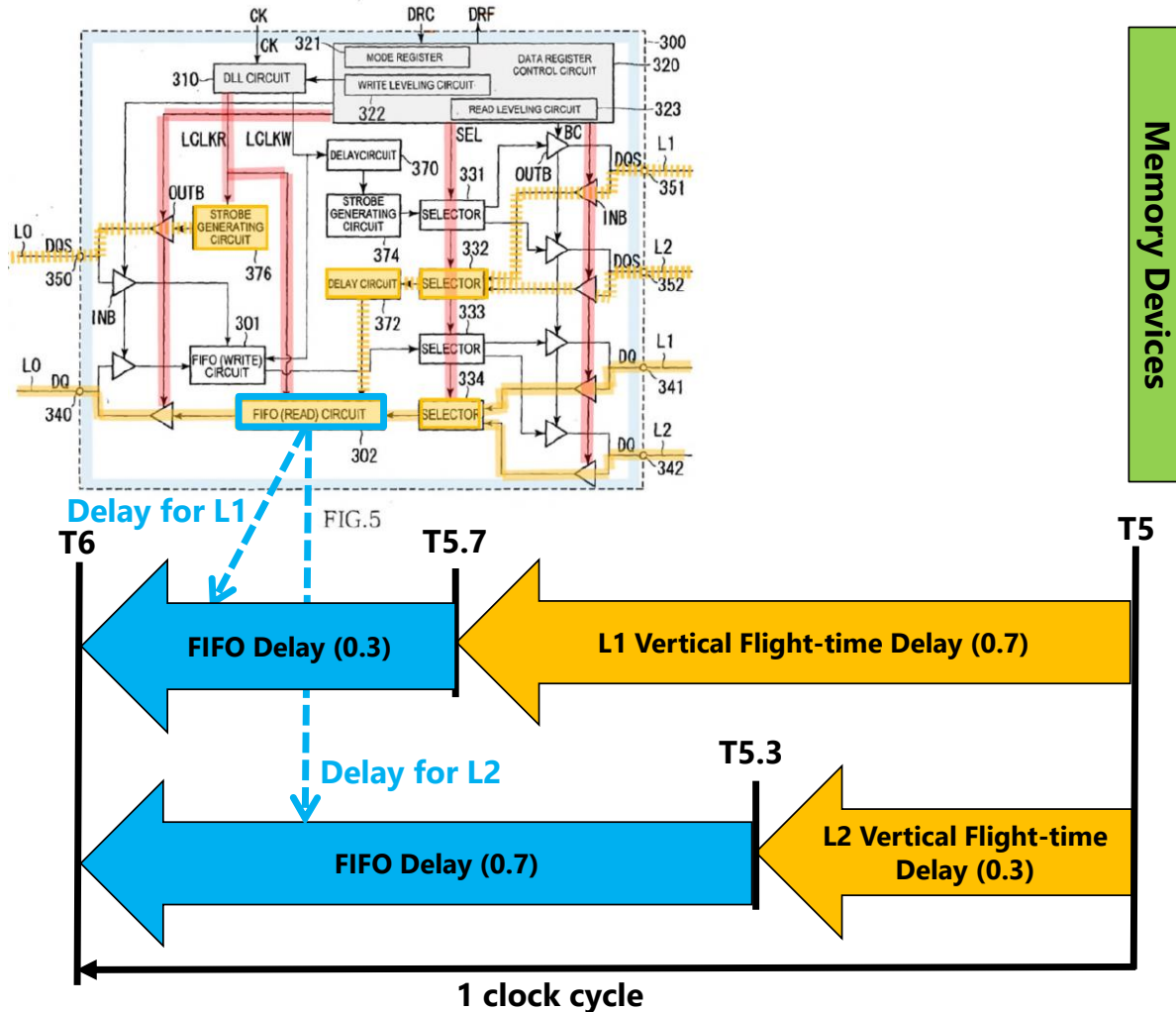
EX1070 at 1



[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005 at ¶[0130] & Fig. 5

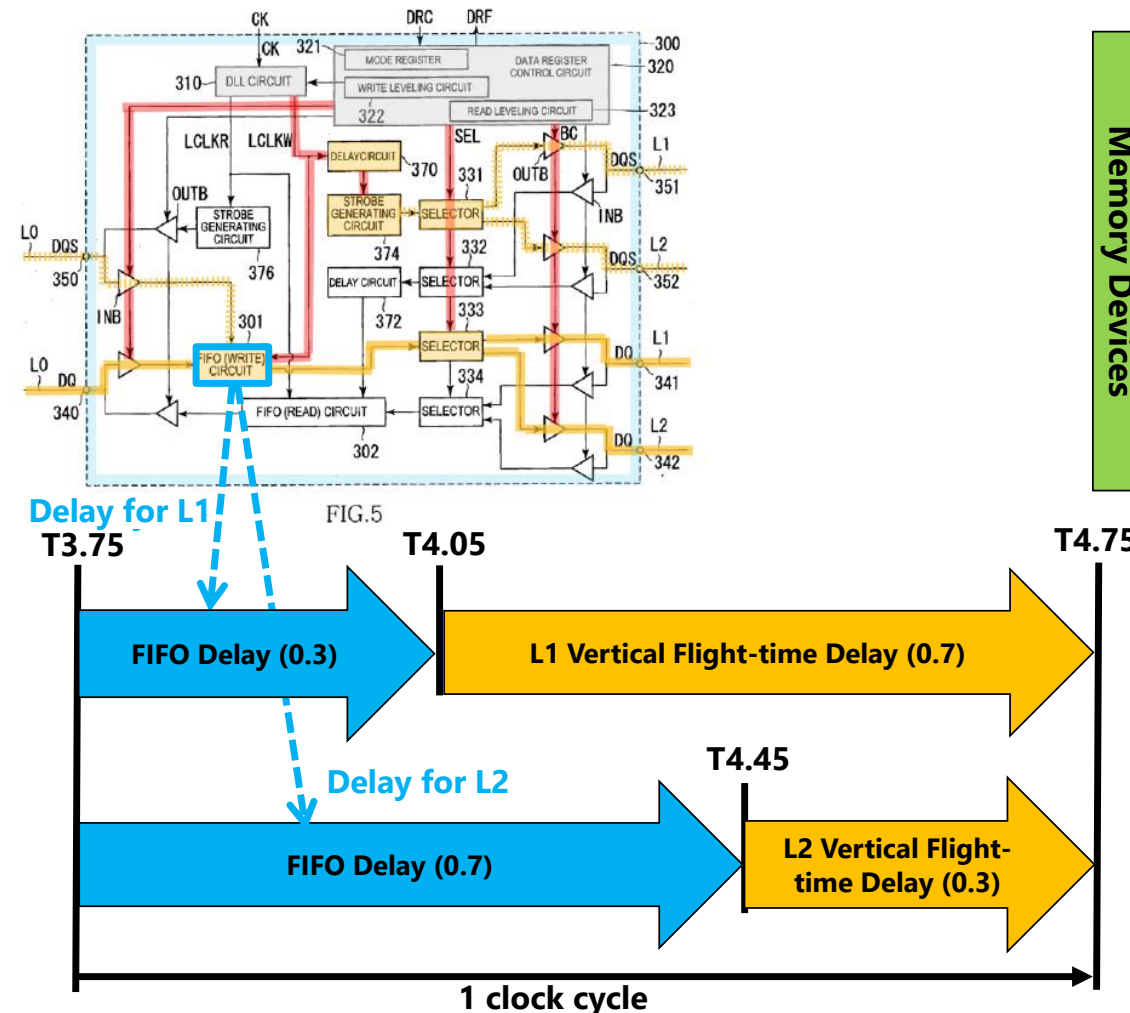
Hiraishi's data buffer provides a variable delay that depends on the amount of the vertical "Flight Time" (or "fly-by") delay (e.g., L1 or L2 delay)



Either L1 or L2 ... would be used at a given time, to avoid conflicts.... [L]ike Figures 15-16 of the '608 Patent ..., Hiraishi's data paths have a "fork in the road" arrangement for routing data and strobe signals from either one (L1) or the other (L2) branch to the same output (terminal 350, coupled to line L0 for strobe signals; terminal 340, coupled to line L0 for data signals) during read operations.

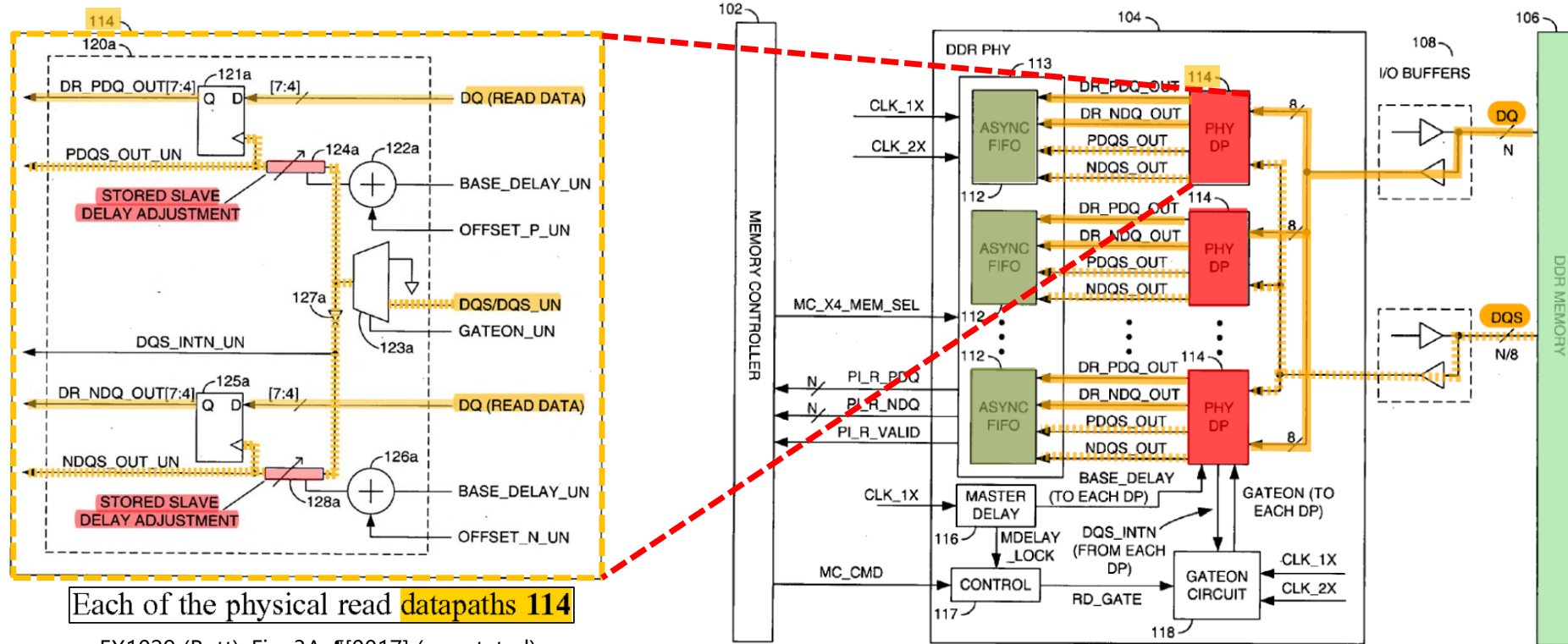
Paper 1 (Pet.) at 68

Hiraishi's data buffer provides a variable delay that depends on the amount of the vertical "Flight Time" (or "fly-by") delay (e.g., L1 or L2 delay)



Butt (U.S. Pat. Pub. No. 2007/0008791) [EX1029]

Butt discloses the details of buffering and adjusting **DQ/DQS signals** in the **data paths**.



Each of the physical read datapaths 114

EX1029 (Butt), Fig. 3A, ¶[0017] (annotated)

EX1029 (Butt), Fig. 2 (annotated)

GROUND 1 02

GROUND 1: HIRAISHI + BUTT

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COMBINATION FOR GROUND 1

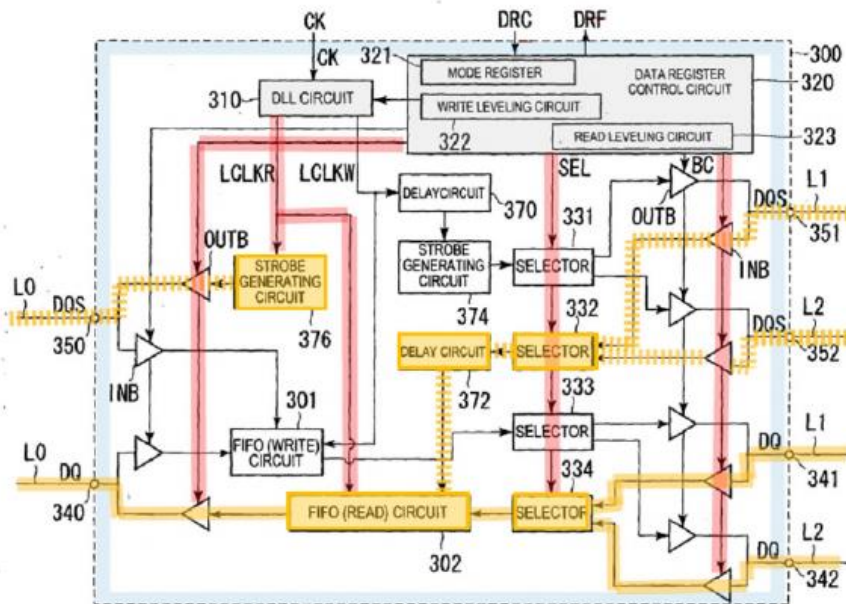
DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



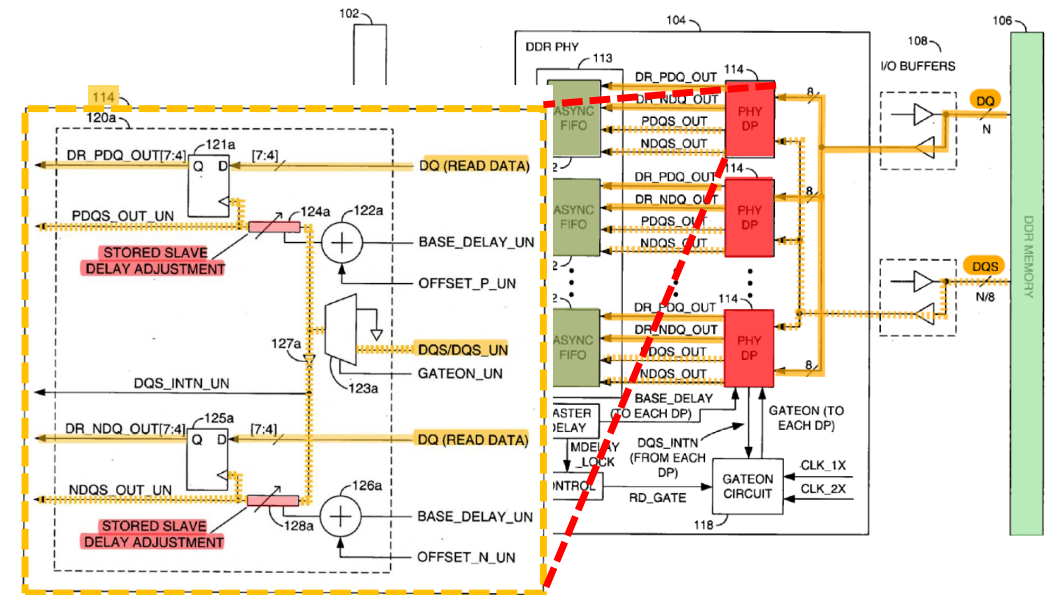
Samsung Electronics Co., Ltd.
Ex. 1059, p. 28

Ground 1: Hiraishi + Butt — data buffer removes vertical flight-time delays in the “data path,” which includes DQ data and DQS strobe signals

Hiraishi: Memory module with **data buffers** that adjust **DQ/DQS signals** to remove vertical flight-time delays



Butt: Details of buffering and adjusting **DQ/DQS signals** in data paths



data path (114)

- Both references directed to accurately timing memory data transmissions
- Both references teaching adjusting DQ/DQS signals, using components such as FIFO
- “[A] POSITA...would have been motivated to implement Butt’s data path controlling technique in Hiraishi’s ... buffer”

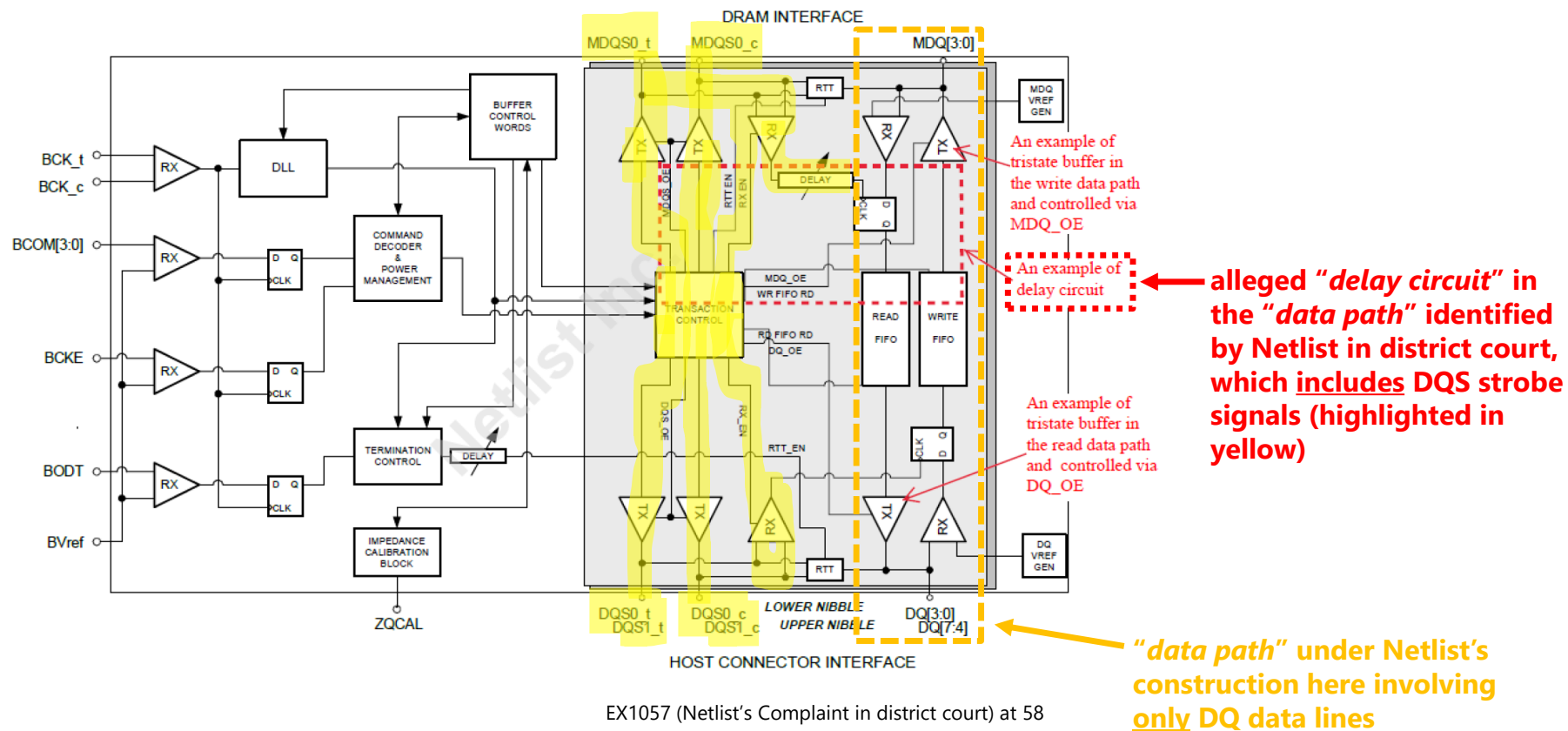
GROUND 1 HAS A "DELAY CIRCUIT" IN THE
"DATA PATH," EVEN UNDER NETLIST'S CONSTRUCTION,
THAT DELAYS IN RESPONSE TO "MODULE CONTROL
SIGNALS" IN RESPONSE TO "SYSTEM COMMAND SIGNALS"

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE



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Netlist has changed its construction for **"data path"**: Before this IPR, Netlist filed a Complaint against Samsung asserting that the **"data path"** (in the dashed red box below) includes DQS strobe signals (highlighted in yellow), but in this IPR Netlist is construing the **"data path"** to be limited to **DQ data lines**



Hiraishi's disclosure (left) is substantially identical to the '608 Patent's preferred embodiment of the "delay circuit" in the "data path," even under Netlist's construction

Figure 5 of Hiraishi [EX1005]

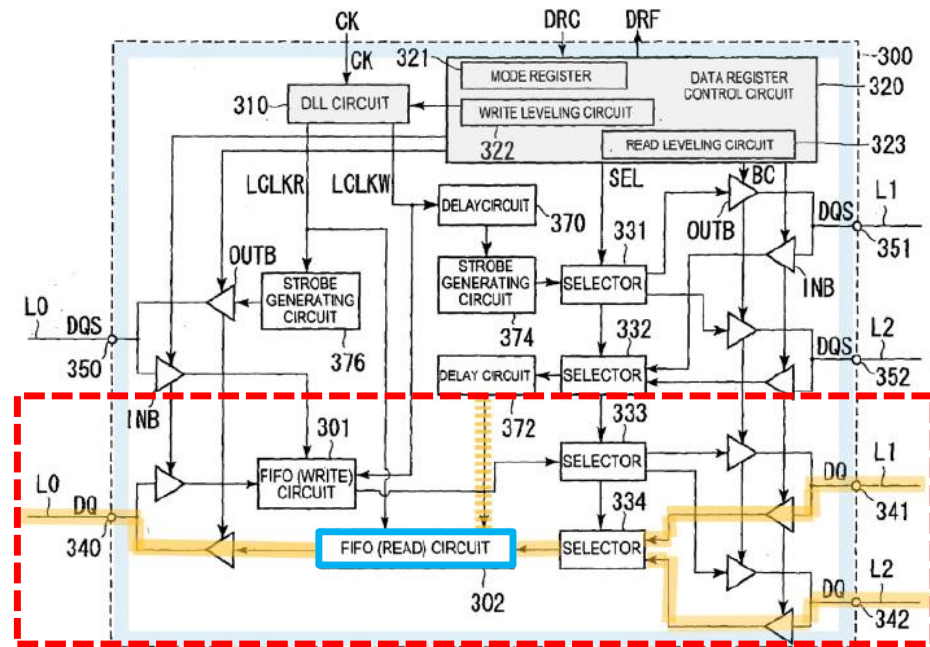


FIG.5

Figure 16 of the '608 Patent [EX1080]

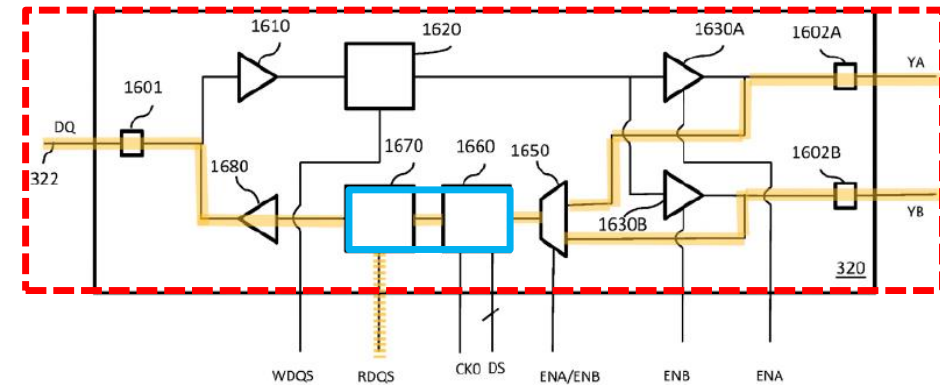


FIG. 16

Hiraishi's data buffer has a **"delay circuit"** for **read operations** (e.g., FIFO (Read) circuit 302) in the **"data path,"** even under Netlist's construction

Therefore, Ground 1 discloses the claimed **"delay circuit"** for read operations, including the FIFO (read) circuit 302 delaying the read data signal,

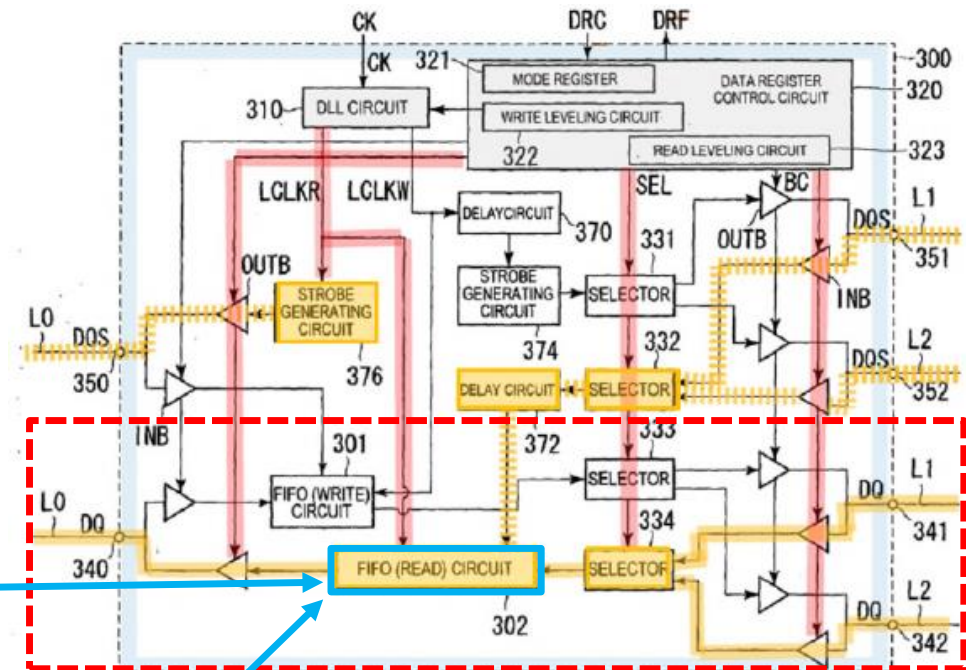
Paper 1 (Pet.) at 51

as an input trigger signal."). The output of the FIFO (read) circuit 302 is timed by the internal clock LCLKR generated by the DLL circuit 310, therefore delaying the read data signal by a variable amount that is determined such that it is output in synchronization with the clock signal CK at CL=6 after the Read command. *Id.* at

EX1003 at 1166

[0130] Thereafter, the data register buffer 300 performs a **re-timing** in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005 at ¶[0130]



"delay circuit" under
Netlist's construction

"data path" under
Netlist's construction

Hiraishi's data buffer has a "delay circuit" for write operations (e.g., FIFO (Write) circuit 301) in the "data path," even under Netlist's construction

Therefore, Ground 1's delay circuit for write operations includes the Write FIFO circuit 301 delaying the write data signal, delay circuit 370 delaying the LCLKW signal,

Paper 1 (Pet.) at 47



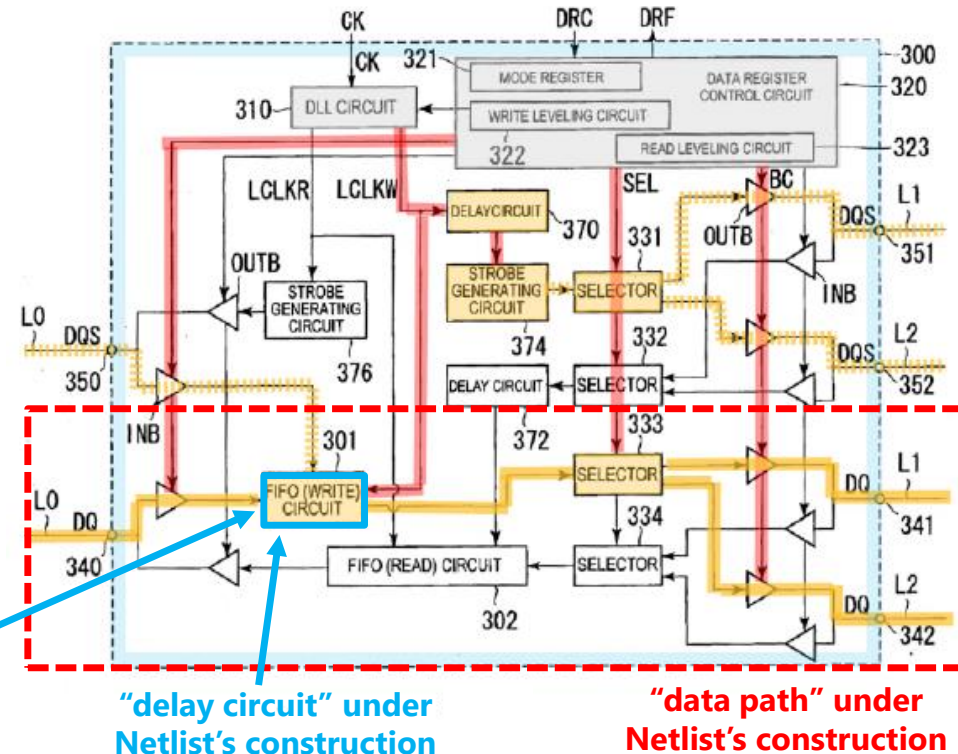
A Skilled Artisan would have understood from this disclosure that Hiraishi's delay circuit for write operations includes the FIFO (write) circuit 301 and performs a re-timing of the DQ/DQS signals in synchronization with the delayed internal clock

LCLKW. The LCLKW signal is generated by DLL circuit 310 and used to time

EX1003 at ¶161

[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above,

EX1005 at ¶[0135]



Hiraishi's disclosure (left) is substantially identical to the '608 Patent's preferred embodiment of the "delay circuit" in the "data path," even under Netlist's construction



Q. The clock signal CK0 and the delay signal DS control the delay circuit 1660 in Figure 16 similar to how they control the delay circuit 1560 in Figure 15; is that fair?

A. CK0 and DS are shown controlling the delayed circuit 1660 and 1560, presumably in a similar, but maybe not identical manner.

...

Q. In Figure 16, the sampler circuit 1670 uses the RDQS strobe signal to sample the output of the delay circuit 1660; is that fair?

A. Yes, I see that.

...

Q. So the delay control circuit 650, which is inside the data buffer which is also sometimes referred to as the isolation device, provides the determined delay amount via the delay signal DS to both the DQ and DQS routing circuits 320 and 620 that are illustrated in more detail in Figures 15 and 16; is that fair?

A. Yes, I think that's fair.

EX1074 at 153:2-8, 154:6-9, 169:25-170:7

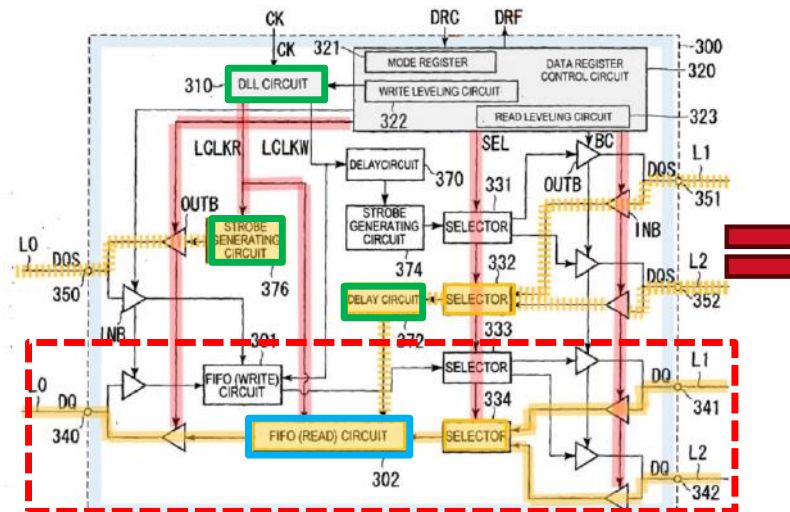
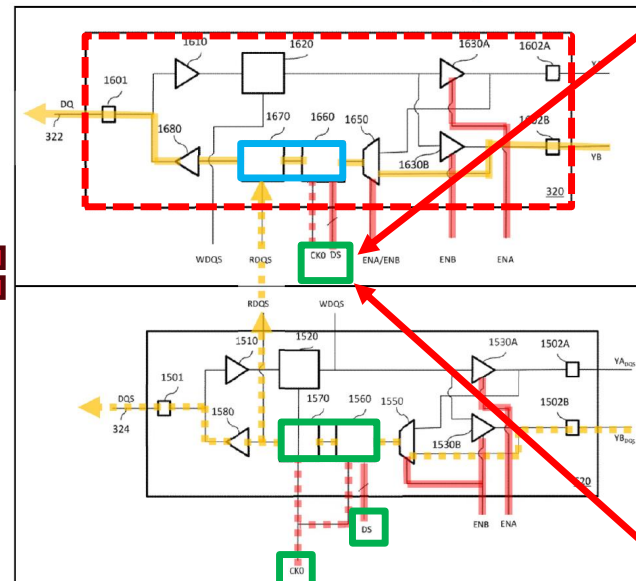


FIG. 5

Read direction — '608 Patent (EX1001) Figures 16 & 15



The Institution Decision correctly found that Hiraishi's data buffer delays data signals "in response to ... module control signals" (e.g., DRC)



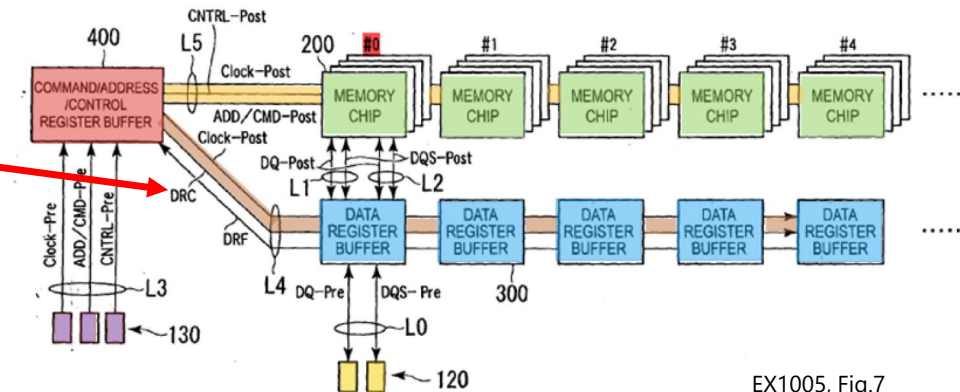
vii. Limitation 1[f]

Petitioner asserts that Hiraishi discloses that the data path corresponding to each data signal line includes at least one tristate buffer, i.e. "output buffers OUTB and input buffers INB," controlled by the command processing circuit, and a delay circuit, i.e., "DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376," configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. Pet. 39.

Although Petitioner asserts that it is ambiguous as to whether the claim 1 language "in response to at least one of the module control signals" modifies the term "to delay" or the term "determined," Petitioner contends that the combination of Hiraishi and Butt discloses either interpretation. *Id.* at 43 (citing Ex. 1003 ¶ 155).

Petitioner also argues that Hiraishi discloses, with respect to the flow chart shown in Figure 13, a step "S4 Read/Write leveling to determine the delay through the data path." Pet. 42 (citing Ex. 1003 ¶ 152; Ex. 1005, Figs. 5, 13). Petitioner asserts that in a write leveling operation that is

We have reviewed the evidence and argument, which includes un rebutted expert testimony, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that the combination of Hiraishi and Butt teaches limitation 1[f].

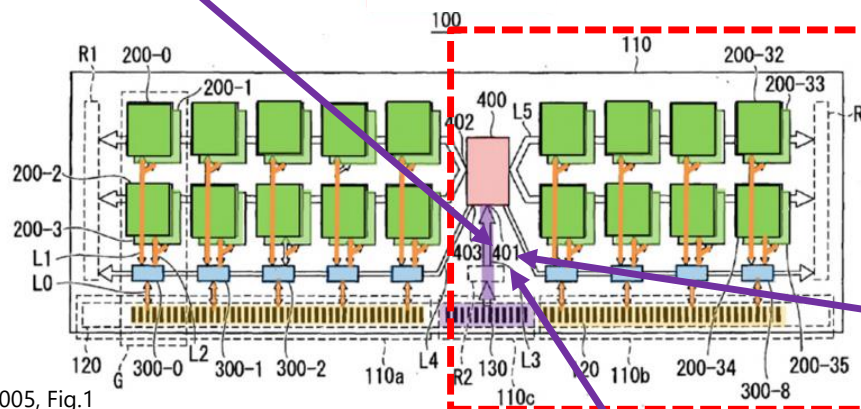


EX1005, Fig. 7

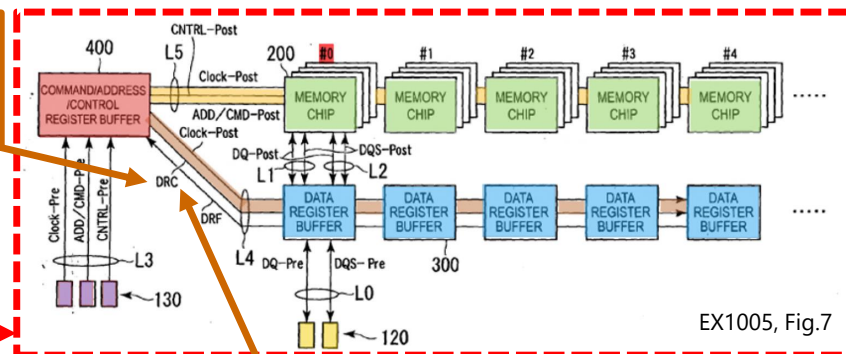
Hiraishi's data buffer performs S4 read/write leveling in response to DRC "module control signals," which are in response to MRS (mode register set) "system command signals" from the host

claim [1.b] "system command signals"

claim [1.f] "module control signals" in response to the [1.b] "system command signals"



EX1005, Fig.1



EX1005, Fig.7

[0099] The control signal generating circuit 430 is a circuit that generates the control signal DRC to be supplied to the data register buffer 300 based on the command/address/control signal supplied via the input terminal 401, of which an operation is performed in synchronization with the internal clock LCLKCA. The control signal DRC for the data register buffer 300 is supplied to the data register buffer 300 via the output terminal 403. The feedback signal DRF is supplied to

EX1005 at ¶[0099]

operation subsequent to the first memory operation." EX1003, ¶172. The memory devices perform the read/write leveling operations and read/write operations in response to commands, including mode register set commands and read/write commands. EX1003, ¶¶172-173; EX1020, 29, 31, 33, 43, 48-54.

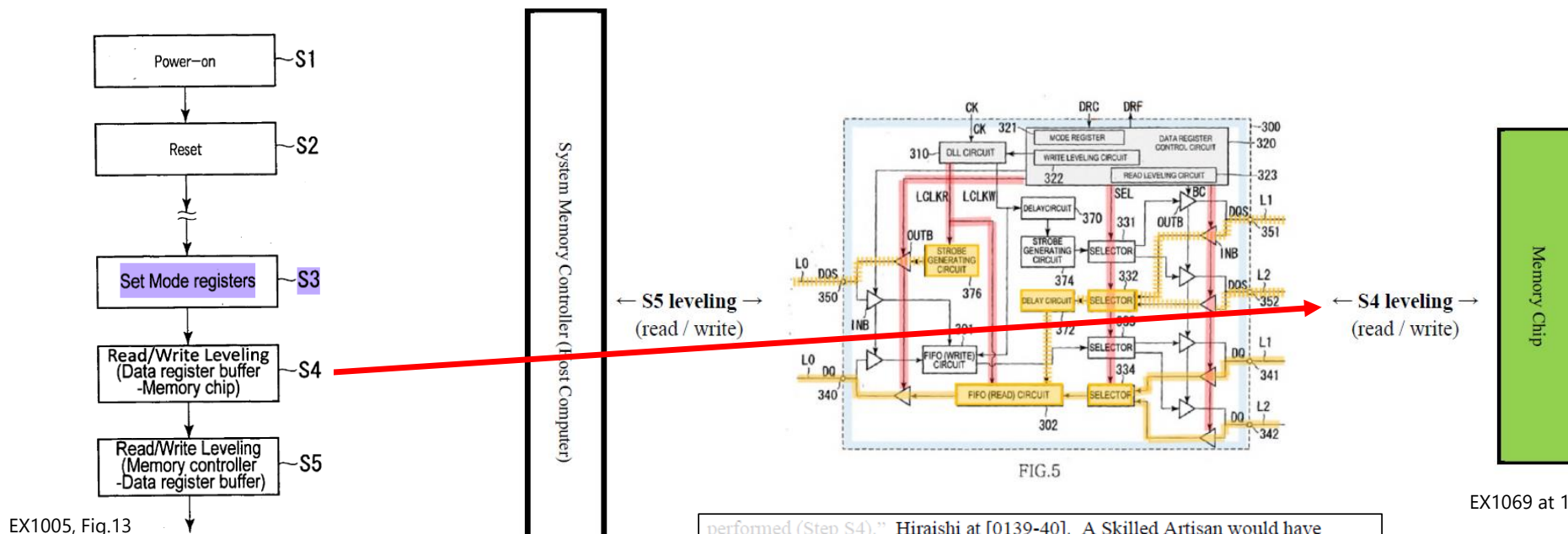
Hiraishi's S-4 write leveling operation is performed during initialization in response to module control signals (e.g., DRC conveying "mode switching" or "mode register set" commands) by a write leveling circuit 322 "to adjust a write timing...in consideration of a propagation time of a signal." EX1003, ¶159;

Paper 1 (Pet.) at 44, 53; see also EX1003 at ¶176

ter buffer 400 performs the initializing operation. The initializing operation includes a mode register setting operation by which predetermined mode information is set in the mode registers 215, 321, and 431 that are included in the memory chip 200, the data register buffer 300, and the command/address/control register buffer 400, respectively (Step S3). [0140] Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The level-

EX1005 at ¶¶[0139]-[0140]

Hiraishi teaches that S4 read/write leveling is performed (during initialization) in response to the MRS command, consistent with the JEDEC standard for DDR3



ter buffer 400 performs the initializing operation. The initial-
izing operation includes a mode register setting operation by
which predetermined mode information is set in the mode
registers 215, 321, and 431 that are included in the memory
chip 200, the data register buffer 300, and the command/
address/control register buffer 400, respectively (Step S3).
[0140] Upon completing the mode register setting opera-
tion, a leveling operation between the data register buffer 300
and the memory chip 200 is performed (Step S4). The level-

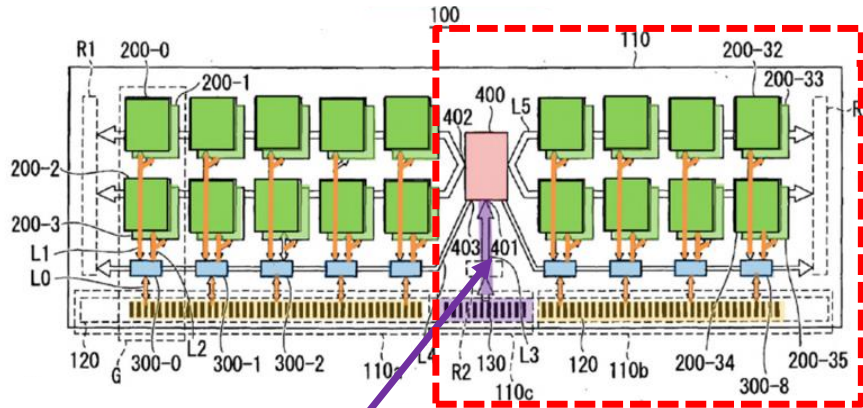
EX1005 at ¶¶[0139]-[0140]

performed (Step S4).” Hiraishi at [0139-40]. A Skilled Artisan would have
understood from this disclosure that the system memory controller instructs the
command/address/control register buffer on Hiraishi’s module to perform the S4
read/write leveling using “a first set of command signals,” similar to the mode
switching commands and mode register set commands for read and write leveling
in the memory devices. See, e.g., EX1020 (JESD79-3C) at 31, 33, 48-54 (multi-
purpose register for read calibration), 43 (mode register setting for write leveling);

EX1003 at ¶176; see also Paper 1(Pet.) at 44, 53-54



The JEDEC standard confirms that Hiraishi's **data buffer** performs **S4 read/write leveling** (during initialization) in response to the **MRS** command



EX1005, Fig.1

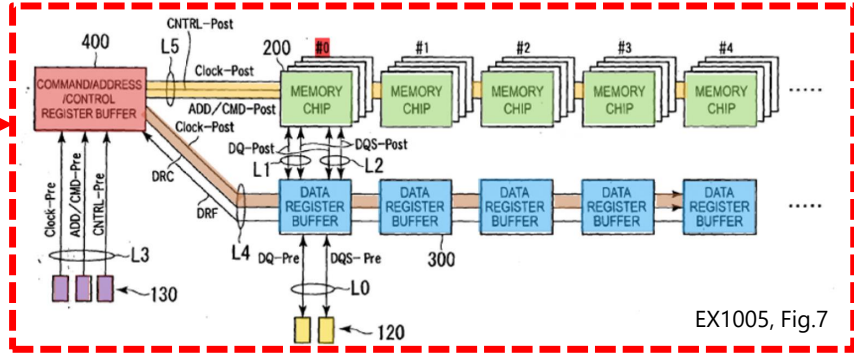
JEDEC DDR3 SDRAM Standard

3.3.1 Power-up Initialization Sequence

The following sequence is required for POWER UP and Initialization.

6. Issue MRS Command to load MR2 with all application settings. (To issue MRS command for MR2, provide "Low" to BA0 and BA2, "High" to BA1.)
7. Issue MRS Command to load MR3 with all application settings. (To issue MRS command for MR3, provide "Low" to BA2, "High" to BA0 and BA1.)
8. Issue MRS Command to load MR1 with all application settings and DLL enabled. (To issue "DLL Enable" command, provide "Low" to A0, "High" to BA0 and "Low" to BA1 - BA2).
9. Issue MRS Command to load MR0 with all application settings and "DLL reset". (To issue DLL reset command, provide "High" to A8 and "Low" to BA0-2).

EX1020 at 19; EX1074 at 105:12-22



EX1005, Fig.7

3.4.5 Mode Register MR3

MPR Operation

A2	MPR
0	Normal operation* ³
1	Dataflow from MPR

MPR Address

A1	A0	MPR location
0	0	Predefined pattern* ²
0	1	RFU
1	0	RFU
1	1	RFU

* 2 : The predefined pattern will be used for read synchronization.

EX1020, 31, 48, 50-51;
EX1074, 79:23-80:14, 89:6-90:9,
123:8-128:21

3.4.3 Mode Register MR1

A7	Write leveling enable
0	Disabled
1	Enabled

EX1020, 26, 42;
EX1074, 89:6-90:9, 119:20-123:7

During S4 read/write leveling, Hiraishi's data buffer determines the amount of delay "in response to ... module control signals" (e.g., DRC)

circuit" must respond *directly* to DRC ("module control signals"). As explained in the Petition, there is a two-step process that satisfies [1.f]: First, **during initialization, the DRC signal causes the Data Register Control Circuit 320 to perform S4 read/write leveling, which determines and stores the *variable*⁴ amount of delay needed** (as shown in Figures 14-15 of Hiraishi), and second, during

Paper 23 (Reply) at 18

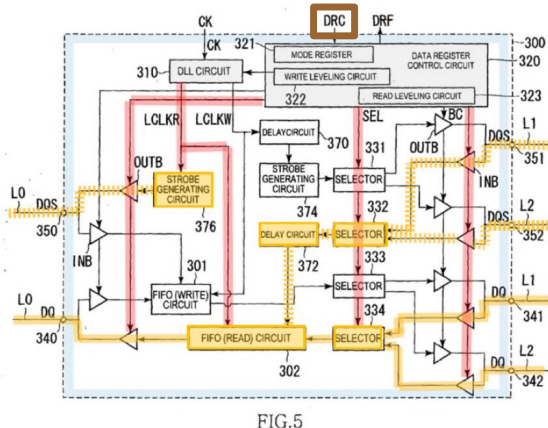


FIG. 5

[0142] FIGS. 14A and 14B are timing charts for explaining the write leveling operation between the data register buffer 300 and the memory chip 200, where FIG. 14A is a timing chart at the time of starting the leveling and FIG. 14B is a timing chart at the time of ending the leveling. This operation is performed by the write leveling circuit 322 shown in FIG. 5.

EX1005 at ¶[0142]

[0147] FIG. 15 is a timing chart for explaining the read leveling operation between the data register buffer 300 and the memory chip 200. This operation is performed by the read leveling circuit 323 shown in FIG. 5.

EX1005 at ¶[0147]

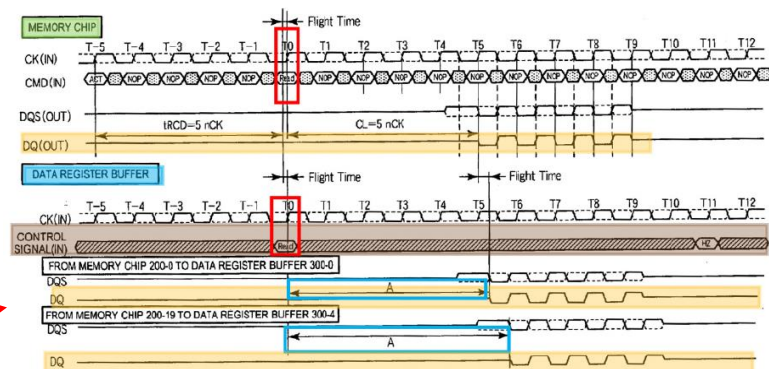
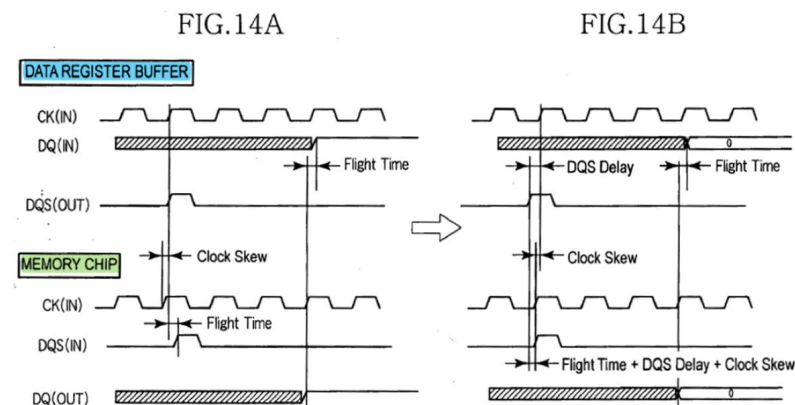


FIG. 15

During normal read/write operations, Hiraishi's data buffer uses the determined amount to delay ("re-time") data signals *"in response to ... module control signals"* (e.g., DRC) in response to read/write *"system command signals"* from the host

of delay needed (as shown in Figures 14-15 of Hiraishi), and second, during normal operation (e.g., in response to a read/write command transmitted via DRC), that stored delay amount is used to control the “*delay circuit*” to delay (i.e., “re-tim[e]”) both the DQ data signals (e.g., using the FIFOs 301/302) and the DQS strobe signals associated with that normal read/write command (as shown in Figures 11-12 of Hiraishi). Pet. 37-51; EX1070 (Figures 11 & 15); EX1071

Paper 23 (Reply) at 18-19

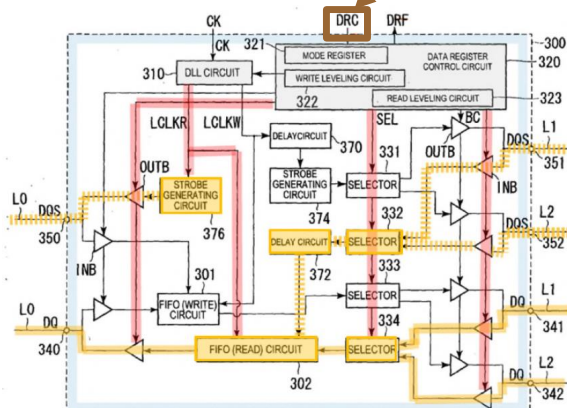


FIG.5

[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS, as described above.

EX1005 at ¶[0135]

[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL-6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

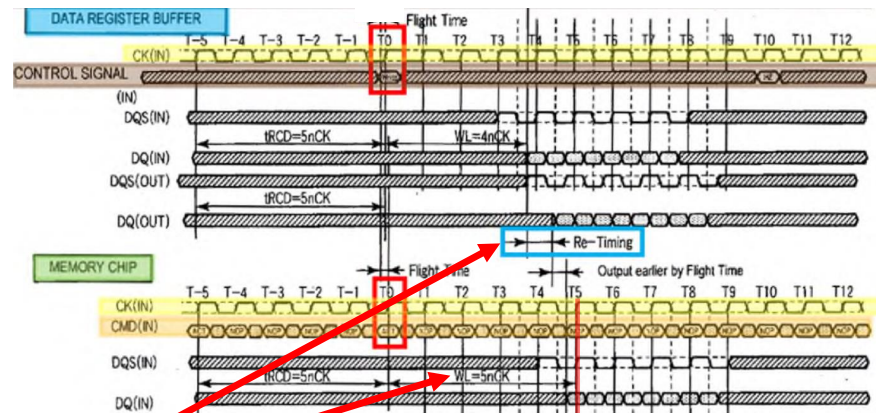
EX1005 at $\Uparrow[0130]$ 

FIG.12

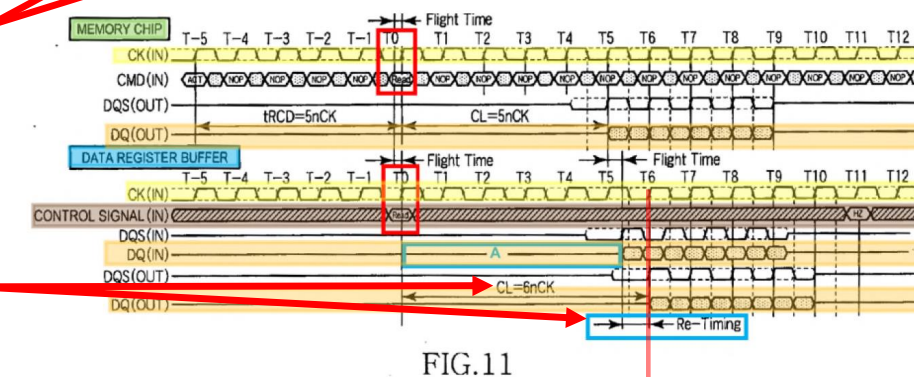
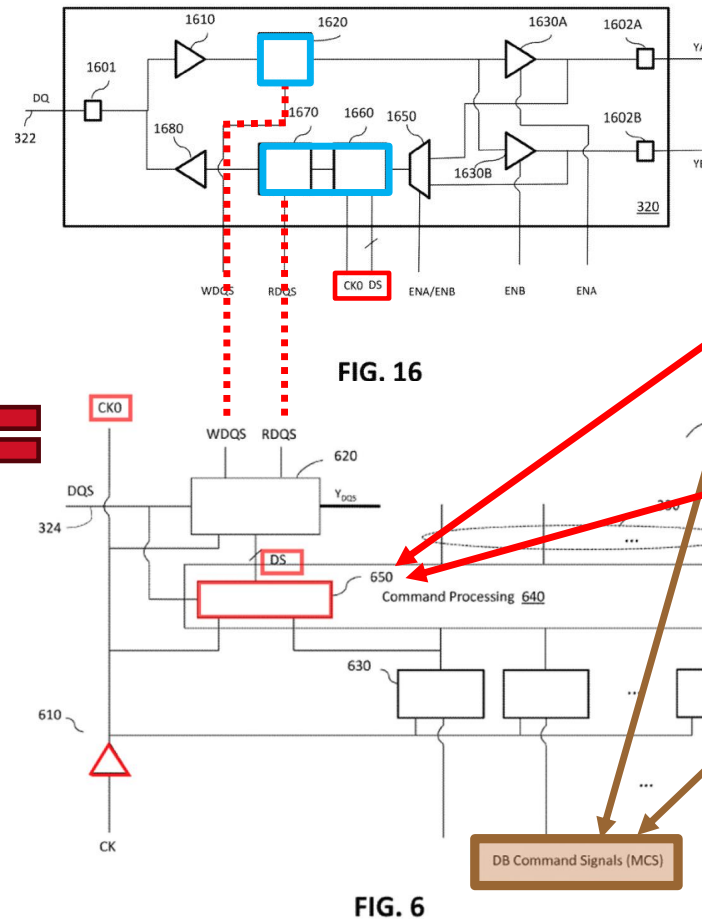
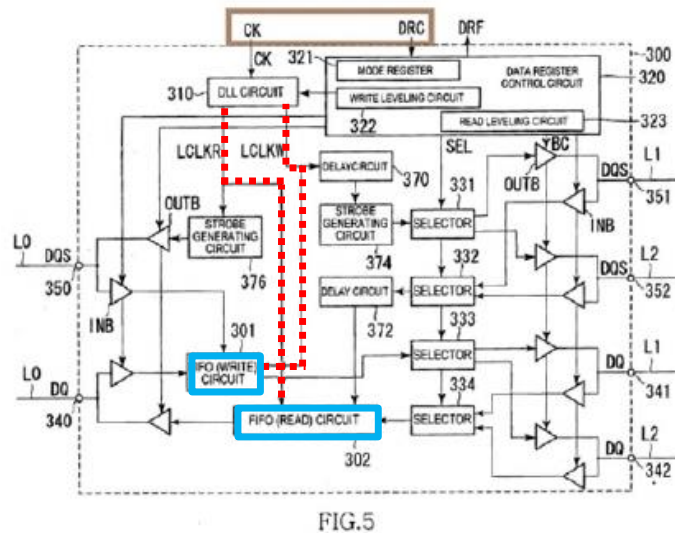


FIG.11

“Module control signals” (e.g., DRC) need not directly control the “*delay circuit*,” as shown by the ‘608 Patent itself (e.g., DB Command Signals)



Q. Turning back to Figure 6 of the '608 patent, the command processing circuit 640 inside of the data buffer will receive the DB command signals that were sent by the controller 116 that was in the middle of the memory module; is that fair?

A. I believe that that's fair, yes.

Q. And then as explained at column 12, starting around line 31, the command processing circuit 640 inside of the data buffer includes a delay control circuit 650 which determines the amount sent via delay signal DS; is that fair?

A. So it does say:

The strobe routing circuit 620 also buffers strobe signals received from either the MCH 101 or the memory devices 112, and output either a write strobe WDQS or read strobe RDQS to the DQ routing circuits 320. In one embodiment, the ID control circuit 310 further includes a delay control circuit 650 that receives one of the module control signals and either a data signal for a strobe signal and determines a delay amount to be used by the DQ routing circuit 320 and the strobe routing circuit 620. The delay amount is provided to the DQ routing circuit 320 and the strobe routing circuit in a delay signal DS.

EX1001 at 12:27-37

Q. So the delay control circuit 650, which is inside the data buffer which is also sometimes referred to as the isolation device, provides the determined delay amount via the delay signal DS to both the DQ and DQS routing circuits 320 and 620 that are illustrated in more detail in Figures 15 and 16; is that fair?

A. Yes, I think that's fair.

EX1074 at 168:23-169:9, 169:25-170:7

"Module control signals" (e.g., DRC) need not directly control the "delay circuit," as shown by the '608 Patent itself (e.g., DB Command Signals)

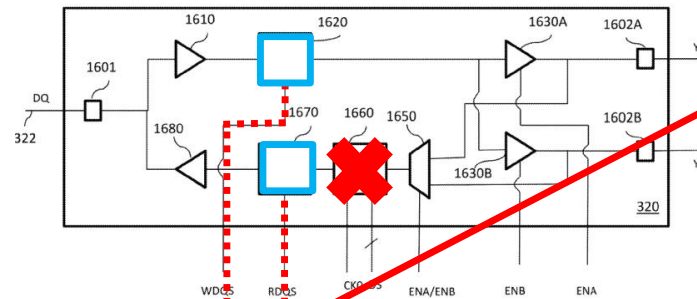
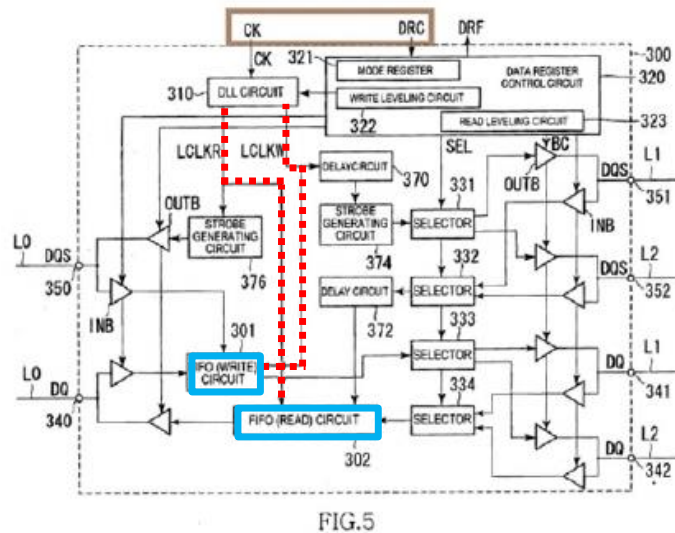


FIG. 16

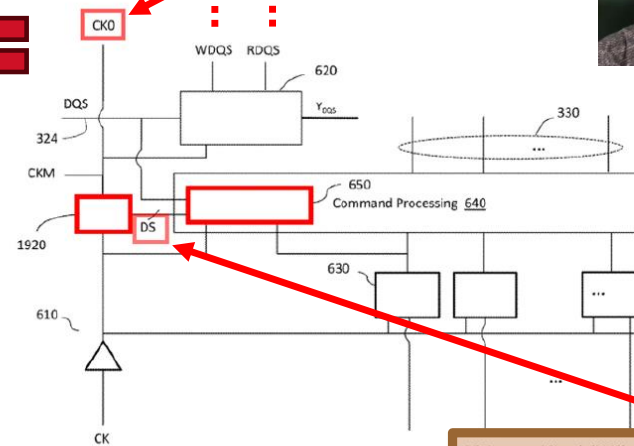


FIG. 19

Q. So in this embodiment of the data buffer shown in Figure 19, the delay circuits 1560 and 1660 in Figures 15 and 16 are not needed because, instead, the clock signal CK0 is delayed by the proper amount; is that fair?

A. I don't see a problem with that as I sit here, no.

Q. And so, for example, if you look back at Exhibit 1080 which has the annotations of Figures 15 and 16, it's possible for a delayed clock signal CK0 to be used in both Figures 15 and 16 to delay both the DQ data signal and the DQS strobe signal by the proper amount; is that fair?

A. Give me a moment. Yes, it's possible to use 15 -- figure -- the circuitry in Figure 15 and 16 without 1560 and 1660 according to the disclosure, that embodiment that we were just looking at.

EX1074 at 171:4-173:3

In certain embodiments, especially the embodiments shown in FIG. 2D, the delay circuits 1560 and 1660 shown in FIGS. 15 and 16 are not needed to provide alignment of the read data. As shown in FIG. 19, the ID control circuit 310 includes a clock regeneration circuit 1920 that regenerates the clock signal CK received from the control circuit 116, according to the delay signal DS. The regenerated clock

EX1001 at 18:65-19:4

NETLIST IS ESTOPPED BY IPR2022-00236 WITH RESPECT TO
DELAYING DATA SIGNALS ON THE "DATA PATH" IN
RESPONSE TO "MODULE CONTROL SIGNALS"

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 44

IPR2022-00236 [EX1066] and -00237 relied on equivalent prior art: Osanai [EX2004] = Hiraishi [EX1005]

1. **The Primary Reference (Hiraishi) Is the Same as the Primary Reference (Osanai) the Board Considered in Micron -0237**

Osanai from Micron -0237 not only “is related to Hiraishi,” (Pet., 113), it is the same as Hiraishi in all material respects, as Samsung’s counsel admitted during oral argument in IPR2022-00711 against the related ’506 patent (“the ’506 IPR”).

Paper 6 (POPR) at 5

IPR2022-00236 determined that Hiraishi's data buffer delays data signals on the "data path" (e.g., L0 to L1/L2)

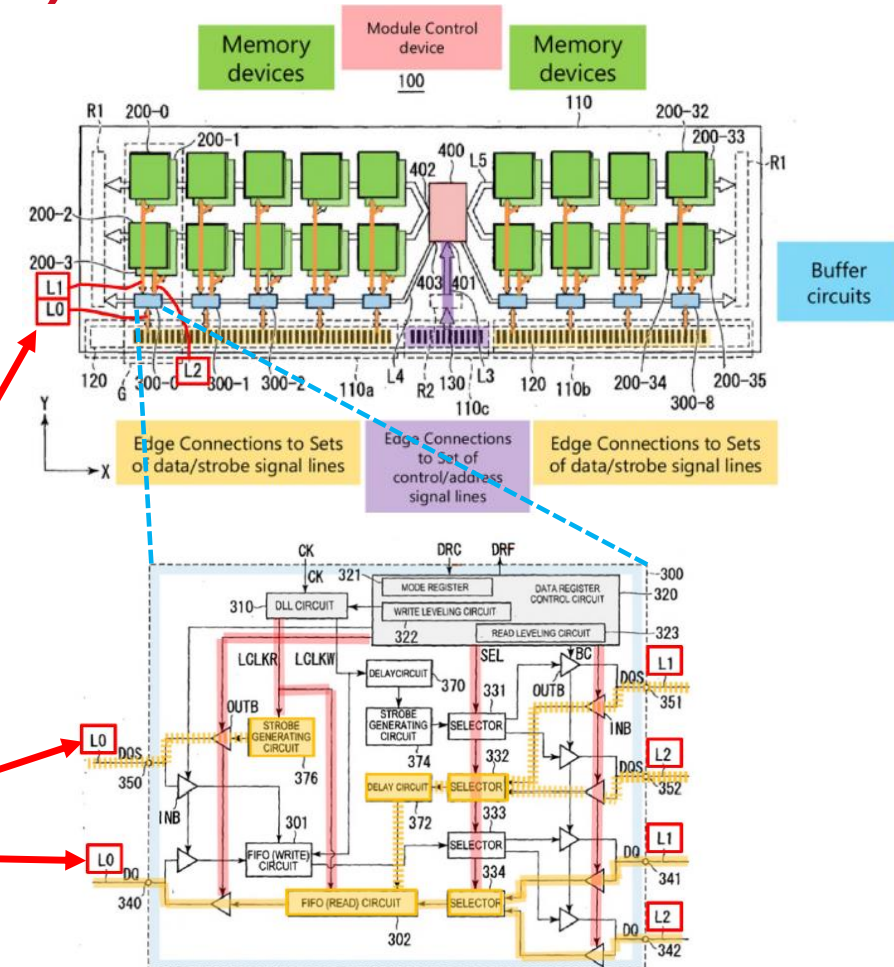


Ex. 5; Ex. 1003 ¶ 111). In its contentions for limitation 1[j] Petitioner explains that the read and write leveling circuits of [Hiraishi] make timing adjustments so that signals between the memory chips and the data register buffer are sent at the appropriate time. Pet. 34 (citing Ex. 1005 ¶¶ 110, 146).

signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of [Hiraishi] are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.

For limitation 1[h] we explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. See § II.D.3.c; Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110; Figs. 1, 5, 7). These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300. Pet. 30–31. Furthermore, we

EX1066 (IPR2022-00236, Paper 34) at 35-36
(with [Hiraishi] inserted in place of Osanai)



EX1005 (Hiraishi), Figs. 1 & 5 (annotated for read direction)

IPR2022-00236 determined that Hiraishi's data buffer delays data signals "in response to ... module control signals" (e.g., DRC)

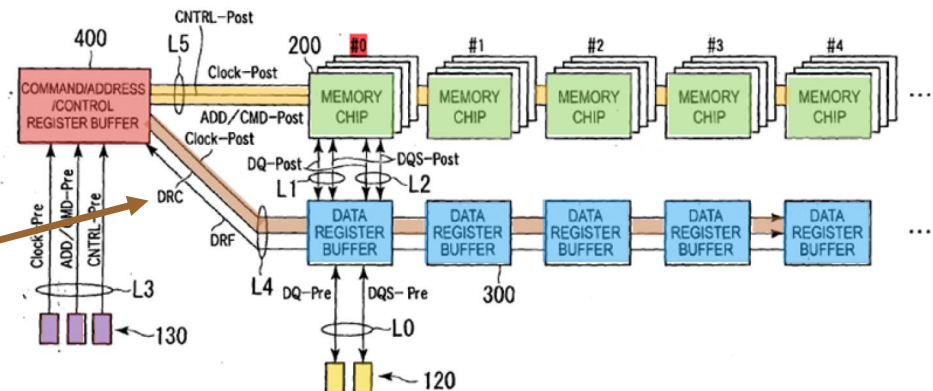


10. Analysis of Claim 21

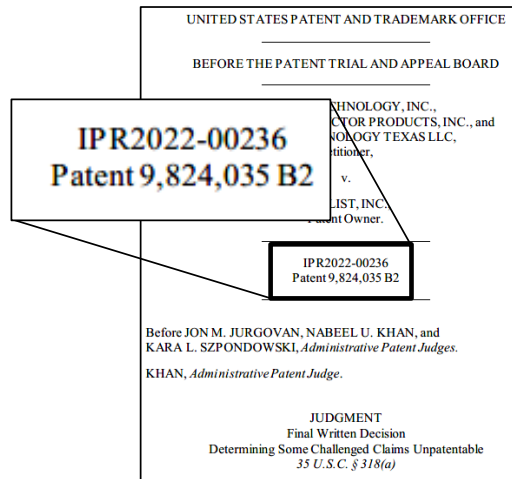
Claim 21 depends from claim 1 and recites "wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device." Ex. 1001, 22:10–13. Petitioner contends that the command/address/control register buffer 400 sends clock signals or alternatively DRC signals ("one or more signals") to the data register buffer 300 ("buffer circuit"). Pet. 47 (citing Ex. 1005, Figs. 5, 7, 14A; Ex. 1003 ¶ 147). Petitioner contends that [Hiraishi]'s read and write leveling circuitry use both these signals to adjust the read and write timing. *Id.* Patent Owner does not separately dispute Petitioner's contentions for claim 21. See PO Resp. 49.

Having reviewed Petitioner's contentions and the underlying evidence we are persuaded that [Hiraishi] teaches the limitations of claim 21 for the reasons summarized above. Dr. Alpert provides credible testimony

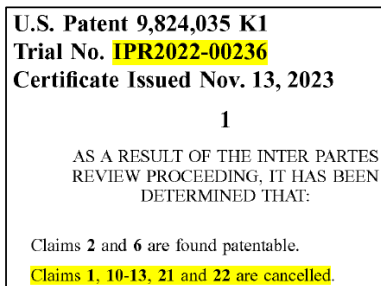
EX1066 (IPR2022-00236, Paper 34) at 52
(with [Hiraishi] inserted in place of Osana)



IPR2022-00236 [EX1066], which was not appealed, is binding against Netlist



EX1066: IPR2022-00236,
Final Written Decision



EX1088, 2

The Federal Circuit has found ***collateral estoppel to be proper in the context of ... non-appealed cases*** . . .

. . . . [A] party may be bound not simply by the ultimate conclusion (e.g., unpatentability of a claim), but by ***any subsidiary factual determinations*** that were actually litigated and essential to the judgment.

Mobile Tech, Inc. v. InVue Security Prods. Inc., IPR2018-00481, Paper 29, at 11, 18 (PTAB July 16, 2019) (emphasis added)



It is well established that ***patent claims need not be identical*** for collateral estoppel to apply....[C]ollateral estoppel may apply even if the patent claims “use slightly different language to describe substantially the same invention,” ***so long as “the differences between the unadjudicated patent claims and adjudicated patent claims do not materially alter the question of invalidity.”*** Whether the differences between the patent claims materially alter the question of patentability is a ***legal conclusion*** based on underlying facts.

Google LLC v. Hammond Dev. Int'l, Inc., 54 F.4th 1377, 1381 (Fed. Cir. 2022) (citations omitted)



The '608 claims are not patentably distinct from the '035 claims

Claim 1 is rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of instant Application, respectively contains every element of claims 1-22 of copending Application No. 15/426,064, now US Patent No. 9,824,035; claims 1-20 of copending Application No. 14/846,993, now US Patent No. 9,563,587; and claims 1-20 of copending Application No. 13/952,599, now US Patent No. 9,128,632, as listed below, and as such anticipate the claims of the copending application:

EX1002 ('608 file history) at 84-85

TERMINAL DISCLAIMER TO OBIVATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Doc Code: DIST.E.FILE Document Description: Electronic Terminal Disclaimer - Filed	PTO/SB/28 U.S. Patent and Trademark Office Department of Commerce
Electronic Petition Request	TERMINAL DISCLAIMER TO OBIVATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT
Application Number	15820076
Filing Date	21-Nov-2017
First Named Inventor	Hyun Lee
Attorney Docket Number	129980-5049US
Title of Invention	MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action	
☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.	
Owner	Percent Interest
NETLIST, INC.	100%
The owner(s) with percent interest listed above in the instant application hereby disclaims, except as provided below, the terminal part of the statutory term of any patent granted on the instant application which would extend beyond the expiration date of the full statutory term of prior patent number(s)	
9128632 9563587 9824035	

EX1002 ('608 file history) at 102

IPR2022-00236 determined Hiraishi's L0 to L1/L2 is a “data path” for data and strobe signals

IPR2022-00236, FWD, pp. 35-36 [EX1066]	'035 Patent Claim 1[j]	'608 Patent Claim 1[e]-[f]
For limitation 1[h] we explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. See § II.D.3.c; Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110, Figs. 1, 5, 7). These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300. Pet. 30–31. Furthermore, we ... signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of Osanai are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.	1[j]: wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information	1[e]: ... the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals ... 1[f] wherein the data path corresponding to the each data signal line includes ... a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals

IPR2022-00236 determined Hiraishi's data buffer controls the timing of (i.e., "delay[s]") the DQ data and DQS strobe signals

IPR2022-00236, FWD, p. 26 [EX1066]	'035 Patent Claim 1[j]	'608 Patent Claim 1[e]-[f]
timing information.” Dr. Alpert provides credible testimony that Osanai discloses both <u>read and write leveling</u> techniques that make timing adjustments by using the module clock signal so that signals between the memory chips 200 and the data register buffer 300 are sent at the appropriate time. Ex. 1003 ¶ 115 (citing Ex. 1005 ¶¶ 96, 110, 146–164). Dr. Alpert further testifies that a timing adjustment, such as a time <u>delay</u> based on the module clock signal, is used to create <u>DQ-Post</u> and <u>DQS-Post</u> and adjust write timing or read timing. <i>Id.</i> ¶ 117 (citing Ex. 1005 ¶¶ 110, 149–157).	1[j]: wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information	1[e]: ... the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals ... 1[f] wherein the data path corresponding to the each data signal line includes ... a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals

IPR2022-00236 determined Hiraishi controls the timing (i.e., delays) data and strobe signals on the “data path”

IPR2022-00236, FWD, pp. 35-36 [EX1066]	'035 Patent Claim 1[j]	'608 Patent Claim 1[e]-[f]
Moreover, we disagree with Patent Owner’s argument that Osanai’s read leveling process, which delays the internal signals that turn on Osanai’s input buffers INB, does not control the timing of the data and strobe signals. Osanai explains that in <u>read leveling</u>, the timing of read data output from the memory chips and the input timing of the read command is measured for each memory chip and “used in an adjustment of an activation timing of the input buffer circuit INB and the like.” Ex. 1005 ¶ 157. But, as Petitioner points out, Osanai does so “in consideration of a propagation time of a signal.” Ex. 1005 ¶ 146. Petitioner further indicates that Dr. Przbylski testified that the input buffers (INB) act as a gate allowing data and strobe signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of Osanai are sufficient to teach <u>controlling the timing of the data and strobe signals on the data paths on which those signals travel</u>.	1[j]: wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information	1[e]: ... the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals ... 1[f] wherein the data path corresponding to the each data signal line includes ... a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals

IPR2022-00236 rejected Netlist’s position (left), and agreed with Samsung’s position (right) that Hiraishi’s data buffer delays data signals “in response to ... module control signals” (e.g., DRC)

Netlist’s POR, p. 29	Samsung’s Reply, pp. 16-17	IPR2022-00236, FWD, p. 52 [EX1066]
“One component of Petitioner’s alleged “delay circuit” is Hiraishi’s delay circuit 370 that allegedly delays the LCLKW local clock signal. Pet., 39, 47. This does not satisfy Element 1[f] because (1) any delay the delay circuit 370 imparts is not ‘in response to at least one of the module control signals.’”	“[T]he Board has already rejected this argument, correctly concluding that the “DRC” signal identified in the Petition (shown below in a brown box) causes Hiraishi’s data buffer to perform read and write leveling, which determines the amount of delay that is applied to the “data and strobe signals on the data paths.” EX1066, 35-36, 52; Pet. 44-47 (“write leveling...performed during initialization in response to module control signals (e.g., DRC conveying ‘mode switching’ or ‘mode register set’ commands)”), 48-51 (similar for read).	“Claim 21 depends from claim 1 and recites “wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device.” Ex. 1001, 22:10–13. Petitioner contends that the command/address/control register buffer 400 sends clock signals or alternatively <u>DRC signals</u> (‘one or more signals’) to the data register buffer 300 (‘buffer circuit’). ... Having reviewed Petitioner’s contentions and the underlying evidence we are persuaded that [Hiraishi] teaches the limitations of claim 21 for the reasons summarized above.”

IN ANY EVENT, NETLIST'S CONSTRUCTION IS WRONG:
"DATA PATH" INCLUDES BOTH DATA AND STROBE SIGNALS

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 54

The Institution Decision correctly found that Ground 1 (Hiraishi + Butt) teaches a “delay circuit” in the “data path”



vii. Limitation 1[f]

Petitioner asserts that Hiraishi discloses that the data path corresponding to each data signal line includes at least one tristate buffer, i.e. “output buffers OUTB and input buffers INB,” controlled by the command processing circuit, and a delay circuit, i.e., “DLL Circuit 310, FIFO (Write) Circuit 301, FIFO (Read) Circuit 302, Delay Circuits 370 and 372, and Strobe Generating Circuits 374 and 376,” configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals. Pet. 39. Although Petitioner asserts that it is ambiguous as to whether the claim 1 language “in response to at least one of the module control signals” modifies the term “to delay” or the term “determined,” Petitioner contends that the combination of Hiraishi and Butt discloses either interpretation. *Id.* at 43 (citing Ex. 1003 ¶ 155).

Petitioner also argues that Hiraishi discloses, with respect to the flow chart shown in Figure 13, a step “S4 Read/Write leveling to determine the delay through the data path.” Pet. 42 (citing Ex. 1003 ¶ 152; Ex. 1005, Figs. 5, 13). Petitioner asserts that in a write leveling operation that is

...

We have reviewed the evidence and argument, which includes un rebutted expert testimony, and on this record, we preliminarily determine that Petitioner has presented sufficient evidence that the combination of Hiraishi and Butt teaches limitation 1[f].

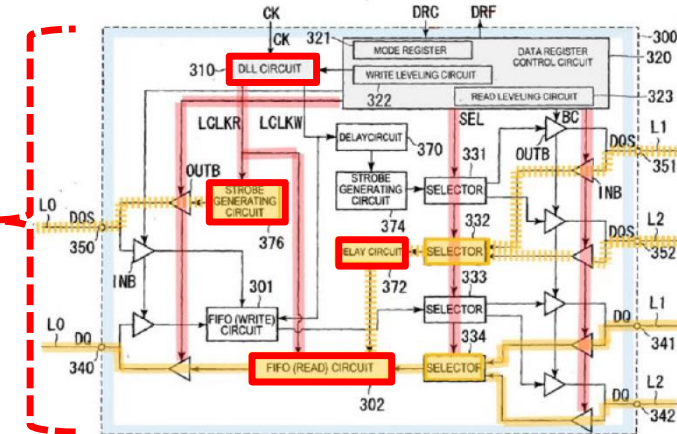


FIG. 5

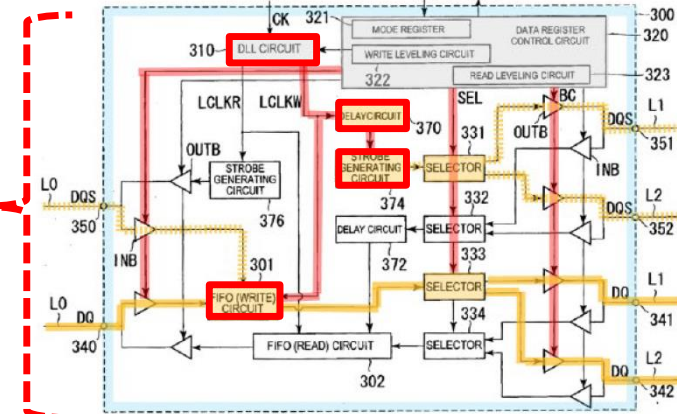


FIG. 5

IPR2022-00236 determined that "data path" includes DQS strobe signals

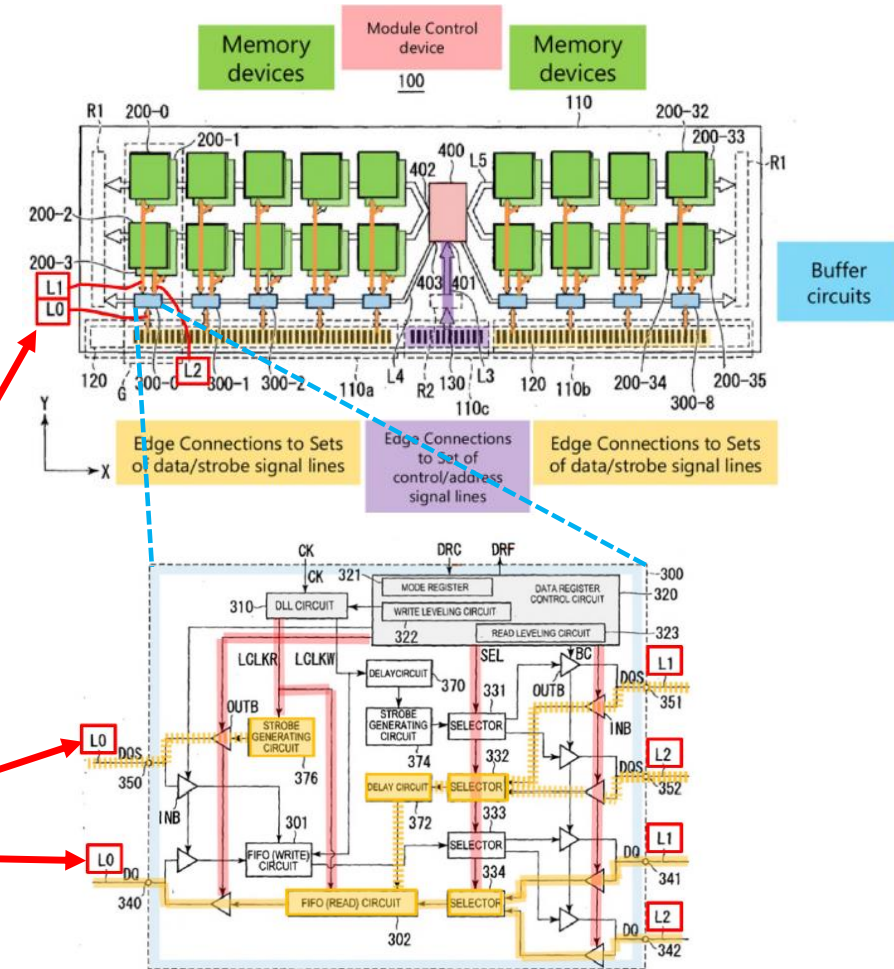


g. 5; Ex. 1003 ¶ 111). In its contentions for limitation 1[j] Petitioner explains that the read and write leveling circuits of [Hiraishi] make timing adjustments so that signals between the memory chips and the data register buffer are sent at the appropriate time. Pet. 34 (citing Ex. 1005 ¶¶ 110, 146).

signals to either pass through or not pass through. Ex. 1022, 70:10–22. We determine that these disclosures of [Hiraishi] are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.

For limitation 1[h] we explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. See § II.D.3.c; Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110; Figs. 1, 5, 7). These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300. Pet. 30–31. Furthermore, we

EX1066 (IPR2022-00236, Paper 34) at 35–36
(with [Hiraishi] inserted in place of Osanai)

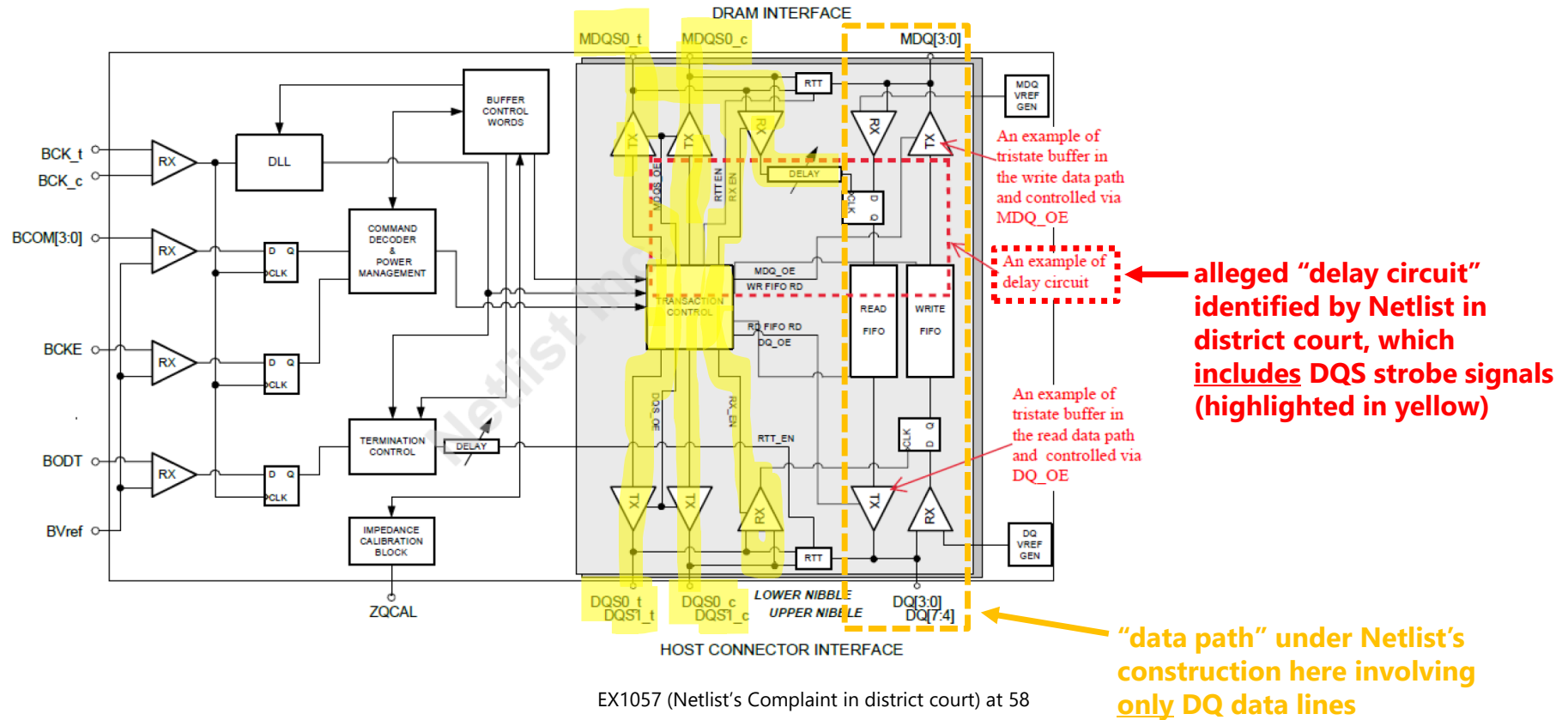


EX1005 (Hiraishi), Figs. 1 & 5 (annotated for read direction)

IPR2022-00236 rejected Netlist's position (left), and agreed with Samsung's position (right) that "*data path*" includes DQS strobe signals

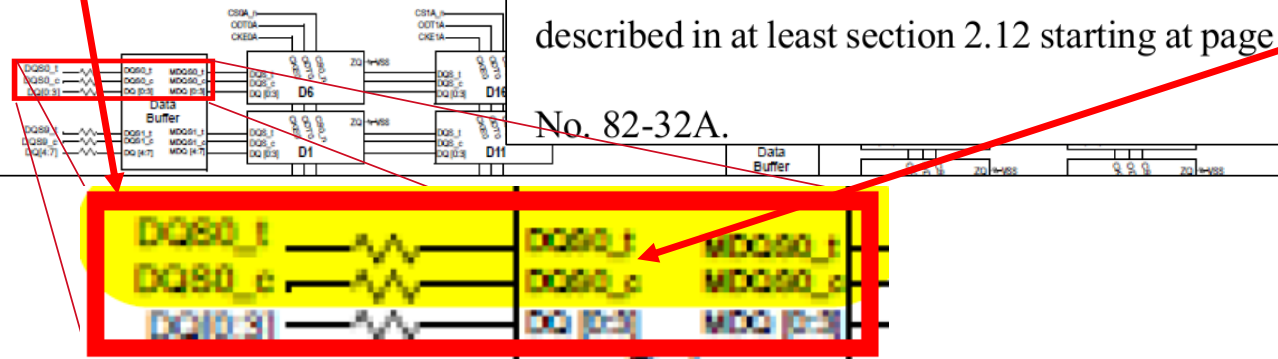
Netlist's POR, pp. 23-24	Samsung's Reply, p. 1	IPR2022-00236, FWD, pp. 35-36 [EX1066]
"Thus, the specification makes clear that strobe signal lines form a strobe path and data signal lines form a data path, as is also reflect in the claim language. As such, each recited 'data path' corresponds to a data signal line carrying data signals, not to a strobe signal lines carrying strobe signals. EX2013, ¶¶70-78. Thus, any reliance by the Petitioner on a 'data path' comprising segments of Hiraishi's strobe signal line(s) fails as a matter of fact."	"Netlist's attempt to exclude 'strobe signal lines' from the claimed 'data path' (POR 1-4, 18-40) is precluded by the Board's recent Final Written Decision in IPR2022-00236 involving the '035 patent, EX1031; Pet. 6, which is the parent of the '608 Patent here and expressly claims strobe signals on the 'data paths':"	"We determine that these disclosures of [Hiraishi] are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel." "[W]e explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. ... These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300."

Netlist admitted in its Complaint for the '608 Patent that the “delay circuit” in the “data path” includes DQS strobe signals (contrary to its construction here where “data path” includes only the DQ data lines)



Netlist admitted in its Complaint for the '608 Patent that a "data path" includes DQS strobe signals (in addition to DQ data signals) corresponding to each data signal line

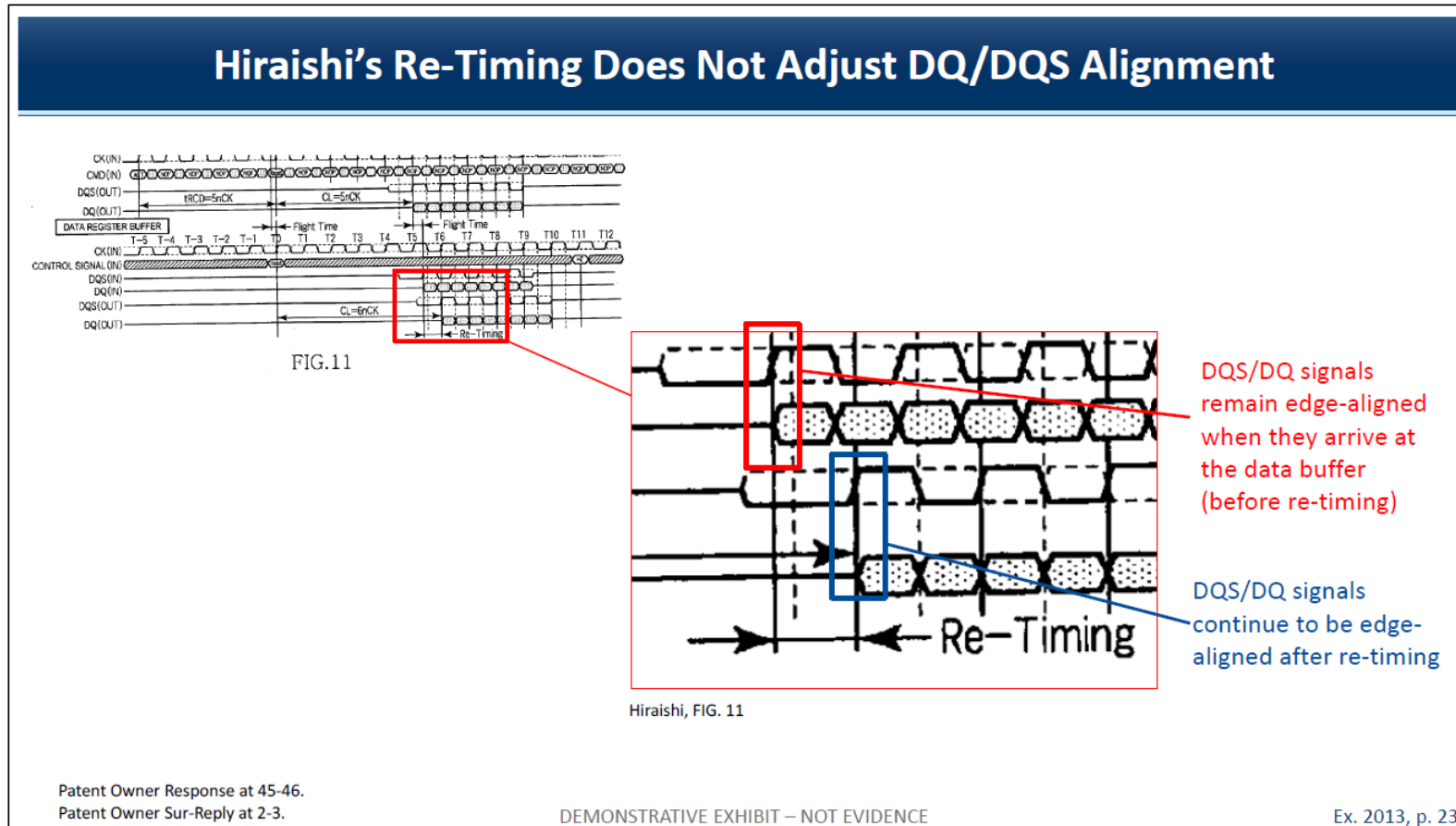
74. As shown above in the example block diagram of Fig. 15 at page 95 of JEDEC Standard No. 82-32A, the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit. As shown above and below, the data path corresponding to the each data signal line also includes a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.



75. Timing delays to be applied to data and data strobe signals are determined as described in at least section 2.12 starting at page 12 and in Table 16 at page 27 of JEDEC Standard No. 82-32A.

EX1057 (Netlist's Complaint in district court) at 59
(red box by Netlist)

DQS strobe signals must travel with DQ data signals to ensure accurate data transmission, as Netlist has admitted and Hiraishi and JEDEC both teach



EX1086 (Netlist's demonstratives for oral argument in the '506 IPR) at 23

Netlist's expert admitted that the JEDEC standard requires the DQS strobe signals to travel with the DQ data signals within a "very tight tolerance"

Q. Yes, there's the heading "Data Timing" and there's the first row. And if you look in the second column, the symbol is tDQSQ. And the permissible range -- the maximum range on the entire range for tDQSQ is 200 picoseconds, correct?

THE WITNESS: It says that there is a -- the options configurations listed here, there is a maximum of 200 picoseconds.

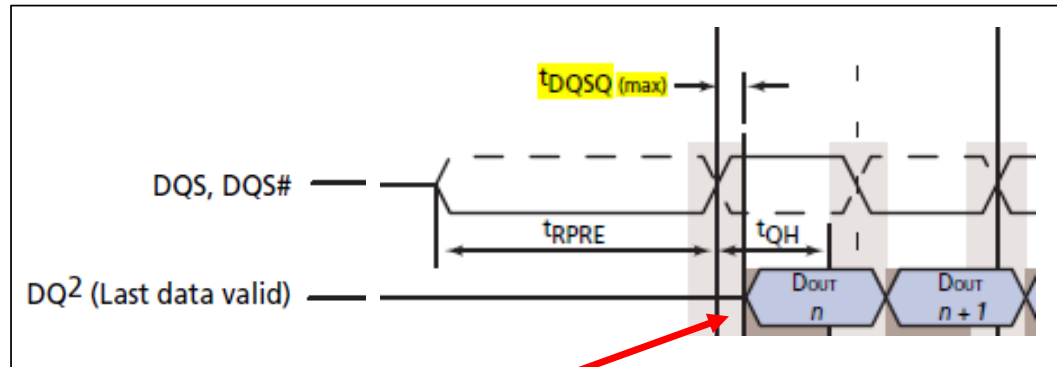
Q. So it would be fair to say that the JEDEC standard for DDR3 memory devices does not permit a large amount of skew between the DQS strobe signal and DQ data signal.

To the contrary, it could fairly be characterized as requiring a very tight tolerance between the DQS strobe signal and the DQ data signal, correct?

THE WITNESS: Yes, it requires a very tight tolerance.

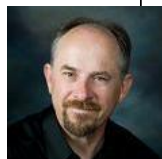
EX1074 at 137:13-22, 139:13-24 (objections omitted)

tDQSQ defines the skew between DQS,DQS# to Data



EX1020 (JEDEC DDR3 standard) at 59

Both experts agreed DQS strobe signals are “essential” for proper transmission of DQ data signals



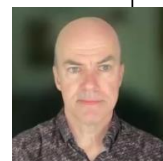
Q. And you said that a person -- I'm sorry. You said that a person skilled in the art would understand that a strobe signal is part of the data path. Why specifically would a strobe signal be part of a data path

THE WITNESS: Well, because it travels -- it travels with the data. It helps to define when the data is valid. It is -- it is specific to a particular data element, and, therefore, is not a CLK, as at least I define a CLK.

Q. Right. But before the double data rate architecture, strobe signals were not used to send data. Is that fair to say?

A. That's my understanding. They were introduced with double data rate RAMs in order to provide the speeds necessary to allow them to operate. As I said, they -- they're essential to allow the data to transfer, and they are associated with individual data lines, so you can't operate a double data rate RAM without them.

EX2012 at 51:22-52:7; 55:2-10 (objections omitted)



Q. And the phrase that Professor Jacob uses in that passage is that a dual-edged signaling scheme needs an additional mechanism beyond the clock, and that additional mechanism for DDR memory devices is the DQS strobe signal; is that fair?

A. Yes. And I think that's accurate for the JEDEC DDR devices for simply -- which is, I think,

Q. In section 4.14.2.2, on page 68 of Exhibit 1020, the JEDEC standard for DDR3 memory devices warns that if the data to strobe timing requirements are violated for any of the strobe edges associated with a write command, then the wrong data might be written to memory, correct?

THE WITNESS: Yes, that's a reasonable characterization of what it says in that passage.

EX1074 at 99:19-25; 141:11-141:21 (objections omitted)

The '035 (left) and '506 (right) Patents, in the '608 Patent family, also confirm the "data path" includes strobe signals

(12) United States Patent Lee et al.	(10) Patent No.: US 9,824,035 B2 (45) Date of Patent: *Nov. 21, 2017
(54) MEMORY MODULE WITH TIMING-CONTROLLED DATA PATHS IN DISTRIBUTED DATA BUFFERS	3/0659 (2013.01); G06F 3/0683 (2013.01); G06F 13/1642 (2013.01); G11C 8/18 (2013.01)
(71) Applicant: Netlist, Inc. , Irvine, CA (US)	(58) Field of Classification Search None See application file for complete search history.
(72) Inventors: Hyun Lee , Ladera Ranch, CA (US); Jayesh R. Bhakta , Cerritos, CA (US)	(56) References Cited

(12) United States Patent Lee et al.	(10) Patent No.: US 10,860,506 B2 (45) Date of Patent: *Dec. 8, 2020
(54) MEMORY MODULE WITH TIMING-CONTROLLED DATA BUFFERING	(56) References Cited U.S. PATENT DOCUMENTS 4,368,515 A 1/1983 Nielsen 4,392,212 A 7/1983 Miyasaka et al. (Continued)
(71) Applicant: Netlist, Inc. , Irvine, CA (US)	
(72) Inventors: Hyun Lee , Ladera Ranch, CA (US); Jayesh R. Bhakta , Cerritos, CA (US)	

EX1046 ('506 patent)

the respective data and strobe signals on the data paths

Claim [1,j] in '035 patent, EX1031, 19:44

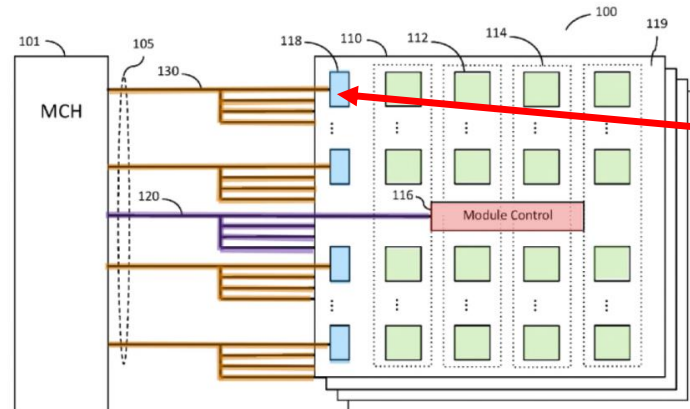


FIG. 1

34. For the isolation devices 118 to properly time such transmissions, the buffer circuits 118 include a command processing circuit 640 that provides decoded and/or processed module control signals to routing circuits. *Id.*, 12:14-19. Buffer circuits 118 also include a delay control circuit 650 that is configured to delay a strobe signal through the data path, in response to the module control signals, by a predetermined amount determined based on signals received by the buffer circuit during one or more previous memory operations. *See id.*, cl. 1 (19:45:49, 19:53-55), 10:11-21, 11:8-13, 12:30-37, 15:23-26, 16:10-12.

EX1076 (Patent Owner's expert declaration for the '506 IPR) at ¶34

The claims and specification distinguish the “**data path**” (through the buffer) from the “**data signal lines**” outside the buffer, and just require a broad “correspond[ence]” between them, consistent with the understanding that strobe and data signals travel together in the “**data path**”

“wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, ...”

EX1001 at 19:36-45 (Claim [1.e])

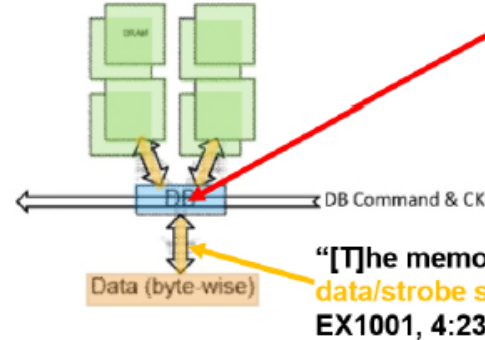
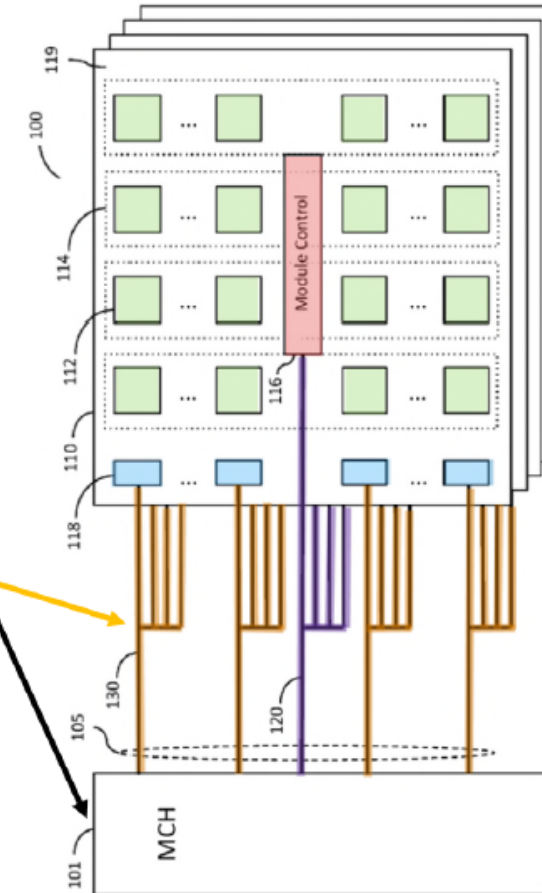


FIG. 2C

“[E]ach buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller.” EX1001, 3:57-:60.

“[T]he memory bus includes...system data/strobe signal lines 130.” EX1001, 4:23-:25.



The claims and specification are consistent with the dictionary definition for “path”: course or direction...a...thing is moving

Google path definition

path : Overview Similar and opposite words Usage examples Pronunciation

Dictionary

Definitions from Oxford Languages · Learn more

path
/paTH/

noun

noun: path; plural noun: paths

a way or track laid down for walking or made by continual treading.
“the path continues alongside the river for half a mile”

Similar: footpath pathway track jogging track trail trackway ride

the course or direction in which a person or thing is moving.
the missile traced a fiery path in the sky

Similar: route way course approach road direction bearing line

a course of action or conduct

the course or direction in which a person or thing is moving

path

DUTCH
pad → path

GERMAN
Pfad → path

Old English *paeth*, of West Germanic origin; related to Dutch *pad*, German *Pfad*, of unknown ultimate origin.

Samsung Ex. 1087, p. 1

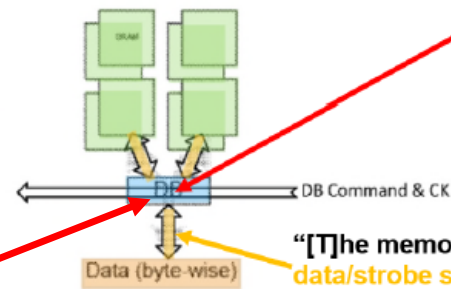


FIG. 2C

“[E]ach **buffer circuit** associated with a respective group of **memory devices** is in the **data paths** between the respective group of **memory devices** and the memory controller.”
EX1001, 3:57-:60.

“[T]he memory bus includes...system **data/strobe signal lines 130**.”
EX1001, 4:23-:25.

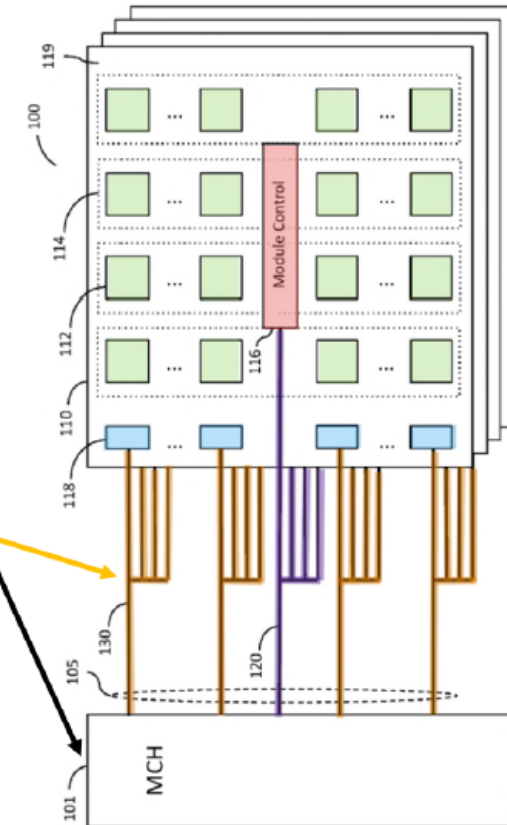


FIG. 1

Claim 10 confirms a “data path” can include a “strobe signal,” consistent with the understanding that strobe and data signals for read/write “memory operation[s]” travel together in the “data path”

1. ... a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines, wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines ...

2. The memory module of claim 1 ... wherein the signal through the data path is a signal associated with the second memory operation.

10. The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation ...

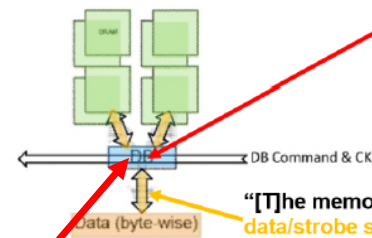


FIG. 2C

“[E]ach buffer circuit associated with a respective group of memory devices is in the data paths between the respective group of memory devices and the memory controller.”
EX1001, 3:57-:60.

“[T]he memory bus includes...system data/strobe signal lines 130.”
EX1001, 4:23-:25.

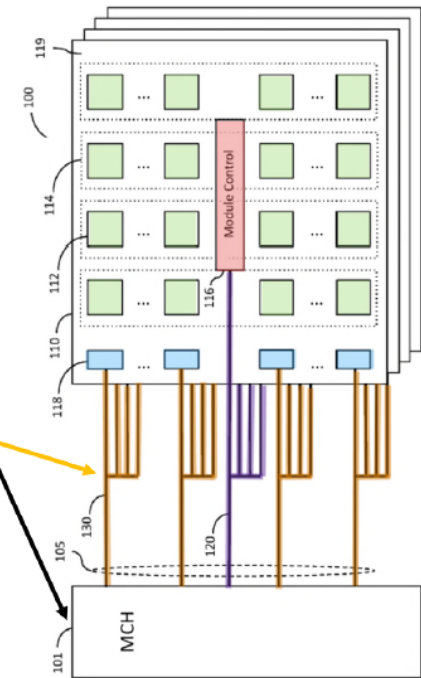


FIG. 1

EX1001

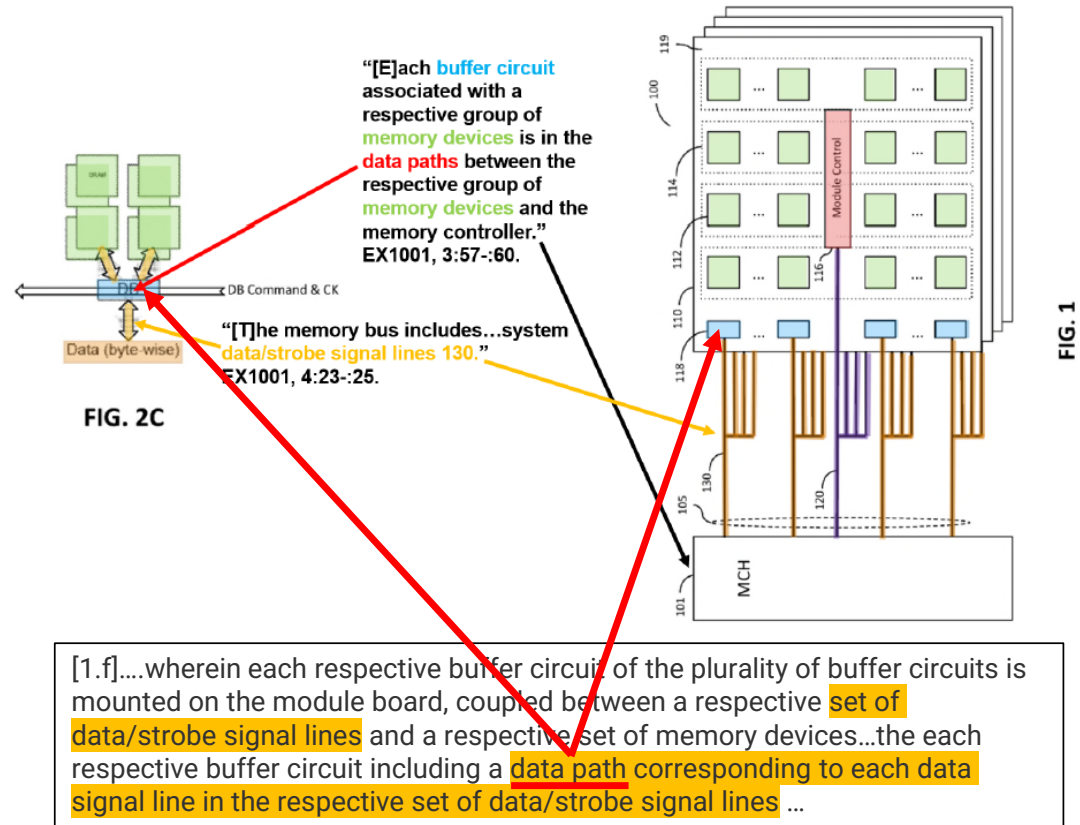
The [first/second] [read/write] paths for data and strobe signals are *subparts of the broader “data path”*

FIG. 15 illustrates a DQS routing circuit 620 according to an embodiment. As shown, the DQS routing circuit 620 includes a first DQS pin 1501 that is coupled to a corresponding DQS signal line 324, a second DQS pin 1502A that is coupled to a corresponding module DQS line YA_{DQS} , a third DQS pin 1502B that is coupled to a corresponding module DQS line YB_{DQS} . The DQS routing circuit 620 further includes a first write strobe path coupled between the first DQS pin 1501 and the second DQS pin 1502A and a second write strobe path coupled between the first DQS pin 1501 and the third DQS pin 1502B. The first write strobe path includes a write strobe buffer 1510 that buffers a write strobe, a write strobe receiver 1520 that samples the write strobe according to the buffered module signal CK0. The sampled write strobe is provided to the DQ routing circuits 320 as the write strobe WDQS. The first write strobe path further includes a first write strobe transmitter 1530A that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YA_{DQS} . The second write strobe path includes the write strobe buffer 1510, the write strobe receiver 1520, and a second write strobe transmitter 1530B that transmits the write strobe to one or more memory devices 112 coupled to the module strobe line YB_{DQS} . The first and second write strobe transmitters, 1530A and 1530B, are controlled by two enable signals, ENA and ENB, respectively, such that the first write strobe path and the second write strobe path can be selectively enabled/disabled by the enable signals, ENA and ENB.

EX1001 at 16:47-17:7

FIG. 16 illustrates a DQ routing circuit 320 according to an embodiment. As shown, the DQ routing circuit 320 includes a first DQ pin 1601 that is coupled to a corresponding DQ signal line 130, a second DQ pin 1602A that is coupled to a corresponding module DQ line YA_{DQ} , a third DQ pin 1602B that is coupled to a corresponding module DQ line YB_{DQ} . The DQ routing circuit 320 further includes a first write data path coupled between the first DQ pin 1601 and the second DQ pin 1602A and a second write data path coupled between the first DQ pin 1601 and the third DQ pin 1602B. The first write data path includes a write data buffer 1610, a write data receiver 1620 that samples write data according to the write strobe WDQS from the DQS routing circuit 620, and a first write data transmitter 1630A that transmits the write data to one or more memory devices 112 coupled to the module data line YA_{DQ} . The second write data path includes the write data buffer 1610, the write data receiver 1620, and a second write data transmitter 1630B that transmits the write data to one or more memory devices 112 coupled to the module data line YB_{DQ} . The first and second write data transmitters, 1630A and 1630B, are controlled by two enable signals, ENA and ENB, respectively. Thus, the first write data path and the second write data path can be selectively enabled/disabled by the enable signals, ENA and ENB.

EX1001 at 17:12-47



The "data path" is not limited to just Figure 16 (top)

Thus, the specification makes clear that strobe signal lines form a strobe path and data signal lines form a data path, as is also reflect in the claim language. As such, each recited "data path" corresponds to a data signal line carrying data signals, not to a strobe signal lines carrying strobe signals. EX2013, ¶¶70-78. Thus, any reliance by the Petitioner on a "data path" comprising segments of Hiraishi's strobe signal line(s) fails as a matter of fact.

Paper 20 (POR) at 23-24

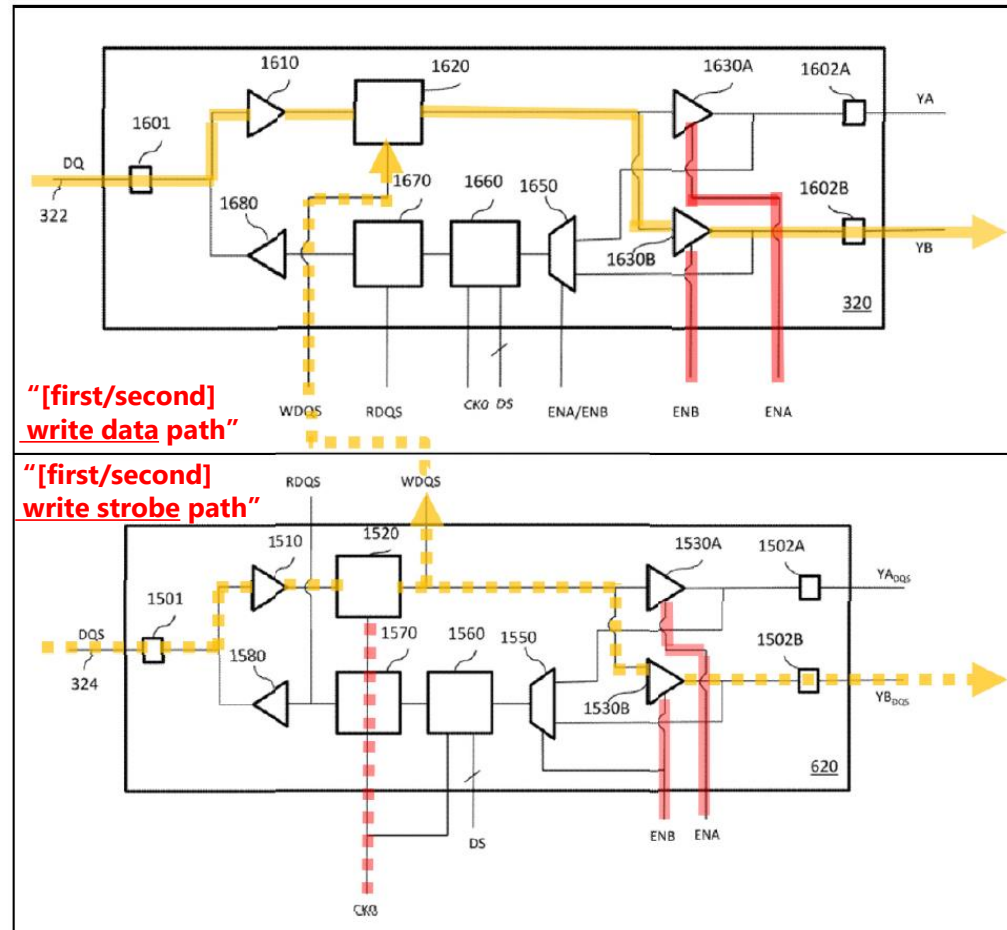


""[A]lthough the specification often describes very specific embodiments of the invention, **we have repeatedly warned against confining the claims to those embodiments.**""

Weber, Inc. v. Provisur Techs., Inc.,
492 F.4th 1059, 1070 (Fed. Cir. 2024)

BAKER BOTTS

Write direction — '608 Patent (EX1001) Figures 16 & 15



DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

Paper 23 (Reply) at 6-9

68

Samsung Electronics Co., Ltd.
Ex. 1059, p. 68

Butt also teaches the “*data path*” (114) includes both DQ data signals and the corresponding DQS strobe signal

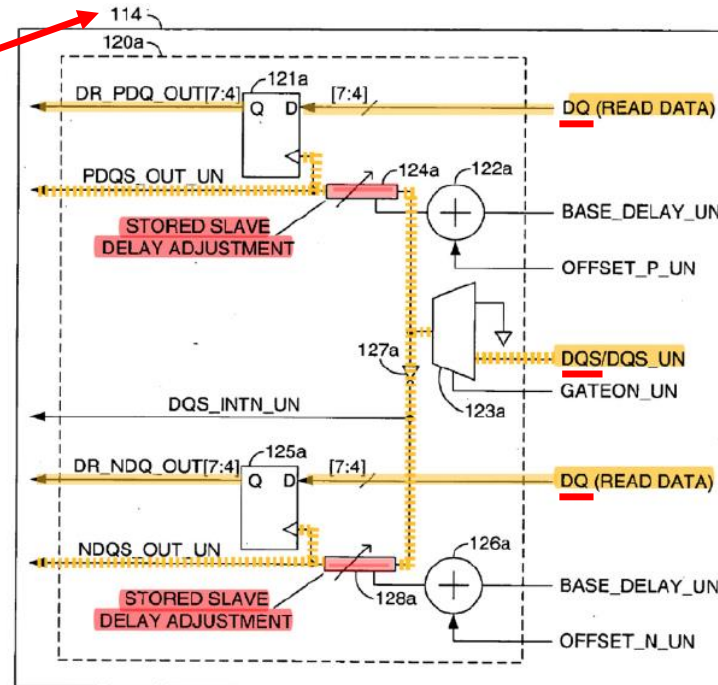


Q. And then looking back at Figure 2 of the Butt reference marked as Exhibit 1029, the number 8 to the right of the physical data paths 114 means that each of the data paths 114 receives 8 DQ data signals and 1 corresponding DQS data strobe signal; is that fair?

So I'm referring to sort of the slash 8 on the line going into the physical data path of 14 for the DQ line, and then the DQS line does not have the slash 8.

A. Yeah, understood. I was just trying to verify that. Yes, that appears to be accurate. There are eight DQ lines going into the PHY DP, the PHY DP, and what I think is an indication of one DQS line going in.

EX1074 at 180:25-181:14

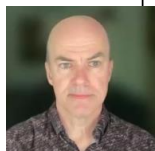


EX1029 at Fig. 3A (annotated)

[0017] Referring to FIG. 2, a more detailed block diagram of the circuit 104 is shown illustrating example read data logic and signal paths in which a preferred embodiment of the present invention may be implemented. In one example, the circuit 104 may comprise a number of asynchronous (ASYNC) first-in first-out (FIFO) buffers 112, FIFO synchronization logic 113, a number of physical read datapaths (DPs) 114, a master delay (MDELAY) logic 116, a control logic 117 and a programmable gating signal generator 118. Each of the physical read datapaths 114 may be configured to receive (i) a respective portion of the read data signals DQ from the DDR memory 106, (ii) a respective read data strobe signal or signals DQS associated with the respective portion of the received read data signals and (iii) a gating signal (e.g., GATEON) from the programmable gating signal generator 118. Each of the physical read datapaths 114 may communicate with a corresponding one of the asynchronous FIFOs 112 via a number of signals (e.g., DR_PDQ_OUT, DR_NDQ_OUT, PDQS_OUT, and NDQS_OUT). In one example, separate signals (e.g., PDQS_OUT_UN, NDQS_OUT_UN, PDQS_OUT_LN, and NDQS_OUT_LN) may be generated for each nibble of the DPs 114. In one example, the asynchronous FIFOs 112 may be configured to interface the physical read datapaths 114 with the memory controller 102.

EX1029 at ¶[0017]

Butt renders obvious a “delay circuit” (e.g., Async FIFO 112) in the “data path” (including both DQ data and DQS strobe signals)



Q. In Figure 2 of the Butt reference, and it's also discussed in paragraphs 18 and 19, each of data paths 114 outputs DQ data via the signals DR_PDQ_out and DR_NDQ_out, and also outputs the corresponding data strobe via the signals PDQS_out, and NDQS_out; is that fair?

A. Yes, I see that.

Q. In Figure 2 of the Butt reference, the data in strobe signals, after they come out of data path 114, go to the asynchronous FIFO 112 as shown in Figure 2 and discussed in paragraphs 17 and 18; is that fair?

A. When those signals emerge from element 114, they go to element 112, which is labeled ASYNC, A-S-Y-N-C, short for asynchronous, FIFO.

Q. And in particular, as explained by paragraph 19 of the Butt reference marked as Exhibit 1029, the read data DR_PDQ_out and DR_NDQ_out are written to the FIFOs 112 in response to the strobe signals PDQS_out and NDQS_out, correct?

A. Yes. It says that that read data is

EX1074 at 181:19-182:14

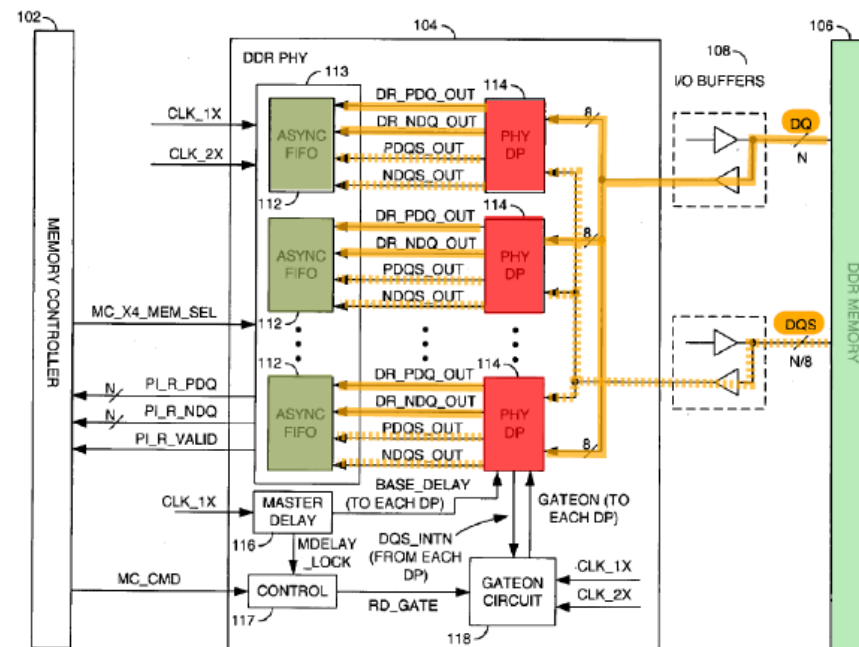


FIG. 2

[0018] In general, the signals DQ and DQS may be presented to the DDR PHY 104 on a number of buses. The signals DQ and DQS may be broken out to multiple instantiations of DP hardmacros. The DPs may be configured via internal settings to delay the read data strobe signals DQS based on one or more control signals (or values) from the MDELAY circuit 116. Each of the DPs 114 may be configured to present the DQ data to a respective asynchronous FIFO 112 via the signals DR_PDQ_OUT and DR_NDQ_OUT, after the data is sampled using the delayed read data strobe signals DQS.

EX1029 at ¶[0018]

Hiraishi similarly discloses “data lines” (L0, L1, and L2) that include both DQ data signals and the corresponding DQS strobe signal



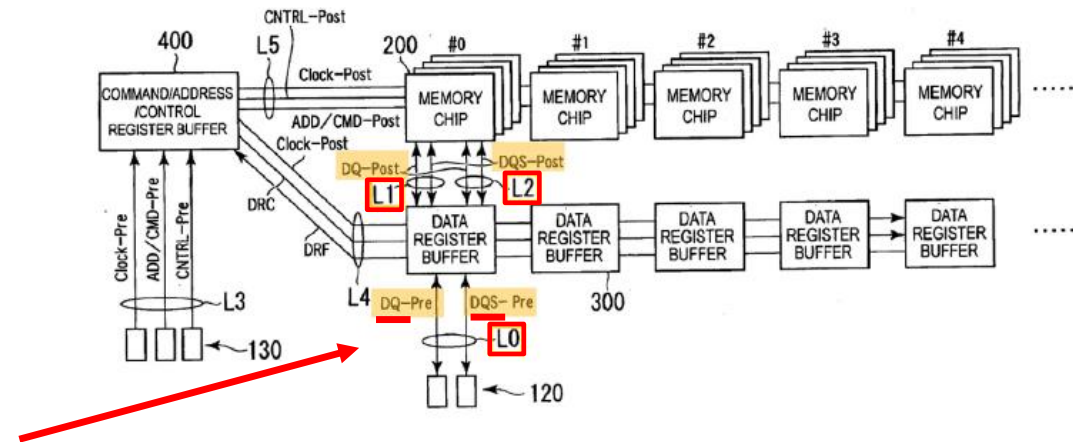
Q. And the data line L0 transfers both data signals DQ-Pre, and the corresponding strobe signals DQS-Pre, correct?

A. Yes, that is how Figure 7 is labeled.

Q. Each of data lines L1 and L2 transfer both data signals DQ-Post and corresponding strobe signals DQS-Post, correct?

A. Yes, that's accurate.

EX1074 at 225:18-21; 226:1-4



[0103] As shown in FIG. 7, in the present embodiment, the data register buffer 300 intervenes between the data connectors 120 and the memory chips 200. The data connectors 120 and the data register buffer 300 are connected to each other with the data line L0, and the data register buffer 300 and the memory chips 200 are connected to each other with the data line L1 or L2. In FIG. 7, a plurality of data transferred through the data line L0 is represented by data DQ-Pre, and a plurality of data transferred through the data lines L1 and L2 is represented by data DQ-Post. Similarly, a data strobe signal transferred through the data line L0 is represented by a data strobe signal DQS-Pre, and a data strobe signal transferred through the data line L1 or L2 is represented by a data strobe signal DQS-Post.

EX1005 at [0103] & Fig. 7

HIRAISHI'S DATA BUFFER DOES NOT SIMPLY ADD
ONE CLOCK CYCLE OF DELAY, OR ALWAYS OUTPUT
DATA AT THE NEXT CLOCK CYCLE (e.g., T6)

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 72

Hiraishi's data buffer determines a variable amount of delay to address different vertical "flight time" delays caused by the different lengths of data/strobe lines L1 and L2

Q. And so the flight time delay in the vertical direction will be different depending on whether that memory chip is in the top row, which is further away and is connected with the longer data line L1, versus whether that memory chip is in the bottom row and is closer to the data buffer and is connected with the shorter data line L2; is that fair?



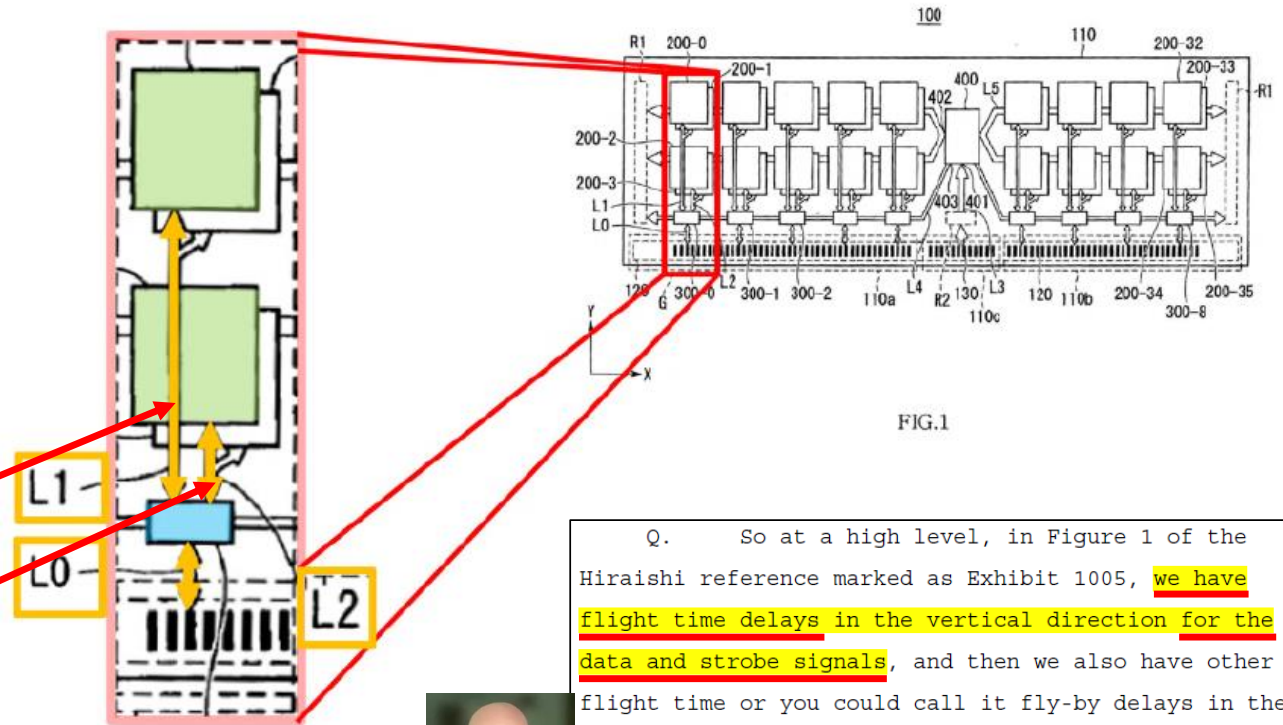
A. Yes, I think that's fair.

EX1074 at 217:2-10

Q. And then if we turn back to Figure 1 of the Hiraishi reference marked as Exhibit 1005, the flight time delay in the vertical direction will be greater for the data line L1 connected to memory chips at the top as compared to the flight time delay for the data on data line L2 that's connected to the memory chips in the bottom row; is that fair?

A. Yes, the length of the wires for L1 is greater than the length of the wires for L2, so the delay should be greater.

EX1074 at 223:20-224:4

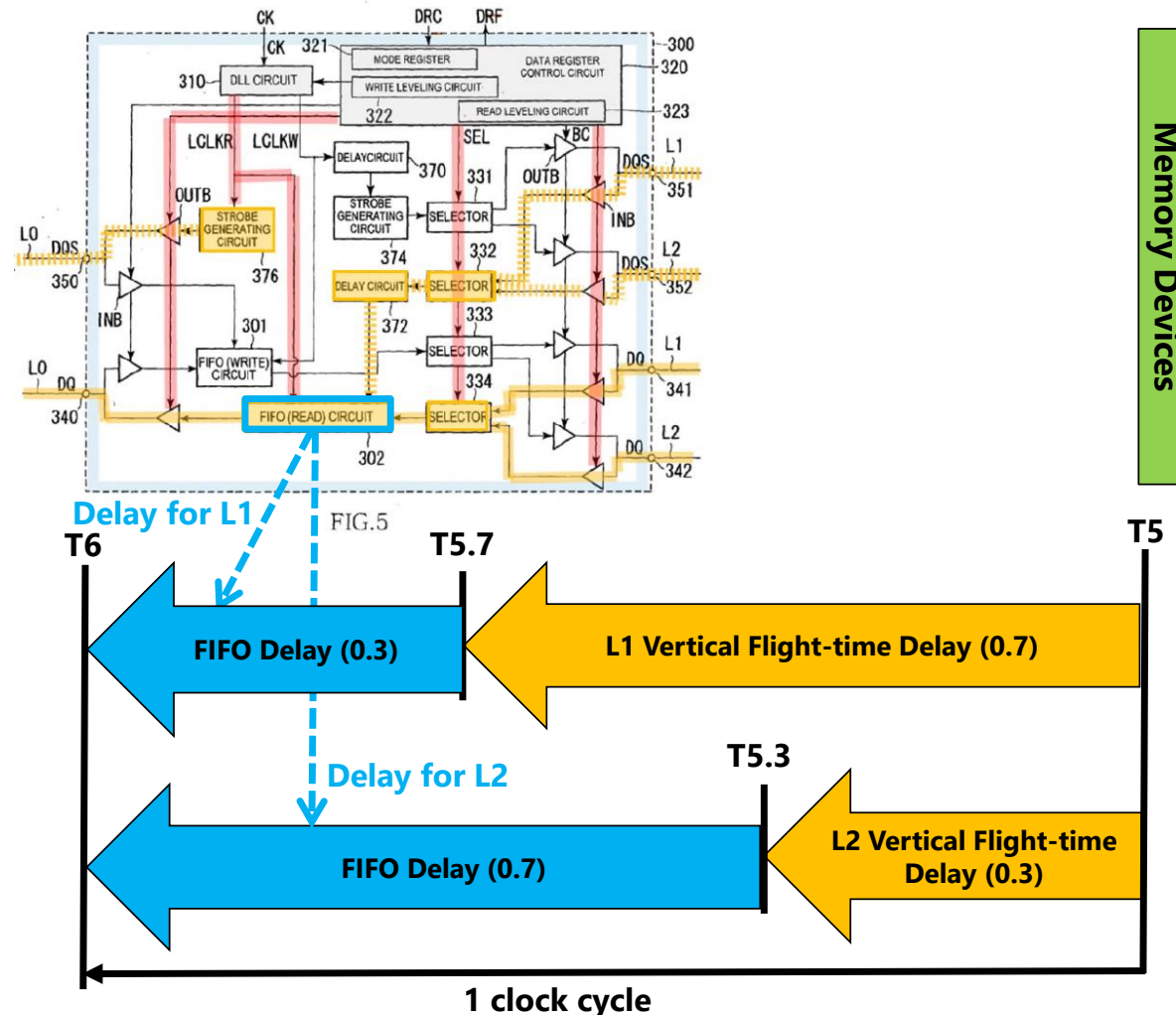


Q. So at a high level, in Figure 1 of the Hiraishi reference marked as Exhibit 1005, we have flight time delays in the vertical direction for the data and strobe signals, and then we also have other flight time or you could call it fly-by delays in the horizontal direction for the control address and clock signals; is that fair?

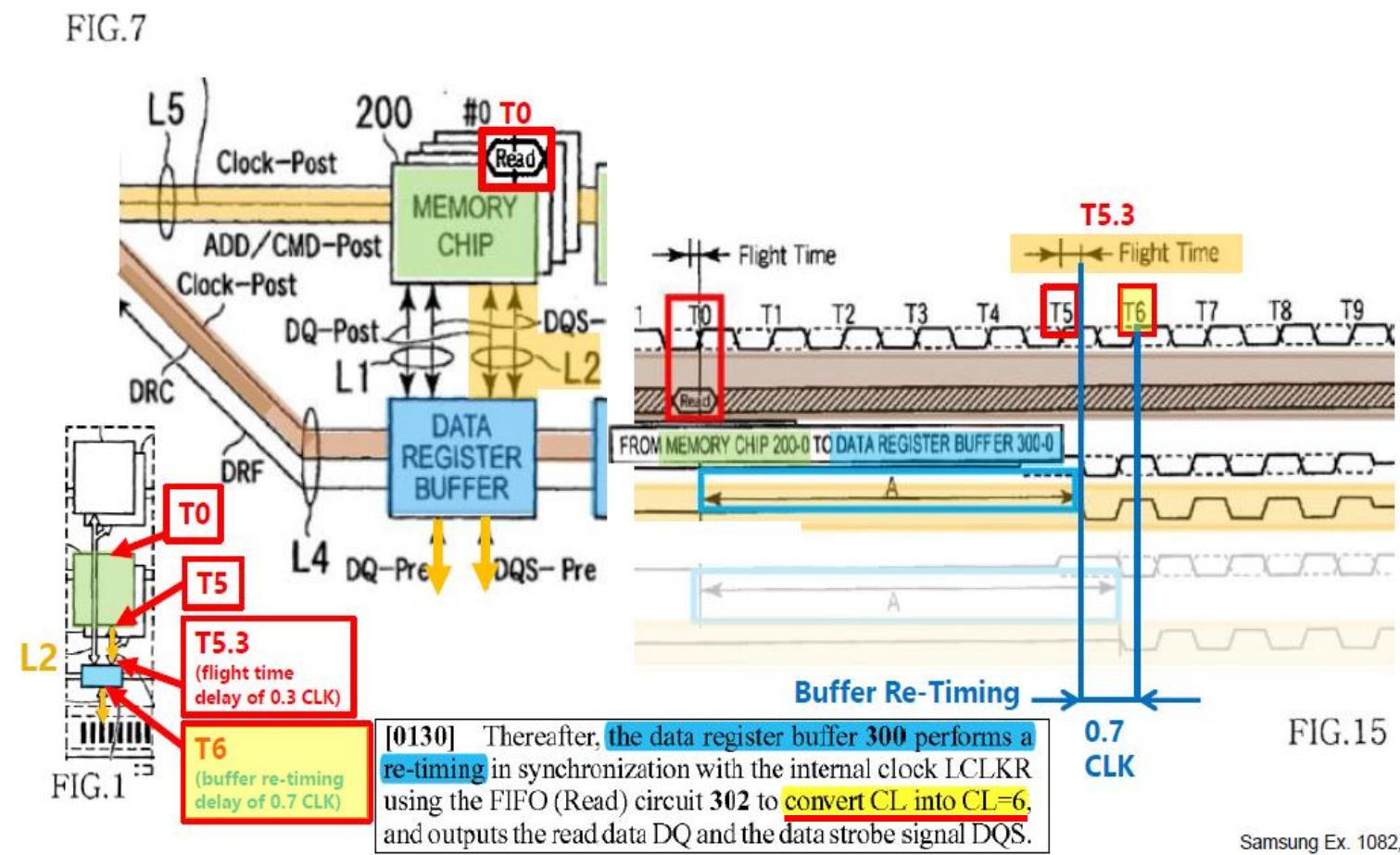
A. Yes, I believe that's fair.

EX1074 at 211:15-22

Hiraishi's “delay circuit” (e.g., FIFO (Read)) provides a variable delay for read data that depends on the amount of the vertical “Flight Time” delay (e.g., L1 and L2 delays)



When the vertical “Flight Time” is 0.3 clock cycles (e.g., on shorter data line L2), then Hiraishi’s data buffer delays (i.e., “re-time[s]”) Read data signals by 0.7 clock cycles and outputs them at T6

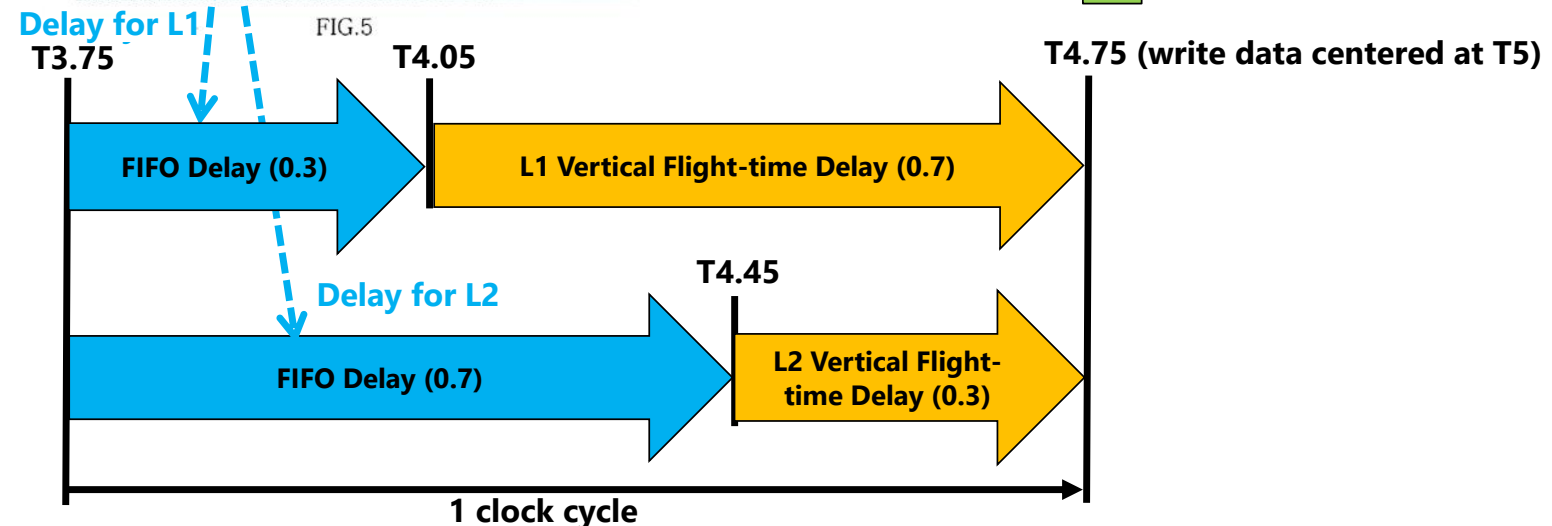
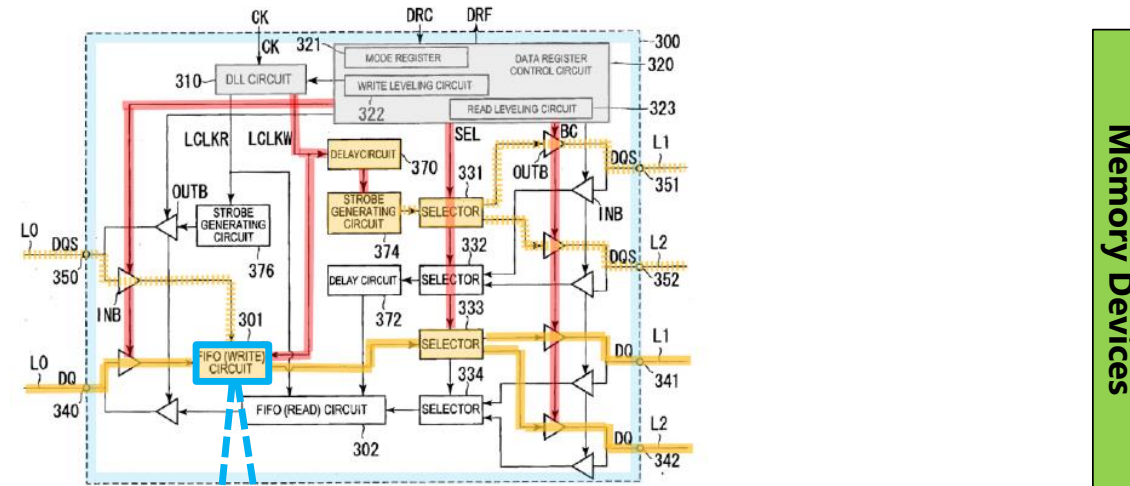


EX1005 at ¶[0130]

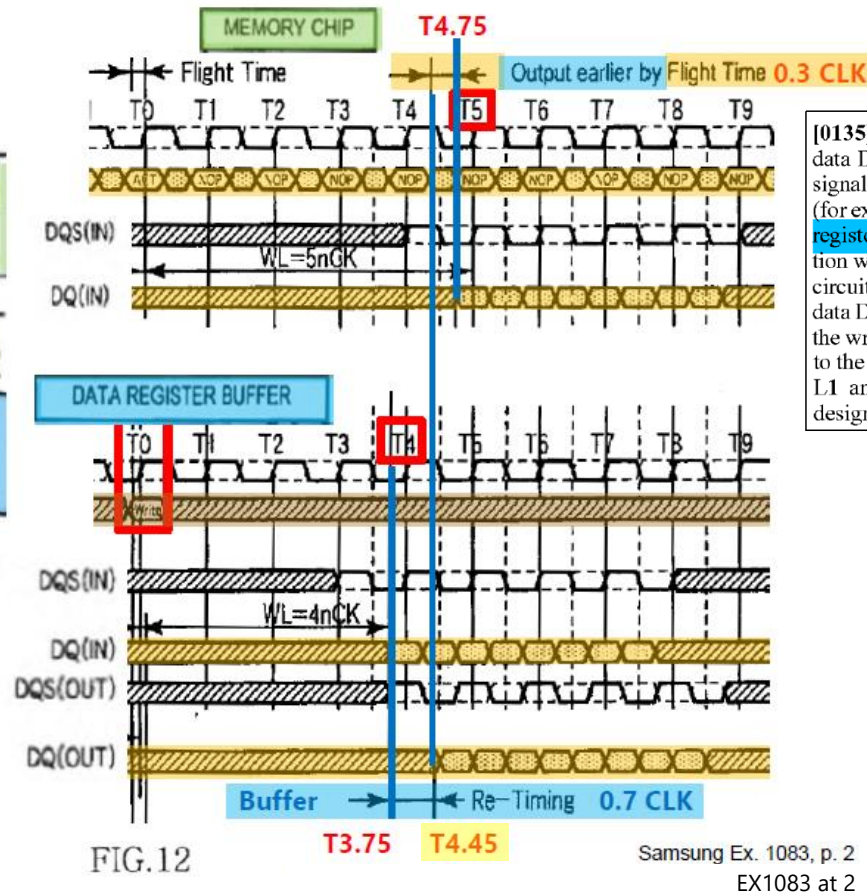
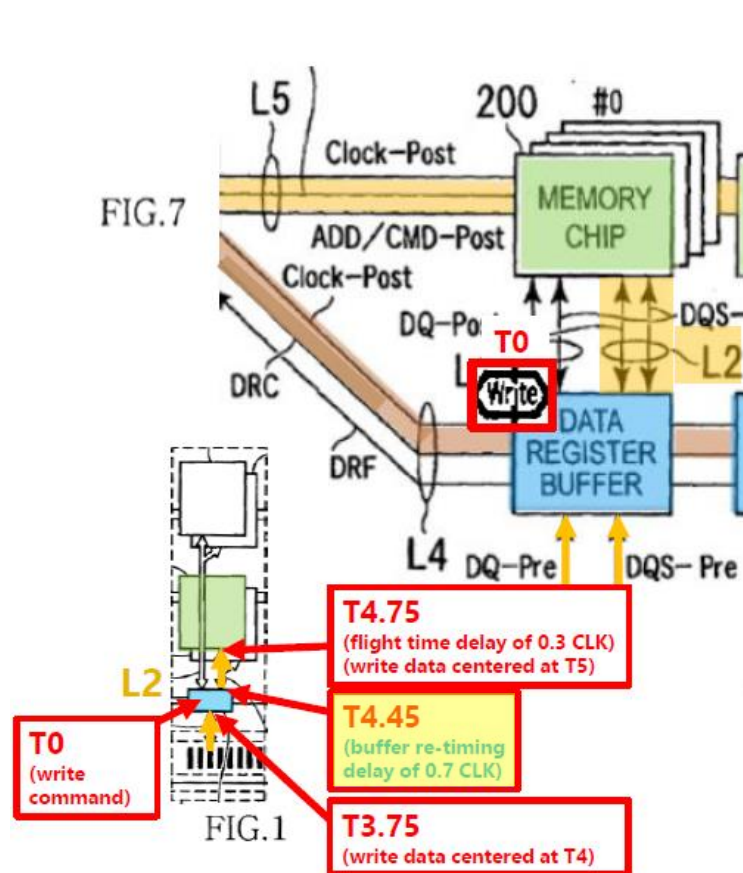
Samsung Ex. 1082, p. 2

EX1082 at 2

Hiraishi's "delay circuit" (e.g., FIFO (Write)) provides a variable delay for write data that depends on the amount of the vertical "Flight Time" delay (e.g., L1 and L2 delays)



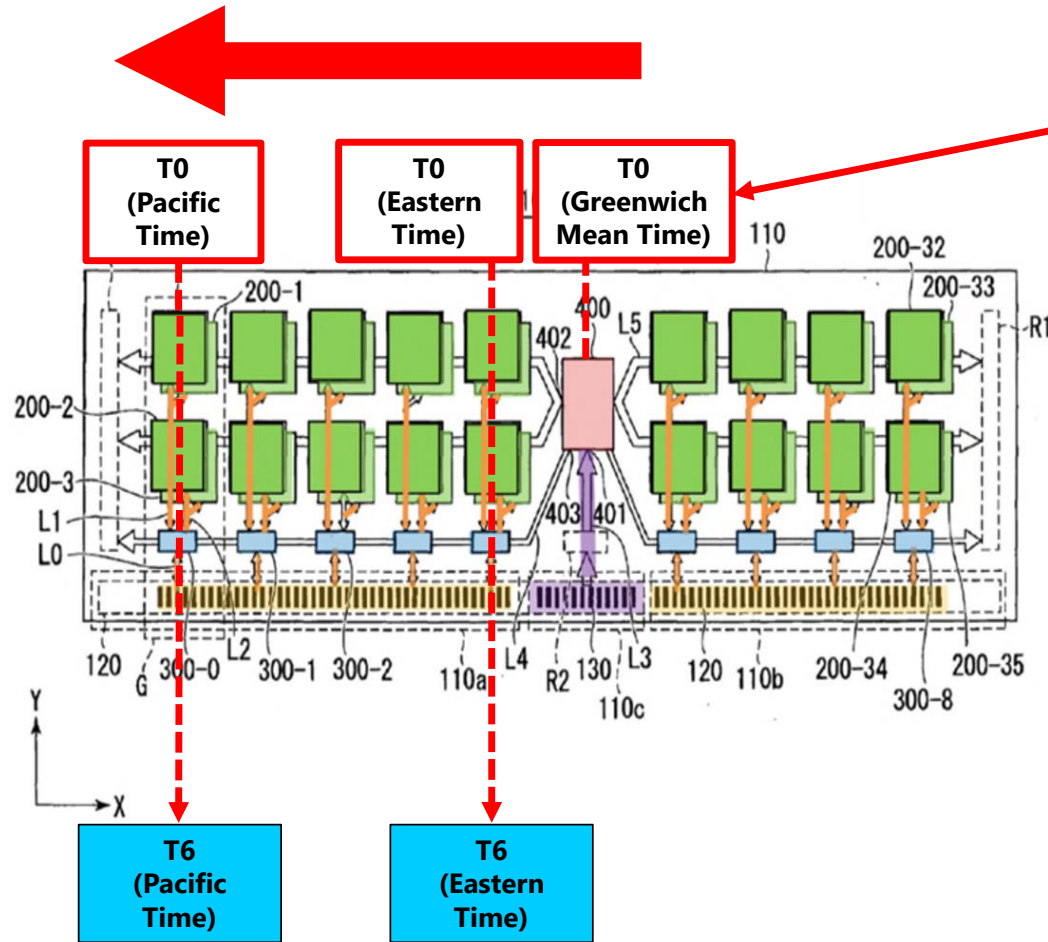
When the vertical “Flight Time” is 0.3 clock cycles (e.g., on shorter data line L2), then Hiraishi’s data buffer delays (i.e., “re-time[s]”) Write data signals by 0.7 clock cycles and outputs them at T4.45



[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank.

EX1005 at ¶[0135]

T0 (and thus T6) is different for each data buffer due to horizontal delays



Horizontal delay (before T0 at a given memory chip and T0 at a given data register buffer) for READ command to travel horizontally from the module controller (in the center of the module) to the memory chip and to the data register buffer

Vertical delay (after T5 at the given memory chip, corresponding to CAS latency of 5 clock cycles) for the DQ data signal and DQS strobe signal to travel vertically (e.g., for 0.3 or 0.7 clock cycles) from the memory chip down to the data register buffer, resulting in "Time A" (e.g., 5.3 clock cycles for shorter vertical data line L2, or 5.7 clock cycles for longer vertical data line L1)

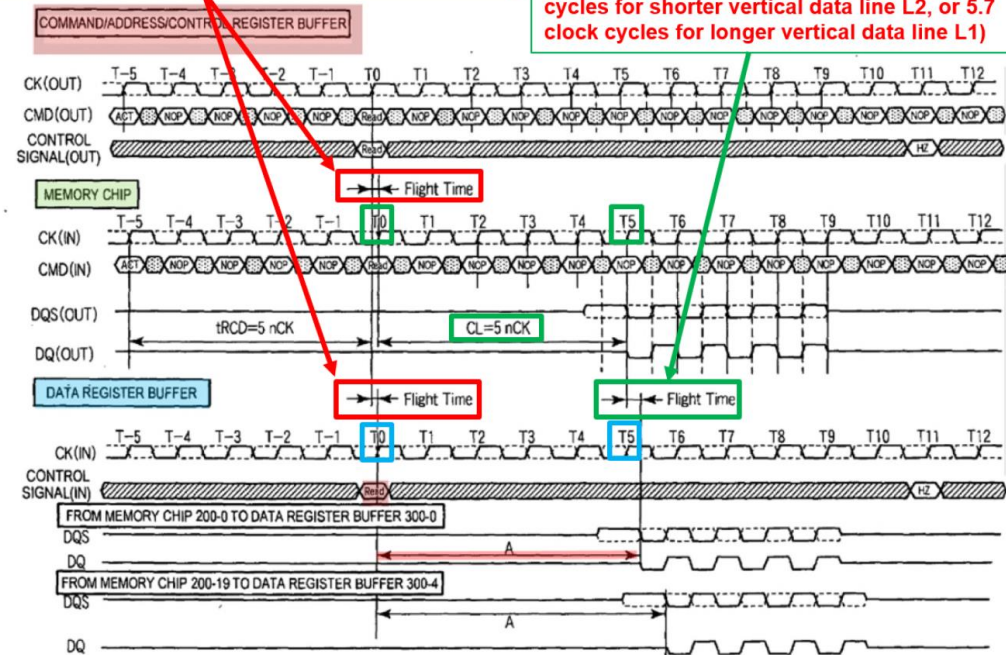


FIG.15

CAS Latency (CL) is measured from the time the memory device receives the command, which is T0



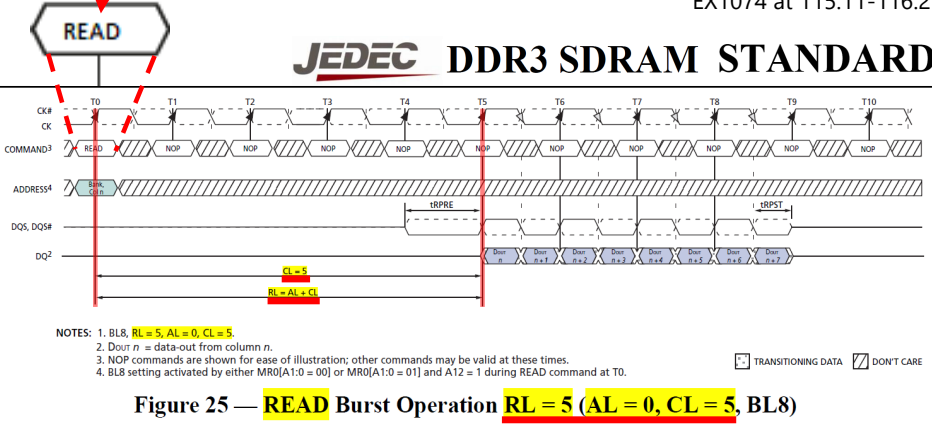
A. Thank you. Yes, I see that now. And, yes, additive latency is programmed at zero and CAS latency is programmed with a value of five.

...

operation, in this example, there is a delay of five clock cycles from the time a DDR3 memory device receives the read command until the time that the DDR3 memory device outputs the first piece of data on the DQ data line; is that fair?

A. Yes. There's a delay of five clock

EX1074 at 115:11-116:2



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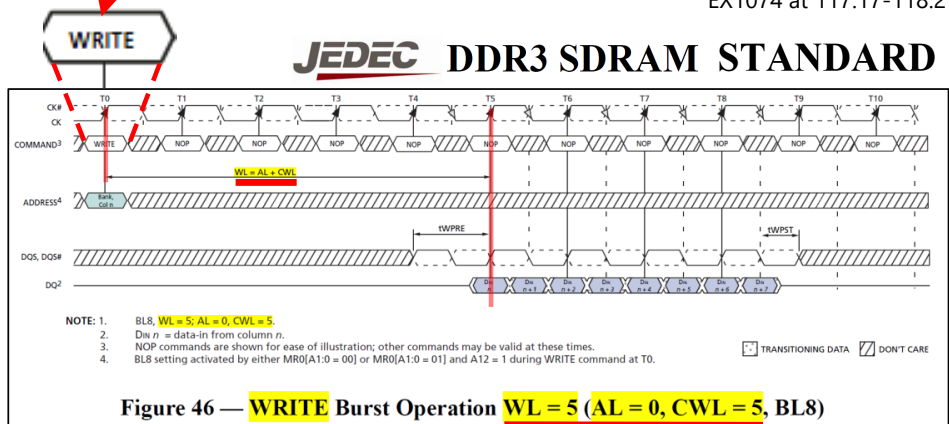
example, additive latency to zero and CAS write latency to five clock cycles, correct?

A. Yes, I see that.

Q. So in this example, there's a delay of five clock cycles from the time the DDR3 memory device receives the write command until the DDR3 memory device receives the first piece of data on the DQ data line, and in this example, that first piece of DQ data is center aligned with the DQS data strobe signal, correct?

A. Yes. This shows the write latency of

EX1074 at 117:17-118:2



Paper 23 (Reply) at 25 79

During S4 read leveling, Hiraishi's data buffer measures and stores "time A," which includes the different vertical "Flight Time" delays for L1 and L2



Q. And the total time from T0 until time, say, 5.3, is labeled as time A for memory chip 200-0 to data register buffer 300-0, correct?

A. Sure.

Q. And that time A comprises the CAS latency delay of five cycles, plus the vertical flight time delay, which looks like is perhaps 0.3 clock cycles for the time A corresponding to the memory chip 200-0 to data register buffer 300-0; is that fair?

A. It looks like that is -- yeah, that might ...

Q. But what is sort of reliable and clear is that the time A comprises the CAS latency delay of five clock cycles, plus the flight time delay in the vertical direction for the read data as it travels from the memory chip down to the data register buffer; is that fair?

A. Yes, that's fair. Starting with when the read command is received at the data buffer, yeah.

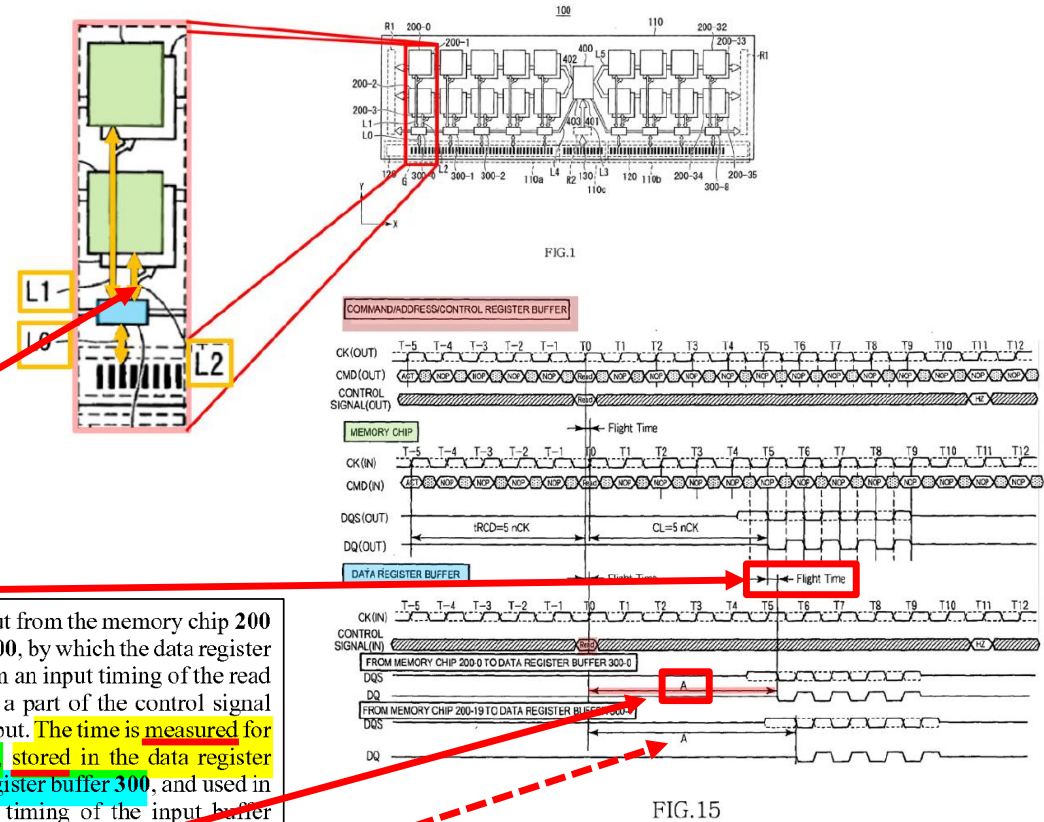
Q. And so in the -- in Figure 15 during read leveling, time A is measured, correct?

A. In essence, yes.

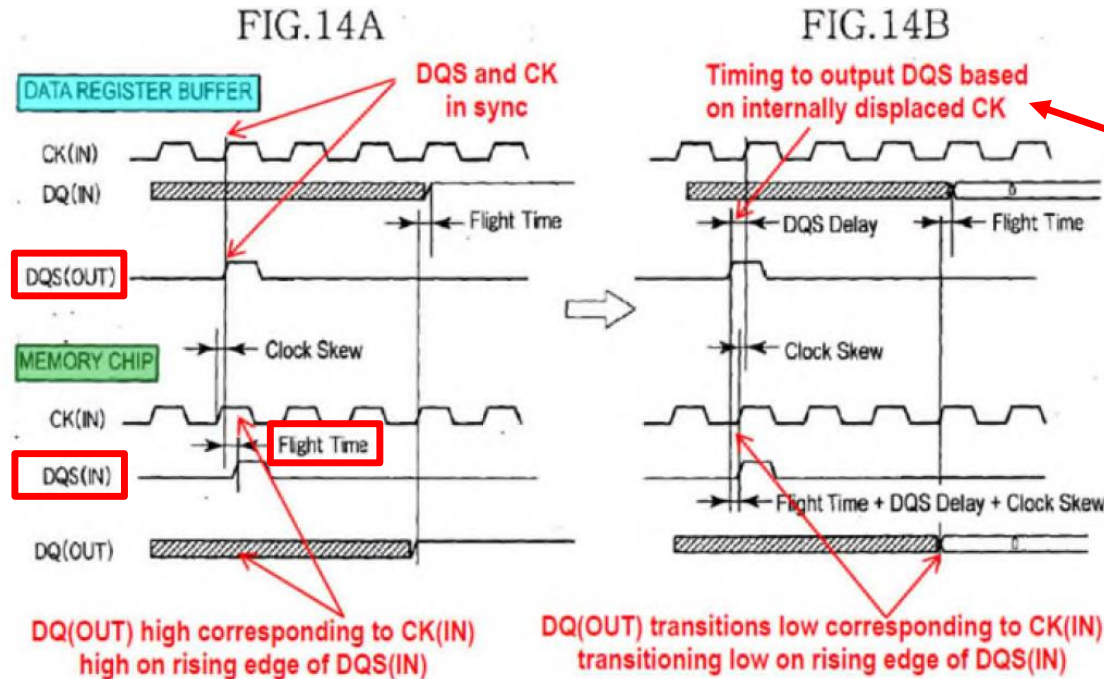
EX1074 at 222:14-223:12, 215:15-17

[0151] The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register control circuit 320 in the data register buffer 300, and used in an adjustment of an activation timing of the input buffer circuit INB and the like. In FIG. 15, two cases are shown including a first case that the time A from the input of the read command Read until the input of the read data DQ is short (between the memory chip 200-0 and the data register buffer 300-0) and a second case that the time A is long (between the memory chip 200-19 and the data register buffer 300-4).

EX1005, ¶[0151]



During S4 write leveling, Hiraishi's data buffer measures and stores the different vertical "Flight Time" delays for L1 and L2 using DQS strobe signals



EX1071 at 1

supplied to the memory chip 200 as described above. Because it takes a certain amount of propagation time until the data strobe signal DQS reaches the memory chip 200, input timings of the clock signal CK and the data strobe signal DQS are not always the same on the memory chip 200 side.

EX1005 at ¶[0143]

[0145] The write leveling circuit 322 of the data register buffer 300 changes an output timing of the data strobe signal DQS by displacing the internal clock LCLKW based on the direction of the phase shift. In the example shown in FIG. 14A, because the data strobe signal DQS is retarded as compared to a rising edge of the clock signal CK reaching the memory chip 200, the data register buffer 300 advances the output timing of the data strobe signal DQS.

EX1005 at ¶[0145]

[0146] By repeating the above operation, as shown in FIG. 14B, the logical level of the clock signal CK is changed to "Low level" at the rising edge of the data strobe signal DQS on the memory chip 200 side. This leads to an end of the write leveling operation, and the data register buffer 300 can find a timing to output the data strobe signal DQS based on the input clock signal CK. A result of the write leveling operation is stored in the data register control circuit 320 in the data register buffer 300. Upon completing the write leveling operation in this manner, the phases of the clock signal CK and the data strobe signal DQS input to the memory chip 200 are substantially matched with each other.

EX1005 at ¶[0146]

During write leveling, delays for DQ data signals are determined based on the measured delays for DQS stroke signals because DQ data signals travel with DQS stroke signals within a “very tight tolerance”



Q. Yes, there's the heading "Data Timing" and there's the first row. And if you look in the second column, the symbol is tDQSQ. And the permissible range -- the maximum range on the entire range for tDQSQ is 200 picoseconds, correct?

THE WITNESS: It says that there is a -- the options configurations listed here, there is a maximum of 200 picoseconds.

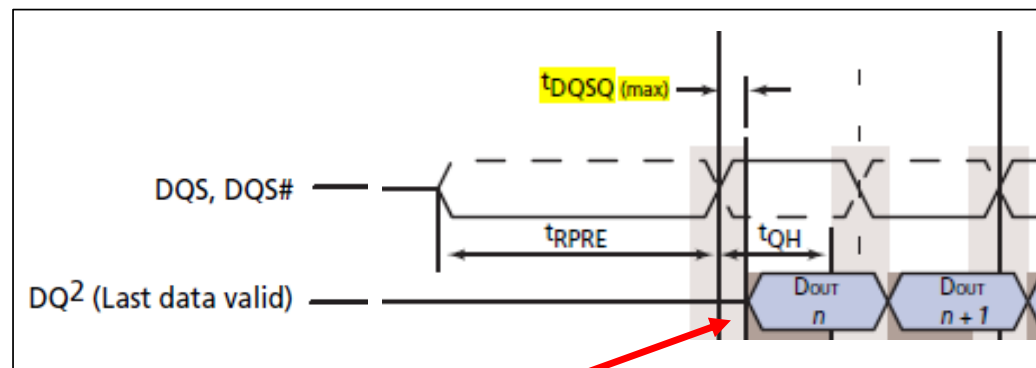
Q. So it would be fair to say that the JEDEC standard for DDR3 memory devices does not permit a large amount of skew between the DQS stroke signal and DQ data signal.

To the contrary, it could fairly be characterized as requiring a very tight tolerance between the DQS stroke signal and the DQ data signal, correct?

THE WITNESS: Yes, it requires a very tight tolerance.

EX1074 at 137:13-22, 139:13-24 (objections omitted)

tDQSQ defines the skew between DQS,DQS# to Data



EX1020 (JEDEC DDR3 standard) at 59

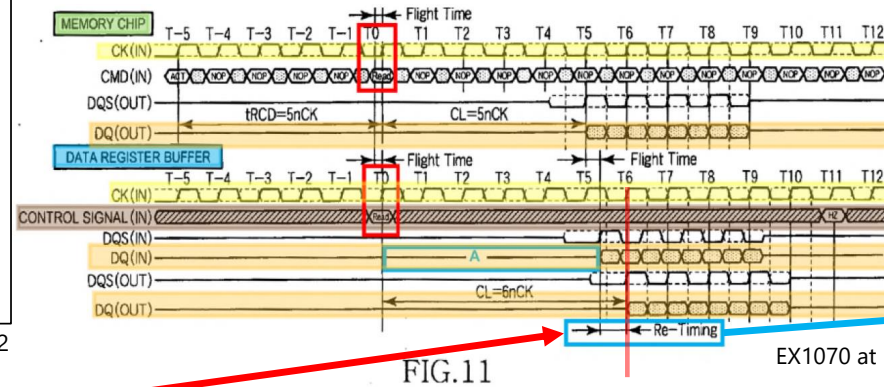
The stored variable delays are used by Hiraishi's "delay circuit" (e.g., **FIFO**) to delay (i.e., "re-time") data signals during normal read/write operations



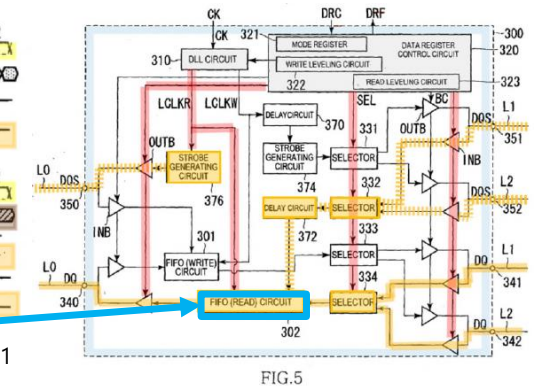
Q. And how is that result used, then, to actually correct these -- for this fly-by issue?

A. So what it does is once you have that -- the necessary delay, as I just said -- or you just said and I agreed with, once it stores that -- that value in the -- in the control section of the data buffer, it then uses that -- it uses that value to tell you how much to delay the DQS signal and its associated DQ data in a -- when you're doing a normal write operation.

EX2012 at 64:4-12

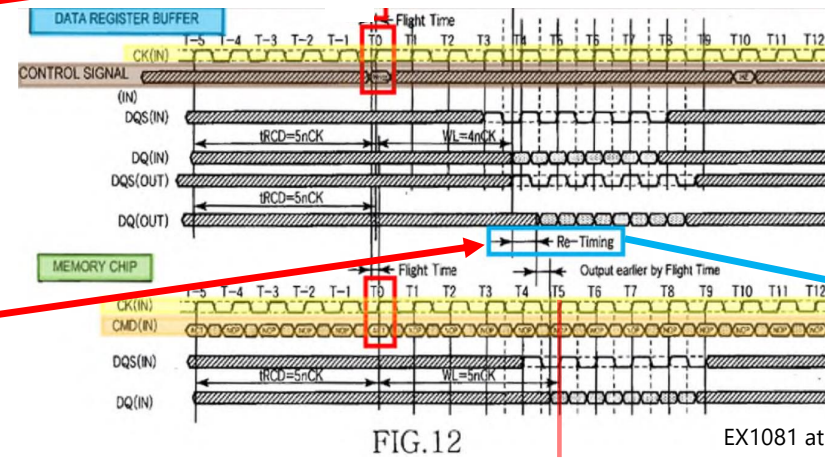


EX1070 at 1

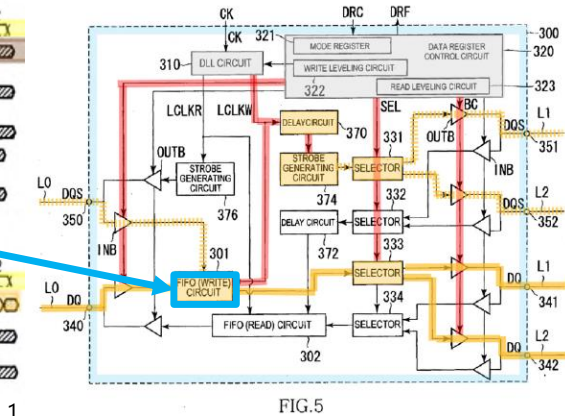


[0130] Thereafter, the data register buffer 300 performs a re-timing in synchronization with the internal clock LCLKR using the FIFO (Read) circuit 302 to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

EX1005 at ¶[0130]



EX1081 at 1



[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DOS. As described above,

EX1005 at ¶[0135]

Hiraishi's data buffer does not simply add a fixed delay of one clock cycle, which would result in a non-integer latency value, contrary to the JEDEC standard



Q. BY MR. LINDSAY: Yeah, and so in Hiraishi's case, his -- he doesn't disclose delays greater than one CLK cycle. So if you delay to one CLK cycle, you'll know that he has accounted for all possible delays in his system?

A. Again, I want to make sure we're clear on this. We don't just delay one CLK cycle. We delay whatever time is necessary --

Q. Right.

A. -- in order that -- in order for it to line up. I mean, in fact -- but you're correct that in the examples, he doesn't show anything more than one CLK cycle, so -- but my understanding from Hiraishi is that you delay the length of time necessary for it to line up.

EX2012 at 79:15-80:3

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3.4.2.2 CAS Latency

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. DDR3 SDRAM does not support any half-clock latencies. The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); $RL = AL + CL$. For more information on the supported CL and AL settings based on the operating clock frequency, refer to "Standard Speed Bins" on page 157. For detailed Read operation, refer to "READ Operation" on page 56.

EX1020 (JEDEC DDR3 standard) at 24

Q. And according to the JEDEC standard for DDR3 memory devices, the permissible CAS latency values are five clock cycles, six clock cycles, seven clock cycles, eight clock cycles, nine clock cycles, or ten clock cycles, or optionally, 11 clock cycles for 1600 DDR3 memory devices; is that correct?

THE WITNESS: Yes, that is what it indicates in that table.

Q. Am I correct there's no listing of any half clock cycle latencies or fractional clock cycle latencies for additive latency? In other words, there are only integer values permitted by Table 4 for additive latency?

THE WITNESS: That's correct.

EX1074 at 108:17-109:1, 110:22-111:4 (objections omitted)

Paper 23 (Reply) at 24-25

84

JEDEC does not allow non-integer latency values (e.g., 5.3 or 5.7 clock cycles)

Programmable CAS Latency

JEDEC's programmable CAS latency is used to allow each system vendor to optimize the performance of its systems. It is programmed at system initialization, and, according to industry designers, it is never set again while the machine is running [Lee 2002, Baker 2002,

EX1021 at 342

Table 6 — Command Truth Table

Function	Abbrevia tion	CKE		CS#	RAS#	CAS#	WE#	BA0- BA2	A13- A15	A12- BC#	A10- AP	A0- A9, A11	Notes
		Previous Cycle	Current Cycle										
Mode Register Set	MRS	H	H	L	L	L	L	BA	OP Code				
Bank Activate	ACT	H	H	L	L	H	H	BA	Row Address (RA)				
Write (Fixed BL8 or BC4)	WR	H	H	L	H	L	L	BA	RFU	V	L	CA	
Read (Fixed BL8 or BC4)	RD	H	H	L	H	L	H	BA	RFU	V	L	CA	
No Operation	NOP	H	H	L	H	H	H	V	V	V	V	V	10
Device Deselected	DES	H	H	H	X	X	X	X	X	X	X	X	11

NOTE 1 All DDR3 SDRAM commands are defined by states of CS#, RAS#, CAS#, WE# and CKE at the rising edge of the clock. The MSB of BA, RA and CA are device density and configuration dependant.

2.10 Pinout Description

Symbol	Type	Function
CK, CK#	Input	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#.
CS#, (CS0#), (CS1#), (CS2#), (CS3#)	Input	Chip Select: All commands are masked when CS# is registered HIGH. CS# provides for external Rank selection on systems with multiple Ranks. CS# is considered part of the command code.
RAS#, CAS#, WE#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.
DQ	Input / Output	Data: Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, DQS#, DQSU, DQSL#, DQSL, DQSL#	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. For the x16, DQSL corresponds to the data on DQ0-DQ7; DQSU corresponds to the data on DQ8-DQ15. The data strobes DQS, DQSL, and DQSU are paired with differential signals DQS#, DQSL#, and DQSU#, respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.

EX1020 (JEDEC DDR3 standard) at 13, 33-34

JEDEC DDR3 SDRAM STANDARD

A6	A5	A4	A2	CAS Latency
0	0	0	0	Reserved
0	0	1	0	5
0	1	0	0	6
0	1	1	0	7
1	0	0	0	8
1	0	1	0	9
1	1	0	0	10
1	1	1	0	11 (Optional for DDR3-1600)

A4	A3	Additive Latency
0	0	0 (AL disabled)
0	1	CL-1
1	0	CL-2
1	1	Reserved

The CAS Latency is defined by MR0 (bits A9-A11) as shown in Figure 9. CAS Latency is the delay, in clock cycles, between the internal Read command and the availability of the first bit of output data. **DDR3 SDRAM does not support any half-clock latencies.** The overall Read Latency (RL) is defined as Additive Latency (AL) + CAS Latency (CL); $RL = AL + CL$. For more information on the supported CL and AL

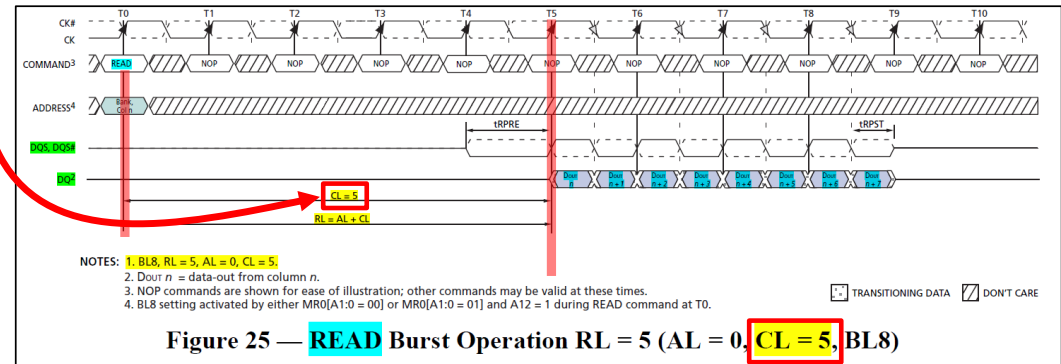


Figure 25 — READ Burst Operation RL = 5 (AL = 0, CL = 5, BL8)

EX1020 (JEDEC DDR3 standard) at 23, 24, 26, 56

In an example of Hiraishi, where a vertical “Flight Time” delay is 0.3 clock cycles (e.g., on shorter data line L2), read data signals arrive at the data buffer at T5.3

FIG.7

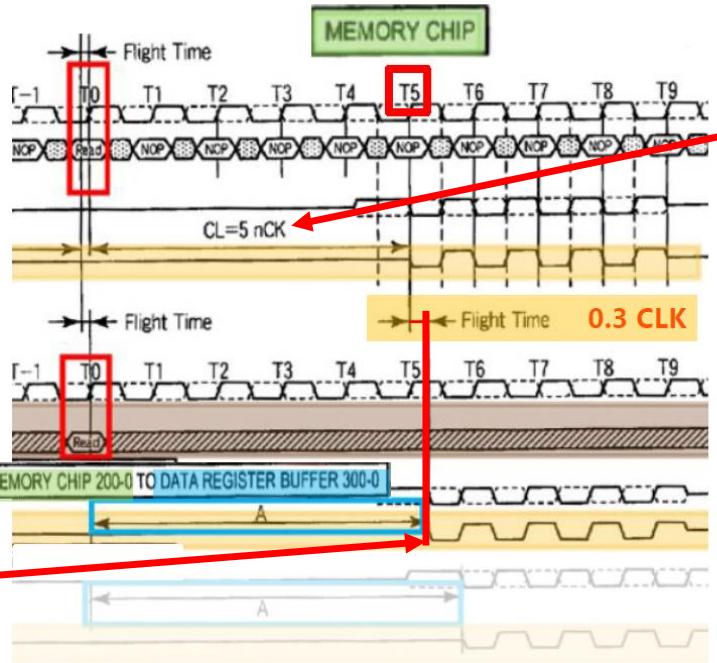
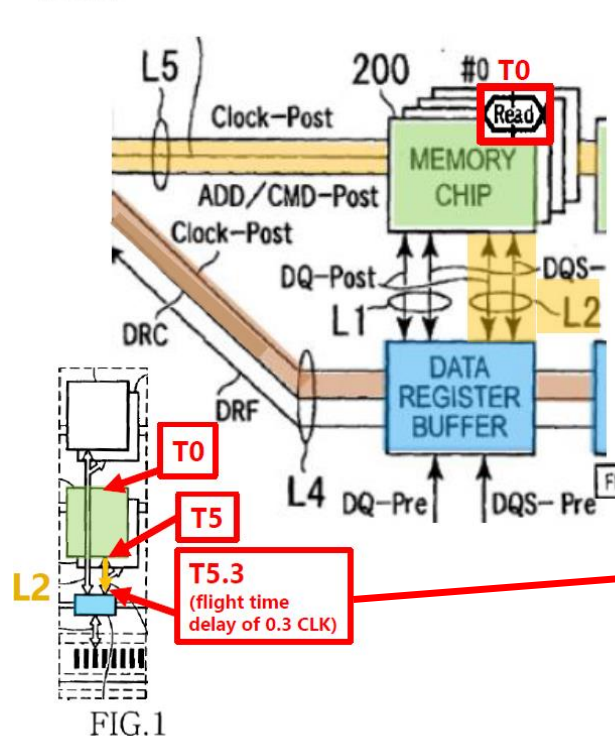


FIG.15

Samsung Ex. 1082, p. 1
EX1082 at 1

Programmable **CAS Latency**
JEDEC's **programmable CAS latency** is used to allow each system vendor to optimize the performance of its systems. **It is programmed at system initialization**, and, according to industry designers, it is never set again while the machine is running [Lee 2002, Baker 2002, Kellogg 2002, Macri 2002, Ryan 2002, Rhoden 2002, Sussman 2002]. *By contrast, with Rambus' variable*
EX1021 at 342



Q. And according to the JEDEC standard for DDR3 memory devices, **the permissible CAS latency values are five clock cycles, six clock cycles, seven clock cycles, eight clock cycles, nine clock cycles, or ten clock cycles, or optionally, 11 clock cycles** for 1600 DDR3 memory devices; is that correct?
THE WITNESS: **Yes**, that is what it indicates in that table.

EX1074 at 108:17-109:1 (objections omitted)

Then, Hiraishi's data buffer delays (i.e., "re-time[s]") the read data signals by **0.7 clock cycles**, so that those signals are output at T6 (i.e., T5.3 + 0.7)

FIG.7

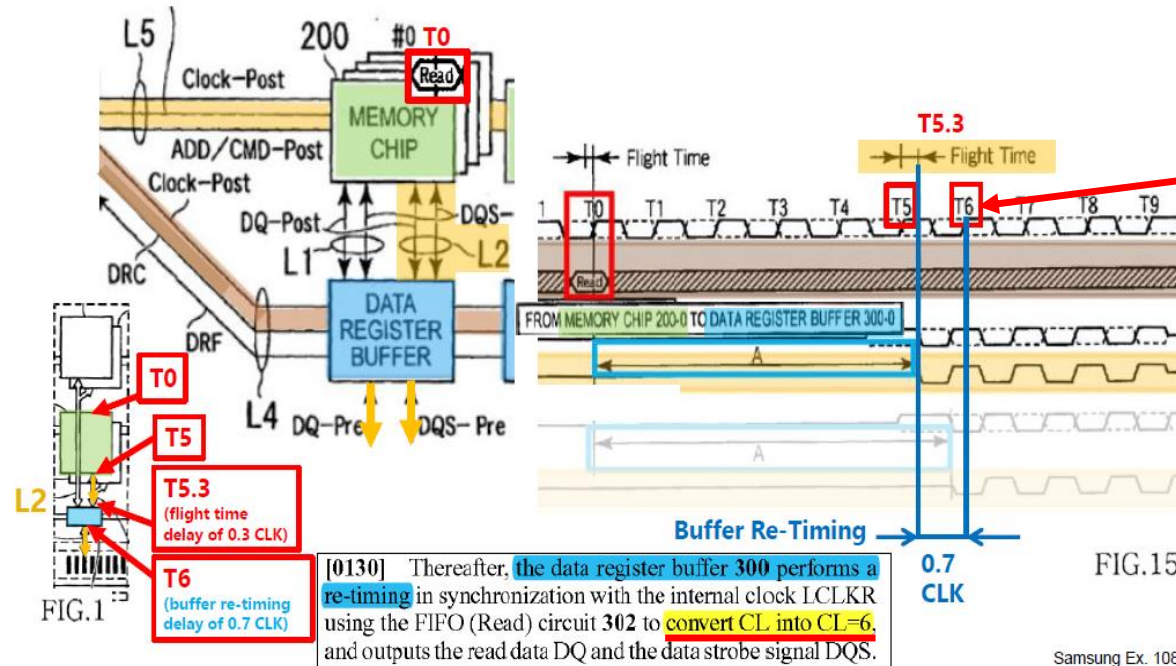


FIG.15

Samsung Ex. 1082, p. 2
EX1082 at 2

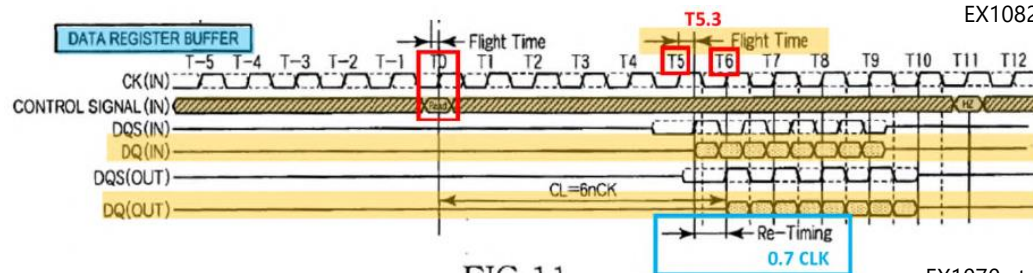


FIG.11

EX1070 at 1

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE



So for the data that arrived earlier, there is a delay, a longer delay, than for the data that arrived later. In the case of the example, it delays it until T6. But it does -- it inserts a necessary delay so that ...

And it does that by inserting the necessary delays. It does not do it -- it does not delay for a fixed time period of only -- of it -- in your hypothetical, it does not delay it until 6.25 or 6.5. it delays it the time necessary so that it can output it at 6 in this example.

Q. BY MR. CHANDLER: So just to follow up on that, and following up on my hypothetical, where the memory device at the top row outputs its read data at time T5, that read data arrived at the buffer circuit at time T5.5. In that hypothetical, how much delay does the buffer circuit add in that examples.

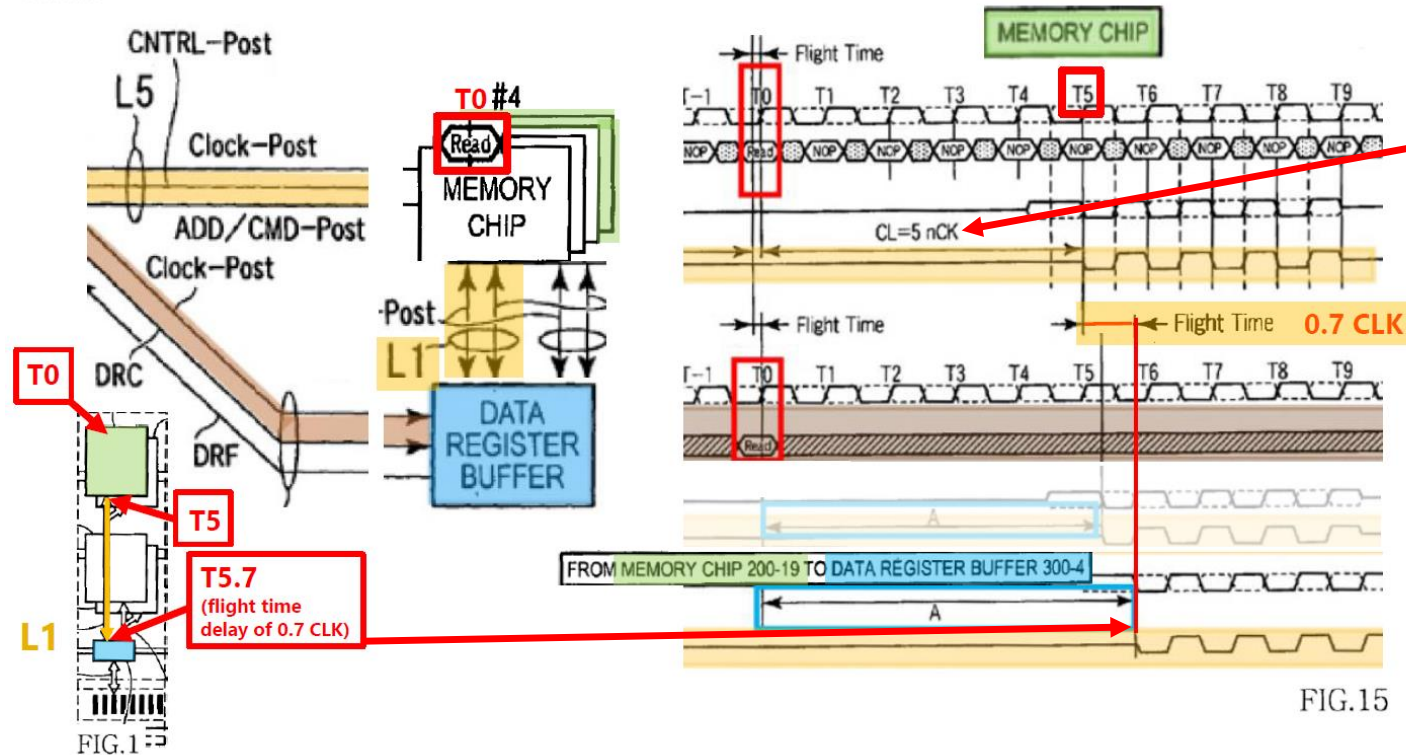
A. In that example, it would add an additional .5 CLK delay for the -- for the upper circuit, and it would delay in the case of the lower circuit, which arrived at 5 -- at CLK 5.25, it would need to add another .75 CLKs in order to make them both outbound at time T6.

EX2012 at 132:16-133:17

Paper 23 (Reply) at 25-27 87

In another example of Hiraishi, where a vertical “Flight Time” delay is 0.7 clock cycles (e.g., on longer data line L1), read data signals arrive at the data buffer at T5.7

FIG.7



Samsung Ex. 1082, p. 3
EX1082 at 3

Programmable CAS Latency

JEDEC's programmable CAS latency is used to allow each system vendor to optimize the performance of its systems. It is programmed at system initialization, and, according to industry designers, it is never set again while the machine is running [Lee 2002, Baker 2002, Kellogg 2002, Macri 2002, Ryan 2002, Rhoden 2002, Sussman 2002]. By contrast, with Rambus' variable

EX1021 at 342



Q. And according to the JEDEC standard for DDR3 memory devices, the permissible CAS latency values are five clock cycles, six clock cycles, seven clock cycles, eight clock cycles, nine clock cycles, or ten clock cycles, or optionally, 11 clock cycles for 1600 DDR3 memory devices; is that correct?

THE WITNESS: Yes, that is what it indicates in that table.

EX1074 at 108:17-109:1 (objections omitted)

Then, Hiraishi's data buffer delays (i.e., "re-time[s]") the read data signals by 0.3 clock cycles, so that those signals are output at T6 (i.e., T5.7 + 0.3)

FIG.7

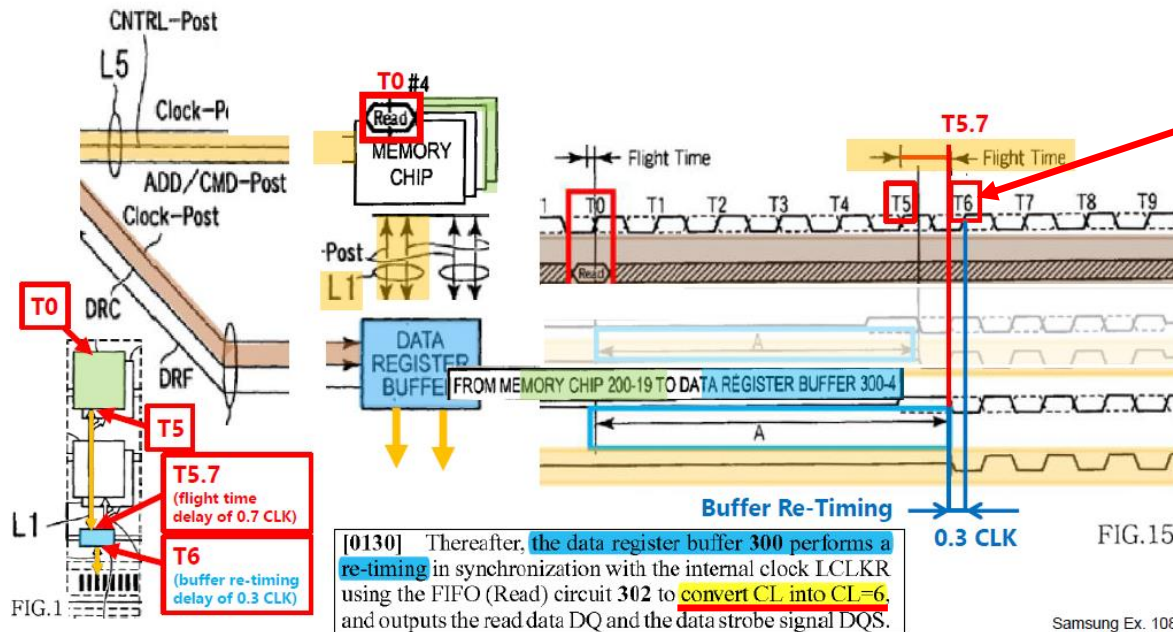


FIG.15

Samsung Ex. 1082, p. 4

EX1082 at 4



So for the data that arrived earlier, there is a delay, a longer delay, than for the data that arrived later. In the case of the example, it delays it until T6. But it does -- it inserts a necessary delay so that ...

And it does that by inserting the necessary delays. It does not do it -- it does not delay for a fixed time period of only -- of it -- in your hypothetical, it does not delay it until 6.25 or 6.5. it delays it the time necessary so that it can output it at 6 in this example.

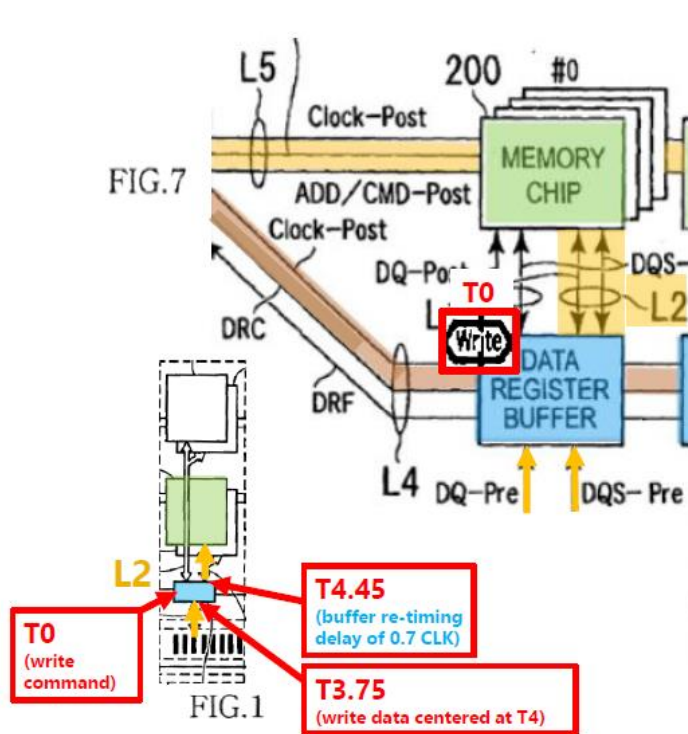
Q. BY MR. CHANDLER: So just to follow up on that, and following up on my hypothetical, where the memory device at the top row outputs its read data at time T5, that read data arrived at the buffer circuit at time T5.5. In that hypothetical, how much delay does the buffer circuit add in that examples.

A. In that example, it would add an additional .5 CLK delay for the -- for the upper circuit, and it would delay in the case of the lower circuit, which arrived at 5 -- at CLK 5.25, it would need to add another .75 CLKs in order to make them both outbound at time T6.

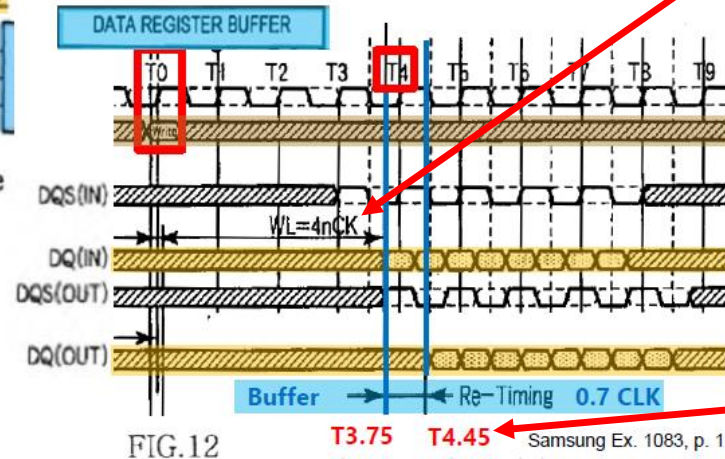
EX2012 at 132:16-133:17

Paper 23 (Reply) at 27-29 89

In another example of Hiraishi, where a vertical “Flight Time” delay is 0.3 clock cycles (e.g., on shorter data line L2), the data buffer delays (i.e., “re-time[s]”) write data signals by 0.7 clock cycles until T4.45



[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL-5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank.



Samsung Ex. 1083, p. 1
EX1083 at 1

Programmable CAS Latency

JEDEC's *programmable CAS latency* is used to allow each system vendor to optimize the performance of its systems. It is programmed at system initialization, and, according to industry designers, it is never set again while the machine is running [Lee 2002, Baker 2002, Kellogg 2002, Macri 2002, Ryan 2002, Rhoden 2002, Sussman 2002]. By contrast, with Rambus' *variable*

EX1021 at 342

Q. And according to the JEDEC standard for DDR3 memory devices, the permissible CAS latency values are five clock cycles, six clock cycles, seven clock cycles, eight clock cycles, nine clock cycles, or ten clock cycles, or optionally, 11 clock cycles for 1600 DDR3 memory devices; is that correct?

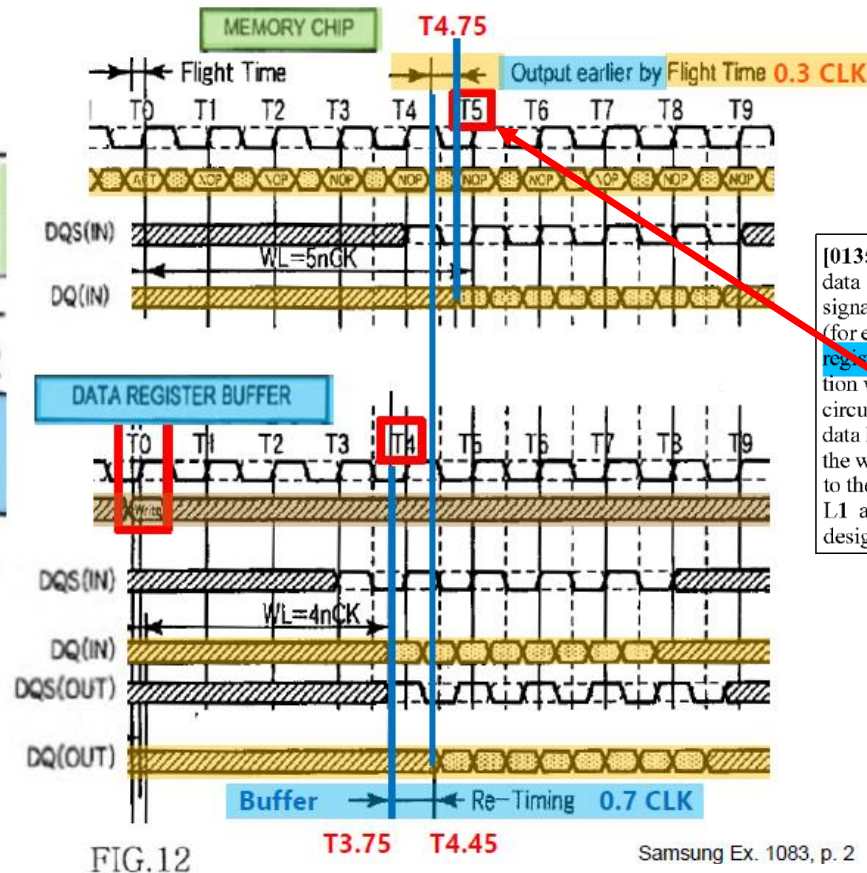
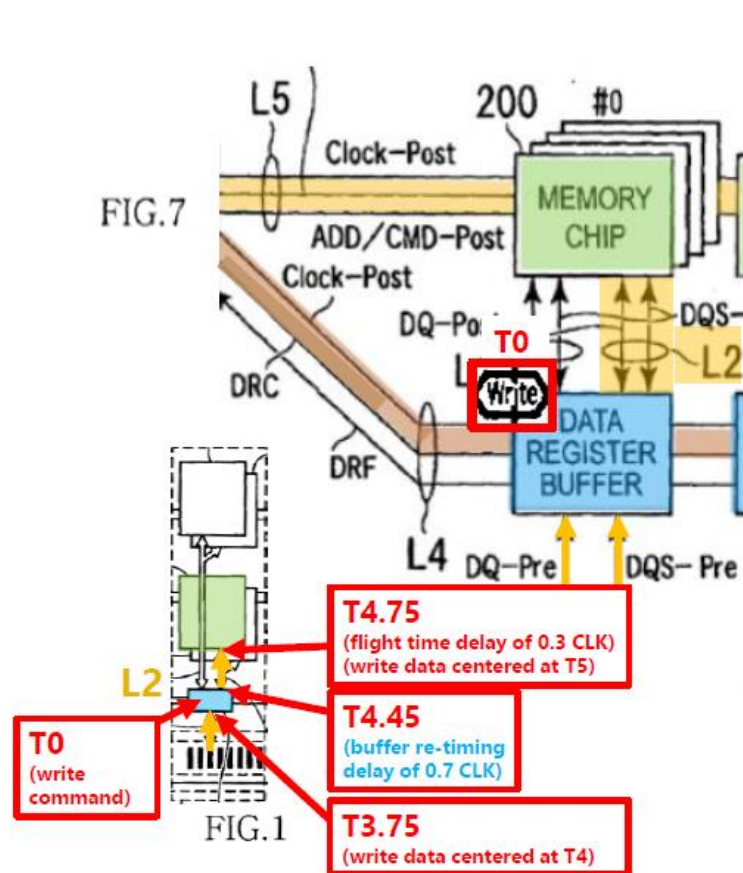
THE WITNESS: Yes, that is what it indicates in that table.

DQ data line, and in this example, that first piece of DQ data is center aligned with the DQS data strobe signal, correct?

A. Yes. This shows the write latency of

EX1074 at 108:17-109:1, 117:24-118:2 (objections omitted)

Next, the write data signals, after the 0.3 clock cycles of vertical “Flight Time” delay, arrive at the memory chip at T4.75 (center aligned at T5)



[0135] The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 with a data strobe signal DQS that is delayed by a predetermined phase amount (for example, phase difference of about 90 degrees). The data register buffer 300 then performs a re-timing in synchronization with the internal clock LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS. As described above, the write data is transferred from the data register buffer 300 to the memory chip 200 using either one of the two data lines L1 and L2. The data line to be used is determined by a designated Rank.

The Board's Institution Decision in the '632 IPR (left), which concluded read data is always output at T6, does not conflict with IPR2022-00236 or Samsung's arguments here, which involve delaying data through the "data path"

the '632 Patent

Claim 1 recites

wherein the each respective buffer circuit is configured to determine a respective time interval based on signals received by the each respective buffer circuit during a memory write operation and is further configured to time transmission of a respective set of read data signals received from the respective group of memory devices in accordance with the time interval and a read latency parameter of the memory system during a memory read operation.

EX1014 (IPR2017-00730, '632 ID, Paper 8) at 10
(reciting Claim 1 in '632 patent)

circuit INB and the like." Ex. 1005 ¶ 14 [Hiraishi] does not teach time A being used to adjust timing of data output by data buffer circuit 300 to the system controller (i.e., to "time transmission of a respective set of read data signals,") as recited in the claim.

EX1014 (IPR2017-00730, '632 ID, Paper 8) at 13
(with [Hiraishi] inserted in place of Saito)

the '608 Patent

module clock signal, wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount determined by the command processing circuit in response to at least one of the module control signals.

EX1001 at 19:49-55 (Claim [1.f])

For determining a respective time interval, Petitioner relies upon [Hiraishi]'s write leveling operation performed by write leveling circuit 322 of data register buffer 300. Pet. 28-29. This operation, depicted in Figures 14A and 14B of Saito, determines an amount of time by which to shift the output of DQS from data register buffer 300 so that it arrives at memory chip 200 substantially matched with clock signal CK. Ex. 1005 ¶¶ 140-144.

EX1014 (IPR2017-00730, '632 ID, Paper 8) at 10
(with [Hiraishi] inserted in place of Saito)

signals to either pass through or not pass through. Ex. 1022, 70:10-22. We determine that these disclosures of [Hiraishi] are sufficient to teach controlling the timing of the data and strobe signals on the data paths on which those signals travel.

EX1066 (IPR2022-00236 Final Written Decision) at 36
(with [Hiraishi] inserted in place of Osanai)

GROUND 2 03

GROUND 2: GROUND 1 + TOKUHIRO

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 93

COMBINATION FOR GROUND 2

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 94

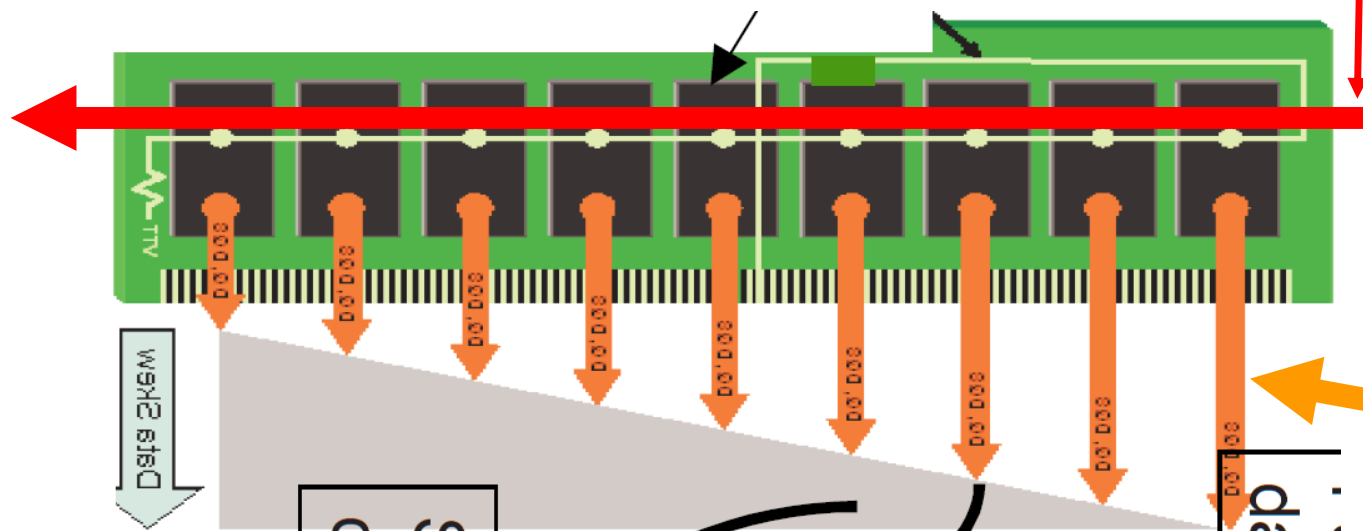
JEDEC's DDR3 standard adopted a "fly-by topology," resulting in horizontal fly-by delays for commands that needed to be corrected with read/write leveling to **unskew the data signals**

JEDEC DDR3 SDRAM

4.8 Write Leveling

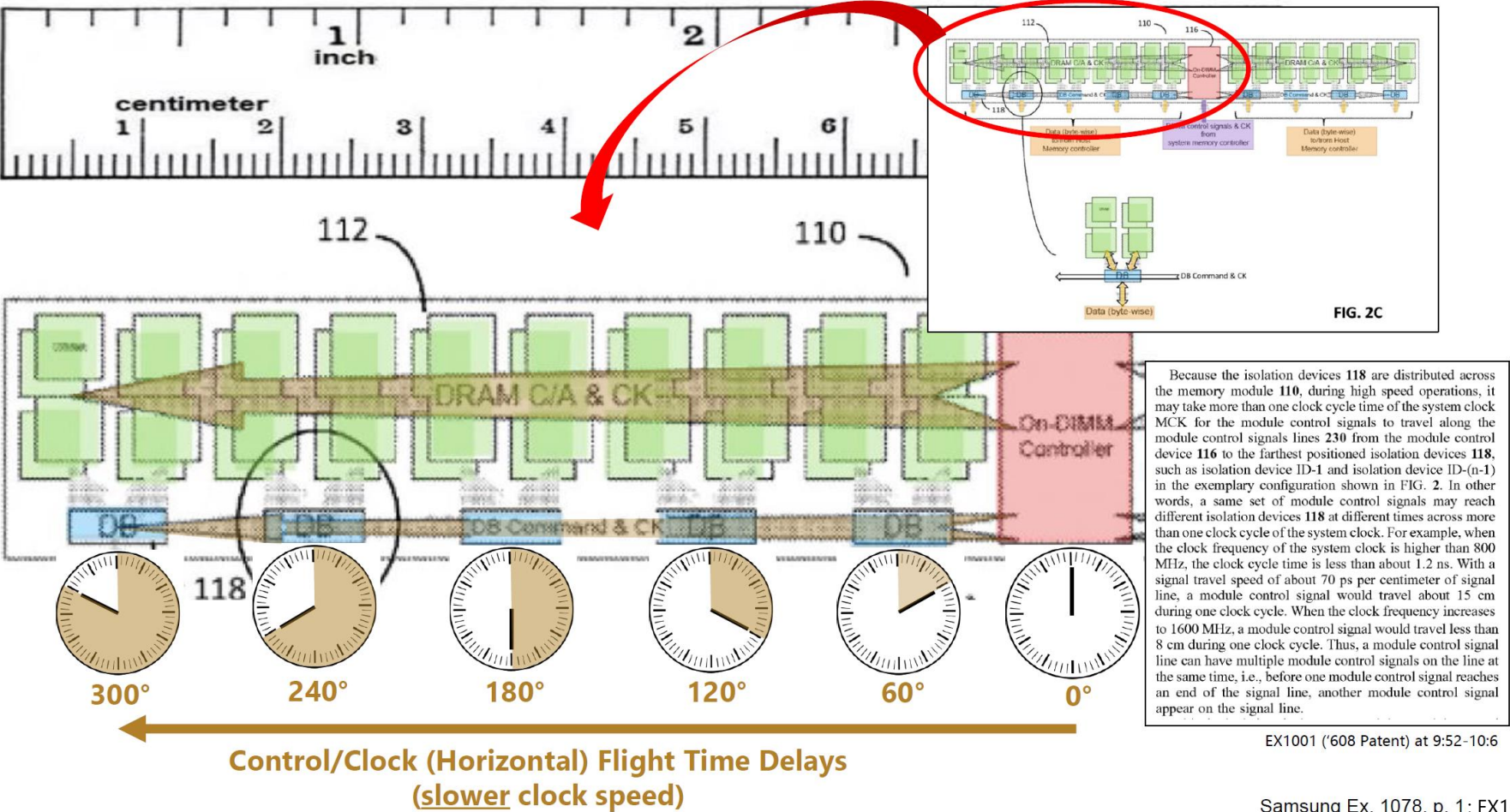
For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and

EX1020, 42



EX1085, 7; EX1074, 79:23-80:14, 89:6-90:9

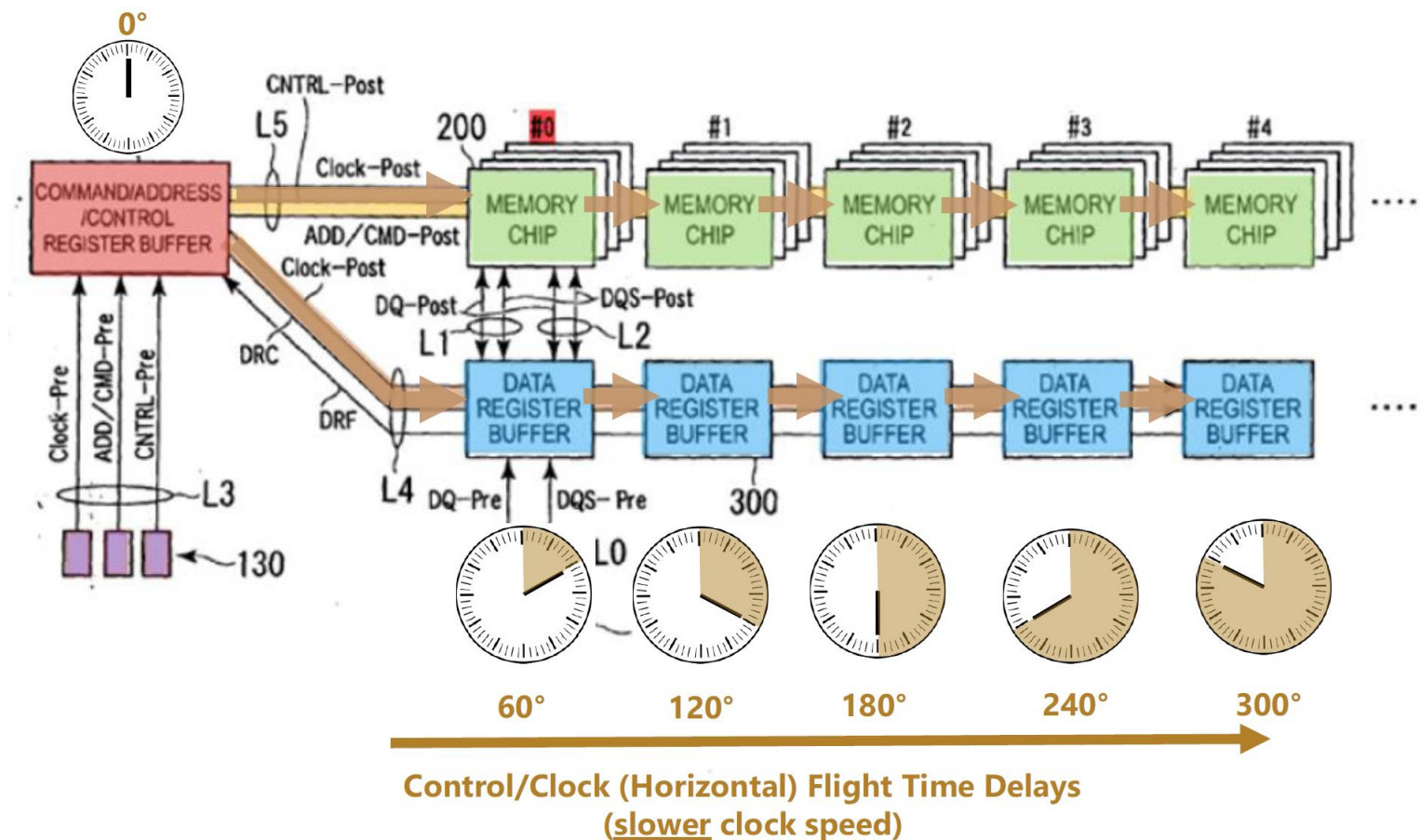
Consistent with JEDEC, the '608 Patent uses DDR3 memory in a “fly-by topology,” resulting in horizontal fly-by delays for commands that needed to be corrected with read/write leveling to unskew the data signals



EX1001 ('608 Patent) at 9:52-10:6

Samsung Ex. 1078, p. 1; EX1074, 66:3-67:18

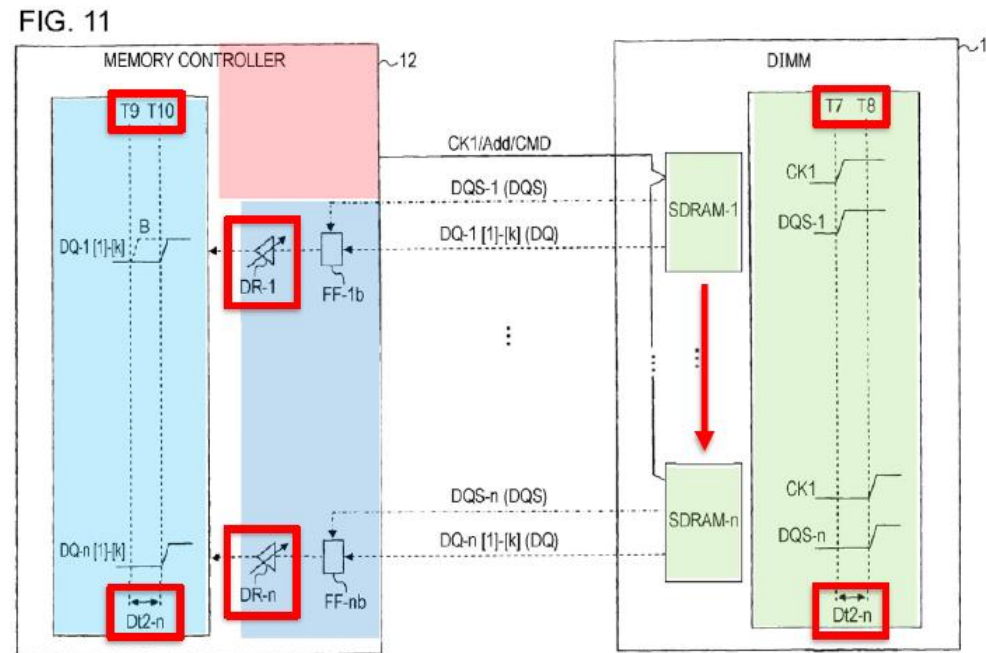
Consistent with JEDEC, Hiraishi used DDR3 memory in a “fly-by topology,” resulting in horizontal fly-by delays for commands that needed to be corrected with read/write leveling to unskew the data signals



EX1079, 1; EX1074, 68:17-69:15

Tokuhiro (U.S. Pat. No. 8,020,022) [EX1006]

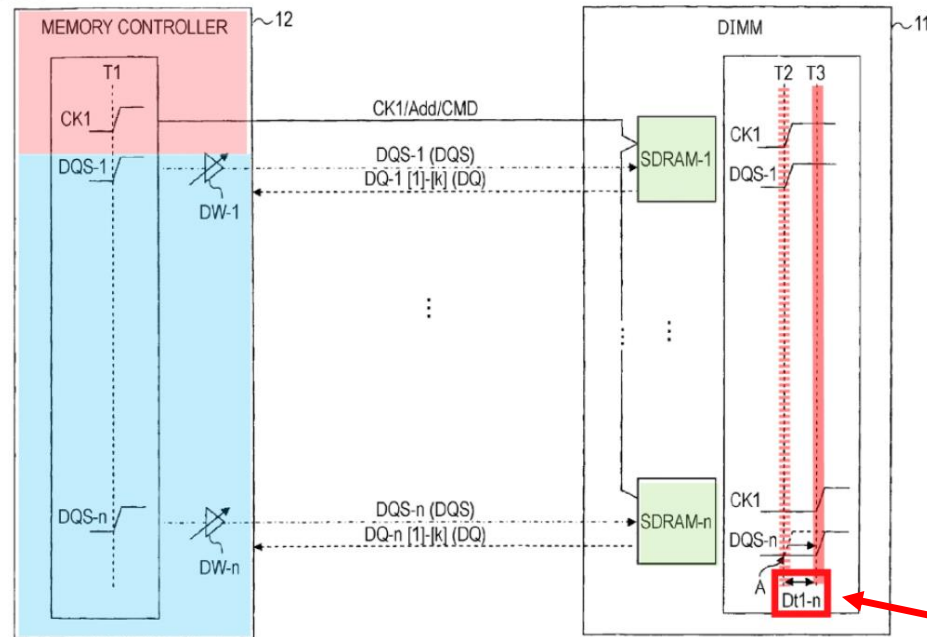
Tokuhiro solves the problem of large fly-by delays (e.g., greater than one clock cycle) by determining a first delay time using the **write** leveling function, and then using that to delay transmission of data during **read** operations (e.g., so all read data arrives at T10)



EX1006 (Tokuhiro), Fig. 11 (annotated)

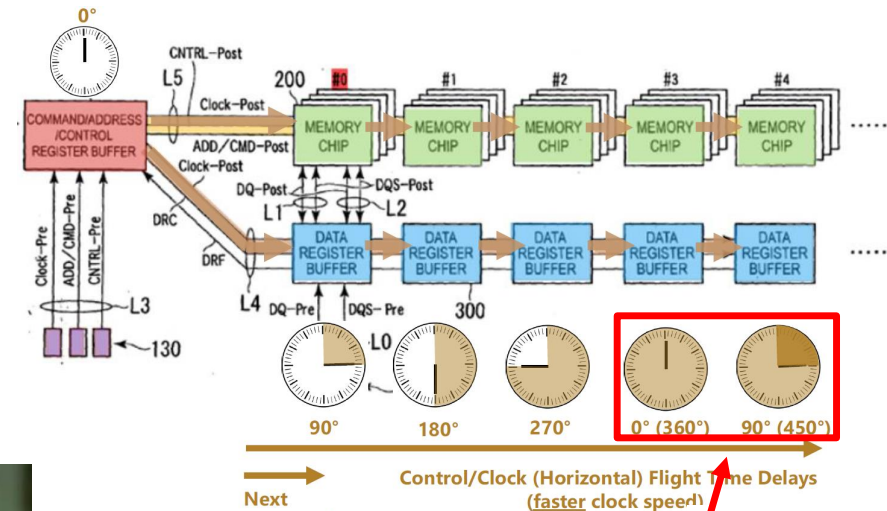
Tokuhiro recognizes fly-by delays greater than one clock cycle and teaches a solution of setting “gradually” longer delays, e.g., 180°, 270°, 360° (not 0°), 450° (not 90°)

FIG. 7



The delay on the order of 1 ns will become greater than a typical data period of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92.

EX1006 at 3:9-12



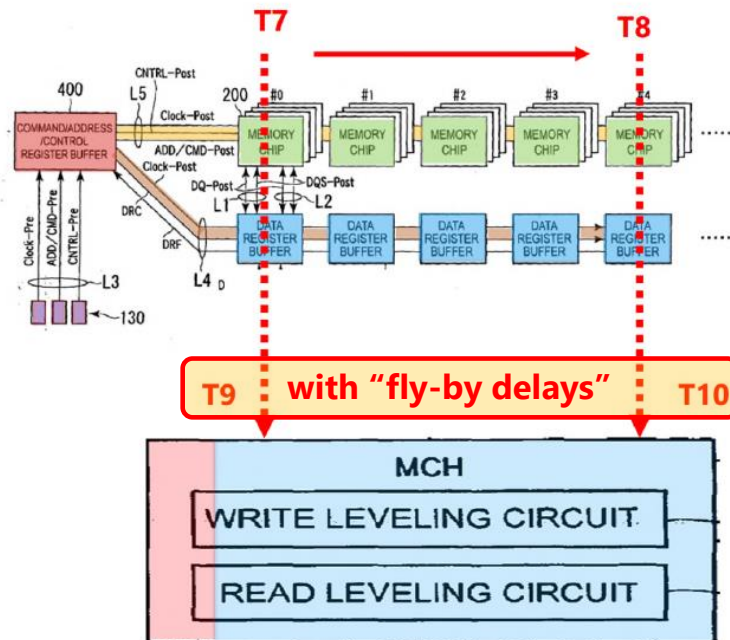
Q. And then if you turn to the next column in the Tokuhiro reference marked as Exhibit 1006 in column 14, starting around line 55, it explains that the delay times DT1-1 to DT1-N corresponding respectively to SDRAM-1 to SDRAM-N, as in Nancy, are set so as to become gradually longer, correct?

A. Yes, that's correct.

EX1074 at 179:6-12

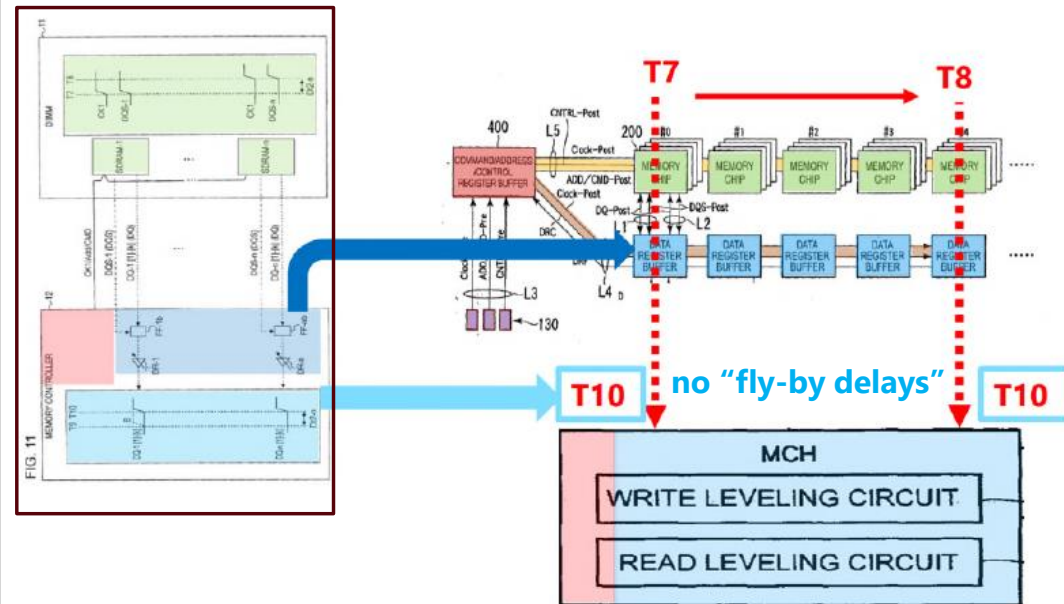
Ground 2: Ground 1 + Tokuhiro — Data Buffers also remove horizontal fly-by delays

Hiraishi alone has horizontal “fly-by delays”
(e.g., read data arriving at T9 to T10)



Ground 2 combination removes the horizontal fly-by delays
(e.g., all read data arriving at T10)

Tokuhiro



Ground 2: Ground 1 + Tokuhiro — Data Buffers also remove horizontal fly-by delays

Hiraishi: Memory module with **data buffers** that adjust **DQ/DQS signals** to remove vertical fly-by delays

+

Butt: Details of buffering and adjusting **DQ/DQS signals** in **data paths**

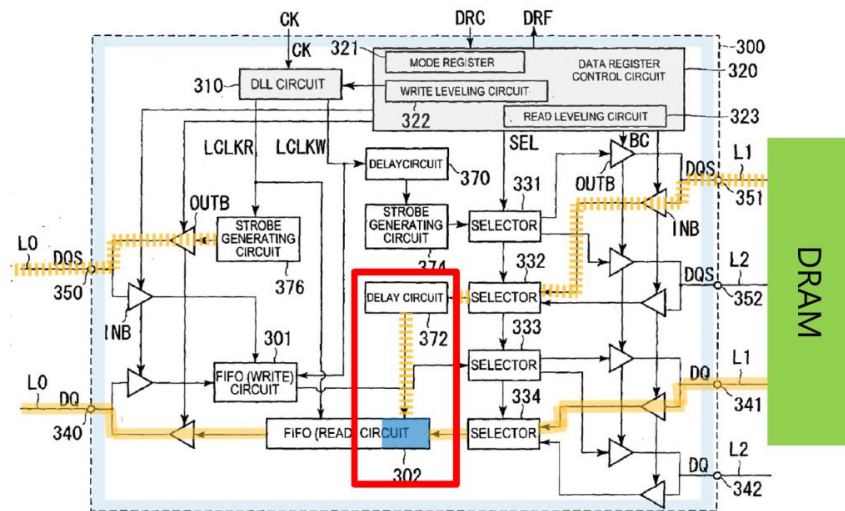
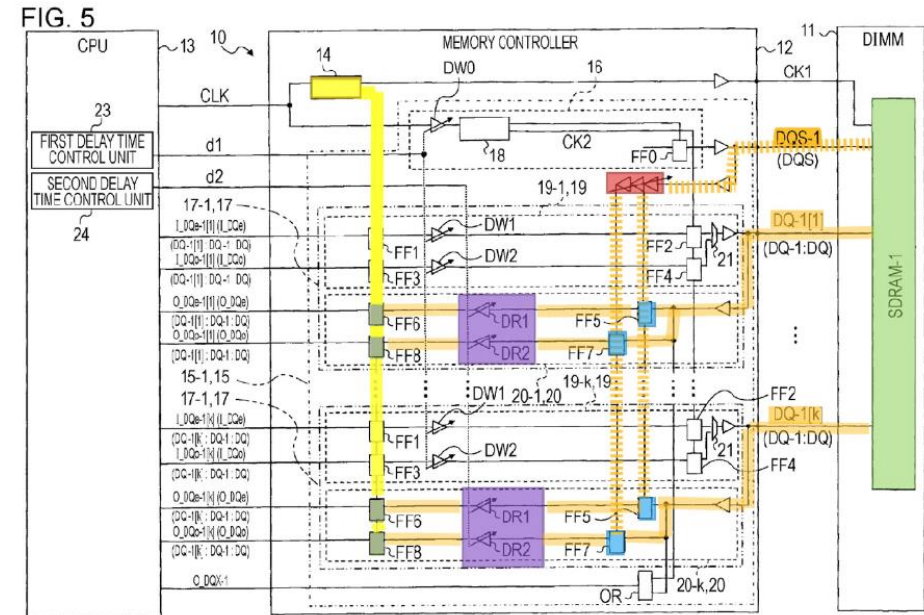


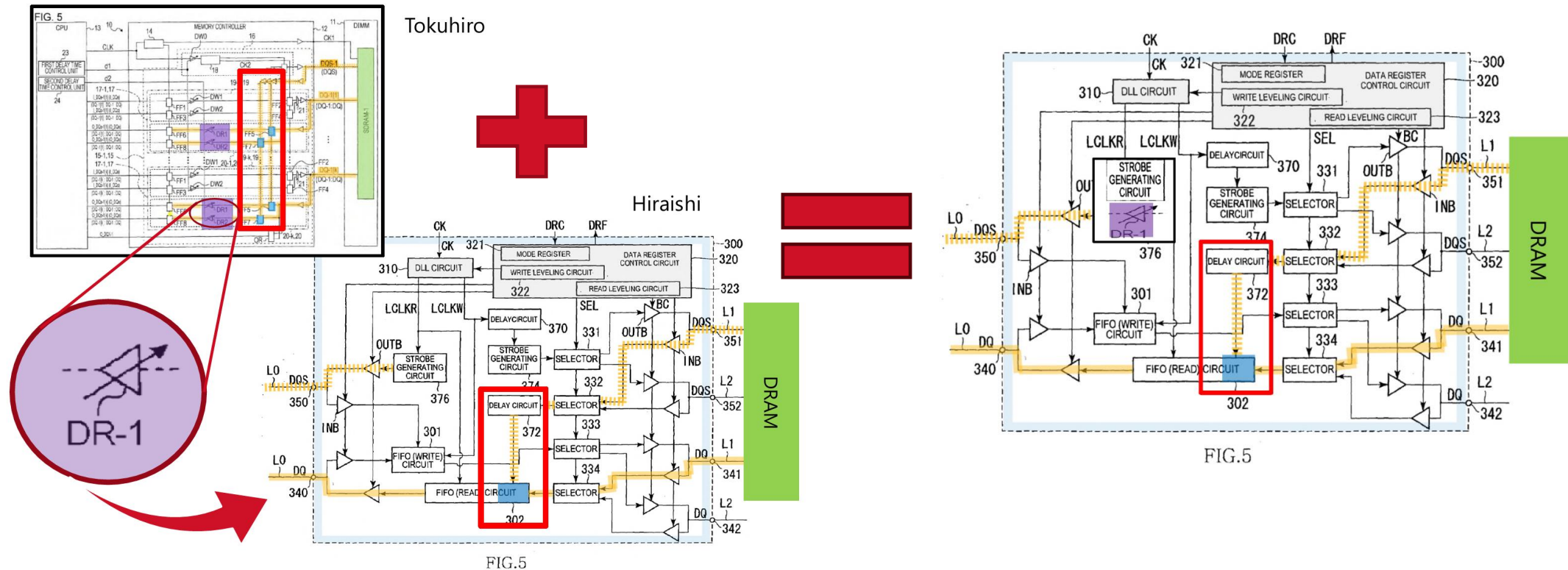
FIG. 5

Tokuhiro: Details of removing horizontal fly-by delays and using write data delays for read data

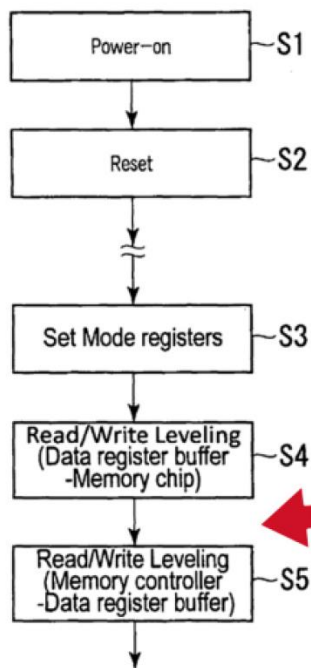


Ground 2: Ground 1 + Tokuhiro — Data Buffers remove horizontal fly-by delays

- Improves efficiency of Hiraishi's module by using write data delays for read data as taught by Tokuhiro
- Removes horizontal fly-by delays on Hiraishi's module using Tokuhiro's technique
- Tokuhiro teaches simple solution for horizontal fly-by delays greater than one clock cycle

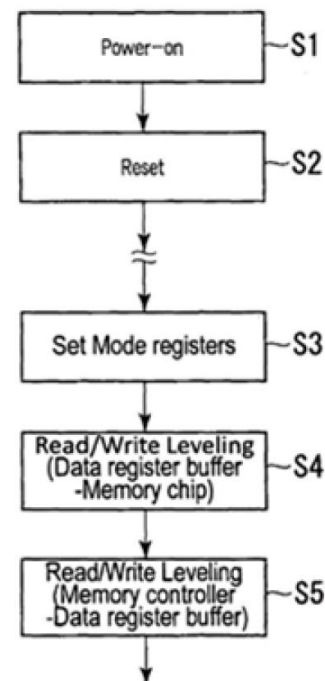


Ground 2: Two ways to set Read delays in **Data Buffers** based on Write delays in the Hiraishi+Tokuhiro combination



- Memory Controller performs write operation;
- **Data Buffers** measure time between write command and corresponding write data;
- **Module Controller** programs additional read delays in **Data Buffers** based on measured times

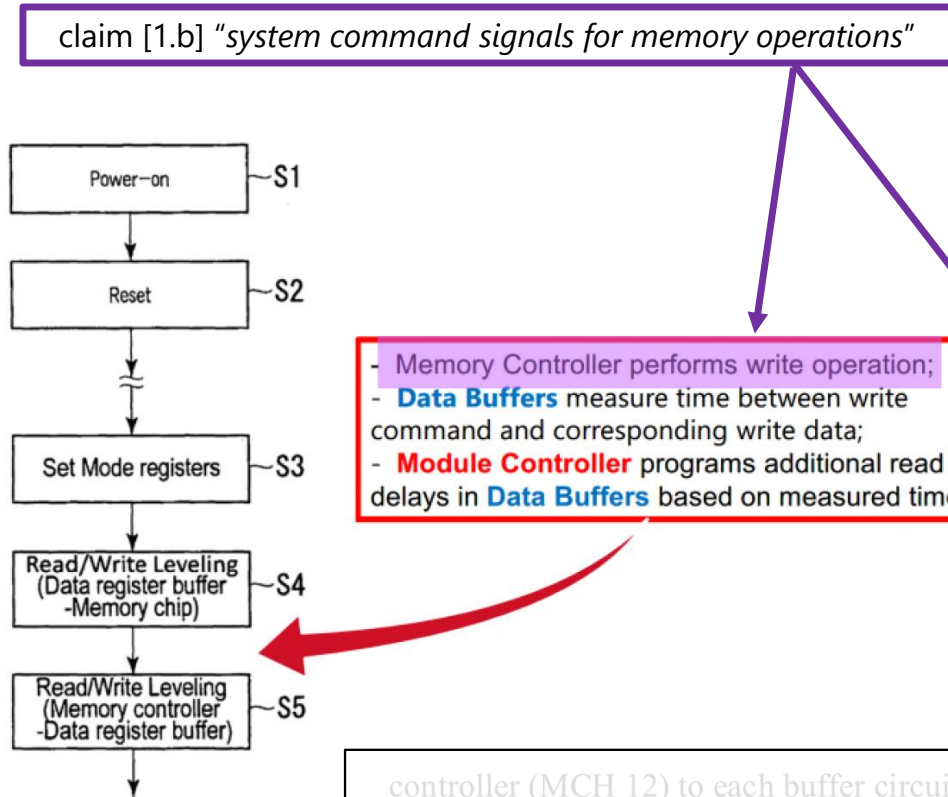
FIG.13



- Between write and read leveling in S5:
 - Memory Controller programs read delays in **Data buffers** based on write delays

FIG.13

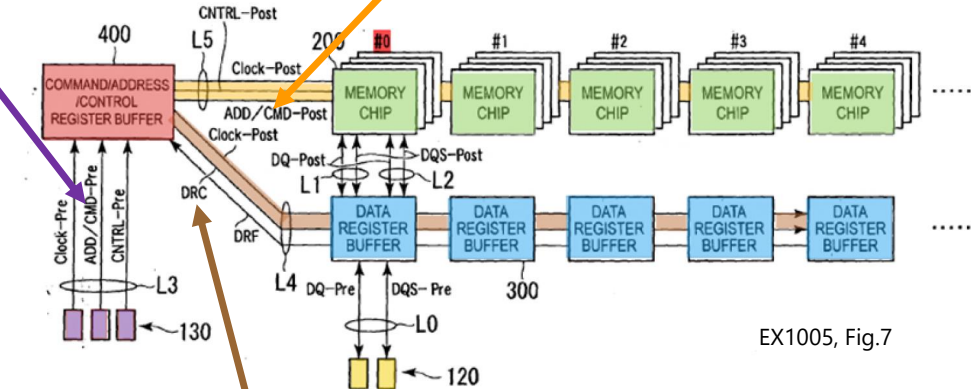
Ground 2: One option is to determine the delay in response to a Write command from the host's memory controller



- Memory Controller performs write operation;
- Data Buffers measure time between write command and corresponding write data;
- Module Controller programs additional read delays in Data Buffers based on measured times

EX1003, ¶291; EX1005, Fig.13. During this operation, a Write command is transmitted from the memory controller to the module controller (command/address/control register buffer 400 receiving "system command signals") which either forwards the write command or sends no-operation commands to the memory devices ("module command signals"). EX1003, ¶291.

Paper 1 (Pet.) at 104

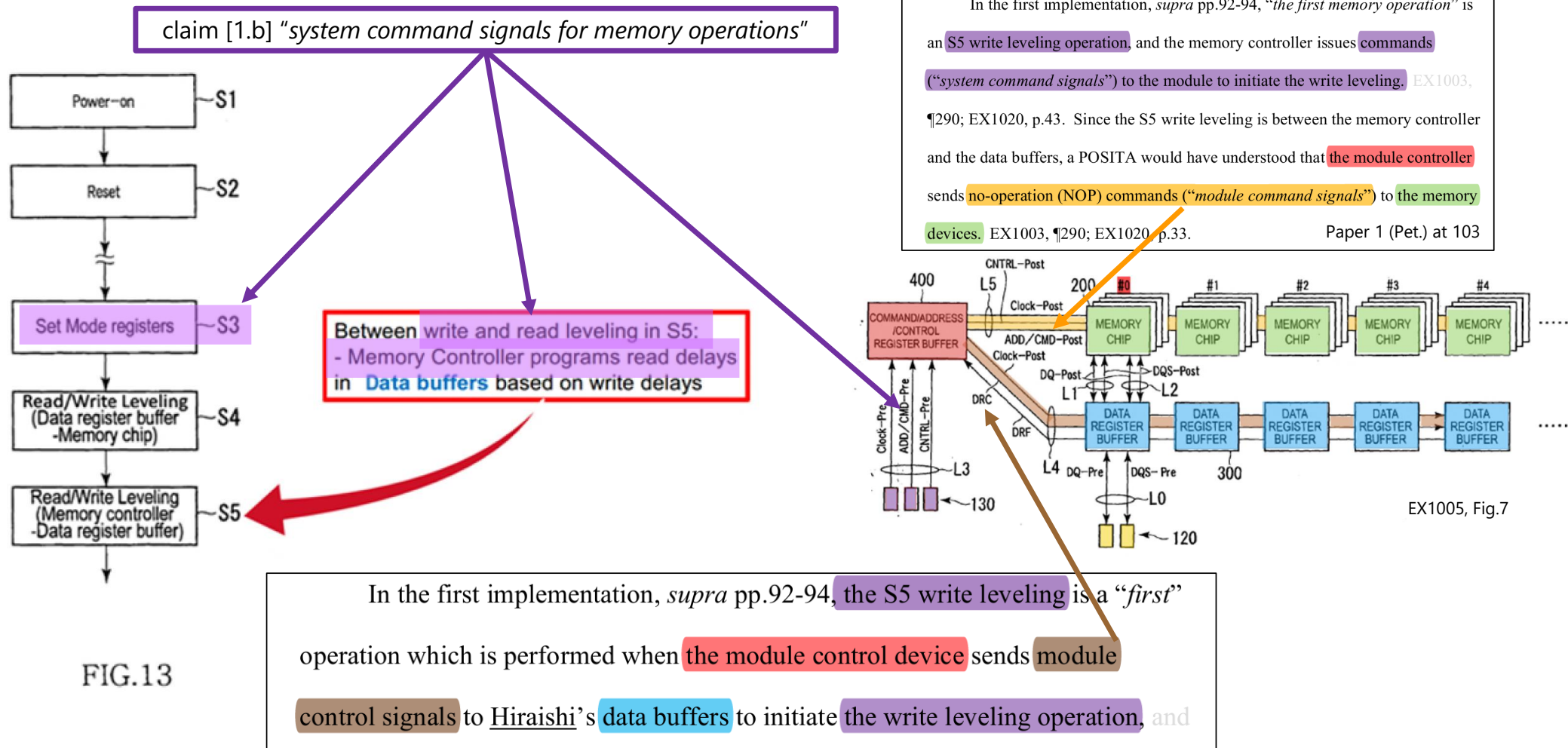


EX1005, Fig.7

controller (MCH 12) to each buffer circuit (300). *Id.* The command/address/control register buffer 400 also transmits the Write command to each buffer circuit.

Paper 1 (Pet.) at 104-105

Ground 2: Another option is to determine the delay in response to the command for (S5) Write Leveling Operations from the host's memory controller



GROUND 2 HAS A “DELAY CIRCUIT” IN THE “DATA PATH,” EVEN UNDER NETLIST’S CONSTRUCTION

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 107

For limitation 1[h] we explained that Petitioner had demonstrated that each buffer circuit includes data paths for transmitting data and strobe signals associated with the first memory operation. See § II.D.3.c; Pet. 29–31 (citing Ex. 1003 ¶¶ 105–108; Ex. 1005 ¶¶ 60, 90, 97, 109–110 Figs. 1, 5, 7). These data paths connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300. Pet. 30–31. Furthermore, we

BAKER BOTTS

Paper 23 (Reply) at 32-33

108

Samsung Electronics Co., Ltd.
Ex. 1059, p. 108

Paper 20 (POR) at 59

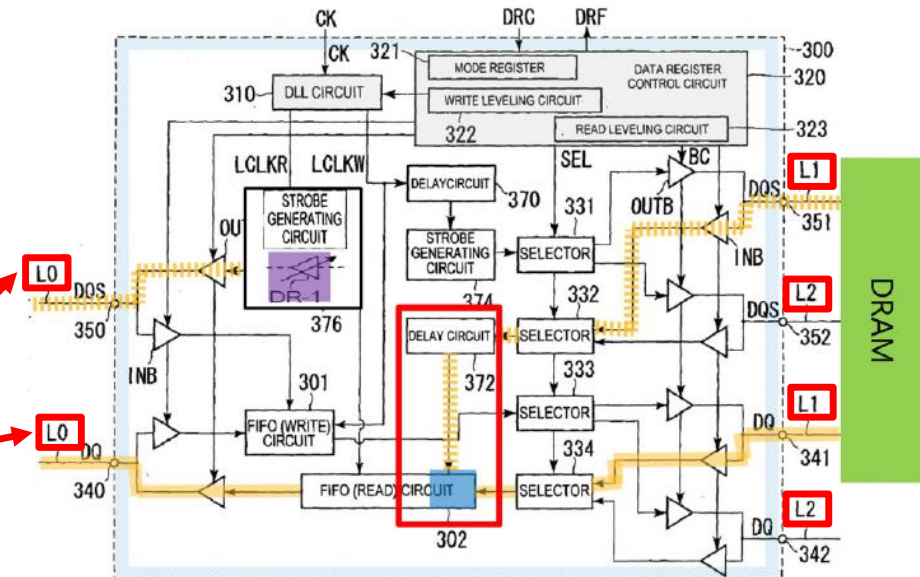
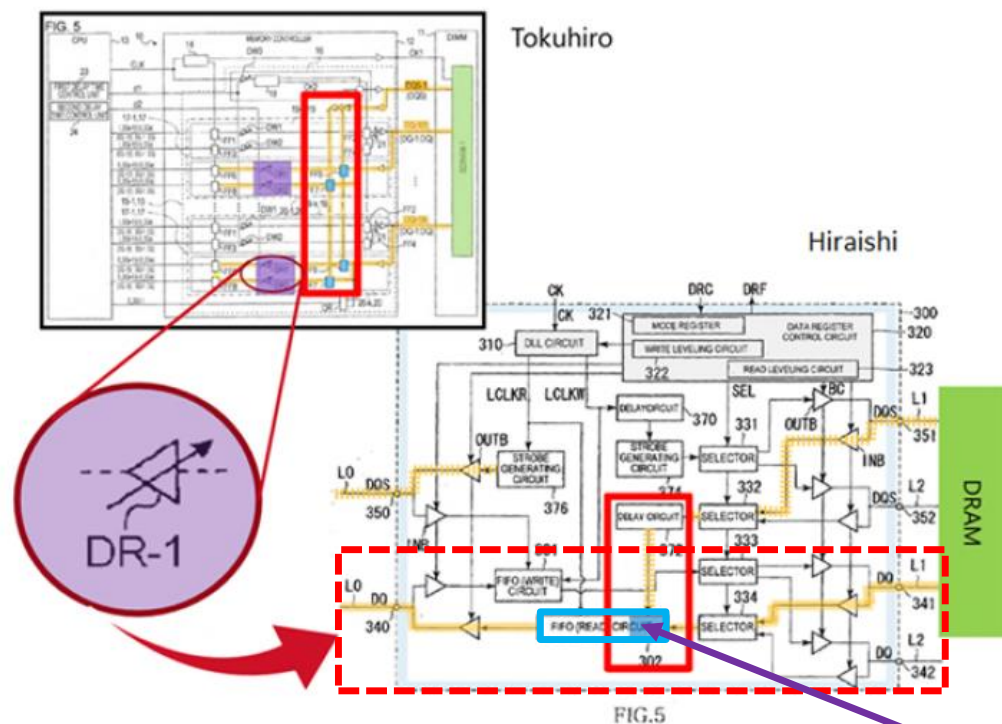


FIG.5

Even under Netlist's construction, Ground 2 discloses a "delay circuit" (e.g., Hiraishi's FIFO or Tokuhiro's DR elements) in the "data path"



[Red dashed box] : "data path" under Netlist's construction
[Blue solid box] : "delay circuit" under Netlist's construction
(FIFO or Tokuhiro's DR elements)



circuitry. "The test for obviousness [however] is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981).
 Petitioner is not required to physically incorporate Tokuhiro's variable delay circuits DR1 and DR2 into [Hiraishi]. Instead, Petitioner proposes to utilize

EX1066 (IPR2022-00236, Paper 34) at 39-40
 (with [Hiraishi] inserted in place of Osana)



Q. And would it be fair to say that a person
of ordinary skill in the art knew how to delay a data
or strobe signal by a predetermined amount?

A. Yes, I think that's fair to say, in
 general.

EX1074 at 164:14-18

EX1020, p.56; EX1006, 18:53-64. Alternatively, delay elements similar to
Tokuhiro's DR elements can be used instead of (or in addition to) Hiraishi's FIFO
circuit for delaying the read data. EX1003, ¶262.

Paper 1 (Pet.) at 90

IPR2022-00236 RESOLVED ISSUES DISPOSITIVE TO GROUND 2

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 110

IPR2022-00236 [EX1066] and -237 relied on equivalent prior art: Tokuhiro [EX1006] + Osanai [EX2004] (same as Hiraishi [EX1005])

- IPR2022-00236's **Tokuhiro** reference [EX1006] is the same reference in this IPR for Grounds 2-3:

The Petition relies on the following references:	
Reference	Exhibit No.
US 2010/0312925A1; filed June 3, 2010; published Dec. 9, 2010 ("Osanai").	1005
US 8,020,022B2; filed Sept. 12, 2008; issued Sept. 13, 2011 (" <u>Tokuhiro</u> ").	1006
US 8,713,379B2; filed Nov. 22, 2011; issued Apr. 29, 2014 ("Takefman")	1007

EX1066 (IPR2022-00236, Paper 34) at 6

- IPR2022-00236's **Osanai** reference [EX2004] is "the same as **Hiraishi** [EX1005, primary reference for all Grounds] in all material respects":

1.	The Primary Reference (<u>Hiraishi</u>) Is the Same as the Primary Reference (<u>Osanai</u>) the Board Considered in Micron -0237
	Osanai from Micron -0237 not only "is related to Hiraishi," (Pet., 113), it is the same as Hiraishi in all material respects , as Samsung's counsel admitted during oral argument in IPR2022-00711 against the related '506 patent ("the '506 IPR").

POPR at 5

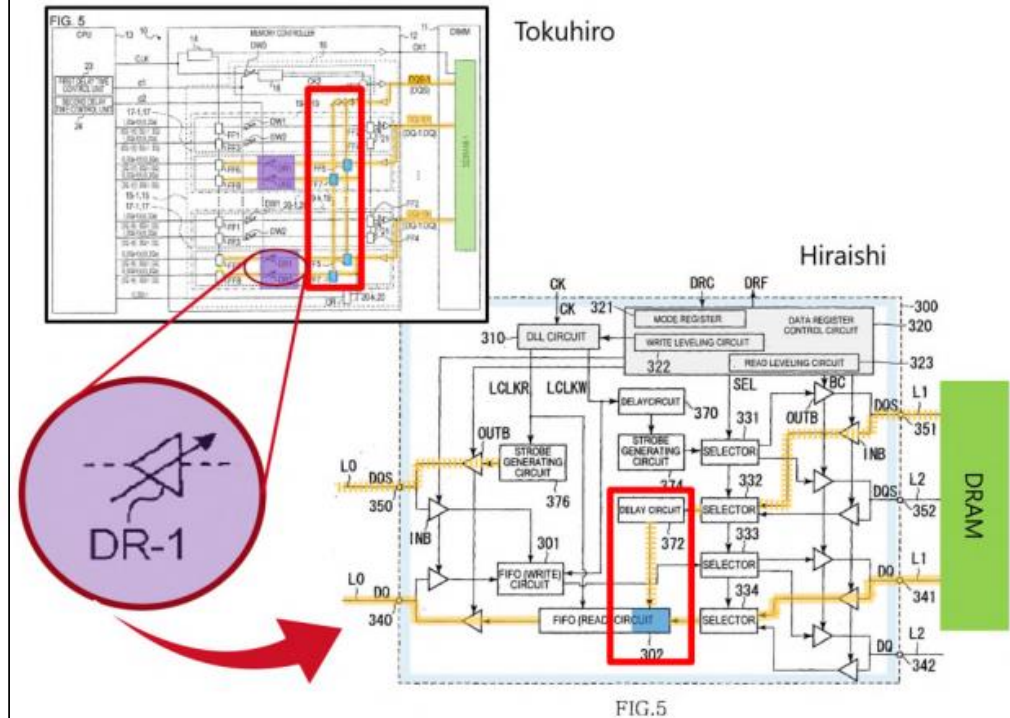
Netlist is estopped by the determination in IPR2022-00236 that a POSITA would have been motivated to combine Tokuhiro's DR-1 delay element with Hiraishi's data buffer with a reasonable expectation of success



Having reviewed the evidence in light of the parties' arguments, we determine that Petitioner has sufficiently demonstrated that one of ordinary skill would have been able to combine [Hiraishi] and Tokuhiro in the way proposed by Petitioner and would have been able to overcome any differences between the two references. Petitioner's proposed modification ...

Petitioner is not required to physically incorporate Tokuhiro's variable delay circuits DR1 and DR2 into [Hiraishi]. Instead, Petitioner proposes to utilize Tokuhiro's teaching of determining the delay for read operations based on the delay calculated during a prior write leveling operation. Pet. 38–39 (citing Ex. 1003 ¶ 126). Petitioner explains that [Hiraishi] includes write leveling operations and that a person of ordinary skill would have been able to modify [Hiraishi]'s write leveling to use Tokuhiro's leveling technique. *Id.* We determine that Petitioner has sufficiently explained the combination of the two references and that one of ordinary skill would have been able to combine the two even with the differences between the two references.

EX1066 (IPR2022-00236, Paper 34) at 38-40
(with [Hiraishi] inserted in place of Osanaï)



IPR2022-00236 rejected Netlist's position (left), and agreed with Samsung's position that a POSITA would have had a reasonable expectation of success combining Tokuhiro and Hiraishi

Netlist's POR, pp. 60, 64	Samsung's Petition, p. 82; Samsung's Reply, pp. 33-34	IPR2022-00236, pp. 38-40 [EX1066]
"A POSA Would Not Have Had a Reasonable Chance of Successfully Achieving the Claimed Invention Based on the Proposed Modification to <u>Hiraishi</u> ...The Added Delay Element is Inoperable" ... "In sum, Petitioner has failed to provide any competent evidence or reasoning that a POSA would have had a reasonable expectation of implementing the claimed delay features because <u>Tokuhiro</u>'s delay element is not provided with any control signal which is required for its algorithm to operate, per <u>Tokuhiro</u>'s express teachings."	"It would have been obvious to a POSITA to implement <u>Tokuhiro</u>'s delay functionality in <u>Hiraishi</u>'s data register buffers, and a POSITA would have had a reasonable expectation of success in doing so." "<u>Hiraishi</u> expressly teaches using the 'data register buffers' to remove delays as part of S4 read/write leveling, ... which the Board has already determined had a reasonable expectation of success with <u>Tokuhiro</u>."	"[W]e determine that Petitioner has sufficiently demonstrated that one of ordinary skill would have been able to combine [<u>Hiraishi</u>] and <u>Tokuhiro</u> in the way proposed by Petitioner and would have been able to overcome any differences between the two references." ... "The test for obviousness [however] is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference.' In re Keller, 642 F.2d 413, 425 (CCPA 1981). Petitioner is not required to physically incorporate <u>Tokuhiro</u>'s variable delay circuits DR1 and DR2 into [<u>Hiraishi</u>]."

IPR2022-00236 rejected Netlist's position (left), and agreed with Samsung's position that a POSITA would have been motivated to combine Tokuhiro and Hiraishi for efficiency

Netlist's POR, pp. 80-81	Samsung's Petition, p. 73; Samsung's Reply, pp. 37-38	IPR2022-00236, p. 41 [EX1066]
"Each of Petitioner's reasons are conclusory and unsupported. ... Thus, Petitioner has not shown that a POSA would have been motivated to undertake the combination." ... "As the combination has been proposed, however, the result would be an increase in the overall time and circuitry required." ... "That these operations are now spread out over nine different components (data buffers) ... necessarily means the number of signaling steps ... would increase, not decrease."	"First motivation: <u>Tokuhiro</u> teaches calculating read delays based on the delays for write operations, which is more efficient than <u>Hiraishi</u>'s technique of performing read leveling independent of the write delays." "Netlist argues that there would be no motivation to combine <u>Hiraishi</u> and <u>Tokuhiro</u> in general ... but the Board has already rejected that argument."	"... Petitioner has sufficiently demonstrated that one of ordinary skill would have been motivated to combine [<u>Hiraishi</u>] and <u>Tokuhiro</u> in the way proposed by Petitioner. Petitioner provides sufficient support for its allegation that one of ordinary skill would have been motivated to combine [<u>Hiraishi</u>] and <u>Tokuhiro</u>." ... "Thus, <u>Tokuhiro</u>'s technique reduces the number of steps because it uses previous measurements and calculations from prior write leveling instead of making additional measurements and calculations to determine the delay for read operations."

IPR2022-00236 rejected Netlist’s position (left), and agreed with Samsung’s position that a POSITA would have been motivated to combine Tokuhiro and Hiraishi on the module

Netlist’s POR, pp. 80-81	Samsung’s Petition, p. 79; Samsung’s Reply, pp. 37-38	IPR2022-00236, p. 39 [EX1066]
“Each of Petitioner’s reasons are conclusory and unsupported. ... Thus, Petitioner has not shown that a POSA would have been motivated to undertake the combination.” ... “Petitioner provides no reason why a POSA would desire to remove fly-by delays on the module side, while a POSA would recognize that the memory controller would remove flyby delays for both write and read (not using different mechanisms for write and read).”	“Second motivation: <u>Tokuhiro</u> provides simple techniques for removing fly-by delays, while <u>Hiraishi</u> does not disclose how its memory controller re-times read data received with fly-by delays” “Netlist argues that there would be no motivation to combine <u>Hiraishi</u> and <u>Tokuhiro</u> in general ... but the Board has already rejected that argument.”	“Petitioner explains that <u>Tokuhiro’s</u> leveling techniques would achieve the benefits of ensuring proper timing of signals even when <u>Tokuhiro’s</u> technique is used for an off module controller.”

A POSITA WOULD HAVE BEEN ABLE TO
COMBINE GROUND 1 WITH TOKUHIRO

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 116

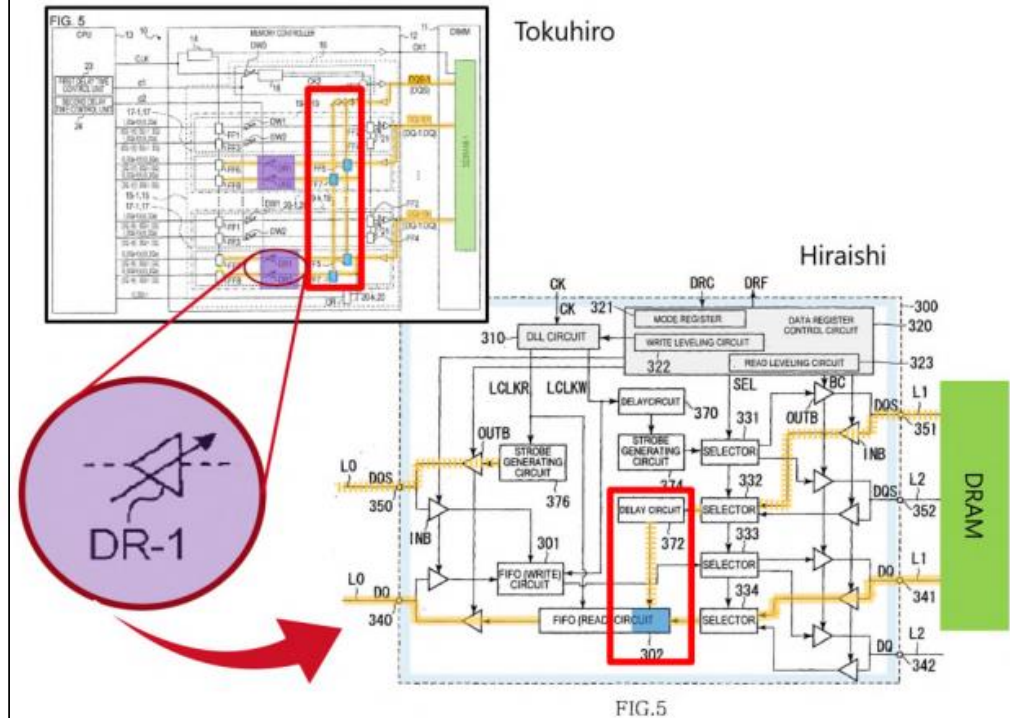
A POSITA would have been motivated to combine Tokuhiro's DR-1 delay element with Hiraishi's data buffer with a reasonable expectation of success



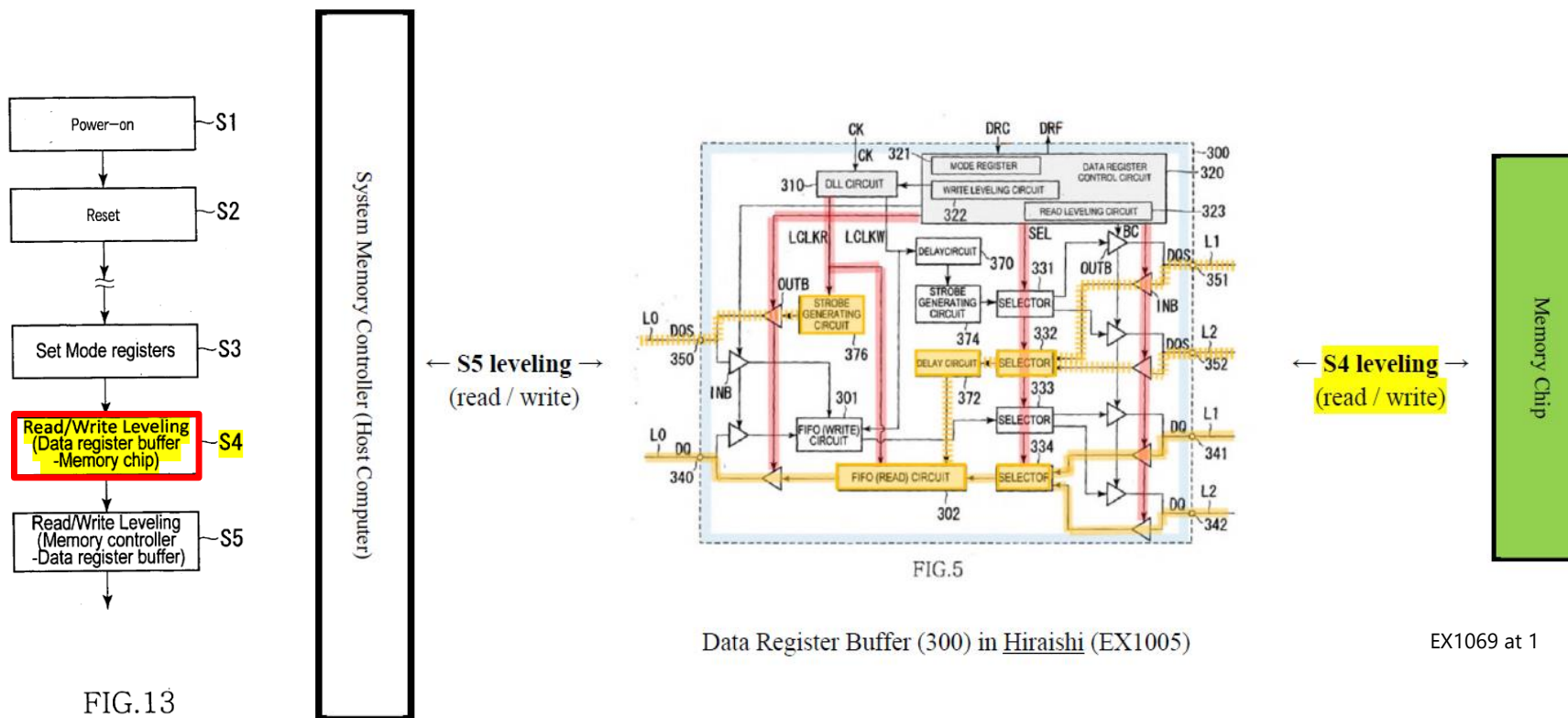
Having reviewed the evidence in light of the parties' arguments, we determine that Petitioner has sufficiently demonstrated that one of ordinary skill would have been able to combine [Hiraishi] and Tokuhiro in the way proposed by Petitioner and would have been able to overcome any differences between the two references. Petitioner's proposed modification ...

Petitioner is not required to physically incorporate Tokuhiro's variable delay circuits DR1 and DR2 into [Hiraishi]. Instead, Petitioner proposes to utilize Tokuhiro's teaching of determining the delay for read operations based on the delay calculated during a prior write leveling operation. Pet. 38–39 (citing Ex. 1003 ¶ 126). Petitioner explains that [Hiraishi] includes write leveling operations and that a person of ordinary skill would have been able to modify [Hiraishi]'s write leveling to use Tokuhiro's leveling technique. *Id.* We determine that Petitioner has sufficiently explained the combination of the two references and that one of ordinary skill would have been able to combine the two even with the differences between the two references.

EX1066 (IPR2022-00236, Paper 34) at 38-40
(with [Hiraishi] inserted in place of Osana)



Netlist's argument that delays would only be removed by the memory controller as part of S5 read/write leveling ignores Hiraishi's express teaching that delays should also be removed in the data buffers as part of S4 read/write leveling



IPR2022-00711 rejected Netlist's argument that the combination would not work due to the lack of express disclosure of some control signals in Hiraishi's Figure 5

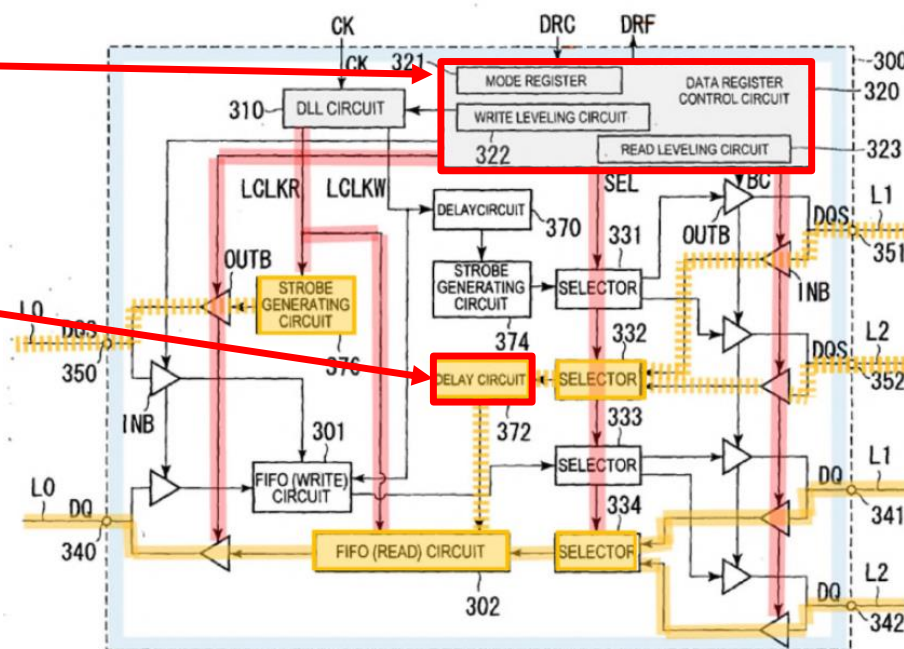


various reasons. PO Resp. 33–40. For example, Patent Owner argues that “Hiraishi’s data register control circuit 320 (which includes the read leveling circuit 323) is neither physically nor functional[ly] connected to the delay circuit 372” and, therefore, that read leveling circuit 323 would not be able to control delay circuit 372 to adjust the strobe timing based on the teachings of Butt. PO Resp. 35–38; see also PO Resp. 28–32 (contending that read leveling circuit 323 does not control delay circuit 372). Patent Owner also

...
We disagree with Patent Owner’s arguments. As an initial matter, the Federal Circuit has

consistently held . . . that “[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.”

MCM Portfolio LLC v. Hewlett-Packard Co., 812 F.3d 1284, 1294 (Fed. Cir. 2015) (quoting *In re Keller*, 642 F.2d 413, 425 (CCPA 1981)). Thus, **Petitioner is not required to show a physical combination of two systems.**



Netlist's expert admitted that lack of similar control signals in Netlist's own figure does not prevent a Skilled Artisan from understanding how the control signals work

Q. And Figure 15 of the '608 patent doesn't expressly show any control input signal to the tri-state buffer 1580, but it'll be reasonable for a person of ordinary skill in the art to understand how and when to enable and disable the tri-state buffer 1580; is that fair?

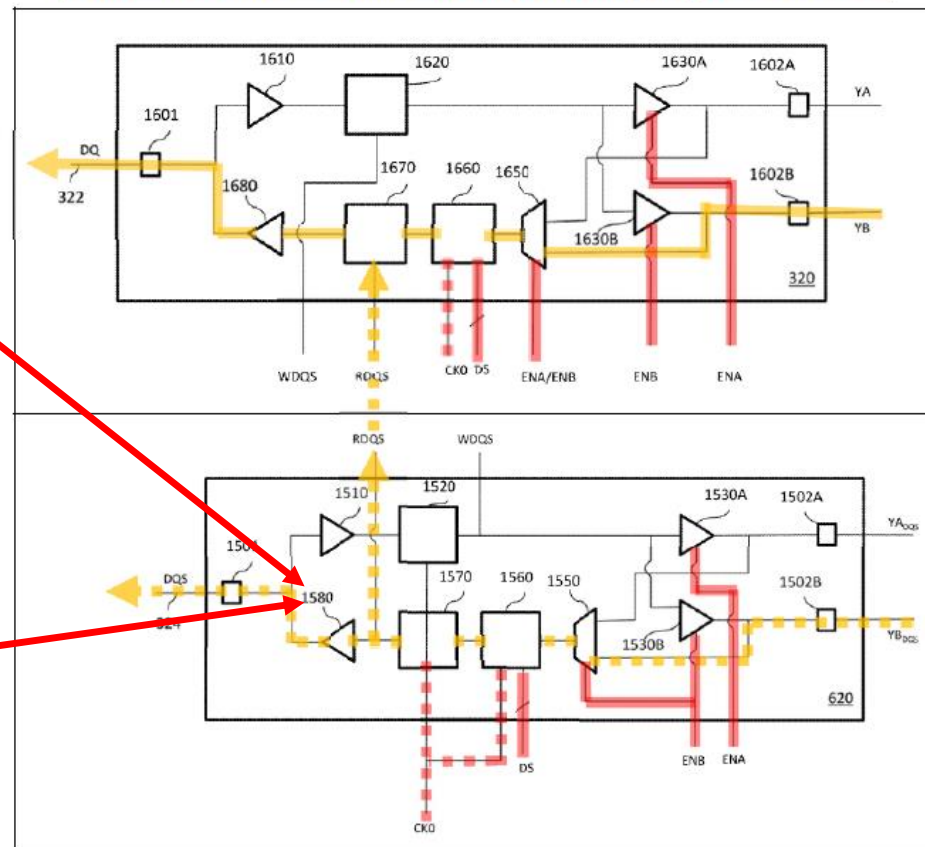
A. I think that that's fair, yes.

Q. And although it's not shown in Figure 15 of the '608 patent, a person of ordinary skill in the art would understand that during a write operation, that you would want to have a control signal that disables the tri-state buffer 1580 to avoid potential conflicts with the incoming strobe signal and also for the benefit of conserving power; is that fair?

A. Yes, that's fair.

EX1074 at 150:2-8, 157:9-16

Read direction — '608 Patent (EX1001) Figures 16 & 15



EX1080 at 1

Netlist's argument that a DQS strobe signal from DR1 cannot replace Hiraishi's original clock signal LCLKR to sample the Read FIFO 302 is another improper "bodily incorporation" argument

In sum, Petitioner fails to provide any motivation for the further modification of using the newly created DQS from DR1 in the strobe generating circuit 376 (that is off the data path) to clock out the read data from the FIFO instead of following the known approach of using a local clock signal. Petitioner's piecemeal modifications of Hiraishi are clearly the product of impermissible hindsight, and do not support obviousness.

Paper 20 (POR) at 70

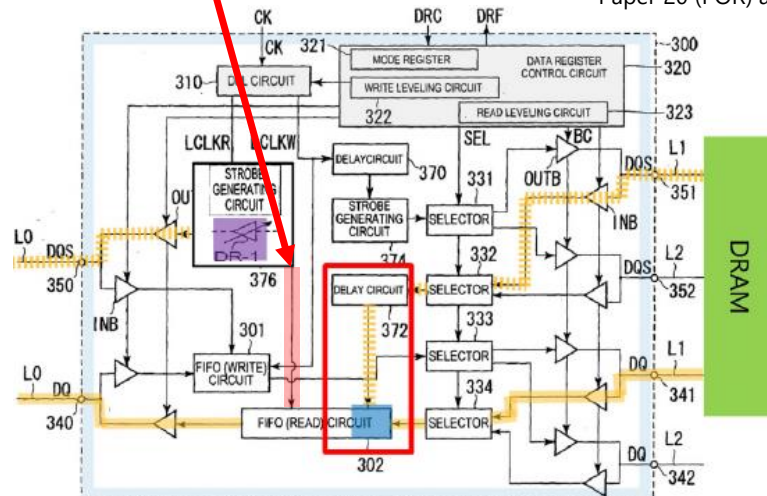


FIG. 5



circuitry. "The test for obviousness [however] is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference." *In re Keller*, 642 F.2d 413, 425 (CCPA 1981). Petitioner is not required to physically incorporate Tokuhiro's variable delay circuits DR1 and DR2 into Hiraishi. Instead, Petitioner proposes to utilize Tokuhiro's teaching of determining the delay for read operations based on the delay calculated during a prior write leveling operation. Pet. 38–39 (citing Ex. 1003 ¶ 126). Petitioner explains that Hiraishi includes write leveling operations and that a person of ordinary skill would have been able to modify Hiraishi's write leveling to use Tokuhiro's leveling technique. *Id.* We determine that Petitioner has sufficiently explained the combination of the two references and that one of ordinary skill would have been able to combine the two even with the differences between the two references.

EX1066 (IPR2022-00236, Paper 34) at 39–40
(with Hiraishi inserted in place of Osana)

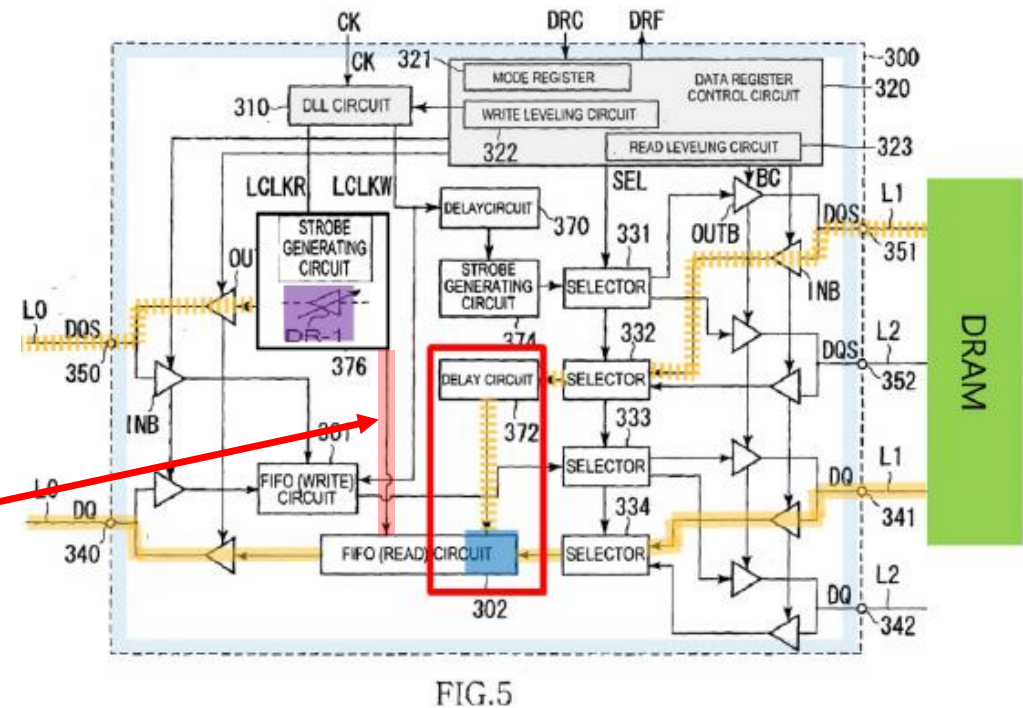
Netlist's expert admitted that either a DQS strobe signal or a clock signal can be used to control sampling



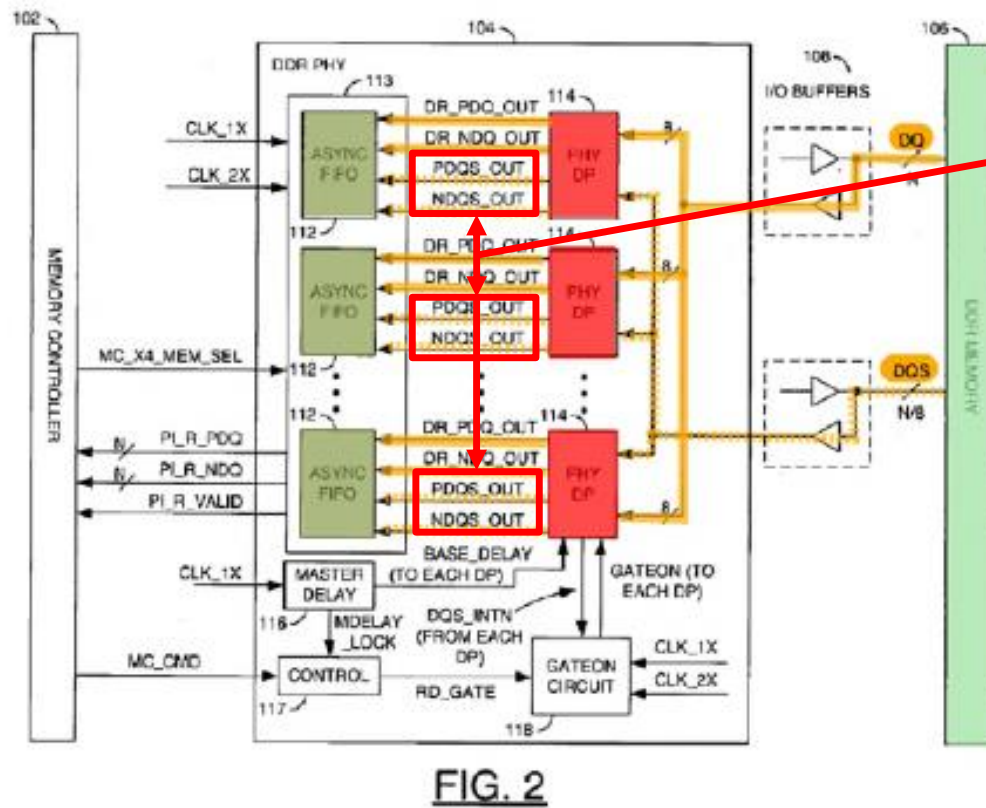
Q. And a person of ordinary skill in the art would understand how to sample using a clock signal such as CK0 and how to sample using a strobe signal such as RDQS; is that fair?

A. Depending on the context of what they wanted to sample, yes, clocks are often used for sampling and, similarly, strobe signals are often used to control sampling.

EX1074 at 154:15-22



Butt also confirms that a DQS strobe signal can be used to clock a FIFO



Q. And in particular, as explained by paragraph 19 of the Butt reference marked as Exhibit 1029, the read data DR_PDQ_out and DR_NDQ_out are written to the FIFOs 112 in response to the strobe signals PDQS_out and NDQS_out, correct?

A. Yes. It says that that read data is generally written into the FIFO based on those DQS signals.

EX1074 at 182:9-16

[0019] The FIFOs 112 are generally configured to transfer the read data DQ from the read data strobe (or DQS) domain to the CLK_1X domain for presentation to the memory controller 102. The read data DR_PDQ_OUT and DR_NDQ_OUT are generally written to the FIFOs 112 in response to (e.g., clocked by) the signals PDQS_OUT and NDQS_OUT, respectively). The memory controller 102 may be configured to read the data DQ (e.g., via signals PI_R_PDQ and PI_R_NDQ) from the FIFOs 112 in response to the clock signal CLK_1X. In one example, the FIFOs 112 may be implemented as eight words deep.

EX1029 at 1[0019]

Butt teaches using a GATEON signal to block the preamble/postamble of the DQS strobe signal, enabling the gated DQS strobe signal (e.g., PDQS_OUT or NDQS_OUT) to clock the FIFO

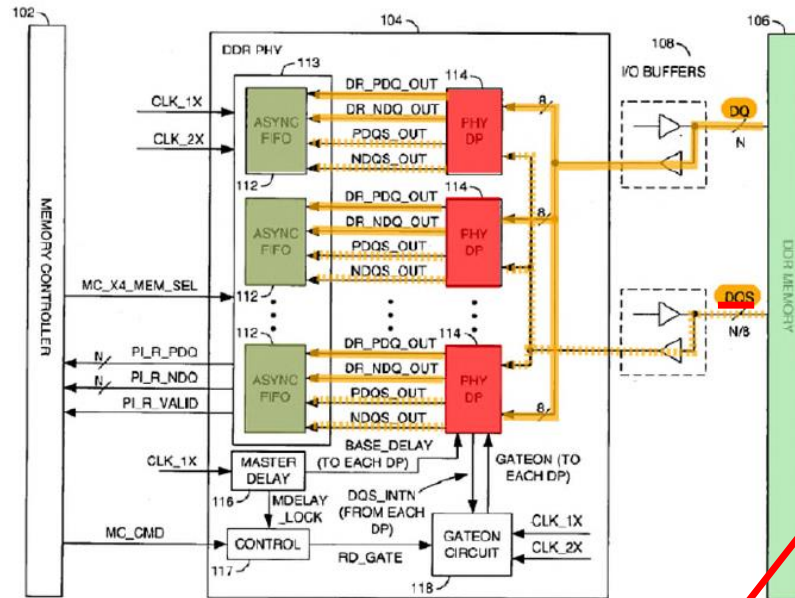
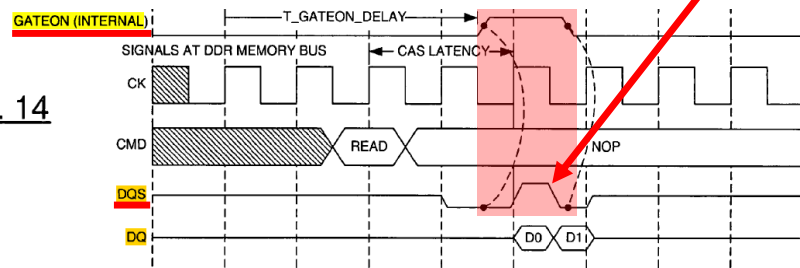


FIG. 2

FIG. 14



EX1084 at Fig. 14



Q. As explained in paragraph 24 of the Butt reference marked as Exhibit 1029, the GATEON signals may be used to gate the DQS data strobe signals, correct?

A. Yes. It says:

EX1074 at 184:1-5

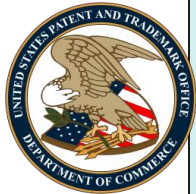
controller 102. The read data DR_PDQ_OUT and DR_NDQ_OUT are generally written to the FIFOs 112 in response to (e.g., clocked by) the signals PDQS_OUT and NDQS_OUT, respectively). The memory controller 102

EX1029 at ¶[0019]

mented. A read GATEON training process, described in a co-pending application Ser. No. _____ (Attorney Docket No. 1496.00419), filed Jul. 1, 2005, which is hereby incorporated by reference in its entirety, may be executed before the DQ-DQS timing adjustment of the present invention is made (except at power-up or reset, when a default slave delay may be loaded before read GATEON training proceeds).

EX1029 at ¶[0047]

Netlist is improperly distinguishing the prior art based on technical details (e.g., the difference between DQS strobe and CK clock signals) neither claimed nor disclosed in the '608 Patent



"[T]he reasonable expectation of success requirement refers to the likelihood of success in combining references *to meet the limitations of the claimed invention*." *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367 (Fed. Cir. 2016) (emphasis added). ... Thus, "the ['160] patent itself does not disclose the level of detail that [Patent Owner] would have us require of the prior art." See *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1570 (Fed. Cir. 1997).

Samsung Elecs. Co. v. Netlist, Inc., IPR2022-001427, Paper 48, 35-36 (PTAB Apr. 1, 2024) (emphasis added)

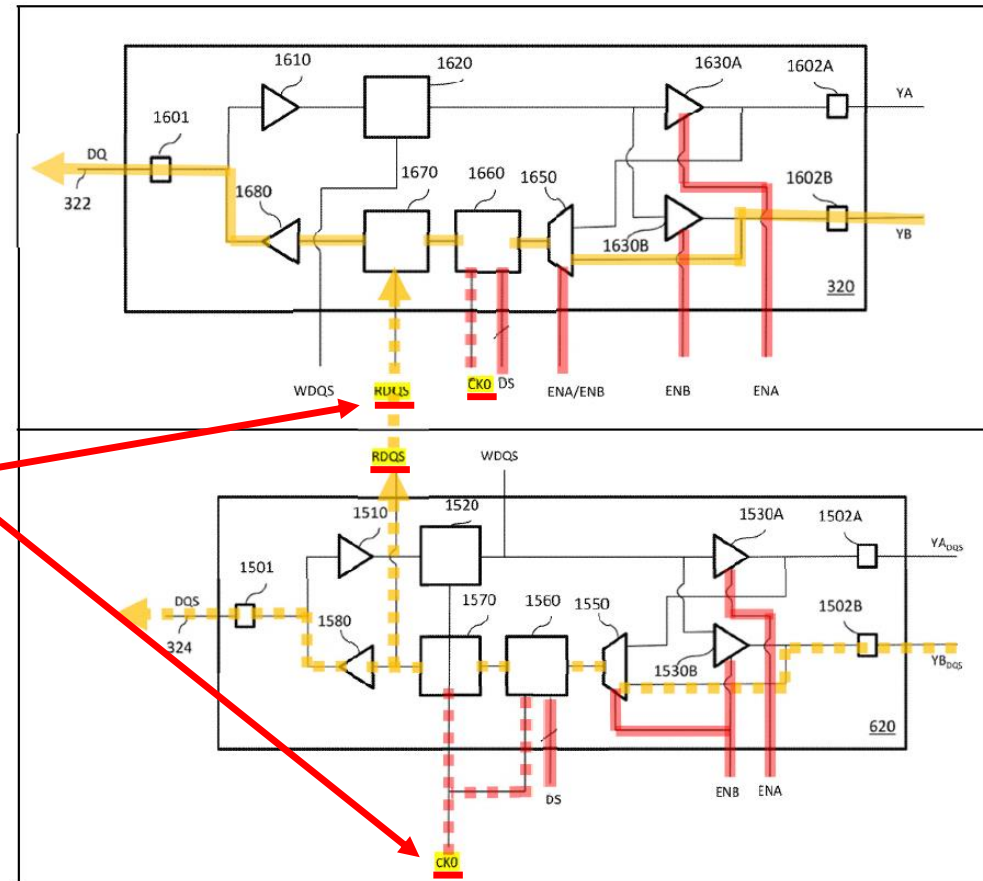
Q. The '608 patent does not go into any further details about how the sampler circuit 1570 uses the clock signal CK0 to sample signals or how the sampler circuit 1670 uses the RDQS strobe signal to sample signals; is that fair?

A. Not that I'm aware of, but it's a 43-page patent. If I was aware of something as I sit here, I would certainly mention it.

changing. But as you said, or suggested, the disclosure of how those various samplers work is pretty thin.



Read direction — '608 Patent (EX1001) Figures 16 & 15



EX1074 at 154:23-155:12, 158:24-159:1

DEMONSTRATIVE EXHIBIT - NOT EVIDENCE

A POSITA WOULD HAVE BEEN MOTIVATED
TO COMBINE GROUND 1 WITH TOKUHIRO

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 126

IPR2022-00236 rejected Netlist's position (left), and agreed with Samsung's position that a POSITA would have been motivated to combine Tokuhiro and Hiraishi for efficiency

Netlist's POR, pp. 80-81	Samsung's Petition, p. 73; Samsung's Reply, pp. 37-38	IPR2022-00236, p. 41 [EX1066]
"Each of Petitioner's reasons are conclusory and unsupported. ... Thus, Petitioner has not shown that a POSA would have been motivated to undertake the combination." ... "As the combination has been proposed, however, the result would be an increase in the overall time and circuitry required." ... "That these operations are now spread out over nine different components (data buffers) ... necessarily means the number of signaling steps ... would increase, not decrease."	"First motivation: <u>Tokuhiro</u> teaches calculating read delays based on the delays for write operations, which is more efficient than <u>Hiraishi</u>'s technique of performing read leveling independent of the write delays." "Netlist argues that there would be no motivation to combine <u>Hiraishi</u> and <u>Tokuhiro</u> in general ... but the Board has already rejected that argument."	"... Petitioner has sufficiently demonstrated that one of ordinary skill would have been motivated to combine [<u>Hiraishi</u>] and <u>Tokuhiro</u> in the way proposed by Petitioner. Petitioner provides sufficient support for its allegation that one of ordinary skill would have been motivated to combine [<u>Hiraishi</u>] and <u>Tokuhiro</u>." ... "Thus, <u>Tokuhiro</u>'s technique reduces the number of steps because it uses previous measurements and calculations from prior write leveling instead of making additional measurements and calculations to determine the delay for read operations."

IPR2022-00236 rejected Netlist’s position (left), and agreed with Samsung’s position that a POSITA would have been motivated to combine Tokuhiro and Hiraishi on the module

Netlist’s POR, pp. 80-81	Samsung’s Petition, p. 79; Samsung’s Reply, pp. 37-38	IPR2022-00236, p. 39 [EX1066]
“Each of Petitioner’s reasons are conclusory and unsupported. ... Thus, Petitioner has not shown that a POSA would have been motivated to undertake the combination.” ... “Petitioner provides no reason why a POSA would desire to remove fly-by delays on the module side, while a POSA would recognize that the memory controller would remove flyby delays for both write and read (not using different mechanisms for write and read).”	“Second motivation: <u>Tokuhiro</u> provides simple techniques for removing fly-by delays, while <u>Hiraishi</u> does not disclose how its memory controller re-times read data received with fly-by delays” “Netlist argues that there would be no motivation to combine <u>Hiraishi</u> and <u>Tokuhiro</u> in general ... but the Board has already rejected that argument.”	“Petitioner explains that <u>Tokuhiro’s</u> leveling techniques would achieve the benefits of ensuring proper timing of signals even when <u>Tokuhiro’s</u> technique is used for an off module controller.”

Netlist's expert admitted that JEDEC's DDR3 standard adopted a "fly-by topology," resulting in horizontal fly-by delays for commands that needed to be corrected with read/write leveling to unskew the data signals

Q. And then write leveling can be used to account for the skew in the other direction, which is when the memory controller is sending data signals to the DDR3 memory module, which is going to have the address, control, and clock signals calling the DDR3 memory module in a fly-by topology, meaning, that there will be fly-by delays for those address controlling clock signals; is that fair?

A. Those address, control, and clock signals will be skewed, and write leveling can be used to allow the system to operate correctly in the context, in the face of those skews.

so, conceptually, it's -- read leveling is a technique for responding or counteracting the fly-by effect by adding some timing variation.

That can be done in a number of places.

As I suggested, it could be done in the DRAMs. It could be done in the memory controller. If there's a buffer, a data buffer between the DRAMs and the memory controller, it can be done in the data buffer.

EX1074 at 80:7-14, 89:23-90:9

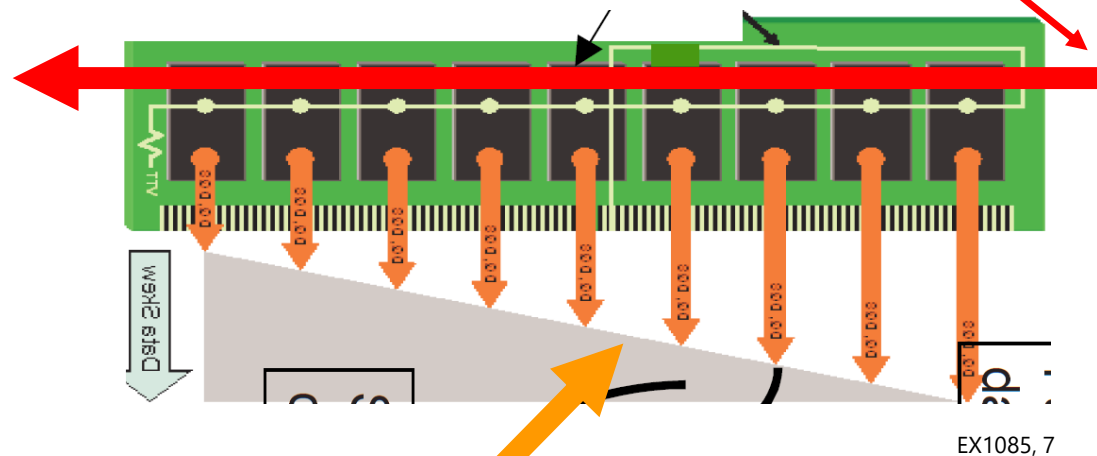


JEDEC DDR3 SDRAM

4.8 Write Leveling

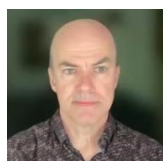
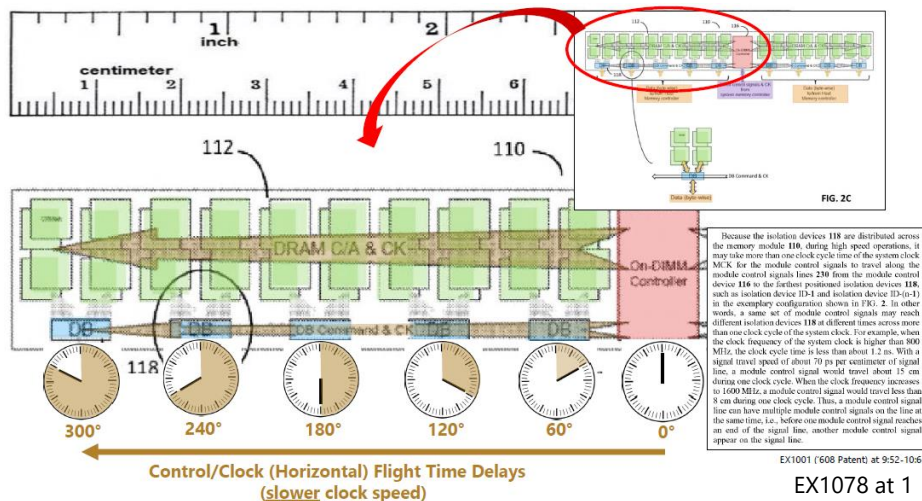
For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and

EX1020, 42



Skewed data
signals, requiring
read/write leveling

Netlist's expert also admitted that both the '608 Patent and Hiraishi have a fly-by topology, resulting in horizontal fly-by delays for commands



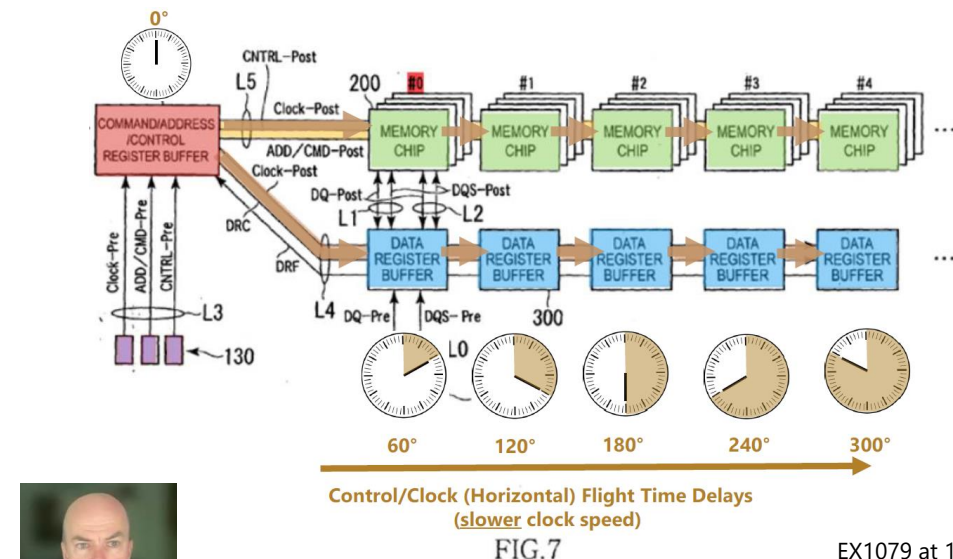
As shown in FIG. 2C, in certain embodiments, the control circuit 116 transmits registered C/A and clock signals to the memory devices 112, and transmits module control signals and a registered clock signal (or module clock signal) to the isolation devices 118, in a fly-by configuration. As the speed

EX1001 at 8:22-26

Q. And would it be fair to say that this is trying to illustrate the concept of the fly-by arrangements in the horizontal direction that you were discussing a moment ago?

A. I think that's a fair characterization of what I expect this -- a fair characterization that it represents the behavior of the fly-by phenomenon that we were discussing previously.

EX1074 at 67:11-18



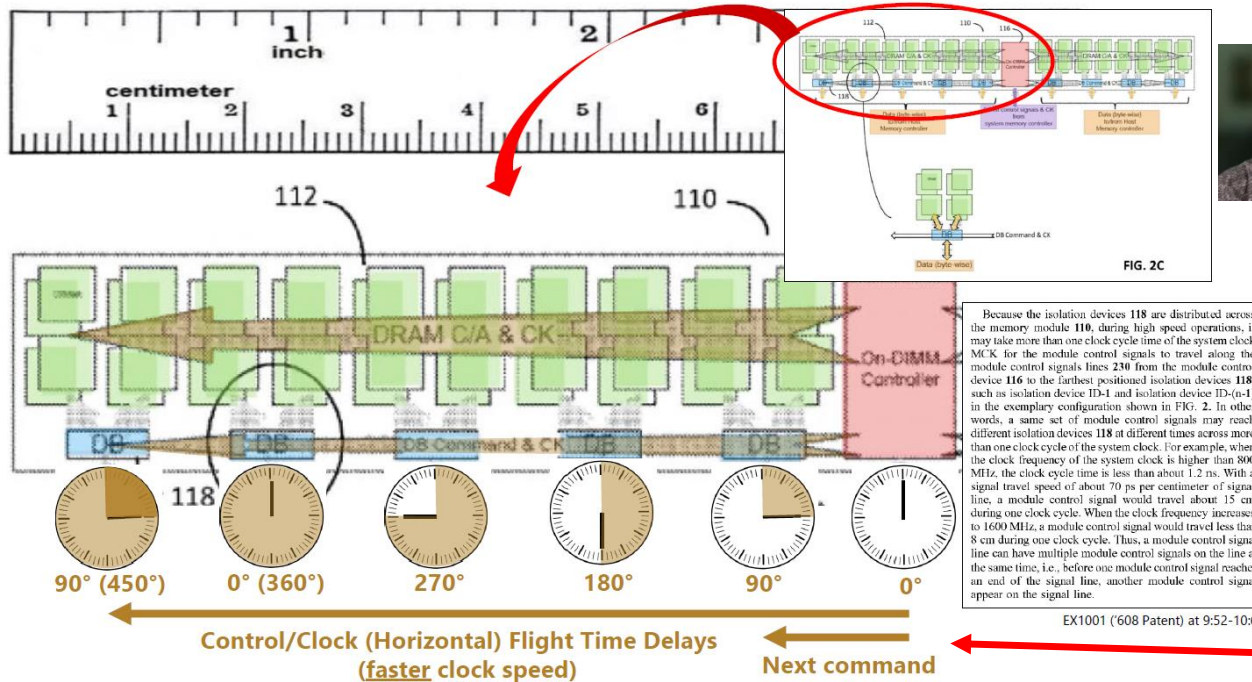
Q. And the fly-by arrangement in Hiraishi as illustrated in Exhibit 1079 is generally similar to the fly-by arrangement in the '608 patent, as illustrated in Exhibit 1078 that we just looked at; is that fair?

MR. LINDSAY: Objection. Form.

THE WITNESS: I think that it's generally similar, yes.

EX1074 at 69:8-15

Netlist's expert also admitted that faster DDR3 clock speeds (e.g., less than 1ns) may result in horizontal fly-by delays greater than one clock cycle



EX1078 at 2; EX1074, 60:23-64:24, 67:19-68:16

JEDEC DDR3 SDRAM Standard

DDR3-2133				Unit
11-11-11	12-12-12	13-13-13	14-14-14	
		0.938		ns

EX2015 at 141



Q. So the fastest clock period shown on this page of the DDR3 standard marked as Exhibit 2015 is less than one nanosecond, which is less than one billionths of a second, correct?

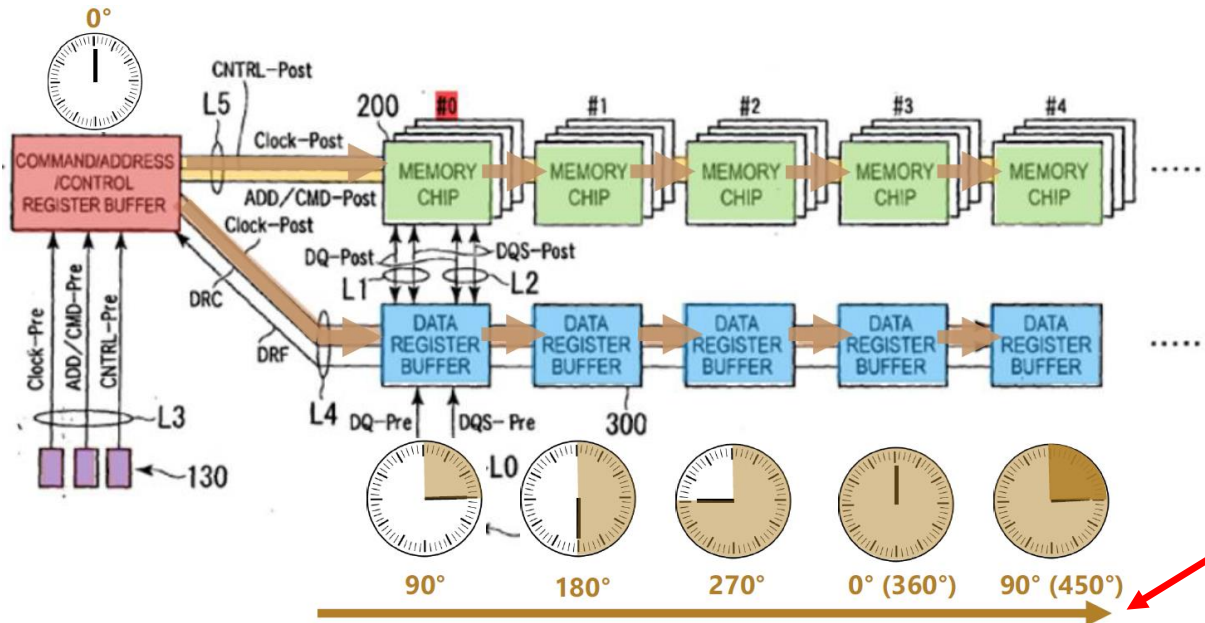
A. Yes, that appears to be correct.

Q. And so according to the '608 patent marked as Exhibit 1001, as you get to these faster clock speeds, which I believe are consistent with some of the clock speeds we were looking at for DDR3 memory devices, a module control signal line can have multiple module control signals on the line at the same time, i.e., before one module control signal reaches an end of the signal line, another module control signal appears on the signal line, correct?

A. Yes, I see that it says that.

EX1074 at 54:11-15, 62:3-12

Netlist's expert agreed that Hiraishi, which "focused on DDR3," would eventually face horizontal fly-by delays greater than one clock cycle, as a consequence of the faster clock speeds



Control/Clock (Horizontal) Flight Time Delays (faster clock speed) EX1079 at 2

FIG.7

The delay on the order of 1 ns will become greater than a typical data period of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92.

EX1006 (Tokuhiro) at 3:9-12

JEDEC **DDR3** SDRAM Standard

DDR3-2133				Unit
11-11-11	12-12-12	13-13-13	14-14-14	
0.938				ns

EX2015 at 141



Q. And so to be clear, Netlist did not invent two clock signals going in the horizontal direction on a memory module at the same time; instead, that is a consequence of the physics of clock signals as they get faster and faster as standardized by JEDEC; is that fair?

THE WITNESS: It's a consequence of the signals getting faster and faster, and then

period. Whereas, page 2 of Exhibit 1079 illustrates the concept of the faster clock speed where a second clock signal is sent out on the line before the first clock signal has reached the furthest memory chip in the furthest data register buffer; is that fair?

A. I think that's fair. However, I don't ...

Q. But Hiraishi certainly does talk about this fly-by arrangement for the memory chips and the data registry buffer, and a person of ordinary skill in the art would understand that concept, correct?

A. Yes. My recollection is that I think they were focused on DDR3 where a lot of these issues were not fundamentally present as a problem, but they were anticipated as becoming a problem eventually.

EX1074 at 69:20-70:14, 244:8-16 (objections omitted)

Tokuhiro teaches a solution to fly-by delays greater than one clock cycle, which is not disclosed by Hiraishi, thus providing a motivation to combine the two references



And that could be extended. If it requires multiple CLK cycles in -- you know, Hiraishi doesn't teach that. But I think one of ordinary skill could extend this using other references to assist in order to help understand how -- you know, a way to do that. But you could extend it to more than a CLK cycle with -- with further information.

Q. Is that -- are you -- you said with other references. Would Tokuhiro be an example of another reference that would suggest delays of greater than one CLK cycle?

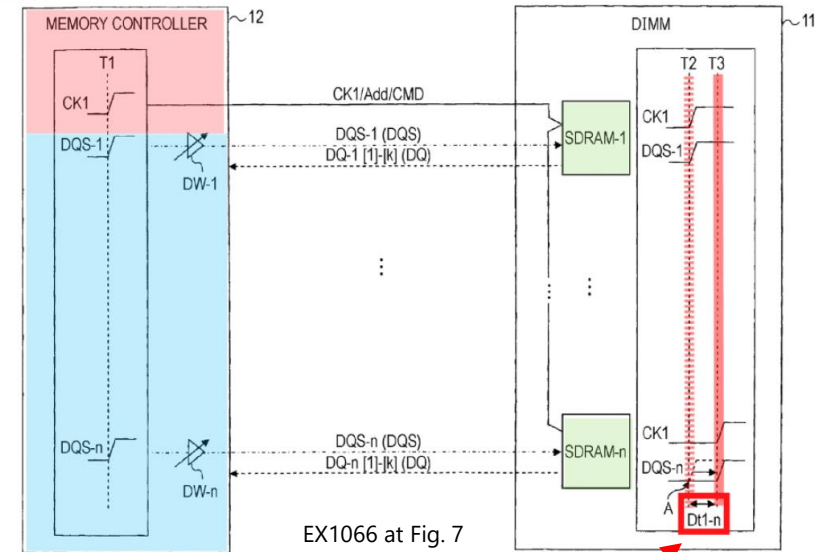
A. Tokuhiro would help and Giovanni would help also.

EX2012 at 80:4-16

during the adjustment process. In particular, if the fly-by delay separation between the clock signal and the data-strobe signal exceeds one clock period, the above-described timing adjustment process will adjust the phase relationship properly, but the timing adjustment may be off by a multiple of a clock period.

EX1024 (Giovanni) at 5:25-31

FIG. 7



EX1066 at Fig. 7



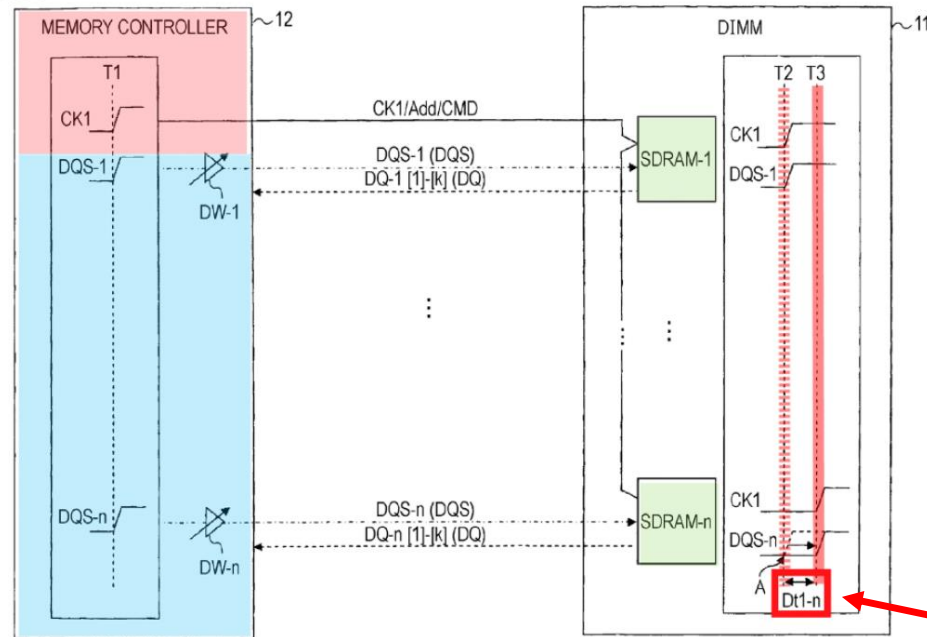
Q. And then if you turn to the next column in the Tokuhiro reference marked as Exhibit 1006 in column 14, starting around line 53, it explains that the delay times DT1-1 to DT1-N corresponding respectively to SDRAM-1 to SDRAM-N, as in Nancy, are set so as to become gradually longer, correct?

A. Yes, that's correct.

EX1074 at 179:6-12

Tokuhiro recognizes fly-by delays greater than one clock cycle and teaches a solution of setting “gradually” longer delays, e.g., 180°, 270°, 360° (not 0°), 450° (not 90°)

FIG. 7



The delay on the order of 1 ns will become greater than a typical data period of the DDR3 memory interface, at minimum 0.625 ns, so that the delay may affect in reading data from the SDRAM 92.

EX1006 at 3:9-12

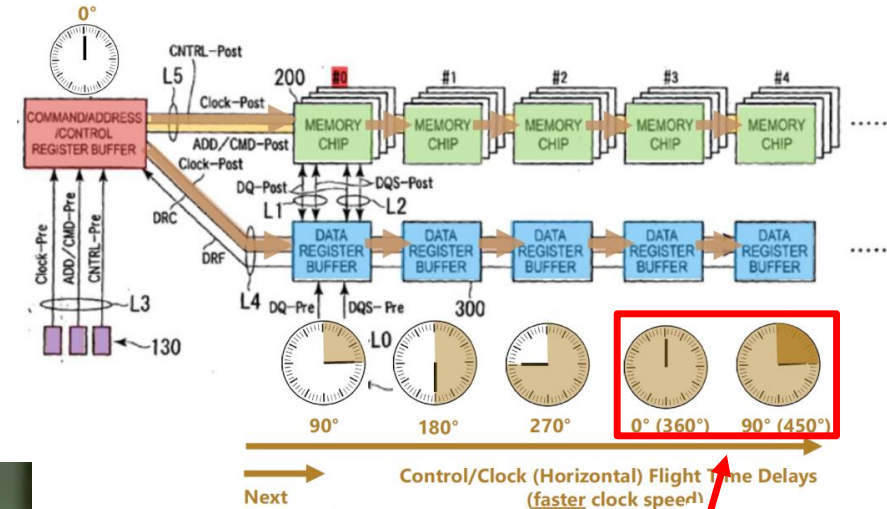


FIG. 7

EX1079 at 2

Q. And then if you turn to the next column in the Tokuhiro reference marked as Exhibit 1006 in column 14, starting around line 55, it explains that the delay times DT1-1 to DT1-N corresponding respectively to SDRAM-1 to SDRAM-N, as in Nancy, are set so as to become gradually longer, correct?

A. Yes, that's correct.

EX1074 at 179:6-12

Netlist's "space-constrained" argument is meritless because Hiraishi's data buffer already has a read/write leveling circuit, so adding Tokuhiro's functionality would require limited changes

A POSA would understand that the memory controller, being on the motherboard, is far less space-constrained than the memory module, as Dr. Wedig confirmed in the related '506 IPR. EX2016, 143:5-144:2; EX2013, ¶179. Moreover, Dr. Wedig confirmed that the JEDEC standards "specify pretty exacting what the size of the memory module should be," but do not prescribe dimensions for the size of the memory controller. EX2016, 94:11-22; EX2016, 142:15-24. Thus, the last place a POSA would be motivated to add extra logic and circuitry would be to a component (here, the data buffer) which is competing with the memory devices for limited space. See *id.* The limited space coupled with intense computing is also detrimental to heat dissipation. EX2013, ¶179; EX2017 (electronic cooling).

Paper 20 (POR) at 76

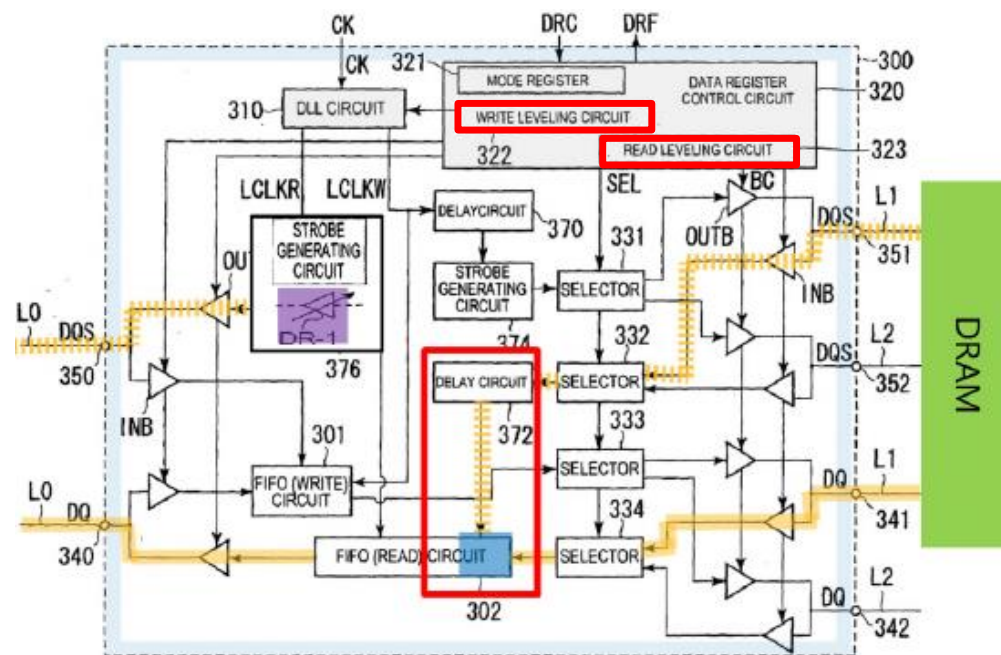


FIG. 5

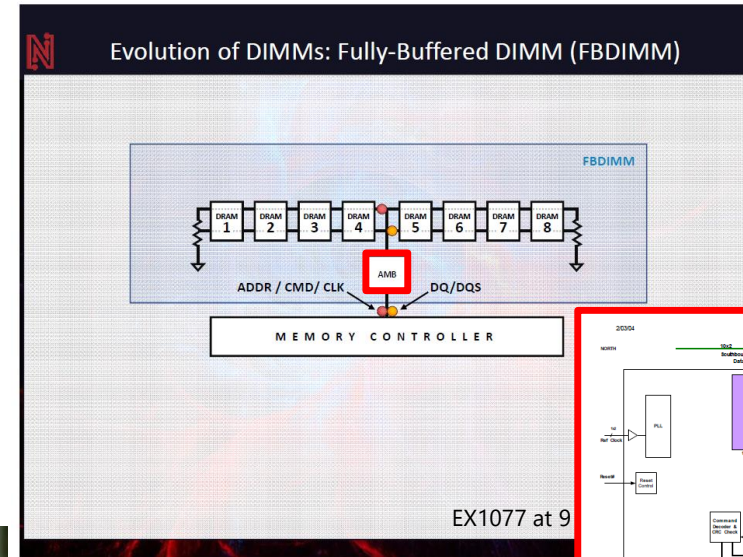
Netlist's "space-constrained" argument is meritless because no claim limitations concern space, and JEDEC allows for data buffers with diverse physical sizes and various functionalities

Q. Do any of the claims of the '608 patent limit the claimed memory module to any particular physical dimensions as set forth in any particular JEDEC specification?

A. No. There's no mention of JEDEC in the claims.

THE WITNESS: Well, there's a lot of different JEDEC standards. There's standards -- I mean, the JEDEC standard for a DDR3 SDRAM. There are standards for physical size, but there are multiple standards for multiple physical sizes. So there is no one JEDEC physical size standard. I mean, I can't name them all to

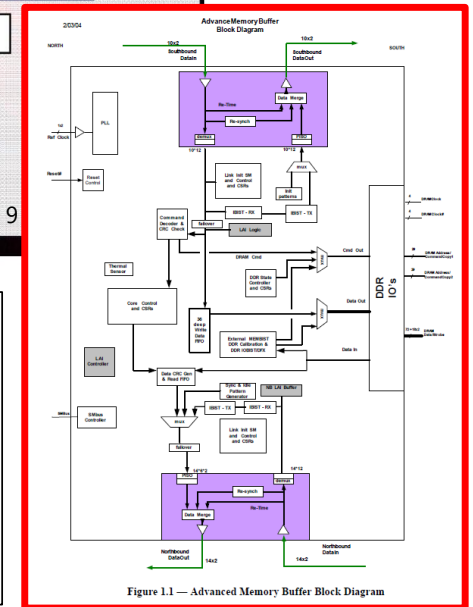
EX2012 at 139:12-16, 140:1-6



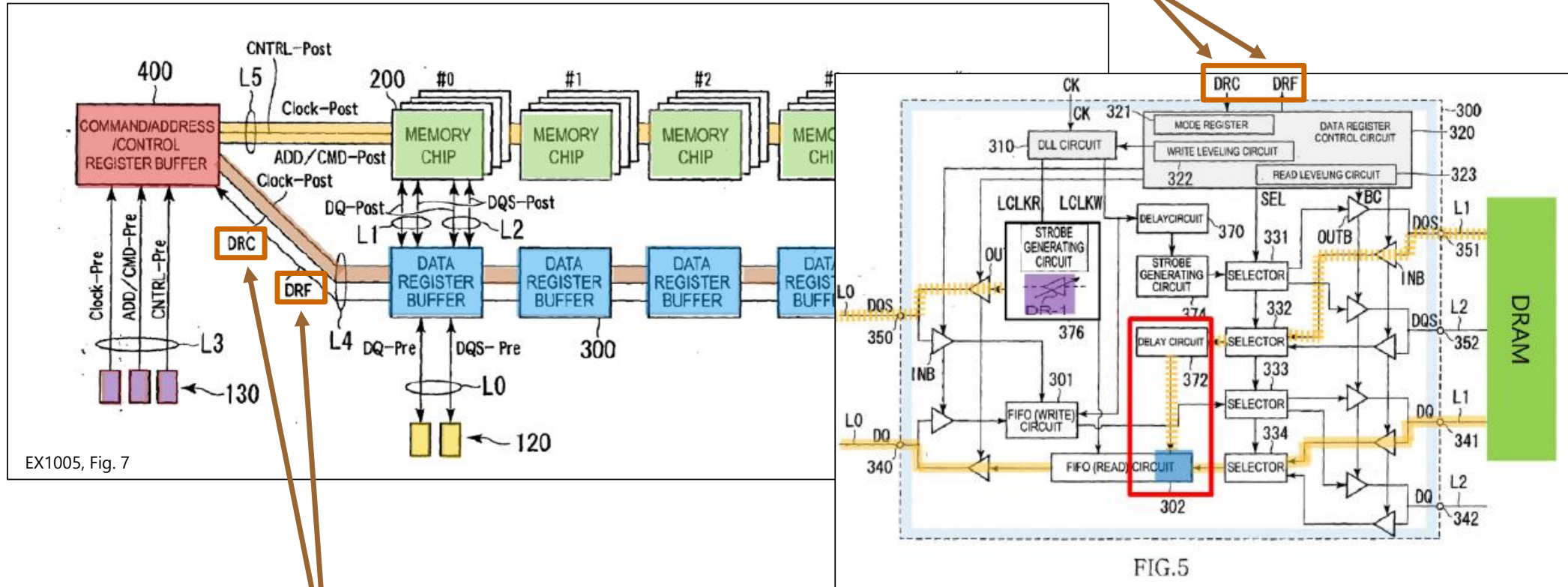
Q. And would it be fair to say at a high level that an FBDIMM buffer is all of the signals on the memory module using the AMB, advance memory buffer, so that would include the address command and clock signals from the memory controller, as well as all of the data signals on the bidirectional data lines?

THE WITNESS: I think that's likely the case, but it's been quite a long time since

EX1074 at 60:8-18 (objections omitted)



Hiraishi's control lines DRC and DRF are already on the module to control Hiraishi's data buffer in the Tokuhiro combination



Hiraishi + Tokuhiro

Netlist ignores that obviousness does not require showing that a data buffer would be better than the memory controller, just it was a known and suitable option



Fourth, there are significant advantages of having Tokuhiro's delay elements implemented in the memory controller. As taught in Tokuhiro, the delays are determined in a process in which "the first delay time control unit 23 ... gradually prolongs the delay time for the first variable delay circuit DW-n until the clock signal CK1 and the data strobe signals DQS-n are input to the n-channel SDRAM-n substantially at the same time." EX1006, 13:55-60. This process would be significantly less complex if performed when the first delay time control unit 23 and the first variable delay circuit DW-n are on the same side of the data bus, due in no small part to the fact that the memory controller can only communicate with the memory module following DDR signaling protocols, while CPU/memory controller communications do not. EX1006, 5:57 ("The memory controller 12 is a DDR3

Paper 20 (POR) at 77

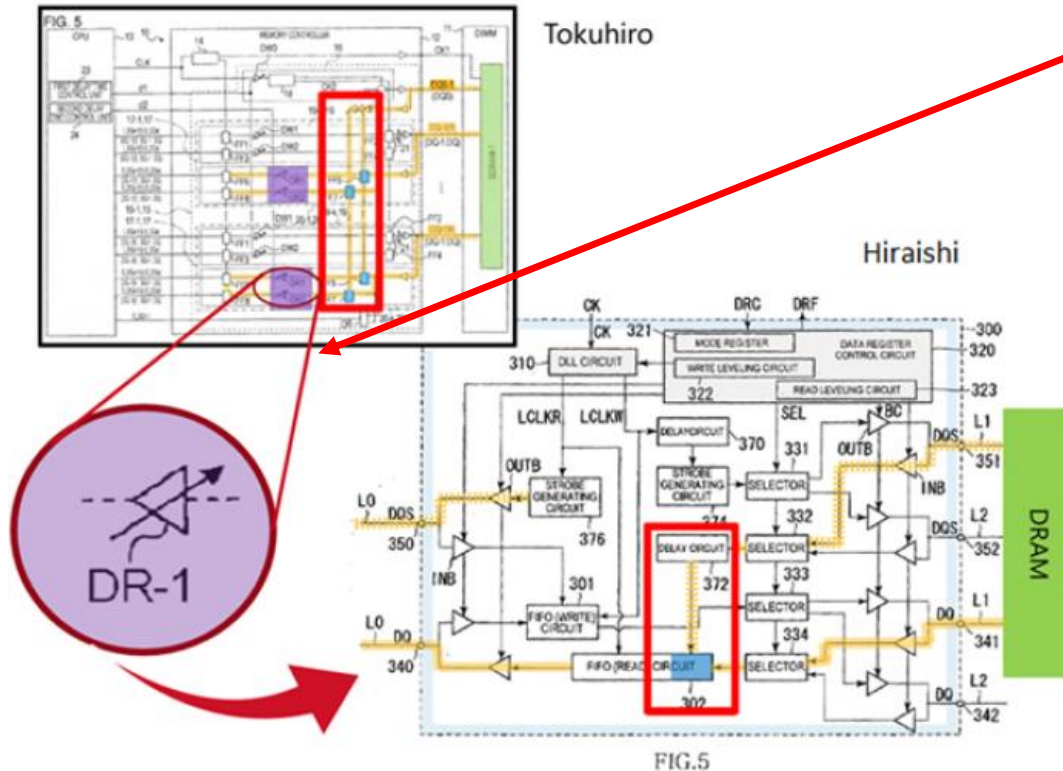
"[I]t's not necessary to show that a combination is the *best* option, only that it be a *suitable* option."

Intel Corp. v. PACT XPP Schweiz AG,
61 F.4th 1373, 1380-81 (Fed. Cir. 2023)

memory controller (MCH). EX1003, ¶263. A POSITA would have understood that the delay functionality of Tokuhiro can be implemented in either the data buffers or the memory controller of Hiraishi—a finite number of predictable solutions to the same problem—rendering both of those solutions obvious. And

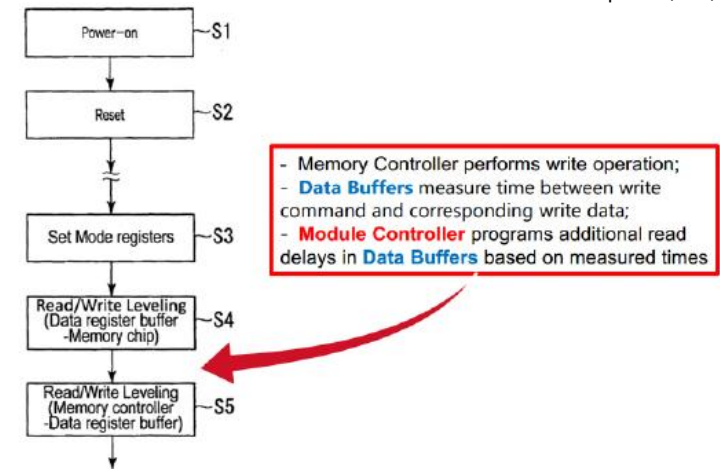
Paper 1 (Pet.) at 83

Netlist's argument that the combination would increase circuitry is meritless because Hiraishi already provides all the circuitry and control signals needed for read/write leveling



In this implementation, Tokuhiro's read delay functionality is added to the data register buffers of Hiraishi's module such that, advantageously, no changes to the circuitry of the memory controller are necessary. EX1003, ¶281. Tokuhiro's functionality of determining the fly-by delays from delays for the write operations and setting the additional read delays accordingly is implemented in Hiraishi's memory module, as shown in modified Fig.13 below. *Id.*

Paper 1 (Pet.) at 98



NETLIST'S MOTION TO SUPPLEMENT

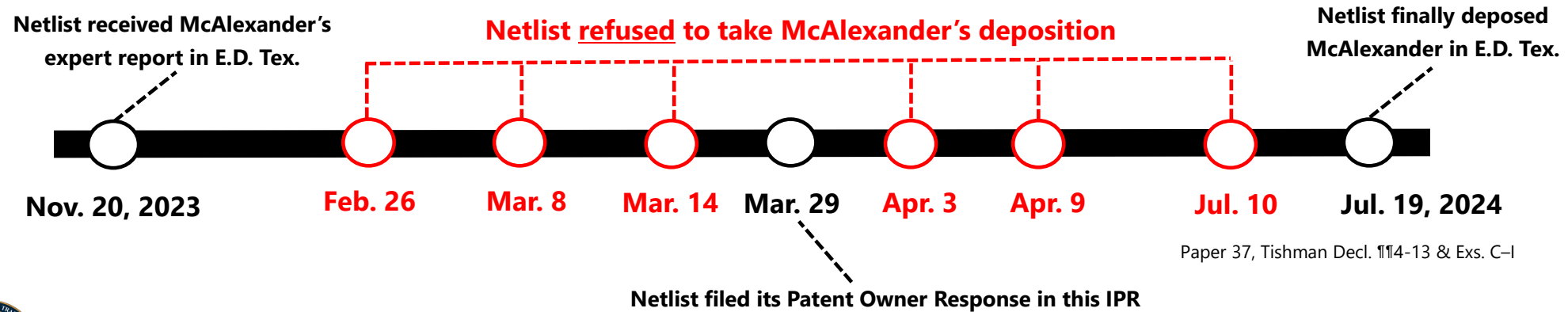
4

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 140

Netlist failed to show that McAlexander's testimony "reasonably could not have been obtained earlier" as required by 37 C.F.R. § 42.123(b)



present a new issue that has not been fully briefed. Patent Owner does not satisfactorily explain why it did not seek to depose Mr. Holbrook in this proceeding or why it did not depose Mr. Holbrook earlier.



Samsung Elecs. Co. v. Netlist, Inc., IPR2022-00996, Paper 48, at 4 (PTAB Dec. 6, 2023)

to parallel proceedings.”). Instead, Patent Owner apparently cancelled Mr. Chess’s scheduled deposition in this case, and never rescheduled it. See *id.* at 1. Accordingly, Patent Owner has not adequately demonstrated why the supplemental information reasonably could not have been obtained earlier.

ExtractionTek Sales LLC v. Gene Pool Technologies, Inc., IPR2022-00625, Paper 33, at 2–5 (PTAB Mar. 30, 2023)



Petitioner admitted that it had not requested additional discovery on these issues earlier during the *inter partes* review, which may have turned up Mr. Rieger’s testimony or similar information. Under these circumstances, Petitioner would not be able to demonstrate persuasively that “the supplemental information reasonably could not have been obtained earlier,” as required by 37 C.F.R. § 42.123(b).

PEAG LLC v. VARTA Microbattery GmbH, IPR2020-01212, Paper 46, at 4 (PTAB Dec. 30, 2021)

McAlexander's testimony is not "relevant" to this IPR under 37 C.F.R. § 42.123(a)(2) because his testimony was based on Netlist's view of the scope of the '608 Patent

1[d2] the each respective buffer circuit including a data path corresponding to each data signal line in the respective set	Based on <u>Netlist's</u> apparent view of the scope of the '608 patent claims , as articulated in its Infringement Contentions and which I disagree with, it is my opinion that Hiraishi alone or in view of the knowledge of a POSITA or in combination with the referenced prior art discloses element 1[d2]. <i>See claim limitation 1[d1] analysis above.</i>
--	--

Paper 37, Tishman Decl. Ex. C (McAlexander expert report) at p.36

Netlist failed to show that consideration of McAlexander's testimony "would be in the interests-of-justice" under 37 C.F.R. § 42.123(b), especially given that it is inadmissible hearsay

UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.,)
Plaintiff,)
vs.) CASE NO. 2:22cv293JRG
SAMSUNG ELECTRONICS CO.,)
LTD.,)
Defendant.)
_____)

CONFIDENTIAL - ATTORNEYS' EYES ONLY

CORRECTED TRANSCRIPT OF
REMOTE VIDEOTAPED DEPOSITION UPON ORAL
EXAMINATION OF JOSEPH McALEXANDER
FRIDAY, JULY 19, 2024
9:08 A.M. (Central Standard Time)

(All participants appeared remotely)

TAKEN AT THE INSTANCE OF THE PLAINTIFF

REPORTED BY:
MONNA J. NICKESON, RPR, CRR, CCR, CSR CA 14430
JOB: 6792757

Page 1

The testimony is hearsay, and no exception applies:

- **FRE 804(b) does not apply**
 - Netlist made "no attempt to bring [him] forward as a witness in this proceeding." *CaptionCall, L.L.C. v. Ultratec, Inc.*, IPR2015-00637, Paper 98, at 15–16 (PTAB Sept. 7, 2016), *appeal dismissed*, No. 2017-1210 (Fed. Cir. Jan. 19, 2022).
- **FRE 801(d)(2)(B)–(D) does not apply**
 - "Since an expert witness is not subject to the control of the party opponent [i.e., Samsung] with respect to consultation and testimony he or she is hired to give, the **expert witness cannot be deemed an agent** [i.e., of Samsung]." *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489–90 (5th Cir. 2021).
 - Construction of "data path" was not an issue in McAlexander's case, and McAlexander was applying Netlist's apparent construction of the '608 Patent
- **Samsung had no reason to object during McAlexander's deposition in E.D. Tex. because Netlist did not give notice it planned to use it in this IPR**

The testimony is also inadmissible under FRE 403:

- **Extrinsic evidence has little "probative value"**
 - "Undue reliance on extrinsic evidence poses **the risk that it will be used to change the meaning of claims** in derogation of the 'indisputable [intrinsic] records'." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1318–19 (Fed. Cir. 2005) (en banc).
 - *Samsung Elecs. Co. v. Netlist, Inc.*, IPR2022-00615, Paper 96, at 52–53 (PTAB Apr. 17, 2024) (dismissing motion to supplement with extrinsic evidence)

SAMSUNG'S MOTION TO EXCLUDE

5

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE



Samsung Electronics Co., Ltd.
Ex. 1059, p. 145

EX2016 is impermissible hearsay and inadmissible under FRE 403

1 UNITED STATES PATENT AND TRADEMARK OFFICE COURT
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3
4 SAMSUNG ELECTRONICS CO., LTD.,
5 Petitioner,
6 vs.
7 NETLIST, INC.,
8 Patent Owner.
9 _____/
10 Case No.: IPR2022-00711
11 U.S. Patent Number 10,860,506
12 -----
13
14
15 REMOTE VIDEOTAPED DEPOSITION OF
16 ROBERT WEDIG, Ph.D
17 Thursday, January 19, 2023
18 9:00 a.m. - 5:16 p.m. (PST)
19
20
21
22 Stenographically Reported By:
23 Kimberly Fontalvo, RPR, CLR
24 Realtime Systems Administrator
25 NCRA, CCRA, FCRA

Page 1

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Netlist EX2016
Samsung v. Netlist
IPR2023-00847

EX2016 is impermissible hearsay:

- **From a different IPR proceeding**
- **FRE 801(d)(1) does not apply**
 - Netlist did not cross-examine the witness about EX2016.
 - There is no prior inconsistent testimony
- **FRE 801(d)(2) does not apply**
 - "Since an expert witness is not subject to the control of the party opponent [i.e., Samsung] with respect to consultation and testimony he or she is hired to give, the expert witness cannot be deemed an agent [i.e., of Samsung]." *HTC Corp. v. Telefonaktiebolaget LM Ericsson*, 12 F.4th 476, 489–90 (5th Cir. 2021).
- **FRE 106 does not apply**
 - Netlist is the party trying to introduce EX2016, so only Samsung could rely on FRE 106, not Netlist
- **Samsung had no reason to object during Dr. Wedig's deposition in IPR2022-00711**
- **FRE 804(b) does not apply**
 - Netlist deposed the expert in this IPR. See EX2012.

EX2016 is inadmissible under FRE 403:

- **Cited testimony concerned different issues**
- **Netlist deposed the same witness regarding the issues relevant to this IPR. See EX2012.**

EX2016 is inadmissible under 37 C.F.R. § 42.53(f)(5)-(6) and 37 C.F.R. § 42.51(b)(1)(iii) does not apply

CERTIFICATE OF REPORTER

STATE OF COLORADO

I, KIMBERLY FONTALVO, Registered Professional Reporter, do hereby certify that I was authorized to and did stenographically report the foregoing remote deposition of ROBERT WEDIG, Ph.D; that a review of the transcript was requested; and that the transcript is a true record of my stenographic notes.

I FURTHER CERTIFY that I am not a relative, employee, attorney, or counsel of any of the parties, nor am I a relative or employee of any of the parties' attorneys or counsel connected with the action, nor am I financially interested in the action.

Dated this 22nd day of January, 2023.


KIMBERLY FONTALVO, RPR, CLR

Page 228

I declare under penalty of perjury that the foregoing is true and correct. Subscribed at _____, California, this _____ day of _____, 2023.

ROBERT WEDIG, Ph.D

Page 226

EX2016 is inadmissible under 37 C.F.R. § 42.53(f)(5)-(6):

- EX2016 lacks the witness's signature and corrections
- The certificate shows the witness did not refuse to read or sign the transcript

37 C.F.R. § 42.51(b)(1)(iii) is not an evidentiary rule and does not permit the admission of EX2016

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