

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2026-00017

Patent 9,824,035

**PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,824,035**

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EXHIBIT LIST

Exhibit #	Description
1001	U.S. Patent No. 9,824,035 (“’035 Patent”)
1002	File History of U.S. Patent No. 9,824,035
1003	Declaration of Dr. Robert Wedig
1004	Curriculum Vitae of Dr. Robert Wedig
1005	U.S. Patent Pub. No. 2010/0312925 to Osanai (“Osanai”) (Exhibit 1005 in IPR2022-00236, and Exhibit 2004 in IPR2023-00847)
1006	U.S. Patent No. 8,020,022 to Tokuhiro (“Tokuhiro”)
1007	U.S. Patent Pub. No. 2006/0277355 by Ellsberry (“Ellsberry”)
1008	U.S. Patent No. 6,184,701 to Kim (“Kim”)
1009	U.S. Patent No. 8,566,516 to Schakel
1010	File History of U.S. Patent No. 9,128,632
1011	File History of U.S. Patent No. 9,563,587
1012	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Petition)
1013	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 1 (PTAB January 20, 2017) (632 Patent Owner Preliminary Response)
1014	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00730, Paper No. 8 (PTAB July 21, 2017) (632 Decision Denying Institution)
1015	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2018-00362, Paper No. 29 (PTAB June 27, 2019) (907 Final Written Decision)
1016	<i>Netlist, Inc. v. Micron Tech., Inc., et al.</i> , No. 6:21-cv-00431 (W.D. Tex. Apr. 28, 2021) (Netlist Complaint)
1017	Declaration of Julie Carlson for JEDEC Standard 21-C

Exhibit #	Description
1018	JEDEC Standard 21-C, DDR SDRAM Registered DIMM Design Specification (January 2002)
1019	Declaration of Julie Carlson for JESD79-3C
1020	JEDEC DDR3 SDRAM Standard, JESD79-3C (April 2008)
1021	Bruce Jacob et al., <u>Memory Systems: Cache, DRAM, Disk</u> (2008) (excerpts)
1022	Harold S. Stone, <u>Microcomputer Interfacing</u> (1982)
1023	Microsoft Computer Dictionary (5th ed. 2002)
1024	U.S. Patent No. 9,263,103 to Giovannini
1025	U.S. App. No. 61/676,883 (provisional application to '632 Patent)
1026	U.S. Patent No. 8,565,033 to Manohararajah
1027	U.S. Patent No. 7,808,849 to Swain
1028	U.S. Patent No. 9,536,579 to Iijima
1029	U.S. Patent Pub. No. 2007/0008791 to Butt (“ <u>Butt</u> ”)
1030	U.S. Patent Pub. No. 2010/0309706 to Saito (“ <u>Saito</u> ”)
1031	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 45 (PTAB Oct. 18, 2023)
1032	Decision Denying Patent Owner’s Request on Rehearing of Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00639, Paper 48 (PTAB Feb. 9, 2024)
1033	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00615, Paper 96 (PTAB Apr. 17, 2024)
1034	Decision Denying Patent Owner’s Request for Director Review of Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00615, Paper 103 (PTAB July 10, 2024)

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Exhibit #	Description
1035	[omitted]
1036	[omitted]
1037	Joint Claim Construction Statement, <i>Netlist, Inc. v. Micron Technology, Inc. et al.</i> , No. 1:22-cv-00136 (W.D. Tex. Apr. 14, 2022)
1038	[omitted]
1039	[omitted]
1040	[omitted]
1041	[omitted]
1042	[omitted]
1043	[omitted]
1044	[omitted]
1045	Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,860,506 (Exhibit 1003 in IPR2022-00711)
1046	U.S. Patent No. 10,860,506
1047	[omitted]
1048	Joint 4-3 Claim Construction and Prehearing Statement, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Aug. 19, 2022 and Aug. 23, 2022)
1049	Joint Claim Construction Chart Pursuant to P.R. 4-5(d), <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Sept. 30, 2022)
1050	Claim Construction Order, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2:21-cv-00463 (E.D. Tex. Dec. 14, 2022)
1051	JEDEC LRDIMM DDR3 Memory Initialization Proposal (2009)

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Exhibit #	Description
1052	Declaration of Julie Carlson for Exhibit 1051
1053	JEDEC AMB standard (March 2007) (Exhibit 1053 in IPR2022-00711)
1054	JEDEC DDR4 SDRAM Standard, JESD79-4 (Sept. 2012)
1055	[omitted]
1056	U.S. Patent Pub. No. 2010/0312956 to Hiraishi (“ <u>Hiraishi</u> ”) (Exhibit 1005 in IPR2023-00847)
1057	U.S. Pat No. 10,268,608
1058	Declaration of Dr. Robert Wedig Regarding U.S. Patent No. 10,268,608 (Exhibit 1003 in IPR2023-00847)
1059	Petitioner's demonstratives for U.S. Patent No. 10,268,608 (Exhibit 1089 in IPR2023-00847)
1060	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2023-00847, Paper 42 (PTAB Dec. 10, 2024) (U.S. Patent No. 10,268,608)
1061	Notice of Docketing, <i>Samsung Electronics Co., Ltd. v Netlist, Inc.</i> , No. 2025-1378 (Fed. Cir. Jan. 21, 2025) (U.S. Patent No. 10,268,608)
1062	Appellant’s Principal Brief, <i>Samsung Electronics Co., Ltd v Netlist, Inc.</i> , No. 2025-1378 (Fed. Cir. Apr. 18, 2025) (U.S. Patent No. 10,268,608)
1063	Netlist’s Response Brief, <i>Samsung Electronics Co., Ltd. v Netlist, Inc.</i> , No. 2025-1378 (Fed. Cir. July 28, 2025) (U.S. Patent No. 10,268,608)
1064	Appellant’s Reply Brief, <i>Samsung Electronics Co., Ltd v Netlist, Inc.</i> , No. 2025-1378 (Fed. Cir. Sept. 15, 2025) (U.S. Patent No. 10,268,608)
1065	[omitted]

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Exhibit #	Description
1066	Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00236, Paper 34 (PTAB June 20, 2023) (U.S. Patent No. 9,824,035)
1067	Decision Granting Petitioner’s Request on Rehearing of Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00236, Paper 36 (PTAB August 16, 2023) (U.S. Patent No. 9,824,035)
1068	Final Written Decision, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , IPR2022-00711, Paper 42 (PTAB Oct. 17, 2023) (U.S. Patent No. 10,860,506)
1069	Denying Patent Owner’s Request on Rehearing of Final Written Decision, <i>Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.</i> , IPR2022-00711, Paper 44 (PTAB Dec. 20, 2023) (U.S. Patent No. 10,860,506)
1070	[omitted]
1071	[omitted]
1072	[omitted]
1073	[omitted]
1074	Transcript of Deposition of Dr. William Mangione-Smith (June 4, 2024) (Exhibit 1074 in IPR2023-00847)
1075	Transcript of Deposition of Dr. William Mangione-Smith on May 4, 2023 (Exhibit 1046 in IPR2022-00711 and Exhibit 1075 in IPR2023-00847)
1076	[omitted]
1077	Netlist’s Technology Tutorial (Exhibit 1047 in IPR2022-00711 and Exhibit 1077 in IPR2023-00847)
1078	[omitted]
1079	[omitted]

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Exhibit #	Description
1080	[omitted]
1081	[omitted]
1082	[omitted]
1083	[omitted]
1084	U.S. Patent No. 7,215,584 to Butt et al. (incorporated by reference in [0047] of Exhibit 1029)
1085	Presentation on read leveling and write leveling for DDR3 memory modules (2008)
1086	Complaint, <i>In the Matter of Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof</i> , Inv. No. 337-TA-3854 (USITC filed Sept. 30, 2025) (U.S. Patent Nos. 9,824,035 and 10,268,608)

CLAIM LISTING

Ref. #	Listing of Challenged Claims (2-9, 14-20)[†]
1[pre]	1. A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:
1[a]	a module board having edge connections for coupling to respective signal lines in the memory bus;
1[b]	a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals; and;
1[c]	memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and;
1[d]	a plurality of buffer circuits mounted on the module board in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines,
1[e]	wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of data/strobe signal lines and a respective set of memory devices, the each respective buffer circuit including data paths for transmitting respective data and strobe signals associated with the first memory operation and logic configured to respond to the module control signals by enabling the data paths,

[†] Claims 1, 10-13, and 21-22, which are highlighted in grey, were cancelled.

See EX1001, 41.

Ref. #	Listing of Challenged Claims (2-9, 14-20) [†]
1[f]	wherein the logic is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information.
2	2. The memory module of claim 1, wherein the first memory operation is a memory read operation and the second memory operation is a memory write operation.
3	3. The memory module of claim 2, wherein the each respective buffer circuit includes a delay control circuit configured to determine, during the memory write operation, a time interval between receiving a first signal from the module control device and receiving a second signal from the memory controller, and wherein the timing information includes the time interval.
4[a]	4. The memory module of claim 3, wherein the each respective buffer circuit is further configured to receive a module clock signal and further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,
4[b]	wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.
5	5. The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
6[a]	6. The memory module of claim 2, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and
6[b]	wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output the respective data and strobe signals.

Ref. #	Listing of Challenged Claims (2-9, 14-20) [†]
7	7. The memory module of claim 3, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.
8[a]	8. The memory module of claim 7, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and
8[b]	wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output the respective data and strobe signals, the two memory devices being in a same rank.
9	9. The memory module of claim 1, wherein the each respective buffer circuit is further configured to receive a module clock signal from the module control device and further includes a receiver circuit for each of the module control signals, the receiver circuit including a metastability detection circuit configured to determine a metastability condition in the each of the module control signals with respect to the module clock signal
10	10. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
11[a]	11. The memory module of claim 10, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and
11[b]	wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to receive or output the respective data and strobe signals.
12	12. The memory module of claim 1, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.

Ref. #	Listing of Challenged Claims (2-9, 14-20) [†]
13[a]	13. The memory module of claim 12, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and
13[b]	wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to receive or output the respective data and strobe signals, the two memory devices being in a same rank.
14[a]	14. The memory module of claim 1, wherein the each respective buffer circuit is further configured to receives a module clock signal and further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,
14[b]	wherein the each respective buffer circuit is configured to output the local clock signal to the respective set of memory devices.
15	15. The memory module of claim 14, wherein the data paths include a first data path for transmitting a strobe signal among the respective data and strobe signals, the first data path including a sampler that samples the strobe signal in accordance with the local clock signal.
16	16. The memory module of claim 15, wherein the data paths include a second data path for transmitting a first data signal among the data and strobe signals, the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.
17	17. The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.
18[a]	18. The memory module of claim 17, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include one memory device from each of the plurality of ranks, and

Ref. #	Listing of Challenged Claims (2-9, 14-20) [†]
18[b]	wherein the module command signals include chip select signals that select one memory device in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal.
19	19. The memory module of claim 14, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits.
20[a]	20. The memory module of claim 19, wherein the memory devices are arranged in a plurality of ranks and the respective set of memory devices include two memory devices from each of the plurality of ranks, and
20[b]	wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices to output or receive the respective data and strobe signals in accordance with the local clock signal, the two memory devices being in a same rank.
21	21. The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the module control device.
22	22. The memory module of claim 1, wherein the one or more signals received by the each respective buffer circuit during the second memory operation include at least one signal from the memory controller.

I. PETITIONER’S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 9,824,035.

The following proceedings are currently pending:

- *In the Matter of Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-3854 (USITC filed Sept. 30, 2025) (U.S. Patent Nos. 9,824,035 and 10,268,608)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, Nos. 6:21-cv-00431 and 1:22-cv-00136 (W.D. Tex. filed Apr. 28, 2021) (U.S. Patent Nos. 9,824,035 and 10,268,608)
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2022-00711, and *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2023-00205, *appeal docketed*, No. 2024-1521 (Fed. Cir. Feb. 27, 2024) (U.S. Patent No. 10,860,506)

Petition for *Inter Partes* Review of U.S. Patent No. 9,824,035

- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (U.S. Patent No. 10,860,506)
- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021) (U.S. Patent No. 10,860,506)
- *Samsung Electronics Co., Ltd. v Netlist, Inc.*, IPR2023-00847, *appeal docketed*, No. 2025-1378 (Fed. Cir. Jan. 21, 2025) (U.S. Patent No. 10,268,608)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293 (E.D. Tex. filed Jul. 20, 2023) (U.S. Patent No. 10,268,608)
- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, IPR2022-00639, *appeal docketed*, No. 2024-1707 (Fed. Cir. Apr. 17, 2024)
- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, IPR2022-00615, *appeal docketed*, No. 2024-204 (Fed. Cir. Sept. 11, 2024)
- U.S. Patent Application No. 18/452,554

The following proceedings are no longer pending:

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00236 (U.S. Patent No. 9,824,035)

Petition for *Inter Partes* Review of U.S. Patent No. 9,824,035

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021) (U.S. Patent No. 10,860,506)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2024-00370 (U.S. Patent No. 10,268,608)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00237 (U.S. Patent No. 10,268,608)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00730 (U.S. Patent No. 9,128,632)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2018-00362 and -00363

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to

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II. INTRODUCTION

Petitioner respectfully requests trial on claims 2-9 and 14-20 of U.S. Patent 9,824,035 (“’035 Patent”) (EX1001).

III. REQUIREMENTS FOR INTER PARTES REVIEW

A. Grounds for Standing (§42.104(a))

Petitioner certifies that the ’035 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the ’035 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 2-9 and 14-20 of the ’035 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	2-9, 14-20	103(a)	<u>Osanai</u> + <u>Butt</u> + <u>Tokuhiro</u>
2	2-9, 14-20	103(a)	Ground 1 + <u>Ellsberry</u>
3	2-9, 14-20	103(a)	Ground 1 + <u>Kim</u>

Petitioner’s proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above starting on page vi, and includes an expert declaration by Robert Wedig, Ph.D., EX1003.

IV. BACKGROUND ON THE ’035 PATENT

A. Effective Filing Date

The ’035 Patent claims priority to a provisional application filed July 27, 2012, EX1001; EX1025, which is after the prior art relied on by Petitioner, so for

purposes of this IPR, Petitioner assumes that the claims of the '035 Patent have an effective filing date of **July 27, 2012**.

B. Person of Ordinary Skill in the Art

A person of ordinary skill in the art in the field of the '035 Patent in July 2012 (“POSITA”) would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field of memory module design and operation, or a bachelor’s degree in such engineering disciplines and at least three years of work experience in the field. EX1003, ¶37. A POSITA would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers. *Id.* A POSITA would also have been familiar with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers. *Id.* In previous IPRs against certain claims of the '035 Patent (IPR2022-00236) and all claims of its child, the '506 Patent (IPR2022-00711), the Board adopted a substantially similar level of skill in the art. EX1066, 8-9; EX1068, 6.

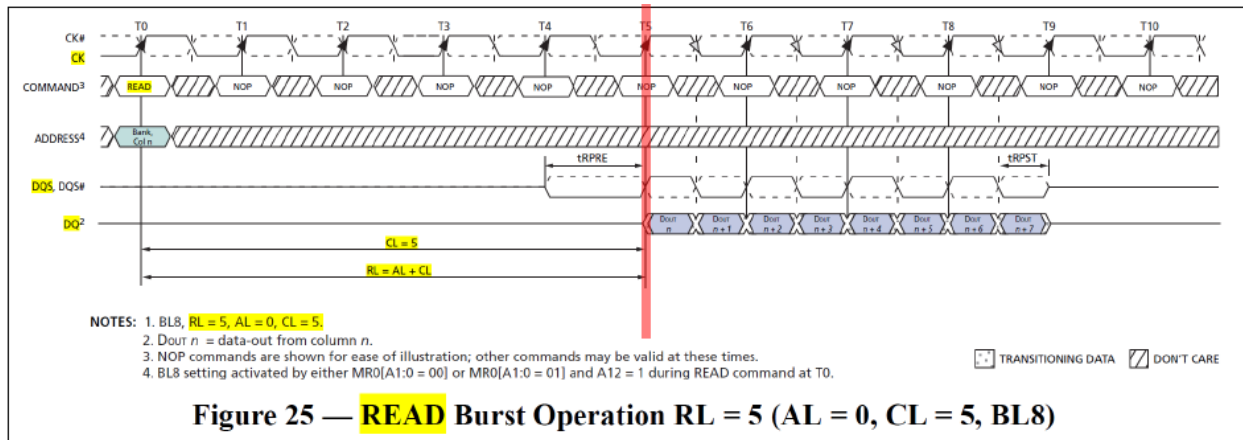
C. Technical Background

The '035 Patent is directed to memory modules with double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices. EX1001, 1:47-52, 8:6-9. Different versions of DDR SDRAMs have been standardized by JEDEC, including a third-generation referred to as DDR3. *See, e.g.*, EX1020 (JESD79-3C). JEDEC is the leading standard setting organization in this field. EX1052, ¶ 4; EX1003, ¶¶39-41.

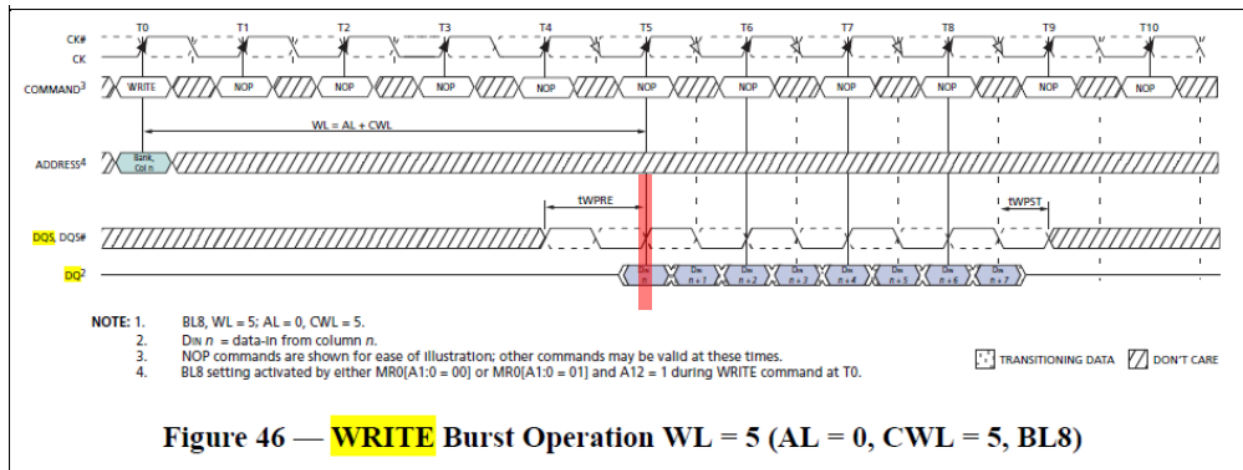
The JEDEC standards define the interface and access to DDR memory devices, including the signals for address (e.g., A0-A15 and BA0-BA2), command (e.g., RAS, CAS, WE, and chip select (CS)), clock (CK), and data/strobe (DQ/DQS). EX1020, p.13; EX1003, ¶42. The salient feature of **DDR** DRAMs is that they use a “**dual-edged clock”¹** for data transmission (resulting in two data transmissions per clock cycle), EX1021 (Jacobs), pp.333-34, which requires properly synchronized clock (CK), data (DQ), and strobe (DQS) signals, as shown by the red lines below. EX1003, ¶¶43-44. Also, the JEDEC DDR3 standard requires setting, during initialization using an MRS command, CAS latency (CL) and additive latency (AL), that together define the read latency (RL=CL+AL),

¹ Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.

which is an integer number of clock cycles (e.g., 5 clock cycles) between a read command (e.g., at time T0) and the first read data (e.g., at time T5) as shown below:



EX1059, p.14; EX1020, p.56; *see also id.* pp.19 (requiring MRS commands at initialization), 23 (permitting CAS Latency (CL) to be set at initialization to 5, 6, 7, 8, 9, or 10 clock cycles), 24 (“DDR3 SDRAM does not support any half-clock latencies.”), 27 (“Read Latency (RL) is controlled by the sum of the AL and CAS Latency (CL) register settings”); EX1021, 342 (explaining JEDEC’s programmable CAS latency); EX1003, ¶44. As shown by the red line above, the clock (CK), strobe (DQS), and data (DQ) signals must be **edge**-aligned for **read** operations. For **write** operations, as shown below, the strobe (DQS) signal, while edge-aligned with the clock (CK) signal, must be **center**-aligned with the data (DQ) signals:



EX1059, p.14; EX1020, p.71; EX1003, ¶44. Similar to read operations, write operations include a write latency (WL), which is a latency between a write command (e.g., at time T0) and the first write data (e.g., at time T5). EX1020, pp.19, 29, 30. The WL is the sum of the additive latency (AL) and a CAS write latency (CWL), both set by a MRS command during initialization. *Id.*; EX1003, ¶44.

The JEDEC standards also define strict timing requirements for DDR DRAM signals, such as “tDQSQ” requiring a very tight tolerance between the DQ data and DQS strobe signals. See, e.g., EX1020, pp.57 (Fig. 27, below left, timing of CK, DQS, and DQ signals for read), 69 (Fig. 43, below right, similar for write), 59 (“tDQSQ”); EX1074, 137:13-22, 139:13-24; EX1003, ¶45.

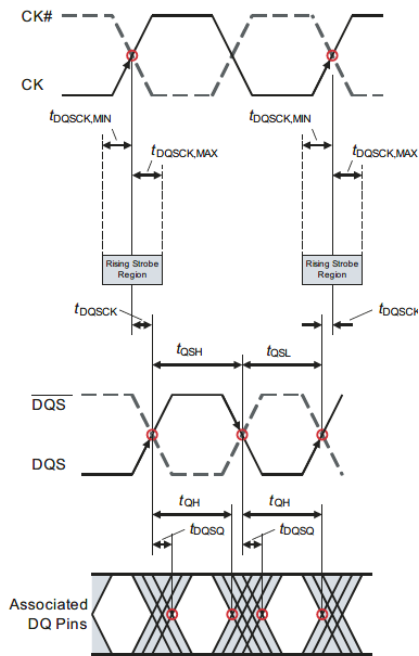


Figure 27 — READ Timing Definition

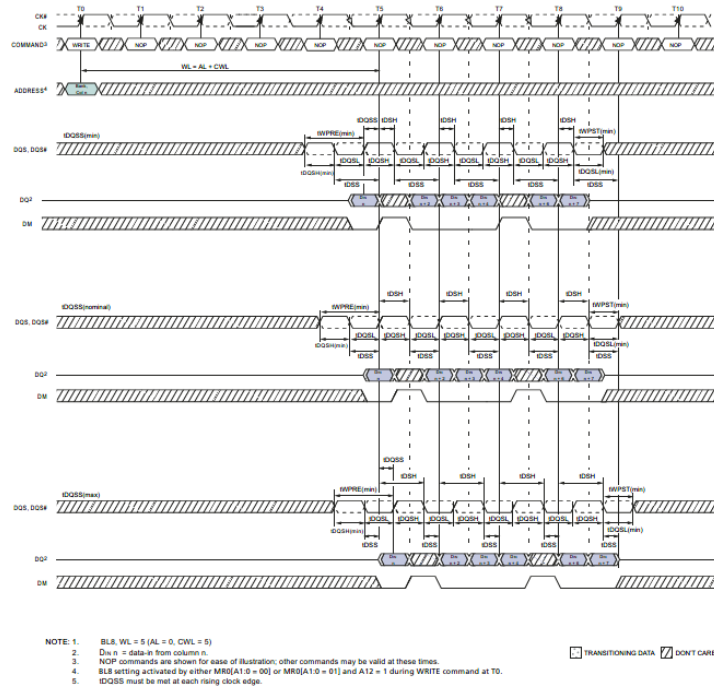
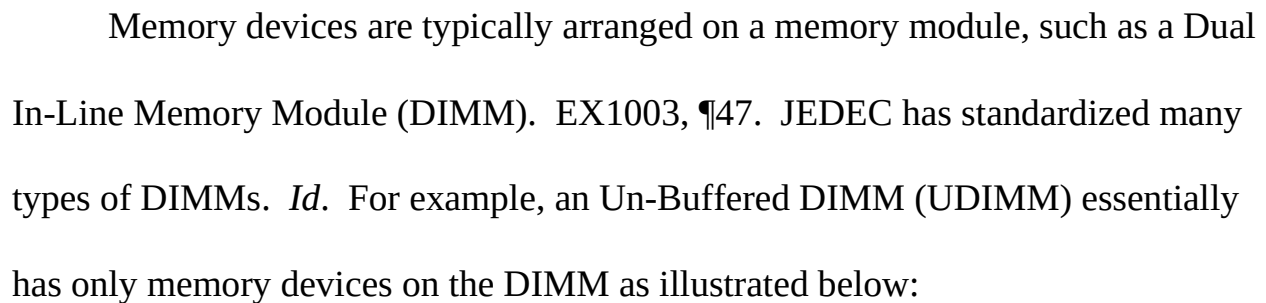
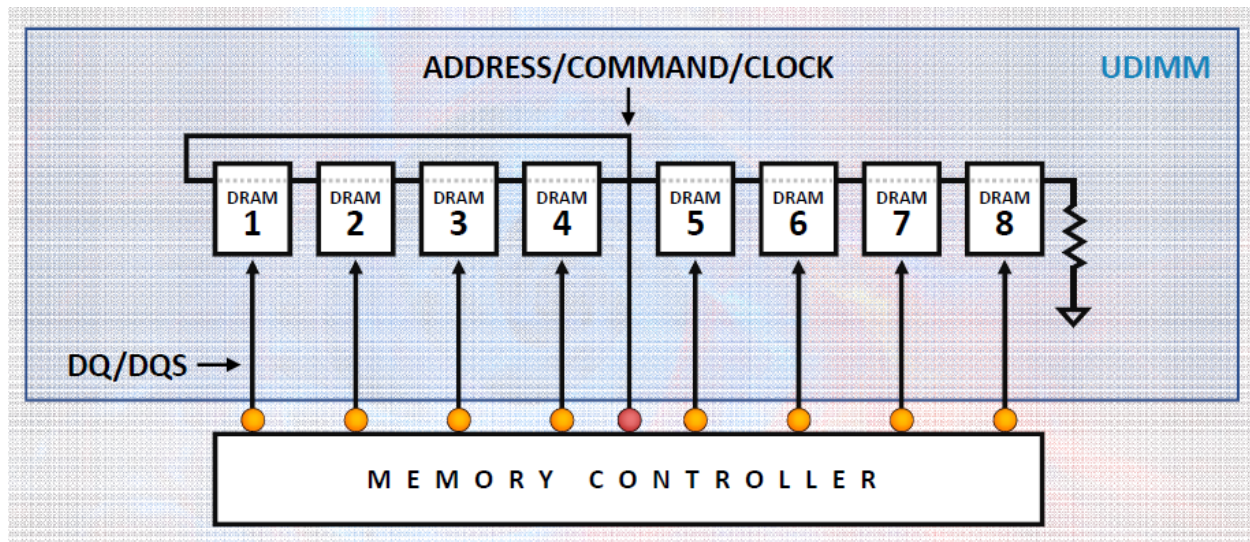


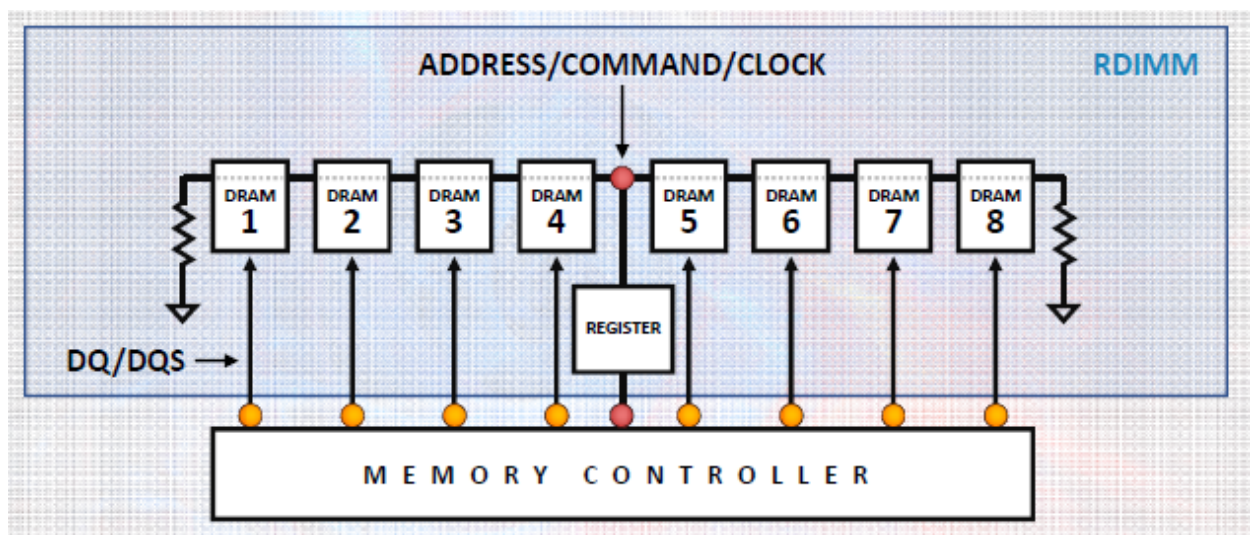
Figure 43 — Write Timing Definition and Parameters

As DDR generations advanced (e.g., DDR1, then DDR2, then DDR3, etc.), the speed of the memory devices became faster to the point that the time required for these signals to travel the distance to and from the memory devices could exceed one clock cycle or even one data period (which is half of the clock period for DDR memory devices):

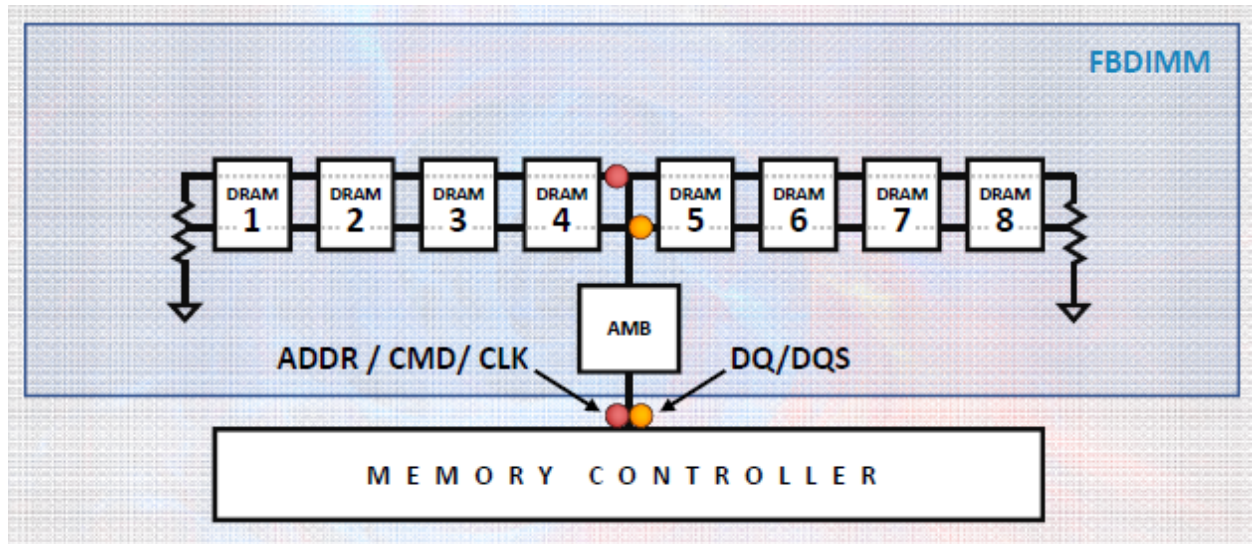




EX1077, p.7; EX1003, ¶47. Another example is a Registered DIMM (RDIMM), which includes a Register on the DIMM for address/command and clock signals:



EX1077, p.8; EX1018; EX1003, ¶47. Another example is a Fully Buffered DIMM (FBDIMM), which buffers all the signals, including the data signals:



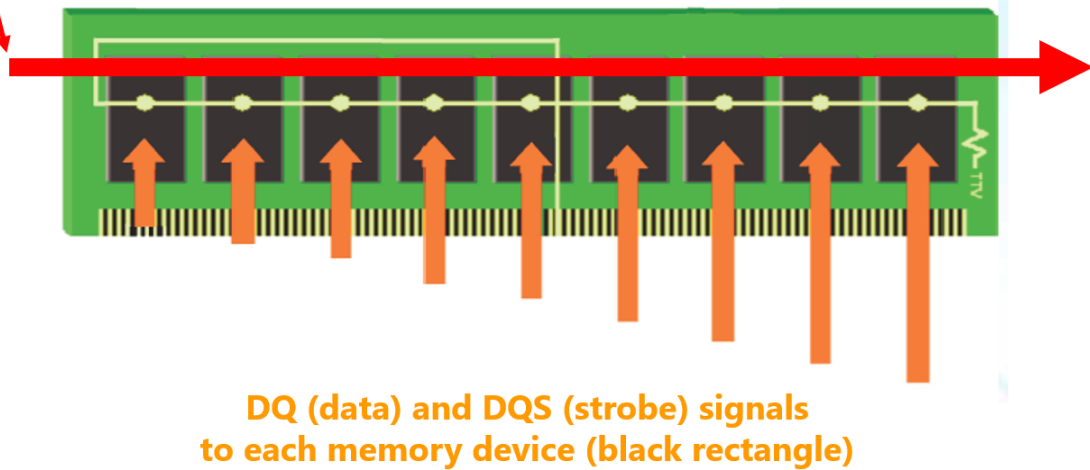
EX1077, p.9; EX1053; EX1003, ¶47.

The JEDEC DDR3 standard adopted a “fly-by topology” for memory modules, EX1020, p.42, where the command and clock signals traveling on the x-axis arrive at each memory device at a different time as illustrated below with the large red arrow pointing to the right:

JEDEC DDR3 SDRAM

4.8 Write Leveling

For better signal integrity, the DDR3 memory module adopted fly-by topology for the commands, addresses, control signals, and clocks. The fly-by topology has benefits from reducing number of stubs and



See EX1085, 9; EX1020, 42; EX1003, ¶48. As discussed above, the DQ (data) and DQS (strobe) signals, which generally travel on the y-axis, must be properly aligned at each memory device with the clock (CK) signal, which travels on the x-axis in a “fly-by topology.” *Id.* To achieve this alignment, the JEDEC standard permits “write leveling” during initialization of the memory module, which allows the transmitter of the data (e.g., the host computer) to adjust the delays for the DQ (data) and DQS (strobe) signals for each memory device to account for “fly-by” delays by the write command and the clock signal traveling on the x-axis. *Id.* In the example illustrated above, write leveling results in the DQ (data) and DQS (strobe) signals (orange arrow) being delayed more for a memory device (black) on the right side of the memory module as compared to a memory device (black) on

the left side of the memory module, to account for the time it takes for the write command and clock signal (red arrow pointing to the right) to travel from left to right. *Id.*

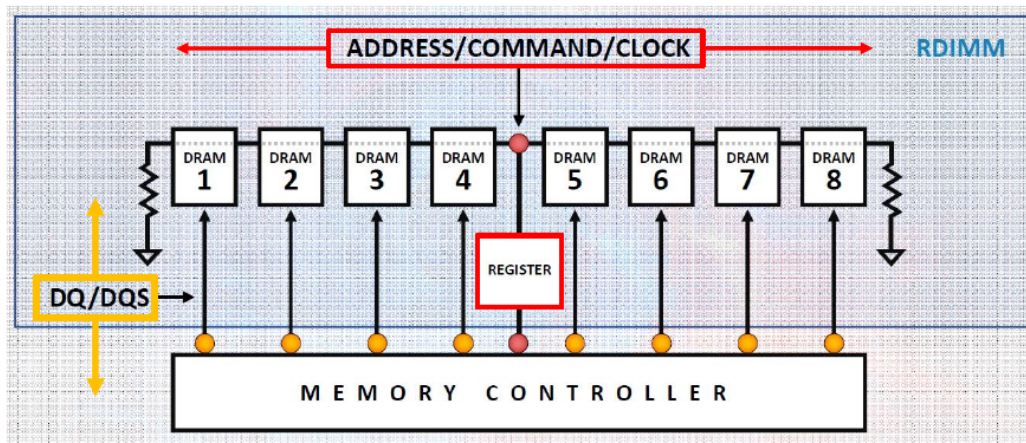
Under the JEDEC standard, the “DRAM enters into Write leveling mode” during initialization in response to a Mode Register Set (MRS) command. EX1020, pp.43, 33, 19, 22, 26 (below showing MRS enabling/disabling Write leveling); EX1003, ¶48.

A7	Write leveling enable
0	Disabled
1	Enabled

After exiting the Write Leveling Mode, normal memory write operations can be carried out, where as a result of write leveling the clock (CK), strobe (DQS), and data (DQ) signals are properly aligned to satisfy JEDEC’s timing requirements, as shown by the vertical red lines above (pp.4-5). EX1020, p.45 (defining the “sequence ...[of] how the Write Leveling Mode should be exited”); EX1003, ¶48.

In some memory modules, like an RDIMM below, the command and clock signals (red) travel on the x-axis from the Register at the center of the module out to both the left and right, while the DQ/DQS data/strobe signals travel on the y-axis directly from the memory controller:

Memory modules transmit address/command and clock (CK) signals in the horizontal direction, and data (DQ) and strobe (DQS) signals in the vertical direction



EX1077, 8

EX1059, 12; EX1077, 8; EX1003, ¶49. This configuration creates a difference at each memory device between the delay of the command/clock signals on the x-axis (with fly-by delays) and the DQ/DQS data/strobe signals on the y-axis (without such delays), causing misalignment between those signals, which must be corrected (e.g., with write leveling) to comply with the timing requirements of the JEDEC standard discussed above. *Id.*

D. The '035 Patent

1. Overview

The '035 Patent, as shown below, discloses a memory module (110) including memory devices (112, green) organized in groups, each group with an associated data buffer (isolation device 118, blue), and one module control device (116, red) located in the center of the module. The groups of memory devices (green) and associated data buffers (blue) are distributed length-wise (i.e.,

horizontally, along the x-axis) across the memory module. EX1001, 3:23-25, 3:49-52, Fig. 2C (below with annotations):

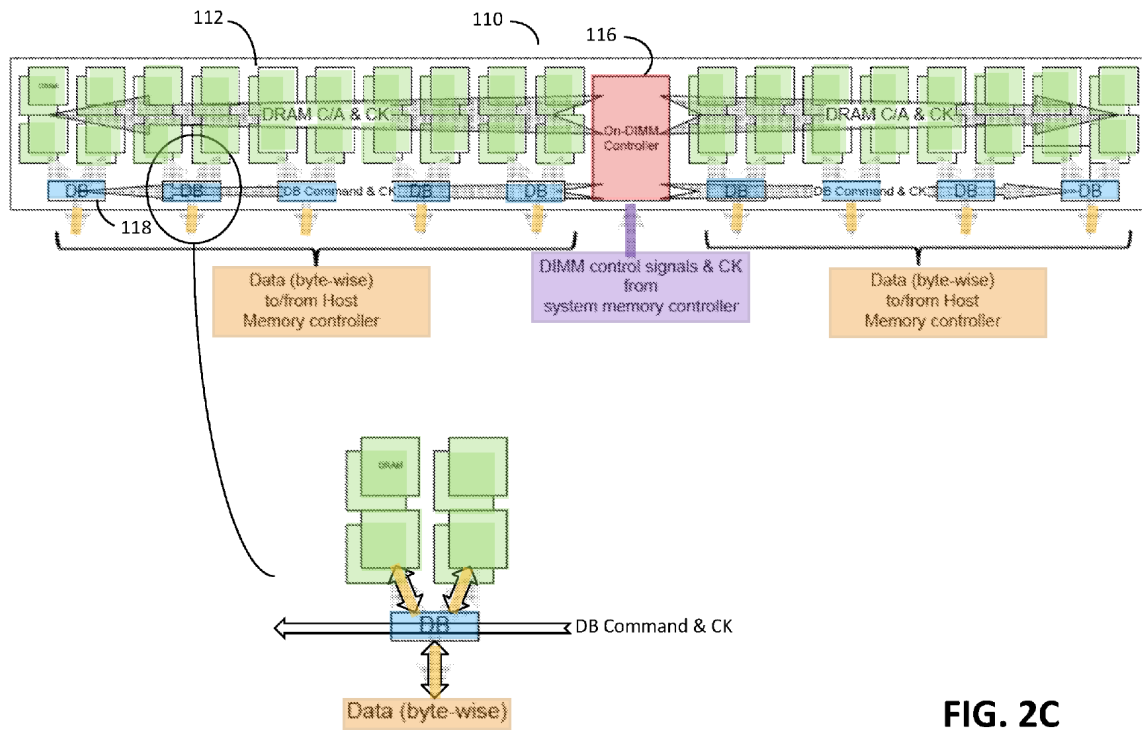


FIG. 2C

As shown below (using a different orientation), the memory module (110) is connected to a memory controller (MCH) (101) on the host computer. EX1001, 3:27-32, FIG.1 (below with annotations):

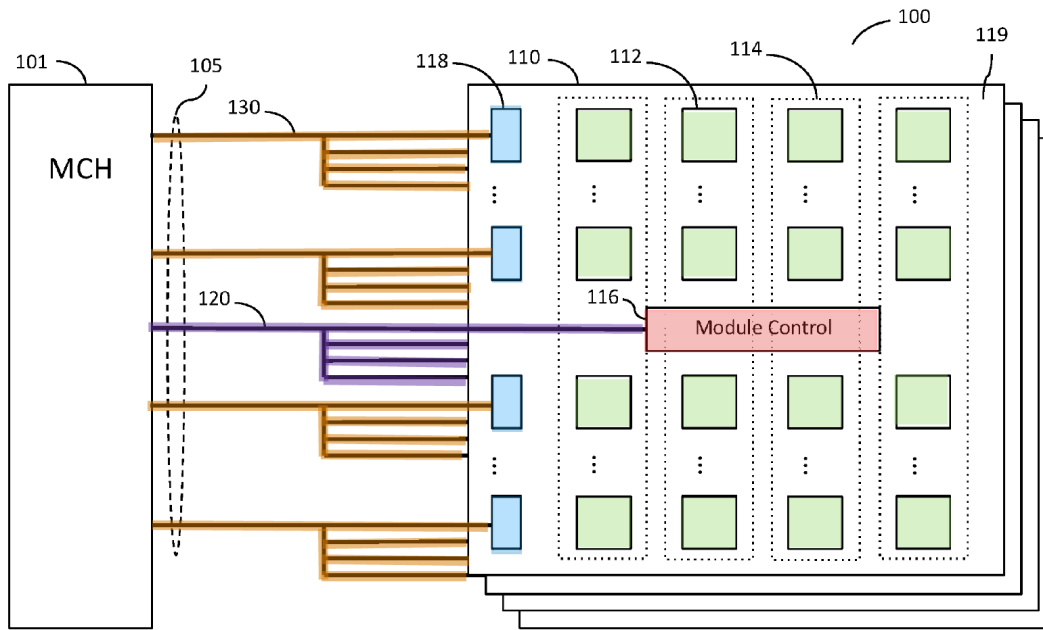
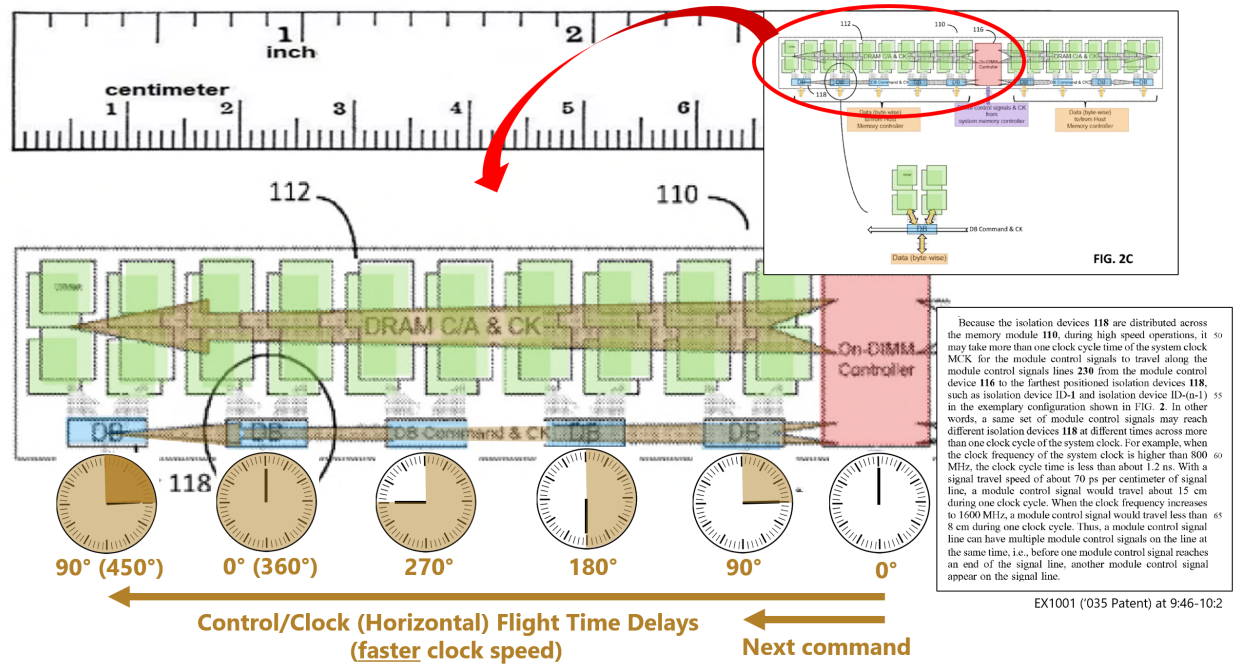


FIG. 1

As shown in Figures 1 and 2C above, a memory bus (105) connects the memory controller (MCH) (101) and the memory module (110), with control/address (C/A) signal lines (120, purple) between the memory controller (101) and the module control device (116, red), and data/strobe signal lines (130, orange) on the y-axis of Figure 2C between the memory controller and each memory device (112, green) via each data buffer (118, blue). EX1001, 4:18-30. The memory controller (MCH) (101) issues C/A signals (on lines 120, purple) to the memory module (110) via the module control device (116, red), and sends and receives data/strobe signals (on lines 130, orange) to/from the memory devices (112, green) via the data buffers (118, blue). *Id.* The module control device (red) receives the system memory commands represented by a set of system C/A signals

from the memory controller (MCH) and generates from them module command signals and module control signals which are transmitted on the x-axis of Figure 2C to the memory devices and data buffers via signal lines. EX1001, 4:63-5:5, 5:55-63, *see also id.* FIGS.2A-2B, 6:10-26, 4:58-62.

The '035 Patent notes that because the data buffers (blue) and their associated memory devices (green) are distributed horizontally across the x-axis of the memory module, “a same set of module control signals may reach different [data buffers (blue)] at different times across more than one clock cycle of the system clock.” EX1001, 9:49-10:3, 10:4-18. This concept is illustrated below by comparing a ruler to Figure 2C of the '035 Patent, where the left-most data buffer in blue is receiving a first control signal at 1.25 clock cycles (i.e., 450°) after it was sent by the module controller (red), while the right-most data buffer in blue is receiving a second control signal at the same time at 0.25 clock cycles (i.e., 90°) after it was sent by the module controller (red). EX1003, ¶55.



Id.

The '035 Patent discloses that each data buffer (blue above) can determine a time interval based upon the reception of signals to the data buffer during a write operation—in particular, the difference (EWD) between reception of module control signal on the x-axis corresponding to a **write command** (W/C, e.g., at t3 or t3' depending on how far the data buffer is from the module controller on the x-axis) and reception of the corresponding data strobe (DQS1) on the y-axis (shown in Fig. 12A, below, e.g., at t4)—which can then be used to adjust signal timing during memory **read operations** (shown in Fig. 12B, annotated below). EX1001, 15:22-45, 15:61-16:4, FIGs.12A-12B:

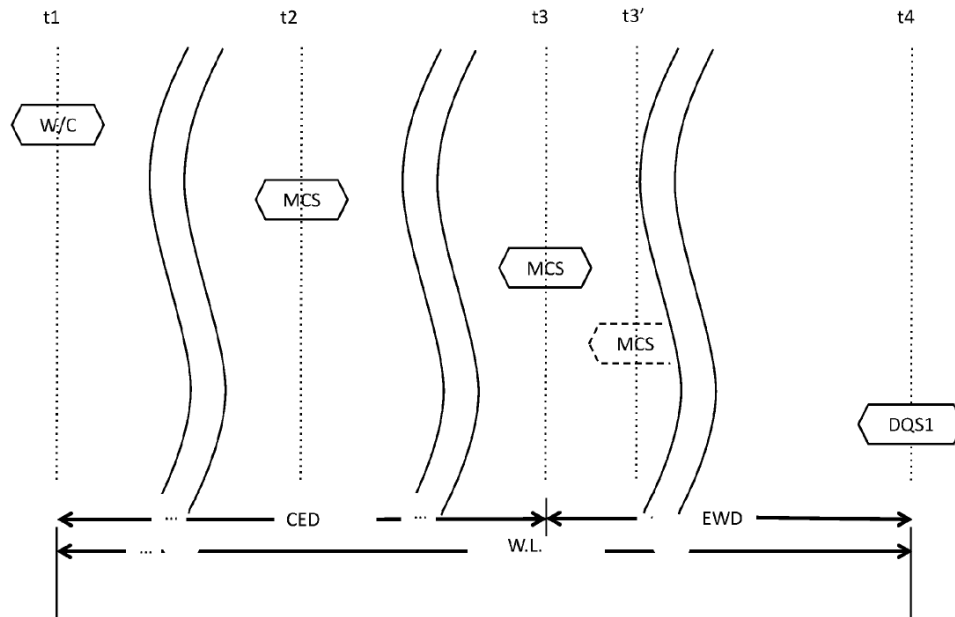


FIG. 12A

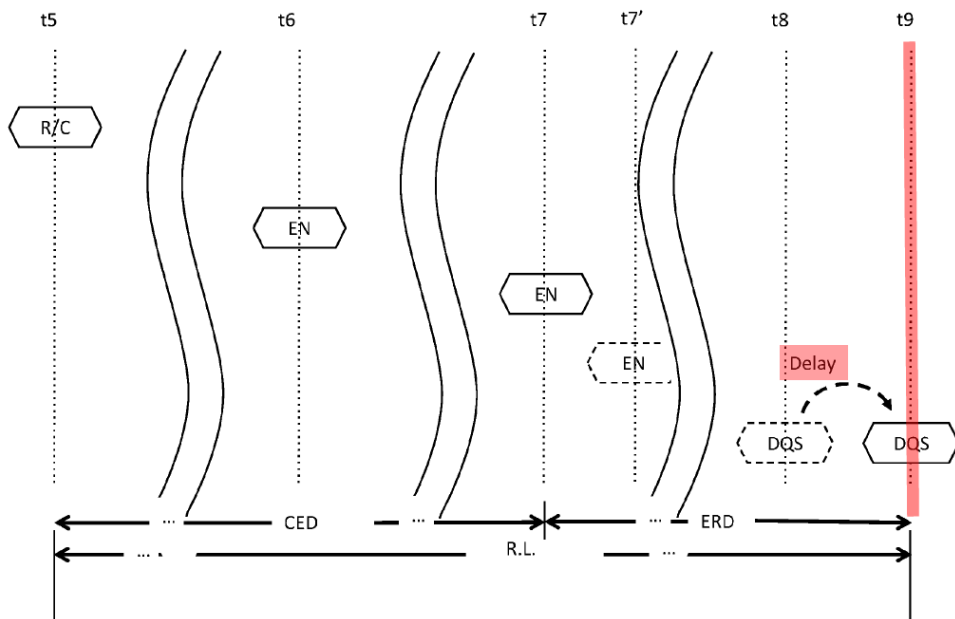


FIG. 12B

2. Prosecution History

During prosecution of the '035 Patent, the Examiner did not consider the references that form the Grounds in this Petition: Osanai (EX1005), Butt

Petition for *Inter Partes* Review of U.S. Patent No. 9,824,035

(EX1029), Tokuhiro (EX1006), Ellsberry (EX1007), and Kim (EX1008). *See generally* EX1001; EX1002; EX1003, ¶71.

The Osanai reference in Ground 1 (EX1005) is materially identical in relevant aspects to two other references referred to as Saito (EX1030) and Hiraishi (EX1056). EX1003, ¶¶64-65. Neither Saito nor Hiraishi was cited during prosecution of the '035 Patent. *See generally* EX1001; EX1002.

The '035 Patent is a continuation of a patent that is a continuation of U.S. Patent No. 9,128,632 (“the '632 Patent”). EX1001, 1-2. The '632 Patent was previously the subject of an IPR petition filed by SK hynix (IPR2017-00730), challenging certain claims as obvious over Saito (EX1030) combined with US7,808,849 (EX1027) and further in view of Kim (EX1008). EX1012, 2. The Board denied institution on the basis of specific limitations in claim 1 of the '632 Patent not found in the '035 Patent. EX1014, 12-13; EX1003, ¶¶63, 67. During prosecution of the '035 Patent, Netlist did not disclose to the Examiner the Board's decision in IPR2017-00730, the prior art discussed by the Board, or any references forming the Grounds in this Petition. EX1003, ¶¶64, 71; EX1002.

In late 2021, Netlist accused Samsung (the Petitioner here) of infringing U.S. Patent No. 10,860,506 (EX1046), which is the grandchild of the '035 Patent. *See* EX1045, ¶ 99, p.258. Netlist did not accuse Samsung of infringing the '035 Patent. In response, on March 22, 2022, Samsung filed IPR2022-00711 against the

'506 Patent, supported by an expert declaration by Robert Wedig, Ph.D. (the same expert here). See EX1045. Dr. Wedig's declaration in March 2022 asserted that all claims of the '506 Patent were invalid in light of the same prior-art combination presented by Ground 1 here: Hiraishi (which is materially identical to Osanai here, see EX1003, ¶¶64-65) in combination with Butt and Tokuhiro. See EX1045, p.187, pp.225-32. In its Final Written Decision, the Board found all claims of the '506 Patent obvious over the combination of Hiraishi (which has the same relevant disclosure as Osanai, part of Ground 1 here), Butt (part of Ground 1 here), Ellsberry (part of Ground 2 here), and Kim (part of Ground 3 here). EX1068, 32-33; EX1069 (denying rehearing). The Board did not reach the Grounds that further included Tokuhiro (part of Ground 1 here). EX1068, 32 n.12.

On June 20, 2023 — long after Samsung had filed IPR2022-00711 above against the '506 Patent — the Board issued a Final Written Decision in IPR2022-00236 filed by Micron (without the involvement of Samsung) against the '035 Patent. EX1066; EX1067. The Board found claims 1, 10-13, and 21-22 of the '035 Patent obvious in light of the combination of Osanai and Tokuhiro, and those claims were cancelled. *Id.*; EX1001, 41. But based on a narrow claim construction that neither side had proposed, and thus which the petition had not addressed, the Board did not find claims 2 and 6 of the '035 Patent obvious. EX1066, 10 ("Patent Owner...does not seek construction of any terms"), 43-45

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(“Patent Owner does not separately dispute claim 2 and instead relies on its arguments for claim 1 [which the Board rejected in finding claim 1 obvious]....Nevertheless, we determine Petitioner has not sufficiently shown that the combination of Osanai and Tokuhiro teach the limitations of claim 2.”). For claims 2 and 6 of the ’035 Patent, the Board did not consider the combination for Ground 1 here (involving Butt) that Dr. Wedig had previously filed with the Board in March 2022, since Dr. Wedig and Samsung were not involved in IPR2022-00236 against the ’035 Patent. *See id.*

In 2023 — shortly after the Board instituted Samsung’s IPR2022-00711 against the ’506 Patent, which is the grandchild of the ’035 Patent — Netlist accused Samsung of infringing U.S. Patent No. 10,268,608, which is the child of the ’035 Patent. *See* EX1057; EX1058, p.247. Again Netlist did not accuse Samsung of infringing the ’035 Patent. In response, Samsung filed IPR2023-00847 against the ’608 Patent supported by an expert declaration by Dr. Wedig relying on the same prior-art references as in IPR2022-00711. *See* EX1058. However, the Board found the challenged claims of the ’608 Patent not invalid based on a narrow construction for “data path,” which the Board found differed from “data paths” (plural) in the ’035 Patent. EX1060, 10-24, 40-42, 69-70, 72-73. In particular, the Board held that the prior art to the ’608 Patent did not teach a “data path” including “a delay circuit” under a narrow claim construction where

the “data path” is “in the data signal line” and thus does not include “strobe signals.” EX1060, 17, 69-70. The Board contrasted the claims in the ’608 Patent with the claims of the ’035 Patent: “Claim 1 of the ’035 patent explicitly recites that the data paths have data and strobe signals transmitted on them. That is unlike claim 1 of the ’608 patent at issue here....” *Id.* at 20-21. Thus, the Board concluded that “claim 1 of the ’608 patent and claim 1 of the ’035 patent [] recite different ‘data paths.’” EX1060, 21. Samsung has appealed the Board’s narrow claim construction for the ’608 Patent to the Federal Circuit, which will hear arguments on December 5, 2025. EX1061-64; EX1003, ¶79.

On September 30, 2025 — shortly after Samsung filed its reply brief on appeal explaining why the Board’s narrow construction for “data path” in the ’608 Patent was incorrect, *see* EX1064, 9-28 — Netlist accused Samsung of infringing the ’035 Patent for the first time. EX1086, p.34, ¶ 111.

E. Estoppel from IPRs against other Netlist patents

As a result of the Final Written Decisions against Netlist in IPR2022-00711 (’506 Patent) and IPR2022-00236 (’035 Patent) discussed above — which, as discussed below in the limitation-by-limitation analysis, found limitations similar to those in the remaining claims of the ’035 Patent obvious in light of Osanai/Hiraishi, Butt, Tokuhiro, Ellsberry, and/or Kim, which are the same references presented here — Netlist is “precluded from taking action inconsistent

with [those] adverse judgment[s].” 37 C.F.R. §42.73(d)(3); *SoftView LLC v. Apple Inc.*, 108 F.4th 1366, 1373 (Fed. Cir. 2024) (“[S]ection 42.73(d)(3) . . . ensur[es] the integrity of the proceedings before the PTO by preventing actions that would undermine the outcomes of those proceedings.”). Netlist is also “bound...by any subsidiary factual determinations that were actually litigated and essential to the judgment[s]” in those prior proceedings. *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, at 18 (PTAB July 16, 2019); *see also B & B Hardware, Inc. v. Hargis Indus., Inc.*, 575 U.S. 138, 148 (2015) (following the Restatement); Restatement (Second) of Judgments §§13, 27.

F. Claim Construction

Petitioner respectfully submits that the Board need not expressly construe any claim term in the '035 Patent because the prior art invalidates the claims regardless of their precise construction. *See* 37 C.F.R. §42.100(b); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (“we need only construe terms ‘that are in controversy, and only to the extent necessary to resolve the controversy’”). Petitioner merely identifies here examples of how various claim terms are used in the '035 Patent, and then in § VI below Petitioner shows how the claim terms are taught by the prior art:

- “*memory operation*”: EX1001, 3:28-32, 5:55-60; EX1003, ¶¶88-91; *see also* EX1048, 2; EX1049, 10-11; EX1066, 31-33.

- “*memory module*”: EX1001, 1:47-52; EX1023, p.334; EX1003, ¶¶92-93.
- “*memory controller*”: EX1001, 4:44-47; EX1003, ¶94.
- “*memory bus*”: EX1001, 4:47-56; EX1003, ¶95.
- “*memory command signals*”: EX1001, 3:27-36; EX1003, ¶¶96-97.
- “*module command signals*”: EX1001, 3:39-42, 3:42-44, 5:55-60, 5:25-39; EX1003, ¶¶98-99.
- “*module control signals*”: EX1001, 3:39-42, 3:42-48, 5:40-48; EX1003, ¶¶100-101.
- “*metastability*”: EX1001, 9:39-42; EX1003, ¶¶102-103.

In IPR2022-00236 involving the '035 Patent, discussed above (pp.19-20), the Board stated that “no terms need to be construed,” EX1066, 10, but the Board interpreted “*memory operation*” to encompass both write operations and write leveling operations, *id.* 31-33, while the Board interpreted “*memory write operation*” in claims 2 and 6 to exclude write leveling operations, *id.* 43-45. As shown in detail below, the Grounds presented in this Petition — which were not considered by the Board in IPR2022-00236 — disclose all challenged limitations, even under the Board’s narrow interpretation for “*memory write operation*” in claims 2 and 6.

In IPR2022-00711 involving the related '506 Patent, the Board did not construe any claims, see EX1068, 6, but in related district court litigation, a phrase not found in the '035 Patent was construed, which does not affect Petitioner's arguments here, see EX1050, 34; EX1003, ¶86. In addition, the parties agreed that the preamble of the '506 Patent was limiting, and that "one or more previous operations" referred to "previous *memory* operations," which Netlist contended were not limited to "ones involving writing to or reading from a DRAM." EX1048, 2; EX1049, 10-11. Petitioner's arguments here are consistent with those agreements and Netlist's contentions for the related '506 Patent. EX1003, ¶91.

As discussed above (pp.20-21), the Board construed "data path" narrowly in IPR2023-00847 involving the related '608 Patent, but the Board expressly indicated that this narrow construction does not apply to the '035 Patent, so it does not affect Petitioner's arguments here.

V. OVERVIEW OF THE PRIOR ART

A. U.S. Pub. No. 2010/0312925 ("Osanai") (EX1005)

Osanai, published on December 9, 2010, is prior art under at least pre-AIA §102(b). EX1005. Osanai was not cited or discussed during prosecution, EX1002, but was discussed in IPR2022-00236 of the '035 Patent, and has a materially identical disclosure to Hiraishi discussed in IPR2022-00711 of the related '506 Patent, *supra* pp.17-21.

Like the '035 Patent, Osanai discloses an information processing system 10 including a memory system (20) with a memory module (100) and a memory controller ("memory control hub," MCH 12) for controlling the memory module. EX1005, ¶¶[0069]-[0071], [0073]-[0074], Figs.2-3 (below).

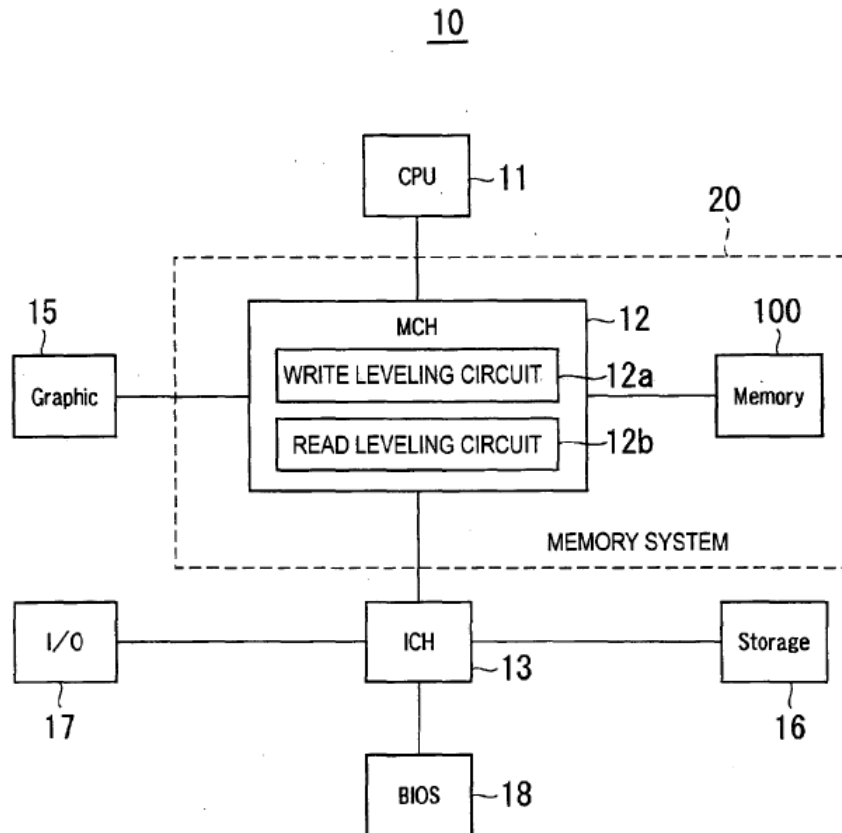


FIG.2

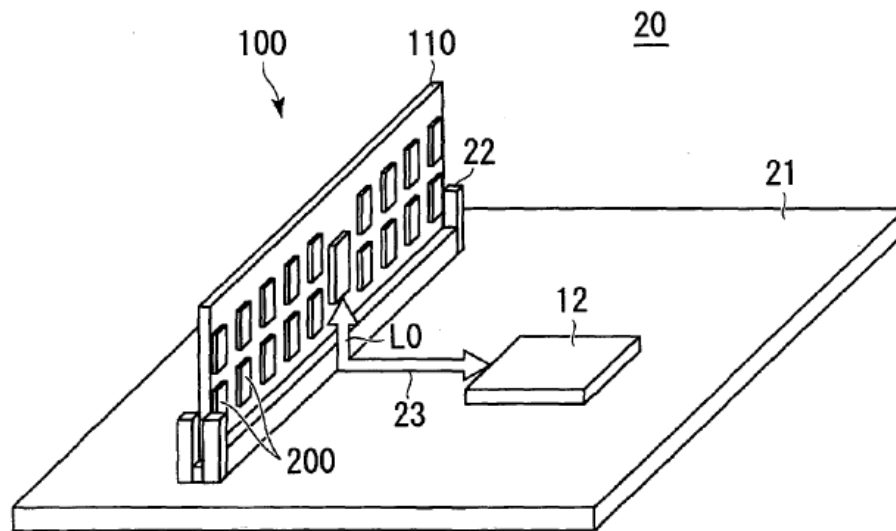
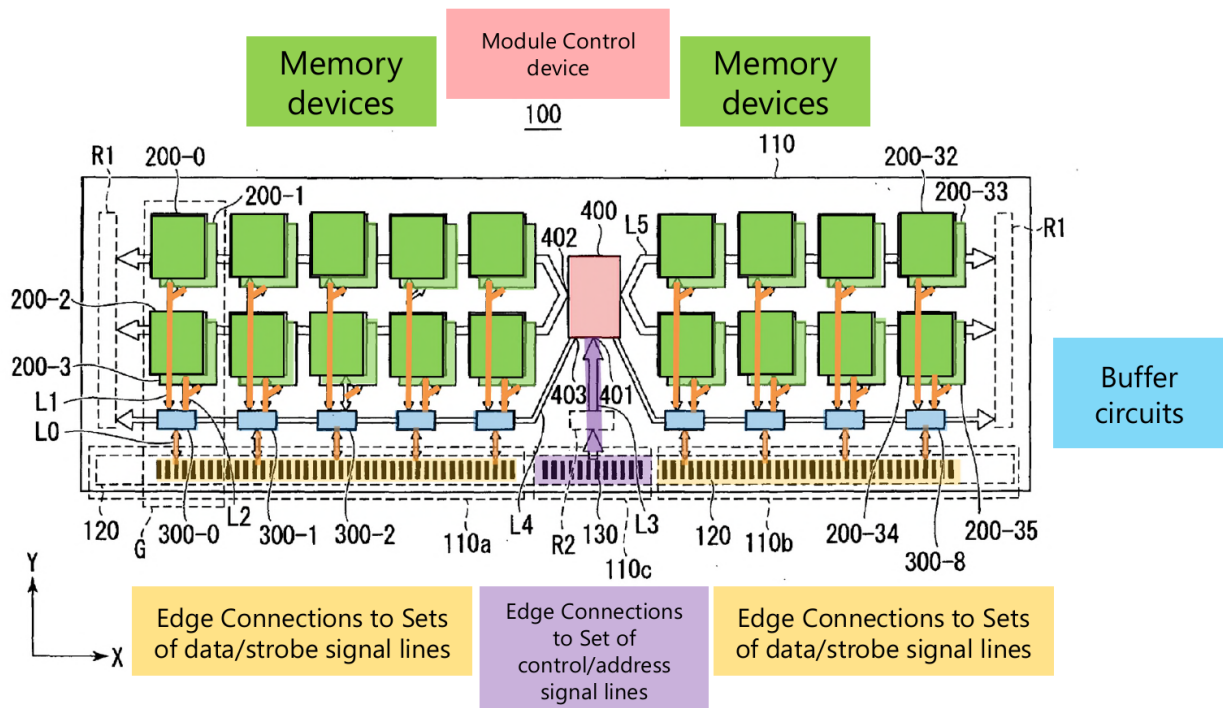


FIG.3

Annotated Figure 1 of Osanai below illustrates an implementation of the memory module 100, which is nearly identical to the memory module of the '035 Patent discussed above (p.13). EX1005, ¶¶[0051]-[0052], [0054]-[0055], [0061], [0065]-[0066], Fig.1 (below, annotated).



As shown above, Osanai's memory module can include 36 memory devices (green) in a 4-rank configuration. EX1005, ¶¶[0052]-[0054], [0057]-[0058], [0061]; *see also* EX1005, ¶¶[0055], [0065] (describing connections to command/address/control register buffer (400, red)).

Annotated Figure 7 below is a connection diagram of the memory module 100 and explains the basic operation. EX1005, ¶¶[0108], [0113], Fig.7 (below, annotated).

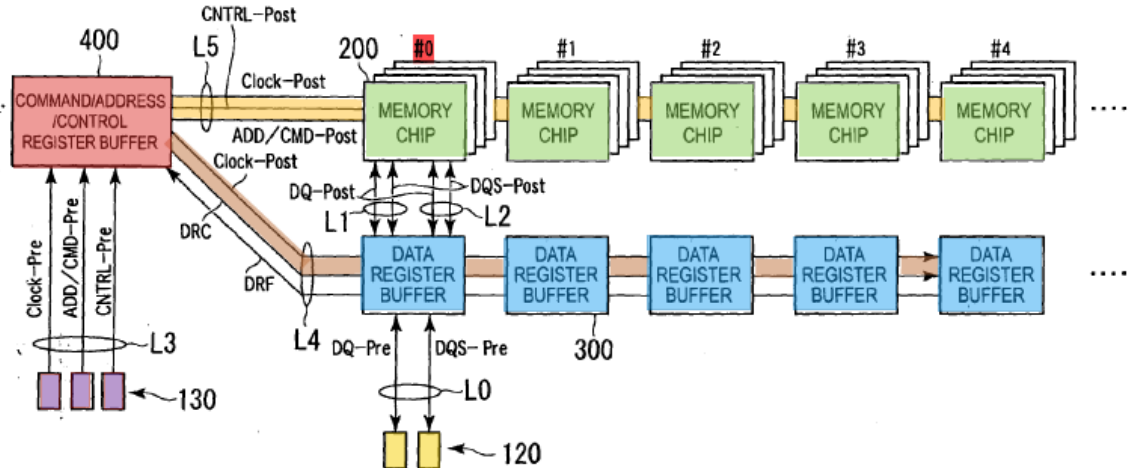


FIG.7

As shown above and below, the “command/address/control register buffer” (400, red) “receives the command signal, the address signal, the control signal, and the clock signal” from the memory controller at an input terminal 401 (purple, below), “buffers the signals, and supplies the signals” at an output terminal 402 (orange, below) to the memory chips (200, green, above). EX1005, ¶¶[0066], [0067]. Simultaneously, the “command/address/control register buffer” (400, red) “generates a control signal” and supplies it at the output terminal 403 (brown, below) to the data register buffers (300, blue). EX1005, ¶¶[0066], [0102]-[0103], FIG.6 (below, annotated).

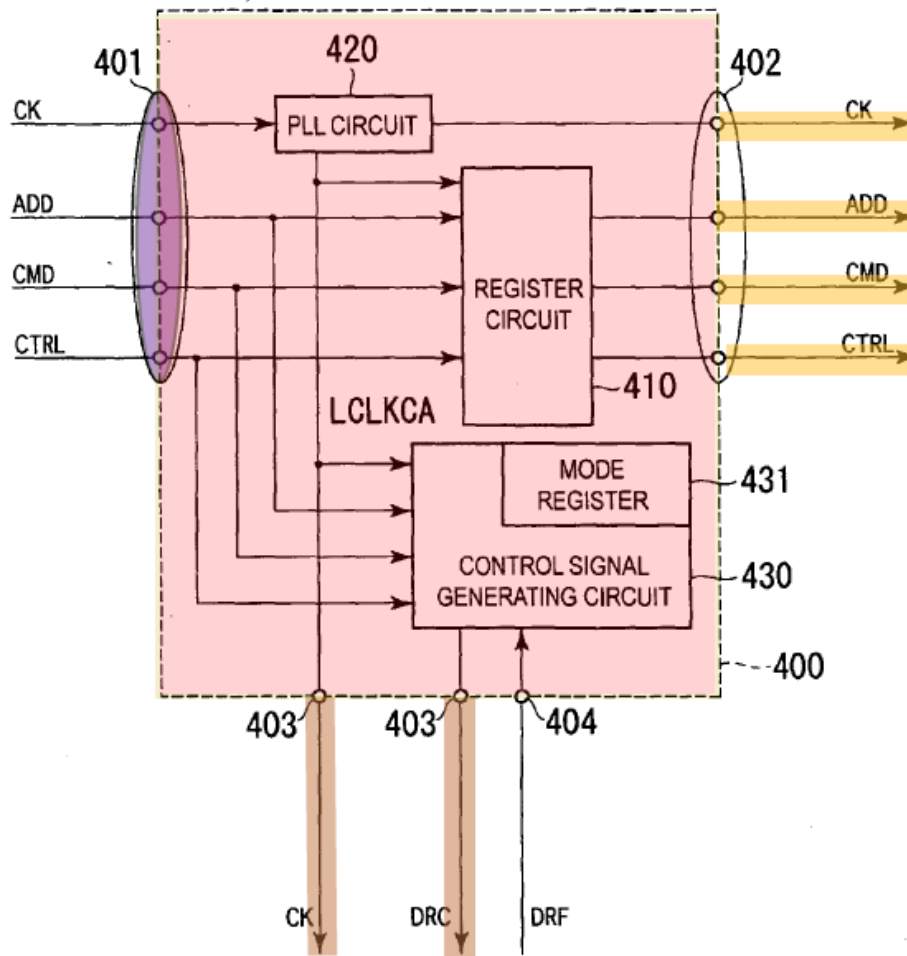


FIG.6

Osanai recognizes that there may be signal timing discrepancies because of high-speed operation and differing distances of the “memory chips” (200, green) and “data register buffers” (300, blue) from the “command/address/control register buffer” (400, red). EX1005, ¶¶[0096], [0110]. Accordingly, Osanai’s memory module makes “timing adjustments” to account for these timing discrepancies during initialization by performing write leveling and read leveling operations. *Id.*, ¶¶[0146]-[0147]. Each group of memory chips/data register buffer performs two

sets of write and read leveling operations, one “between the data register buffer 300 and the memory chip 200” referred to as “Step S4,” *id.*, ¶[0146], and one “between the memory controller and the data register buffer 300” referred to as “Step S5,” *id.*, ¶[0147]; *see also* ¶¶[0148], [0153], [0090]-[0091], [0093], Fig.5 (annotated below, showing specific implementation of the register buffer 300 for read/write leveling).

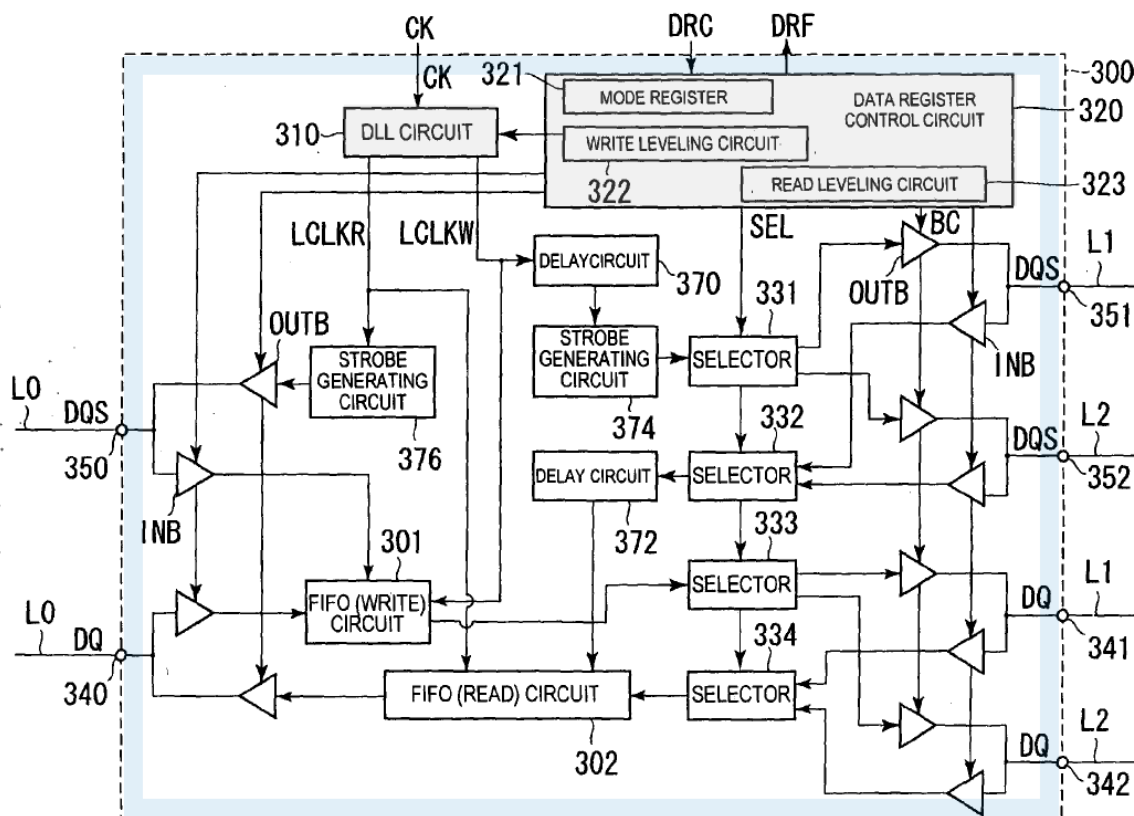


FIG.5

B. U.S. Pub. No. 2007/0008791 (“Butt”) (EX1029)

Butt, published in 2007, is prior art under at least pre-AIA §102(b).

EX1029. Butt was not cited or discussed during prosecution, EX1002, but was discussed in IPR2022-00711 of the related ’506 Patent, *supra* pp.17-21.

Butt discloses the details for delaying a DQS strobe signal during initialization so that it is properly aligned with the DQ data signal (as required by the JEDEC standards discussed above, pp.4-5). See EX1029, ¶¶[0003]-[0005], [0014], [0017]-[0018], [0022], [0035], [0045]-[0046], Figs.2, 5. Butt further teaches using normal read/write operations during initialization. EX1029, ¶¶[0038], [0044], claims 11, 18.

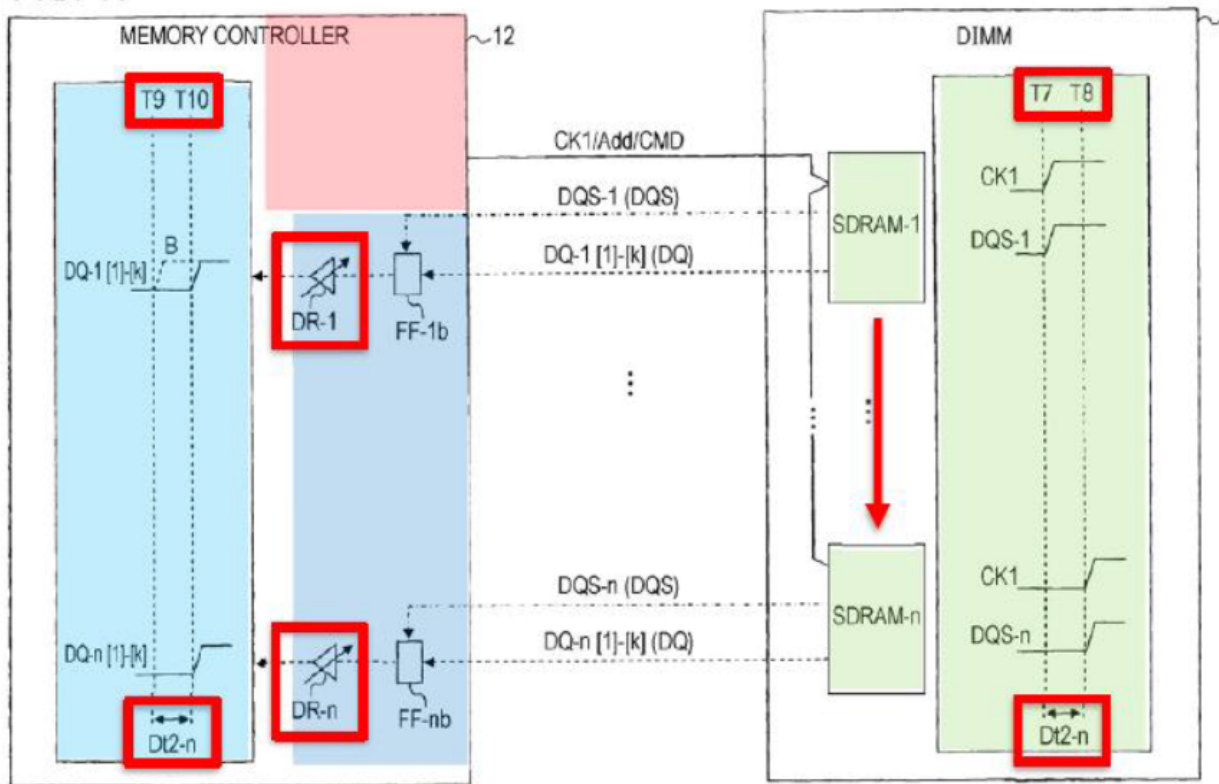
C. U.S. Patent No. 8,020,022 (“Tokuhiko”) (EX1006)

Tokuhiko, issued September 13, 2011, is prior art under at least pre-AIA §102(a). EX1006. Tokuhiko was not cited or discussed during prosecution, EX1002, but was discussed in IPR2022-00236 of the ’035 Patent, *supra* pp.17-21.

Tokuhiko recognizes the problems of fly-by delays, for example in DDR3 memory systems, particularly where the delay is greater than one data period, which is half a clock cycle for DDR memories. EX1006, 1:63-29, 2:10-13, 2:54-59, 3:1-9, 3:10-13; *see also* EX1020, 42 (JEDEC DDR3 standard for write leveling to address fly-by delays), 160 (“tCK”); EX1077, 6 (“tCK”); EX1021, 333-34 (“DDR”); *supra* pp.9-12.

As a solution to this problem, Tokuhiro proposes determining a first delay utilizing the **write** leveling function, and using this delay not just for write operations but also to delay the transmission of data during **read** operations (e.g., by using delay elements DR-1 to DR-n below) to realign the read data pieces from the different memories (e.g., SDRAM-1 to SDRAM-n below in green). EX1006, 3:15-26, Fig.11 (below, annotated).

FIG. 11

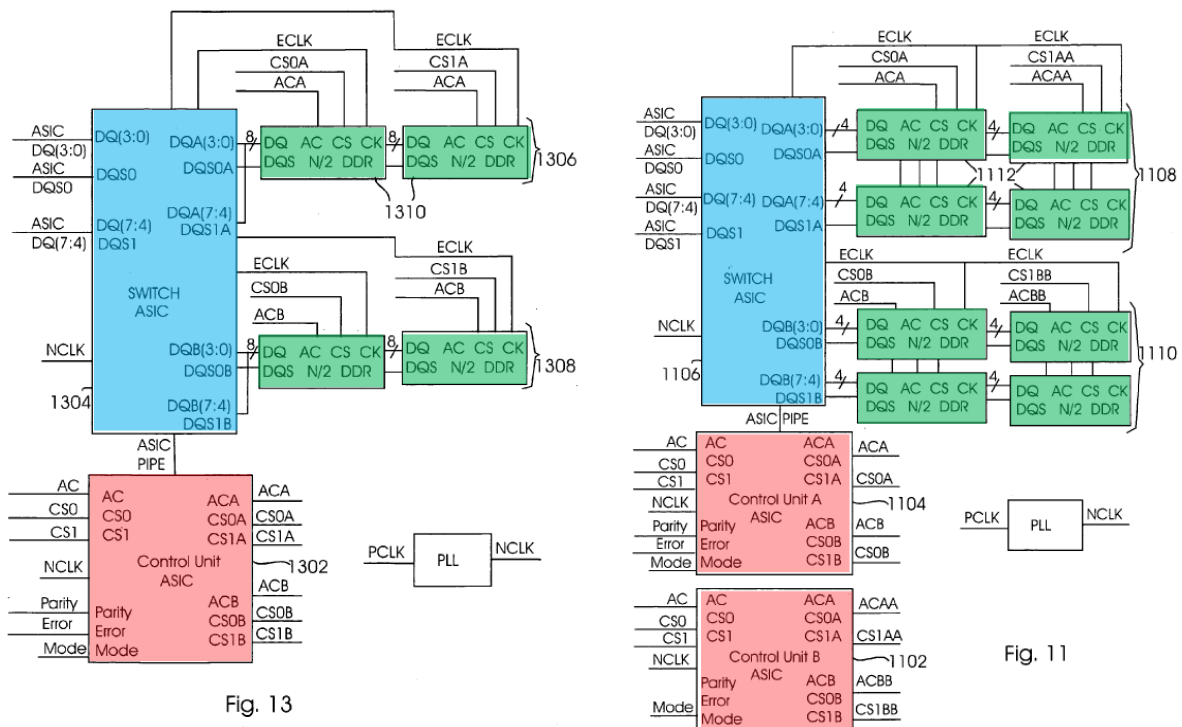


D. U.S. Pub. No. 2006/0277355 (“Ellsberry”) (EX1007)

Ellsberry, published December 7, 2006, is prior art under at least pre-AIA §102(b). EX1007. Ellsberry was not cited or discussed during prosecution,

EX1002, but was discussed in IPR2022-00711 of the related '506 Patent, *supra* pp.17-21.

Ellsberry discloses a memory module with the same distributed buffer architecture and four ranks of memories as Osanai and the '035 Patent, and as shown below additionally expressly describes modules with 8-bit wide data buffers (blue) and with either 8-bit wide memory devices (EX1007, Figs.2, 5, 13 (below left, green)) or pairs of 4-bit wide memory devices (EX1007, Figs.2, 6, 11 (below right, green)), as confirmed by the Board in a Final Written Decision against Netlist. EX1007, ¶[0056]; EX1015, pp.57, 60, 66, 68, 77, 81.



E. U.S. Patent No. 6,184,701 (“Kim”) (EX1008)

Kim, issued February 6, 2001, is prior art under at least pre-AIA §102(b). EX1008. Kim was not cited or discussed during prosecution, EX1002, but was discussed in IPR2022-00711 of the related ’506 Patent, *supra* pp.17-21.

Kim recognizes the problem of generating an output in a metastable state, which “may result in device failure.” EX1008, 1:21-31. To solve that problem, Kim discloses “a metastability detection/prevention circuit 20” to be incorporated with any “main active circuit 10” in need thereof. EX1008, 2:21-22, 2:30-31, 2:3-37.

VI. ARGUMENT

As explained below, claims 2-9 and 14-20 of the ’035 Patent are obvious in light of Grounds 1-3. Grounds 1-3 are consistent with the grounds that Petitioner presented in IPR2022-00711 of the related ’506 Patent, *see* EX1045, pp.187, 225-32, before the Board’s Final Written Decision in IPR2022-00236 of the ’035 Patent, *see supra* pp.17-21. Also, as explained below, Grounds 1-3 satisfy the Board’s narrow interpretation of “*memory write operation*” in IPR2022-00236, which excluded write leveling operations, *see* EX1066, 44-45; *supra* pp.22-23, because Grounds 1-3 teach using normal write operations during initialization, not just write leveling operations.

A. Ground 1 combination: Osanai (EX1005) + Butt (EX1029) + Tokuhiko (EX1006)

1. Motivations to combine Osanai, Butt, and Tokuhiko

Osanai, Butt, and Tokuhiko are analogous art to the '035 Patent since each is directed to improving memory systems using memory modules in which the memory chips are arranged in a fly-by configuration, such as modules with DDR3 memory devices. EX1003, ¶139. A POSITA would have been motivated to combine Osanai, Butt, and Tokuhiko for a number of reasons, discussed below. EX1003, ¶¶139-168. The Board has already agreed that a POSITA would have been motivated to combine Butt with Hiraishi (which is materially identical to Osanai here), see EX1068, 14-19, and also would have been motivated to combine Tokuhiko with Osanai, see EX1066, 41.

a) *Motivation to combine with Butt: Butt discloses read training that can establish optimum strobe alignment while Osanai and Tokuhiko are silent about optimizing strobe alignment*

As discussed above (pp.3-7), it is important to keep the DQ data signal properly aligned with the DQS strobe signal. Although DQ and DQS are supposed to remain aligned, in reality the two signals may fall out of alignment for various reasons. EX1075, 163:9-167:17. Butt teaches a solution to that problem.

Butt teaches a specific technique to precisely align DQ data and DQS strobe signals during initialization, EX1029, ¶[0002], which is not specifically disclosed by Osanai or Tokuhiko, see, e.g., EX1005, ¶¶[0097] (“DQS [] delayed by about 90

degrees”), [0167], Fig.5; EX1006, Fig.5; EX1003, ¶¶140-143. Specifically, Butt teaches a training method that determines “optimum offset delay [of strobe signals] for each datapath” by executing “a routine...that writes to, reads from, and compares a selected data pattern to a selected range of the DDR memory.” EX1029, ¶¶[0038], [0044], claims 11, 18, [0037] (“[a] write/read/compare test”), [0033] (“optimum DQS strobe settings”), [0035], Fig.5(below)-7; EX1003, ¶144.

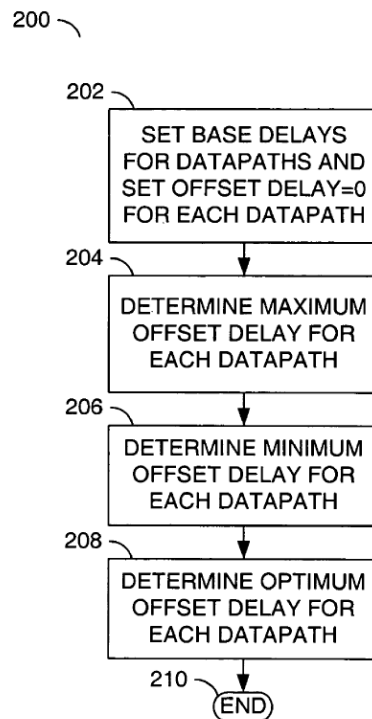


FIG. 5

Thus, a POSITA would have been motivated to implement Butt’s strobe signal optimization technique in the memory module of Osanai and Tokuhiro (discussed further below), which “enables a reliable data read operation for high

speed applications.” EX1029, ¶[0036]; EX1003, ¶145. Further, the combination involves a simple application of known techniques to improve similar technology in Osanai and Tokuhiro. *Id.* In IPR2022-00711 of the related ’506 Patent, the Board agreed with this motivation to combine Butt with Hiraishi (which is materially identical to Osanai). EX1068, 14-19.

b) Motivation to combine with Tokuhiro

While implementing Butt’s teaching above ensures proper alignment of DQ data and DQS strobe signals (which travel on the y-axis), those signals also must be properly aligned with the clock (CK) signals (which travel on the x-axis in a fly-by topology), as discussed above (pp.3-7). To solve that problem, a POSITA would have been further motivated to further combine with Tokuhiro for at least three reasons discussed below. EX1003, ¶146.

Tokuhiro teaches that DDR3 memory modules employ fly-by topology, EX1006, 1:22-33, 1:63-2:9, Fig.1, which causes the clock, command, and address signals on the x-axis to reach different DDR3 memory devices at different times as discussed above (pp.9-12). The fly-by delays affect meeting JEDEC timing requirements and proper memory operations, especially when these delays are greater than one data period, which is half a clock cycle for DDR memories. EX1006, 1:22-26 (referencing DDR3 JEDEC standard), 3:9-12 (fly-by delays “greater than a typical data period of the DDR3 memory interface”). Although the

JEDEC standards specify a write leveling procedure to address fly-by delays for write data, Tokuhiro points out they do not address those delay for read data.

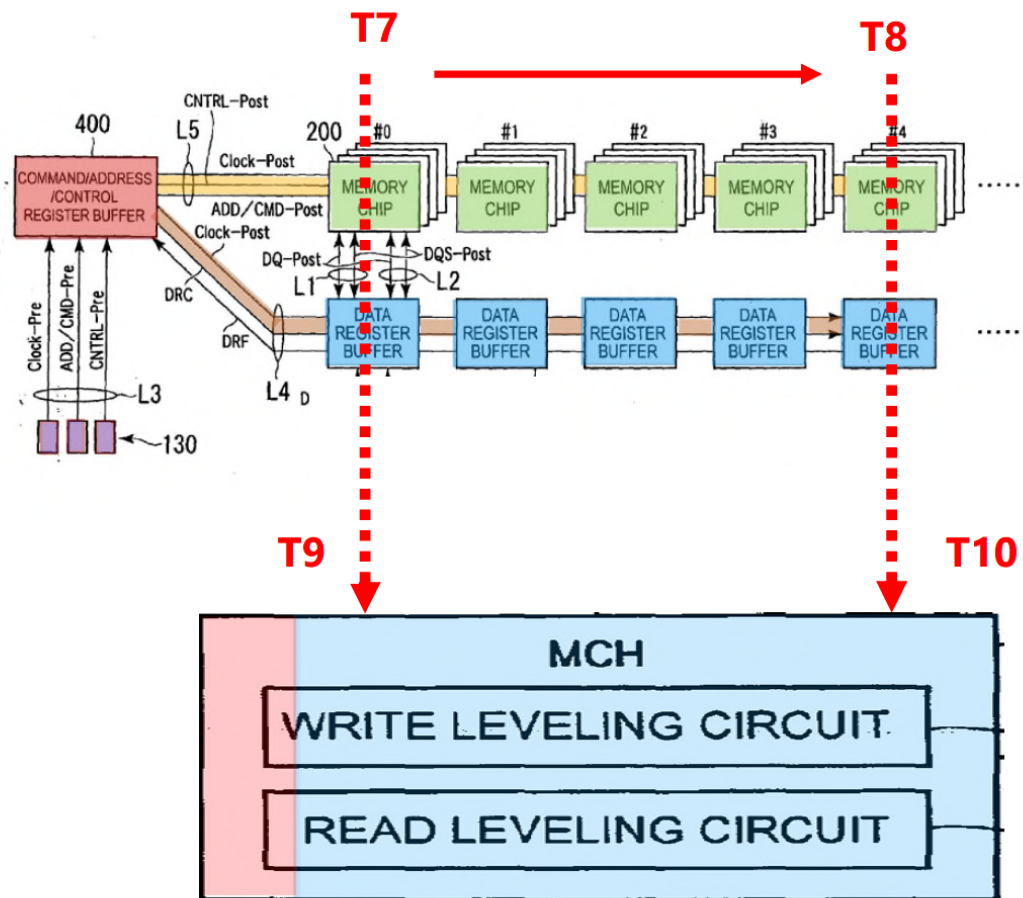
EX1006, 2:54-59; EX1020, 42 (DDR3 supporting “write leveling” feature);

EX1003, ¶¶130-131. Thus, Tokuhiro teaches techniques to solve the problem of large fly-by delays for read data without requiring “a special mechanism, such as an FIFO” in the system memory controller. EX1006, 18:66-19:7. The read “delay time...is set based on the [] delay time” obtained during “the write operation.”

EX1006, 3:16-26; EX1003, ¶¶132-133. A POSITA would have been motivated to combine Tokuhiro with Osanai and Butt for at least three reasons discussed below.

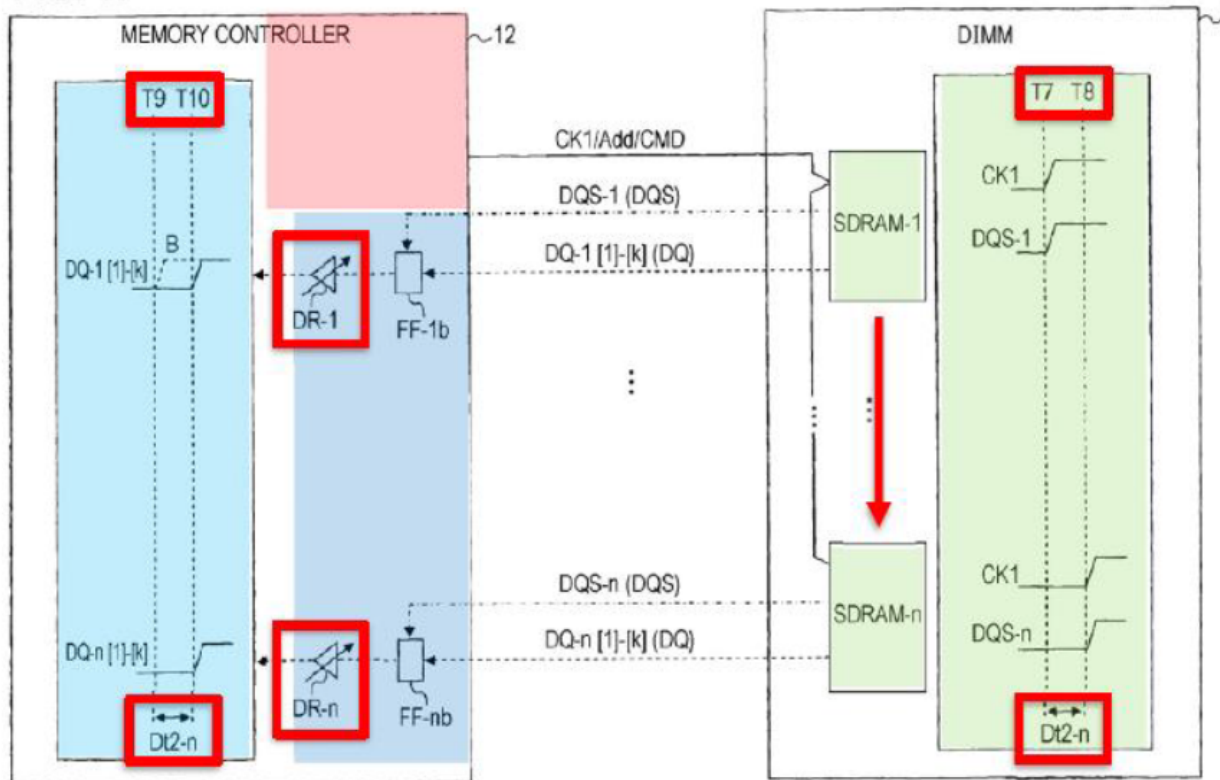
- (1) ***First motivation: Tokuhiro teaches calculating read delays based on the delays for write operations, which is more efficient than Osanai’s technique of performing read leveling independent of the write delays***

Both Osanai and Tokuhiro have a similar “fly-by” topology for the memory devices (green below) where, for example, the clock and command signals reach the closest memory device at time T7 and the furthest memory device at time T8, meaning that read data would reach the system memory controller at different times (e.g., T9 to T10) if no timing adjustments were made:



EX1003, ¶155 (annotating EX1005, Figs.2, 7)

FIG. 11



EX1003, ¶154 (annotating EX1006, Fig.11).

As shown below, Osanai discloses data register buffers on the memory module (blue) that affect the timing of DQ data and DQS strobe signals to/from the memory devices (green). EX1005, ¶[0110], Fig.7 (annotated below).

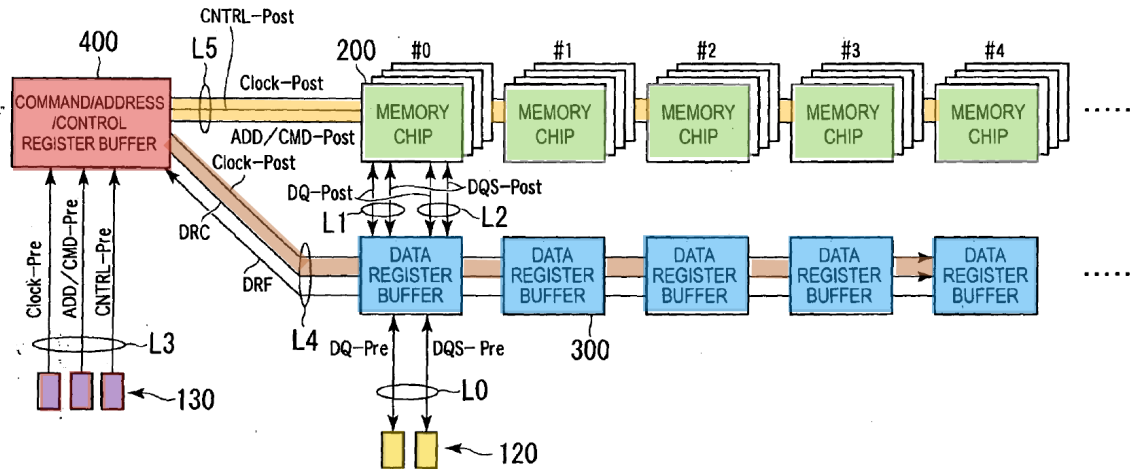
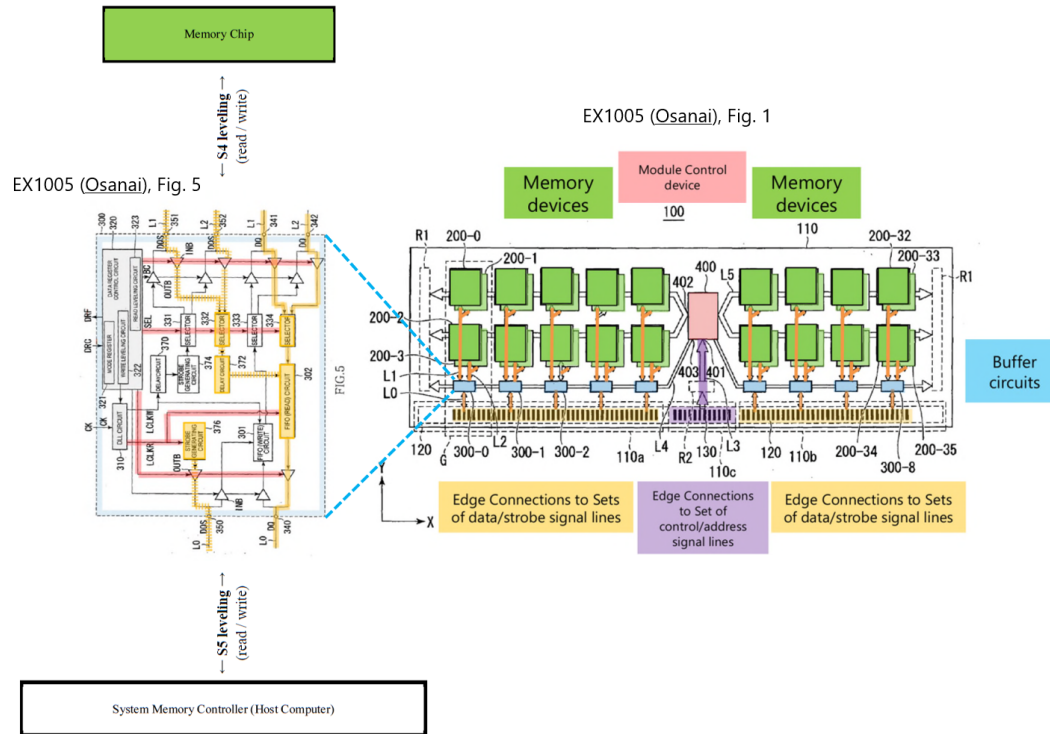


FIG.7

Osanai teaches that the data buffers (blue) each adjust the timing of DQ/DQS signals using delays calculated by independent read and write leveling operations during steps “S4” (upper left in the annotation below) and “S5” (below left in the annotation below) at initialization:



EX1003, ¶¶148-149 (annotating EX1005, Figs.1, 5, 13). For example, Osanai teaches using a normal read operation to measure “time A” and “time B” during read leveling at steps S4 and S5, as shown below, and to use those measurements to adjust the timing of the DQ/DQS signals for read operations (but not write operations). EX1003, ¶¶150-152; EX1005, ¶¶[0146], [0157], [0167], FIGs.15 (“S4” read leveling below), Fig.17 (“S5” read leveling below).

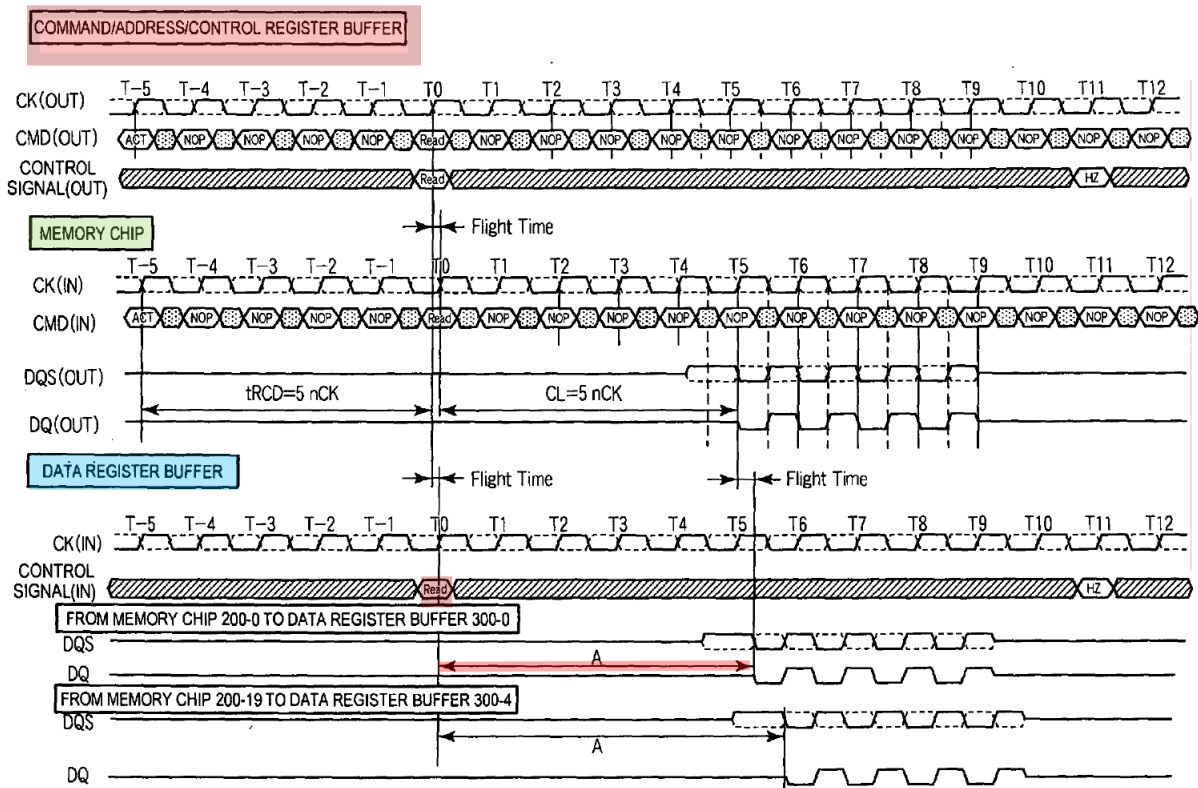
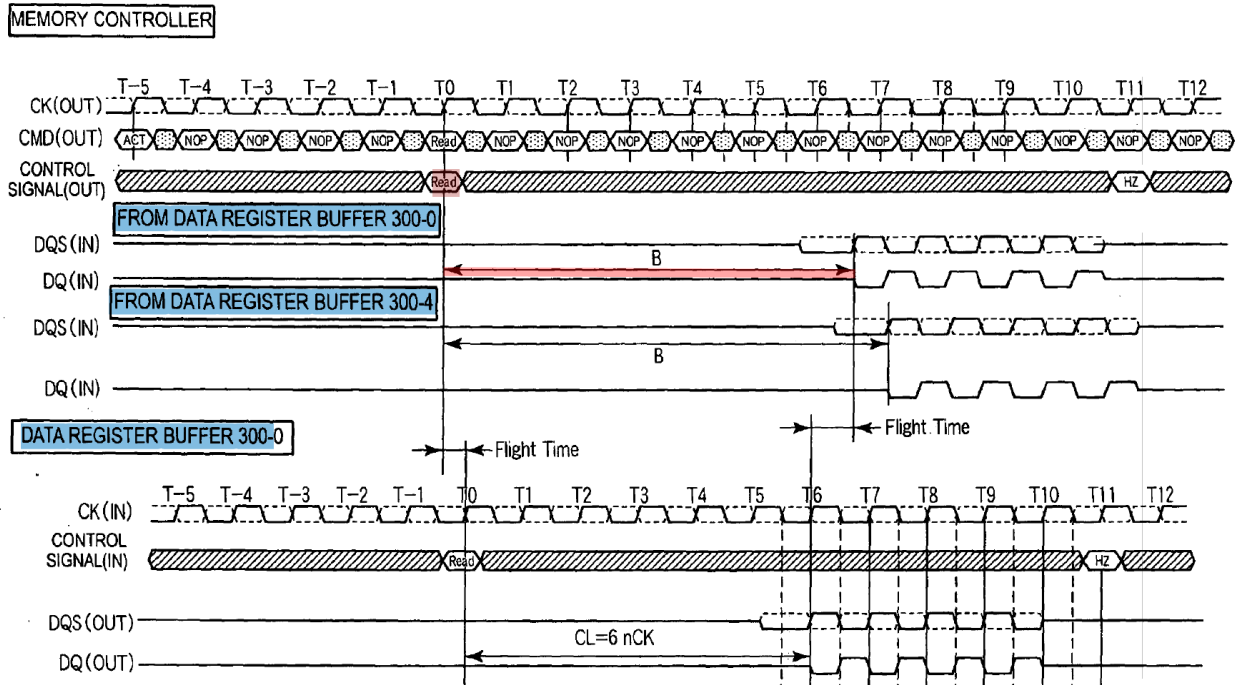


FIG. 15



A POSITA would have understood that performing these read leveling operations independently from write leveling, as in Osanai, requires time and corresponding circuitry, thus motivating her to simplify these operations by using Tokuhiro's technique of setting the read delays based on the write delays “without...a special mechanism, such as an FIFO.” EX1006 (Tokuhiro), 3:16-26, 18:66-19:7, Abstract, FIG.11 (annotated above, illustrating read delay elements DR-1 to DR-n compensating for fly-by delays from T7 to T8); EX1005 (Osanai), ¶[0136], Fig.7 (annotated above); EX1003, ¶¶152-157.

The combination would have been well within the level of skill at the time, since Tokuhiro details how to calculate the read delays based on the write delays, and this would have provided what is expected from the combination: a memory system where the read leveling operation is simplified by using the write delays. EX1003, ¶157. The Board has agreed with this motivation to combine Osanai and Tokuhiro. EX1066, 41.

(2) *Second motivation: Tokuhiro provides simple techniques for removing fly-by delays, while Osanai does not disclose how its memory controller re-times read data received with fly-by delays*

Osanai's “S4” and “S5” read leveling, discussed above, do not remove the large delays created by the fly-by topology on the x-axis, meaning each memory device will respond to the read command at a different time, as shown by the clock

annotations below, and meaning that Osanai's system memory controller will receive the DQ data and DQS strobe signals from each memory device at a different time, as shown by the red arrow further below:

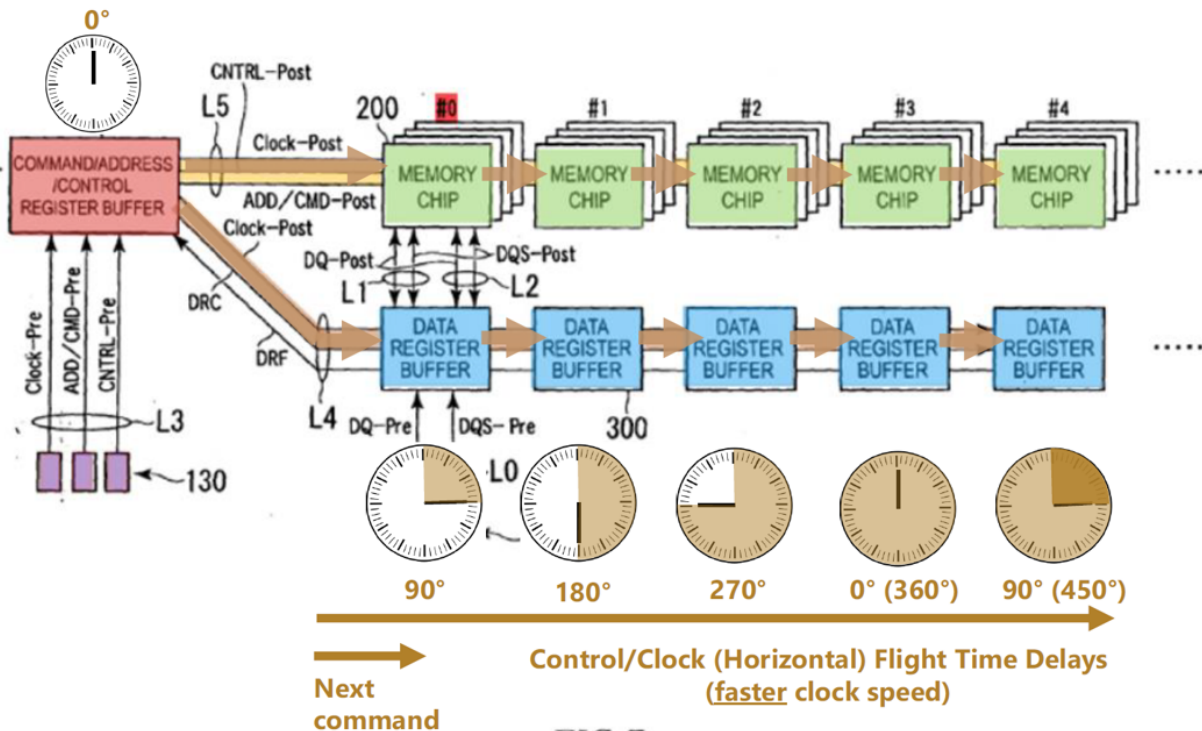
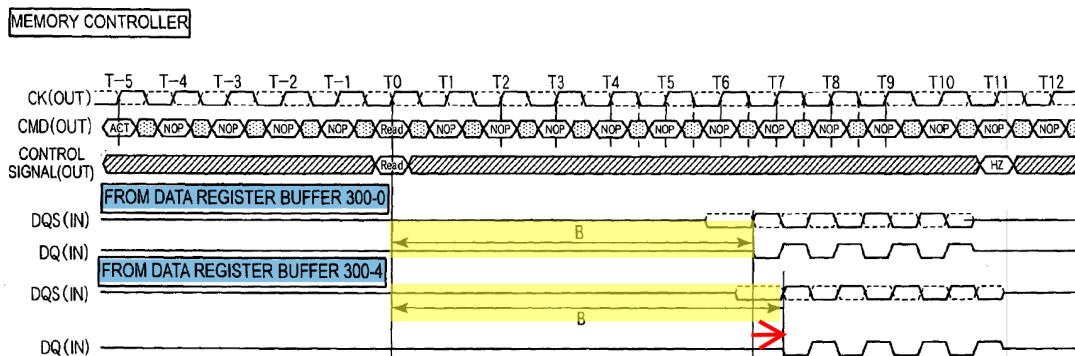


FIG. 7

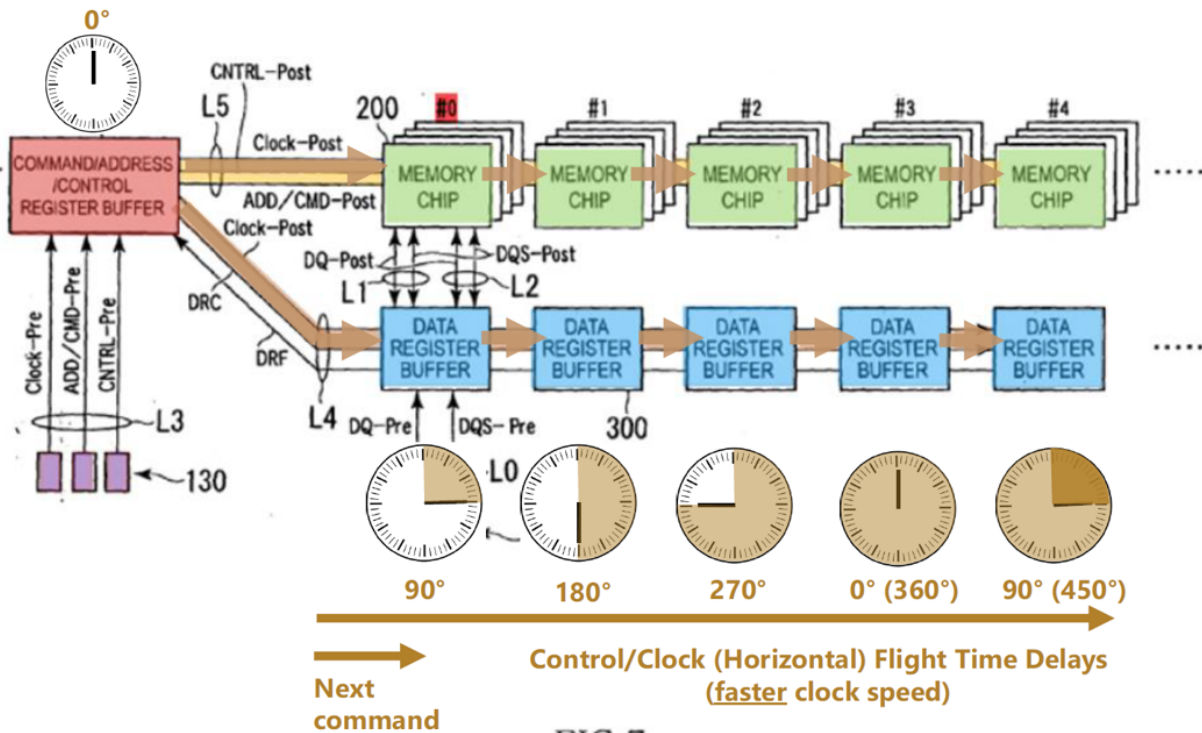


EX1003, ¶¶158-159; EX1005, FIGs.17, 7 (annotated above), ¶¶[0157], [0136], [0167].

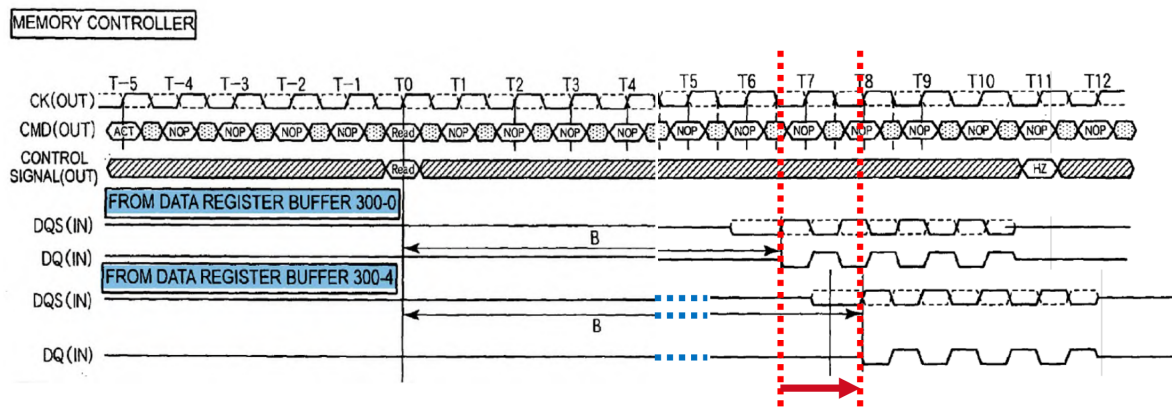
Tokuhiro teaches removing the fly-by delays using simple “DR” delay circuits without adding complex circuitry like a “FIFO” to the system memory controller. EX1006, 18:66-19:7. A POSITA would have been motivated to implement the teachings of Tokuhiro’s delay circuits in Osanai’s data buffers — which are already performing adjustments to the timing of the DQ/DQS signals — so that the system memory controller does not need to make corrections for the large delays created by the fly-by topology on the x-axis, thus simplifying the overall read leveling process and improving reliability. EX1003, ¶¶160-161. The Board has agreed that a POSITA would have been motivated to implement the teachings from Tokuhiro’s “DR” delay circuits in Osanai’s data buffers. EX1066, 39-40.

(3) *Third motivation: Tokuhiro discloses simple solutions for fly-by delays greater than one clock cycle, while Osanai does not*

As discussed above (pp.38-40), both Osanai and Tokuhiro have a similar “fly-by” topology, meaning that as clock speeds get faster, *see* EX1077, 6, it may take more than one clock cycle for command signals to reach the furthest memory devices (green below):



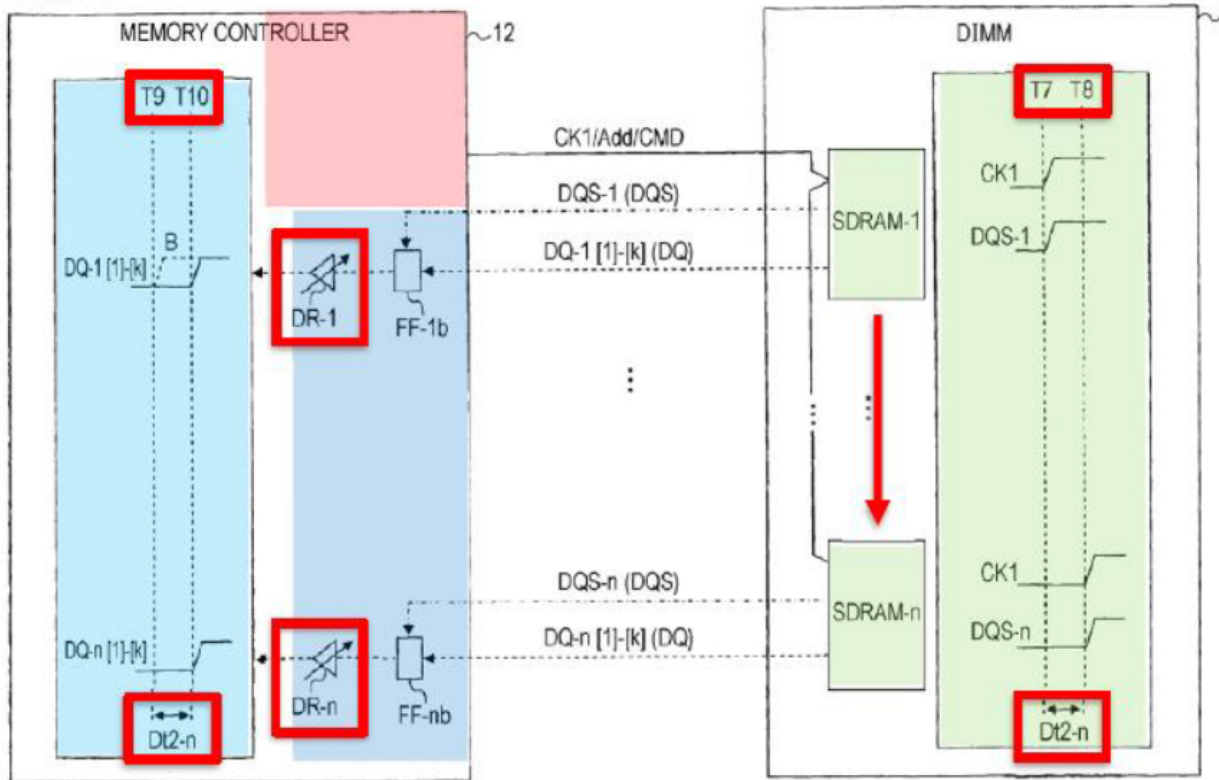
EX1003, ¶¶162-164 (annotating EX1005, Fig.1); EX1074, 68:17-70:14. In this situation, the system memory controller would receive read data from different memory devices over the course of more than one clock cycle, as illustrated by the modification to Figure 17 below, meaning the system memory controller would receive a second piece of data from the closest memory device (“Next command” above) before it has even received the first piece of data from the furthest memory device.



EX1003, ¶165 (modifying EX1005, Fig.17).

Fly-by delays greater than one clock cycle, as illustrated above, cannot be solved by simply delaying the clock, because clocks repeat every cycle, making any delay beyond one cycle “disappear.” *Id.*; EX1075, 229:5-9. Osanai does not teach a solution to this problem, but such delays greater than one clock cycle were a known problem that had been solved with special FIFO circuitry. EX1024, 5:25-31, 6:56-7:2. Tokuhiro teaches a simpler solution that does **not** require modifying the system memory controller to add special “FIFO” circuitry and instead uses “DR” delay circuits to gradually change the delay for the data signals from each memory device to match the increasing fly-by delay for each memory device (e.g., from T7 to T8) so that all the data arrives at the system memory controller at the same time (e.g., at T10):

FIG. 11



EX1006 (Tokuhiro) at 3:9-12, 14:55-:58, 18:15-19:7, Fig.11; EX1003, ¶¶136-138.

A POSITA would have been motivated to implement Tokuhiro's solution in Osanai to avoid changing the circuitry in the system memory controller to include a FIFO and to take advantage of the existing circuitry in Osanai's data buffers.

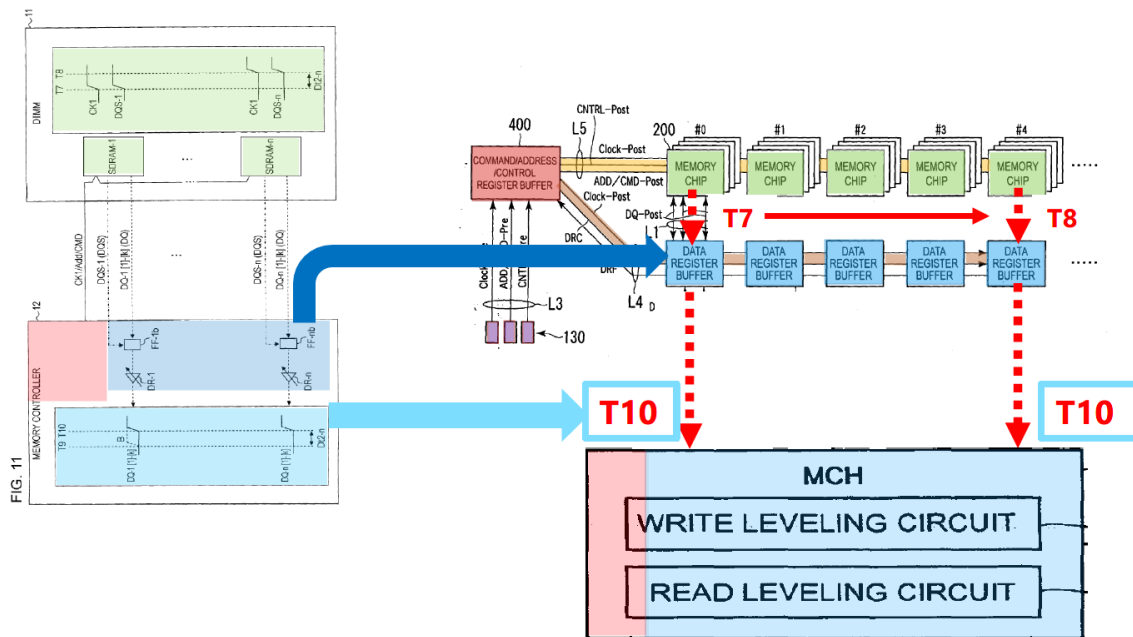
EX1003, ¶¶163-168.

2. **The combination of Osanai in view of Tokuhiro and Butt relied upon here**

a) *It would have been obvious to implement Tokuhiro's delay elements in Osanai's data register buffers*

In the combination of Osanai with Tokuhiro and Butt, Tokuhiro's "DR" delay elements (from Figure 11, below left) are implemented in Osanai's data

buffers (as illustrated by the dark blue arrow to Osanai's Figure 7, below right), such that the read data arrives at the system memory controller (MCH) at substantially the same time (e.g., T10), enabling the system memory controller to correctly capture all the read data from all the memories even with fly-by delays larger than one clock cycle (e.g., from T7 to T8):

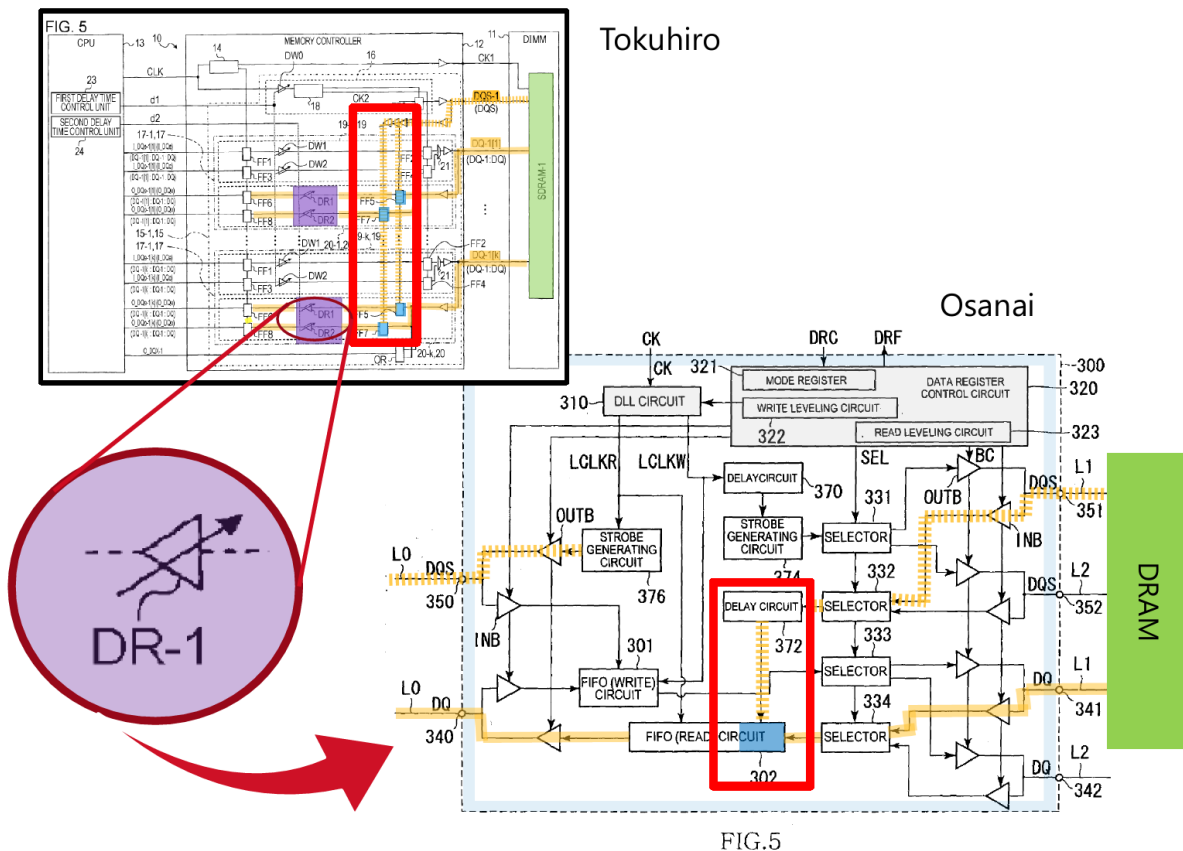


EX1003, ¶¶169-176.

The combination shown above avoids the memory controller having to manage large fly-by delays during either training or normal operation, thus requiring less circuitry and functionality for implementation, such as extra logic and circuitry (e.g., FIFOs) to re-order read data that has been captured in different clock cycles. EX1003, ¶174. Another advantage is that large fly-by delays are removed on the module at the first practically available location (the data buffers,

since JEDEC-compliant memory devices would not have such delay elements, *see* EX1006, 2:54-59), preventing the rest of the system from having to manage those large fly-by delays. EX1003, ¶175.

As shown in more detail below, in the combination, a POSITA would have been motivated to add Tokuhiro's read delay elements (e.g., DR-1, purple, below left) to Osanai's data buffer (blue, below right) immediately after the DQ data signal from the memory is latched (red box below), which is done using the DQS strobe that has been centered using Butt's technique discussed above (pp.35-37):



EX1003, ¶170 (annotating EX1006, Fig.5; EX1005, Fig.5).

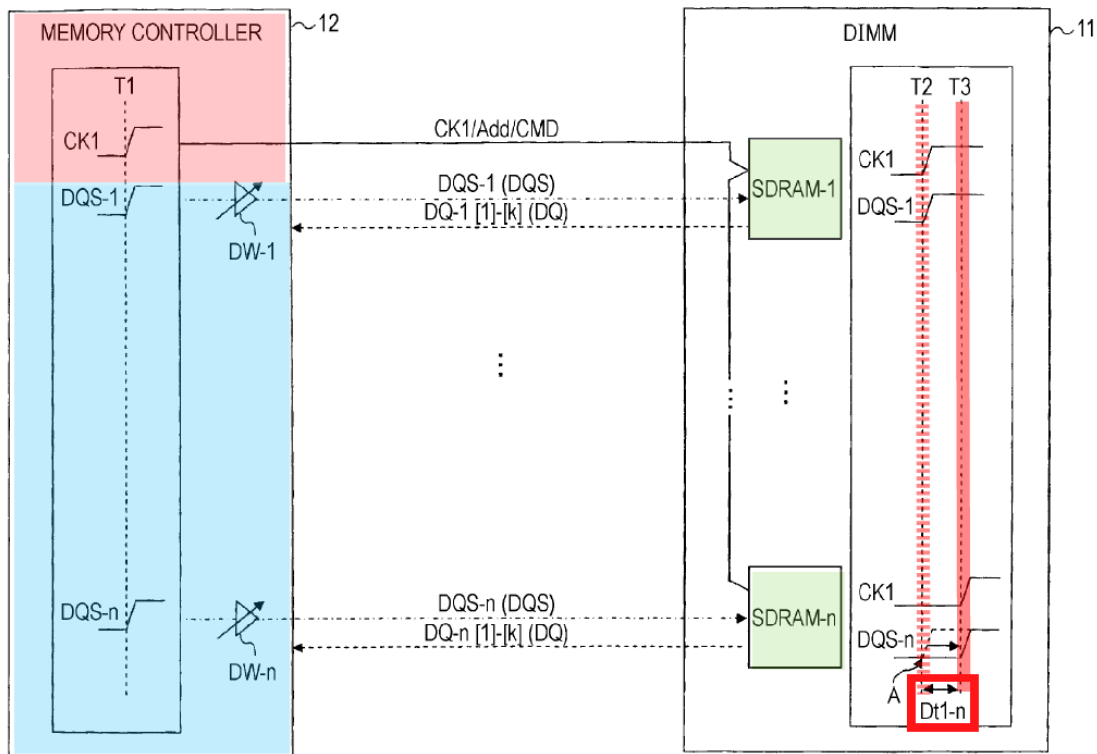
In the combination shown above, Tokuhiro's purple "DR" delay elements in Osanai's data buffer would cause both the DQS strobe signal output on 350 (dashed orange line on the left) and the DQ data signal output on 340 (solid orange line on the left) to both be delayed so that they both arrive at the system memory controller at the correct time (e.g., at time T10) while remaining "edge-aligned" with each other as required by the JEDEC standard discussed above (p.4).

EX1003, ¶171; EX1059, 60.

b) It would have been obvious for Osanai's module controller to program Tokuhiro's delay elements in Osanai's data buffers based on time intervals measured during Butt's write operations

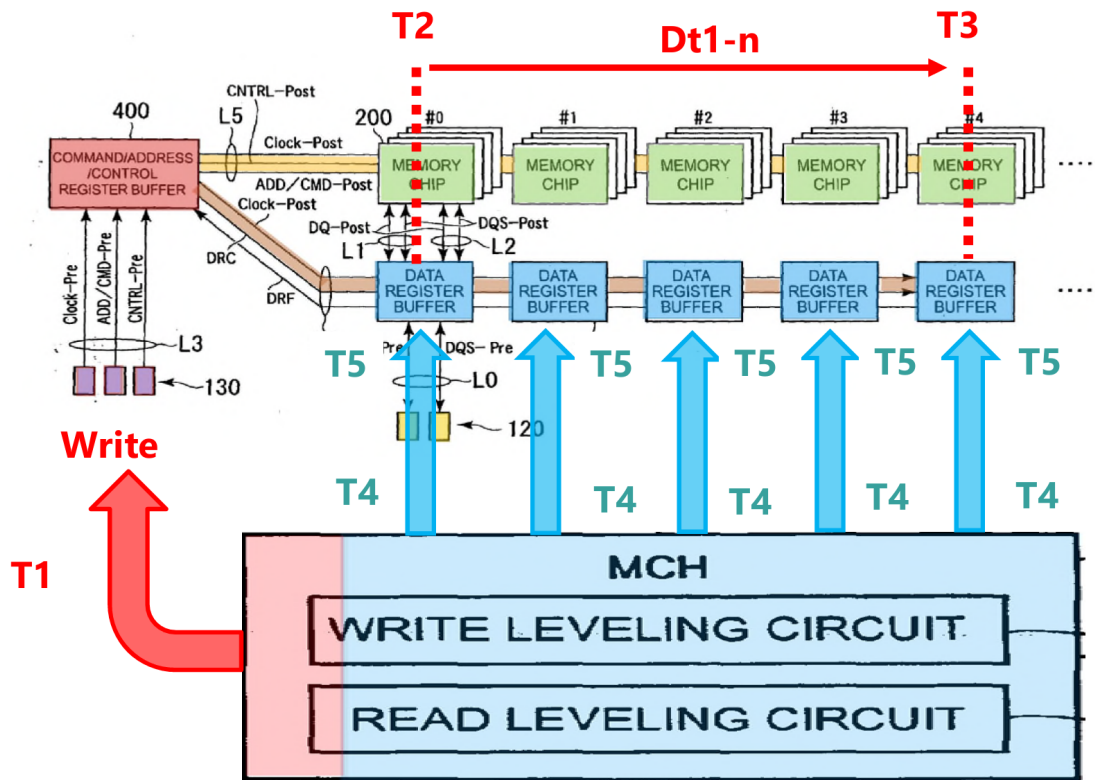
As discussed above (pp.38-44), Tokuhiro teaches measuring delays in the write direction and then using those delays in the read direction. For example, as shown below, Tokuhiro teaches that before any corrections are made, the DQS write strobe signals all arrive at the memory module at substantially the same time (e.g., T2), but the corresponding clock/address/command signals have fly-by delays causing them to arrive between T2 and T3 at the memory devices (green), requiring a delay of Dt_{1-n} for the n-th memory device:

FIG. 7



EX1003, ¶180 (annotating EX1006, Fig.7); *see also* EX1006, Fig.10, 13:30-37.

Thus, in the combination for Ground 1, as shown below, Osanai's module controller measures the impact of the fly-by delays at each data buffer during a write operation (e.g., the interval of time at each data buffer between receipt of a write command between T2 and T3, and receipt of the write data at T5, as shown in the example below), and, in turn, programs Tokuhiro's DR delay elements in the data buffers to remove those fly-by delays in subsequent read operations so that the system memory controller receives all read data at substantially the same time (as explained above, pp.49-52):



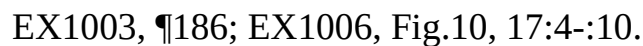
EX1003, ¶¶181-182; EX1006, 16:18 (Formula 3-6 for calculating the read delays from the write delays, including the maximum of those write delays).

In the combination, Butt's strobe-centering includes "a routine ... that writes to, reads from, and compares a selected data pattern to a selected range of the DDR memory 106," EX1029, ¶[0038], *supra* pp.35-37, motivating a POSITA to use those existing write operations during initialization to measure the fly-by delays as shown above. EX1003, ¶178. Implementing a write operation during initialization for timing measurements (using the existing system memory controller, which normally issues read/write commands) was well within the level of skill in the art. EX1003, ¶187; EX1051, p.9 (disclosing "normal [writes/reads]" during DQ/DQS

marginizing “training”); EX1052, ¶ 7 & p.19 (same); EX1053, p.37 (“These [DDR bus calibration] functions issue a series of write and read transactions”).

Furthermore, Osanai teaches using the data buffers to measure the time interval between receipt of a command on the DRC line (brown, above) and receipt of the corresponding data, *see, e.g.*, EX1005, FIG.5, ¶[0157], motivating a POSITA to apply Osanai’s time measuring technique to determine the fly-by delays as shown above. EX1003, ¶¶178-180. DDR3 memory devices do not have a mechanism to measure these time internals and report them to the module controller, while Osanai’s data buffers do. EX1003, ¶185. Osanai includes a feed-back channel DRF (brown above, between the data buffers, blue, and the module controller, red, *see* EX1005, ¶¶[0095], [0105]) which a POSITA would be motivated to use to communicate the measured time intervals from each of the data buffer circuits back to the module controller which, in turn, would program Tokuhiro’s DR delay elements in the data buffers to remove those fly-by delays in subsequent read operations (as explained above, pp.49-52). EX1003, ¶185.

The combination of Ground 1 teaches removing the large fly-by delays not only in the read direction, as explained above, but also in the write direction. EX1003, ¶186. For example, as illustrated below, a POSITA would be motivated for reasons similar to those above to implement Tokuhiro’s write delay elements



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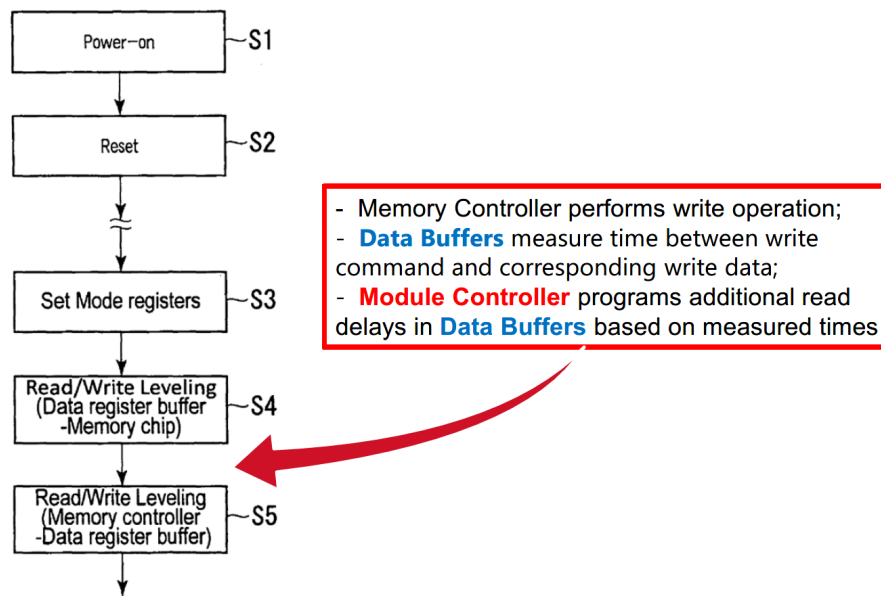


FIG.13

EX1003, ¶187 (annotating EX1005, Fig.13 according to the combination of Ground 1).

B. Ground 2 combination: Ground 1 + Ellsberry (EX1007)

Ground 2 is the combination of Ground 1 and Ellsberry (EX1007). Similar to Osanai and the '035 Patent, Ellsberry discloses a memory module with the same distributed buffer architecture (as shown in Figures 5 and 6 of Ellsberry) with four ranks of memories, see EX1031, 33 (Board's finding that Ellsberry discloses "ranks"); EX1033, 38-39 (similar), and expressly describes modules with 8-bit wide data buffers (SWITCH ASIC with DQ[3:0] and DQ [7:4], shown in blue below), similar to Osanai, coupled to either 8-bit wide memory chips (e.g., Fig.13, below right, in green, indicated by "/8" on the DQ line) or pairs of 4-bit wide

memory chips (e.g., Fig.11, below left, in green, indicated by “/4” on the DQ line).

EX1003, ¶188; EX1007, Figs.11, 13:

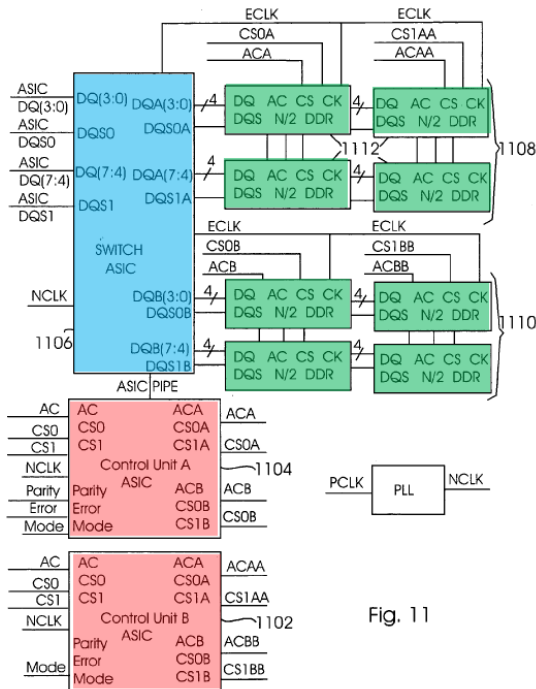


Fig. 11

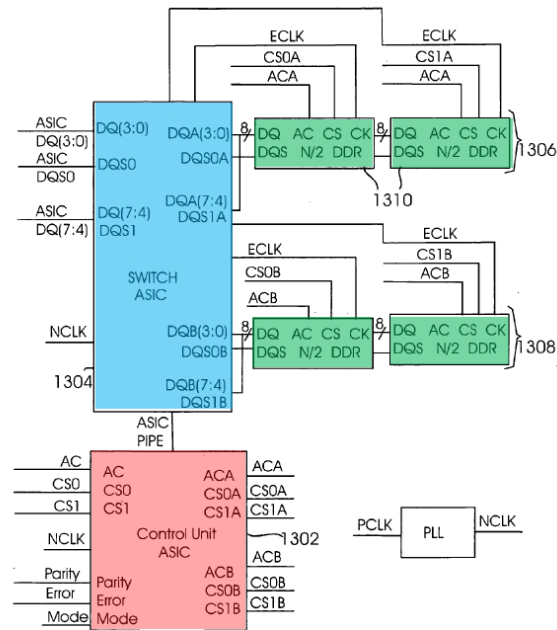


Fig. 13

Consistent with the teachings of Ellsberry above, *see, e.g.*, EX1007, ¶[0051] & Figs.6, 11, JEDEC had already standardized both 8-bit wide memory devices (referred to as “x8,” *see* EX1021, 317) and 4-bit wide memory devices (referred to as “x4,” *see id.*), which could be stacked, *see, e.g.*, EX1020, 3 (“x4”), 4 (“x8”), 6 (“Stacked / dual die DDR3 SDRAM x4”). EX1003, ¶189. Accordingly, a POSITA would have been motivated by Ellsberry with a reasonable expectation of success to use either a x8 memory device or a pair of x4 memory devices with each of Osanai’s data buffer circuits in the combination for Ground 2. EX1003, ¶190.

The Board has already agreed with this motivation to combine Hiraishi (which has the same relevant disclosure as Osanai) and Ellsberry. EX1068, 25-26.

C. Ground 3 combination: Ground 1 + Kim (EX1008)

Ground 3 is the combination of Ground 1 and Kim (EX1008). Kim is analogous art to Osanai and the '035 Patent, since each is directed to solving the problem of reliable communication between integrated circuits, including between Osanai's command/address/control register buffer 400 and data buffers 300. EX1003, ¶191; EX1008, 1:12-14, 1:21-31. Kim identifies the problem of a metastable state (i.e., a signal greater than logic 0 level, but less than logic 1 level), and discloses a solution in the form of “a metastability detection/prevention circuit 20” to be incorporated with any “main active circuit 10” in need thereof, including “a data input buffer.” EX1008, 1:21-31, 2:23-37.

It would have been obvious to combine the functionality of Kim's metastability detection circuitry with the DRC inputs in Osanai's data register buffers. EX1003, ¶192; EX1005, Figs.5, 7. A POSITA would have been motivated to make the combination to obtain more reliable communication by avoiding metastability at the input of the DRC signals, which carry important control information for Osanai's data buffers. EX1003, ¶¶192-193; EX1005, ¶[0106]. Making the combination would have been well within the level of skill at the time and provided nothing more than expected from the prior art: detecting

metastability at the DRC input and removing the metastability by using Osanai's DLL circuit 310 to adjust the phase of the corresponding internal clock. *Id.* The Board has already agreed that a POSITA “would have been motivated to include [Kim's] metastability condition detector functionality” in Hiraishi (which has the same relevant disclosure as Osanai). EX1068, 26-30.

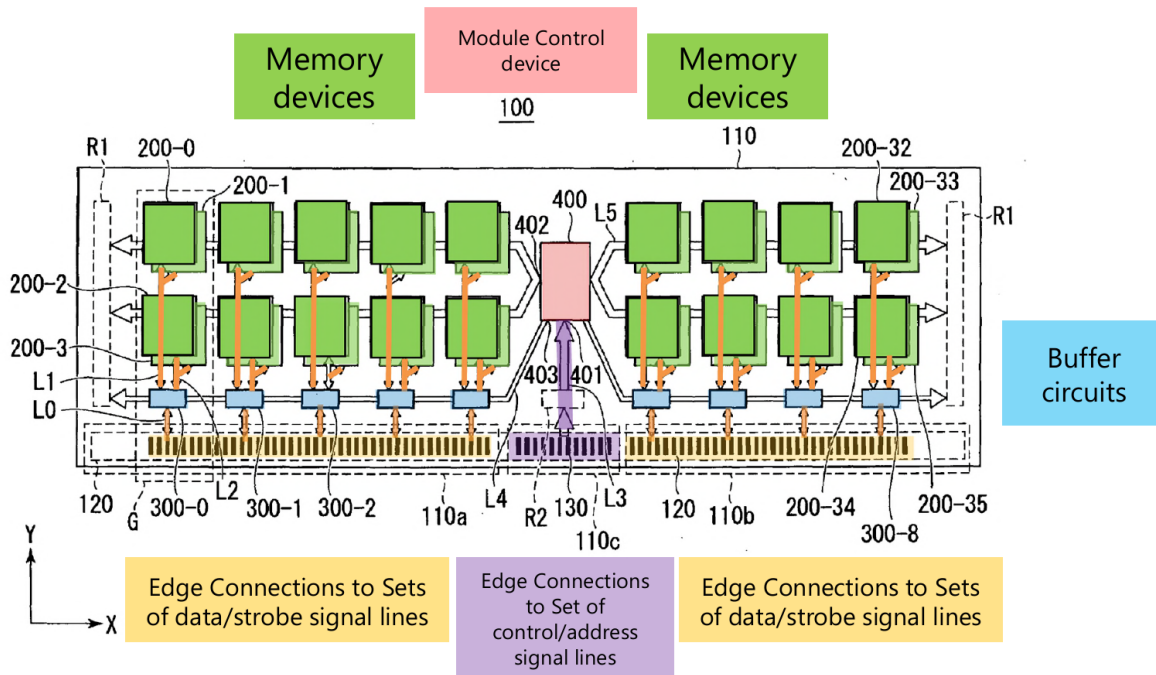
D. Grounds 1-3 render claims 2-9 and 14-20 obvious

As explained below, Grounds 1-3 each render obvious claims 2-9 and 14-20 of the '035 Patent.

1. Claim 2 (depends on Claim 1)

c) 1[pre]

Grounds 1-3 disclose “*a memory module [such as memory module 100] operable to communicate with a memory controller [MCH 12 in Figs.2-3] via a memory bus [line 23 in Fig.3], the memory bus including signal lines, the signal lines including a set of control/address signal lines [to couple to command/address/control line L3 on the module, purple] and a plurality of sets of data/strobe signal lines [to couple to data line L0 on the module, orange]*”:



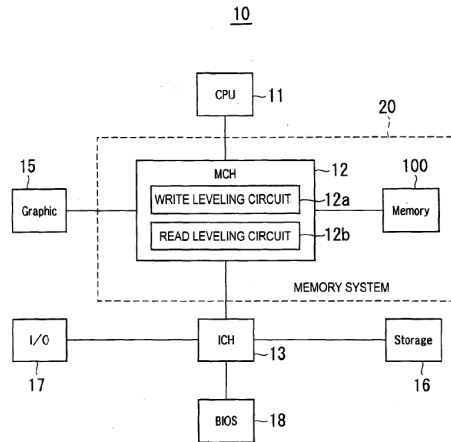


FIG.2

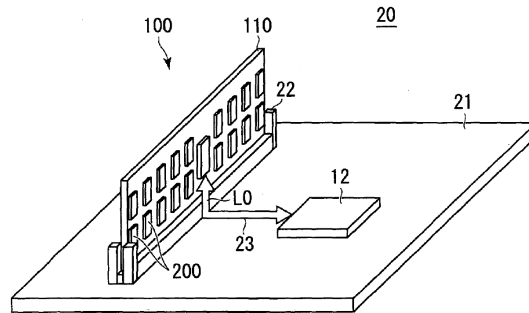


FIG.3

The memory bus (line 23) includes signal lines, including as shown below a set of control/address signal lines coupling, through connectors 130 (purple), to command/address/control line L3, and a plurality of sets of data/strobe signal lines, each set coupling, through connectors 120 (orange), to data line L0. EX1005, ¶¶[0053], [0055], [0075], [0108]-[0109], FIGS.1&7.

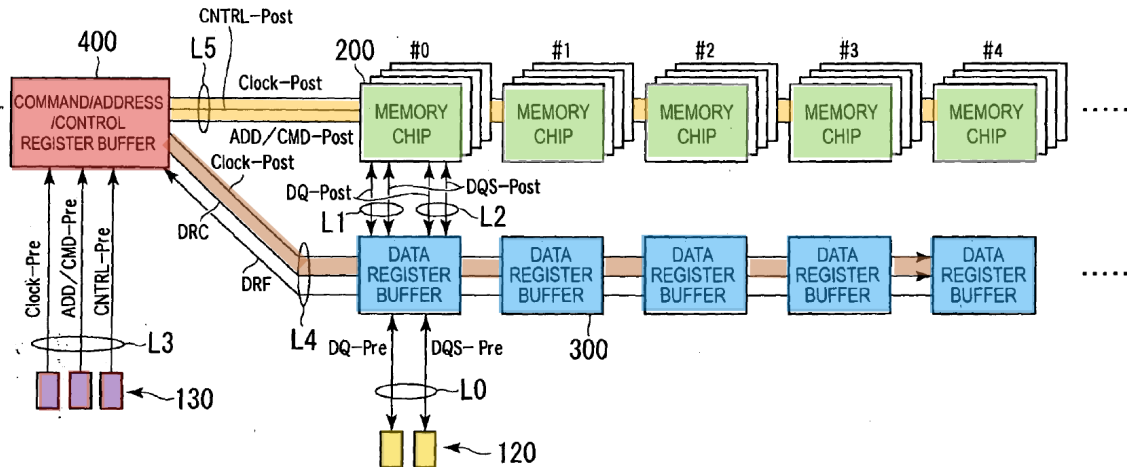
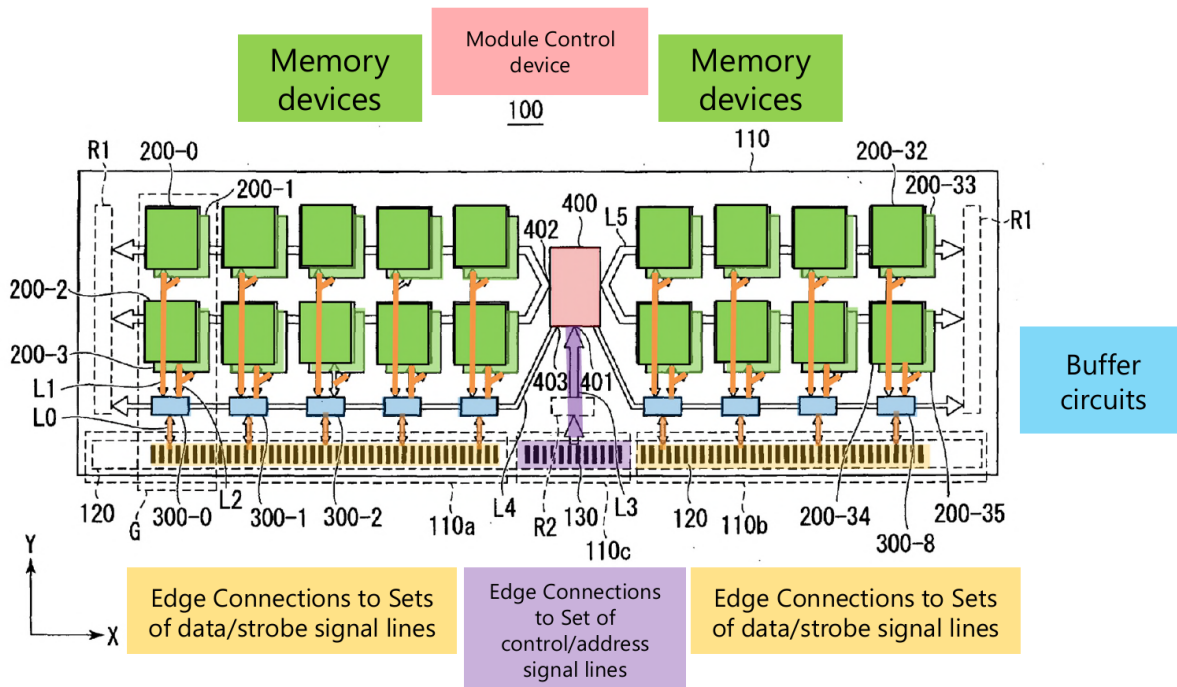


FIG.7

d) 1[a]: module board

Grounds 1-3 disclose “*a module board [module PCB 110] having edge connections [including command/address/control connectors 130 (purple) and data connectors 120 (orange)] for coupling to respective signal lines in the memory bus [line 23, above in Fig.3]”*”:



EX1005, Fig.1.

The Board has already found that Osanai teaches this limitation. EX1066, pp.23-24. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, discloses similar limitations. EX1068, 7-10; EX1003, ¶75.

As shown above, memory module 100 includes a module printed circuit board (“module PCB 110”). EX1005, ¶[0051]. Module PCB 110 has “edge connections” 120 and 130 arranged at the edge of the PCB for coupling to respective signal lines in the memory bus to connect to the memory controller (MCH 12 in Figs.2-3 above). EX1005, ¶¶ [0053]-[0055]. Osanai provides even more detail about the “edge connections” than the ’035 Patent. Compare EX1005, Fig.1 (above), with EX1001, Fig.2C (below).

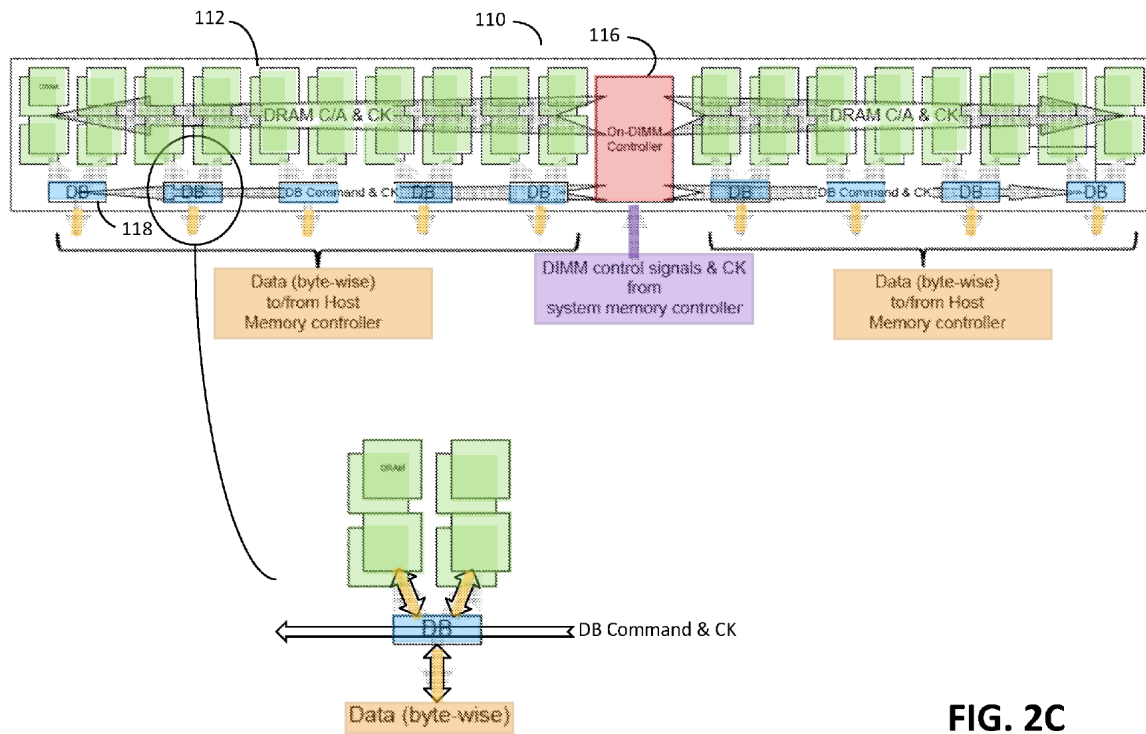
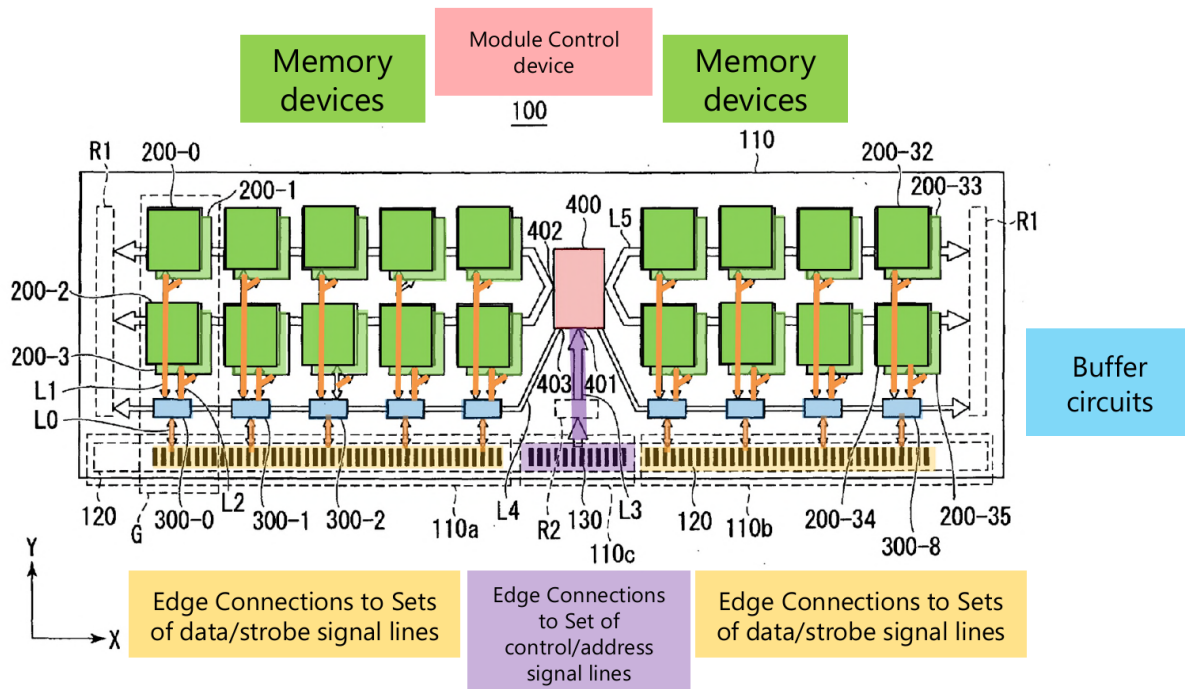


FIG. 2C

e) 1[b]: module control device

Grounds 1-3 disclose “a module control device [command/address/control register buffer 400, red] mounted on the module board [PCB 110]”:



EX1005, ¶[0065], Fig.1.

Grounds 1-3 also disclose, as shown below, the “*module control device*” (400, red, in Figures 1, 6, and 7) is “*configured to receive memory command signals for a first memory operation [such as a read operation] from the memory controller [MCH 12] via the set of control/address signal lines [through command/address/control connectors 130 and command/address/control line L3 (Fig.7) at input terminal 401 (Fig.6, purple)] and to output module command signals [module command/address/control line L5 (Fig.7) at output terminal 402 (Fig.6, orange)], and module control signals [(including DRC and Clock-Post, brown) on control line L4 (Fig.7) at output terminal 403 (Fig.6)] in response to the*

memory command signals [received on command/address/control connectors 130 (Fig.7, purple)].”

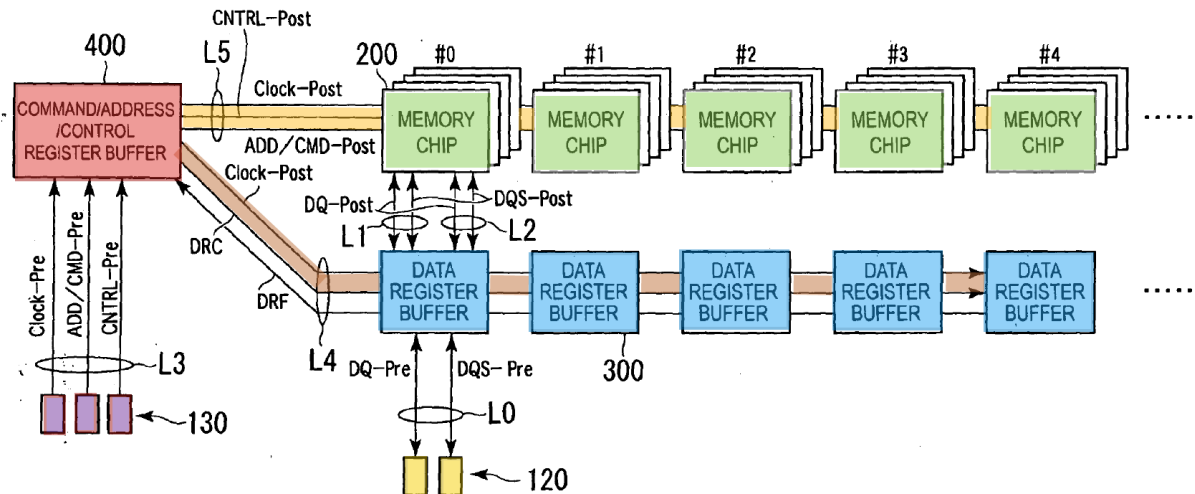


FIG.7

EX1005, $\bar{1}[0026]$, Fig.7 (color added).

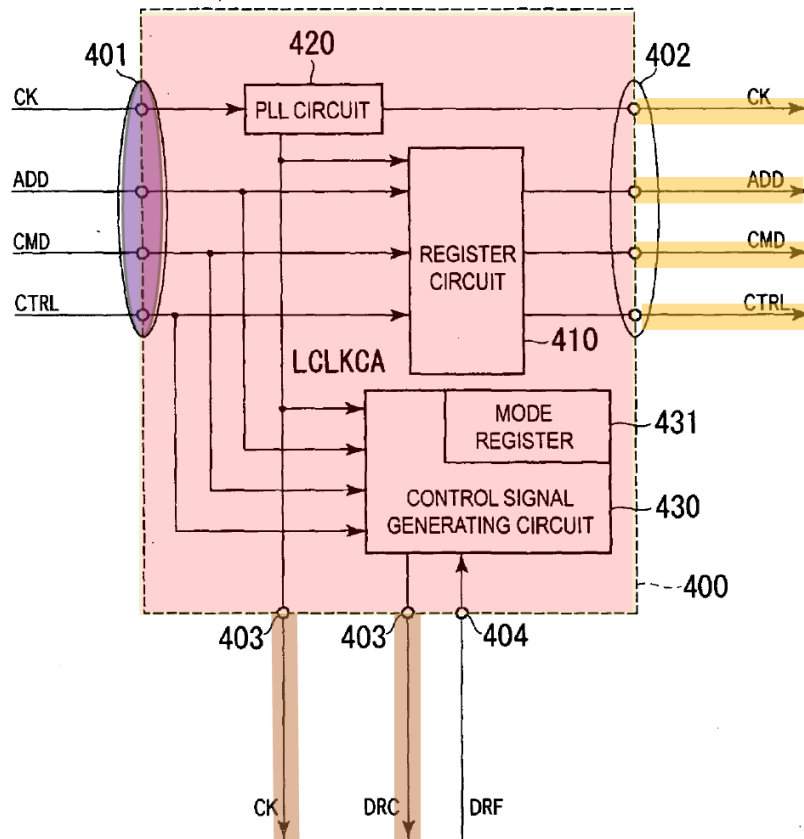


FIG.6

EX1005, ¶[0025], Fig.6 (color added).

The Board has already found that Osanai teaches this limitation. EX1066, p.24. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, discloses similar limitations. EX1068, 7-10; EX1003, ¶75.

Osanai teaches that the module control device (400, red) is configured to receive memory command signals for memory operations from the memory controller via the set of control/address signal lines (EX1005, ¶¶[0053], [0066],

[0103]) and output module command signals and module control signals in response to the memory command signals (EX1005, ¶¶[0066], [0103], [0105]).

Osanai discloses that one memory operation is a read operation. EX1005, ¶¶[0128]-[0137]. Figure 11 (annotated below) shows the timing of a read operation, including receiving a read command (red box at “T0”) on line CMD(IN) (orange) by the Command/Address/Control Register Buffer (red), and outputting corresponding signals on line CMD(OUT) (orange) to the memory chips (green) and on line CONTROL SIGNAL(OUT) (brown) to the Data Register Buffer (blue):

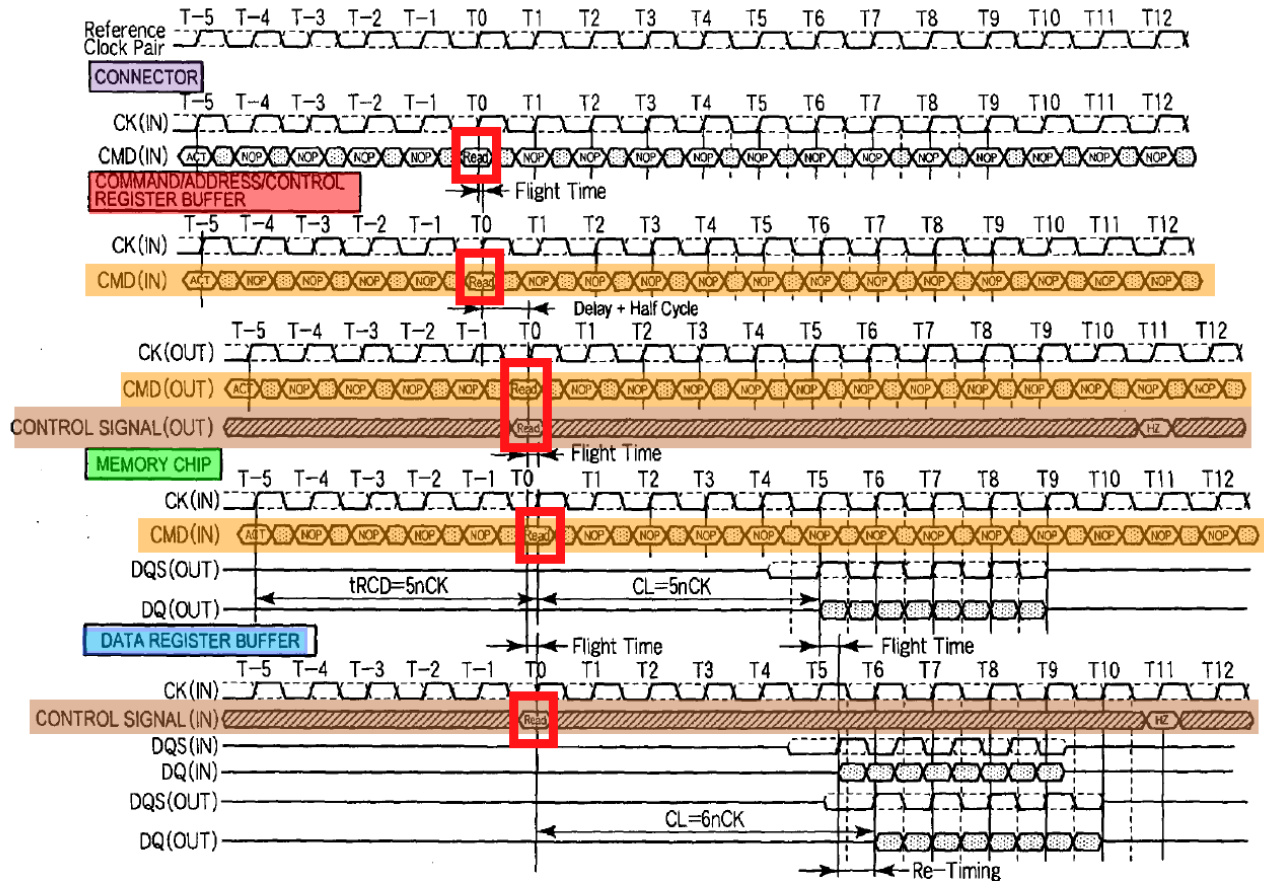


FIG. 11

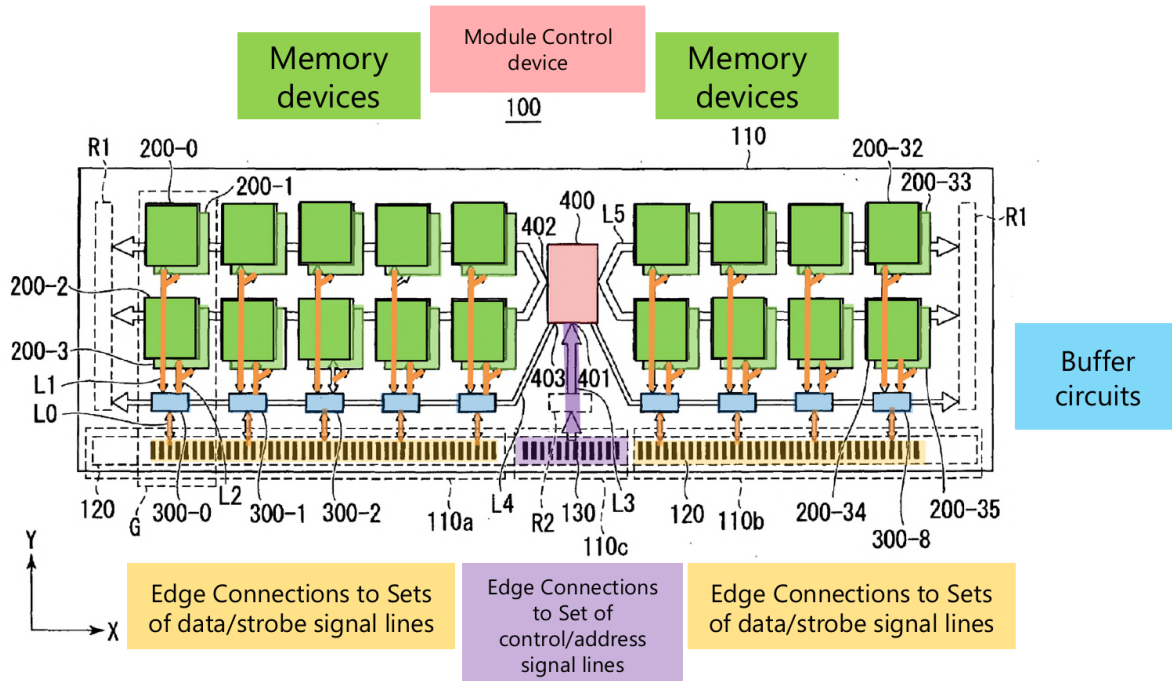
EX1005, Fig. 11 (annotated). Thus, Osanai discloses this limitation where the “*first memory operation*” is a read operation. *Id.*

f) 1[c]: memory devices

As shown by Figures 1 and 7 below, Grounds 1-3 disclose “*memory devices* [200-0 to 200-35 (green)] *mounted on the module board and configured to perform the first memory operation* [such as a read operation] *in response to the module command signals* [(on line L5)], *the memory devices including a plurality of sets of memory devices* [such as a set including memory devices 200-0 to 200-3]

corresponding to respective sets of the plurality of sets of data/strobe signal lines

[the data/strobe lines in the memory bus coupled to L0]”:



EX1005, Fig.1 (annotated).

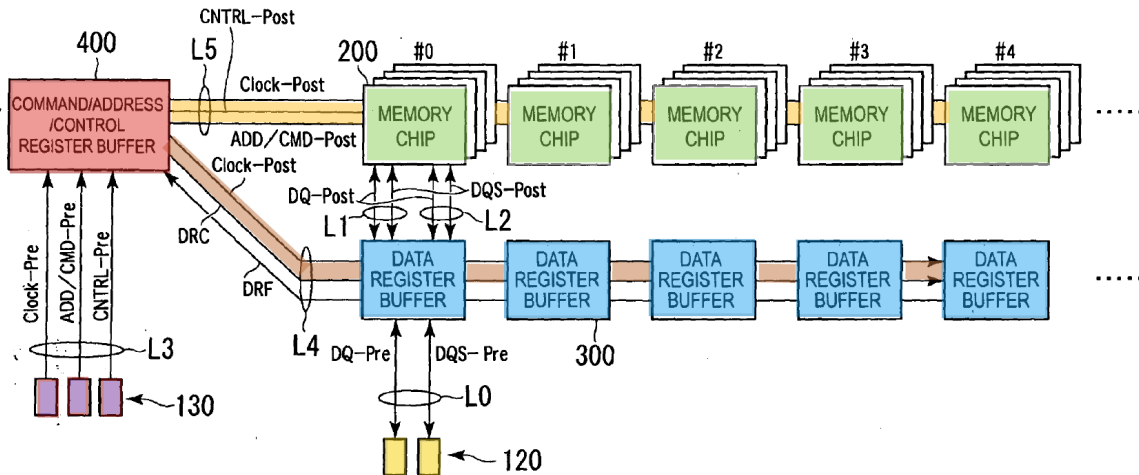


FIG. 7

EX1005, Fig.7 (annotated); EX1003, ¶208.

The Board has already found that Osanai teaches this limitation. EX1066, pp.24-25. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, discloses similar limitations. EX1068, 7-10; EX1003, ¶75.

Osanai discloses that memory module 100 includes a plurality of memory chips 200 mounted on the module PCB 110 (EX1005, ¶[0051]) which are configured to perform the first memory operation in response to the module command signals. EX1005, ¶[0060]. The memory operation can be a read operation, which is performed in response to “ACT” and “Read” commands issued by command/address/control register buffer 400. EX1005, ¶¶[0128]-[0137]. Thus, the memory chips 200 are configured to perform a read operation (“*first memory*

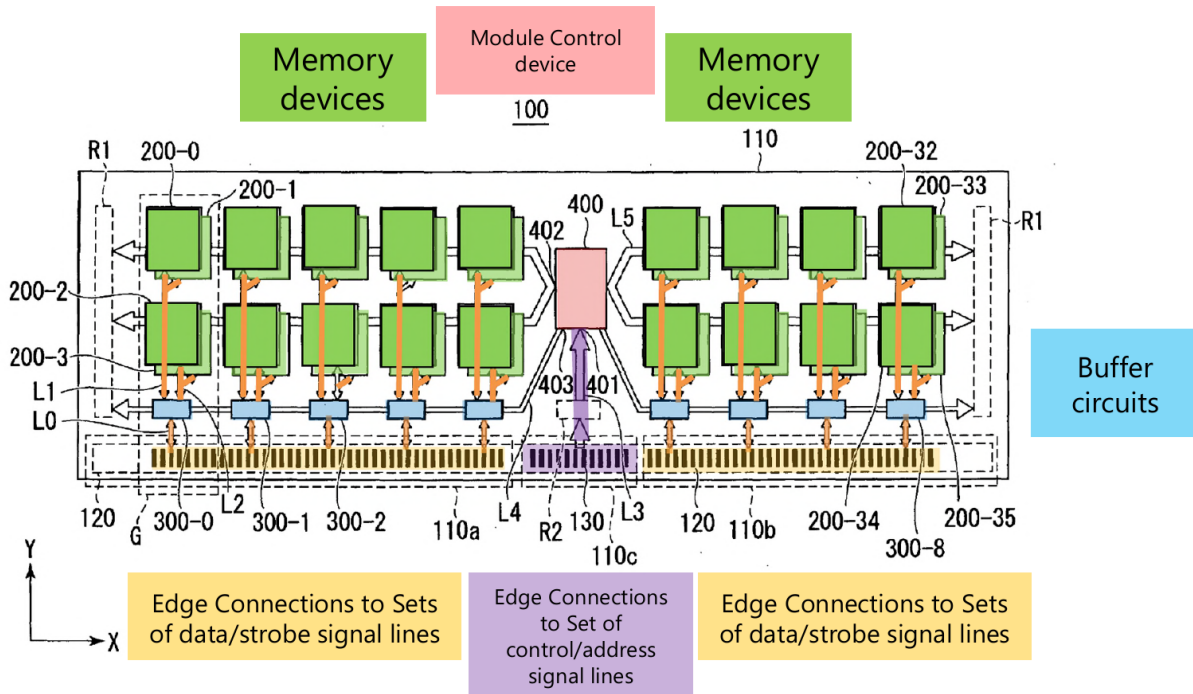
operation”) in response to the module command signals. *See also* EX1005, ¶¶[0169], [0176] (memory chips can be DDR3); EX1020, 56-67 (standard for DDR3 describing read operations).

Osanai discloses that the memory devices include a plurality of sets of memory devices (*e.g.*, 200-0 to 200-3) corresponding to respective sets of the plurality of sets of data/strobe signal lines. For example, as shown by Figure 1 above, memory devices 200-0 and 200-1 are connected to data register buffer 300-0 by line L1, and memory devices 200-2 and 200-3 are connected by line L2, and data register buffer 300-0 is associated with line L0. EX1005, ¶¶[0059], [0109]. Thus, one set of memory devices (200-0 to 200-3) corresponds to one of the sets of data/strobe signal lines (L0, which comprises DQ-pre and DQS-pre). Osanai also discloses that each other set of memory devices correspond to other respective sets of data/strobe lines (*e.g.*, as illustrated in Figure 1, a set for each buffer 300-0 through 300-8).

g) 1[d]: buffer circuits

Grounds 1-3 disclose “*a plurality of buffer circuits mounted on the module board [data register buffer circuits 300-0 to 300-8 (blue)] in positions corresponding to respective sets of the plurality of sets of data/strobe signal lines [e.g., buffer circuit 300-0 (blue) is positioned between the set of memory devices*

200-0 to 200-3 (green) and the connectors 120 (yellow) connecting to the data line L0].



EX1005, Fig.1 (annotated).

The Board has already found that Osanai teaches this limitation. EX1066, p.25. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, discloses similar limitations. EX1068, 7-10; EX1003, ¶75.

Figure 1 above shows nine data register buffers, each of which is allocated to four memory chips, such that each data register buffer buffers read and write data that is transferred via line L0 to data lines L1 and L2 and *vice versa*. EX1005, ¶¶[0051], [0061]. Osanai further explains that a single data register buffer, data

connectors 120, and the four memory chips corresponding thereto constitute a group (G, shown in Figure 1 as a dashed rectangle on the left), such that a relative position relationship between each of the buffers and corresponding four memory chips is constant in all groups. EX1005, ¶[0062].

Figure 5 below also confirms that the data register buffer 300 is positioned between respective sets of data(DQ)/strobe(DQS) signal lines (L0 on one side and L1/L2 on the other). EX1005, ¶¶[0024], [0090-91], Fig.5.

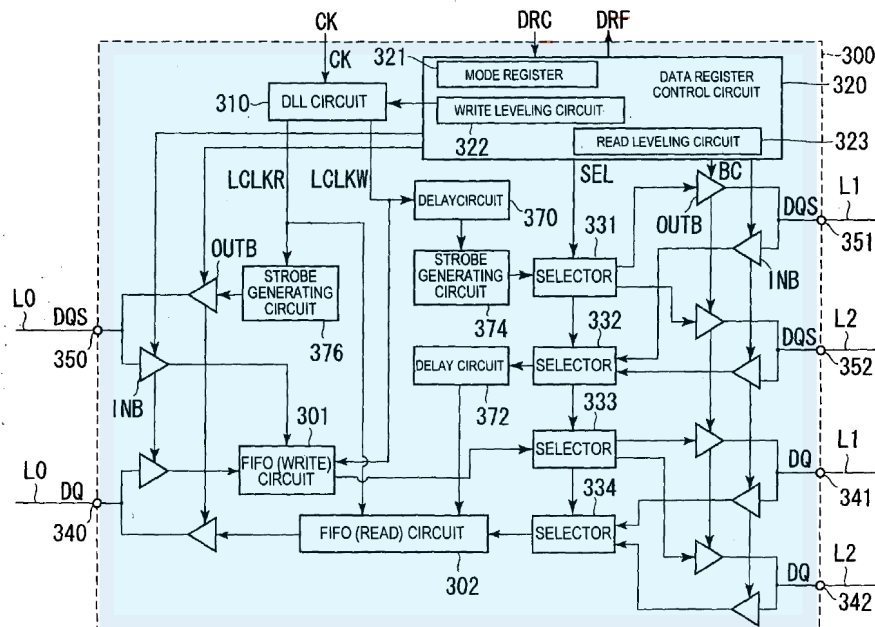
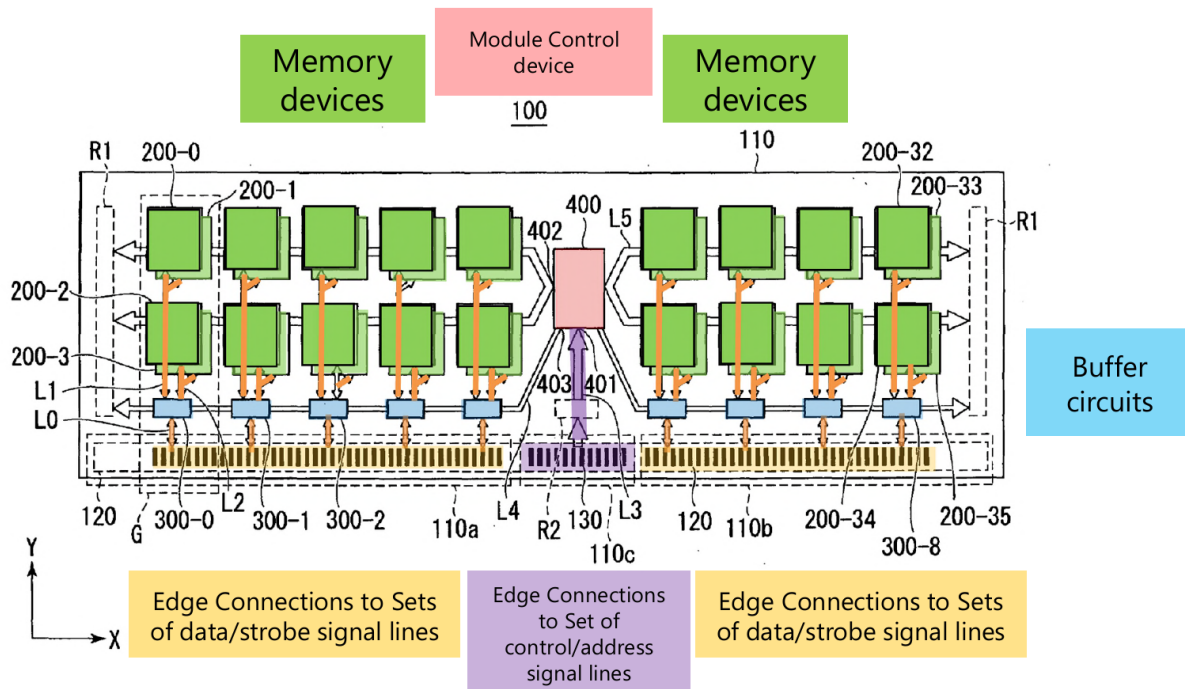


FIG.5

Figure 7 below also confirms that data register buffer 300 is positioned between the data connectors 120 and the memory chips 200, such that the data connectors 120 are connected to the buffer via data line L0 (comprising data and strobe signals DQ-pre and DQS-pre), and the buffer is connected to the memory



EX1005, Fig.1 (annotated).

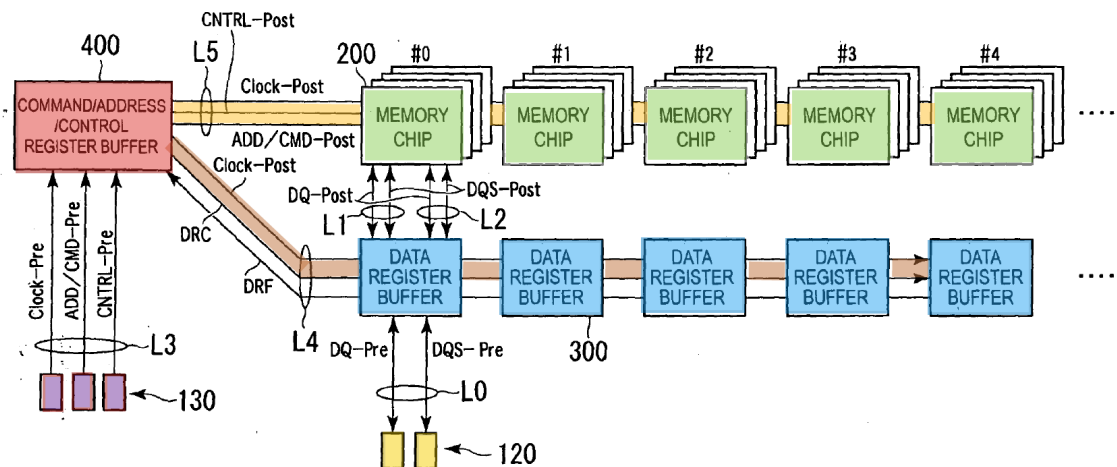


FIG.7

EX1005, Fig.7 (annotated).

Grounds 1-3 also disclose that “*the each respective buffer circuit includes data paths for transmitting respective data [(orange, solid)] and strobe signals [(orange, dashed)] associated with the first memory operation [(here, a read operation from a memory rank on either data line L1 or L2)] and logic [including Data Register Control (DRC) Circuit 320 and DLL Circuit 310, grey], configured to respond to the module control signals [including DRC and CK (brown)] by enabling the data paths,*” for example during a read operation, using control signal lines (red), including lines for setting the selectors 332 and 334 and activating the correct input buffer circuits INB on the L1 or L2 lines, the output buffers OUTB on the L0 line, and the Strobe Generating Circuit 376 and FIFO read circuit 302 at the right time:

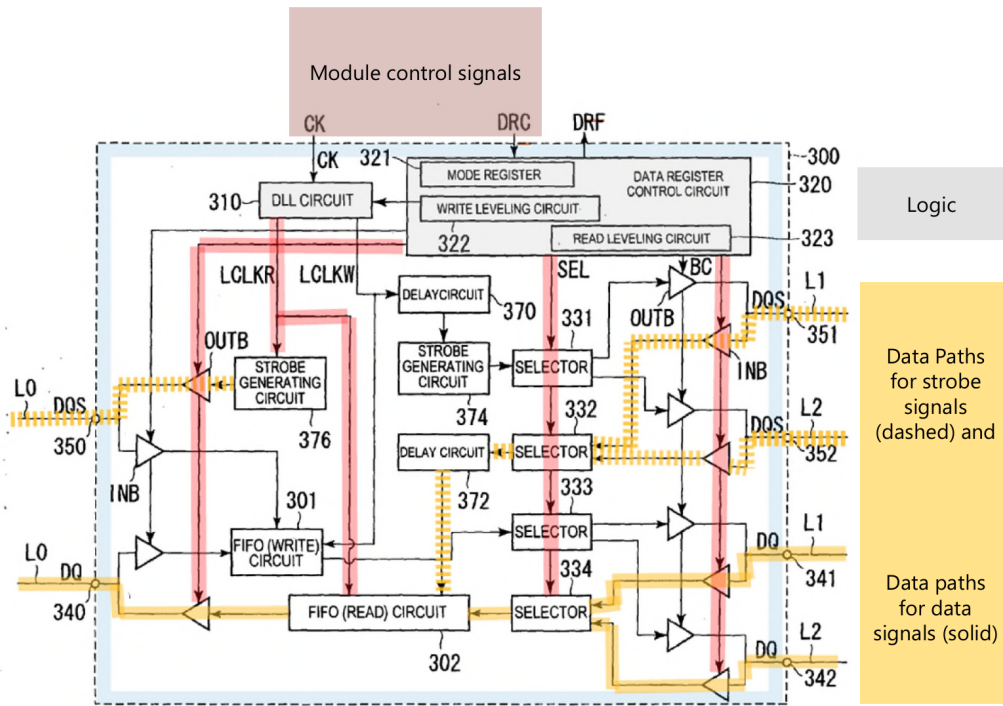


FIG. 5

EX1003, ¶217; EX1005, FIG. 5 (annotated).

The Board has already found that Osanai teaches this limitation. EX1066, pp.25-26. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, discloses similar limitations. EX1068, 7-10, 13; EX1003, ¶75.

Osanai teaches with Figure 5 above that, for a read operation from memory devices on data line L1, the input buffers on terminals 351 and 341 are activated, the selectors 332 and 334 respectively select the lines from terminals 351 and 341, and the output buffers to terminals 350 and 340 are also activated. EX1003, ¶218; EX1005, ¶¶[0094], [0097]. Thus, the logic in the data register control circuit (320)

enables the data paths for transmitting data and strobe signals associated with the read operation from a memory on data line L1. *Id.* The process is similar for a read operation from memory devices on data line L2 (using terminals 352/342). *Id.* Thus, Osanai discloses that each of the selectors 332 and 334 can select only one of the two connected input buffers at a time, to avoid bus conflicts. *Id.*; EX1022, 89-90.

As explained above for limitation 1[d], Osanai discloses that each buffer circuit is coupled between a respective set of data/strobe signal lines and a respective set of memory devices. EX1005, ¶¶[0061]-[0062], [0090-91], [0109].

Osanai also discloses that each respective buffer circuit includes data paths for transmitting respective data and strobe signals associated with the first memory operation. EX1003, ¶220; EX1005, ¶[0090-91], Fig.5. For example, Figure 5 above shows each buffer circuit 300 including data paths for transmitting data (solid orange) and strobe signals (dashed orange). *Id.* Osanai further discloses that where the “*first memory operation*” is a read operation, each respective buffer circuit includes data paths for transmitting data and strobe signals associated therewith. *Id.*

Osanai additionally discloses that the buffer circuit includes logic configured to respond to the module control signals by enabling the data paths. EX1003, ¶221. For example, the operation of the data register buffer 300 is

controlled based on control signals supplied by the command/address/control register buffer 400. *Id.*; EX1005, ¶[0064]. Osanai teaches that the logic within the buffer circuit responds to module control signals (*e.g.*, control signal DRC supplied from command/address/control register buffer 400) by enabling the data paths. EX1003, ¶221; EX1005, ¶¶[0093]-[0094].

i) 1[f]: second wherein clause; obtain timing information and control timing

Grounds 1-3 disclose this limitation. As explained above, *supra* pp.35-57, the combination of Osanai, Butt, and Tokuhiro — where Tokuhiro's delay elements are added to Osanai's data buffer circuits and a time interval is measured by the data buffers during a write operation — includes “*logic [e.g., in data register buffers 300] further configured to obtain timing information based on one or more signals [e.g., by comparing the timing of write data/strobe signals (from the memory controller) and a corresponding Write command (transmitted to the buffer circuits from the memory controller via the module controller)] received by the each respective buffer circuit during a second memory operation [e.g., during a write operation initiated after S4 leveling but prior to S5 leveling during initialization (see modified Osanai Fig. 13 below)] prior to the first memory operation [e.g., a read operation after the completion of initialization] and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information [e.g., using delay elements, as taught by*

Tokuhiro, to delay DQ/DQS signals on data path L0 (see demonstrative figure annotated below showing Tokuhiro Fig. 5 and Osanai Fig. 5)].”

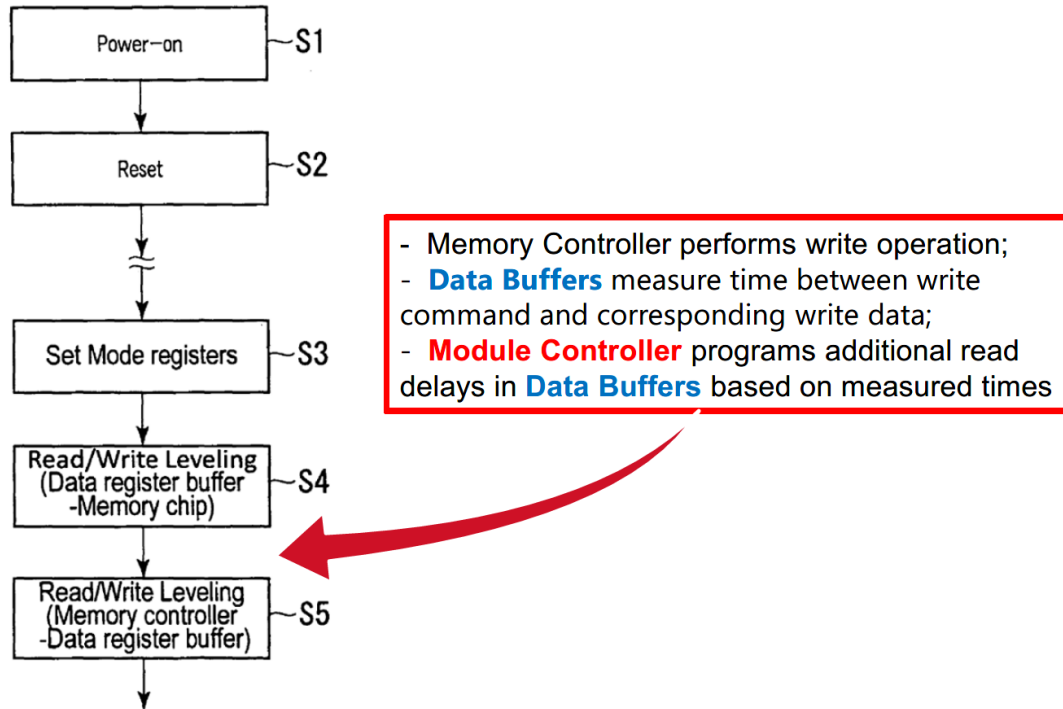
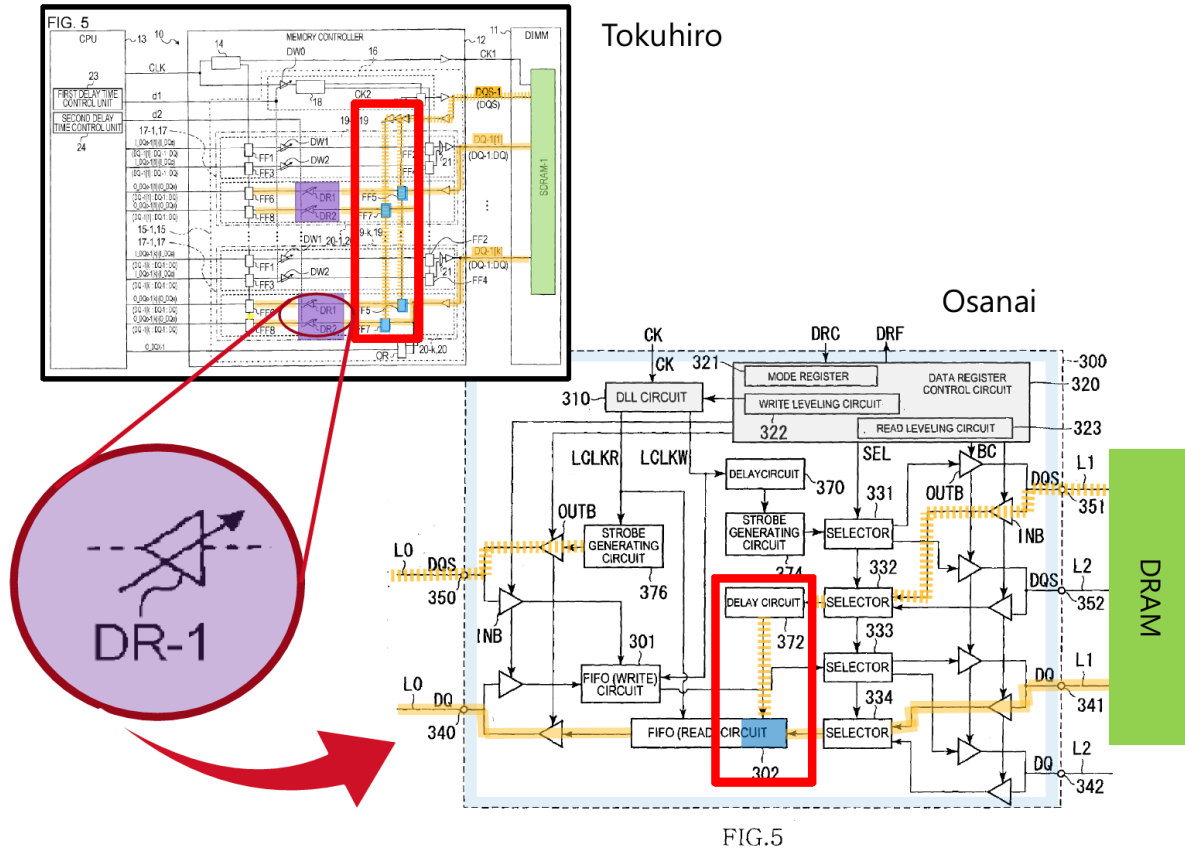


FIG.13



EX1003, ¶¶222-223; *supra* pp.49-57 (discussing annotated figures above).

Accordingly, Grounds 1-3 teach all limitations of claim 1.

- j) [2]: *first memory operation is a memory read operation, second memory operation is a memory write operation*

Grounds 1-3 disclose this limitation. As explained above, *supra* pp.35-57, 70-73, 81-83, Osanai in light of Butt and Tokuhiro renders obvious that the “second memory operation is a memory write operation,” where time intervals for a normal write operation is measured as part of initialization (as illustrated below between S4 and S5) to remove large fly-by delays without adding circuitry in the system memory controller, and that the subsequent “first memory operation is a

memory read operation,” where the previously measured timing information is applied to normal read data/strobe signals using Tokuhiro’s delay elements implemented in Osanai’s buffer circuit. EX1005, Fig.13 (below, annotated); EX1003, ¶224.

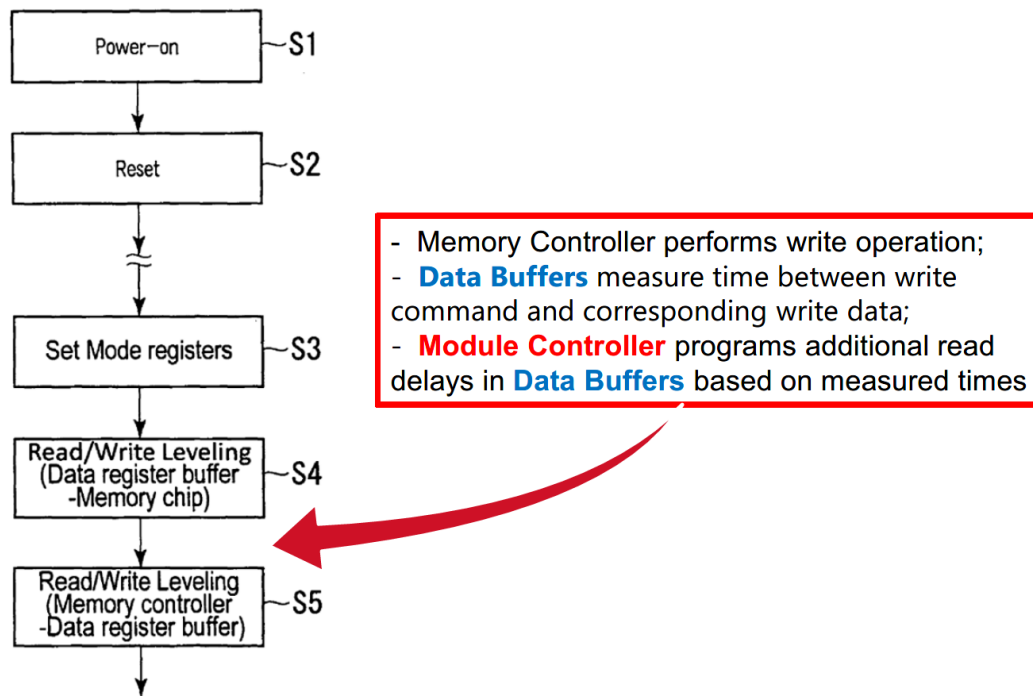


FIG.13

The combination for Grounds 1-3 satisfies the Board’s interpretation of “*memory read operation*” and “*memory write operation*” in IPR2022-00236 discussed above, *supra* pp.19-20, 23 (citing EX1066, 43-45), because in the combination the “*memory write operation*” is a normal write operation by the system memory controller during initialization to remove the large fly-by delays

before read/write leveling (as shown by annotated Figure 13 directly above), *supra* pp.52-57; EX1003, ¶¶184, 187, 118, and the “*memory read operation*” is a normal read operation after initialization, all of which is consistent with the examples in the ’035 Patent discussed above, *supra* pp.12-17; EX1003, ¶¶56, 89. EX1003, ¶225.

2. Claim 3

As explained above, *supra* pp.35-57, Grounds 1-3 disclose “*wherein the each respective buffer circuit includes a delay control circuit [e.g., similar to the one determining “time A” in Osanai’s buffer circuit, EX1005, ¶[0157]], configured to determine, during the memory write operation [e.g., issued by the memory controller between Osanai’s S4 and S5 leveling operations as shown by the annotated Figure 13 of Osanai, supra pp.52-57], a time interval between receiving a first signal [e.g., the re-driven write command] from the module control device and receiving a second signal [e.g., write data/strobe signals] from the memory controller, and wherein the timing information [from 1[f] above (pp.81-83)] includes the time interval [e.g., the respective delay for read data/strobe signals for each data buffer as explained for 1[f], supra pp.52-57, 81-83].*” EX1003, ¶¶226-227.

3. Claim 4

Grounds 1-3 disclose “the each respective buffer circuit is further configured to receive a module clock signal [e.g., CK] and further includes a clock regeneration circuit [e.g., including DLL circuit 310] configured to generate a local clock signal [e.g., for internal operations] having a programmable phase relationship with the module clock signal [e.g., CK],” just like the local clocks LCLKW and LCLKR have a programmable phase relationship with the module clock signal CK. EX1005, Fig.5 (below); EX1003, ¶¶229-230.

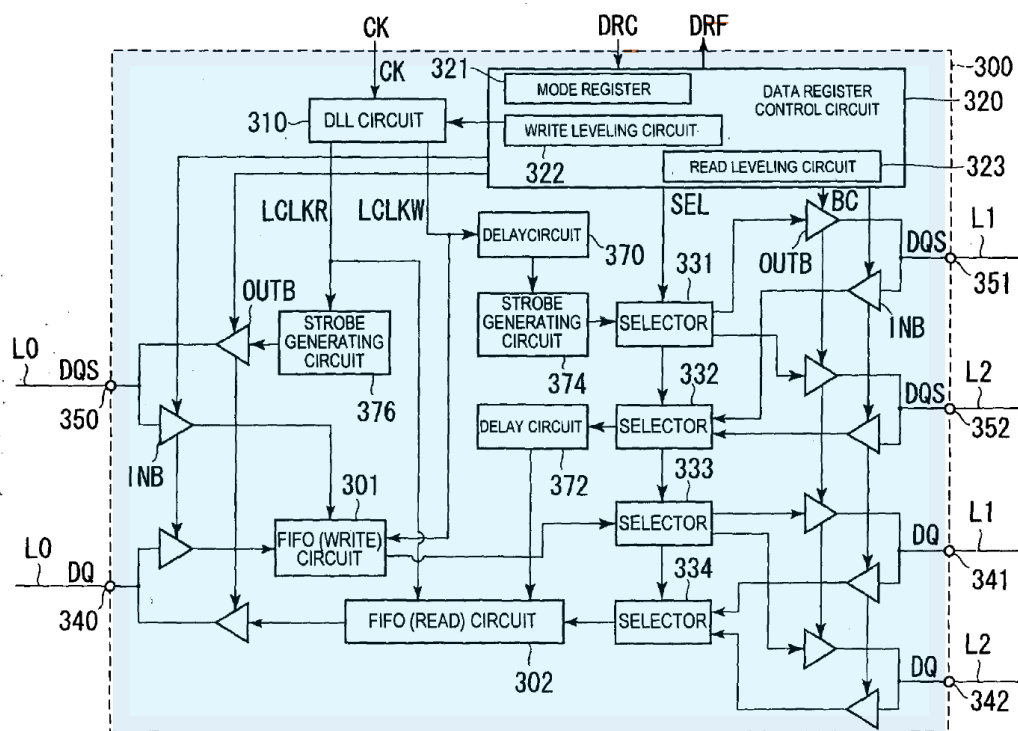


FIG.5

For example, Osanai teaches that the DLL circuit 310 (above) generates local clock signals LCLKR and LCLKW based on the module clock signal CK,

EX1005, ¶[0093], and further teaches that DLL circuit 310 is a clock regeneration circuit configured to generate local clock signals (for the internal operation of the data register buffer 300) where those local clock signals have a programmable phase relationship relative to the module clock signal CK, EX1005, ¶¶[0080], [0151], [0169].

Grounds 1-3 further disclose “*wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices [e.g., when the memory devices do not contain a DLL circuit].*” EX1003, ¶¶231-233. Although Osanai discloses embodiments in which the buffer circuits 300 and memory devices 200 each have their own DLL circuits (and thus there is no need for the local clock of the buffer circuits to be output to the memory devices), Osanai also discloses that:

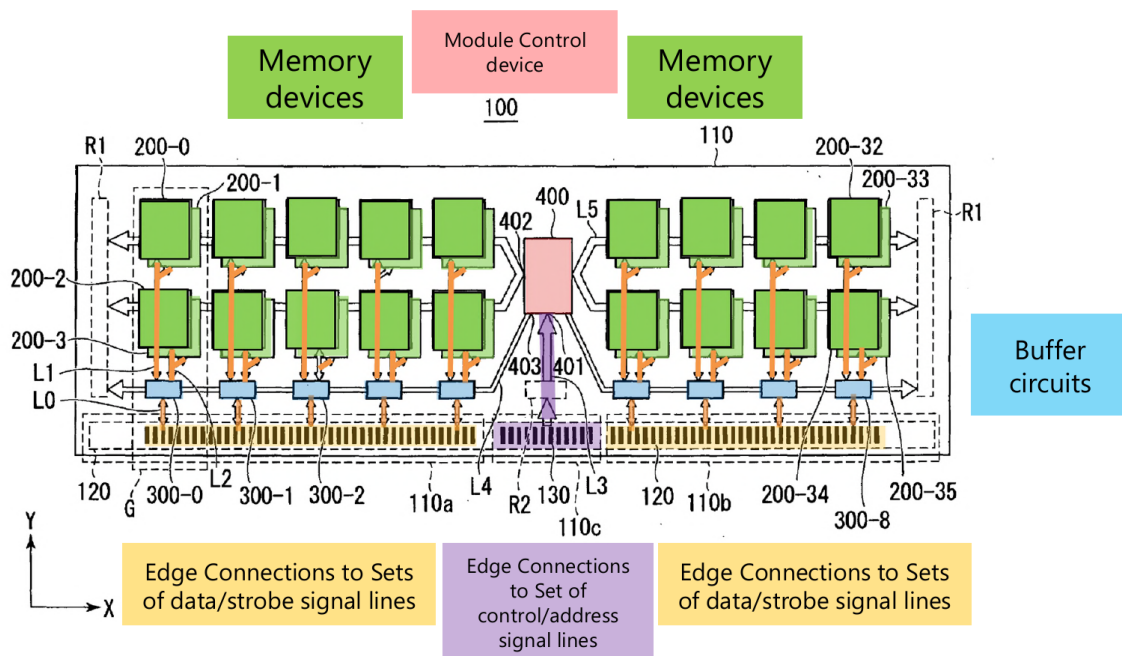
[W]hile the above embodiment has described a memory chip that includes a DLL circuit therein as the memory chip 200, ***a memory chip that does not include a DLL circuit therein can be alternatively used.*** In this case, ***the DLL circuit included in the data register buffer 300 is used to adjust the input/output timing.***

EX1005, ¶[0206]. Thus, Osanai teaches that when the memory devices do not include a DLL circuit, it is the DLL circuit in the buffer circuit 300 which is used as the “*local clock signal*” to adjust the input/output timing in the memory devices as well, to synchronize the operations of those memory devices with the buffer

circuit. *Id.*; EX1003, ¶232; *see also* EX1009, 4:5-14, 4:31-41, FIG.1B (similar); EX1003, ¶233.

4. Claim 5

Grounds 1-3 disclose “wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.” *See, e.g.,* EX1005, ¶¶[0059] (“An arrow of each of the data lines L1 and L2 [(orange)] shown in FIG. 1 indicates a line of 1 byte (8 bits).”), [0090-91] (“a single data register buffer 300 inputs and outputs 1-byte data.”), FIG.1 (annotated below).



The Board has already found that Osanai teaches claim 10, EX1066, pp.46-47, which is substantially similar to claim 5. EX1003, ¶235. The Board has also

found that Hiraishi, which has the same relevant disclosure as Osanai, in view of Ellsberry discloses similar limitations. EX1068, 25-26; EX1003, ¶¶75, 235.

The disclosure above teaches that each memory chip is connected to the data buffer by a one byte (8-bit) wide data line and, accordingly, “*each of the memory devices has a data width of 1 byte.*” EX1003, ¶236. At the time, memory devices with a data width of 8-bits, including DDR3 memory devices expressly described by Osanai, (EX1005, ¶¶[0169], [0176]), had been standardized as one of only a few possible data widths for such memory devices, and 8-bit wide (“x8”) memory devices were commonly used for DIMM memory modules. EX1003, ¶236; EX1020, 3-12 (describing standard DDR3 memory devices with x4, x8, and x16 data widths); EX1018, 4.20.4-25 to -27 (x8 and x4 memory devices). Furthermore, Ellsberry in Ground 2 expressly teaches x8 memory devices. EX1007, Fig.13 (“/8”); *supra* pp.57-59. The disclosure above also teaches that each data register buffer has a data width of one “byte,” see EX1005, ¶¶[0090-91], and thus “*each of the plurality of buffer circuits has a data width of 1 byte.*”

5. Claim 6

Grounds 1-3 disclose “*wherein the memory devices are arranged in a plurality of ranks [e.g., Osanai’s “four-Rank configuration,” EX1005, ¶[0057]] and the respective set of memory devices include one memory device from each of the plurality of ranks [e.g., “memory chips 200-0 to 200-3 belong[ing] to different*

Ranks from each other,” *id.*, ¶[0058]], and wherein the module command signals include chip select signals [“a chip select (CS) signal,” *id.*, ¶[0057]] that select one memory device in the respective set of memory devices to output the respective data and strobe signals [see EX1005, ¶¶[0084]-[0087], Fig.4 (204 for DQ data signals and 205 for DQS strobe signals)].”

The Board has already found that Osanai teaches claim 11, EX1066, pp.47-48, which is substantially similar to claim 6. EX1003, ¶239. The Board has also found that Hiraishi, which has the same relevant disclosure as Osanai, in view of Ellsberry discloses similar limitations. EX1068, 7-10, 25-26; EX1003, ¶¶75, 239.

Osanai discloses a “four-Rank configuration,” where there are four memory chips in a group, and each is in a different rank. EX1005, ¶¶[0057]-[0058]; EX1003, ¶240. Ellsberry in Ground 2 discloses a similar arrangement, with four separate chip-select (CS) signals corresponding to separate memory devices in four different ranks, consistent with the JEDEC standard. *Supra* pp.57-59; EX1020, 13 (“Chip Select....provides for external Rank selection”). Osanai also discloses that each rank of memory devices is selected by a respective chip select signal. EX1005, ¶¶[0057] (“one of the Ranks is selected by exclusively activating a chip select (CS) signal”). Thus, because the “*respective set of memory devices*” includes one memory chip from each rank, the chip select signals select one memory device in that “*respective set.*” *Id.*; EX1003, ¶241. In addition, the chip

select signals are part of the “*module command signals*” sent to the memory devices, EX1005, ¶[0082], consistent with the JEDEC standards, EX1020, 13 (“Chip Select”), 33 (Command Table showing chip selects (CS) part of every command signal to DDR3 memory devices), 34 n.1. EX1003, ¶241. Osana further discloses that the selected memory device inputs (for a write operation) or “*output[s]*” (for a read operation) “*respective data*” (DQ) and “*strobe*” (DQS) signals on terminals 204 and 205, as shown below. *Id.*; EX1005, ¶¶[0084]-[0087], Fig.4 (below).

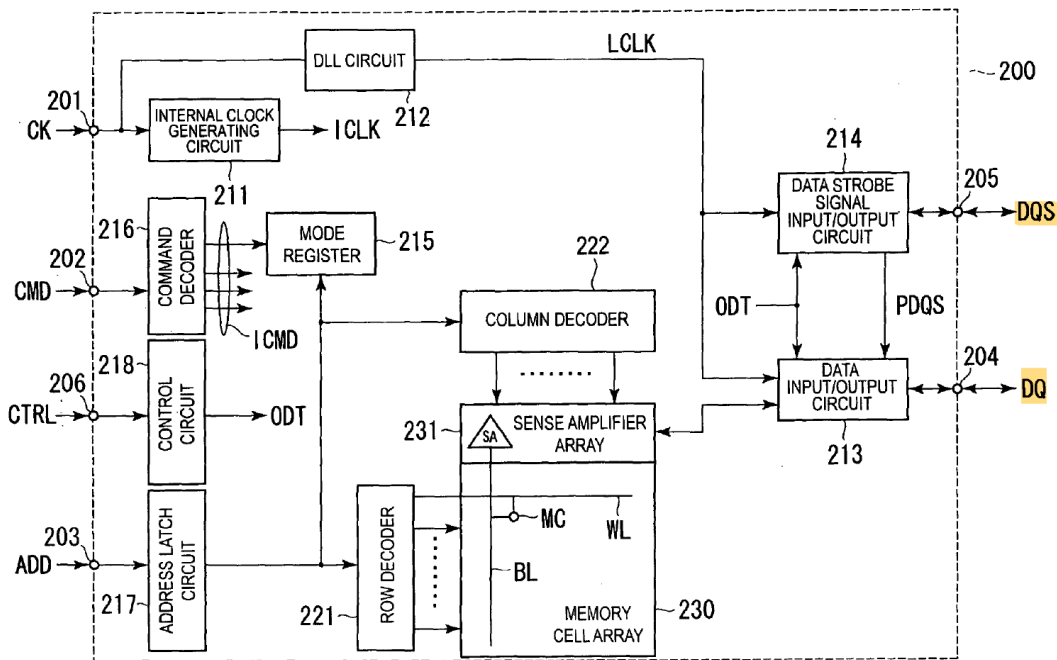


FIG.4

6. Claim 7

Grounds 1-3 disclose “*each of the plurality of buffer circuits has a data width of 1 byte [as explained for claim 5 (pp.88-89)], and wherein each of the*

memory devices has a data width of 4 bits [e.g., “x4” DDR3 memory devices, as was a standard option, EX1005, ¶[0169] (“DDR3”); EX1020, 3, 6 (“x4”).”

The Board has already found that Osanai teaches claim 12, EX1066, pp.48-50, which is substantially similar to claim 7. EX1003, ¶243. The Board has also found that the combination of Hiraishi (which has the same relevant disclosure as Osanai) and Ellsberry teaches similar limitations. EX1068, 25-26; EX1003, ¶¶75, 243.

As explained above for claim 5, *supra* pp.88-89, Osanai discloses byte-wide buffer circuits, each coupled with a byte-wide DDR3 memory device. Osanai also renders obvious that such a byte-wide DDR3 memory device could be replaced with two 4-bit wide memory devices, as was a standard option at the time for DDR3. EX1005, ¶[0169] (“DDR3”); EX1020, 3-12 (describing standard DDR3 memory devices with x4, x8, and x16 data widths); EX1018, 4.20.4-25 to -27 (showing either x8 or pairs of x4 memory devices can be used on a DIMM); EX1003, ¶244.

Also, as explained above, pp.57-59, Ellsberry in Ground 2 expressly describes byte-wide data buffers, each coupled with either a byte-wide (below right) or two 4-bit wide memory devices (below left). *See, e.g.*, EX1007, Figs.11 (“/4”), 13 (“/8”) (below); EX1003, ¶245.

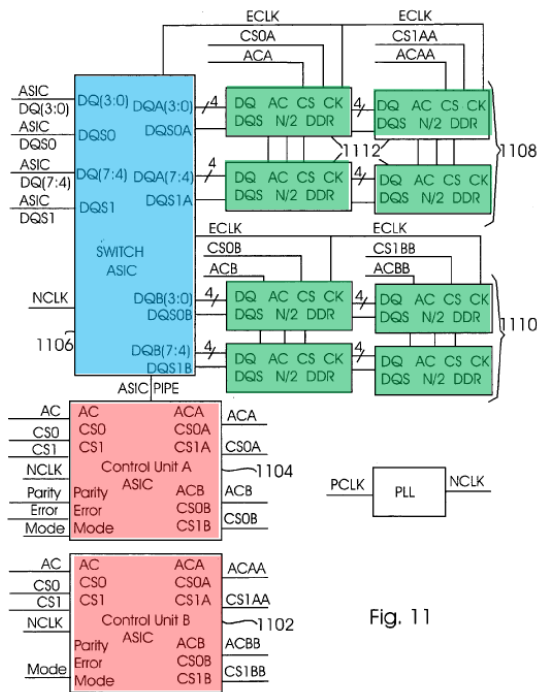


Fig. 11

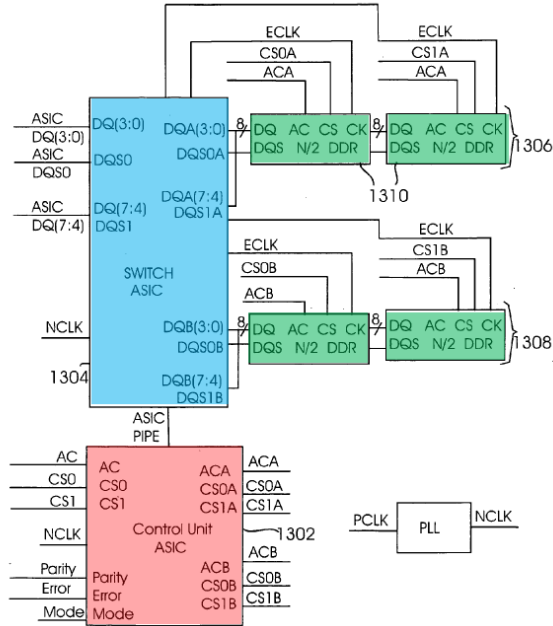


Fig. 13

The Board has already found that Figures 2, 5, and 13 of Ellsberry correspond to an embodiment utilizing byte-wide memory devices, while Figures 2, 6, and 11 correspond to another embodiment utilizing pairs of 4-bit wide memory devices. EX1015, 77-78. For the 4-bit embodiment relevant here, Ellsberry explains that the memory module of Figure 6 “uses a dual stack configuration (similar to that illustrated in FIG. 11).” EX1007, ¶[0051]. Thus, in Figure 11 above, two 4-bit wide memory devices are stacked in each “CSP” package (like in Figure 6) rather than using byte wide memory devices as shown in Figure 13; furthermore, a pair of 4-bit wide memory devices receive the same chip select (CS) signal (as shown in Figure 11). EX1007, ¶¶[0051], [0054]; EX1003, ¶246. The Board has repeatedly found in Final Written Decisions against Netlist

that Ellsberry discloses pairs of 4-bit memory devices. EX1015, pp.77-78; EX1031, pp.35, 62-63.

7. Claim 8

Grounds 1-3 disclose “*wherein the memory devices are arranged in a plurality of ranks [as explained for claim 6 (pp.89-91)] and the respective set of memory devices include two memory devices from each of the plurality of ranks [each 4-bits wide, as explained for claim 7 (pp.91-94)], and wherein the module command signals include chip select signals that select two memory devices in the respective set of memory devices [as explained for claim 7 (pp.91-94), such as chip-select signal “CS0A” in the upper left of Figure 11 of Ellsberry, EX1007] to output the respective data and strobe signals [as explained for claim 6 (pp.89-91)], the two memory devices being in a same rank [as explained for claim 7 (pp.91-94), such as the two 4-bit memory devices connected to chip-select signal “CS0A” in the upper left of Figure 11 of Ellsberry, EX1007].*”

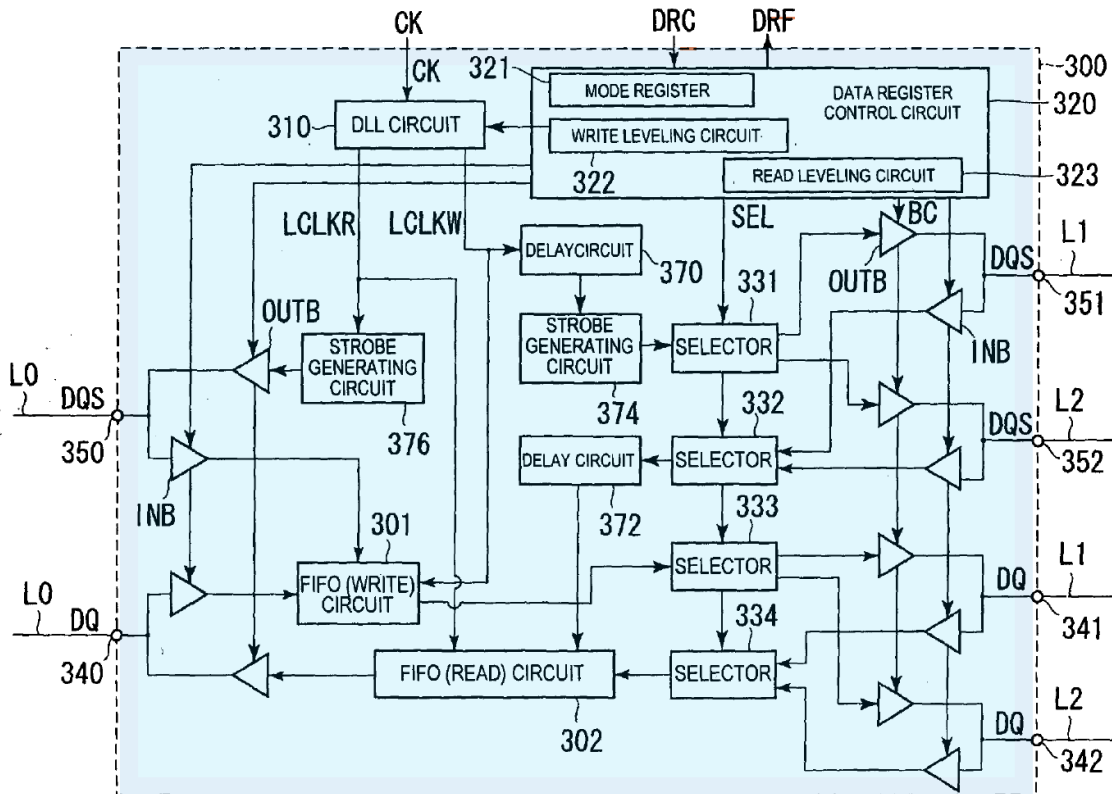
The Board has already found that Osanai teaches claim 13, EX1066, p.51, which is substantially similar to claim 8. EX1003, ¶248. The Board has also found that the combination of Hiraishi (which has the same relevant disclosure as Osanai) and Ellsberry teaches similar limitations. EX1068, 7-10, 25-26; EX1003, ¶¶75, 248.

When 4-bit wide memory devices are used for Osanai's byte-wide data buffers, as discussed above for claim 7, *supra* pp.91-94, two 4-bit memory devices are needed for each rank to match the byte-wide data buffers, in which case chip select signals in the “*module command signals*,” *supra* pp.89-91, select the two memory devices in the same rank to output respective data/strobe signals. EX1003, ¶¶249-250; EX1018, 4.20.4-15 (showing two ranks of x4 memory devices, with each rank of memory devices connected to the same chip select (CS) signal).

Also, as explained above for claim 7, *supra* pp.91-94, Ellsberry in Ground 2 expressly discloses byte-wide data buffers, each coupled to two 4-bit wide memory devices, which are in the same rank, and thus coupled to and selected by the same chip select signals (e.g., “CS0A” in Figure 11). EX1007, Fig.11, ¶¶[0051], [0054]; EX1020, 13 (“Chip Select . . . provides for external Rank selection on systems with multiple Ranks”); EX1003, ¶¶251-252.

8. Claim 9

Grounds 1-3 disclose “*each respective buffer circuit is further configured to receive a module clock signal [e.g., CK] from the module control device and further includes a receiver circuit [e.g., in DLL circuit 310 and Data Register Control circuit 320] for each of the module control signals [e.g., DRC], the receiver circuit includes a metastability detection circuit configured to determine a*



The Board has already found that the combination of Hiraishi (which has the same relevant disclosure as Osanai) and Kim teaches similar limitations. EX1068, 26-30; EX1003, ¶¶75, 254.

For example, Osanai discloses that the control signal DRC and the corresponding clock CK are transmitted on control line L4 to multiple Data Register Buffers (blue). EX1005, Fig.7 (annotated below); EX1003, ¶256.

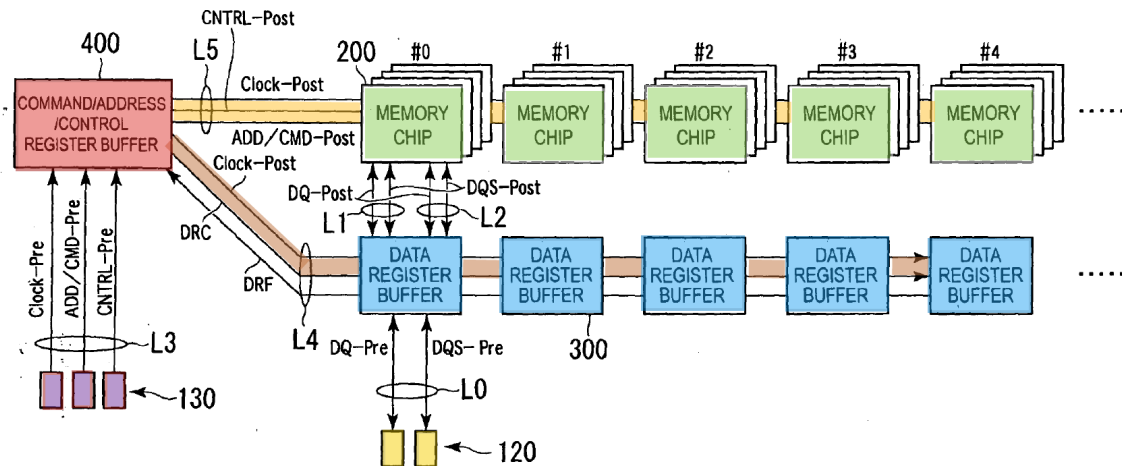


FIG.7

Osanai also discloses that the DLL circuit 310 in the data buffer receives the module clock signal CK and generates from this CK signal a number of internal clocks, including LCLKR and LCLKW, with fine phase adjustments that are used for the internal operation of the data buffer (*see, e.g.*, EX1005, FIG.5) and that the DRC signal is captured by the Data Register Control unit 320. *Id.* Thus, Osanai discloses that DLL circuit 310 generates, based on the received clock signal CK, the internal clock that is used to capture the DRC signal, EX1003, ¶257, and that the internal clock is generated with a specific phase that is selected to avoid

metastability because the control information conveyed by the DRC signal may not be correctly captured if there is a metastability condition at the input of the DRC signal. *Id.* (citing EX1008, 1:21-31). Due to the high speed at which the memory devices operated at the time, Osanai teaches that the “use of the DLL circuit is substantially essential.” EX1005, ¶[0169].

In light of the possibility of erroneous DRC signal reading, the Data Register Control Circuit 320 includes a known metastability condition detector (such as taught by Kim, EX1008) and implements the DLL circuit 310 to avoid such potential metastability by adjusting the phase of the internal clock signal that is used to capture the DRC signal (like how Osanai’s DLL circuit adjusts the LCLKW signal’s phase). EX1003, ¶258. Such a metastability condition detector can be used, e.g., during initialization to indicate the presence of a metastability condition so that the phase of the internal clock is adjusted to avoid the metastability condition. *Id.*

Ground 3 (with Kim) further renders obvious this claim. As explained above for Ground 3 (pp.59-60), Kim expressly discloses “a metastability detection/prevention circuit 20” in “a data input buffer,” EX1008, 2:23-37, which a POSITA would have been motivated to incorporate in Osanai’s data buffers to detect metastability at the DRC input and remove the metastability by adjusting the phase of the corresponding internal clock, EX1003, ¶259. As discussed above, the

Board has already agreed that a POSITA “would have been motivated to include [Kim’s] metastability condition detector functionality” in Hiraishi (which has the same relevant disclosure as Osanai). EX1068, 26-30.

9. Claims 14 and 17-20

The limitations of claims 14 and 17-20 are substantially similar to earlier limitations, as shown in the following table, and thus they are obvious in light of Grounds 1-3 for at least the same reasons discussed above and further below:

This limitation...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[14]	[4]
[17]	[5]
[18]	[6]
[19]	[7]
[20]	[8]

Claims 18 and 20 further recite a “*memory device...to output or receive the respective data and strobe signals in accordance with the local clock signal,*” which is also taught by Grounds 1-3 for the reasons discussed above for claim 4. *See supra* pp.86-88. As discussed above, when “a memory chip...does not include a DLL circuit...[and thus] the DLL circuit included in the data register buffer 300 is used,” EX1005, ¶[0206], the memory chip communicates data/strobe signals in

accordance with the local clock signal generated by the data buffer's DLL circuit to synchronize data transfers. EX1003, ¶¶273, 279.

10. Claim 15

Grounds 1-3 disclose “the data paths [e.g., for read operations] include a first data path for transmitting a strobe signal [e.g., the data path coupled to the line L1 or L2 at the input/output terminal 351 or 352, for transmitting data strobe signals (DQS, dashed orange line), as already found by the Board for 1[e] discussed above, *supra* pp.76-81 (citing EX1066, 25-26; EX1068, 7-10, 13)] among the respective data and strobe signals.” EX1003, ¶¶263-264; EX1005, FIG.5 (below, annotated).

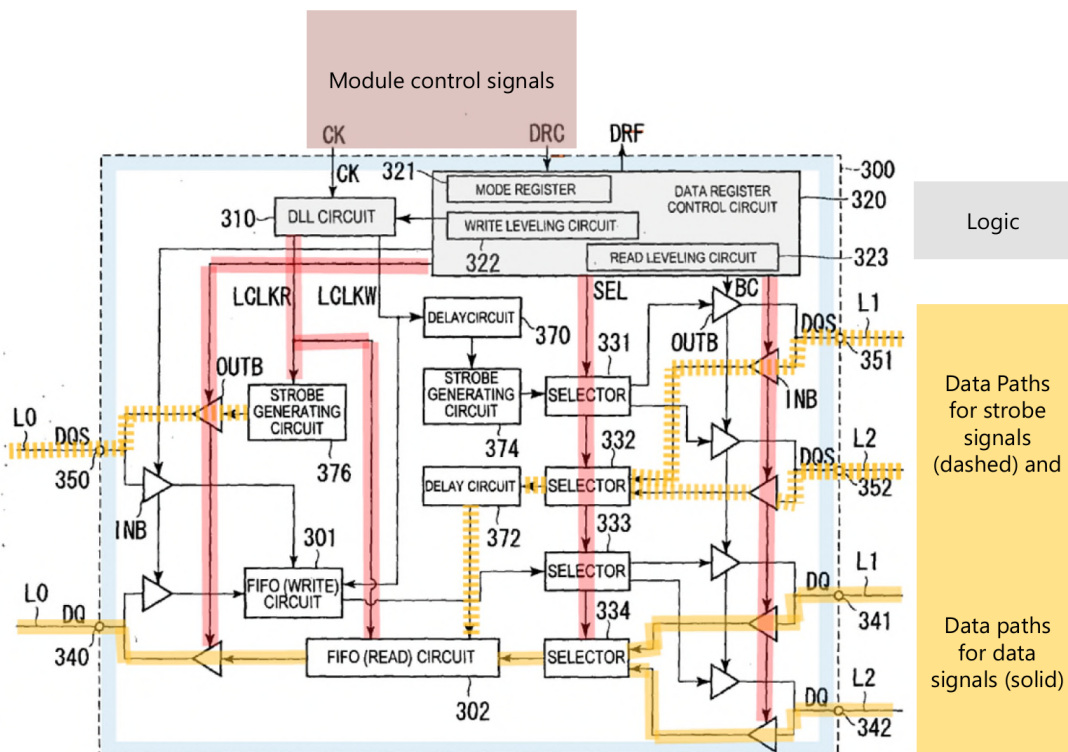


FIG.5

As shown above, either L1 or L2 could be considered a “*first data path*,” but only one of them would be used at a given time, to avoid conflicts. EX1003, ¶264. In other words, like Figure 15 of the ’035 Patent (below), Osanai’s data paths have a “fork in the road” arrangement for routing data strobe signals from either one (L1) or the other (L2) branch to the same output (terminal 350, coupled to line L0) during read operations. *Id.*; compare EX1005, Fig.5, with EX1001, Fig.15 (both reproduced below with annotations: dashed orange lines added to indicate paths for data strobe signals during read operations—the gap in the dashed orange lines includes circuitry that provides the required delays of strobe signals through the data buffer).

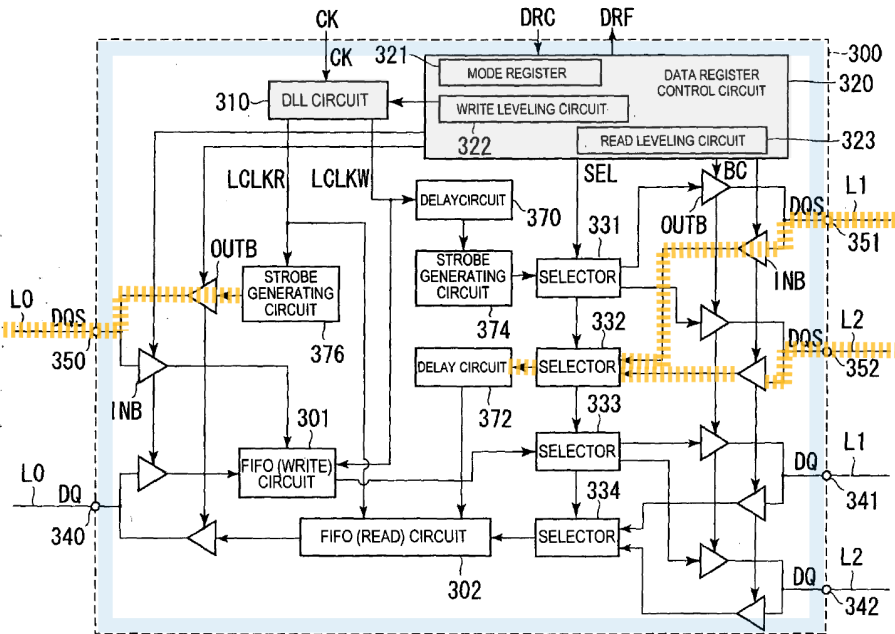


FIG.5

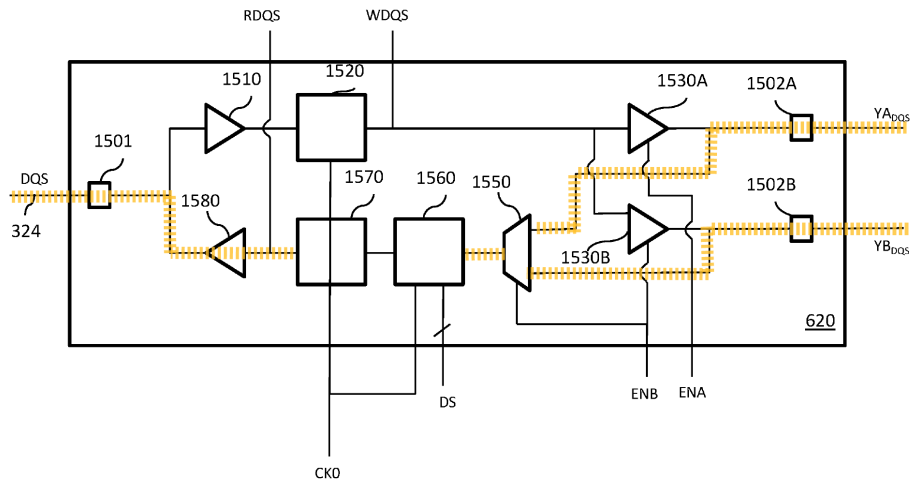


FIG. 15

Grounds 1-3 also disclose “the first data path including a sampler [e.g., Osanai’s delay circuit 372 in Figure 5 above] that samples the strobe signal [DQS, dashed orange] in accordance with the local clock signal [discussed above for claims 4 and 14 (pp.86-88, 99)],” just like the data path disclosed in Figure 15 of the ’035 Patent (above). EX1003, ¶265; cf. EX1001, 13:23-27 (’035 Patent disclosing that “a sampler or register circuit ... samples the ... signal ... according to the clock signal”), 17:10-13 (similar). Specifically, Osanai teaches that sampling happens at delay circuit 372 to sample the DQS signal, in accordance with the local clock of the data register buffer (e.g., in order to detect the phase of the DQS signal and to delay the signal “by about 90 degrees” relative to the local clock). EX1005, ¶[0097]; EX1074, 154:15-22 (confirming either clock or strobe signals may be used for sampling); EX1003, ¶265; see also EX1028, FIG.2 (showing phase comparator 35 sampling the strobe signal DQS in accordance with

a local clock CLKb to delay the strobe signal by 90 degrees), 5:37-7:11 & FIGs.3-4 (showing the DQS strobe signal delayed by about 90 degrees relative to the local clock).

11. Claim 16

Grounds 1-3 disclose “*the data paths [e.g., for read operations] include a second data path for transmitting a first data signal [e.g., the data path coupled to the data line L1 or L2 at the input/output terminal 341 or 342 for transmitting a data signal (DQ, solid orange line)] among the data and strobe signals.*” EX1003, ¶¶266-267; EX1005, FIG.5 (below, annotated).

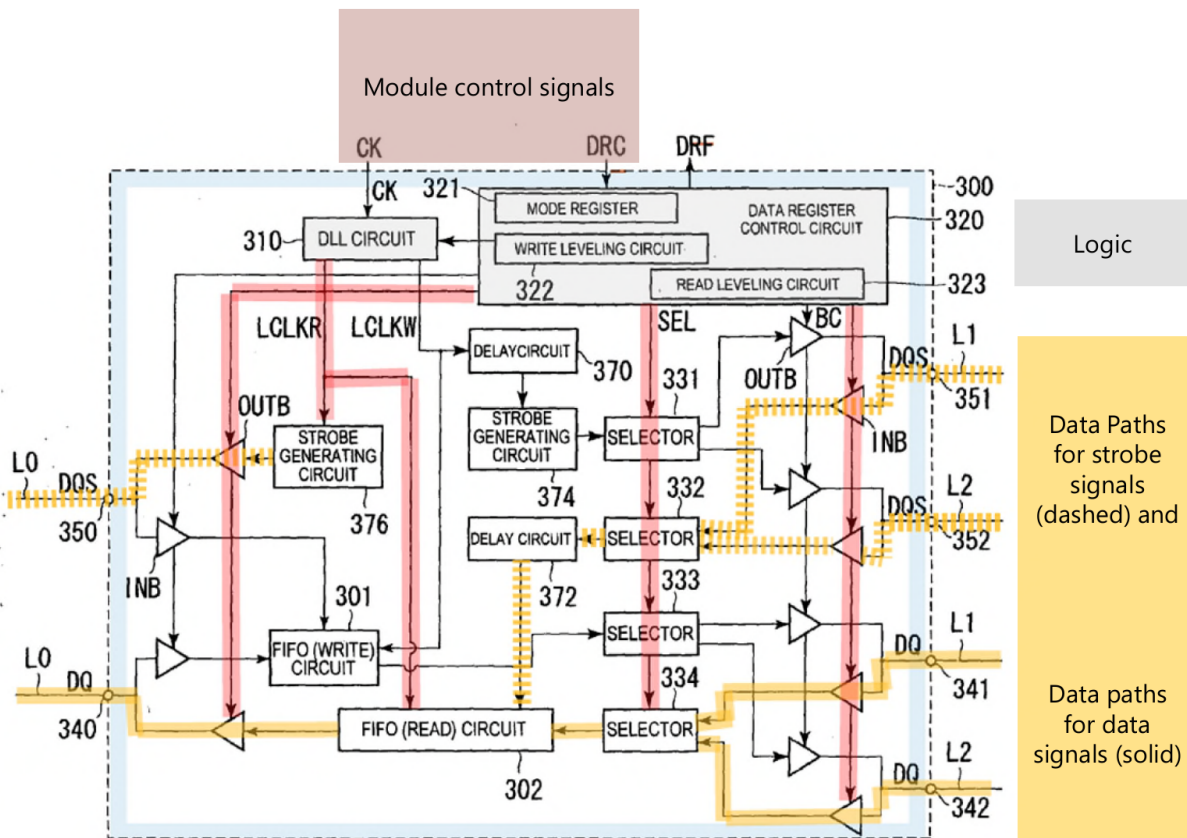


FIG.5

As also shown in the figure above and similar to the DQS strobe signals discussed for claim 15, *supra* pp.100-103, the data paths in Osanai have a “fork in the road” arrangement for routing DQ data signals from either one (L1) or the other (L2) branch to the same output (terminal 340, coupled to line L0) during read operations, similar to Figure 16 of the '035 Patent (below). EX1003, ¶267; Compare EX1005, Fig.5, with EX1001, Fig.16 (both reproduced below with annotations: solid orange lines added to indicate paths for data signals during read operations, and dashed orange lines added to indicate the sampled strobe signal).

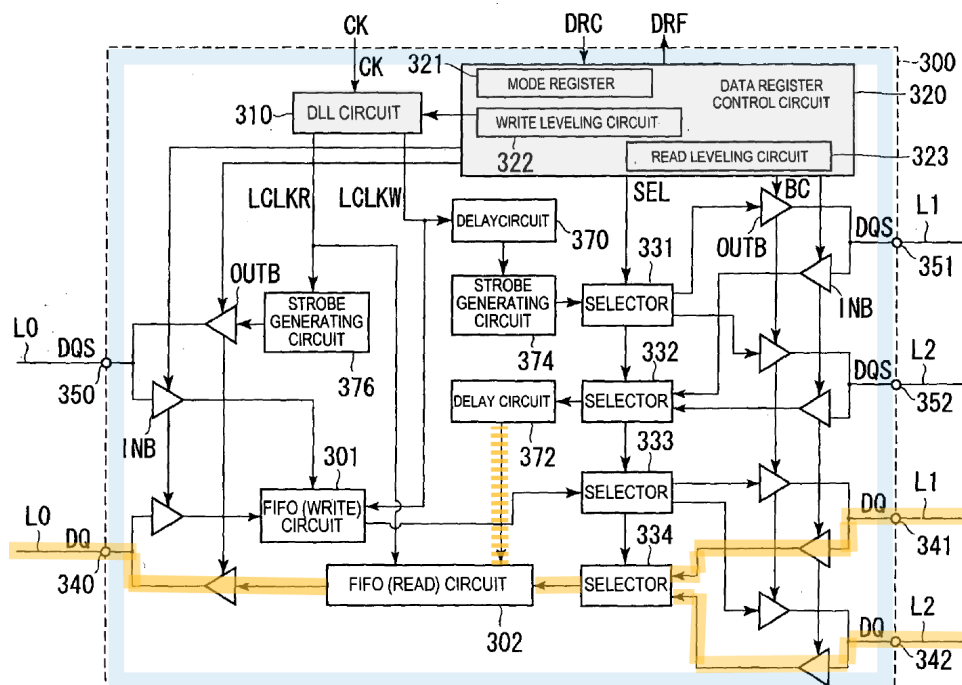


FIG.5

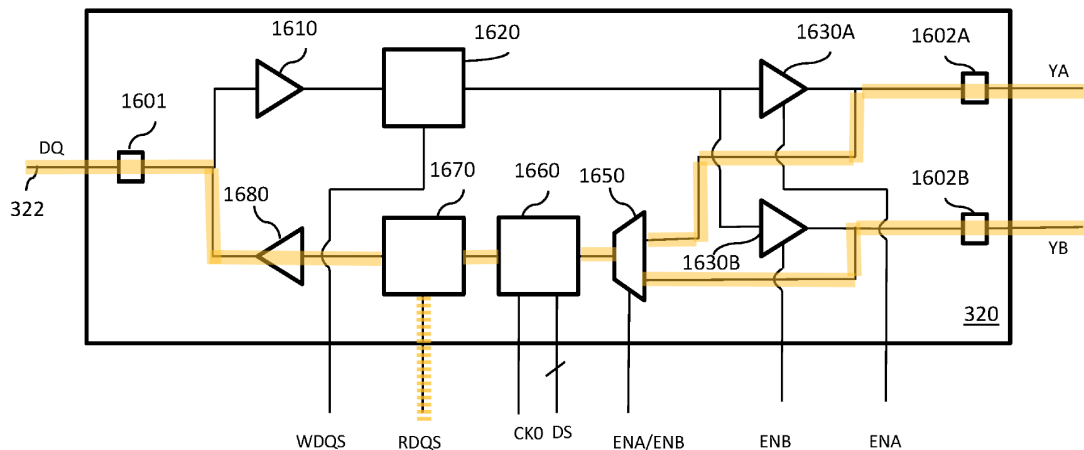


FIG. 16

Grounds 1-3 also disclose “*the second data path including a sampler [e.g., Osanai’s FIFO (Read) circuit (302)] that samples the first data signal in accordance with the sampled strobe signal,*” just like the data path disclosed in Figure 16 of the ’035 Patent (above). EX1003, ¶268; EX1001, 13:23-27, 17:51-53. Specifically, Osanai teaches that sampling the data signal in accordance with the sampled strobe signals happens at the FIFO (Read) circuit (302) and that this process requires a latch where the delay circuit 372 provides the sampled strobe signal “as an input trigger signal” that determines the timing for how the FIFO clocks in the data. EX1003, ¶268; EX1005, ¶[0097]. When the data signal is latched in the FIFO, it is necessarily sampled (registered) like in the ’035 Patent, and because the delayed DQS signal from 372 acts “as an input trigger signal” to

latch the data in the FIFO (Read) circuit 302, the data signal is necessarily sampled in accordance with the sampled strobe signal from 372. *Id.*

VII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 2-9 and 14-20 be canceled as unpatentable.

Dated: October 27, 2025

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24(a)(1)(i) (“14,000 words”) because it contains 13,597 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24(a)(1).

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CERTIFICATE OF SERVICE

I hereby certify that on this 27th day of October, 2025, a copy of this
Petition, including all exhibits, has been served in its entirety by FedEx Express on
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