

No. 2025-1378

**IN THE
UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

SAMSUNG ELECTRONICS CO., LTD.,

Appellant,

v.

NETLIST, INC.,

Appellees.

Appeal from the United States Patent and Trademark Office,
Patent Trial and Appeal Board in No. IPR2023-00847

APPELLANT'S PRINCIPAL BRIEF

April 18, 2025

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Netlist EX2052
Samsung v. Netlist
IPR2026-00017

PATENT CLAIM LANGUAGE AT ISSUE
(Appx117 (19:14-20:4, 20:42-61))

1. [pre] A memory module operable to communicate with a memory controller via a memory bus, the memory bus including signal lines, the signal lines including a set of control/address signal lines and a plurality of sets of data/strobe signal lines, the memory module comprising:

[a] a module board having edge connections for coupling to respective signal lines in the memory bus;

[b] a module control device mounted on the module board and configured to receive system command signals for memory operations via the set of control/address signal lines and to output module command signals and module control signals in response to the system command signals, the module control device being further configured to receive a system clock signal and output a module clock signal; and

[c] memory devices mounted on the module board and configured to receive the module command signals and the module clock signal, and to perform the memory operations in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines; and

[d] a plurality of buffer circuits corresponding to respective sets of the plurality of sets of data/strobe signal lines,

[e] wherein each respective buffer circuit of the plurality of buffer circuits is mounted on the module board, coupled between a respective set of data/strobe signal lines and a respective set of memory devices, and configured to receive the module control signals and the module clock signal, the each respective buffer circuit including a data path corresponding to each data signal line in the respective set of data/strobe signal lines, and a command processing circuit configured to decode the module control signals and to control the data path in accordance with the module control signals and the module clock signal,

[f] wherein the data path corresponding to the each data signal line includes at least one tristate buffer controlled by the command processing circuit and a delay circuit configured to delay a signal through the data path by an amount

determined by the command processing circuit in response to at least one of the module control signals.

2. [a] The memory module of claim 1, wherein the memory operations include a first memory operation and a second memory operation subsequent to the first memory operation,

[b] wherein the command signals include a first set of command signals for the first memory operation and a second set of command signals for the second memory operation,

[c] wherein the module control signals include a first set of module control signals output by the module control device in response to the first set of command signals and a second set of module control signals output by the module control device in response to the second set of command signals,

[d] wherein the at least one of the module control signals include at least one of the first set of module control signals, and

[e] wherein the signal through the data path is a signal associated with the second memory operation.

9. [a] The memory module of claim 1, wherein the each respective buffer circuit further includes a clock regeneration circuit configured to generate a local clock signal having a programmable phase relationship with the module clock signal,

[b] wherein the each respective buffer circuit is further configured to output the local clock signal to the respective set of memory devices.

10. [a] The memory module of claim 9, wherein the each respective buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory operation and a second data path for transmitting a first data signal associated with the second memory operation,

[b] the first data path including a sampler that samples the strobe signal in accordance with the local clock signal, and the second data path including a sampler that samples the first data signal in accordance with the sampled strobe signal.

11. The memory module of claim 10, wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 1 byte.

FORM 9. Certificate of Interest

Form 9 (p. 1)
March 2023

**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

CERTIFICATE OF INTEREST

Case Number 2025-1378

Short Case Caption Samsung Electronics Co., Ltd. v. Netlist, Inc.

Filing Party/Entity Samsung Electronics Co., Ltd.

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☒ None/Not Applicable ☐ Additional pages attached

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STATEMENT OF RELATED CASES

No appeal in or from the same action was previously before this or any other appellate court. Below are cases known to counsel to be pending in any tribunal that will directly affect or be affected by this Court's decision in the pending appeal:

1. *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 24-1521 (Fed. Cir.) (appeal of IPR2022-00711 involving related U.S. Patent No. 10,860,506)
2. *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:22-cv-00293-JRG (U.S. District Court, Eastern District of Texas)
3. *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 1:22-cv-00136-DII (U.S. District Court, Western District of Texas)
4. *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No 1:21-cv-01453-RGA-JLH (U.S. District Court, District of Delaware)
5. *Netlist, Inc. v. Samsung Electronics Co., Ltd.*, No. 8:20-cv-00993-MCS-ADS (U.S. District Court, Central District of California)

JURISDICTIONAL STATEMENT

The Patent Trial and Appeal Board had jurisdiction over the *inter partes* review proceeding under 35 U.S.C. §§ 6(b)(4), 311. The Board entered a Final Written Decision on December 10, 2024. Appx1. Samsung timely appealed on January 13, 2025. Appx10520-26. This Court has jurisdiction to hear the appeal under 28 U.S.C. § 1295(a)(4)(A) and 35 U.S.C. §§ 141(c), 319.

STATEMENT OF THE ISSUES

1. Whether the Board improperly required that the “*data path*” limitation recited in claims 1, 2, and 10 must be located in the separately claimed “*data signal line*,” while excluding, *inter alia*, any “*strobe signal*” from the “*data path*,” where:

- claim 1 only requires a “*a data path **corresponding to each data signal line in the respective set of data/strobe signal lines***”;
- the “*data path*” in claim 1 expressly includes “*a delay circuit configured to delay **a signal** through the data path*,” which dependent claim 10 shows can be “*a **strobe signal***” not just a “*data signal*”; and
- the Board adopted a level of ordinary skill in the art that included knowledge of JEDEC standards under which data signals and strobe signals must travel together within a very tight tolerance.

2. Whether the Board erred in refusing to assess collateral estoppel as to underlying *factual* findings about the prior art made in a previous Final Written Decision involving the parent patent.

3. Whether the Board improperly rejected Samsung’s FIFO-based “*data path*” theory for Ground 1 based on factual findings that were precluded by and contrary to its previous Final Written Decision, and which lacked substantial evidence.

4. Whether the Board erred in refusing to consider whether it would have been obvious to replace the prior-art FIFO of Ground 2 with a delay circuit physically on the DQ data line.

INTRODUCTION

The Board’s decision finding all challenged claims non-obvious depended on its overly narrow construction for claim 1, which recites “*a data path **corresponding to each data signal line in the respective set of data/strobe signal lines . . . wherein the data path . . . includes . . . a delay circuit configured to delay a signal through the data path.***” The Board improperly construed that language to mean that the “*data path*” “**is in**” (rather than merely “correspond[s] to”) the “*data signal line*”—and thus the “*data path*” excludes any “*strobe signal*”—contrary to (i) the ordinary meaning of “*corresponding to*,” (ii) dependent claim 10 reciting “*a first **data path for transmitting a strobe signal,***” and (iii) the understanding of those of ordinary skill about the close relationship between strobe signals and data signals. That legal error requires reversal of the claim construction and remand to assess obviousness under the ordinary meaning of “*corresponding to*” as merely being functionally related, such that the “*data path*” can transmit “*strobe signal[s]*” in addition to the related data signals.

The Board also improperly limited its analysis of collateral estoppel, contrary to the Restatement (Second) of Judgments and binding decisions of this Court. Samsung identified how fact findings regarding the prior art in a previous Final Written Decision precluded contrary findings in this IPR. However, the Board focused on differences in claim language and only analyzed whether collateral

estoppel applied to legal issues, which was irrelevant to the previous factual findings regarding the scope and content of the prior art. On remand, the Board should reassess obviousness in a manner consistent with its previous factual findings about the prior art.

Independently, the Board failed to provide any ruling on Samsung's argument that a person of ordinary skill would be motivated to replace Hiraishi's FIFO circuit with a delay circuit physically on the DQ data line, which would satisfy even the Board's narrow claim construction. Vacatur and remand is required for consideration of Samsung's argument.

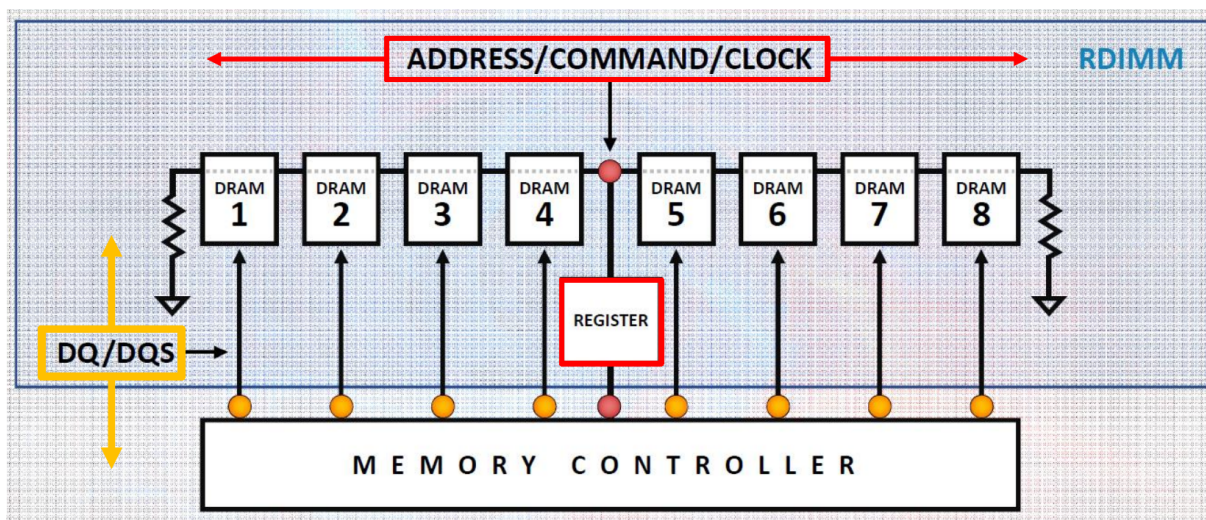
STATEMENT OF THE CASE

I. Technical Overview

Both parties accepted, and the Board adopted, a level of ordinary skill in the art that requires certain educational and work qualifications, as well as “familiar[ity] with the JEDEC industry standards”; “knowledge[] about the design and operation of computer memories, including DRAM and SDRAM devices that were compliant with various standards, and how they interact with other components of a computer system, such as memory controllers”; and “familiar[ity] with the structure and operation of circuitry used to access and control computer memories and other components of a memory system, including sophisticated circuits such as ASICs and

CPLDs, as well as low level circuits such as data buffers, tri-state buffers, flip flops and registers.” Appx8-9.

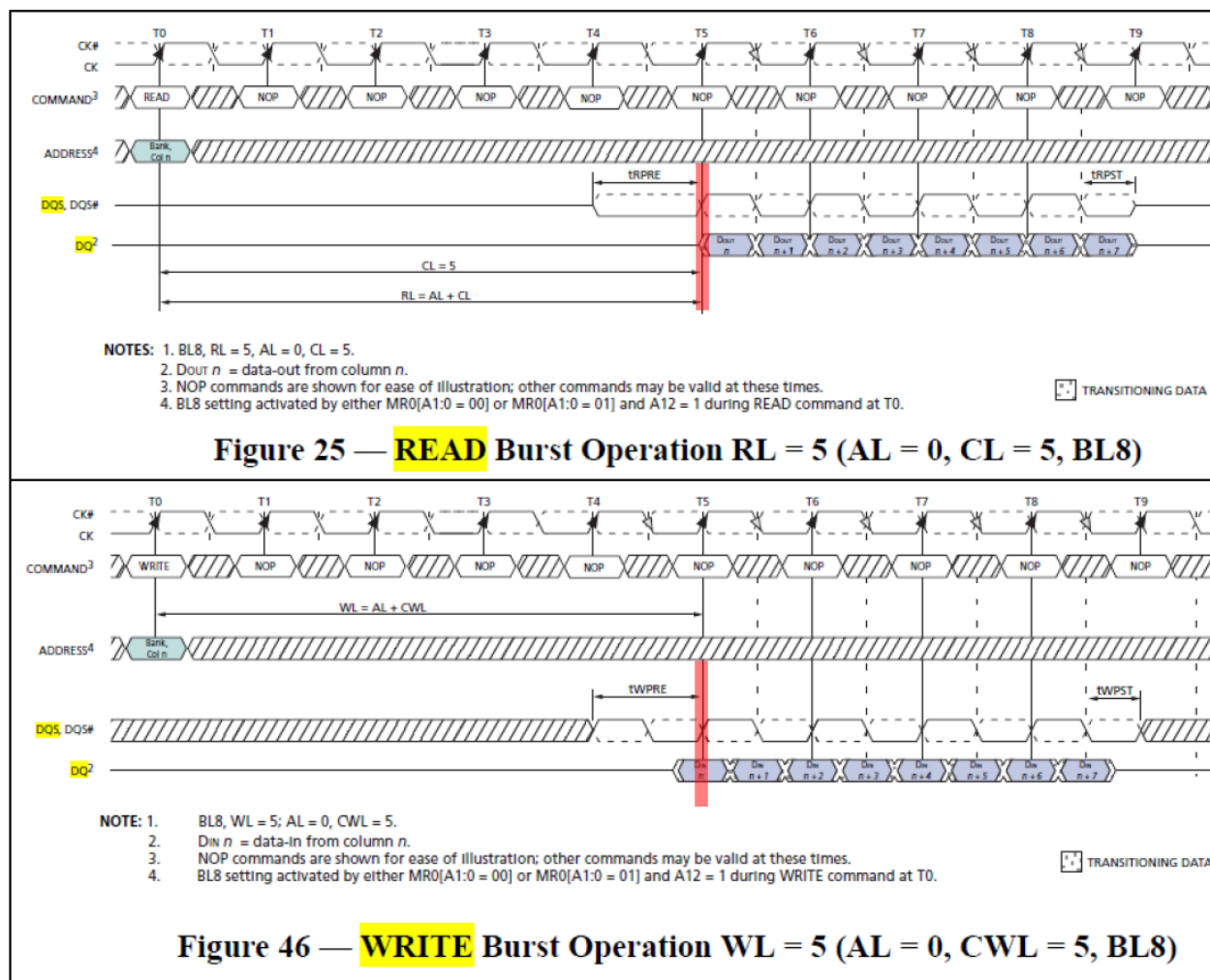
JEDEC is a standards organization that specifies technical requirements for memory devices and memory modules. Under the JEDEC standards, a defining characteristic of DDR (double data rate) DRAM memory is the use of **strobe** (DQS) signals that travel with the data (DQ) signals within a very tight tolerance. Appx3415-16 (“The strobe is called DQS.”); Appx 8933 (91:10-:24), Appx8934-35 (92:16-93:13), Appx8941-42 (99:3-100:4), Appx8981 (139:13-:24). The figure below shows the general layout for a memory module with third-generation DDR3 DRAM memory devices (black rectangles) and how the relevant signals travel. The address, command, and clock (CK) signals (red dots and arrows) are illustrated as travelling **horizontally** across the DDR3 DRAM memory devices—an arrangement called a “fly-by” topology because those signals fly across each memory device rather than arriving at all of the memory devices at the same time, Appx3151—while the data (DQ) and strobe (DQS) signals (orange dots and arrows) are the ones travelling **vertically** to and from the DDR3 DRAM memory devices:



Appx10206 (annotating Appx9585); Appx8899-90 (57:10-58:24). For the memory module to work properly, the red and orange signals above must intersect and align with each other at each DDR3 DRAM memory device at the correct time. Appx10393-94 (6:14-7:2); Appx6920-22. Precise alignment of the signals is particularly important with third-generation DDR3 DRAM memory devices because, by 2012, their clock speeds were in the billionths of a second (e.g., 1.25 ns), leaving little room for misalignment of the signals. Appx9583; Appx7643 (“tCK”); Appx3168, Appx3273 (requiring any misalignment to be less than “tDQSQ” trillionths of a second).

As shown below, the figures in the JEDEC standard require precise alignment of the DQ data signal, DQS strobe signal, and CK clock signal for read and write operations. For read operations (top), all three signals must be “edge-aligned” (e.g., at time T5 as shown by the red line), while for write operations (bottom), the DQ

data signal must be “center-aligned” with the edge of the DQS strobe and CK clock signals (e.g., at time T5 as shown by the red line):



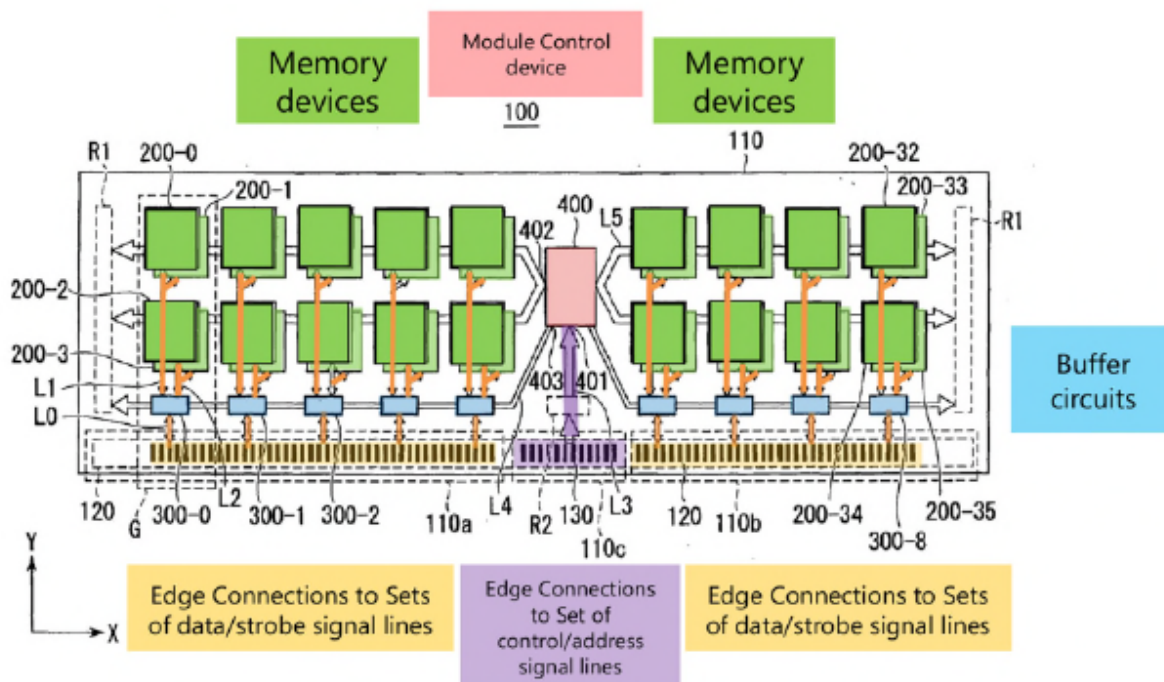
Appx10208 (annotating Appx3165, Appx3180); Appx6921-22 (citing Appx3487-88; Appx7220-21 ¶¶ 22-23); Appx3415-16 (“center-aligned” and “edge-aligned”).

Of particular relevance here, it is undisputed that the JEDEC standard above requires the DQS strobe signal, on the DQS line, to stay aligned with the DQ data signals, on the DQ lines, within a “very tight tolerance.” Appx8981 (139:13-:24); Appx3168, Appx3273 (“tDQSQ”); Appx10255.

II. Summary of the Prior Art and '608 Patent

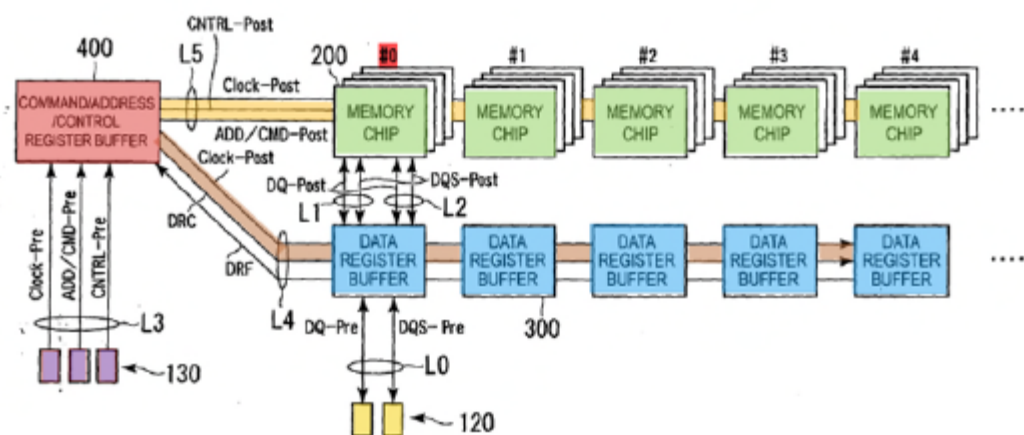
A. Hiraishi

The primary prior-art reference in this IPR was Hiraishi (U.S. Patent Publication No. 2010/0312956), which discloses a memory module with DDR3 DRAM memory devices that comply with the timing and alignment requirements of the JEDEC standard discussed above. Appx871 ¶ 163. Figure 1 below depicts a memory module 100 that includes a plurality of memory chips 200 (green), data register buffers 300 (blue) distributed underneath the memory chips 200, and command/address/control register buffer 400 (red) in the middle:



Appx149 (annotating Appx833).

Figure 7 below provides additional detail to Figure 1, and together they illustrate that Hiraishi's memory module includes a central command/address/control register buffer 400 (red) and a "fly-by" configuration of memory chips 200 (green) and data register buffers 300 (blue).



Appx149 (annotating Appx839). Figure 7 above shows the vertical "data lines" labeled L0, L1, and L2 transferring (through data connectors 120 at the bottom) both DQ data signals (on the left) and DQS strobe signals (on the right). Appx867 ¶ 103. Hiraishi explains that the data register buffer 300 (blue) causes the "timing [to be] off" between DQ-Pre/DQS-Pre (on one side of the buffer) and DQ-Post/DQS-Post (on the other side of the buffer). Appx867 ¶ 104. Thus, Hiraishi teaches that "it is required to perform a timing adjustment between the memory chips 200 and the data register buffer 300." *Id.* In particular:

Upon completing the mode register setting operation, a leveling operation between the data register buffer 300 and the memory chip 200 is performed (Step S4). The leveling operation is to adjust a

write timing or a read timing in consideration of a propagation time of a signal. The adjustment of the write timing is performed by a write leveling operation, and the adjustment of the read timing is performed by a read leveling operation.

Appx870 ¶ 140. Hiraishi's Figure 5 below illustrates a data register buffer 300 (outer blue box) in more detail and shows that it includes both a write leveling circuit 322 and a read leveling circuit 323 (upper right) to determine the timing adjustments needed for the DQ data signals (solid orange) and DQS strobe signals (dashed orange) as described above.

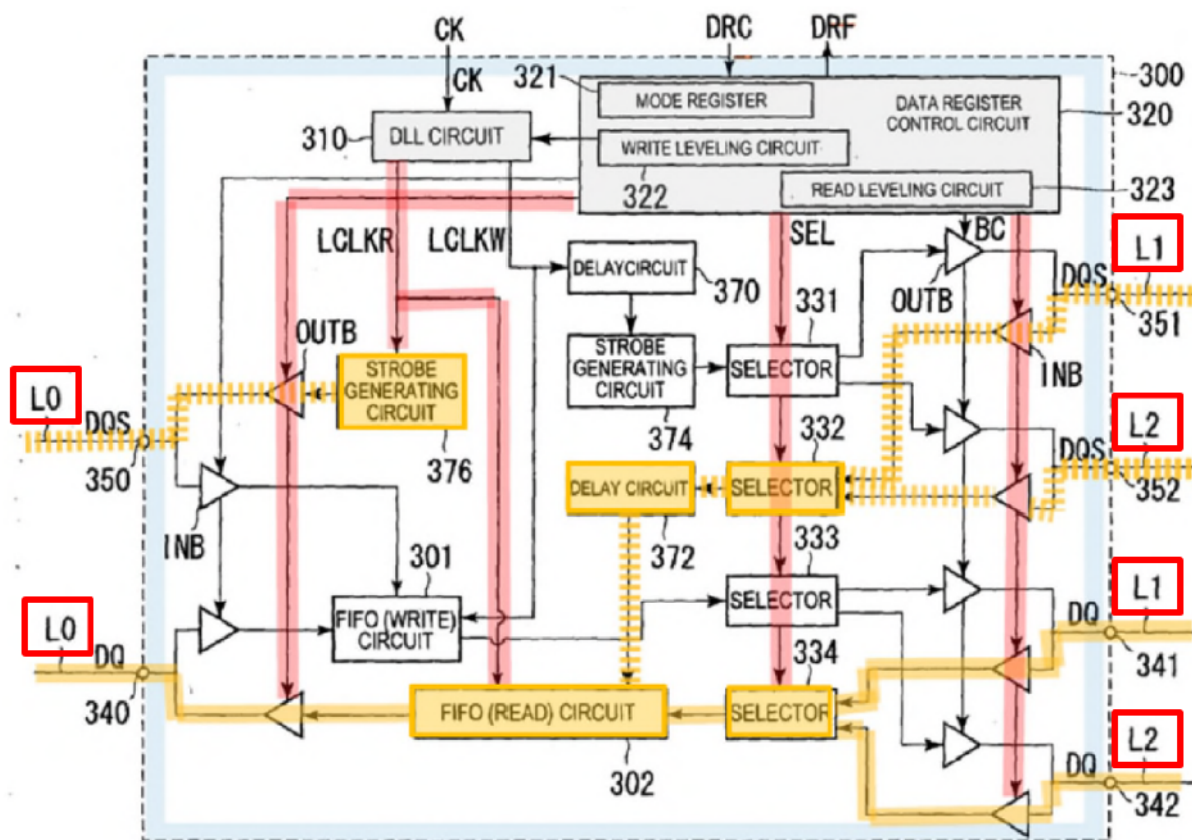


FIG.5

Appx10472 (annotating Appx837).

Hiraishi's Figures 11 and 12 below are detailed timing diagrams showing that the data register buffer 300 above delays (i.e., “performs a re-timing” of) both the DQ data signal and the DQS strobe signal so that they are both properly aligned with the CK clock signal (consistent with the JEDEC standard discussed above, pp.6-7). Appx869-70 ¶¶ 130, 135, Appx843-44; Appx10214; Appx184-93. For example, Figure 11 shows a read operation where the data register buffer (blue) is delaying (i.e., “re-timing,” Appx869 ¶ 130) both the DQ data signal and DQS strobe signal—taking into account the “Flight Time” needed for those signals to propagate from the memory chip to the data register buffer, Appx869-70 ¶¶ 129, 140—so that they are both properly aligned with the CK clock signal (yellow) at time T6:

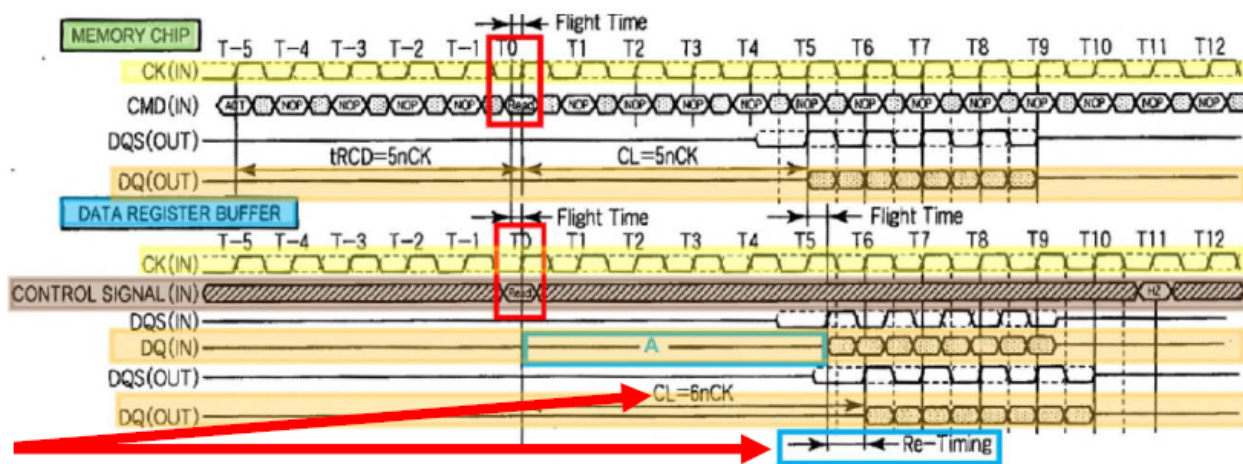


FIG. 11

Appx10214; Appx188-89 (annotating Appx843); Appx869 ¶ 130. Similarly, Figure 12 shows a write operation where the data register buffer (blue) is delaying (i.e., “re-timing,” Appx870 ¶ 135) both the DQ data signal and DQS strobe signal—taking into account the “Flight Time” needed for those signals to propagate from the data

register buffer to the memory chip, Appx870 ¶¶ 136, 140—so that they are both properly aligned with the CK clock signal (yellow) at time T5:

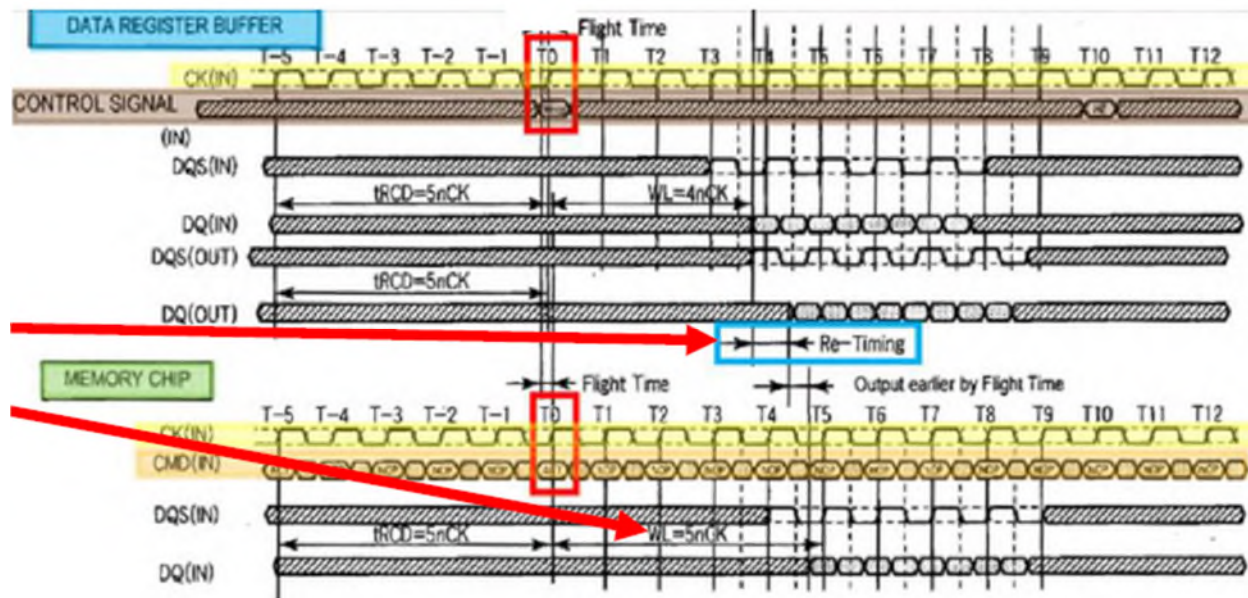
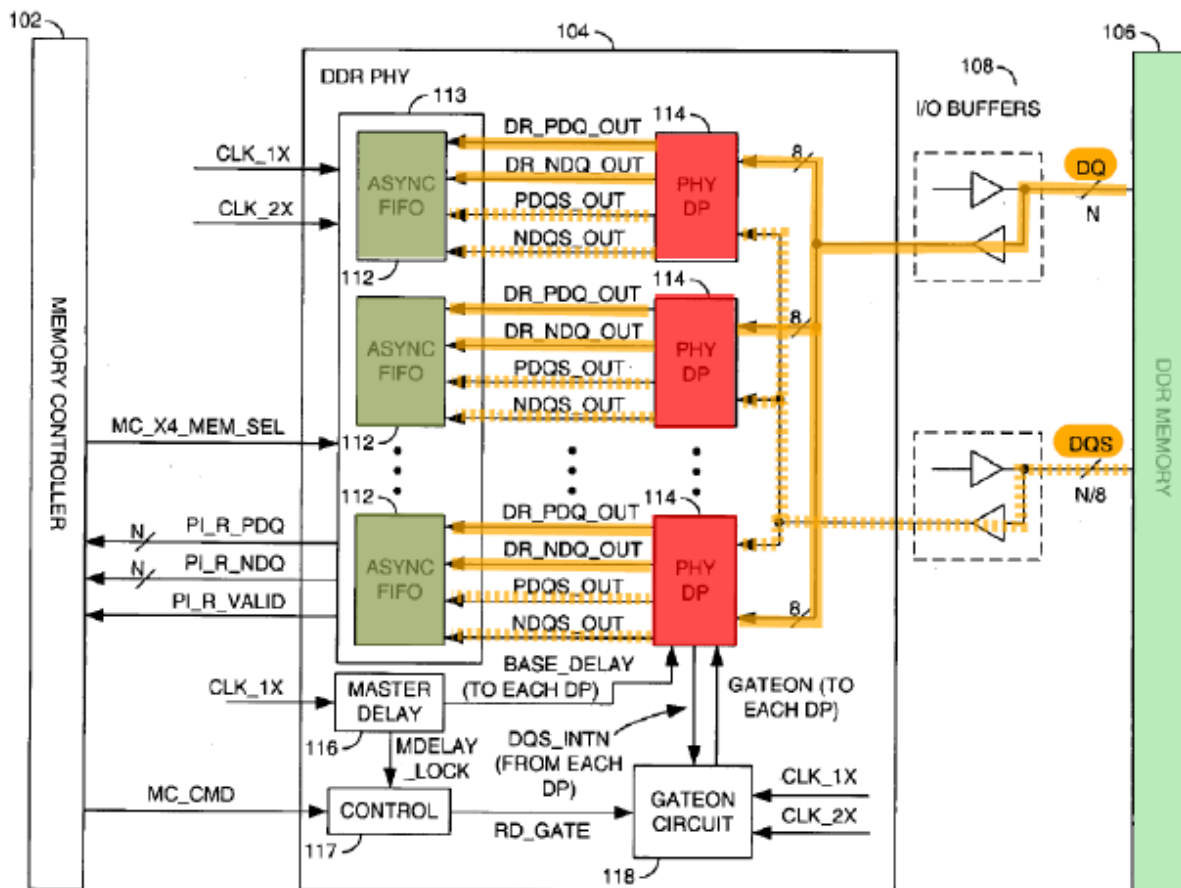


FIG.12

Appx10214; Appx186 (annotating Appx844); Appx870 ¶ 135.

B. Butt

Another prior-art reference in this IPR was Butt (U.S. Patent Publication No. 2007/0008791), which teaches “datapaths” 114 (red boxes below), each handling both DQ data signals (solid orange) and DQS strobe signals (dashed orange) for DDR memory devices 106 (green, right):

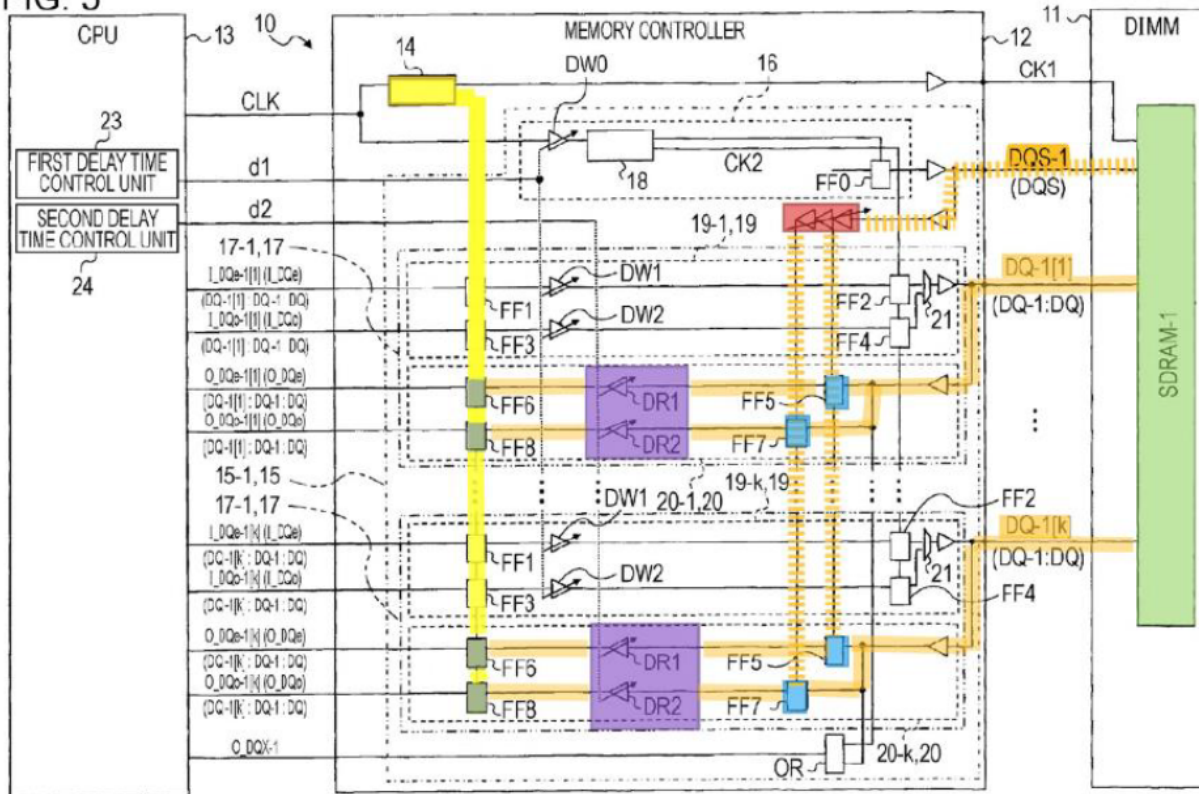
**FIG. 2**

Appx153 (annotating Appx4139); Appx4147 ¶ 17; Appx175-76; Appx10479-80; Appx671-73 ¶ 144.

C. Tokuhira

Another prior-art reference in this IPR was Tokuhira (U.S. Patent No. 8,020,022), which teaches using delay circuit DR1 (purple) to delay a DQ data signal (orange, on the right) from a DDR3 memory device (green) for proper alignment with the clock signal (yellow, on the left):

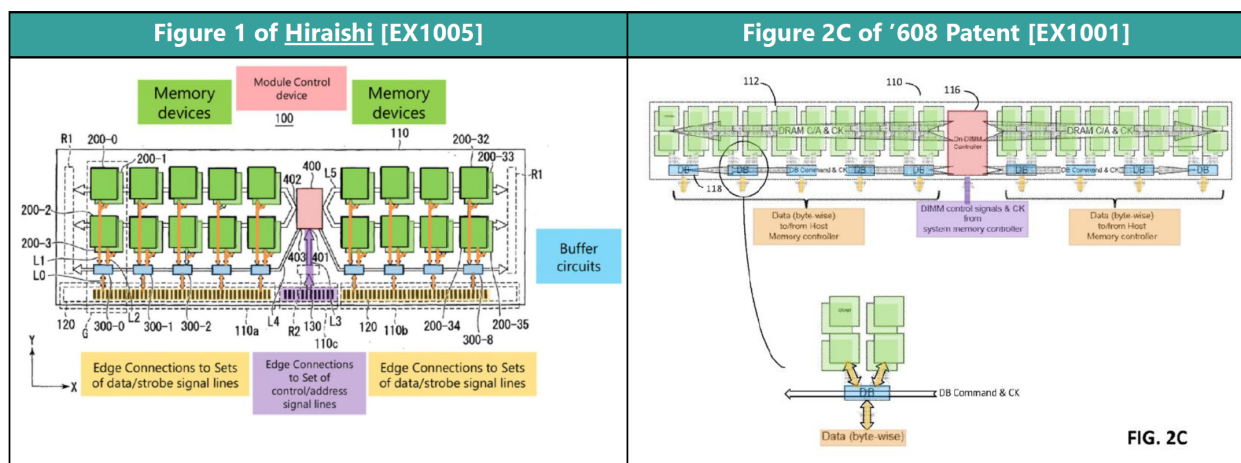
FIG. 5



Appx225-27 (annotating Appx880); Appx757-59 ¶¶ 235-36; Appx896 (1:63-2:9), Appx900-01 (10:63-11:16), Appx904-05 (18:66-19:7).

D. '608 Patent

The '608 Patent discloses a memory module (right) that is remarkably similar to the prior-art Hiraishi memory module (left):



Appx10211. Similar to Hiraishi, Figure 2C of the '608 Patent (above right and below) discloses a memory module 110 with a module control device 116 (red) located in the center of the module, and memory devices 112 (green) organized in groups, with each group having an associated data buffer 118 (blue):

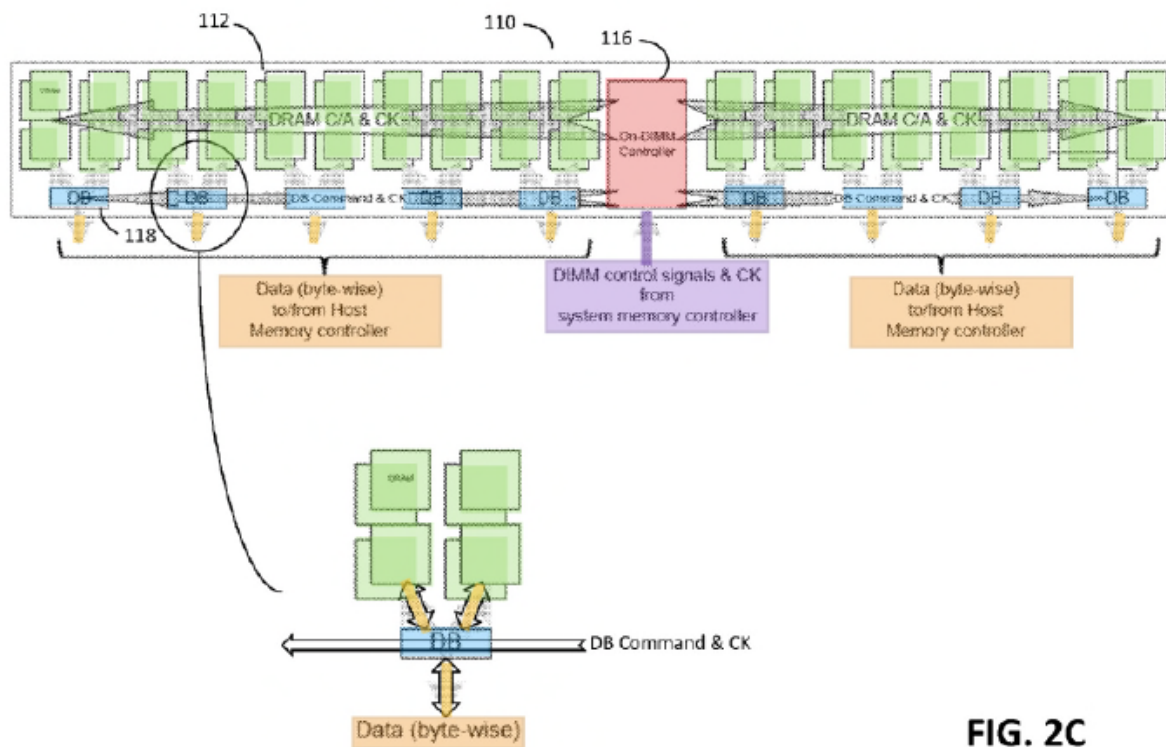
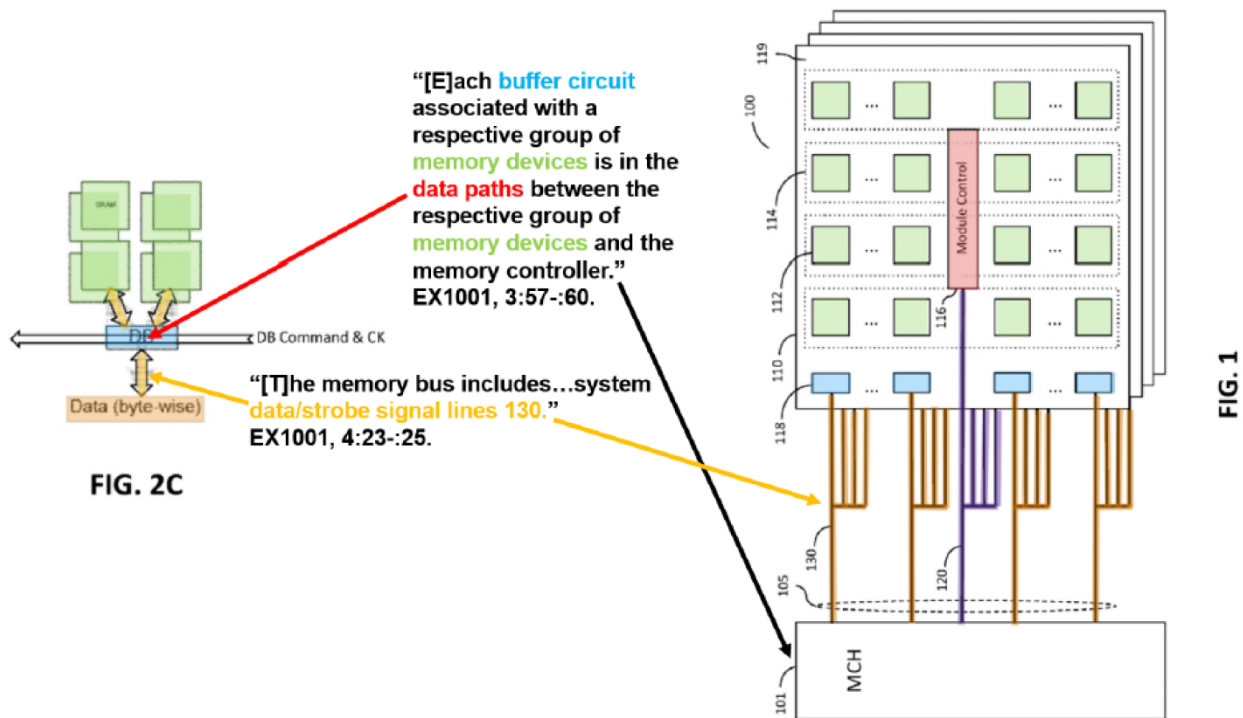


FIG. 2C

Appx143 (annotating Appx85); see also Appx109 (3:25-27, 3:51-54, 4:20-35), Appx111 (8:22-35). Figures 1 and 2C of the '608 Patent (below) disclose “data/strobe signal lines 130” (orange) going to the data buffer (blue), and teach that “each buffer circuit [blue] . . . is in the **data paths** between the respective group of memory devices [green] and the memory controller [MCH on the bottom right].” Appx109 (3:57-:60, 4:23-:25);¹ see also Appx110 (6:59-:62), Appx115 (15:17-:19) (same).



Appx10258 (annotating Appx82, Appx85).

¹ All emphasis added unless otherwise noted.

The '608 Patent does not include any detailed timing diagrams showing how the data buffers (blue) can delay the DQ data signal and DQS strobe signal to be in alignment with the CK clock signal, as required by the JEDEC standard (pp.6-7) and taught by the prior-art Hiraishi reference above (pp.11-12).

III. Related Proceedings

A. '035 IPR Proceeding

The '608 Patent is a continuation of U.S. Patent No. 9,824,035. Appx75; Appx4170. During prosecution, the claims of the '608 Patent were rejected as not patentably distinct from the claims of the '035 patent, resulting in a terminal disclaimer. Appx146; Appx340-48, Appx359-60.

Before this IPR proceeding against the '608 Patent, a third-party had filed an IPR petition against the parent '035 patent based primarily on a reference called Osanai, which Netlist concedes “is the same as Hiraishi [here] in all material respects,” Appx6099.² After the Petition was filed in this IPR proceeding against

² Hiraishi and Osanai are both U.S. Patent Publications that have the same inventors, the same publication dates, and the same disclosures. Appx832-74; Appx6214-57. The only difference between Hiraishi and Osanai (other than the claims at the end) is in the “Summary.” Compare Appx862 ¶¶ 10-11, with Appx6244 ¶¶ 9-18. Also, Hiraishi uses two separate paragraph numbers for Figures 9A and 9B, while Osanai uses just one. Compare Appx863 ¶¶ 21-22, with Appx6245 ¶ 28. The figures and “Detailed Description of the Embodiments” are the same in both references, with the paragraph numbering in Hiraishi six numbers behind Osanai. Compare, e.g., Appx870 ¶ 140 (“Upon completing the mode register setting . . .”), with Appx6252 ¶ 146 (same).

the '608 Patent, the Board issued a Final Written Decision (Appx6702-65) finding several claims of the '035 patent obvious in light of Osanai/Hiraishi and Tokuhito, which is similar to the Ground 2 combination in this IPR. See Appx141; Appx10303. Netlist did not appeal the Board's Final Written Decision with respect to the '035 Patent, so the Patent Office cancelled the claims determined to be unpatentable. Appx9750 (cancelling claims 1, 10-13, 21-22).

The Board's Final Written Decision against the '035 patent includes several factual findings about the prior art that are relevant to this appeal. Appx6719-44. For example, the Board determined that Osanai/Hiraishi's data buffer "includes ***data paths*** for transmitting ***data and strobe*** signals," and the "disclosures of Osanai[/Hiraishi] are sufficient to teach controlling the timing of the ***data and strobe*** signals on the ***data paths*** on which those signals travel." Appx6736, Appx6737 (citing Osanai, Appx6252 ¶ 146, which is the same as Hiraishi, Appx870 ¶ 140). The Board specifically identified the "data paths" it was referring to as the "data paths [that] connect lines L0 to lines L1 and L2 through the circuitry of data register buffer 300" in Osanai/Hiraishi, Appx6736, which Samsung has identified with orange lines below (for the read direction):

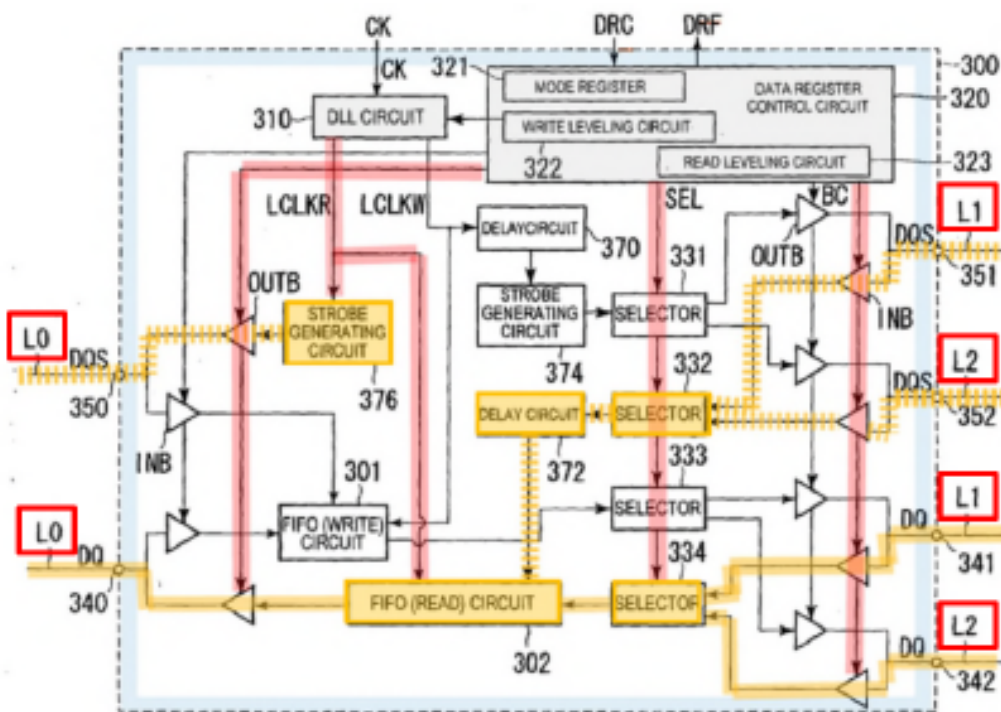
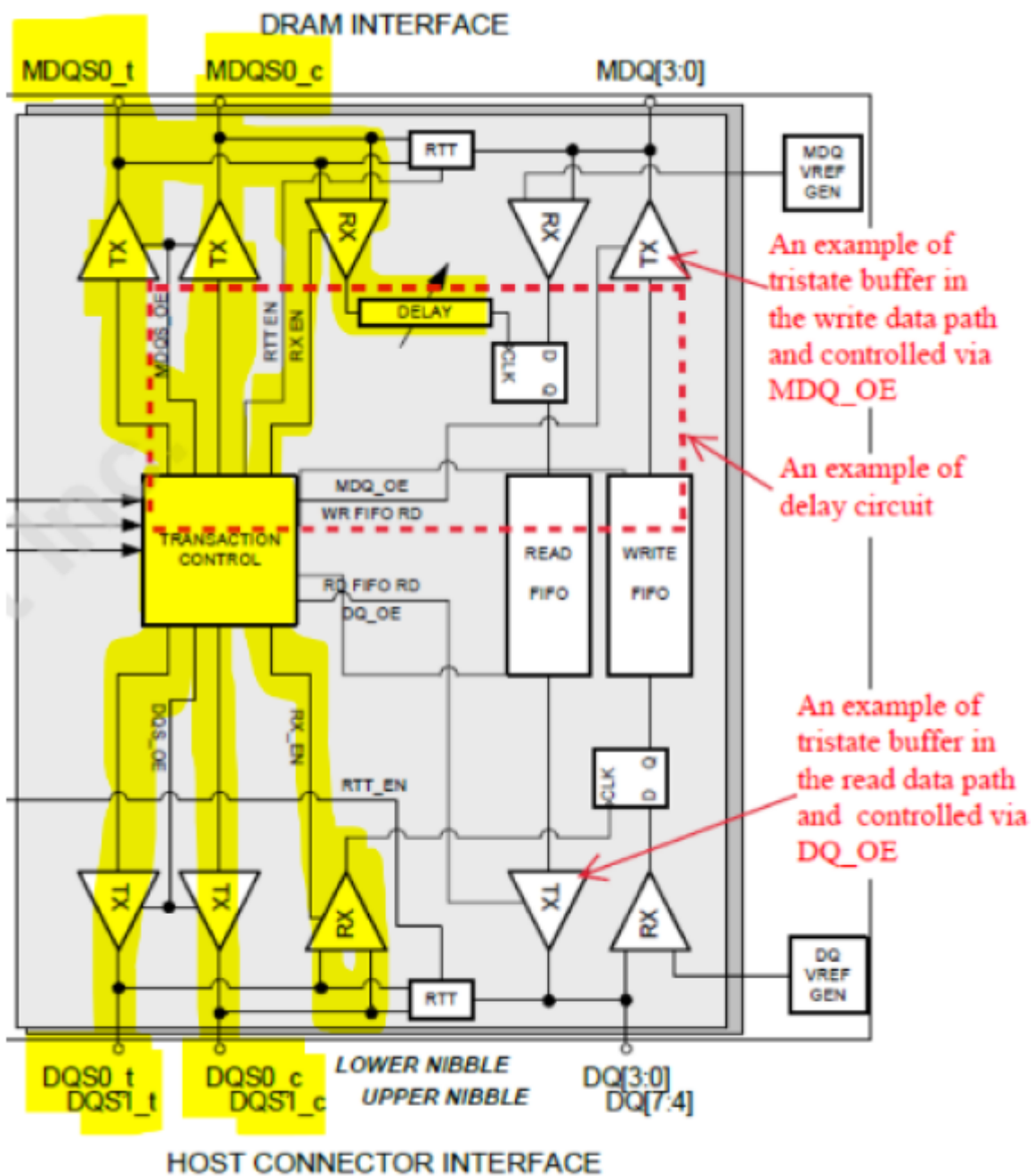


FIG.5

Appx10472 (annotating Hiraishi, Appx837, which is the same as Osanai, Appx6219).

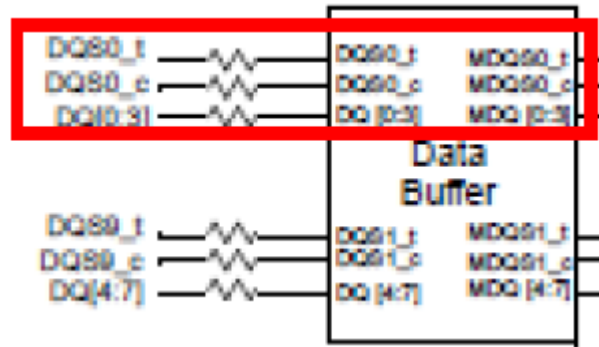
B. Netlist’s Complaint against Samsung

Before Samsung filed the petition in this IPR proceeding, Netlist filed a complaint against Samsung in district court asserting the '608 Patent. In that complaint, Netlist specifically identified the ***DQS strobe*** signals (highlighted by Samsung in yellow below) as being included in the “*delay circuit*” in the “*data path*” (indicated by Netlist with a dashed red box):



Appx9906 (annotating Appx5759-60); Appx10225, Appx10252-53. In particular, Netlist wrote, “As shown above and below, the **data path** corresponding to the each data signal line also **includes a delay circuit** configured to delay a signal through the

data path” Appx5760 ¶ 74. To further specify the “*data path*,” Netlist put a red box around **both** the **DQS *strobe*** signal **and** the DQ data signal:



Id.

IV. This IPR Proceeding

A. The Positions of the Parties

In this proceeding, Samsung filed an IPR petition against the '608 Patent that asserted five grounds against claims 1-12. Appx141. Netlist quickly disclaimed claims 6-12, *see* Appx6126, leaving three grounds in the IPR: (1) claims 1-5 would have been obvious over Hiraishi and Butt; (2) claims 1-5 would have been obvious over Ground 1 and Tokuhiro; and (3) claim 5 would have been obvious over either Ground 1 or 2 combined with Ellsberry. Appx141; Appx8.

Ground 1 identified the combination of Hiraishi and Butt as disclosing that each buffer circuit includes a “*data path corresponding to each data signal line in the respective set of data/strobe signal lines.*” Appx173-77. Consistent with the IPR against the '035 patent as well as Netlist’s complaint against Samsung, both discussed above (pp.17-21), Samsung explained that Hiraishi’s Figure 5 depicted

data paths for read operations (first figure below) and write operations (second figure below) that included both DQ data signals (solid orange) and DQS strobe signals (dashed orange):

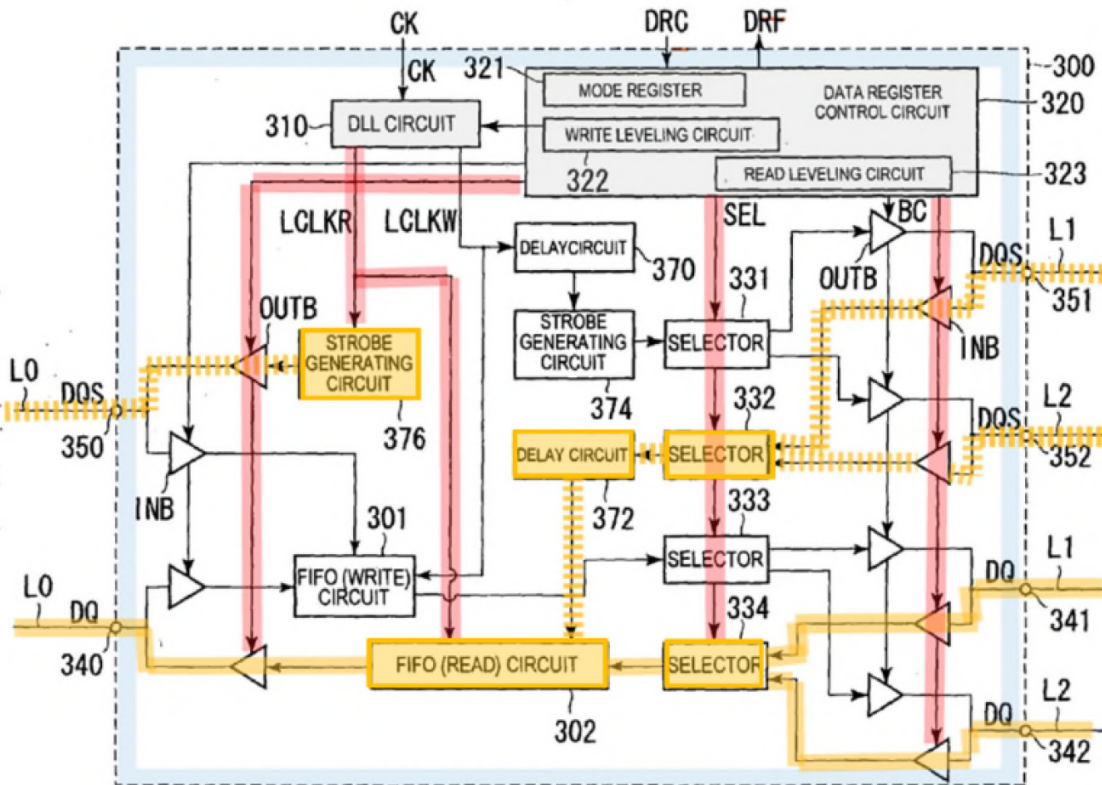


FIG.5

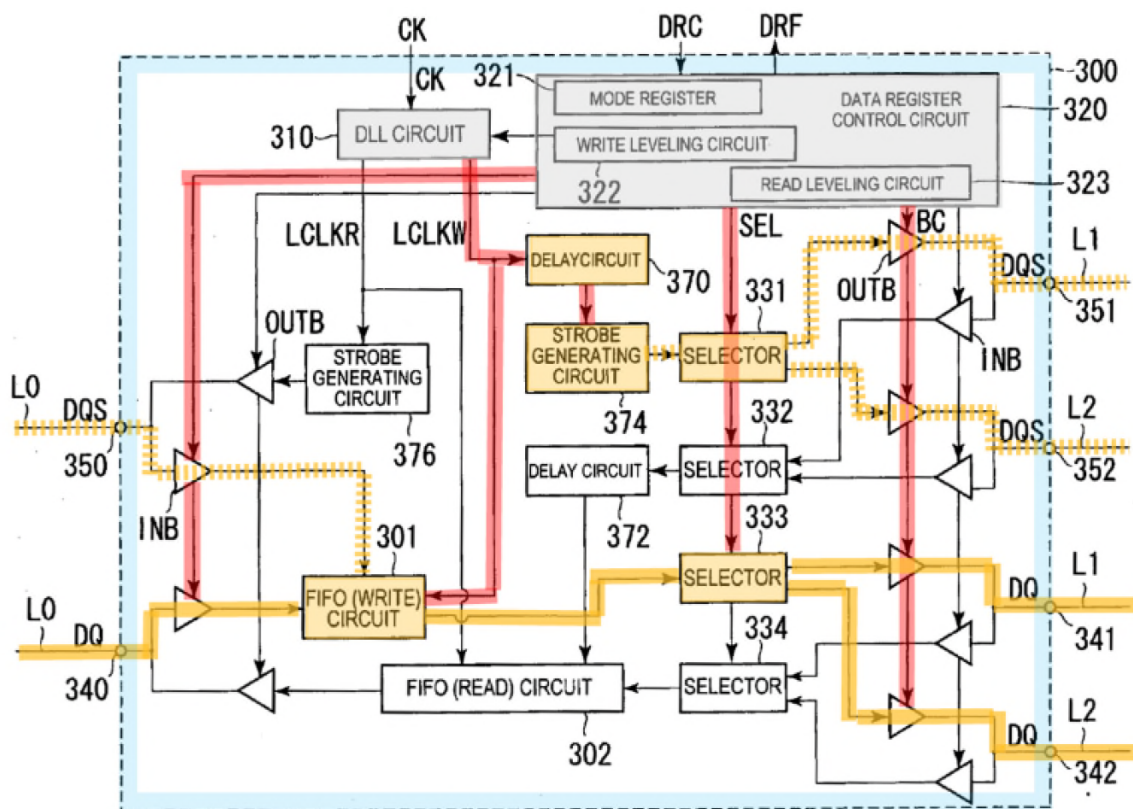


FIG. 5

Appx173-74 (annotating Appx837); Appx10485 (citing Appx5759).

Samsung's Petition also identified a "data path" (114 below) in Butt's Figures 2 and 3A that included both DQ data signals (solid orange) and DQS strobe signals (dashed orange):

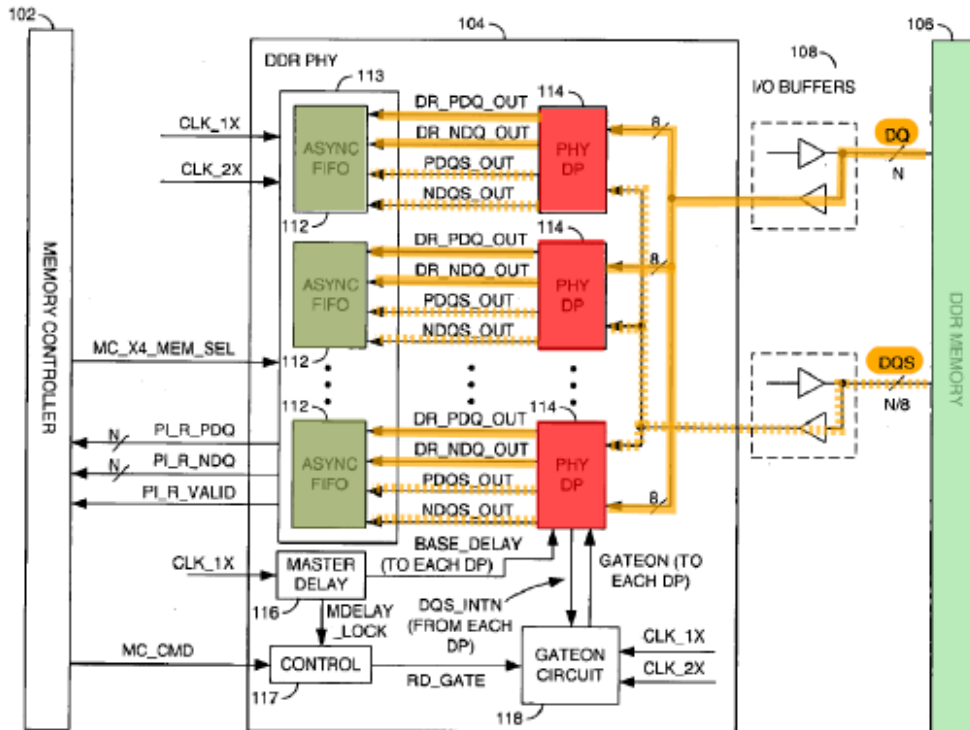


FIG. 2

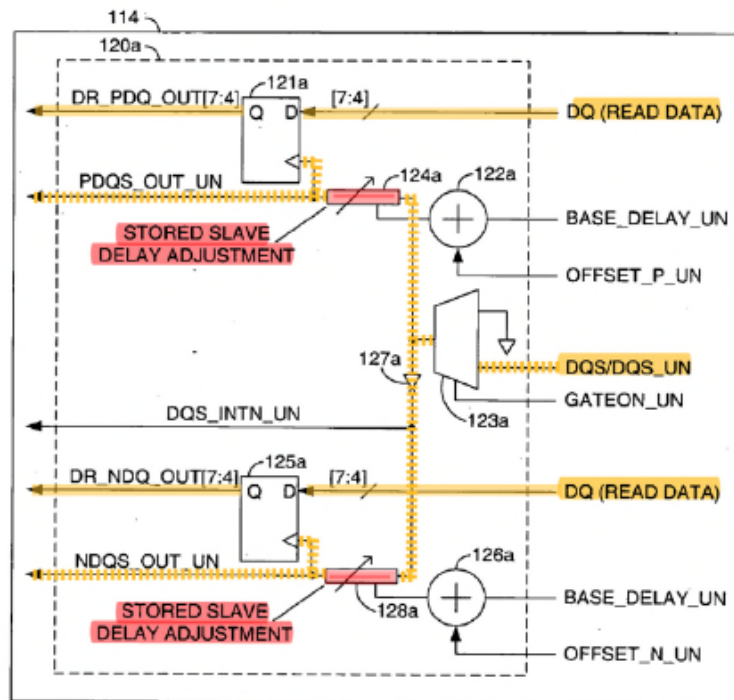
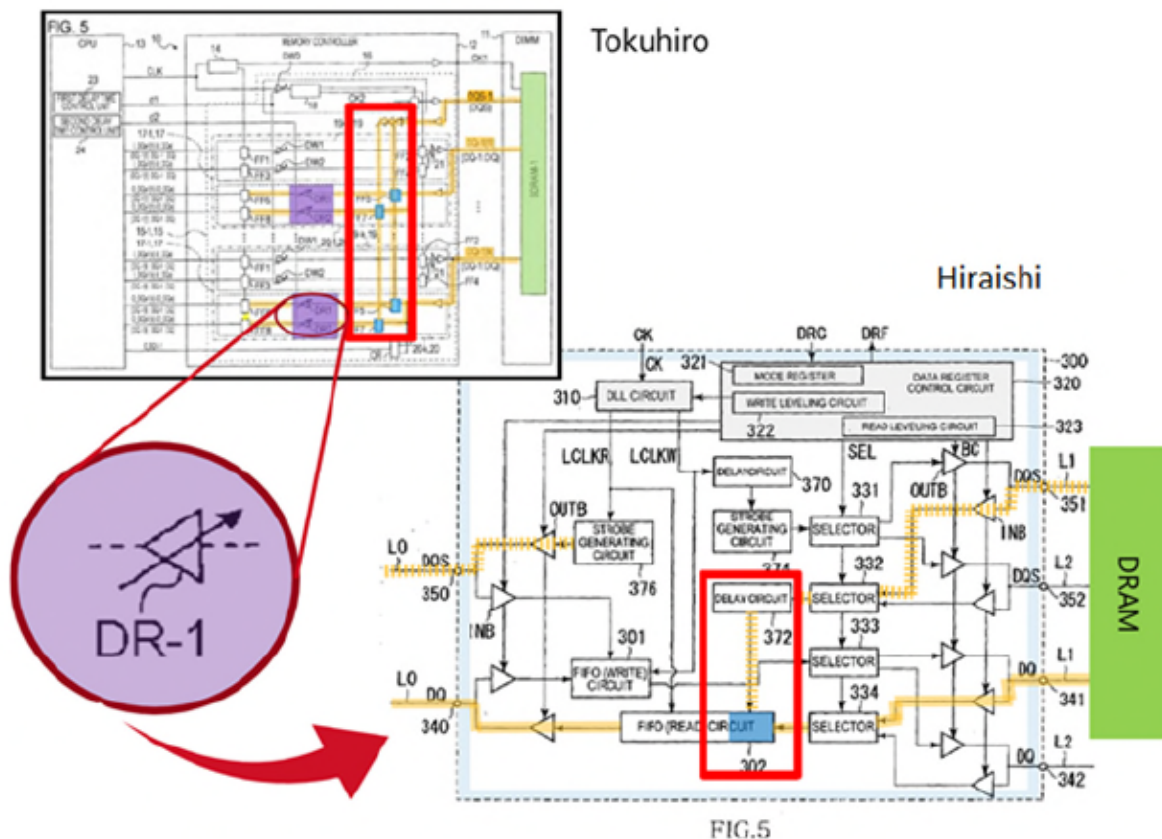


FIG. 3A

Appx175-76 (annotating Appx4139, Appx4140).

For Ground 2, the Petition explained that Tokuhiro teaches that delay circuit DR1 (purple below) is “a delay circuit configured to delay a signal through the data path” that could be implemented in Figure 5 of Hiraishi to delay “both data and strobe signals”:



Appx229-30, Appx239-41. The Petition also identified an alternative combination where “delay elements similar to Tokuhiro’s DR elements can be used instead of (or

in addition to) Hiraishi's FIFO^[3] circuit for delaying the read data." Appx229-30; Appx782-85 ¶ 262.

In its Patent Owner Response, Netlist argued for the first time that the term "*data path*" should be limited to the DQ data line and thus should exclude the DQS strobe signal and any delay circuitry for the DQS strobe signal (contrary to Netlist's complaint against Samsung discussed above, pp.19-21). See Appx6934-41; Appx6843 (Board concluding that Netlist "[did] not present any proposed claim constructions" in its preliminary response); Appx10434 (47:24-:25) (Netlist admitting it did not present "a fully fleshed out claim construction position" in its preliminary response).

Samsung's Reply asserted that Netlist's arguments were precluded by the recent Final Written Decision against the parent '035 patent. Appx10470-71, Appx10482, Appx10486, Appx10501-03, Appx10506-07. Samsung's Reply also disagreed with Netlist's narrow claim construction for "*data path*" and explained that the '608 Patent uses the term "*data path*" consistent with its plain and ordinary meaning, which is "the course or direction in which a . . . thing is moving." Appx10470-81 (quoting Appx9748). Samsung's Reply also addressed why Grounds 1-3 invalidated the claims even under Netlist's narrow construction for "*data path*" limited to the DQ data line. Appx10481-85, Appx10489-502. Samsung

³ "FIFO stands for first in, first out." Appx9041 (199:2-:4).

explained that the “*data path*” includes the DQ data signals (solid orange in the first figure below) that are delayed by the FIFO 302 in Figure 5 of Hiraishi. Appx10482-84. That directly corresponds to the preferred embodiment shown in Figure 16 of the '608 Patent (second figure below):

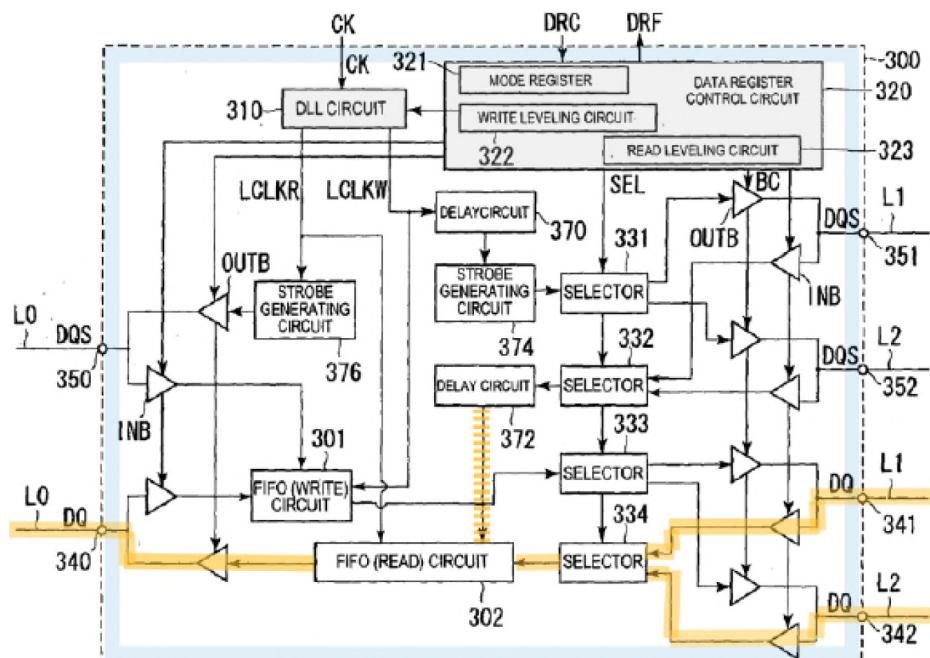


FIG.5

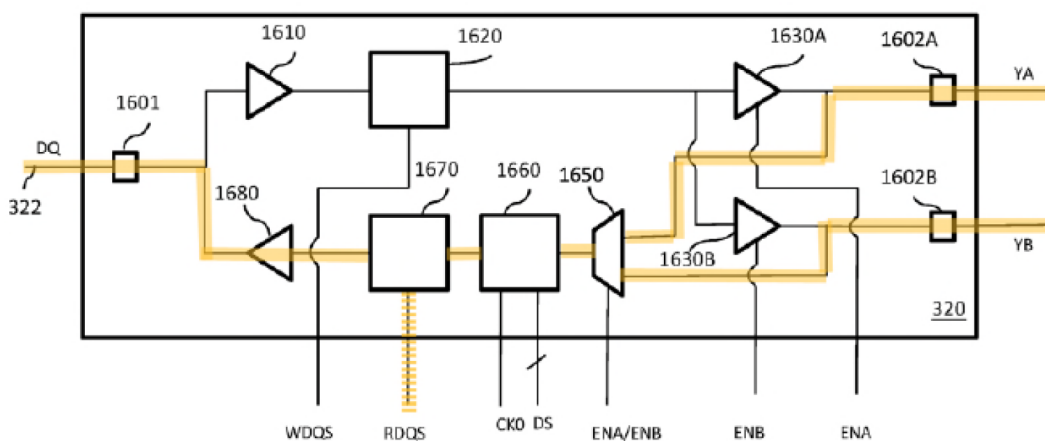


FIG. 16

Appx10482-84 (annotating Appx837 and Appx104).

For Ground 2, Samsung explained that its alternative combination with Tokuhito satisfied even Netlist’s narrow construction for “*data path*.” Appx10501-02. In that alternative combination, Hiraishi’s FIFO 302 on the DQ data line is replaced by “delay elements similar to Tokuhito’s DR elements,” consistent with the combination used to invalidate the claims of the parent ’035 patent. Appx10502 (citing Appx230; Appx6740-41 (’035 Final Written Decision); Appx9006 (164:14-:18)).

B. The Board’s Final Written Decision

In its Final Written Decision, the Board agreed with Netlist’s narrow claim construction for “*data path*” and based on that narrow claim construction concluded that claims 1-5 had not been shown to be unpatentable. Appx10-70. The Board provided 15 pages of analysis under the heading “Claim Interpretation,” Appx10-24, in which the Board concluded that the claimed “data path . . . is in the data signal line” and “therefore, is not in a strobe signal line.” Appx17.

Specifically, the Board concluded that neither Hiraishi nor Butt in Ground 1 disclosed the claimed “*data path*” because the Petition included lines that carry strobe signals—and circuitry to delay those strobe signals—in the alleged “*data path*.” Appx37-43. However, given that Netlist raised its narrow construction for “*data path*” after the Institution Decision, the Board also considered Samsung’s

argument in Reply that Hiraishi's FIFO on the DQ data line satisfied even Netlist's narrow claim construction for "*data path*." Appx43-46. But the Board disagreed with Samsung's argument in Reply. Appx47-68.

With respect to collateral estoppel, the Board focused on whether "the Board's statement in the [previous] -00236 IPR acts to preclude the interpretation here of the term 'data path' of claim 1 of the '608 patent." Appx19-20. The Board then relied on alleged differences in claim language and unpatentability theories to conclude that estoppel should not apply. Appx20-24. However, the Board did not address whether Netlist's factual arguments about Hiraishi were precluded by the Board's contrary factual findings in that previous IPR.

For Ground 2, the Board addressed only Samsung's first combination where Tokuhiko's delay circuit DR1 is added to Hiraishi's strobe generating circuit 376 to teach the claimed "*delay circuit*" in the "*data path*." Appx68-70. The Board rejected Samsung's argument, again based on the narrow construction for "*data path*" that excluded "strobe signal lines that carry strobe signals." Appx69-70. The Board did not address Samsung's alternative combination for Ground 2 where delay elements similar to Tokuhiko's delay circuit DR1 are used instead of Hiraishi's FIFO circuit on the DQ data line, which would satisfy even Netlist's narrow construction for "*data path*." Appx229-30; Appx10501-02 ("Netlist completely ignores the alternative combination for Ground 2 . . .").

SUMMARY OF ARGUMENT

The Board incorrectly interpreted claim language describing “*a data path corresponding to each data signal line in the respective set of data/strobe signal lines*” as requiring that the recited “*data path*” must be “***in*** the data signal line” and “***not in*** a strobe signal line,” contrary to the ordinary meaning of “corresponding to.” By imposing that requirement, the Board excluded all “*strobe signal[s]*” from the “*data path*,” despite (i) claim 1 expressly requiring “*a delay circuit configured to delay a signal through the data path*,” which dependent claim 10 shows can be “*a strobe signal*,” and (ii) the undisputed fact that strobe signals have a close functional relationship with data signals under the JEDEC standard. The Board erred by adopting a construction contrary to the ordinary meaning of “corresponding to” as “having a functional relationship with.” Applying the ordinary meaning of “corresponding to” results in a claim construction that fits with the dependent claims as well as with the understanding of persons of ordinary skill in the art about the close functional relationship between strobe signals and data signals.

The Board expressly relied on its claim interpretation as the sole reason for rejecting Ground 2 and as the primary reason for rejecting Ground 1. Given the importance of that interpretation, vacatur and remand to reconsider the petition’s grounds for unpatentability in view of the proper construction is appropriate.

The Board also erred by failing to apply its previous factual findings against Netlist about materially identical prior art in an unappealed decision regarding the parent '035 patent. Under both caselaw and the Restatement (Second) of Judgments § 27, “an issue of fact” is preclusive regardless of whether legal conclusions in the same decision are also preclusive. The Board focused on alleged differences between the '608 Patent claims and '035 patent claims—an analysis that would need to be revisited if the interpretation of the '608 Patent is corrected. However, the teachings of the prior-art Hiraishi reference is an independent factual issue that does not depend on claim language or unpatentability theories. The Board erred when it linked those issues and refused to consider factual preclusion based on its conclusion regarding legal preclusion. The Board’s contrary factual findings should be vacated, both because the Board failed to properly consider preclusion and because those findings contradict key disclosures in Hiraishi and the JEDEC industry standard adopted as part of the ordinary skill in the art.

Independent of the improper claim interpretation and factual findings contrary to the Board’s previous decision, the Board failed to follow the APA when it ignored an obviousness theory put forward by Samsung for Ground 2 in its petition, expert declaration, reply, and at argument. Throughout the IPR, Samsung argued that a person of ordinary skill would be motivated to replace Hiraishi’s FIFO circuit with a delay element physically on the data signal line as a suitable configuration for

reducing the risk of misaligned signals in a high-speed memory circuit. Given the Board’s restrictive claim interpretation, that obviousness argument was particularly important because it satisfied the Board’s narrow construction of “*corresponding to each data signal line*” as meaning “in the data signal line.” However, the Board simply did not address this obviousness theory, despite Samsung asserting it at every stage and Netlist failing to rebut it. At minimum, the Board’s decision should be vacated and remanded to consider Samsung’ argument.

ARGUMENT

I. Standard of Review

Claim construction is a question of law reviewed de novo, based on underlying facts. *Teva Pharms. USA, Inc. v. Sandoz, Inc.*, 574 U.S. 318, 321-22 (2015).

This Court reviews the Board’s legal conclusions de novo and factual findings for substantial evidence. *Almirall, LLC v. Amneal Pharms. LLC*, 28 F.4th 265, 271-72 (Fed. Cir. 2022). Substantial evidence means “such relevant evidence as a reasonable mind might accept as adequate to support a conclusion.” *In re Gartside*, 203 F.3d 1305, 1312 (Fed. Cir. 2000) (quoting *Consol. Edison Co. v. NLRB*, 305 U.S. 197, 229-30 (1938)).

“Whether a claimed invention is unpatentable as obvious under § 103 is a question of law based on underlying findings of fact.” *In re Gartside*, 203 F.3d at

1316. Those underlying facts include the “scope and content of the prior art, differences between the prior art and the claims at issue, the level of ordinary skill in the pertinent art, and any objective indicia of non-obviousness.” *Randall Mfg. v. Rea*, 733 F.3d 1355, 1362 (Fed. Cir. 2013) (citing *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007); *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966)). A finding as to the scope and content of the prior art is reviewed for substantial evidence, which considers whether “the Board reasonably found that a skilled artisan would have understood that [disclosure].” *Genentech, Inc. v. Hospira, Inc.*, 946 F.3d 1333, 1340 (Fed. Cir. 2020).

II. The Board Wrongly Construed “Data Path” as Limited to the Data Signal Line, Excluding, Inter Alia, Corresponding Strobe Signals and Delay Circuitry

The Board improperly construed claim 1’s limitation of “*a data path corresponding to each data signal line in the respective set of data/strobe signal lines . . . , wherein the data path . . . includes . . . a delay circuit configured to delay a signal through the data path*” to require a “data path that is *in*” the data signal line, thereby excluding all other signals, such as “*strobe signal[s]*” in dependent claim 10 that correspond to the data signals and travel alongside the data signal lines. Appx16-17.

A. The Board Construed “A Data Path Corresponding to Each Data Signal Line in the Respective Set of Data/Strobe Signal Lines”

Although the Board stated that it was “not performing claim construction of a specific claim term or phrase *per se*,” Appx16, this Court has recognized that such language “is not dispositive as to whether claim construction occurred,” *Google LLC v. EcoFactor, Inc.*, 92 F.4th 1049, 1056 (Fed. Cir. 2024). What matters is whether the Board’s “assessment established the scope of the . . . limitation.” *Id.* Here, the Board construed the term “*data path*” in response to Netlist’s express arguments for a construction of “data path.” See Appx6934-41 (“The Recited ‘Data Path’ Does Not Include Strobe Signal Lines”); Appx10351-59 (“Claim Construction: Claim 1’s ‘data path’ does not include strobe signal lines”).

It is black letter law that the “interpretation” of a claim is claim construction. *Markman v. Westview Instruments, Inc.*, 517 U.S. 370, 372 (1996) (“The question here is whether the interpretation of a so-called patent claim . . . is a matter of law We hold that the construction of a patent, including terms of art within its claim, is exclusively within the province of the court.”). The Board itself conceded that it considered the “***interpretation*** of the language of limitation 1[e], together with the limitation 1[f].” Appx16; see also Appx18 (“[T]here is support in the Specification for the ***interpretation*** of the language of claim 1 that the data path as recited in claim 1 is in the data signal lines, that are separate from the strobe line”).

The Board established the scope of “*data path*” when it stated: “Limitation 1[e] identifies that ‘a data path’ corresponds to the data signal line in the set of data/strobe signal lines; **that is**, it is a data path that **is in** the data signal line.” Appx17. The Court has recognized that the use of the term “that is” “signals an intent to define the word to which it refers.” *TF3 Ltd. v. Tre Milano, LLC*, 894 F.3d 1366, 1372 (Fed. Cir. 2018) (quoting *Edwards Lifesciences LLC v. Cook Inc.*, 582 F.3d 1322, 1334 (Fed. Cir. 2009)). Furthermore, through its definition the Board narrowed the meaning of “*a data path corresponding to*,” as recited in 1[e], by equating “*corresponding to*” with “that is in.” *Cf. Restem, LLC v. Jadi Cell, LLC*, No. 23-2054, ___ F.4th ___, 2025 WL 679195, at *2 (Fed. Cir. Mar. 4, 2025) (“The Board **implicitly** construed ‘isolated cell’ as a ‘cell population’” (citation omitted)). From there, the Board established the “scope” of the limitation “*data path*” when it concluded—based on its “interpretation” of the term—that a “*data path*” cannot be “in a strobe signal line of the set of data/strobe signal lines.” Appx17. Thus, the Board construed “*data path*.”

B. The Board’s Construction Conflicts with the Plain and Ordinary Meaning of the Claim’s Full Language

Claim limitation 1[e]’s own language and its interaction with other claim limitations indicates the error in the Board’s construction. Limitation 1[e] states that a “*data path correspond[s] to each data signal line in the respective set of data/strobe signal lines.*” Appx117 (19:44-:45). The Board, in contrast, required

the data path to be “in” the data signal line, thus equating “*correspond[s] to*” with “is in” or “is located in,” and the Board also further barred the “*data path*” from carrying signals from the corresponding strobe signal lines. Appx17. The Board’s narrow reading contradicts the plain and ordinary meaning of “corresponds to,” which is broader than “equal to” and encompasses two things that are “functionally related to one another.” *Respironics, Inc. v. Invacare Corp*, 303 F. App’x 865, 880-81 (Fed. Cir. 2008) (relying on plain and ordinary meaning of “corresponds to” as “similar, comparable, and/or matching”). As in *Respironics*, it does not make sense to equate a “*data path*” with a “*data signal line*” where they only share a functional relationship. See *id.* (“It would make no sense, then, to say that a flow rate or volume is ‘equal to’ a signal Two such things cannot be equal to one another. Rather, it is more proper to say that the two are functionally related to one another[.]”). “Indeed the claim does not use language of equation but of correspondence, a much broader concept.” *Broadcom Corp. v. Emulex Corp.*, 732 F.3d 1325, 1333 (Fed. Cir. 2013); Appx10407-09 (20:25-22:22); Appx10258 (claims just require a broad “correspond[ence]”); Appx10474.

Under a proper reading of “*corresponding to*” in limitation 1[e], the “*data path*” is not “in” the data signal line. Rather, the “*data path*” merely needs to have a relationship with each of the data signal lines in the respective set of data/strobe signal lines, and thus the claimed “*data path*” is not limited to carrying just signals

from the data signal lines. Indeed, there is no support for excluding other signals “functionally related to” the data signals, such as the corresponding strobe signals. Both parties acknowledge that the strobe signals are essential to the transmission of data signals, which is why both signals maintain “a very tight tolerance” with each other. Appx8981 (139:13-24); Appx6920 (“strobe signal . . . ensure[s] accurate timing for driving and sampling/capturing . . . data”). Because the strobe signals are functionally related to the data signals, the Board was incorrect to bar the strobe signals from travelling through the “*data path*.” See *Luminara Worldwide, LLC v. Liown Elecs. Co.*, 814 F.3d 1343, 1353 (Fed. Cir. 2016) (“Absent lexicography or disavowal, we do not depart from the plain meaning of the claims.”).

Limitation 1[e] as a whole confirms that the “*data path*” and “*data signal lines*” are related, but still different. Each “*buffer circuit include[es] a data path*,” and, further, the “*buffer circuit*” (and its “*data path*”) must be separate from the “*data signal lines*” because it is “*coupled **between***” the “*respective set of data/strobe signal lines*” and the “*respective set of memory devices*.” This is very similar to the claim in *Indacon, Inc. v. Facebook, Inc.*, 824 F.3d 1352 (Fed. Cir. 2016) which included “a link to be established **between** the at least one alias term and the any of the plurality of files” for which the Court concluded that “[a]s such, a link can be established to connect an ‘alias’ or other link term to files in the database, but *the*

alias is not itself the link.” *Id.* at 1354, 1356. In claim 1 here, the buffer circuit, including its “*data path*,” is not itself the “*data signal lines*.”

Limitation 1[f] further confirms this understanding. “Proper claim construction . . . demands interpretation of the entire claim in context, not a single element in isolation.” *Hockerson-Halberstadt, Inc. v. Converse Inc.*, 183 F.3d 1369, 1374 (Fed. Cir. 1999). Limitation 1[f] recites “*the data path **corresponding** to the each data signal line **includes** at least one tristate buffer . . . and a delay circuit configured to delay **a signal** through the data path . . .*” Appx117 (19:49-55). The broad “*corresponding to*” language is repeated, and the data path allows “**a signal**”—not just a **data** signal—to traverse it (and be delayed while traversing it). Given the detail of “*data*” and “*strobe*” used in the claim’s earlier recitation of “*sets of data/strobe signal lines*,” limitation 1[f]’s use of “*a signal*” suggests to one of ordinary skill in the art that the “*data path*” is broad enough to have different types of signals traversing “*through*” it, including data signals **and** strobe signals.

The claim language “*corresponding to **each** data signal line*” does not exclude the strobe signal, but instead broadens the claimed “*data path*” to encompass **multiple** data signals through the buffer (in addition to the strobe signal): the buffer has “*a data path [(singular) which] correspond[s] to **each** data signal line in the respective set of data/strobe signal lines*,” and not just to **one** of those data signal lines as the Board erroneously held. Normally there will be **multiple** data signal

lines in the “set of data/strobe signal lines,” as confirmed by dependent claim 11 requiring a “data width of 1 byte.” Appx117 (20:58-61); *see also* Appx112 (10:31-33) (“signal lines 130 [in Figure 3] include a set of *n* data (DQ) signal lines [plural] 322 . . . and at least one strobe (DQS) signal line [singular] 324”). Both parties acknowledge that the strobe signal is essential to the transmission of the data signals, which is why both signals travel together within “a very tight tolerance.” Appx8981 (139:13-24); Appx6920. The “data path” is broad enough to include all data and strobe signals from “the respective set of data/strobe signal lines.” The Board therefore was incorrect to bar the strobe signals from travelling through the “data path.”

Limitation 1[f]’s inclusion of “a delay circuit” as part of the “data path” also conflicts with the Board’s construction equating the “data path” with nothing more than the “data signal line.” As the Court explained in *Apex Inc. v. Raritan Computer, Inc.*, 325 F.3d 1364, 1373 (Fed. Cir. 2003), “the term ‘circuit’ with an appropriate identifier such as ‘interface,’ ‘programming’ and ‘logic,’ certainly identifies some structural meaning to one of ordinary skill in the art.” The Board got it backwards by construing the “data path” to be in the “data signal line” when the claim actually says an entire “delay circuit” is included in the “data path” (without any mention of the “data path” being “in” the “data signal line”). The claim also says there is “at least one tristate buffer” included in the “data path.” Once freed from the Board’s

restrictive interpretation, the claim’s use of the general term “*data path*” can naturally carry both data and strobe signals—and can include the “*delay circuit*” and “*tristate buffer*” for those signals as the claim expressly requires. *See Lexion Med., LLC. v. Northgate Techs., Inc.*, 641 F.3d 1352, 1356 (Fed. Cir. 2011) (“This court prefers a claim interpretation that harmonizes the various elements of the claim to define a workable invention.”).

C. The Board’s Construction Ignores the Level of Ordinary Skill That It Adopted

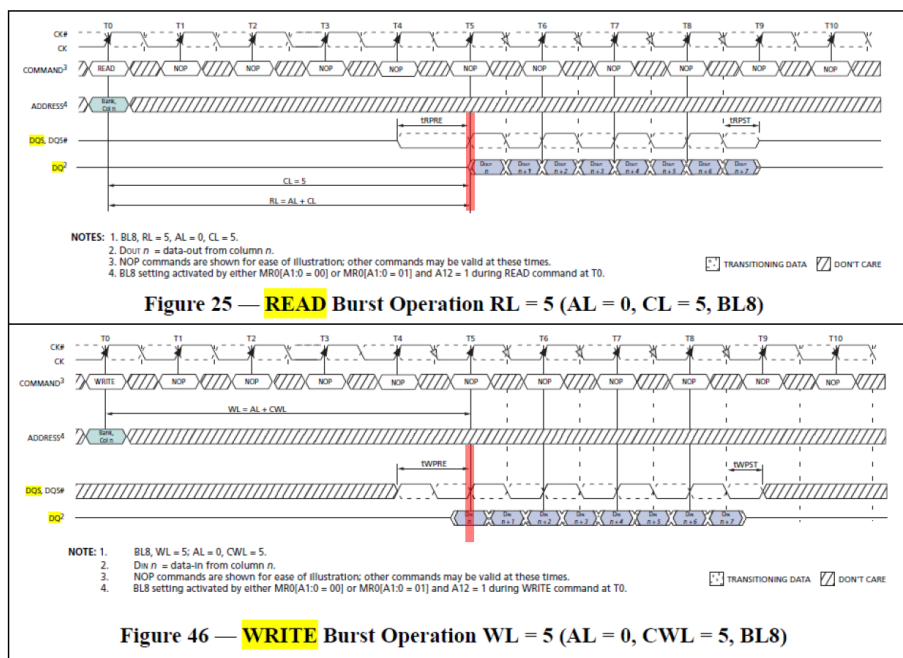
Of course, the general understanding of “*corresponds to*” should be analyzed in the context of “a person of ordinary skill.” *Polaris Innovations Ltd. v. Brent*, 48 F.4th 1365, 1376 (Fed. Cir. 2022). The Board’s construction requiring that a “*data path*” be located “in” a data signal line conflicts with the undisputed level of ordinary skill in the art. Specifically, the Board adopted a level of ordinary skill in the art that included knowledge of the JEDEC standards requiring data signals and strobe signals to travel together within a very tight tolerance, as discussed above (pp.6-7). *See* Appx9 (adopting a level of ordinary skill in the art in which a skilled artisan “would have been familiar with the JEDEC industry standards”).

There is no dispute that those JEDEC standards require keeping the data signals and the strobe signals together within a very tight tolerance. In its Patent Owner Response, Netlist cited to the JEDEC standards stating that strobe signals are “[e]dge-aligned with read data [and] centered in write data.” Appx6922 (citing

Appx7383, Appx7403). Moreover, the annotated figures from the JEDEC standards below, presented to the Board by Samsung, illustrate the requirement that DQS strobe signals and DQ data signals travel together for read and write operations.

JEDEC DDR3 SDRAM STANDARD

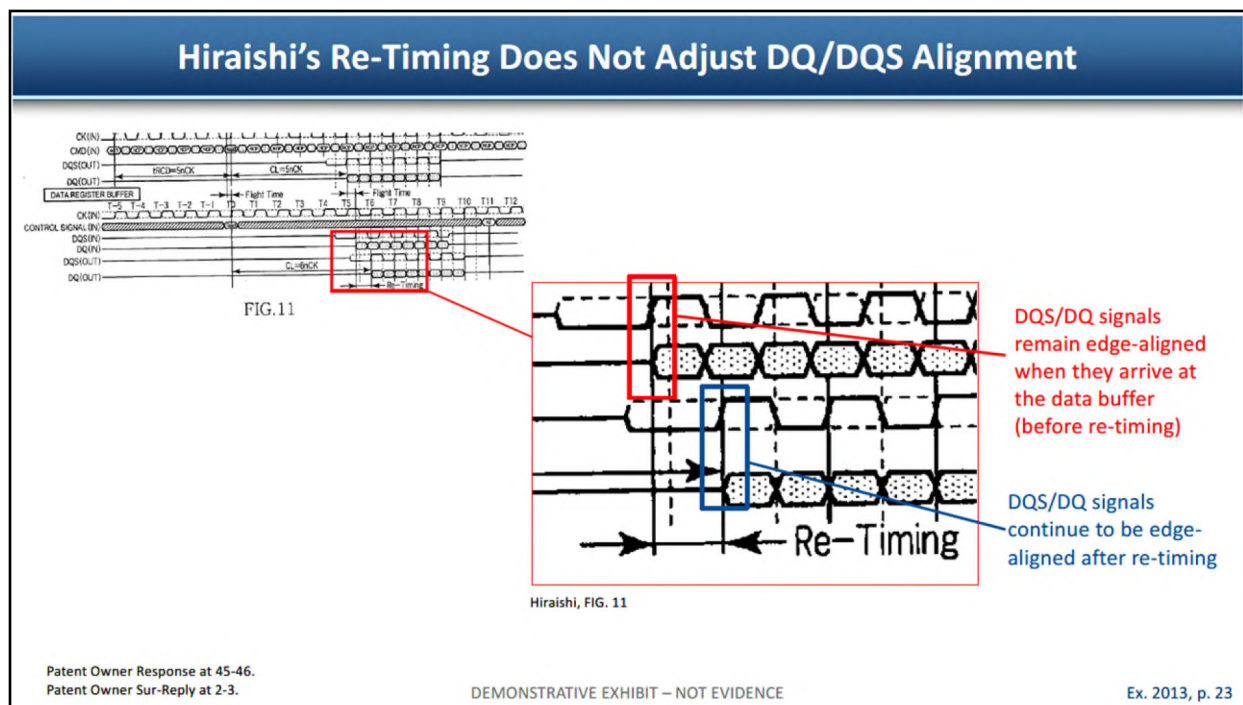
Read is edge aligned:



EX1020, 56, 71

Appx10208; see also Appx10498 n.10.

Netlist also admitted that “DQS signals . . . *ensur[e]* accurate timing for sampling/capturing DQ data.” Appx10479 (quoting Appx6921). And Netlist itself emphasized with its annotations below that Hiraishi teaches that the DQS strobe signal remains aligned with the DQ data signal, consistent with a POSITA’s knowledge of the JEDEC standards:



Appx9671-72; Appx10479. As admitted by Netlist's annotations above, when the DQ data signal is delayed, the DQS strobe signal needs to be delayed by the same amount, to “*ensur[e]* accurate timing for sampling/capturing DQ data,” Appx6921. The '608 Patent teaches the same thing. See Appx106 (step 1880: “Delaying the read strobe signal *and* the one or more read data signals according to the delay signal”).

While the Board acknowledged Samsung's argument, Appx13, it ignored this evidence when considering what “*corresponding to*” would mean to a POSITA in the claim language “*a data path corresponding to each data signal line in the respective set of data/strobe signal lines.*” In light of the adopted level of skill, a POSITA would have considered the claimed “*data path*” with circuitry for delaying

“a signal” to include not only data signals but also the corresponding strobe signal. See Appx668-74 ¶¶ 142-47.

D. The Board’s Construction Conflicts with the Intrinsic Evidence

Of course, “the ‘ordinary meaning’ of a claim term is its meaning to the ordinary artisan after reading the entire patent.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1321 (Fed. Cir. 2005) (en banc). Here, the intrinsic evidence also supports that the proper construction of “data path” encompasses circuitry that can carry signals including strobe signals.

For example, the Board relied on an erroneous analysis of dependent claim 10, which recites a “first **data path** for transmitting a **strobe signal**” and a “second data path for transmitting a first data signal.” Appx18-19; Appx117 (20:49-53). That language in dependent claim 10 relates to the requirement in claim 1 of “a delay circuit configured to delay a signal through the data path,” which dependent claim 10 shows can be “a **strobe signal**.” The cases cited by the Board fail to support its conclusion that claim 10 “recites new elements” when it claims the first and second data paths. Appx18. In neither of the cited cases did this Court give a different construction to the exact same term (“data path”) found in both dependent and independent claims. For example, in *Phillips*, the independent claim involved “baffles,” and the dependent claim further limited the “baffles” by requiring they be “oriented with the panel sections disposed at angles for deflecting projectiles such

as bullets able to penetrate the steel plates.” 415 F.3d at 1324. And in *Liebel-Flarsheim*, the independent claims “lack[ed] any reference to a pressure jacket” whereas the dependent claims added the “pressure jacket limitation.” *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). Therefore, contrary to the Board’s assertion that “*data path*” can have different meanings between claim 1 and claim 10, the use of “*data path*” in claim 10 confirms that a “*data path*” in claim 1 is broad enough to include circuitry transmitting strobe signals as well as a “*delay circuit*” for those strobe signals. See *Littelfuse, Inc. v. Mersen USA EP Corp.*, 29 F.4th 1376, 1380 (Fed. Cir. 2022) (“By definition, an independent claim is broader than a claim that depends from it, so if a dependent claim reads on a particular embodiment of the claimed invention, the corresponding independent claim must cover that embodiment as well. Otherwise, the dependent claims would have no scope and thus be meaningless.” (citation omitted)); *Samsung Elecs. Co. v. Power2B, Inc.*, No. 23-1630, 2025 WL 471124, at *4 (Fed. Cir. Feb. 12, 2025) (following *Littelfuse* and rejecting Board’s narrow claim construction).

Moreover, a claim limitation “is presumed to have the same meaning throughout all of the claims in the absence of any reason to believe otherwise.” *Digital-Vending Servs. Int’l, LLC v. Univ. of Phoenix, Inc.*, 672 F.3d 1270, 1275 (Fed. Cir. 2012). Claim 10 adds the limitation that the “*buffer circuit includes a first data path for transmitting a strobe signal associated with the second memory*

operation^[4] and a second **data path** for transmitting a first **data signal** associated with the second memory operation.” Appx117 (20:49-53). Consistent with the ordinary meaning of “corresponds to,” claim 10’s language confirms that the “**data path**,” as a claim term, is broad enough to encompass circuitry transmitting both a “**strobe signal**” and a “**data signal**,” in addition to including the “**tristate buffer**” and “**delay circuit**” of claim 1[f]. The Board’s construction of “**data path**” to exclude circuitry transmitting the “**strobe signal**” directly contradicts claim 10 and should be rejected.

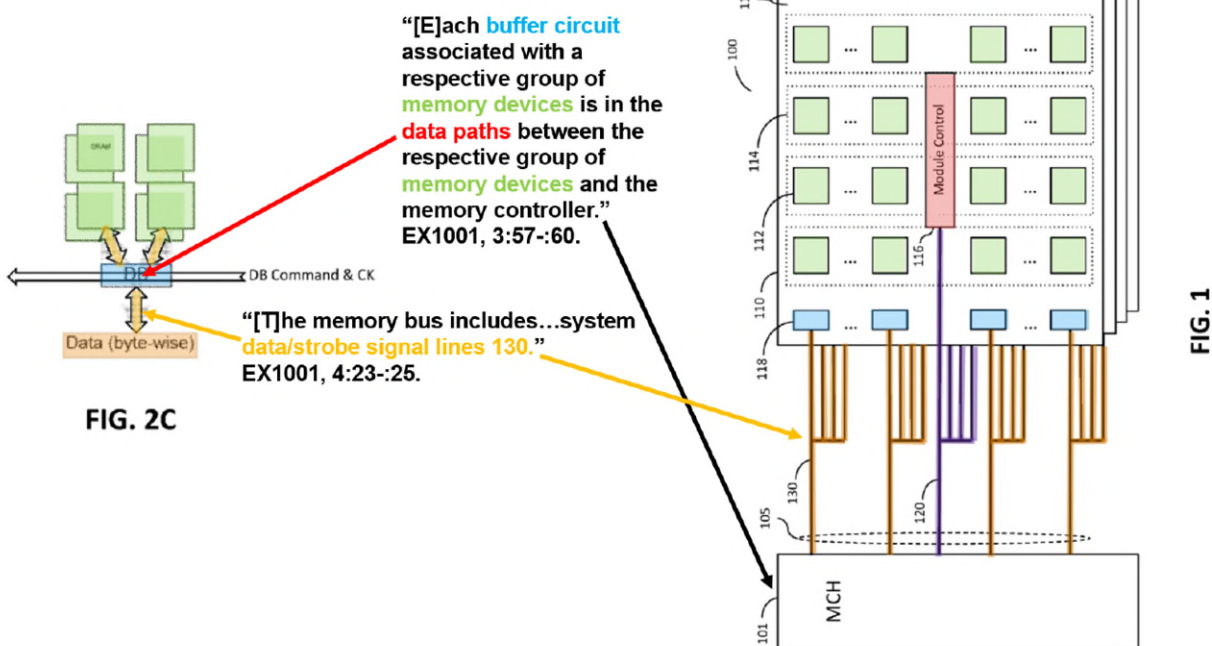
The Board recognized this contradiction but failed to resolve it. The Board’s conclusion that claim 10’s “**first data path**” and “**second data path**” are “new elements” that “are different than the element of ‘a data path’ of claim 1,” Appx18, makes no logical sense, particularly where claim 10 depends from claim 1,⁵ and both claims use the same term “**data path**.” The adjectives “first” and “second” are used in patent claims to identify particular instances of the **same** limitation, not create

⁴ The antecedent basis for “**the second memory operation**” is found in claim limitation 2[a]. Limitation 2[e] provides that “**the signal through the data path is a signal associated with the second memory operation**,” which again does not limit the “**signal**” in the data path to a **data** signal, given that strobe signals are also “**associated**” with “**memory operation[s]**,” as confirmed by claim 10 above. Although claim 10 states that it depends from claim 9, which depends from claim 1, the only antecedent basis for claim 10 is claim 2, which also depends from claim 1. Appx207 (n.3); Appx743 ¶ 221.

⁵ See *supra* p.45 n.4.

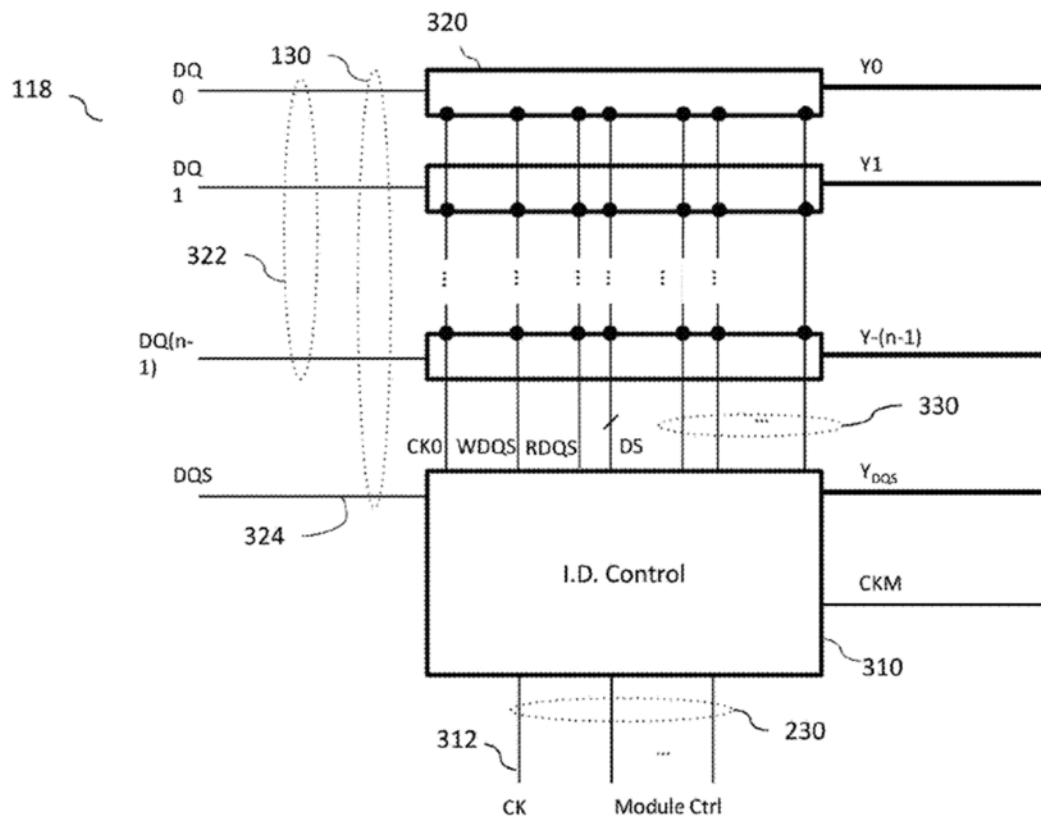
“new elements” as stated by the Board. *See 3M Innovative Props. Co. v. Avery Dennison Corp.*, 350 F.3d 1365, 1371 (Fed. Cir. 2003) (“The use of the terms ‘first’ and ‘second’ is a common patent-law convention to distinguish between repeated instances of an element or limitation.”). As expected of a dependent claim, claim 10 is more specific than claim 1, identifying a “*first*” and “*second*” data path, but it still refers to the same “*data path*” described in claims 1 and 2. Claim 10 does not impose on claim 1 its specific embodiment of “*separate data paths* for data signals and for strobe signals” as assumed by the Board. Appx19. Instead, the dependent claim’s language is only consistent with an understanding of “*data path*” as a broad claim term that can transmit, *inter alia*, a “*strobe signal*” or a “*data signal*,” or both.

The written description also supports a broad scope of “*data path*” that is not limited to just the “*data signal line*.” The written description states that “each buffer circuit [blue below] . . . is in the *data paths* between the respective group of memory devices [green below] and the memory controller [MCH].” Appx109 (3:57-:60); *see also* Appx110 (6:59-:62), Appx115 (15:17-:19). Furthermore, the “data/strobe signal *lines* 130” [orange below] are illustrated as *outside* the buffer circuit and *separate* from the data path inside the buffer circuit, Appx109 (4:20-25), Appx82, Appx85, contrary to the Board’s construction that the “*data path*” is “*in*” the “*data signal line*,” Appx16-17:



Appx10258-61 (annotating Appx82, Appx85); Appx10474.

Figure 3 illustrates an exemplary buffer circuit (118) and shows that a buffer circuit includes both DQ data signals (going horizontally toward the top) and at least one DQS strobe signal (going horizontally toward the middle) through the buffer. See Appx108 (2:46-47), Appx111 (8:4-8), Appx112 (10:31-61).

**FIG. 3**

Appx87. Accordingly, the buffer circuit (118)—and the data path through the buffer circuit—corresponds to both the data signal lines and the strobe signal line. Appx112 (10:31-61).

The Board acknowledged that “the buffer may receive both data and strobe signals, as shown in Figure 3,” but provided no support for its tautological conclusion that Figure 3 therefore supports its “interpretation” that “the data signal lines, which are on the claimed data path, carry data signals only.” Appx18. In Figure 3, the data signal (DQ) lines 322 are parallel to the strobe signal (DQS) lines

324, and collectively make up a group of data/strobe signal lines 130 that correspond to a given buffer 118. Appx112 (10:31-61). The Board purports to cite to discussions of Figures 3, 4A, and 4B to show “that there are different transmission lines (*data paths*) with a separate signal transmission line for transmitting/receiving data signals and a separate strobe line for transmitting/[receiving] strobe signals.” Appx17. But none of these figures or discussions equates “*data path*” with “data signal lines,” as the Board does. In fact, none of the cited figures or discussions even use the term “data path” at all. Appx112-13 (10:31-11:8, 11:20-45).⁶

The Board also improperly conflated “*data path*” with “*data signal line*” when it addressed testimony from Netlist’s expert that the data and strobe signals “must travel together within a ‘very tight tolerance.’” Appx19 (citing Appx10478 (quoting Appx8981 (139:13-24))). The Board ignored this testimony because “the data signal and strobe may travel on different transmission lines.” Appx19. The Board misses the point. The Board’s observation that data and strobe signals “travel on different transmission lines” is only relevant if the Board limits the “path” to just one of the “lines,” which is incorrect because, as noted above, a “data path” can contain

⁶ In this discussion of Figures 3, 4A, and 4B, the Board also cites to the abstract for the ’608 Patent as “identifying that the ‘data path’ corresponds with the data signal line in the set of data/strobe signal lines.” Appx17 (citing Appx75). This language in the abstract, added years after the filing date, *compare* Appx330 (Nov. 21, 2017), *with* Appx1024 (July 27, 2013), is identical to the limitation 1[e] itself and thus provides no additional illumination on the meaning of “*data path*” as of the effective filing date of the patent.

multiple signals, including strobe signals. While the data and strobe signals will travel on different lines, labeled DQ and DQS respectively, they still travel together on the same “*data path*” within a very tight tolerance, as admitted by Netlist’s expert and as a POSITA would know because it is required by JEDEC for proper operation.

Equating the “*data path*” with the separate claim limitation “*data signal line*” is also contrary to “precedent instruct[ing] that different claim terms are presumed to have different meanings.” *Helmsderfer v. Bobrick Washroom Equip., Inc.*, 527 F.3d 1379, 1382 (Fed. Cir. 2008). The Board attempted to overcome that presumption by stating that its interpretation does not “conflate[] ‘data path’ with the ‘data signal line.’” Appx17. However, the Board provided no meaningful distinction between the two terms: “A reasonable plain meaning of ‘data path’ is that it is the path that data is transmitted on, and, as discussed above, the claimed ‘data signal line’ is the actual data signal line of the respective set of data/strobe lines.” Appx17-18 (footnote omitted). But if the “*data path*” can only be located “in” the “*data signal line*,” as determined by the Board, *id.*, then the Board’s purported distinction vanishes. It is only where the “*data path*” is broader than the “*data signal line*,” such that it can carry the strobe signals and include the “*delay circuit*” as required by limitation 1[f], that the “*data path*” and “*data signal line*” terms are given distinctive meanings.

Furthermore, the other intrinsic evidence cited by the Board also does not support its construction. The Board focused on Figures 15 and 16 of the '608 Patent showing “data paths” and “strobe paths,” which the Board concluded shows “separate data paths for data signals and for strobe signals.” Appx19. As an initial matter, it would be inappropriate for the Board to limit the meaning of “*data path*” based only on a single embodiment, particularly where the term “data path” is discussed more broadly in other portions of the specification. *See, e.g., Weber, Inc. v. Provisur Techs., Inc.*, 92 F.4th 1059, 1070 (Fed. Cir. 2024) (“[W]e have repeatedly warned against confining the claims to [specific] embodiments.”). The '608 Patent itself confirms that general rule in no uncertain terms. Appx112 (10:25-28) (“It should be strongly noted that the following information is set forth for illustrative purposes and should not be construed as limiting in any manner.”). Furthermore, the specification’s occasional use of the terms “data paths” and “strobe paths” does not require all data paths to exclude strobe signals. The claims of the '608 Patent exclusively use the term “*data path*,” and where the claims refer to a “path” that includes a strobe signal, such as in claim 10, it still uses the term “*data path*.” As a result, the Board’s reading of Figures 15 and 16 would conflict with the claims themselves. Such an improper reading should be rejected.

E. Correction of the Board’s Improperly Narrow Construction Requires Remand for Reconsideration of Grounds 1-3

The Court should reverse the Board’s narrow claim construction and remand for reconsideration of Grounds 1-3⁷ using the correct claim construction. *Kaken Pharm. Co. v. Iancu*, 952 F.3d 1346, 1355 (Fed. Cir. 2020) (“We conclude that the appropriate course in this case, as in so many others involving a reversal of a Board claim construction, is to vacate the Board’s decision and remand the matter.”).

The Board’s rejection of Ground 2 relied entirely on its narrow claim construction with no additional analysis. Appx69-70. After setting out the parties’ arguments regarding Ground 2, Appx68-69, the Board’s only discussion concerned its exclusion of strobe signals from the claimed “*data path*”:

As we discussed above, claim 1 should be interpreted such that a “data path” corresponds to data signal lines that carry data signals, and not to strobe signal lines that carry strobe signals. The data path that Petitioner relies upon in the combination of Hiraishi and Tokuhiro ***includes lines that carry strobe signals***. Thus, Petitioner has not met its burden to demonstrate how the combination of Hiraishi, Butt, and Tokuhiro [Ground 2] teaches the limitations of claim 1. By virtue of their dependency from independent claim 1, the challenges to dependent claims 2–5 also fail.

Appx69-70.

⁷ Ground 3 combined an additional reference (Ellsberry) with either Ground 1 or 2. Appx141; Appx70. Netlist only challenged Grounds 1 and 2 and did not separately challenge Ground 3.

Likewise, the Board’s consideration of the petition’s so-called “Original Contentions” for Ground 1 was also limited exclusively to its narrow claim construction. *See* Appx31-43. Based on that construction, the Board concluded that neither Hiraishi nor Butt discloses a “*delay circuit*” in the “*data path*” that delays a “*signal through the data path.*” *Id.* The Board repeatedly relied on its narrow construction requiring that the “*data path*” “correspond to data signal lines carrying data signals, not to strobe signal lines carrying strobe signals.” Appx40, Appx41, Appx42.

Thus, the Board should reconsider Grounds 1-3 using the correct claim construction.

III. The Board Erred in Failing to Apply Collateral Estoppel to Underlying Facts and in Ignoring Inconsistent Assessments of Prior Art Teachings Across the Two IPRs of Related Patents

The Board also made another, independent error: The Board should have applied collateral estoppel but instead improperly ignored its own previous Final Written Decision involving a materially identical prior art reference. Samsung argued to the Board that Netlist’s characterization of the Hiraishi reference was precluded by several specific factual findings previously made by the Board against Netlist in the ’035 Final Written Decision. *See* Appx10470-71, Appx10482, Appx10486, Appx10501-03, Appx10506-07 (citing Appx6706-08, Appx6723-44, Appx6747-53). Such previous determinations regarding the teachings and scope of

the prior art are factual determinations. *Genentech, Inc. v. Sandoz Inc.*, 55 F.4th 1368, 1377 (Fed. Cir. 2022) (“it is well established that what the prior art teaches is a factual question”); *In re Urbanski*, 809 F.3d 1237, 1241 (Fed. Cir. 2016) (“Obviousness is a question of law based on underlying factual findings, including what a reference teaches” (citation omitted)).

Despite Samsung identifying specific factual findings regarding the prior art that were contrary to Netlist’s current arguments, the Board analyzed the issue by focusing on whether there were differences between the **claims** of the ’035 and ’608 patents. Appx20 (“The claims of the ’035 patent and the instant ’608 patent are different.”). In doing so, the Board failed to address whether the underlying **factual findings** that Samsung identified were identical and otherwise met the requirements for collateral estoppel. Appx20-23.

Factual findings are subject to collateral estoppel, even if they are made with respect to different ultimate issues. See Restatement (Second) of Judgments § 27 note c (“[a]n issue on which relitigation is foreclosed may be one of evidentiary **fact**”); *Mother’s Rest., Inc. v. Mama’s Pizza, Inc.*, 723 F.2d 1566, 1571-73 (Fed. Cir. 1983) (“[W]e hold that the TTAB properly gave preclusive effect to the Texas court’s findings of **fact**”). The Board erred in this IPR by allowing Netlist to relitigate identical factual issues regarding the teachings of the prior art based only on differences in legal issues. The Board should have determined whether the

requirements of collateral estoppel are met for the asserted factual findings themselves. In addition, because the basis for the collateral estoppel was the Board’s own prior ruling, the Board erred in failing to provide any “reasoned basis” for the “direct conflict between the Board’s fact findings” in the two Final Written Decisions, and thus its decision should be vacated and remanded for that reason as well. *Vicor Corp. v. SynQor, Inc.*, 869 F.3d 1309, 1323 (Fed. Cir. 2017). These points are discussed in more detail below.

A. Samsung Argued that the Board’s Previous Fact Findings Regarding Materially Identical Prior Art in the ’035 IPR Precluded Netlist’s Contrary Positions Regardless of Differences in the Claims

After Netlist asserted that the Hiraishi reference did not teach certain operations, Samsung identified how the Board’s recent Final Written Decision addressing the related ’035 patent had already made findings that those operations were taught by Osanai, which is the same as Hiraishi “in all material respects” as discussed above. *Supra* p.17 & n.2. For example, Samsung identified the Board’s findings that read and write leveling were performed in response to particular signals, including the DRC signal conveying a “mode register set” (MRS) command, and, as part of that process, that the timing of **both** data signals **and strobe** signals was delayed. Appx10470-71, Appx10482, Appx10486. Samsung argued that this important factual finding was controlling “even under Netlist’s narrow

construction,” and that it was independent of the claim construction dispute. Appx10481-82; Appx10404 (17:14-22); Appx10242-47.

Samsung also identified the specific circuitry in Hiraishi—a data buffer—that the Board had previously identified as performing read and write leveling to control the timing of both data and strobe signals. Appx10486. During the oral argument before the Board, after Netlist had argued that collateral estoppel could be avoided based only on a difference in claim language, Samsung again explained that estoppel would still apply based on the ’035 Final Written Decision’s “subsidiary factual determinations.” Appx10436 (49:9-13). Samsung identified in both its reply brief and at oral argument specific factual findings against Netlist in the previous Final Written Decision such as rejection of Netlist’s argument that Osanai/Hiraishi “doesn’t control the timing of the data [and] strobe signals on the data paths in accordance with tim[ing] information.” Appx10436 (49:3-25); Appx10244-47; Appx10470-73, Appx10481-82, Appx10485-86, Appx10501-03, Appx10506-07. As a result, the Board was aware of Samsung’s arguments that Netlist was precluded from relitigating specific factual issues regardless of the claim construction dispute.

B. Collateral Estoppel for Subsidiary Fact Findings Must Be Evaluated Independently of the Ultimate Legal Issues

The Board erred when it refused to apply collateral estoppel as to subsidiary factual findings based on differences in claim language and overall obviousness grounds. Obviousness and claim construction are both legal issues, the

determination of which can be based on underlying or subsidiary facts. *See Graham*, 383 U.S. at 17-18; *Teva*, 574 U.S. at 326-27. A party can seek to apply collateral estoppel to such an “ultimate” issue and the factors would then be applied at the level of that issue, including legal considerations such as claim scope. *See, e.g., Google LLC v. Hammond Dev. Int’l, Inc.*, 54 F.4th 1377, 1381 (Fed. Cir. 2022). However, under this Court’s law, collateral estoppel is not limited to such ultimate issues. Thus, one, the other, or both of the determinations about claim construction and the teachings of a reference can be separately subject to collateral estoppel. *See, e.g., Papst Licensing GMBH & Co. KG v. Samsung Elecs. Am., Inc.*, 924 F.3d 1243, 1252-53 (Fed. Cir. 2019) (separately considering collateral estoppel as to both “the claim-construction and Aytac-teaching issues”).

Collateral estoppel should be applied consistent with the Restatement (Second) of Judgments (1980), including section 27 of the Restatement, which applies collateral estoppel to “an issue of **fact** or law” that is “actually litigated and determined by a valid and final judgment” where “the determination is essential to the judgment.” *B & B Hardware, Inc. v. Hargis Indus., Inc.*, 575 U.S. 138, 148 (2015) (quoting § 27). This Court has also long looked to the Restatement in applying the principles of collateral estoppel. *See, e.g., Voter Verified, Inc. v. Election Sys. & Software LLC*, 887 F.3d 1376, 1383 (Fed. Cir. 2018); *Jackson*

Jordan, Inc. v. Plasser Am. Corp., 747 F.2d 1567, 1575-76 (Fed. Cir. 1984) (citing cases).

The Board identified the requirements of applying collateral estoppel and emphasized the first prong:

(1) *the issue is identical to one decided in the first action*; (2) the issue was actually litigated in the first action; (3) resolution of the issue was essential to a final judgment in the first action; and (4) [the party against whom collateral estoppel is being asserted] had a full and fair opportunity to litigate the issue in the first action.

Appx20 (alteration and emphasis in original). However, the Board then slightly, but significantly, altered the test for collateral estoppel by changing the singular “issue” in the first prong to the plural “issues.” Appx20 (“The *issues* in this proceeding and those at issue in the -00236 IPR are not identical. The claims of the ’035 patent and the instant ’608 patent are different.”). The Board did not analyze whether the particular fact findings Samsung identified were identical; instead it required the issues in the proceedings as a whole to be identical and then pivoted to claim construction as an issue it concluded was not identical.

However, “[a]n issue on which relitigation is foreclosed may be one of evidentiary fact, of ‘ultimate fact’ (i.e., the application of law to fact), or of law.” Restatement (Second) of Judgments § 27 cmt. c (1980). That broad scope of potential estoppel issues is consistent with this Court’s separate analysis in *Papst Licensing* of collateral estoppel with respect to a legal issue (claim construction) and

a factual issue (teachings of the Aytac reference). *See* 924 F.3d at 1252-53. The Board erred by refusing to consider the preclusive effect of the specific fact issues previously decided, or even consider whether, in the '035 Final Written Decision, those fact issues had been identical, actually litigated, resolved in a manner essential to that decision, and subject to Netlist's full and fair opportunity to contest them.

In previous cases, the Board has recognized the need to analyze the specific factual issues that may be precluded. For example, in *Mobile Tech, Inc. v. InVue Security Products Inc.*, IPR2018-00481, Paper 29 (PTAB July 16, 2019), the Board acknowledged that “[u]nder traditional principles of issue preclusion . . . a party may be bound not simply by the ultimate conclusion (e.g., unpatentability of a claim), *but by any subsidiary factual determinations that were actually litigated and essential to the judgment.*” *Id.* at 18. That understanding of issue preclusion is consistent with this Court's explanation in *Mother's Restaurant, Inc. v. Mama's Pizza, Inc.*, 723 F.2d 1566 (Fed. Cir. 1983). The *Mother's Restaurant* Court clarified that “the requirement that a finding be ‘necessary’ to a judgment does not mean that the finding must be so crucial that, without it, the judgment could not stand.” *Id.* at 1571. Instead, it was sufficient that the fact was a “focus” of the parties' arguments in the previous state court action and that it was among the “determinations leading to [that court's] judgment.” *Id.*

As shown below with respect to the Board's analysis of Ground 1, each of the factual findings Samsung argued was preclusive was identical to factual findings decided in the '035 Final Written Decision as part of the analysis leading to the cancellation of claims in the '035 patent. *See infra* § IV, pp.62-74. Samsung therefore requests that this Court apply collateral estoppel for the specific factual findings identified by Samsung, or in the alternative remand to the Board to perform that analysis. The Board did not reach any of the other three requirements for collateral estoppel, but Netlist never disputed them.

C. The Board Failed to Provide a Reasoned Analysis for Its Contrary Factual Findings Reached in IPRs of Related Patents

The Court should also reject the Board inconsistent factual findings for an independent reason: it constitutes an unjustified conflict with a previous Board decision. While a judgment by a court, such as the one in *Mother's Restaurant*, can result in collateral estoppel, a previous decision by the Board has further consequences under the APA. Under the APA, the Court also considers whether Board's actions are "arbitrary" or "capricious." 5 U.S.C. § 706(2). Of course, "not every instance of an agency reaching inconsistent outcomes in similar, related cases will necessarily be erroneous," but analyzing the circumstances and findings of the Board's previous '035 Final Written Decision establishes conflicts sufficient for this Court to vacate and remand. *Vicor Corp.*, 869 F.3d at 1322.

In *Vicor*, the factual inconsistency at issue involved a broader and more complicated issue: “inconsistent conclusions regarding the weight to be accorded the objective indicia evidence.”⁸ As the Court noted, the weight to be accorded such evidence depended on its nexus to the claims in each patent. *Id.* at 1321-22 (comparing “[i]n the ’290’s reexamination, the Board found the objective evidence to be so persuasive that it approved of the examiner’s decision to withdraw rejections” with “no nexus between the objective evidence and the claims of the ’021 patent”). Furthermore, the Court had earlier explained that there were claim differences because the “substantially uninterrupted flow of power” limitation was not found in the ’290 claims, but was “in all claims of the ’021 patent.” *Id.* at 1315.

By contrast, the Board’s inconsistent findings here do not have the added complication of weighing evidence in view of the nexus to different claims. Instead, they concern claim-independent questions regarding the teachings of the Osanai/Hiraishi prior art reference, as discussed above (pp.55-56). Additional inconsistencies are discussed below. *See infra* § IV, pp.62-74. The ’608 Decision offered no explanation or justification for its inconsistent factual findings. Thus, at a minimum, the Board’s decision should be vacated and remanded in accordance with *Vicor Corp.*

⁸ There was also a legal inconsistency in how the *Graham* factors were assessed. *See Vicor Corp.*, 869 F.3d at 1321 (discussing “[t]he Board’s legal error”).

IV. The Board’s Factual Findings Regarding Ground 1 Are Precluded by the ’035 Final Written Decision and Lack Substantial Evidence

Applying Netlist’s narrow claim construction for “*data path*,” the Board improperly rejected Samsung’s FIFO theory for Ground 1 based on erroneous factual findings about Hiraishi, discussed below, including those about MRS commands, write leveling, the FIFO circuit, and read leveling. Those findings are inconsistent with and precluded by the ’035 Final Written Decision, and lack substantial-evidence support because they contradict key disclosures in Hiraishi and the JEDEC industry standard adopted as part of the level of ordinary skill in the art. The Court should therefore vacate and remand the decision to the Board to reconsider Ground 1, regardless of how the Court construes “*data path*.”

A. The Board’s Finding That the MRS Command Is Not Used for Leveling Is Inconsistent with the ’035 Decision and Lacks Substantial Evidence

The Board disagreed that “an MRS [mode register set] command, as disclosed in the JEDEC standard, is a command signal that one of skill in the art would use in Hiraishi” for read/write leveling. Appx65-67. That finding directly conflicts with the ’035 Decision, which found that in Osanai/Hiraishi, “the write leveling operation is performed in response to a memory command such as the ***Mode Register Set (MRS) command*** and . . . memory devices receive this command to perform ***write leveling***.” Appx6732; *see also* Appx6753 (agreeing with the contention that “Osanai/[Hiraishi]’s read and write leveling circuitry use both these signals

[including DRC signals, which convey the MRS command] to adjust the read and write timing”).

The Board’s finding that a POSITA would not understand Hiraishi to use an MRS command for read/write leveling also lacks substantial evidence. It is undisputed that a POSITA “would have been familiar with the JEDEC industry standards,” which governed the operations of the DDR3 memory devices used in Hiraishi. Appx9; Appx871 ¶ 163 (“DDR3”). The JEDEC standard teaches that read/write leveling is performed in response to the MRS command, Appx3142, which sets various “mode registers” to appropriate values to perform read/write leveling. See Appx10486, Appx10486 (n.3); Appx184-87, Appx188-91; Appx10233. For example, and as admitted by Netlist’s expert, the JEDEC standard requires “[i]ssuing MRS Command to load MR1” during initialization, including “A7” which is what “enable[s]” “Write leveling.” Appx3128, Appx3135, Appx3151-52; Appx8947-48 (105:12-106:6), Appx8961-65 (119:20-123:7). For read leveling, the JEDEC standard similarly teaches “[i]ssuing MRS Command to load MR3” during initialization, including “A2” which is what initiates read leveling by “enabl[ing] the MPR” containing a “predefined pattern . . . used for read synchronization,” as admitted by Netlist’s expert. Appx3128, Appx3140, Appx3157, Appx3159-60; Appx8965-70 (123:8-128:22).

Consistent with the JEDEC standard and Netlist’s expert testimony, Hiraishi teaches that “[t]he initializing operation includes a mode register setting [MRS] operation by which predetermined mode information is set in the mode registers . . . (Step S3)” and “[u]pon *completing the mode register setting* operation, a leveling operation . . . is performed (Step S4).” Appx870 ¶¶ 139-40; Appx689-90 ¶ 159, Appx698-99 ¶ 164, Appx713-14 ¶ 176. The Board ignored the level of skill in the art (which includes familiarity with the JEDEC standard) when it found that a POSITA would not have used an MRS command in Hiraishi. Appx65-67. The Board reasoned that “the mode register setting occurs, not as part of the S4 read/write leveling, but rather as a separate earlier step (S3), so the S3 mode register setting step would not be relevant to S4 read/write leveling in Hiraishi.” Appx66. To the contrary, as discussed directly above and as previously found by the Board in the ’035 Final Written Decision, Appx6732, the JEDEC standard requires an MRS command (in Step S3 of Hiraishi) to enable read and write leveling (in Step S4 of Hiraishi).

B. The Board’s Finding That Write Leveling Does Not Adjust for Different Flight Time Delays on the DQ Data Lines Is Inconsistent with the ’035 Decision and Lacks Substantial Evidence

The Board incorrectly assumed that because Hiraishi’s “write leveling is done to address mismatches between . . . the clock signal CK and the data strobe signal DQS,” that write leveling is “*not* done to determine delays in [DQ] data signal lines

to account for different flight time delays for L1/L2.” Appx56. In fact, write leveling does both, and the Board’s assumption that write leveling is irrelevant to the DQ data signal is contrary to the ’035 Final Written Decision, which found that the “read and write leveling circuits of Osanai/[Hiraishi] make timing adjustments [to] **data** and strobe signals associated with read and write operations.” Appx6736; *see also* Appx6727 (Osanai/Hiraishi teaches “write leveling” to make “timing adjustments,” including “a time **delay** based on the module clock signal . . . to create **DQ-Post** . . . and adjust write timing . . .”).

The Board’s finding also lacks substantial evidence and is contrary to Hiraishi’s teachings in light of the agreed knowledge of a POSITA and both experts’ testimony. Hiraishi teaches that the delay measured during write leveling is applied to **both** the DQ data signals **and** the DQS strobe signals during subsequent write operations “to ensure that the standard data to strobe timing requirements are met.” Appx186 (citing Appx844; Appx691-92 ¶ 160; Appx3177); *see also* Appx10489-92, Appx10492 n.6. Specifically, Hiraishi teaches that “write leveling” results in “displacing the internal clock LCLKW.” Appx870 ¶ 145. Hiraishi then explains that during a subsequent write operation, **the same internal clock LCLKW signal** is what delays (i.e., “re-tim[es]”) the **DQ data signal**:

The data register buffer 300 loads the received write data DQ in the FIFO (Write) circuit 301 The data register buffer 300 then performs **a re-timing in synchronization with the internal clock**

LCLKW using the FIFO (Write) circuit 301 to convert WL into WL=5, and outputs the write data DQ and the data strobe signal DQS.

Appx869 ¶ 135. Figure 12 of Hiraishi confirms that **both** the DQ data signal **and** the DQS strobe signal are delayed (i.e., “re-tim[ed]”) by the data register buffer (as shown by comparing DQ(IN) to DQ(OUT), and DQS(IN) to DQS(OUT)) so that they are both properly aligned with the CK clock signal at time T5 at the memory chip:

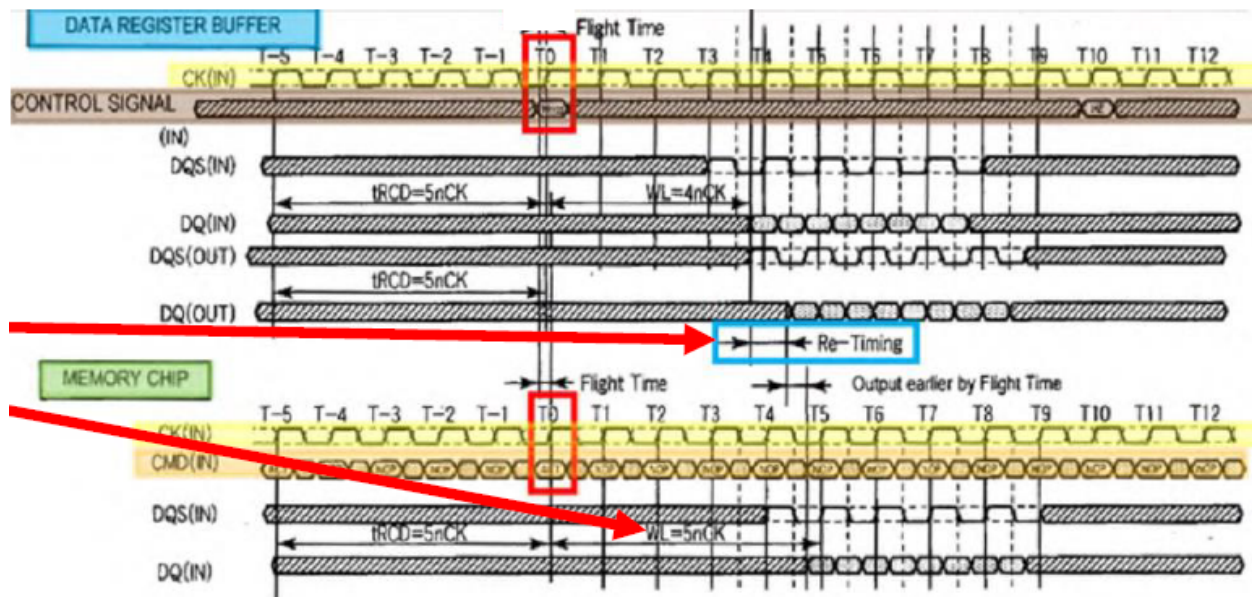
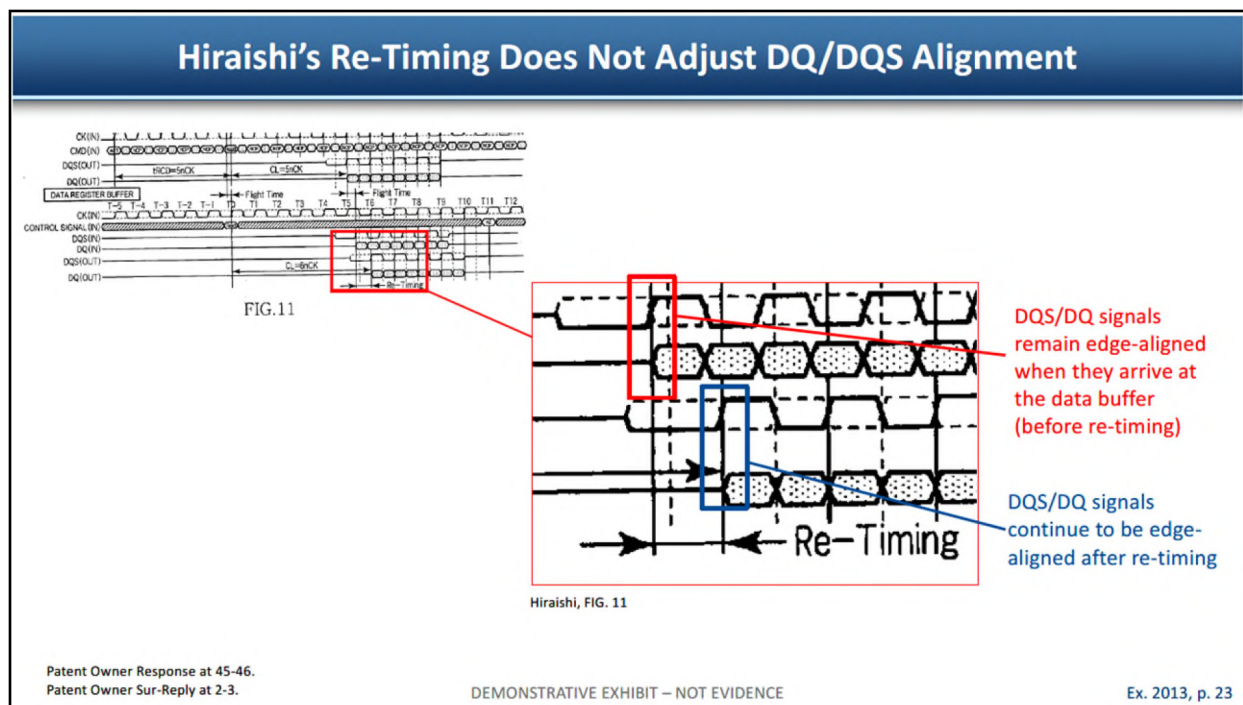


FIG.12

Appx10214; Appx186 (annotating Appx844); see also Appx870 ¶ 136 (“[T]he data register buffer 300 [blue] **outputs the write data DQ earlier by an amount equivalent to the Flight Time,**” so that “it becomes possible for the memory chip 200 [green] to receive the write data DQ in a correct manner.”); Appx870 ¶ 140 (“The leveling operation is to adjust a write timing . . . in consideration of a

propagation time [i.e., Flight Time] of a signal. The adjustment of the write timing is performed by a write leveling operation”); Appx10436-38 (49:26-51:3).

The Board disregarded all of the evidence above based on testimony by Netlist’s expert that write leveling only affects the DQS strobe signal. Appx59-62. But expert testimony that conflicts with the reference’s actual disclosures is not substantial evidence. *See Homeland Housewares, LLC v. Whirlpool Corp.*, 865 F.3d 1372, 1378 (Fed. Cir. 2017) (“we must disregard the testimony of an expert that is plainly inconsistent with the record”); *OSI Pharms., LLC v. Apotex Inc.*, 939 F.3d 1375, 1383 (Fed. Cir. 2019) (“When the references are properly read, the Board’s finding . . . is not supported by substantial evidence.”). And that expert testimony also conflicted with the Board’s previous finding in the ’035 Decision that Osanai/Hiraishi teaches “write leveling” to make “timing adjustments” to “delay” the DQ data signal (not just the DQS strobe signal). Appx6727, Appx6736. Indeed, it is undisputed that the DQ data signal must stay aligned with the DQS strobe signal within “a very tight tolerance,” Appx8981 (139:13-24), which is why write leveling delays both signals, not just one, as taught by Hiraishi above. Netlist itself has admitted this, as shown below: Hiraishi teaches delaying **both** the DQS strobe signal **and** the DQ data signal by the **same** amount, to “**ensur[e]** accurate timing for sampling/capturing DQ data,” Appx6921.



Appx9671-72; Appx10479.

Additionally, under the correct construction of “*data path*” — which includes both data and strobe signals — the Board’s finding that write leveling is “used to delay . . . the DQS [strobe] signal” provides an independent ground for remand. Appx62. Hiraishi’s “delay circuit” delays the DQS strobe signal (e.g., “strobe generating circuits 374 generating a delayed strobe signal”) by an amount determined during write leveling, meeting the claim requirement under the correct claim construction that includes strobe signals. Appx185-87. The Board disregarded these arguments and supporting evidence based on its improper narrow construction that excluded the strobe signal from the “*data path*.” Appx40 (“strobe

generating circuit 374 . . . sends a strobe signal . . . which is not on a ‘data path’ as claimed”).

C. The Board’s Finding that Hiraishi’s FIFO Cannot Be a Delay Circuit Is Inconsistent with the ’035 Decision and Lacks Substantial Evidence

The Board found that Hiraishi’s “FIFO” in Figure 5 is not a “delay circuit” for the DQ data signal. Appx49-50. Again, however, the Board’s finding is inconsistent with the ’035 Final Written Decision, which found that Osanai/Hiraishi “teach controlling the timing of the data and strobe signals on the data paths [L0 to L1/L2, which goes through the FIFO] on which those signals travel.” Appx6737; *see also* Appx6736 (“data paths connect lines L0 to lines L1 and L2”). The lines L0 to L1/L2, which go through the FIFO 301 in the write direction, are highlighted below, and those lines also go through FIFO 302 in the read direction:

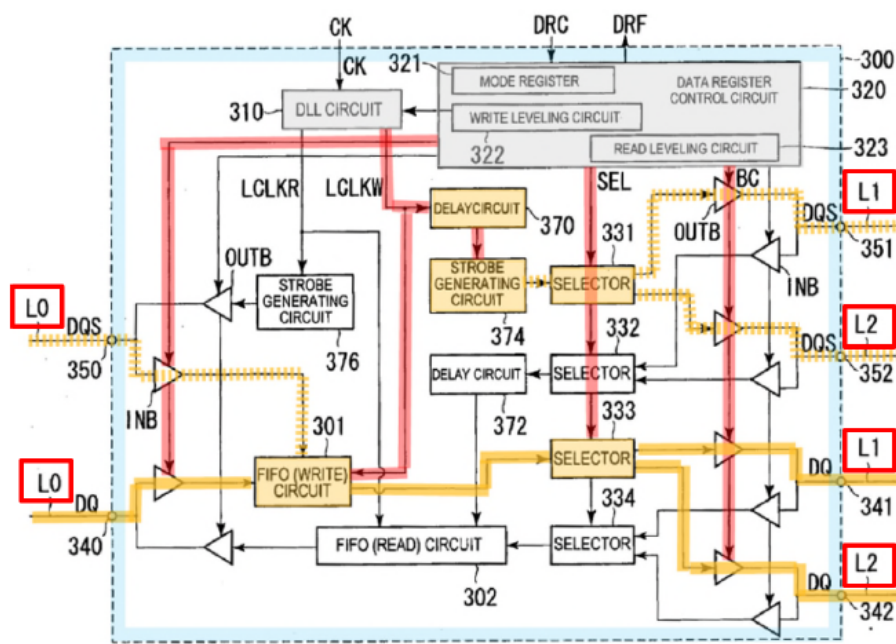


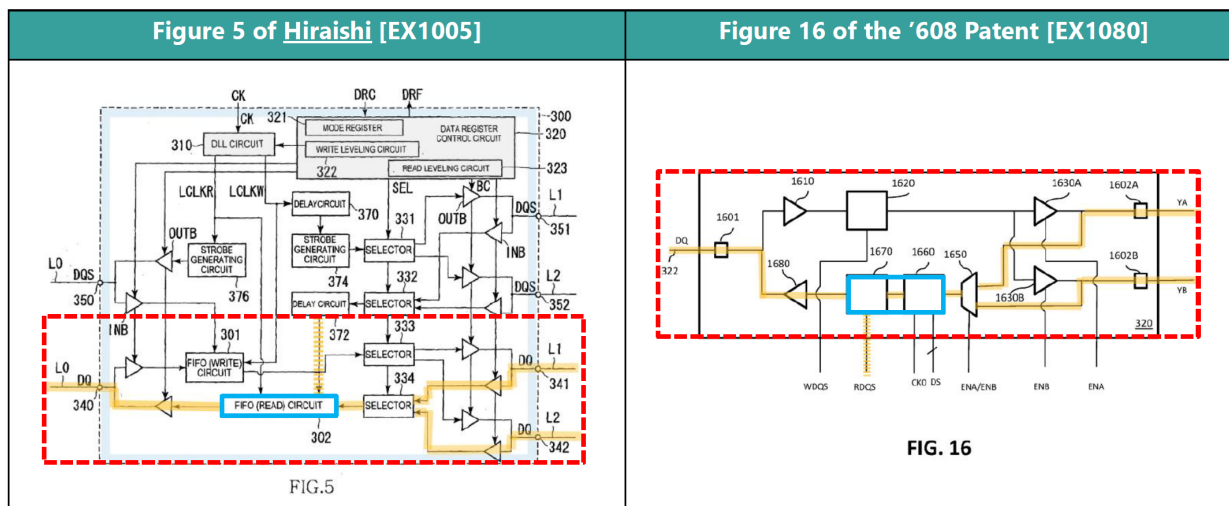
FIG. 5

Appx10472 (annotating Appx837, which is the same as Appx6219); *see also* Appx10227-28.

The Board’s finding also lacked substantial evidence and was contrary to Hiraishi’s teachings. Hiraishi expressly teaches delaying the DQ data signal by “perform[ing] a re-timing . . . **using the FIFO . . .**” Appx869-70 ¶¶ 130, 135, Appx843-44 (showing “re-timing”); Appx10214. That was explained in both Samsung’s Petition and supporting expert declaration. Appx187 (“Ground 1’s delay circuit for write operations includes the Write FIFO 301 delaying the write data signal . . .”), Appx191 (“Ground 1 discloses the claimed ‘*delay circuit*’ for read operations, including the FIFO (read) circuit 302 delaying the read signal . . .”); Appx693-95 ¶ 161, Appx701-03 ¶ 166; Appx10227-28.

The Board incorrectly stated that “[t]here is no declaratory expert testimony in the record . . . in support of Petitioner’s new assertion in Reply that only Hiraishi’s FIFO circuits teach the claimed ‘delay circuit.’” Appx49. To the contrary, Samsung’s expert explained that “Hiraishi’s **delay circuit** for write operations includes the **FIFO (write)** circuit 301,” Appx693-95 ¶ 161, and “Hiraishi discloses the claimed ‘**delay circuit**’ for read operations, including the **FIFO (read)** circuit 302 delaying the data signal,” Appx701-03 ¶ 166. Samsung also explained in its Reply, Appx10484-85, that the FIFO circuit in Hiraishi (blue, below left) directly corresponds to the “*delay circuit*” in Figure 16 of the ’608 Patent (blue, below right)

under Netlist’s narrow construction for “*data path*” that excludes everything that is not physically on top of the DQ data line:



Appx10226. The Board reasoned that Hiraishi’s FIFO could not be a “*delay circuit*” because it connects to other circuitry not physically on top of the DQ “*data path*” such as DLL 310, delay circuits 370/372, and strobe generating circuits 374/376. Appx49. But Netlist’s expert admitted that the “*delay circuit*” in Figure 16 of the ’608 Patent (above right) also requires a “*delay signal DS*” from another circuit that is **not** physically on top of the “*data path*” under Netlist’s narrow construction limited to the DQ data line, Appx8995-96 (153:2-154:5). The Board’s narrow interpretation of “*delay circuit*” when evaluating Hiraishi’s teachings would exclude the preferred embodiment in the ’608 Patent (above right), which is “rarely, if ever correct.” *Kaufman v. Microsoft Corp.*, 34 F.4th 1360, 1372 (Fed. Cir. 2022).

D. The Board’s Finding That Hiraishi’s FIFO Does Not Delay During Read Leveling Is Inconsistent with the ’035 Decision and Lacks Substantial Evidence

The Board also found that Hiraishi’s FIFO circuit does not “act[] to ‘delay a signal through the data path’ in Hiraishi’s read leveling process.” Appx64. Again, however, the Board’s finding is inconsistent with the ’035 Final Written Decision, which found that the “*read* and write *leveling circuits* of Osanai[/Hiraishi] mak[e] timing *adjustments [to] data* and strobe signals associated with read and write operations,” Appx6736, and “teach controlling the timing of the data and strobe signals on the data paths [L0 to L1/L2, which goes through the FIFO] on which those signals travel,” Appx6737; *see also* Appx6736 (“data paths connect lines L0 to lines L1 and L2”).

Citing only two paragraphs from Hiraishi discussing read leveling, the Board concluded that “Hiraishi’s read leveling adjusts the activation timing of the *input buffers [INB]* and is not related to the FIFO.” Appx64-65. That finding is inconsistent with the ’035 Final Written Decision. In the ’035 IPR, the petitioner never relied on the input buffers (INB). *See* Appx6716-22 (“Summary of Petitioner’s Contentions”), Appx6724 (“We agree with and adopt Petitioner’s contentions”). Without relying on the INB input buffer, the Board agreed with the petitioner’s contention that the “read and write leveling circuits of Osanai[/Hiraishi] making timing adjustments [to] data and strobe signals

associated with read and write operations.” Appx6736. In response, Netlist argued to the Board that “Osanai[/Hiraishi]’s read leveling process delays the internal signals that turn on Osanai[/Hiraishi]’s **input buffers INB** rather than controlling the timing of the read data and strobe signals themselves.” Appx6735. But the Board **rejected** Netlist’s argument. Appx6736-37 (“[W]e disagree with Patent Owner’s argument”).

The Board’s conclusion here that Hiraishi’s Read FIFO circuit does not delay the DQ data signal as a result of read leveling lacks substantial evidence and is contrary to the record. Hiraishi expressly teaches that “[t]he leveling operation is to adjust . . . a read timing in consideration of a propagation time [i.e., Flight Time] of a signal. The adjustment of the . . . read timing is performed by a read leveling operation.” Appx870 ¶ 140. Hiraishi also expressly teaches using the Read FIFO to make these timing adjustments:

[T]here occurs a predetermined time difference (**Flight Time**) between a timing at which the read data DQ and the data strobe signal DQS are output from the memory chip 200 and a timing at which the read data DQ and the data strobe signal DQS are input to the data register buffer 300.

Thereafter, the data register buffer 300 performs a **re-timing** in synchronization with the internal clock LCLKR **using the FIFO (Read) circuit 302** to convert CL into CL=6, and outputs the read data DQ and the data strobe signal DQS. With this configuration, it becomes possible for the memory controller to receive the read data DQ in a correct manner.

Appx869 ¶¶ 129-30. Figure 11 shows this “Re-Timing” (performed by the Read FIFO as explained directly above) to account for the “Flight Time” delay measured during read leveling so that the DQ(OUT) data signal is properly aligned with the CK clock signal at time T6:

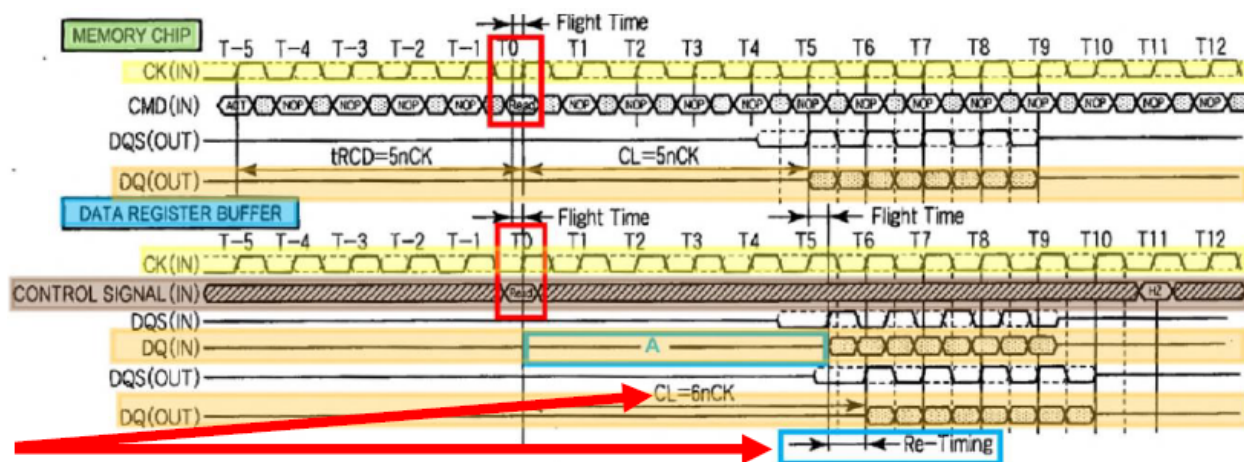


FIG. 11

Appx10214; Appx188-89 (annotating Appx843).

* * * * *

The Board’s findings above are inconsistent with and precluded by the ’035 Final Written Decision and lack substantial evidence. The Court should therefore vacate and remand to the Board to reconsider Ground 1, regardless of how the Court construes “*data path*.”

V. The Board Never Addressed Samsung’s Alternative Combination Under Ground 2 That a “Delay Circuit” in the “Data Path” Is Disclosed Even Under Netlist’s Narrow Construction

Regardless of the construction of “*data path*,” and independent of all the other errors discussed above, the Board also erred when it ignored Samsung’s alternative

combination for Ground 2 teaching a “*delay circuit*” in the “*data path*” even under Netlist’s narrow construction for “*data path*.” Specifically, Samsung’s Petition stated: “Alternatively, delay elements similar to Tokuhiro’s DR elements can be used ***instead of*** . . . Hiraishi’s FIFO circuit for ***delaying the read data***.” Appx230; Appx782-85 ¶ 262. In this alternative combination for Ground 2, Tokuhiro’s delay circuit would be physically on the DQ data line and delay the data signal, thereby satisfying even Netlist’s narrow construction for a “*delay circuit*” in the “*data path*.” Appx10303.

Indeed, the Board already adopted a combination in the ’035 IPR very similar to this alternative combination for Ground 2: “Petitioner is not required to physically incorporate Tokuhiro’s variable delay circuits DR1 and DR2 into Osanai[/Hiraishi]. Instead, Petitioner proposes to utilize Tokuhiro’s teaching of determining the delay for read operations based on the delay calculated during a prior write leveling operation.” Appx6741. Similarly, here, a POSITA would have understood how to modify or replace Hiraishi’s FIFO circuit with Tokuhiro’s teachings of a delay circuit. Netlist’s expert, Dr. Mangione-Smith, admitted as much:

Q. And would it be fair to say that a person of ordinary skill in the art knew how to delay a data or strobe signal by a predetermined amount?

A. Yes, I think that’s fair to say, in general.

Appx9006 (164:14-18).

The Board provided no explanation for ignoring this alternative combination for Ground 2. Samsung expressly made this argument in its Petition as discussed above, Appx230, and then again in its Reply, arguing that “Ground 2 satisfies even Netlist’s unreasonably narrow claim constructions” and that “Netlist completely ignores the alternative combination for Ground 2.” Appx10502. Samsung also raised this argument during the oral hearing. See Appx10301-03, Appx10306-07; Appx10435-36 (48:25-49:8) (discussing Netlist’s attempt to relitigate issues determined in the ’035 IPR related to Samsung’s alternative combination under Ground 2). The Board never addressed this alternative combination for Ground 2 in its Final Written Decision, however. See Appx68-70. Therefore, the Court should, at minimum, remand Ground 2 to the Board to address Samsung’s alternative combination, regardless of the Court’s disposition on claim construction and the other errors discussed above.

CONCLUSION

The Board’s decision should be vacated and remanded.

Dated: April 18, 2025

Respectfully submitted,

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FORM 19. Certificate of Compliance with Type-Volume Limitations

Form 19
July 2020

**UNITED STATES COURT OF APPEALS
FOR THE FEDERAL CIRCUIT**

CERTIFICATE OF COMPLIANCE WITH TYPE-VOLUME LIMITATIONS

Case Number: 2025-1378

Short Case Caption: Samsung Electronics Co., Ltd. v. Netlist, Inc.

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Date: 04/18/2025

Signature: /s/ Michael Hawes

Name: Michael Hawes