PTO/AIA/15 (10-17)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	022955-000090
First Named Inventor	Chi-She Chen, et al.
Title	FLASH-DRAM HYBRID MEMORY MODULE
Priority Mail Express® Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. ☐ **Fee Transmittal Form** (PTO/SB/17 or equivalent)
2. ☐ **Applicant asserts small entity status.** See 37 CFR 1.27
3. ☐ **Applicant certifies micro entity status.** See 37 CFR 1.29. Applicant must attach form PTO/SB/15A or B or equivalent.
4. ☑ **Specification** [*Total Pages* 77] Both the claims and abstract must start on a new page. *(See MPEP § 608.01(a) for information on the preferred arrangement)*
5. ☑ **Drawing(s)** (35 U.S.C. 113) [*Total Sheets* 22]
6. **Inventor's Oath or Declaration** [*Total Pages* 4] *(including substitute statements under 37 CFR 1.64 and assignments serving as an oath or declaration under 37 CFR 1.63(e))*
   a. ☐ Newly executed (original or copy)
   b. ☑ A copy from a prior application (37 CFR 1.63(d))
7. ☑ **Application Data Sheet** ** See note below.* See 37 CFR 1.76 (PTO/AIA/14 or equivalent)
8. **CD-ROM or CD-R** in duplicate, large table, or Computer Program (*Appendix*)
   ☐ Landscape Table on CD
9. **Nucleotide and/or Amino Acid Sequence Submission** (*if applicable, items a. – c. are required*)
   a. ☐ Computer Readable Form (CRF)
   b. ☐ Specification Sequence Listing on:
      i. ☐ CD-ROM or CD-R (2 copies); or
      ii. ☐ Paper
   c. ☐ Statements verifying identity of above copies

ADDRESS TO:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

ACCOMPANYING APPLICATION PAPERS

10. ☐ **Assignment Papers** (cover sheet & document(s))
    Name of Assignee _____
11. ☐ **37 CFR 3.73(c) Statement** (*when there is an assignee*) ☑ **Power of Attorney**
12. ☐ **English Translation Document** (*if applicable*)
13. ☐ **Information Disclosure Statement** (PTO/SB/08 or PTO-1449)
    ☐ Copies of citations attached
14. ☑ **Preliminary Amendment**
15. ☐ **Return Receipt Postcard** (*MPEP § 503*) (*Should be specifically itemized*)
16. ☐ **Certified Copy of Priority Document(s)** (*if foreign priority is claimed*)
17. ☐ **Nonpublication Request** Under 35 U.S.C. 122(b)(2)(B)(i). Applicant must attach form PTO/SB/35 or equivalent.
18. ☐ **Other:** _____

***Note**: (1) Benefit claims under 37 CFR 1.78 and foreign priority claims under 1.55 **must** be included in an Application Data Sheet (ADS).
(2) For applications filed under 35 U.S.C. 111, the application must contain an ADS specifying the applicant if the applicant is an assignee, person to whom the inventor is under an obligation to assign, or person who otherwise shows sufficient proprietary interest in the matter. See 37 CFR 1.46(b).

19. CORRESPONDENCE ADDRESS

☑ The address associated with Customer Number: 151145 **OR** ☐ Correspondence address below

Name					
Address					
City		State		Zip Code	
Country		Telephone		Email	

Signature	/Khaled Shami/	Date	January 24, 2022
Name (Print/Type)	Khaled Shami	Registration No. (Attorney/Agent)	38745

This collection of information is required by 37 CFR 1.53(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	44819531
Application Number:	17582797
International Application Number:	
Confirmation Number:	3546
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000090
Receipt Date:	24-JAN-2022
Filing Date:	
Time Stamp:	17:11:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	261304 30ebf733d33f0f76d66b665610463e482bc026ec	no	9

Warnings:

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Information:					
2		022955-000090_Appl_Text.pdf	638118 25e3644bd94b899a1ab5a2ca6849c07204c048bb	yes	77

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Specification	1	75
	Claims	76	76
	Abstract	77	77

Warnings:					
Information:					
3	Oath or Declaration filed	022955-000090_Inventors_Oath.PDF	372159 f091bc0e76caebbd5677e65b65d09f9c9b91d709	no	4
Warnings:					
Information:					
4		022955-000090_PA_ConApp.pdf	369499 caa2f8c64291b78a46631b0b21b311961a81f9ec	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3

Warnings:					
Information:					
5	Power of Attorney	022955-000090_SignedPOA.PDF	144453 352febe72ca1aa53e1537cb9c39def3fd9480d79	no	1
Warnings:					
Information:					

6	Drawings-only black and white line drawings	022955-000090_Appl_Drawings_ForFiling.pdf	6452231 f25d28133d2a7a6c4efa22b0fe87e19f4c69aaf2	no	22
Warnings:					
Information:					
7	Transmittal of New Application	022955-000090_NewAppTransmittal_aia0015.pdf	282121 393d79d68ded9f915027833dbb026297133b0b3c	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	8519885		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Walnut	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	944 Crystal Water Lane		
Address 2			
City	Walnut	State/Province	CA
Postal Code	91789	Country i	US

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	6 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country i	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Scott	H.	Milton	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	49 Statehouse Place		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92602	**Country** i	US

Inventor 4

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Jayesh		Bhakta	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Cerritos	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	**State/Province**	CA
Postal Code	90703	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	151145		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	022955-000090	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	22	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	151145		

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

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Ex. 1002, p. 8

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17328019	2021-05-24

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17328019	Continuation of	17138766	2020-12-30	11016918	2021-05-25

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
17138766	Continuation of	15934416	2018-03-23

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15934416	Continuation of	14840865	2015-08-31	9928186	2018-03-27

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13559476	Claims benefit of provisional	61512871	2011-07-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:	

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Applicant:

Address 1	111 Academy Way		
Address 2	Suite 100		
City	Irvine	**State/Province**	CA
Country[i] US		Postal Code	92617
Phone Number	US	Fax Number	
Email Address			

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

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Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

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First Name	Khaled	Last Name	Shami	Registration Number	38745

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FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 17/138,766, filed December 30, 2020, titled "Flash-Dram Hybrid Memory", now U.S. Patent No. 11,016918, which is a continuation of U.S. Patent Application No 15/934,416, filed March 23, 2018, titled "Flash-Dram Hybrid Memory Module," which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled "Non-Volatile Memory Module," now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

[0002] This application may be considered related to U.S. Patent Application No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed February 5, 2014, which is a continuation of U.S. Patent Application 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Patent 8,677,060, issued

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March 18, 2014, which is a continuation of U.S. Patent Application 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed June 28, 2012, now U.S. Patent 8,516,187, issued August 20, 2013, which is a divisional of U.S. Patent Application 12/240,916, titled "Non-Volatile Memory Module," filed September 29, 2008, now U.S. Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007, the contents of which are incorporated by reference herein in their entirety.

[0003] This application may also be considered related to U.S. Patent Application No. 15/000,834, filed January 19, 2016 (abandoned), which is a continuation of U.S. Patent Application No. 14/489,332, filed September 17, 2014, now U.S. Patent No. 9,269,437, which is a continuation of U.S. Patent Application No. 14/173,219, filed February 5, 2014, now U.S. Patent No. 8,904,099, which is a continuation of U.S. Patent Application No. 13/905,048, filed May 29, 2013, now U.S. Patent No. 6,671,243, which is a continuation U.S. Patent Application 13/536,173 above.

[0004] This application may also be considered related to U.S. Patent Application No. 15/924,866, (abandoned), which is a continuation of U.S. Patent Application No. 14/489,281, filed September 17, 2014, now U.S. Patent No. 9,921,762, which is a continuation of U.S. Patent Application No. 13/625,563, filed September 24, 2012, now U.S. Patent No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed September 23, 2011.

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TECHNICAL FIELD

[0005] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0006] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0007] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as 'finance transactions' (for example, point-of-service, inter-bank transaction, stock market transaction), 'scientific computation' (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), 'medical diagnostics' (for example, diagnostics based on the fuzzy logic, medical data processing), 'simple information sharing and searching' (for example, web search, retail store website, company home page), 'email' (information distribution and archive), 'security service', 'entertainment' (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high

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speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0008] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0009] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM . The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a

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data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MBs for the EcoRAM vs. 104MBs for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™), which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0010] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0011] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash

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DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0012] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

[0013] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0014] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

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[0015] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

[0016] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0017] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

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subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0018] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0019] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0020] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0021] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

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[0022] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0023] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0024] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0025] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0026] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0027] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0028] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

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[0029] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0030] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0031] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0032] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0033] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0034] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

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[0035] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0036] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0037] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0038] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0039] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0040] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

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[0041] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0042] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0043] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0044] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0045] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0046] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

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[0047] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0048] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0049] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0050] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0051] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0052] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0053] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

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[0054] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0055] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0056] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0057] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0059] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

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[0060] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0061] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0062] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0063] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0064] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0065] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

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commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0066] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0067] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0068] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0069] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

[0070] Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to

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allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

[0071] Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

[0072] Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

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BRIEF DESCRIPTION OF THE DRAWINGS

[0073] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0074] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

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FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. 12 is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. 13 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. 14 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. 15A-15C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. 16 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

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FIG. 17 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. 18 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. 19 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. 20 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. 22 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0075] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to

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implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0076] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0077] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only

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Memory), EEPROM (Electrically Eraseable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0078] The term "exemplary" where used herein is intended to mean "serving as an example, instance or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0079] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0080] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

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[0081] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0082] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or

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commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0083] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

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[0084] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0085] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400'supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then

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the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0086] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0087] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0088] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory

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module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0089] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In

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the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0090] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0091] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH

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510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0092] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0093] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the

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DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0094] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0095] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate

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and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0096] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0097] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or

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provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received form MCH 510.

[0098] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0099] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[00100] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

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[00101] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash–DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[00102] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 506 and the other for the DRAM memory DRAM 508. The MCH treats the DRAM 508 and Flash 506 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash 506 and DRAM 508 allows for direct data transfer to occur between the Flash 506 and the DRAM 508 in response to control information from Ctrl 502. In this embodiment, this data transfer mechanism provides direct support for executing commands from

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the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 506 to the DRAM 508. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[00103] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

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[00104] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[00105] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a

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first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[00106] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

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[00107] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[00108] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502

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monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00109] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1061

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field, a Block address 1051 field, a Plane address 1041, a Page address 1031, and a group of least significant address bits A_0A_1 1021. The Plane address 1041 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00110] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00111] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400μs, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash

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memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00112] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

((#of blocks per bank)/(ratio of 'Flash_block_write_time' to 'Flash_read_time'))*(
(Block usage time)/('Flash_block_write_time'))

[00113] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00114] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00115] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up

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the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[00116] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by th controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[00117] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor

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array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[00118] In certain embodiments, the power module. transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[00119] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or. reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[00120] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[00121] FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory

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subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.

[00122] In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 10 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for

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example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[00123] In certain preferred embodiments, the memory system 1010 is in electrical communication with the host system. In other embodiments, the memory system 1010 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system 1010 can be in communication with a disk controller of a computer system, for example. The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.

[00124] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem 1040 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 1030. In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and

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synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00125] In certain embodiments, the second plurality of non-volatile memory elements 1042 comprises one or more flash memory elements. Types of flash memory elements 1042 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. 12, the second memory bank 1040 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 1042. In addition, nonvolatile memory elements 1042 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 1042 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00126] FIG. 13 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 1030 with nine volatile memory elements

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1032 and a non-volatile memory subsystem 1040 with five non-volatile memory elements 1042 in accordance with certain embodiments described herein. The additional memory element 1032 of the first memory bank 1030 and the additional memory element 1042 of the second memory bank 1040 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 1030 comprises other numbers of volatile memory elements 1032 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 1040 comprises other numbers of nonvolatile memory elements 1042 (e.g., 2, 3, more than 5).

[00127] Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one

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embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.

[00128] In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system.

[00129] In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one

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or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150.

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash "mirror" to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10

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percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[00131] As schematically illustrated by FIGS. 12 and 13, in certain embodiments, the controller 1062 may comprise a microcontroller unit (MCU) 1060 and a logic element 1070. In certain embodiments, the MCU 1060 provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 and the nonvolatile memory subsystem 1040. The MCU 1060 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. 12 and 13, the logic element 1070 of certain embodiments is in electrical communication with the non-volatile memory subsystem 1040 and the MCU 1060. The logic element 1070 can provide signal level translation between the volatile memory elements 1032 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 1042 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 1070 is also programmed to perform address/address translation between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 1042 because of their superior read speed and compact structure.

[00132] The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the

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volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[00133] The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.

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[00134] The isolation or operational decoupling of the volatile memory subsystem 1030 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 1010 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 1030. For example, in one embodiment during such periods of operation, the controller 1062 and the nonvolatile memory subsystem 1040 do not add a significant capacitive load to the volatile memory system 1030 when the memory system 1010 is in the first state. In certain such embodiments, the capacitive load of the controller 1062 and the non-volatile memory subsystem 1040 do not significantly affect the signals propagating between the volatile memory subsystem 1030 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 1052 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 1052 comprises other types of isolation devices.

[00135] Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. In certain embodiments, the memory system 1010 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 1010 enters the second state in response to a trigger condition. In certain embodiments, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory

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subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.

[00136] In certain embodiments, the second power supply 1080 does not comprise a battery. Because a battery is not used, the second power supply 1080 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. 12-14, the second power supply 1080 comprises a step-up transformer 1082, a step-down transformer 1084, and a capacitor bank 1086 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 1080 is configured to power the volatile memory subsystem 1030 for less than thirty minutes. In certain embodiments, the second power supply 1080 may comprise a battery. For example, in certain embodiments, the second power supply 1080 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 1030 for no more than thirty minutes.

[00137] In certain embodiments, the capacitor bank 1086 of the second power supply 1080 is charged by the first power supply while the memory system 1010 is in the first state. As a result, the second power supply 1080 is fully charged when the memory system 1010 enters the second state. The memory system 1010 and the second power supply 1080 may be located on the same printed circuit board 1020. In other embodiments, the second power supply 1080 may not be on

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the same printed circuit board 1020 and may be tethered to the printed circuit board 1020, for example.

[00138] When operating in the first state, in certain embodiments, the step-up transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the step-down transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. 12-14, the memory module 1010 further comprises a switch 1090 (e.g., FET switch) that switches power provided to the controller 1062, the volatile memory subsystem 1030, and the non-volatile memory subsystem 1040, between the power from the second power supply 1080 and the power from the first power supply (e.g., system power) received via the interface 1022. For example, the switch 1090 may switch from the first power supply to the second power supply 1080 when the voltage monitor 1050 detects a low voltage condition. The switch 1090 of certain embodiments advantageously ensures that the volatile memory elements 1032 and non-volatile memory elements 1042 are powered long enough for the data to be transferred from the volatile memory elements 1032 and stored in the non-volatile memory elements 1042. In certain embodiments, after the data transfer is complete, the switch 1090 then switches back to the first power supply and the controller 1062 transmits a signal to the at least one circuit 1052 to operatively decouple the controller 1062 from the volatile memory subsystem 1030, such that the memory system 1010 reenters the first state.

[00139] When the memory system 1010 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 via the

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controller 1062. The host system can then resume accessing the volatile memory subsystem 1030 of the memory module 1010. In certain embodiments, after the memory system 1010 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 1030 rather than the non-volatile memory subsystem 1040 because the volatile memory elements 1032 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 1030 to the nonvolatile memory bank 1040, or from the non-volatile memory bank 1040 to the volatile. memory bank 1030, takes less than one minute per GB.

[00140] In certain embodiments, the memory system 1010 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 1010 copies the entire contents of the volatile memory subsystem 1030 into the nonvolatile memory subsystem 1040 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are copied back into the volatile memory subsystem 1030 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 1040 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 1010. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 1010 and can improve the performance of the memory system 1010. In certain other embodiments, the entire contents of the volatile memory subsystem 1030 are not copied into the non-volatile memory subsystem 1040 on each backup operation, but only a partial copy is performed. In certain embodiments, other

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management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 1040 are performed in the controller 1062.

[00141] The memory system 1010 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 1030 which then writes the data to non-volatile storage which is not part of the memory system 1010, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 1010 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 1010 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 1010 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 1010 may be operated as a write-through cache or as some other type of cache.

[00142] FIG. 16 schematically illustrates an example power module 1100 of the memory system 1010 in accordance with certain embodiments described herein. The power module 1100 provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. In certain embodiments, the power module 1100 comprises one or more of the components described above with respect to FIG. 12. For example, in certain embodiments, the power module 1100 includes the second power supply 1080 and the switch 1090.

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[00143] The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110.

[00144] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106.

[00145] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element

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1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120.

[00146] In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.

[00147] In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For

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example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142.

[00148] The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate

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amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.

[00149] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.

[00150] FIG. 17 is a flowchart of an example method 1200 of providing a first voltage 1102 and a second voltage 1104 to a memory system 1010 including volatile and nonvolatile memory subsystems 1030, 1040. While the method 1200 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-15, other memory systems are also compatible with embodiments of the method 1200. During a first condition, the method 1200

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comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 and providing the second voltage 1104 to the memory system 1010 from a first power subsystem in operational block 1210. For example, in one embodiment, the first power subsystem comprises the first power element 1130 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, other first power subsystems are used.

[00151] The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.

[00152] The method 1200 further comprises charging a second power subsystem in operational block 1240. In certain embodiments, the second power subsystem comprises the second power element 1140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 1140 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, some other second power subsystem is used.

[00153] The method 1200 further comprises detecting a third condition in an operational block 1250 and during the third condition, providing the first voltage 1102 and the second

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voltage 1104 to the memory system 1010 from the second power subsystem 1140 in an operational block 1260. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 1200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 1140 is charged before detecting the second condition.

[00154] In certain embodiments, the memory system 1010 comprises a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 1010 also comprises a controller 1062 operatively coupled to the volatile memory subsystem 1030 and operatively coupled to the non-volatile memory subsystem 1040. The controller 1062 can be configured to allow data to be communicated between the volatile memory subsystem 1030 and the host system when the memory system 1010 is operating in a first state and to allow data to be communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040 when the memory system 1010 is operating in a second state.

[00155] Although the memory system 1010 having extra storage capacity of the non-volatile memory subsystem 1040 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In various embodiments, there may be at least 200, 300, or 400 percent more

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storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In other embodiments, the non-volatile memory subsystem 1040 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 1030. In some embodiments, the non-volatile memory subsystem 1040 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 1030. In one embodiment, the non-volatile memory subsystem 1040 includes less than 100 percent more storage capacity than does the volatile memory subsystem 1030.

[00156] The extra storage capacity of the non-volatile memory subsystem 1040 can be used to improve the backup capability of the memory system 1010. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 1040 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem 1040 allows the volatile memory subsystem 1030 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to backup the volatile memory subsystem 1030 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 1030 is copied to a first, previously erased portion of the nonvolatile memory subsystem 1040 via the controller 1062. Since the non-volatile memory subsystem 1040 has more storage capacity than does the volatile memory subsystem 1030, there is a second portion of the non-volatile memory subsystem 1040 which does not have data from the volatile memory subsystem 1030 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 1062 of the memory system 1010 restores the data to the volatile memory subsystem 1030 by copying the backed-up data from the non-volatile memory

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subsystem 40 back to the volatile memory subsystem 1030. After the data is restored, the memory system 1010 erases the non-volatile memory subsystem 1040. While the first portion of the non-volatile memory subsystem 1040 is being erased, it may be temporarily unaccessible.

[00157] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 1040 is completely erased, the volatile memory subsystem 1030 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 1040 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 1040, the memory system 1010 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 1040.

[00158] FIG. 18 is a flowchart of an example method 1300 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. In certain embodiments, the non-volatile memory subsystem 1040 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 1300 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-14, the method 1300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 1310, the method 1300 comprises communicating data between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation. The method 1300 further comprises storing a first copy of data from the

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volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a first time when the memory system 1010 is in a second mode of operation in an operational block 1320.

[00159] In an operational block 1330, the method 1300 comprises restoring the first copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030. The method 1300 further comprises erasing the first copy of data from the non-volatile memory subsystem 1040 in an operational block 1340. The method further comprises storing a second copy of data from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a second time when the memory system 1010 is in the second mode of operation in an operational block 1350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 1040.

[00160] In some embodiments, the memory system 1010 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 1040. The method 1300 can also include restoring the second copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 in an operational block 1360. The operational blocks of method 1300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem 1030 at operational block 1360 before the first copy of data is completely erased in the operational block 1340.

[00161] FIG. 19 schematically illustrates an example clock distribution topology 1400 of a memory system 1010 in accordance with certain embodiments described herein. The clock

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distribution topology 1400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 1010. A clock source 1402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 1402 may feed a clock generator 1404 which provides a clock signal 1406 to the controller 1062, which may be an FPGA. In one embodiment, the clock generator 1404 generates a 125 MHz clock signal 1406. The controller 1062 receives the clock signal 1406 and uses it to clock the controller 1062 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 1062.

[00162] The clock signal 1406 can also be input into a clock divider 1410 which produces a frequency-divided version of the clock signal 1406. In an example embodiment, the clock divider 1410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 1406. A non-volatile memory phase-locked loop (PLL) block 1412 can be included (e.g., in the controller 1062) which distributes a series of clock signals to the non-volatile memory subsystem 1040 and to associated control logic. For example, a series of clock signals 1414 can be sent from the controller 1062 to the non-volatile memory subsystem 1040. Another clock signal 1416 can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem 1040. For example, the clock signal 1416 may clock the portion of the controller 1062 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 1040. A feedback clock signal 1418 is fed back into the non-volatile memory PLL block 1412. In one embodiment, the PLL block 1412 compares the feedback clock 1418 to the reference clock 1411 and varies the phase and frequency of its output until the reference 1411 and feedback 1418 clocks are phase and frequency matched.

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[00163] A version of the clock signal 1406 such as the backup clock signal 1408 may be sent from the controller to the volatile memory subsystem 1030. The clock signal 1408 may be, for example, a differential version of the clock signal 1406. As described herein, the backup clock signal 1408 may be used to clock the volatile memory subsystem 1030 when the memory system 1010 is backing up the data from the volatile memory subsystem 1030 into the non-volatile memory subsystem 1040. In certain embodiments, the backup clock signal 1408 may also be used to clock the volatile memory subsystem 1030 when the memory system 1010 is copying the backed-up data back into the volatile memory subsystem 1030 from the nonvolatile memory subsystem 1040 (also referred to as restoring the volatile memory subsystem 1030). The volatile memory subsystem 1030 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the nonvolatile memory subsystem 1040 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 1030 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 1030 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 1010.

[00164] In one embodiment, the backup clock 1408 and the volatile memory system clock signal 1420 are received by a multiplexer 1422, as schematically illustrated by FIG. 19. The multiplexer 1422 can output either the volatile memory system clock signal 1420 or the backup clock signal 1408 depending on the backup state of the memory system 1010. For example, when the memory system 1010 is not performing a backup or restore operation and is

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communicating with the host system (e.g., normal operation), the volatile memory system clock signal 1420 may be provided by the multiplexer 422 to the volatile memory PLL block 1424. When the memory system 1010 is performing a backup (or restore) operation, the backup clock signal 1408 may be provided.

[00165] The volatile memory PLL block 1424 receives the volatile memory reference clock signal 1423 from the multiplexer 1422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 1030 and associated control logic. For example, in one embodiment, the PLL block 1424 generates a series of clock signals 1426 which clock the volatile memory elements 1032. A clock signal 1428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal 1430 may be sent to the controller 1062. A feedback clock signal 1432 is fed back into the volatile memory PLL block 1424. In one embodiment, the PLL block 1424 compares the feedback clock signal 1432 to the reference clock signal 1423 and varies the phase and frequency of its output until the reference clock signal 1423 and the feedback clock signal 1432 clocks are phase and frequency matched.

[00166] The clock signal 1430 may be used by the controller 1062 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 1030. For example, control logic in the controller 1062 may be used to control the volatile memory subsystem 1030 during a backup or restore operation. The clock signal 1430 may be used as a reference clock signal for the PLL block 1434 which can generate one or more clocks 1438 used by logic in the controller 1062. For example, the PLL block 1434 may generate one or more clock signals 1438 used to drive logic circuitry associated with

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controlling the volatile memory subsystem 1030. In certain embodiments, the PLL block 1434 includes a feedback clock signal 1436 and operates in a similar manner to other PLL blocks described herein.

[00167] The clock signal 1430 may be used as a reference clock signal for the PLL block 1440 which may generate one or more clock signals used by a sub-block 1442 to generate one or more other clock signals 1444. In one embodiment, for example, the volatile memory subsystem 1030 comprises DDR2 SDRAM elements and the sub-block 1442 generates one or more DDR2 compatible clock signals 1444. A feedback clock signal 1446 is fed back into the PLL block 1440. In certain embodiments, the PLL block 1440 operates in a similar manner to other PLL blocks described herein.

[00168] While described with respect to the example embodiment of FIG. 19, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 1030 operates on the volatile memory clock signal 1420 and there is no backup clock signal 1408. In some embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a restore operation and not during a backup operation.

[00169] FIG. 20 is a flowchart of an example method 1500 of controlling a memory system 1010 operatively coupled to a host system. Although described with respect to the memory

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system 1010 described herein, the method 1500 is compatible with other memory systems. The memory system 1010 may include a clock distribution topology 1400 similar to the one described above with respect to FIG. 19 or another clock distribution topology. The memory system 1010 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 1040.

[00170] In an operational block 1510, the method 1500 comprises operating the volatile memory subsystem 1030 at a first frequency when the memory system 1010 is in a first mode of operation in which data is communicated between the volatile memory subsystem 1030 and the host system. In an operational block 1520, the method 1500 comprises operating the non-volatile memory subsystem 1040 at a second frequency when the memory system 1010 is in a second mode of operation in which data is communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. The method 1500 further comprises operating the volatile memory subsystem 1030 at a third frequency in an operational block 1530 when the memory system 1010 is in the second mode of operation. In certain embodiments, the memory system 1010 is not powered by a battery when it is in the second mode of operation. The memory system 1010 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

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[00171] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 1010.

[00172] FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062. In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 1630, 1640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice

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from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[00173] In certain embodiments, the switches 1650, 1652 can each be selectively switched to selectively operatively couple the data lines 1632, 1642, respectively from the first and second DRAM segments 1630, 1640 to the controller 1062. The chip select lines 1634, 1644 enable the first and second DRAM segments 1630, 1640, respectively, of the volatile memory subsystem 1030, and the self-refresh lines 1636, 1646 toggle the first and second DRAM segments 1630, 1640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[00174] In certain embodiments, when the memory system 1010 is backing up the volatile memory system 1030, data slices from only one of the two DRAM segments 1630, 1640 at a time are sent to the controller 1062. For example, when the first slice is being written to the controller 1062 during a back-up, the controller 1062 sends a signal via the CKe line 1636 to the first DRAM segment 1630 to put the first DRAM segment 1630 in active mode. In certain embodiments, the data slice from the first DRAM segment 1630 for multiple words (e.g., a block of words) is written to the controller 1062 before writing the second data slice from the second DRAM segment 1640 to the controller 1062. While the first data slice is being written to the controller 1062, the controller 1062 also sends a signal via the CKe line 1646 to put the second DRAM segment 1640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 1062, the controller 1062 puts the first DRAM segment 1630

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into self-refresh mode by sending a signal via the CKe line 1636 to the first DRAM segment 1640. The controller 1062 also puts the second DRAM segment 1640 into active mode by sending a signal via the CKe line 1646 to the DRAM segment 1640. The second slice for a word or for a block of words is written to the controller 1062. In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.

[00175] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1042 write each backed-up data word to the controller 1062 which writes a first slice of the data word to the volatile memory subsystem 1030 and then a second slice of the data word to the volatile memory subsystem 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00176] FIG. 22 is a flowchart of an example method 1600 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. Although described with respect to the memory system 1010 described herein with respect to FIGS. 12-14 and 21, the method 1600 is compatible with other memory systems. The method 1600 comprises communicating data words between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation in an operational block 1610. For example, the memory

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system 1010 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[00177] In an operational block 1620, the method further comprises transferring data words from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 when the memory system 1010 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.

[00178] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The

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40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[00179] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[00180] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1040 write each backed-up data word to the controller 1062 which writes a first portion of the data word to the volatile memory subsystem 1030 and then a second portion of the data word to the volatile memory 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00181] The method 1600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem 1030 comprises DRAM elements, only the slice of the DRAM which is currently being accessed

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(e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 1600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[00182] In addition, the connection between the DRAM elements and the controller 1062 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 1062 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 1062 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 1030. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[00183] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

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CLAIMS

What is claimed is:

1. A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;

a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;

a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;

a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and

a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:

a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and

at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein one of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes.

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ABSTRACT

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/489269

filed on September 17, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Chi-She Chen Date (Optional): Oct-17-2014

Signature: Chi-She Chen

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE

As the below named inventor, I hereby declare that:

This declaration is directed to:

☐ The attached application, or

☒ United States application or PCT international application number 14/489269

filed on September 17, 2014.

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

LEGAL NAME OF INVENTOR

Inventor: Jeffrey C. Solomon Date (Optional) :

Signature: Jeffrey C. Solomon

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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LEGAL NAME OF INVENTOR

Inventor: Scott H. Milton Date (Optional): 10/17/2014

Signature: Scott H. Milton

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

This collection of information is required by 35 U.S.C. 115 and 37 CFR 1.63. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 1 minute to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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filed on September 17, 2014.

The above-identified application was made or authorized to be made by me.

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LEGAL NAME OF INVENTOR

Inventor: Jayesh Bhakta Date (Optional): 9-17-2014

Signature: Jayesh Bhakta

Note: An application data sheet (PTO/SB/14 or equivalent), including naming the entire inventive entity, must accompany this form or must have been previously filed. Use an additional PTO/AIA/01 form for each additional inventor.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: TBA

SERIAL NO.: TBA ART UNIT: TBA

FILING DATE: TBA EXAMINER: TBA

TITLE: FLASH-DRAM HYBRID MEMORY MODULEY

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Commissioner:

Applicants respectfully request amendment of this application as directed herein.

Amendments to the Specification are discussed on page **2.**

Remarks begin on page **3**.

In the Specification

Please insert the following paragraph as the first paragraph, and renumber the subsequent paragraphs accordingly:

[0001] This application is a continuation of U.S. Patent Application No. 17/328,019, filed May 24, 2021, titled "FLASH-DRAM HYBRID MEMORY MODULE", now US Patent No. 11,232,054, which is a continuation of U.S. Patent Application No. 17/138,766, filed December 30, 2020, titled "Flash-Dram Hybrid Memory", now U.S. Patent No. 11,016918, which is a continuation of U.S. Patent Application No 15/934,416, filed March 23, 2018, titled "Flash-Dram Hybrid Memory Module," which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled "Non-Volatile Memory Module," now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 97

REMARKS

Entry of the foregoing amendment prior to substantive examination is respectfully requested. Claim 1 is pending.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Vorys, Sater, Seymour and Pease LLP
1909 K Street, N.W.
9th Floor
Washington, D.C. 20006
Phone: (202) 467-8860
Fax: (202) 467-8900

Respectfully submitted,

/Khaled Shami/
Khaled Shami
Reg. No. 38,745
Date: January 24, 2022

Samsung Electronics Co., Ltd.
Ex. 1002, p. 98

Doc Code: PA..
Document Description: Power of Attorney

PTO/AIA/82B (07-13)
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POWER OF ATTORNEY BY APPLICANT

I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

☑ I hereby appoint the Patent Practitioner(s) associated with the following Customer Number as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above: 151145

OR

☐ I hereby appoint Practitioner(s) named in the attached list (form PTO/AIA/82C) as my/our attorney(s) or agent(s), and to transact all business in the United States Patent and Trademark Office connected therewith for the patent application referenced in the attached transmittal letter (form PTO/AIA/82A) or identified above. (Note: Complete form PTO/AIA/82C.)

Please recognize or change the correspondence address for the application identified in the attached transmittal letter or the boxes above to:

☑ The address associated with the above-mentioned Customer Number

OR

☐ The address associated with Customer Number:

OR

☐ Firm or Individual Name					
Address					
City		State		Zip	
Country					
Telephone		Email			

I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Netlist, Inc.

☐ Inventor or Joint Inventor (title not required below)

☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)

☑ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)

☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature		Date (Optional)	10/5/19
Name	Noel S. Whitley		
Title	VP, IP & Licensing		

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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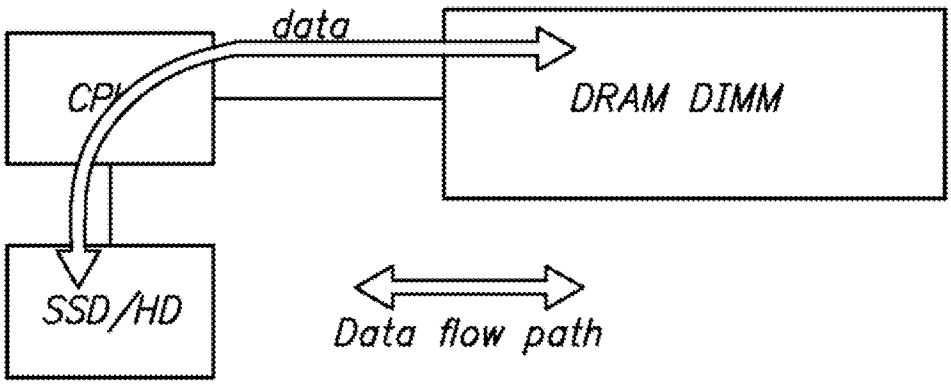


FIG. 1
(PRIOR ART)

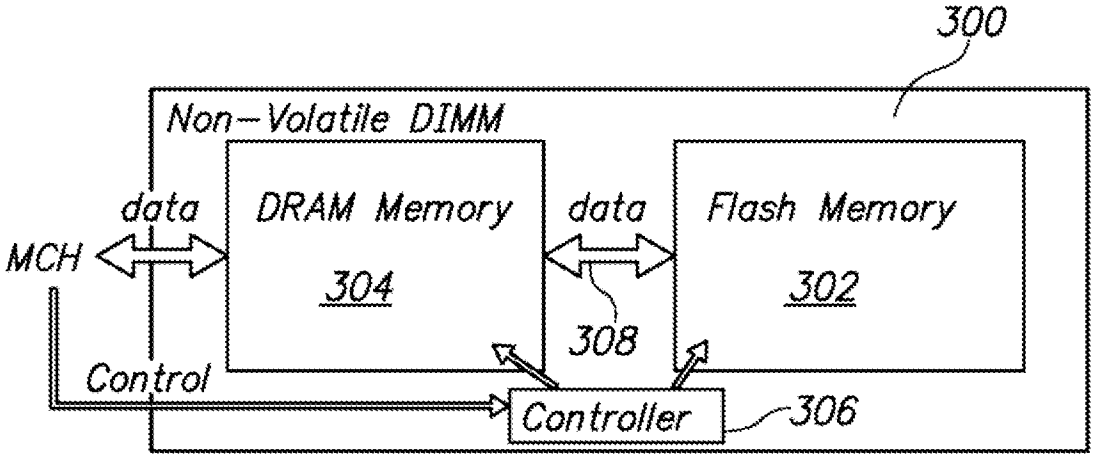
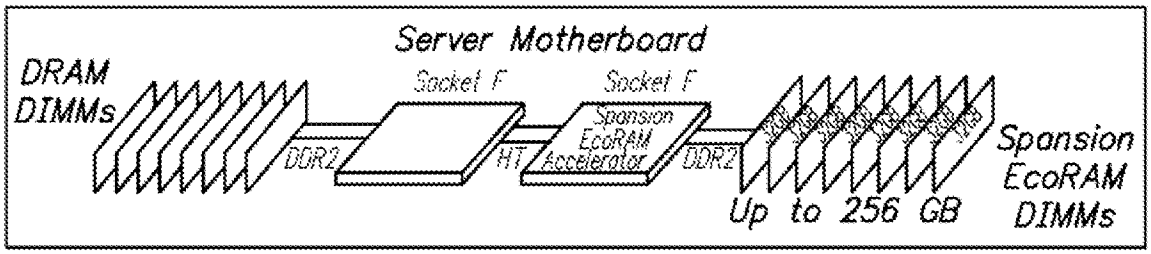


FIG. 3A

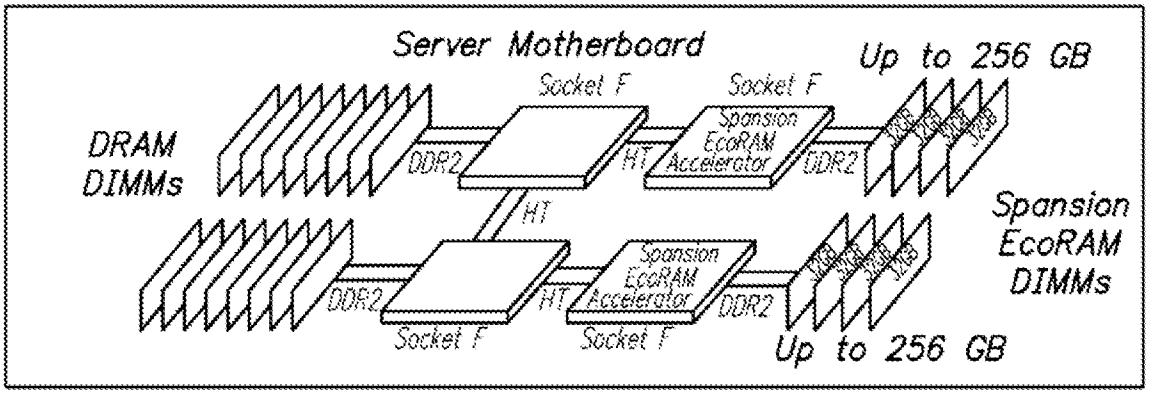
Spansion EcoRAM Configurations

256GB Spansion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

256GB Spansion EcoRAM Solution – Dual Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

FIG. 2
(PRIOR ART)

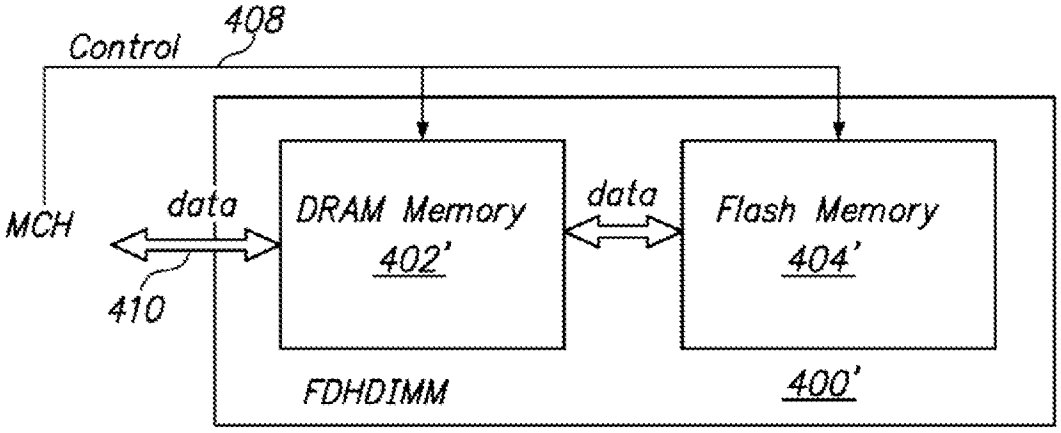


FIG. 4B

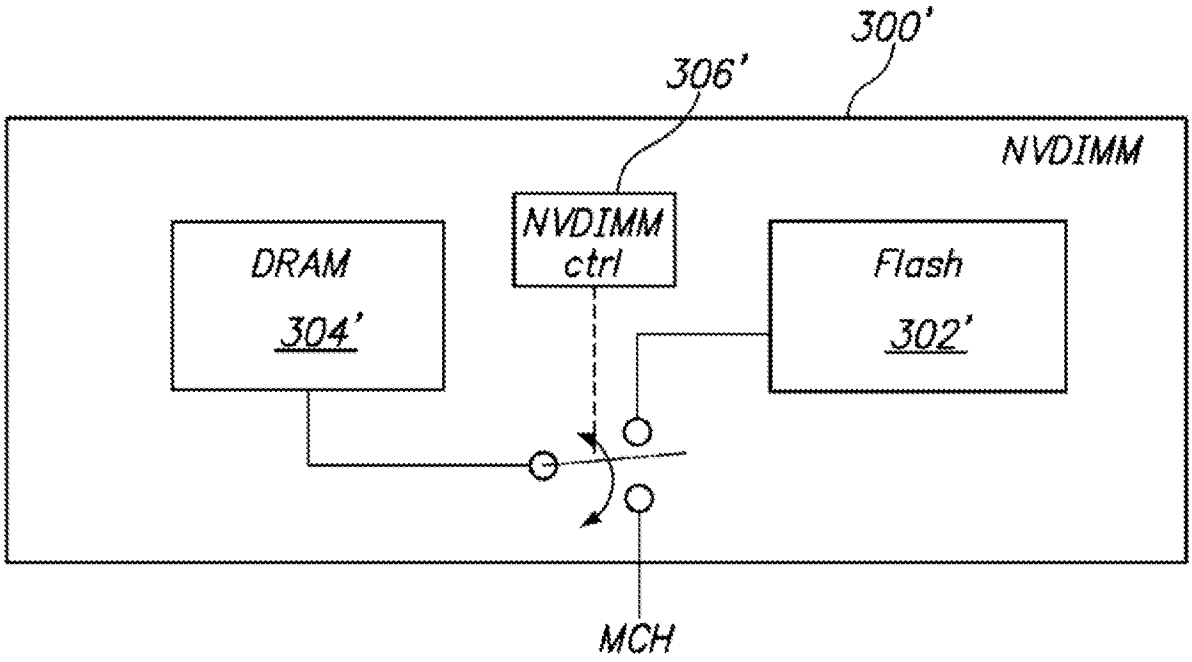

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

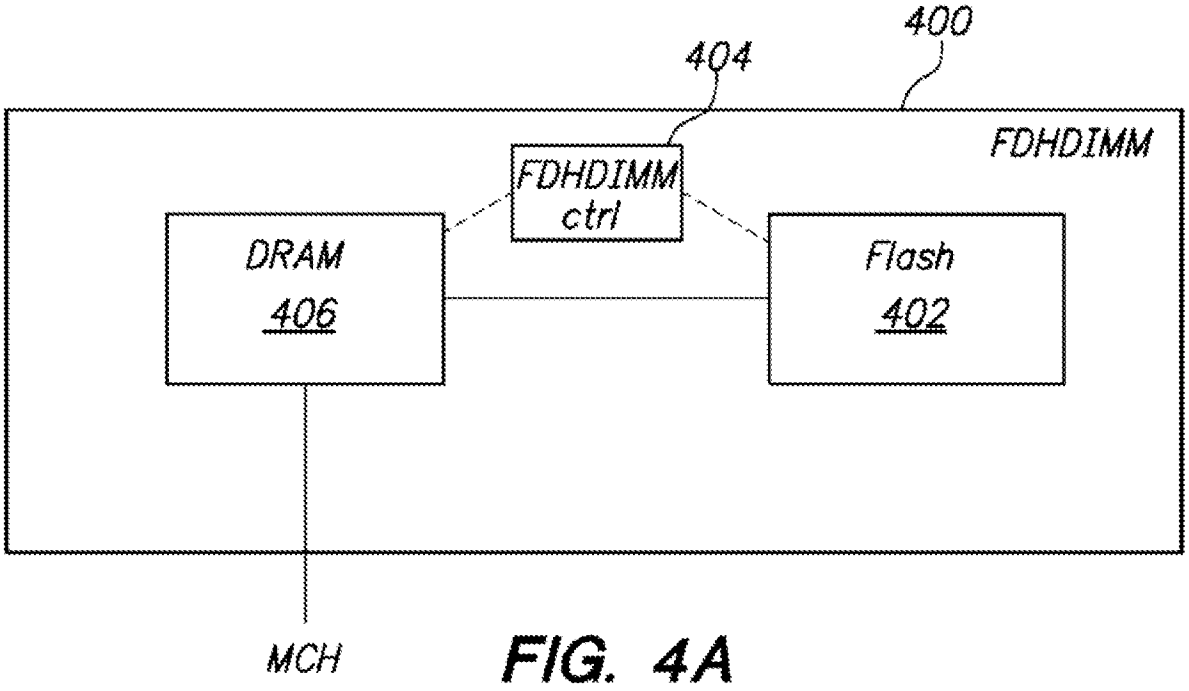

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

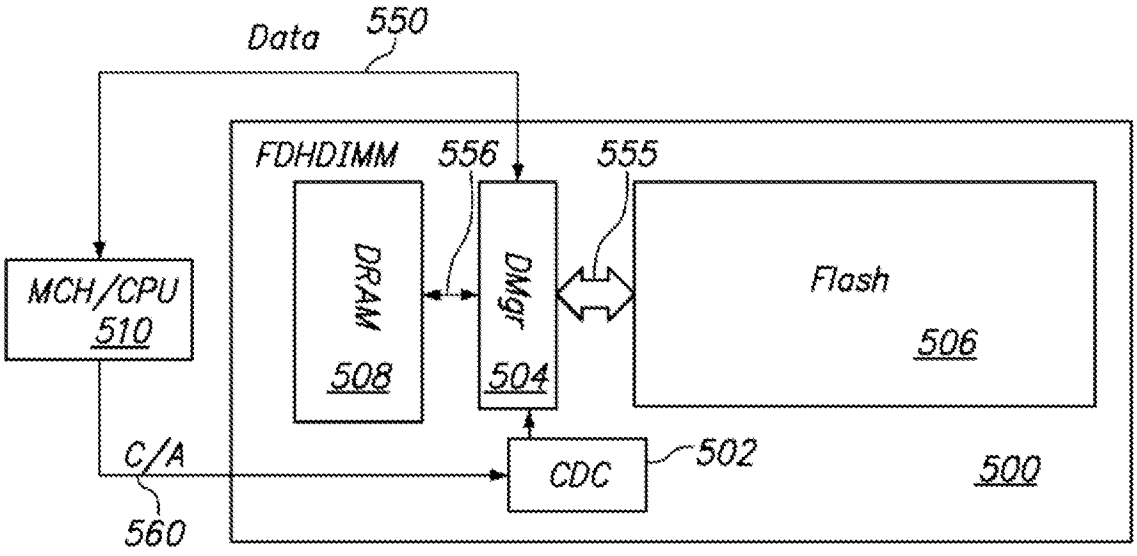

Data
550
FDHDIMM
556
555
DRAM
508
DMgr
504
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

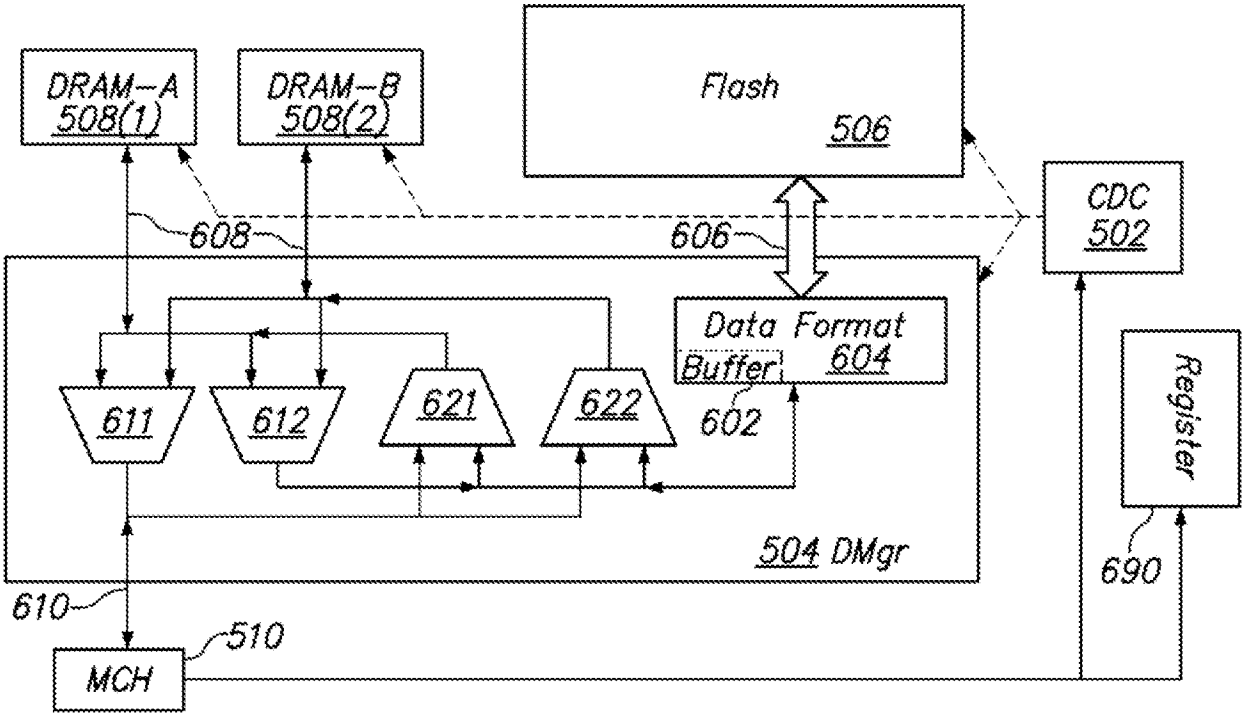

DRAM–A
508(1)
DRAM–B
508(2)
Flash
506
CDC
502
608
606
Data Format
Buffer
604
602
611
612
621
622
Register
690
504 DMgr
610
MCH
510

FIG. 6

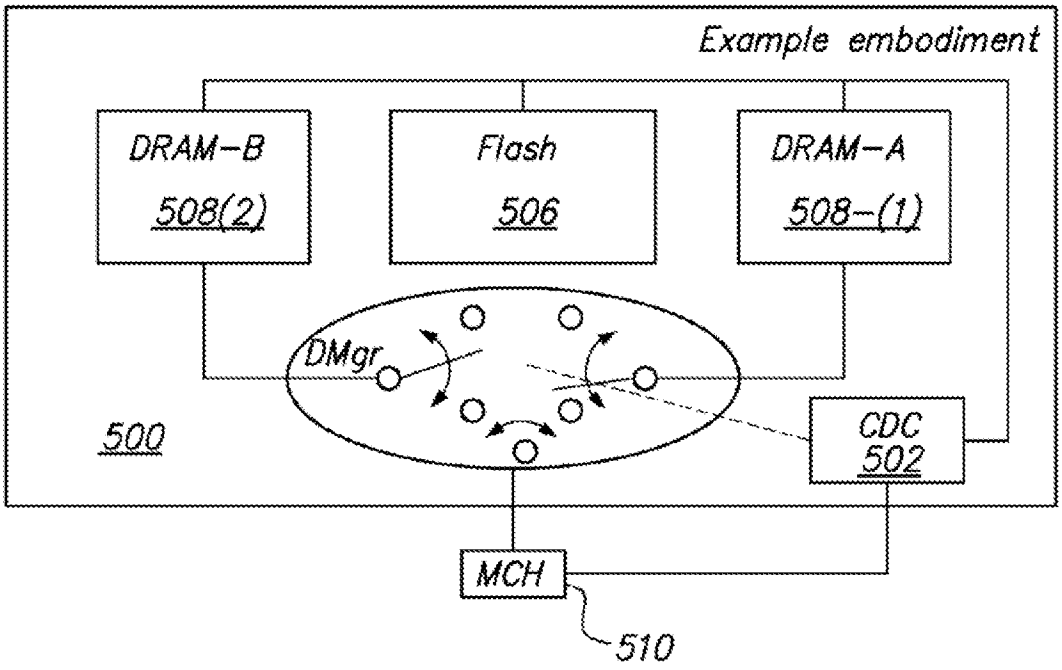

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

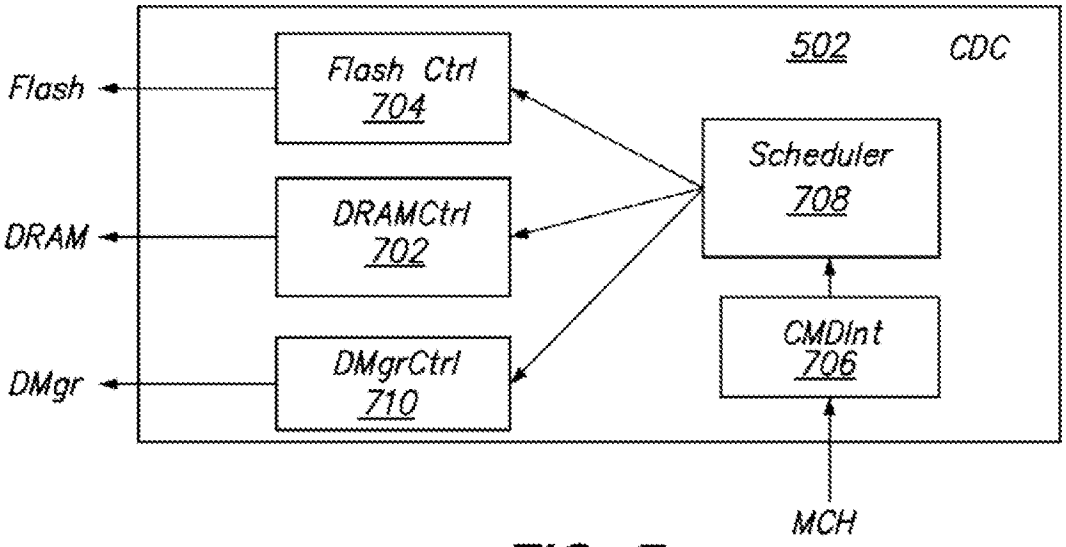

Flash
DRAM
DMgr
Flash Ctrl
704
DRAMCtrl
702
DMgrCtrl
710
502
CDC
Scheduler
708
CMDInt
706
MCH

FIG. 7

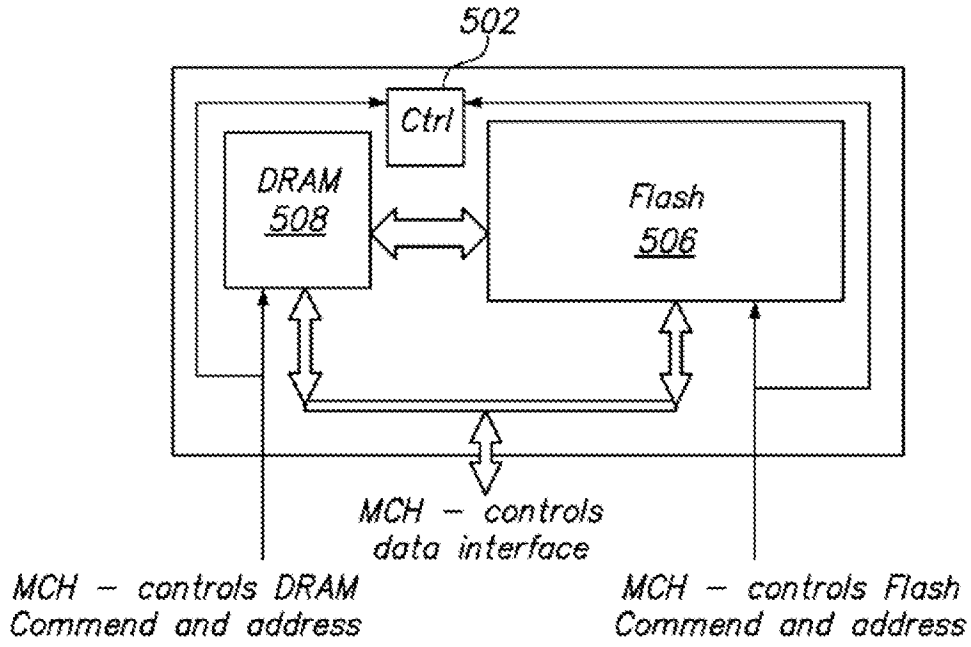

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

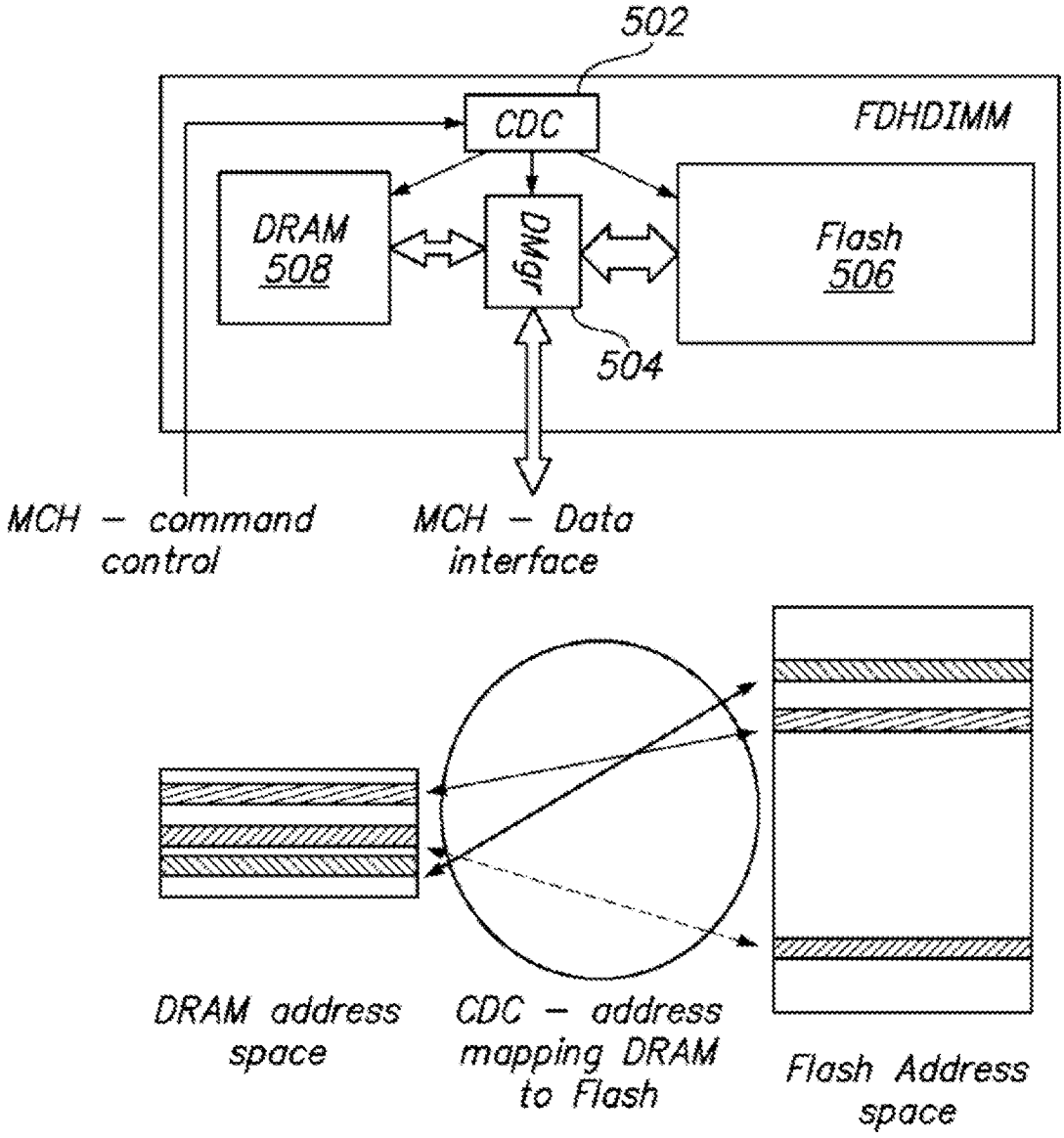

502
CDC
FDHDIMM
DRAM
508
DMGI
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

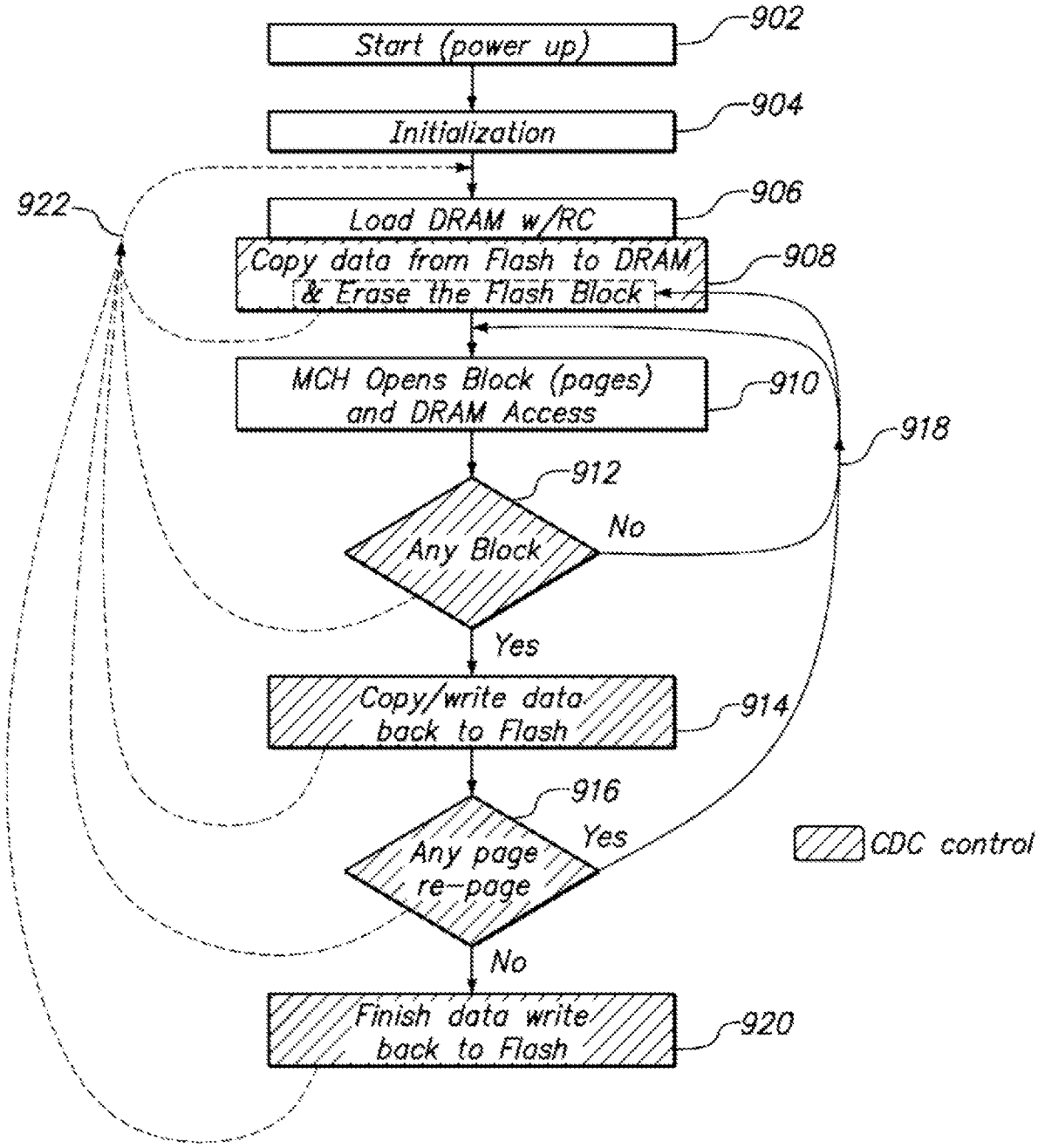

Start (power up)
902
Initialization
904
Load DRAM w/RC
906
Copy data from Flash to DRAM & Erase the Flash Block
908
MCH Opens Block (pages) and DRAM Access
910
Any Block
912
No
Yes
Copy/write data back to Flash
914
Any page re-page
916
Yes
No
Finish data write back to Flash
920
922
918
CDC control

FIG. 9

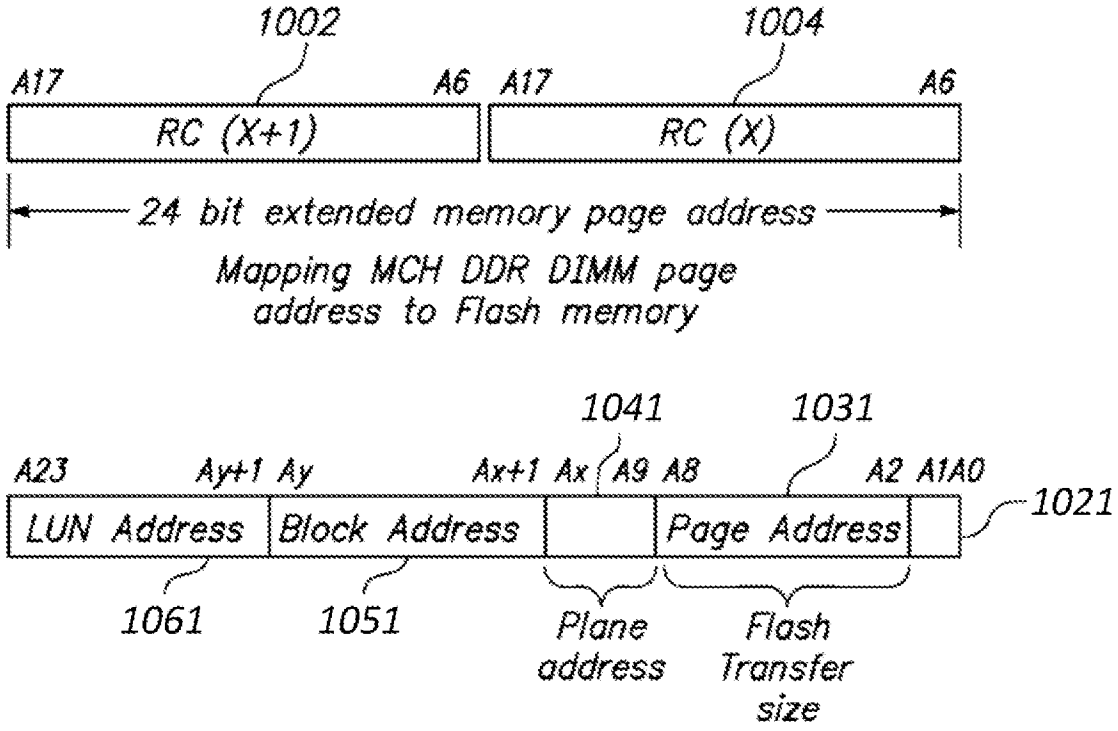

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1041
1031
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1A0
LUN Address
Block Address
Page Address
1021
1061
1051
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

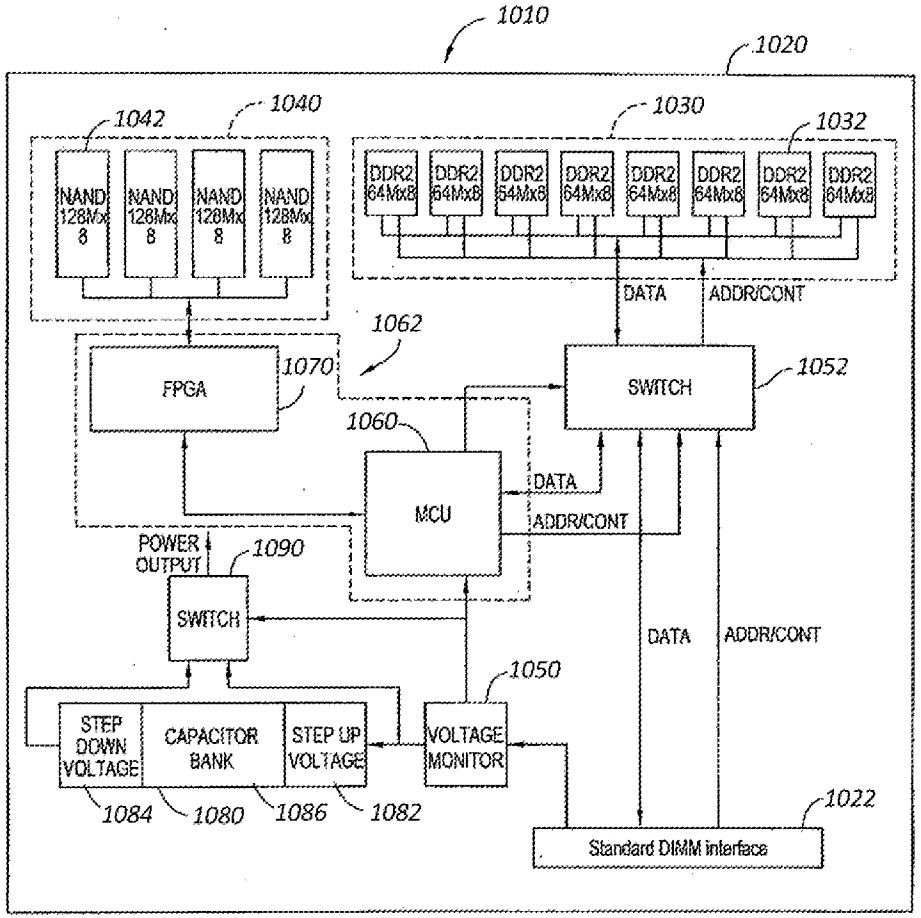

1010
1020
1042
1040
1030
1032
NAND 128Mx8
NAND 128Mx8
NAND 128Mx8
NAND 128Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DDR2 64Mx8
DATA
ADDR/CONT
1062
FPGA
1070
SWITCH
1052
1060
MCU
DATA
ADDR/CONT
POWER OUTPUT
1090
SWITCH
DATA
ADDR/CONT
1050
STEP DOWN VOLTAGE
CAPACITOR BANK
STEP UP VOLTAGE
VOLTAGE MONITOR
1084
1080
1086
1082
1022
Standard DIMM interface

FIG. 12

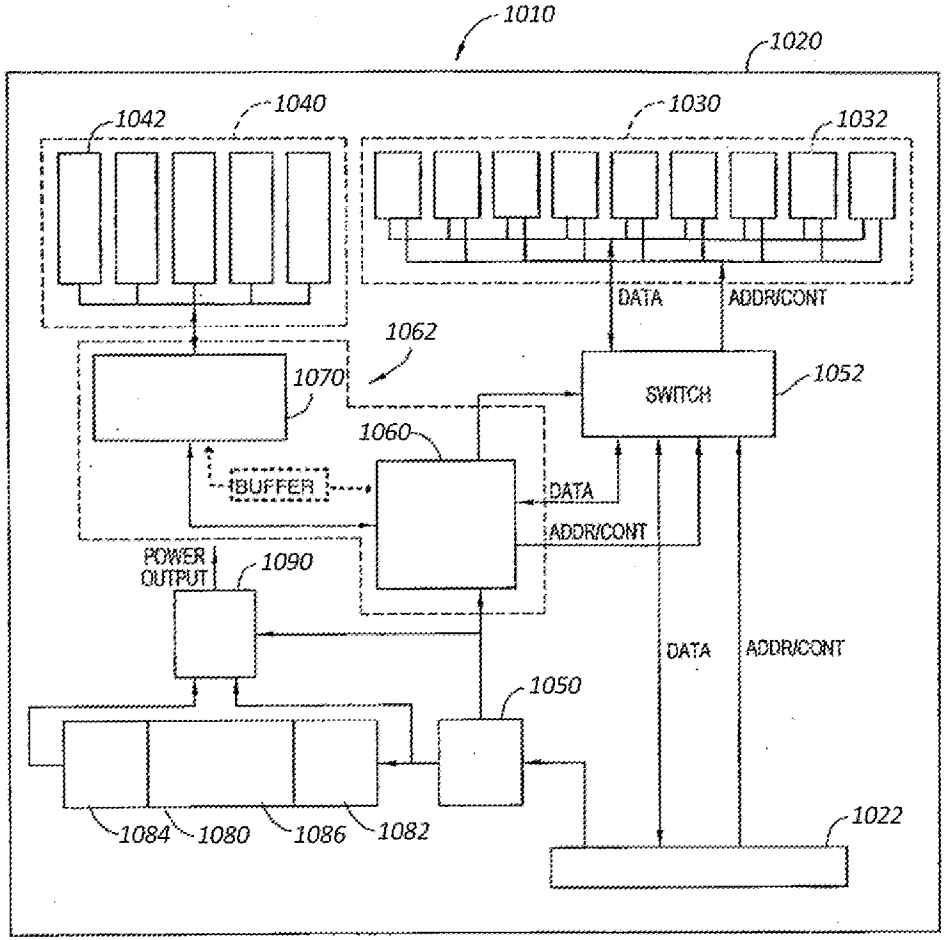

1010
1020
1042
1040
1030
1032
DATA
ADDR/CONT
1062
1070
SWITCH
1052
1060
BUFFER
DATA
ADDR/CONT
POWER OUTPUT
1090
DATA
ADDR/CONT
1050
1084
1080
1086
1082
1022

FIG. 13

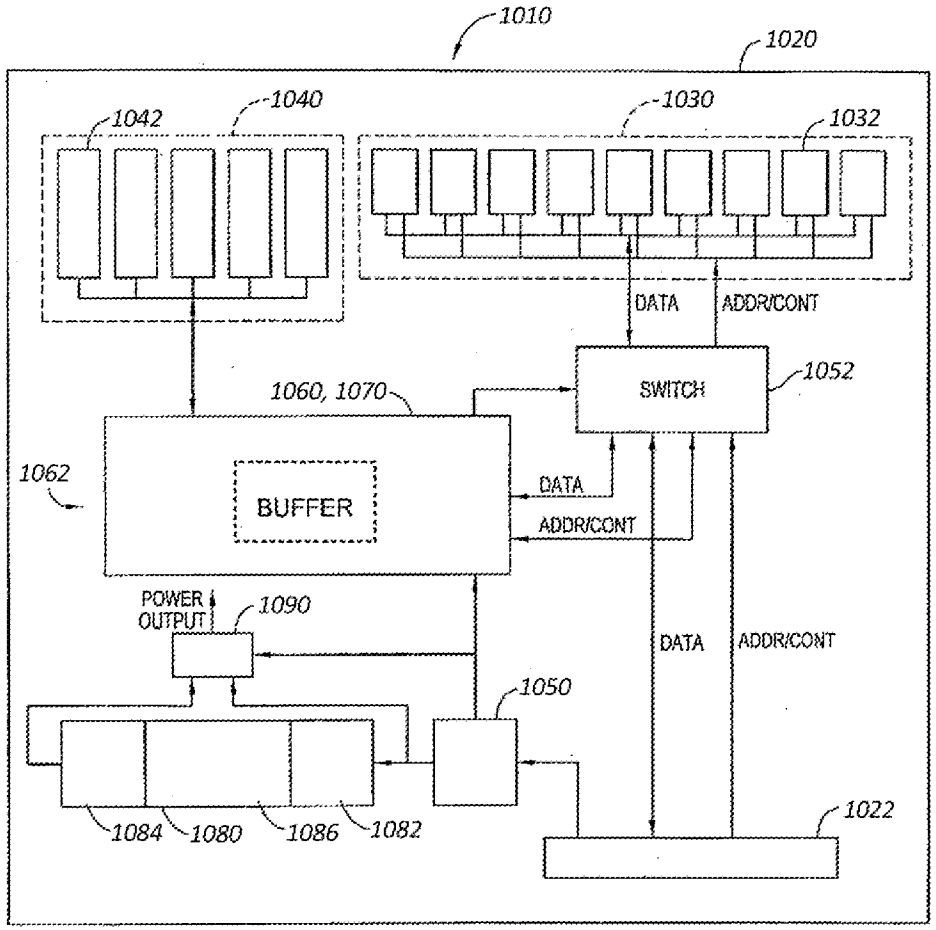

1010
1020
1042
1040
1030
1032
DATA
ADDR/CONT
SWITCH
1052
1060, 1070
1062
BUFFER
DATA
ADDR/CONT
POWER OUTPUT
1090
DATA
ADDR/CONT
1050
1084
1080
1086
1082
1022

FIG. 14

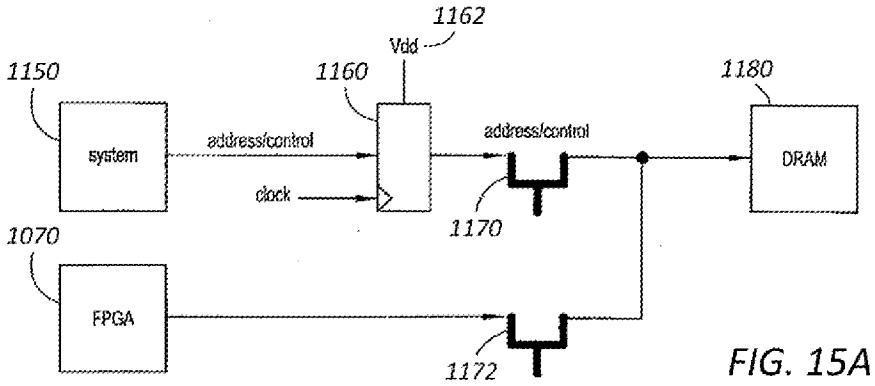


FIG. 15A

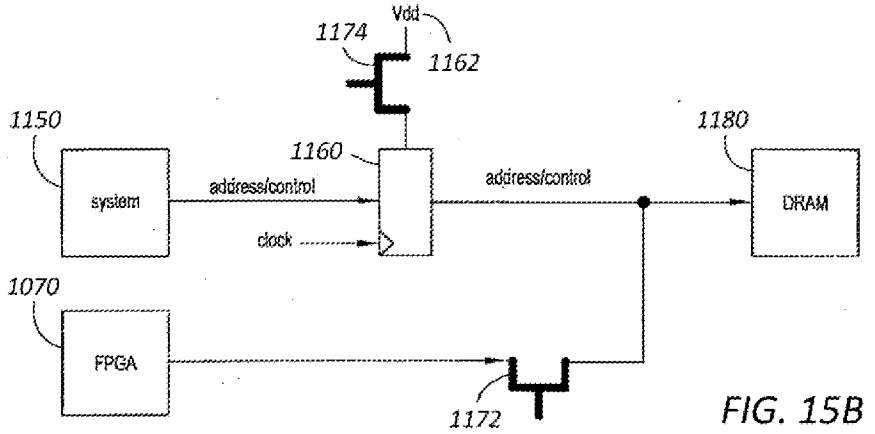


FIG. 15B

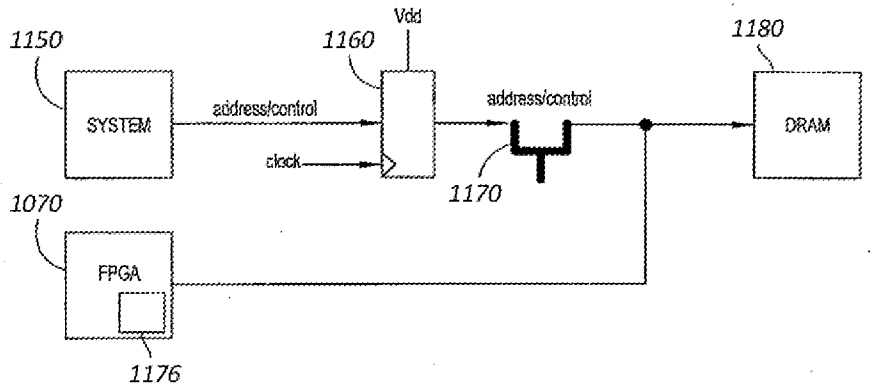

1150
SYSTEM
address/control
clock
1160
Vdd
address/control
1170
1180
DRAM
1070
FPGA
1176

FIG. 15C

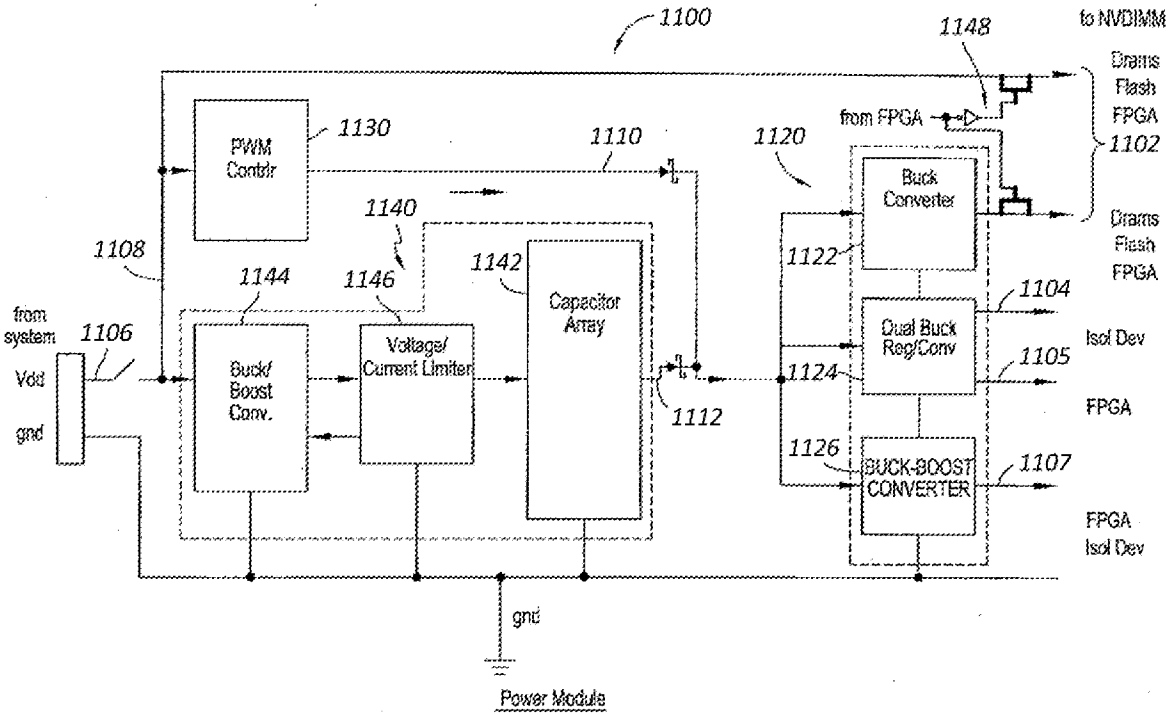


FIG. 16

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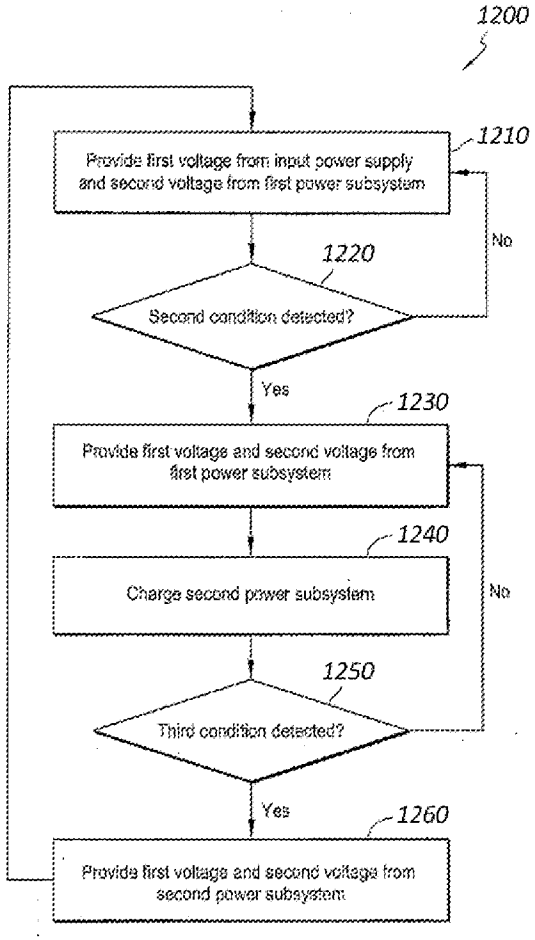

1200
1210
Provide first voltage from input power supply and second voltage from first power subsystem
No
1220
Second condition detected?
Yes
1230
Provide first voltage and second voltage from first power subsystem
1240
Charge second power subsystem
No
1250
Third condition detected?
Yes
1260
Provide first voltage and second voltage from second power subsystem

FIG. 17

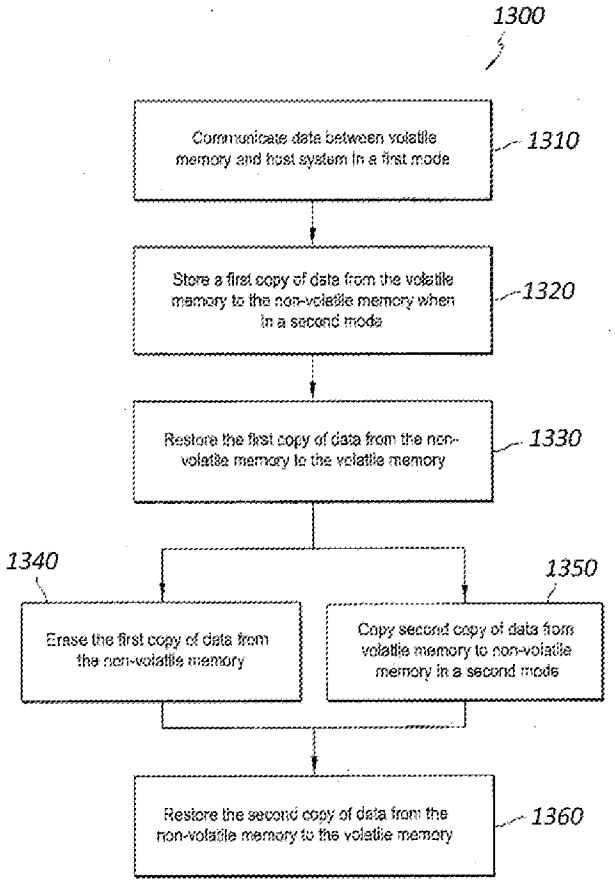

1300
Communicate data between volatile memory and host system in a first mode
1310
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
1320
Restore the first copy of data from the non-volatile memory to the volatile memory
1330
1340
Erase the first copy of data from the non-volatile memory
1350
Copy second copy of data from volatile memory to non-volatile memory in a second mode
Restore the second copy of data from the non-volatile memory to the volatile memory
1360

FIG. 18

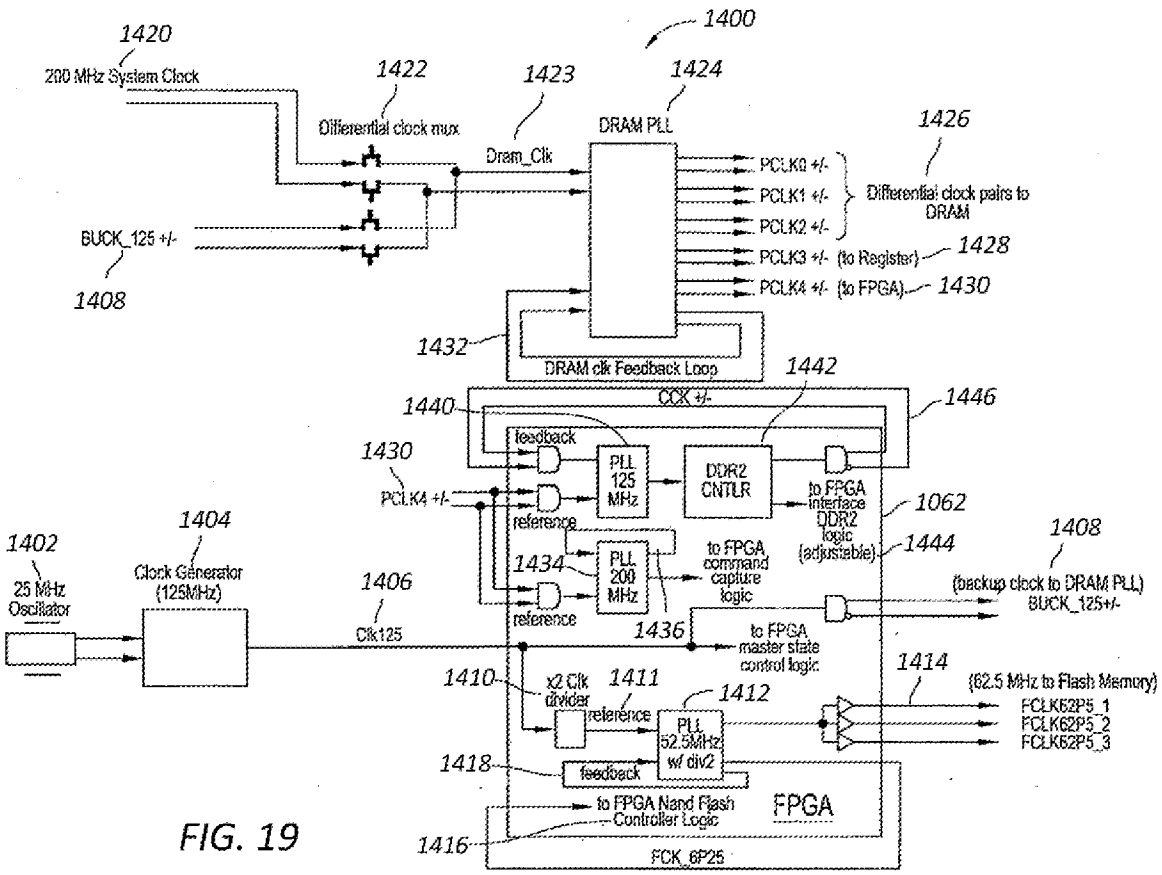

1400
1420
200 MHz System Clock
1422
Differential clock mux
1423
Dram_Clk
1424
DRAM PLL
1426
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
Differential clock pairs to DRAM
PCLK3 +/- (to Register)
1428
PCLK4 +/- (to FPGA)
1430
BUCK_125 +/-
1408
1432
DRAM clk Feedback Loop
1442
CCK +/-
1446
1440
feedback
1430
PCLK4 +/-
PLL 125 MHz
DDR2 CNTLR
to FPGA interface DDR2 logic (adjustable)
1062
1444
reference
1404
1402
Clock Generator (125MHz)
25 MHz Oscillator
1434
PLL 200 MHz
to FPGA command capture logic
1408
(backup clock to DRAM PLL) BUCK_125+/-
1406
Clk125
reference
1436
to FPGA master state control logic
1414
1410
x2 Clk divider
1411
reference
1412
PLL 52.5MHz w/ div2
(62.5 MHz to Flash Memory)
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
1418
feedback
to FPGA Nand Flash Controller Logic
FPGA
1416
FCK_6P25

FIG. 19

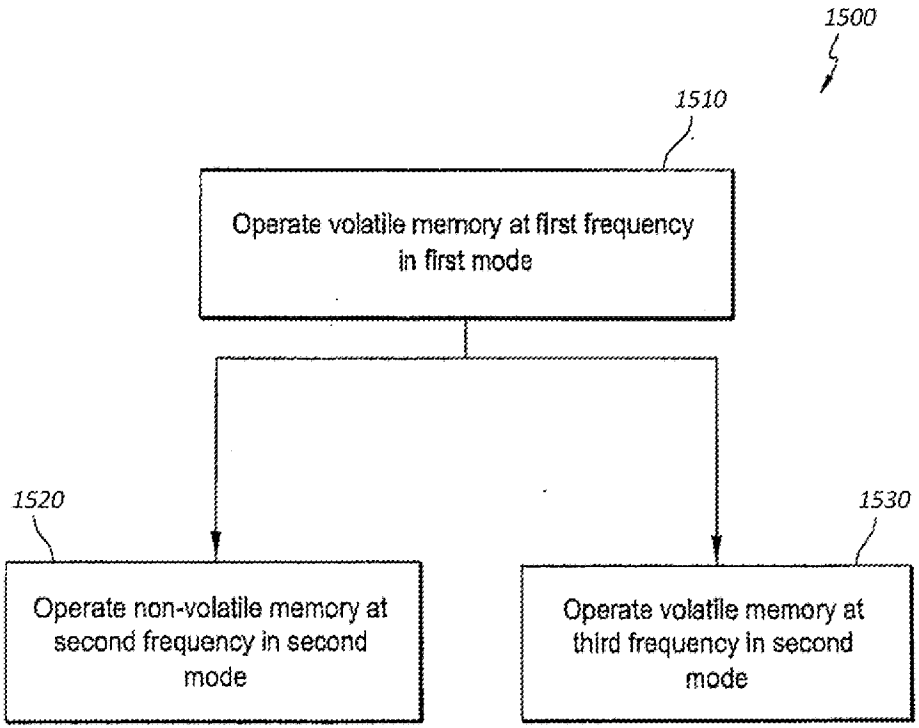

1500
1510
Operate volatile memory at first frequency in first mode
1520
Operate non-volatile memory at second frequency in second mode
1530
Operate volatile memory at third frequency in second mode

FIG. 20

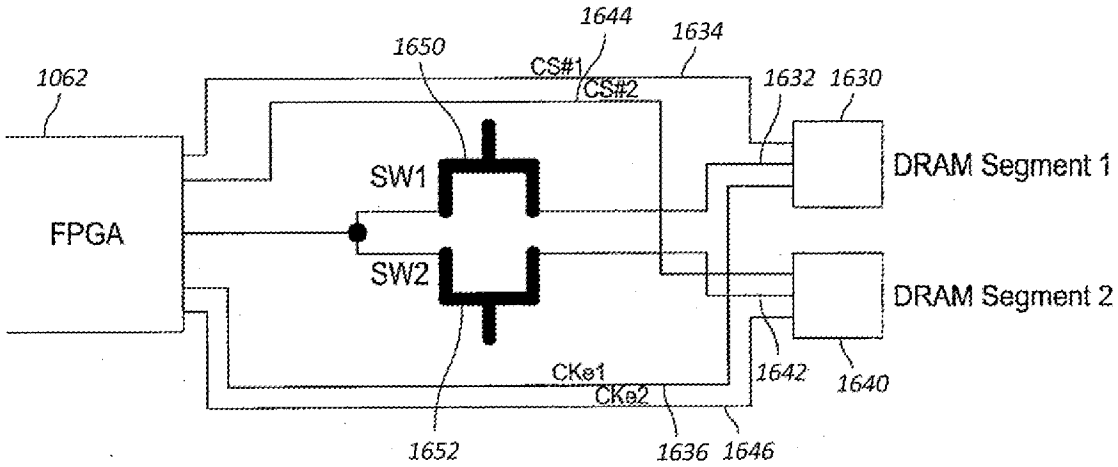

1644
1634
1650
CS#1
CS#2
1062
1632
1630
SW1
FPGA
DRAM Segment 1
SW2
DRAM Segment 2
CKe1
1642
1640
CKe2
1652
1636
1646

FIG. 21

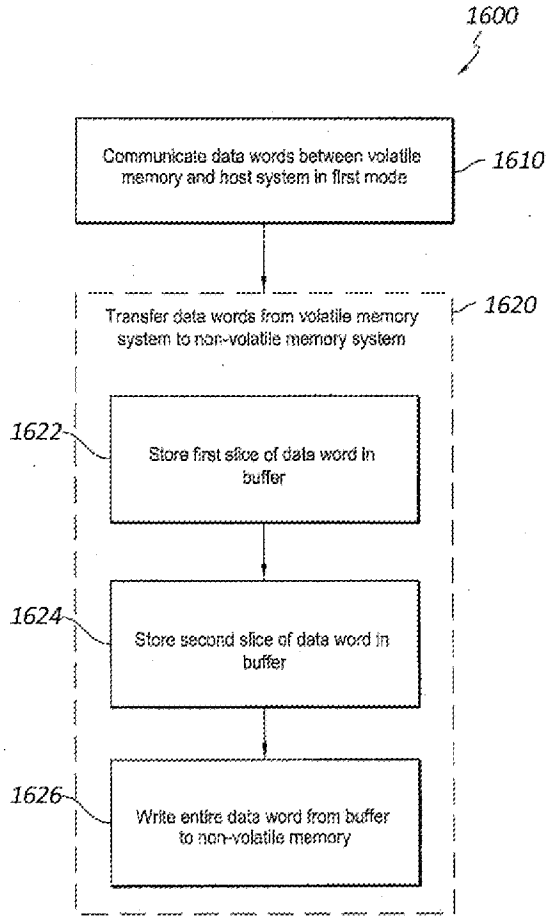

1600
Communicate data words between volatile memory and host system in first mode
1610
Transfer data words from volatile memory system to non-volatile memory system
1620
1622
Store first slice of data word in buffer
1624
Store second slice of data word in buffer
1626
Write entire data word from buffer to non-volatile memory

FIG. 22

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/582,797	01/24/2022	1731	0.00	022955-000090	1	1

CONFIRMATION NO. 3546

FILING RECEIPT

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

OC000000131509999

Date Mailed: 02/02/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 17/328,019 05/24/2021 PAT 11232054
which is a CON of 17/138,766 12/30/2020 PAT 11016918
which is a CON of 15/934,416 03/23/2018 ABN
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

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Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/01/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/582,797**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No
Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

501

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/582,797

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/582,797	01/24/2022	Chi-She Chen	022955-000090

CONFIRMATION NO. 3546

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

FORMALITIES LETTER

OC000000131510000

Date Mailed: 02/02/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 17 - 19, & 22 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of

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small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

	Chi-She Chen, et al.
Appl. No.:	17/582,797
Filing Date:	January 24, 2022
Exam:	Not Yet Assigned
Art Unit:	1731
Conf.:	3546
Title:	**FLASH-DRAM HYBRID MEMORY MODULE**

PRELIMINARY AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Please enter the following amendments:

Amendment to the Drawings begin on page **2**;

Remarks begin on page **3**.

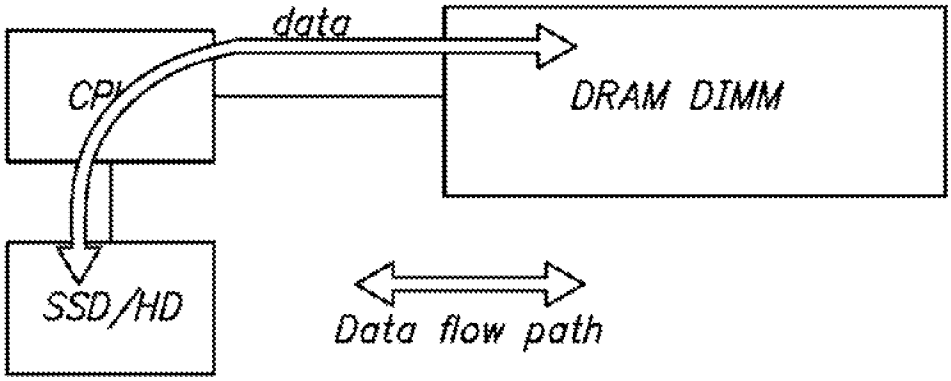


FIG. 1
(PRIOR ART)

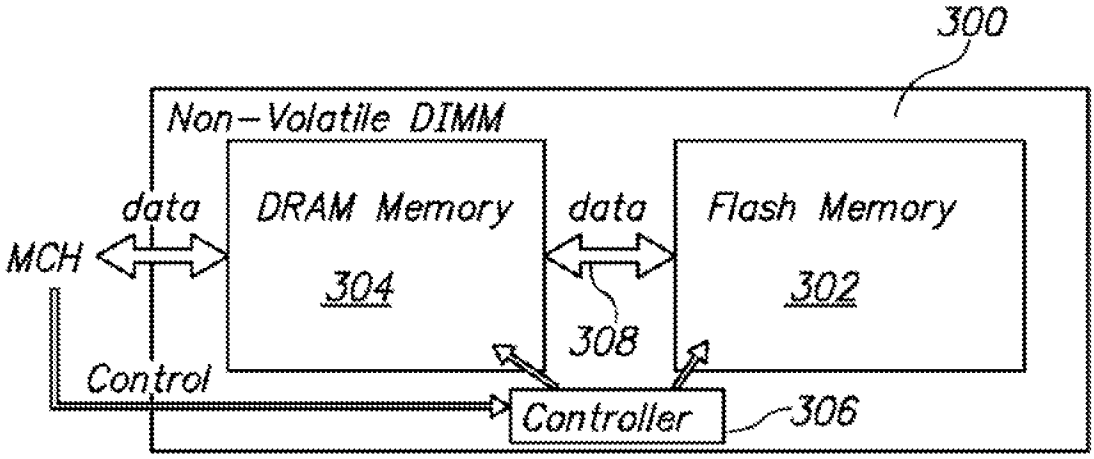


FIG. 3A

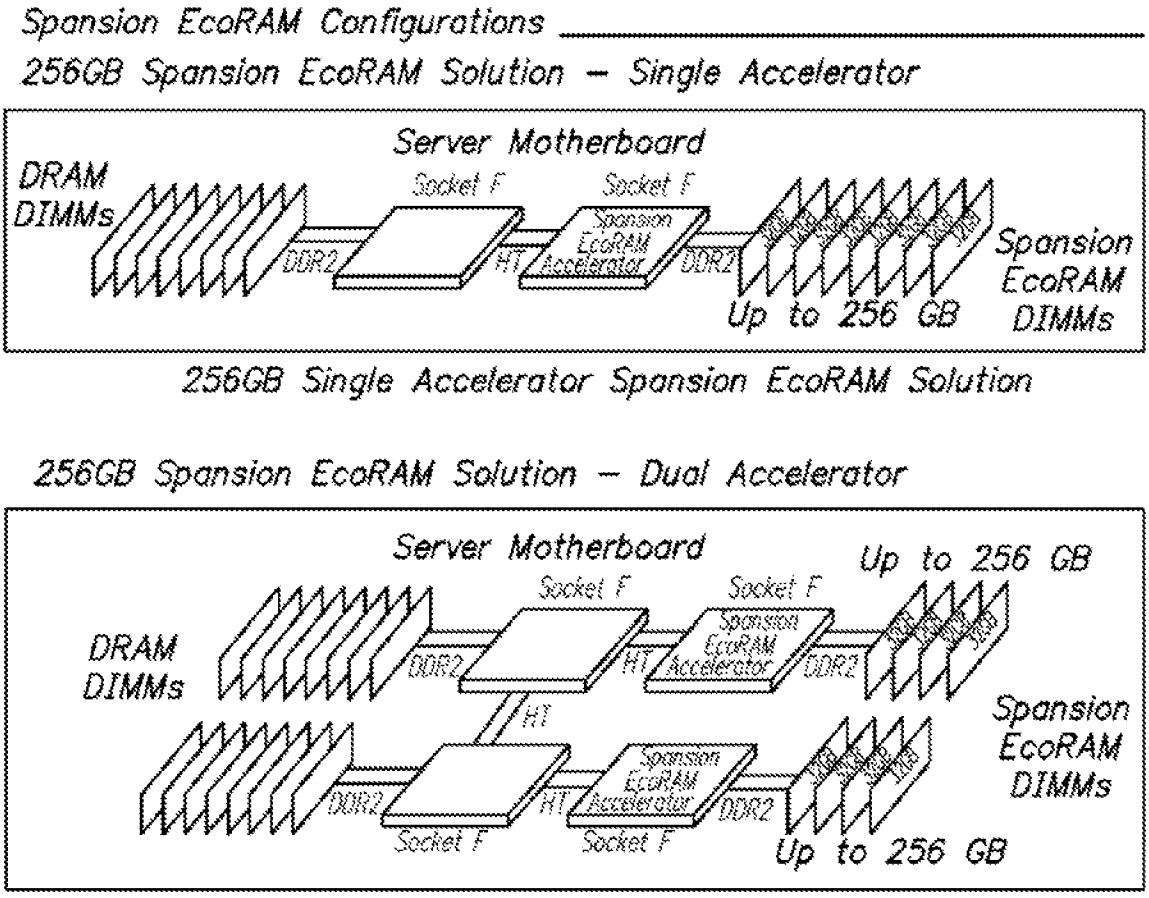


FIG. 2
(PRIOR ART)

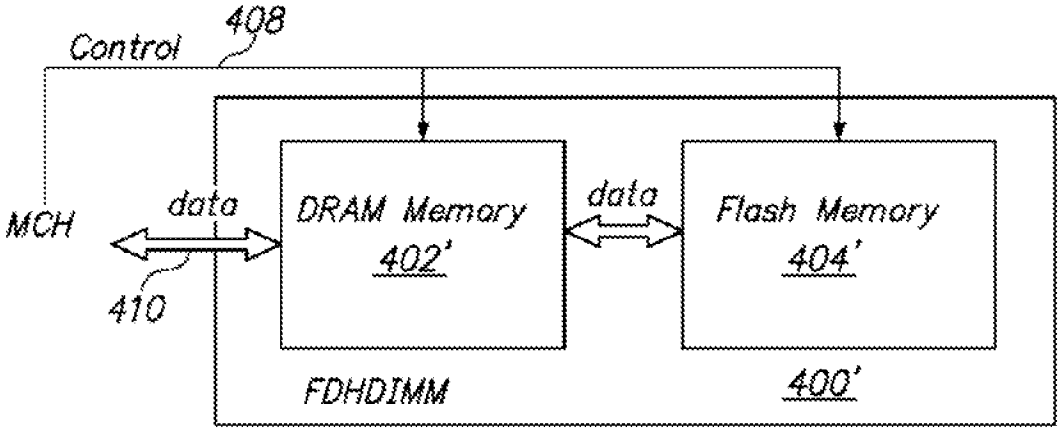


FIG. 4B

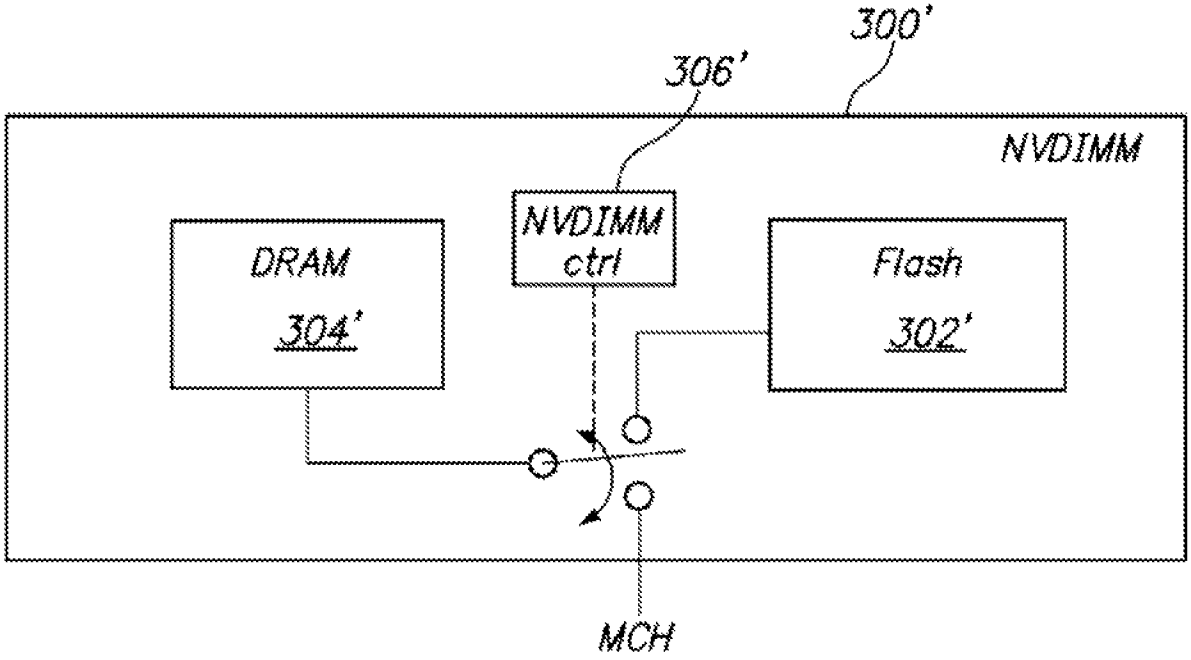

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

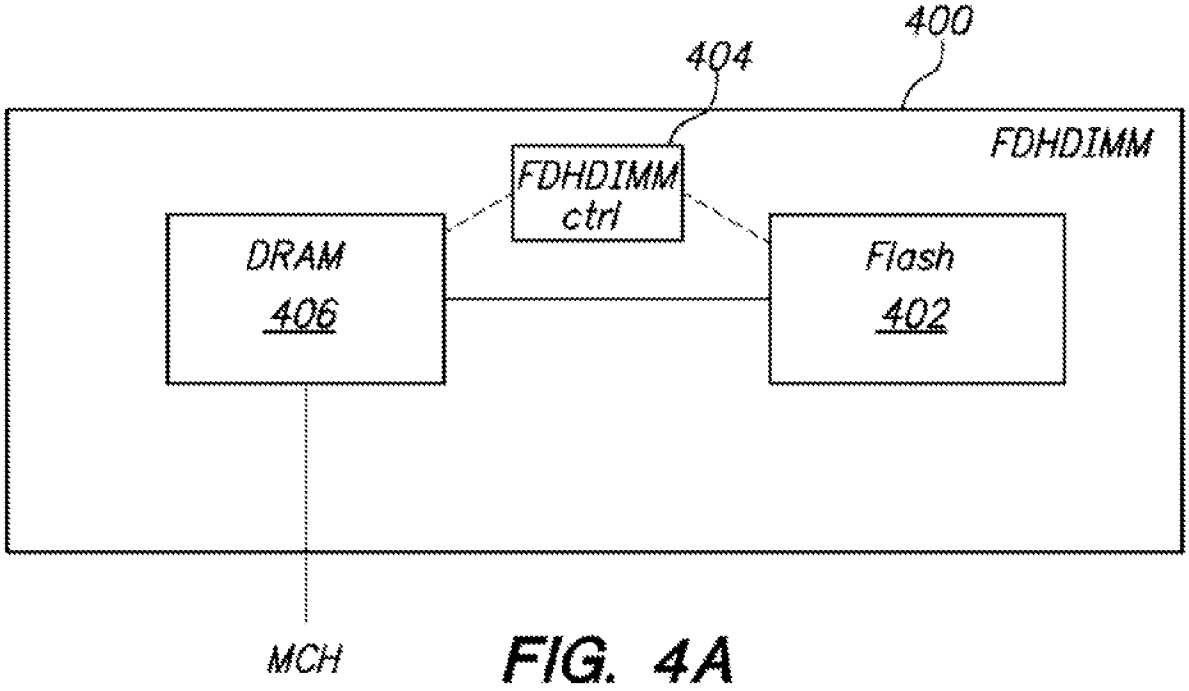

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

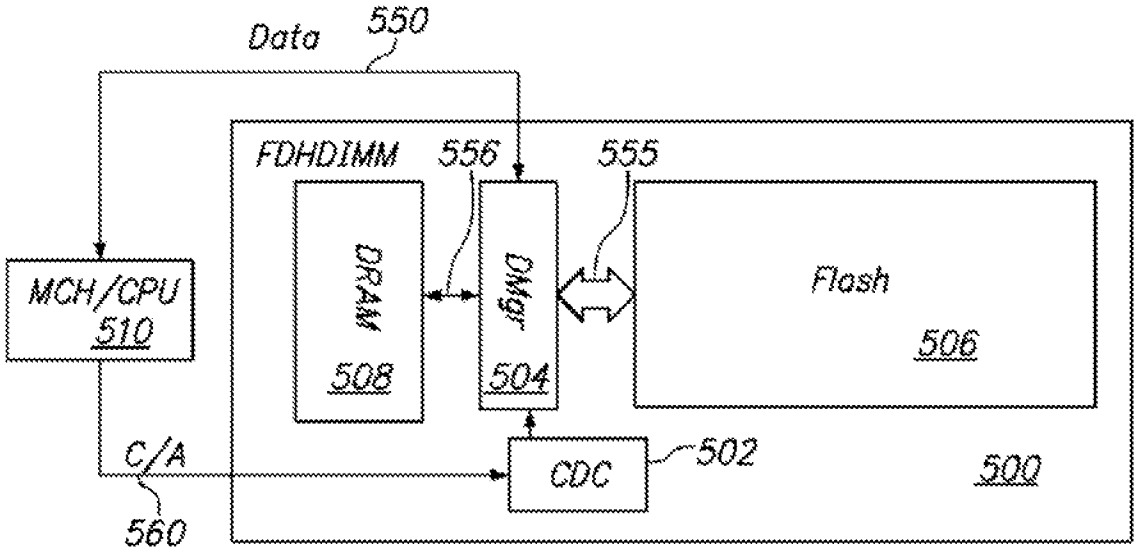

Data
550
FDHDIMM
556
555
DRAM
508
DMgr
504
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

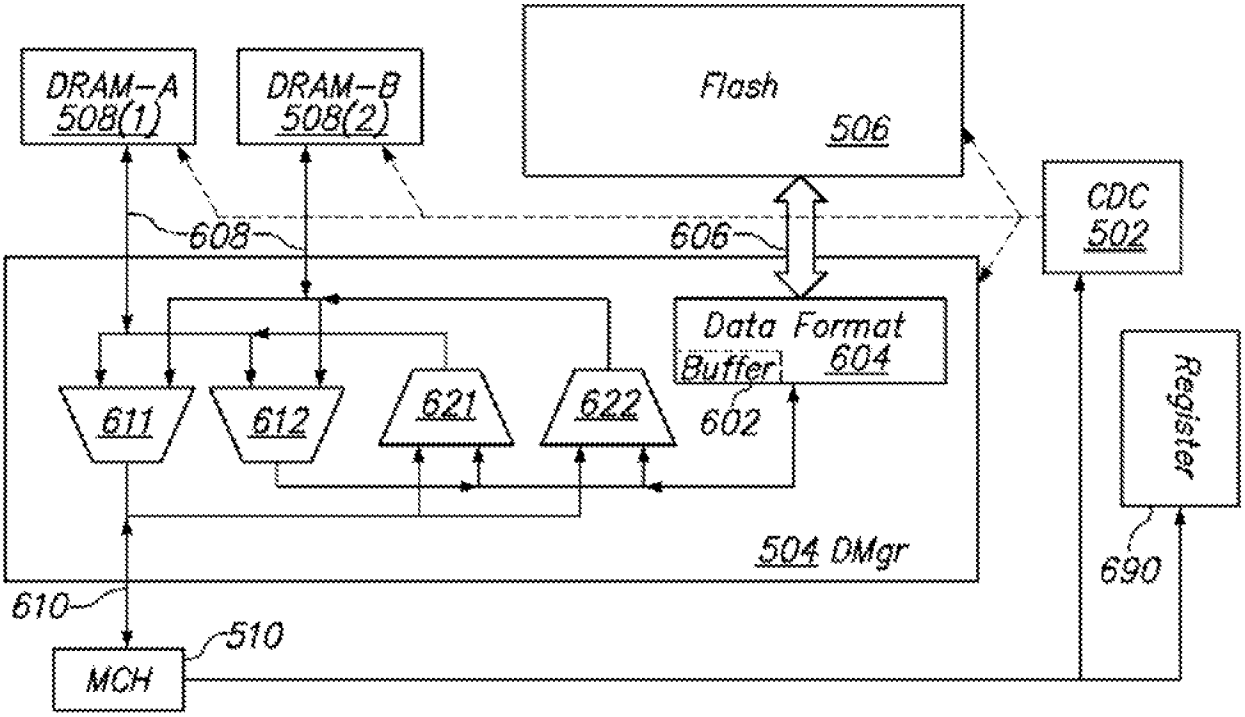

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
CDC
502
608
606
Data Format
Buffer
604
602
611
612
621
622
Register
690
504 DMgr
610
MCH
510

FIG. 6

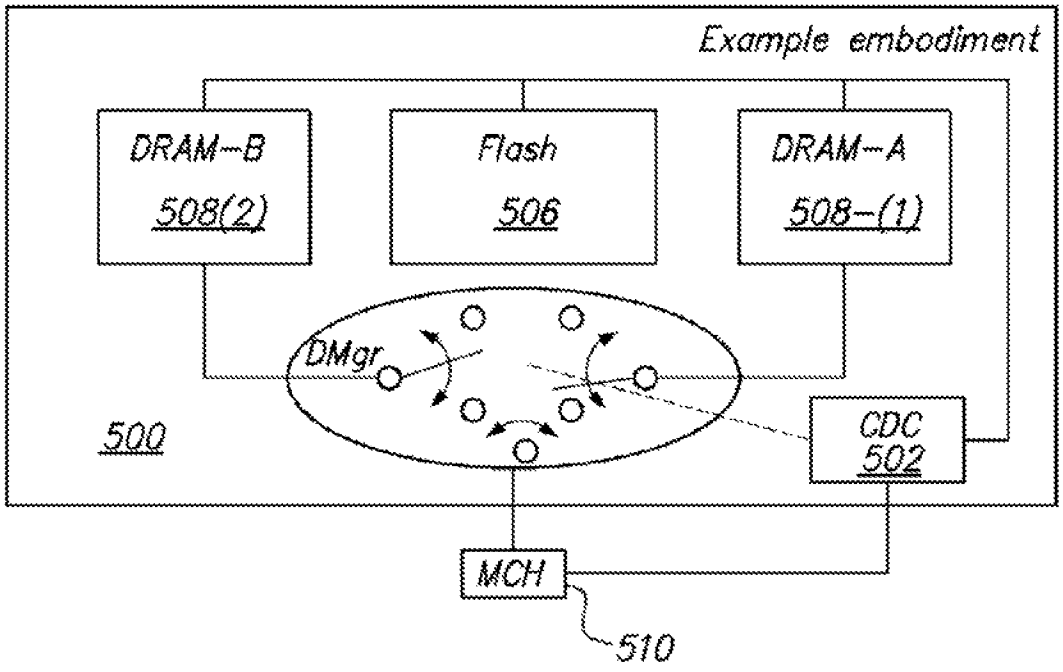

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

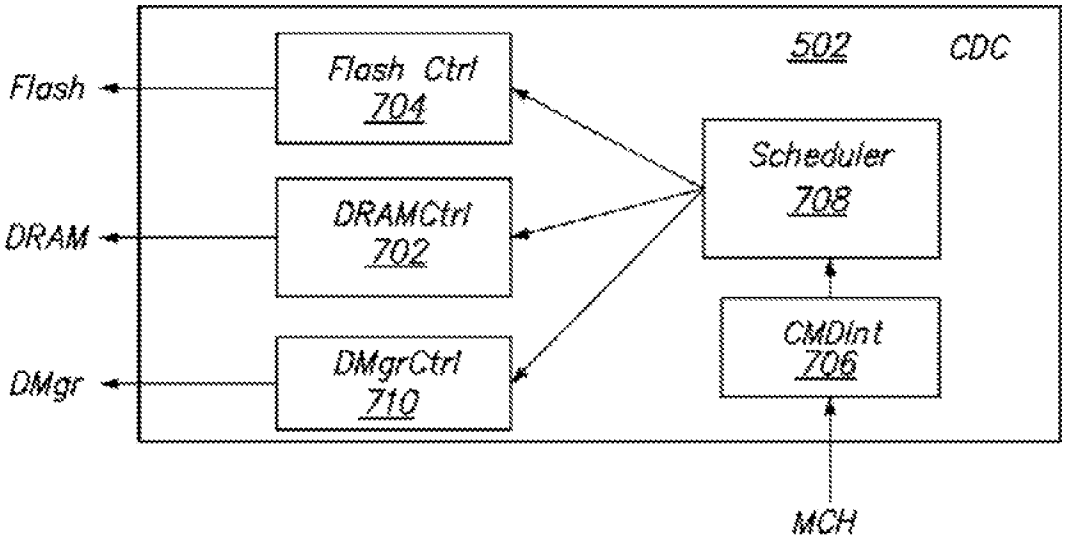

502
CDC
Flash
DRAM
DMgr
Flash Ctrl
704
DRAMCtrl
702
DMgrCtrl
710
Scheduler
708
CMDint
706
MCH

FIG. 7

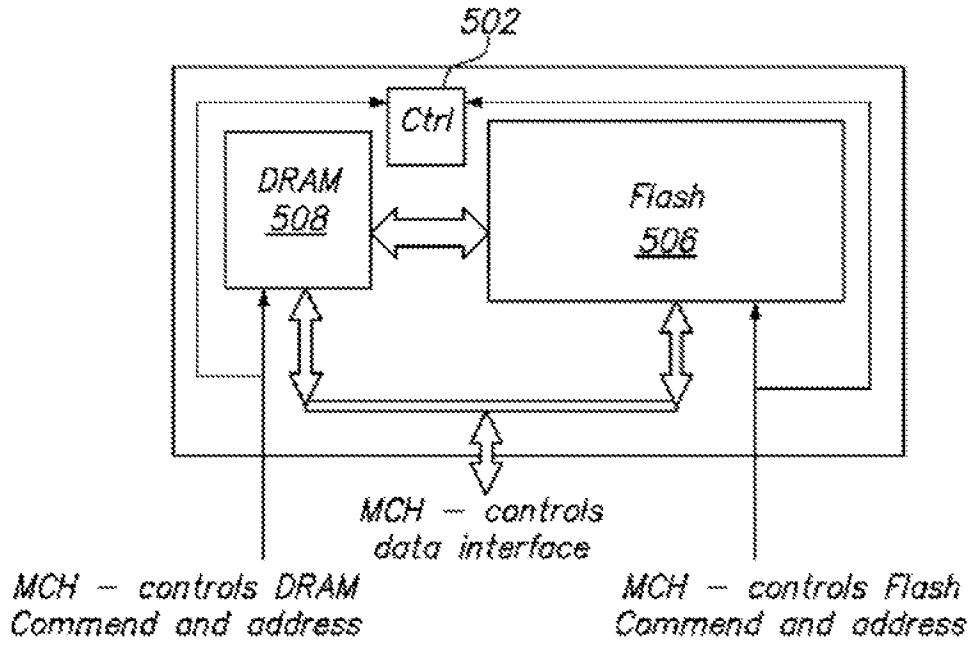

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

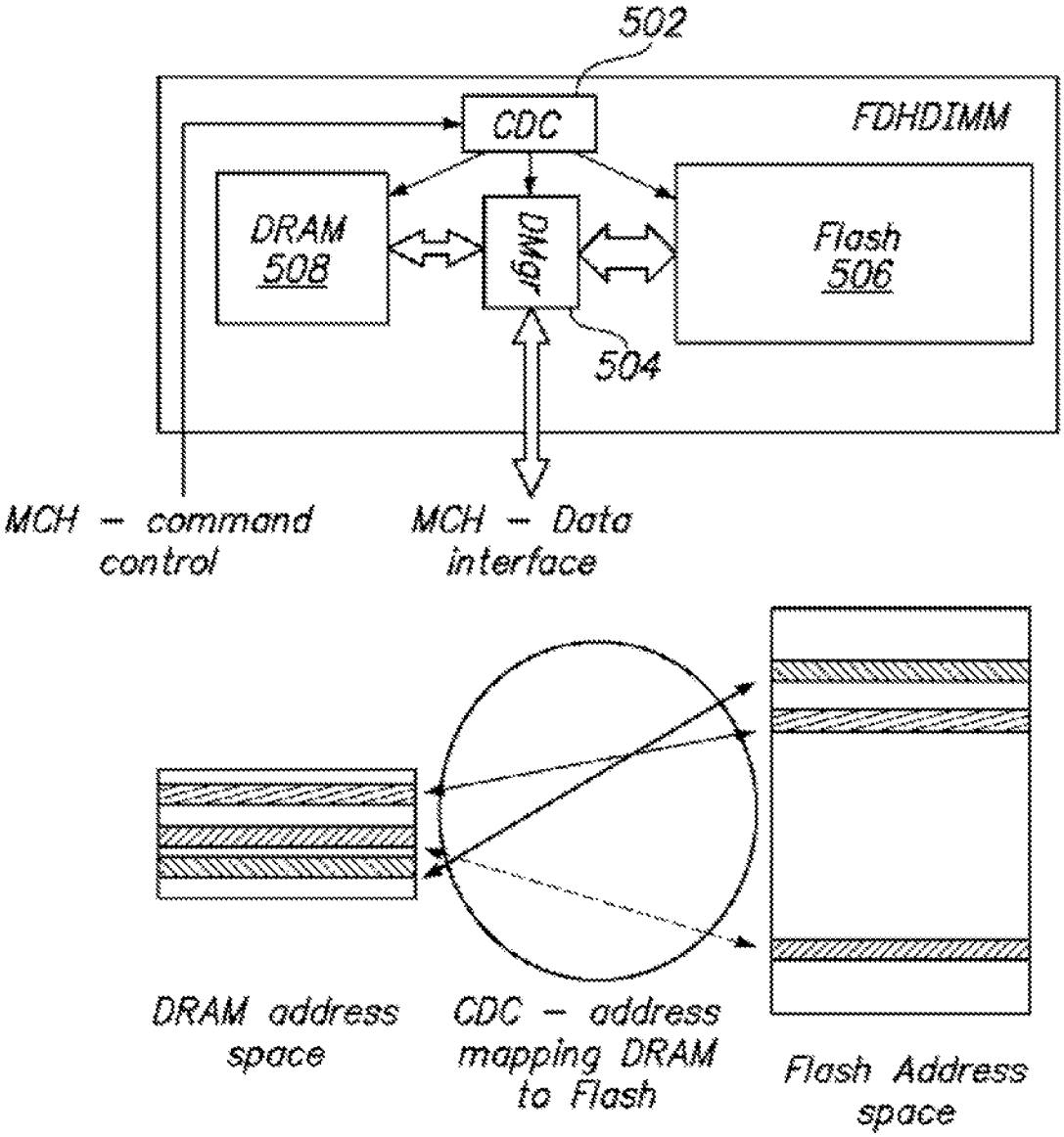

502
CDC
FDHDIMM
DRAM
508
DMUX
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

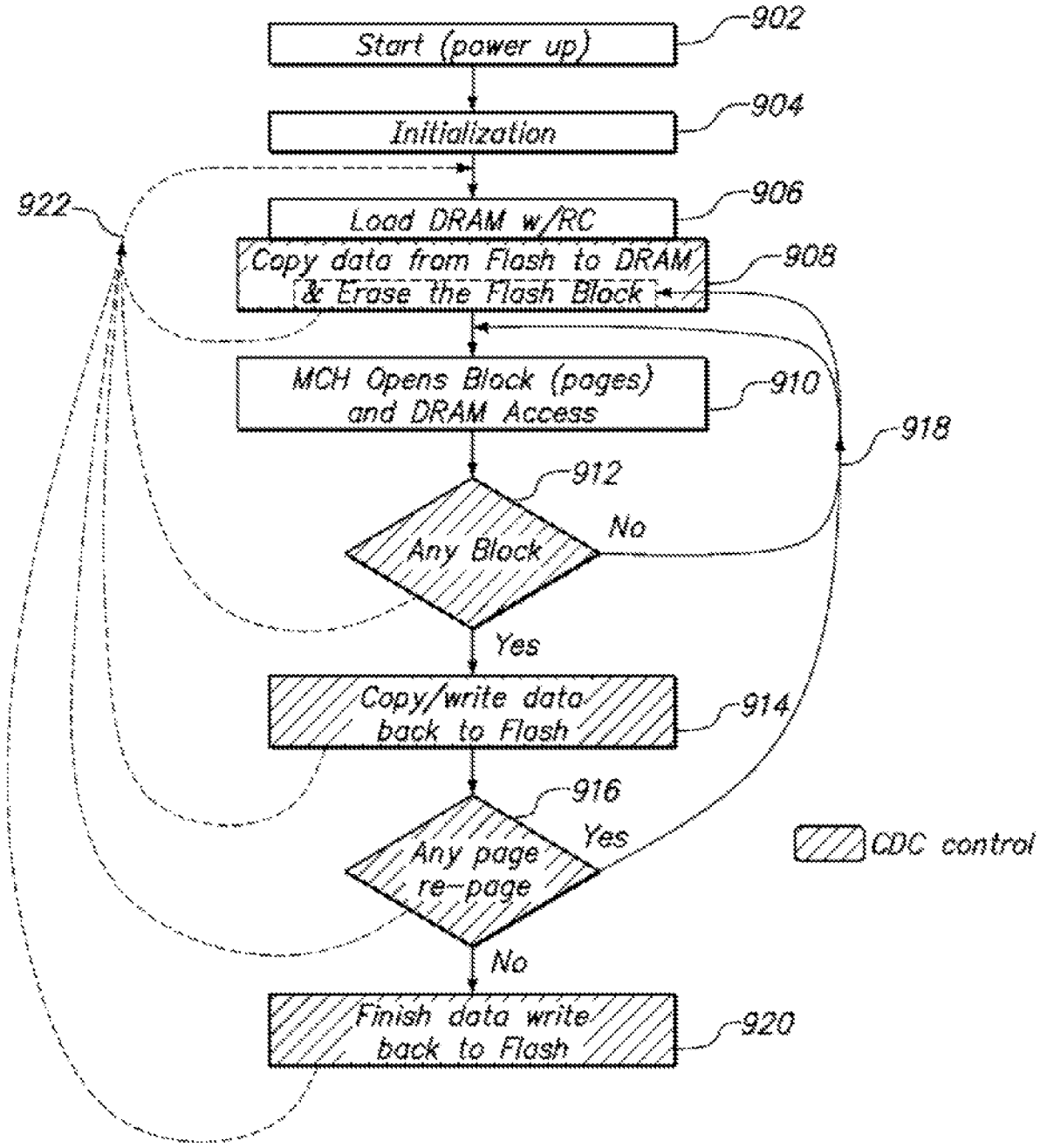

Start (power up)
902
Initialization
904
Load DRAM w/RC
906
Copy data from Flash to DRAM & Erase the Flash Block
908
MCH Opens Block (pages) and DRAM Access
910
Any Block
912
No
Yes
Copy/write data back to Flash
914
Any page re-page
916
Yes
No
Finish data write back to Flash
920
922
918
CDC control

FIG. 9

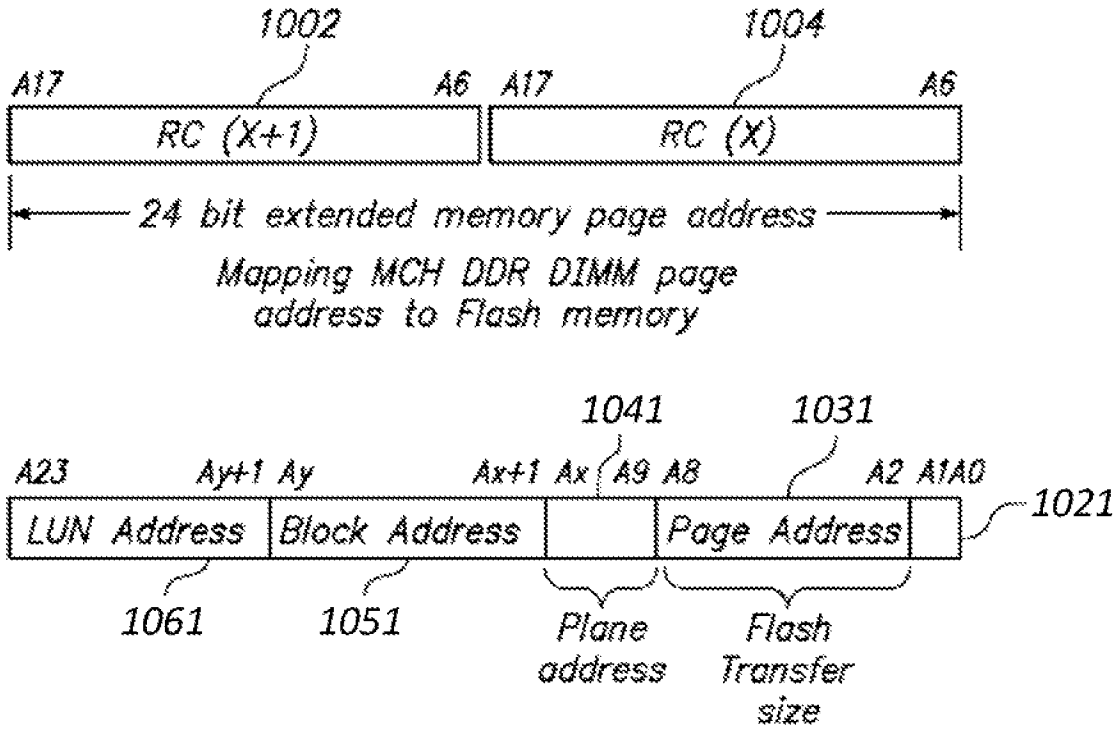
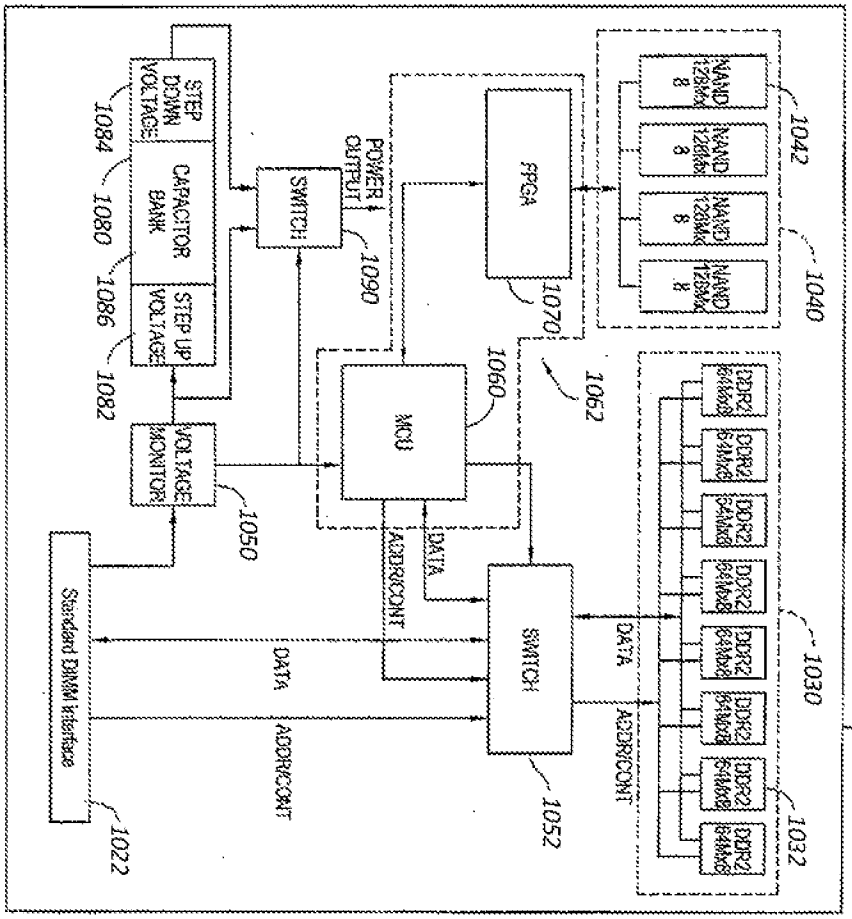

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1041
1031
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1A0
LUN Address
Block Address
Page Address
1021
1061
1051
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

FIG. 12


1010
1020
1030
1032
1040
1042
NAND 128MX 8
DDR2 64MX8
1050
MONITOR
VOLTAGE
1052
SWITCH
DATA
ADDR/CONT
1060
MCU
1062
1070
FPGA
1080
CAPACITOR BANK
1082
STEP UP VOLTAGE
1084
STEP DOWN VOLTAGE
1086
1090
POWER OUTPUT
SWITCH
1022
Standard DIMM Interface

REPLACEMENT SHEET

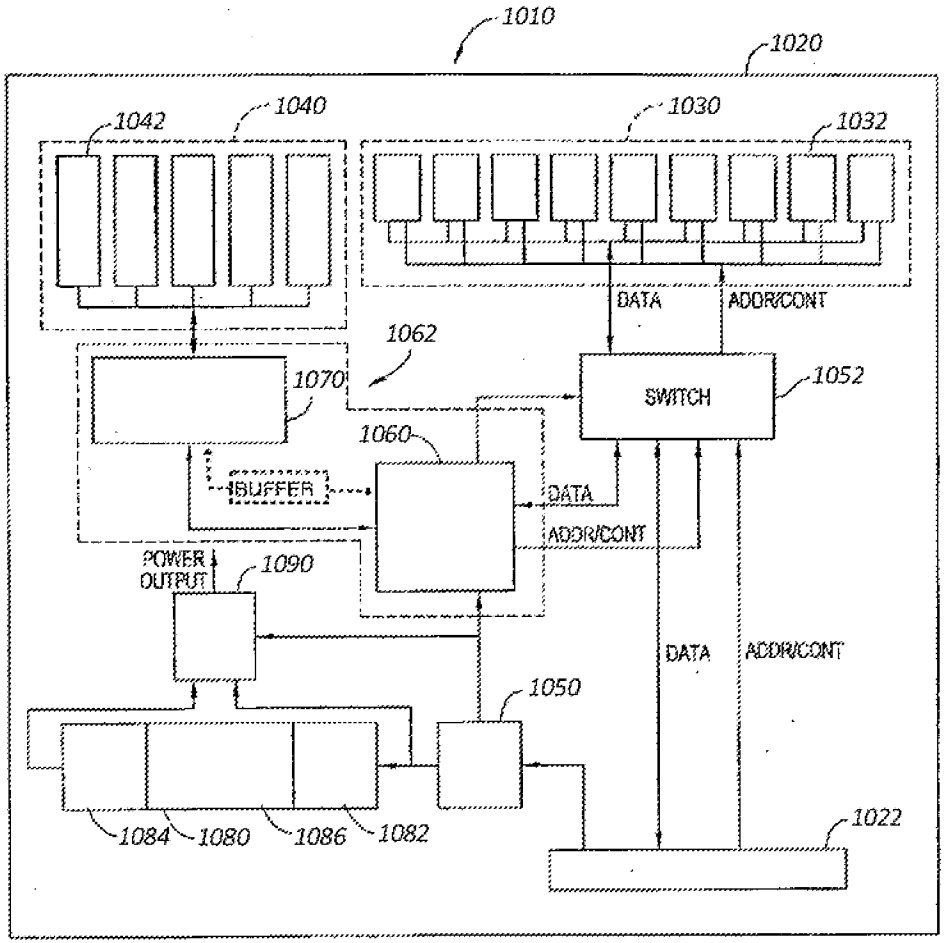


FIG. 13

REPLACEMENT SHEET

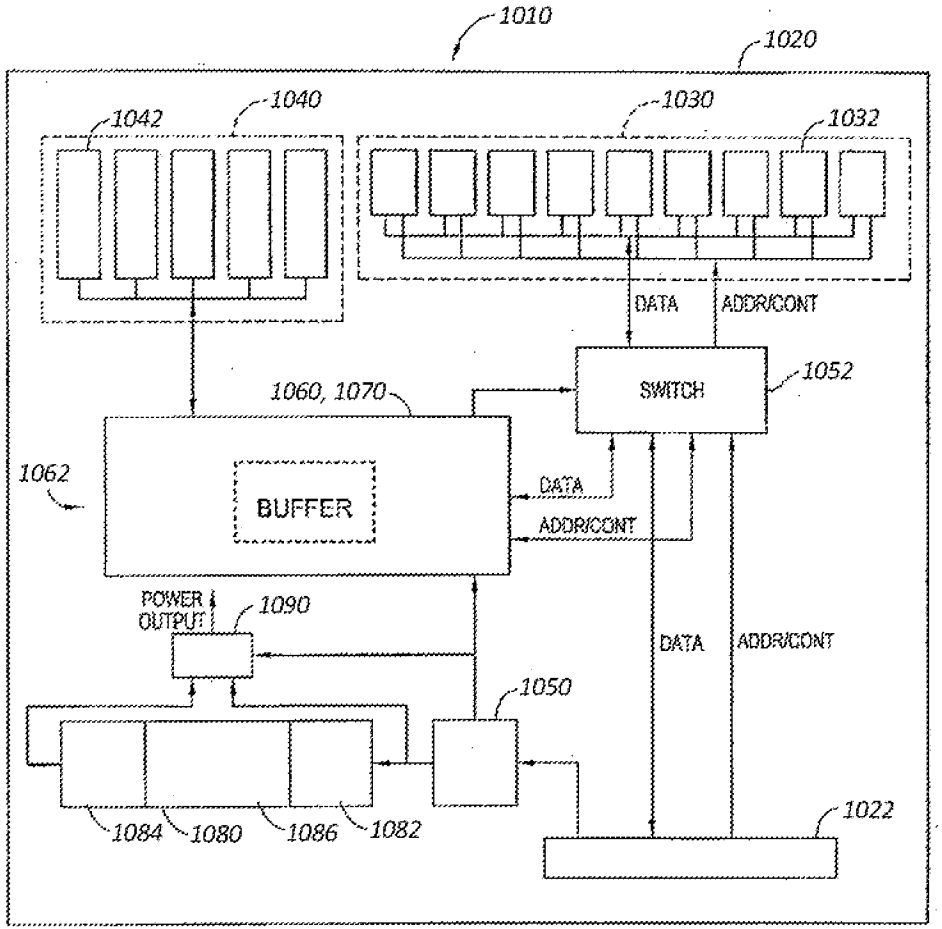


FIG. 14

REPLACEMENT SHEET

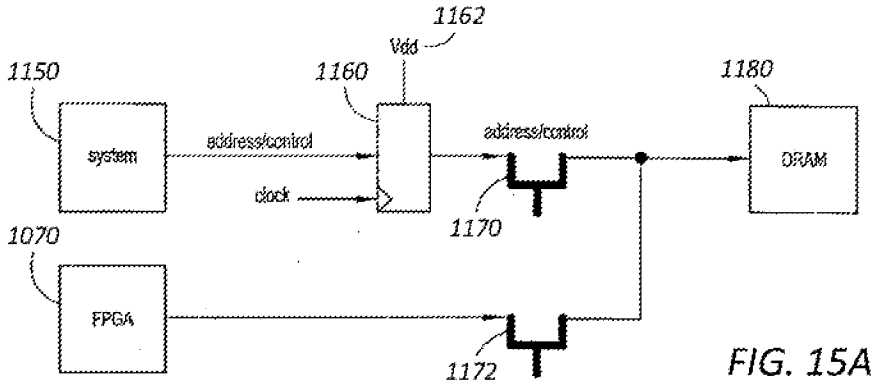


FIG. 15A

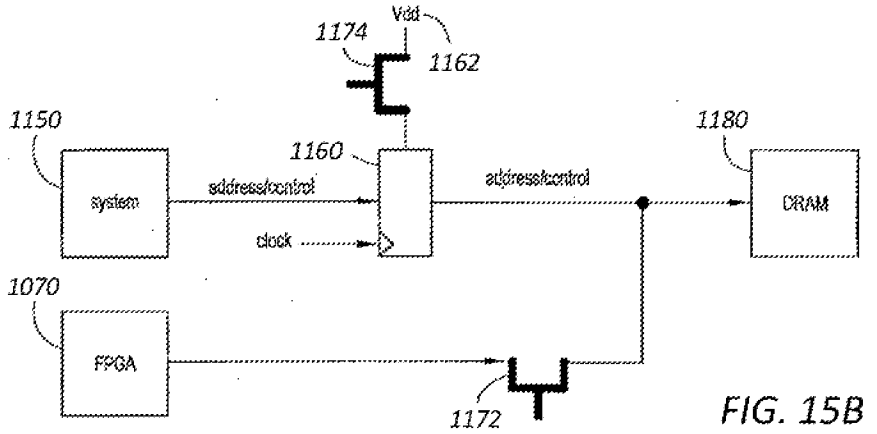


FIG. 15B

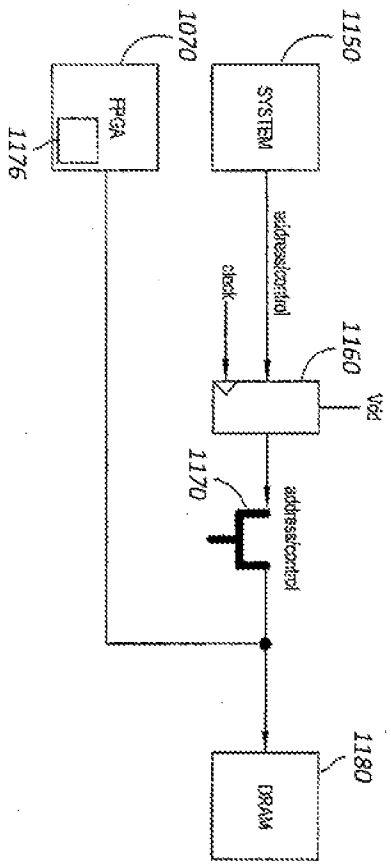

1070
FPGA
1176
1150
SYSTEM
address/control
clock
1160
Vtt
1170
address/control
1180
DRAM

FIG. 15C

REPLACEMENT SHEET

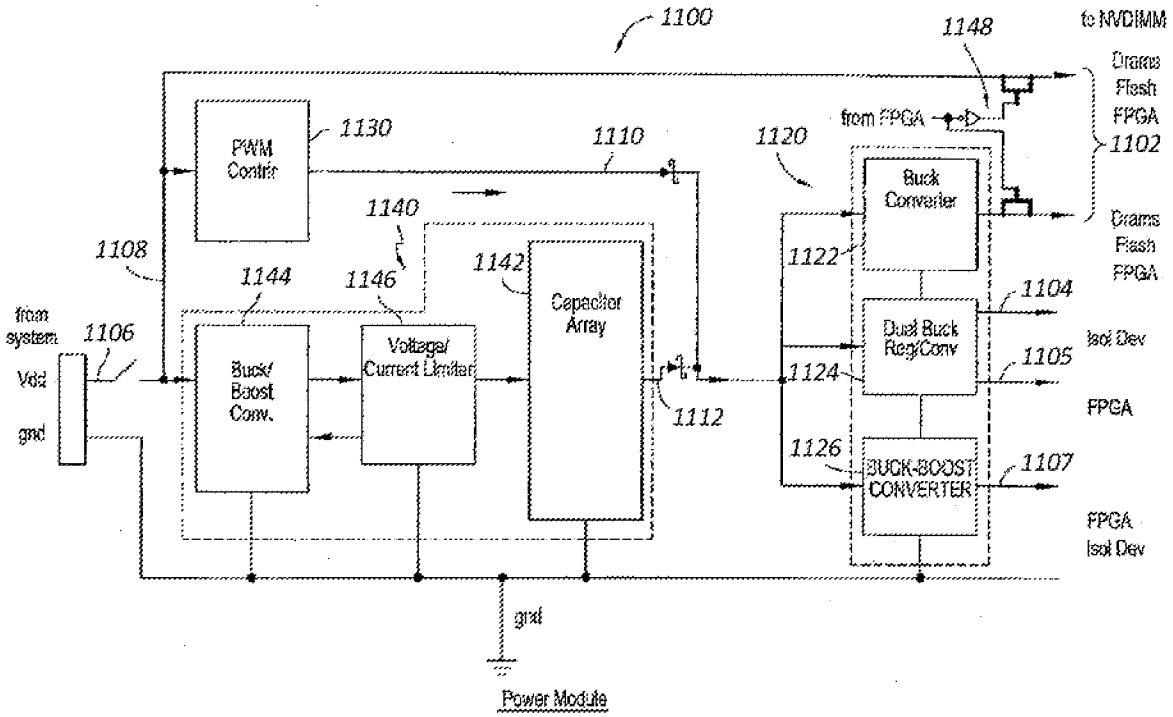


FIG. 16

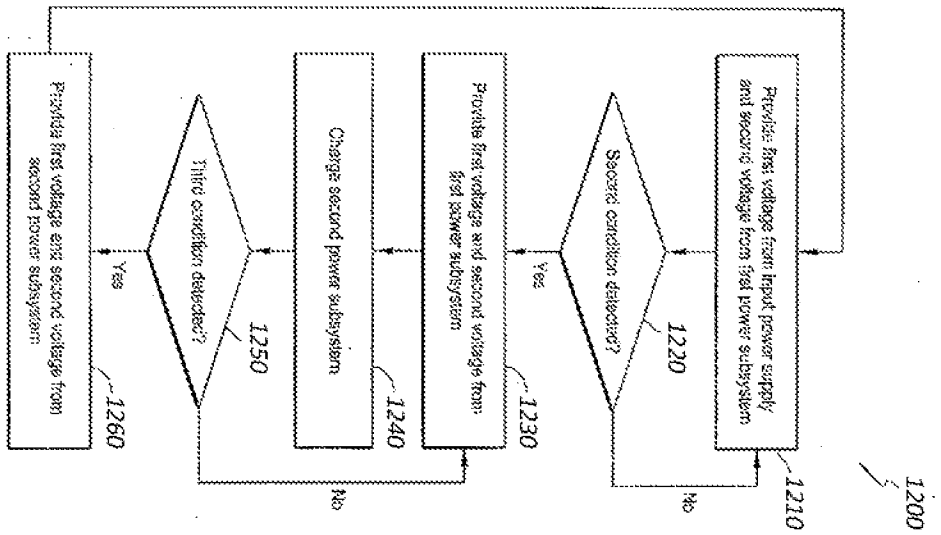

1200
Provide first voltage from input power supply and second voltage from first power subsystem
1210
Second condition detected?
1220
No
Yes
Provide first voltage and second voltage from first power subsystem
1230
Charge second power subsystem
1240
Third condition detected?
1250
No
Yes
Provide first voltage and second voltage from second power subsystem
1260

FIG. 17

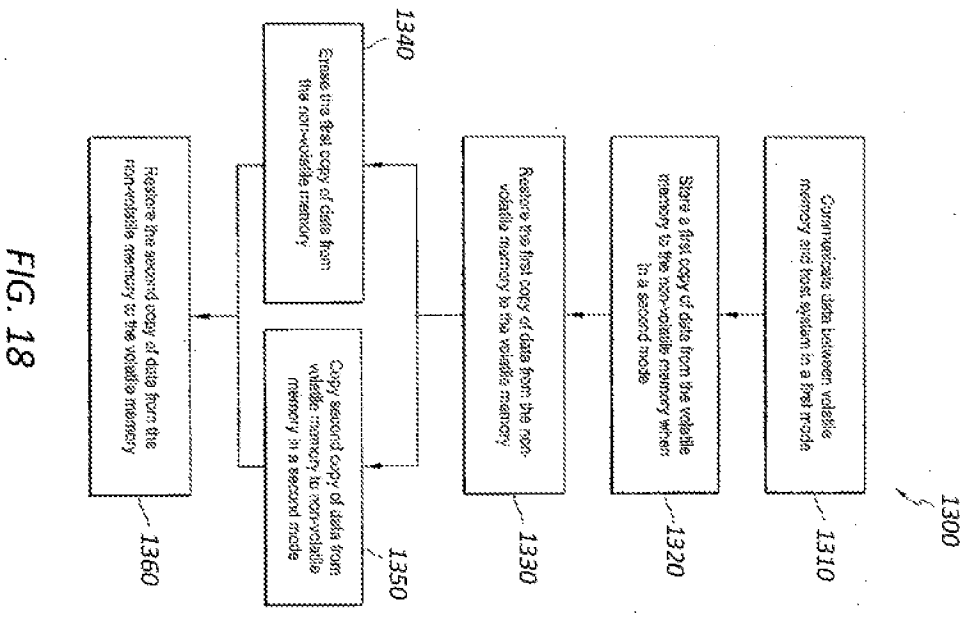

1300
Communicate data between volatile memory and host system in a first mode
1310
Store a first copy of data from the volatile memory to the non-volatile memory when in a second mode
1320
Restore the first copy of data from the non-volatile memory to the volatile memory
1330
Copy second copy of data from volatile memory to non-volatile memory in a second mode
1350
Erase the first copy of data from the non-volatile memory
1340
Restore the second copy of data from the non-volatile memory to the volatile memory
1360

FIG. 18

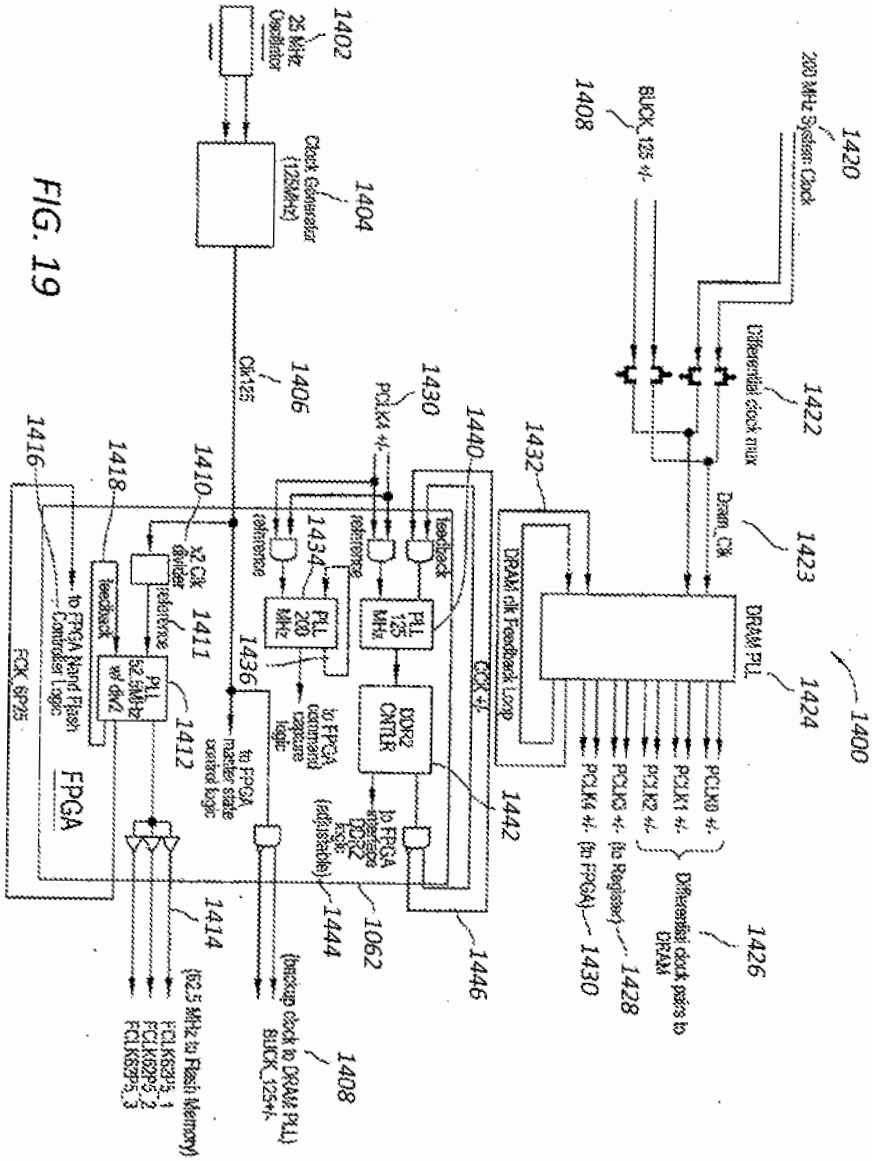

1420
200 MHz System Clock
1422
Differential clock mux
1423
Dram_Clk
1424
DRAM PLL
1400
1408
BUCK_125 +/-
PCLK0 +/-
PCLK1 +/-
PCLK2 +/-
Differential clock pairs to DRAM
1426
PCLK3 +/- (to Registers)
1428
PCLK4 +/- (to FPGA)
1430
1432
DRAM clk Feedback Loop
1440
DCM #2
1442
1446
1402
25 MHz Oscillator
1404
Clock Generator (125MHz)
1406
Clk125
1410
1430
PCLK4 +/-
1434
feedback
reference
PLL 125 MHz
PLL 200 MHz
1436
DDR2 CNTLR
to FPGA command capture logic
to FPGA master state control logic
to FPGA memory DDR2 clock (adjustable)
1444
1062
1408
(backup clock to DRAM PLL) BUCK_125+/-
1411
x2 Clk divider
reference
PLL 62.5MHz w/ clk/2
1412
1414
(62.5 MHz to Flash Memory)
FCLK62P5_1
FCLK62P5_2
FCLK62P5_3
1416
1418
feedback
to FPGA Nand Flash Controller Logic
FCK_62P5
FPGA

FIG. 19

REPLACEMENT SHEET

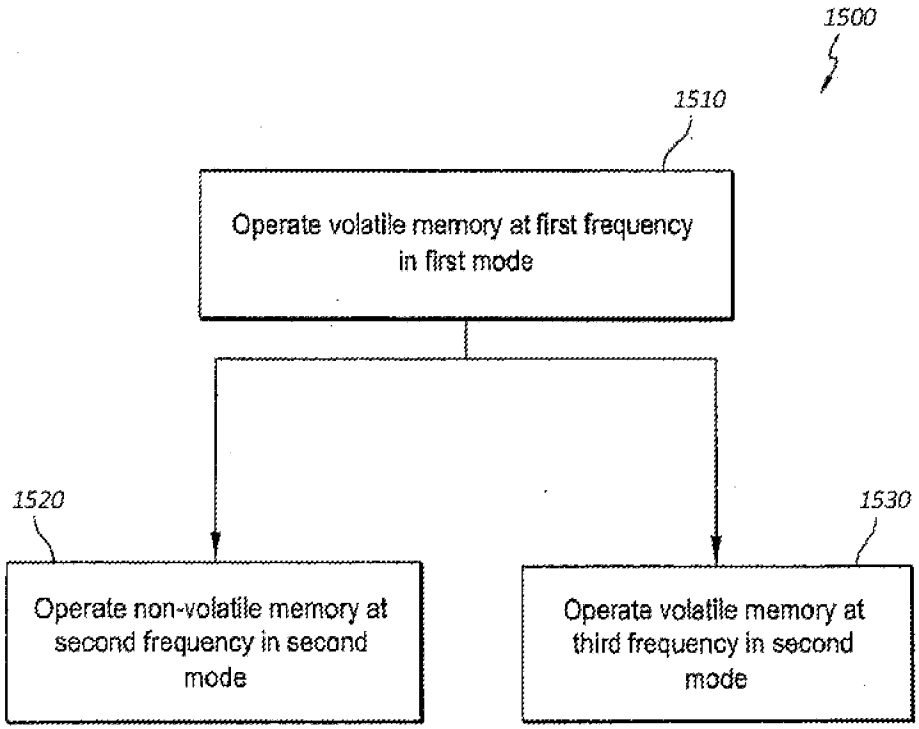


FIG. 20

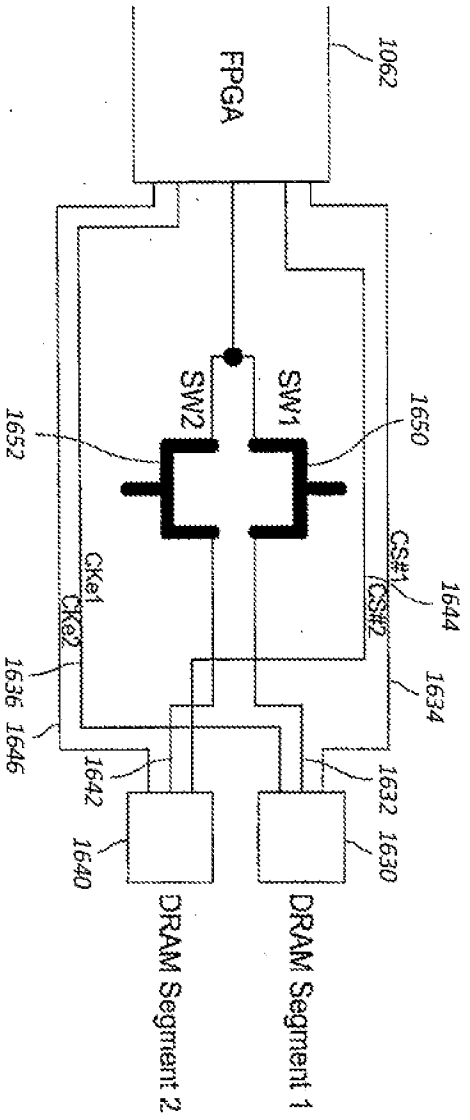

FPGA
1062
SW2
SW1
1652
1650
CKe1
CKe2
CS#1
CS#2
1644
1636
1646
1634
1642
1632
1640
1630
DRAM Segment 2
DRAM Segment 1

FIG. 21

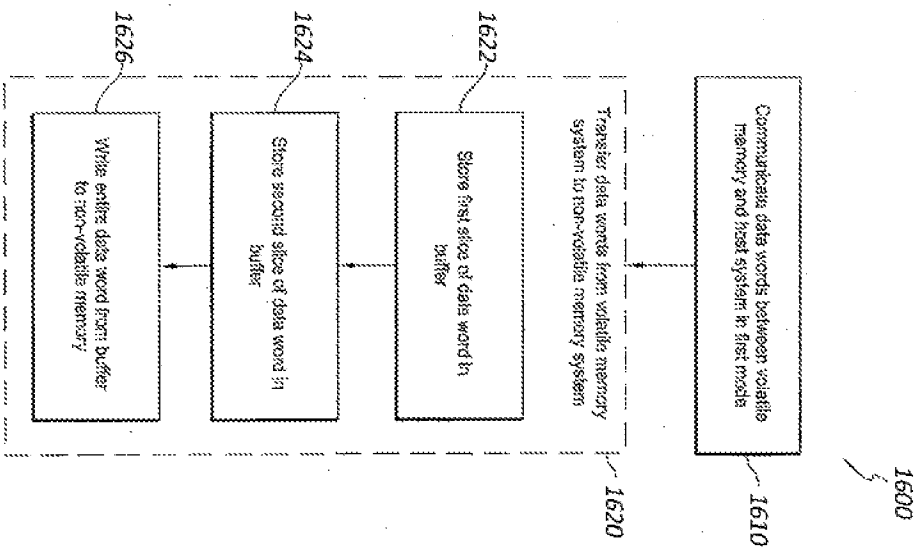

1600
1610
Communicate data words between volatile memory and host system in first mode
1620
Transfer data words from volatile memory system to non-volatile memory system
1622
Store first slice of data word in buffer
1624
Store second slice of data word in buffer
1626
Write entire data word from buffer to non-volatile memory

FIG. 22

Electronic Patent Application Fee Transmittal

Application Number:	17582797
Filing Date:	24-Jan-2022
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Khaled Shami/Yayoi Bourne
Attorney Docket Number:	022955-000090

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
Pages:				
Claims:				
Miscellaneous-Filing:				
LATE FILING FEE FOR OATH OR DECLARATION	1051	1	160	160
Petition:				

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Ex. 1002, p. 152

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**1980**

Electronic Acknowledgement Receipt

EFS ID:	45385028
Application Number:	17582797
International Application Number:	
Confirmation Number:	3546
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000090
Receipt Date:	04-APR-2022
Filing Date:	24-JAN-2022
Time Stamp:	11:48:53
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1980
RAM confirmation Number	E202244B49101498
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Applicant Response to Pre-Exam Formalities Notice	022955-000090_RNFMP.pdf	421552 9a89c778d707d67e4f0ec06de84875ee2fcb2be2	no	3
Warnings:					
Information:					
2		022955-000090_RNFMP_PA.pdf	6371403 9afe3ed9a4daea78de44d874851f2a3a34ceeeea	yes	25

Multipart Description/PDF files in .zip description

Document Description	Start	End
Preliminary Amendment	1	1
Drawings-only black and white line drawings	2	2
Applicant Arguments/Remarks Made in an Amendment	3	3
Drawings-only black and white line drawings	4	25

Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	46679 9d1243a43dc1c7b60741c7a239f0ce56ba52aba9	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	6839634	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Chi-She Chen, et al.

Appl. No.: 17/582,797
Filing Date: January 24, 2022
Exam: Not Yet Assigned
Art Unit: 1731
Conf.: 3546
Title: **FLASH-DRAM HYBRID MEMORY MODULE**

RESPONSE TO NOTICE TO FILE MISSING PARTS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

This paper is submitted in response to the Notice to File Missing Parts mailed February 2, 2022, making a response due on or before April 2, 2022. Accordingly, this response is timely filed. Submitted herewith are the following:

1) Preliminary Amendment
2) Replacement Drawings
3) Fee payment of $1,980, for the surcharge ($160), basic filing fee ($320), the search fee ($700), and the examination fee ($800).

It is submitted that the amendment submitted herewith overcomes the requirement for additional claim fees. The remaining required fees are filed by EFS-WEB.

In view of the foregoing, Applicant respectfully submits that the application is in condition for examination on the merits. The Examiner is invited to contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

/Khaled Shami/
Khaled Shami, Registration No.: 38745
Customer No.: 151145

Date: April 4, 2022

VORYS, SATER, SEYMOUR and PEASE LLP
1909 K Street, NW, 9th Floor
Washington, DC 20006-1152
Tel: (202) 467-8800

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/582,797	01/24/2022	Chi-She Chen	022955-000090

CONFIRMATION NO. 3546

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

FORMALITIES LETTER

OC000000131510000

Date Mailed: 02/02/2022

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

The application is informal since it does not comply with the regulations for the reason(s) indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- Replacement drawings in compliance with 37 CFR 1.84 and 37 CFR 1.121(d) are required. The drawings submitted are not acceptable because:
  - The drawings submitted to the Office are not electronically reproducible because portions of figures 17 - 19, & 22 are missing and/or blurry.

Applicant is cautioned that correction of the above items may cause the specification and drawings page count to exceed 100 pages. If the specification and drawings exceed 100 pages, applicant will need to submit the required application size fee.

- The statutory basic filing fee is missing.
- The application search fee must be submitted.
- The application examination fee must be submitted.
- Surcharge as set forth in 37 CFR 1.16(f) must be submitted.
  The surcharge is due for any one of:
  - late submission of the basic filing fee, search fee, or examination fee,
  - late submission of inventor's oath or declaration,
  - filing an application that does not contain at least one claim on filing, or
  - submission of an application filed by reference to a previously filed application.

SUMMARY OF FEES DUE:

The fee(s) required within **TWO MONTHS** from the date of this Notice to avoid abandonment is/are itemized below. No entity status discount is in effect. If applicant is qualified for small entity status, a written assertion of

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Ex. 1002, p. 158

small entity status must be submitted to establish small entity status. (See 37 CFR 1.27). If applicant is qualified for micro entity status, an acceptable Certification of Micro Entity Status must be submitted to establish micro entity status. (See 37 CFR 1.29 and forms PTO/SB/15A and 15B.)

- $ **320** basic filing fee.
- $ **160** surcharge.
- $ **700** search fee.
- $ **800** examination fee.
- $(**0**) previous unapplied payment amount.
- $ **1980** TOTAL FEE BALANCE DUE.

Replies must be received in the USPTO within the set time period or must include a proper Certificate of Mailing or Transmission under 37 CFR 1.8 with a mailing or transmission date within the set time period. For more information and a suggested format, see Form PTO/SB/92 and MPEP 512.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web, including a copy of this Notice and selecting the document description "Applicant response to Pre-Exam Formalities Notice". https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/afessehaye/

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Amendments to the drawings:

Please enter the twenty two (22) sheets of Replacement Drawings attached herewith.

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Ex. 1002, p. 160

Remarks

Each of the required items identified in the Notice of Missing Parts has been provided.

Applicant submits herewith replacement sheets for all figures. Applicant submits that the drawing sheets are in compliance with 37 CFR 1.84 and 1.121(d). No new matter has been added.

Applicant reserves the right to reintroduce any cancelled subject matter to this application or to any child applications, or to reintroduce the full scope of any the original or previous claim amended herein, in a continuing application.

Accordingly, the Examiner is respectfully requested to enter the above amendments. Favorable consideration is requested.

Conclusion

In view of the foregoing, Applicant respectfully submits that the application is in condition for allowance. The Examiner is invited to contact the undersigned attorney if it is believed that such contact will expedite the granting of the application.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of this paper, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Vorys, Sater, Seymour and Pease LLP
1909 K Street, N.W.9th Floor
Washington, D.C. 20006
Phone: (202) 467-8843
Fax: (202) 467-8800

Respectfully submitted,
/Khaled Shami/
Khaled Shami
Reg. No. 38745
Date: April 4, 2022

Samsung Electronics Co., Ltd.
Ex. 1002, p. 161

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number: 17/582,797

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	700
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800
TOTAL CLAIMS (37 CFR 1.16(i))	1 minus 20 =	*			OR	x 100 =	0.00
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1 minus 3 =	*				x 480 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
	Application Size Fee (37 CFR 1.16(s))									
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
17/582,797	01/24/2022	1731	1980	022955-000090	1	1

CONFIRMATION NO. 3546

UPDATED FILING RECEIPT

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

OC000000132950211

Date Mailed: 04/06/2022

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA;

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 17/328,019 05/24/2021 PAT 11232054
which is a CON of 17/138,766 12/30/2020 PAT 11016918
which is a CON of 15/934,416 03/23/2018 ABN
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

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Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

Permission to Access Search Results: Yes

Applicant may provide or rescind an authorization for access using Form PTO/SB/39 or Form PTO/SB/69 as appropriate.

If Required, Foreign Filing License Granted: 02/01/2022

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/582,797**

Projected Publication Date: 07/14/2022

Non-Publication Request: No

Early Publication Request: No
Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

501

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

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Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4258).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

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The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/582,797	01/24/2022	Chi-She Chen	022955-000090

CONFIRMATION NO. 3546

151145
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

PUBLICATION NOTICE

OC000000135164891

Title:FLASH-DRAM HYBRID MEMORY MODULE

Publication No.US-2022-0222191-A1
Publication Date:07/14/2022

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently https://portal.uspto.gov/pair/PublicPair. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

151145 7590 10/12/2022

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2135	

NOTIFICATION DATE	DELIVERY MODE
10/12/2022	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

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Ex. 1002, p. 168

Office Action Summary	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 01/24/2022.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☐ This action is **FINAL.** 2b) ☑ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 1 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 1 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/04/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☐ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date _____.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. The instant application having application No. 17/582,797 has a total of 20 claims pending in the application; there are 3 independent claim and 17 dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*3. As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING CLAIMS:

Double Patenting

4. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process... may obtain a patent therefor..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to

identical subject matter. See Miller v. Eagle Mfg. Co., *151 U.S. 186 (1894);* In re Vogel, *422 F.2d 438, 164 USPQ 619 (CCPA 1970);* In re Ockert, *245 F.2d 467, 114 USPQ 330 (CCPA 1957).*

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the claims that are directed to the same invention so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 1 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 11,016,918 B2. This is a statutory double patenting rejection.

1. Claim 1 of instant application (Application No. 17/582,797) is compared to claim 1 of Patent No. 11,016,918 B2 in the following table:

Patent No. 11,016,918 B2	***Application No. 17/582,797***
Claim 1:	***Claim 1:***
1. A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between	**1**. A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between

the memory module and the host system; a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated	the memory module and the host system; a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM)

voltage, and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein **a first one** of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.	devices coupled to the first regulated voltage, and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein **one** of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes.

Conclusion

The prior art made of record and not relied upon are as follows:

1. Chen et al. (US 20120271990 A1).

2. Bates (US 20070136523 A1).

3. Prete et al. (US 20080126624 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

October 6, 2022

Notice of References Cited	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	Page 1 of 1

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*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
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Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
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	HASHEM FARROKH	2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/06/2022								
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
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CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L1	1	"17582797"	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 08:56 AM
L2	1	("11232054").pn.	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 08:57 AM
L3	1	("11016918").pn.	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 10:06 AM
L5	732	(buck ADJ converter) WITH (regulated near2 voltage) WITH (voltage mear2 (amplitude OR value))	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 11:02 AM
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L8	0	7 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 11:20 AM
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L11	129	("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2022/10/06 11:34 AM

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		voltage)).clm.					
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PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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HF

1 - 50

Power control unit with digitally supplied system parameters

Methods and apparatuses provide voltage regulation for a processor. Control or configuration parameters for a voltage regulator (VR) are provided digitally over a configuration bus to a VR controller. The parameters may be provided directly from a storage element, or via a processing element or...

TAHOE RSCH LTD

US7685441 | US Patents | 2010-03-23 | 4

Power control unit with digitally supplied system parameters

Methods and apparatuses provide voltage regulation for a processor. Control or configuration parameters for a voltage regulator (VR) are provided digitally over a configuration bus to a VR controller. The parameters may be provided directly from a storage element, or via a processing element or...

TAHOE RSCH LTD

US8037328 | US Patents | 2011-10-11 | 4

Voltage regulator with multi-level, multi-phase buck architecture

A voltage regulator having a multi-level, multi-phase architecture is disclosed. The circuit includes a two-level buck converter and an N-level buck converter each coupled to an output node, wherein N is an integer value of three or more. During operation, the two-level buck converter provides one...

APPLE INC

US10886851 | US Patents | 2021-01-05 | 4

Voltage regulator with multi-level multi-phase buck architecture

A voltage regulator having a multi-level, multi-phase architecture is disclosed. The circuit includes a two-level buck converter and an N-level buck converter each coupled to an output node, wherein N is an integer value of three or more. During operation, the two-level buck converter provides one...

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WO2021050183A1 | WIPO Applications | 2021-03-18 | 4

Result 1

Relevance

Publication Date

1995

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A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are ...

https://patents.google.com › patent

DC-DC converter with a dynamically adapting load-line

Nov 27, 2018 — G05F1/461 Regulating voltage or current wherein the variable actually regulated by the final control device is dc using an operational ...

https://patents.google.com › patent

Multilevel buck converter with a flying capacitor and charge ...

Jan 9, 2018 — The multilevel DC-DC converter 110 includes an output node VOUT coupled between the central high-side primary switch 134 and the central low- ...

https://www.analog.com › media › Section1 PDF

point-of-load (POL) - Practical Power Solutions

Switching regulators, such as the buck (step-down) converter shown in 8, transfer energy from input to output via an inductor that has the voltage polarity ...

72 pages

https://www.ti.com › lit › pdf › slyt293 PDF

Understanding output voltage limitations of DC/DC buck ...

The buck converter is used to generate a lower output voltage from a higher DC input voltage. Texas Instruments Incorporated. Power Management. By John Tucker.

Missing: coupled plurality SDRAM

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Switching regulator fundamentals (Rev. C) - Texas Instruments

The buck converter uses a transistor as a switch that alternately connects and disconnects the input voltage to an inductor (see Figure 5).

https://www.eng.auburn.edu › Erikson_DC_2_DC PDF

DC-DC Power Converters

by RW Erickson · Cited by 258 — A basic dc-dc converter circuit known as the buck converter is illustrated ... double-throw (SPDT) switch is connected to the dc input voltage Vg as shown.

19 pages

Missing: SDRAM | Must include: SDRAM

https://www.maximintegrated.com › technical-documents

DC to DC Buck Converter Tutorial & Diagram - Maxim Integrated

Voltage-mode PWM · Current-mode PWM · Point-of-Load (POL) Boost Regulators · nanoPower Boost Converter · Buck Regulators · DDR Memory Power Supply Buck Controller.

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https://www.quora.com › Is-it-good-use-buck-converter-t...

Is it good use buck converter to supply microcontroller? - Quora

Yes of course. It's very popular, majority of MCU's and processors are powered by buck converters or its derivatives like the multiphase buck converter on ...

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How to Reconfigure a Buck Converter for Multiple Outputs

Introduction. Power supply circuits come in the form of voltage step-up (boost) or the more common step-down (buck). DC/DC converter.

Missing: plurality SDRAM

Related searches

point-of-load converter	**limitations** of buck **converter**
buck **converter** voltage **drop under load**	**point** of **load vs ldo**
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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**02/13/2023 05:29:16 PM ET**	**022955-000090**

Title of Invention

FLASH-DRAM HYBRID MEMORY MODULE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	61588211	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 100

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NPL--IDS1-16-21cv01453Document18-5-20220125_Segment1of28.pdf	37	Non Patent Literature	25439 KB
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NPL--IDS1-39-IPR2022-00999-PatOwnPrelimResp-2022-09-08_Segment2of2.pdf	FA05A1F57028105A4B9850B8BF57F14B13474BAA82923C5F206EE46C4CF2CF026D155DB95432EDD66BAA6249E19AD4FF202539F2F4B165A4516D27A90B8DBE6F
NPL--IDS1-40-IPR2022-00999-InstitDecision-2022-12-06_Segment1of2.pdf	AA62B5B60D330565AC010B8A9C0FE679B7F127BEEB78817AC03C49AC743145DA1E96FFB1116085DA6C914217899146259ED254AE18ED1D955DC50A4CD5AEE942
NPL--IDS1-40-IPR2022-00999-InstitDecision-2022-12-06_Segment2of2.pdf	CA1DDEA7986072760072BBC4DB048686E001108FF47FAA05AF9866D9A18C4AE35B2E98CFA17ADC0BF6DC0CB7B9B4DEDFC20AFE2CBB9F25224037EEFABB6357D2
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment1of10.pdf	5C44783A37A559D81CCEE8B5375A8019FEE71D27ECD80B56181B5EEF33947CF16E6D1E747988B5B826EFF3DBF8CFAC73EBE97F2BE704FD44D42CA0A17402EAD4
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment2of10.pdf	6A92A1B3929CC0471CD03F932A745875771921A6567D76DD972C23D005B074A3DA435660CBD36F01438B539EC3E34735723D6B19EEC7DC4AE00896634DA8FDC1
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment3of10.pdf	33916FCB6A372B4AA130B741BC9D63C4ED68E4A9F2FFB7CC11ACA3EE9DA01293AD04BE2C25B14F9BDBC176D0719875C62D4F21DA4E5E5F74548C59C11D37451F

NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment4of10.pdf	CBAE62F48A53273867A88F28D3E87F55B802D586AAA5CC028285311FF7CB09FE5671AD67F6F00F8C499A00077FE5C2807B298A398EBDC783A2DB62EA72B6DF26
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment5of10.pdf	C92AB94D779D2D54D22A0F5287CE7BB4DFF29B6FABA48D0F7BFF12DD6D7AEDFB972B635B328294C5F3D0DEFF0422239E651EADECDC5FFD8BF3C6426F2BEA80DE
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment6of10.pdf	53968BC21AEBAE57D2C66E87919148695FAE5E5407053DCEBBBAA8EB28C136564FB83653594D47165E598D1CBA1874AF883024CA7D60E99AA838B9CE9C547480
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment7of10.pdf	3EDFE913F74E4C12817C5790FBB50A1F64DFB4332F090FFF024502F55CEE37A2049806C95AE070EE20647E1C0AFE6326604062D67EB22B8955D31AA7BFD63480
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment8of10.pdf	1208E96545EF705B9AB6A062441668DA3247970830F7AEB358A1B66DE2BC76040B8E70490DFC2762C20A19EA35C09088256CB68ADBFFA1345C6105D1261506CD
NPL--IDS1-41-IPR2022-00996-Exhibit1003-WolfeDecl-918Pat-2022-05-17_Segment9of10.pdf	5D44A26E0CD1A978AB15716BE664B1C6E768D7868B447DA8F120DEFDA40DE40A6F3FED32D5C9202350FD5DE6641BF364D1D30CA21B1A7CB0480DE469AE463D3A
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NPL--IDS1-42-IPR2022-00999-Exhibit1003-WolfeDecl-054Pat-2022-05-17_Segment1of9.pdf	CCC9860BCEB48C3BE8F86195D1DDD5823F5D3D5851B1F640A5B887E8276775C24F3D8E97ED19C9B5544DE0ABB5F985413052167A04642437961A87EF05BBF36F
NPL--IDS1-42-IPR2022-00999-Exhibit1003-WolfeDecl-054Pat-2022-05-17_Segment2of9.pdf	9E53DC0E6B6E73C52058EBD09D338ABF4FCC73FD976046E267398D8EE9F6CEE0F6FCBC063B4513C820AE31DCDBB13FC5C332F3126A7D168D2F29C51EE9238C98
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NPL--IDS1-42-IPR2022-00999-Exhibit1003-WolfeDecl-054Pat-2022-05-17_Segment4of9.pdf	59F47AE874FF5C83730B1D587FC6C290BDC4F27C874C6BEA A85432DFA67761C0E48FB199A3A39C1F5505F8012564107411 CDA000546914EF6B1E372934FBFEB2
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NPL--IDS1-42-IPR2022-00999-Exhibit1003-WolfeDecl-054Pat-2022-05-17_Segment7of9.pdf	C622FC2A00C057C4F1AA60CDC91565B80938A8673E747FF61 42A4FA155FA98BF9005210C2D8045C523F5C2FD5278EFF3356 D23D29E16268A8302037A69B7445E
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NPL--IDS1-42-IPR2022-00999-Exhibit1003-WolfeDecl-054Pat-2022-05-17_Segmeni9of9.pdf	FC5F821A6A30C6850935D0B694109993C082238B5195761A549 7F05BD442D5D85C1FF6BA9755FA607ABA824DAE95505766BE 611F032714464DA6410D82E97B39
NPL--IDS1-43-IPR2022-00996-Exhibit1014-IPR2014-00994-Paper1-2022-05-17_Segment1of2.pdf	07C7346DBEEDACC13AF5D1D8DF62F46342D4726B1D5B0BC9 9616A8FCBD03800C32E125A9059D4F8D62A70D2975A2FB3A1 DDFC04E3AA4204A44B9E2937DEB8B4E
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NPL--IDS1-44-IPR2022-00996-Exhibit1015-IPR2014-00994-Paper8-2022-05-17.pdf	535215158DB222348271F2A2C5371674B3DB8A4287D2984B41 0EA75D60F397CCA5F644BF86485F25D8E10B895BAB7953A19 DA0CEAAAA9430E56DC27BA2EF30FC
NPL--IDS1-45-IPR2022-00996-Exhibit1016-IPR2014-01370-Paper8-2022-05-	82C641239B01ED6789413A93212056FCD91402905D662644221 C25F7301F6F718EC38386E72FDE0F3320BEEAB5486FB36A44 05FD94BA99F2B70FBA99DCBA3839

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NPL--IDS1-45-IPR2022-00996-Exhibit1016-IPR2014-01370-Paper8-2022-05-17_Segment2of2.pdf	3BB3B603250BE450CD66D02ECA6ACFD9D6FF903CBCCF4038133FE2AEA35CE15EA66706F1B01F85F22C9EC72A6FD5B16432EE5CF520BFF00820050A792BB2221A
NPL--IDS1-46-IPR2022-00996-Exhibit1017-IPR2014-01370-Paper13-2022-05-17.pdf	08DB422BFFD8D68423765D7AD45D7BF2BE895928E0762E67AC11DD7CE844BCD8E873462F63BC4F6565198B5997B686BD4BDD5748F02C4A195453443225O673AC
NPL--IDS1-47-IPR2022-00996-Exhibit1018-IPR2017-00649-Paper1-2022-05-17_Segment1of2.pdf	0EDCA957538DC9FC90422BE01C14BFAD420C1522874BB6536E2AEEDD210B344A7BF31442C8782CC3AA30203DC3910371EEAE20BF18BE8441E6E03519ACEB22B7
NPL--IDS1-47-IPR2022-00996-Exhibit1018-IPR2017-00649-Paper1-2022-05-17_Segment2of2.pdf	87F02A47F19C47CF17D2EEE7F4121395D35438782CDD724856A31E5970AD9701CDF2EBEADD89A77917F85213115F5675A50F0DACA65535F3B77E855EC71488D2
NPL--IDS1-48-IPR2022-00996-Exhibit1019-IPR2017-00649-Paper7-2022-05-17.pdf	BC983A5B2DF0A553A8757FBF08312680CACA2874E4D9BEA3BC26C6BA770BF2C1614C7A81562D29F036F743AD473CC95392EACF49B241F568A4348913956B95DD
NPL--IDS1-49-IPR2022-00996-Exhibit1005-60941586FileHist-2022-05-17.pdf	D79A7FB579CD46BF49A5755F8D885D539B7840A0AFCE8EBDCCA18DAFE4BAFF7CA71F4EC010894D0DCE59A9DC63ED14AD75F328A4387DCDEB7BFBA7EDD0E14840
NPL--IDS1-50- IPR2022-00996-Exhibit1006-12131873FileHist-2022-05-17_Segment2of2.pdf	DBCCA1D5FD2CF0A9F2E6A4F9F7C1E4709836861760D0D9708367AB611AA3A1A8121F889726EEEB3FF4BEDCFD645BB93D4984C73AE94FE0222C9DDA4DDDA0905A6
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Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	3	Exhibits of Complaint, Document 1-1, Case 1:21-cv-01453, filed October 15, 2021.	
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	45	IPR2014-01370 Paper 8, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22, 2014. (Exhibit 1016 of IPR2022-00996 and IPR2022-00999).
	46	IPR2014-01370 Paper 13, Institution Decision, dated March 13, 2015. (Exhibit 1017 of IPR2022-00996 and IPR2022-00999).
	47	IPR2017-00649 Paper 1, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017. (Exhibit 1018 of IPR2022-00996 and IPR2022-00999).
	48	IPR2017-00649 Paper 7, Institution Decision, dated July 24, 2017. (Exhibit 1019 of IPR2022-00996 and IPR2022-00999).
	49	US60/941586 File History. (Exhibit 1005 of IPR2022-00996 and IPR2022-00999).
	50	US12/131873 File History. (Exhibit 1006 of IPR2022-00996 and IPR2022-00999).

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	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

EXAMINER SIGNATURE			
Examiner Signature		Date Considered	

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(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-02-13
Name/Print	Khaled Shami	Registration Number	38745

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**02/13/2023 05:14:52 PM ET**	**022955-000090**

Title of Invention

FLASH-DRAM HYBRID MEMORY MODULE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	61587828	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 90

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2023-02-13 IDS1.pdf	11	Information Disclosure Statement (IDS) Form (SB08)	626 KB
NPL--IDS1-01-21cv00463Document1-20211220_Segment1of9.pdf	44	Non Patent Literature	25139 KB
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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First Named Inventor	CHEN
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Examiner Name	FARROKH
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	1	IPR2017-00692 Paper 1, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017. (Exhibit 1020 of IPR2022-00996 and IPR2022-00999).	
	2	IPR2017-00692 Paper 25, Institution Decision, dated July 5, 2018. (Exhibit 1021 of IPR2022-00996 and IPR2022-00999).	
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	13	Double Data Rate (DDR) SDRAM Specification, JEDEC Standard JESD79, June 2000. (Exhibit 1045 of IPR2022-00996 and IPR2022-00999).	
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	Attorney Docket Number	022955-000090

	45	SDR SDRAM, MT48LC16M4A2 – 4 Meg x 4 x 4 Banks, MT48LC8M8A2 – 2 Meg x 8 x 4 Banks, MT48LC4M16A2 – 1 Meg x 16 x 4 Banks, 64Mb: x4, x8, x16 SDRAM, Micron, 64mb_x4x8x16_sdram.pdf - Rev. V 05/15 EN. (EX2026 of IPR2022-00996 and IPR2022-00999).	
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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-02-13
Name/Print	Khaled Shami	Registration Number	38745

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APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**02/13/2023 05:44:14 PM ET**	**022955-000090**

Title of Invention

FLASH-DRAM HYBRID MEMORY MODULE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	61588381	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

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Digest

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NPL--IDS2-27-IPR2022-00996-EX2007-LP2996N-2022-09-09.pdf	66627DADB7FDB5255E61420BD9D59C3DB609CA99C8671424D5F975A57E07B82DC7A2ECD92D327C5B6F6D985BED3981F24ED5E9446313244F7B71ECA629DBCA9E
NPL--IDS2-28-IPR2022-00996-EX2008-LP2996-2022-09-09.pdf	4C9B54C7F9C8FD2210F6D9AD91582B47E7ABDEED76FA420E1BD68004F9B8DB2BB047399B8483D47D768BBDA5205B985E96C048DF8E4373B279E7A93CD8C735EC
NPL--IDS2-29-IPR2022-00996-EX2009-LP2997-2022-09-09.pdf	4B147E1198A2925ED256BA6E57CABD9C7DA972FB95940D7C8D0F5C7E2BBA93CF175FA3110CE426DC9949CF19B3F45C72D12360D420E3128CCEFEC0C7BBE5CDAD
NPL--IDS2-30-IPR2022-00996-EX2010-LP2998-2022-09-09.pdf	102A838376DF03F7C053187CDA80ACC4E70D1ECEF8EFCC0D18AD3CAF563B5966EE189918079345E891E5359172F7B66E15948119FC10B27FA1ACFD9F97F7DFEC
NPL--IDS2-31-IPR2022-00996-EX2011-Bergveld-2022-09-09_Segment1of8.pdf	DADB66E7A2F595560ADFB6A1DBE9B71B217876745EC1908885B1875A2AE409BE861A7875576D11D69CC329C419FE98245939EDABC47060E9C6D7D0FFDE6134DA

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NPL--IDS2-32-IPR2022-00996-EX2012-Romo-2022-09-09.pdf	EC97FFA56F2B3AC16369A57C36F6EC950B26D4E0FCF0BD587CDA7FDB774C4A3F184DA70399FB9F451F44AA351A00ABDC9A5F8CBC45DB1902E80A97EE1D52B33A
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NPL--IDS2-41-IPR2022-00996-EX2022-ElectronicDesign-2022-09-09.pdf	4F35832549D91687B6842D9D1A0DD6F0C419A6D25A4BCDD7F62D0D8393F0F9D6E12838104E4FCC8501D8D9CDDA528EB43D1E536C377C81812ED482B3079717A3
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NPL--IDS2-43-IPR2022-00996-EX2024-Schmid-2022-09-09.pdf	38C2925208831EE9F973CB21E1B2E2E3E9ED8F65AFF11E25A84197737BC97FF03EE6F81F0BF8BCC8B837D15875945C44AB389B8ACA68294D4C2632F2F902D3F4
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NPL--IDS2-46-IPR2022-00996-EX2027-DDR2-SO-DIMM-2022-09-09.pdf	0B24F141143E94CF21124E133D5CF372BB155DA5A2A105ACFD6A5826A7876C776437E1501E0D6D40CA7FC994FF0B0FEA98EEE44D56E1984D043982A44CD41EA9
NPL--IDS2-47-IPR2022-00996-EX2028-TN-41-13-2022-09-09.pdf	E71F84D2F6EA355C104A4DDD24B1A55BE33C68AD2ACAC425068C7DA0C50BB936DB4D5956DE430F0B9B61990787D0F4CCAEAB577B400D316230372E1997E9FEF7
NPL--IDS2-48-IPR2022-00996-EX2029-PCIOverview-2022-09-09.pdf	177AB36A9ADB7662BFF4B88C454F77A5CD2F017CCF5B607DCA8180128009C241EEB4E19EC7DF305868CDA31CF21F8C94CC658D875D7D743D33719C02FFEE5692
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(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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	2	10860506		2020-12-08	Netlist, Inc.	
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That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-02-13
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	02/13/2023 10:10:10 PM ET	022955-000090

Title of Invention

FLASH-DRAM HYBRID MEMORY MODULE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	61588621	AUTHORIZED BY	Khaled Shami
CUSTOMER #	151145	FILING DATE	01/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Chi-She Chen

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 220585	E20232CM11255902	Lisa Elliott

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1806	SUBMISSION OF AN INFORMATION DISCLOSURE STATEMENT	260.00	1	260.00
			TOTAL AMOUNT:	$260.00

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

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CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 58

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2023-02-13 IDS3.pdf	8	Information Disclosure Statement (IDS) Form (SB08)	625 KB
NPL--IDS3-01-288pin_Samsung.pdf	42	Non Patent Literature	744 KB
NPL--IDS3-02-288pin_Rev14_Samsung.pdf	41	Non Patent Literature	24411 KB
NPL--IDS3-03-JESD82-32A.pdf	6	Non Patent Literature	542 KB
NPL--IDS3-04-JESD79-4C.pdf	3	Non Patent Literature	1690 KB

NPL--IDS3-05-JESD301-1.pdf	3	Non Patent Literature	115 KB
NPL--IDS3-06-JESD79-5.pdf	7	Non Patent Literature	3553 KB
NPL--IDS3-07-JESD82-511.pdf	7	Non Patent Literature	145 KB
NPL--IDS3-08-JESD82-32.pdf	148	Non Patent Literature	3812 KB
NPL--IDS3-09-JESD82-31_Segment1of2.pdf	81	Non Patent Literature	25363 KB
NPL--IDS3-09-JESD82-31_Segment2of2.pdf	69	Non Patent Literature	16864 KB
NPL--IDS3-10-JESD82-29_Segment1of2.pdf	53	Non Patent Literature	25567 KB
NPL--IDS3-10-JESD82-29_Segment2of2.pdf	17	Non Patent Literature	5439 KB
NPL--IDS3-11-JESDxx-x proposal_Segment1of2.pdf	48	Non Patent Literature	25464 KB
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NPL--IDS3-26-JESD82-31A.pdf	27	Non Patent Literature	2596 KB
NPL--IDS3-27-JEDEC21C.pdf	9	Non Patent Literature	838 KB
NPL--IDS3-28-IPR202300406Petition.pdf	151	Non Patent Literature	3752 KB
NPL--IDS3-29-IPR202300405Petition.pdf	147	Non Patent Literature	2240 KB
NPL--IDS3-30-IPR2022-00418-PrelimResp.pdf	71	Non Patent Literature	1425 KB
NPL--IDS3-31-IPR2022-00418-PatOwnResp.pdf	60	Non Patent Literature	1757 KB
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NPL--IDS3-36-IPR202200418-Ex1019_Segment2of2.pdf	56	Non Patent Literature	23962 KB
NPL--IDS3-37-IPR202200418-Ex2003.pdf	2	Non Patent Literature	926 KB
NPL--IDS3-38-IPR202200418-Ex2004.pdf	58	Non Patent Literature	1327 KB
NPL--IDS3-39-IPR202200418-Ex2005_Segment1of5.pdf	66	Non Patent Literature	25584 KB
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NPL--IDS3-39-IPR202200418-Ex2005_Segment3of5.pdf	64	Non Patent Literature	25341 KB
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Digest

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NPL--IDS3-30-IPR2022-00418-PrelimResp.pdf	D82F19F71B1476E272C44D4BD28BFBE8B092896D4DDFE894461FB08483FBECC3E3C37C3B2C09AA1F6051D4EFB765E6D3CD1F57BABBEBCD3307907C1895FC4DC3
NPL--IDS3-31-IPR2022-00418-PatOwnResp.pdf	3215F47B4E98B0D90DAD2919FEDBA67E248BEF47C03C87B217FC3F24C5F4735D4FDF013EFCD0747053C4AF931E1292879D4D8B12305A10585CA0B3CA55759911
NPL--IDS3-32-IPR202200418-Ex1003_Segment1of4.pdf	1C1C31606A2006EFAE92824DB81DFFD0C8CF1DF4C148C813FA35A00A19D47D0F09F7BD4679BD57EA1F9483761E53B73570B3B3C8B0D146BDF69425FB8BD946E8
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NPL--IDS3-40-IPR202200418-Ex2006.pdf	A14D950F370A30329273649BB4AFC21104FA00A8C5EC906D63D175E54A6277AE30DAD4C3785151E71F947D5EE697799A29B7A0BAF117CE5E12EC6EE6304C9AA7

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	04/12/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/TAWANA E CAMPBELL/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PTO/AIA/22 (12-22)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PETITION FOR EXTENSION OF TIME UNDER 37 CFR 1.136(a)

Docket Number (Optional): 022955-000090

Application Number: 17/582,797

Filed: January 24, 2022

For: FLASH-DRAM HYBRID MEMORY MODULE

Art Unit: 2138

Examiner: FARROKH

This is a request under the provisions of 37 CFR 1.136(a) to extend the period for filing a reply in the above-identified application.

The requested extension and fee are as follows (check time period desired and enter the appropriate fee below):

	Fee	Small Entity Fee	Micro Entity Fee	
☐ One month (37 CFR 1.17(a)(1))	$220	$88	$44	$
☐ Two months (37 CFR 1.17(a)(2))	$640	$256	$128	$
☑ Three months (37 CFR 1.17(a)(3))	$1,480	$592	$296	$ 1480
☐ Four months (37 CFR 1.17(a)(4))	$2,320	$928	$464	$
☐ Five months (37 CFR 1.17(a)(5))	$3,160	$1,264	$632	$

☐ Applicant asserts small entity status. See 37 CFR 1.27.

☐ Applicant certifies micro entity status. See 37 CFR 1.29.
Form PTO/SB/15A or B or equivalent must either be enclosed or have been submitted previously.

☐ A check in the amount of the fee is enclosed.

☐ Payment by credit card. Form PTO-2038 is attached.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☐ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment, to Deposit Account Number _____.

☑ Payment made via USPTO's patent electronic filing system (Patent Center or EFS-Web).

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

I am the

☐ applicant.

☑ attorney or agent of record. Registration number 38745.

☐ attorney or agent acting under 37 CFR 1.34. Registration number _____.

/Khaled Shami/ — Signature

April 12, 2023 — Date

Khaled Shami — Typed or printed name

202-467-8800 — Telephone Number

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. Submit multiple forms if more than one signature is required, see below*.

☑ * Total of 1 forms are submitted.

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0031. Public burden for this form is estimated to average 6 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS**. If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450**.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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Routine uses of the information in this record may include disclosure to: 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law; 2) a Federal, state, local, or international agency, in response to its request; 3) a contractor of the USPTO having need for the information in order to perform a contract; 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record; 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record; 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations; 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals; 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)); 9) the Office of Personnel Management (OPM) for personnel research purposes; and 9) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

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Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

Electronic Patent Application Fee Transmittal

Application Number:	17582797
Filing Date:	24-Jan-2022
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Filer:	Khaled Shami/Lisa Elliott
Attorney Docket Number:	022955-000090

Filed as Large Entity

Filing Fees for Utility under 35 USC 111(a)

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 3 months with $0 paid	1253	1	1480	1480
Miscellaneous:				
			Total in USD ($)	**1480**

Electronic Acknowledgement Receipt

EFS ID:	47832726
Application Number:	17582797
International Application Number:	
Confirmation Number:	3546
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Lisa Elliott
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000090
Receipt Date:	12-APR-2023
Filing Date:	24-JAN-2022
Time Stamp:	16:24:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	$1480
RAM confirmation Number	E20234BG25339706
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Amendment/Request for Reconsideration-After Non-Final Rejection	022955-000090__Resp_10-12-22_NFOA.pdf	127139 1d5b70088752cd4c46aa7ade3b44118c8fa6cc70	no	7
Warnings:					
Information:					
2	Extension of Time	EOTx3_large_022955-90.pdf	109762 32356f964227423fa705ad37c7e4a021d1444681	no	2
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	38123 f04f35518bfa4075263dfa637c4af1979d31afbc	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	275024		

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

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New International Application Filed with the USPTO as a Receiving Office

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONF. NO: 3546

APPLICATION NO: 17/582,797 ART UNIT: 2138

FILING DATE: January 24, 2022 EXAMINER: FARROKH

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

AMENDMENT AND/OR REPLY TO OFFICE ACTION

Commissioner:

In response to the non-final Office Action mailed October 12, 2022, Applicant submits the following Amendment and Remarks.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **6**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (New) A dual in-line memory module (DIMM) comprising:

a printed circuit board (PCB) including a set of voltage supply lines electrically connected to corresponding edge connections of a first set of edge connections, sixty four data lines electrically connected to corresponding edge connections of a second set of edge connections, and a set of address and control lines electrically connected to corresponding edge connections of a third set of edge connections;

a DIMM interface including the first, second and third set of edge connections, the DIMM interface configured to (i) fit into a memory socket connector of a host system, and (ii) provide a conduit for power, sixty four data signals, and address and control signals between the host system and the DIMM via the first, second and third set of edge connections, respectively;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) receive and monitor an input voltage from the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to other portions of the controller, wherein the controller is configured to perform one or more operations in response to the trigger signal, the one or more operations including a write operation to write data into the non-volatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a plurality of components coupled to the PCB, the plurality of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices; and

first, second, third and fourth buck converters coupled to the PCB and to the input

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Ex. 1002, p. 299

voltage supply line and configured to (i) receive power from the input voltage supply line, (ii) generate first, second, third and fourth regulated voltages from the power received from the input voltage supply line, and (iii) output the first, second, third and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively;

wherein each component of the plurality of components (i) is not electrically connected to the input voltage supply line, (ii) is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and (iii) receives power only from one or more of the first, second, third and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices (i) is not electrically connected to the input voltage supply line, and (ii) receives power only from one or more of the first, second, third and fourth regulated voltage lines.

3. (New) The DIMM of claim 2, wherein the controller is further configured to control a plurality of power transition sequences.

4. (New) The DIMM of claim 3, wherein the plurality of power transition sequences includes first and second power transition sequences, the first power transition sequence includes turning power on or off to the first regulated voltage line in response to a first trigger condition of a plurality of trigger conditions, and the plurality of trigger conditions includes a request from the host.

5. (New) The DIMM of claim 4, wherein the input voltage supply line is a first input voltage supply line, and wherein the first, second, third and fourth buck converters are coupled to a second input voltage supply line, and

wherein, during the second power transition sequence, the first, second, third and fourth buck converters are further configured to (i) receive power from the first input voltage supply line or the second input voltage supply line in response to a second trigger condition of the plurality of trigger conditions, (ii) generate the first, second, third and fourth regulated voltages from either the power received from the first input voltage supply line or the power received from the second input voltage supply line, and (iii) o output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively.

6. (New) The DIMM of claim 2, wherein the controller is further configured to generate a

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plurality of trigger signals in connection with a plurality of trigger conditions that include (i) a request from the host system and (ii) detecting input voltage deviation from one or more threshold voltages.

7. (New) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages specified as certain voltage values.

8. (New) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages corresponding to percentages of an operating voltage.

9. (New) the DIMM of claim 4, wherein the DIMM is configured to operate in a plurality of states including a first state and a second state, wherein the DIMM is further configured (i) to operate in the first state while power is turned on to the first regulated voltage line, and (ii) to operate in the second state while power is turned off to the first regulated voltage line.

10. (New) The DIMM of claim 9, wherein the first power transition sequence further includes turning power on to the plurality of DDR SDRAM devices, during both the first and second states, via one or more of the second, third and fourth regulated voltage lines.

11. (New) The DIMM of claim 10 further comprising:

a register coupled to the PCB, to the first regulated voltage line, and to the set of address and control lines, wherein:

during the first state, the register is configured to (i) receive and register address and control signals from the host via the set of address and control lines, and (ii) output registered address and control signals to the plurality of the DDR SDRAM devices, and

during the second state, the register does not couple address and control signals from the host to the plurality of the DDR SDRAM devices.

12. (New) The DIMM of claim 2, wherein the DIMM interface comprises a standard 240-pin DDR2 edge connector.

13. (New) The DIMM of claim 2, wherein the controller is further configured to periodically perform the one or more operations at regular intervals of time.

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14. (New) The DIMM of claim 13, wherein the regular intervals of time are every millisecond.

15. (New) The DIMM of claim 2, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

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REMARKS

The non-final Office Action mailed October 12, 2022, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

Upon entry of the foregoing amendment, claims 2-15 are pending in this application, with claim 2 being the independent claim.

Canceled Claims

Claim 1 has been canceled without prejudice or disclaimer of the subject matter contained therein.

Rejection(s) Pursuant to Judicially-Created Double Patenting

Claim 1 stands rejected pursuant to the judicially-created doctrine of obviousness-type double patenting as allegedly being unpatentable over claim 1 of U.S. pat. no. 11,016,918 B2. Claim 1 has been canceled without prejudice or disclaimer of its subject matter, and the double-patenting rejection thereof is moot.

Newly-Added Claims

Claims 2-15 have been added to further particularly point out and distinctly claim certain aspects of the invention.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

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If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: April 12, 2023
/Khaled Shami/
Khaled Shami, Reg. No. 38,745

Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

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Ex. 1002, p. 304

Notice of References Cited	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20120271990-A1	10-2012	Chen; Chi-She	G06F3/065	711/E12.008
*	B	US-20070136523-A1	06-2007	Bonella; Randy M.	G06F12/0866	711/E12.019
*	C	US-20080126624-A1	05-2008	Prete; Edoardo	G11C7/106	710/53
	D					
	E					
	F					
	G					
	H					
	I					
	J					
	K					
	L					
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FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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Ex. 1002, p. 305

Index of Claims	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/582,797	Chen et al.
	Examiner	**Art Unit**
	HASHEM FARROKH	2138

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIM		DATE								
Final	Original	10/06/2022	07/07/2023							
	1	✓	-							
	2		✓							
	3		✓							
	4		✓							
	5		✓							
	6		✓							
	7		✓							
	8		✓							
	9		✓							
	10		✓							
	11		✓							
	12		✓							
	13		✓							
	14		✓							
	15		✓							

Samsung Electronics Co., Ltd.
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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/582,797	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	17/582,797	Chen et al.
	Examiner	Art Unit
	HASHEM FARROKH	2138

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

Samsung Electronics Co., Ltd.
Ex. 1002, p. 308

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	~~2135~~ 2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	11016918		2021-05-25	Netlist, Inc.	
	2	8301833		2012-10-10	Netlist, Inc.	
	3	8874831		2014-10-28	Netlist, Inc.	
	4	9158684		2015-10-13	Netlist, Inc.	
	5	9928186		2018-03-27	Netlist, Inc.	
	6	7724604		2010-05-25	SMART Modular Technologies, Inc.	
	7	7719866		2010-05-18	Agence Spatiale Europeenne	
	8	7721130		2010-05-18	Qimonda AG	

All References Considered Except Where Lined Through. /H.F/

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	9	6798709		2004-09-28	Samsung Electronics Co., Ltd.	
	10	6856556		2005-02-15	Siliconsystems, Inc.	
	11	7023187		2006-04-04	Intersil Americas Inc.	
	12	7692938		2010-04-06	Northern Power Systems, Inc.	
	13	5563839		1996-10-18	Simtek Corporation	
	14	6693840		2004-02-17	Matsushita Electric Industrial Co., Ltd.	
	15	7061214		2006-06-13	Texas Instruments Incorporated	
	16	5630096		1997-05-13	Microunity Systems Engineering, Inc.	
	17	10672458		2020-06-02	Rambus Inc.	
	18	6067241		2000-05-23	International Power Devices, Inc.	

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Attorney Docket Number	022955-000090

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20190004985		2019-01-03	Netlist, Inc.	
	2	20060174140		2006-08-03	Shaun Harris, et al.	
	3	20060080515		2006-04-13	LEFTHAND NETWORKS, INC.	
	4	20080238536		2008-10-02	ELPIDA MEMORY, INC	
	5	20100257304		2010-10-07	GOOGLE INC.	
	6	20100205470		2010-08-12	STEC, Inc.	
	7	20080101147		2008-05-01	Hossein Amidi	
	8	20070136523		2007-06-14	Randy Bonella, et al.	
	9	20090034354		2009-02-05	MICRON TECHNOLOGY, INC.	

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First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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	1							

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Complaint, Document 1, Case 2:21-cv-00463, filed December 20, 2021.	
	2	~~Complaint, Document 1, Case 1:21-cv-01453, filed October 15, 2021.~~	
	3	~~Exhibits of Complaint, Document 1-1, Case 1:21-cv-01453, filed October 15, 2021.~~	
	4	~~Exhibits of Complaint, Document 1-2, Case 1:21-cv-01453, filed October 15, 2021.~~	
	5	~~Exhibits of Complaint, Document 1-3, Case 1:21-cv-01453, filed October 15, 2021~~	
	6	~~Opening Brief, Document 11, Case 1:21-cv-01453, filed December 20, 2021.~~	
	7	~~Exhibits to Opening Brief, Document 11, Case 1:21-cv-01453, filed December 20, 2021.~~	

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Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

	8	~~First Amended Complaint, Document 14, Case 1:21-cv-01453, filed January 18, 2022.~~
	9	~~Exhibits to First Amended Complaint, Document 14-1, Case 1:21-cv-01453, filed January 18, 2022.~~
	10	~~Exhibits to First Amended Complaint, Document 14-2, Case 1:21-cv-01453, filed January 18, 2022~~
	11	~~Exhibits to First Amended Complaint, Document 15, Case 1:21-cv-01453, filed January 18, 2022~~
	12	~~Second Amended Complaint, Document 18-1, Case 1:21-cv-01453, filed January 25, 2022~~
	13	~~Exhibits to Second Amended Complaint, Document 18-2, Case 1:21-cv-01453, filed January 25, 2022.~~
	14	~~Exhibits to Second Amended Complaint, Document 18-3, Case 1:21-cv-01453, filed January 25, 2022~~
	15	~~Exhibits to Second Amended Complaint, Document 18-4, Case 1:21-cv-01453, filed January 25, 2022~~
	16	~~Exhibits to Second Amended Complaint, Document 18-5, Case 1:21-cv-01453, filed January 25, 2022.~~
	17	~~Exhibits to Second Amended Complaint, Document 18-6, Case 1:21-cv-01453, filed January 25, 2022~~
	18	~~Notice of Supplemental Authority with Exhibits, Document 32, Case 1:21-cv-01453, filed May 12, 2022.~~

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	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	19	~~Defendant's Answer, Document 49, Case 1:21-cv-01453, filed August 22, 2022.~~
	20	~~Defendant's First Amended Answer, Document 45, Case 1:21-cv-01453, filed September 12, 2022.~~
	21	~~Defendant's Second Amended Answer, Document 58, Case 1:21-cv-01453, filed November 1, 2022.~~
	22	~~Exhibits to Defendant's Second Amended Answer, Document 58-1, Case 1:21-cv-01453, filed November 1, 2022.~~
	23	~~Exhibits to Defendant's Second Amended Answer, Document 58-2, Case 1:21-cv-01453, filed November 1, 2022.~~
	24	~~Exhibits to Defendant's Second Amended Answer, Document 58-3, Case 1:21-cv-01453, filed November 1, 2022.~~
	25	~~Exhibits to Defendant's Second Amended Answer, Document 58-4, Case 1:21-cv-01453, filed November 1, 2022.~~
	26	~~Exhibits to Defendant's Second Amended Answer, Document 58-5, Case 1:21-cv-01453, filed November 1, 2022.~~
	27	~~Exhibits to Defendant's Second Amended Answer, Document 58-6, Case 1:21-cv-01453, filed November 1, 2022.~~
	28	~~Exhibits to Defendant's Second Amended Answer, Document 58-7, Case 1:21-cv-01453, filed November 1, 2022.~~
	29	Exhibits to Defendant's Second Amended Answer, Document 58-8, Case 1:21-cv-01453, filed November 1, 2022.

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	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	30	~~Exhibits to Defendant's Second Amended Answer, Document 58-9, Case 1:21-cv-01453, filed November 1, 2022.~~
	31	~~Exhibits to Defendant's Second Amended Answer, Document 58-10, Case 1:21-cv-01453, filed November 1, 2022.~~
	32	~~Answer to Second Amened Counterclaims, Document 62, Case 1:21-cv-01453, filed November 15, 2022.~~
	33	~~Defendant's Answer, Document 16, Case 2:21-cv-00463, filed April 12, 2022.~~
	34	~~First Amended Complaint, Document 23, Case 2:21-cv-00463, filed May 3, 2022.~~
	35	~~Petition for Inter Partes Review of US Patent No. 11,016,018, IPR2022-00006, filed May 17, 2022.~~
	36	~~Patent Owner Preliminary Response, IPR2022-00006, filed September 8, 2022.~~
	37	~~Institution Decision, IPR2022-00006, dated December 7, 2022.~~
	38	~~Petition for Inter Partes Review of US Patent No. 11,232,054, IPR2022-00000, filed May 17, 2022.~~
	39	~~Patent Owner Preliminary Response, IPR2022-00000, filed September 8, 2022.~~
	40	~~Institution Decision, IPR2022-00999, dated December 7, 2022.~~

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	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	41	~~Wolfe Declaration on US Patent No. 11,010,918, IPR2022-00996, filed May 17, 2022.~~
	42	~~Wolfe Declaration on US Patent No. 11,232,05, IPR2022-00999, filed May 17, 2022.~~
	43	~~IPR2014-00994 Paper 1, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014. (Exhibit~~ 1014 of IPR2022-00996 and IPR2022-00999).
	44	~~IPR2014-00994 Paper 8, Institution Decision, dated December 10, 2014. (Exhibit 1015 of IPR2022-00996 and~~ IPR2022-00999).
	45	~~IPR2014-01370 Paper 8, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22,~~ 2014. (Exhibit 1016 of IPR2022-00996 and IPR2022-00999).
	46	~~IPR2014-01370 Paper 13, Institution Decision, dated March 13, 2015. (Exhibit 1017 of IPR2022-00006 and~~ IPR2022-00999).
	47	~~IPR2017-00649 Paper 1, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017. (Exhibit~~ 1018 of IPR2022-00996 and IPR2022-00999).
	48	~~IPR2017-00649 Paper 7, Institution Decision, dated July 24, 2017. (Exhibit 1019 of IPR2022-00006 and~~ IPR2022-00999).
	49	~~US60/941586 File History. (Exhibit 1005 of IPR2022-00996 and IPR2022-00999).~~
	50	~~US12/131873 File History. (Exhibit 1006 of IPR2022-00996 and IPR2022-00999).~~

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	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

EXAMINER SIGNATURE			
Examiner Signature	/HASHEM FARROKH/	Date Considered	07/07/2023

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-02-13
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L21	1	"17582797"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 04:25 PM
L22	4	("11016918").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 04:28 PM
L23	6	"15934416"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 04:35 PM
L24	0	((dual ADJ in$1line ADJ memory ADJ module) AND ((printed ADJ circuit ADJ board) OR PCB) AND (buck ADJ converters) AND DDR).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/06 04:47 PM
L25	9	((dual ADJ in$1line ADJ memory ADJ module) AND ((printed ADJ circuit ADJ board) OR PCB) AND (buck ADJ converters) AND DDR)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/06 04:48 PM
L26	0	25 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2023/07/06 04:49 PM
L27	31	((printed ADJ circuit ADJ board) OR PCB) AND (buck ADJ converters) AND ((((double ADJ data ADJ	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	OFF	ON	2023/07/06 04:53 PM

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HF
Ex. 1002, p. 520

		rate) OR DDR) adj5 SDRAM)	EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L28	0	(((printed ADJ circuit ADJ board) OR PCB) AND (buck ADJ converters) AND (((double ADJ data ADJ rate) OR DDR) adj5 SDRAM)).clm.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/06 04:54 PM
L29	0	27 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2023/07/06 04:54 PM
L30	10	"14489269"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 04:56 PM
L31	39	("10949339" "10860506" "10217523" "10474595" "9858218" "7619912" "11232054" "6026465" "20100110748" "20060212651" "20030028733").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 05:22 PM
L32	108	("11016918" "8301833" "874831" "9158684" "9928186" "7724604" "7719866" "7721130" "6798709" "6856556" "7023187" "7692938" "5563839" "8693840" "7061214" "5630096" "10672458" "6067241" "20190004985" "20060174140" "20060080515" "20080238536" "20100257304" "20100205470"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/06 05:30 PM

		"20080101147" "20070136523" "20090034354").pn.					
L33	841	(buck near2 converter) SAME (coupl$3 OR connected OR attached) SAME ((printed ADJ circuit ADJ board) OR PCB)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:25 AM
L34	1	1 AND 33	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:25 AM
L35	74	("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:46 AM
L36	7	((plurality OR multiple OR several) WITH (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM) near2 (devices OR chips OR dies)) WITH (coupled OR connected) SAME (regulated near2 voltage)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:46 AM
L37	5	35 AND 36	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/07/07 11:47 AM

			JPO; DERWENT; IBM_TDB)				
L38	10797	(buck near5 converters).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:48 AM
L39	5	35 AND 38	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:50 AM
L40	989	(buck SAME PCB)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:52 AM
L41	51	(buck SAME PCB).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:53 AM
L42	4	35 AND 41	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 11:53 AM
L43	0	((plurality OR multiple OR several OR many OR two) near2 (DDR adj5 SDRAM)) SAME (regulated ADJ voltage)	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 12:02 PM
L44	2250	((plurality OR multiple OR several OR many OR two) near2 (DDR adj5 SDRAM))	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 12:08 PM
L45	0	1 AND 44	(US-PGPUB; USPAT;	OR	ON	ON	2023/07/07

			USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				12:09 PM
L46	15687	((plurality OR multiple OR several OR many OR two) near2 (DDR OR SDRAM))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 12:10 PM
L47	1	1 AND 46	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 12:10 PM
L48	107	(buck SAME (DDR OR SDRAM))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 12:13 PM
L49	10	48 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2023/07/07 12:14 PM
L50	4	(31 OR 32) AND 48	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY,	OR	ON	ON	2023/07/07 12:24 PM

			CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L51	3	((plurality OR multiple OR several OR many OR two) near2 (DDR OR SDRAM)) SAME ((buck OR buck$1boost) near5 (converters OR regulators))	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 01:26 PM
L52	3	(((plurality OR multiple OR several OR many OR two) near2 (DDR OR SDRAM)) SAME ((buck OR buck$1boost) near5 (converters OR regulators))).clm.	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH, TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 01:31 PM
L53	20	(voltage near2 monitor) SAME monitor$3 SAME (input near2 voltage) SAME (generat$3 OR creat$3 OR provid$3) SAME (trigger$3 near2 signal) SAME (when OR "if" OR based OR in$1case OR in$1event) SAME (input near2 voltage) SAME ((exceed$3 OR greater	(US-PGPUB; USPAT; USOCR; FIT (AP, AT, AU, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, MC, MD, MY, NL, NO, NZ, OA, PH, PL, PT, RO, RS, RU, SE, SG, SI, SK, SU, TH,	OR	OFF	ON	2023/07/07 01:42 PM

		OR higher OR more OR above) near5 threshold)	TN, TR, TW, UA, VN, WO); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L54	4	(voltage near2 monitor) SAME monitor$3 SAME (input near2 voltage) SAME (generat$3 OR creat$3 OR provid$3) SAME (trigger$3 near2 signal) SAME (when OR "if" OR based OR in$1case OR in$1event) SAME (input near2 voltage) SAME ((exceed$3 OR greater OR higher OR more OR above) near5 threshold)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 01:42 PM
L55	4	(voltage near2 monitor) SAME monitor$3 SAME (input near2 voltage) SAME (generat$3 OR creat$3 OR provid$3 OR produc$3) SAME (trigger$3 near2 signal) SAME (when OR "if" OR based OR in$1case OR in$1event) SAME (input near2 voltage) SAME ((exceed$3 OR greater OR higher OR more OR above) near5 threshold)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 01:51 PM
L56	154	(voltage near2 monitor) SAME monitor$3 SAME (input near2 voltage) SAME (generat$3 OR creat$3 OR provid$3 OR produc$3) SAME (signal) SAME (when OR "if" OR based OR in$1case OR in$1event) SAME (input near2 voltage) SAME ((exceed$3 OR greater OR higher OR more OR above) near5 threshold)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 01:53 PM
L57	19	56 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2023/07/07 01:56 PM
L58	39597	(trigger$3 near5 condition) SAME signal	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 02:07 PM
L59	1	1 AND ((trigger$3 near5 condition) SAME signal)	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2023/07/07 02:08 PM

			JPO; DERWENT; IBM_TDB)				
L60	178518	(voltage near5 monitor$3).clm.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 02:45 PM
L61	10	35 AND 60	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 02:47 PM
L62	672603	(G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 04:56 PM
L63	0	55 AND 62	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA,	OR	ON	ON	2023/07/07 04:57 PM

			EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)				
L64	0	53 AND 62	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 04:57 PM
L65	135	("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/07/07 04:58 PM
L66	17	65 AND (buck near5 converters)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/07/07 04:59 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	~~2135~~ 2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /F.H./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

	1	IPR2017-00692 Paper 1, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017. (Exhibit 1020 of IPR2022-00996 and IPR2022-00999).
	2	IPR2017-00692 Paper 25, Institution Decision, dated July 5, 2018. (Exhibit 1021 of IPR2022-00996 and IPR2022-00999).
	3	IPR2022-00418 Paper 2, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 14, 2022. (Exhibit 1022 of IPR2022-00996 and IPR2022-00999).
	4	DDR2 SDRAM SPECIFICATION, JEDEC Standard JESD79-2B (Revision of JESD79-2A), January 2005. (Exhibit 1026 of IPR2022-00996 and IPR2022-00999).
	5	FBDIMM: Advanced Memory Buffer (AMB), JEDEC Standard JESD82-20, March 2007. (Exhibit 1027 of IPR2022-00996 and IPR2022-00999).
	6	FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JEDEC Standard JESD205, March 2007. (Exhibit 1028 of IPR2022-00996 and IPR2022-00999).
	7	PCI Local Bus Specification, Revision 2.2, PCI Local Bus, December 18, 1998. (Exhibit 1031 of IPR2022-00996 and IPR2022-00999).
	8	Mohan, N., et al. "Power Electronics: Converters, Application, and Design" Second Edition, 1989. (Exhibit 1032 of IPR2022-00996 and IPR2022-00999).
	9	TPS51020, DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER, Texas Instruments, December 2003. (Exhibit 1040 of IPR2022-00996 and IPR2022-00999).
	10	FAN5026 Dual DDR/Dual-Output PWM Controller, Fairchild Semiconductor, October 2005. (Exhibit 1041 of IPR2022-00996 and IPR2022-00999).
	11	Power Supply Reference Guide for Xilinix FPGAs, Murata Manufacturing Co Ltd, September 2006. (Exhibit 1042 of IPR2022-00996 and IPR2022-00999).

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.F./

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2135
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	12	Power Supply Reference Guide for Altera FPGAs, Murata Manufacturing Co Ltd, 2008. (Exhibit 1043 of IPR2022-00996 and IPR2022-00999).
	13	Double Data Rate (DDR) SDRAM Specification, JEDEC Standard JESD79, June 2000. (Exhibit 1045 of IPR2022-00996 and IPR2022-00999).
	14	DDR3 SDRAM Specification, JEDEC Standard JESD79-3A, September 2007. (Exhibit 1046 of IPR2022-00996 and IPR2022-00999).
	15	MPD4S014S, DC-DC Converter Specification (DRAFT), Murata Manufacturing Co Ltd, January 2008. (Exhibit 1048 of IPR2022-00996 and IPR2022-00999).
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Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2135
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-02-13
Name/Print	Khaled Shami	Registration Number	38745

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Art Unit	~~2135~~ 2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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	1	10949339		2021-03-16	Netlist, Inc.	
	2	10860506		2020-12-08	Netlist, Inc.	
	3	10217523		2019-02-26	Netlist, Inc.	
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	6	7619912		2009-11-17	Netlist, Inc.	
	7	11232054		2022-01-25	Netlist, Inc.	
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	1	20100110748		2010-05-06	Best, Scott C.	
	2	20060212651				
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	1	288pin Load-Reduced DIMM based on 8Gb B-die, Datasheet, Samsung, Rev. 1.6, 2017.	

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	14	MB Initialization sequence Item 142.35, JEDEC presentation, June 2009.
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	16	IPR2018-00362, Petition for Inter Partes Review of US Patent No. 9,606,007, filed December 22, 2017.
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	19	IPR2020-01042, Petition for Inter Partes Review of US Patent No. 10,474,595, filed June 8, 2020.
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	25	~~288pin Load Reduced DIMM based on 16Gb B-die, Datasheet, Samsung, Rev. 1.0, February 2019.~~
	26	~~DDR4 Registering Clock Driver - DDR4RCD02, JESD82-31A, JEDEC Standard, August 2019.~~
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	29	~~IPR2023-00405, Petition for Inter Partes Review of US Patent No. 11,232,054, filed January 2022.~~
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	31	~~IPR2022-00418, Patent Owner's Response, filed November 25, 2022.~~
	32	~~Declaration of Ron Matliel, IPR2022-00418 Exhibit 1003, filed in IPR on January 14, 2022.~~
	33	~~Netlist, Inc.'s Preliminary Proposed Claim Constructions in Civil Action Nos. 6:21-cv-00431-ADA and 6:21-cv-00430-ADA, IPR2022-00418 Exhibit 1012, filed in IPR on January 14, 2022.~~
	34	Micron's Preliminary Identivicaiton of Proposed Claim Constructions in Civil Action Nos. 6:21-cv-00431-ADA and 6:21-cv-00430-ADA, IPR2022-00418 Exhibit 1013, filed in IPR on January 14, 2022.

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	35	Double Data Rate (DDR) SCRAM Specification, JESD79, JEDEC Standard, (IPR2022-00418 Exhibit 1018) June 2000.
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	40	FSA1208 Low-Power, Eight-Port, High-Speed Isolation Switch, Fairchild, (IPR2022-00418 Exhibit 2006) December 2014.

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Name/Print	Khaled Shami	Registration Number	38745

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 344

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /H.P/

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

151145 7590 07/13/2023

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
07/13/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 345

Office Action Summary	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☑ Responsive to communication(s) filed on 04/12/2023.

☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2a)☑ This action is **FINAL.** 2b) ☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

5) ☑ Claim(s) 2-15 is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6) ☐ Claim(s) _____ is/are allowed.

7) ☑ Claim(s) 2-15 is/are rejected.

8) ☐ Claim(s) _____ is/are objected to.

9) ☐ Claim(s) _____ are subject to restriction and/or election requirement

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov.**

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☑ The drawing(s) filed on 04/04/2022 is/are: a)☑ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a)☐ All b)☐ Some** c)☐ None of the:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☑ Notice of References Cited (PTO-892)

2) ☑ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b) Paper No(s)/Mail Date 02/13/2022.

3) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date _____.

4) ☐ Other: _____.

Notice of Pre-AIA or AIA Status

1. The present application is being examined under the pre-AIA first to invent provisions.

2. This Office Action is response to the communications file on 04/12/2023. There are a total of 14 claims pending in the application. Claim 1 has been canceled and claims 2-15 have been added.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*3. As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b),** no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 02/13/2023 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the Examiner. The US patent and or the patent application with missing publication data and/or patentee or applicant show as lined-through. The

documents listed as NPL in the IDS' are shown by lined-through because the corresponding document are not readily identifiable from the description listed in the IDS.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

> *(a) IN GENERAL. —The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

> *The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

1. Claim 2-15 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. The independent claim 2, in part, recites the limitation:

"first, second, third and **fourth** buck converters coupled to PCB and to the input voltage supply line and configured to (i) receive power from the input voltage supply line, (ii) generate first, second, third and **fourth regulated voltages** from the power received from the input voltage supply line, and (iii) output the first, second, third and fourth

regulated voltages via first, second, third, and fourth regulated voltage lines, respectively"

The specification does not appear to describe/support the limitation(s) as claimed above. The Abstract of instant application appears to be closest portion of the specification describing the subject matter. For convenience, the Abstract reproduced as shown below:

Abstract

"In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. **A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage**. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage" *(emphasis added).*

As shown above, the fourth voltage is not produced (e.g., generated) by a buck converter. The dependent claims 3-15 are rejected by virtue of their dependency from the independent claim 2.

Response to Remarks

In non-final office action mailed 10/12/2022, claim 1 was rejected under the statutory type (35 U.S.C. 101) as claiming the same invention as that of prior U.S. Patent No. 11,016,918 B2. Applicant has canceled the claim 1. Therefore, the statutory double-patenting rejection is withdrawn.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, ***THIS ACTION IS MADE FINAL****. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	08/08/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/LAVINIA D JOHNSON/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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PATENT AND TRADEMARK OFFICE

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**08/08/2023 12:17:41 PM ET**	**022955-000090**

Title of Invention

FLASH-DRAM HYBRID MEMORY MODULE

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	62578850	FILING DATE	01/24/2022
CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 2

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
022955-000090 Supplemental NFOA to amend title.pdf	3	Supplemental Response or Supplemental Amendment	146 KB
SADS.pdf	9	Application Data Sheet	263 KB

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Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)

022955-000090 Supplemental NFOA to amend title.pdf	33B8CF85246E16AC90E0D1BBE88EC18E1516CAB1797EC8969BB5E12AC9A7F3A1FD008001DEC5F93D3E1334F110194E82971DCB0C1F09698B52A6584E775B95FF
SADS.pdf	7A20BE0811F0FC121B335BDC0657D8AB63223419D9A6ECABABC7BB26E958EB93A4FF3F3A9758BA5B62C94FD9DB3E893ED0705E3FEA55881AB90B5D1FE9166C61

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONF. NO: 3546

APPLICATION NO: 17/582,797 ART UNIT: 2138

FILING DATE: January 24, 2022 EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Commissioner:

In response to the non-final Office Action mailed October 12, 2022, Applicant submits the following Amendment and Remarks.

Amendments to the Specification, beginning on page **2**.

Remarks begin on page **3**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

AMENDMENT TO THE SPECIFICATION

Please amend the title of the application as follows:

~~FLASH-DRAM HYBRID~~ MEMORY WITH ON-MODULE POWER MANAGEMENT

Samsung Electronics Co., Ltd.
Ex. 1002, p. 356

REMARKS

The non-final Office Action mailed October 12, 2022, has been carefully considered.

Reconsideration in view of the remarks filed on April 12, 2023, is respectfully requested.

Herein, the Applicant has amended the title to read as "MEMORY WITH ON-MODULE POWER MANAGEMENT". A Supplemental Application Data Sheet is also provided to show the amendment to the title.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: August 8, 2023
/Khaled Shami/
Khaled Shami, Reg. No. 38,745

Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

Samsung Electronics Co., Ltd.
Ex. 1002, p. 357

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Inventor Information:

Inventor 1

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Walnut	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	944 Crystal Water Lane		
Address 2			
City	Walnut	State/Province	CA
Postal Code	91789	Country i	US

Inventor 2

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ○ Non US Residency ○ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence i	US

Mailing Address of Inventor:

Address 1	6 Silver Fir		
Address 2			
City	Irvine	State/Province	CA
Postal Code	92604	Country i	US

Inventor 3

Legal Name

Prefix	Given Name	Middle Name	Family Name	Suffix
	Scott	H.	Milton	

Samsung Electronics Co., Ltd.
Ex. 1002, p. 358

PTO/AIA/14 (08-15)
Approved for use through 04/30/2017. OMB 0651-0032
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Irvine	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	49 Statehouse Place		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92602	**Country** i	US

Inventor 4

Legal Name

Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Jayesh		Bhakta	

Residence Information (Select One)	◉ US Residency	○ Non US Residency	○ Active US Military Service		
City	Cerritos	**State/Province**	CA	**Country of Residence** i	US

Mailing Address of Inventor:

Address 1	12220 Rose Street		
Address 2			
City	Cerritos	**State/Province**	CA
Postal Code	90703	**Country** i	US

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	151145		
Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	~~FLASH-DRAM HYBRID MEMORY MODULE~~ MEMORY WITH ON-MODULE POWER MANAGEMENT		
Attorney Docket Number	022955-000090	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Total Number of Drawing Sheets (if any)	22	**Suggested Figure for Publication (if any)**	

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:	◉ Customer Number	○ US Patent Practitioner	○ Limited Recognition (37 CFR 11.9)
Customer Number	151145		

Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					
Prefix	**Given Name**	Middle Name	**Family Name**	Suffix	Remove
Registration Number					

Additional Representative Information blocks may be generated within this form by selecting the **Add** button.

Samsung Electronics Co., Ltd.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.
When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
	Continuation of	17328019	2021-05-24

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
17328019	Continuation of	17138766	2020-12-30	11016918	2021-05-25

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
17138766	Continuation of	15934416	2018-03-23

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15934416	Continuation of	14840865	2015-08-31	9928186	2018-03-27

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status	Patented		Remove		
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
13559476	Claims benefit of provisional	61512871	2011-07-28

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Prior Application Status	Patented			Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

Prior Application Status	Abandoned		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country[i]	Filing Date (YYYY-MM-DD)	Access Code[i] (if applicable)

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013.
NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

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PTO/AIA/14 (08-15)
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

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Ex. 1002, p. 363

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

Clear

◉ Assignee	○ Legal Representative under 35 U.S.C. 117	○ Joint Inventor
○ Person to whom the inventor is obligated to assign.	○ Person who shows sufficient proprietary interest	

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Applicant:

Address 1	111 Academy Way		
Address 2	Suite 100		
City	Irvine	**State/Province**	CA
Country[i]	US	Postal Code	92617
Phone Number	US	Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Samsung Electronics Co., Ltd.
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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1

Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.

If the Assignee or Non-Applicant Assignee is an Organization check here. ☒

Organization Name	Netlist, Inc.

Mailing Address Information For Assignee including Non-Applicant Assignee:

Address 1	111 Academy Way		
Address 2	Suite 100		
City	Irvine	**State/Province**	CA
Country i	US	Postal Code	92617
Phone Number	US	Fax Number	
Email Address			

Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	022955-000090
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e. g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	~~/Khaled Shami/~~ /Khaled Shami/			Date (YYYY-MM-DD)	~~2022-01-24~~ 2023-08-07
First Name	Khaled	Last Name	Shami	Registration Number	38745

Additional Signature may be generated within this form by selecting the Add button.

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UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

151145 7590 08/18/2023

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
08/18/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

Samsung Electronics Co., Ltd.
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Advisory Action Before the Filing of an Appeal Brief	**Application No.** 17/582,797	**Applicant(s)** Chen et al.	
	Examiner HASHEM FARROKH	**Art Unit** 2138	**AIA (FITF) Status** No

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 08 August 2023 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

NO NOTICE OF APPEAL FILED

1. ☑ The reply was filed after a final rejection. No Notice of Appeal has been filed. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114 if this is a utility or plant application. Note that RCEs are not permitted in design applications. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires ____ months from the mailing date of the final rejection.
   b) ☑ The period for reply expires on: (1) the mailing date of this Advisory Action; or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.
   c) ☐ A prior Advisory Action was mailed more than 3 months after the mailing date of the final rejection in response to a first after-final reply filed within 2 months of the mailing date of the final rejection.The current period for reply expires ____ months from the mailing date of *the prior Advisory Action* or SIX MONTHS from the mailing date of the final rejection, whichever is earlier.
   Examiner Note: If box 1 is checked, check either box (a), (b) or (c). ONLY CHECK BOX (b) WHEN THIS ADVISORY ACTION IS THE FIRST RESPONSE TO APPLICANTS FIRST AFTER-FINAL REPLY WHICH WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. ONLY CHECK BOX (c) IN THE LIMITED SITUATION SET FORTH UNDER BOX (c). See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) or (c) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendments filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   b) ☐ They raise the issue of new matter (see NOTE below);
   c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.
   NOTE: _____ (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☐ For purposes of appeal, the proposed amendment(s):(a) ☐ will not be entered, or (b) ☐ will be entered, and an explanation of how the new or amended claims would be rejected is provided below or appended.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____
9. ☐ The affidavit or other evidence filed after final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
10. ☐ The affidavit or other evidence filed after the date of filing the Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
11. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

12. ☑ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
13. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____
14. ☐ Other: _____.

STATUS OF CLAIMS

15. The status of the claim(s) is (or will be) as follows:
    Claim(s) allowed:_____.
    Claim(s) objected to:_____.
    Claim(s) rejected:2-15.
    Claim(s) withdrawn from consideration:1.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

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Continuation of REQUEST FOR RECONSIDERATION/OTHER 12. The request for reconsideration has been considered but does NOT place the application in condition for allowance because: In the Office Action mailed on 07/13/2023, claims 2-15 were rejected. Applicant request for consideration does not appears to address the rejection.

DO NOT ENTER: /H.F/

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONF. NO: 3546

APPLICATION NO: 17/582,797 ART UNIT: 2138

FILING DATE: January 24, 2022 EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL AMENDMENT

Commissioner:

In response to the non-final Office Action mailed October 12, 2022, Applicant submits the following Amendment and Remarks.

Amendments to the Specification, beginning on page **2**.

Remarks begin on page **3**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

AMENDMENT TO THE SPECIFICATION

Please amend the title of the application as follows:

~~FLASH-DRAM HYBRID~~ MEMORY WITH ON-MODULE POWER MANAGEMENT

Samsung Electronics Co., Ltd.
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REMARKS

The non-final Office Action mailed October 12, 2022, has been carefully considered.

Reconsideration in view of the remarks filed on April 12, 2023, is respectfully requested.

Herein, the Applicant has amended the title to read as "MEMORY WITH ON-MODULE POWER MANAGEMENT". A Supplemental Application Data Sheet is also provided to show the amendment to the title.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: August 8, 2023
/Khaled Shami/
Khaled Shami, Reg. No. 38,745

Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

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Ex. 1002, p. 372

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

151145 7590 09/21/2023

Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	

ART UNIT	PAPER NUMBER
2138	

NOTIFICATION DATE	DELIVERY MODE
09/21/2023	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

Samsung Electronics Co., Ltd.
Ex. 1002, p. 373

Applicant-Initiated Interview Summary	**Application No.** 17/582,797	**Applicant(s)** Chen et al.		
	Examiner HASHEM FARROKH	**Art Unit** 2138	**AIA (First Inventor to File) Status** No	**Page** 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	**Title**	**Type**
HASHEM FARROKH	Primary Examiner	Telephonic
Khaled Shami	Attorney	

Date of Interview: 13 September 2023

Issues Discussed:

35 U.S.C. 112

In the final office action mailed on 07/13/2023, claims 2-13 were rejected under 36 USC 112(a), first paragraph as failing to comply to written description requirement. The Examiner rejected the independent claim 2 indicating the claimed specification does not describe/support the limitation of a fourth buck converter providing or supplying a fourth regulated voltage. During the interview the Applicant stated paragraph 0148 and Fig 16 of application describes/shows a dual buck converter, which provides two regulated voltages.Therefore there are four voltages supplied by three buck converters 1122, 1124 and 1126, wherein the dual buck converter 1124 is being or equivalent to two buck converters. The Examiner agreed.

☑ Attachment

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	

Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04
Please further see:
MPEP 713.04
Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)
37 CFR § 1.2 Business to be transacted in writing

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 374

Doc Code: M865 or FAI.REQ.INTV

PTOL-413A (07-16)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Applicant Initiated Interview Request Form

Application No.: 17/582,797 First Named Applicant: Chi-She Chen
Examiner: Farrokh, Hashem Art Unit: 2138 Status of Application: Final/Advisory

Tentative Participants:
(1) Examiner Farrokh (2) Mr. Khaled Shami

(3) Mr. Marwan Fawal (4) _____

Proposed Date of Interview: Sept. 13, 2023 **Proposed Time:** 3:00 (○AM ◉PM)

Type of Interview Requested:
(1) ☑ Telephonic (2) ☐ Personal (3) ☐ Video Conference

Exhibit To Be Shown or Demonstrated: ☐ YES ☑ NO
If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) 112(a)	2-15		☐	☐	☐
(2)			☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached ☐ Proposed Amendment or Arguments Attached

Brief Description of Arguments to be Presented: Mr. Shami to show support in the specification for claimed 4th buck converter and 4th regulated voltage

An interview was conducted on the above-identified application on _____

NOTE: This form should be completed and filed by applicant in advance of the interview (see MPEP § 713.01). If this form is signed by a registered practitioner not of record, the Office will accept this as an indication that he or she is authorized to conduct an interview on behalf of the principal (37 CFR 1.32(a)(3)) pursuant to 37 CFR 1.34. This is not a power of attorney to any above named practitioner. See the Instruction Sheet for this form, which is incorporated by reference. By signing this form, applicant or practitioner is certifying that he or she has read the Instruction Sheet. After the interview is conducted, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible. This application will not be delayed from issue because of applicant's failure to submit a written record of this interview.

/Khaled Shami
Applicant/Applicant's Representative Signature

_____
Examiner/SPE Signature

Khaled Shami
Typed/Printed Name of Applicant or Representative

650-745-5353
Applicant's/Applicant's Representative's Telephone Number

36745
Registration Number, if applicable

A Federal agency may not conduct or sponsor, and a person is not required to respond to, nor shall a person be subject to a penalty for failure to comply with an information collection subject to the requirements of the Paperwork Reduction Act of 1995, unless the information collection has a currently valid OMB Control Number. The OMB Control Number for this information collection is 0651-0031. Public burden for this form is estimated to average 24 minutes per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the information collection. Send comments regarding this burden estimate or any other aspect of this information collection, including suggestions for reducing this burden to the Chief Administrative Officer, United States Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450 or email InformationCollection@uspto.gov. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. If filing this completed form by mail, send to: **Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
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PTOL-413A (07-16)
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Instruction Sheet for:
APPLICANT INITIATED INTERVIEW REQUEST FORM

(Not to be Submitted to the USPTO)

1. If this form is signed by a registered practitioner not of record, the authority to submit the Applicant Initiated Interview Request Form is pursuant to limited authority to act in a representative capacity under 37 CFR 1.34 and further proof of authority to act in a representative capacity may be required. *See* 37 CFR 1.34.

   The Office will accept the signed form as an indication that the registered practitioner not of record is authorized to conduct an interview on behalf of the principal in pursuant to 37 CFR 1.34.

   For more information, see the "Conducting an Interview with a Registered Practitioner Acting in a Representative Capacity" notice which is available on the USPTO Web site at: http://www.uspto.gov/patents/law/notices/2010.jsp.

2. This is not a power of attorney to any named practitioner. Accordingly, any registered practitioner not of record named on the form does not have authority to sign a request to change the correspondence address, a request for express abandonment, a disclaimer, a power of attorney, or other document requiring the signature of the applicant, assignee of the entire interest or an attorney of record. If appropriate, a separate power of attorney to the named practitioner should be executed and filed in the US Patent and Trademark Office.

3. Any interview concerning an unpublished application under 35 U.S.C. § 122(b) with a registered practitioner not of record who obtains authorization through use of the PTOL-413A will be conducted based on the information and files supplied by the practitioner in view of the confidentiality requirements of 35 U.S.C. § 122(a).

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Additional USPTO uses of the information in this record may include disclosure to: 1) the International Bureau of the World Intellectual Property Organization, if the record is related to an international application filed under the Patent Cooperation Treaty; 2) the public i) after publication of the application pursuant to 35 U.S.C. 122(b), ii) after issuance of a patent pursuant to 35 U.S.C. 151, iii) if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections, or an issued patent, or iv) without publication of the application or patent under the specific circumstances provided for by 37 CFR 1.14(a)(1)(v)-(vii); and/or 3) the National Archives and Records Administration, for inspection of records.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed

ENTITY: ☑ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA		RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*		x $100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		x $480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).				
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))					
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT	10/13/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0		x $100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0		x $480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	0

		(Column 1)		(Column 2)	(Column 3)			
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		RATE ($)	ADDITIONAL FEE ($)
	Total (37 CFR 1.16(i))	*	Minus	**	=		x $0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=		x $0 =	
	☐ Application Size Fee (37 CFR 1.16(s))							
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							
							TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.	HSLIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".	/DEREK A SAUNDERS/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".	
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.	

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5563839	A	1996-10-08	HERDT et al.	
	2	6067241	A	2000-05-23	LU	
	3	6693840	B2	2004-02-17	SHIMADA et al.	
	4	6798709	B2	2004-09-28	SIM et al.	
	5	6856556	B1	2005-02-15	HAJECK	
	6	7023187	B2	2006-04-04	SHEARON et al.	
	7	7061214	B2	2006-06-13	MAYEGA et al.	
	8	7692938	B2	2010-04-06	PETTER	

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	9	7719866	B2	2010-05-18	BOLDO	
	10	7721130	B2	2010-05-18	PRETE et al.	
	11	7724604	B2	2010-05-25	AMIDI et al.	
	12	10672458	B1	2020-06-02	SHAEFFER et al.	

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	1	20060080515	A1	2006-04-13	SPIERS et al.	
	2	20060174140	A1	2006-08-03	HARRIS et al.	
	3	20070136523	A1	2007-06-14	BONELLA et al.	
	4	20080101147	A1	2008-05-01	AMIDI	
	5	20080238536	A1	2008-10-02	HAYASHI et al.	

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	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	6	20090034354	A1	2009-02-05	RESNICK	
	7	20100205470	A1	2010-08-12	MOSHAYEDI et al.	
	8	20100257304	A1	2010-10-07	RAJAN et al.	

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	1	Transcript, Day 2 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 17, 2023, 375 pages.	☐
	2	Transcript, Day 4 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 19, 2023, 338 pages.	☐
	3	Exhibit 1003, IPR 2022-00999, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,232,054, 431 pages, executed on May 16, 2022.	☐

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	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	4	Exhibit 1014, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014, 69 pages.	☐
	5	Exhibit 1015, IPR 2014-00994, Decision - Denying Institution of Inter Partes Review, issued December 16, 2014, 16 pages.	☐
	6	Exhibit 1016, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22, 2014, 67 pages.	☐
	7	Exhibit 1017, IPR 2014-01370, Decision - Denying Institution of Inter Partes Review, issued March 13, 2015, 19 pages.	☐
	8	Exhibit 1018, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017, 70 pages.	☐
	9	Exhibit 1019, IPR 2017-00649, Decision - Denying Institution of Inter Partes Review, issued July 24, 2017, 17 pages.	☐
	10	Exhibit 1020, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017, 78 pages.	☐
	11	Exhibit 1021, IPR 2017-00692, Final Written Decision, issued July 5, 2018, 42 pages.	☐
	12	Exhibit 1022, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 14, 2022, 76 pages.	☐
	13	Exhibit 1026, JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2B (Revision of JESD7-2A), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, January 2005, 113 pages.	☐
	14	Exhibit 1027, JEDEC STANDARD, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 190 pages.	☐

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	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	15	Exhibit 1028, JEDEC STANDARD, FBDIMM Specification: DDR2 SDRAM Fully Buffered, DIMM (FBDIMM) Design Specification, JESD205, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 129 pages.	☐
	16	Exhibit 1031, PCI Local Bus Specification, Revision 2.2, December 18, 1998, 322 pages.	☐
	17	Exhibit 1032, Power Electronics: Converters, Applications, and Design, Second Edition, copyright 1995 by John Wiley & Sons, Inc., 37 pages.	☐
	18	Exhibit 1040, Texas Instruments, TPS51020, Dual, Voltage Mode, DDR Selectable, Synchronous, Step-Down Controller for Notebook System Power, SLUS564B, July 2003 (revised December 2003), 27 pages.	☐
	19	Exhibit 1041, Fairchild Semiconductor, FAN5026, Dual DDR/Dual-Output PWM Controller, October 2005, 17 pages.	☐
	20	Exhibit 1042, Murata Manufacturing Co., Ltd, Power Supply Reference Guide for XILINX FPGAs, September 2006, 33 pages.	☐
	21	Exhibit 1043, Murata Products, Power Supply Reference Guide for ALTERA FPGAs, Catalog No. DC-03-A, 2008, 40 pages.	☐
	22	Exhibit 1045, JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, June 2000, 77 pages.	☐
	23	Exhibit 1046, JEDEC STANDARD, DDR3 SDRAM Specification, JESD79-3A (Revision of JESD79-3), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, September 2007, 189 pages.	☐
	24	Exhibit 1048, Murata Manufacturing, DC-DC Converter Specification(DRAFT), MPD4S014S, January 21, 2008, 11 pages.	☐
	25	Exhibit 1049, Micron, NAND Flash Memory, MT29F2G08AABWP/MT29F2G16AABWP, MT29F4G08BABWP/ MT29F4G16BABWP, MT29F8G08FABWP, copyright 2004 by Micron Technology, Inc., 57 pages.	☐

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	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	26	Exhibit 1058, LENK, Simplified Design of Switching Power Supplies, Linear Technology, EDN Series for Design Engineers, copyright 1995 by Butterworth-Heinemann, 9 pages.	☐
	27	Exhibit 1061, Analog Devices, Super Sequencer with Margining Control and Auxiliary ADC Inputs, ADM1066, copyright 2006 by Analog Devices, Inc., 36 pages.	☐
	28	Exhibit 1062, Analog Devices, Analog Dialogue, Volume 40, Number 2, 2006, 24 pages.	☐
	29	Exhibit 1063, National Semiconductor, LMC6953, PCI Local Bus Supervisor, October 1996, 12 pages.	☐
	30	Exhibit 1067, Lattice Semiconductor Corporation, LatticeXP Family Data Sheet, Version 04.2, March 2006, 127 pages.	☐
	31	Exhibit 1068, Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed October 15, 2021, 82 pages.	☐
	32	Exhibit 1069, First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed January 18, 2022, 122 pages.	☐
	33	Exhibit 1071, Complaint, filed December 20, 2021, 49 pages.	☐
	34	Exhibit 1072, The Samsung Defendants' Answer, filed April 12, 2022, 37 pages.	☐
	35	Exhibit 1073, First Amended Complaint, filed May 3, 2022, 71 pages.	☐
	36	Exhibit 1075, IPR 2022-00999, Deposition of William Mangione-Smith, Ph.D. regarding US Patent No. 11,232,054, 245 pages, dated June 12, 2023.	☐

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	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	37	Exhibit 1076, IPR 2022-00999, redline comparing Declarations - Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,232,054, 165 pages, executed on March 29, 2022.	☐
	38	Exhibit 1077, Netlist, Technology Tutorial: In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same, Inv No. 337-TA-1023, May 8, 2017, 11 pages.	☐
	39	Exhibit 1078, Analog Devices, Step-Down DC-to-DC Controller, ADP1821, copyright 2005-2007 by Analog Devices, Inc., 24 pages.	☐
	40	Exhibit 2001, IPR 2022-00999, Declaration of Dr. Sunil P. Khatri regarding US Patent No. 11,232,054, 68 pages, executed on September 8, 2022.	☐
	41	Exhibit 2003, BELLONI et al., 24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current, ISSCC 2008 / Session 24 / Analog Power Techniques / 24.6, 2008 IEEE International Solid-State Circuits Conference, 3 pages.	☐
	42	Exhibit 2004, MA et al., Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode, IEEE Journal of Solid-State Circuits, Volume 38, Number 1, January 2003, pages 89-100 (12 pages).	☐
	43	Exhibit 2006, Micron, Technical Note: Power Solutions for DDR2 Notebook PCs, TN-47-05 DDR2 Power Solutions for Notebooks, copyright 2004 by Micron Technology, Inc., 16 pages.	☐
	44	Exhibit 2007, Texas Instruments, LP2996-N, LP2996A DDR Termination Regulator, SNOSA40K, November 2002 (revised December 2016), 39 pages.	☐
	45	Exhibit 2008, JAMECO ELECTRONICS, Jameco Part Number 843868, National Semiconductor: LP2996: DDR Termination Regulator, June 2006, 19 pages.	☐
	46	Exhibit 2009, JAMECO ELECTRONICS, Jameco Part Number 843930, National Semiconductor: LP2997: DDR-II Termination Regulator, June 2006, 13 pages.	☐
	47	Exhibit 2010, National Semiconductor: LP2998: DDR-II and DDR-I Termination Regulator, December 12, 2007, 18 pages.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	48	Exhibit 2011, BERGVELD, Battery Management Systems: Design by Modelling, copyright 2001 by Royal Philips Electronics N.V., 328 pages.	☐
	49	Exhibit 2012, ROMO, DDR Memories: Comparison and Overview, NXP, pages 70-73 (4 pages), September 21, 2007.	☐
	50	Exhibit 2013, JEDEC Standard No. 21-C, Page 4.20.3-1; PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, 26 pages. downloaded August 16, 2022.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(**Not for submission under 37 CFR 1.99)**

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-10-13
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc code: RCEX
Doc description: Request for Continued Examination (RCE)

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	17582797	Filing Date	2022-01-24	Docket Number (if applicable)	022955-000090	Art Unit	2138
First Named Inventor	CHEN			Examiner Name	FARROKH		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☒ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☒ Other Response After Final Action filed August 8, 2023

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other Request for Continued Examination (RCE)

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 220585

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (02-18)
Approved for use through 11/30/2020. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-10-13
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

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The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: 3546

SERIAL NO.: 17/582,797 ART UNIT: 2138

FILING DATE: 2022-01-24 EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following proceedings involving patents that are in the family of the above-identified patent application:

Proceeding	Status
Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas LLC v. Netlist, Inc., Case No. IPR2022-00418 (P.T.A.B.), filed January 14, 2022	Final Written Decision - Determining All Challenged Claims Unpatentable entered August 28, 2023
Samsung Electronics Co., Ltd. v. Netlist, Inc., Case No. IPR2022-00615 (P.T.A.B.), filed February 17, 2022	Institution Granted October 19, 2022
Samsung Electronics Co., Ltd. v. Netlist, Inc., Case No. IPR2022-00996 (P.T.A.B.), filed May 17, 2022	Institution Granted December 7, 2022
Samsung Electronics Co., Ltd. v. Netlist, Inc., Case No. IPR2022-00999 (P.T.A.B.), filed May 17, 2022	Institution Granted December 6, 2022
2:21-cv-00463-JRG (EDTX Case asserting '918 and '054 against Samsung)	Closed - Termination Date August 11, 2023
2:22-cv-00203-JRG (EDTX Case asserting '918 and '054 against Micron)	Open - Filing Date June 10, 2022
1:22-cv-00134-DII (WDTX Case asserting the '833 against Micron)	Open - Filing Date April 28, 2021

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Information Disclosure Statement

Listed on accompanying two IDS Forms PTO/SB/08a are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). Due to the Request for Continued Examination (RCE) filed concurrently, this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL 1-50 and NPL 1-36** (as listed on the two PTO/SB/08a forms) are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 17/328,019, filed 05-24-2021 (now U.S. Pat. No. 11,232,054), 17/138,766, filed 12-30-2020 (now U.S. Pat. No. 11,016,918), 15/934,416, filed 03-23-2018 (now abandoned), 14/840,865, filed 08-31-2015 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next

Samsung Electronics Co., Ltd.
Ex. 1002, p. 393

communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed two IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

Date: October 13, 2023

/Khaled Shami/
Khaled Shami, Registration No.: 38745
Customer No.: 151145

VORYS, SATER, SEYMOUR and PEASE LLP
1909 K Street, NW, 9th Floor
Washington, DC 20006-1152
Tel: (202) 467-8800

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Ex. 1002, p. 394

PTO/SB/08a (01-22)
Approved for use through 05/31/2024. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	1	Exhibit 2014, Qimonda, Internet Data Sheet, Rev. 1.25, June 2007, 24 pages.	☐
	2	Exhibit 2015, Siemens, 3.3V 2M x 64/72-Bit 1 BANK SDRAM Module, HYS64/72V2200GU-8/-10, 3.3V 4M x 64/72-Bit 2 BANK SDRAM Module, HYS64/72V4200GU-8/-10, 168 pin unbuffered DIMM Modules, downloaded from www.datasheetcatalog.com; 1998, 18 pages	☐
	3	Exhibit 2016, PCI Bus Variation - Technology Note, copyright 2006 by Euresys, 9 pages.	☐
	4	Exhibit 2017, Qimonda, Internet Data Sheet, Rev. 1.42, September 2007, 27 pages.	☐
	5	Exhibit 2018, Transcend, Product Support, What is the difference between SDRAM, DDR1, DDR2, DDR3 and DDR4?, available online at https://www.transcend-info.com/support/faq-296#:~:text=DDR3's prefetch buffer width is,according to the temperature variation, downloaded August 24, 2022, 2 pages.	☐
	6	Exhibit 2021, Texas Instruments: Application Report, Low Dropout Operation in a Buck Converter, SLUA928A - December 2018 - revised March 2019, 18 pages.	☐
	7	Exhibit 2022, Electronic Design, Simple Soft-Start Circuitry Provides Long Startup Times, available online at http://electronicdesign.com/power/simple-soft-start-circuitry-provides-long-startup-times, published June 22, 1998, 3 pages.	☐
	8	Exhibit 2024, SCHMID, Understanding Hard Drive Performance, available online at https://www.tomshardware.com/reviews/understanding-hard-drive-performance,1557-5.html, downloaded August 15, 2022, published March 5, 2007, 17 pages.	☐
	9	Exhibit 2025, Micron, SDR SDRAM, MT48LC64M4A2 - 16 Meg x 4 x 4 Banks, MT48LC32M8A2 - 8 Meg x 8 x 4 Banks, MT48LC16M16A2 - 4 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 94 pages.	☐
	10	Exhibit 2026, Micron, SDR SDRAM, MT48LC16M4A2 - 4 Meg x 4 x 4 Banks, MT48LC8M8A2 - 2 Meg x 8 x 4 Banks, MT48LC4M16A2 - 1 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 84 pages.	☐
	11	Exhibit 2027, Transcend, DDR2 SO-DIMM, copyright 2012 by Transcend, 3 pages.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	17582797
	Filing Date	2022-01-24
	First Named Inventor	CHEN
	Art Unit	2138
	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	12	Exhibit 2028, Micron Technical Note: DDR3 Point-to-Point Design Support, copyright 2013 by Micron Technology, Inc., 27 pages.	☐
	13	Exhibit 2030, IPR 2022-00996 and IPR 2022-00999, Videoconference Deposition of Andrew Wolfe, Ph.D. regarding US Patent Nos. 11,016,918 and 11,232,054, 311 pages, dated March 16, 2023.	☐
	14	Exhibit 2031, IPR 2022-00996, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,016,918, 452 pages, executed on May 16, 2022.	☐
	15	Exhibit 2031, IPR 2022-00996, Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,016,918, 144 pages, executed on March 28, 2023.	☐
	16	Exhibit 2032, Claim Construction Order, filed December 14, 2022, 35 pages.	☐
	17	Exhibit 2033, Defendants' Objections to Claim Construction Memorandum Order, filed December 29, 2022, 11 pages.	☐
	18	Exhibit 2043, Samsung Unveils New Power Management Solutions for DDR5 Modules, May 18, 2021, 6 pages.	☐
	19	Exhibit 2044, Micron, DDR2 SDRAM RDIMM, MT9HTF3272Y - 256MB, MT9HTF6472PY - 512MB, MT9HTF12872PY - 1GB, copyright 2003 by Micron Technology, Inc., 23 pages.	☐
	20	Exhibit 2046, JEDEC Standard No. 21C, Page 4.20.11-1, PC2-6400/PC2-5300/PC2-4200/PC2-3200, DDR2 Unbuffered SO-DIMM, Reference Design Specification, Revision 2.5, July 2008, 60 pages.	☐
	21	Exhibit 2048, Micron, DDR2 SDRAM FBDIMM, MT18HTF12872FD - 1GB, MT18HTF25672FD - 2GB, copyright 2005 by Micron Technology, Inc., 39 pages.	☐
	22	Exhibit 2056, IPR 2022-00615, Remote Videotaped Deposition by Virtual Zoom of Andrew Wolfe, Ph.D. regarding US Patent No. 7,619,912, 297 pages, dated January 4, 2023.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
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	Filing Date	2022-01-24
	First Named Inventor	CHEN
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	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	23	Exhibit 2057, Micron Technical Brief: Micron DDR5: Key Module Features, DDR4 vs. DDR5 DIMM, copyright 2020 by Micron Technology, Inc., 7 pages.	☐
	24	Exhibit 2063, Netlist, Demonstrative Exhibit for IPR 2022-00996 and IPR 2022-00999, filed September 6, 2023, 180 pages.	☐
	25	Exhibit 2102, LEE et al., PCI Express Power and Mini Card Solutions - Design Note 346, Linear Technology - Design Notes, copyright 2004 by Linear Technology Corporation, 2 pages.	☐
	26	Paper 1, IPR 2022-00996, Petition for Inter Partes Review of US Patent No. 11,016,918, filed May 17, 2022, 151 pages.	☐
	27	Paper 1, IPR 2022-00999, Petition for Inter Partes Review of US Patent No. 11,232,054, filed May 17, 2022, 149 pages.	☐
	28	Paper 7, IPR 2022-00996, Patent Owner Preliminary Response, filed September 9, 2022, 85 pages.	☐
	29	Paper 7, IPR 2022-00999, Patent Owner Preliminary Response, filed September 8, 2022, 82 pages.	☐
	30	Paper 10, IPR 2022-00996, Decision - Granting Institution of Inter Partes Review, dated December 7, 2022, 56 pages.	☐
	31	Paper 21, IPR 2022-00996, Patent Owner Response, filed March 28, 2023, 91 pages.	☐
	32	Paper 22, IPR 2022-00999, Patent Owner Response, filed March 28, 2023, 90 pages.	☐
	33	Paper 25, IPR 2022-00996, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
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	Examiner Name	FARROKH
	Attorney Docket Number	022955-000090

	34	Paper 26, IPR 2022-00999, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐
	35	Paper 31, IPR 2022-00996, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐
	36	Paper 33, IPR 2022-00999, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-10-13
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ELECTRONIC PAYMENT RECEIPT

APPLICATION #	RECEIPT DATE / TIME	ATTORNEY DOCKET #
17/582,797	**10/13/2023 05:28:08 PM ET**	**022955-000090**

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE	Utility - Nonprovisional Application under 35 USC 111(a)	PATENT #	-
CONFIRMATION #	3546	FILED BY	Lisa Elliott
PATENT CENTER #	62993059	AUTHORIZED BY	Khaled Shami
CUSTOMER #	151145	FILING DATE	01/24/2022
CORRESPONDENCE ADDRESS	-	FIRST NAMED INVENTOR	Chi-She Chen

Payment Information

PAYMENT METHOD	PAYMENT TRANSACTION ID	PAYMENT AUTHORIZED BY
DA / 220585	**E20230CH28438201**	**Lisa Elliott**

FEE CODE	DESCRIPTION	ITEM PRICE($)	QUANTITY	ITEM TOTAL($)
1801	REQUEST FOR CONTINUED EXAMINATION (RCE) - 1ST REQUEST (SEE 37 CFR 1.114)	1360.00	1	1360.00
			TOTAL AMOUNT:	**$1,360.00**

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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CUSTOMER #	151145	FIRST NAMED INVENTOR	Chi-She Chen
CORRESPONDENCE ADDRESS	-	AUTHORIZED BY	Khaled Shami

Documents

TOTAL DOCUMENTS: 96

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
2023-10-13 - IDS Pleading - 022955-000090.pdf	3	Miscellaneous Incoming Letter	146 KB
2023-10-13 - IDS1 - 022955-000090.pdf	10	Information Disclosure Statement (IDS) Form (SB08)	1444 KB
2023-10-13 - IDS2 - 022955-000090.pdf	7	Information Disclosure Statement (IDS) Form (SB08)	1406 KB
2023-10-13 - RCE - 022955-000090.pdf	3	Request for Continued Examination (RCE)	1368 KB
2023-10-13 - Resp to 7-13-23 FOA - 022955-000090.pdf	8	Amendment Submitted/Entered with Filing of Continued	152 KB

		Prosecution Application (CPA)/Request for Continued Examination(RCE)	
NPL--Day 4 redacted.pdf	338	Non Patent Literature	733 KB
NPL--Day 2 redacted.pdf	375	Non Patent Literature	745 KB
NPL--Ex_1041_Fairchild_Semiconductor_FAM2056_Datasheet.pdf	17	Non Patent Literature	416 KB
NPL--Ex_1040_Tex_Instruments_TPS51020_Datasheet.pdf	27	Non Patent Literature	1188 KB
NPL--Ex_1042_Power_Supply_Ref_Guide_Xilinx_FPGAs.pdf	33	Non Patent Literature	1142 KB
NPL--Ex_1048_DC-DC_Converter_Spec-Draft-_MPD4S014S.pdf	11	Non Patent Literature	1036 KB
NPL--Ex_1049_Micron_NAND_Flash_Memory_Datasheet.pdf	57	Non Patent Literature	1788 KB
NPL--Ex_1063_PCI_Local_Bus_Power_Supervisor.pdf	12	Non Patent Literature	253 KB
NPL--Ex_1071_Complaint_EDTX.pdf	49	Non Patent Literature	4082 KB
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NPL--Ex_1018_Petition_IPR-833_SK_hynix.pdf	70	Non Patent Literature	409 KB
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NPL--Ex_1026_JEDEC_Standard_DDR2_SDRAM_Spec.pdf	113	Non Patent Literature	2775 KB
NPL--Ex_1043_Power_Supply_Ref_Guide_Altera_FPGAs.pdf	40	Non Patent Literature	4544 KB
NPL--Ex_1045_JEDEC_Standard_DDR_SDRAM_Spec.pdf	77	Non Patent Literature	4358 KB
NPL--Ex_1061_Analog_Devices_ADM1066_Datasheet.pdf	36	Non Patent Literature	531 KB
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NPL--Ex_1046_JEDEC_Standard_DDR3_SDRAM_Spec.pdf	189	Non Patent Literature	8872 KB
NPL--Ex_1078_Analog_Devices.pdf	24	Non Patent Literature	581 KB
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NPL--Ex_2013_JEDEC_Standard_SDRAM_Unbuffered_SO-DIMM.pdf	26	Non Patent Literature	1875 KB
NPL--Ex_2102_PCI_Express_Power_and_Mini_Card_Solutions.pdf	2	Non Patent Literature	287 KB
NPL--Ex_2030_Wolfe_Depo.pdf	311	Non Patent Literature	895 KB
NPL--Ex_1003_Decl_Andrew_Wolfe.pdf	431	Non Patent Literature	20899 KB
NPL--Ex_2027_Transcend_DDR2_SO-DIMM.pdf	3	Non Patent Literature	2196 KB
NPL--Paper_10 - Decision Granting Institution.pdf	56	Non Patent Literature	990 KB
NPL--Paper_25 - Sams Reply to POR - IPR2022-00996.pdf	57	Non Patent Literature	4995 KB
NPL--Paper_26 - Sams Reply to POR - IPR2022-00999.pdf	57	Non Patent Literature	5309 KB
NPL--Paper_1 - Petition for IPR - IPR2022-00999.pdf	149	Non Patent Literature	12734 KB
NPL--Paper_1 - Petition for IPR - IPR2022-00996.pdf	151	Non Patent Literature	14323 KB
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NPL--Ex_1031_PCI_Local_Bus_Spec_Segment_06of06.pdf	15	Non Patent Literature	4469 KB
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NPL--Ex_1032_Power_Electronics_Converters_Applications_Design_Segment_01of03.pdf	16	Non Patent Literature	24422 KB
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NPL--Ex_1032_Power_Electronics_Converters_Applications_Design_Segment_03of03.pdf	5	Non Patent Literature	7738 KB
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NPL--Ex_1032_Power_Electronics_Converters_Applications_Design_Segment_02of03.pdf	16	Non Patent Literature	23863 KB

Digest

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NPL--Ex_2025_Micron_256Mb_SDR_SDRAM.pdf	363D9B5F778B50A48E69553FCA0311A2875D04EC7E425AD2A366309FD3013545772A84988607B719DE5B949FB0773D1C8F2E15FAAF592261DE9CA2721893C8AD
NPL--Ex_2032_CC_Order.pdf	03E2A169C9EAA5AE3D69566D04C58A66A61C4BEC9C57CE22735FEE0F16ADFBC81B8B6F55D13F4C8FBF3A8AF67C23D505AB190E6B2CE80043D3640098C41EDB73
NPL--Ex_2044_Micron_DDR2_SDRAM_RDIMM.pdf	18C5CA51CA966717F6A99F299408293F16E04CF9379B1D10B58356B71B7B33CF0E5768B07D5DAC9A86B9D532DF059759F21957EEF30F9B4645E3B1C1095ACB96

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NPL--Ex_2048_Micron_DDR2_SDRAM_FBDIMM.pdf	0B69975D3C1C7EFE1D9A455EE3D7C4C71E74D194992D95C0D41643F9B322BBF6C6FEC10C1280CA378F040CF74B54C8F543799AB66D83303567FF217368C16DDE
NPL--Ex_2043_Sams_Unveils_New_Power_Mgmt_DDR5_Modules.pdf	0892AF0BCE8570EC616259E317CC310ABEFD5508D21B303606F715AB0C989EDF559CAF377BB3D729A7EF264ED7E79CBC06CC187B8AD0E14A4EE63307E3BAB3D2
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NPL--Ex_2057_Micron_DDR5_Key_Module_Features.pdf	FE8EFA00A5DBA1A8502130DA557E4E033FACDFE0F867471322891FD472B898E4B5B27A601D6C03B43E7F770606811B267B20B082F3E8187E6BF31E652ECA486E
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NPL--Ex_1022_Petition_IPR-833_Micron.pdf	42274BB240E3EC970788FAAEDBD9AD07929769C96AD619A200105C92700F75D95A6B35EF2BD6346664565AAC7206F7D77007A68DED05B4371C60E98E4ABED8F

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage

submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.