

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AFTER FINAL REJECTION

Commissioner:

In response to the Final Office Action mailed July 13, 2023, and the Advisory Action mailed August 18, 2023, Applicant submits the following Amendment and Remarks.

Listing of Claims begins on page **2**.

Remarks begin on page **6**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) comprising:

a printed circuit board (PCB) including a set of voltage supply lines electrically connected to corresponding edge connections of a first set of edge connections, sixty four data lines electrically connected to corresponding edge connections of a second set of edge connections, and a set of address and control lines electrically connected to corresponding edge connections of a third set of edge connections;

a DIMM interface including the first, second and third set of edge connections, the DIMM interface configured to (i) fit into a memory socket connector of a host system, and (ii) provide a conduit for power, sixty four data signals, and address and control signals between the host system and the DIMM via the first, second and third set of edge connections, respectively;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) receive and monitor an input voltage from the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to other portions of the controller, wherein the controller is configured to perform one or more operations in response to the trigger signal, the one or more operations including a write operation to write data into the non-volatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a plurality of components coupled to the PCB, the plurality of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices; and

first, second, third and fourth buck converters coupled to the PCB and to the input

voltage supply line and configured to (i) receive power from the input voltage supply line, (ii) generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and (iii) output the first, second, third and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively;

wherein each component of the plurality of components (i) is not electrically connected to the input voltage supply line, (ii) is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and (iii) receives power only from one or more of the first, second, third and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices (i) is not electrically connected to the input voltage supply line, and (ii) receives power only from one or more of the first, second, third and fourth regulated voltage lines.

3. (Previously presented) The DIMM of claim 2, wherein the controller is further configured to control a plurality of power transition sequences.

4. (Currently amended) The DIMM of claim 3, wherein the plurality of power transition sequences includes first and second power transition sequences, the first power transition sequence includes turning power on or off to the first regulated voltage line in response to a first trigger condition of a plurality of trigger conditions, ~~and the plurality of trigger conditions includes a request from the host.~~

5. (Currently amended) The DIMM of claim 4, wherein the input voltage supply line is a first input voltage supply line, and wherein the first, second, third and fourth buck converters are coupled to a second input voltage supply line, and

wherein, during the second power transition sequence, the first, second, third and fourth buck converters are further configured to (i) receive power from the first input voltage supply line or the second input voltage supply line in response to a second trigger condition of the plurality of trigger conditions, (ii) generate, respectively, the first, second, third and fourth regulated voltages from either the power received from the first input voltage supply line or the power received from the second input voltage supply line, and (iii) ~~output~~ output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively.

6. (Currently amended) The DIMM of claim 24, wherein the controller is further configured to generate a respective trigger signal of a plurality of trigger signals in connection response to with a respective trigger condition of the plurality of trigger conditions, wherein the plurality of trigger conditions ~~that~~ include (i) a request from the host system ~~and or~~ (ii) the voltage monitor circuit detecting input voltage level deviation from one or more threshold voltages.

7. (Previously presented) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages specified as certain voltage values.

8. (Previously presented) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages corresponding to percentages of an operating voltage.

9. (Previously presented) the DIMM of claim 4, wherein the DIMM is configured to operate in a plurality of states including a first state and a second state, wherein the DIMM is further configured (i) to operate in the first state while power is turned on to the first regulated voltage line, and (ii) to operate in the second state while power is turned off to the first regulated voltage line.

10. (Previously presented) The DIMM of claim 9, wherein the first power transition sequence further includes turning power on to the plurality of DDR SDRAM devices, during both the first and second states, via one or more of the second, third and fourth regulated voltage lines.

11. (Currently amended) The DIMM of claim 10 further comprising:

a register coupled to the PCB, ~~to~~ the first regulated voltage line, and ~~to~~ the set of address and control lines, wherein:

during the first state, the register is configured to (i) receive and register address and control signals from the host via the set of address and control lines, and (ii) output registered address and control signals ~~to the plurality of the DDR SDRAM devices, and~~

during the second state, the register does not ~~couple output registered~~ address and control signals ~~from the host to the plurality of the DDR SDRAM devices.~~

12. (Previously presented) The DIMM of claim 2, wherein the DIMM interface comprises a standard 240-pin DDR2 edge connector.
13. (Previously presented) The DIMM of claim 2, wherein the controller is further configured to periodically perform the one or more operations at regular intervals of time.
14. (Previously presented) The DIMM of claim 13, wherein the regular intervals of time are every millisecond.
15. (Previously presented) The DIMM of claim 2, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

REMARKS

The Final Office Action mailed July 13, 2023, has been carefully considered.

Interview Record

Applicants gratefully acknowledge the courtesy extended to the undersigned representative during the Examiner interview conducted on September 13, 2023 between Mr. Khaled Shami, Mr. Marwan Fawal, and Examiner Hashem Farrokh. The substance of the interview related to the 35 USC 112(a) rejection as discussed below.

Rejection(s) Under 35 U.S.C. § 112, First Paragraph

Claims 2-15 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. The claims allegedly contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-A/A 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants respectfully disagree. The subject matter at issue is a fourth buck converter and a fourth regulated voltage, and as pointed out during the Examiner interview, paragraphs [00148] – [00149] of the originally-filed description, as well as FIG. 16 of the drawings, are example locations where support for these claimed components can be found.

Specifically, voltage conversion element 1120 is shown in FIG. 16 as comprising a buck converter 1122 (*i.e.* 1st buck converter); dual buck converter 1124 (*i.e.* 2nd and 3rd buck converters); and buck-boost converter 1126 (*i.e.* 4th buck converter). In addition, paragraph [00148] states that “[t]he conversion element 1120 may comprise a plurality of subblocks 1122, 1124, 1126 as schematically illustrated by FIG. 16,” that “[t]he sub-blocks [1122, 1124, 1126] may comprise various converter circuits such as buck-converters, boost converters, and buck-

boost converter circuits,” and that “sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16.” (ll. 4-9). Hence there are four buck converters described in [0148] that are referenced to schematic illustration of FIG. 16.

FIG. 16 schematically illustrates and labels the sub-blocks 1122, 1124, 1126 of the conversion element 1120 matching the description of paragraph [0148]. Specifically, the sub-block 1122 is labeled “Buck Converter”, the sub-block 1124 is labeled “Dual Buck Reg/Conv”, and the sub-block 1126 is labeled “Buck-Boost Converter”. Hence there are four buck converters illustrated in FIG. 16, which further shows the buck converters 1122, 1124, 1126 outputting four regulated voltages: 1102, 1104, 1105 and 1107.

Further support for a fourth buck converter and fourth regulated voltage can be found in paragraph [00149], which states that “[f]or example, there may be more or less sub-blocks [in conversion element 1120] which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values.” (ll. 3-5).

For these reasons at least, Applicants respectfully maintain that the claimed fourth buck converter and fourth regulated voltage are sufficiently described in the specification to meet the written description requirement of 35 U.S.C. § 112, and the rejection thereunder should be withdrawn.

Amendment to Claims

Claims 2, 4-6 and 11 have been amended for improved clarity in particularly pointing out and distinctly claiming certain aspects of the invention. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references. Any remarks made herein with respect to a given claim or amendment is intended

only in the context of that specific claim or amendment, and should not be applied to other claims, amendments or aspects of the claimed arrangement.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: DRAFT
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/DRAFT/
Khaled Shami, Reg. No. 38,745



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022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Lisa Elliott

PATENT CENTER # 62996054

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 16

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NPL-- Ex_1073_Netlist_FAC_Segm ent_04of10.pdf	5	Non Patent Literature	12163 KB
NPL-- Ex_1073_Netlist_FAC_Segm ent_01of10.pdf	21	Non Patent Literature	18258 KB
NPL-- Ex_1073_Netlist_FAC_Segm ent_05of10.pdf	1	Non Patent Literature	21819 KB
NPL-- Ex_1073_Netlist_FAC_Segm ent_02of10.pdf	10	Non Patent Literature	21195 KB

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Ex. 1002, p. 433

NPL-- Ex_1073_Netlist_FAC_Segment_06of10.pdf	2	Non Patent Literature	23814 KB
NPL-- Ex_1073_Netlist_FAC_Segment_03of10.pdf	19	Non Patent Literature	22137 KB
NPL-- Ex_1073_Netlist_FAC_Segment_07of10.pdf	2	Non Patent Literature	24066 KB
NPL-- Ex_1073_Netlist_FAC_Segment_08of10.pdf	3	Non Patent Literature	17591 KB
NPL-- Ex_1073_Netlist_FAC_Segment_09of10.pdf	3	Non Patent Literature	14195 KB
NPL-- Ex_1073_Netlist_FAC_Segment_10of10.pdf	5	Non Patent Literature	14286 KB
NPL-- Ex_2063_Netlist_Demonstratives_Segment_06of06.pdf	14	Non Patent Literature	7416 KB
NPL-- Ex_2063_Netlist_Demonstratives_Segment_01of06.pdf	32	Non Patent Literature	24114 KB
NPL-- Ex_2063_Netlist_Demonstratives_Segment_02of06.pdf	26	Non Patent Literature	23780 KB
NPL-- Ex_2063_Netlist_Demonstratives_Segment_04of06.pdf	32	Non Patent Literature	24053 KB

NPL-- Ex_2063_Netlist_Demonstrati ves_Segment_03of06.pdf	35	Non Patent Literature	24549 KB
NPL-- Ex_2063_Netlist_Demonstrati ves_Segment_05of06.pdf	41	Non Patent Literature	23385 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as

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Ex. 1002, p. 436

described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 = *		x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 = *		x \$480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

		(Column 1)		(Column 2)	(Column 3)	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	10/17/2023	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA		
	Total (37 CFR 1.16(i))	* 14	Minus	** 20	= 0	x \$100 =	0
	Independent (37 CFR 1.16(h))	* 1	Minus	*** 3	= 0	x \$480 =	0
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	0
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =	
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =	
	☐ Application Size Fee (37 CFR 1.16(s))						
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
						TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						HSLIE	
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/LELAND WATKINS/	
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".							
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.							

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

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022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Lisa Elliott

PATENT CENTER # 63014851

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
022955-000090 Supplemental Resp to 7-13- 23 FOA.pdf	8	Supplemental Response or Supplemental Amendment	152 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
022955-000090 Supplemental Resp to 7-13-23 FOA.pdf	9232DB88AFA16DFC24CF93DD50D9B19CC95244C7843EDD0D B7300698B356CA0AA6EE113BFE2723B30FA2A30FE04C4ED03 3965B9950B306382E179D1B20DE98E8

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE AFTER FINAL REJECTION

Commissioner:

This supplemental response is being filed in order to provide the signature of Applicant's representative. The previous response, filed on October 13, 2023, was marked "DRAFT" and was not signed or dated.

In response to the Final Office Action mailed July 13, 2023, and the Advisory Action mailed August 18, 2023, Applicant submits the following Amendment and Remarks.

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LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) comprising:

a printed circuit board (PCB) including a set of voltage supply lines electrically connected to corresponding edge connections of a first set of edge connections, sixty four data lines electrically connected to corresponding edge connections of a second set of edge connections, and a set of address and control lines electrically connected to corresponding edge connections of a third set of edge connections;

a DIMM interface including the first, second and third set of edge connections, the DIMM interface configured to (i) fit into a memory socket connector of a host system, and (ii) provide a conduit for power, sixty four data signals, and address and control signals between the host system and the DIMM via the first, second and third set of edge connections, respectively;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) receive and monitor an input voltage from the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to other portions of the controller, wherein the controller is configured to perform one or more operations in response to the trigger signal, the one or more operations including a write operation to write data into the non-volatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a plurality of components coupled to the PCB, the plurality of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices; and

first, second, third and fourth buck converters coupled to the PCB and to the input

voltage supply line and configured to (i) receive power from the input voltage supply line, (ii) generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and (iii) output the first, second, third and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively;

wherein each component of the plurality of components (i) is not electrically connected to the input voltage supply line, (ii) is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and (iii) receives power only from one or more of the first, second, third and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices (i) is not electrically connected to the input voltage supply line, and (ii) receives power only from one or more of the first, second, third and fourth regulated voltage lines.

3. (Previously presented) The DIMM of claim 2, wherein the controller is further configured to control a plurality of power transition sequences.

4. (Currently amended) The DIMM of claim 3, wherein the plurality of power transition sequences includes first and second power transition sequences, the first power transition sequence includes turning power on or off to the first regulated voltage line in response to a first trigger condition of a plurality of trigger conditions, ~~and the plurality of trigger conditions includes a request from the host.~~

5. (Currently amended) The DIMM of claim 4, wherein the input voltage supply line is a first input voltage supply line, and wherein the first, second, third and fourth buck converters are coupled to a second input voltage supply line, and

wherein, during the second power transition sequence, the first, second, third and fourth buck converters are further configured to (i) receive power from the first input voltage supply line or the second input voltage supply line in response to a second trigger condition of the plurality of trigger conditions, (ii) generate, respectively, the first, second, third and fourth regulated voltages from either the power received from the first input voltage supply line or the power received from the second input voltage supply line, and (iii) ~~output~~ output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively.

6. (Currently amended) The DIMM of claim 24, wherein the controller is further configured to generate a respective trigger signal of a plurality of trigger signals in connection response to with a respective trigger condition of the plurality of trigger conditions, wherein the plurality of trigger conditions ~~that~~ include (i) a request from the host system ~~and or~~ (ii) the voltage monitor circuit detecting input voltage level deviation from one or more threshold voltages.

7. (Previously presented) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages specified as certain voltage values.

8. (Previously presented) The DIMM of claim 6, wherein the one or more threshold voltages include threshold voltages corresponding to percentages of an operating voltage.

9. (Previously presented) the DIMM of claim 4, wherein the DIMM is configured to operate in a plurality of states including a first state and a second state, wherein the DIMM is further configured (i) to operate in the first state while power is turned on to the first regulated voltage line, and (ii) to operate in the second state while power is turned off to the first regulated voltage line.

10. (Previously presented) The DIMM of claim 9, wherein the first power transition sequence further includes turning power on to the plurality of DDR SDRAM devices, during both the first and second states, via one or more of the second, third and fourth regulated voltage lines.

11. (Currently amended) The DIMM of claim 10 further comprising:

a register coupled to the PCB, ~~to~~ the first regulated voltage line, and ~~to~~ the set of address and control lines, wherein:

during the first state, the register is configured to (i) receive and register address and control signals from the host via the set of address and control lines, and (ii) output registered address and control signals ~~to the plurality of the DDR SDRAM devices, and~~

during the second state, the register does not ~~couple output registered~~ address and control signals ~~from the host to the plurality of the DDR SDRAM devices.~~

12. (Previously presented) The DIMM of claim 2, wherein the DIMM interface comprises a standard 240-pin DDR2 edge connector.
13. (Previously presented) The DIMM of claim 2, wherein the controller is further configured to periodically perform the one or more operations at regular intervals of time.
14. (Previously presented) The DIMM of claim 13, wherein the regular intervals of time are every millisecond.
15. (Previously presented) The DIMM of claim 2, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

REMARKS

The Final Office Action mailed July 13, 2023, has been carefully considered.

Interview Record

Applicants gratefully acknowledge the courtesy extended to the undersigned representative during the Examiner interview conducted on September 13, 2023 between Mr. Khaled Shami, Mr. Marwan Fawal, and Examiner Hashem Farrokh. The substance of the interview related to the 35 USC 112(a) rejection as discussed below.

Rejection(s) Under 35 U.S.C. § 112, First Paragraph

Claims 2-15 stand rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. The claims allegedly contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-A/A 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

Applicants respectfully disagree. The subject matter at issue is a fourth buck converter and a fourth regulated voltage, and as pointed out during the Examiner interview, paragraphs [00148] – [00149] of the originally-filed description, as well as FIG. 16 of the drawings, are example locations where support for these claimed components can be found.

Specifically, voltage conversion element 1120 is shown in FIG. 16 as comprising a buck converter 1122 (*i.e.* 1st buck converter); dual buck converter 1124 (*i.e.* 2nd and 3rd buck converters); and buck-boost converter 1126 (*i.e.* 4th buck converter). In addition, paragraph [00148] states that “[t]he conversion element 1120 may comprise a plurality of subblocks 1122, 1124, 1126 as schematically illustrated by FIG. 16,” that “[t]he sub-blocks [1122, 1124, 1126] may comprise various converter circuits such as buck-converters, boost converters, and buck-

boost converter circuits,” and that “sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16.” (ll. 4-9). Hence there are four buck converters described in [0148] that are referenced to schematic illustration of FIG. 16.

FIG. 16 schematically illustrates and labels the sub-blocks 1122, 1124, 1126 of the conversion element 1120 matching the description of paragraph [0148]. Specifically, the sub-block 1122 is labeled “Buck Converter”, the sub-block 1124 is labeled “Dual Buck Reg/Conv”, and the sub-block 1126 is labeled “Buck-Boost Converter”. Hence there are four buck converters illustrated in FIG. 16, which further shows the buck converters 1122, 1124, 1126 outputting four regulated voltages: 1102, 1104, 1105 and 1107.

Further support for a fourth buck converter and fourth regulated voltage can be found in paragraph [00149], which states that “[f]or example, there may be more or less sub-blocks [in conversion element 1120] which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values.” (ll. 3-5).

For these reasons at least, Applicants respectfully maintain that the claimed fourth buck converter and fourth regulated voltage are sufficiently described in the specification to meet the written description requirement of 35 U.S.C. § 112, and the rejection thereunder should be withdrawn.

Amendment to Claims

Claims 2, 4-6 and 11 have been amended for improved clarity in particularly pointing out and distinctly claiming certain aspects of the invention. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references. Any remarks made herein with respect to a given claim or amendment is intended

only in the context of that specific claim or amendment, and should not be applied to other claims, amendments or aspects of the claimed arrangement.

Conclusion

In view of the preceding discussion, Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: October 17, 2023
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

Search Notes 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/ 205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF
711	110	11/01/2023	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF
Inventor/Assignee Search Updated	10/31/2023	HF
EAST Text, CPC, FACET Search Updated	10/31/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F3/0685	G06F3/00	11/01/2023	HF
G06F13/28	G06F13/00	11/01/2023	HF
G06F2212/205	G06F2212/00	11/01/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	01 November 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06F	/	3	/ 06
NON-CLAIMED			
/		/	

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	110

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	14	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	01 November 2023	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	2	6

<i>Issue Classification</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47															
CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	9	10												
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4	5	13	14												
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6	7														
7	8														
8	9														

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 14	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner) _____ (Date) 01 November 2023		O.G. Print Claim(s) 2	O.G. Print Figure 6

Bibliographic Data

Application No: 17/582,797

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /HASHEM FARROKH/

Examiner's Signature

Initials

Title:

MEMORY WITH ON-MODULE POWER MANAGEMENT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/24/2022	711	2138	
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA, UNITED STATES

INVENTORS

Chi-She Chen, Walnut, CA, UNITED STATES

Jeffrey C. Solomon, Irvine, CA, UNITED STATES

Scott H. Milton, Irvine, CA, UNITED STATES

Jayesh Bhakta, Cerritos, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17328019 05/24/2021 PAT 11232054

17328019 is a CON of 17138766 12/30/2020 PAT 11016918

17138766 is a CON of 15934416 03/23/2018ABN

15934416 is a CON of 14840865 08/31/2015 PAT 9928186

14840865 is a CON of 14489269 09/17/2014 PAT 9158684

14489269 is a CON of 13559476 07/26/2012 PAT 8874831

13559476 has PRO of 61512871 07/28/2011

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12240916 is a CON of 12131873 06/02/2008ABN

12131873 has PRO of 60941586 06/01/2007

FOREIGN APPLICATIONS

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UNITED STATES

ADDRESS

Samsung Electronics Co., Ltd.
Ex. 1002, p. 454

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797	
	Filing Date		2022-01-24	
	First Named Inventor	CHEN		
	Art Unit	2138		
	Examiner Name	FARROKH		
	Attorney Docket Number	022955-000090		

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Art Unit	2138	
Examiner Name	FARROKH	
Attorney Docket Number	022955-000090	

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2	Exhibit 2015, Siemens, 3.3V 2M x 64/72 Bit 1 BANK SDRAM Module, HYS64/72V2200GU-8/-10, 3.3V 4M x 64/72 Bit 2 BANK SDRAM Module, HYS64/72V4200GU-8/-10, 168 pin unbuffered DIMM Modules, downloaded from www.datasheetcatalog.com; 1998, 18 pages	☐
3	Exhibit 2016, PCI Bus Variation Technology Note; copyright 2006 by Euresys, 9 pages.	☐
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5	Exhibit 2018, Transcend, Product Support, What is the difference between SDRAM, DDR1, DDR2, DDR3 and DDR4?, available online at https://www.transcend-info.com/support/faq-296#:~:text=DDR3's prefetch buffer width is,according to the temperature variation , downloaded August 24, 2022, 2 pages.	☐
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8	Exhibit 2024, SCHMID, Understanding Hard Drive Performance, available online at https://www.tomshardware.com/reviews/understanding-hard-drive-performance,1557-5.html , downloaded August 15, 2022, published March 5, 2007, 17 pages.	☐
9	Exhibit 2025, Micron, SDR SDRAM, MT48LC64M4A2 - 16 Meg x 4 x 4 Banks, MT48LC32M8A2 - 8 Meg x 8 x 4 Banks, MT48LC16M16A2 - 4 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 94 pages.	☐
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11	Exhibit 2027, Transcend, DDR2 SO-DIMM, copyright 2012 by Transcend, 3 pages.	☐

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Art Unit		2138
Examiner Name	FARROKH	
Attorney Docket Number		022955-000090

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13	Exhibit 2030, IPR 2022-00996 and IPR 2022-00999, Videoconference Deposition of Andrew Wolfe, Ph.D. regarding US Patent Nos. 11,016,918 and 11,232,054, 311 pages, dated March 16, 2023.	☐
14	Exhibit 2031, IPR 2022-00996, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,016,918, 452 pages, executed on May 16, 2022.	☐
15	Exhibit 2034, IPR 2022-00996, Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,016,918, 144 pages, executed on March 28, 2023.	☐
16	Exhibit 2032, Claim Construction Order, filed December 14, 2022, 35 pages.	☐
17	Exhibit 2033, Defendants' Objections to Claim Construction Memorandum Order, filed December 29, 2022, 11 pages.	☐
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20	Exhibit 2046, JEDEC Standard No. 21G, Page 4-20-11-1, PG2-6400/PG2-5300/PG2-4200/PG2-3200, DDR2 Unbuffered SO-DIMM, Reference Design Specification, Revision 2.5, July 2008, 60 pages.	☐
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22	Exhibit 2056, IPR 2022-00645, Remote Videotaped Deposition by Virtual Zoom of Andrew Wolfe, Ph.D. regarding US Patent No. 7,619,912, 297 pages, dated January 4, 2023.	☐

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Art Unit	2138	
Examiner Name	FARROKH	
Attorney Docket Number	022955-000090	

23	Exhibit 2057, Micron Technical Brief: Micron DDR5: Key Module Features, DDR4 vs. DDR5 DIMM, copyright 2020 by Micron Technology, Inc., 7 pages.	☐
24	Exhibit 2069, Netlist, Demonstrative Exhibit for IPR 2022-00990 and IPR 2022-00999, filed September 8, 2023, 180 pages.	☐
25	Exhibit 2102, LEE et al., PCI Express Power and Mini Card Solutions - Design Note 346, Linear Technology - Design Notes, copyright 2004 by Linear Technology Corporation, 2 pages.	☐
26	Paper 1, IPR 2022-00996, Petition for Inter Partes Review of US Patent No. 11,016,918, filed May 17, 2022, 151 pages.	☐
27	Paper 1, IPR 2022-00999, Petition for Inter Partes Review of US Patent No. 11,232,054, filed May 17, 2022, 149 pages.	☐
28	Paper 7, IPR 2022-00996, Patent Owner Preliminary Response, filed September 9, 2022, 85 pages.	☐
29	Paper 7, IPR 2022-00999, Patent Owner Preliminary Response, filed September 8, 2022, 82 pages.	☐
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31	Paper 21, IPR 2022-00996, Patent Owner Response, filed March 28, 2023, 91 pages.	☐
32	Paper 22, IPR 2022-00999, Patent Owner Response, filed March 28, 2023, 90 pages.	☐
33	Paper 25, IPR 2022-00996, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐

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Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

34	Paper 26, IPR 2022-00000, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐
35	Paper 31, IPR 2022-00006, Patent Owner's Sur Reply, filed August 4, 2023, 48 pages.	☐
36	Paper 32, IPR 2022-00000, Patent Owner's Sur Reply, filed August 4, 2023, 48 pages.	☐

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EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	10/30/2023
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

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STATEMENT BY APPLICANT**
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Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-10-13
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc. CONFIRMATION NO.: 3546
SERIAL NO.: 17/582,797 ART UNIT: 2138
FILING DATE: 2022-01-24 EXAMINER: FARROKH
TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Commissioner:

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following proceedings involving patents that are in the family of the above-identified patent application:

Proceeding	Status
<i>Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas LLC v. Netlist, Inc.</i> , Case No. IPR2022-00418 (P.T.A.B.), filed January 14, 2022	Final Written Decision - Determining All Challenged Claims Unpatentable entered August 28, 2023
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00615 (P.T.A.B.), filed February 17, 2022	Institution Granted October 19, 2022
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00996 (P.T.A.B.), filed May 17, 2022	Institution Granted December 7, 2022
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00999 (P.T.A.B.), filed May 17, 2022	Institution Granted December 6, 2022
2:21-cv-00463-JRG (EDTX Case asserting '918 and '054 against Samsung)	Closed - Termination Date August 11, 2023
2:22-cv-00203-JRG (EDTX Case asserting '918 and '054 against Micron)	Open - Filing Date June 10, 2022
1:22-cv-00134-DII (WDTX Case asserting the '833 against Micron)	Open - Filing Date April 28, 2021

/HASHEM FARROKH/

10/30/2023

Information Disclosure Statement

Listed on accompanying two IDS Forms PTO/SB/08a are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). Due to the Request for Continued Examination (RCE) filed concurrently, this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL 1-50 and NPL 1-36** (as listed on the two PTO/SB/08a forms) are submitted. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 17/328,019, filed 05-24-2021 (now U.S. Pat. No. 11,232,054), 17/138,766, filed 12-30-2020 (now U.S. Pat. No. 11,016,918), 15/934,416, filed 03-23-2018 (now abandoned), 14/840,865, filed 08-31-2015 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next

communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed two IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

Date: October 13, 2023

/Khaled Shami/

Khaled Shami, Registration No.: 38745

Customer No.: 151145

VORYS, SATER, SEYMOUR and PEASE LLP

1909 K Street, NW, 9th Floor
Washington, DC 20006-1152
Tel: (202) 467-8800

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

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	1	5563839	A	1996-10-08	HERDT et al.	
	2	6067241	A	2000-05-23	LU	
	3	6693840	B2	2004-02-17	SHIMADA et al.	
	4	6798709	B2	2004-09-28	SIM et al.	
	5	6856556	B1	2005-02-15	HAJECK	
	6	7023187	B2	2006-04-04	SHEARON et al.	
	7	7061214	B2	2006-06-13	MAYEGA et al.	
	8	7692938	B2	2010-04-06	PETTER	

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9	7719866	B2	2010-05-18	BOLDO	
10	7721130	B2	2010-05-18	PRETE et al.	
11	7724604	B2	2010-05-25	AMIDI et al.	
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	1	20060080515	A1	2006-04-13	SPIERS et al.	
	2	20060174140	A1	2006-08-03	HARRIS et al.	
	3	20070136523	A1	2007-06-14	BONELLA et al.	
	4	20080101147	A1	2008-05-01	AMIDI	
	5	20080238536	A1	2008-10-02	HAYASHI et al.	

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6	20090034354	A1	2009-02-05	RESNICK	
7	20100205470	A1	2010-08-12	MOSHAYEDI et al.	
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	1	Transcript, Day 2 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 17, 2023, 375 pages.	☐
	2	Transcript, Day 4 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 19, 2023, 338 pages.	☐
	3	Exhibit 1003, IPR 2022-00999, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,232,054, 431 pages, executed on May 16, 2022.	☐

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Examiner Name	FARROKH
Attorney Docket Number	022955-000090

4	Exhibit 1014, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014, 69 pages.	☐
5	Exhibit 1015, IPR 2014-00994, Decision - Denying Institution of Inter Partes Review, issued December 16, 2014, 16 pages.	☐
6	Exhibit 1016, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22, 2014, 67 pages.	☐
7	Exhibit 1017, IPR 2014-01370, Decision - Denying Institution of Inter Partes Review, issued March 13, 2015, 19 pages.	☐
8	Exhibit 1018, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017, 70 pages.	☐
9	Exhibit 1019, IPR 2017-00649, Decision - Denying Institution of Inter Partes Review, issued July 24, 2017, 17 pages.	☐
10	Exhibit 1020, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017, 78 pages.	☐
11	Exhibit 1021, IPR 2017-00692, Final Written Decision, issued July 5, 2018, 42 pages.	☐
12	Exhibit 1022, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 14, 2022, 76 pages.	☐
13	Exhibit 1026, JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2B (Revision of JESD7-2A), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, January 2005, 113 pages.	☐
14	Exhibit 1027, JEDEC STANDARD, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 190 pages.	☐

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15	Exhibit 1028, JEDEC STANDARD, FBDIMM Specification: DDR2 SDRAM Fully Buffered, DIMM (FBDIMM) Design Specification, JESD205, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 129 pages.	☐
16	Exhibit 1031, PCI Local Bus Specification, Revision 2.2, December 18, 1998, 322 pages.	☐
17	Exhibit 1032, Power Electronics: Converters, Applications, and Design, Second Edition, copyright 1995 by John Wiley & Sons, Inc., 37 pages.	☐
18	Exhibit 1040, Texas Instruments, TPS51020, Dual, Voltage Mode, DDR Selectable, Synchronous, Step-Down Controller for Notebook System Power, SLUS564B, July 2003 (revised December 2003), 27 pages.	☐
19	Exhibit 1041, Fairchild Semiconductor, FAN5026, Dual DDR/Dual-Output PWM Controller, October 2005, 17 pages.	☐
20	Exhibit 1042, Murata Manufacturing Co., Ltd, Power Supply Reference Guide for XILINX FPGAs, September 2006, 33 pages.	☐
21	Exhibit 1043, Murata Products, Power Supply Reference Guide for ALTERA FPGAs, Catalog No. DC-03-A, 2008, 40 pages.	☐
22	Exhibit 1045, JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, June 2000, 77 pages.	☐
23	Exhibit 1046, JEDEC STANDARD, DDR3 SDRAM Specification, JESD79-3A (Revision of JESD79-3), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, September 2007, 189 pages.	☐
24	Exhibit 1048, Murata Manufacturing, DC-DC Converter Specification(DRAFT), MPD4S014S, January 21, 2008, 11 pages.	☐
25	Exhibit 1049, Micron, NAND Flash Memory, MT29F2G08AABWP/MT29F2G16AABWP, MT29F4G08BABWP/MT29F4G16BABWP, MT29F8G08EABWP, copyright 2004 by Micron Technology, Inc., 57 pages.	☐

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Attorney Docket Number	022955-000090	

26	Exhibit 1058, LENK, Simplified Design of Switching Power Supplies, Linear Technology, EDN Series for Design Engineers, copyright 1995 by Butterworth-Heinemann, 9 pages.	☐
27	Exhibit 1061, Analog Devices, Super Sequencer with Margining Control and Auxiliary ADC Inputs, ADM1066, copyright 2006 by Analog Devices, Inc., 36 pages.	☐
28	Exhibit 1062, Analog Devices, Analog Dialogue, Volume 40, Number 2, 2006, 24 pages.	☐
29	Exhibit 1063, National Semiconductor, LMC6953, PCI Local Bus Supervisor, October 1996, 12 pages.	☐
30	Exhibit 1067, Lattice Semiconductor Corporation, LatticeXP Family Data Sheet, Version 04.2, March 2006, 127 pages.	☐
31	Exhibit 1068, Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed October 15, 2021, 82 pages.	☐
32	Exhibit 1069, First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed January 18, 2022, 122 pages.	☐
33	Exhibit 1071, Complaint, filed December 20, 2021, 49 pages.	☐
34	Exhibit 1072, The Samsung Defendants' Answer, filed April 12, 2022, 37 pages.	☐
35	Exhibit 1073, First Amended Complaint, filed May 3, 2022, 71 pages.	☐
36	Exhibit 1075, IPR 2022-00999, Deposition of William Mangione-Smith, Ph.D. regarding US Patent No. 11,232,054, 245 pages, dated June 12, 2023.	☐

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Attorney Docket Number	022955-000090	

37	Exhibit 1076, IPR 2022-00999, redline comparing Declarations - Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,232,054, 105 pages, executed on March 29, 2022.	☐
38	Exhibit 1077, Netlist, Technology Tutorial: In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same, Inv No. 337-TA-1023, May 8, 2017, 11 pages.	☐
39	Exhibit 1078, Analog Devices, Step-Down DC-to-DC Controller, ADP1821, copyright 2005-2007 by Analog Devices, Inc., 24 pages.	☐
40	Exhibit 2001, IPR 2022-00999, Declaration of Dr. Sunil P. Khatri regarding US Patent No. 11,232,054, 68 pages, executed on September 8, 2022.	☐
41	Exhibit 2003, BELLONI et al., 24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current, ISSCC 2008 / Session 24 / Analog Power Techniques / 24.6, 2008 IEEE International Solid-State Circuits Conference, 3 pages.	☐
42	Exhibit 2004, MA et al., Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode, IEEE Journal of Solid-State Circuits, Volume 38, Number 1, January 2003, pages 89-100 (12 pages).	☐
43	Exhibit 2006, Micron, Technical Note: Power Solutions for DDR2 Notebook PCs, TN-47-05 DDR2 Power Solutions for Notebooks, copyright 2004 by Micron Technology, Inc., 16 pages.	☐
44	Exhibit 2007, Texas Instruments, LP2996-N, LP2996A DDR Termination Regulator, SNOSA40K, November 2002 (revised December 2016), 39 pages.	☐
45	Exhibit 2008, JAMECO ELECTRONICS, Jameco Part Number 843868, National Semiconductor: LP2996: DDR Termination Regulator, June 2006, 19 pages.	☐
46	Exhibit 2009, JAMECO ELECTRONICS, Jameco Part Number 843930, National Semiconductor: LP2997: DDR-II Termination Regulator, June 2006, 13 pages.	☐
47	Exhibit 2010, National Semiconductor: LP2998: DDR-II and DDR-I Termination Regulator, December 12, 2007, 18 pages.	☐

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Attorney Docket Number	022955-000090

48	Exhibit 2011, BERGVELD, Battery Management Systems: Design by Modelling, copyright 2001 by Royal Philips Electronics N.V., 328 pages.	☐
49	Exhibit 2012, ROMO, DDR Memories: Comparison and Overview, NXP, pages 70-73 (4 pages), September 21, 2007.	☐
50	Exhibit 2013, JEDEC Standard No. 21-C, Page 4.20.3-1; PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, 20 pages, downloaded August 16, 2022.	☐

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Examiner Signature	/HASHEM FARROKH/	Date Considered	10/30/2023
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Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2023-10-13
Name/Print	Khaled Shami	Registration Number	38745

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L67	92	("5563839" "6067241" "6693840" "6798709" "6856556" "1023187" "7061214" "7692938" "7719866" "7721130" "1724604" "10672458" "20060080515" "20060174140" "20070136523" "20080101147" "20080238536" "20090034354" "20100205470" "20100257304").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/23 04:41 PM
L68	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 11:04 AM
L69	7	((plurality OR multiple OR several) WITH (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM) near2 (devices OR chips OR dies OR modules)) WITH (coupled OR connected) SAME (regulated near2 voltage)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/10/31 12:03 PM
L70	7	((plurality OR multiple OR several) WITH (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM) near2 (devices OR chips OR dies OR modules)) WITH (coupled OR connected) SAME (regulated near2 voltage)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 12:03 PM
L71	5	70 AND ("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 12:04 PM

L72	7	((plurality OR multiple OR several) WITH (((synchronous ADJ dynamic ADJ random ADJ access ADJ memory) OR SDRAM) near2 (devices OR chips OR dies OR modules)) WITH (coupled OR connected) SAME (regulated near2 voltage))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2023/10/31 12:07 PM
L73	5	72 AND ("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 12:07 PM
L74	5	72 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 12:09 PM
L75	7	72 AND ((G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2023/10/31 12:09 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 11/08/2023
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/08/2023

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	02/08/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

151145 7590 11/08/2023
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	02/08/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via Patent Center or EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	11/08/2023	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW			ART UNIT	
9th Floor			PAPER NUMBER	
Washington, DC 20006-1152			2138	

DATE MAILED: 11/08/2023

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/17/2023.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-15. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>10/13/2023</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
---	--

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION:

2. This office action is in response to the communication(s) filed on 10/17/2023. There are a total of 14 claims pending in the application. Claims 2, 4-6 and 11 have been amended; claim 1 has been canceled; and no new claims have been added.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 10/13/2023 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the Examiner. However, the documents listed as non-patent literature documents and shown by lined-through have not be considered by the Examiner. The reason for not considering is that title of actual documents are not readily identifiable and/or are different from IDS list. For example, in IDS listing many documents include an Exhibit number, which are not included in the actual documents. Furthermore, many of documents listed appear to have large number pages with small portion of pages may be relevant to the claims of current application. It is being suggested that applicant(s) include a title for each of one-to-one correspond to the title that has been listed, point to the portion(s) of the listed non-literature documents, which is/are directly relevant to the claims of the instant application. See MPEP 609.04(a) for more information.

RESPONSE TO REMARKS:

4. Applicant's arguments have been fully considered and the have been persuasive. In the final office action mailed 07/13/2023, the Examiner rejected claims 2-15 under 35 USC § 112(a), first paragraph, indication there is no description/support for a fourth buck converter as claimed in the independent claim 2. However, The Applicant states that each of the sub-blocks 1122, 1124, and 1126 in the conversion element 1120 in the Fig.16 matching description of paragraph [0148] describe or support buck converters,

including the fourth buck converter. Specifically, sub-block 1122 is buck converter, sub-block 1126 is buck-boost converter, and sub-block 1124 is a dual buck converter is generating two regulated output voltages. Thus, the three buck converters generate or supply 4 regulated voltages (e.g., page 6 and 7 of the Remarks, see also the interview summary mailed 09/21/2023).

REASON FOR ALLOWANCE:

5. *Claims 2-14 are considered to be allowable.*

The reason for allowance of the independent claim 2 are the following: in interpreting the pending claim(s), in view of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates , nor renders obvious the recited combination as a whole including the limitation(s):

“first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line, generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and output the first, second, third and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively; wherein each component of the plurality of components is not electrically connected to the input voltage supply line, is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only from one or more of the first, second, third and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM devices is not electrically connected to the input voltage supply line, and receives power only from one or more of the first, second, third and fourth regulated voltage lines.”

6. *Dependent claims 3-15 are allowable at least for the reasons indicated above including all the limitations of the allowable base claim 2 upon which they depend.*

7. *Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably*

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

DIRECTION OF FUTURE CORRESPONDENCES:

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 17/582,797	Filing Date 01/24/2022	☐ To be Mailed
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ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE (\$)	FEE (\$)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	x \$100 =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	x \$480 =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED - PART II

	(Column 1)		(Column 2)	(Column 3)	RATE (\$)	ADDITIONAL FEE (\$)
AMENDMENT	02/08/2024		CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	* 19	Minus	** 20	= 0	x \$100 = 0
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$480 = 0
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						0
AMENDMENT			CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =
	☐ Application Size Fee (37 CFR 1.16(s))					
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))					
TOTAL ADD'L FEE						
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LIE
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/BRENDA L TURNER/
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".						
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.						

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
02/08/2024 04:28:49 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Yayoi Bourne

PATENT CENTER # 64262523

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Michael Messinger

Documents

TOTAL DOCUMENTS: 11

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
RCE - 022955-90.pdf	3	Request for Continued Examination (RCE)	1322 KB
NPL--3--Decision Granting Institution and Joinder_11016918__IPR202 300406.pdf	7	Non Patent Literature	36 KB
NPL--4--Decision Granting Institution and Joinder_11232054__IPR202 300405.pdf	7	Non Patent Literature	36 KB
NPL--2--IPR Petition_11232054__IPR202 300405.pdf	147	Non Patent Literature	8935 KB
NPL--1--IPR	151	Non Patent Literature Samsung Electronics Co., Ltd. Ex. 1002, p. 488	10266 KB

Petition_11016918__IPR202
300406.pdf

NPL --5--Decision Final

Written Decision Determining_11016918__IP R202200996.pdf	91	Non Patent Literature	3097 KB
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NPL--6--Decision Final

Written Decision Determining_11232054__IP R202200999.pdf	80	Non Patent Literature	19492 KB
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IDS - 022955-90.pdf	4	Information Disclosure Statement (IDS) Form (SB08)	1241 KB
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022955-000090 2-8-24 Amendment.pdf	13	-	147 KB
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022955-000090 2-8-24 Amendment-AMSB.pdf	(1-1)	1	Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE)	109 KB
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022955-000090 2-8-24 Amendment-CLM.pdf	(2-9)	8	Claims	132 KB
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022955-000090 2-8-24 Amendment-REM.pdf	(10-13)	4	Applicant Arguments/Remarks Made in an Amendment	117 KB
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Digest

DOCUMENT

MESSAGE DIGEST(SHA-512)

RCE - 022955-90.pdf	754EBCA98506D4E03E86715E1FD28A9EB806B98E304FABCB 189B8C5717870CA4EB81802566F05FE991B7185D5AC014BAC B94CFF9095FAFA92D5D6A636E672C5F
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NPL--4--Decision Granting Institution and Joinder_11232054__IPR20230 0405.pdf	CAE036AF208BB02ED2D27776DABD67FD523814A8305933412 DB94C544263025A788CBC77E89702ABE96A24C5BDDE8F5FA 1F54E8D1761CF766F35D22A67B7D2A0
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NPL--2--IPR Petition_11232054__IPR20230	DE0564DD24012EDF04CB151F8A126F2CC20A7E8CA9B9DAA9 B5DCF3AF01006C5322F24CD97FBA2B96756C1B4C67E0CC8D
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0405.pdf	564B899C1F58A74F96CB0BF2A1D463D6
NPL--1--IPR Petition_11016918__IPR20230 0406.pdf	0E275C8054348DE217AF1776BE839D4CE5C6CF4F3245E567F 0B27E8338C6801A7BCBB3A2B8A5D3381592707F7D5E1B94A5 1427BA8EC48B547B3AB8C106DF2509
NPL --5--Decision Final Written Decision Determining_11016918__IPR2 02200996.pdf	042C79ED4B350DB84D66A25070780B61F8829E44236C925632 94C1393212FABCD74D5525A85927BB452AC107F3A789F624 F0B81BCA6A80E8169E380A38CC802
NPL--6--Decision Final Written Decision Determining_11232054__IPR2 02200999.pdf	44B52A818BBEDC12A6F43CDA745E0EF3821BA909367F91972 689BD71C23EBF00C9B7DFCC58D47A05927AE3D4555C37639 9395E5CD0B91E1DA1BA5D0AC2D0C40D
IDS - 022955-90.pdf	86B78FC874B6D878228462CFAEB9E6874FD32839201466B438 38D58EF5B5CE2E078F84ADC0C0AF02892538472DF84F3EB3 B729D81B2CB826B9E88073A57074FF
022955-000090 2-8-24 Amendment.pdf	E00EA22CA74F62D645121BF4C27CCE4CA05CAFCEBB01AB0 1AD7BB242CBC814C184A5D106E7265AA27518702230DFE247 401C06D31D0BE556DBD1DC2C1F0388A9
022955-000090 2-8-24 Amendment-AMSB.pdf	160B076E801BFB2E0CEA0E8128F08F6E012B4715F8765185F0 5F5FDD212EF872BB7C46ACF47118D91B7890E69F8EC6F7FE 75DFC06E5F09274DD68E7C2BCA602F
022955-000090 2-8-24 Amendment-CLM.pdf	989E25C388AFB38A7642F04232B2017B3F0A14B69A783754B8 7306EBCF1120F201C9F510C307CA89F497DAB6483D5DFEB4 DE4B81F0BBC7DDD3068B8262AAB5A3
022955-000090 2-8-24 Amendment-REM.pdf	64720DEB8227E73E63CD14871B0CFAEB9784FACA2BD76F88 B1A1724EDBFED1A6A44C8AF9719FF44DD346EDC35D3A0B4 AF01607C396D2F9BFF19EC7A4DC21B449

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)
2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to
~~corresponding edge connections of a~~ the first set of edge connections, a set of~~sixty four~~ data lines electrically connected to ~~the corresponding edge connections of a~~ a second set of edge connections,
and a set of address and control lines electrically connected to ~~the corresponding edge connections of a~~ a third set of edge connections;

~~a DIMM interface including the first, second and third set of edge connections, the DIMM interface configured to (i) fit into a memory socket connector of a host system, and (ii) provide a conduit for power, sixty four data signals, and address and control signals between the host system and the DIMM via the first, second and third set of edge connections, respectively;~~

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) ~~receive and~~ monitor an input voltage ~~from~~ supplied via

the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, ~~one or more operations~~ in response to the trigger signal, ~~the one or more operations including~~ a write operation to write data into the ~~non-volatile~~ nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a ~~plurality set~~ of components coupled to the PCB, the ~~plurality set~~ of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines; and

first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line and configured to ~~(i)~~ receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, ~~the first, second, third and fourth buck converters being further configured to~~ ~~(ii)~~ generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and ~~(iii)~~ to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line ~~;~~

wherein each component of the ~~plurality set~~ of components ~~(i) is not electrically connected to the input voltage supply line,~~ ~~(ii)~~ is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and ~~(iii)~~ receives power only ~~from~~ via the one or more of the first, second, third and fourth regulated voltage lines, ~~and wherein the plurality of DDR SDRAM devices (i) is not electrically connected to the input voltage supply line, and (ii) receives power only from one or more of the first, second, third and fourth regulated~~

voltage lines[[.]], and

wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control power delivery to one or more components of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is turned off and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state.

3 – 5. (Canceled)

6. (Currently amended) The DIMM of claim 2[[4]], wherein the controller is further configured to periodically perform one or more write operations at regular intervals of time in response to an additional trigger signal that is associated with an additional trigger condition, the additional trigger condition including a request from the host system or detection of a generate a respective trigger signal of a plurality of trigger signals in response to a respective trigger condition of the plurality of trigger conditions, wherein the plurality of trigger conditions include (i) a request from the host system ~~[[or]]~~ (ii) the voltage monitor circuit detecting input voltage level deviation from one or more threshold voltages.

7. (Currently amended) The DIMM of claim 6, wherein the first preset threshold voltage or the one or more threshold voltages include threshold voltages specified as certain voltage values.

8. (Currently amended) The DIMM of claim 6, wherein the first preset threshold voltage or the one or more threshold voltages include threshold voltages specified as a percentage corresponding to percentages of an operating voltage of the DIMM.

9 – 10. (Canceled)

11. (Currently amended) The DIMM of claim 2[[10]] further comprising:

a register coupled to the PCB, the first regulated voltage line, and the set of address and control lines, wherein:

during the first state, the register is configured to receive power via the first regulated voltage line, [(i)] receive and register address and control signals from the host system via the set of address and control lines, and [(ii)] output registered address and control signals, and

during the second state, the register does not output registered address and control signals.

12 -13. (Canceled)

14. (Currently amended) The DIMM of claim 6[[13]], wherein the regular intervals of time are every millisecond.

15. (Previously presented) The DIMM of claim 2, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

16. (New) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, a set of data lines electrically connected to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to monitor an input voltage supplied via the input voltage

supply line, generate a trigger signal upon detecting a first trigger condition, and transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the first trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines; and

first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line of the set of voltage supply lines and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, third and fourth buck converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line,

wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines,

wherein, in response to a second trigger condition, the controller is configured to turn power via the first regulated voltage line off or on, and

wherein, in response to a third trigger condition, the controller is configured to turn power via the second regulated voltage line off or on.

17. (New) The DIMM of claim 16, wherein the second or third trigger condition includes a request from the host system or detection of a voltage level deviation from one or more threshold voltages.

18. (New) The DIMM of claim 17, wherein the controller is further configured to periodically perform write operations in response to a fourth trigger condition, each of the write operations being performed in a respective time period of a plurality of time periods.

19. (New) The DIMM of claim 18, wherein each time period is about a millisecond.

20. (New) The DIMM of claim 17, wherein the first preset threshold voltage and the one or more threshold voltages include a threshold voltage specified as a voltage value and/or a threshold voltage specified as a percentage of an operating voltage of the DIMM.

21. (New) The DIMM of claim 16, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

22. (New) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, a set of data lines electrically connected to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller

coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to monitor an input voltage supplied via the input voltage supply line, to generate a trigger signal upon detecting a first trigger condition, and to transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the first trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines; and

first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, third and fourth buck converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line,

wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines, and

wherein, in response to a second trigger condition, the controller is further configured to turn off power via the first regulated voltage line while power via the second, third and fourth regulated voltage lines is turned on.

23. (New) The DIMM of claim 22, wherein the second trigger condition includes a request from the host system or detection of a voltage level deviation from one or more threshold voltages.
24. (New) The DIMM of claim 23, wherein the controller is further configured to periodically perform write operations in response to a third trigger condition, each of the write operations being performed in a respective time period of a plurality of time periods.
25. (New) The DIMM of claim 24, wherein each time period is about a millisecond.
26. (New) The DIMM of claim 23, wherein the first preset threshold voltage and the one or more threshold voltages include a threshold voltage specified as a voltage value and/or a threshold voltage specified as a percentage of an operating voltage of the DIMM.
27. (New) The DIMM of claim 22, wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

**Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

AMENDMENT

Commissioner:

In response to the Notice of Allowance mailed November 8, 2023, Applicant submits the following Amendment and Remarks, accompanied by a Request for Continued Examination (RCE) and Information Disclosure Statement (IDS).

Listing of Claims begins on page **2**.

Remarks begin on page **10**.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

REMARKS

By this Amendment, Applicant has **amended claims 2, 6-8, 11 and 14; canceled claims 3-5, 9-10, and 12-13; and added new claims 16-27.**

Claims 2, 6-8, 11, and 14-27 are now pending.

Information Disclosure Statement

Acknowledgement of the Information Disclosure Statement filed concurrently herewith is respectfully requested.

Amendment to Claims

Claims 2, 6-8, 11 and 14 have been amended for improved clarity in particularly pointing out and distinctly claiming certain aspects of the invention. No amendment made is related to the statutory requirements of patentability unless expressly stated herein. No amendment is made for the purpose of narrowing the scope of any claim, unless Applicant argues herein that such amendment is made to distinguish over a particular identified reference or combination of references.

For the examiner's convenience, claim 2 is reproduced hereinbelow in clean version for ease of reading:

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, a set of data lines electrically connected to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to (i) monitor an input voltage supplied via the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines; and

first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, third and fourth buck converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line,

wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines, and

wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control power delivery to one or more components of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is turned off and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state.

Canceled Claims

Claims 3-5, 9-10, and 12 have been canceled without prejudice or disclaimer of the subject matter contained therein.

Newly-Added Claims

Claims 16-27 have been added to further particularly point out and distinctly claim certain aspects of the invention.

Conclusion

Applicant respectfully urges that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 22-0585.

Respectfully submitted,

Date: February 8, 2024
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

UNITED STATES
PATENT AND TRADEMARK OFFICEP.O. Box 1450
Alexandria, VA 22313 - 1450
www.uspto.gov

ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/582,797RECEIPT DATE / TIME
02/08/2024 04:28:49 PM Z ETATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY Yayoi Bourne

PATENT CENTER # 64262523

AUTHORIZED BY Michael Messinger

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE
ADDRESS -FIRST NAMED
INVENTOR Chi-She Chen

Payment Information

PAYMENT METHOD
DA / 220585PAYMENT TRANSACTION ID
E202428G29348203PAYMENT AUTHORIZED BY
Yayoi BournePRE-AUTHORIZED ACCOUNT
220585PRE-AUTHORIZED CATEGORY
37 CFR 1.16 (National application filing, search, and examination fees); 37
CFR 1.17 (Patent application and reexamination processing fees); 37 CFR
1.19 (Document supply fees); 37 CFR 1.20 (Post Issuance fees); 37 CFR 1.21
(Miscellaneous fees and charges)

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1820	REQUEST FOR CONTINUED EXAMINATION (RCE)- 2ND AND SUBSEQUENT REQUEST (SEE 37 CFR 1.114)	2000.00	1	2000.00
TOTAL AMOUNT:				\$2,000.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

Samsung Electronics Co., Ltd.
Ex. 1002, p. 504

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

1	Copy of Petition for Inter Partes Review of US Patent No.: 11,016,918, IPR No.: IPR2023-00406, 151 pages, filed January 6, 2023.	☐
2	Copy of Petition for Inter Partes Review of US Patent No.: 11,232,054, IPR No.: IPR2023-00405, 147 pages, filed January 6, 2023.	☐
3	Copy of Decision Granting Institution of Inter Partes Review and Granting Motion for Joinder for US Patent No.: 11,016,918, IPR No.: IPR2023-00406, 7 pages, entered June 23, 2023.	☐
4	Copy of Decision Granting Institution of Inter Partes Review and Granting Motion for Joinder for US Patent No.: 11,232,054, IPR No.: IPR2023-00405, 7 pages, entered June 23, 2023.	☐
5	Copy of Decision of Final Written Decision Determining All Challenged Claims Unpatentable Dismissing Petitioner's Motion to Exclude for US Patent No.: 11,016,918, IPR No.: IPR2022-00996, 91 pages, entered December 6, 2023.	☐
6	Copy of Decision of Final Written Decision Determining All Challenged Claims Unpatentable Dismissing Petitioner's Motion to Exclude for US Patent No.: 11,232,054, IPR No.: IPR2022-00999, 80 pages, entered December 5, 2023.	☐

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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***EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-02-08
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	17582797	Filing Date	2022-01-24	Docket Number (if applicable)	022955-000090	Art Unit	2138
First Named Inventor	CHEN			Examiner Name	FARROKH		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 220585

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-02-08
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

<i>Notice of References Cited</i>	Application/Control No. 17/582,797		Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH		Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
*	A	US-20120271990-A1	10-2012	Chen; Chi-She	G06F3/065	711/E12.008
*	B	US-20070136523-A1	06-2007	Bonella; Randy M.	G06F12/0866	711/E12.019
*	C	US-20080126624-A1	05-2008	Prete; Edoardo	G11C7/106	710/53
	D					
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	I					
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FOREIGN PATENT DOCUMENTS

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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
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	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
 Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

Search Notes 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/ 205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF
711	110	11/01/2023	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF
Inventor/Assignee Search Updated	10/31/2023	HF
EAST Text, CPC, FACET Search Updated	10/31/2023	HF
Inventor/Assignee Search Updated	02/22/2024	HF
EAST Text, CPC, FACET Search Updated	02/22/2024	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F3/0685	G06F3/00	11/01/2023	HF
G06F13/28	G06F13/00	11/01/2023	HF
G06F2212/205	G06F2212/00	11/01/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
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NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	22 February 2024	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

INTERNATIONAL CLASSIFICATION			
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NON-CLAIMED			
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US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	110

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	19	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138 (Primary Examiner)	22 February 2024 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1		10	11	19										
1	2	6	11	12	20										
	3		12	13	21										
	4		13	14	22										
	5	6	14	15	23										
2	6	7	15	16	24										
3	7	8	16	17	25										
4	8	9	17	18	26										
	9	10	18	19	27										

NONE	Total Claims Allowed:	
(Assistant Examiner)	(Date)	19
/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	22 February 2024	O.G. Print Claim(s)
(Primary Examiner)	(Date)	1
		O.G. Print Figure
		6

PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L79	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 01:54 PM
L80	4	("11016918").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 01:58 PM
L81	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 02:04 PM
L82	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	ON	2024/02/22 02:04 PM

			IBM_TDB)				
L83	0	((first near2 second near2 third near2 fourth) OR four OR "4" OR plurality) near5 (buck ADJ converters)) SAME (coupled OR connected OR attached) SAME ((printed ADJ circuit ADJ board) OR PCB) SAME (input near2 voltage near2 supply near2 line) SAME (receiv\$3 near2 power) SAME (supply near2 line)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 03:01 PM
L84	0	((double ADJ data ADJ rate) OR DDR) near2 SDRAM) SAME (devices OR chips OR dies OR ICs) SAME (operable OR configured) SAME ((receiv\$3 OR output\$4) near2 data) SAME (data ADJ lines) SAME based SAME (control near5 address signals)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 03:18 PM
L85	0	(buck ADJ converters) SAME (coupled OR connected OR attached) SAME ((printed ADJ circuit ADJ board) OR PCB) SAME (input near2 voltage near2 supply near2 line) SAME (receiv\$3 near2 power) SAME (supply near2 line)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/02/22 03:24 PM
L86	51	(buck ADJ converters) SAME (coupled OR connected OR attached) SAME ((printed ADJ circuit ADJ board) OR PCB)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2024/02/22 03:25 PM
L87	8	((buck ADJ converters) SAME (coupled OR connected OR attached) SAME ((printed ADJ circuit ADJ board) OR PCB)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2024/02/22 03:25 PM
L88	2	86 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/02/22 03:26 PM
L89	3	87 AND ("BHAKTA; JAYESH".ine. OR	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/02/22 03:27 PM

		"CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)					
L90	5	86 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/02/22 03:29 PM
L91	7	86 AND ((G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/02/22 03:31 PM

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

U.S.PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear		
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.						T ⁵

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

1	Copy of Petition for Inter Partes Review of US Patent No.: 11,016,918, IPR No.: IPR2023-00406, 151 pages, filed January 6, 2023.	☐
2	Copy of Petition for Inter Partes Review of US Patent No.: 11,232,054, IPR No.: IPR2023-00405, 147 pages, filed January 6, 2023.	☐
3	Copy of Decision Granting Institution of Inter Partes Review and Granting Motion for Joinder for US Patent No.: 11,016,918, IPR No.: IPR2023-00406, 7 pages, entered June 23, 2023.	☐
4	Copy of Decision Granting Institution of Inter Partes Review and Granting Motion for Joinder for US Patent No.: 11,232,054, IPR No.: IPR2023-00405, 7 pages, entered June 23, 2023.	☐
5	Copy of Decision of Final Written Decision Determining All Challenged Claims Unpatentable Dismissing Petitioner's Motion to Exclude for US Patent No.: 11,016,918, IPR No.: IPR2022-00996, 91 pages, entered December 6, 2023.	☐
6	Copy of Decision of Final Written Decision Determining All Challenged Claims Unpatentable Dismissing Petitioner's Motion to Exclude for US Patent No.: 11,232,054, IPR No.: IPR2022-00999, 80 pages, entered December 5, 2023.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	02/22/2024
--------------------	------------------	-----------------	------------

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-02-08
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Bibliographic Data

Application No: 17/582,797

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged: /HASHEM FARROKH/

Examiner's Signature

Initials

Title:

MEMORY WITH ON-MODULE POWER MANAGEMENT

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
01/24/2022	711	2138	
RULE			

APPLICANTS

Netlist, Inc., Irvine, CA, UNITED STATES

INVENTORS

Chi-She Chen, Walnut, CA, UNITED STATES

Jeffrey C. Solomon, Irvine, CA, UNITED STATES

Scott H. Milton, Irvine, CA, UNITED STATES

Jayesh Bhakta, Cerritos, CA, UNITED STATES

CONTINUING DATA

This application is a CON of 17328019 05/24/2021 PAT 11232054

17328019 is a CON of 17138766 12/30/2020 PAT 11016918

17138766 is a CON of 15934416 03/23/2018ABN

15934416 is a CON of 14840865 08/31/2015 PAT 9928186

14840865 is a CON of 14489269 09/17/2014 PAT 9158684

14489269 is a CON of 13559476 07/26/2012 PAT 8874831

13559476 has PRO of 61512871 07/28/2011

13559476 is a CIP of 12240916 09/29/2008 PAT 8301833

12240916 is a CON of 12131873 06/02/2008ABN

12131873 has PRO of 60941586 06/01/2007

FOREIGN APPLICATIONS

IF REQUIRED, FOREIGN LICENSE GRANTED**

02/01/2022

STATE OR COUNTRY

UNITED STATES

ADDRESS

Samsung Electronics Co., Ltd.
Ex. 1002, p. 526

FILING FEE RECEIVED

\$1,980



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 02/28/2024
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 02/28/2024

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	05/28/2024

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 40% the amount of undiscounted fees, and micro entity fees are 20% the amount of undiscounted fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via the USPTO patent electronic filing system.

By mail, send to: Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications. **Because electronic patent issuance may occur shortly after issue fee payment, any desired continuing application should preferably be filed prior to payment of this issue fee in order not to jeopardize copendency.**

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

151145 7590 02/28/2024
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via the USPTO patent electronic filing system or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546

TITLE OF INVENTION: MEMORY WITH ON-MODULE POWER MANAGEMENT

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	05/28/2024

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2138	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required)

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via the USPTO patent electronic filing system ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	02/28/2024	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW				
9th Floor				
Washington, DC 20006-1152			ART UNIT	PAPER NUMBER
			2138	
DATE MAILED: 02/28/2024				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. The United States Patent and Trademark Office (USPTO) collects the information in this record under authority of 35 U.S.C. 2. The USPTO's system of records is used to manage all applicant and owner information including name, citizenship, residence, post office address, and other information with respect to inventors and their legal representatives pertaining to the applicant's/owner's activities in connection with the invention for which a patent is sought or has been granted. The applicable Privacy Act System of Records Notice for the information collected in this form is COMMERCE/PAT-TM-7 Patent Application Files, available in the Federal Register at 78 FR 19243 (March 29, 2013).

<https://www.govinfo.gov/content/pkg/FR-2013-03-29/pdf/2013-07341.pdf>

Routine uses of the information in this record may include disclosure to:

- 1) law enforcement, in the event that the system of records indicates a violation or potential violation of law;
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- 3) a contractor of the USPTO having need for the information in order to perform a contract;
- 4) the Department of Justice for determination of whether the Freedom of Information Act (FOIA) requires disclosure of the record;
- 5) a Member of Congress submitting a request involving an individual to whom the record pertains, when the individual has requested the Member's assistance with respect to the subject matter of the record;
- 6) a court, magistrate, or administrative tribunal, in the course of presenting evidence, including disclosures to opposing counsel in the course of settlement negotiations;
- 7) the Administrator, General Services Administration (GSA), or their designee, during an inspection of records conducted by GSA under authority of 44 U.S.C. 2904 and 2906, in accordance with the GSA regulations and any other relevant (i.e., GSA or Commerce) directive, where such disclosure shall not be used to make determinations about individuals;
- 8) another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c));
- 9) the Office of Personnel Management (OPM) for personnel research purposes; and
- 10) the Office of Management and Budget (OMB) for legislative coordination and clearance.

If you do not furnish the information requested on this form, the USPTO may not be able to process and/or examine your submission, which may result in termination of proceedings, abandonment of the application, and/or expiration of the patent.

Notice of Allowability	Application No. 17/582,797	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 02/08/2024.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2,6-8,11 and 14-27. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. _____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>02/08/2024</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
---	--

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

DETAILED ACTION:

2. This office action is in response to the communication(s) filed on 02/08/2024. There are a total of 19 claims pending in the application. Claims 2, 6-8, 11 and 14 have been amended; claims 1, 3-5, 9-10, and 12-13 have been canceled; and new claims 16-27 have been added.

INFORMATION CONCERNING IDS:

The information disclosure statement (IDS) submitted on 02/08/2024 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the Examiner.

RESPONSE TO REMARKS:

3. Applicant's arguments have been fully considered and they have been persuasive. Applicant has amended the independent claim 2 and added the new independent claims 16 and 22. The amended independent claim 2 includes the allowable subject matters that previously made the claim allowable. The new independent claims 16 and 22 recite substantially similar features as independent claim 2.

REASON FOR ALLOWANCE:

5. Claims 2, 6-8, 11, and 14-27 are considered to be allowable. The reason for allowance of the independent claim 2 are the following: in interpreting the pending claim(s), in view of the specification, the Examiner finds the claimed invention to be patentably distinct from the prior art of record. The prior art of record neither anticipates, nor renders obvious the recited combination as a whole including the limitation(s):

“a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the

set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines; and first, second, third and fourth buck converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, third and fourth buck converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line[;]], wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage line”

Independent claims 16 and 22 include similar limitations and are allowed for the reasons indicated above with respect to the independent claim 1.

6. *Dependent claims 2, 6-8, 11, 14-15, 17-21, and 23-27 are allowable at least for the reasons indicated above including all the limitations of the allowable base claims upon which they depend.*

7. *Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”*

DIRECTION OF FUTURE CORRESPONDENCES:

Art Unit: 2138

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

9. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

10. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/HASHEM FARROKH/
Primary Examiner, Art Unit 2138



UNITED STATES PATENT AND TRADEMARK OFFICE

USPTO Automated Interview Request (AIR)

May 10 2024

This paper requesting to schedule and/or conduct an interview is appropriate because:

This submission is requested to be accepted as an authorization for this interview to communicate via the internet. Recognizing that Internet communications are not secure, I hereby authorize the USPTO to communicate with the undersigned concerning scheduling of the interview via video conference, instant messaging, or electronic mail, and to conduct the interview in accordance with office practice including video conferencing.

Name(s) :

Michael Milan Stojsavljevic

S-signature:

/Michael Milan Stojsavljevic/

Registration Number:

80857

U.S. Application Number:

17582797

Confirmation Number:

3546

E-mail Address:

mmstojsavljevic@vorys.com

Phone Number:

+1 2163733437

Proposed Time of Interview:

5-16-2024 1:30 PM ET

Preferred Interview Type:

Video Conference

I am the applicant or applicant's representative for this application.

Topic for Discussion:

Presenting example IDS documents and listings to confirm that each document in the IDS is considered by the Examiner.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	05/28/2024	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW			ART UNIT	
9th Floor			PAPER NUMBER	
Washington, DC 20006-1152			2138	
			NOTIFICATION DATE	DELIVERY MODE
			05/28/2024	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/582,797	Applicant(s) Chen et al.		
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No	Page 1 of 1

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
HASHEM FARROKH	Primary Examiner	Video Conference
MileTyson Ovich	Attorney	

Date of Interview: 22 May 2024

Issues Discussed:

Other

An applicant initiated interview with the Applicant, Mr. Mike Tyson Ovich (Reg. # 80,857), was conducted on 05/22/2024 (a copy of the interview agenda is attached). In the Notice of Allowance (NOA) mailed 11/08/2023, the Examiner stated the IDS' filed 10/13/2023 list/include a number of NPL documents not readily identifiable and some of documents contain many number pages. The Examiner suggested the Applicant provide the documents with a unique title or sequence number that can be identified from the corresponding document title or sequence number listed in the IDS'. The Examiner also suggested, since some of documents have large number pages and some portions of each document may include subject matters not related to the claims of instant application, the Applicant identify the portion(s) of NPL documents, which are more relevant to claims of instant application. The interview was video conference in order to see and communicate the best way for the Applicant to provide the IDS'

☒ Attachment

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
<p>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</p> <p>Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing</p>	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

Interview Agenda for Application No.: 17/582,797; Attn. Docket No. 022955-000090

Attendees:

Primary Examiner Hashem Farrokh, Art Unit 2138

Mike Stojcavljevic, USPTO Registration No. 80,857

Summary:

Discuss the IDS list below and appended documents corresponding to the IDS list to ensure consideration by the Examiner. The non-patent literature listed in the IDS of the Notice of Allowance dated 8 November 2023 (NOA) were shown lined-through and were not considered by the Examiner. The reasoning provided on page 2 of the NOA stated that the:

“title of actual documents are not readily identifiable and are different from the IDS list. For example, in IDS listing many documents include an Exhibit number, which are not included in the actual documents... It is being suggested that applicant(s) include a title for each of one-to-one corresponding to the title that has been listed, point to the portions(s) of the listed non-literature documents, which is/are directly relevant to the claims of the instant application.”

Accordingly, the documents appended correspond to the brief example IDS list below and are provided as an example of documents that include a title that correspond to the title that has been listed. Additionally, most of the documents were cited as exhibits in related proceedings, such that the documents are wholly relevant, but listings will point to portions of the listed non-literature documents where appropriate.

	1	Exhibit 2014, Qimonda, Internet Data Sheet, Rev. 1.25, June 2007, 24 pages.	
	...		
	3	Exhibit 2016, PCI Bus Variation -- Technology Note, copyright 2006 by Euresys, 9 pages.	
	...		

查询HYB39SC256[80/16]0FE-6供应商

德多邦，专业PCB打样工厂，24小时加急出货

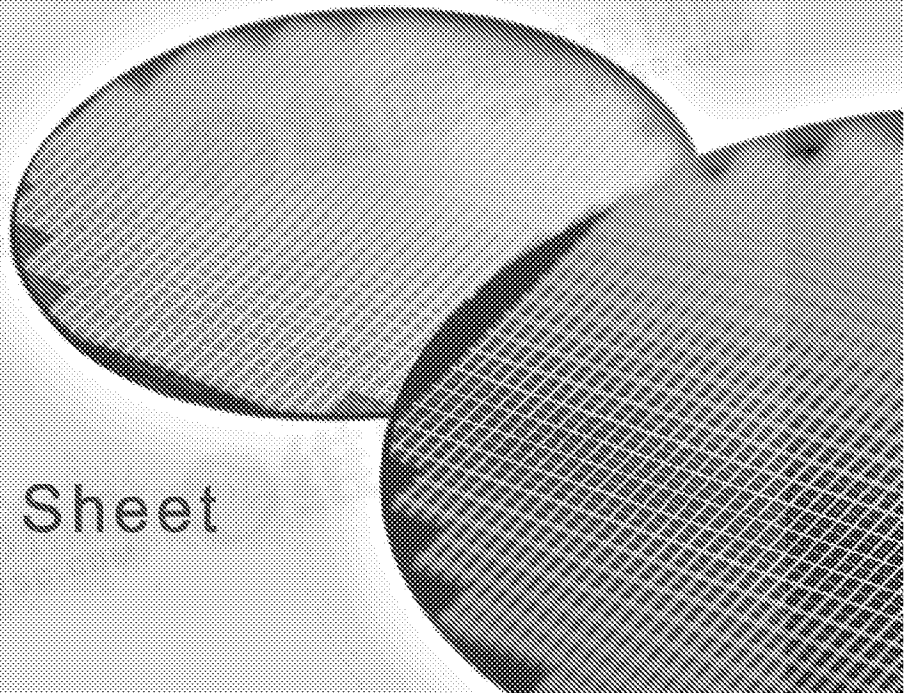
June 2007

HYB39SC256[80/16]0FE HYI39SC256[80/16]0FF

256-MBit Synchronous DRAM
Green Product
SDRAM

Internet Data Sheet

Rev. 1.25



Netlist Ex 2014
Samsung v Netlist
IPR2022-00999

Qimonda
Samsung Electronics Co., Ltd.
Ex. 1002, p. 540

PDF
www.qimonda.com
netlistase.com



HY[B/I]39SC256[80/16]0F[E/F]
256-MBit Synchronous DRAM

HYB39SC256[80/16]0FE, HYI39SC256[80/16]0FF	
Revision History: 2007-06, Rev. 1.25	
Page	Subjects (major changes since last revision)
All	Adapted internet edition
41	Corrected in figure 28 (auto refresh) tRC to tRFC
Previous Revision: 2007-06, Rev. 1.24	
8	Corrected figure 1
11,12	Corrected block diagram
Previous Revision: 2007-06, Rev. 1.23	
18	Added text for Auto Refresh Command (CBR)
Previous Revision: 2007-06, Rev. 1.22	
6	Corrected ball DQ0 to 2,8A for data signals x16 organization
6	Corrected data Data Signal Bus [7:0] for data signals x8 organization
Previous Revision: 2007-06, Rev. 1.21	
13	Corrected operation command "Power Down / Clock suspend ..." in truth table
Previous Revision: 2007-05, Rev. 1.2	
13	Corrected operation command "Power Down Exit" to X (WE#)
15	Corrected text to "After the mode register is set a NOP command is required", chapter 3.2
19	Corrected text to "One clock delay is required for mode entry and exit", chapter 3.4
21	Corrected the line "Input Capacitances: CK" in table 10, chapter 4
21	Corrected to A0-A12 in table 10, chapter 4
22	Corrected tCK MIN in table 13
22	Corrected CLE setup time in table 13
Previous Revision: 2007-05, Rev. 1.11	
6	Corrected A6 position from H to 3H in table 3
Previous Revision: 2006-09, Rev. 1.1	

We Listen to Your Comments

Any information within this document that you feel is wrong, unclear or missing at all?

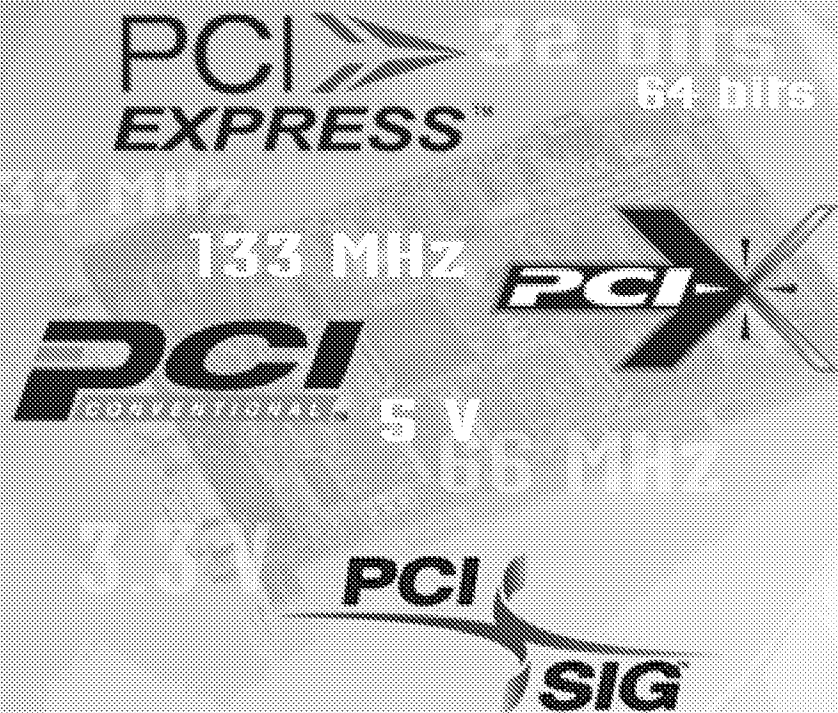
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Please send your proposal (including a reference to this document) to:

techdoc@qimonda.com

Technology Note

PCI Bus Variation



www.euresys.com

info@euresys.com

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Ex. 1002, p. 542

PCI Bus Variation

Yves Joskin, R&D Manager

Euresys s.a.

14, Avenue du Pré-Aily

B-4031 Angleur

Belgium

info@euresys.com

Contents

Purpose of this Application Note	3	Signaling Voltage	5
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PCI-X	3	Add-in Card Variants	5
PCI Express	3	Interoperability	6
PCI Performance	3	General rules	6
Characterizing Parameters	3	Bus width interoperability	6
Bus Width	3	Signaling voltage interoperability	7
Clock Speed	3	Bus variant interoperability	8
Data Rate	4	Clock speed interoperability	8
PCI Bandwidth Summary	4	Powering Voltage	8
Number of Slots	4		
The PCI Bus as a Set of Slots	4		
Maximum Slot Summary	4		

References

PCI

The PCI bus specification is handled by the PCI-SIG (PCI Special Interest Group), which is an association of numerous industrial actors in the field.

Euresys s.a. is a member of the PCI-SIG (vendor ID h1805).

The web site address of PCI-SIG is <http://www.pcisig.com>

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5563838	A	1996-10-08	MART et al.	
	2	6351827	B1	2002-02-26	CO et al.	
	3	6418065	B2	2002-07-09	SATO et al.	
	4	6434044	B1	2002-08-13	GONGWER et al.	
	5	7034569	B1	2006-04-25	BALASUBRAMANIAN et al.	
	6	7161820	B2	2007-01-09	FUNABA et al.	
	7	7166934	B2	2007-01-23	DEWEY	
	8	7269764	B2	2007-09-11	DART et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

9	7426649	B2	2008-09-16	BRITTAIN et al.	
10	7613880	B2	2009-11-03	MIURA	
11	7644216	B2	2010-01-05	FAHR et al.	
12	7656735	B2	2010-02-02	KAGAN et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

Add

U.S.PATENT APPLICATION PUBLICATIONS

Remove

Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20090020608	A1	2009-01-22	BENNETT et al.	
	2	20090027844	A1	2009-01-29	CHEN et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

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FOREIGN PATENT DOCUMENTS

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1	10-2005-0073902	KR	A	2005-07-18	SAMSUNG ELECTRONICS CO LTD	Machine Translation included as NPL 1	☒

If you wish to add additional Foreign Patent Document citation information please click the Add button

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NON-PATENT LITERATURE DOCUMENTS

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17582797
Filing Date		2022-01-24
First Named Inventor	CHEN	
Art Unit	2138	
Examiner Name	FARROKH	
Attorney Docket Number	022955-000090	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Machine Translation of KR 10-2005-0073902 A, published July 18, 2005, 7 pages.	☐
	2	RENESAS, ISL6537 ACPI Regulator/Controller for Dual Channel DDR Memory Systems Data Sheet, Rev 6.00, 16 pages, July 18, 2007.	☐
	3	Intersil, ISL6532B ACPI Regulator/Controller for Dual Channel DDR Memory Systems Data Sheet, 16 pages, July 2004.	☐
	4	Freescale Semiconductor, Hardware and Layout Design Considerations for DDR Memory Interfaces, Rev. 6, NXP, 48 pages, April 2007.	☐
	5	PLESSL and PLATZNER, TKDM - A Reconfigurable Co-processor in a PC's Memory Slot, Swiss Federal Institute of Technology, January 15, 2004, 8 pages.	☐
	6	RENESAS, ISL6534 Dual PWM with Linear Data Sheet, Rev 2.00, 29 pages, November 18, 2005.	☐
	7	Maxim Integrated, DC-DC Converter Tutorial, APP 2031, 14 pages, November 29, 2001.	☐

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
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ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 65697055

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 11

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
NPL--1-MachTrans_KR20050073902 A.pdf	7	Non Patent Literature	76 KB
NPL--5-TKDM.pdf	8	Non Patent Literature	402 KB
NPL--7-MAXIM.pdf	14	Non Patent Literature	779 KB
NPL--6-ISL6534.pdf	29	Non Patent Literature	928 KB
NPL--2-ISL6537.pdf	16	Non Patent Literature	2034 KB
NPL--3-ISL6532B.pdf	16	Non Patent Literature	2254 KB

FOR--1-KR20050073902A.pdf	10	Foreign Reference	4164 KB
NPL--4-NXP.pdf	48	Non Patent Literature	4730 KB
022955-000090 Resp to 2-28-24 RCE Response to Notice of Allowance.pdf	4	Amendment Submitted/Entered with Filing of Continued Prosecution Application (CPA)/Request for Continued Examination(RCE)	158 KB
022955-000090 RCE form.pdf	3	Request for Continued Examination (RCE)	1334 KB
IDS3 - 022955-000090.pdf	5	Information Disclosure Statement (IDS) Form (SB08)	1242 KB

Digest

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B3185B95DF423C9E4605DC0E65DBEDB

022955-000090 Resp to 2-28-
24 RCE Response to Notice of
Allowance.pdf A6AABCC0D7E2095224749D7D85121EC0774E1524E12DFF903
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022955-000090 RCE form.pdf 39D5F896E9CB2A57BDAA73606678254660F9B433BF935A6964
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IDS3 - 022955-000090.pdf E7C30BD96605E7FD9C4AD28A330307F840EAA0043FAAC990C
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B1FC5F337CA0298BD22A537ED5648A

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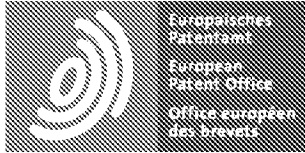
National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

**Espacenet**

KR20050073902A SEMICONDUCTOR MEMORY MODULE AND METHOD OF TESTING OPERATING MARGIN THEREOF, AND SEMICONDUCTOR MEMORY APPARATUS

Applicants: SAMSUNG ELECTRONICS CO LTD [KR]

Inventors: LEE HI CHOON [KR], CHOI HYE IN [KR]

Classifications:

IPC **G11C29/00**; (IPC1-7): G11C29/00;

CPC **B29C70/06 (KR); E01F7/045 (KR);**

Priorities: KR20040002020A 2004-01-12

Application: KR20040002020A 2004-01-12

Publication: KR20050073902A 2005-07-18

Published as: KR20050073902A

SEMICONDUCTOR MEMORY MODULE AND METHOD OF TESTING OPERATING MARGIN THEREOF, AND SEMICONDUCTOR MEMORY APPARATUS

Abstract

The present invention discloses a semiconductor memory module, a test method thereof, and a semiconductor memory device. The semiconductor memory module of the present invention includes a circuit board having a plurality of external input/output terminals, an interface circuit installed on the circuit board, a plurality of semiconductor memory chips, and a non-volatile memory chip. The interface circuit interfaces signal transmission between a plurality of external input terminals and the internal circuit. A plurality of semiconductor memory chips are connected to an interface circuit, input an external address signal with mode setting information, decode the input mode setting information, and generate a mode setting control signal. In normal mode, the mode setting control signal is transmitted to the normal operation circuit unit. and, in test mode, a mode setting control signal is provided to the test operation circuit. The nonvolatile memory chip stores the initial values of the semiconductor memory chips to provide the initial values of the semiconductor memory chips to the outside through the interface circuit when the system is initially booted. Therefore, in the present invention, various tests can be performed on the chips inside the memory module by mode setting, thereby improving test efficiency during the test process.

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경기도용인시기흥읍구갈리세종리첸시빌2-3BL203-201
최혜인
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심사청구 : 없음

(54) 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트방법과 반도체 메모리 장치

요약

본 발명은 반도체 메모리 모듈 및 그 테스트 방법과 반도체 메모리 장치를 개시한다. 본 발명의 반도체 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스회로, 복수의 반도체 메모리 칩들, 및 불휘발성 메모리 칩을 포함한다. 인터페이스회로는 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스한다. 복수의 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 모드세팅 제어신호를 테스트동작회로부에 제공한다. 불휘발성 메모리 칩은 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 따라서, 본 발명에서는 메모리 모듈 내부의 칩들을 모드세팅에 의해 다양한 테스트를 수행할 수 있어서, 테스트 과정에서 테스트 효율을 향상시킬 수 있다.

도면도

도 2

명세서

도면의 간단한 설명

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도.

도 2는 도 1의 내부 메모리 칩의 회로 블록도.

도 3은 도 2의 반도체 메모리 칩의 모드세팅회로의 일예를 나타낸 도면.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸 도면.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도.

* 도면의 주요 부분에 대한 간단한 부호설명 *

100 : 메모리 모듈 110 : 회로기판

120 : 인터페이스부 130 : 메모리 칩, SDRAM

140 : 인식부, EEPROM 206 : 모드 레지스터

207 : 모드 세팅회로 MRD : 모드 세팅 디코더

FS1, FS2 : 퓨징회로부 NC : 정상 동작 회로부

TC : 테스트 동작 회로부

발명의 상세한 설명

발명의 목적

발명이 속하는 기술 및 그 분야의 종래기술

본 발명은 동작마진 테스트가 가능한 반도체 메모리 모듈 및 테스트 방법과 반도체 메모리 장치에 관한 것으로서, 특히 테스트 동작시 모드 세팅을 프로그램할 수 있도록 함으로써 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 테스트 방법에 관한 것이다.

컴퓨터 시스템의 중앙처리장치의 성능 향상과 더불어 많은 양의 데이터를 고속으로 처리하기 위하여 고속 동작의 대용량 메인 메모리들이 사용되고 있다. 특히 퍼스널 컴퓨터 시스템의 메인 메모리로는 DDR(Double Data Rate) 또는 램버스 디램 칩들을 하나의 패키지로 구성한 메모리 모듈이 상품화되어 제공되고 있다.

이러한 메모리 모듈은 복수의 단위 메모리 칩들을 회로기판 상에 구성하고 구성된 모듈을 마더보드에 장착하여 시스템에 연결한다.

컴퓨터 시스템에서는 시스템 부팅 동작을 고속으로 하기 위하여 메모리 모듈을 초기화하기 위한 초기화 정보를 메모리 모듈 내부에 저장하도록 요구하고 있다.

컴퓨터 시스템이 부팅을 할 때 제대로 작동하기 위해서는 메모리 모듈의 구성형태를 인식할 수 있어야 한다. PPD(Parallel Presence Detect - 병렬 구성 인식장치)는 필요로 하는 정보를 연결시키기 위해 레지스터를 사용하는 일반적인 방법으로 주로 SIMM(Single-In-Line Memory Module)방식의 모듈에서 사용하고, SPD(Serial Presence Detect - 직렬 구성 인식장치)란 DIMM(Dual-In-Line Memory Module)방식의 모듈에서 사용하는 방식으로 모듈에 관한 정보 저장 장치 EEPROM을 이용하는 것이다.

이와 같은 메모리 모듈의 테스트 범위는 단위 메모리 칩의 구성에 따라 제한된다. 통상적으로 동기형 DRAM의 경우 칩 내부에 모드 레지스터를 구비하고 테스트 모드로 세팅하도록 구성되어 있다. 즉, 단위 칩에서 세팅은 단순히 칩을 테스트 모드로 세팅할 것인지 아니면 노말 모드로 할 것인지를 선택하는 정도의 모드 세팅만 주어진 상태이다.

그러나, 이러한 단위 칩들을 모듈로 구성할 경우 복수의 칩들 간의 데이터 입출력 동작 마진이 서로 차이가 있을 수 있으며, 실장환경이나 모듈에 따라 미세한 동작 파라미터들의 차이가 형성될 우려가 있었다. 그러므로 모듈 실장 후에 이들 파라미터들을 측정하여 모듈 전체의 가장 적합한 마진을 찾아서 모듈 내부의 각 메모리 칩들을 세팅하지 않으면 안되었다. 즉 처음 모듈 생산시에 가장 적당한 마진이 어느 것인지 알 수 없으므로 다양한 동작 마진을 가진 테스트용 샘플 모듈들을 제작한 다음에 실장된 상태에서 테스트하여 최적의 마진을 찾아내는 과정이 요구되었다.

그러나, 각 개별적인 메모리 칩들에는 테스트 모드시 파라미터 값들을 변경하면서 동작 마진을 테스트하기 위한 기능이 없으므로 각 변경값들 마다 각각 별도의 테스트용 모듈을 마련하여 테스트하여야 하기 때문에 많은 비용과 시간이 소요되었다.

이와 같은 작업과정은 시간과 비용을 증가시키므로 모듈 생산 코스트를 상승시킨다.

발명이 이루고자 하는 기술적 과제

본 발명의 목적은 이와 같은 종래 기술의 문제점을 해결하기 위하여 복수의 메모리 칩들 사이의 최적 동작마진을 테스트할 수 있는 반도체 메모리 모듈 및 그 테스트 방법을 제공하는 데 있다.

본 발명의 다른 목적은 복수의 동작마진 테스트를 프로그램할 수 있는 반도체 메모리 장치를 제공하는 데 있다.

발명의 구성 및 작용

상기 목적을 달성하기 위하여 본 발명의 메모리 모듈은 복수의 외부 입출력단자들을 가지는 회로기판과, 회로기판 상에 설치된 인터페이스 회로, 복수의 반도체 메모리 칩들 및 인식부를 포함한다.

인터페이스부는 메모리 칩들과 입출력단자 사이의 신호전송을 인터페이스 한다. 인터페이스부는 타이밍 레지스터를 포함한다. 각 반도체 메모리 칩들은 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작회

로부에 제공하고, 테스트 모드에서는 모드선택 제어신호를 테스트동작회로부에 제공한다. 여기서 반도체 메모리 칩들은 각각 DDR SDRAM 또는 랩메스 디램으로 구성될 수 있다. 인자부는 시스템 초기 부팅시에 상기 인티페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한다. 여기서 인자부는 직접 입출력방식 및 EEPROM으로 구성한다.

본 발명의 목적을 달성하기 위한 본 발명의 테스트 방법은 다음 단계들을 포함한다.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리더하는 단계;

c) 상기 리더된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 선택정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 선택정보에 응답하여 대응하는 테스트 모드로 선택하는 단계;

f) 상기 선택된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계; 및

g) 메모리 모듈에 제공되는 테스트 모드 선택정보를 변경하면서 상기 d 내지 f단계를 반복하여 최종 동작의 모드 선택정보를 검출하는 단계.

본 발명에서 테스트용 메모리 모듈은 전기적 특징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램 하는 단계를 더 포함한다.

상기 다른 목적을 달성하기 위하여 본 발명의 반도체 메모리 장치는 모드선택 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터와, 모드 레지스터에 저장된 모드선택 정보를 다코딩하여 모드 선택 제어신호를 발생하는 모드선택 디코더와, 정상모드에서는 상기 모드선택 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드선택 제어신호를 테스트동작회로부에 제공하기 위해 출력되는 출력회로부를 구비한다.

이하, 첨부한 도면을 참조하여 본 발명의 바람직한 실시예를 구체적으로 설명하고자 한다. 이 실시예는 이 기술에 속한 자들이 본 발명을 실시할 수 있게 충분히 상세하게 기술한다.

도 1은 본 발명에 의한 반도체 메모리 모듈의 구성도를 나타낸다.

도 1에서 본 발명의 메모리 모듈(100)은 회로기판(110) 상에 인티페이스부(120), 복수의 SDRAM(130), 인자부(140)를 설치하여서 된 것이다. 구체적인 예는 본 출원인이 2003년 8월에 공개한 DDR SDRAM Registered Module의 데이터 매뉴얼에 개시되어 있다. 회로기판(110)에는 데이터, 데이터 스트로브 신호, 어드레스 신호, 타이밍 신호, 전원 신호 등을 입출력하기 위한 184핀의 입출력단자들(112)이 형성된다.

인티페이스부(120)는 어드레스 및 타이밍 레지스터로 구성한다. 뱅크 어드레스 BA0~BA1, 어드레스 신호 A0~A12, 타이밍 신호를 CS0~CS1, RAS, CAS, CKE0, CKE1, WE 등을 입력하여 내부칩선택신호, 내부 뱅크 어드레스 신호, 내부 어드레스 신호, 내부 타이밍 신호 등을 발생한다.

SDRAM(130)은 메모리 용량에 따라 512M, 1G, 2G 등으로 구성할 수 있다.

인자부(140)는 EEPROM으로 구성하고 시리얼 클럭신호에 응답하여 시리얼 데이터를 입출력한다.

도 2는 도 1의 내부 메모리 칩의 회로 블록도를 나타낸다. 도 2에서 본 발명에 의한 SDRAM(Synchronous Dynamic Random Accesses Memory)(130)은 어드레스 레지스터(202), 타이밍 레지스터(204), 모드 레지스터(206), 모드 선택회로(207), 포우 디코더(208), 클럭 디코더(210), 메모리 제어레이(212), 데이터 입출력회로 및 데이터 입출력 레지스터(214), 데이터 출력회로(216), 데이터 스트로브 출력회로(218), DLL(220) 등을 포함한다.

어드레스 레지스터(202)는 뱅크 어드레스 신호 및 어드레스 신호(ADD) 등을 입력하여 비퍼링하여 타이밍 제어신호에 응답하여 포우 어드레스, 클럭 어드레스, 모드선택 어드레스 등을 제공한다.

타이밍 레지스터(204)는 CKE, CS, RAS, CAS, WE 등의 외부 타이밍 제어신호를 입력하여 비퍼링하여 내부 타이밍 제어신호를 생성한다.

모드 레지스터(206)는 타이밍 제어신호, 예컨대 모드 세트 키맨드에 응답하여 모드 세트 어드레스를 래치하여 모드 세트 정보를 저장한다.

모드 선택회로(207)는 모드 선택회로(TC)를 포함한다.

도 3을 참조하면, 모드세팅 디코더(MRD)는 MRS 커멘드(MRSCMD)신호와 모드세팅 어드레스 비트(Ai, Aj)를 G1 내지 G4의 게이트를 통하여 디코딩하여 4개의 모드세팅 제어신호(MRS1~MRS4)를 각각 출력한다.

제1 퓨즈회로(FS1) 및 제2 퓨즈회로(FS2)는 과도전류를 흘려서 퓨즈를 절단시킴으로써 '0' 또는 '1'의 상태에서 '1' 또는 '0'의 상태로 출력이 변환되는 통상적인 퓨즈회로로 구성한다.

정상적인 메모리 칩에서는 FS2는 모두 턴오프되고 FS1은 모두 턴온되어 MRS1~MRS4 신호가 정상동작회로에 인가되도록 퓨징된다. 따라서, 정상동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 정상동작회로가 프로그램된다.

테스트용 메모리 칩에서는 FS1은 모두 턴오프되고 FS2는 모두 턴온되도록 퓨징된다. 따라서, 테스트 동작시에는 외부에서 어드레스 비트 Ai, Aj 값을 변경하는 것에 모드세팅 제어신호(MRS1~MRS4)를 발생하고 그 중에 대응하는 모드세팅에 의해 테스트 동작회로가 프로그램된다.

도 4는 본 발명에 의한 모드 레지스터 세팅 코드 테이블의 일예를 나타낸다.

즉, 어드레스 비트 Ai, Aj값에 의해 4가지 테스트 모드의 설정이 가능하다. 도시한 바와 같이, 디램의 액세스 타임(tAC) 값을 +100ps, +200ps, -100ps, -200ps 등으로 동작마진을 조금씩 변경하면서 설정할 수 있도록 프로그램할 수 있다.

도 5는 도 1의 반도체 메모리 모듈의 테스트 동작을 설명하기 위한 흐름도를 나타낸다.

먼저 모듈 테스트 장비에 테스트용 메모리 모듈(TMM)을 장착한다(S10). 여기서 테스트용 메모리 모듈(TMM)은 상술한 테스트 모드 프로그램이 가능한 메모리 칩들로 구성된 메모리 모듈을 칭하며, 내부 칩들이 테스트모드로 퓨징된 모듈을 말한다.

테스트 장비에서 장착된 메모리 모듈에 SPD 리드명령을 전달하여 모듈의 인식부로부터 읽혀진 SPD 코드 값을 전송받아 장착된 메모리 모듈의 초기값 정보를 해석한다(S12).

해석된 초기값 정보에 따라 TMM을 초기화시킨다(S14).

이어서, 초기화된 TMM에 모드세트 어드레스 정보를 제공하고 MRS 커멘드를 내려서 제1테스트 모드로 모드세팅시킨다(S16).

이어서 주어진 테스트 패턴에 의해 메모리 모듈을 테스트하고, 테스트 결과를 분석한다(S18).

테스트 결과 분석에 의해 최적 동작마진이 아닐 경우에는 모드변경을 수행하여(S20) S16, S18 단계를 반복 수행한다.

상기 테스트에 의해 최적 동작마진이 검출되면 그 테스트 결과를 저장한다(S22).

예컨대 이와 같은 방식에 의해 메모리 칩의 액세스 타임을 초기치에서부터 +200ps로부터 -200ps로 4단계로 바꾸어가면서 최적의 액세스 타임을 세팅할 수 있게 된다.

실시예를 참조하여 설명하였지만, 해당 기술 분야의 숙련된 당업자는 하기의 특허 청구의 범위에 기재된 본 발명의 사상 및 영역으로부터 벗어나지 않는 범위 내에서 본 발명을 다양하게 수정 및 변경시킬 수 있음을 이해할 수 있을 것이다.

발명의 효과

상술한 바와 같이 본 발명에서는 메모리 모듈의 테스트시 동작마진을 조금씩 변경하면서 테스트 할 수 있으므로 하나의 테스트 메모리 모듈을 사용하여 최적의 동작마진을 손쉽게 검출할 수 있게 된다. 그러므로, 종래의 4개의 테스트 메모리 모듈을 하나의 테스트 모듈로 모두 테스트 할 수 있으므로 테스트 비용을 절감할 수 있고 테스트 작업 효율을 향상시킬 수 있다.

(67) 청구의 범위

청구항 1.

모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 저장하는 모드 레지스터;

상기 모드 레지스터에 연결되고, 상기 모드 레지스터에 저장된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하는 모드세팅 디코더;

정상모드에서는 상기 모드세팅 제어신호를 정상동작회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하기 위해 퓨징되는 퓨즈회로부를 구비한 것을 특징으로 하는 반도체 메모리 장치.

청구항 2.

복수의 외부 입출력단자들을 가지는 회로기판;

상기 회로기판 상에 설치되고, 상기 복수의 외부 입력단자들과 내부 회로 사이의 신호전송을 인터페이스 하기 위한 인터페이스 회로;

상기 회로기판 상에 설치되고, 상기 인터페이스 회로와 연결되고, 모드세팅 정보를 가진 외부 어드레스 신호를 입력하여 입력된 모드세팅정보를 디코딩하여 모드세팅 제어신호를 발생하고, 정상모드에서는 상기 모드세팅 제어신호를 정상동작 회로부에 제공하고, 테스트 모드에서는 상기 모드세팅 제어신호를 테스트동작회로부에 제공하는 복수의 반도체 메모리 칩들; 및

상기 회로기판 상에 설치되고, 시스템 초기 부팅시에 상기 인터페이스 회로를 통하여 외부로 상기 반도체 메모리 칩들의 초기값을 제공하기 위하여 상기 초기값을 저장한 인식부를 구비한 것을 특징으로 하는 메모리 모듈.

청구항 3.

a) 메모리 테스트 장비에 테스트용 메모리 모듈을 장착하는 단계;

b) 상기 장착된 테스트용 메모리 모듈로부터 초기값 정보를 리드하는 단계;

c) 상기 리드된 초기값 정보에 응답하여 상기 테스트용 메모리 모듈을 초기화 하는 단계;

d) 상기 초기화된 테스트용 메모리 모듈에 테스트 모드 세팅정보를 제공하는 단계;

e) 상기 메모리 모듈 내부에 탑재된 복수의 메모리 칩들을 제공된 테스트 모드 세팅정보에 응답하여 대응하는 테스트 모드로 세팅하는 단계;

f) 상기 세팅된 테스트 모드로 상기 메모리 모듈을 테스트 하는 단계;

g) 메모리 모듈에 제공되는 테스트 모드 세팅정보를 변경하면서 상기 d 내지 f단계를 반복하여 최적 동작의 모드 세팅정보를 검출하는 단계를 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

청구항 4.

제3항에 있어서, 상기 테스트용 메모리 모듈은 퓨징에 의해 내부에 탑재된 복수의 메모리 칩들을 테스트 모드로 프로그램하는 단계를 더 포함하는 것을 특징으로 하는 반도체 메모리 모듈 테스트 방법.

도면

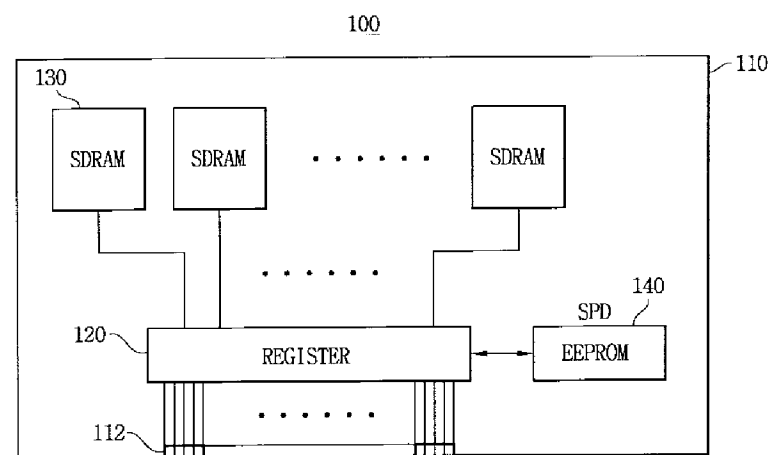
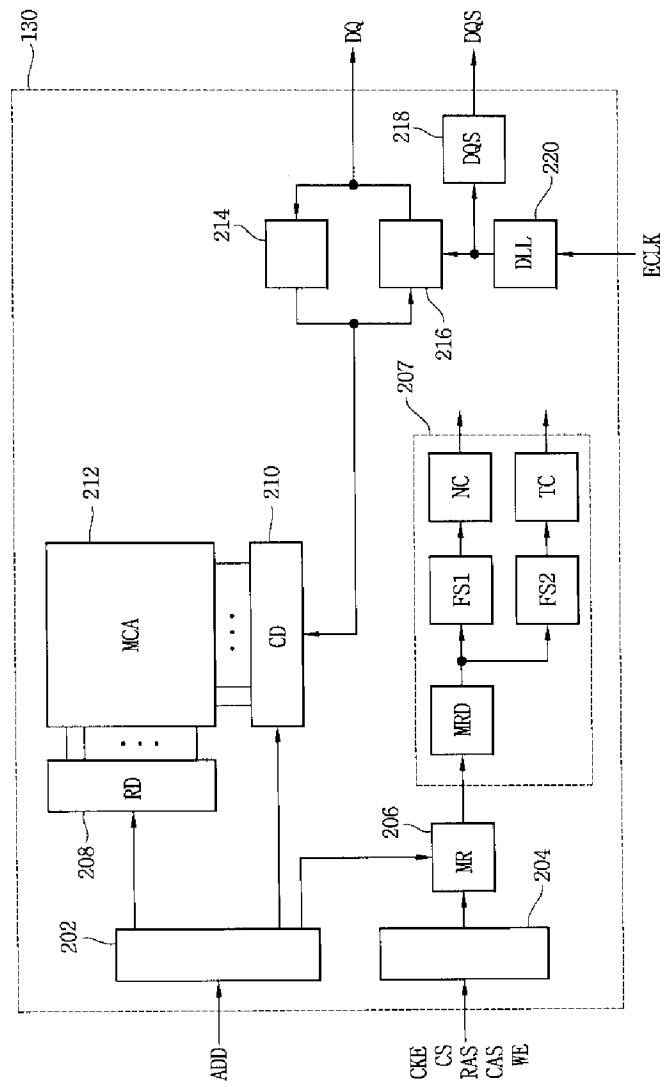
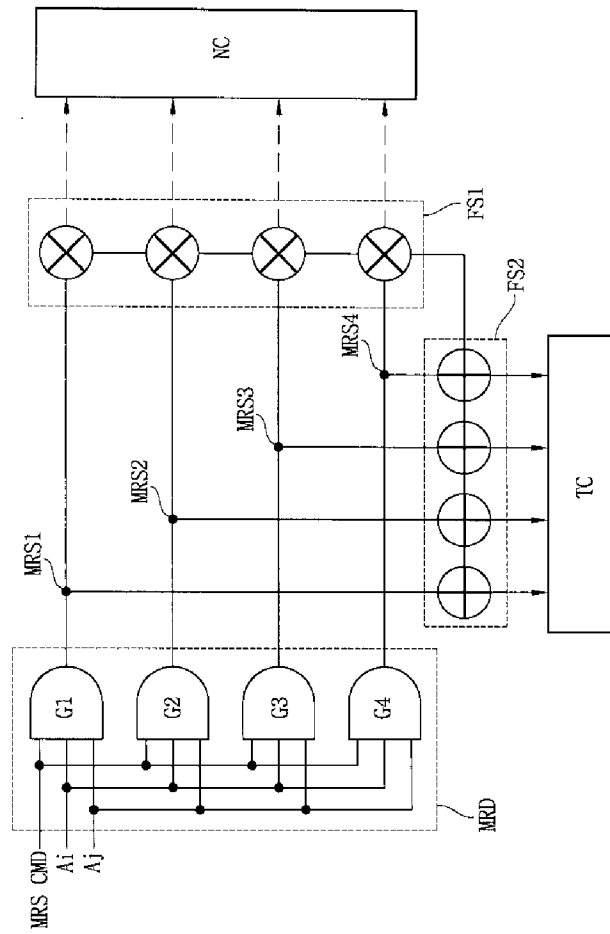


FIG. 1

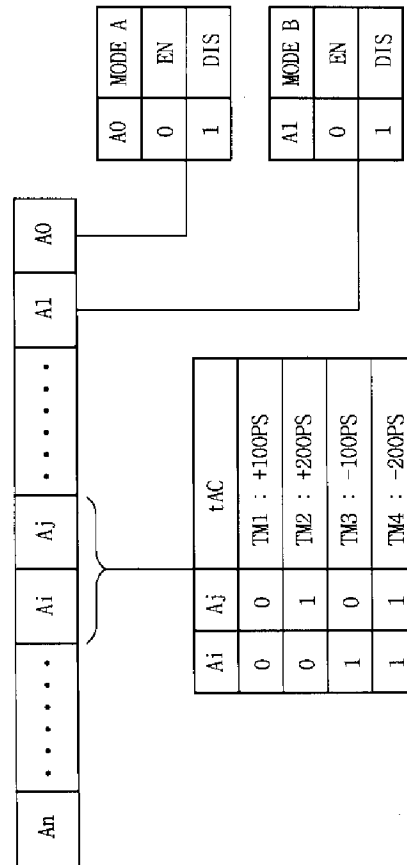
도면 2



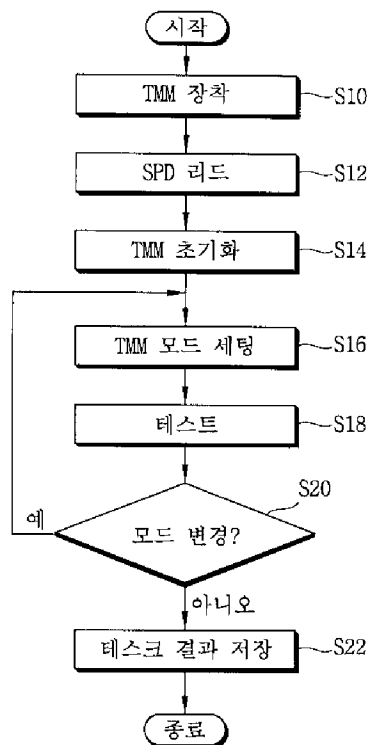
도면 3



도면 4



도면 5





ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
05/28/2024 04:28:40 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 65697055

AUTHORIZED BY Khaled Shami

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE
ADDRESS -

FIRST NAMED
INVENTOR Chi-She Chen

Payment Information

PAYMENT METHOD
DA / 220585

PAYMENT TRANSACTION ID
E20245RG30167823

PAYMENT AUTHORIZED BY
LISA MARGARET ELLIOTT

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1820	REQUEST FOR CONTINUED EXAMINATION (RCE)- 2ND AND SUBSEQUENT REQUEST (SEE 37 CFR 1.114)	2000.00	1	2000.00
TOTAL AMOUNT:				\$2,000.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

Samsung Electronics Co., Ltd.
Ex. 1002, p. 563

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

Application Number	17/582,797	Filing Date	2022-01-24	Docket Number (if applicable)	022955-000090	Art Unit	2138
First Named Inventor	Chi-She Chen			Examiner Name	Hashem Farrokh		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

☐ Other _____

☒ Enclosed

☒ Amendment/Reply

☒ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☐ Other _____

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to
Deposit Account No 220585

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop RCE

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

RESPONSE AFTER NOTICE OF ALLOWANCE

Commissioner:

In response to the Notice of Allowance issued February 28, 2024, Applicant submits the following:

Remarks begin on page 3.

Applicant does not believe that extensions of time are required beyond those provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 22-0585.

REMARKS

The Notice of Allowance mailed February 28, 2024, has been carefully considered. The following remarks and accompanying Information Disclosure Statements are being submitted with a Request for Continued Examination.

Interview Record

Applicants gratefully acknowledge the courtesy extended to the undersigned representative during the Examiner interview conducted on May 22, 2024 between Michael Stojavljevic and Examiner Hashem Farrokh. The substance of the interview related to previously submitted Information Disclosure Statements (IDS) and listing that were not considered, as discussed below. Specifically, two IDS listings and accompanying documents were proposed, the documents having the IDS listings inserted as headers. Accordingly, it was agreed that the header (e.g., titles) provided to the documents corresponding to IDS listings would enable identification and ensure consideration.

Notice of Prior and Concurrent Proceedings

Applicant hereby calls to the attention of the Patent and Trademark Office the following proceedings involving patents that are in the family of the above-identified patent application:

Proceeding	Status
<i>Micron Technology, Inc.; Micron Semiconductor Products, Inc.; and Micron Technology Texas LLC v. Netlist, Inc.</i> , Case No. IPR2022-00418 (P.T.A.B.), filed January 14, 2022	Final Written Decision - Determining All Challenged Claims Unpatentable entered August 28, 2023
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00615 (P.T.A.B.), filed February 17, 2022	Pending Director Review Responsive to Request Email entered May 20, 2023, following Judgment Final Written Decision – Determining All Challenged Claims Unpatentable entered April 17, 2024
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00996 (P.T.A.B.), filed May 17, 2022	Final Written Decision – Determining All Challenged Claims Unpatentable entered December 6, 2023

Proceeding	Status
<i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , Case No. IPR2022-00999 (P.T.A.B.), filed May 17, 2022	Final Written Decision – Determining All Challenged Claims Unpatentable entered December 5, 2023
2:21-cv-00463-JRG (EDTX Case asserting ‘918 and ‘054 against Samsung)	Closed - Termination Date August 11, 2023
2:22-cv-00203-JRG (EDTX Case asserting ‘918 and ‘054 against Micron)	Open - Filing Date June 10, 2022
1:22-cv-00134-DII (WDTX Case asserting the ‘833 against Micron)	Open - Filing Date April 28, 2021

Information Disclosure Statement

Listed on accompanying three IDS Forms PTO/SB/08a are documents that may be considered material to the patentability of this application as defined in 37 C.F.R. §1.56, and in compliance with the duty of disclosure requirements of 37 C.F.R. §§ 1.97 and 1.98.

Applicant has listed publication dates on the attached IDS Forms based on information presently available to the undersigned. However, the listed publication dates should not be construed as an admission that the information was actually published on the date indicated.

Applicant reserves the right to establish the patentability of the claimed invention over any of the information provided herewith, and/or to prove that this information may not be prior art, and/or to prove that this information may not be enabling for the teachings purportedly offered.

This statement should not be construed as a representation that a search has been made, or that information more material to the examination of the present patent application does not exist. The Examiner is specifically requested not to rely solely on the material submitted herewith.

Filing under 37 C.F.R. § 1.97(b). Due to the Request for Continued Examination (RCE) filed concurrently, this Information Disclosure Statement is being filed before the mailing date of a first Office Action on the merits. No statement or fee is required.

Copies of documents **NPL 1-50** and **NPL 1-36** (as listed on two PTO/SB/08a forms) are submitted. NPL 1-50 and NPL 1-36 were previously submitted, but not considered. The Notice of Allowance dated November 8, 2023 at page 2 states that these IDS listings and the above Notice of Prior and Concurrent Proceedings were not considered because the “title of actual documents were not readily identifiable and/or are different from IDS list. For example, in the IDS listing

many documents include an Exhibit number, which are not included in the actual documents.” Accordingly, the documents are being submitted again with proper headings that reflect the listing and exhibit numbers provided in the corresponding IDS listing. Moreover, a third IDS (as listed on a third PTO/SB/08a form) is being submitted in a similar manner with documents not previously submitted. Specifically, the third IDS lists six NPL documents and 16 patent publications. However, in accordance with 37 C.F.R. § 1.98(a)(2)(ii), no copies of U.S. patents and patent application publications are submitted.

It is expected that the examiner will review the prosecution and cited art in the parent application no(s). 17/328,019, filed 05-24-2021 (now U.S. Pat. No. 11,232,054), 17/138,766, filed 12-30-2020 (now U.S. Pat. No. 11,016,918), 15/934,416, filed 03-23-2018 (now abandoned), 14/840,865, filed 08-31-2015 (now U.S. Pat. No. 9,928,186); 14/489,269, filed 09-17-2014 (now U.S. Pat. No. 9,158,685); 13/559,476, filed 07-26-2012 (now U.S. Pat. No. 8,874,831); 12/240,916, filed 09-29-2008 (now U.S. Pat. No. 8,301,833); and 12/131,873, filed 06-02-2008 (now abandoned) in accordance with MPEP 2001.06(b), and indicate in the next communication from the office that the art cited in the earlier prosecution history has been reviewed in connection with the present application.

It is respectfully requested that the Examiner initial and return a copy of the enclosed two IDS Forms, and indicate in the official file wrapper of this patent application that the documents have been considered.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

Date: May 28, 2024
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5563839	A	1996-10-08	HERDT et al.	
	2	6067241	A	2000-05-23	LU	
	3	6693840	B2	2004-02-17	SHIMADA et al.	
	4	6798709	B2	2004-09-28	SIM et al.	
	5	6856556	B1	2005-02-15	HAJECK	
	6	7023187	B2	2006-04-04	SHEARON et al.	
	7	7061214	B2	2006-06-13	MAYEGA et al.	
	8	7692938	B2	2010-04-06	PETTER	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

9	7719866	B2	2010-05-18	BOLDO	
10	7721130	B2	2010-05-18	PRETE et al.	
11	7724604	B2	2010-05-25	AMIDI et al.	
12	10672458	B1	2020-06-02	SHAEFFER et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

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U.S.PATENT APPLICATION PUBLICATIONS

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20060080515	A1	2006-04-13	SPIERS et al.	
	2	20060174140	A1	2006-08-03	HARRIS et al.	
	3	20070136523	A1	2007-06-14	BONELLA et al.	
	4	20080101147	A1	2008-05-01	AMIDI	
	5	20080238536	A1	2008-10-02	HAYASHI et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

6	20090034354	A1	2009-02-05	RESNICK	
7	20100205470	A1	2010-08-12	MOSHAYEDI et al.	
8	20100257304	A1	2010-10-07	RAJAN et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. [Add](#)

FOREIGN PATENT DOCUMENTS

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Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ²	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							☐

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NON-PATENT LITERATURE DOCUMENTS

[Remove](#)

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Transcript, Day 2 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 17, 2023, 375 pages.	☐
	2	Transcript, Day 4 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 19, 2023, 338 pages.	☐
	3	Exhibit 1003, IPR 2022-00999, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,232,054, 431 pages, executed on May 16, 2022.	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

4	Exhibit 1014, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014, 69 pages.	☐
5	Exhibit 1015, IPR 2014-00994, Decision - Denying Institution of Inter Partes Review, issued December 16, 2014, 16 pages.	☐
6	Exhibit 1016, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22, 2014, 67 pages.	☐
7	Exhibit 1017, IPR 2014-01370, Decision - Denying Institution of Inter Partes Review, issued March 13, 2015, 19 pages.	☐
8	Exhibit 1018, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 13, 2017, 70 pages.	☐
9	Exhibit 1019, IPR 2017-00649, Decision - Denying Institution of Inter Partes Review, issued July 24, 2017, 17 pages.	☐
10	Exhibit 1020, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017, 78 pages.	☐
11	Exhibit 1021, IPR 2017-00692, Final Written Decision, issued July 5, 2018, 42 pages.	☐
12	Exhibit 1022, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 14, 2022, 76 pages.	☐
13	Exhibit 1026, JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2B (Revision of JESD7-2A), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, January 2005, 113 pages.	☐
14	Exhibit 1027, JEDEC STANDARD, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 190 pages.	☐

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Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

15	Exhibit 1028, JEDEC STANDARD, FBDIMM Specification: DDR2 SDRAM Fully Buffered, DIMM (FBDIMM) Design Specification, JESD205, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 129 pages.	☐
16	Exhibit 1031, PCI Local Bus Specification, Revision 2.2, December 18, 1998, 322 pages.	☐
17	Exhibit 1032, Power Electronics: Converters, Applications, and Design, Second Edition, copyright 1995 by John Wiley & Sons, Inc., 37 pages.	☐
18	Exhibit 1040, Texas Instruments, TPS51020, Dual, Voltage Mode, DDR Selectable, Synchronous, Step-Down Controller for Notebook System Power, SLUS564B, July 2003 (revised December 2003), 27 pages.	☐
19	Exhibit 1041, Fairchild Semiconductor, FAN5026, Dual DDR/Dual-Output PWM Controller, October 2005, 17 pages.	☐
20	Exhibit 1042, Murata Manufacturing Co., Ltd, Power Supply Reference Guide for XILINX FPGAs, September 2006, 33 pages.	☐
21	Exhibit 1043, Murata Products, Power Supply Reference Guide for ALTERA FPGAs, Catalog No. DC-03-A, 2008, 40 pages.	☐
22	Exhibit 1045, JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, June 2000, 77 pages.	☐
23	Exhibit 1046, JEDEC STANDARD, DDR3 SDRAM Specification, JESD79-3A (Revision of JESD79-3), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, September 2007, 189 pages.	☐
24	Exhibit 1048, Murata Manufacturing, DC-DC Converter Specification(DRAFT), MPD4S014S, January 21, 2008, 11 pages.	☐
25	Exhibit 1049, Micron, NAND Flash Memory, MT29F2G08AABWP/MT29F2G16AABWP, MT29F4G08BABWP/MT29F4G16BABWP, MT29F8G08FABWP, copyright 2004 by Micron Technology, Inc., 57 pages.	☐

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26	Exhibit 1058, LENK, Simplified Design of Switching Power Supplies, Linear Technology, EDN Series for Design Engineers, copyright 1995 by Butterworth-Heinemann, 9 pages.	☐
27	Exhibit 1061, Analog Devices, Super Sequencer with Margining Control and Auxiliary ADC Inputs, ADM1066, copyright 2006 by Analog Devices, Inc., 36 pages.	☐
28	Exhibit 1062, Analog Devices, Analog Dialogue, Volume 40, Number 2, 2006, 24 pages.	☐
29	Exhibit 1063, National Semiconductor, LMC6953, PCI Local Bus Supervisor, October 1996, 12 pages.	☐
30	Exhibit 1067, Lattice Semiconductor Corporation, LatticeXP Family Data Sheet, Version 04.2, March 2006, 127 pages.	☐
31	Exhibit 1068, Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed October 15, 2021, 82 pages.	☐
32	Exhibit 1069, First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed January 18, 2022, 122 pages.	☐
33	Exhibit 1071, Complaint, filed December 20, 2021, 49 pages.	☐
34	Exhibit 1072, The Samsung Defendants' Answer, filed April 12, 2022, 37 pages.	☐
35	Exhibit 1073, First Amended Complaint, filed May 3, 2022, 71 pages.	☐
36	Exhibit 1075, IPR 2022-00999, Deposition of William Mangione-Smith, Ph.D. regarding US Patent No. 11,232,054, 245 pages, dated June 12, 2023.	☐

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37	Exhibit 1076, IPR 2022-00999, redline comparing Declarations - Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,232,054, 165 pages, executed on March 29, 2022.	☐
38	Exhibit 1077, Netlist, Technology Tutorial: In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same, Inv No. 337-TA-1023, May 8, 2017, 11 pages.	☐
39	Exhibit 1078, Analog Devices, Step-Down DC-to-DC Controller, ADP1821, copyright 2005-2007 by Analog Devices, Inc., 24 pages.	☐
40	Exhibit 2001, IPR 2022-00999, Declaration of Dr. Sunil P. Khatri regarding US Patent No. 11,232,054, 68 pages, executed on September 8, 2022.	☐
41	Exhibit 2003, BELLONI et al., 24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current, ISSCC 2008 / Session 24 / Analog Power Techniques / 24.6, 2008 IEEE International Solid-State Circuits Conference, 3 pages.	☐
42	Exhibit 2004, MA et al., Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode, IEEE Journal of Solid-State Circuits, Volume 38, Number 1, January 2003, pages 89-100 (12 pages).	☐
43	Exhibit 2006, Micron, Technical Note: Power Solutions for DDR2 Notebook PCs, TN-47-05 DDR2 Power Solutions for Notebooks, copyright 2004 by Micron Technology, Inc., 16 pages.	☐
44	Exhibit 2007, Texas Instruments, LP2996-N, LP2996A DDR Termination Regulator, SNOSA40K, November 2002 (revised December 2016), 39 pages.	☐
45	Exhibit 2008, JAMECO ELECTRONICS, Jameco Part Number 843868, National Semiconductor: LP2996: DDR Termination Regulator, June 2006, 19 pages.	☐
46	Exhibit 2009, JAMECO ELECTRONICS, Jameco Part Number 843930, National Semiconductor: LP2997: DDR-II Termination Regulator, June 2006, 13 pages.	☐
47	Exhibit 2010, National Semiconductor: LP2998: DDR-II and DDR-I Termination Regulator, December 12, 2007, 18 pages.	☐

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48	Exhibit 2011, BERGVELD, Battery Management Systems: Design by Modelling, copyright 2001 by Royal Philips Electronics N.V., 328 pages.	☐
49	Exhibit 2012, ROMO, DDR Memories: Comparison and Overview, NXP, pages 70-73 (4 pages), September 21, 2007.	☐
50	Exhibit 2013, JEDEC Standard No. 21-C, Page 4.20.3-1; PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, 26 pages. downloaded August 16, 2022.	☐

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
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Attorney Docket Number	022955-000090

1	Exhibit 2014, Qimonda, Internet Data Sheet, Rev. 1.25, June 2007, 24 pages.	☐
2	Exhibit 2015, Siemens, 3.3V 2M x 64/72-Bit 1 BANK SDRAM Module, HYS64/72V2200GU-8/-10, 3.3V 4M x 64/72-Bit 2 BANK SDRAM Module, HYS64/72V4200GU-8/-10, 168 pin unbuffered DIMM Modules, downloaded from www.datasheetcatalog.com; 1998, 18 pages	☐
3	Exhibit 2016, PCI Bus Variation - Technology Note, copyright 2006 by Euresys, 9 pages.	☐
4	Exhibit 2017, Qimonda, Internet Data Sheet, Rev. 1.42, September 2007, 27 pages.	☐
5	Exhibit 2018, Transcend, Product Support, What is the difference between SDRAM, DDR1, DDR2, DDR3 and DDR4?, available online at https://www.transcend-info.com/support/faq-296#:~:text=DDR3's prefetch buffer width is,according to the temperature variation , downloaded August 24, 2022, 2 pages.	☐
6	Exhibit 2021, Texas Instruments: Application Report, Low Dropout Operation in a Buck Converter, SLUA928A - December 2018 - revised March 2019, 18 pages.	☐
7	Exhibit 2022, Electronic Design, Simple Soft-Start Circuitry Provides Long Startup Times, available online at http://electronicdesign.com/power/simple-soft-start-circuitry-provides-long-startup-times , published June 22, 1998, 3 pages.	☐
8	Exhibit 2024, SCHMID, Understanding Hard Drive Performance, available online at https://www.tomshardware.com/reviews/understanding-hard-drive-performance,1557-5.html , downloaded August 15, 2022, published March 5, 2007, 17 pages.	☐
9	Exhibit 2025, Micron, SDR SDRAM, MT48LC64M4A2 - 16 Meg x 4 x 4 Banks, MT48LC32M8A2 - 8 Meg x 8 x 4 Banks, MT48LC16M16A2 - 4 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 94 pages.	☐
10	Exhibit 2026, Micron, SDR SDRAM, MT48LC16M4A2 - 4 Meg x 4 x 4 Banks, MT48LC8M8A2 - 2 Meg x 8 x 4 Banks, MT48LC4M16A2 - 1 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 84 pages.	☐
11	Exhibit 2027, Transcend, DDR2 SO-DIMM, copyright 2012 by Transcend, 3 pages.	☐

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12	Exhibit 2028, Micron Technical Note: DDR3 Point-to-Point Design Support, copyright 2013 by Micron Technology, Inc., 27 pages.	☐
13	Exhibit 2030, IPR 2022-00996 and IPR 2022-00999, Videoconference Deposition of Andrew Wolfe, Ph.D. regarding US Patent Nos. 11,016,918 and 11,232,054, 311 pages, dated March 16, 2023.	☐
14	Exhibit 2031, IPR 2022-00996, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,016,918, 452 pages, executed on May 16, 2022.	☐
15	Exhibit 2031, IPR 2022-00996, Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,016,918, 144 pages, executed on March 28, 2023.	☐
16	Exhibit 2032, Claim Construction Order, filed December 14, 2022, 35 pages.	☐
17	Exhibit 2033, Defendants' Objections to Claim Construction Memorandum Order, filed December 29, 2022, 11 pages.	☐
18	Exhibit 2043, Samsung Unveils New Power Management Solutions for DDR5 Modules, May 18, 2021, 6 pages.	☐
19	Exhibit 2044, Micron, DDR2 SDRAM RDIMM, MT9HTF3272Y - 256MB, MT9HTF6472PY - 512MB, MT9HTF12872PY - 1GB, copyright 2003 by Micron Technology, Inc., 23 pages.	☐
20	Exhibit 2046, JEDEC Standard No. 21C, Page 4.20.11-1, PC2-6400/PC2-5300/PC2-4200/PC2-3200, DDR2 Unbuffered SO-DIMM, Reference Design Specification, Revision 2.5, July 2008, 60 pages.	☐
21	Exhibit 2048, Micron, DDR2 SDRAM FBDIMM, MT18HTF12872FD - 1GB, MT18HTF25672FD - 2GB, copyright 2005 by Micron Technology, Inc., 39 pages.	☐
22	Exhibit 2056, IPR 2022-00615, Remote Videotaped Deposition by Virtual Zoom of Andrew Wolfe, Ph.D. regarding US Patent No. 7,619,912, 297 pages, dated January 4, 2023.	☐

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23	Exhibit 2057, Micron Technical Brief: Micron DDR5: Key Module Features, DDR4 vs. DDR5 DIMM, copyright 2020 by Micron Technology, Inc., 7 pages.	☐
24	Exhibit 2063, Netlist, Demonstrative Exhibit for IPR 2022-00996 and IPR 2022-00999, filed September 6, 2023, 180 pages.	☐
25	Exhibit 2102, LEE et al., PCI Express Power and Mini Card Solutions - Design Note 346, Linear Technology - Design Notes, copyright 2004 by Linear Technology Corporation, 2 pages.	☐
26	Paper 1, IPR 2022-00996, Petition for Inter Partes Review of US Patent No. 11,016,918, filed May 17, 2022, 151 pages.	☐
27	Paper 1, IPR 2022-00999, Petition for Inter Partes Review of US Patent No. 11,232,054, filed May 17, 2022, 149 pages.	☐
28	Paper 7, IPR 2022-00996, Patent Owner Preliminary Response, filed September 9, 2022, 85 pages.	☐
29	Paper 7, IPR 2022-00999, Patent Owner Preliminary Response, filed September 8, 2022, 82 pages.	☐
30	Paper 10, IPR 2022-00996, Decision - Granting Institution of Inter Partes Review, dated December 7, 2022, 56 pages.	☐
31	Paper 21, IPR 2022-00996, Patent Owner Response, filed March 28, 2023, 91 pages.	☐
32	Paper 22, IPR 2022-00999, Patent Owner Response, filed March 28, 2023, 90 pages.	☐
33	Paper 25, IPR 2022-00996, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐

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34	Paper 26, IPR 2022-00999, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐
35	Paper 31, IPR 2022-00996, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐
36	Paper 33, IPR 2022-00999, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐

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SIGNATURE

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

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ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
05/28/2024 04:31:47 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 65669799

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 100

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4-NPL-- Ex_2017_Qimonda_256- MBit_Synchronous_DRAM_S D.pdf	27	Non Patent Literature	583 KB
6-NPL-- Ex_2021_Low_Dropout_Oper ation_Buck_Converter.pdf	18	Non Patent Literature	700 KB
2-NPL-- Ex_2015_Siemens_168_Pin_ Unbuffered_DIMM_Module.p df	18	Non Patent Literature	785 KB
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Digest

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16-NPL-- Ex_2032_CC_Order.pdf	D1D99DAB042C199720DD40F456BD2069E345B16559F7E1047 97B53027BBEB72AEFD76F068AF2CE82B2DC211D6DBE82069 8148F77527FD3B371476DAB273FEF50
18-NPL-- Ex_2043_Sams_Unveils_New_Power_Mgmt_DDR5_Mod.pdf	30A44AD7D4F9928F11EEFD345427059FC5FDA84F4C608B555 DF17B7818D54E74AA2D63D0162E8C7323E8000A4FE06394CA 466FB94EAF58F37A8FE3D06D6DF483
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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR SUSPENSION OF ACTION

Commissioner:

In connection with the Request for Continuation of Examination (RCE) filed May 28, 2024, Applicant hereby requests a two (2) month suspension of action.

Applicant hereby authorizes to be charged the processing fee set forth in 37 CFR 1.17(i) to our Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

Date: May 29, 2024
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Customer No.: 151145
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745



UNITED STATES
PATENT AND TRADEMARK OFFICE

P.O. Box 1450
Alexandria, VA 22313 - 1450
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ELECTRONIC PAYMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
05/29/2024 09:02:35 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 65725464

AUTHORIZED BY Khaled Shami

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE
ADDRESS -

FIRST NAMED
INVENTOR Chi-She Chen

Payment Information

PAYMENT METHOD
DA / 220585

PAYMENT TRANSACTION ID
E20245SL03577505

PAYMENT AUTHORIZED BY
LISA MARGARET ELLIOTT

FEE CODE	DESCRIPTION	ITEM PRICE(\$)	QUANTITY	ITEM TOTAL(\$)
1830	PROCESSING FEE, EXCEPT IN PROVISIONAL APPLICATIONS	140.00	1	140.00
TOTAL AMOUNT:				\$140.00

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

Samsung Electronics Co., Ltd.
Ex. 1002, p. 611

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



ELECTRONIC ACKNOWLEDGEMENT RECEIPT

APPLICATION #
17/582,797

RECEIPT DATE / TIME
05/29/2024 09:02:35 PM Z ET

ATTORNEY DOCKET #
022955-000090

Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

Application Information

APPLICATION TYPE Utility - Nonprovisional Application
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 65725464

FILING DATE 01/24/2022

CUSTOMER # 151145

FIRST NAMED
INVENTOR Chi-She Chen

CORRESPONDENCE
ADDRESS -

AUTHORIZED BY Khaled Shami

Documents

TOTAL DOCUMENTS: 1

DOCUMENT	PAGES	DESCRIPTION	SIZE (KB)
022955-000090 Request for Suspension of Action.pdf	1	Letter Requesting Suspension of Action	103 KB

Digest

DOCUMENT	MESSAGE DIGEST(SHA-512)
022955-000090 Request for Suspension of Action.pdf	1A627646B89079663584265C3D10CCA55CB2B8DE1A32223F6 D9AA5507E7ECA997E86943A7BCD6FC68DB72B304CBE6E4E6 9BA1430071AEE0C2AA75488FE170484

by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

<i>Notice of References Cited</i>	Application/Control No. 17/582,797		Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH		Art Unit 2138	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Name	CPC Classification	US Classification
*	A	US-20120271990-A1	2012-10-25	Chen; Chi-She	G11C29/52	711/E12.008
*	B	US-20070136523-A1	2007-06-14	Bonella; Randy M.	G06F12/0866	711/E12.019
*	C	US-20080126624-A1	2008-05-29	Prete; Edoardo	G11C7/1006	710/53
*	D	US-20060174140-A1	2006-08-03	Harris; Shaun L.	G11C5/04	713/300
*	E	US-7724604-B2	2010-05-25	Amidi; Mike H.	G11C7/22	711/115
*	F	US-6856556-B1	2005-02-15	Hajeck; Michael J.	G11C16/30	365/189.11
*	G	US-20060080515-A1	2006-04-13	Spiers; John	G06F11/1456	714/14
	H					
	I					
	J					
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date YYYY-MM-DD	Country	Name	CPC Classification
	N					
	O					
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	Q					
	R					
	S					
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	JEDEC STANDARD, FBDIMM, Advanced Memory Buffer (AMB), JES82-20 JEDEC SOLID STATE TECHNOLOGY ASSOCIATION , March 2007, 190 pages
	V	JEDEC STANDARD, FBDIMM Specification, DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification,, JESD205, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 129 pages
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

CPC - Searched*		
Symbol	Date	Examiner
G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/ 205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00	10/06/2022	HF

CPC Combination Sets - Searched*		
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US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	10/06/2022	HF
711	110	11/01/2023	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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<i>Search Notes</i> 	Application/Control No. 17/582,797	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2138

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	10/06/2022	HF
EAST Text, CPC, FACET Search	10/06/2022	HF
IP Search	10/06/2022	HF
Google Search	10/06/2022	HF
Inventor/Assignee Search Updated	07/07/2023	HF
EAST Text, CPC, FACET Search Updated	07/07/2023	HF
Inventor/Assignee Search Updated	10/31/2023	HF
EAST Text, CPC, FACET Search Updated	10/31/2023	HF
Inventor/Assignee Search Updated	02/22/2024	HF
EAST Text, CPC, FACET Search Updated	02/22/2024	HF
Inventor/Assignee Search Updated	08/05/2024	
EAST Text, CPC, FACET Search Updated	08/05/2024	

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G06F3/0685	G06F3/00	11/01/2023	HF
G06F13/28	G06F13/00	11/01/2023	HF
G06F2212/205	G06F2212/00	11/01/2023	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17582797
	Filing Date		2022-01-24
	First Named Inventor	CHEN	
	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5563838	A	1996-10-08	MART et al.	
	2	6351827	B1	2002-02-26	CO et al.	
	3	6418065	B2	2002-07-09	SATO et al.	
	4	6434044	B1	2002-08-13	GONGWER et al.	
	5	7034569	B1	2006-04-25	BALASUBRAMANIAN et al.	
	6	7161820	B2	2007-01-09	FUNABA et al.	
	7	7166934	B2	2007-01-23	DEWEY	
	8	7269764	B2	2007-09-11	DART et al.	

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Application Number	17582797
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Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

9	7426649	B2	2008-09-16	BRITTAIN et al.	
10	7613880	B2	2009-11-03	MIURA	
11	7644216	B2	2010-01-05	FAHR et al.	
12	7656735	B2	2010-02-02	KAGAN et al.	

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	1	20090020608	A1	2009-01-22	BENNETT et al.	
	2	20090027844	A1	2009-01-29	CHEN et al.	

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	1	10-2005-0073902	KR	A	2005-07-18	SAMSUNG ELECTRONICS CO LTD	Machine Translation included as NPL 1	☒

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	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1	Machine Translation of KR 10-2005-0073902 A, published July 18, 2005, 7 pages.	☐
	2	RENESAS, ISL6537 ACPI Regulator/Controller for Dual Channel DDR Memory Systems Data Sheet, Rev 6.00, 16 pages, July 18, 2007.	☐
	3	Intersil, ISL6532B ACPI Regulator/Controller for Dual Channel DDR Memory Systems Data Sheet, 16 pages, July 2004.	☐
	4	Freescale Semiconductor, Hardware and Layout Design Considerations for DDR Memory Interfaces, Rev. 6, NXP, 48 pages, April 2007.	☐
	5	PLESSL and PLATZNER, TKDM - A Reconfigurable Co-processor in a PC's Memory Slot, Swiss Federal Institute of Technology, January 15, 2004, 8 pages.	☐
	6	RENESAS, ISL6534 Dual PWM with Linear Data Sheet, Rev 2.00, 29 pages, November 18, 2005.	☐
	7	Maxim Integrated, DC-DC Converter Tutorial, APP 2031, 14 pages, November 29, 2001.	☐

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Examiner Signature	/HASHEM FARROKH/	Date Considered	07/01/2024
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**INFORMATION DISCLOSURE
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(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

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PE2E SEARCH - Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	British Equivalents	Time Stamp
L92	51	("5563838" "6351827" "6418065" "6434044" "7034569" "7161820" "7166934" "7269764" "7426649" "7613880" "7644216" "7656735" "20090020608" "20090027844").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/01 01:19 PM
L93	2	92 AND (buck near5 (conver\$3 OR regulat\$3))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/01 01:25 PM
L94	16	("8301833").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/01 03:47 PM
L95	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/01 05:00 PM
L96	2	("8874831").pn.	(US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/02 09:00 AM
L97	2	("8874831").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2024/07/02 09:00 AM

			JPO; DERWENT; IBM_TDB)				
L99	2	("20060174140").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/02 02:16 PM
L100	10	("7724604" "20060080515" "6856556").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/02 02:24 PM
L101	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/03 10:03 AM
L102	4	("11232054").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/07/30 10:26 AM
L103	2	("20070136523").pn.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 01:59 PM
L104	532	periodic\$4 WITH (backup OR replicat\$3 OR cop\$4) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:30 PM
L105	2281	periodic\$4 WITH (backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:31 PM
L106	97	105 AND (trigger\$3 near5 signal)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:31 PM
L107	0	97 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:32 PM
L108	410	105 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:32 PM
L109	13	106 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 02:33 PM
L110	55	(backup OR replicat\$3 OR cop\$4 OR writ\$4	(US-PGPUB; USPAT; USOCR; FPRS; EPO;	OR	ON	ON	2024/08/02 04:48 PM

		OR sav\$3) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD)) WITH milli\$1second	JPO; DERWENT; IBM_TDB)				
L111	24	110 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:48 PM
L112	530	(backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3 OR stor\$2) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD)) WITH (every OR each) near5 (milli\$1second OR ms)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:51 PM
L113	143	112 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:52 PM
L114	71	(backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3 OR stor\$2) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD)) WITH (every OR each) ADJ (milli\$1second OR ms)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:53 PM
L115	14	114 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:54 PM
L116	6	(backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3 OR stor\$2) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD)) WITH (every OR each) ADJ (milli\$1second)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:55 PM
L117	0	116 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 04:55 PM
L118	0	periodic\$4 WITH (backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD))	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:09 PM

		WITH millisecond					
L119	145	periodic\$4 WITH (backup OR replicat\$3 OR cop\$4 OR writ\$4 OR sav\$3) WITH ((non\$volatile OR flash) near2 (memory OR storage OR SSD)) WITH second	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:09 PM
L120	26	119 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:09 PM
L121	0	120 AND dimm	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:19 PM
L122	19	"backup may occur every millisecond"	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:39 PM
L123	0	122 AND (@ad<"20070601")	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:39 PM
L124	19	(backup near5 occur near5 every near5 millisecond)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:40 PM
L125	19	(backup near5 occur near5 (every OR each OR one) near5 millisecond)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	ON	ON	2024/08/02 05:41 PM
L126	31	(buck ADJ converters) SAME (regulat\$3 near2 voltage) SAME ((printed ADJ circuit ADJ board) OR PCB)	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2024/08/05 08:32 AM
L127	3	((buck ADJ converters) SAME (regulat\$3 near2 voltage) SAME ((printed ADJ circuit ADJ board) OR PCB)).clm.	(US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)	OR	OFF	ON	2024/08/05 08:32 AM
L128	3	127 AND ("BHAKTA; JAYESH".ine. OR "CHEN; CHI-SHE".ine. OR "MILTON; SCOTT H.".ine. OR "SOLOMON; JEFFREY C.".ine.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/08/05 08:33 AM
L129	5	126 AND ("NETLIST, INC.".ase.)	(US-PGPUB; USPAT; USOCR; IBM_TDB)	OR	ON	ON	2024/08/05 08:34 AM
L130	6	126 AND ((G06F1/185	(US-PGPUB; USPAT;	OR	ON	ON	2024/08/05

		OR G06F12/0246 OR G06F12/0638 OR G06F13/1694 OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018 OR G11C16/10 OR G11C7/1072 OR Y02D10/00).cpc. OR (711/110).ccls. OR (G06F1/18 OR G06F12/02 OR G06F12/06 OR G06F13/16 OR G06F13/28 OR G06F13/40 OR G06F13/42 OR G06F3/06 OR G11C14/00 OR G11C7/10).ipc.)	USOCR; IBM_TDB)				08:35 AM
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PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

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	Filing Date		2022-01-24
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	Art Unit	2138	
	Examiner Name	FARROKH	
	Attorney Docket Number	022955-000090	

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Examiner Name	FARROKH
Attorney Docket Number	022955-000090

1	Exhibit 2014, Qimonda, Internet Data Sheet, Rev. 1.25, June 2007, 24 pages.	☐
2	Exhibit 2015, Siemens, 3.3V 2M x 64/72-Bit 1 BANK SDRAM Module, HYS64/72V2200GU-8/-10, 3.3V 4M x 64/72-Bit 2 BANK SDRAM Module, HYS64/72V4200GU-8/-10, 168 pin unbuffered DIMM Modules, downloaded from www.datasheetcatalog.com; 1998, 18 pages	☐
3	Exhibit 2016, PCI Bus Variation - Technology Note, copyright 2006 by Euresys, 9 pages.	☐
4	Exhibit 2017, Qimonda, Internet Data Sheet, Rev. 1.42, September 2007, 27 pages.	☐
5	Exhibit 2018, Transcend, Product Support, What is the difference between SDRAM, DDR1, DDR2, DDR3 and DDR4?, available online at https://www.transcend-info.com/support/faq-296#:~:text=DDR3's prefetch buffer width is,according to the temperature variation , downloaded August 24, 2022, 2 pages.	☐
6	Exhibit 2021, Texas Instruments: Application Report, Low Dropout Operation in a Buck Converter, SLUA928A - December 2018 - revised March 2019, 18 pages.	☐
7	Exhibit 2022, Electronic Design, Simple Soft-Start Circuitry Provides Long Startup Times, available online at http://electronicdesign.com/power/simple-soft-start-circuitry-provides-long-startup-times , published June 22, 1998, 3 pages.	☐
8	Exhibit 2024, SCHMID, Understanding Hard Drive Performance, available online at https://www.tomshardware.com/reviews/understanding-hard-drive-performance,1557-5.html , downloaded August 15, 2022, published March 5, 2007, 17 pages.	☐
9	Exhibit 2025, Micron, SDR SDRAM, MT48LC64M4A2 - 16 Meg x 4 x 4 Banks, MT48LC32M8A2 - 8 Meg x 8 x 4 Banks, MT48LC16M16A2 - 4 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 94 pages.	☐
10	Exhibit 2026, Micron, SDR SDRAM, MT48LC16M4A2 - 4 Meg x 4 x 4 Banks, MT48LC8M8A2 - 2 Meg x 8 x 4 Banks, MT48LC4M16A2 - 1 Meg x 16 x 4 Banks, copyright 1999 by Micron Technology, Inc., 84 pages.	☐
11	Exhibit 2027, Transcend, DDR2 SO-DIMM, copyright 2012 by Transcend, 3 pages.	☐

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12	Exhibit 2028, Micron Technical Note: DDR3 Point-to-Point Design Support, copyright 2013 by Micron Technology, Inc., 27 pages.	☐
13	Exhibit 2030, IPR 2022-00996 and IPR 2022-00999, Videoconference Deposition of Andrew Wolfe, Ph.D. regarding US Patent Nos. 11,016,918 and 11,232,054, 311 pages, dated March 16, 2023.	☐
14	Exhibit 2031, IPR 2022-00996, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,016,918, 452 pages, executed on May 16, 2022.	☐
15	Exhibit 2031, IPR 2022-00996, Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,016,918, 144 pages, executed on March 28, 2023.	☐
16	Exhibit 2032, Claim Construction Order, filed December 14, 2022, 35 pages.	☐
17	Exhibit 2033, Defendants' Objections to Claim Construction Memorandum Order, filed December 29, 2022, 11 pages.	☐
18	Exhibit 2043, Samsung Unveils New Power Management Solutions for DDR5 Modules, May 18, 2021, 6 pages.	☐
19	Exhibit 2044, Micron, DDR2 SDRAM RDIMM, MT9HTF3272Y - 256MB, MT9HTF6472PY - 512MB, MT9HTF12872PY - 1GB, copyright 2003 by Micron Technology, Inc., 23 pages.	☐
20	Exhibit 2046, JEDEC Standard No. 21C, Page 4.20.11-1, PC2-6400/PC2-5300/PC2-4200/PC2-3200, DDR2 Unbuffered SO-DIMM, Reference Design Specification, Revision 2.5, July 2008, 60 pages.	☐
21	Exhibit 2048, Micron, DDR2 SDRAM FBDIMM, MT18HTF12872FD - 1GB, MT18HTF25672FD - 2GB, copyright 2005 by Micron Technology, Inc., 39 pages.	☐
22	Exhibit 2056, IPR 2022-00615, Remote Videotaped Deposition by Virtual Zoom of Andrew Wolfe, Ph.D. regarding US Patent No. 7,619,912, 297 pages, dated January 4, 2023.	☐

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23	Exhibit 2057, Micron Technical Brief: Micron DDR5: Key Module Features, DDR4 vs. DDR5 DIMM, copyright 2020 by Micron Technology, Inc., 7 pages.	☐
24	Exhibit 2063, Netlist, Demonstrative Exhibit for IPR 2022-00996 and IPR 2022-00999, filed September 6, 2023, 180 pages.	☐
25	Exhibit 2102, LEE et al., PCI Express Power and Mini Card Solutions - Design Note 346, Linear Technology - Design Notes, copyright 2004 by Linear Technology Corporation, 2 pages.	☐
26	Paper 1, IPR 2022-00996, Petition for Inter Partes Review of US Patent No. 11,016,918, filed May 17, 2022, 151 pages.	☐
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28	Paper 7, IPR 2022-00996, Patent Owner Preliminary Response, filed September 9, 2022, 85 pages.	☐
29	Paper 7, IPR 2022-00999, Patent Owner Preliminary Response, filed September 8, 2022, 82 pages.	☐
30	Paper 10, IPR 2022-00996, Decision - Granting Institution of Inter Partes Review, dated December 7, 2022, 56 pages.	☐
31	Paper 21, IPR 2022-00996, Patent Owner Response, filed March 28, 2023, 91 pages.	☐
32	Paper 22, IPR 2022-00999, Patent Owner Response, filed March 28, 2023, 90 pages.	☐
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34	Paper 26, IPR 2022-00999, Petitioner's Reply to Patent Owner's Response, filed June 20, 2023, 57 pages.	☐
35	Paper 31, IPR 2022-00996, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐
36	Paper 33, IPR 2022-00999, Patent Owner's Sur-Reply, filed August 4, 2023, 48 pages.	☐

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

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9	7719866	B2	2010-05-18	BOLDO	
10	7721130	B2	2010-05-18	PRETE et al.	
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	6	20090034354	A1	2009-02-05	RESNICK	
	7	20100205470	A1	2010-08-12	MOSHAYEDI et al.	
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	1	Transcript, Day 2 (redacted), Trial on the Merits, Netlist, Inc. (plaintiff) vs. Samsung Electronics Co., Ltd., et al. (defendants), April 17, 2023, 375 pages.	☐	
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	3	Exhibit 1003, IPR 2022-00999, Declaration of Dr. Andrew Wolfe regarding US Patent No. 11,232,054, 431 pages, executed on May 16, 2022.	☐	

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4	Exhibit 1014, Petition for Inter Partes Review of US Patent No. 8,301,833, filed June 20, 2014, 60 pages.	☐
5	Exhibit 1015, IPR 2014-00994, Decision - Denying Institution of Inter Partes Review, issued December 16, 2014, 16 pages.	☐
6	Exhibit 1016, Corrected Petition for Inter Partes Review of US Patent No. 8,301,833, filed September 22, 2014, 67 pages.	☐
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10	Exhibit 1020, Petition for Inter Partes Review of US Patent No. 8,874,831, filed January 17, 2017, 78 pages.	☐
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12	Exhibit 1022, Petition for Inter Partes Review of US Patent No. 8,301,833, filed January 14, 2022, 76 pages.	☐
13	Exhibit 1026, JEDEC STANDARD, DDR2 SDRAM SPECIFICATION, JESD79-2B (Revision of JESD7-2A), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, January 2005, 113 pages.	☐
14	Exhibit 1027, JEDEC STANDARD, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 190 pages.	☐

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15	Exhibit 1028, JEDEC STANDARD, FBDIMM Specification: DDR2 SDRAM Fully Buffered, DIMM (FBDIMM) Design Specification, JESD205, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, March 2007, 129 pages.	☐
16	Exhibit 1031, PCI Local Bus Specification, Revision 2.2, December 18, 1998, 322 pages.	☐
17	Exhibit 1032, Power Electronics: Converters, Applications, and Design, Second Edition, copyright 1995 by John Wiley & Sons, Inc., 37 pages.	☐
18	Exhibit 1040, Texas Instruments, TPS51020, Dual, Voltage Mode, DDR Selectable, Synchronous, Step-Down Controller for Notebook System Power, SLUS564B, July 2003 (revised December 2003), 27 pages.	☐
19	Exhibit 1041, Fairchild Semiconductor, FAN5026, Dual DDR/Dual-Output PWM Controller, October 2005, 17 pages.	☐
20	Exhibit 1042, Murata Manufacturing Co., Ltd, Power Supply Reference Guide for XILINX FPGAs, September 2006, 33 pages.	☐
21	Exhibit 1043, Murata Products, Power Supply Reference Guide for ALTERA FPGAs, Catalog No. DC-03-A, 2008, 40 pages.	☐
22	Exhibit 1045, JEDEC STANDARD, Double Data Rate (DDR) SDRAM Specification, JESD79, JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, June 2000, 77 pages.	☐
23	Exhibit 1046, JEDEC STANDARD, DDR3 SDRAM Specification, JESD79-3A (Revision of JESD79-3), JEDEC SOLID STATE TECHNOLOGY ASSOCIATION, September 2007, 189 pages.	☐
24	Exhibit 1048, Murata Manufacturing, DC-DC Converter Specification(DRAFT), MPD4S014S, January 21, 2008, 11 pages.	☐
25	Exhibit 1049, Micron, NAND Flash Memory, MT29F2G08AABWP/MT29F2G16AABWP, MT29F4G08BABWP/MT29F4G16BABWP, MT29F8G08FABWP, copyright 2004 by Micron Technology, Inc., 57 pages.	☐

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26	Exhibit 1058, LENK, Simplified Design of Switching Power Supplies, Linear Technology, EDN Series for Design Engineers, copyright 1995 by Butterworth-Heinemann, 9 pages.	☐
27	Exhibit 1061, Analog Devices, Super Sequencer with Margining Control and Auxiliary ADC Inputs, ADM1066, copyright 2006 by Analog Devices, Inc., 36 pages.	☐
28	Exhibit 1062, Analog Devices, Analog Dialogue, Volume 40, Number 2, 2006, 24 pages.	☐
29	Exhibit 1063, National Semiconductor, LMC6953, PCI Local Bus Supervisor, October 1996, 12 pages.	☐
30	Exhibit 1067, Lattice Semiconductor Corporation, LatticeXP Family Data Sheet, Version 04.2, March 2006, 127 pages.	☐
31	Exhibit 1068, Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed October 15, 2021, 82 pages.	☐
32	Exhibit 1069, First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, filed January 18, 2022, 122 pages.	☐
33	Exhibit 1071, Complaint, filed December 20, 2021, 49 pages.	☐
34	Exhibit 1072, The Samsung Defendants' Answer, filed April 12, 2022, 37 pages.	☐
35	Exhibit 1073, First Amended Complaint, filed May 3, 2022, 71 pages.	☐
36	Exhibit 1075, IPR 2022-00999, Deposition of William Mangione-Smith, Ph.D. regarding US Patent No. 11,232,054, 245 pages, dated June 12, 2023.	☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

37	Exhibit 1076, IPR 2022-00999, redline comparing Declarations - Declaration of Dr. William Henry Mangione-Smith regarding US Patent No. 11,232,054, 165 pages, executed on March 29, 2022.	☐
38	Exhibit 1077, Netlist, Technology Tutorial: In the Matter of Certain Memory Modules and Components Thereof and Products Containing Same, Inv No. 337-TA-1023, May 8, 2017, 11 pages.	☐
39	Exhibit 1078, Analog Devices, Step-Down DC-to-DC Controller, ADP1821, copyright 2005-2007 by Analog Devices, Inc., 24 pages.	☐
40	Exhibit 2001, IPR 2022-00999, Declaration of Dr. Sunil P. Khatri regarding US Patent No. 11,232,054, 68 pages, executed on September 8, 2022.	☐
41	Exhibit 2003, BELLONI et al., 24.6 A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current, ISSCC 2008 / Session 24 / Analog Power Techniques / 24.6, 2008 IEEE International Solid-State Circuits Conference, 3 pages.	☐
42	Exhibit 2004, MA et al., Single-Inductor Multiple-Output Switching Converters With Time-Multiplexing Control in Discontinuous Conduction Mode, IEEE Journal of Solid-State Circuits, Volume 38, Number 1, January 2003, pages 89-100 (12 pages).	☐
43	Exhibit 2006, Micron, Technical Note: Power Solutions for DDR2 Notebook PCs, TN-47-05 DDR2 Power Solutions for Notebooks, copyright 2004 by Micron Technology, Inc., 16 pages.	☐
44	Exhibit 2007, Texas Instruments, LP2996-N, LP2996A DDR Termination Regulator, SNOSA40K, November 2002 (revised December 2016), 39 pages.	☐
45	Exhibit 2008, JAMECO ELECTRONICS, Jameco Part Number 843868, National Semiconductor: LP2996: DDR Termination Regulator, June 2006, 19 pages.	☐
46	Exhibit 2009, JAMECO ELECTRONICS, Jameco Part Number 843930, National Semiconductor: LP2997: DDR-II Termination Regulator, June 2006, 13 pages.	☐
47	Exhibit 2010, National Semiconductor: LP2998: DDR-II and DDR-I Termination Regulator, December 12, 2007, 18 pages.	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17582797
Filing Date	2022-01-24
First Named Inventor	CHEN
Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

48	Exhibit 2011, BERGVELD, Battery Management Systems: Design by Modelling, copyright 2001 by Royal Philips Electronics N.V., 328 pages.	☐
49	Exhibit 2012, ROMO, DDR Memories: Comparison and Overview, NXP, pages 70-73 (4 pages), September 21, 2007.	☐
50	Exhibit 2013, JEDEC Standard No. 21-C, Page 4.20.3-1; PC133 SDRAM Unbuffered SO-DIMM, Reference Design Specification, Revision 1.02, 26 pages. downloaded August 16, 2022.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	07/02/2024
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17582797
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Art Unit	2138
Examiner Name	FARROKH
Attorney Docket Number	022955-000090

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2024-05-28
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/582,797	01/24/2022	Chi-She Chen	022955-000090	3546
151145	7590	08/08/2024	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW			ART UNIT	
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			08/08/2024	
			ELECTRONIC	

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

Notice of Pre-AIA or AIA Status

1. The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.

Continued Examination Under 37 CFR 1.114

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 05/28/2024 has been entered.

Applicant's request for Suspension of Action

3. Applicant's request filed 05/29/2024, for suspension of action in this application under 37 CFR 1.103(b) or (c) is denied as being improper. The request was not filed at the time of filing a CPA or RCE, and/or (2) not accompanied by the requisite fee as set forth in 37 CFR 1.17(i). See MPEP § 709.

The RCE was filed on 05/28/2024 (e.g., different from time of suspension request).

DETAILED ACTION:

4. This office action is in response to the communication(s) filed on 05/28/2024. There are a total of 19 claims pending in the application. Claims 2, 6-8, 11 and 14 have been amended; claims 1, 3-5, 9-10, and 12-13 have been canceled; and new claims 16-27 have been added.

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 05/28/2024 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the Examiner.

RESPONSE TO REMARKS:

5. Applicant's arguments have been fully considered and based on Trial Termination (Trial-Term) or Final Written Decision, by United State Patent and Trademark. The Trial-Term appears, for most part, to be based IDS's that may or may not filed by the Applicant. The Trial-Terms Final Written Decision considered that Applications 17/138,766 (now US 11,016,918 B2); and 17/328,019 (now US 11,232,054 B2 not patentable. Therefore, the Examiner considers the claims of Application 17/582,797, that substantially include limitations similar to claims of Applications 17/138,766 and 17/328,019, not to be patentable. Therefore, the Examiner as shown below rejected the claims.

INFORMATION CONCERNING CLAIMS:

Claim Rejections - 35 USC § 103

In the event the determination of the status of the application as subject to AIA 35 U.S.C. 102 and 103 (or as subject to pre-AIA 35 U.S.C. 102 and 103) is incorrect, any correction of the statutory basis (i.e., changing from AIA to pre-AIA) for the rejection will not be considered a new ground of rejection if the prior art relied upon, and the rationale supporting the rejection, would be the same under either status.

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2, 6-8, 11, 15-18, and 20-24 are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Harris et al. "Harris" (US 2006/0174140 A1) in view of FBDIMM Standards (Exhibitions 1027, 2028 provided by Applicant) and Amidi et al. "Amidi" (US 7,724,604 B2). The rejection is based on information provided in Trial Termination or Final Written Decision (hereinafter Trial-Trim, dated 12/06/2023) by the USPTO Trial and Appeal Board on Application 17/138,766 (now US patent 11,016,918 B2), which appears, in most part, to be based on Exhibition 1001, IPR 2022-00996. The instant Application, which is a continuation of US Patent 11,016,918 B2 includes substantially the same or similar claim limitations.

6. *Regarding claim 2, Harris teaches or suggests:*

"A dual in-line memory module (DIMM) (e.g., Fig. 1A, ¶ 0009, memory module 100A) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:" (e.g., Harris: Fig. 1A, ¶ 0009, a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address; ¶ 0010, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure ¶ 0013, It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards; Fig 1B, ¶ 0014, ¶ 0010, Reference numerals 120-1 through 120-K refer to K supply voltage paths

which may be coupled to various voltage sources provided within the electronic system; Trial-Trim: pages 42-56, power, data, address and control signal; Trial-Trim: pages 18-84). *Fig. 1B Harris shows a block diagram of memory module 100B comprising DRAM devices 110, inputs a plurality voltages 120 from external source and generates a plurality of regulated voltages 106 and 108. The memory module 100B also comprises Buffer 112 that receives command, address, and data from the external source via interface path 114.*

“a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected the first set of edge connections, a set of data lines electrically connected to second set of edge connections, and a set of address and control lines electrically connected to third set of edge connections;” **(e.g., Harris: Fig. 3, ¶ 0017, a block diagram of an exemplary memory assembly 300 according to one embodiment. A memory controller 302 is operable to drive a bidirectional memory link 304 to which a plurality of memory boards 306-1 through 306-M are coupled in a daisy-chain fashion at their respective buffers; Fig. 4, ¶ 0018, an exemplary computer system 400 according to one embodiment... A number of memory modules 410 are coupled to the memory control block 408 via a memory link 411; Trial-Term: pages 18-84).** *Figs 3 and 4 of Harris shows a plurality of Boards 306 or modules connected to external device (e.g., memory controller). Fig. 3 of Harris that the plurality of boards or modules 306 comprising edge connections to connect to the external memory controller or device.*

“a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of

data lines based on control and address signals received from the host system via the set of address and control lines;” (e.g., **Harris: Fig. 1A, ¶ 0009, a Dual In-line Memory Module (DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device having a particular density, e.g., 256 Mb, 512 Mb, 1 Gb or 2 Gb, etc. Also, the memory devices can be of any known or heretofore unknown DDR type; Trial-Term: pages 18-84**). *Harris teaches supplying voltages to Fully-Buffered DIMM (FBDIMM). However, Harris does not appear to expressly teach while:*

*FBDIMM Standards discloses: “and first, second, third and **fourth buck converters** coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, **third and fourth buck** converters being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line, wherein each component of the set of is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines,” (e.g., **Trial-Trim: Pages 20-40 and 56-59; Trial-Trim: pages 18-84**). *Trial-Trim discloses that combining Harris with FBDIMM Standard teaches or render obvious all limitation recited above comprising regulated voltage converters (e.g., including buck converters) recited in the claim.**

“wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control

power delivery to one or more **components** of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is **turned off** and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state.” (e.g., **Trial-Trim: Pages 16-41 and 64-65, The combination of Harris and the FBDIMM Standards discloses an S3 sleep mode switch that selectively switches off the second voltage to turn off the power to one or more registers while the DRAMS remains powered on to refresh data in DRAMS; Trial-Trim: pages 18-84**). *Trial-Trim discloses the combination of Harris provides or maps regulated voltages as specified in the claim and DIMMs configured to operate in a plurality mode at least the normal mode or state and sleep mode or state.*

Amidi disclose: “a controller including a voltage **monitor** circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage **monitor** circuit configured to (i) **monitor** an input voltage supplied via the input voltage supply line, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;” (e.g., **Amidi: Fig. 5, col. 4, lines 14-22, Power management block 500 includes the actual power management module 510, an incoming system supply 520, an incoming battery supply 530, and an outgoing memory power supply 540. Power management block 500 may thus be used to attempt to ensure a stable power supply even in the face of disruptions in system supply 520, for example, Figs 5-6 of Amidi and the corresponding text descriptions; TRIAL-TRM: pages 70-64; pages 18-84**).

Disclosures by Harris, FBDIMM Standards, and Amidi are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the Voltage Distribution System and Method for a Memory Assembly taught by Harris to include the voltage (power), data, and address/control signals disclosed by FBDIMM Standards; furthermore, to include Clock and Power Fault Detection disclosed by Amidi.

The motivation for including the voltages, data, address, and control signal as taught by page 41 of TRIAL-TRM is to look/obtain information concerning voltages for the FBDIMM; furthermore, the motivation to include Clock and Power Fault Detection is to attempt to ensure a stable power supply even in the face of disruptions in system supply 520, for example.

Therefore, it would have been obvious to combine teaching of FBDIMM Standards and Amidi with Harris to obtain the invention as specified in the claim.

7. *Regarding claim 16, Harris teaches or suggests:*

“A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:” (e.g., Harris: Fig. 1A, ¶ 0009, a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address; ¶ 0010, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure ¶ 0013, It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards;

Fig 1B, ¶ 0014, ¶ 0010, Reference numerals 120-1 through 120-K refer to K supply voltage paths which may be coupled to various voltage sources provided within the electronic system; Trial-Term: pages 42-56, power, data, address and control signal; Trial-Term: pages 18-84). *Fig. 1B Harris shows a block diagram of memory module 100B comprising DRAM devices 110, inputs a plurality voltages 120 from external source and generates a plurality of regulated voltages 106 and 108. The memory module 100B also comprises Buffer 112 that receives command, address, and data from the external source via interface path 114.*

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, a set of data lines electrically connected to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections;”
(e.g., Harris: Fig. 3, ¶ 0017, a block diagram of an exemplary memory assembly 300 according to one embodiment. A memory controller 302 is operable to drive a bidirectional memory link 304 to which a plurality of memory boards 306-1 through 306-M are coupled in a daisy-chain fashion at their respective buffers; Fig. 4, ¶ 0018, an exemplary computer system 400 according to one embodiment... A number of memory modules 410 are coupled to the memory control block 408 via a memory link 411; Trial-Term: pages 18-84). *Figs 3 and 4 of Harris shows a plurality of Boards 306 or modules connected to external device (e.g., memory controller). Fig. 3 of Harris that the plurality of boards or modules 306 comprising edge connections to connect to the external memory controller or device.*

“a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM)

devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines;" (e.g., **Harris: Fig. 1A, ¶ 0009, a Dual In-line Memory Module (DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device having a particular density, e.g., 256 Mb, 512 Mb, 1 Gb or 2 Gb, etc. Also, the memory devices can be of any known or heretofore unknown DDR type; Trial-Term: pages 18-84**). *Harris teaches supplying voltages to Fully-Buffered DIMM (FBDIMM). However, Harris does not appear to expressly teach while:*

*FBDIMMM Standards discloses: "and first, second, **third and fourth buck converters** coupled to the PCB and to the input voltage supply line of the set of voltage supply lines and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, third and **fourth buck converters** being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line, wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines," (e.g., **Trial-Trim: Pages 20-40 and 56-59; Trial-Trim: pages 18-84**). *Trial-Trim discloses that combining Harris with FBDIMM Standard teaches or render obvious all limitation recited above comprising regulated voltage converters (e.g., including buck converters) recited in the claim.**

“wherein, in response to a second **trigger** condition, the controller is configured to turn power via the first regulated voltage line off or on, and wherein, in response to a third trigger condition, the controller is configured to turn power via the second regulated voltage line off or on.” (e.g., **Trial-Trim: Pages 16-41 and 64-65, The combination of Harris and the FBDIMM Standards discloses an S3 sleep mode switch that selectively switches off the second voltage to turn off the power to one or more registers while the DRAMS remains powered on to refresh data in DRAMS; Trial-Trim: pages 18-84**). *Trial-Trim discloses that FBDIMM Standards teaches/provides S3 mode switch that turns components off/on.*

Amidi discloses: “a controller including a voltage **monitor** circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage **monitor** circuit configured to **monitor** an input voltage supplied via the input voltage supply line, generate a **trigger** signal upon detecting a first trigger condition, and transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the first trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;” (e.g., **Amidi: Fig. 5, col. 4, lines 14-22, Power management block 500 includes the actual power management module 510, an incoming system supply 520, an incoming battery supply 530, and an outgoing memory power supply 540. Power management block 500 may thus be used to attempt to ensure a stable power supply even in the face of disruptions in system supply 520, for example, Figs 5-6 of Amidi and the corresponding text descriptions; TRIAL-TRM: pages 70-64; pages 18-84**). *The motivation for combining is based on the same rationale presented for rejection of the independent claim 1.*

8. *Regarding claim 22, Harris teaches or suggests:*

“A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein power from the host

system is provided to the DIMM via the set of power conduits, data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits, the DIMM comprising:” (e.g., Harris: Fig. 1A, ¶ 0009, a fully buffered DIMM wherein a buffer/logic component 112 is provided for buffering command/address; ¶ 0010, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure ¶ 0013, It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible with applicable Joint Electron Device Engineering Council (JEDEC) standards; Fig 1B, ¶ 0014, ¶ 0010, Reference numerals 120-1 through 120-K refer to K supply voltage paths which may be coupled to various voltage sources provided within the electronic system; Trial-Trim: pages 42-56, power, data, address and control signal; Trial-Trim: pages 18-84). *Fig. 1B Harris shows a block diagram of memory module 100B comprising DRAM devices 110, inputs a plurality voltages 120 from external source and generates a plurality of regulated voltages 106 and 108. The memory module 100B also comprises Buffer 112 that receives command, address, and data from the external source via interface path 114.*

“a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including a first set of edge connections configured to be electrically connected to the set of power conduits, a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits, the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, a set of data lines electrically connected to the second set of edge connections, and a set of address and control lines electrically connected to the third set of edge connections;” (e.g., Harris: Fig. 3, ¶ 0017, a block diagram of an exemplary memory assembly 300 according to one embodiment. A memory controller 302 is operable to drive a

bidirectional memory link 304 to which a plurality of memory boards 306-1 through 306-M are coupled in a daisy-chain fashion at their respective buffers; Fig. 4, ¶ 0018, an exemplary computer system 400 according to one embodiment... A number of memory modules 410 are coupled to the memory control block 408 via a memory link 411; Terial-Term: pages 18-84). *Figs 3 and 4 of Harris shows a plurality of Boards 306 or modules connected to external device (e.g., memory controller). Fig. 3 of Harris that the plurality of boards or modules 306 comprising edge connections to connect to the external memory controller or device.*

“a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on control and address signals received from the host system via the set of address and control lines;” **(e.g., Harris: Fig. 1A, ¶ 0009, a Dual In-line Memory Module (DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device having a particular density, e.g., 256 Mb, 512 Mb, 1 Gb or 2 Gb, etc. Also, the memory devices can be of any known or heretofore unknown DDR type; Trial-Term: pages 18-84). Harris teaches supplying voltages to Fully-Buffered DIMM (FBDIMM). However, Harris does not appear to teach while:**

*FBDIMMM Standards discloses: “first, second, third and fourth **buck converters** coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power to the set of components via first, second, third and fourth regulated voltages lines, the first, second, **third and fourth buck converters** being further configured to generate first, second, third and fourth regulated voltages, respectively, from the power received from the input voltage supply line, and to output the first, second, third and fourth regulated voltages via the first, second, third, and fourth regulated voltage lines, respectively, the set of components including a first component configured to receive power via at least the first regulated voltage line, a second component configured to receive power via at least the second regulated voltage line, a third component configured to receive power via at least the*

third regulated voltage line, and a fourth component configured to receive power via at least the fourth regulated voltage line, wherein each component of the set of components is electrically connected to one or more of the first, second, third and fourth regulated voltages lines, and receives power only via the one or more of the first, second, third and fourth regulated voltage lines,” (e.g., **Trial-Trim: Pages 20-40 and 56-59; Trial-Trim: pages 18-84**). *Trial-Trim discloses that combining Harris with FBDIMM Standard teaches or render obvious all limitation recited above comprising regulated voltage converters (e.g., including buck converters) recited in the claim.*

“wherein, in response to a second **trigger** condition, the controller is further configured to turn off power via the first regulated voltage line while power via the second, third and fourth regulated voltage lines is turned on.” (e.g., **Trial-Trim: Pages 16-41 and 64-65, The combination of Harris and the FBDIMM Standards discloses an S3 sleep mode switch that selectively switches off the second voltage to turn off the power to one or more registers while the DRAMS remains powered on to refresh data in DRAMS; Trial-Trim: pages 18-84**). *Trial-Trim discloses that FBDIMM Standards teaches/provides S3 mode switch that turns components off/on.*

Amidi discloses: “a controller including a voltage **monitor** circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage **monitor** circuit configured to **monitor** an input voltage supplied via the input voltage supply line, to generate a **trigger** signal upon detecting a first trigger condition, and to transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the first trigger condition occurs when the input voltage exceeds a first preset threshold voltage that is above an operating voltage of the DIMM;” (e.g., **Amidi: Fig. 5, col. 4, lines 14-22, Power management block 500 includes the actual power management module 510, an incoming system supply 520, an incoming battery supply 530, and an outgoing memory power supply 540. Power management block 500 may thus be used to attempt to ensure a stable power supply even in the face of disruptions in system supply 520, for example, Figs 5-6 of Amidi and**

the corresponding text descriptions; TRIAL-TRM: pages 70-64; pages 18-84). *The motivation for combining is based on the same rational presented for rejection of the independent claim 1.*

9. *Regarding claims 6, Trial-Term teaches:*

“wherein the controller is further configured to periodically perform one or more write operations at regular intervals of time in response to an additional trigger signal that is associated with an additional trigger condition, the additional trigger condition including a request from the host system **or** detection of a voltage level deviation from one or more threshold voltages.” **(e.g., Trial-Term: pages 78-80).** *Generating trigger signals for overvoltage detection and undervoltage detection for different DIMM voltage values, requires setting of threshold voltage of different values.*

10. *Claims 7-8, 17, 20, 23, and 26 are rejected based on the same ground of rejection as claim 6.*

11. *Regarding claims 11, Trial-Term teaches:*

“a register coupled to the PCB, the first regulated voltage line, and the set of address and control lines, wherein: during the first state, the register is configured to receive power via the first regulated voltage line, receive and register address and control signals from the host system via the set of address and control lines, and output registered address and control signals, and during the second state, the register does not output registered address and control signals.” **(e.g., Trial-Trim: Pages 16-41 and 64-65, The combination of Harris and the FBDIMM Standards discloses an S3 sleep mode switch that selectively switches off the second voltage to turn off the power to one or more registers while the DRAMS remains powered on to refresh data in DRAMS; Trial-Trim: pages 18-84).** *Trial-Trim discloses the combination of Harris provides or maps regulated voltages as specified in the claim and DIMMs configured to operate in a plurality mode at least the normal mode or state and sleep mode or state.*

12. *Regarding claims 15, 21, and 27, Trial-Term teaches:*

“wherein two of the first, second, third and fourth buck converters are configured to operate as a dual-buck converter.” (e.g., **Trial-Trim: Page 63**). *It would have been obvious to implement two or more regulate voltages using dual-buck converter.*

Claims 14, 18, 19, and 25 rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Harris, FBDIMM Standards, and Amidi as applied to claims 6, 18, and 24 above, and further in view of Levkovitz et al. “Levkovitz” (US 2007/0088838 A1).

13. *Regarding claim 14, Harris, FBDIMM Standards, and Amidi teach all limitations recited in claim 6 but do not expressly teach while Levkovitz discloses:*

“wherein the regular intervals of time are every millisecond.” (e.g., ¶ 0075) periodically, at pre-defined intervals dump or copy data into a non-volatile memory. Specifying a certain periodic time-interval is a design choice.

Disclosures by Harris, FBDIMM Standards, Amidi and Levkovitz are analogous because they are in the same field of endeavor and/or solving a similar or common problem.

It would have been obvious to a person of having ordinary skill in the art before the effective filing date of the claimed invention to modify the Voltage Distribution System and Method for a Memory Assembly taught by Harris to include the voltage (power), data, and address/control signals disclosed by FBDIMM Standards; furthermore, to include Clock and Power Fault Detection disclosed by Amidi; furthermore, to include the periodically copying data to non-volatile memory disclosed by Levkovitz.

The motivation for including the voltages, data, address, and control signal as taught by page 41 of TRIAL-TRM is to look/obtain information concerning voltages for the FBDIMM; furthermore, the motivation to include Clock and Power Fault Detection is to attempt to ensure a stable power supply even in the face of disruptions in system supply 520, for example; furthermore, the motivation for copying the data to non-volatile memory as taught by paragraph [0275] of Levkovitz is to limit the data loss in case of a power outage which may erase the volatile memory unit.

Therefore, it would have been obvious to combine teaching of Levkovitz, FBDIMM Standards, and Amidi with Harris to obtain the invention as specified in the claim.

Claims 18, 19 and 25 include similar limitations.

DIRECTION OF FUTURE CORRESPONDENCES:

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

15. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/HASHEM FARROKH/
Primary Examiner, Art Unit 2138*



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/582,797	Applicant(s) Chen et al.		
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No	Page 1 of 2

All Participants (applicant, applicants representative, PTO personnel)	Title	Type
HASHEM FARROKH	Primary Examiner	Telephonic
Khaled Shami	Attorney	

Date of Interview: 06 September 2024

Issues Discussed:

35 U.S.C. 103

An applicant initiated interview with the Applicant, Mr. Khaled Shami (reg. # 38,745), conducted on 09/06/2024. The interview was in response to the non-final office action mailed 08/08/2024. Applicant presented a proposed amendment of claims in which claim 2 was amended, claims 1 and 3-27 canceled and claims 28-23 added. Applicant summarize the differences between the amended newly amended claims and the prior art of record in Items I through VI shown below. However, amendments fails to point the portion(s) of the specification that describe amendment (or arguments).

I. The limitation recite "a input voltage line from the memory socket...", then I.a recites power from system board provided by the set of power conduits. Specification does not describe/support the set of power conduits.

II. The specification does not describe/support a set of edge connection configure to be connected to a set of data conduits (or address and control conduits).

III. Applicant appears to state the claim limitation(s) that DIMM operates in two states no longer is being claimed. In discussion related to item number III, Applicant appears to discuss limitations or subject matters that are not described/supported by the specification, as an example the specification does not describe a plurality of packages. Furthermore, In the non-final rejection, mailed on 08/08/2024, the Trial Termination document also used as additional reference information. The Applicant arguments, for most part, appear to based on Harris and FBDIMM. The Examiner suggests that Applicant also refer to the relevant portion(s) of Trial-Term document and describe why the amendment overcome issues related to the board final decision.

IV. Regarding voltage regulation and mapping, the board has decided that combination of Harris and FBDIMM standards renders obvious limitations regarding voltage regulators (including buck converters). Applicant needs to describe what is new in claim limitations that overcome the discussion in Trial-Term document and the board decision.

V. Amidi teaches that memory (comprising backup power) may operate in backup mode, in response, for example, in response to change to voltage level (e.g., a triggering condition). The backup comprises a plurality of write operations.

VI. Paragraph [0075] teaches periodically dump or copy data to non-volatile memory. The reason for periodic of copying is to limit data loss in the event of sudden power loss. The copying or backup performed in a pre-defined time intervals. A timer may be programmed to trigger the copying at pre-defined time interval

<i>Applicant-Initiated Interview Summary</i>	Application No. 17/582,797	Applicant(s) Chen et al.		
	Examiner HASHEM FARROKH	Art Unit 2138	AIA (First Inventor to File) Status No	Page 2 of 2

/HASHEM FARROKH/ Primary Examiner, Art Unit 2138	
<p>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</p> <p>Please further see: MPEP 713.04 Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b) 37 CFR § 1.2 Business to be transacted in writing</p>	

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 3546

APPLICATION NO: 17/582,797

ART UNIT: 2138

FILING DATE: January 24, 2022

EXAMINER: FARROKH

TITLE: MEMORY WITH ON-MODULE POWER MANAGEMENT (as amended)

PROPOSED AMENDMENT AND INTERVIEW AGENDA

FOR DISCUSSION PURPOSES ONLY

LISTING OF PROPOSED CLAIMS

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~slot connector socket~~ of a system board of a ~~host computer~~ system, the memory ~~slot connector socket~~ including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the ~~host system board system~~ is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data ~~signal~~ signal is electrically conducted between the ~~host system board~~ and the DIMM are transferred via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the ~~host system board~~ are transferred to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB), the PCB including:

an interface having edge connections disposed along the width of the PCB and configured to fit into the memory ~~slot connector socket~~ of the ~~host system~~, the edge connections including a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits, a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits,

the PCB further including a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board,

a set of data lines electrically ~~connected~~ coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is

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configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines, and

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a set of address and control lines electrically ~~connected~~ coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller including a voltage monitor circuit, a data storage element configured to store a plurality of data bits, a logic element, and nonvolatile memory, the controller coupled to the PCB and electrically connected to the ~~to an~~ input voltage supply line ~~of the set of voltage supply lines~~, the controller configured to receive the system power when the input voltage is electrically conducted by the input voltage supply line, the voltage monitor circuit configured to (i) monitor an input voltage by comparing the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage ~~supplied via the input voltage supply line~~, (ii) generate a trigger signal upon detecting a trigger condition, and (iii) transmit the trigger signal to the logic element ~~at least one other portion of the controller~~, wherein the controller logic element is configured to perform, in response to the trigger signal, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element, and then a third write operation to write the first and second sets of data bits from the data storage element into the nonvolatile memory, wherein the DIMM is operable when the input voltage is within a range of operating voltage values of the DIMM, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, wherein the lower operating voltage value is below a specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value, wherein the input voltage corresponds to the specified operating voltage value, wherein the first threshold voltage matches the lower operating voltage value, and the second threshold voltage matches the upper operating voltage value, and wherein the trigger condition occurs when the input voltage exceeds the second ~~a first preset~~ threshold voltage ~~that is above an operating voltage of the DIMM~~;

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a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR SDRAM) devices;

packages coupled to the set of address and control lines and to the set of data lines, the each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and devices being operable to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines based on address and control signals received from the system via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third and fourth converter circuits being configured coupled to the PCB and to the controller, each of the first, second, third and fourth converter circuits input voltage supply lines configured to receive power from the controller when the system power is received by the controller, the first, second, third and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power received from the controller and (ii) output the first, second, third, and fourth regulated voltages via first, second, third and fourth regulated voltage lines, wherein the first regulated voltage line is configured to output the first regulated voltage, the second regulated voltage line is configured to output the second regulated voltage, the third regulated voltage line is configured to output the third regulated voltage, and the fourth regulated voltage line is configured to output the fourth regulated voltage, wherein the first converter circuit is a buck converter, the second converter circuit is a buck converter, the third converter circuit is a buck converter, and the fourth converter circuit is a voltage reducing circuit, and wherein the first converter circuit is a buck converter, the second converter circuit is a buck converter, the third converter circuit is a buck converter, and the fourth converter circuit is a voltage reducing circuit,

wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit,

wherein each component of the set of components (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines, and (ii) is powered, when the system power is received by the controller, (a) receives power only by one or more of the first, second, third, and fourth converter circuits, and (b) only via the one or more of the first, second, third and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM packages is configured to receive power using at least the first regulated voltage supplied from the first converter circuit via the first regulated voltage line;

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wherein the plurality of DDR SDRAM packages includes a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal, and a second group of at least three DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal.

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wherein the first group of DDR SDRAM packages is operable to be (i) accessible and not in self-refresh mode, and (ii) enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines.

wherein the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals, and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data lines of the set of data lines, and the total number of data lines is at least 72 data lines.

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wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control power delivery to one or more components of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is turned off and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state.

3 – 5. (Canceled)

6 – 27 (Canceled)

28. (New) The DIMM of claim 2, wherein the second component (i) is electrically connected to both the first and second regulated voltage lines, and (ii) is powered on when the first and second

regulated voltages are turned on by the first and second converter circuits, respectively.

29. (New) The DIMM of claim 2, wherein the data storage element is a buffer configured to store the plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

30. (New) The DIMM of claim 2, wherein the PCB is configured to have a form factor with a width of 133.35 millimeters.

31. (New) The DIMM of claim 30, wherein the form factor of the PCB is selected from one of a plurality of profiles ranging in height from 18.3 millimeters to 50 millimeters.

32. (New) The DIMM of claim 2, wherein the third write operation to write the first and second sets of data bits from the data storage element into the nonvolatile memory includes the logic element combining the first set of data bits and the second set of data bits and writing the combined first and second sets of data bits into the nonvolatile memory.

33. (New) The DIMM of claim 2, wherein the third write operation to write the first and second sets of data bits from the data storage element into the nonvolatile memory includes the logic element writing the plurality of data bits from the data storage element into the nonvolatile memory.

34. (New) The DIMM of claim 2, wherein, when the system power is received by the controller, the nonvolatile memory is not powered using the first regulated voltage.

35. (New) A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB), the PCB including:

an interface having edge connections disposed along the width of the PCB and configured to fit into the memory socket, the edge connections including a first set of edge connections configured to be electrically connected to respective power conduits of the set of

power conduits, a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller including a voltage monitor circuit, a data storage element configured to store a plurality of data bits, a logic element, and nonvolatile memory, the controller coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power when the input voltage is electrically conducted by the input voltage supply line, the voltage monitor circuit configured to monitor the input voltage by comparing the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage, wherein the logic element is configured to periodically perform, at regular intervals of time and in response to a trigger condition, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element, wherein the DIMM is operable when the input voltage is within a range of operating voltage values of the DIMM, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, wherein the lower operating voltage value is below a specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value, wherein the input voltage corresponds to the specified operating voltage value, wherein the first threshold voltage matches the lower operating voltage value, and the second threshold voltage matches the upper operating voltage value, and wherein the trigger condition occurs when the input voltage exceeds the second threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and operable to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines based on address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth converter circuits coupled to the PCB and to the controller, each of the first, second, third, and fourth converter circuits configured to receive power from the controller when the system power is received by the controller, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power received from the controller, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, the set of components including a first component electrically connected to the first regulated voltage line and powered on when the first regulated voltage is turned on by the first converter circuit, a second component electrically connected to the second regulated voltage line and powered on when the second regulated voltage is turned on by the second converter circuit, a third component electrically connected to the third regulated voltage line and powered on when the third regulated voltage is turned on by the third converter circuit, and a fourth component electrically connected to the fourth regulated voltage line and powered on when the fourth regulated voltage is turned on by the fourth converter circuit, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit;

wherein each component of the set of components (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines, and (ii) is powered, when the system power is received by the controller, (a) only by one or more of the first, second, third, and fourth converter circuits, and (b) only via the one or more of the first, second, third, and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM packages is configured to receive power using at least the first regulated voltage supplied from the first converter circuit via the first regulated voltage line;

wherein the plurality of DDR SDRAM packages includes a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal, and a second group of at least three DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein the first group of DDR SDRAM packages is operable to be (i) accessible and not in

self-refresh mode, and (ii) enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;

wherein the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data lines of the set of data lines, and the total number of data lines is at least 72 data lines.

36. (New) The DIMM of claim 35, wherein each of the regular intervals of time is one millisecond duration.

37. (New) The DIMM of claim 35, wherein the logic element is further configured to read and combine first and second data bits from the first and second portions of the data storage element, respectively.

38. (New) The DIMM of claim 37, wherein the plurality of write operations includes a third write operation, and wherein the logic element is further configured to perform the first and second write operations and subsequently to perform the third write operation to write the combined data bits from the first and second portions of the data storage element into the nonvolatile memory.

39. (New) The DIMM of claim 35, wherein the data storage element is a buffer configured to store the plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

40. (New) The DIMM of claim 35, wherein the PCB is configured to have a form factor with a width of 133.35 millimeters.

41. (New) The DIMM of claim 41, wherein the form factor of the PCB is selected from one of a plurality of profiles ranging in height from 18.3 millimeters to 50 millimeters.

42. (New) The DIMM of claim 35, wherein, when the system power is received by the controller, the nonvolatile memory is not powered using the first regulated voltage.

43. (New) A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB), the PCB including:

an interface having edge connections disposed along the width of the PCB and configured to fit into the memory socket, the edge connections including a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits, a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;

a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller including a voltage monitor circuit, a data storage element configured to store a plurality of data bits, a logic element, and nonvolatile memory, the controller coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power when the input voltage is electrically conducted by the input voltage supply line, the voltage

monitor circuit configured to monitor the input voltage by comparing the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage, wherein the logic element is configured to periodically perform every millisecond, in response to a trigger condition, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element, wherein the DIMM is operable when the input voltage is within a range of operating voltage values of the DIMM, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, wherein the lower operating voltage value is below a specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value, wherein the input voltage corresponds to the specified operating voltage value, wherein the first threshold voltage matches the lower operating voltage value, and the second threshold voltage matches the upper operating voltage value, and wherein the trigger condition occurs when the input voltage exceeds the first threshold voltage and is below the second threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and operable to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines based on address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

first, second, third, and fourth converter circuits coupled to the PCB and to the controller, each of the first, second, third, and fourth converter circuits configured to receive power from the controller when the system power is received by the controller, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power received from the controller, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, the set of components including a first component electrically connected to the first regulated voltage line and powered on when the first regulated voltage is turned on by the first converter circuit, a second component electrically connected to the second regulated voltage line and powered on when the second regulated voltage is turned on by the second converter circuit, a third component electrically connected to the third regulated voltage line and powered on when the third regulated voltage is turned on by the third converter circuit, and a fourth component electrically connected to the fourth regulated voltage line and powered on when the fourth regulated voltage is turned on by the fourth converter circuit, wherein each of the first, second, and third

converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit;

wherein each component of the set of components (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines, and (ii) is powered, when the system power is received by the controller, (a) only by one or more of the first, second, third, and fourth converter circuits, and (b) only via the one or more of the first, second, third, and fourth regulated voltage lines, and wherein the plurality of DDR SDRAM packages is configured to receive power using at least the first regulated voltage supplied from the first converter circuit via the first regulated voltage line;

wherein the plurality of DDR SDRAM packages includes a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal, and a second group of at least three DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein the first group of DDR SDRAM packages is operable to be (i) accessible and not in self-refresh mode, and (ii) enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;

wherein the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data lines of the set of data lines, and the total number of data lines is at least 72 data lines.

REMARKS

By this Proposed Amendment, submitted for purposes of discussion only, Applicant has **amended claim 2; canceled claims 6-8 and 11 and 14-27; and added new claims 28-43.** (Claims 3-5, 9-10, and 12-13 were previously canceled). **Claims 2 and 28-43 are now pending.**

Agenda for Examiner Interview

Points of Distinction to Discuss

- I. **The system power used by four converters is electrically connected to an input voltage line from the memory socket of a system board of a computer system in a particular form and on particular first set of edge connections of the PCB having edge connections configured to fit into the memory slot connector.**
- a. “wherein power from the system board is provided to the DIMM via the memory socket by the set of power conduits” and
 - b. “a printed circuit board (PCB) having edge connections configured to fit into the memory socket, the edge connections including a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits”

Neither Harris nor FBDIMM, singularly or in combination, disclose this feature. Harris discloses “since the Vdd and Vcc power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types) . . .” Para. [0011]. This passage makes clear that the DIMM of Harris draws power from a source external to the system, i.e. “external voltage sources,” as does a reference to “hot-pluggability” especially in light of DRAM technology independence. Each DDR generation standardizes a different set of voltages for memory modules, and the power management system on the motherboard of DDR4 and previous generations exclusively provides power via the socket to the DIMM. Thus, the ONLY way to have hot pluggability and DRAM technology independence is to have power from a source external to the host system.

This source external to the system is confirmed in Para. [0012] of Harris, which further states “a voltage-independent FBD design incorporating the embodiment of FIG. 1A is capable of replacing these power supply interface pins with as few as six +12V pins (from an external voltage source) with local conversion . . .” Paragraph [0019] is even more conclusive.

“Based on the foregoing Detailed Description, it should be appreciated that an implementation of the embodiments described herein thus provides a technology-independent voltage distribution scheme for memory devices where system board power supply and associated voltage plane(s) are eliminated.”

Later in the same paragraph, Harris discloses “reduction in the pin count on DIMM connector to system board or memory riser card (whereby a smaller connector or wider pin spacing may be accommodated); . . . reservation of extra pins for implementing addition standard or proprietary functions.” Thus, it is conclusive that power does not come from the system board or through the socket because those edge connections normally used for power are either eliminated or repurposed.

Moreover, the FBDIMM Standards and Amidi provide no cure for this defect, as they use the same FBDIMM edge connections as Harris.

II. Separate address and control signals, and data signals from system board to the claimed module in a particular form and on particular second and third sets of edge connections of the PCB having edge connections configured to fit into the memory slot connector:

- a. “data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals from the host system are transferred to the DIMM via the set of address and control conduits” and
- b. “a second set of edge connections configured to be electrically connected to the set of data conduits, and a third set of edge connections configured to be electrically connected to the set of address and control conduits”

The JEDEC standard modules which the applied prior art use a packetized signaling protocol. Data and command/control/address signals do not travel on separate lines, because they are sent

in packetized forms called “frames” – “After initialization the host communicates with the AMBs on the channel using southbound frames of information containing commands and data.” JESD206.01, pg. 55

- c. Thus, the data signals are not on “the set of data conduits” and the address and control signals are not on “the set of address and control conduits” as recited in the claim, rather they are on the same set of conduits, referred to as “lanes” by JESD206.01.
- d. Moreover, the FBDIMM Standards and Amidi provide no cure for this defect, as they use the same FBDIMM protocols as Harris.
- e. Thus, the current claims are allowable for at least this additional reason.

III. Applicant’s additional amendments to further distinguish over the teachings of Harris and FBDIMM in the combination such that the claimed DIMM is no longer (i) operable in two states, or (ii) turning off power to any component of the set of components on the claimed DIMM, specifically:

- a. The wherein clause for the DIMM operating in two states and power is turned off to one component is completely deleted, and thus at least for this reason the rejection is no longer applicable.
- b. The claim as currently amended always provide power to all components via all regulated voltage when system power is turned on, and
- c. Additional wherein clauses are added to specifically claim that the DDR SDRAM are accessible and not in self-refresh mode.
- d. At least for the reasons above the claimed DIMM is no longer (i) operable in two states, or (ii) turning off power to any component of the set of components on the claimed DIMM.
- e. Thus, the rejection over Harris and FBDIMM in the combination over the S3 mode is not applicable to the currently amended Claim 2.

IV. Each component of the set of components

- a. is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines, and
- b. is powered, when the system power is received by the controller,

- i. only by one or more of the first, second, third, and fourth converter circuits, and
- ii. only via the one or more of the first, second, third, and fourth regulated voltage lines.

The above listed additional limitations further distinguishes over claim 2 as amended on 2/8/2024 and that none of Harris, FBDIMM, and Amidi, individually or in the combination, teach any of these additional limitations, at least because:

- iii. none of Harris, FBDIMM, and Amidi, individually or in the combination, teach Harris teach a controller configured to receive system power and provide power to each of the four converter circuits, as summarized in limitation 4.a above
- iv. none of Harris, FBDIMM, and Amidi, individually or in the combination, teach Harris teach that four converter circuits receive power from the controller and generates regulated voltages, as summarized in limitations 4.b above.
- v. none of Harris, FBDIMM, and Amidi, individually or in the combination, teach Harris teach that that each component of the set of components including the plurality of DDR SDRAM packages are powered ONLY from the converter circuits regardless of whether a trigger condition is detected by the voltage monitor circuit, and that all four converters are required to receive power from the controller when the system power is received by the controller, as summarized in limitations 4.c and 4.d above.
- c. Thus, none of Harris, FBDIMM, and Amidi, individually or in the combination, teach any of the additional limitations currently presented in sections 4a-4.d above.
- d.

V. Performing a plurality of write operations in response to a trigger condition:

- a. Currently presented limitations further distinguish over Claim 2 as amended on 2/8/2024 and further require that the logic element of the controller, in response to a trigger signal generated by a voltage monitor circuit, performs

- i. first and second write operations to write first and second sets of data bits to data storage element, and then
- ii. write operation to write the first and second set of data bits from the data storage element into the NVM
- iii. the trigger signal generated by the voltage monitor circuit that monitors the input voltage line that supplies the claimed system power to the controller, and compares the input voltage against a range of operating voltages bounded by first and second threshold voltages,
- iv. the trigger condition occurs when the input voltage exceeds the second threshold voltage.

Amidi does not teach writing to NVM in response to detection of any power faults, as required by claim 2. Amidi only teaches a “backup system” and describes ways to “initiate backup system”. However, the “backup system” that Amidi teaches is only about (i) switches the power to the DRAM to a “backup” voltage source such as a battery, and (ii) maintain the DRAM in a self-refresh state using the “backup system” power supply. Please note that Amidi expressly teaches DRAM are not accessible (because they are in self-refresh mode) until main system power is restored. (See at least in Fig. 15 and Col. 9:13-39)

Amidi does not teach that all components of a set components are powered only from the buck converters, as required by claim 2. Amidi teaches that DRAM are powered from system power, and upon detection of power failure switches the DRAM components to a backup system using a battery supplied voltage. (Fig. 5, Fig. 6, Fig. 7, and Fig. 14, and at least in Col. 8:23-61). Thus, Amidi teaches away from powering any component from the system power upon detecting a power fault.

Amidi does not teach the detection of an input voltage that exceed a threshold voltage which is above an operating voltage of the claimed DIMM, as required by claim 2.

Amidi only teaches the detection of power failure and provide many examples of power failure including when input voltage is below a reference voltage such as a 3.0V for a 3.3V rail (Fig. 14 and Col. 8:27-29)

VI. Additional currently presented limitations regarding periodically performing a plurality of write operations in response to a trigger condition, as claimed in independent claim 35:

Levkovitz teaches the periodic dump or copy from volatile to nonvolatile is **always performed every 60 seconds, every 5 minutes, every hour**, and not in response to a trigger condition, as required by the claims.

Furthermore, Levkovitz teaches that memory unit 118 ad server 110 is a volatile memory unit, and thus cannot include nonvolatile memory. Thus, Levkovitz does not teach that the nonvolatile memory is on a memory module that includes the volatile memory (plurality of DDR SDRAM), as required by the claims.

Moreover, **the periodic dump or copy**, as taught by Levkovitz, is to “limit the data loss in case of a power outage which erase the volatile memory unit 118.” Thus, Levkovitz teachings eliminates the needs for Amidi’s teachings.

Respectfully submitted,

Date: September 5, 2024
Vorys, Sater, Seymour, and Pease LLP
1909 K Street, NW 9th Floor
Washington, DC 20006-1152
Tel: (202) 467-8800

/Khaled Shami/
Khaled Shami, Reg. No. 38,745

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(73) Proprietors:
• **NEC CORPORATION**
Tokyo (JP)
• **NEC Electronics Corporation**
Kawasaki, Kanagawa 211-8668 (JP)

(72) Inventors:
• **Maesako, Taketo**
Minato-ku, Tokyo (JP)

• **Yamamoto, Kouki**
Minato-ku, Tokyo (JP)
• **Matsui, Yoshinori**
Minato-ku, Tokyo (JP)
• **Sakakibara, Kenichi**
Minato-ku, Tokyo (JP)

(74) Representative: **Glawe, Delfs, Moll & Partner**
Patentanwälte
Postfach 26 01 62
80058 München (DE)

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor integrated circuit device and, particularly, to a semiconductor integrated circuit device having a main memory portion and a sub-memory portion formed in a semiconductor substrate and a data transfer circuit provided between the main memory portion and the sub-memory portion.

Description of the Related Art

[0002] In general, a relatively low speed, inexpensive semiconductor device having large memory capacity, such as general purpose DRAM, is used as a main memory in a computer system.

[0003] In a recent computer system, an operating speed of a DRAM constituting a main memory is increased with increase of an operating speed of the system, particularly, of a MPU thereof. However, the operating speed of the DRAM is still insufficient and, in order to solve this problem, it is usual to provide a sub-memory between the MPU and the main memory. Such sub-memory is generally called as a cache memory and is constructed with a high speed SRAM or an ECLRAM.

[0004] The cache memory is generally provided externally of the MPU or within the MPU. In a recent workstation or a personal computer, a semiconductor memory device composed of a DRAM constituting the main memory and a high speed SRAM as the cache memory which are formed on one and the same semiconductor substrate is used. Japanese Patent Application Laid-open Nos. Sho 57-20983, Sho 60-7690, Sho 62-38590 and Hei 1-146187 disclose examples of such semiconductor memory. Such semiconductor memory is sometimes called as cache DRAM or CDRAM since it includes the DRAM and the SRAM functioning as the cache memory, etc. The cache memory can transfer data with respect to the DRAM and the SRAM bi-directionally. These prior arts have problems such as delay of data transfer operation in a case of cache mishit and techniques which solve such problem has been proposed. Examples of the proposed techniques are disclosed in Japanese Patent Application Laid-open Nos. Hei 4-252486, Hei 4-318389 and Hei 5-2872. In the techniques disclosed in these Japanese Patent Application Laid-open Nos., a latch or register function is provided in a bi-directional data transfer circuit between a DRAM portion and an SRAM portion, so that a data transfer from the SRAM portion to the DRAM portion and a data transfer from the DRAM portion to the SRAM portion can be done simultaneously and a speed of data transfer (copy back) at the cache mishit can be increased. This will be described with reference to Japanese

Patent Application Laid-open No. Hei 4-318389 as an example. Fig. 92 shows schematically an example of a construction of a memory array portion of a CDRAM. In Fig. 92, a semiconductor memory device includes a DRAM array 9201 including dynamic memory cells, an SRAM array 9202 including static memory cells and a bi-directional transfer gate circuit 9203 for transferring data between the DRAM array 9201 and the SRAM array 9202. The DRAM array 9201 and the SRAM array 9202 are provided with row decoders and column decoders, respectively. Addresses given to the row decoder and the column decoder of the DRAM and the row decoder and the column decoder of the SRAM are mutually independent and given through different address pin terminals. Figs. 93 and 94 show a construction of the bi-directional transfer gate circuit 9203 in detail. According to this construction, the data transfer from SBL to GIO and the data transfer from GIO to SBL are made through different data transfer paths and it is possible to execute these data transfers simultaneously by functions of a latch 9302 and an amplifier 9306.

[0005] However, there are the following problems in the above mentioned CDRAM. First, since address pin terminals and control pin terminals are provided separately for the DRAM array and the SRAM array, the number of external pin terminals is very large compared with that of a single DRAM. Therefore, there is no compatibility of a substrate, etc., on which the semiconductor memory is mounted, with respect to that of a usual DRAM, etc. Second, in the bi-directional transfer gate circuit, the number of circuits each having a area large enough to realize the above mentioned transfer is limited and, therefore, the number of transfer buses is limited. As a result, the number of bits which can be transferred at once between the DRAM array and the SRAM array is limited to 16 bits. Further, the transfer buses are arranged in an area in which column selection lines are not arranged and the number of the transfer buses is limited by a width of the area. Generally, the smaller the number of bits transferred at once provides the lower the cache bit rate.

[0006] Japanese Patent Application Laid-open No. Hei 5-210974 discloses a technique in which address input signal pins of a CDRAM are made common for both a DRAM array and an SRAM array. Figs. 95 and 96 show a construction of this technique. In this example, the second problem that the number of bits transferred at once between the DRAM array and the SRAM array is limited to 16 bits as in the CDRAM is left as it is. Figs. 97 and 98 show a construction in which a memory capacity of an SRAM is increased in order to improve the cache hit rate. In this construction, however, the substrate compatibility is lost due to input pins for selecting SRAM cell and the second problem that the number of bits transferred at once between the DRAM cell array and the SRAM cell array is limited to 16 bits as in the CDRAM is solved.

[0007] As another example in this technical field,

there is an EDRAM (Enhanced DRAM) which is a DRAM with a cache SRAM, as disclosed in, for example, EDN JANUARY 5, 1995, pp. 46 to 56. An EDRAM shown in Fig. 99 is different in construction from a general purpose DRAM having the same memory capacity and has no substrate compatibility although a DRAM and an SRAM commonly use address input terminals. The number of bits transferred at once to the SRAM is the same as the number of sense amplifiers which are activated at once and, in this example, 512($\times 4$) bits are transferred at once. Although, in this construction of the EDRAM, the number of bits transferred at once is large, the SRAM thereof which holds data has a memory capacity of only 1 set (1 row) for bits to be transferred at once. Although the larger the number of bits transferred at one generally provides the higher the cache hit rate, the cache mishit rate is increased since the EDRAM has cache memories of only 1 set (1 row) and, therefore, a sufficient speed-up of the whole system can not be achieved. In order to increase the number of sets (the number of rows) of the cache memories in the EDRAM, an SRAM register and a block selector, etc., must be additionally provided for every predetermined number of blocks of DRAM cell arrays, resulting in a substantial increase of the area occupied by the circuits.

[0008] Further, there is a recent problem of degradation of cache hit rate when there are access requests from a plurality of processing devices as shown in Fig. 100. When the CDRAM or the EDRAM is used as a main memory shown in Fig. 100 and there are access requests from a plurality of processing devices (memory masters), the cache hit rate is lowered and the speed-up of the whole system operation is restricted since the number of address requests of different sets (rows) may be increased.

SUMMARY OF THE INVENTION

[0009] With popularization of the system having a plurality of processing devices (memory masters), a memory portion which can respond to not access requests of one kind as in the conventional memory portion but access requests of a plurality of kinds. That is, a memory having a construction different from that of the conventional memory is required.

[0010] An object of the present invention is to provide a semiconductor integrated circuit device which, in order to achieve a high speed operation of a whole system without lowering cache hit rate even when there are access requests from a plurality of memory masters, includes a main memory portion and a sub memory portion capable of being assigned correspondingly to a plurality of access requests.

[0011] Another object of the present invention is to provide a semiconductor integrated circuit device having a main memory portion and a sub memory portion, an external terminal thereof being constructed similarly to a construction of that of the main memory portion.

[0012] A further object of the present invention is to provide a semiconductor integrated circuit device including a main memory portion and a sub memory portion, the number of bits capable of being transferred between the main memory portion and the sub memory portion at once and the number of sets thereof being optimized.

[0013] Another object of the present invention is to provide a semiconductor integrated circuit device including a main memory portion and a sub memory portion, in which a read/write operation of the sub memory portion and a data transfer operation between the main memory portion and the sub memory portion can be performed simultaneously.

[0014] The invention is defined by claim 1.

BRIEF DESCRIPTION OF THE DRAWINGS

[0015] The above and other objects, features and advantages of the present invention will become more apparent by reference to the following detailed description of the present invention taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing a whole construction of a semiconductor memory device according to a first embodiment of the present invention;

Fig. 2 is a block diagram of a memory system including the semiconductor memory device shown in Fig. 1 and a plurality of memory masters which perform access requests with respect to the semiconductor memory device;

Fig. 3 is a block diagram of a memory system including the semiconductor memory device shown in Fig. 1 and a plurality of memory masters which perform access requests with respect to the semiconductor memory device;

Fig. 4 is a block diagram of a semiconductor device comprising the semiconductor memory device shown in Fig. 1 and a memory control device for controlling and generating an input signal to the semiconductor memory device, which are formed on one and the same semiconductor substrate;

Fig. 5 is a block diagram of a semiconductor device comprising the semiconductor memory device shown in Fig. 1 and a memory control device for controlling and generating an input signal to the semiconductor memory device, which are formed on one and the same semiconductor substrate;

Fig. 6 is a block diagram of a semiconductor device comprising the semiconductor memory device shown in Fig. 1 and a memory control device for controlling and generating an input signal to the semiconductor memory device, which are formed on one and the same semiconductor substrate;

Fig. 7 shows an arrangement of external terminals of the semiconductor memory device shown in Fig. 1;

Fig. 8 shows an arrangement of external terminals of the semiconductor memory device shown in Fig. 1;

Fig. 9 shows an arrangement of external terminals of the semiconductor memory device shown in Fig. 1;

Fig. 10 shows a correspondence between various commands determining operating functions of the semiconductor memory device shown in Fig. 1 and the external terminals;

Fig. 11 shows states of the external terminals showing a read command shown in Fig. 10;

Fig. 12 shows states of the external terminals showing a write command shown in Fig. 10;

Fig. 13 shows states of the external terminals showing a prefetch command shown in Fig. 10;

Fig. 14 shows states of the external terminals showing a prefetch command with auto precharge shown in Fig. 10;

Fig. 15 shows states of the external terminals showing a restore command shown in Fig. 10;

Fig. 16 shows states of the external terminals showing a restore command with auto precharge shown in Fig. 10;

Fig. 17 shows states of the external terminals showing an active command shown in Fig. 10;

Fig. 18 shows states of the external terminals showing a precharge command with auto precharge shown in Fig. 10;

Fig. 19 shows states of the external terminals showing a whole bank precharge command shown in Fig. 10;

Fig. 20 shows states of the external terminals showing a CBR refresh command shown in Fig. 10;

Fig. 21 shows states of the external terminals showing a device non-selection command shown in Fig. 10;

Fig. 22 shows states of the external terminals showing a non-operation command shown in Fig. 10;

Fig. 23 shows states of the external terminals showing a register setting command (1) shown in Fig. 10;

Fig. 24 shows states of the external terminals showing a register setting command (2) shown in Fig. 10;

Fig. 25 shows states of the external terminals showing a register setting command shown in Fig. 10;

Fig. 26 shows states of the external terminals showing a mode register setting command which is a portion of the register setting command shown in Fig. 10;

Fig. 27 shows an address sequence accessed correspondingly to respective lap times and burst lengths of data input/output mode;

Fig. 28 is a timing chart of data output having burst length of 4 and read latency of 2 at a read command input;

Fig. 29 is a timing chart of data output having burst length of 4 and write latency of 0 at a write command input;

Fig. 30 is a flowchart of an address assignment and data in a read command operation;

Fig. 31 is a flowchart of an address assignment and data in a write command operation;

Fig. 32 is a flowchart of an address assignment and data in a prefetch command operation;

Fig. 33 is a flowchart of an address assignment and data in a restore command operation;

Fig. 34 is a flowchart of an address assignment and data in an active command operation;

Fig. 35 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 36 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 37 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 38 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 39 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 40 is a layout of arrays schematically showing an array arrangement of a semiconductor memory device according to an embodiment of the present invention;

Fig. 41 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 42 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 43 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 44 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 45 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 46 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 47 schematically shows a whole layout of chips of a semiconductor memory device according to an embodiment of the present invention;

Fig. 48 schematically shows blocks which use a common power source of a semiconductor memory device according to an embodiment of the present

invention;

Fig. 49 schematically shows blocks which use a common power source of a semiconductor memory device according to an embodiment of the present invention;

Fig. 50 shows a wiring construction in a DRAM array portion of a semiconductor memory device according to an embodiment of the present invention;

Fig. 51 shows a wiring construction of a DRAM array portion, a data transfer portion and an SRAM array portion of a semiconductor memory device according to an embodiment of the present invention;

Fig. 52 shows a wiring construction of a DRAM array portion, a data transfer portion and an SRAM array portion of a semiconductor memory device according to an embodiment of the present invention;

Fig. 53 shows a wiring construction of a DRAM array portion, a data transfer bus line and an SRAM array portion of a semiconductor memory device according to an embodiment of the present invention;

Fig. 54 is a block diagram of an operation control circuit of the semiconductor memory device shown in Fig. 1;

Fig. 55 shows in detail a construction of the DRAM portion and the data transfer circuit shown in Fig. 1;

Fig. 56 shows in detail an example of the array construction of a DRAM array 110-1 of the whole layout which is an embodiment of the present invention shown in Fig. 41;

Fig. 57 shows in detail an example of a connecting relation between the transfer bus line and the bit lines for a portion (corresponding to 4 pairs of bit lines) of the layout shown in Fig. 56;

Fig. 58 is a circuit diagram showing the data transfer circuit in detail;

Fig. 59 shows an example of a construction for solving the problem of the example shown in Fig. 57;

Fig. 60 is a block diagram showing an example of a DRAM line control circuit;

Fig. 61 shows an example of a concrete construction of a DRAM row control circuit and a DRAM row decoder shown in Fig. 55;

Fig. 62 shows an example of a concrete circuit construction of a DRAM bit line selection circuit;

Fig. 63 shows an example of a concrete circuit construction of a DRAM bit line selection circuit;

Fig. 64 shows an example of a concrete circuit construction of a DRAM bit line selection circuit;

Fig. 65 shows an example of a concrete circuit construction of a DRAM bit line selection circuit;

Fig. 66 shows a relation between a pair of data transfer bus lines, the DRAM bit line selection circuit and the SRAM cells in the array layout shown in Fig. 36;

Fig. 67 shows signal waveforms showing an oper-

ation of the respective data transfer bus lines in Fig. 66;

Fig. 68 shows a concrete example of the SRAM portion and the data input/output terminals shown in Fig. 1;

Fig. 69 shows an example of a construction of the SRAM memory cell;

Fig. 70 is a concrete circuit of a flip-flop of the SRAM cell shown in Fig. 69;

Fig. 71 shows a concrete example of a connecting circuit for connecting the SRAM bit lines shown in Fig. 69;

Fig. 72 shows a concrete example of a connecting circuit for connecting the SRAM bit lines shown in Fig. 69;

Fig. 73 shows a concrete example of a connecting circuit for connecting the SRAM bit lines shown in Fig. 69;

Fig. 74 shows a concrete example of a SRAM row control circuit shown in Fig. 68;

Fig. 75 shows a concrete example of a SRAM column control circuit shown in Fig. 68;

Fig. 76 shows a concrete example of a multiplexer and latch circuit shown in Fig. 75;

Fig. 77 shows signal waveforms showing an operation of the multiplexer shown in Fig. 76;

Fig. 78 is a block diagram showing the SRAM row decoder, the data control circuit and the DRAM array shown in Fig. 1;

Fig. 79 shows signal waveforms showing an operation of the SRAM row decoder, the data control circuit and the SRAM array shown in Fig. 78;

Fig. 80 shows a concrete example of a construction of the SRAM portion and the data input/output terminal;

Fig. 81 shows a concrete construction in a case where a row redundancy line of the SRAM array portion;

Fig. 82 shows an example of a power source voltage supplied to the DRAM array portion and the SRAM array portion;

Fig. 83 shows an example of a power source voltage supplied to the DRAM array portion and the SRAM array portion;

Fig. 84 shows a result of simulation of dependency of write time to the SRAM cell on power source voltage;

Fig. 85 shows a concrete example of construction of the SRAM array portion realizing a temporary cell transfer function;

Fig. 86 shows signal waveforms showing an operation of the SRAM cell when, in Fig. 85, data of the SRAM cell is read out by performing the temporary cell transfer;

Fig. 87 shows signal waveforms showing an auto successive prefetch transfer function;

Fig. 88 shows a concrete example of the SRAM line control circuit for realizing a plural line successive

read/write function;

Fig. 89 shows a concrete example of a read out function of the plural row successive read/write function;

Fig. 90 is a correspondence table showing read(3) /write(3) command of a real time mode setting function and the state of the respective input terminals; Fig. 91 shows signal waveforms showing the real time mode setting function;

Fig. 92 schematically shows a construction of a memory array portion of a CDRAM;

Fig. 93 is a block diagram of a bi-directional transfer gate circuit of the CDRAM shown in Fig. 92;

Fig. 94 is a circuit diagram of the CDRAM bi-directional transfer gate circuit shown in Fig. 92;

Fig. 95 is a block diagram schematically showing the CDRAM;

Fig. 96 is a circuit diagram of the SRAM of the CDRAM shown in Fig. 95;

Fig. 97 is a block diagram schematically showing a construction of the CDRAM;

Fig. 98 is a circuit diagram of the SRAM block of the CDRAM shown in Fig. 97;

Fig. 99 is a block diagram schematically showing a construction of an EDRAM; and

Fig. 100 is a block diagram schematically showing a construction of the memory system having a plurality of processing devices.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

(1) Basic Construction

[0016] A basic construction of an embodiment of the present invention will be described.

[0017] A semiconductor integrated circuit device according to the present invention includes a semiconductor memory device and a control device of the semiconductor memory device. The semiconductor memory device includes a main memory portion and a sub memory portion and a bi-directional data transfer is possible between the main memory portion and the sub memory portion. The sub memory portion is constructed with a plurality of memory cell groups each being able to function as an independent cache memory. In the semiconductor memory device of the present invention, the number of control terminals and the number of address terminals can be the same as those necessary to control the main memory portion.

[0018] The semiconductor integrated circuit device will be described by taking an embodiment which has a synchronous interface having a $\times 8$ 2-bank construction including a 64-Mbit DRAM array as the main memory portion and a 16-Kbit SRAM array as the sub memory portion.

(2) Block Diagram

[0019] Fig. 1 is a block diagram schematically showing a construction of a whole semiconductor memory device according to an embodiment of the present invention. In Fig. 1, the semiconductor memory device 100 includes a dynamic RAM (DRAM) portion 101 as a main memory portion, a static RAM (SRAM) portion 102 as a sub memory portion and a bi-directional data transfer circuit 103 for data transfer between the DRAM portion 101 and the SRAM portion 102.

[0020] The DRAM portion 101 includes a DRAM array 110 having a plurality of dynamic memory cells arranged in a row and column matrix, a DRAM row control circuit 115 for generating a DRAM row selection signal and a bank selection signal from internal address signals iA0 ~ iA13, a DRAM row decoder 113 responsive to the DRAM row selection signals iADR0 ~ iADR12 and the bank selection signal iAD13 for selecting a corresponding row of the DRAM array 110, a DRAM column control circuit 116 for generating a DRAM column selection signal from the internal address signals iA5 and iA6 and a DRAM column decoder 114 responsive to the DRAM column selection signals iADC5 and iADC 6 for selecting a corresponding column. Further, the DRAM array 110 includes a memory cell portion 111 and a sense amplifier 112 for detecting and amplifying data held in the selected DRAM cell. Further, the DRAM array 110 is divided to a plurality of blocks called banks and, in this embodiment, to two banks A and B one of which is selected by the bank selection signal iAD13.

[0021] The SRAM portion 102 includes an SRAM array 120 having a plurality of static memory cells arranged in a row and column matrix, an SRAM row control circuit 124 for generating an SRAM row selection signal from the internal address signals iA0 ~ iA3, an SRAM row decoder 121 responsive to SRAM row selection signals iASR0 ~ iASR3 for selecting one of SRAM cell groups (in this embodiment, cell groups divided every row), an SRAM column control circuit 122 for generating an SRAM column selection signal from the internal address signals iA0 ~ iA3 and iA4 ~ iA13 and an SRAM column decoder 123 for selecting a column by SRAM column selection signals iASC4 ~ iASC10.

[0022] The semiconductor memory device 100 further includes an operation control circuit 150 for controlling an operation of the semiconductor memory device in response to an external input signal and a data control circuit 160 for controlling an external data input/output operation.

[0023] Although, in this embodiment, the DRAM and SRAM are used as the main memory portion and the sub memory portion, respectively, the present invention is not limited thereto. Instead of the DRAM, a memory such as SRAM, mask ROM, programmable ROM (PROM), erasable PROM (EPROM), electrically erasable PROM (EEPROM), flush EEPROM and ferroelectric

memory may be used as the main memory portion. The memory constituting the main memory portion is preferably constructed such that the kind and specific function thereof can be efficiently utilized. For example, in a case where a DRAM is used as the main memory portion, a usual DRAM, an EDODRAM, a synchronous DRAM, a synchronous GRAM, a burst EDODRAM, a DDR synchronous DRAM, a DDR synchronous GRAM, an SLDRAM or a RambusDRAM may be used. Further, any random access memory may be used as the sub memory portion provided that the memory allows access at higher speed than that of a memory used as the main memory portion. In a case where the main memory portion is constituted with a flush EEPROM, a memory capacity of the sub memory portion is preferably a half or more of a capacity of a unit erase sector of the flush EEPROM.

(3) System

[0024] The semiconductor memory device according to the present invention is provided with the SRAM column control circuit 122 and, therefore, an SRAM column control mode can be changed in SRAM cell group unit, as to be described in detail later. This function allows the setting of a lap time, a burst length and a latency, etc., (referred to as "data input/output mode", hereinafter) every SRAM cell group, so that the data input/output mode of each SRAM cell group is automatically determined within the semiconductor memory device when the SRAM cell group is selected, by preliminarily providing the setting. Therefore, there is no need of data control externally of the semiconductor memory device or an external data processing control for switching the data input/output mode.

[0025] The semiconductor memory device of the present invention has a function that, when it receives a plurality of access requests, the semiconductor memory device receives an allocation, assignment and/or re-assignment in SRAM cell group unit for every access request. Fig. 2 shows a memory system having a plurality of memory masters which perform access request to the semiconductor memory device 100 shown in Fig. 1. In Fig. 2, SRAM cell groups 01, 02 and 03 are assigned to an access request from a memory master 180a, SRAM cell group 04 is assigned to an access request from a memory master 180b and the SRAM cell groups 05, 06, 07 and 08 are assigned to an access request from a memory master 180c. The assignment of the SRAM cell groups to these access requests is variable and can be changed any time. Further, in Fig. 2, when the data input/output mode requested for the semiconductor memory device 100 by the memory master 180a is different from the data input/output mode requested for the semiconductor memory device by the memory master 180b, it is possible to perform the data input/output operation for the memory master 180a and the data input/output operation for the memory master

180b successively without using a special control signal. In order to realize such operation, the SRAM column control circuit 122 of the semiconductor memory device 100 includes a data input/output mode memory portion. The data input/output mode memory portion may have a 1:1 correspondence to the SRAM cell groups as shown in Fig. 2 or may correspond to a plurality of SRAM cell groups as shown in Fig. 3.

[0026] Figs. 4, 5 and 6 show a mixed semiconductor device 190 composed of the semiconductor memory device 100 and a memory control device 191 mounted on one and the same semiconductor substrate as that of the semiconductor memory device, for controlling and generating an input signal to the semiconductor memory device 100 according to an access request from the memory masters. Such mixed semiconductor device 190 may have a construction in which an input/output operation for all signals is performed through a memory control device as shown in Fig. 4, a construction in which an input/output operation is performed by the semiconductor memory device 100 directly as shown in Fig. 5 or a construction in which a data input/output operation is performed by the semiconductor memory device 100 through a data buffer 192 as shown in Fig. 6. However, the present invention is not limited to these constructions of the mixed semiconductor device 190. In the mixed semiconductor device 190, it becomes possible to automatically assign the SRAM cell group or groups to access requests from the respective memory masters in the system shown in Fig. 2 or 3 within the semiconductor device.

(4) Pin Arrangement

[0027] Fig. 7 shows an example of a pin arrangement of a package of the semiconductor memory device according to the present invention. The semiconductor memory device shown in Fig. 7 has a $\times 8$ -bit, 2-bank construction including a 64-Mbit DRAM array and a 16-Kbit SRAM array and a synchronous interface and is housed in a 54 pin TSOP type II plastic package of 400 mil $\times$ 875 mil with lead pitch of 0.8 mm. The number of pins and the pin arrangement of this pin construction are the same as those of a usual 64-Mbit synchronous DRAM. Further, the number of pins and the pin arrangement of a $\times 4$ -bit construction (Fig. 8), a $\times 16$ -bit construction (Fig. 9), a $\times 1$ -bit construction or a $\times 32$ -bit construction are the same as those of a corresponding synchronous DRAM, regardless of the number of banks.

[0028] Signals of the respective pins are defined as follows:

CLK: A clock signal CLK is a reference clock commonly used for all other input/output signals. That is, the clock signal CLK determines take-in timing of other input signals and output signal timing. A setup/hold time of each external signal is defined with reference to a rising edge of the clock CLK.

CKE: A clock enable signal CKE determines whether or not a CLK signal subsequent thereto is effective. When the CKE signal is HIGH at the rising edge of the CLK signal, the CLK signal is determined as being effective and, when it is LOW, the CLK signal is determined as being invalid.

/CS: A chip select signal /CS determines whether or not external input signals /RAS, /CAS, /WE are accepted. When the signal /CS is LOW at the leading edge of the signal CLK, the /RAS signal, the /CAS signal and the /WE signal which are input at the same timing are taken in the operation control circuit. When the signal /CS is HIGH at the leading edge of the CLK signal, the /RAS signal, the /CAS signal and the /WE signal input at the same timing are neglected.

/RAS, /CAS, /WE: The respective control signals /RAS, /CAS and /WE in combination determine the operation of the semiconductor memory device.

A0 ~ A13: Address signals A0 ~ A13 are taken in the address control circuit correspondingly to the clock signal, sent to the DRAM row decoder, the DRAM column decoder, the SRAM row decoder and the SRAM column decoder and used to select a cell of the DRAM portion and a cell of the SRAM portion. Further, the address signals are taken in a mode register to be described later, according to an internal command signal to set the data input/output mode of the internal operation. The address signal A13 is a bank selection signal of the DRAM cell array, too.

DQM: A data mask signal DQM functions to invalidate (mask) a data input and output in byte unit.

DQ0 ~ DQ7: Data signals DQ0 ~ DQ7 are input/output data signals.

(5) Basic Operation

[0029] A basic operation of the semiconductor memory device according to the present invention will be described. It should be noted that commands and the number of data are a mere embodiment and other combinations are possible arbitrarily.

[0030] Fig. 10 shows an example of various commands determining operation functions of the semiconductor memory device according to the present invention and states of the external input control signals. It should be noted, however, that any other combination of the various commands determining the operational functions of the semiconductor memory device and the states of the external input control signals can be used.

[0031] In Fig. 10, the states of the respective input control signals at a rising edge of a reference clock signal CLK and operations determined thereby are shown. A symbol "H" indicates a logical high level, "L" a logical low level and "x" an arbitrary level. Further, input control signals CKEn-1 in Fig. 10 shows a state of the input control signal CKE in a period of a reference clock just pre-

ceding to an aimed reference clock and the control signal CKE to be described for the respective commands is the CKEn-1. The commands shown in Fig. 10 will be described in sequence.

1. [Read Command]

[0032] Read command is to execute a data read operation from an SRAM cell.

[0033] As shown in Fig. 11, the states of the respective input control signals at the rising edge of the external clock signal are CKE = H, /CS = L, /RAS = H, /CAS = L and /WE = H. At the time when this read command is input, the addresses A0 ~ A3 and the addresses A4 ~ A10 are taken in as the SRAM row selection addresses and as the SRAM column selection addresses, respectively. Data at these addresses are output to DQ0 ~ DQ7 at a time delayed from the input of the read command by a latency.

[0034] When DQM = H with the clock set for the read command, the data output of the DQ0 ~ DQ7 are masked and are not output externally.

[0035] Fig. 30 shows an address signal and a data flow in an internal operation according to this read command. SRAM cells are selected by the row selection of the SRAM row decoder by the internal address signals iA0 ~ iA3 and the column selection of the SRAM column decoder by the SRAM selection signals iASC4 ~ iASC10 generated from the internal address signals iA4 ~ iA13. Data of the selected SRAM cells are output externally through the data amplifier in an assigned data input/output mode.

2. [Write Command]

[0036] The write command is to perform a write operation of data to the SRAM cell.

[0037] As shown in Fig. 12, the states of the respective input control signals at the rising edge of the external clock signal are CKE = H, /CS = L, /RAS = H, and /CAS = /WE = L. At the time when the write command is input, the addresses A0 ~ A3 are taken as SRAM row selection addresses and the addresses A4 ~ A10 are taken in as SRAM column selection addresses. As data to be written, the data of DQ0 ~ DQ7 is taken in at a time delayed from the input of the write command by a latency.

[0038] When DQM = H with the clock for data take-in of DQ0 ~ DQ7, the data output of the DQ0 ~ DQ7 are masked and are not taken inside.

[0039] Fig. 31 shows an address signal and a data flow in an internal operation according to this write command. SRAM cells are selected by the row selection of the SRAM row decoder by the SRAM row selection signals iASR0 ~ iASR3 generated from the internal address signals iA0 ~ iA3 and the column selection of the SRAM column decoder by the SRAM selection signal iASC4 ~ iASC10 generated from the internal address signals iASR0 ~ iASR3 and iA4 ~ iA13. The write data taken

from DQ0 ~ DQ7 is written in the selected SRAM cell through the write buffer.

[0040] As shown in Figs. 30 and 31, the read command and the write command perform the read and write regardless of the DRAM portion and the data transfer portion. Therefore, these commands can operate even when data transfer operation between SRAM cell groups other than the SRAM row selected for the data input/output and the DRAM portion and/or the operation inside the DRAM portion still continues. On the contrary, even if the read command or the write command is operated, it is possible to operate by commands of data transfer operation between SRAM cell groups other than the SRAM row selected for the data input/output and the DRAM portion and/or the operation inside the DRAM portion.

3. [Prefetch Command]

[0041] The prefetch command is to perform a data transfer from a DRAM cell group to an SRAM cell group.

[0042] As shown in Fig. 13, the states of the respective input control signals at the rising edge of the external clock signal are CKE = H, /CS = L, /RAS = /CAS = H and /WE = L. Further, A10 = L and A9 = L. At the time when the prefetch command is input, the addresses A0 ~ A3 are taken as SRAM row selection addresses, the addresses A4 ~ A6 are taken in as SRAM column selection addresses and A13 is taken in as a bank selection address of the DRAM array. In this embodiment, the bank A is selected.

[0043] Fig. 32 shows an address signal and a data flow in an internal operation according to this prefetch command. Among DRAM cell groups already selected by an active command to be described later, an SRAM cell in a bank assigned by iA13 is selected. In this embodiment, the bank A is selected. Bit lines of the DRAM cell group assigned by the addresses iA5 and iA6. Data of the bit lines is amplified by the sense amplifier at the time of the active command and the data of the selected bit lines is transmitted to a data transfer bus line through the data transfer circuit. The cells on the row of the SRAM selected by the addresses iA0 ~ iA3 stop the holding of the previous data, take in the data on the data transfer bus line and hold data transferred thereafter. An output from the sense amplifier through the data transfer circuit to the data transfer line is stopped after the data transfer.

[0044] In this embodiment, the number of data transferred by the prefetch command at once is 128×8 .

4. [Prefetch Command with Auto Precharge]

[0045] The prefetch command with auto precharge is to transfer data from the DRAM cell group to the SRAM cell group and to automatically precharge the DRAM portion after data transfer.

[0046] As shown in Fig. 14, the states of the respective

input control signals at the rising edge of the external clock signal are CKE = H, /CS = L, /RAS = /CAS = H and /WE = L. Further, A10 = H and A9 = L. Similarly to the above mentioned prefetch command, the addresses A0 ~ A3 are taken as SRAM row selection addresses, the addresses A5 and A6 are taken in as DRAM column selection addresses and A13 is taken in as a bank selection address of the DRAM array at the time when the prefetch command with auto precharge is input.

[0047] Address signals in an internal operation and data flow caused by the prefetch command with auto precharge will be described. Among DRAM cell groups already selected by the active command to be described later, an SRAM cell in a bank assigned by iA13 is selected. Bit lines of the DRAM cell group assigned by the addresses iA5 and iA6. Data of the bit lines is amplified by the sense amplifier at the time of the active command and the data of the selected bit lines is transmitted to a data transfer bus line. The cells on the row of the SRAM selected by the addresses iA0 ~ iA3 stop the holding of the previous data, take in the data on the data transfer bus line and hold data transferred thereafter. An output from the sense amplifier through the data transfer circuit to the data transfer line is stopped after the data transfer. After a predetermined time from the stoppage of output to the data transfer bus line, the word line is made in non-selection state and the internal operation (potential equilibration of the bit line and the sense amplifier) to be described for the precharge command is performed. After a predetermined time from the input of the prefetch command with auto precharge, the DRAM is automatically made in a precharge (non selection) state.

5. [Restore Command]

[0048] The restore command is to perform a data transfer from the SRAM cell group to the DRAM cell group. As shown in Fig. 15, this command is a continuous input command extending over the external clock signals CLK1 and CLK2.

[0049] The states of the respective input control signals at the rising edge of the external clock signal shown in Fig. 15 are CKE = H, /CS = L, /RAS = /CAS = H and /WE = L. Further, A10 = L and A9 = H. At the rising edge of the first external clock signal CLK1, the addresses A0 ~ A3 are taken as SRAM row selection addresses and the addresses A5 and A6 are taken in as DRAM column selection addresses and, at the rising edge of the second external clock signal CLK2, addresses A0 ~ A12 are taken in as bank selection addresses of the DRAM array which is a destination of transfer. The addresses A13 are taken in as the bank selection addresses of the DRAM array at the rising edges of the CLK1 and CLK2. The A13 addresses input by the CLK1 and CLK2 must be identical.

[0050] Fig. 33 shows address signals in an internal operation and data flow caused by this restore command. Internal address signals iA0 ~ iA12 shown in

Fig. 33 are internal address data at the time of the first clock CLK1 and internal address signals i2A0 ~ i2A12 are internal address data at the time of the second clock CLK, data of identical internal address signal line being shown for each clock. Data of SRAM cell group selected by the addresses i1A0 ~ i1A3 generated from the address at the first clock CLK1 is transferred to a data transfer bus line of a bank selected by the address iA13. Thereafter, the data of the data transfer bus line is transferred to bit lines of the DRAM selected by the addresses i1A5 and i1A6. Thereafter, word lines of the DRAM are selected by the addresses i2A0 ~ i2A12 and iA13 are selected and data of the cell groups on the selected word lines are output to corresponding bit lines, respectively. Sense amplifiers corresponding to the bit lines of the DRAM detect and amplify the data of the DRAM cell groups output to the bit lines, respectively. The sense amplifiers corresponding to the bit lines selected by the addresses i1A5 and i1A6 detect and amplify write data transmitted from the data transfer bus line. A data output through the data transfer bus line to the bit lines of the DRAM is stopped after the word line is raised.

[0051] In this embodiment, the number of data transferred at once is 128×8 .

6. [Restore Command with Auto Precharge]

[0052] The restore command with auto precharge is to perform a data transfer from an SRAM cell group to a DRAM cell group and to automatically perform a precharge of the DRAM portion after the data transfer.

[0053] As shown in Fig. 16, the states of the respective input control signals at the rising edges of the external clock signal CLK1 and CLK2 are $\text{CKE} = \text{H}$, $\text{/CS} = \text{L}$, $\text{/RAS} = \text{/CAS} = \text{H}$ and $\text{/WE} = \text{L}$ and, further, $\text{A10} = \text{H}$ and $\text{A9} = \text{H}$. At the rising edge of the first external clock signal CLK1, the addresses A0 ~ A3 are taken as SRAM row selection addresses and the addresses A5 and A6 are taken in as DRAM column selection addresses and, at the rising edge of the next, second external clock signal CLK2, addresses A0 ~ A12 are taken in as selection addresses of the DRAM array which is a destination of transfer. The addresses A13 are taken in as the bank selection addresses of the DRAM array at the rising edges of the CLK1 and CLK2. The A13 addresses input by the CLK1 and CLK2 must be identical.

[0054] Address signals in an internal operation and data flow caused by this restore command with auto precharge will be described. Data of the SRAM cell group selected by the addresses i1A0 ~ i1A3 generated from the addresses at the time of the first clock CLK1 is transmitted to the data transfer bus line of the bank selected by the address iA13. Thereafter, the data of the data transfer bus line is transmitted to the bit line of the DRAM selected by the addresses i1A5 and i1A6. Thereafter, word lines of the DRAM are selected by the addresses i2A0 ~ i2A12 and iA13 generated by the addresses at the time of the next clock CLK2 and data of the cell

groups on the selected word lines are output to corresponding bit lines. The sense amplifiers corresponding to the respective bit lines detect and amplify data of the DRAM cell group output to the bit lines and the sense amplifiers corresponding to the bit lines selected by the addresses i1A5 and i1A6 detect and amplify write data transferred from the data transfer bus line. The output to the bit lines of the DRAM through the data transfer bus line is stopped after the word line is raised. The word line is made in non-selection state after a predetermined time therefrom and an internal operation (equilibration of the bit line and the sense amplifier) indicated by a precharge command to be described later is performed. After a predetermined time from the command, the DRAM automatically becomes in a precharge (non-selection) state.

7. [Active Command]

[0055] The active command is to activate a bank selected from the DRAM array.

[0056] As shown in Fig. 17, the states of the respective input control signals at the rising edges of the external clock signal CLK are $\text{CKE} = \text{H}$, $\text{/CS} = \text{/RAS} = \text{L}$, $\text{/CAS} = \text{/WE} = \text{H}$. An address A13 at the input time of this active command is taken in a bank selection address of the DRAM and addresses A0 ~ A12 are taken in as row selection address of the DRAM.

[0057] Fig. 34 shows address signals in an internal operation caused by the active command and data flow. In the bank selected by the address iA13, the word lines of the DRAM are selected by the addresses iA0 ~ iA12. Data of the DRAM cell groups on the selected word lines are output to bit lines connected thereto and the sense amplifiers corresponding to the respective bit lines detect and amplify the data of the DRAM cell groups output to the bit lines. In this embodiment, the number of data transferred at once is 512×8 .

[0058] In a case where another word line selection is to be performed with respect to a bank which is already activated, it is necessary to make the bank in a precharge state and then to newly input an active command.

[0059] This command corresponds to a case where a /RAS signal of a usual DRAM is made LOW.

8. [Precharge Command]

[0060] The precharge command is to precharge (inactivation) of a bank selected from a DRAM array.

[0061] As shown in Fig. 18, the states of the respective input control signals at the rising edges of the external clock signal CLK are $\text{CKE} = \text{H}$, $\text{/CS} = \text{/RAS} = \text{L}$, $\text{/CAS} = \text{H}$ and $\text{/WE} = \text{L}$. When, at an input of the precharge command, $\text{A10} = \text{L}$ and $\text{A13} = \text{valid data}$, a bank assigned by data of the address A13 is precharged (non-selection). The bank is selected at the active command input prior to this precharge and, when there is no

active command input to the bank assigned by this precharge command prior to the input of the latter command thereto, the precharge command is invalid.

[0062] Address signals in an internal operation caused by the precharge command and data flow will be described.

[0063] Bit line potential and sense amplifier potential are equilibrated by making a word line of a DRAM whose bank selected by the address iA13 is activated in non-selection state. After an operation of the precharge command completes, the selected bank becomes ready to receive a next active command.

[0064] The precharge command corresponds to a case where a RAS signal of a usual DRAM is made HIGH.

9. [All Bank Precharge Command]

[0065] The all bank precharge command is to precharge (inactivation) all banks of a DRAM array. With this command, the DRAM portion is set to a precharge state and the active state of all banks can be ended.

[0066] As shown in Fig. 19, the states of the respective input control signals at the rising edges of the external clock signal CLK are CKE = H, /CS = /RAS = L, /CAS = H and /WE = L. Further, A10 = H.

[0067] Address signals in an internal operation caused by the precharge command and data flow will be described.

[0068] Bit line potential and sense amplifier potential are equilibrated by making all word lines of a selected DRAM in non-selection state. After an operation of this command is completed, all banks become ready to receive a next active command input.

[0069] The all bank precharge command corresponds to a case where a /RAS signal of a usual DRAM is made HIGH.

10. [CBR Refresh Command]

[0070] The CBR refresh command is to refresh cell data of a DRAM portion. Address signal necessary for refresh is automatically generated internally.

[0071] As shown in Fig. 20, the states of the respective input control signals at the rising edges of the external clock signal CLK are CKE = H, /CS = /RAS = /CAS = L and /WE = H.

[0072] Address signals in an internal operation caused by the CBR refresh command and data flow will be described.

[0073] Addresses iA0 ~ iA12 and iA13 are automatically generated internally. A bank is selected by the internally generated address iA13, word lines of a DRAM are selected by the internally generated addresses iA0 ~ iA12, DRAM cell groups on the selected word lines output their data to corresponding bit lines, respectively. Sense amplifiers corresponding to the respective bit lines detect and amplify the data of the DRAM cell

groups output to the bit lines. The data detected and amplified by the sense amplifiers are written in the DRAM cell groups again through the bit lines. After a predetermined time from the re-write of the data, the word lines are made non-selection state to equilibrate the bit line and sense amplifiers potential, completing a refresh operation.

11. [Non-Operation Command]

[0074] Non-operation commands of CKE = H, /CS = L, /RAS = /CAS = /WE = H shown in Fig. 21 are not execution commands.

12. [Device Non-Selection Command]

[0075] Device non-selection commands of CKE = H, /CS = H shown in Fig. 22 are not execution commands.

13. [Register Setting Command]

[0076] The register setting command is to set setting data in various operation modes in a register.

[0077] As shown in Figs. 23 and 24, the states of the respective input control signals at the rising edges of the external clock signal CLK are CKE = H, /CS = /RAS = /CAS = /WE = L. At a time of input of this command, valid data of the addresses A0 ~ A13 are taken in as setting data of operation modes. An input of register setting by this command is necessary in order to initialize a device after a power source is connected.

[0078] Fig. 25 shows an operation by address data at the register setting command.

[0079] Portions of register setting commands (a), (b), (c) and (d) shown in Fig. 25 are input by one clock shown in Fig. 23 and another portion of the register setting command (d) to be described later is input by two clocks shown in Fig. 24.

[0080] The register setting command (a) in Fig. 25 is a test set of a refresh counter, which is similar to that of a usual synchronous DRAM. This address set is selected at an input of A7 = L and A8 = L.

[0081] The register setting command (b) in Fig. 25 is an unused set. This address set is selected at an input of A7 = L and A8 = H.

[0082] The register setting command (c) in Fig. 25 is a device test set. This address set is selected at an input of A7 = H and A8 = H.

[0083] The register setting command (d) in Fig. 25 is a mode register setting set. This address set is selected at an input of A7 = L and A8 = L and various data input/output modes to be described later are set. A mode register stores data input/output modes of the respective SRAM cell groups of the sub memory portion.

[0084] Fig. 26 is a list of detailed setting items of the mode register setting.

[0085] A mode register setting (1) command is to switch between a latency mode and an input/output ad-

dress sequence (lap type). This command is input by one clock of an external clock signal such as shown in Fig. 23. This address set is selected when A6 = L, A7 = L and A8 = L.

[0086] The latency mode setting is made by data of A1, A2 and A3 input simultaneously and the input/output sequence (lap type) is set by data of A0. The latency mode is set to latency = 2 when A1 = L, A2 = H and A3 = L and, otherwise, becomes non-setting or unused state. The input/output address sequence (lap type) is set to sequential when A0 = L and to interleave when A0 = H.

[0087] The mode register setting (2) command is an address data set for setting a burst length of every selected row of the SRAM and, in order to input the row assignment of the SRAM and the burst length data, is continuously input over two clocks of the external clock signal as shown in Fig. 24. This address set is selected when A6 = H, A7 = L and A8 = L.

[0088] An SRAM cell group is selected by data of A1, A2 and A3 of the first clock CLK1 and the burst length of the selected cell group is set by data of A3, A4 and A5 of the next clock CLK2. The burst length is set to 1 when A3 = L, A4 = L and A5 = L, to 2 when A3 = H, A4 = L and A5 = L, to 4 when A3 = L, A4 = L and A5 = L, to 8 when A3 = H, A4 = H and A5 = L and to 16 when A3 = L, A4 = L and A5 = H.

[0089] Various data input/output modes will be described briefly.

[0090] Burst Length: burst length represents the number of data continuously input/output by an input of read command or write command. The continuous data input/output is performed on the basis of a clock signal. Fig. 27 shows a timing of the respective signals for data read, in which the burst length is 4. That is, when the read command is input at CLK0, four data are successively output at CLK2, CLK3, CLK4 and CLK5. Fig. 28 shows a timing of the respective signals for data write. Since the burst length is 4, when the write command is input at CLK0, four data are successively taken in at CLK0, CLK1, CLK2 and CLK3.

[0091] Latency: latency represents a waiting time from the input time of a read command or write command to a time at which data input/output becomes possible by the number of clocks. Fig. 27 shows a timing of respective signals at the data read. In this embodiment, the latency at data read is 2. That is, when a read command is input at CLK0, output of data to a DQ terminal is started at CLK2. Fig. 28 shows a timing of the respective signals at a data write. In this embodiment, the latency at data write is 0. That is, when the write command is input at CLK0, the data take-in from the DQ terminal is started simultaneously with the CLK0 input.

[0092] Lap Type: Lap type (input/output address sequence) determines an address sequence of data input/output when data is input/output successively for a time corresponding to a set burst length and includes sequence and interleave. Fig. 29 shows address sequenc-

es of data for the respective sequence and interleave.

[0093] As another operation, there is a function control by control of the clock enable signal CKE, as in the usual synchronous DRAM.

[0094] A portion of the operation of the semiconductor memory device according to the present invention will be described.

[0095] Read operation when there is an externally assigned data in the SRAM portion: as shown in Fig. 30, data assigned by only read command is output externally through a data amplifier.

[0096] Read when there is no externally assigned data in the SRAM portion: after the active command shown in Fig. 34 is completed, the prefetch command shown in Fig. 32 is executed and the assigned data is transferred to the SRAM portion. Then, the assigned data is externally output through the data amplifier by the read command shown in Fig. 30.

[0097] Read when there is no externally assigned data in the SRAM portion and there is a write data which is not restored as yet: the write data is transferred to the DRAM portion by the restore command shown in Fig. 33. Thereafter, the active command shown in Fig. 34 and the prefetch command shown in Fig. 32 are executed and the assigned data is transferred to the SRAM portion. Then, the assigned data is output externally through the data amplifier by the read command shown in Fig. 30.

(6) Layout

1. [Array Layout]

[0098] Fig. 35 is an array layout schematically showing an array arrangement of the semiconductor memory device according to an embodiment of the present invention.

[0099] In the construction of the array arrangement shown in Fig. 35, the whole DRAM array is divided to a DRAM array 110-1 and a DRAM array 110-2 and an SRAM array 120 and an SRAM column decoder 123 are provided between the DRAM arrays. Thus, it is possible to transfer data between the cell groups on any DRAM selected by the DRAM row decoder 113 adjacent to the DRAM arrays 110-1 and 110-2 and the cell groups on a certain row of the SRAM selected by the SRAM row decoder 121 and a direct mapping system and a mapping system of set associative system become possible.

[0100] The data transfer bus lines for transferring data are arranged such that these lines traverse the DRAM array 110-1, the DRAM array 110-2, the SRAM array 120 and the SRAM column decoder 123.

[0101] In this embodiment, the DRAM array 110-1 and the DRAM array 110-2 correspond to the banks A and B, respectively.

[0102] Fig. 50(1) is a plan view of a wiring in the DRAM array portion of this construction and Fig. 50(2) is a hierarchical view of the wiring in the DRAM array portion

in a cross sectional direction. A data transfer bus line TBL is formed by an upper wiring layer than those of the word lines DWL, the bit lines DBL and a wiring which is used for the sense amplifiers although not shown. As in the conventional DRAM, the column selection signal does not exist in an upper portion of the DRAM cells and the data transfer bus lines TBL are arranged therein. An operation corresponding to the column selection of the usual DRAM is performed by selectively connecting the bit lines and the data transfer bus lines by bit line selector switches DBSW. In this embodiment, one of four pairs of bit lines is selected and connected to the data transfer bus line pair. The wiring of the bit line selection signal is arranged such that it traverses the data transfer lines and the bit lines. The data transfer bus lines are arranged in parallel to the bit lines in the upper cell portion in the cell array of the DRAM portion and perpendicular to the word lines. In Fig. 50, the connection between the data transfer bus lines and the SRAM array is omitted.

[0103] Fig. 36 shows another construction which, in addition to the construction shown in Fig. 35, selector circuits 131 are provided between the DRAM arrays 110-1 and 110-2 and the SRAM array 120 so that the data transfer bus line can be selectively connected therethrough. With this construction, it is possible to disconnect the data transfer bus line of the DRAM array on the non-operational side by using a signal for selecting one of the DRAM arrays 110-1 and 110-2, resulting in a reduction of charging/discharging current during a data transfer and an improvement of data transfer speed.

[0104] Figs. 51(1) and 51(2) are a plan view of a wiring in the DRAM array portion of this construction and a hierarchical view of the wiring in the DRAM array portion in a cross sectional direction, respectively. The data transfer bus line is divided every DRAM array to a first data transfer bus line TBLA and a second data transfer bus line TBLB and one of the data transfer bus lines TBLA and TBLB is selected by the data transfer selector circuit 131. In this figure, the bit line selector switch and bit lines connected to the data transfer lines are omitted.

[0105] Similarly to Fig. 35, in this embodiment, the DRAM array 110-1 and the DRAM array 110-2 correspond to the banks A and B, respectively. Therefore, in this construction, when data is transferred between a certain bank and the SRAM portion immediately after the data transfer between the other bank and the SRAM portion is performed, that is, when a bank ping-pong operation is performed, it is possible to disconnect a load of the data transfer bus on one side when the bank assignment is performed and thus an interval of successive operations during the bank ping-pong operation is not limited by the operating frequency of the data transfer bus line of the DRAM array portion.

[0106] It may be possible to further divide the DRAM array finely and provide a selector circuit for connecting them to the data transfer bus lines. Further, it may be possible to divide the SRAM array more finely and pro-

vide a selector circuit for connecting them to the data transfer bus lines.

[0107] Fig. 37 shows another example of the array layout of the semiconductor memory device to which the present invention is applied.

[0108] The construction shown in Fig. 37 differs from that shown in Fig. 35 in that the DRAM array is not divided and the SRAM array and the SRAM column decoder are provided adjacent to both sides of the DRAM array, respectively. With this construction, it is possible to shorten a distance between the SRAM portion and the data control circuit and a distance between the data control circuit and the data input/output terminals DQ and hence speed up the read or write operation. In this example, it is also possible to transfer data between the cell groups on any row of the DRAM selected by the DRAM row decoder 113 adjacent to the DRAM array 110 and the cell groups on a certain row of the SRAM selected by the SRAM row decoder 121 and a direct mapping system and a mapping system of set associative system become possible.

[0109] The data transfer bus lines for transferring data are arranged such that these lines traverse the DRAM array 110-1, the DRAM array 110, the SRAM array 120. In this embodiment, the banks A and B exist in mixed state in the DRAM array 110.

[0110] Fig. 38 shows an layout when the DRAM array in Fig. 37 is divided. In this layout, the data transfer bus line is divided in order to make the connection between the DRAM arrays and the SRAM array 120 through the data transfer selection circuit 131 by using a wiring layer different from the data transfer bus lines. In this embodiment, the connection line between the data transfer selection circuit 131 and the SRAM array is a global data transfer bus line GTL.

[0111] Figs. 52(1) and 52(2) are a plan view of a wiring in the DRAM array portion of this construction and a hierarchical view of the wiring in the DRAM array portion in a cross sectional direction, respectively. In Fig. 52, the data transfer bus line is divided to a first data transfer bus line TBLA and a second data transfer bus line TBLB and one of the data transfer bus line TBLA and TBLB is selected by the data transfer selection circuit 131 and connected to the global data transfer bus line GTL. Since the global data transfer bus line GTL is connected to the SRAM array 120, it is possible to mutually transfer data between the DRAM and the SRAM. Although the DRAM array is divided by two in this embodiment, it is possible to divide the DRAM more finely. Fig. 53 shows an example in which the DRAM array is divided finely. This construction has the features of the layouts shown in Figs. 36 and 38. In Fig. 53, the DRAM array is divided by four and it is possible to transfer data between the DRAM and the SRAM by performing the selection of the data transfer bus lines by the first data transfer selector circuits 132 and the selection of the global data transfer bus lines GTL by the second data transfer selector circuits 133, making the direct mapping system and a map-

ping system of set associative system possible. The DRAM array can be divided more finely. In such case, the data transfer bus lines and the first data transfer selector circuits are connected in parallel to the global data transfer bus lines.

[0112] Fig. 39 shows another example of the array layout of the semiconductor memory device to which the present invention is applied.

[0113] In Fig. 39, wiring layers which are different from the data transfer bus lines shown in Fig. 36 or 38 are used. The wiring for connecting data transfer bus lines arranged on the DRAM array to the SRAM array is formed in a wiring layer which is different from that for the data transfer bus lines. In Fig. 39, the SRAM array and the SRAM column decoder are provided adjacent to the DRAM row decoder. In this example, it is also possible to transfer data between the cell groups on any row of the DRAM selected by the DRAM row decoder 113 adjacent to the DRAM array 110 and the cell groups on a certain row of the SRAM selected by the SRAM row decoder 121 adjacent to the SRAM array 120, making the direct mapping system and a mapping system of set associative system possible.

[0114] As shown in Fig. 40, the data transfer bus lines are not always necessary to arrange adjacent to the DRAM row decoder and the position in which the SRAM array, the SRAM column decoder and the SRAM row decoder are arranged is not limited so long as the DRAM array and the SRAM array are connected such that a mutual data transfer therebetween is possible.

[0115] In a case where bus lines such as the data transfer bus lines and the global data transfer bus lines are formed as different wiring layers, these bus lines may be constructed with different wiring layers by combining, in addition to the usual metal wiring, polysilicon wiring, polycide wiring, silicide wiring and/or high melting point metal wiring, etc. In such case, the combination of them is optimized by taking wiring resistance and limitation in process into consideration. For example, a combination of (the first layer of aluminum wiring and the second layer of aluminum wiring) or a combination of (the first layer of tungsten silicide wiring and the second layer of aluminum wiring) may be considered.

2. [Overall Layout]

[0116] Fig. 41 shows an overall chip layout of an embodiment of the semiconductor memory device to which the present invention is applied. The semiconductor memory device shown in Fig. 41 includes a 64-Mbit DRAM array of $\times 8$ -bit, 2-bank construction as the main memory portion, a 16-Kbit SRAM array as a sub memory portion and a synchronous interface. However, it is possible to construct the semiconductor memory device in other ways.

[0117] A cross shape area including a vertical center portion and a lateral center portion is provided as shown in Fig. 41. DRAM arrays 110-1, 110-2, 110-3 and 110-4

each having a memory capacity of 16 Mbits are arranged in four areas divided by the cross shape area, respectively. An overall memory capacity of the DRAM arrays 110-1, 110-2, 110-3 and 110-4 is 64 Mbits. DRAM row decoders 113 are provided adjacent to lower portions of the DRAM arrays 110-1 and 110-2, respectively. Similarly, DRAM row decoders 113 are arranged adjacent to upper portions of the DRAM arrays 110-3 and 110-4, respectively. An SRAM array 120-1, an SRAM row decoder 121 and an SRAM column decoder 123 are arranged between the DRAM arrays 110-1 and 110-2. Similarly, an SRAM array 120-2, an SRAM row decoder 121 and a column decoder 123 are arranged between the DRAM arrays 110-3 and 110-4. The data transfer bus line traverses the DRAM array 110-1, the SRAM array 120 and the DRAM array 110-2 such that the data transfer between selected DRAM cell groups and a selected SRAM cell group is possible. Similarly, the data transfer bus line traverses the DRAM array 110-3, the SRAM array 120 and the DRAM array 110-4 such that selected DRAM cell groups and a selected SRAM cell group is possible.

[0118] An operation control circuit and a data control circuit, etc., are arranged in other portions of Fig. 41. Although other arrangement may be possible, an input/output signal terminal is arranged in the lateral center portion in the shown embodiment.

[0119] In Fig. 41, the main memory portion has the 2-bank construction having a layout in which portions which are selected simultaneously are not concentrated in a portion so that, when the bank A is selected, the DRAM arrays 110-1 and 110-4 are selected simultaneously and, when the bank B is selected, the DRAM arrays 110-2 and 110-3 are selected simultaneously. That is, as shown in Fig. 48, the arrangement of the DRAM arrays is constructed such that a load on an internal power source wiring VCC and an internal ground wiring GND, etc., is not one sided. It is, of course, possible to use the DRAM arrays 110-1 and 110-3 as the bank A and the DRAM arrays 110-2 and 110-4 as the bank B, to increase the number of division to thereby disperse areas to be selected simultaneously or reduce areas to be selected simultaneously.

[0120] Fig. 42 shows an overall chip layout of another embodiment of the semiconductor memory device to which the present invention is applied. DRAM arrays 110-1, 110-2, 110-3 and 110-4 are arranged in divided four areas, respectively. The DRAM arrays 110-1, 110-2, 110-3 and 110-4 each having a memory capacity of 16 Mbits and grouped in banks A and B provide a total memory capacity of 64 Mbits. DRAM row decoders 113 are provided adjacent to lower portions of the DRAM arrays 110-1 and 110-2, respectively. Similarly, DRAM row decoders 113 are arranged adjacent to upper portions of the DRAM arrays 110-3 and 110-4, respectively. Between the DRAM arrays 110-1 and 110-2 and between the DRAM arrays 110-3 and 110-4, SRAM arrays 120-1, 120-2, 120-3 and 120-4, SRAM row decoders 121 and

SRAM column decoders 123 are arranged, respectively. Although, in Fig. 42, the SRAM column decoders 123 are shown as one block for the SRAM arrays on both sides, it is possible to provide one SRAM column decoder 123 for each SRAM array. The data transfer bus line for exchanging data between a selected DRAM cell group and a selected SRAM cell group traverses the DRAM array 110-1 and the SRAM array 120-1 such that the data transfer between them is possible. Similarly, the data transfer bus line is provided between other DRAM arrays and other SRAM arrays.

[0121] An operation control circuit and a data control circuit, etc., are arranged in other portions of Fig. 42. Although other arrangement may be possible, an input/output signal terminal is arranged in the lateral center portion in the shown embodiment.

[0122] Fig. 43 shows an overall chip layout of another embodiment of the semiconductor memory device to which the present invention is applied. DRAM arrays 110-1, 110-2, 110-3 and 110-4 are arranged in divided four areas, respectively. The DRAM arrays 110-1, 110-2, 110-3 and 110-4 each having a memory capacity of 16 Mbits and grouped in banks A and B provide a total memory capacity of 64 Mbits. DRAM row decoders 113 are provided adjacent to upper or lower portions of the DRAM arrays 110-1 and 110-2, respectively. Similarly, SRAM arrays 120, SRAM row decoders 121 and SRAM column decodes 123 corresponding to the respective DRAM arrays 110 are arranged adjacent to the DRAM row decoders 113. The data transfer bus line for exchanging data between a selected DRAM cell group and a selected SRAM cell group traverses the DRAM arrays and are connected to the SRAM arrays through a wiring layer difference from that of the data transfer bus line.

[0123] An operation control circuit and a data control circuit, etc., are arranged in other portions of Fig. 43.

[0124] Fig. 44 shows an overall chip layout of another embodiment of the semiconductor memory device to which the present invention is applied. In Fig. 44, the arrangement of the SRAM arrays, the SRAM row decoders and the SRAM column decoders shown in Fig. 43 is changed. However, this arrangement may be further changed so long as the data transfer between a selected DRAM cell group and a selected SRAM cell group is possible.

[0125] Fig. 45 shows an overall chip layout of another embodiment of the semiconductor memory device to which the present invention is applied. In Fig. 45, two of the layout construction shown in Fig. 41 are combined by more finely dividing the main memory portion and the sub main memory portion. The layout may be constructed by combining a number of constructions each shown in Fig. 41 or by using a combination of the constructions each shown in Fig. 42.

[0126] Incidentally, the main memory portion shown in Fig. 45 is of 2-bank construction in which the portions selected simultaneously are not concentrated to portions of the banks A and banks B. Therefore, as shown

in Fig. 49, the arrangement of the DRAM arrays is constructed such that a load on an internal power source wiring VCC and an internal ground wiring GND, etc., is not one sided. It is, of course, possible to disperse or reduce areas to be selected simultaneously.

[0127] Fig. 46 shows an overall chip layout of another embodiment of the semiconductor memory device to which the present invention is applied. In Fig. 46, the data transfer bus lines extend vertically contrary to Fig. 45. Although the DRAM row decoder and the SRAM row decoder are shown in Fig. 46 as one block for the DRAM array and the SRAM array on both sides, the DRAM row decoder may be provided for each DRAM array and the SRAM row decoder may be provided for each SRAM array.

[0128] Further, the banks on both sides of the DRAM row decoder may be connected through a common data transfer bus line as shown in Fig. 47.

(7) Detailed Description of the Respective Blocks

[0129] The respective circuit blocks of the overall block diagram shown in Fig. 1 will be described in detail. It should be noted that the following description is for a mere embodiment and this invention is not limited thereto.

1. {Operation Control Circuit}

[0130] Fig. 54 is a circuit diagram of the operation control circuit 150.

[0131] The operation control circuit 150 is constructed with an internal clock generator circuit 410, a command decoder 420, a control logic 430, an address control circuit 440 and a mode register 450.

[0132] The internal clock generator circuit 410 generates an internal clock signal iCLK from the external input signals CLK and CKE.

[0133] The internal clock signal ICLK is supplied to the command decoder 420, the control logic 430, the address control circuit 440 and the data control circuit to control the timing of the respective portions.

[0134] The command decoder 420 includes a buffer 421 for receiving the respective input signals and a command judge circuit 422. The /CS signal, the /RAS signal, the /CAS signal and the /WE signal are transmitted to the command judge circuit 421 in synchronism with the internal clock signal ICLK to generate an internal command signal iCOM. The command generator circuit 421 responds to the respective input signals in manners indicated in a correspondence table of the commands and the respective input terminal states as shown in Fig. 10.

[0135] The control logic 430 responds to the internal command signal iCOM, the internal clock signal ICLK and the register signal iREG to generate the control signal necessary to perform operations assigned by these signals. The control logic 430 includes a DRAM control circuit 431, a transfer control circuit 432 and an SRAM

control circuit 433 which generate respective control signals.

[0136] The register 450 functions to hold data defined by a combination of data of a specific address input when it receives a specific register write signal from the command judge circuit and holds the data until a register write signal is input again. The data held in the register is referenced when the control logic 430 operates.

2. {DRAM Portion}

[DRAM Portion and Data Transfer Circuit]

[0137] Fig. 55 shows a concrete construction of the DRAM portion and the data transfer circuit shown in Fig. 1.

[0138] In Fig. 55, the DRAM portion 101 includes a plurality of dynamic memory cells DMC arranged in a matrix. Each memory cell DMC includes a memory transistor N1 and a memory capacitor C1. A constant potential V_{gg} (1/2V_{cc}, etc.) is applied to one terminal of the memory capacitor C1. Further, the DRAM portion 101 includes DRAM word lines DWL to which the DRAM cells DMC are connected in rows and DRAM bit lines DBL to which the DRAM cells DMC are connected in columns. Each bit line is paired with a complementary bit line. The DRAM cells DMC are positioned at cross points of the word lines DWL and the bit lines DBL, respectively. The DRAM portion 101 includes DRAM sense amplifiers DSA correspondingly to the bit lines DBL. The sense amplifier DSA functions to detect and amplify a potential difference between the paired bit lines and is controlled by sense control signals DSAP and DSAN. Since the DRAM array has a $\times 8$ -bit, 2-bank construction and has a memory capacity of 64 Mbits, the DRAM array includes word lines DWL1 ~ DWL8192, bit lines DBL1 ~ DBL512 and sense amplifiers DSA1 ~ DSA512. This is a construction corresponding to $\times 1$ bit of 1 bank.

[0139] The DRAM portion 101 includes the DRAM row decoder 113 for selecting one of the word lines DWL1 - DWL8192 and the DRAM row control circuit 115 for generating DRAM internal row address signals iADR0 ~ iADR12 and bank selection signal iAD13. Further, the DRAM portion 101 includes a DRAM bit line selection circuit DBSW which selects one of four bit line pairs by the DRAM bit line selection signals DBS1 ~ DBS4 generated by the DRAM column decoder 114 and connects it to the data transfer bus line TBL through the data transfer circuit 103. Further, the DRAM portion 101 includes a DRAM column control circuit 116 for generating DRAM column address signals iADC5 and iADC6 which are used by the DRAM column decoder.

[0140] Fig. 56 shows an example of a concrete array construction of the DRAM array 110-1 of the overall layout shown in Fig. 41.

[0141] In Fig. 56, the DRAM array is divided to 16 memory cell blocks DMB1 ~ DMB16. DRAM row decod-

ers DRB1 ~ DRB16 corresponding to the respective memory cell blocks DMB1 ~ DMB16 and blocks SAB1 ~ SAB17 corresponding to (sense amplifier + DRAM bit line selector circuit + data transfer circuit) are provided.

In this figure, each memory cell blocks DMB1 ~ DMB16 has a memory capacity of 1 Mbits in 512 rows $\times$ 2048 columns. It should be noted that the number of memory cell blocks is not limited to 16.

[0142] As shown in Fig. 56, when the DRAM memory cell array is divided to a plurality of portions, the length of each bit line is shortened. Therefore, the capacitance of the bit line and it is possible to increase the potential difference between the paired bit lines when data is read out. Further, since, during the operation, only sense amplifier corresponding to the memory block including word line selected by the row decoder is operated, it is possible to reduce power consumption due to charging/discharging of the bit line.

[0143] Fig. 57 shows, in detail, an example of a connecting relation between the transfer bus line and bit lines in a portion 140 (including 4 pairs of bit lines) of the layout shown in Fig. 56.

[0144] In Fig. 57, sense amplifiers DSA are arranged in zigzag manner such that a sense amplifier DSA1 corresponding to 1 column is located in one end of a memory cell block and a sense amplifier DSA2 corresponding to a next column is located in the other end of the memory cell block, etc. Such zigzag arrangement of the sense amplifiers is employed for the reason that, although the size of the memory cell can be miniaturized in the recent process technology, the miniaturization of sense amplifier in proportion to the miniaturization of memory cell is not achieved, and is necessary when there is no margin for arranging the sense amplifiers correspondingly to the bit line pitch. Therefore, when the bit line pitch is large enough, the sense amplifiers can be arranged in only one end of the memory cell block. One sense amplifier DSA is commonly used by two memory cell blocks through a shared selector circuit. Each bit line pair is provided with a bit line control circuit for equilibrating a potential difference between the bit lines thereof and precharging. The bit line control circuit may be used by two memory cell blocks similarly to the sense amplifier.

[0145] The bit lines and the data transfer bus lines are connected through DRAM bit line selector circuits DBSW1 ~ DBSW4 selected by DRAM bit line selection signals DBS1 ~ DBS4 and data transfer circuits TSW1 and TSW2 which use switching transistors SWTR each shown in Fig. 58, in detail. Data transfer activation signals TE1 and TE2 for activating the data transfer circuits are obtained by logical operation of the transfer control signal generated by the operation control circuit shown in Fig. 54 and the address signals for selecting the memory cell block. In Fig. 57, since the bit line is connected to the data transfer bus line through the DRAM the data transfer circuit and the data transfer circuit, the data transfer circuit of a memory cell block, which is not ac-

tivated, is in non-conduction state and there is no load of a DRAM bit line selection circuit connected thereto. There, it is possible to minimize the load of the data transfer bus line in operation. In the construction shown in Fig. 57, however, there is a problem that a chip area is increased since the data transfer circuits are arranged and the wiring for transmitting the data transfer activation signal for activating the data transfer circuits is provided. Fig. 59 shows an example of construction which solves such problem.

[0146] In Fig. 59, the bit line and the data transfer bus line are connected to each other through only the DRAM bit line selector circuits DBSW1 ~ DBSW4 selected by the DRAM bit line selection signals DBS1 ~ DBS4. This construction can be realized by providing the function of the data transfer circuit by adding a logic of the data transfer activation signal to the DRAM column decoder generating the DRAM bit line selection signal DBS1 ~ DBS4. Although the load of the data transfer bus line is increased during operation, it is possible to make the chip area very small.

[0147] The activation of the DRAM portion and the column selection and data transfer operation will be described with reference to Figs. 55 and 57. The activation of the DRAM portion will be described first. In Fig. 55, when the DRAM row selection control signal which is one of the DRAM portion control signals generated by the operation control circuit shown in Fig. 54 and the internal address signal iA0 ~ iA13 are input to the DRAM row control circuit 115, the bank selection signal IAD13 and the internal DRAM row address signal IADR0 ~ IADR12 are generated and the word line DWL of the bank assigned by the DRAM row decoder 113 is selected. With the selected word line DWL, data held in the cell DMC is output to the bit line DBL. The potential difference between the paired bit lines is detected and amplified by the sense amplifier DSA in response to the sense amplifier drive signals DSAN and DSAP. The number of sense amplifiers activated simultaneously in the DRAM portion 101 is 512 and, since the DRAM portion has the $\times 8$ -bit construction, the total number of the simultaneously activated sense amplifiers becomes $512 \times 8 = 4096$.

[0148] The column selection of the DRAM portion and the data transfer will be described. The DRAM column selection circuit 116 shown in Fig. 55 is input with a control signal which is one of the DRAM portion control signals generated by the operation control circuit shown in Fig. 54 in response to the internal address signals iA5 and iA6 and generates the DRAM column address signals IADC5 and IADC6. The DRAM column address signals IADC5 and IADC6 are input to the DRAM column decoder 114 and, after the DRAM bit line selection signals DBS1 ~ DBS4 are generated and the bit line is selected, data of the bit line is transmitted to the data transfer bus line TBL by the data transfer activation signal TE obtained by a logic between the transfer control signal generated by the operation control circuit shown in Fig.

54 and the address signal for selecting the memory cell block. As shown in Fig. 59, with the logic of the data transfer activation signal in the DRAM column decoder, it is possible to provide the data transfer circuit function and the DRAM bit line selection signals DBS1 ~ DBS4 can be made signals with which the column selection and the transfer operation are performed simultaneously.

[0149] Assuming, in Fig. 59, that the DRAM bit line selection signal DBS1 is selected, a signal synchronized with the transfer control signal is input to the DRAM bit line selection circuit DBSW1 and the data on the bit lines DBL1 and /DBL1, which is amplified by the sense amplifier DSA1 is transmitted to the data transfer bus lines TBL1 and /TBL1. The DRAM portion 101 shown in Fig. 55 includes 128 portions each shown in Fig. 59 and, since it has the $\times 8$ -bit construction, a total number of data transferred simultaneously from the bit line to the transfer bus line is $128 \times 8 = 1024$. This number of data transferred simultaneously is the same in other bit construction.

[DRAM Row Control Circuit and DRAM Row Decoder]

[0150] Fig. 60 is a block diagram of the DRAM row control circuit 115. The DRAM row control circuit 115 includes a DRAM internal row address latch circuit 460, a multiplexer 470, an internal address counter circuit 480 and a refresh control circuit 490.

[0151] In the usual activation of the DRAM portion, the DRAM row control circuit 115 outputs the DRAM internal row address signal IADR0 ~ IADR12 and the bank selection signal IAD13 from the address latch circuit 460 which is input with the DRAM row address latch signal ADRL and the internal address signal iA0 ~ iA13 to the DRAM row decoder 113 through the multiplexer 470.

[0152] In the refresh operation, the DRAM row control circuit 115 receives the refresh control signal and the refresh control circuit 490 operates the internal address counter circuit 480 to control the multiplexer 470 such that the selection signal from the internal address counter circuit is output. As a result, the DRAM internal row address signal IADR0 ~ IADR12 and the bank selection signal IAD13 are output to the DRAM row decoder 113 without input of the address signal. The internal address counter circuit 480 automatically add or subtract the address according to a predetermined method every time the refresh operation is performed, making an automatic selection of all of the DRAM rows possible.

[DRAM Column Control Circuit and DRAM Column Decoder]

[0153] Fig. 61 shows a concrete example of the DRAM column control circuit and the DRAM column decoder shown in Fig. 55.

[0154] In Fig. 61, the DRAM column control circuit 116 comprises a DRAM internal column address latch circuit

495 and the DRAM internal column address signals IADC5 ~ IADC6 are generated by the internal address signals iA5 and iA6 and the DRAM column address latch signal ADCL taken in a clock cycle of a command input of data transfer from the DRAM cell to the SRAM cell (prefetch transfer operation) and data transfer from the SRAM cell to the DRAM cell (restore transfer operation). The DRAM column address latch signal ADCL is one of the transfer control signals generated in the operation control circuit shown in Fig. 54. Further, the DRAM column decoder 114 decodes the DRAM internal column address signals IADC5 ~ IADC6 generated by the DRAM column control circuit 116 and outputs the DRAM column selection signal generated when the memory block selection address signal and the transfer control signal TE are activated. Therefore, the activation signals TE1 and TE2 of the data transfer circuit shown in Fig. 57 are the output signal of the DRAM column decoder 114 and the function of the data transfer circuit is performed by the DRAM bit line selection circuit to be described later.

[DRAM Bit Line Selection Circuit]

[0155] Figs. 62 to 65 show concrete examples of the circuit construction of the DRAM bit line selection circuit shown in Fig. 59.

[0156] Fig. 62 shows the simplest construction including N channel MOS switching transistors (referred to as NMOS transistors, hereinafter) N200 and N201, in which the DRAM bit line DBL and the data transfer bus line TBL are connected by the DRAM column selection signal.

[0157] Fig. 63 shows another construction of the DRAM bit line selection circuit which comprises a switching transistor circuit including NMOS transistors N210 and N211 having gates connected to respective paired DRAM bit lines and differentially amplifying data on the DRAM bit lines when the data on the DRAM bit lines DBL is transmitted to the data transfer bus line TBL and NMOS transistors N212 and N213 for transmitting the amplified signal to the data transfer bus line TBL by the prefetch transfer DRAM column selection signal. One terminals of the NMOS transistors N210 and N211 are connected to a fixed potential such as ground potential. Further, when the data on the data transfer bus line TBL is transmitted to the DRAM bit line DBL, the DRAM bit line selection circuit comprises a switching transistor circuit composed of NMOS transistors N214 and N215 as in the circuit shown in Fig. 62 and the DRAM bit line DBL and the data transfer bus line TBL are connected by the restore transfer DRAM column selection signal.

[0158] Fig. 64 shows another construction of the DRAM bit line selection circuit, which comprises a switching transistor circuit including NMOS transistors N230 and N231 having gates connected to respective paired DRAM bit lines and differentially amplifying data

on the DRAM bit lines when the data on the DRAM bit lines DBL is transmitted to the data transfer bus lines TBL and NMOS transistors N232 and N233 for transmitting the amplified signal to the data transfer bus lines TBL by the prefetch transfer DRAM column selection signal, as in the construction shown in Fig. 63. One terminals of the NMOS transistors N230 and N231 are connected to a fixed potential such as ground potential. Further, when the data on the data transfer bus lines TBL is transmitted to the DRAM bit lines DBL, the DRAM bit line selection circuit comprises a switching transistor circuit composed of NMOS transistors N250 and N251 as in the circuit shown in Fig. 63 and NMOS transistors B234 and N235 for transmitting the amplified signal to the DRAM bit lines DBL by a restore transfer DRAM column selection signal. One ends of the NMOS transistors N250 and N251 are connected to a fixed potential such as ground potential.

[0159] Fig. 65 shows another construction of the DRAM bit line selection circuit which realizes the construction shown in Fig. 64 with using only one data transfer bus lines. In the construction shown in Fig. 65, an NMOS transistor N260 does not differentially amplify the data on the DRAM bit lines DBL but remove the data transfer bus line by a potential of the DRAM bit line. An NMOS transistor N280 operates similarly. Alternatively, this may be constructed with only a switching transistor circuit as in the case shown in Fig. 62. By using only one data transfer bus line, the wiring layout becomes simple and it is possible to reduce noise between the data transfer bus lines.

[0160] Further, in the constructions in which data is received by the DRAM bit lines or the data transfer bus lines and transmitted, as shown in Figs. 63 to 65, the DRAM bit lines can be completely separated from the data transfer bus lines. Therefore, noise generated in one side is hardly transmitted to the other and a high speed operation becomes possible.

[Construction of DRAM Bit Line Selection Circuit and SRAM cell]

[0161] Fig. 66 is a constructive diagram showing a relation between paired data transfer bus lines, the DRAM bit line selection circuit and the SRAM cells in the layout shown in Fig. 36.

[0162] In Fig. 66, memory cells on one column of the DRAM cell array are connected to the data transfer bus lines through the DRAM bit line selection circuit, so that data transfer between the cells and cells on one column of the SRAM cell array is possible. Further, the data transfer bus lines and the SRAM cell array are connected to each other through transfer bus control circuits 498. The data transfer bus control circuit 498 includes a circuit for selecting and connecting one of DRAM arrays (in this example, banks A and B) arranged on both sides of the SRAM cell array so that only an activated bank can be connected and, therefore, it is possible to

realize a reduction of charging/discharging current and speed up of data transfer by the reduction of load of the data transfer bus lines. Further, since, in performing data transfer of the both banks alternately (bank ping-pong operation), the data transfer bus line of one bank can be separated from the other as shown in Fig. 67, it is possible to execute the data transfers on the both banks simultaneously to thereby shorten an effective data transfer period.

[0163] As mentioned previously, since the number of bits which can be transmitted at once by the semiconductor memory device according to this embodiment is 1024 bits and the load of the data transfer bus lines is very large, a peak current and current consumption become very large when amplitude of voltage of all data transfer bus lines is increased to the power source voltage level. In order to substantially reduce the peak current and current consumption, the amplitude of voltage of the data transfer bus lines is limited to a half of the power source voltage at most.

[0164] However, if the amplitude of voltage of the data transfer bus line is small, data of the SRAM cell must be amplified by such small potential difference and so the data transfer speed is lowered to some extent. In order to allow only the voltage of the data transfer bus line TBLS in the SRAM cell portion fully changed, a differential amplifier circuit connected to the gate of the data transfer bus line TBLA or TBLB in the DRAM bank for differentially amplifying may be provided. Alternatively, a sense amplifier for amplifying only the voltage on the data transfer bit line TBLS in the DRAM bank in a state where the data transfer bus line TBLA or TBLB in the DRAM bank is separated may be provided. Alternatively, the transfer bus control circuit 498 includes a circuit for equilibrating or precharging.

3.{SRAM portion}

[Construction of SRAM Portion and Data Input/Output Terminal]

[0165] Fig. 68 shows an example of a concrete construction of the SRAM portion shown in Fig. 1 corresponding to one bit of the data input/output terminal DQ. Although this embodiment has the 16-Kbit, $\times 8$ -bit construction, the present invention is not limited thereto and can take various constructions in combination of the construction of the main memory portion, with similar effect.

[0166] In Fig. 68, the SRAM portion includes the SRAM memory cells SMC each includes a flip-flop circuit 311, which may be any other circuit provided that it can store static data, connecting circuits 312 provided on both sides of the flip-flop circuit 311 for connection to the data transfer bus lines TBL and connecting circuits 313 also provided on the both sides of the flip-flop circuit 311 for connection to the SRAM bit lines SBL, as shown in Fig. 69. The SRAM portion further includes the SRAM

row decoder 121 for generating SRAM cell data transfer row selection signals TWL1 to TWL16 for activating the connecting circuits 312 in transferring data between the DRAM cell and the SRAM cell and the SRAM cell read/write row selection signals SWL1 to SWL16 in performing read or write and the SRAM row control circuit 124 for generating the SRAM internal row address signals iASR0 to iASR3 input to the SRAM row decoder 121 on the basis of the internal address signals iA0 to iA3 and the SRAM portion control signal. It is, of course, possible to commonly use the SRAM cell data transfer row selection signals TWL and the SRAM cell read/write row selection signals SWL. The SRAM bit line control circuit 303 for equilibrating and/or precharging the bit lines and the SRAM column selection circuit 304 for making the data input/output line SIO and the SRAM bit line SBL are connected to the SRAM bit lines SBL. The SRAM portion further includes the SRAM column decoder 123 for generating the selection signals SSL1 to SSL128 input to the SRAM column selection circuit 304 and the SRAM column control circuit 122 for generating the SRAM internal column address signals iASC4 to iASC10 on the basis of the internal address signals iA0 to iA13 and the SRAM portion control signal. The SRAM bit line control circuit 303 may include sense amplifier circuits for detecting and amplifying levels of the SRAM bit lines SBL. Further, the data input/output lines SIO are connected to the external data input/output terminals DQ through the data input/output circuit 308 and the read/write amplifier 307. The data input/output lines SIO may be provided for read and write separately.

[0167] Since the transfer bus lines TBL for data transfer and the SRAM bit lines SBL for read are provided, it is possible to perform the read operation regardless of the data transfer operation.

[SRAM Cell]

[0168] Figs. 70(a) to 70(d) show concrete circuits of the flip-flop circuit 311 of the SRAM cell shown in Fig. 69. Fig. 70(a) shows the flip-flop circuit constructed with P channel MOS transistors (referred to as PMOS transistors, hereinafter) P100 and P101 and NMOS transistors N100 and N101 and Fig. 70(b) shows a flip-flop circuit constructed with resistors R100 and R101 and NMOS transistors N100 and N101, both of which are usually employed in the SRAM. Fig. 70(c) shows a flip-flop circuit constructed with the construction shown in Fig. 70(a) added with a PMOS transistor P102 controlled by control signals PE and NE for power cut, an NMOS transistor N102 and a balancer circuit 315. One of the transistors P102 and N102 and the balancer circuit 315 may be omitted. Fig. 70(d) shows a construction which is similar to a usual sense amplifier used in the DRAM and includes a plurality of the flip-flop circuits each having the construction shown in Fig. 70(a) and arranged in the row direction, a PMOS transistor P103 for controlling a contact point 316 by the control signal

SPE, an NMOS transistor N103 for controlling a contact point 317 by the control signal SNE, a balancer circuit 318 for balancing the contact points 316 and 317 and balancers 315 provided in each of the flip-flop circuit as in the case shown in Fig. 70(c). The power source voltage may be an external power source voltage or an internal power source voltage generated by a power source voltage converter circuit. The PMOS transistor P102 for power cut and the PMOS transistor P103 for controlling the contact point 316 by the control signal SPE may be NMOS transistors, respectively, in which case, the levels of the control signals PE and SPE may be the level of an internally generated power source voltage which is higher than the power source voltage generated by the power source voltage converter circuit.

[0169] By reducing a current flowing through the flip-flop by using the flip-flop circuit shown in Fig. 70(c) or 70(d), it is possible to substantially reduce noise generated in the transfer operation. Further, by performing the data transfer while balancing the opposite contact points, it is possible to realize a stable, high speed transfer operation.

[0170] The transistors constituting the flip-flop circuit are not special and may be identical to those used in the peripheral circuit or the DRAM sense amplifiers.

[Connection Circuits for SRAM Bit Line and Data Transfer Bus Line]

[0171] Figs. 71 to 73 show circuit examples of the connection circuits for connection to the SRAM bit lines SBL.

[0172] Fig. 71 shows the simplest construction which includes NMOS switching transistor N104 and N105 and is connected to the SRAM bit lines SBL by a read/write row selection signal SWL.

[0173] The construction shown in Fig. 72 includes a switching transistor circuit composed of NMOS transistors N108 and N109 having gates connected to the respective opposite terminals of the flip-flop circuit for differentially amplifying signals on the terminals in reading data from the flip-flop circuit and NMOS transistors N106 and N107 for transmitting the amplified signals to the SRAM bit lines SBL by a read row selection signal SRWL. One terminals of the NMOS transistors N108 and N109 are connected to a fixed potential such as ground potential. In writing data in the flip-flop circuit, the construction shown in Fig. 72 further includes a switching transistor circuit composed of NMOS transistors N110 and N111, as shown in Fig. 71, which connect the SRAM bit lines SBL to the flip-flop circuit by a write row selection signal SWWL.

[0174] A construction shown in Fig. 73 includes a switching transistor circuit composed of NMOS transistors N108 and N109 having gates connected to the respective opposite terminals of the flip-flop circuit for differentially amplifying signals on the terminals in reading data from the flip-flop circuit as in the case shown in Fig.

72 and NMOS transistors N106 and N107 for transmitting the amplified signals to the SRAM bit lines SRBL for SRAM read by a read row selection signal SRWL. One terminals of the NMOS transistors N108 and N109 are connected to a fixed potential such as ground potential. In writing data in the flip-flop circuit, the construction shown in Fig. 73 further includes a switching transistor circuit composed of NMOS transistors N114 and N115 having gates connected to the SRAM write bit line pair for differentially amplifying the signals on the SRAM write bit lines SWBL in writing data in the flip-flop circuit and NMOS transistors N112 and N113 for transmitting the amplified signals to the opposite terminals of the flip-flop circuit by a write row selection signal SWWL. One terminals of the NMOS transistors N114 and N115 are connected to a fixed potential such as ground potential.

[0175] In the construction shown in Fig. 72 or 73 in which data is transferred by connecting the opposite ends of the flip-flop circuit or the SRAM bit lines SBL to the gates of the transistors, it is possible to completely separate the opposite terminals of the flip-flop circuit from the SRAM bit lines SBL. Therefore, noise generated in one side is hardly transmitted to the other and a high speed operation becomes possible.

[0176] It is possible to construct the connection circuit to the data transfer bus lines TBL in the same manner as in the case shown in Fig. 71, 72 or 73.

[SRAM Row Control Circuit]

[0177] Fig. 74 shows, in detail, the circuit construction of the SRAM row control circuit shown in Fig. 68. In Fig. 74, the SRAM row control circuit is constructed with a SRAM internal row address latch circuit 350 and SRAM internal row address signals iASR0 to iASR3 are generated by the internal address signals iA0 to iA3 and a latch signal ASRL which takes the internal address signals in a clock cycle of a read/write command input. The latch signal ASRL is one of the SRAM control signals generated by the operation control circuit shown in Fig. 54.

[SRAM Column Control Circuit]

[0178] Fig. 75 shows, in detail, the construction of the SRAM column control circuit shown in Fig. 68.

[0179] In Fig. 75, the SRAM column control circuit includes an SRAM internal column address latch circuit 507 for latching the internal address signals iA4 to iA10 by a latch signal ASCL generated by the clock cycle at the read/write command input and a counter circuit 506 for taking in the output of the SRAM internal column address latch circuit 507 by a control signal SCE and counting up in a predetermined sequence by an internal count-up signal CLKUP operable during a burst operation for performing read/write with respect to the SRAM and the SRAM internal column address signals iASC4 to iASC10 is output through a multiplexer 508 which

passes the output of either the latch circuit 507 or the counter circuit 506. The multiplexer 508 selects the output of the latch circuit 507 in the clock cycle at the read/write command input and is controlled by the control signal SCSL such that the SRAM internal column address signal can be output at a speed as high as possible. Further, the SRAM column control circuit according to the present invention includes a data input/output mode memory portion 505 which, in order to set completely different data input/output modes, for example, burst length, data input/output address sequence and latency, etc., for a plurality of SRAM cell groups (in this example, SRAM cell groups divided every row), takes the data input/output modes according to the states of the internal address iA0 to iA13 in the previously mentioned mode register setting (2) command cycle (in this example, although only the burst length can be set for the respective SRAM cell groups, it is possible to set the data input/output address sequence, latency, etc., for them) and stores the data input/output modes. The data input/output mode memory portion 505 includes take-in logic 502 provided in respective divided SRAM cell groups for generating setting data to be taken in according to the states of the internal address iA0 to iA13, registers 503 provided for the respective take-in logic for taking in the setting data (outputs of the take-in logic 502) of the data input/output modes of the respective SRAM cell groups by an output of the decoder circuit 501 which is selected by the enable signal CRE generated in the previously mentioned mode register setting (2) command cycle, the setting data being decoded by the address iA0 to iA3, and a multiplexer 504 for passing one of the outputs of the registers 503 holding the setting data of the SRAM cell groups by selectively controlling the iASR0 to iASR3 output from the SRAM internal row address latch circuit 350 in the read/write command cycle by using the signal decoded by the decoder circuit 509. The counter circuit 506 takes in an output of the multiplexer 504 to operate the semiconductor memory device in the data input/output mode set in the respective SRAM cell groups. The data input/output mode memory portion 505 must be provided for each of the data input/output modes to be set. The internal count-up signal CLKUP, the enable signal CRE, the control signals SCE and SCSL and the latch signal ASCL are the SRAM portion control signals generated by the operation control circuit shown in Fig. 54. Of course, it is possible to make the latch signal AS-RL input to the SRAM internal row address latch circuit 350 and the latch signal ASCL input to the SRAM internal column address latch circuit 507 common.

[0180] Instead of the setting of the data input/output mode memory portion 505 performed for the respective SRAM cell groups by the mode register setting (2) command cycle, it is possible to set the same setting data of two or more SRAM cell groups at once or to set a logic of addresses A4 and A6 in setting the SRAM row data of the mode register setting (2) command shown in Fig. 10. For example, when A4 = L and A5 = L, the data input/

output mode is set in every SRAM cell group, when A4 = H and A5 = L, the data input/output mode is set in two SRAM cell groups neglecting least 2 bits of the SRAM row data. In such manner, the data input/output mode memory portion 505 can be set in various combinations. Further, the number of the take-in logic 502 as well as the registers 503 is not always the same as that of the divided SRAM cell groups and it is possible to use one set of the take-in logic 502 and the register 503 commonly for a plurality of SRAM cell groups. Further, the addresses iASR0 to iASR3 are not always the signals from the SRAM internal row address latch circuit 350 and it is possible to provide a separate circuit therefor.

[0181] Further, it is possible to generate the internal address signals at high speed by constructing the SRAM internal column address latch circuit 507 and the multiplexer 508 such that the internal address is output immediately after a logic between the internal address and the internal clock signal iCLK synchronized with the external reference clock signal, as shown in Fig. 76. In Fig. 76, INTAi and /INTAi are address signals from the counter circuit 506 and EXT Ai and /EXT Ai are address signals generated from the internal address signal iAi. These signals are switched by the control signals SCSL and /SCSL and the burst control signal. SCSL is the control signal and /SCSL is a control signal having a phase opposite to that of the control signal SCSL. Fig. 77 shows an example of operation of this circuit. In this circuit construction, a delay from the internal clock iCLK to a time at which the internal address signal Yi is output corresponds to one stage of inverter and is minimized. The internal address signals Yi and YiB are output as address pulse signals.

[SRAM Column Decoder and Data Control Circuit Construction]

[0182] Fig. 78 shows an example of construction of the SRAM column decoder 123 and the data control circuit. The circuit construction includes a first column decoder 390 and a second column decoder 391 and the SRAM column selection signal iASC is transmitted to these column decoders sequentially. In order to operate the first and second column decoders by one address selection data iASC, the first and second column decoders are connected to a first column address buffer 392 and a second column address buffer 393, respectively. Selection signal lines SSL from the first and second column decoders are juxtaposed in column direction and a first data latch circuit 395 associated with a data input/output line SIO and a second data latch circuit 396 associated with a data input/output line SIO are also provided correspondingly.

[0183] Fig. 79 shows an internal operation timing of the SRAM column decoders. The respective column address buffers perform column decoder selection signal (iASC-1 and iASC-2) sequentially on the basis of the CLK signal. That is, when the column address selection

is successively performed as in the burst mode, the first column decoder and the second column decoder operate alternately. Data of the columns (SSL-1 and SSL-2) selected by the respective column decoders are output sequentially to the corresponding data input/output lines (SIO-1 and SIO-2). These data input/output lines operate with a cycle time which is twice a request cycle time and the first data latch circuit 395 and the second data latch circuit 396 hold the data temporarily. These two sets of data are synthesized before the data out buffer and output from the data input/output terminals DQ in the requested cycle time.

[0184] With using the above mentioned construction, it is possible to increase the cycle speed of the successive data output and/or successive data write without increasing the internal operation cycle speed. This is also true in the synchronous DRAM of DOUBLE DATA RATE (DDR).

[Other Construction of SRAM Portion including Data Input/Output Terminals]

[0185] Fig. 80 schematically shows another example of construction of the SRAM portion including the data input/output terminals in a case where it has the X8-bit construction. In a case of the data output from the SRAM, data of the SRAM cells of a selected column are output to the respective data input/output lines SIO. The data input/output lines SIO of the selected row is connected to the global data input/output line GIO and the data are sent to a corresponding data amplifier 153. Thereafter, the data pass through a read/write bus line RWL, a data latch circuit 151 and a data buffer 152 to the data input/output terminal DQ. Since the SRAM portion has the X8-bit construction, 8 sets of data input/output circuits operate simultaneously and output 8 data. Data are written in the SRAM cells along a path reverse to the data read path. With using this circuit construction using the data input/output lines SIO and the global data input/output lines GIO, the SRAM row selection of every SRAM cell becomes unnecessary, the load of the SRAM row selection signal lines is reduced and a high speed data input/output of the SRAM cells becomes possible. Further, with using this construction, the load of the data input/output lines SIO is not increased, realizing high speed operation even when the number of rows of the SRAM cells is increased.

[SRAM Column Redundancy Circuit]

[0186] Fig. 81 shows an example of construction of the SRAM column redundancy circuit for an SRAM cell array corresponding to one of the input/output terminals DQ. In Fig. 81, a redundancy SRAM cell column is arranged in an upper end of the SRAM cell array. A redundancy data input/output line extends upward from the SRAM cell array through an SRAM row selection switch and a usual (non-redundancy) data input/output line ex-

tends downward from the SRAM cell array through another row selection switch. A global data input/output line is arranged in an upper portion of the SRAM array and connected to a redundancy data amplifier and write buffer and a usual (non-redundancy) global data input/output line is arranged in a lower portion of the SRAM array and connected to a usual data amplifier and write buffer. A switching from an SRAM cell column to a redundancy SRAM cell column is performed by switching the global data input/output line or switching of the data amplifier and write buffer. With such construction, a switching of the SRAM array to the redundancy cell column for every input/output terminal DQ becomes possible and it is possible to remove a difference in access time to the redundancy cell column even when the switching to the redundancy cell column. Although, in this example, the redundancy SRAM cell column, the data input/output line and the global data input/output line are arranged in the upper portion of the SRAM cell array, the arrangement of them is not limited thereto.

(8) Others

1. {Power Source Voltage}

[Power Source Voltage Applied to DRAM and SRAM]

[0187] Fig. 82 shows an example of construction of the power source connection to the DRAM array portion and the SRAM array portion.

[0188] In Fig. 82, this semiconductor memory device includes a power source voltage converter circuit 603 which generates an internal power source voltage VINT on the basis of an external power source voltage VEXT. The internal power source voltage VINT is applied to the DRAM array portion 601 and the external power source voltage VEXT is applied to the SRAM array portion 602 directly. In the recent DRAM, the miniaturization of process is enhanced and the breakdown voltage of a memory cell becomes lower. In order to solve this problem, it is usual that the power source voltage in a memory cell array is made lower than an external power source voltage. However, the driving ability of transistor is necessarily degraded with lower power source voltage, which is an obstacle for speed-up of operation. In this embodiment, the miniaturization of the SRAM array portion is restricted compared with that of the DRAM array portion and the high operation speed of the SRAM portion is achieved by allowing the external power source voltage VEXT to be used in the SRAM portion. For example, the write speed in writing data in an SRAM cell is increased by 41% in a case where external power source voltage VEXT = 3.3V and the internal power source voltage VINT = 2.5V, as shown in Fig. 84 which is a result of simulation of the power source voltage dependency of data write time in an SRAM cell.

[0189] Fig. 83 shows another example of construction of the power source connection to the DRAM array por-

tion and the SRAM array portion.

[0190] In Fig. 83, this semiconductor memory device includes a power source voltage converter circuit 603 which generates a first internal power source voltage VINT1 and a second internal power source voltage VINT2 on the basis of an external power source voltage VEXT. The first internal power source voltage VINT1 is applied to the DRAM array portion 601 and the second internal power source voltage VINT2 is applied to the SRAM array portion 602 directly. In this case, the same effect as that obtained by the construction shown in Fig. 82 is obtainable by making the second internal power source voltage VINT2 higher than the first internal power source voltage VINT1. In this case, it may be possible to use two power source voltage converters 603 for generating the first internal power source voltage VINT1 and the second internal power source voltage VINT2, respectively.

[0191] As to the substrate potential which is related to the power source voltage, various cases may be considered depending upon the kinds of memory cell constituting the main memory portion and the sub memory portion. For example, when the main memory portion is constructed with dynamic memory cells, it is possible to use the potential of the substrate for the main memory portion lower or for the main memory portion, the sub memory portion and the bi-directional data transfer circuit lower than other area of the substrate. These substrate potentials may be realized by forming, in a P type substrate, a P well, an N well and a deeper N well.

2. (Description of Other Functions)

[Function 1: Copy Transfer]

[0192] The semiconductor memory device according to the present invention may have a function of data transfer between SRAM memory cells on the same column, for example, between a memory cell SMC1 and a memory cell SMC16 in Fig. 68.

[0193] With such function, it is possible to copy a cell data of one row of the SRAM cell array to another row at substantially higher speed than that in a case of transfer from the DRAM cell. Further, this function can be executed without influence of data transfer operation with respect to the DRAM.

[0194] A data transfer operation from cells of one row including the memory cell SMC1 to cells of one row including the memory cell SMC16 will be described with reference to Fig. 68. First, SRAM cell read/write row selection signal SWL1 is activated and transmit data of the cells of one row including the memory cell SMC1 to the respective SRAM bit lines. Thereafter, the SRAM cell read/write row selection signal SWL16 is activated to transmit the data of the respective bit lines to the cells of one row including the memory cell SMC16 and rewrite the cell data. Since the data is transferred by using the SRAM bit lines SBL, the data transfer between, for ex-

ample, the cells of one row including the memory cell SMC2, which is selected by the SRAM cell data transfer row selection signal TWL2, and the DRAM cells can be performed by using the data transfer bus lines TBL regardless of the data transfer from the cells of the row including the memory cell SMC1 to the cells of the row including the memory cell SMC16. All of these operations are performed by command input and, therefore, commands for assigning a transferring SRAM cell group and a transferred SRAM cell group must be added.

[Function 2: Temporary Cell Transfer]

[0195] In the construction of the SRAM array portion shown in Fig. 68, when there is data in the assigned SRAM cell and the data is newly read by performing a data transfer (prefetch transfer operation) from a DRAM cell of another row, the data written in the SRAM cell is read by temporarily transferring the data to the DRAM (restore transfer operation) and then performing a data transfer from a DRAM of another row (prefetch transfer operation). Depicting the cycle time of data transfer to the DRAM cell as tRC and a time from the data transfer from the DRAM cell to the DRAM cell (prefetch transfer operation) to the read-out of the data of the SRAM cell as tRAC, it takes a time tRC + tRAC to complete the data read. However, it is possible to read the data at higher speed by providing the following function. Fig. 85 shows an example of concrete construction of an SRAM array portion which realizes the function.

[0196] In Fig. 85, the construction is substantially the same as that shown in Fig. 68 except that the construction shown in Fig. 85 includes additionally one row of temporary SRAM cells and a selector circuit 309 for selecting temporary cell row by a control signal TCSL. The control signal TCSL is one of the transfer control signals generated by the operation control circuit shown in Fig. 54 and is generated when a data transfer to the temporary cell is performed. Instead thereof, it is possible to construct the SRAM array such that one of the existing SRAM cell rows can be selected as the temporary SRAM cell row or to add a plurality of temporary SRAM cell rows.

[0197] An example of operation when, in Fig. 85, data of the SRAM cells is read by transferring (copying) data of memory cells of one row including the memory cell SMC1 to memory cells of one row including a temporary memory cell SMCD and transferring (prefetching) data from the DRAM cells to the cells of one row including the memory cell SMC1 will be described with reference to Fig. 86.

[0198] First, an active command is input to select a certain DRAM cell row having data to be read out. Then, when a newly added command (temporary cell copy command) for transfer of data to the temporary SRAM cells is input, the control signal TCSL is activated. the SRAM cell read/write row selection signal SWL1 is ac-

tivated by an SRAM row address which is input simultaneously with the command and to which the data is transferred, and the data of the cells of one row including the memory cell SMC1 is transmitted to the respective SRAM bit lines. Thereafter, the SRAM temporary cell read/write row selection signal SWLD is activated by the control signal TCSL, and the data of the respective bit lines are transmitted to the temporary cells of one row including the temporary memory cell SMCD to rewrite the cell data. This operation is the same as the operation for copying the cell data of a certain one row of the SRAM cell array described in the term of [Function 1]. With this operation, it is possible to temporarily store the cell data to be transferred to the DRAM. Then, the prefetch command is input to perform a data transfer (prefetch transfer operation) from the DRAM cells to the cells of one row including the memory cell SMC1 to transmit the data to be read out to the SRAM memory cells. Then, the read command is input to read the data from the SRAM cells. As mentioned above, it is possible to remove the time tRC and to read the data for the time tRAC. Thereafter, the data transferred to the temporary cells is transferred (temporary cell restore transfer operation) to the DRAM.

[Function 3: Simultaneous Transfer of Plural Rows]

[0199] The semiconductor memory device according to the present invention can have a function of transferring same data by simultaneously selecting SRAM cell groups of a plurality of rows when the data of cell groups in a selected row of a DRAM is transferred to the SRAM portion.

[0200] This function can be added by a simple circuit. In Fig. 68, it is enough to activate a plurality of SRAM cell data transfer row selection signals TWL by adding a control signal to be generated by a newly added command for executing the above function to the SRAM row control circuit 124 and controlling the SRAM internal row address signal by the control signal.

[Function 4: Auto Successive Prefetch/Restore Transfer]

[0201] When, among data of DRAM cells of a selected row, data of DRAM cell groups selected by the DRAM column decoder is transferred to the SRAM portion, the semiconductor memory device may have a function of reducing a total time of data transfer by not repeating the data transfer by a plurality of commands but successively repeating the transfer operation with interval corresponding to a predetermined in-chip delay time by one command.

[0202] Fig. 87 shows an example of an internal operation related to this function. In this description, it is assumed that the DRAM cells in one row are divided to four DRAM cell groups by the DRAM column decoder. However, the DRAM cells can be divided to any number

of DRAM cell groups.

[0203] In Fig. 87, when the newly added command (prefetch (2) command) defining this function is input, four internal count-up signals are generated successively with the interval corresponding to the predetermined delay time in the chip. The DRAM column control circuit for generating the internal column address signal and the SRAM row control circuit for generating the SRAM internal row address signal are provided with counter circuits, respectively. The DRAM column address and the SRAM row address, which are input simultaneously with the input of the command, are taken in by an initial internal count-up signal and the respective addresses are counted up sequentially by the succeeding internal count-up signals. The respective data are transferred in the cycle of the four internal count-up signals.

[0204] Similarly, when data of a plurality of SRAM cell groups is transferred to a plurality of DRAM cell groups selected by the DRAM row decoder and the DRAM column decoder, the semiconductor memory device may have a function of transferring the plurality of the DRAM cell groups, respectively, by not repeating the data transfer by a plurality of commands but successively repeating the transfer operation with interval corresponding to a predetermined in-chip delay time by one command. This function can be realized similarly to the preceding function, by generating internal count-up signals successively with the interval corresponding to the predetermined delay time in the chip and providing counter circuits in the DRAM column control circuit for generating the internal column address signal and the SRAM row control circuit for generating the SRAM internal row address signal, respectively.

[Function 5: Plural Row Successive Read/Write]

[0205] The semiconductor memory device according to the present invention may have a function of reading/writing all data of SRAM cell groups of a plurality of rows according to a sequence predetermined for the SRAM cell groups of the plurality of rows successively with a predetermined interval by one command.

[0206] With such function, when, for example, data of cells of one row of a DRAM is held in a plurality of SRAM cell groups, it becomes possible to successively read/write all cell data of one row of the DRAM in a predetermined sequence, so that the load of the memory controller and/or chip set for controlling the semiconductor memory device is reduced and the operation of the latter together with other SRAM cell groups and the DRAM portion becomes possible. Further, it is possible to provide other effects when this function is used together with the function 4.

[0207] Fig. 88 shows an example of concrete construction of an SRAM row control circuit for realizing this function.

[0208] In Fig. 88, this SRAM row control circuit is con-

structured by adding a counter circuit 351 for taking in the output of the SRAM internal row address latch circuit 350 shown in Fig. 74 by a control signal SRE and counting up the output in a predetermined address sequence by an internal count-up signal SRUP generated when the SRAM column address becomes the uppermost address and a multiplexer 352 for passing either one of the outputs of the latch circuit 350 and the counter circuit 351 to the SRAM internal row address latch circuit 350. The multiplexer 352 is controlled by a control signal SRS� such that it selects the output of the latch circuit 350 in the clock cycle at the input of the read/write command and outputs the SRAM internal row address signal as fast as possible. The SRAM column control circuit has a function of sequentially shifting up from the taken column address to the uppermost address when the newly added command defining this function is input to the counter circuit 506 shown in Fig. 75.

[0209] Fig. 89 shows an example of internal operation of a read function of this function.

[0210] In Fig. 89, when a newly added command (read (2) command) defining this function is input, the control signal SRS� is generated and the output of the SRAM internal row address latch circuit 350 becomes the SRAM internal row address iASR0 to iASR3 by the multiplexer 352 and is taken in the counter circuit 351 by the control signal SRE. Thereafter, the column address is incremented in synchronism with the reference clock signal CLK and the counter 351 increments the row address by the internal count-up signal SRUP generated when the count becomes the uppermost address. After the count becomes the uppermost address, the multiplexer 352 is controlled by the control signal SRS� and the output of the counter circuit 351 becomes the SRAM internal row address iASR0 to iASR3. Thus, it is possible to successively read all data of the SRAM cell groups of a plurality of rows by shifting the row and column addresses sequentially.

[0211] The internal count-up signal SRUP, the control signal SRE and the control signal SRS� are SRAM portion control signals generated by the operation control circuit shown in Fig. 54.

[Function 6: Real Time Mode Setting]

[0212] The semiconductor memory device according to the present invention may have a function of setting the data input/output modes such as burst length, data input/output address sequence and latency, etc., simultaneously with a read/write command input when read/write operation is performed with respect to the SRAM cell by an input of the command.

[0213] With such function, it is possible to substantially reduce the load of the memory controller and chip set for controlling the semiconductor memory device of the present invention and improve the system performance since it is possible to assign different data input/output modes at once every time of requests of such modes.

[0214] Fig. 90 shows a correspondence table between read(3)/write (3) commands according to this function and the states of respective input terminals. The table shown in Fig. 90 differs from the table shown in Fig. 10 in that burst length selection is assigned to address terminals A11, A12 and A13 which are not used at the time of read/write command input. Thus, according to the states of the 3-bit address terminals, it is possible to select/assign the burst length shown in Fig. 26 simultaneously with the read (3)/write (3) command input. Although the burst length selection is assigned in this embodiment, it is possible to assign the data input/output modes such as data input/output address sequence, latency, etc., in the similar manner.

[0215] Fig. 91 shows an example of operation when this function is used. In Fig. 91, the data input/output address sequence is set to sequential and the latency is set to 2 and the burst length is changed by the address signals A11 to A13 (internal address signal iA11 to iA13) at the read (3) command input. This can be realized by controlling the counter circuit in the SRAM column control circuit shown in Fig. 75 according to the setting of the burst length and controlling the SRAM internal column address iASC4 to iASC10, as in the usual SDRAM.

[Function 7: Auto Restore/Prefetch Transfer]

[0216] Further, the semiconductor memory device according to the present invention may have a function of transferring, after data is transferred from a DRAM cell group to an SRAM cell group, data of another SRAM cell group to the DRAM cell group. In order to realize this function, it is enough to internally hold the DRAM row address and the DRAM column address at the data transfer, and, therefore, it is possible to realize the function by using the DRAM internal row address latch circuit shown in Fig. 60 and the DRAM internal column address latch circuit shown in Fig. 61. Further, by providing such latch circuits every bank, an alternate access of different banks becomes possible. Therefore, there is no need of assigning the DRAM row address and the DRAM column address at the restore transfer operation and an effective time required for the restore operation is shortened, so that the control in the memory controller and chip set for controlling the semiconductor memory device becomes simple, the load is reduced and the system performance is improved.

[0217] Completely similarly thereto, the semiconductor memory device according to the present invention may have a function of transferring, after data is transferred from a DRAM cell group to an SRAM cell group, data of another DRAM cell group to the SRAM cell group.

[0218] According to the present invention, in a system including a plurality of processing devices (memory masters), it is possible to obtain a semiconductor integrated circuit device having a main memory portion and a sub memory portion capable of being assigned corre-

sponding to a plurality of access requests in order to increase an operation speed of the whole system without reducing the cache hit even when there are access requests from a plurality of memory masters.

Claims

1. A semiconductor memory device comprising:

a main memory portion (101) including memory cells arranged in a plurality of rows and in a plurality of columns; and
a sub memory portion (102) having memory cell groups each including memory cells arranged in a plurality of rows and in a plurality of columns,

characterized in that said sub memory portion (102) includes a plurality of registers (503) coupled to a corresponding one of said memory cell groups, each of said registers (503) storing a data input/output mode selected from the group consisting of an address sequence, a burst length and a latency, to set said data input/output mode for said corresponding one of said memory cell groups, and that

at least one of address input terminals assigning rows or columns of said main memory portion and at least one of address input terminals assigning rows or columns of said sub memory portion are commonly used.

2. A semiconductor memory device as claimed in claim 1, wherein address signals assigning rows or columns of said main memory portion and address signals assigning rows or columns of said sub memory portion are internal address signals generated by external address signals and external clock signals or external control signals and at least one of the internal address signals is commonly used by said main memory portion and said sub memory portion.

3. A semiconductor memory device as claimed in claim 1, further comprising:

a first internal address signal generator circuit responsive to an address input terminal signal for generating a first internal address signal;
a second internal address signal generator circuit responsive to the first internal address signal for successively generating a second internal address signal during a burst mode operation; and
means for selecting either of the first internal address signal or the second internal address signal.

4. The semiconductor memory device as claimed in claim 1, said device further comprising:

a first internal address signal generator circuit responsive to an address input terminal signal for generating a first internal address signal;
a second internal address signal generator circuit responsive to the first internal address signal for successively generating a second internal address signal during a burst mode operation; and
a circuit for selecting either of the first internal address signal or the second internal address signal and generating a third address signal by synchronizing the selected signal with an external clock signal or an external control signal.

5. The device as claimed in claim 1, wherein said main memory portion (101), said sub memory portion (102) and said registers (503) are formed on a single chip.

6. The semiconductor memory device as claimed in claim 1, wherein said sub memory portion (102) has an access speed greater than an access speed of said main memory portion (101).

7. The semiconductor memory device as claimed in claim 1, wherein an allocation, assignment, or re-assignment of said memory cell groups is received for each of a plurality of received access requests.

8. The semiconductor memory device as claimed in claim 1, wherein multiple data input/output operations are performed successively devoid of any external data control signal and an external data control processing signal.

9. The semiconductor memory device as claimed in claim 1, wherein memory cells arranged in a column of said main memory portion (101) are connected to memory cells arranged in a column of said sub memory portion (102).

10. The semiconductor memory device as claimed in claim 1, wherein said main memory portion (101) includes a plurality of memory cell groups each arranged in a plurality of rows and in a plurality of columns, and

wherein multiple ones of said plurality of memory cell groups of said main memory portion (101) are selectively connected to a memory cell group of said sub memory portion (102).

11. The semiconductor memory device as claimed in claim 1, wherein an address signal is used to set a data input/output mode of each of said memory cell groups automatically, without an external data con-

trol signal or an external data processing control signal, when the memory cell group is selected.

nen Adresssignals oder des zweiten internen Adresssignals.

Patentansprüche

1. Halbleiterspeichervorrichtung mit:

einem Hauptspeicherteil (101), der Speicherzellen aufweist, die in einer Anzahl von Zeilen und einer Anzahl von Spalten angeordnet sind; und
einem Subspeicherteil (102) mit Speicherzellengruppen, die jeweils Speicherzellen enthalten, die in einer Anzahl von Zeilen und einer Anzahl von Spalten angeordnet sind,

dadurch gekennzeichnet, dass der Subspeicherteil (102) eine Anzahl von Registern (503) enthält, die an eine entsprechende eine der Speicherzellengruppen gekoppelt sind, wobei jedes der Register (503) einen Dateneingangs-/ausgangsmodus speichert, der von der Gruppe, bestehend aus einer Adressensequenz, einer Burstlänge und einer Latenz gewählt worden ist, um den Dateneingangs-/ausgangsmodus für die entsprechende eine der Speicherzellengruppen zu setzen, und dass wenigstens einer der Adresseingangsanschlüsse, die dem Hauptspeicherteil Zeilen oder Spalten zuweisen und wenigstens einer der Adresseingangsanschlüsse, die dem Subspeicherteil Zeilen oder Spalten zuweisen, gemeinsam genutzt werden.

2. Halbleiterspeichervorrichtung nach Anspruch 1, wobei Adresssignale, die Zeilen oder Spalten des Hauptspeicherteils zuweisen und Adresssignale, die Zeilen oder Spalten des Subspeicherteils zuweisen interne Adresssignale sind, die durch externe Adresssignale und externe Taktsignale oder externe Steuersignale erzeugt worden sind, und wenigstens eines der internen Adresssignale wird von dem Hauptspeicherteil und dem Subspeicherteil gemeinsam genutzt.

3. Halbleiterspeichervorrichtung nach Anspruch 1, weiterhin mit:

einer ersten internen Adresssignalgeneratorschaltung, die auf ein Adresseingangsanschlußsignal antwortet, um ein erstes internes Adresssignal zu erzeugen;
einer zweiten internen Adresssignalgeneratorschaltung, die auf das erste interne Adresssignal antwortet, um während einer Burstmodusoperation sukzessive ein zweites internes Adresssignal zu erzeugen; und
Mitteln zum Wählen entweder des ersten inter-

4. Halbleiterspeichervorrichtung nach Anspruch 1, wobei die Vorrichtung weiterhin aufweist:

eine erste interne Adresssignalgeneratorschaltung, die auf ein Adresseingangsanschlußsignal antwortet, um ein erstes internes Adresssignal zu erzeugen;
eine zweite interne Adresssignalgeneratorschaltung, die auf das erste interne Adresssignal antwortet, um während einer Burstmodusoperation sukzessive ein zweites internes Adresssignal zu erzeugen; und
eine Schaltung zum Wählen entweder des ersten internen Adresssignals oder des zweiten internen Adresssignals und Erzeugen eines dritten Adresssignals durch Synchronisieren des gewählten Signals mit einem externen Taktsignal oder einem externen Steuersignal.

5. Vorrichtung nach Anspruch 1, wobei der Hauptspeicherteil (101), der Subspeicherteil (102) und die Register (503) auf einem einzigen Chip ausgebildet sind.

6. Halbleiterspeichervorrichtung nach Anspruch 1, wobei der Subspeicherteil (102) eine Zugangsgeschwindigkeit hat, die größer als die Zugangsgeschwindigkeit des Hauptspeicherteils (101) ist.

7. Halbleiterspeichervorrichtung nach Anspruch 1, wobei eine Zuordnung, eine Zuweisung oder eine Wiederzuweisung der Speicherzellengruppen für jede der Anzahl von empfangenen Zugangsanfragen empfangen wird.

8. Halbleiterspeichervorrichtung nach Anspruch 1, wobei Mehrfachdateneingangs-/ausgangsoperationen sukzessive ohne irgendein externes Datensteuersignal und externes Datensteuerverarbeitungssignal durchgeführt werden.

9. Halbleiterspeichervorrichtung nach Anspruch 1, wobei Speicherzellen, die in dem Hauptspeicherteil (101) in Spalten angeordnet sind, mit Speicherzellen verbunden sind, die in dem Subspeicherteil (102) in Spalten angeordnet sind.

10. Halbleiterspeichervorrichtung nach Anspruch 1, wobei der Hauptspeicherteil (101) eine Anzahl von Speicherzellengruppen aufweist, die jeweils in einer Anzahl von Zeilen und in einer Anzahl von Spalten angeordnet sind, und
wobei mehrere der Anzahl von Speicherzellengruppen des Hauptspeicherteils (101) selektiv mit einer Speicherzellengruppe des Subspeicher-

teils (102) verbunden sind.

11. Halbleiterspeichervorrichtung nach Anspruch 1, wobei ein Adresssignal dazu verwendet wird, um einen Dateneingangs-/ausgangsmodus jeder der Speicherzellengruppen ohne ein externes Datensteuersignal oder ein externes Datenverarbeitungssteuersignal automatisch zu setzen, wenn die Speicherzellengruppe gewählt ist.

Revendications

1. Dispositif de mémoire à semi-conducteur comprenant :

une partie de mémoire principale (101) incluant des cellules de mémoire agencées en une pluralité de rangées et en une pluralité de colonnes ; et

une partie de sous-mémoire (102) ayant des groupes de cellules de mémoire incluant chacun des cellules de mémoire agencées en une pluralité de rangées et en une pluralité de colonnes,

caractérisé en ce que ladite partie de sous-mémoire (102) inclut une pluralité de registres (503) couplés à un groupé correspondant desdits groupes de cellules de mémoire, chacun desdits registres (503) stockant un mode d'entrée / sortie de données sélectionné à partir du groupe constitué d'une séquence d'adresse, d'une longueur de salve et d'un temps d'attente, pour fixer ledit mode d'entrée / sortie de données pour ledit groupe correspondant desdits groupes de cellules de mémoire, et **en ce que** :

au moins une des bornes d'entrée d'adresse attribuant des rangées ou des colonnes de ladite partie de mémoire principale et au moins une des bornes d'entrée d'adresse attribuant des rangées ou des colonnes de ladite partie de sous-mémoire sont habituellement utilisées.

2. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel des signaux d'adresse attribuant des rangées ou des colonnes de ladite partie de mémoire principale et des signaux d'adresse attribuant des rangées ou des colonnes de ladite partie de sous-mémoire sont des signaux d'adresse internes générés par des signaux d'adresse externes et des signaux d'horloge externes ou des signaux de commande externes et au moins un des signaux d'adresse internes est habituellement utilisé par ladite partie de mémoire principale et ladite partie de sous-mémoire.

3. Dispositif de mémoire à semi-conducteur selon la revendication 1, comprenant en outre :

un premier circuit générateur de signal d'adresse interne sensible à un signal de borne d'entrée d'adresse pour générer un premier signal d'adresse interne ;

un second circuit générateur de signal d'adresse interne sensible au premier signal d'adresse interne pour successivement générer un deuxième signal d'adresse interne pendant un fonctionnement en mode salve ; et

des moyens pour sélectionner l'un ou l'autre du premier signal d'adresse interne ou du deuxième signal d'adresse interne.

4. Dispositif de mémoire à semi-conducteur selon la revendication 1, ledit dispositif comprenant en outre :

un premier circuit générateur de signal d'adresse interne sensible à un signal de borne d'entrée d'adresse pour générer un premier signal d'adresse interne ;

un second circuit générateur de signal d'adresse interne sensible au premier signal d'adresse interne pour successivement générer un deuxième signal d'adresse interne pendant un fonctionnement en mode salve ; et

un circuit pour sélectionner l'un ou l'autre du premier signal d'adresse interne ou du deuxième signal d'adresse interne et générer un troisième signal d'adresse en synchronisant le signal sélectionné avec un signal d'horloge externe ou un signal de commande externe.

5. Dispositif selon la revendication 1, dans lequel ladite partie de mémoire principale (101), ladite partie de sous-mémoire (102) et lesdits registres (503) sont formés sur une puce unique.

6. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel ladite partie de sous-mémoire (102) a une vitesse d'accès supérieure à la vitesse d'accès de ladite partie de mémoire principale (101).

7. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel une allocation, une attribution, ou une réattribution desdits groupes de cellules de mémoire est reçue pour chaque demande d'une pluralité de demandes d'accès reçues.

8. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel des opérations d'entrée / sortie de données multiples sont successivement effectuées en l'absence de tout signal de commande de données externe et de tout signal de trai-

tement de commande de données externe.

9. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel des cellules de mémoire agencées en une colonne de ladite partie de mémoire principale (101) sont connectées à des cellules de mémoire agencées en une colonne de ladite partie de sous-mémoire (102). 5
10. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel ladite partie de mémoire principale (101) comprend une pluralité de groupes de cellules de mémoire agencés chacun en une pluralité de rangées et en une pluralité de colonnes, et 10
- dans lequel de multiples groupes de ladite pluralité de groupes de cellules de mémoire de ladite partie de mémoire principale (101) sont connectés de manière sélective à un groupe de cellules de mémoire de ladite partie de sous-mémoire (102). 15 20
11. Dispositif de mémoire à semi-conducteur selon la revendication 1, dans lequel un signal d'adresse est utilisé pour fixer un mode d'entrée / sortie de données de chacun desdits groupes de cellules de mémoire automatiquement, sans signal de commande de données externe ou sans signal de commande de traitement de données externe, quand le groupe de cellules de mémoire est sélectionné. 25 30

35

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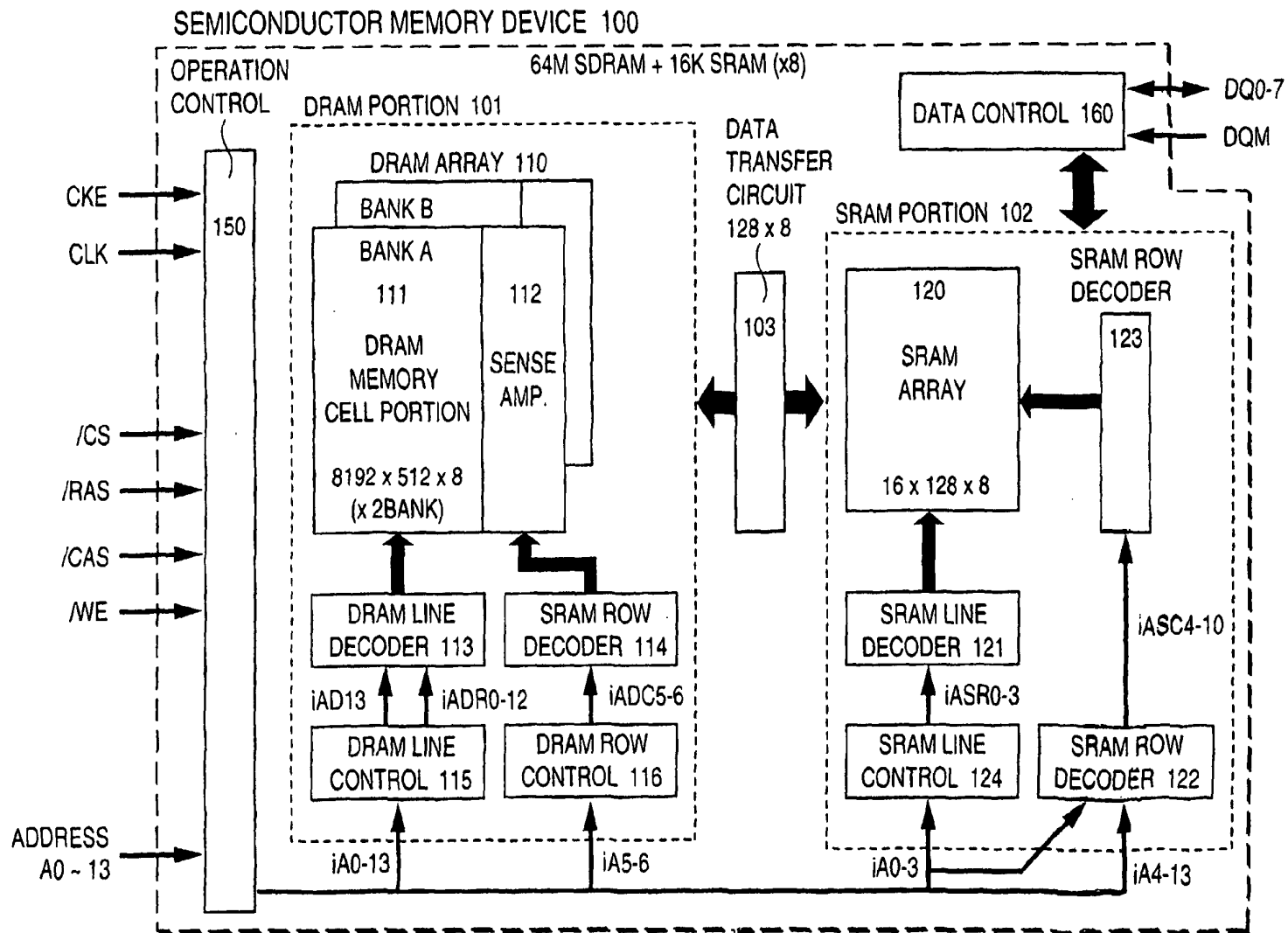


FIG. 1

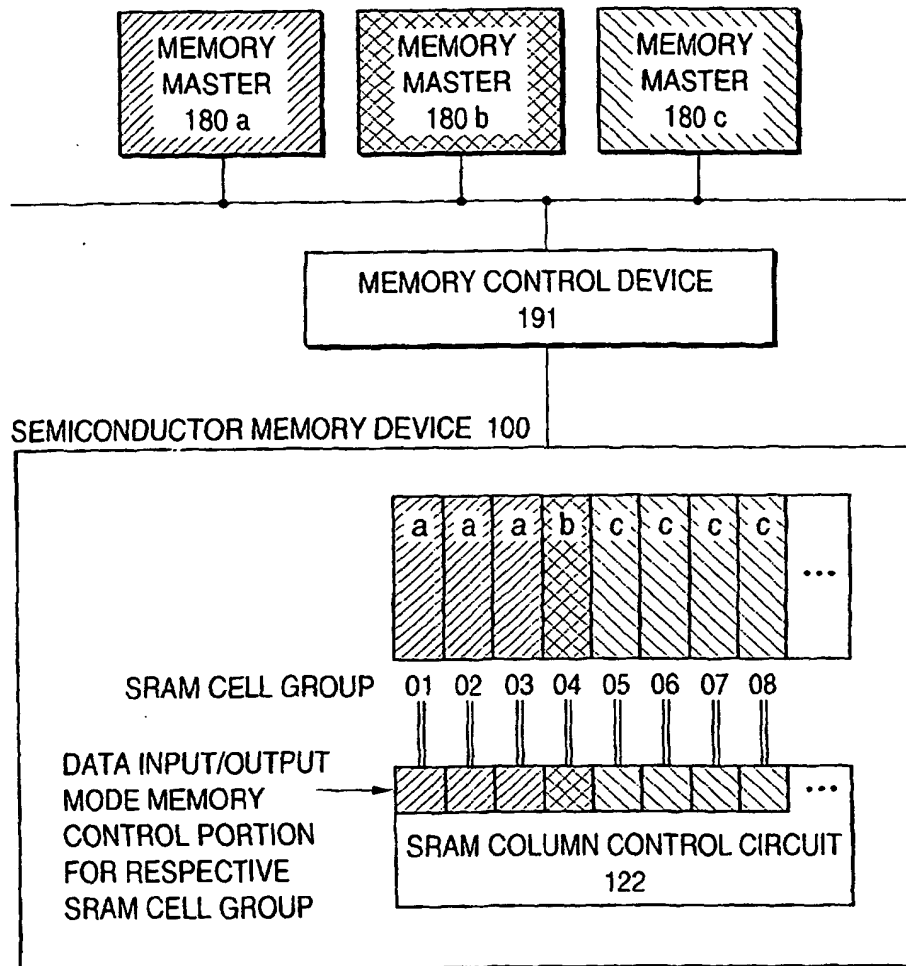


FIG. 2

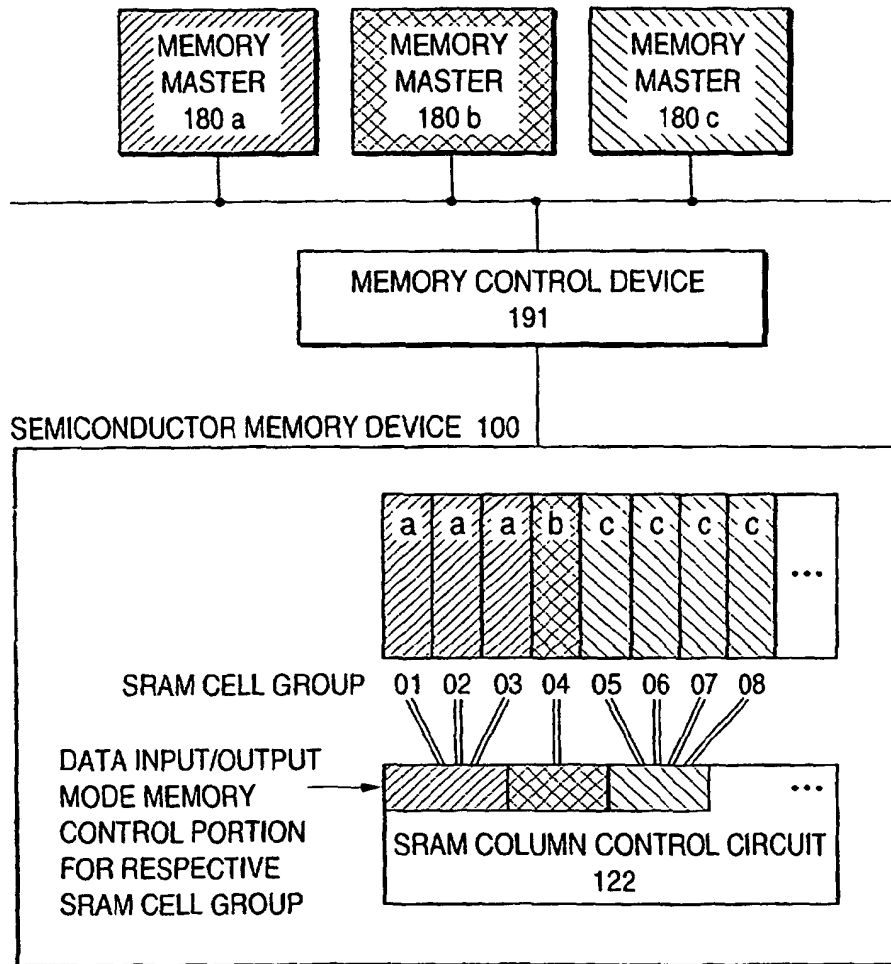


FIG. 3

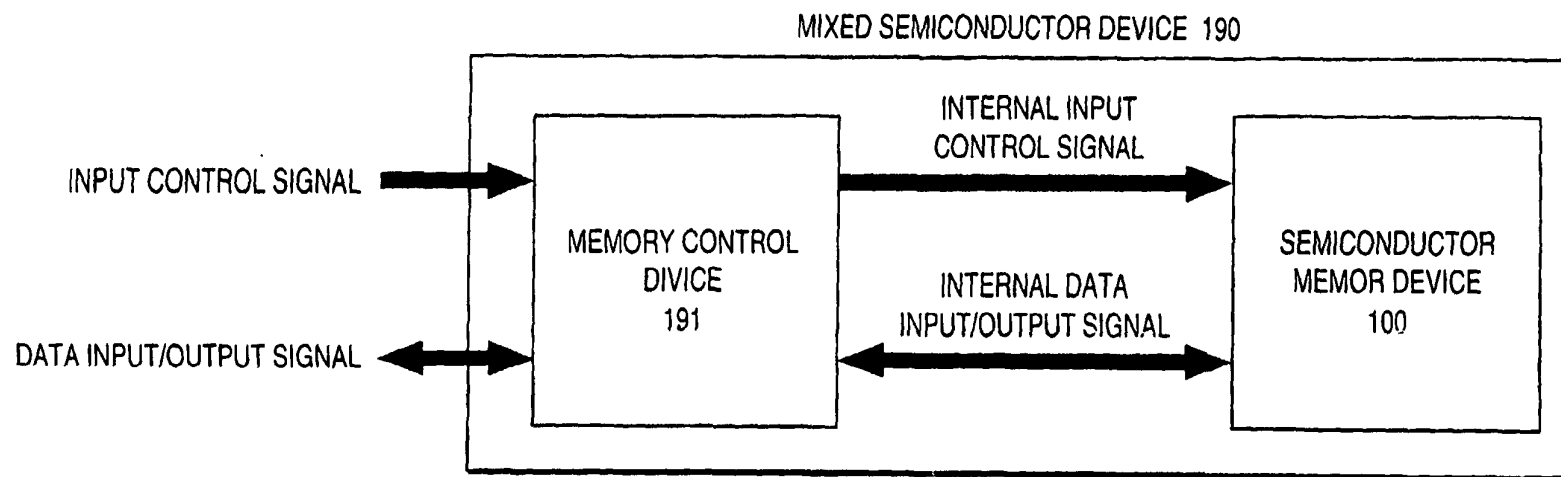


FIG. 4

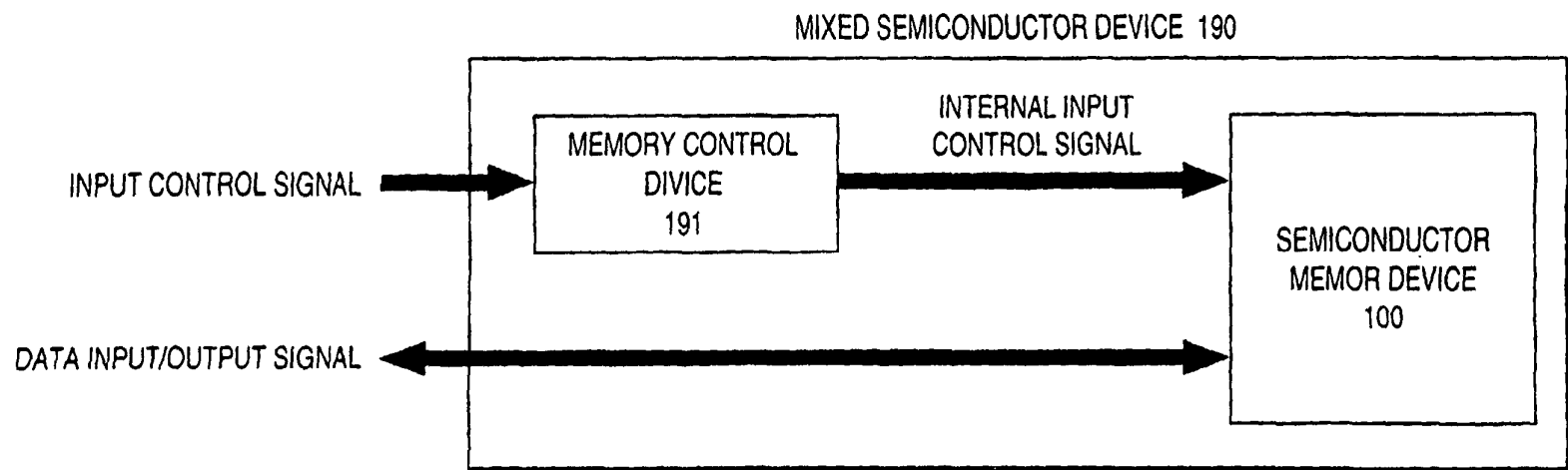


FIG. 5

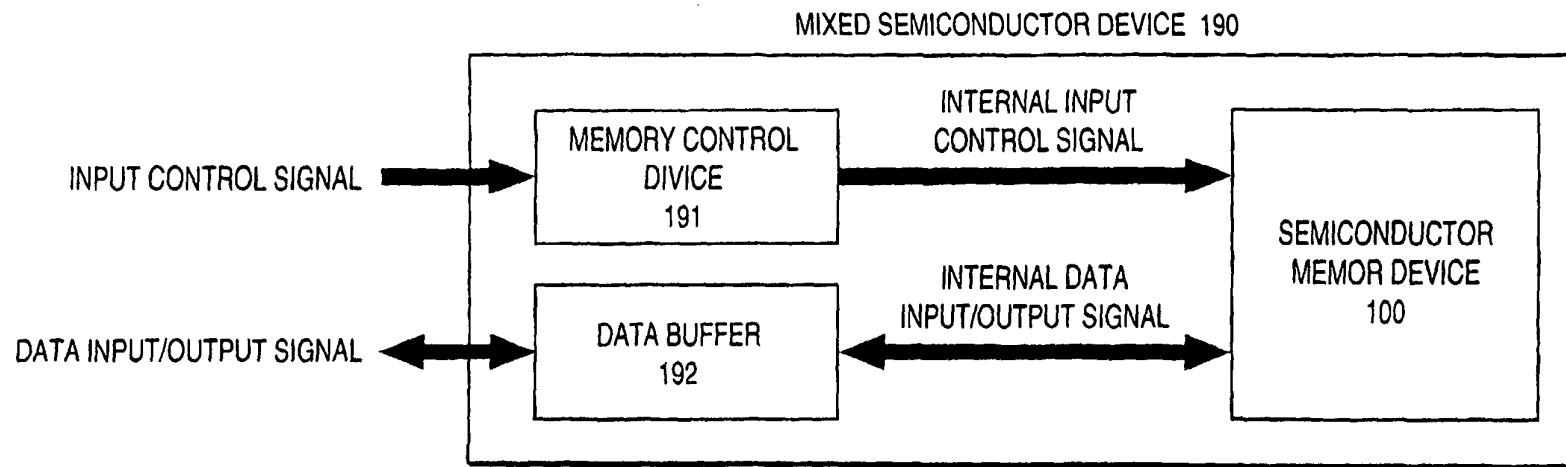


FIG. 6

PIN ARRANGEMENT

64M SDRAM + 16K SRAM (x 8)

Vcc	1	54	Vss
DQ0	2	53	DQ7
VccQ	3	52	VssQ
NC	4	51	NC
DQ1	5	50	DQ6
VssQ	6	49	VccQ
NC	7	48	NC
DQ2	8	47	DQ5
VccQ	9	46	VssQ
NC	10	45	NC
DQ3	11	44	DQ4
VssQ	12	43	VccQ
NC	13	42	NC
Vcc	14	41	Vss
NC	15	40	NC, VREF
/WE	16	39	DQM
/CAS	17	38	CLK
/RAS	18	37	CKE
/CS	19	36	NC
A13 (BA)	20	35	A11
A12	21	34	A9
A10 (AP)	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
Vcc	27	28	Vss

FIG. 7

PIN ARRANGEMENT

64M SDRAM + 16K SRAM (x 4)

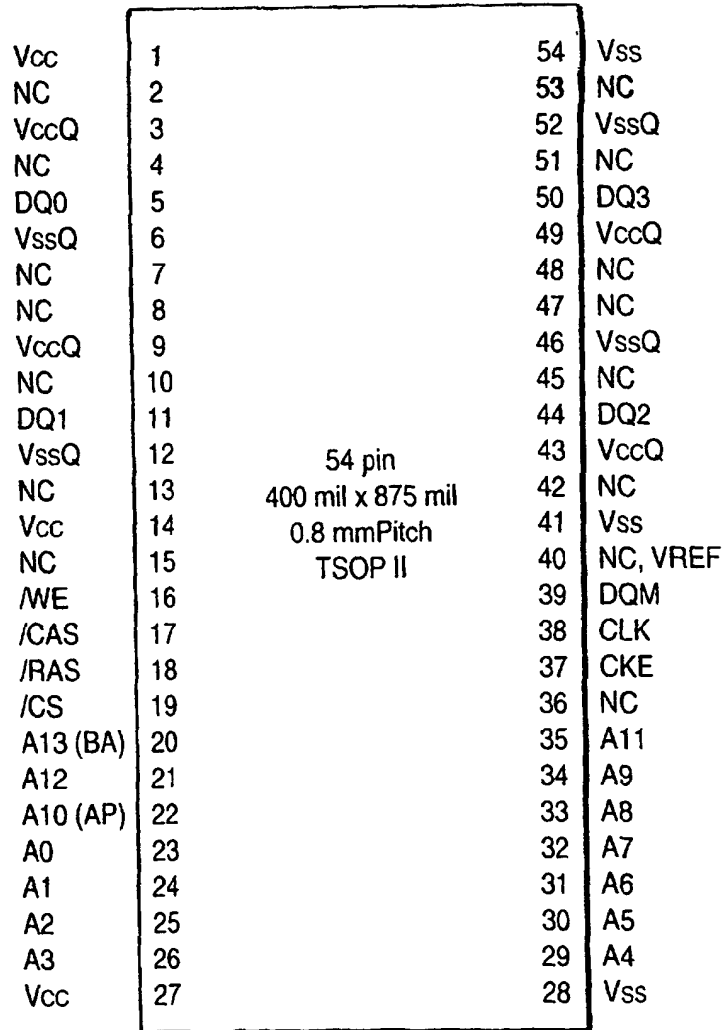


FIG. 8

PIN ARRANGEMENT

64M SDRAM + 16K SRAM (x 4)

Vcc	1	54	Vss
DQ0	2	53	DQ15
VccQ	3	52	VssQ
DQ1	4	51	DQ14
DQ2	5	50	DQ13
VssQ	6	49	VccQ
DQ3	7	48	DQ12
DQ4	8	47	DQ11
VssQ	9	46	VssQ
DQ5	10	45	DQ10
DQ6	11	44	DQ9
VssQ	12	43	VccQ
DQ7	13	42	DQ8
Vcc	14	41	Vss
LDQM	15	40	NC, VREF
/WE	16	39	UDQM
/CAS	17	38	CLK
/RAS	18	37	CKE
/CS	19	36	NC
A13 (BA)	20	35	A11
A12	21	34	A9
A10 (AP)	22	33	A8
A0	23	32	A7
A1	24	31	A6
A2	25	30	A5
A3	26	29	A4
Vcc	27	28	Vss

FIG. 9

CORRESPONDENCE BETWEEN COMMANDS AND INPUT TERMINAL STATES

	COMMAND	CKE		/CS	/RAS	/CAS	/WE	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
		n-1	n																		
①	READ	H	x	L	H	L	H	x	x	x	SRAM COLUMN SELECTION						SRAM ROW SELECTION				
②	WRITE	H	x	L	H	L	L	x	x	x	SRAM COLUMN SELECTION						SRAM ROW SELECTION				
③	PREFETCH	H	x	L	H	H	L	BANK SELECTION	x	x	L	L	x	x			x	SRAM ROW SELECTION			
④	PREFETCH (AUTO PRECHARGE)	H	x	L	H	H	L	BANK SELECTION	x	x	H	L	x	x			x	SRAM ROW SELECTION			
⑤	RESTORE	H	x	L	H	H	L	BANK SELECTION	x	x	L	H	x	x			x	SRAM ROW SELECTION			
⑥	RESTORE (AUTO PRECHARGE)	H	x	L	H	H	L	BANK SELECTION	DRAM ROW SELECTION												
									x	x	H	H	x	x			x	SRAM ROW SELECTION			
⑦	ACTIVE	H	x	L	L	H	H	BANK SELECTION	DRAM ROW SELECTION						DRAM COLUMN SELECTION						
⑧	PRECHARGE	H	x	L	L	H	L	BANK SELECTION	x	x	L	x	x	x	x	x	x	x	x	x	x
⑨	ALL BANK PRECHARGE	H	x	L	L	H	L	x	x	x	H	x	x	x	x	x	x	x	x	x	x
⑩	CBR REFRESH	H	x	L	L	L	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x
⑪	NON-OPERATION	H	x	L	H	H	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x
⑫	DEVICE NON-SELECTION	H	x	H	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
⑬	REGISTER SETTING	(1)	H	x	L	L	L	REGISTER SETTING													
	(2)	H	x	L	L	L	L	L	L	L	L	L	L	L	H	REGISTER SETTING					
																REGISTER SETTING					

H: HIGH LEVEL L: LOW LEVEL x: HIGH OR LOW (DON'T CARE)

FIG. 10

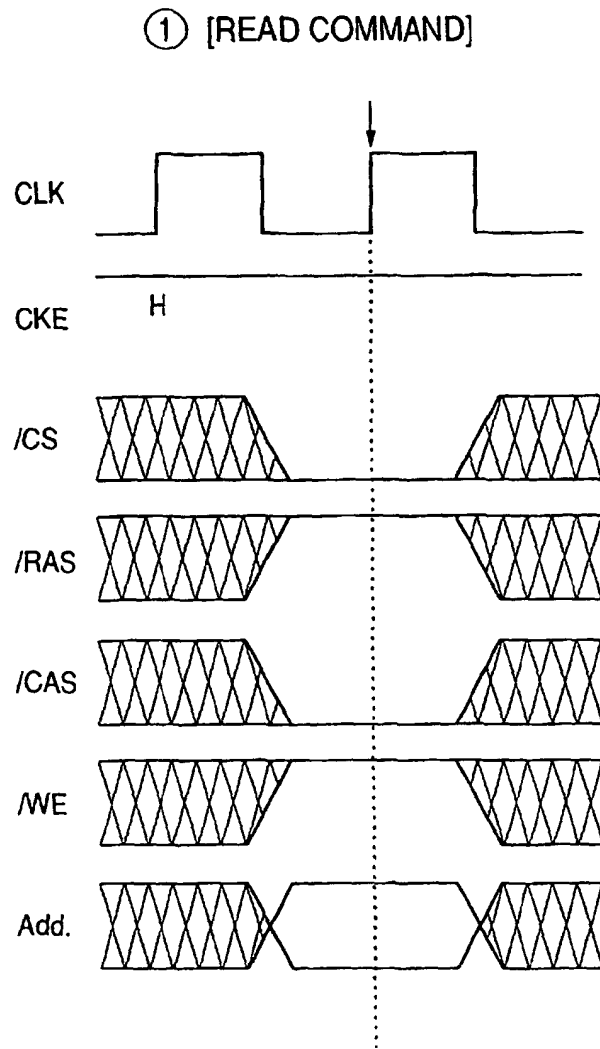


FIG. 11

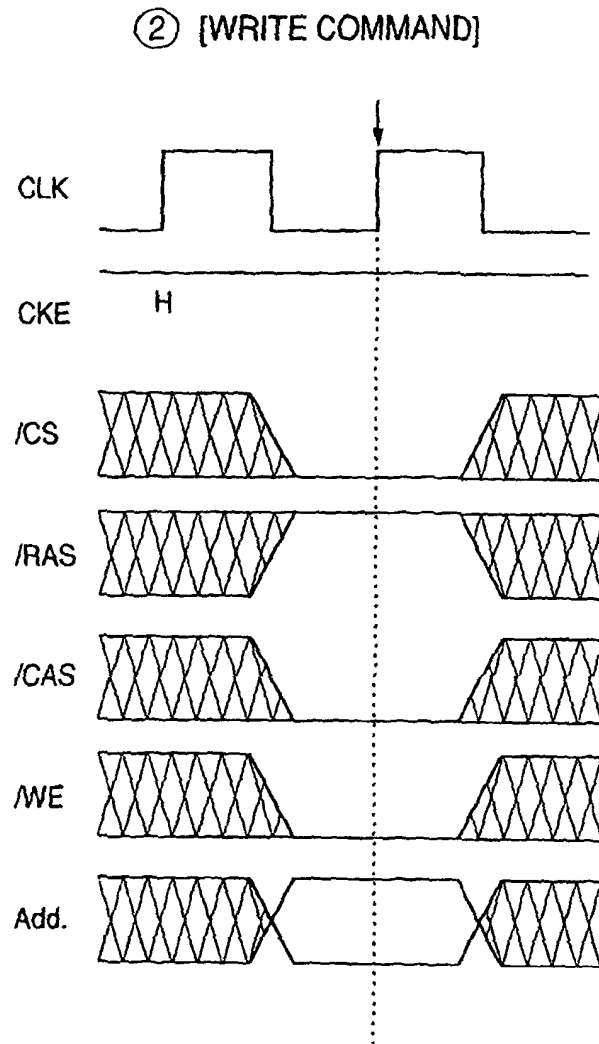


FIG. 12

③ [PREFETCH COMMAND]

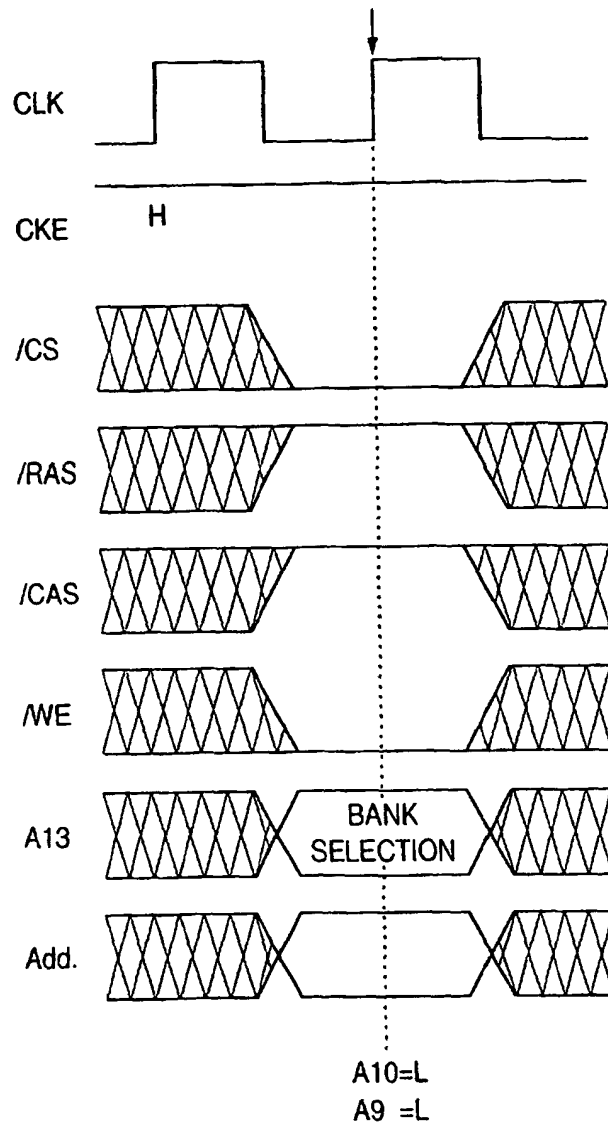


FIG. 13

④ [PREFETCH (AUTO PRECHARGE) COMMAND]

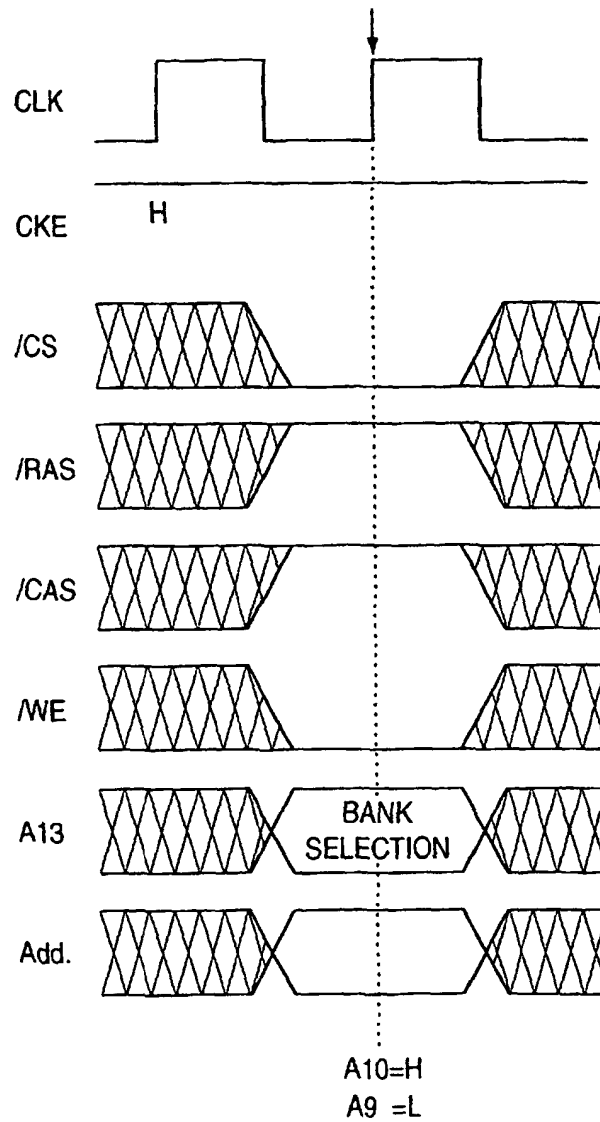


FIG. 14

⑤ [RESTORE COMMAND]

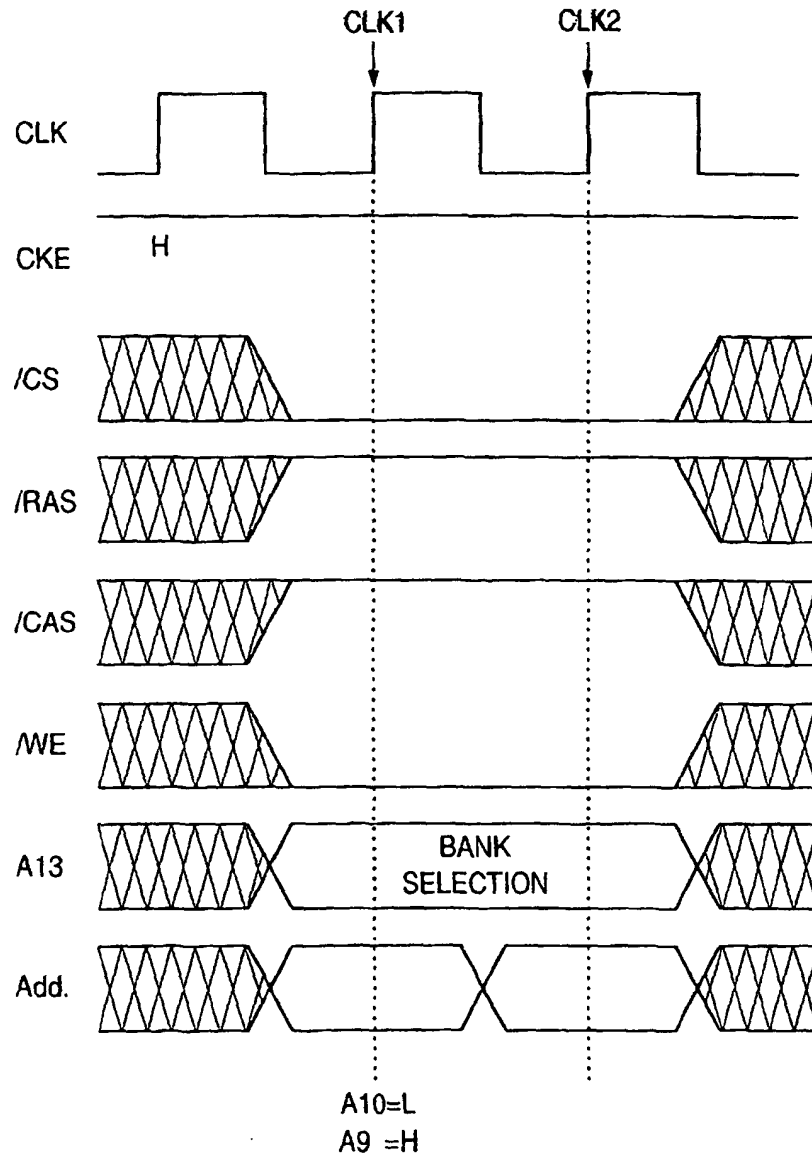


FIG. 15

⑥ [RESTORE (AUTO PRECHARGE) COMMAND]

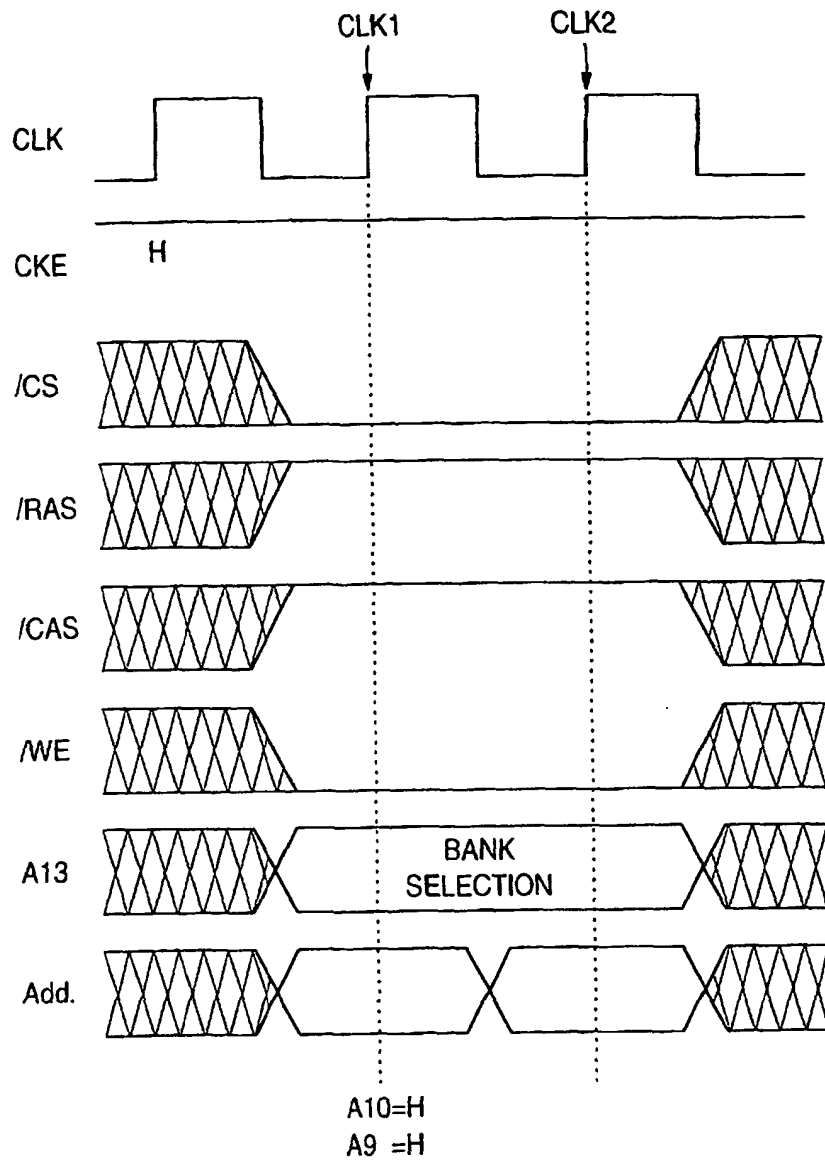


FIG. 16

⑦ [ACTIVE COMMAND]

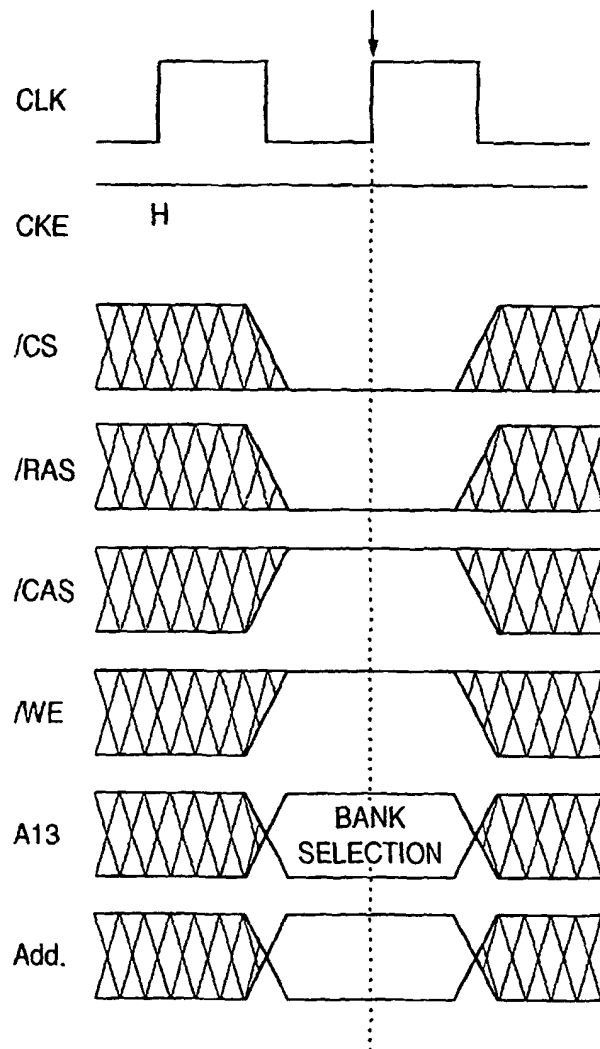


FIG. 17

⑧ [PRECHARGE COMMAND]

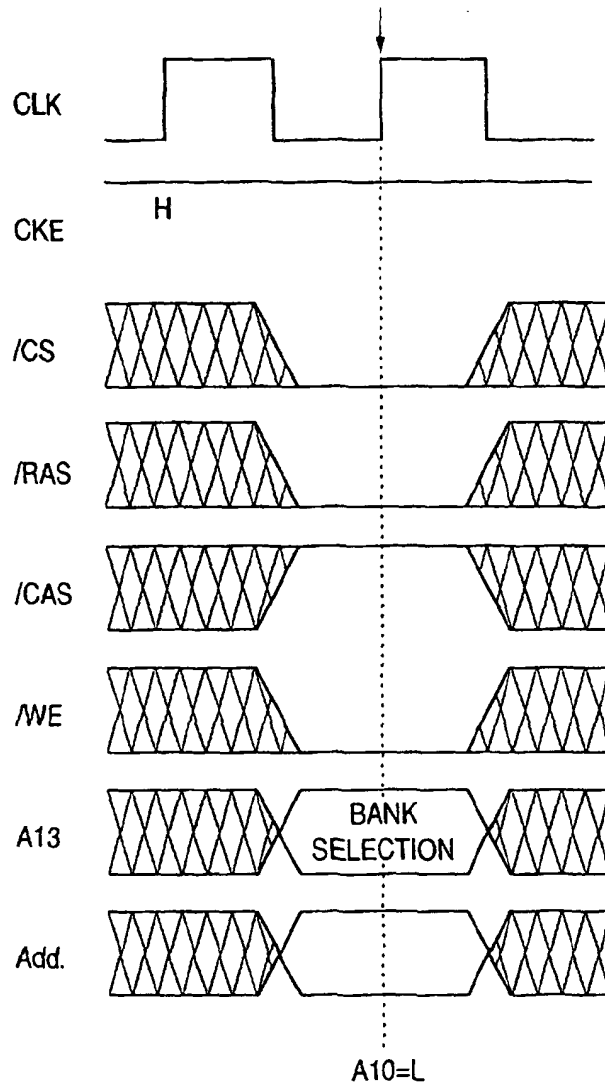


FIG. 18

⑨ [ALL BANK PRECHARGE COMMAND]

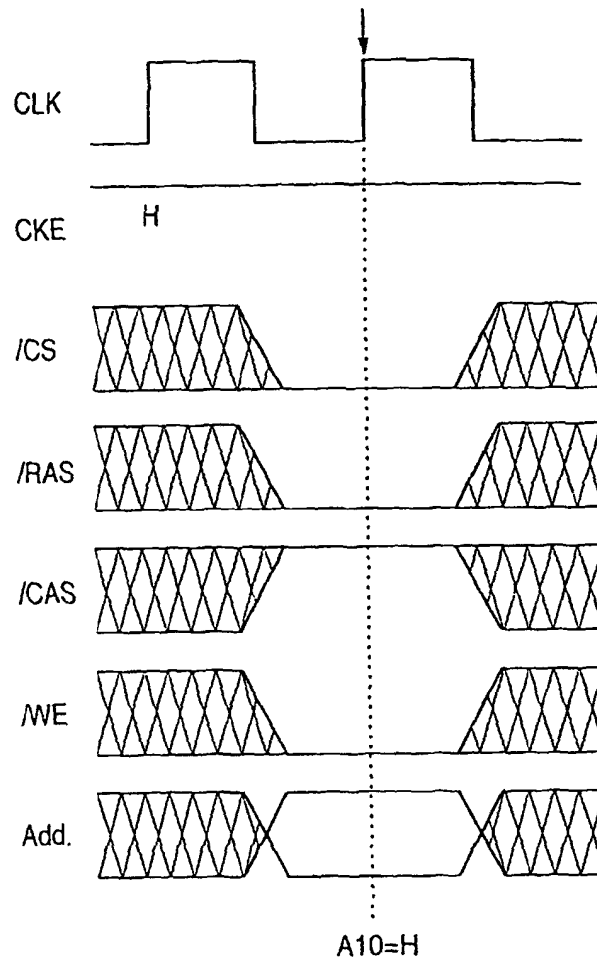


FIG. 19

⑩ [CBR REFRESH COMMAND]

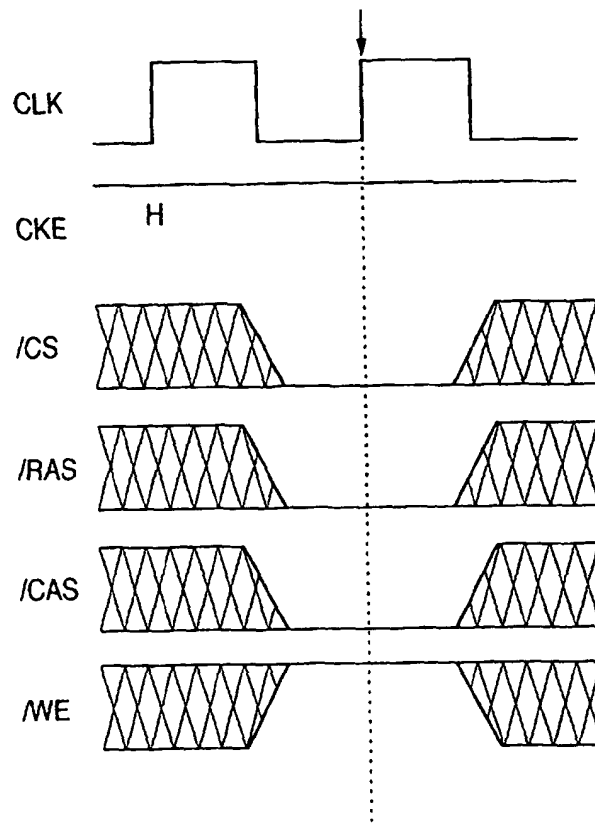


FIG. 20

⑪ [NON-OPERATION COMMAND]

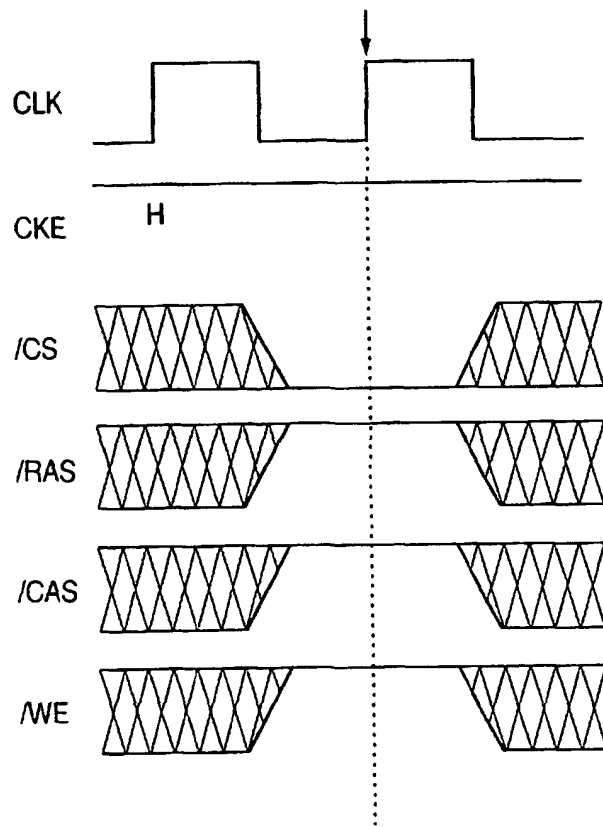


FIG. 21

⑫ [DEVICE NON-SELECTION COMMAND]

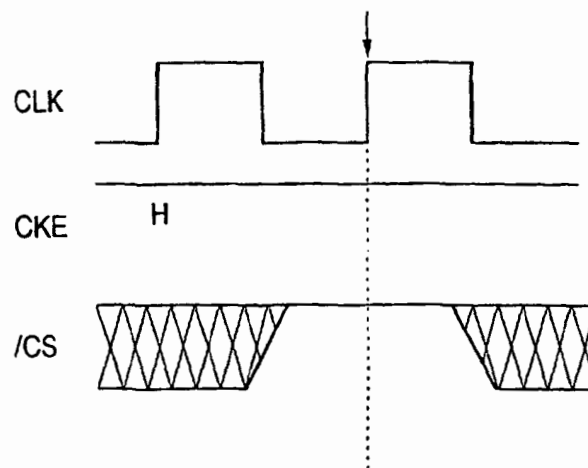


FIG. 22

⑬ (1) [MODE REGISTER SETTING (1) COMMAND] OF
[REGISTER SETTING COMMAND] (a), (b), (c) AND (d)

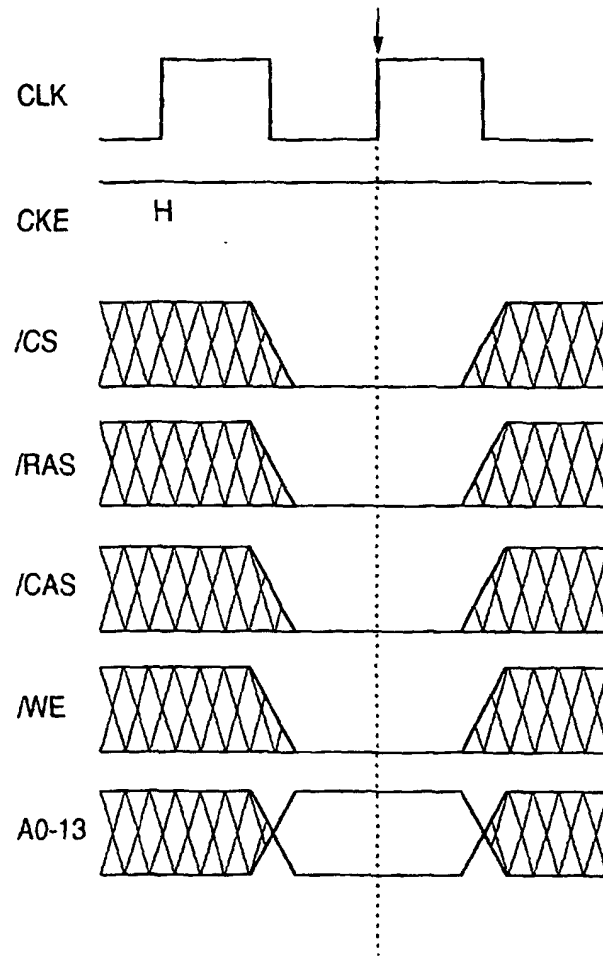


FIG. 23

⑬ (2) [MODE REGISTER SETTING (2) COMMAND] OF
[REGISTER SETTING COMMAND] (d)

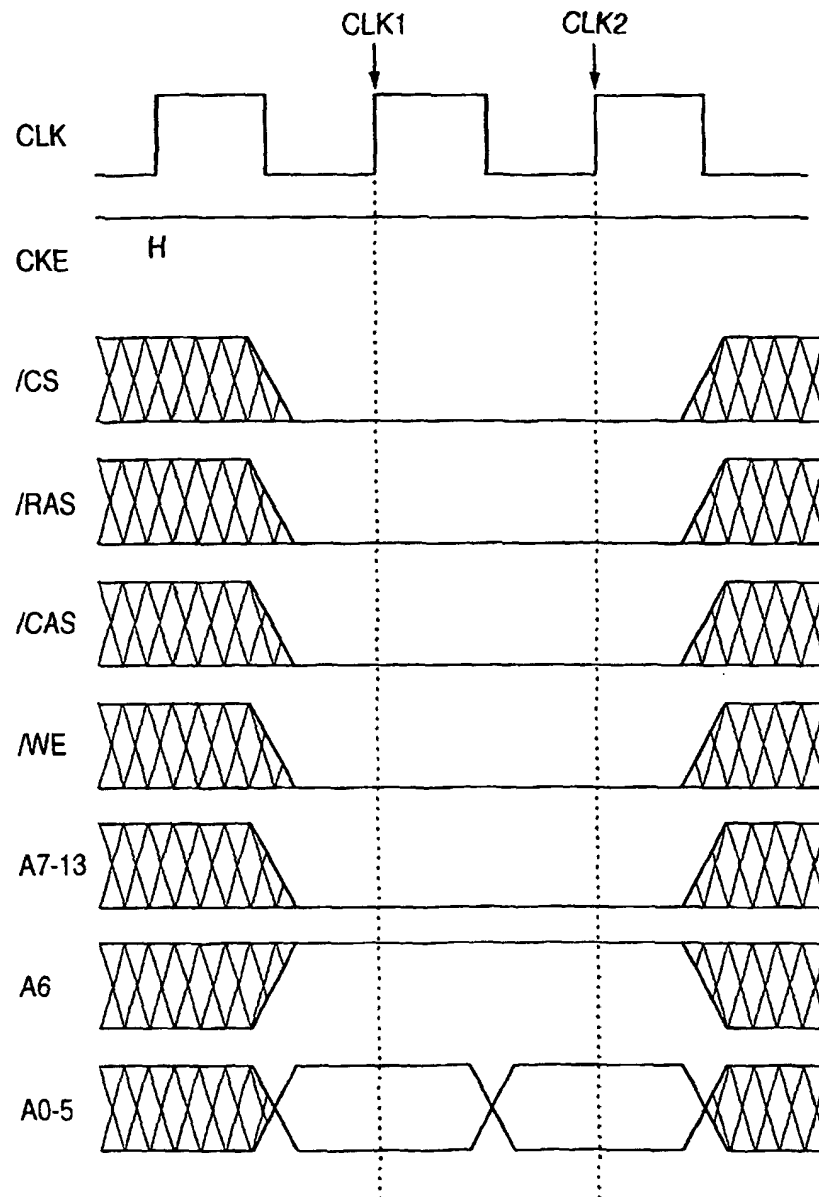


FIG. 24

REGISTER SETTING

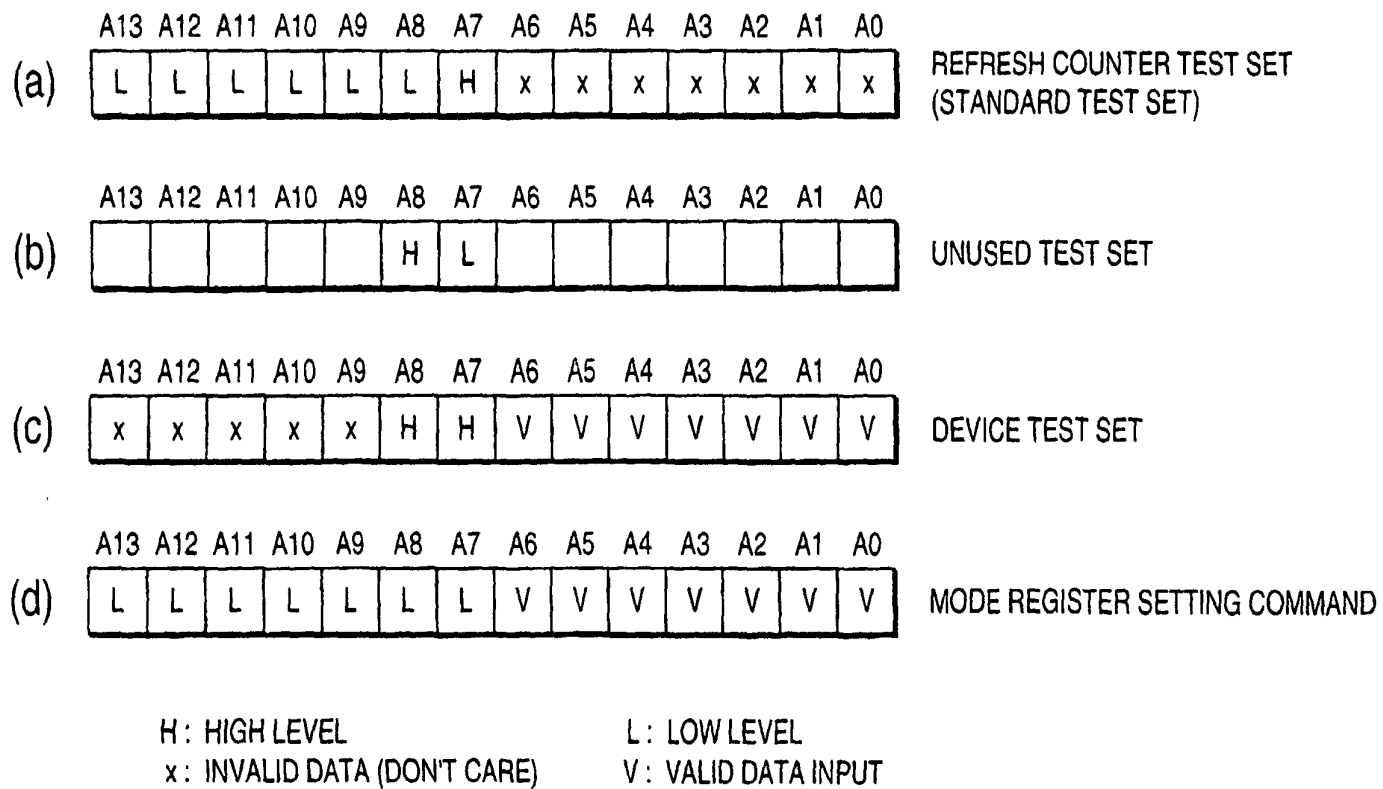


FIG. 25

MODE REGISTER SETTING COMMAND

MODE REGISTER SETTING (1) COMMAND

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
L	L	L	L	L	L	L	L	x	x	LATENCY	LAP TYPE		

LATENCY			
A3	A2	A1	CAS LATENCY
L	L	L	UNUSE
L	L	H	UNUSE
L	H	L	2
L	H	H	UNUSE
H	L	L	UNUSE
H	L	H	UNUSE
H	H	H	UNUSE
H	H	H	UNUSE

A0	LAP TYPE
L	SEQUENTIAL
H	INTERLEAVE

BURST LENGTH				
A5	A4	A3	SEQUENTIAL	INTERLEAVE
L	L	L	1	1
L	L	H	2	2
L	H	L	4	4
L	H	H	8	8
H	L	L	16	16
H	L	H	UNUSE	UNUSE
H	L	L	UNUSE	UNUSE
H	H	H	UNUSE	UNUSE

MODE REGISTER SETTING (2) COMMAND

CLK2	L	L	L	L	L	L	L	H	BURST LENGTH	x	x	x
------	---	---	---	---	---	---	---	---	--------------	---	---	---

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----

CLK1	L	L	L	L	L	L	L	H	UNUSE	SRAM ROW DATA			
------	---	---	---	---	---	---	---	---	-------	---------------	--	--	--

FIG. 26

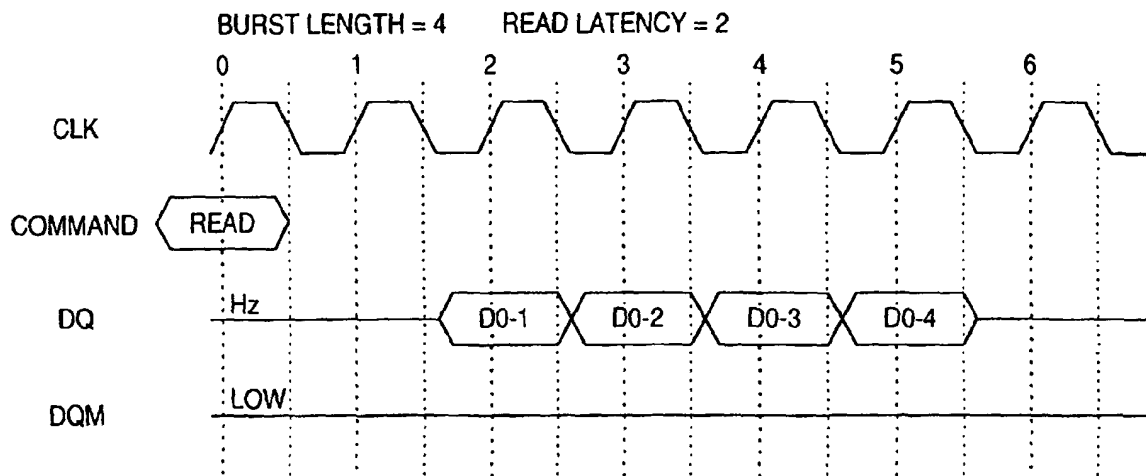


FIG. 27

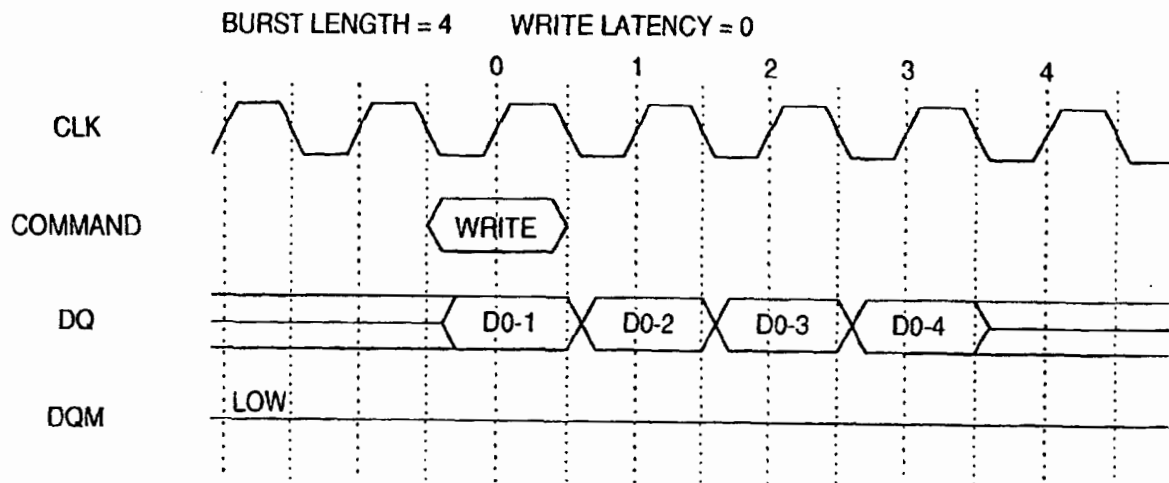


FIG. 28

LAP TYPE AND BURST ADDRESS SEQUENCE

BURST LENGTH = 2		LAP TYPE	
START ADDRESS (A0)		SEQUENTIAL	INTERLEAVE
0		0, 1	0, 1
1		1, 0	1, 0

BURST LENGTH = 4		LAP TYPE	
START ADDRESS (A1 - A0)		SEQUENTIAL	INTERLEAVE
0 0		0, 1, 2, 3	0, 1, 2, 3
0 1		1, 2, 3, 0	1, 0, 3, 2
1 0		2, 3, 0, 1	2, 3, 0, 1
1 1		3, 0, 1, 2	3, 2, 1, 0

BURST LENGTH = 8		LAP TYPE	
START ADDRESS (A2 - A0)		SEQUENTIAL	INTERLEAVE
0 0 0		0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
0 0 1		1, 2, 3, 4, 5, 6, 7, 0	1, 0, 3, 2, 5, 4, 7, 6
0 1 0		2, 3, 4, 5, 6, 7, 0, 1	2, 3, 0, 1, 6, 7, 4, 5
0 1 1		3, 4, 5, 6, 7, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4
1 0 0		4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
1 0 1		5, 6, 7, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2
1 1 0		6, 7, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1
1 1 1		7, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0

BURST LENGTH = 16		LAP TYPE	
START ADDRESS (A3 - A0)		SEQUENTIAL	INTERLEAVE
0 0 0 0		0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15
0 0 0 1		1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0	1, 0, 3, 2, 5, 4, 7, 6, 9, 8, 11, 10, 13, 12, 15, 14
0 0 1 0		2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1	2, 3, 0, 1, 6, 7, 4, 5, 10, 11, 8, 9, 14, 15, 12, 13
0 0 1 1		3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2	3, 2, 1, 0, 7, 6, 5, 4, 11, 10, 9, 8, 15, 14, 13, 12
0 1 0 0		4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3, 12, 13, 14, 15, 8, 9, 10, 11
0 1 0 1		5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4	5, 4, 7, 6, 1, 0, 3, 2, 13, 12, 15, 14, 9, 8, 11, 10
0 1 1 0		6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5	6, 7, 4, 5, 2, 3, 0, 1, 14, 15, 12, 13, 10, 11, 8, 9
0 1 1 1		7, 8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6	7, 6, 5, 4, 3, 2, 1, 0, 15, 14, 13, 12, 11, 10, 9, 8
1 0 0 0		8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7	8, 9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7
1 0 0 1		9, 10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8	9, 8, 11, 10, 13, 12, 15, 14, 1, 0, 3, 2, 5, 4, 7, 6
1 0 1 0		10, 11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9	10, 11, 8, 9, 14, 15, 12, 13, 2, 3, 0, 1, 6, 7, 4, 5
1 0 1 1		11, 12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10	11, 10, 9, 8, 15, 14, 13, 12, 3, 2, 1, 0, 7, 6, 5, 4
1 1 0 0		12, 13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	12, 13, 14, 15, 8, 9, 10, 11, 4, 5, 6, 7, 0, 1, 2, 3
1 1 0 1		13, 14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12	13, 12, 15, 14, 9, 8, 11, 10, 5, 4, 7, 6, 1, 0, 3, 2
1 1 1 0		14, 15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13	14, 15, 12, 13, 10, 11, 8, 9, 6, 7, 4, 5, 2, 3, 0, 1
1 1 1 1		15, 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14	15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

FIG. 29

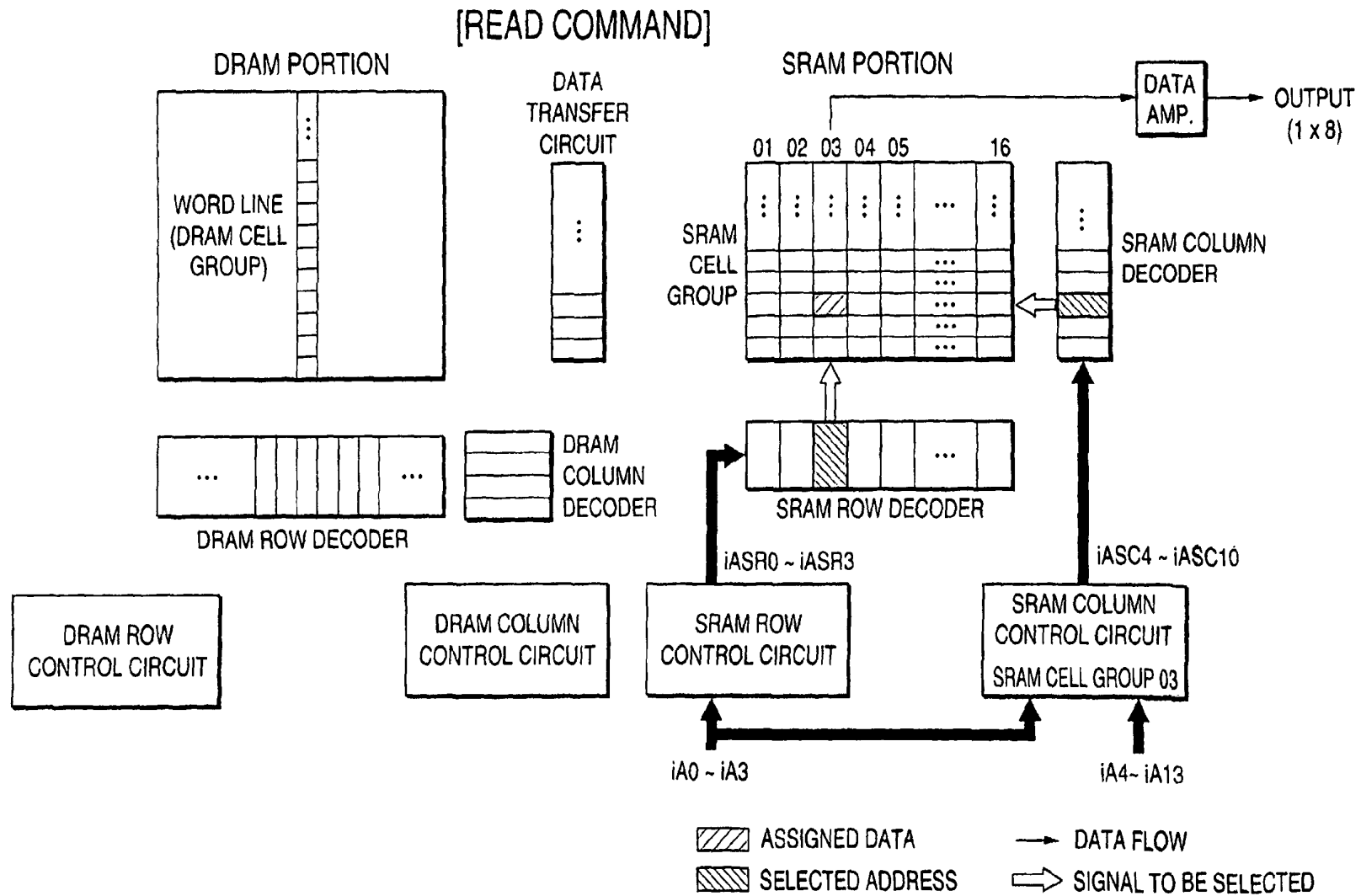


FIG. 30

[WRITE COMMAND]

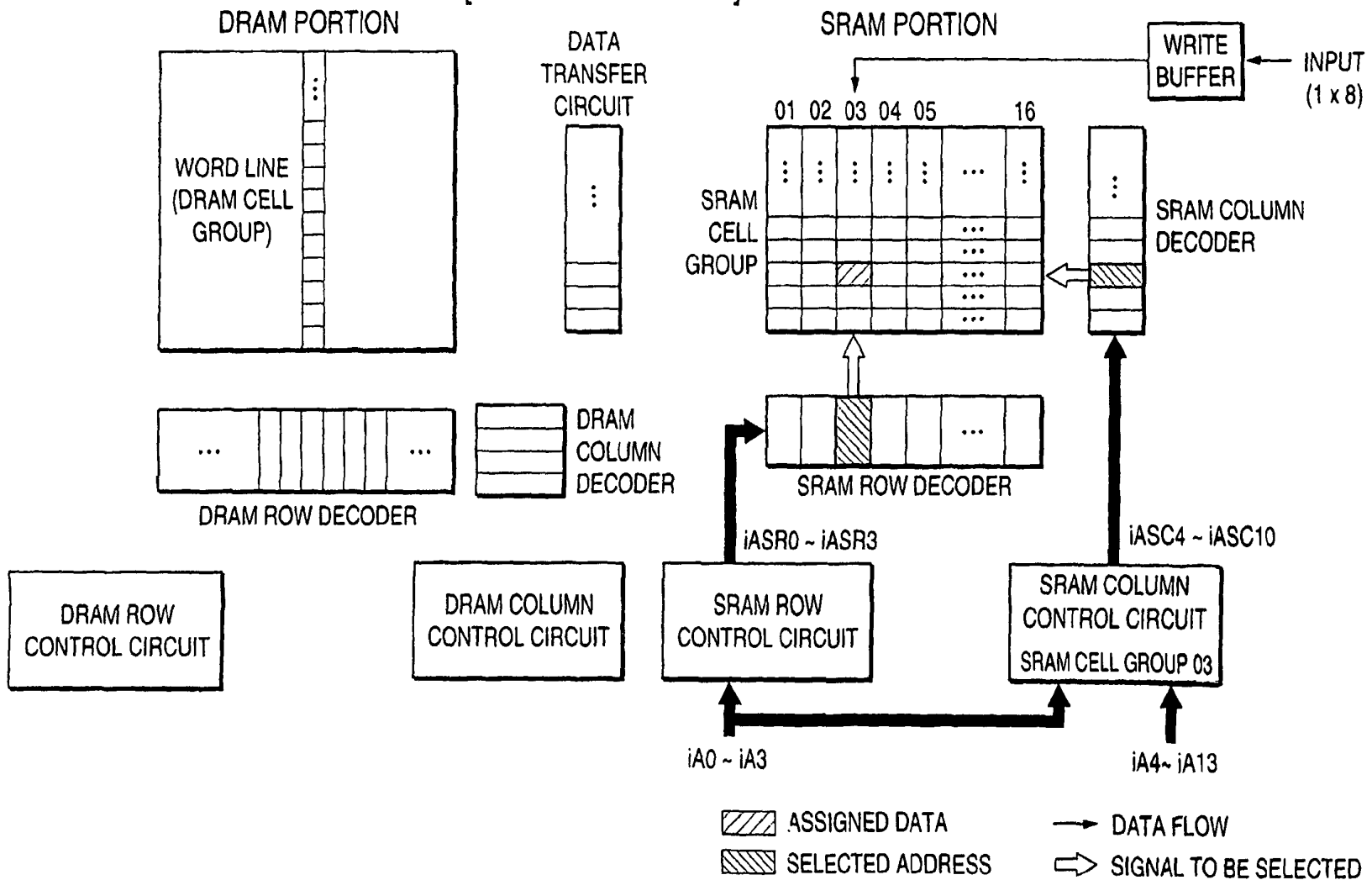


FIG. 31

[PREFETCH COMMAND]

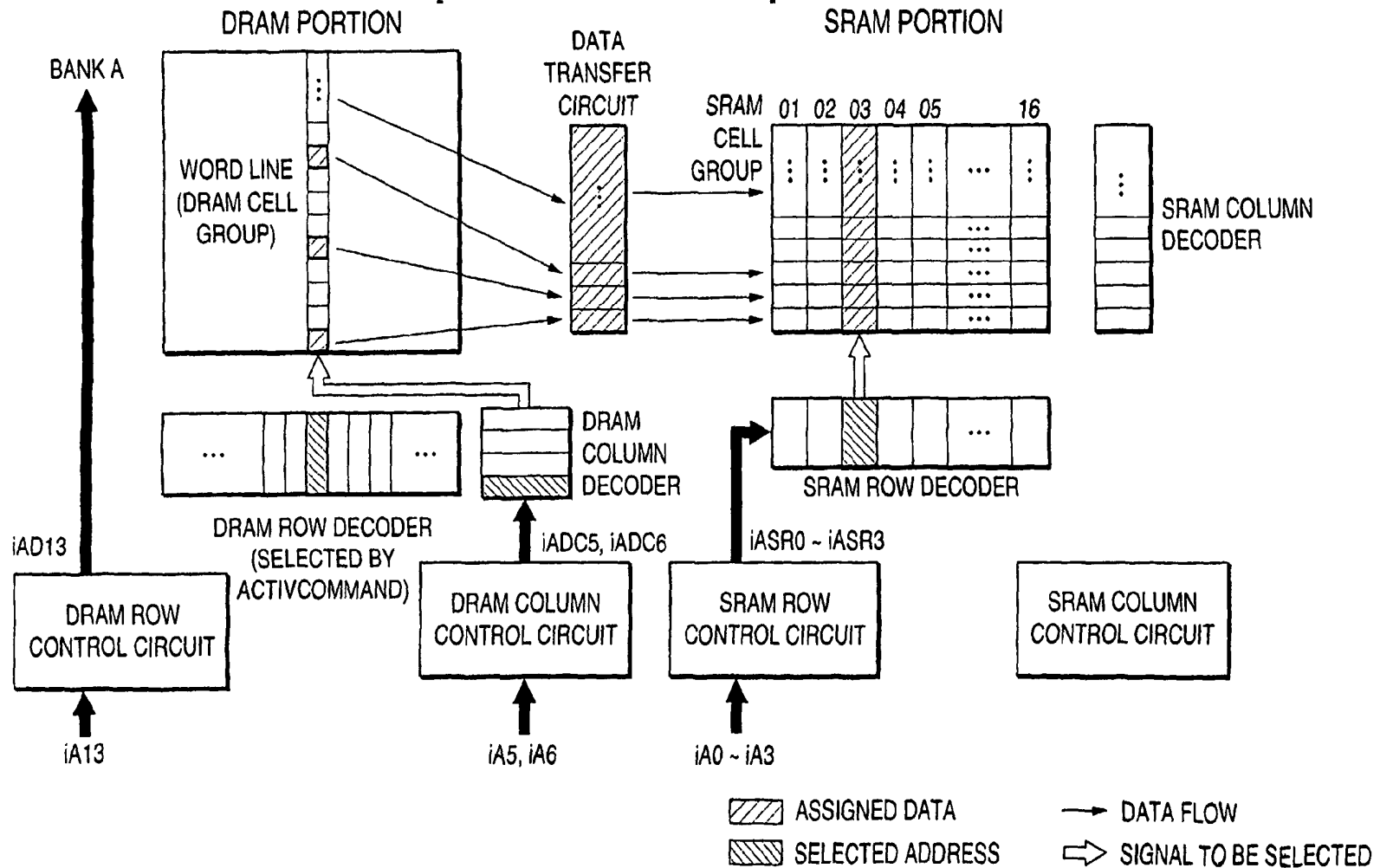


FIG. 32

[RESTORE COMMAND]

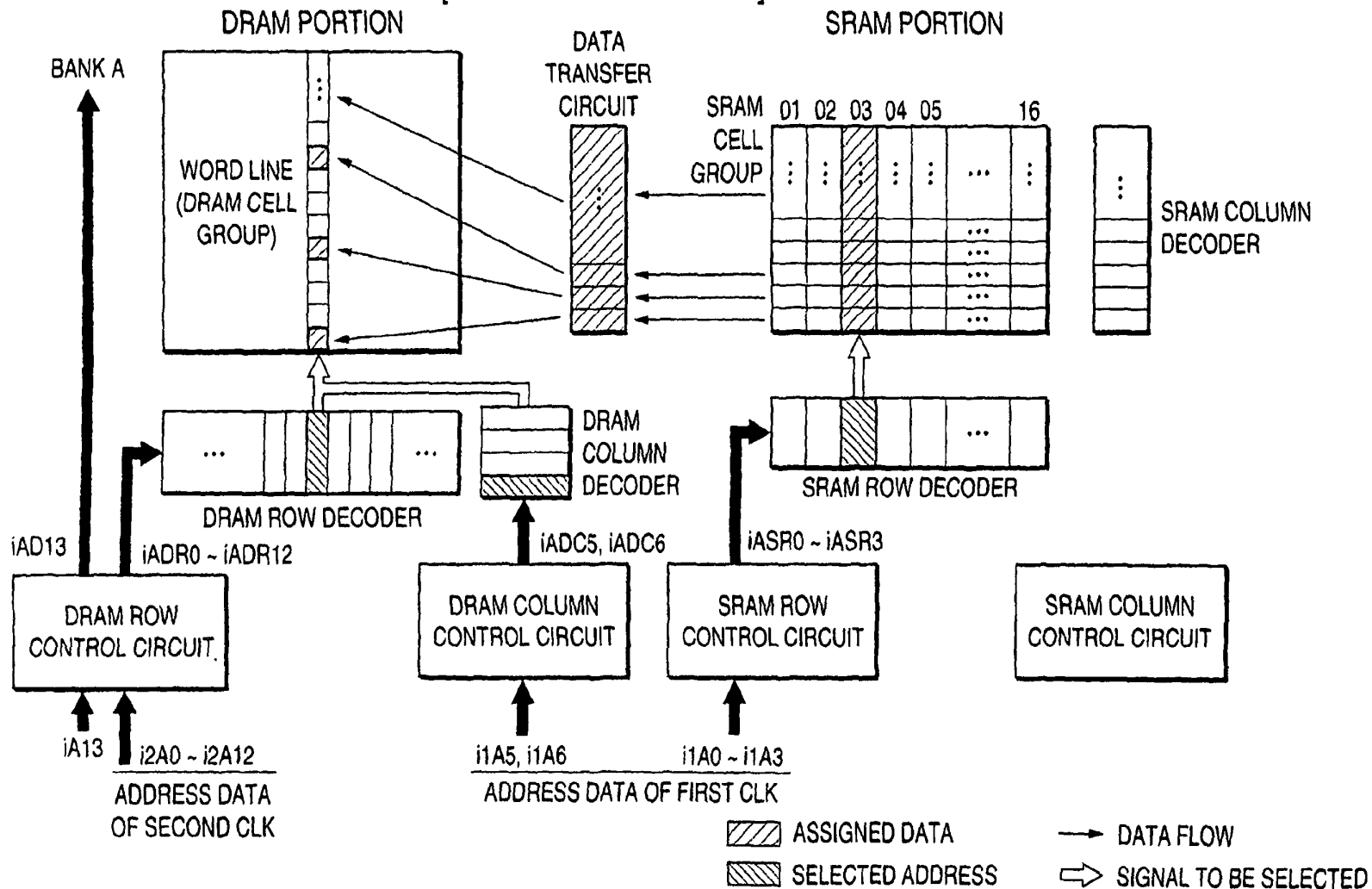


FIG. 33

[ACTIVE COMMAND]

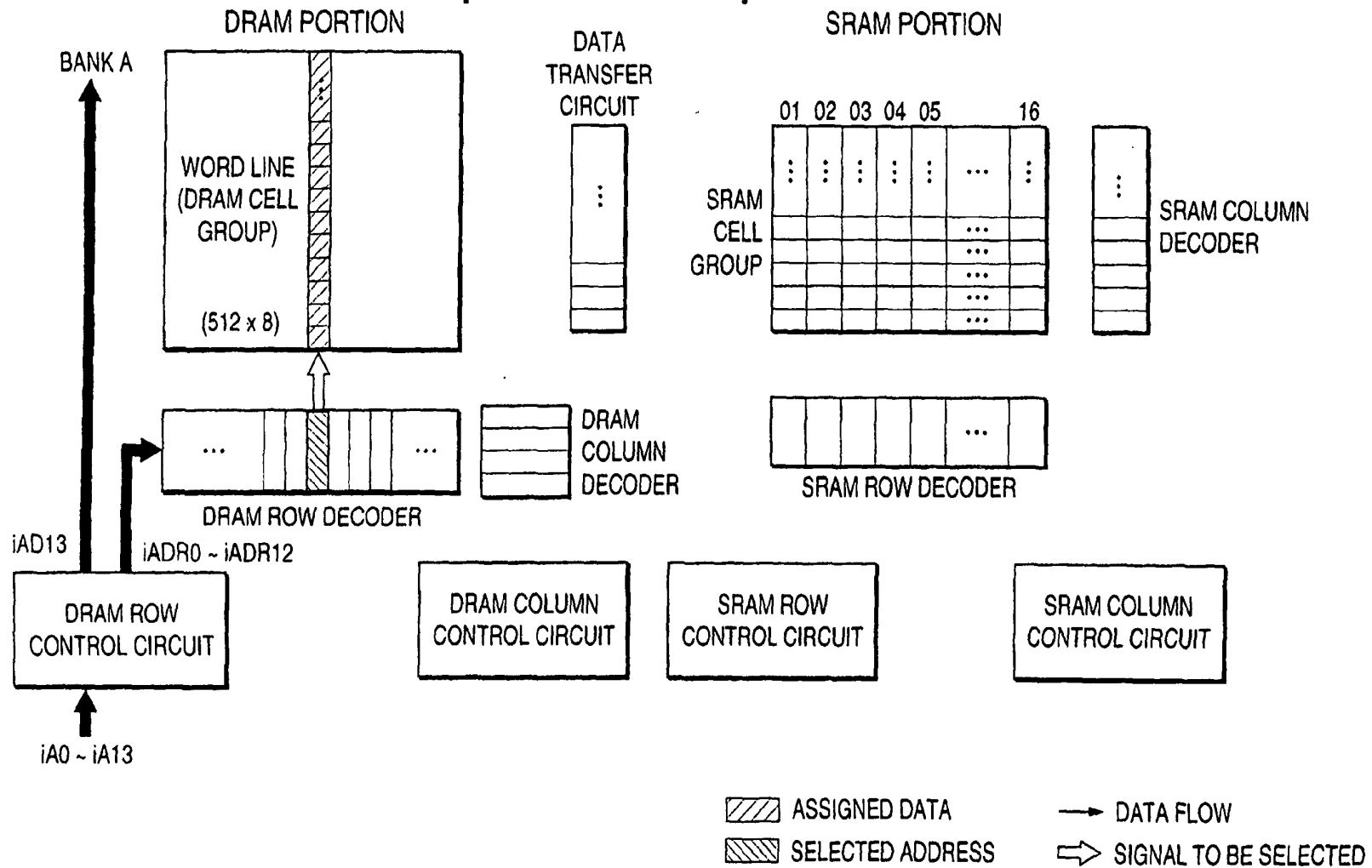


FIG. 34

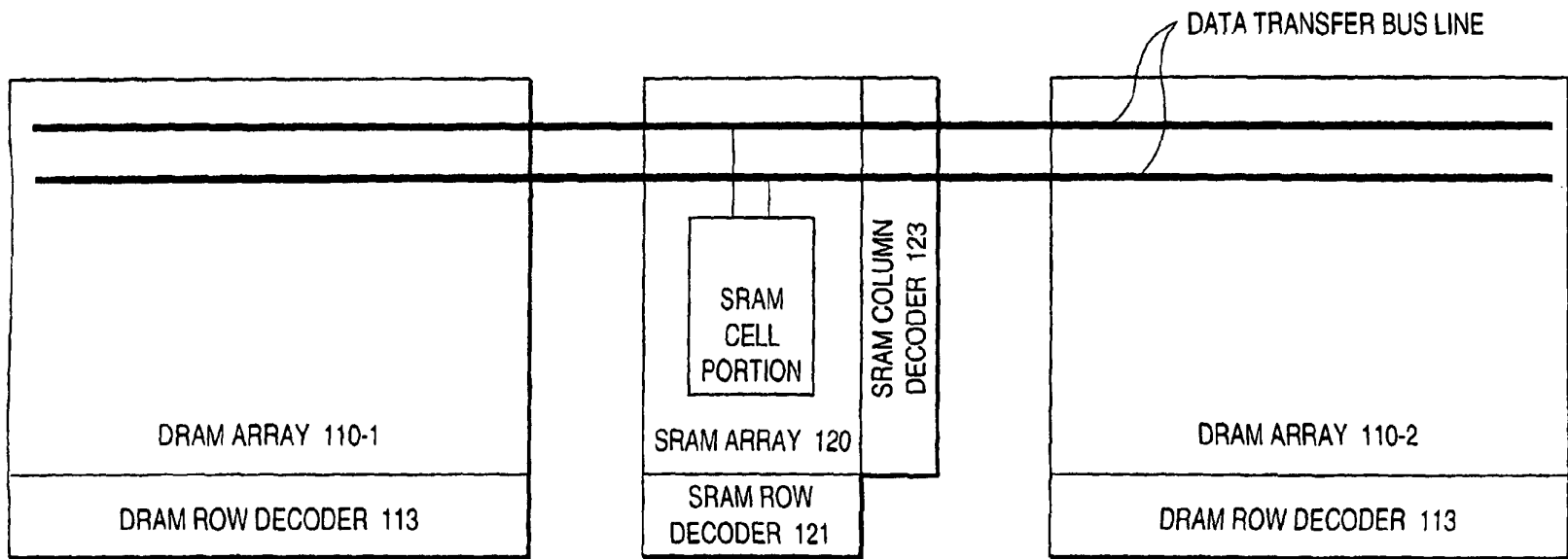


FIG. 35

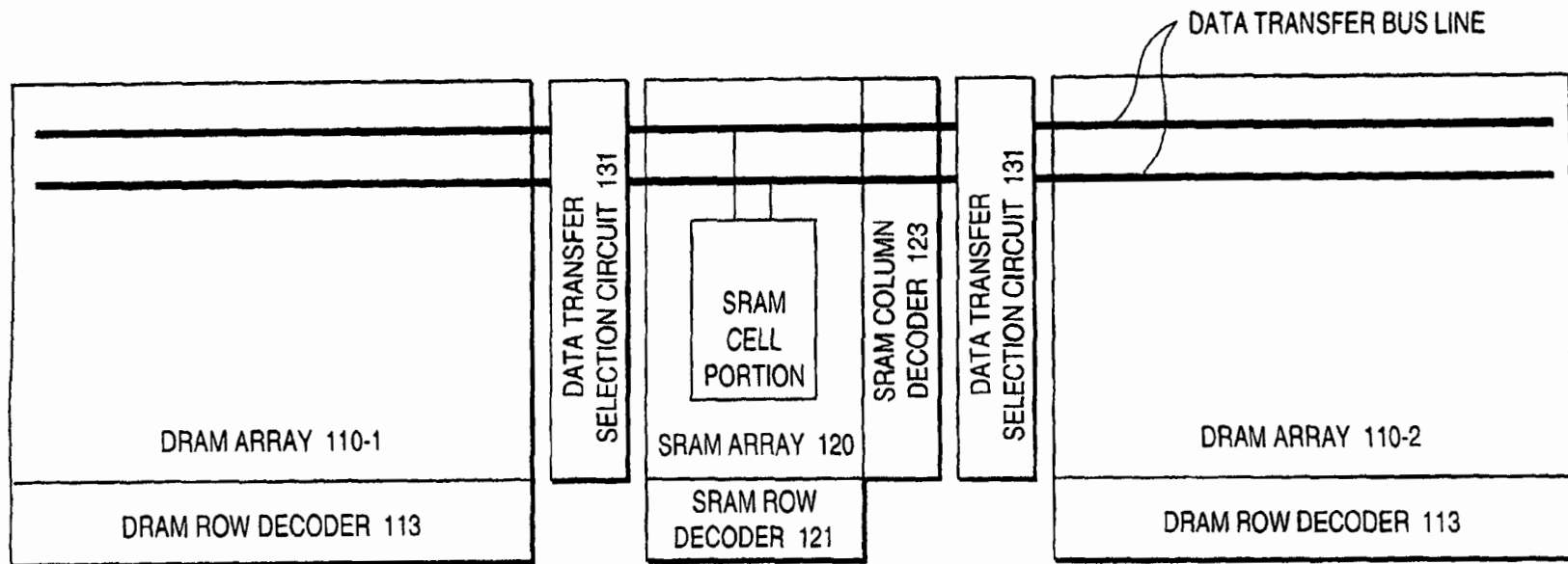


FIG. 36

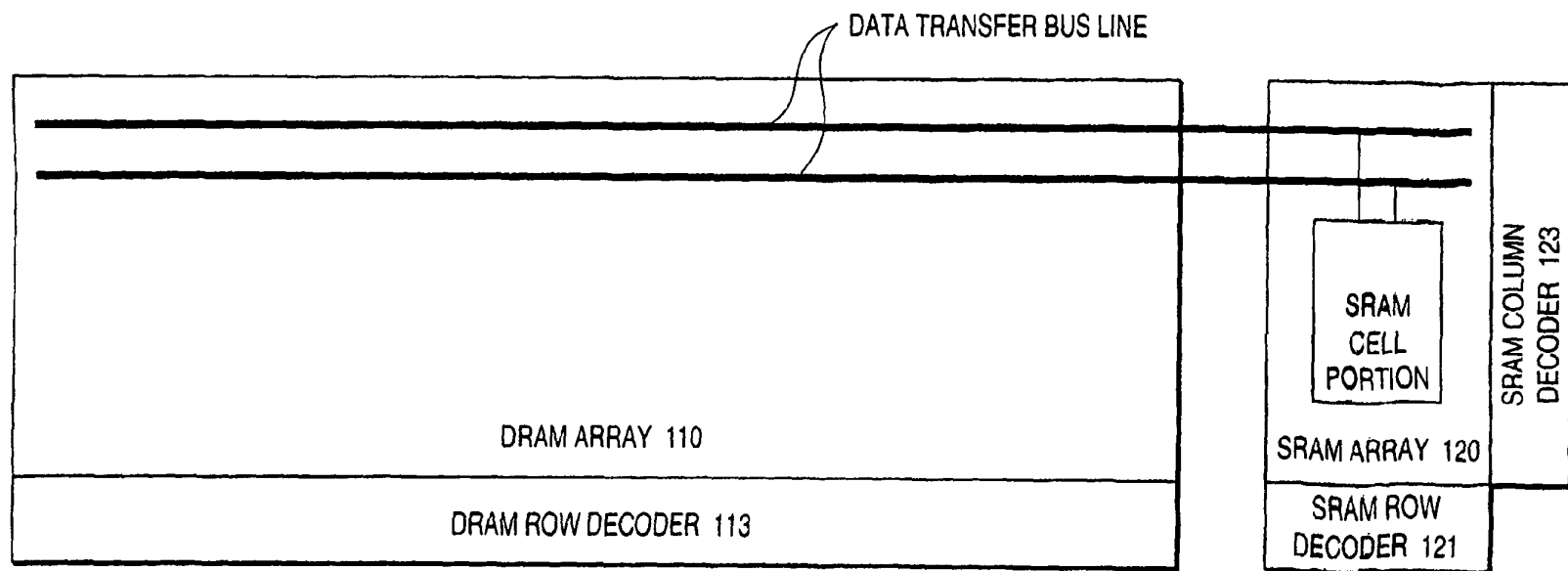


FIG. 37

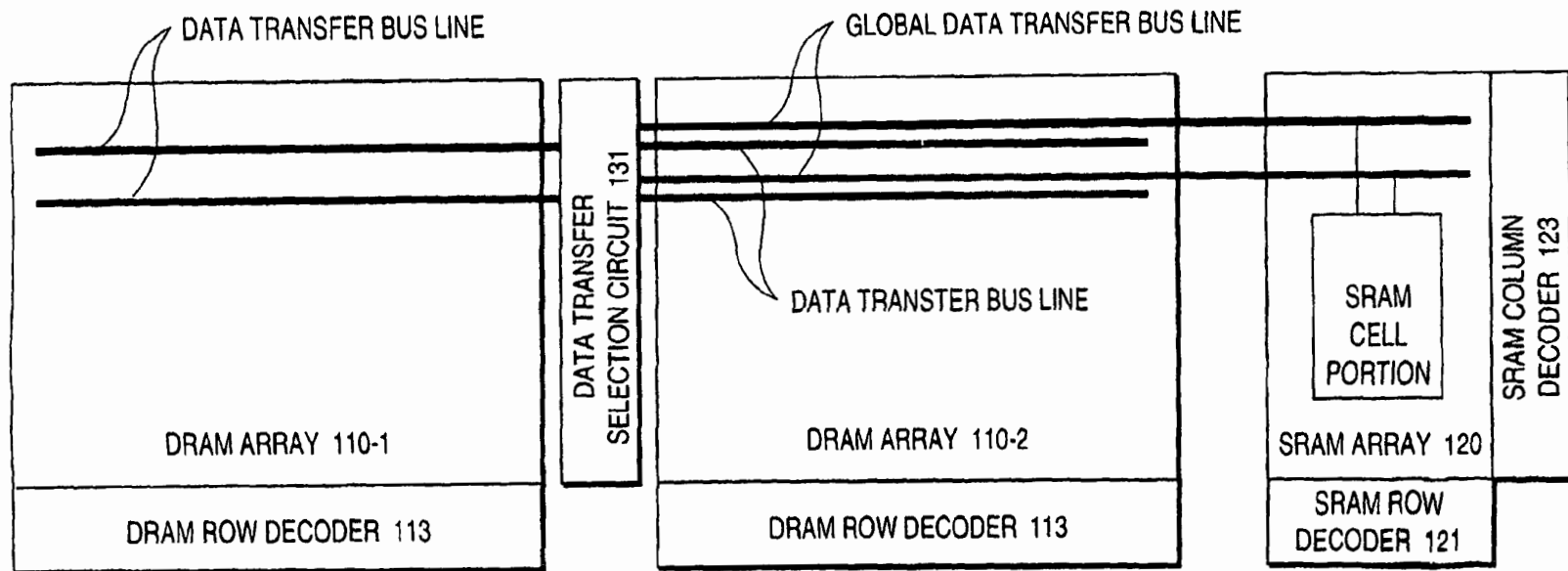


FIG. 38

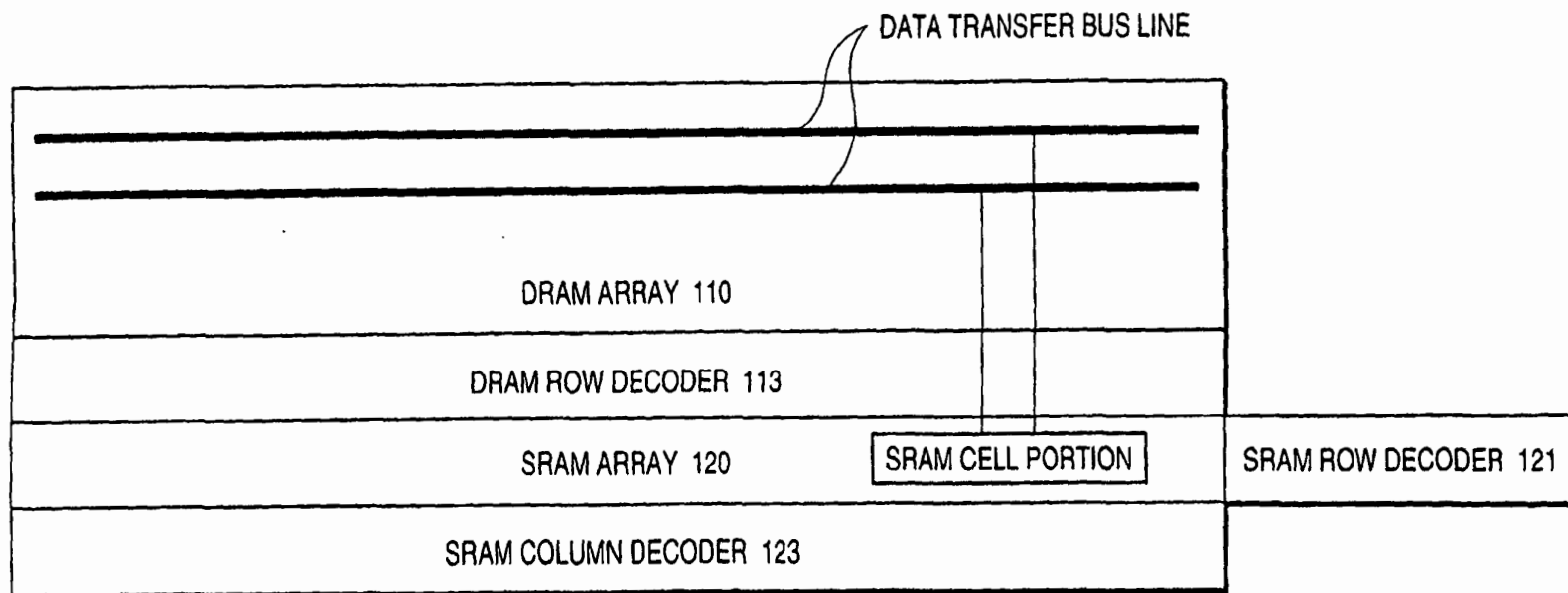


FIG. 39

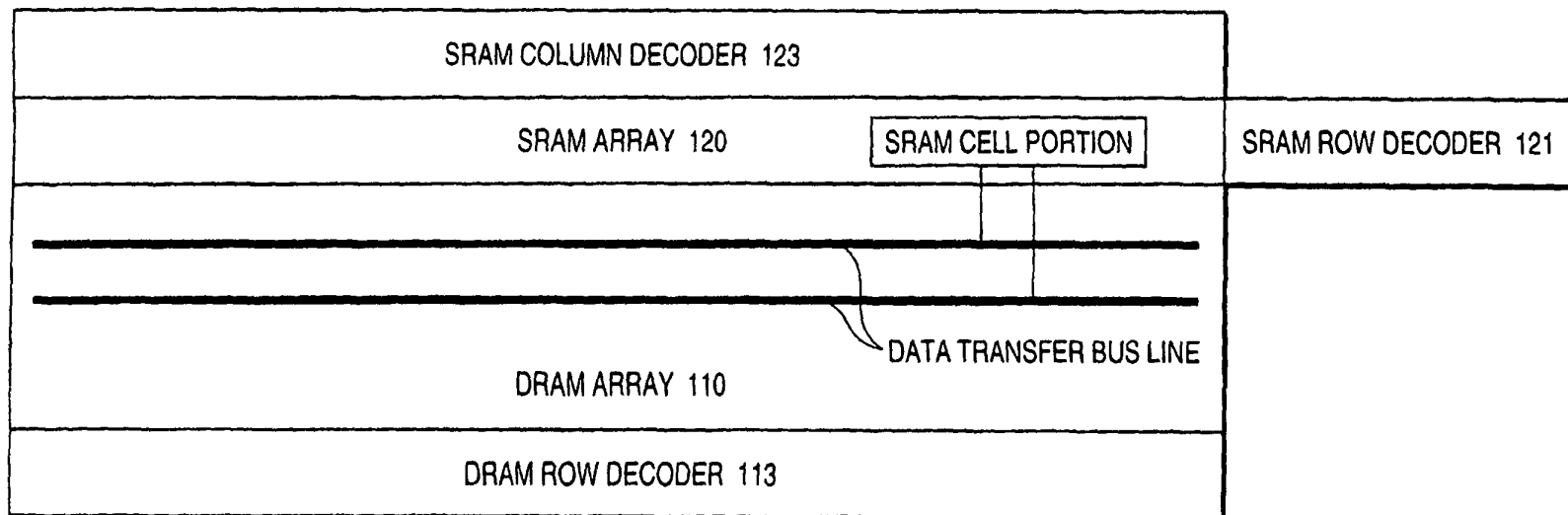


FIG. 40

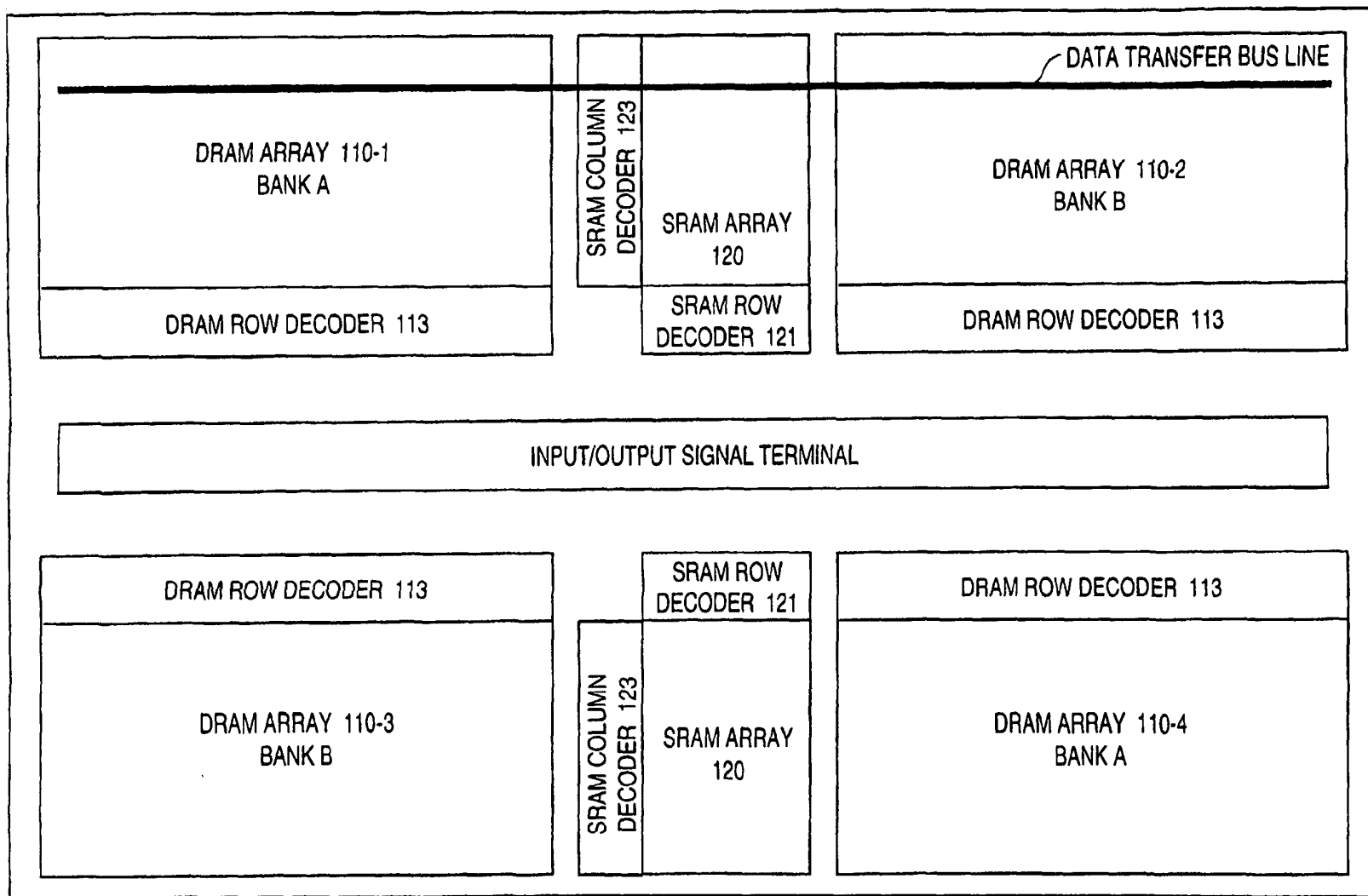


FIG. 41

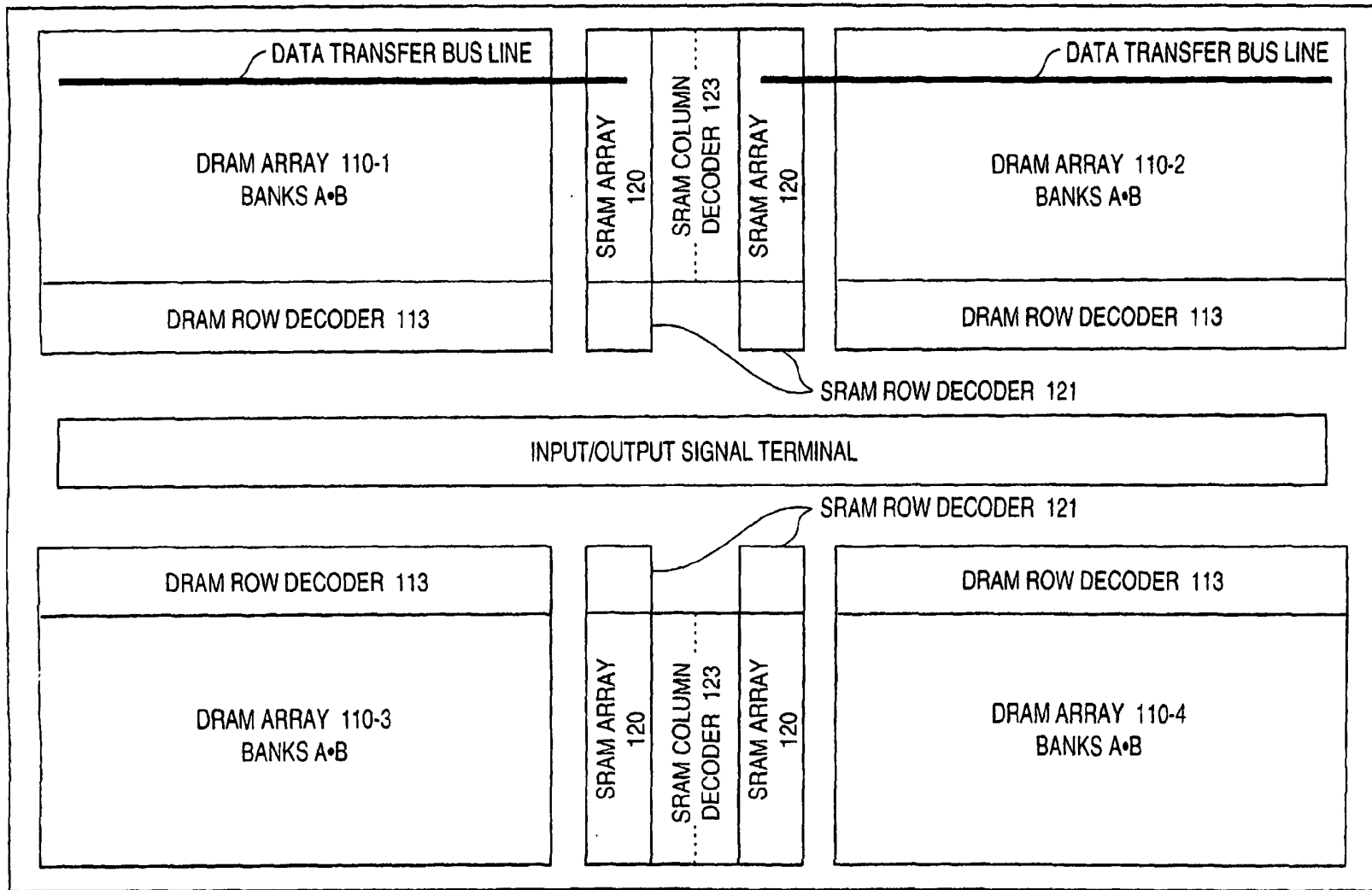


FIG. 42

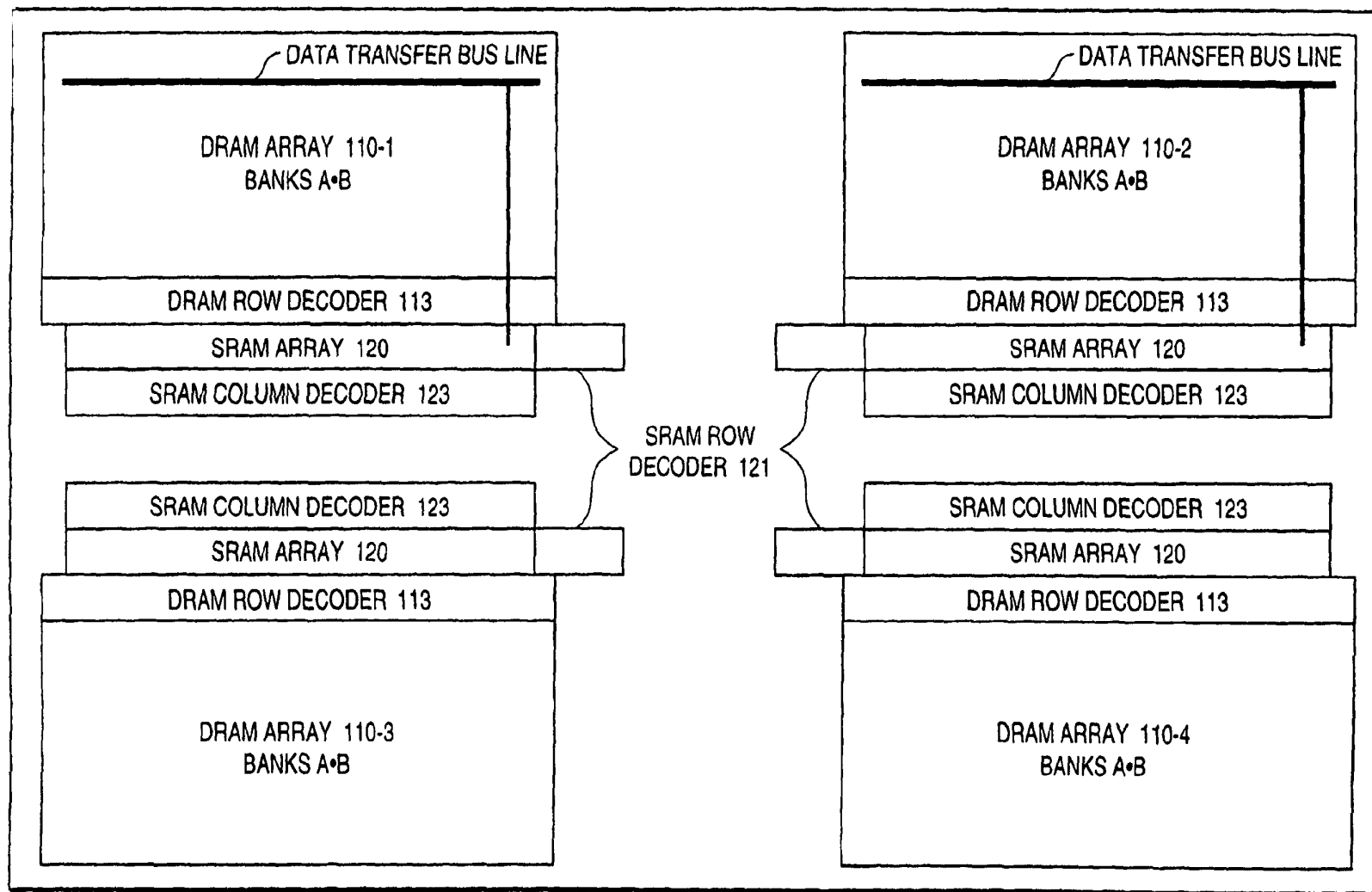


FIG. 43

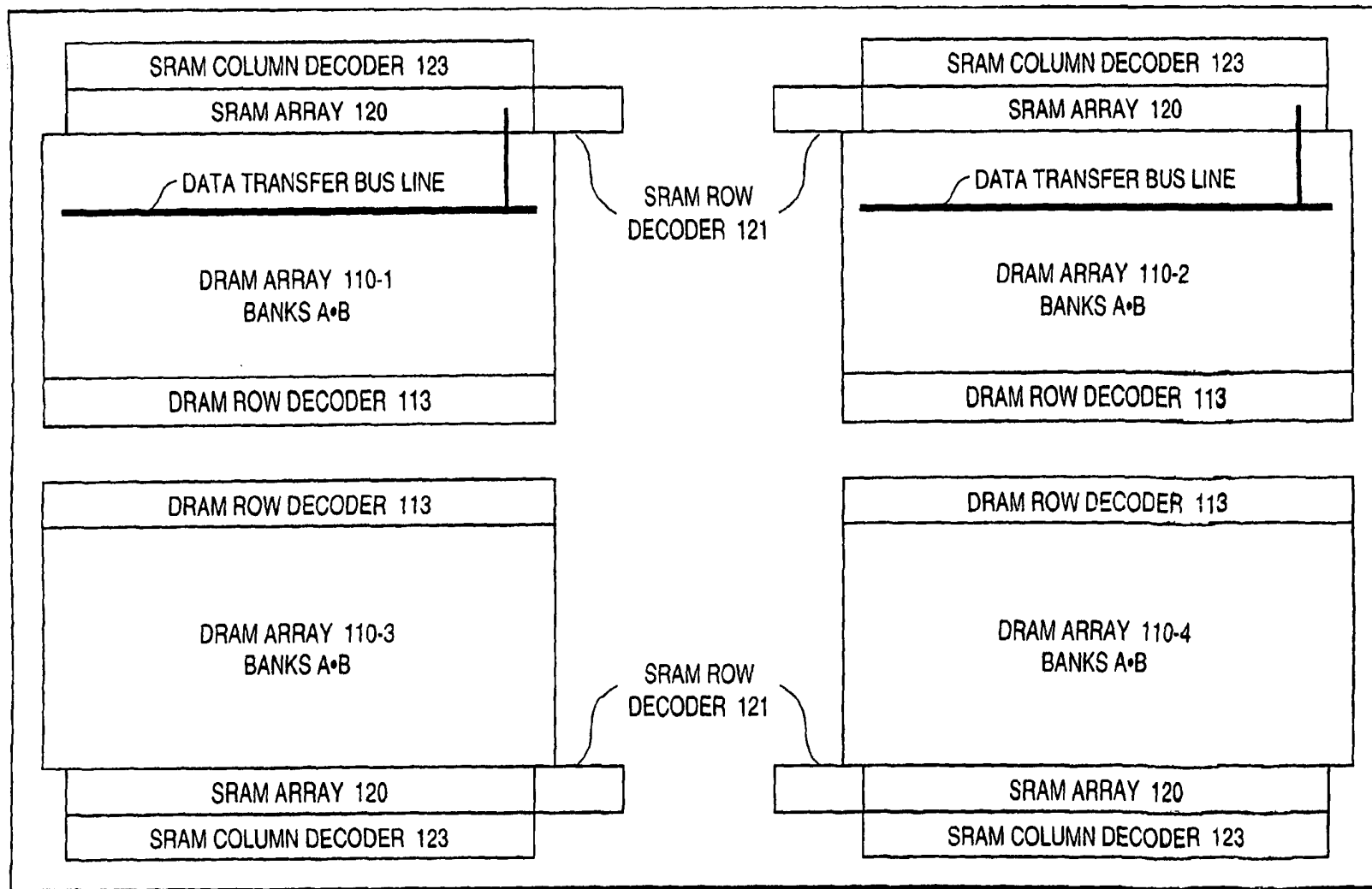


FIG. 44

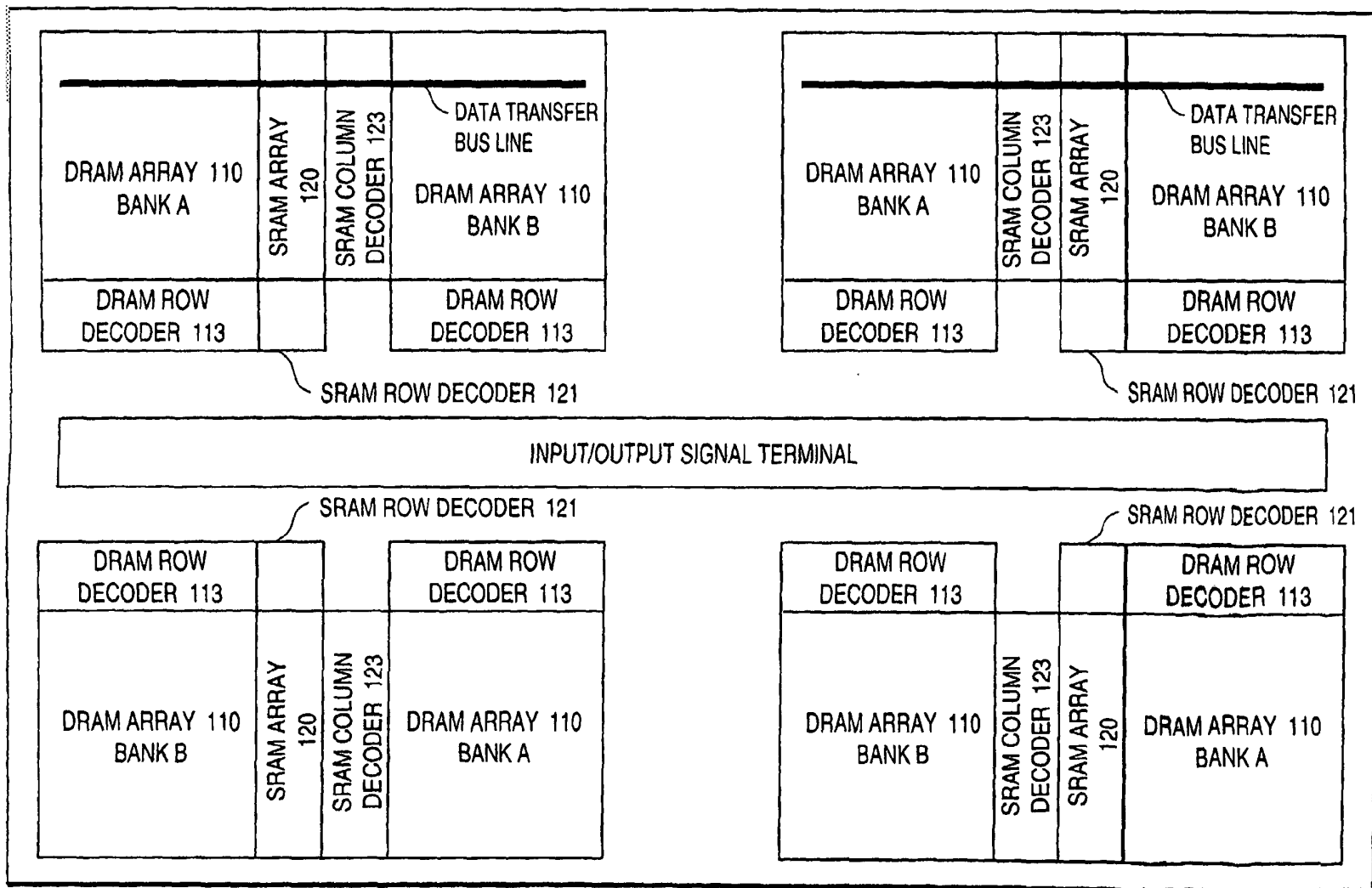


FIG. 45

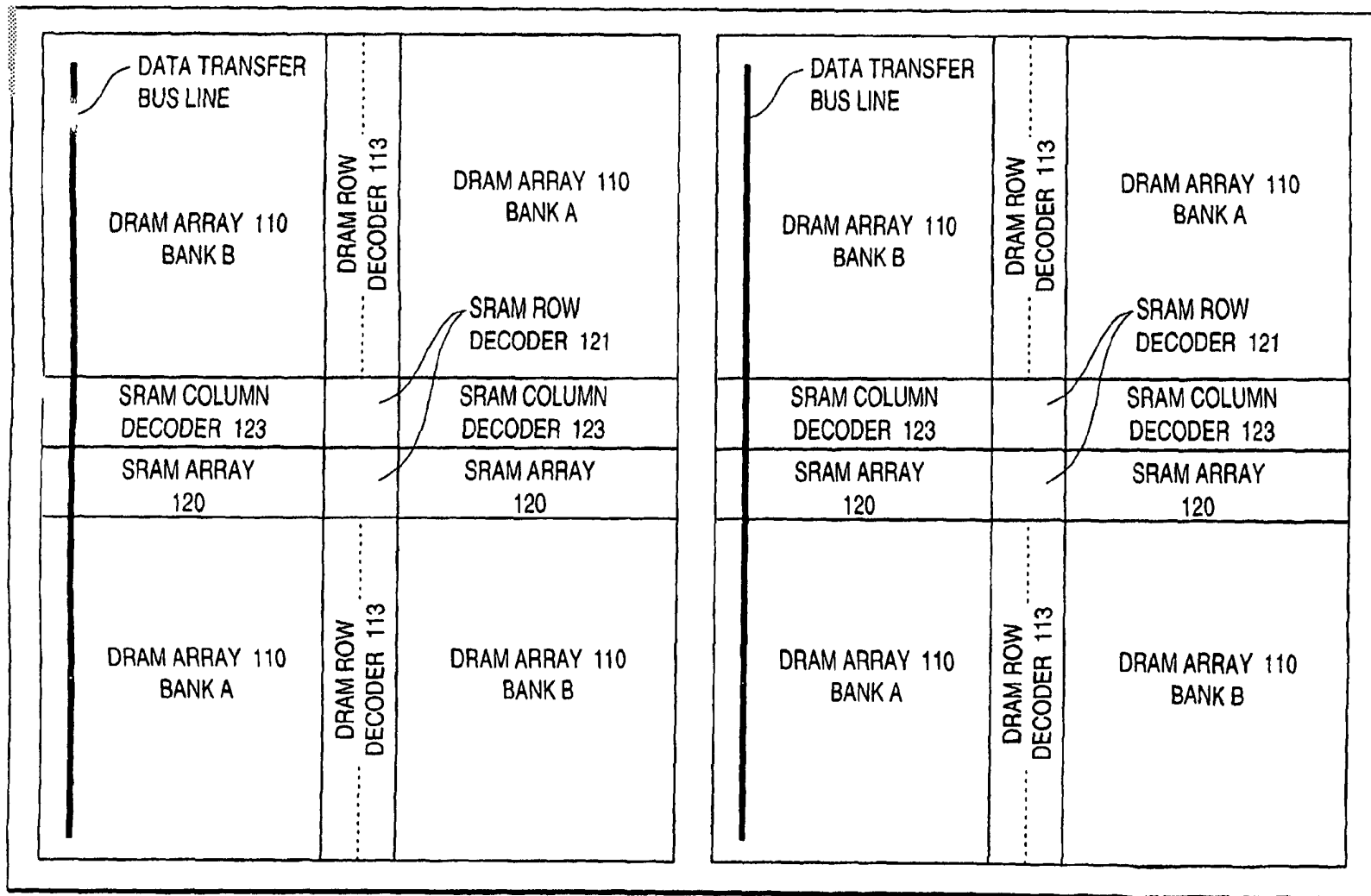


FIG. 46

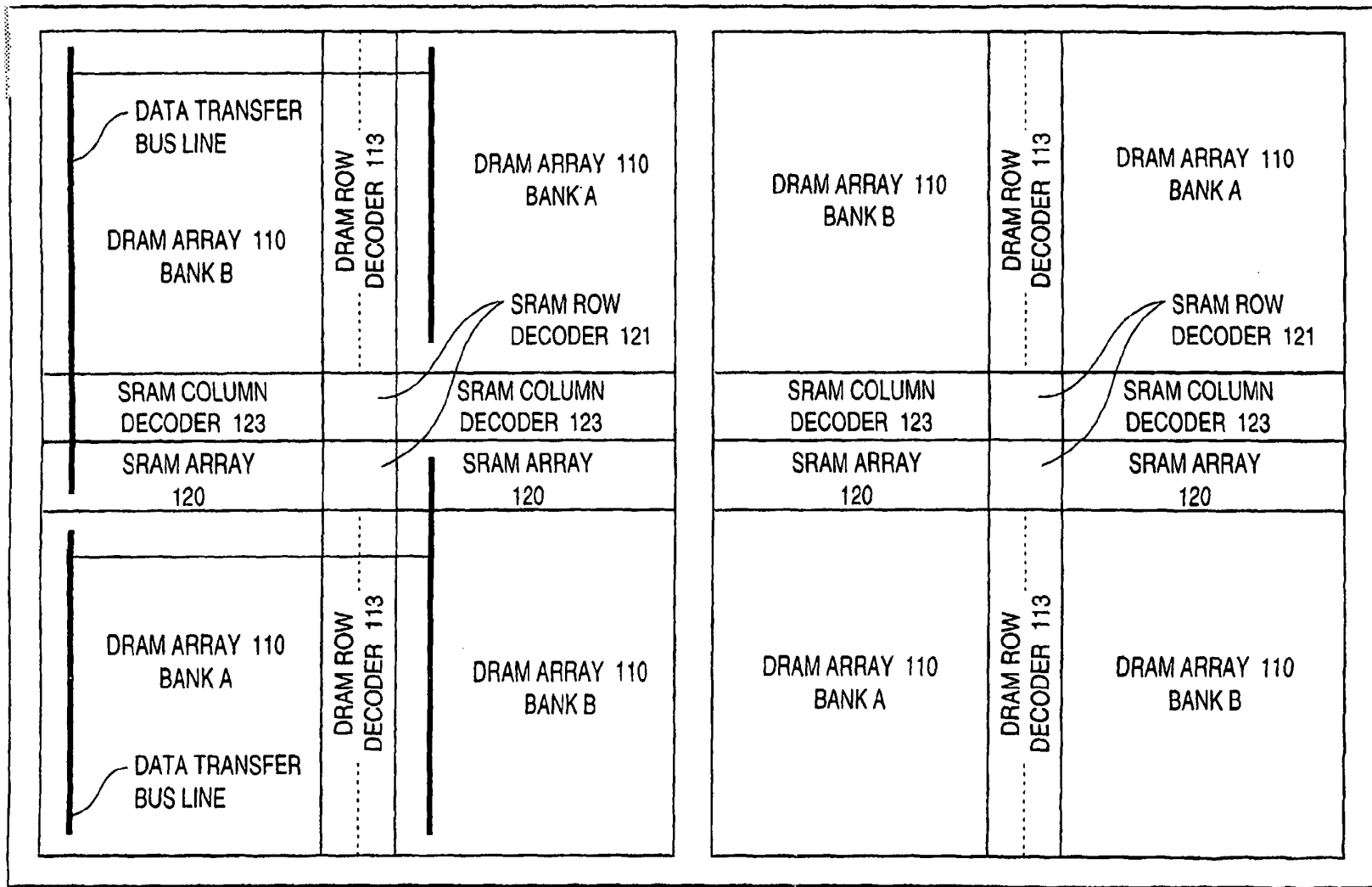


FIG. 47

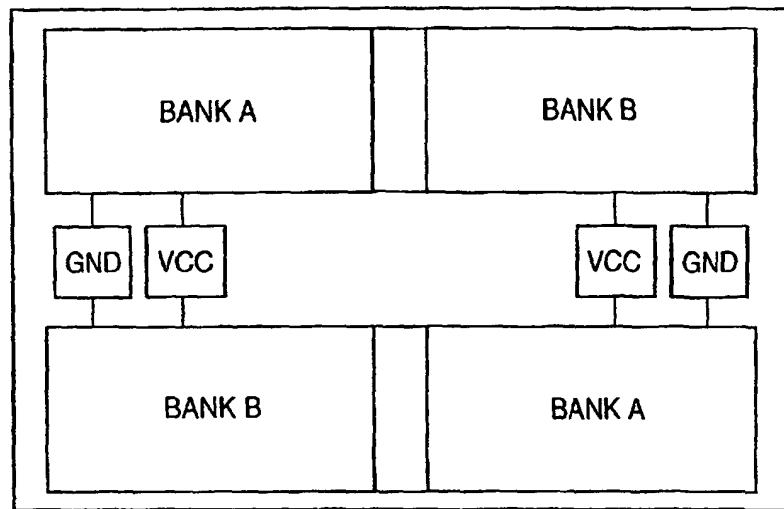


FIG. 48

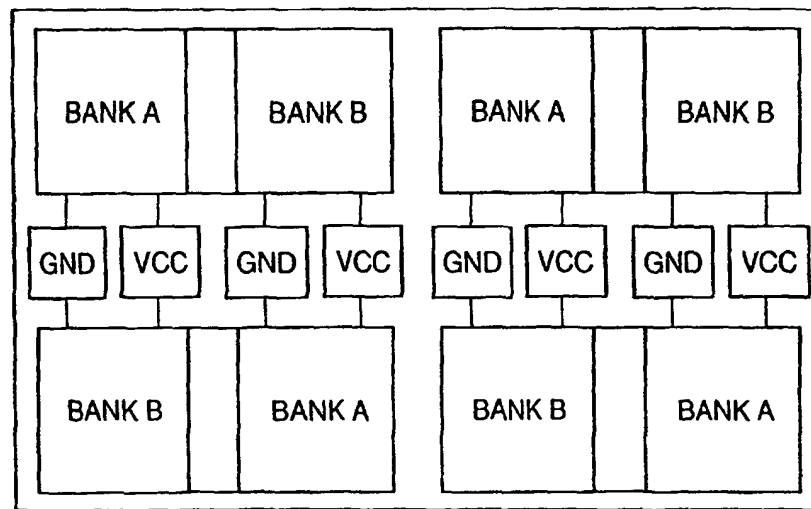


FIG. 49

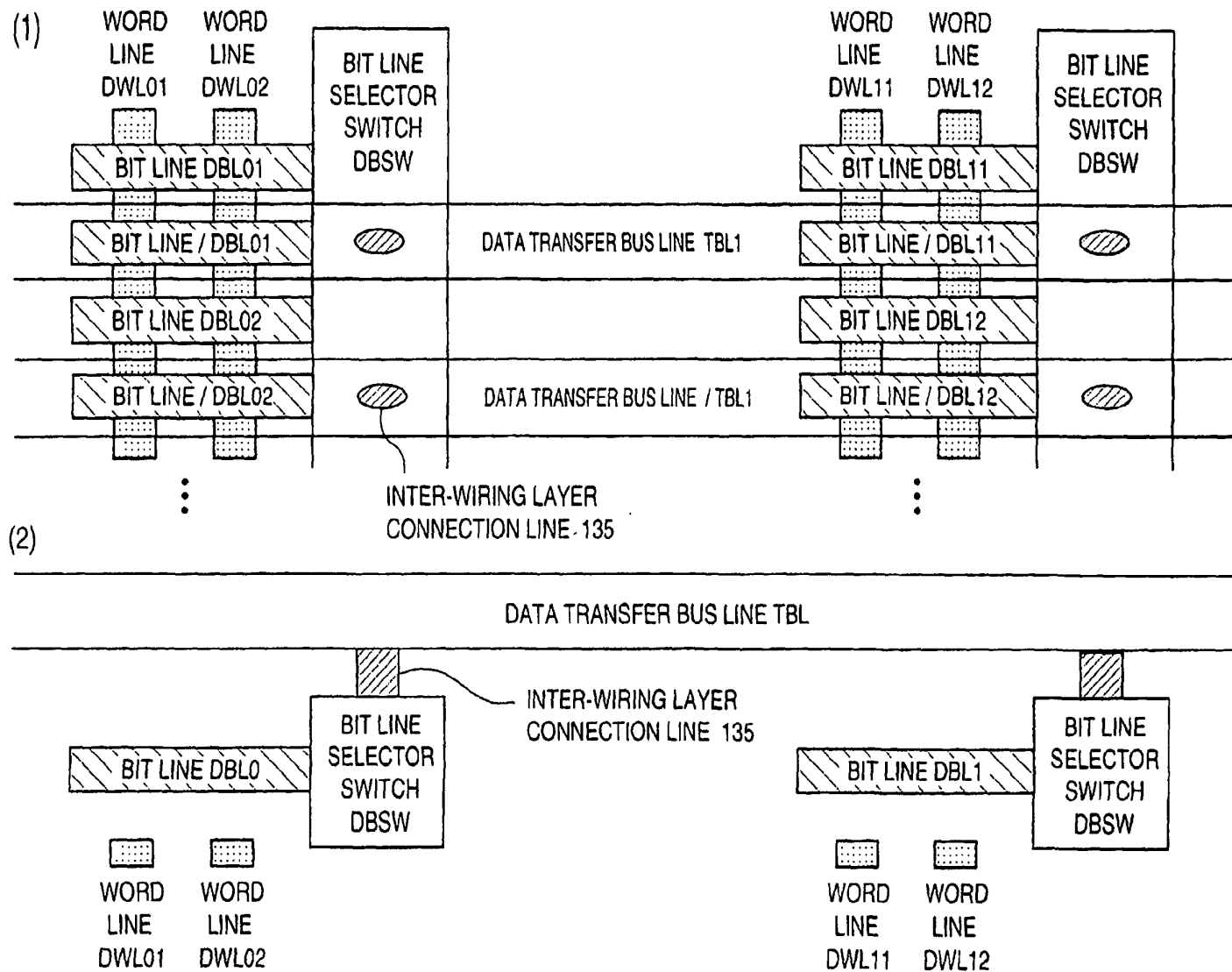


FIG. 50

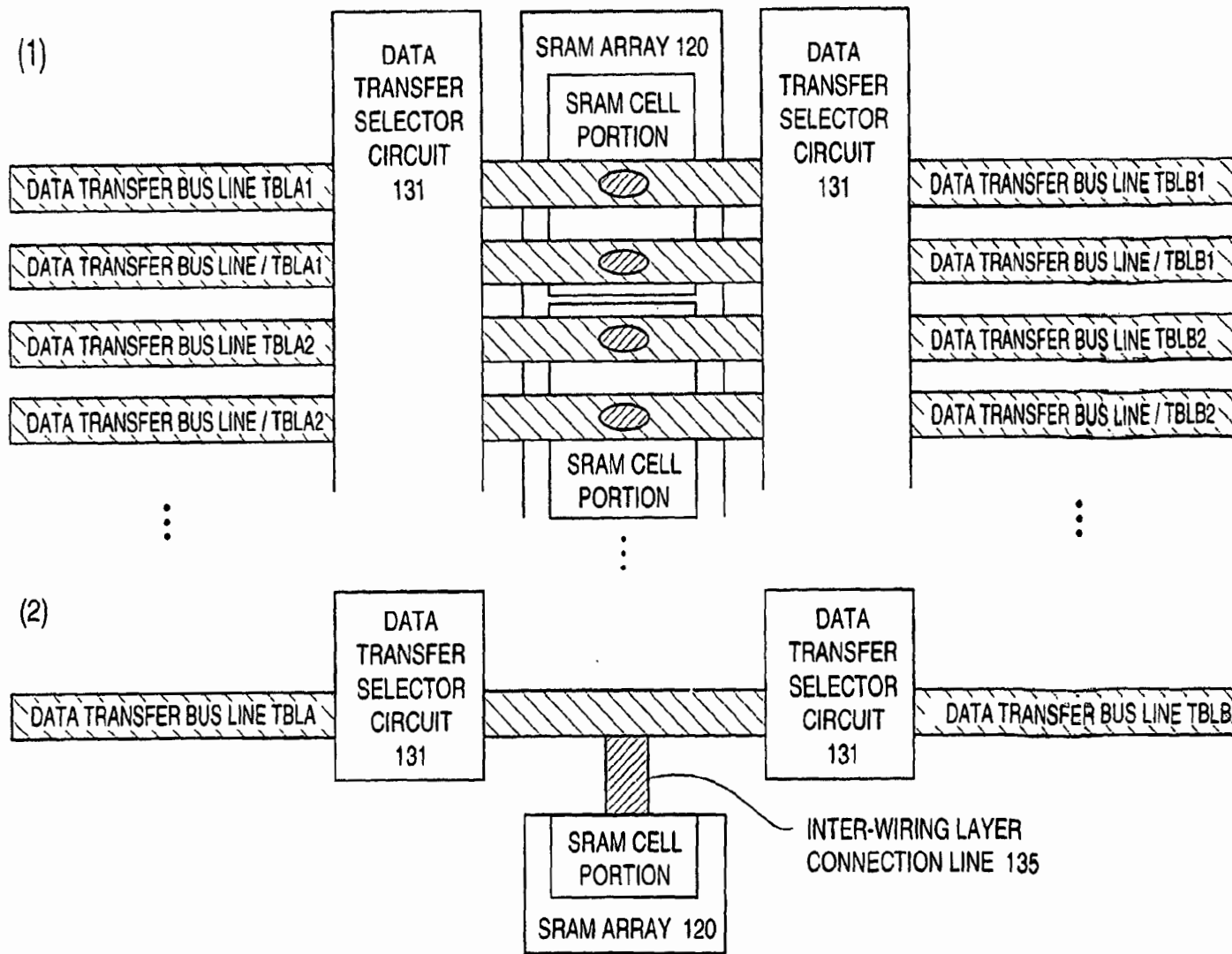


FIG. 51

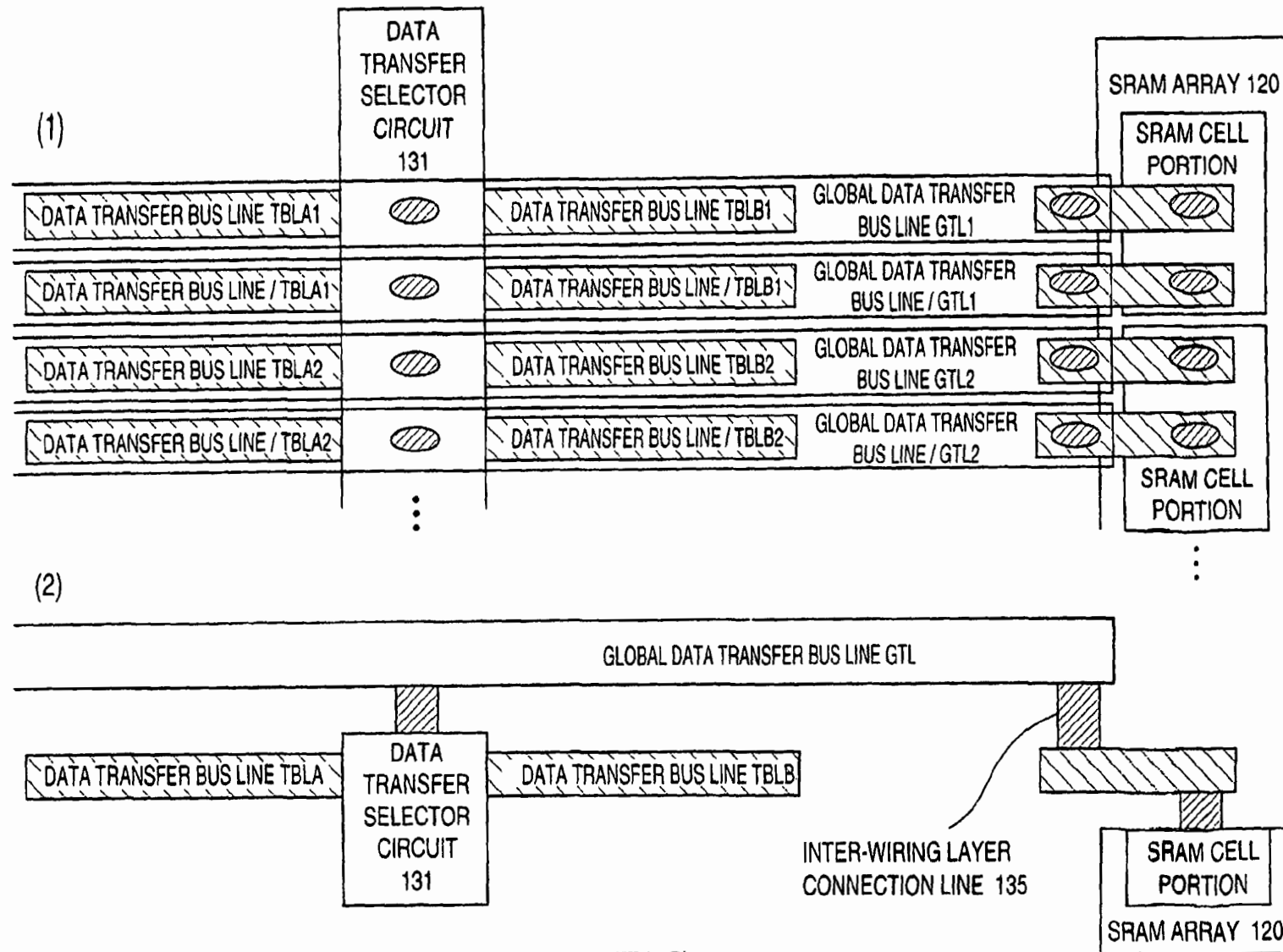


FIG. 52

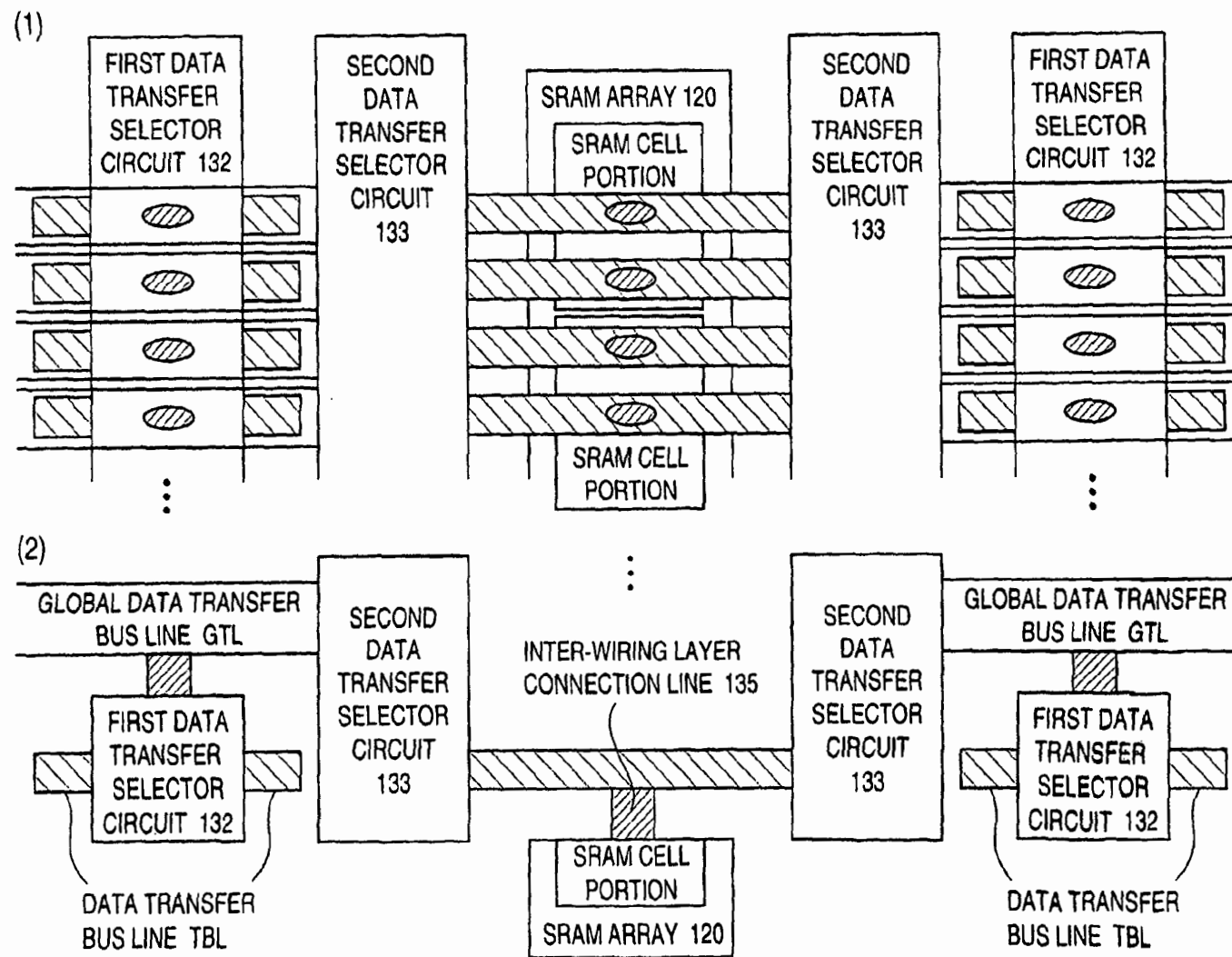


FIG. 53

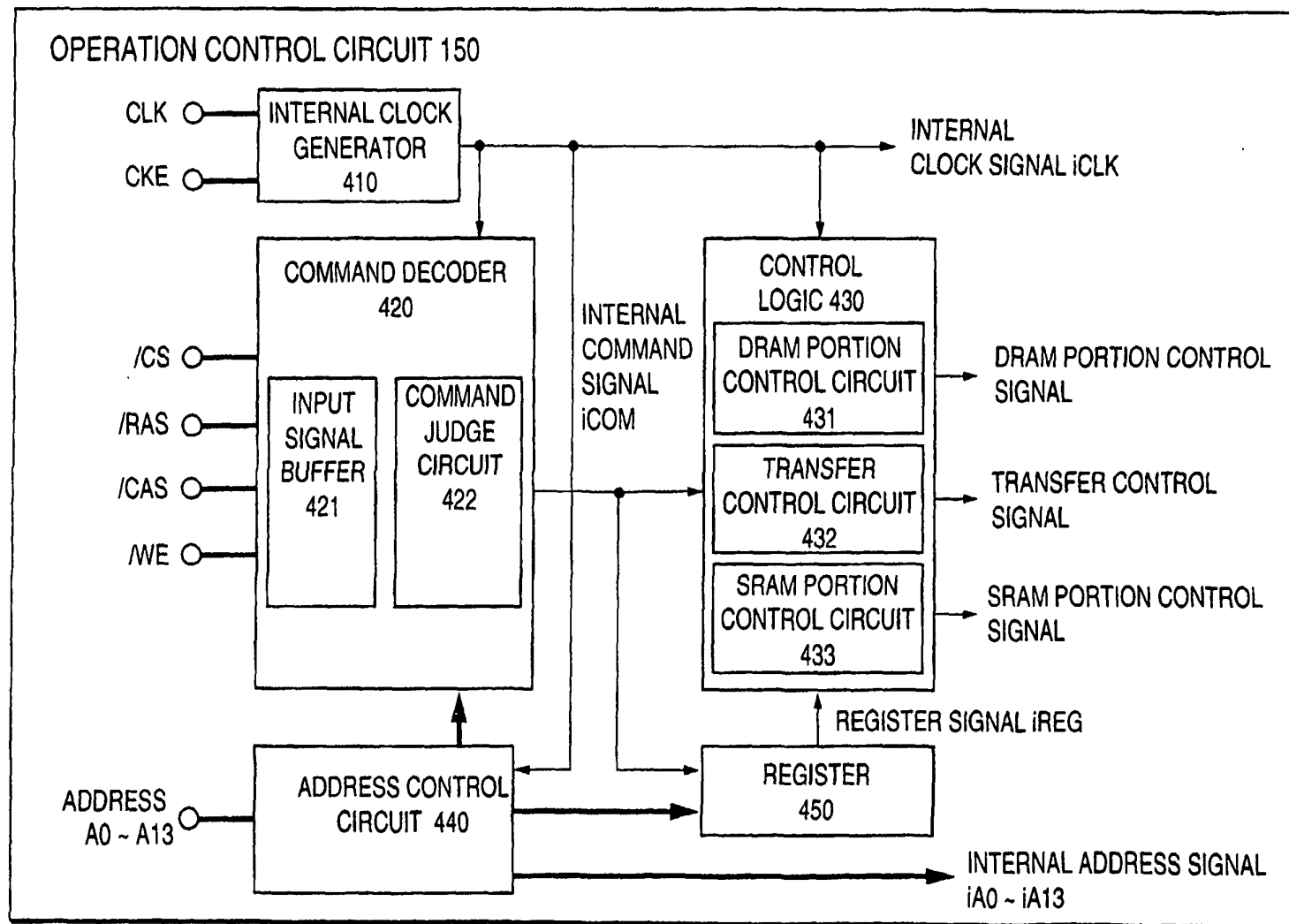


FIG. 54

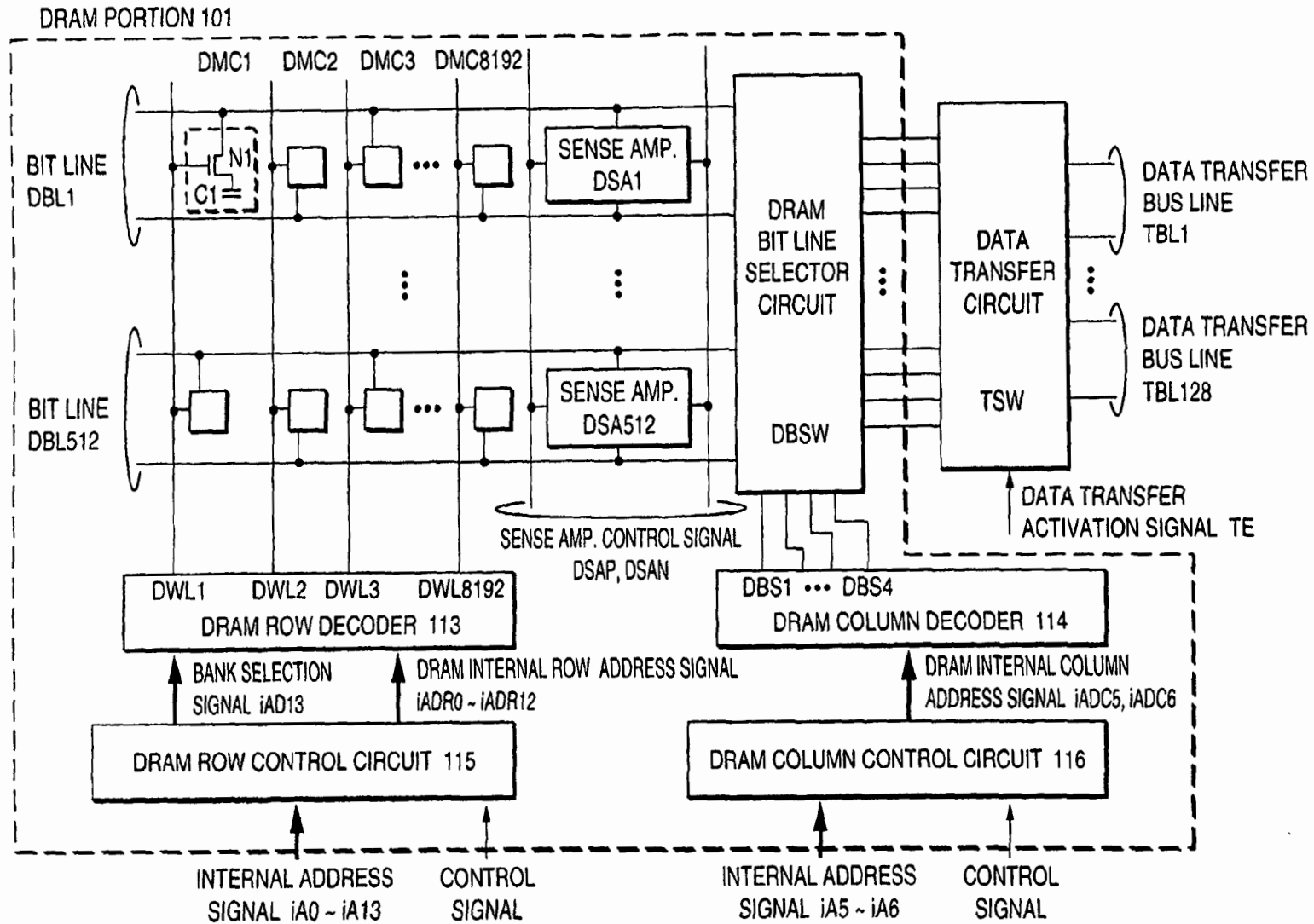


FIG. 55

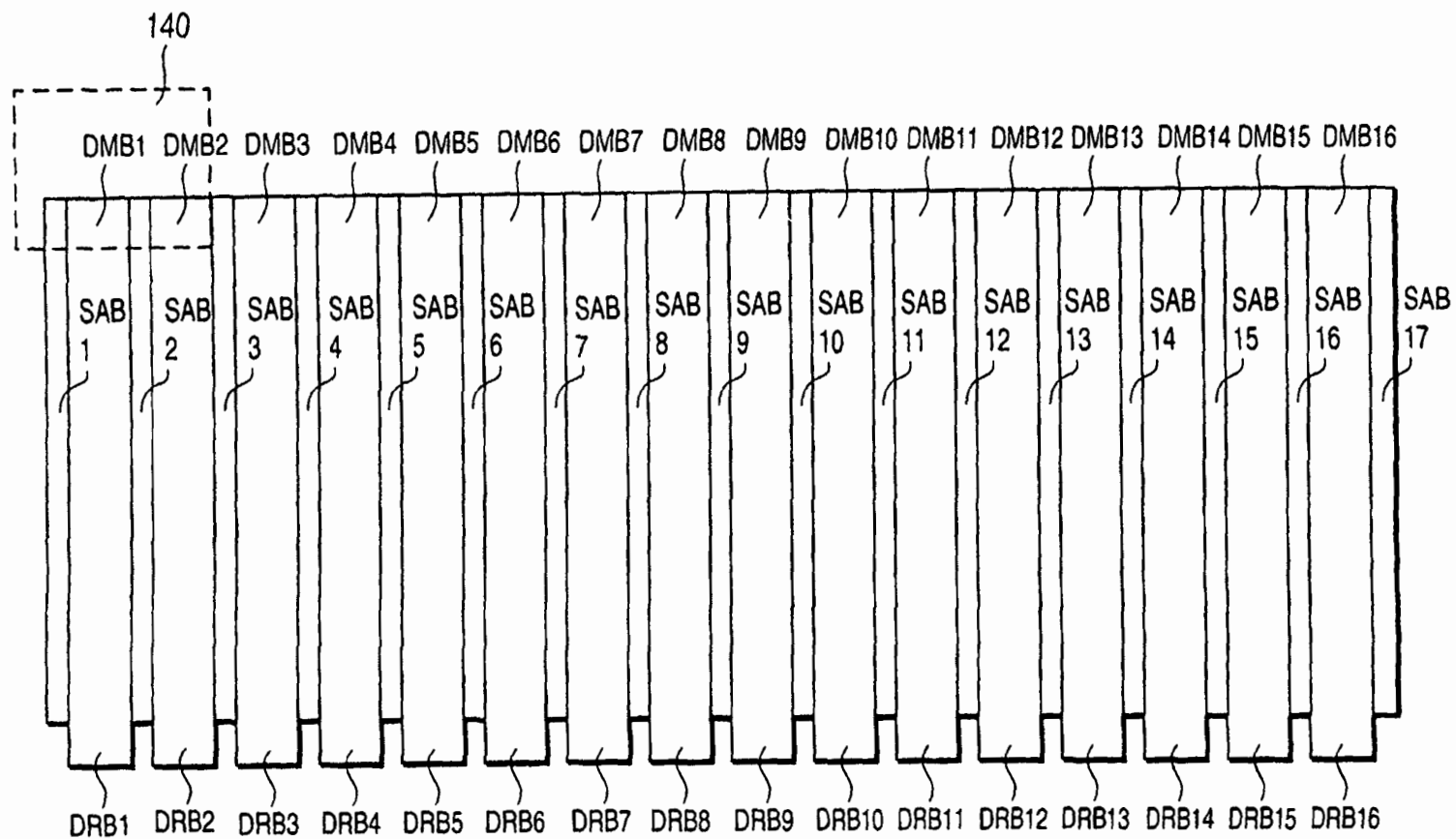


FIG. 56

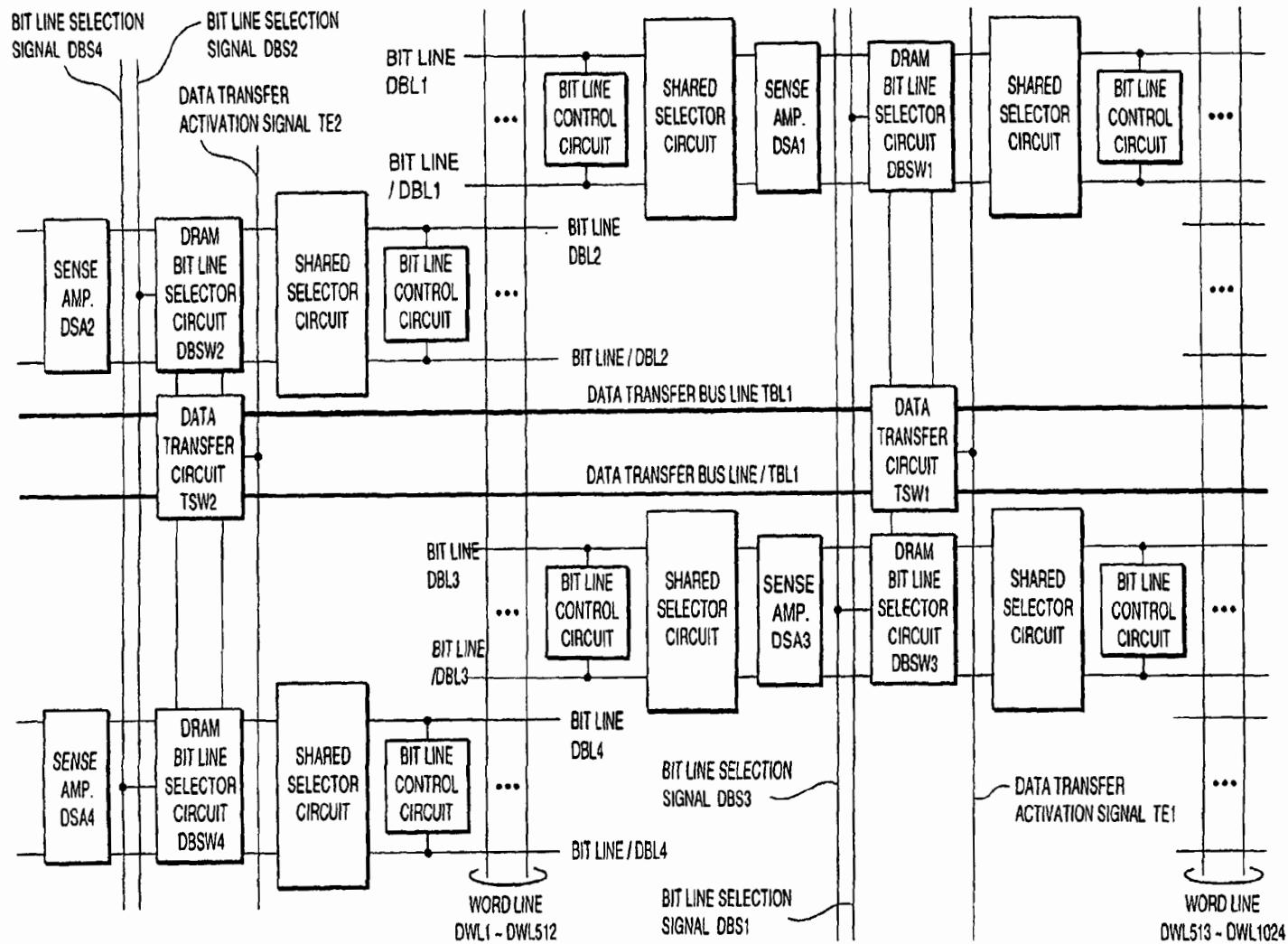


FIG. 57

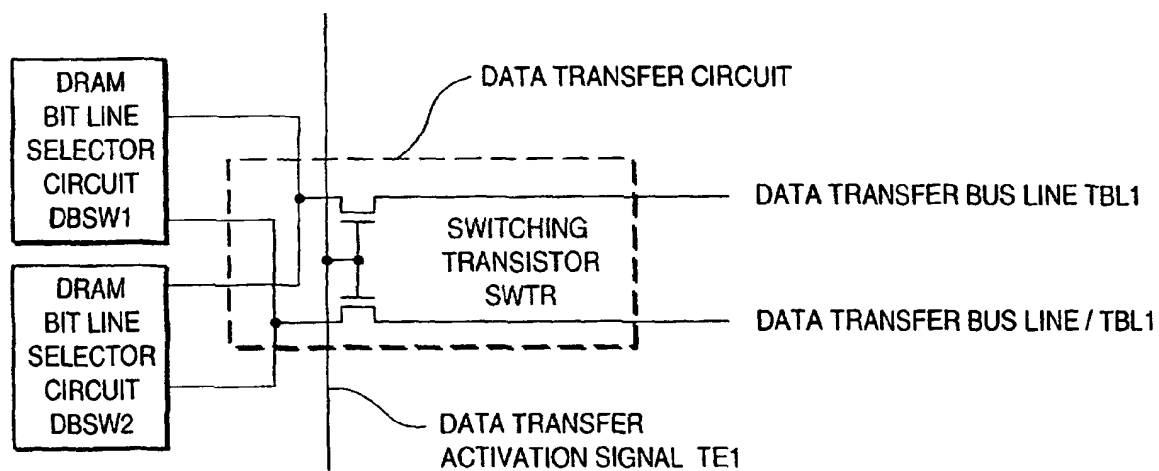


FIG. 58

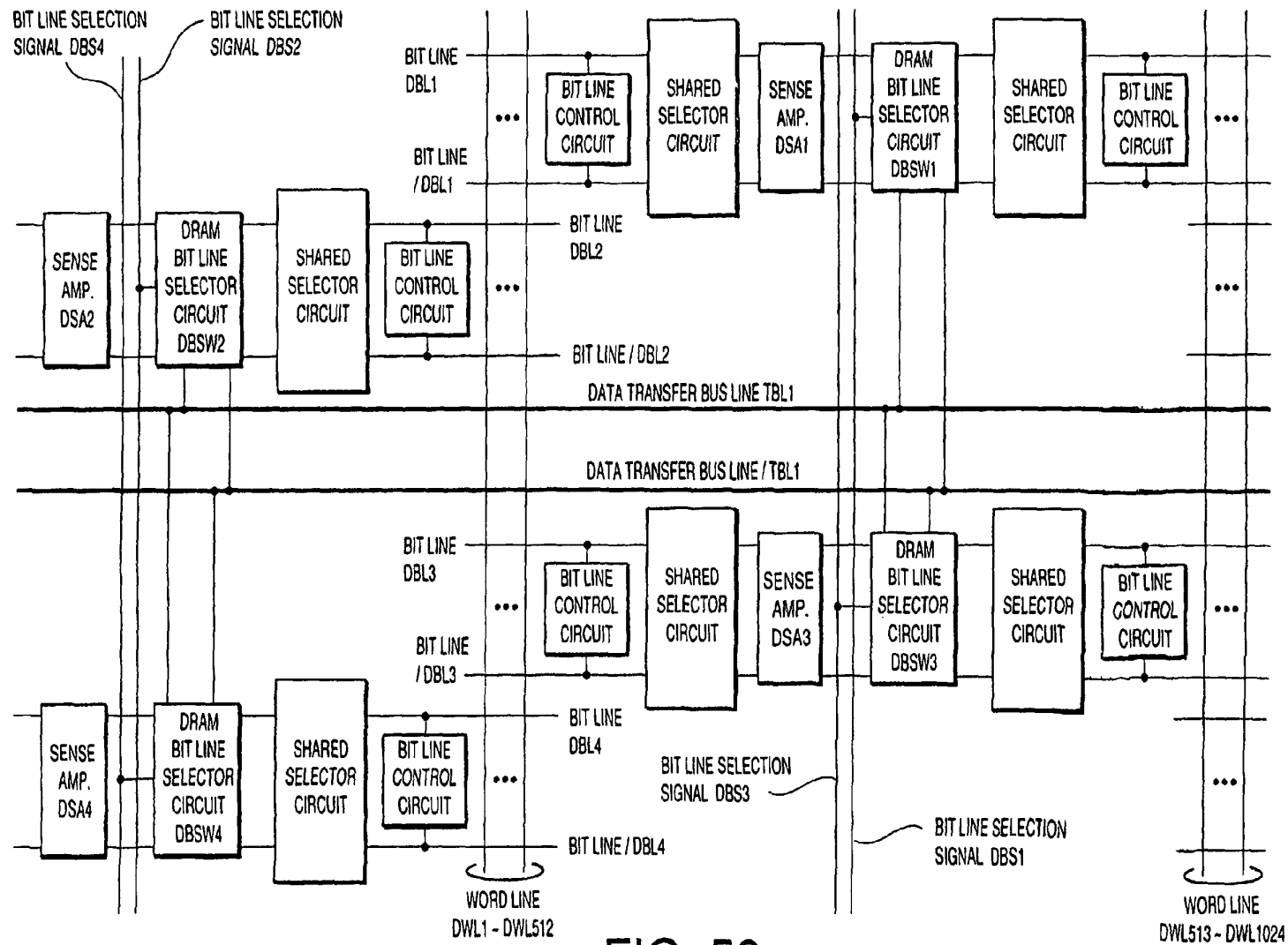


FIG. 59

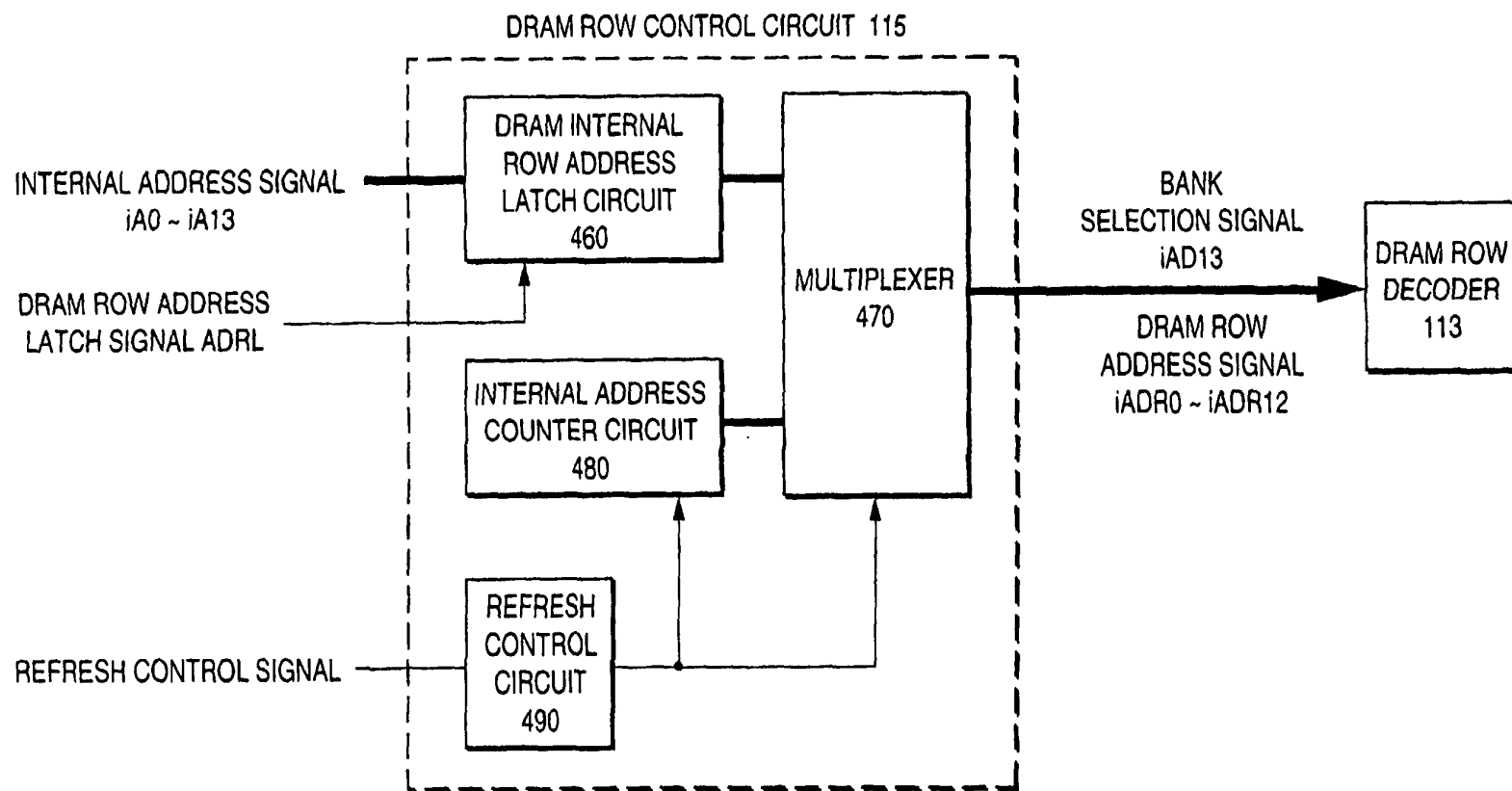


FIG. 60

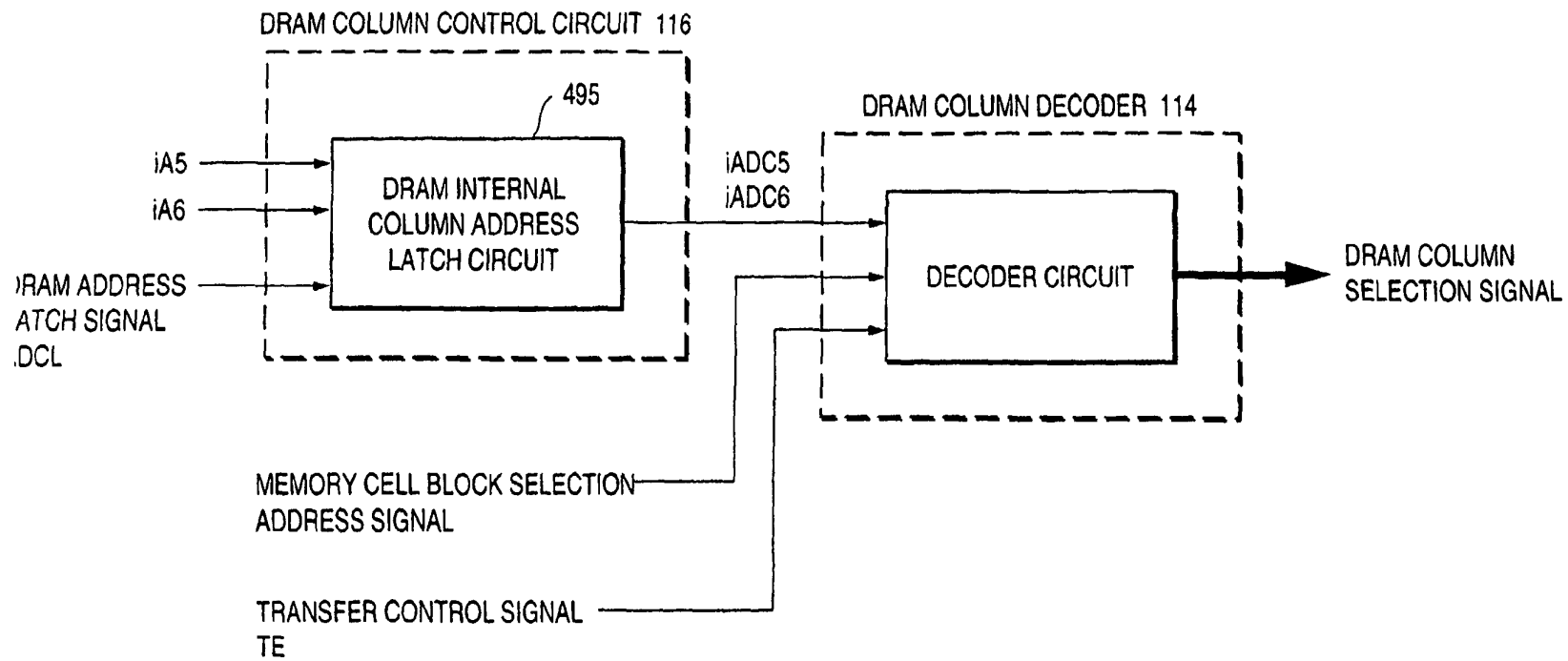


FIG. 61

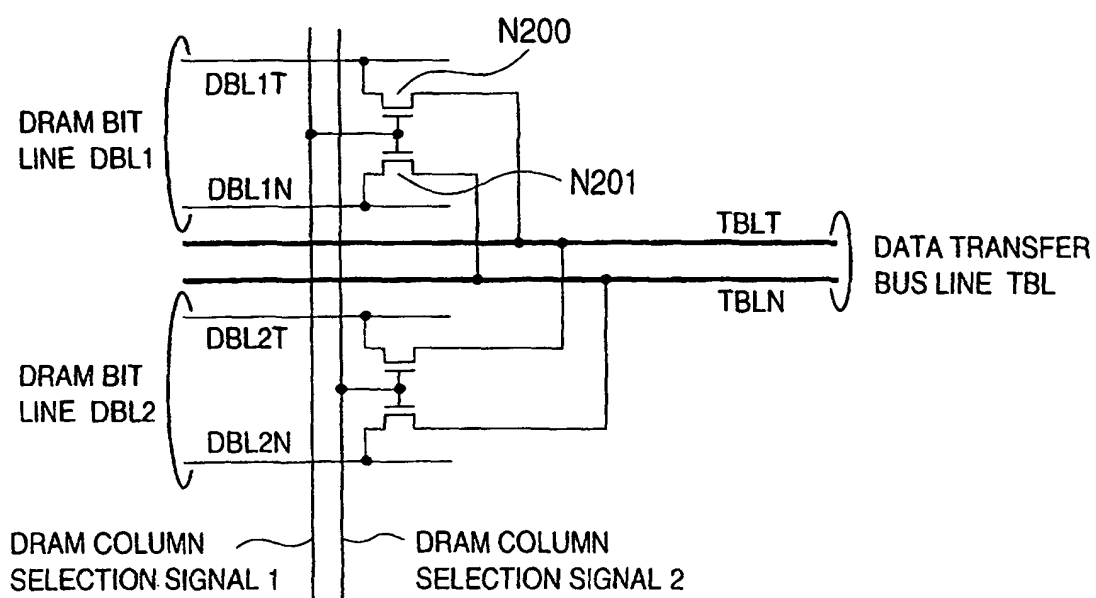


FIG. 62

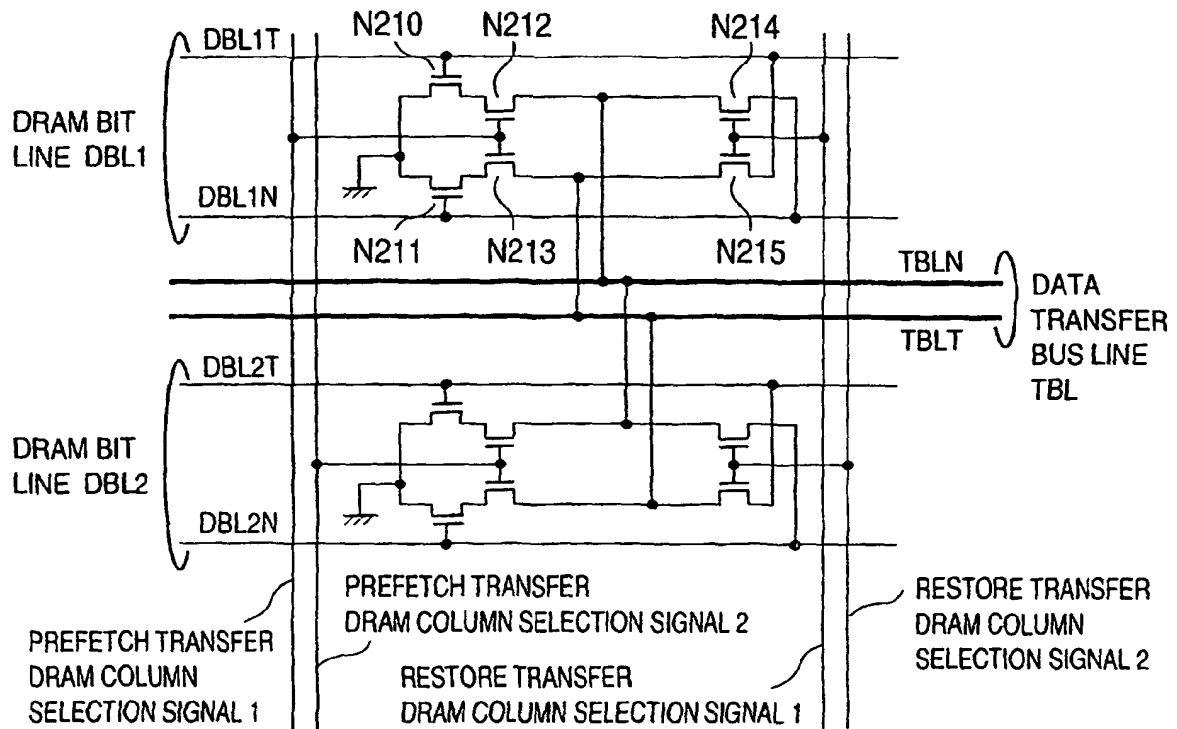


FIG. 63

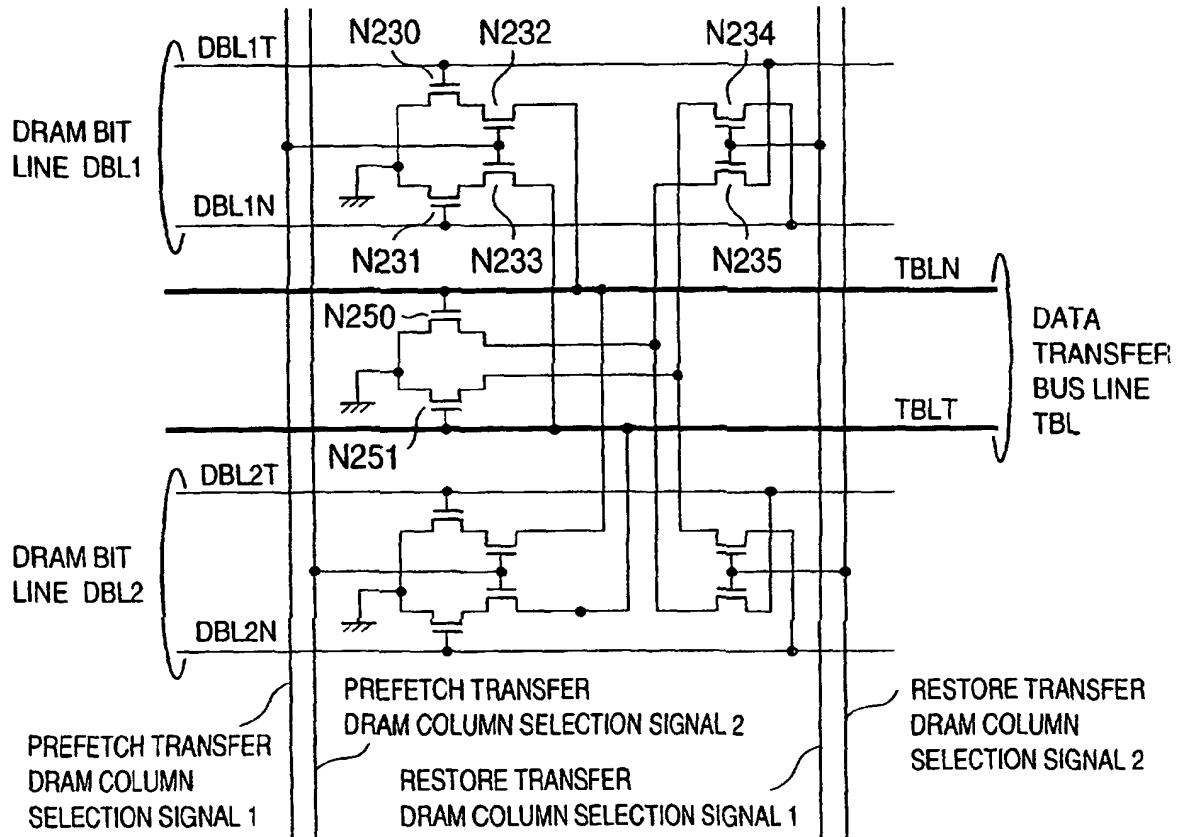


FIG. 64

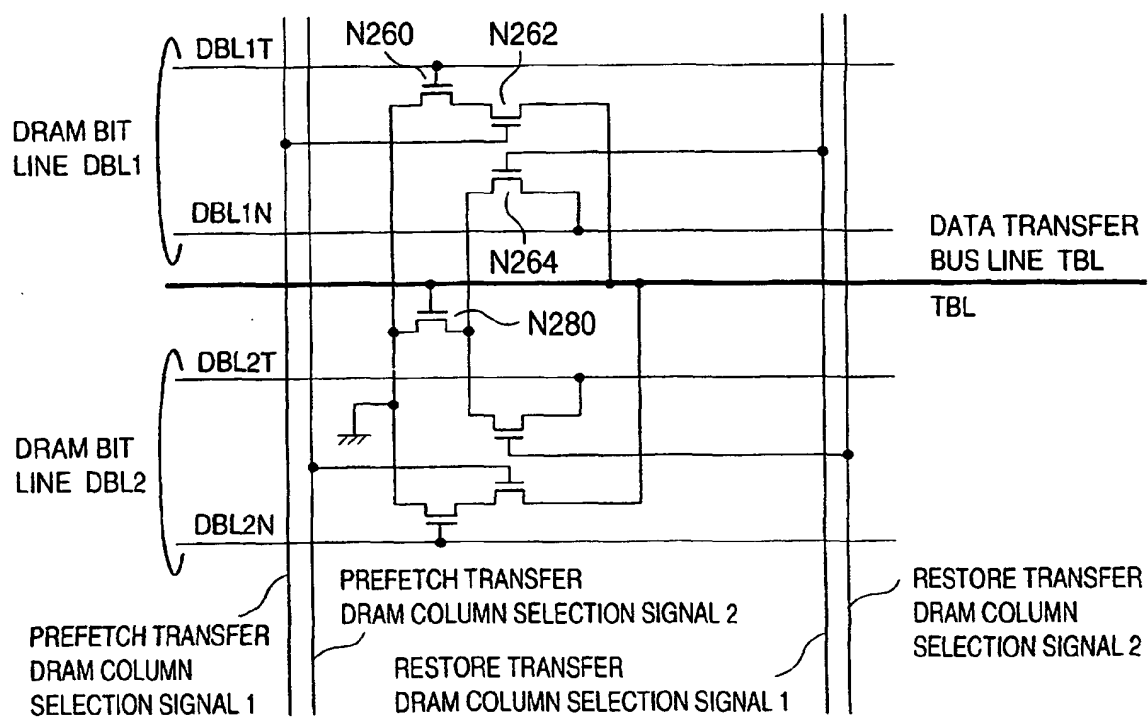


FIG. 65

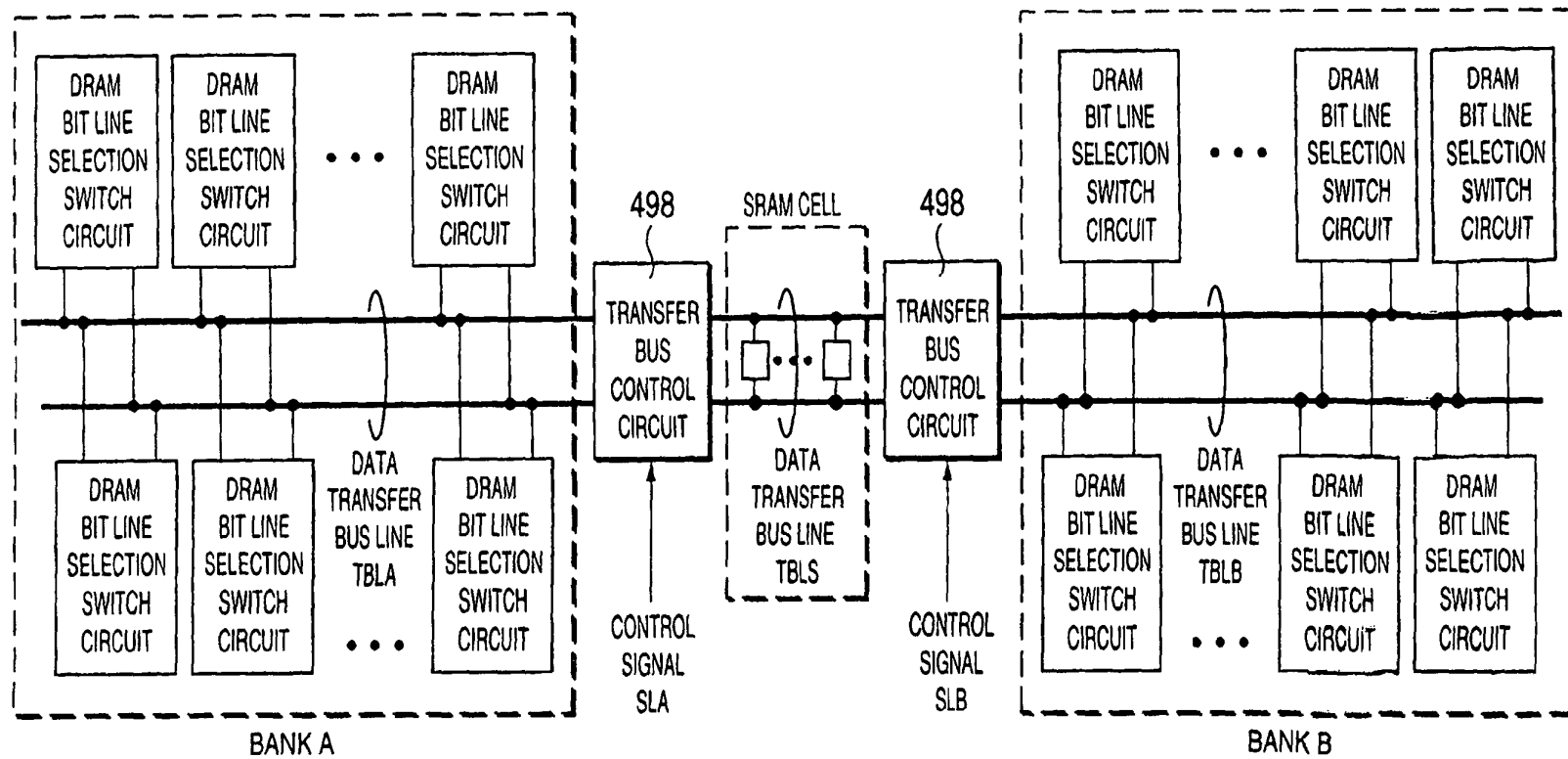


FIG. 66

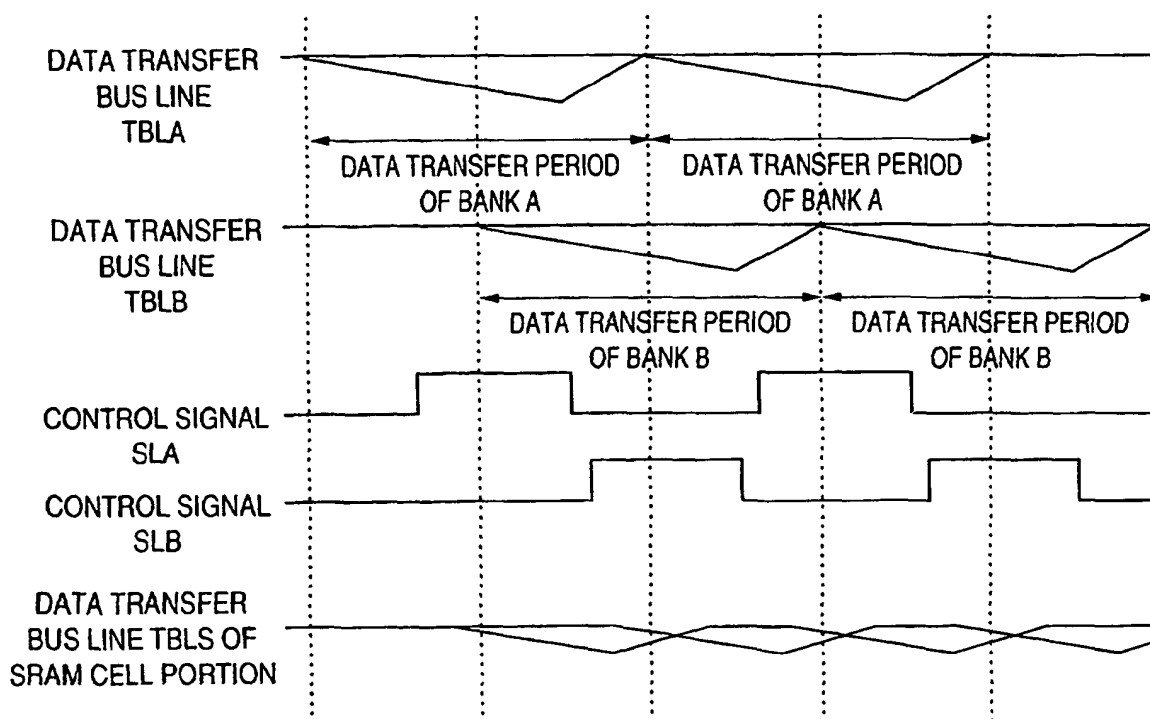


FIG. 67

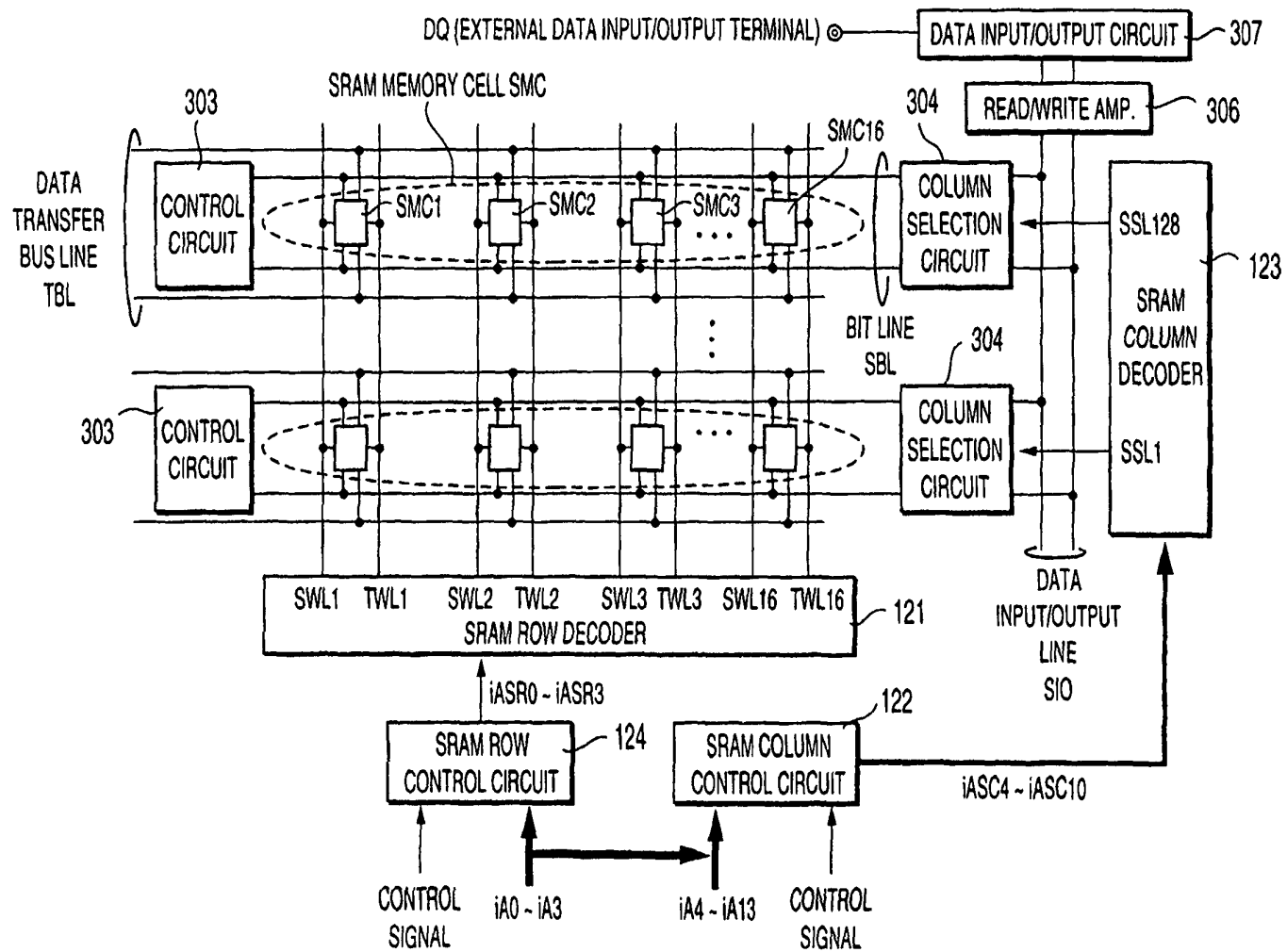


FIG. 68

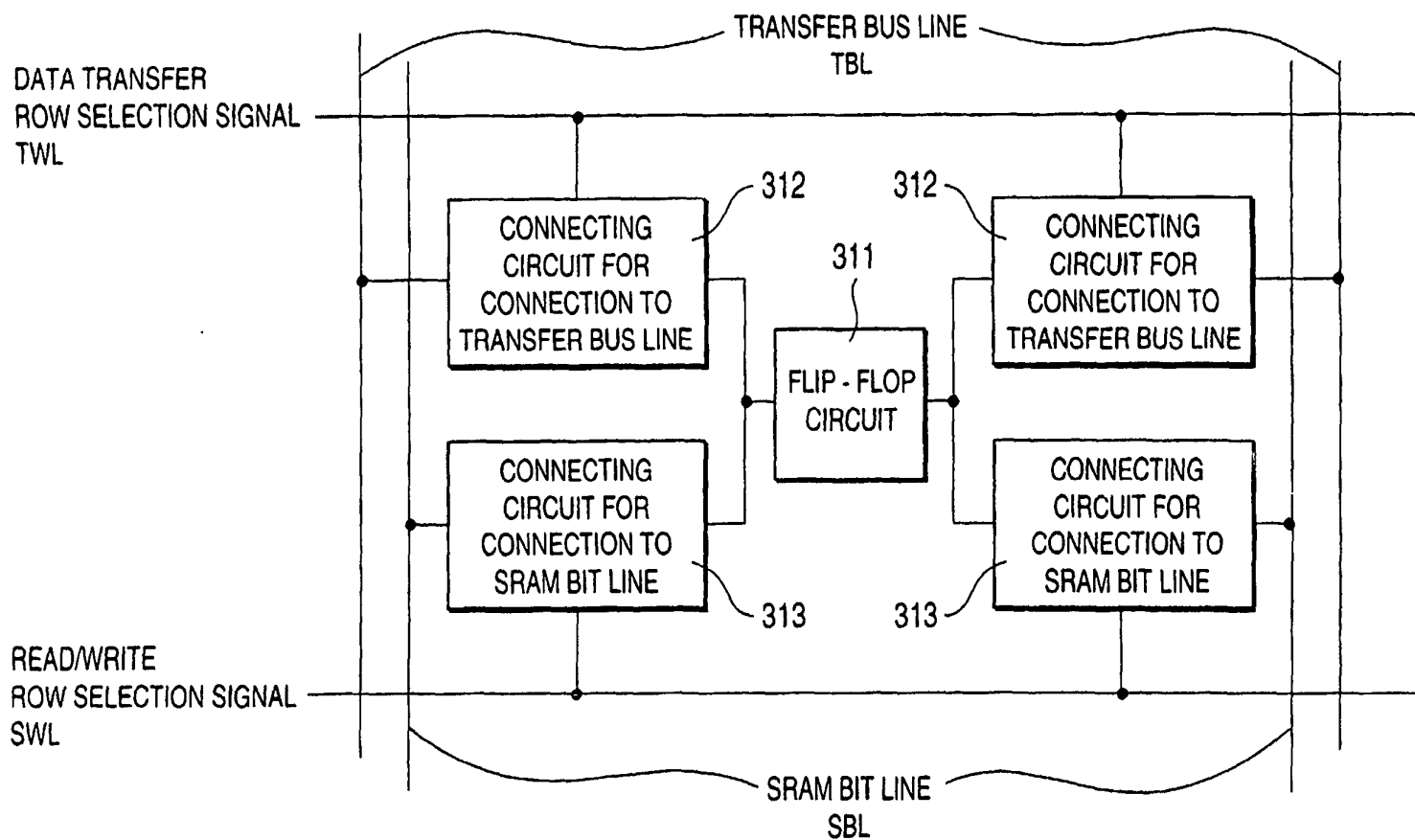
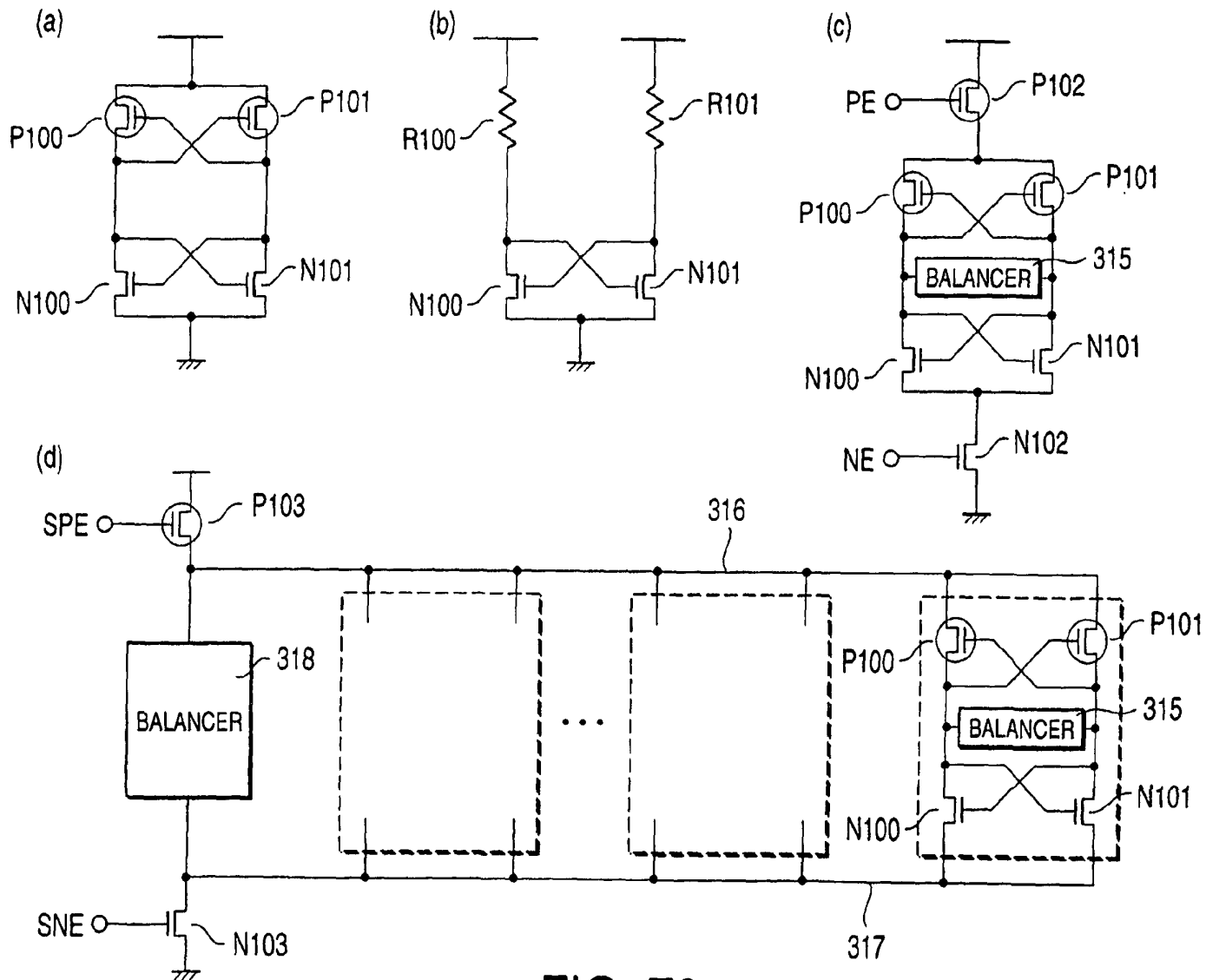


FIG. 69



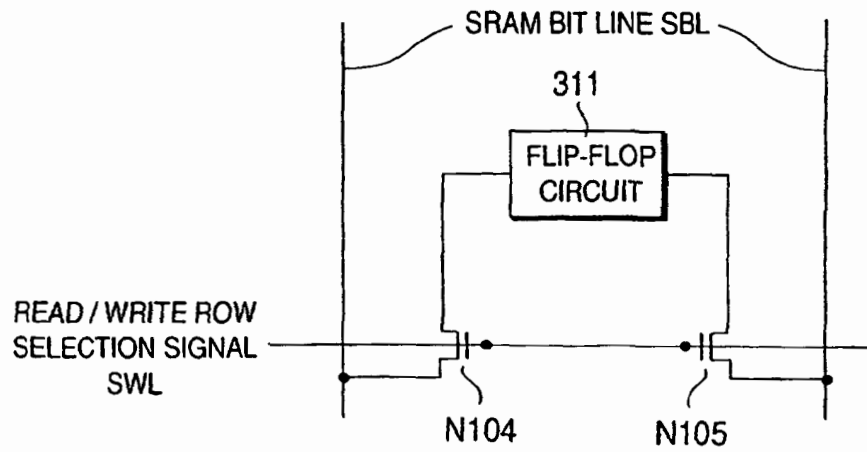


FIG. 71

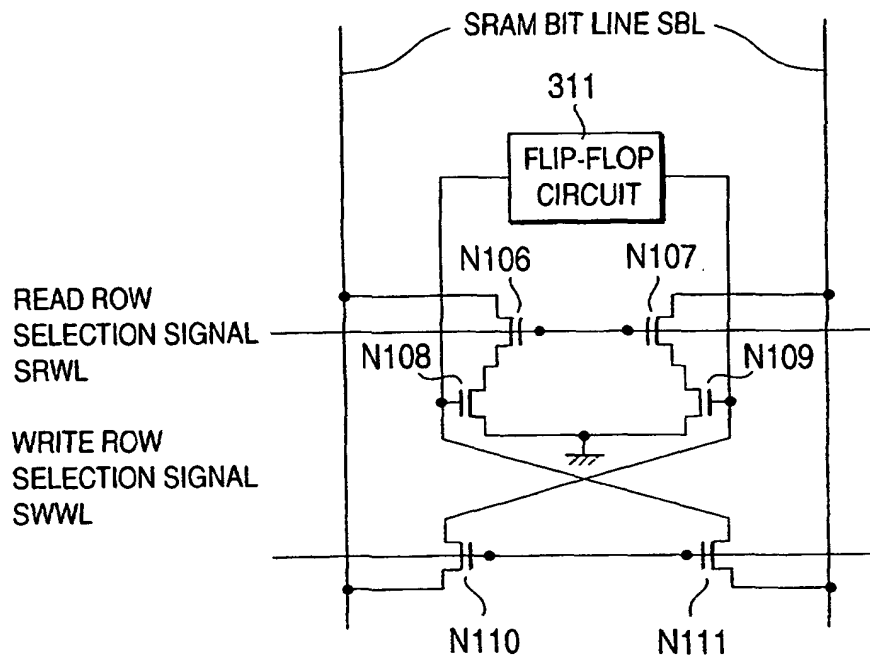


FIG. 72

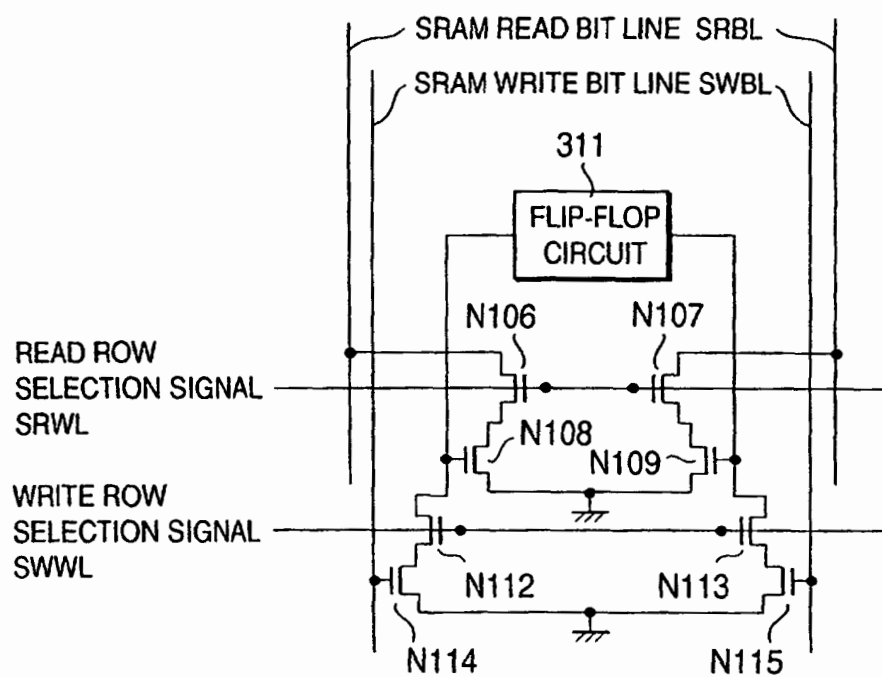


FIG. 73

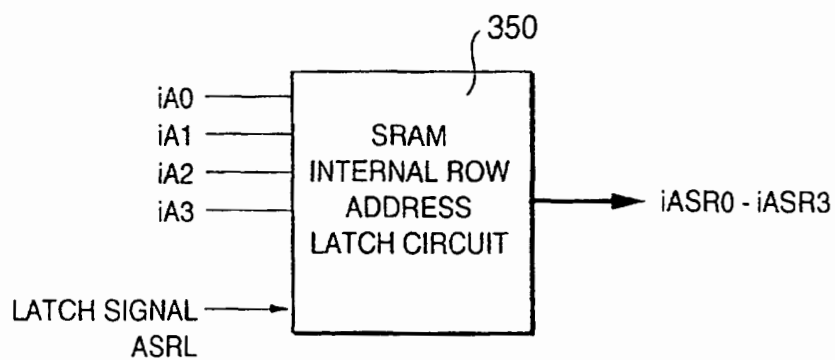


FIG. 74

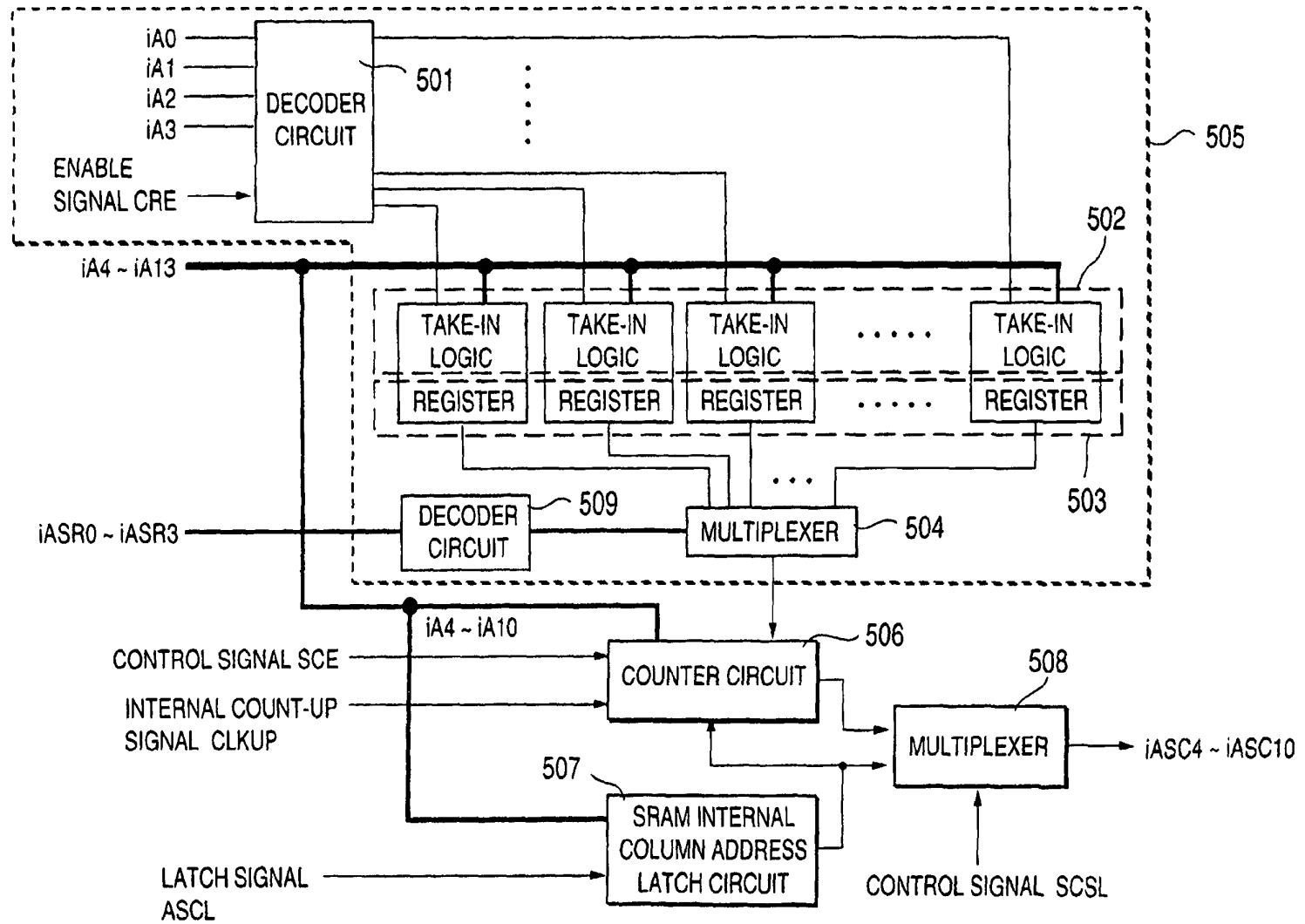


FIG. 75

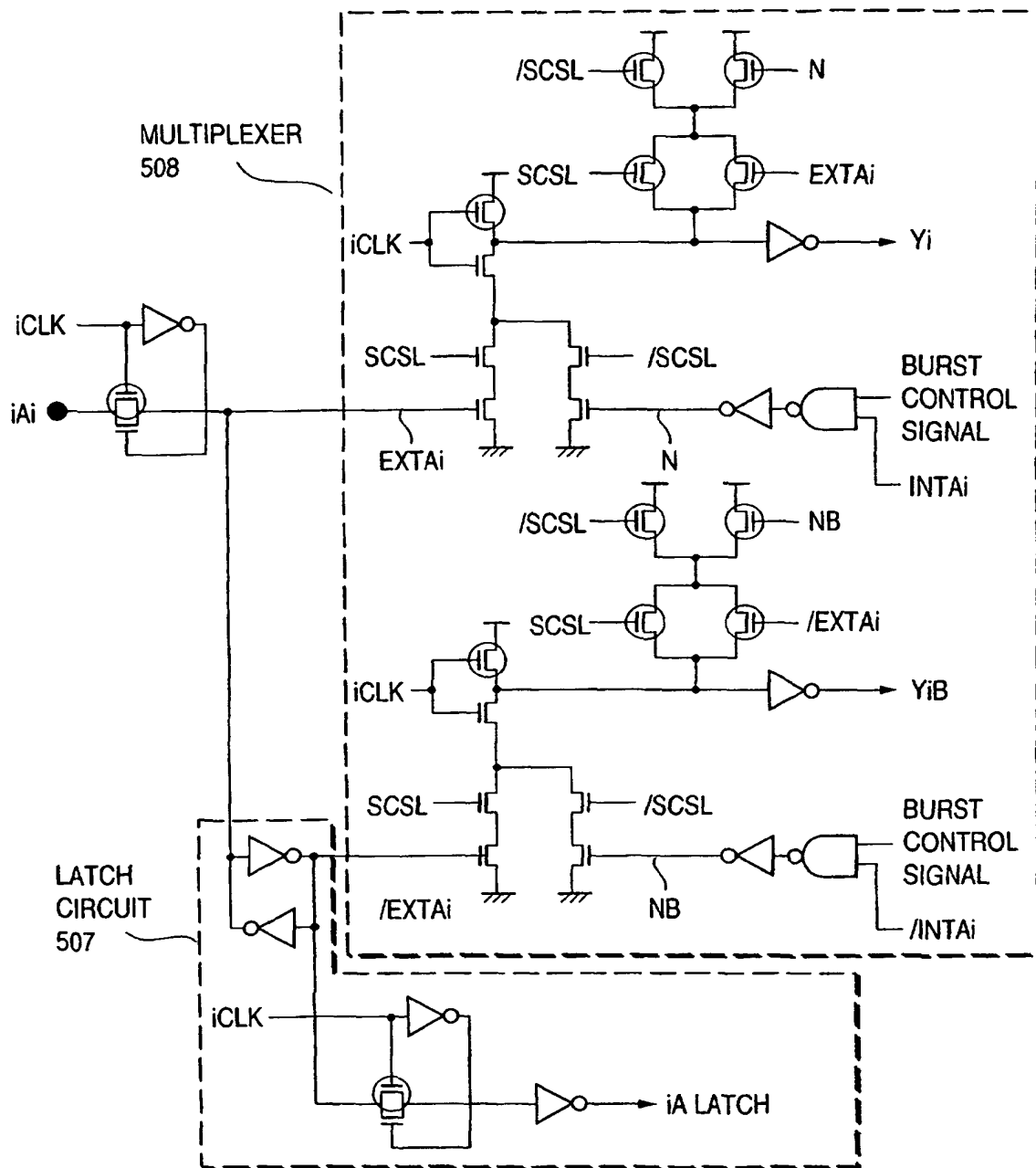


FIG. 76

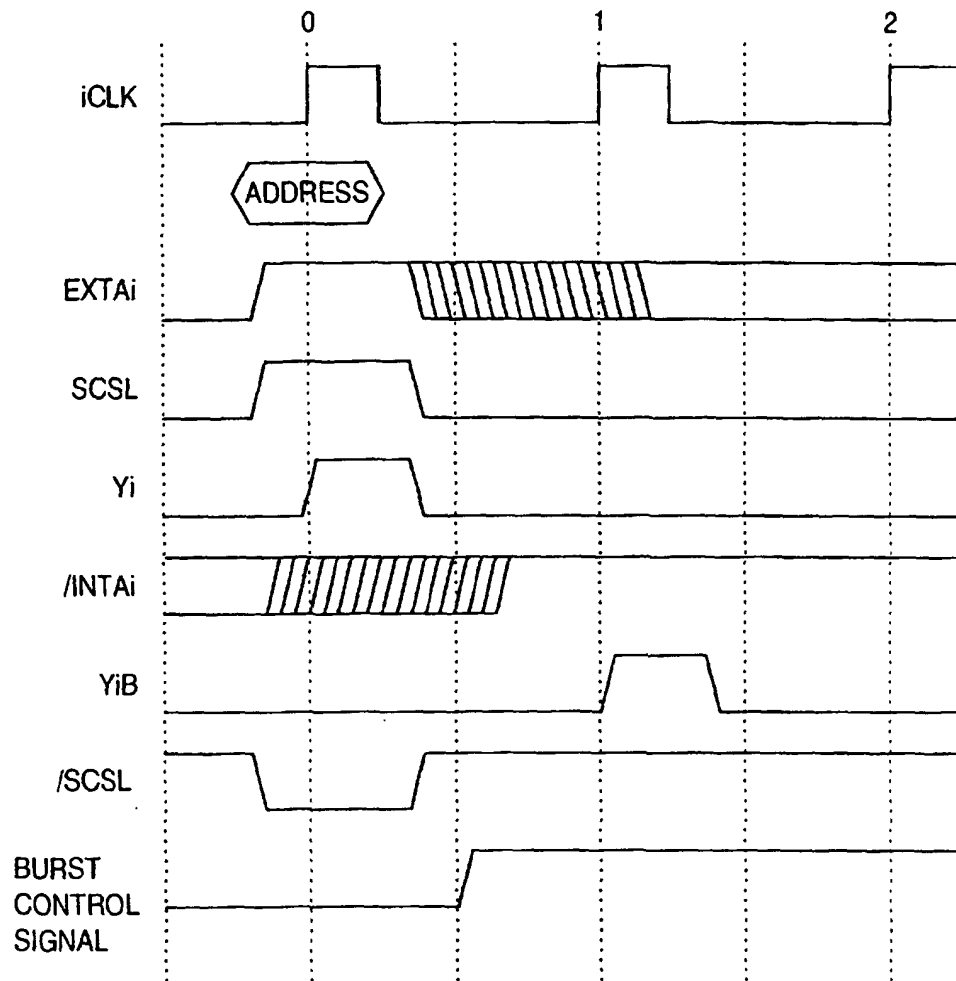


FIG. 77

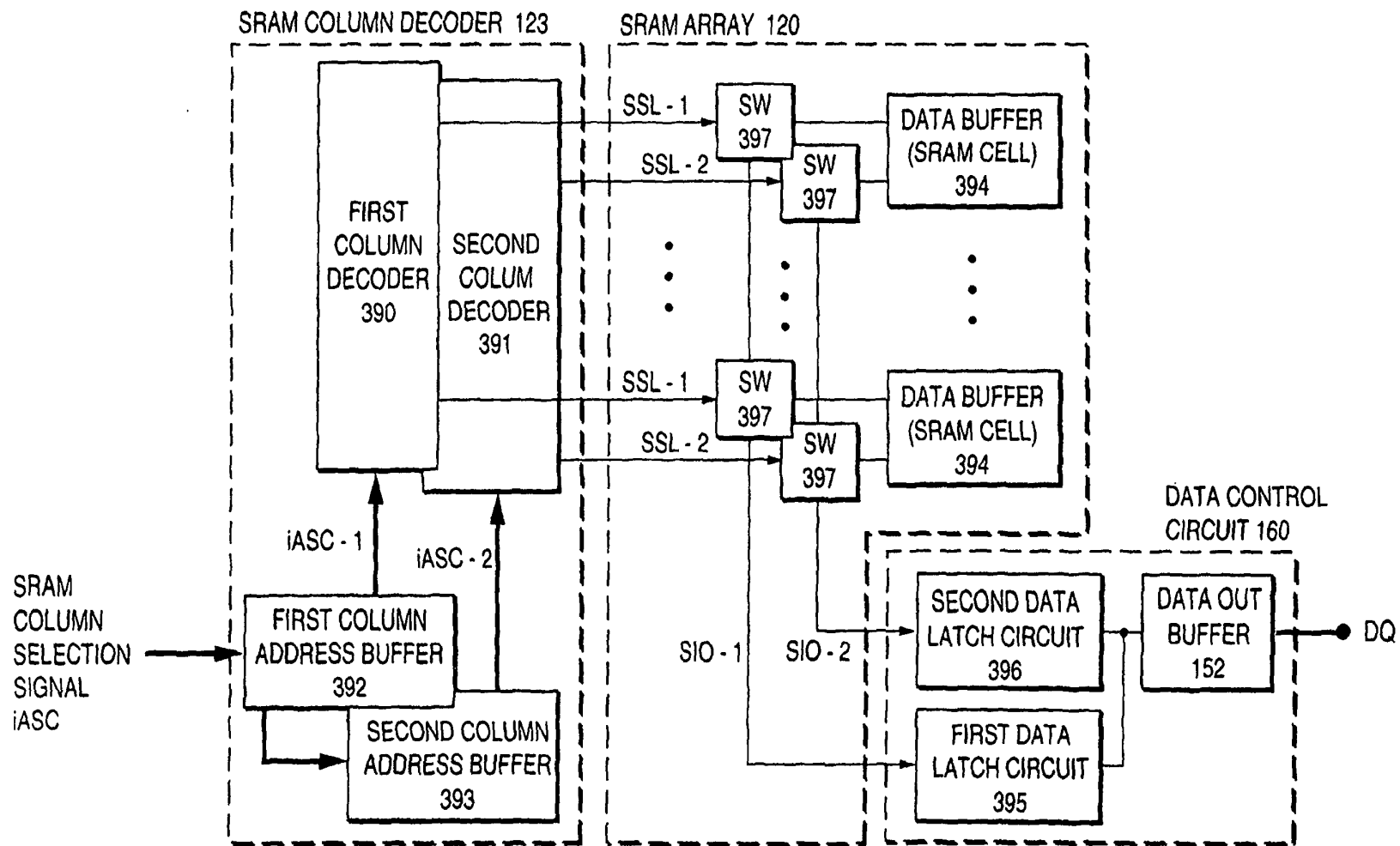


FIG. 78

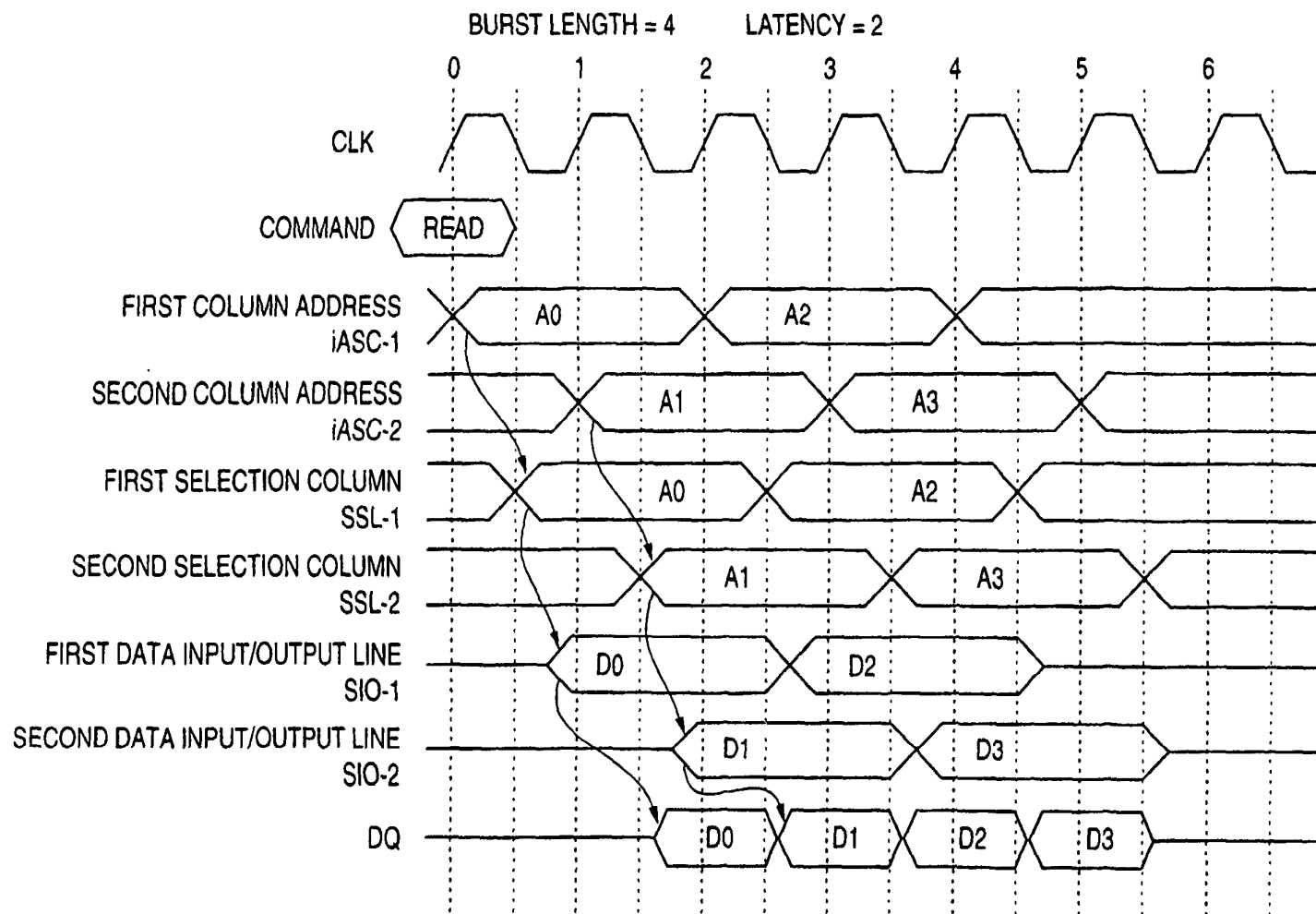


FIG. 79

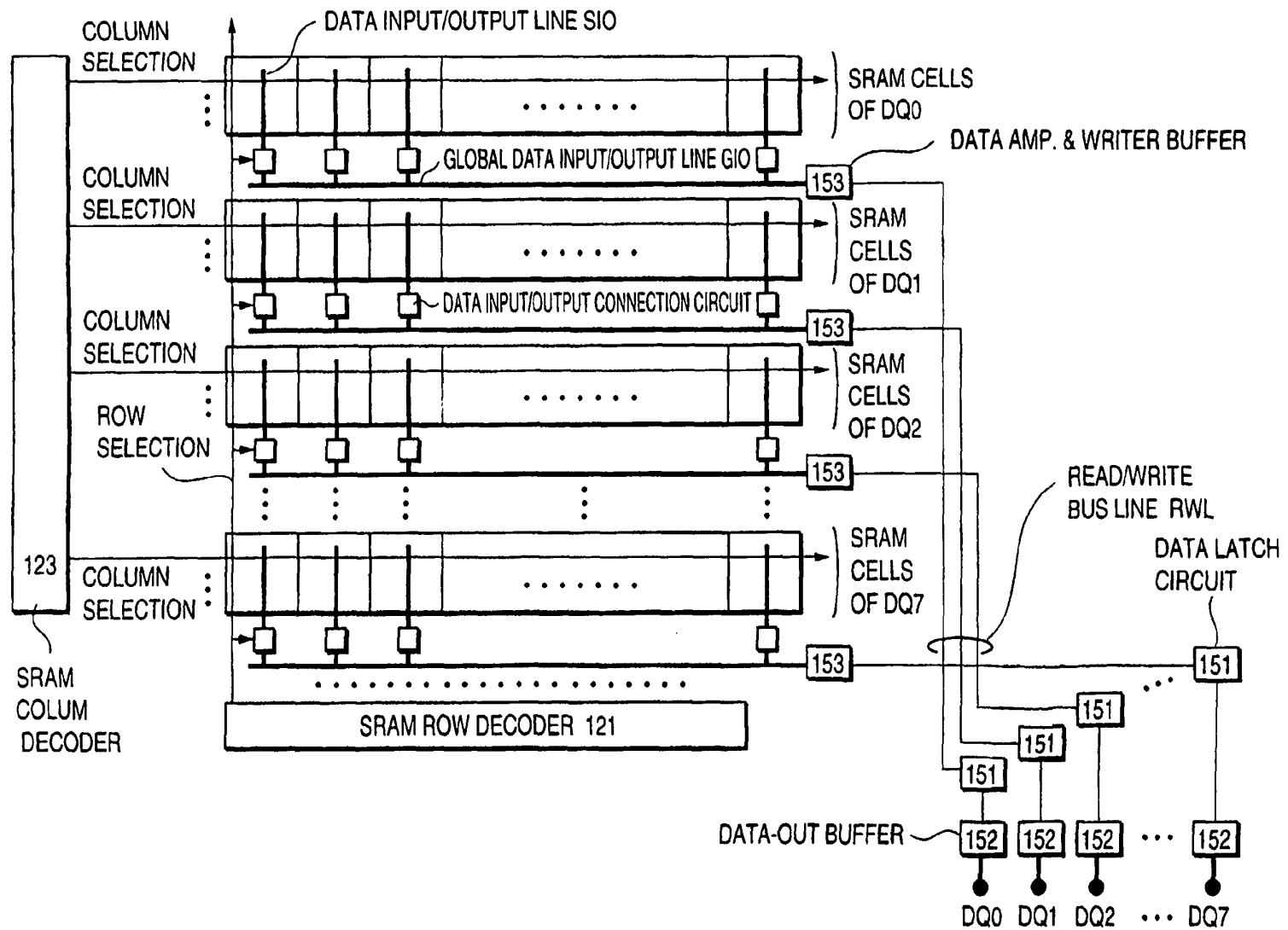


FIG. 80

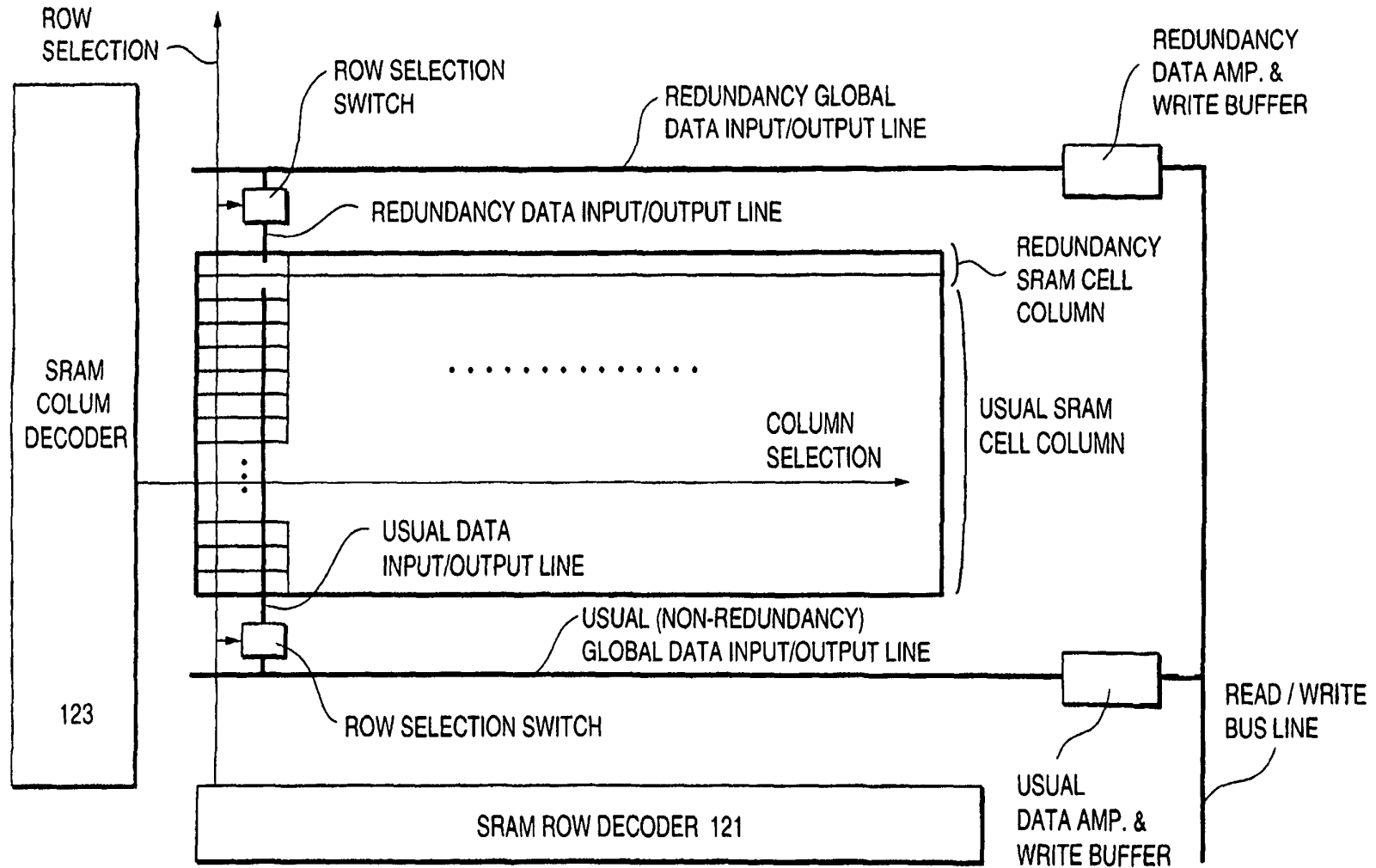


FIG. 81

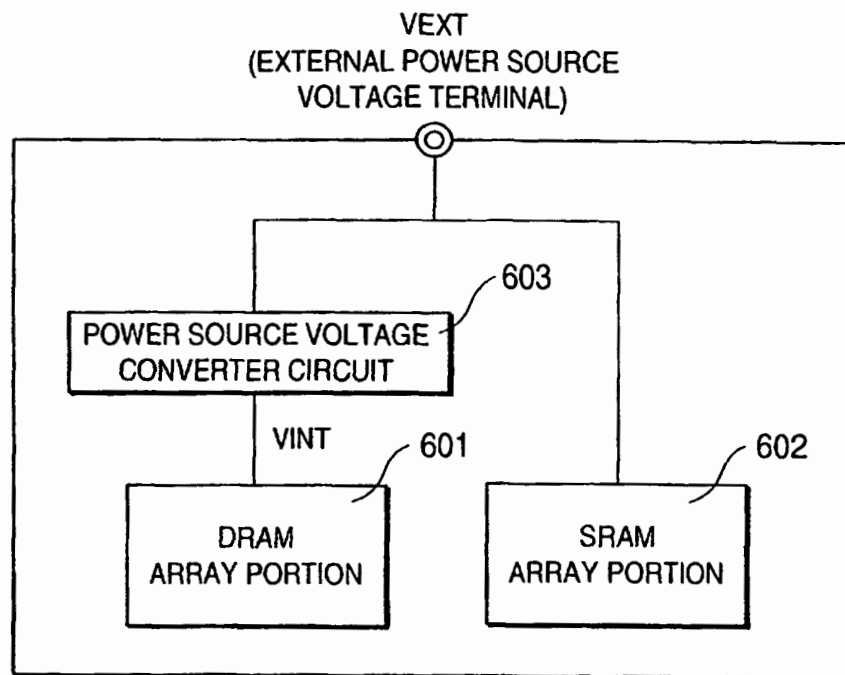


FIG. 82

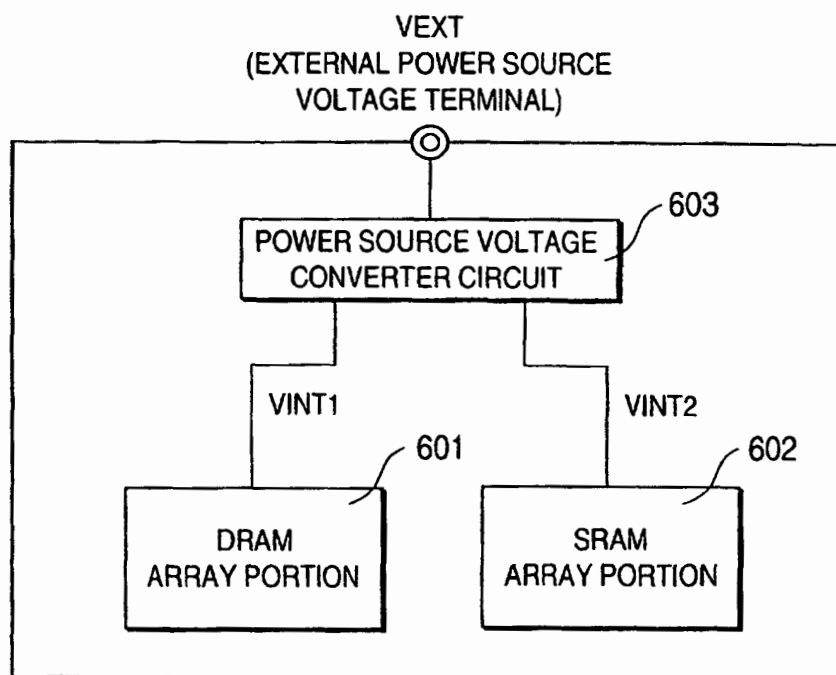


FIG.83

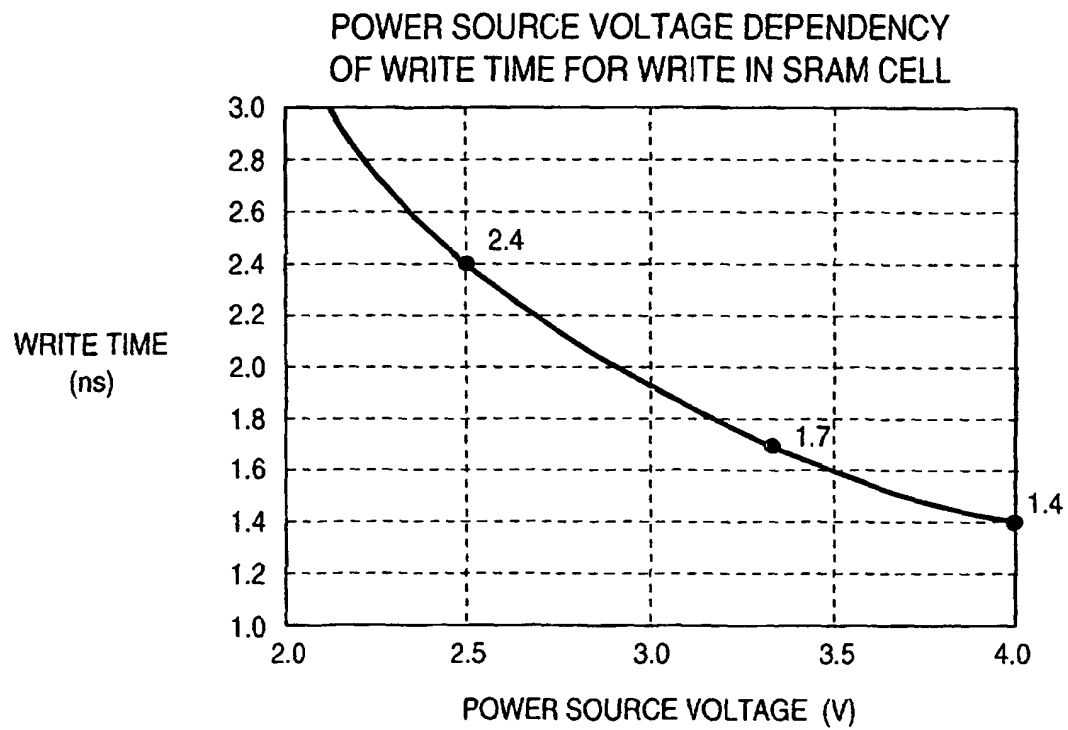


FIG. 84

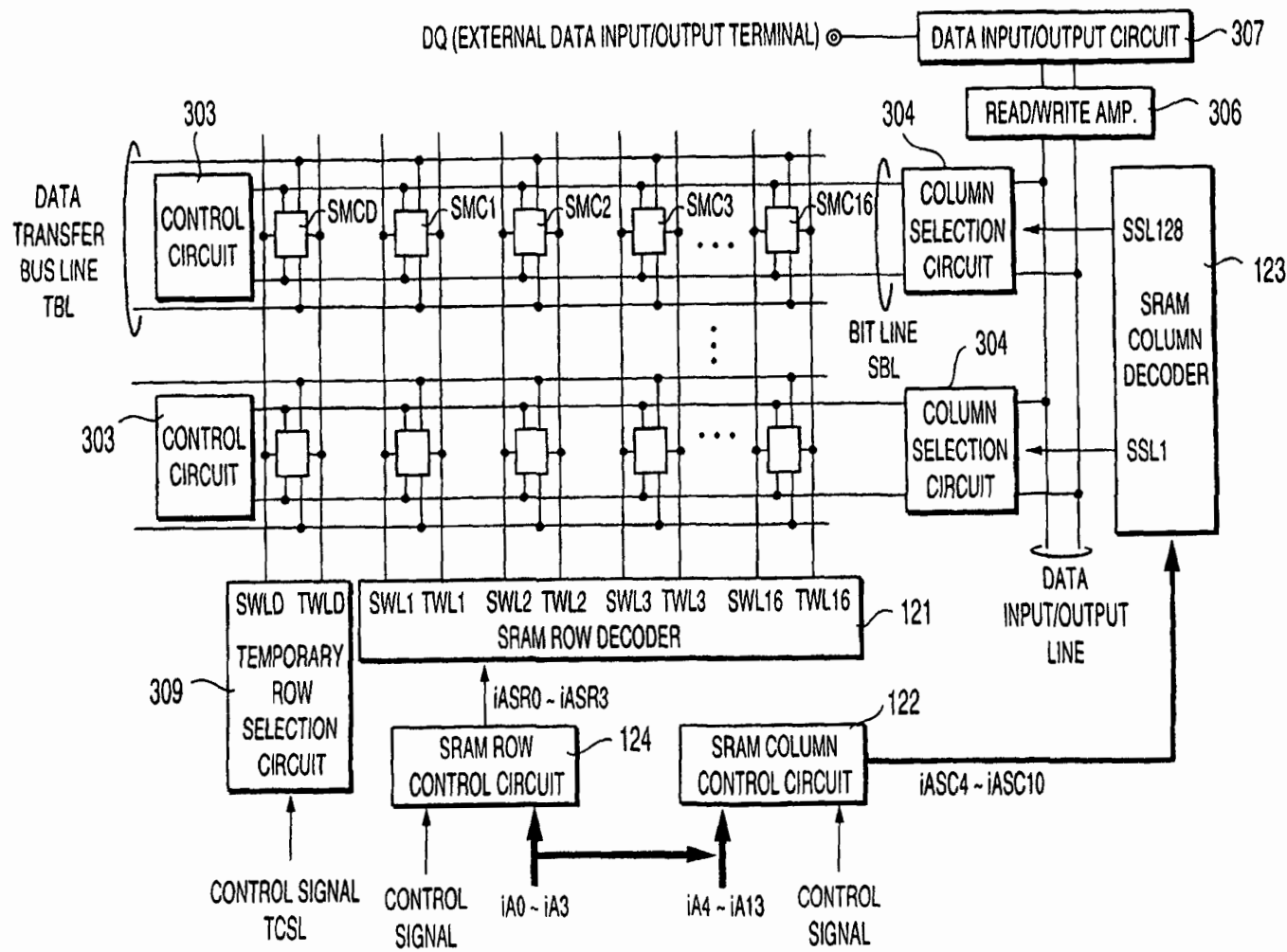


FIG. 85

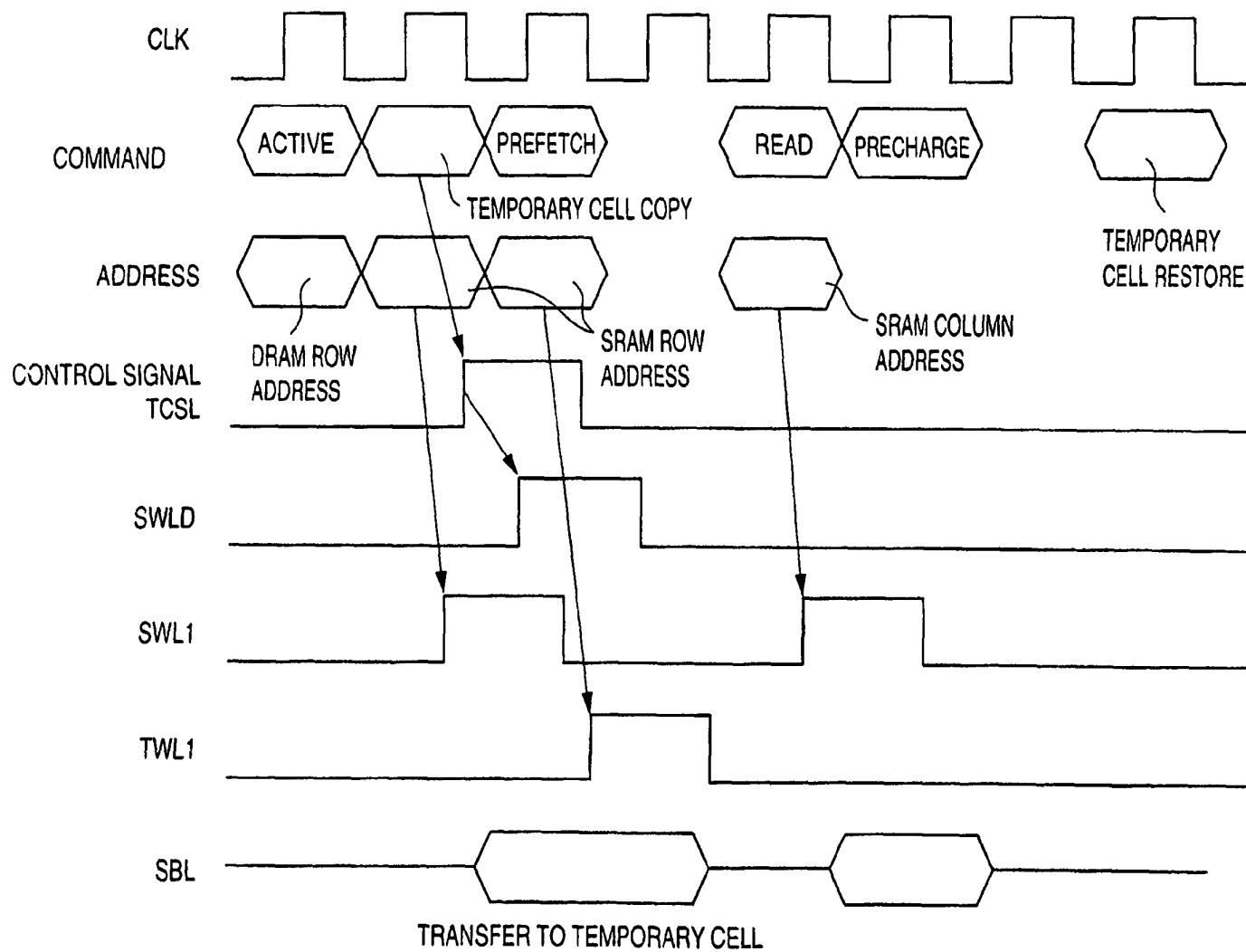


FIG. 86

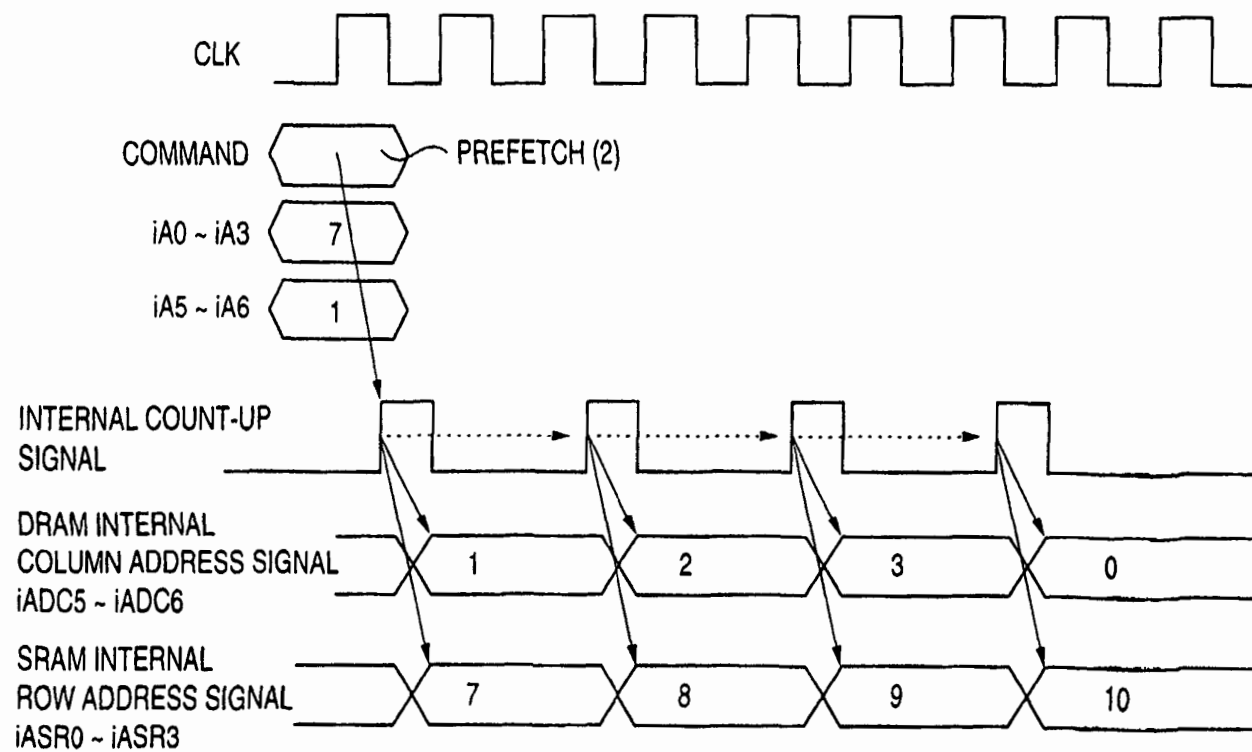


FIG. 87

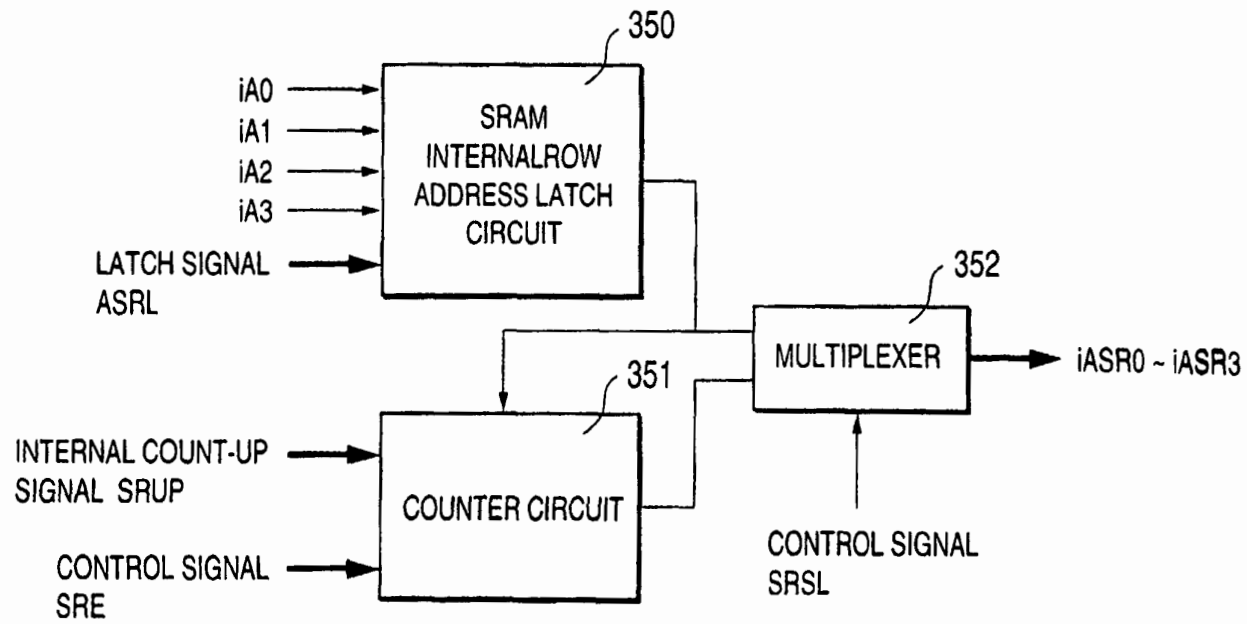


FIG. 88

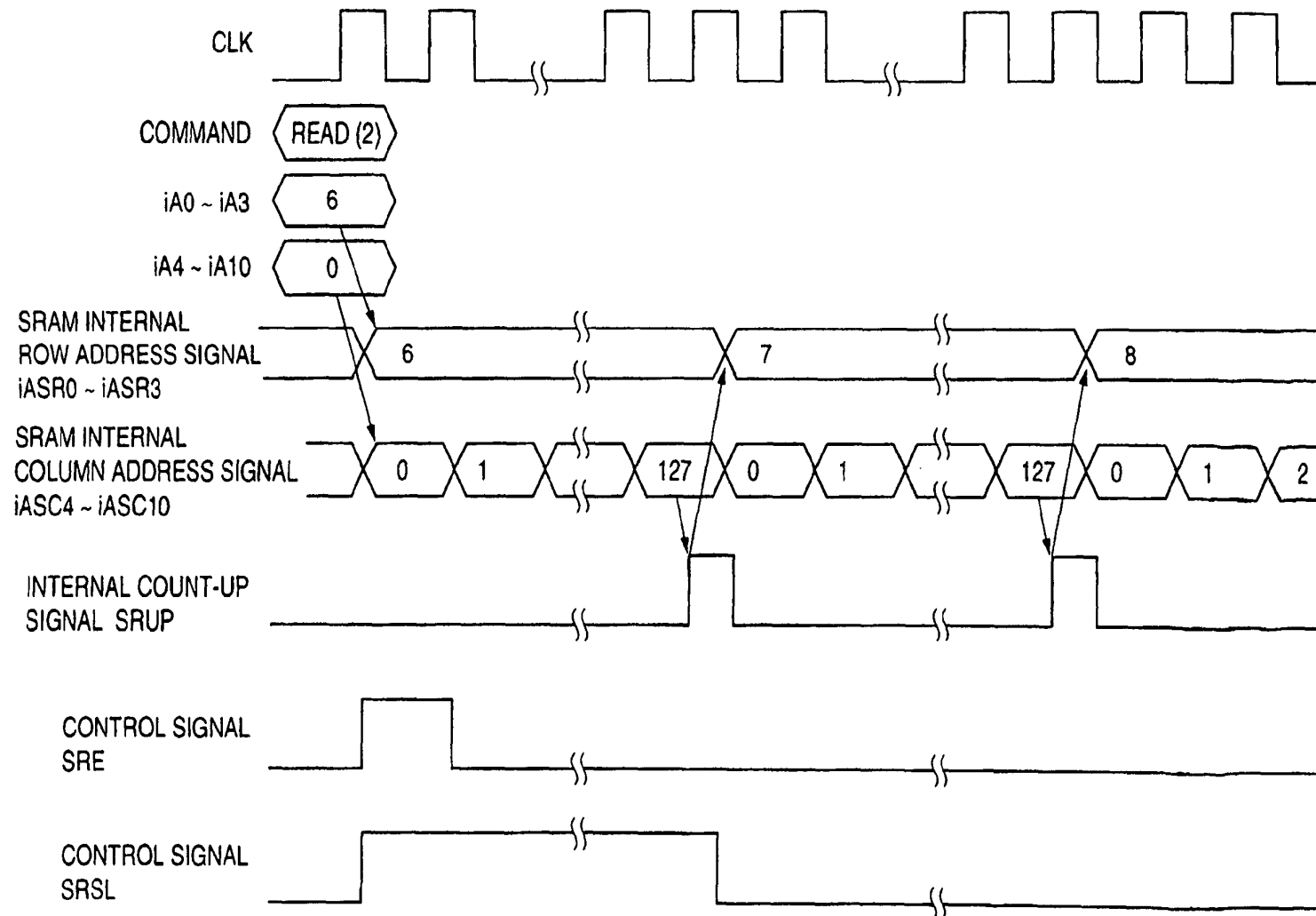


FIG. 89

COMMAND	CKE		$\overline{\text{CS}}$	$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
	n-1	n																		
READ (3)	H	x	L	H	L	H	BURST LENGTH SELECTION			SRAM COLUMN SELECTION							SRAM ROW SELECTION			
WRITE (3)	H	x	L	H	L	H	BURST LENGTH SELECTION			SRAM COLUMN SELECTION							SRAM ROW SELECTION			

H: HIGH LEVEL L: LOW LEVEL x: HIGH OR LOW (DON'T CARE)

FIG. 90

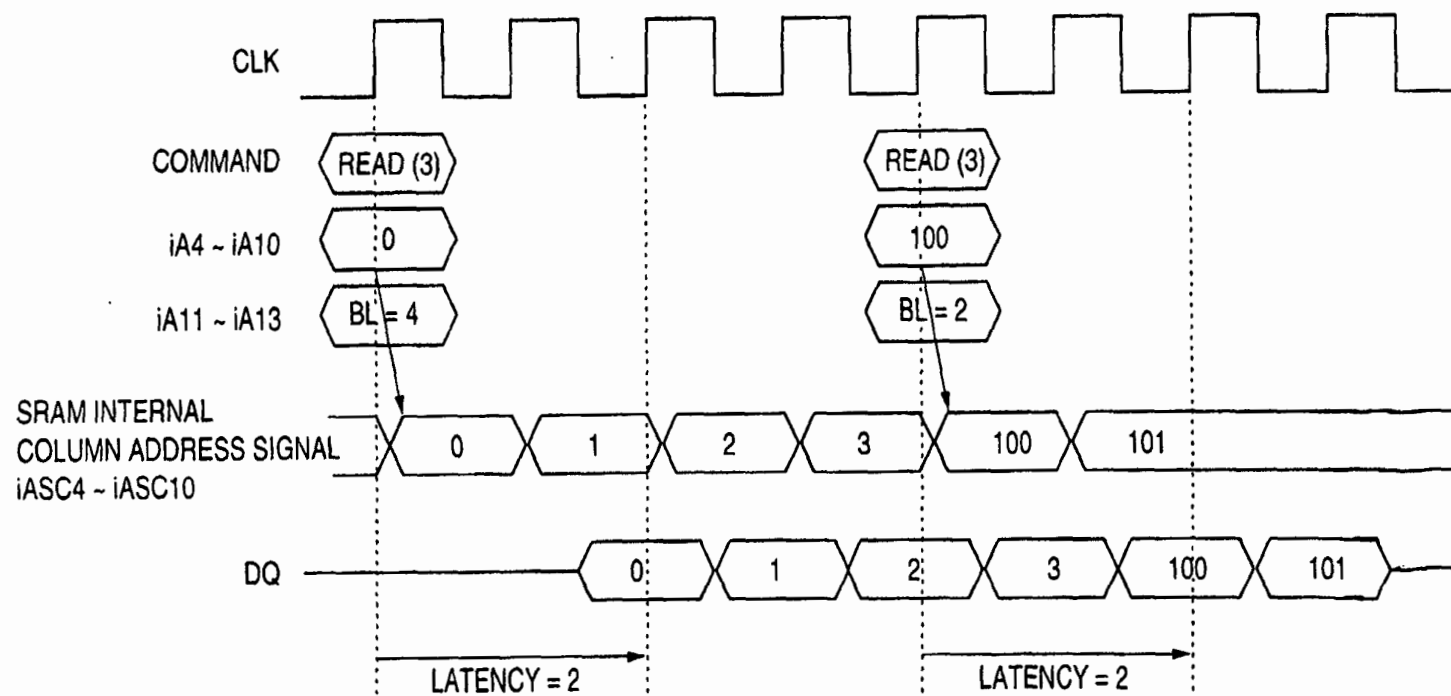


FIG. 91

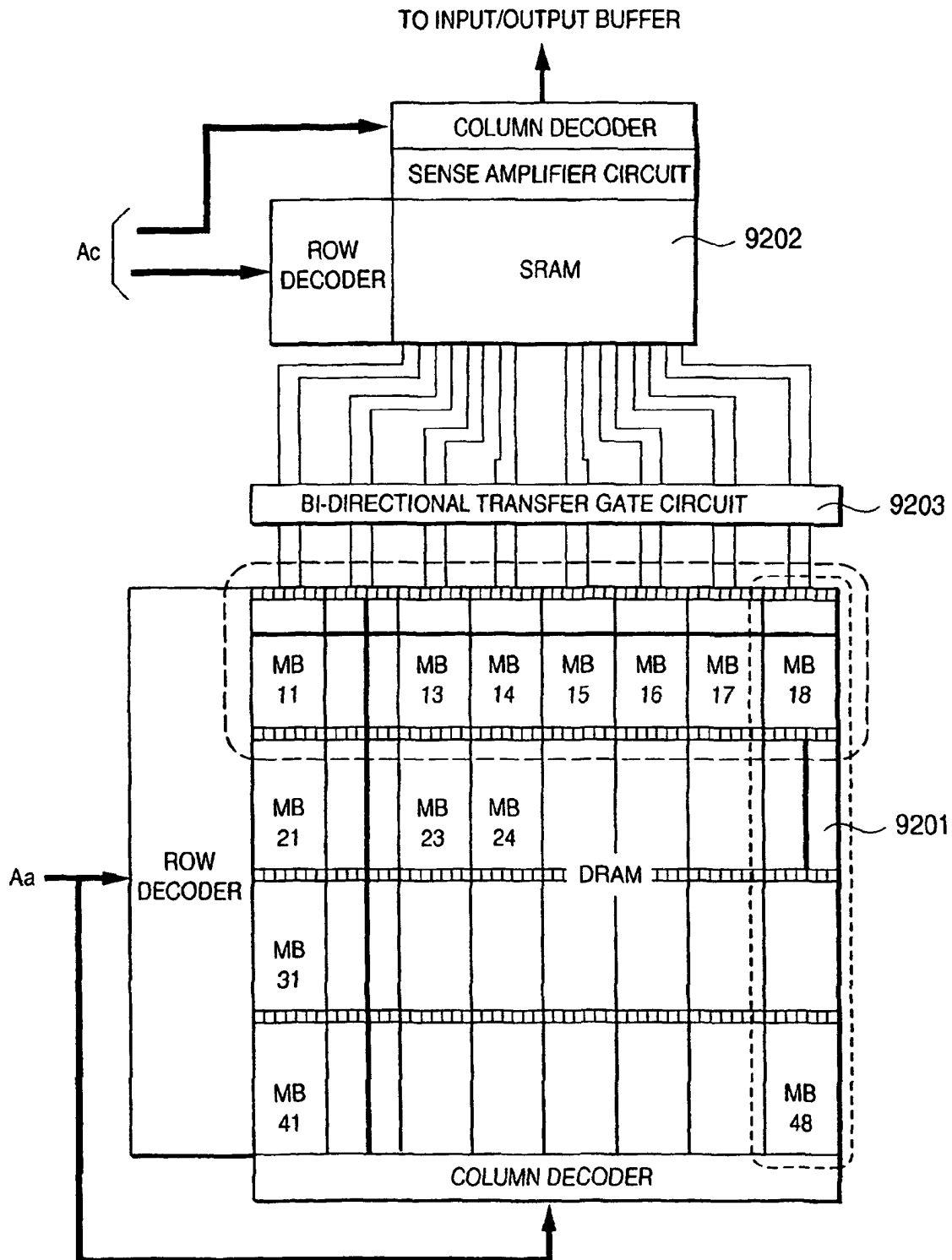


FIG. 92

PRIOR ART

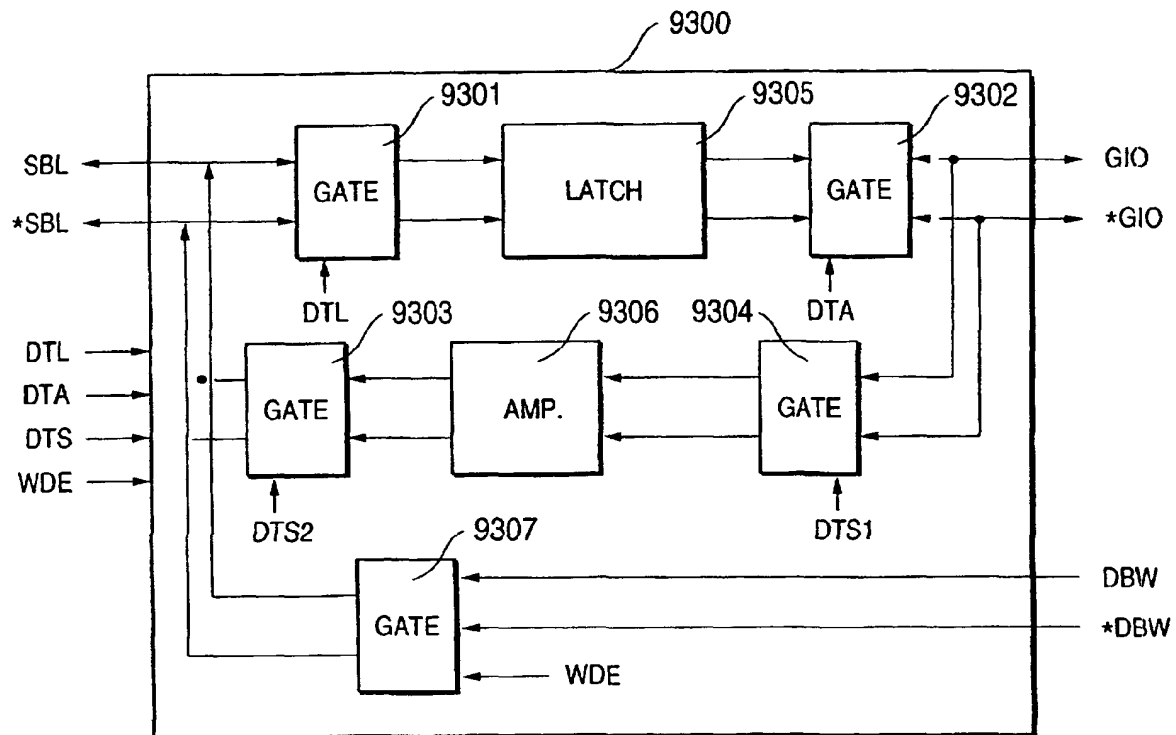


FIG. 93 PRIOR ART

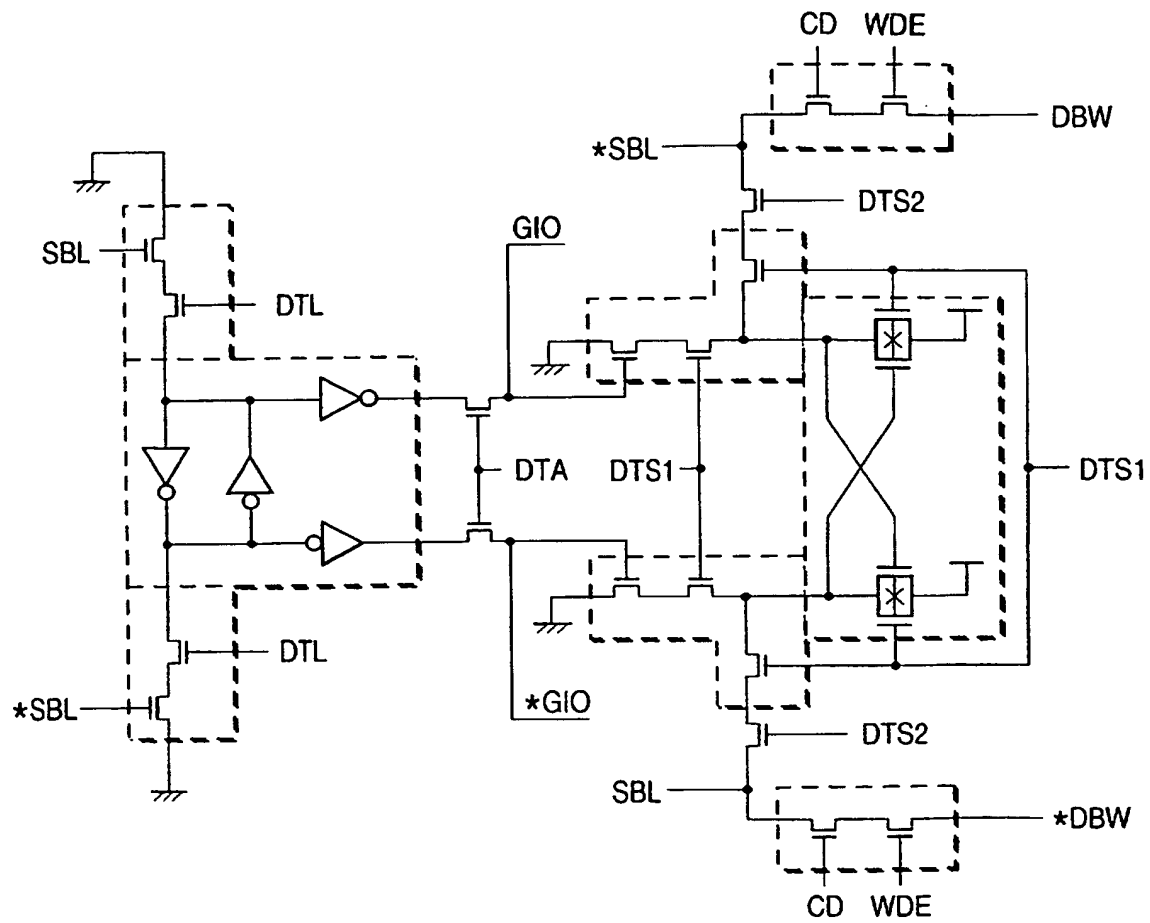


FIG. 94

PRIOR ART

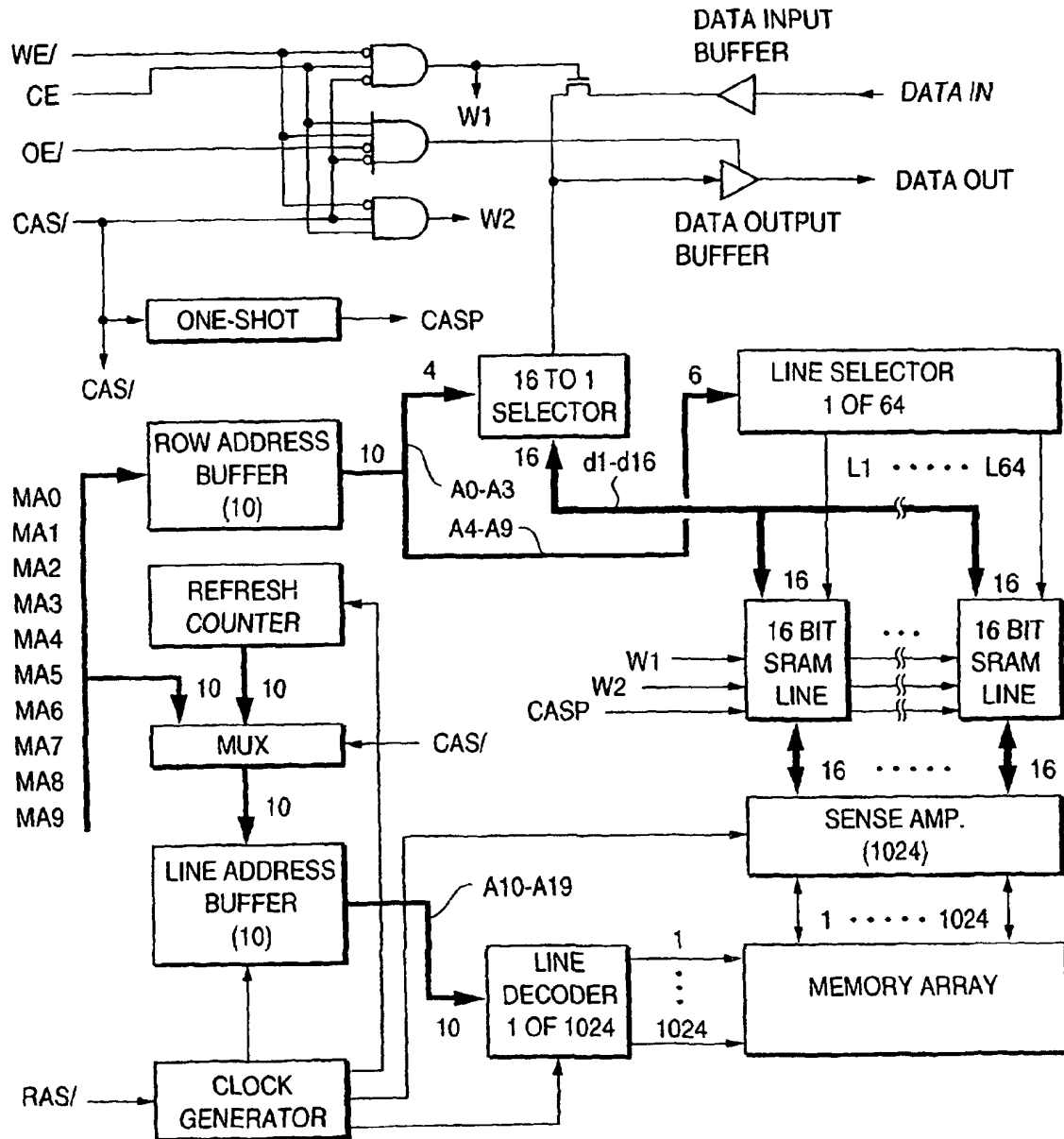


FIG. 95

PRIOR ART

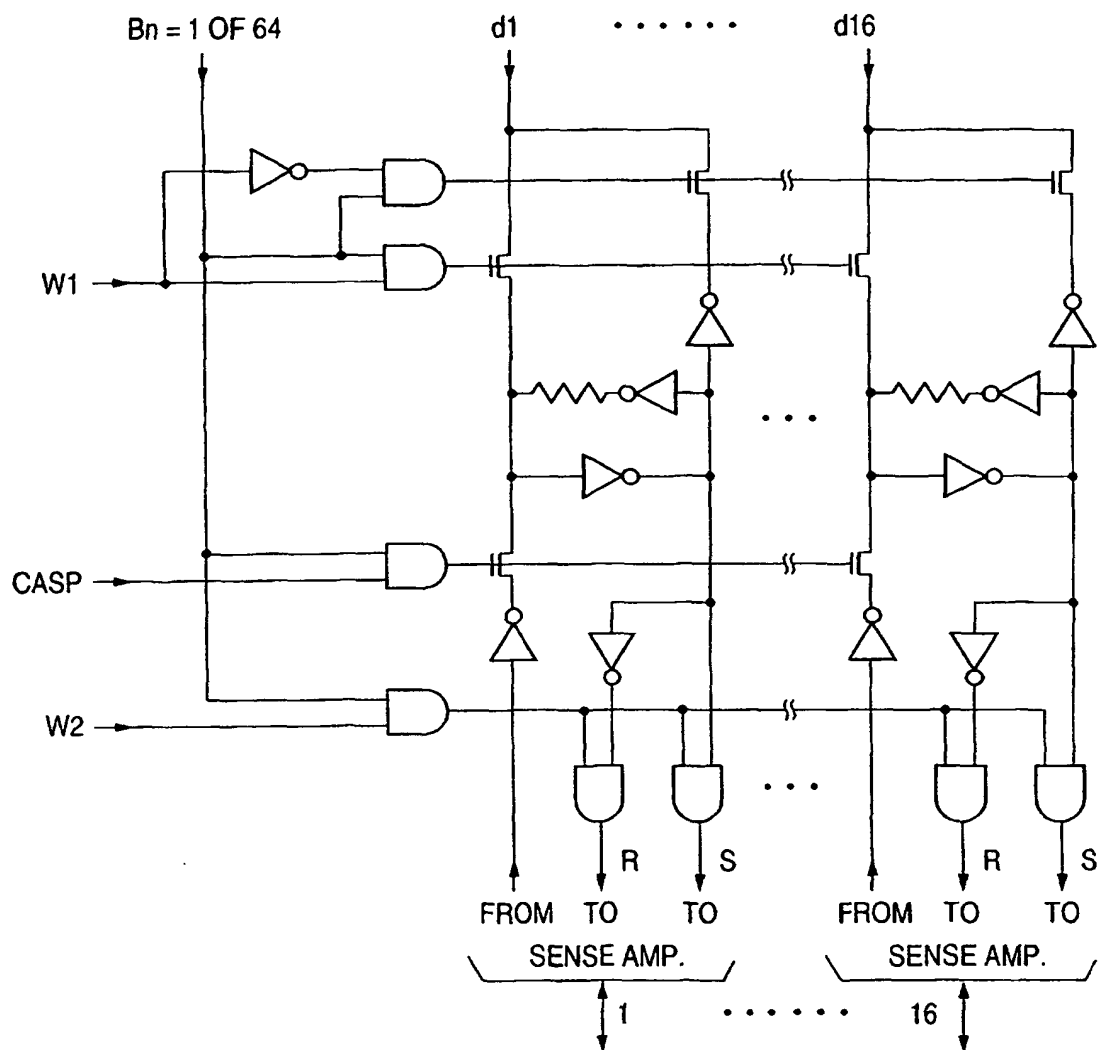


FIG. 96

PRIOR ART

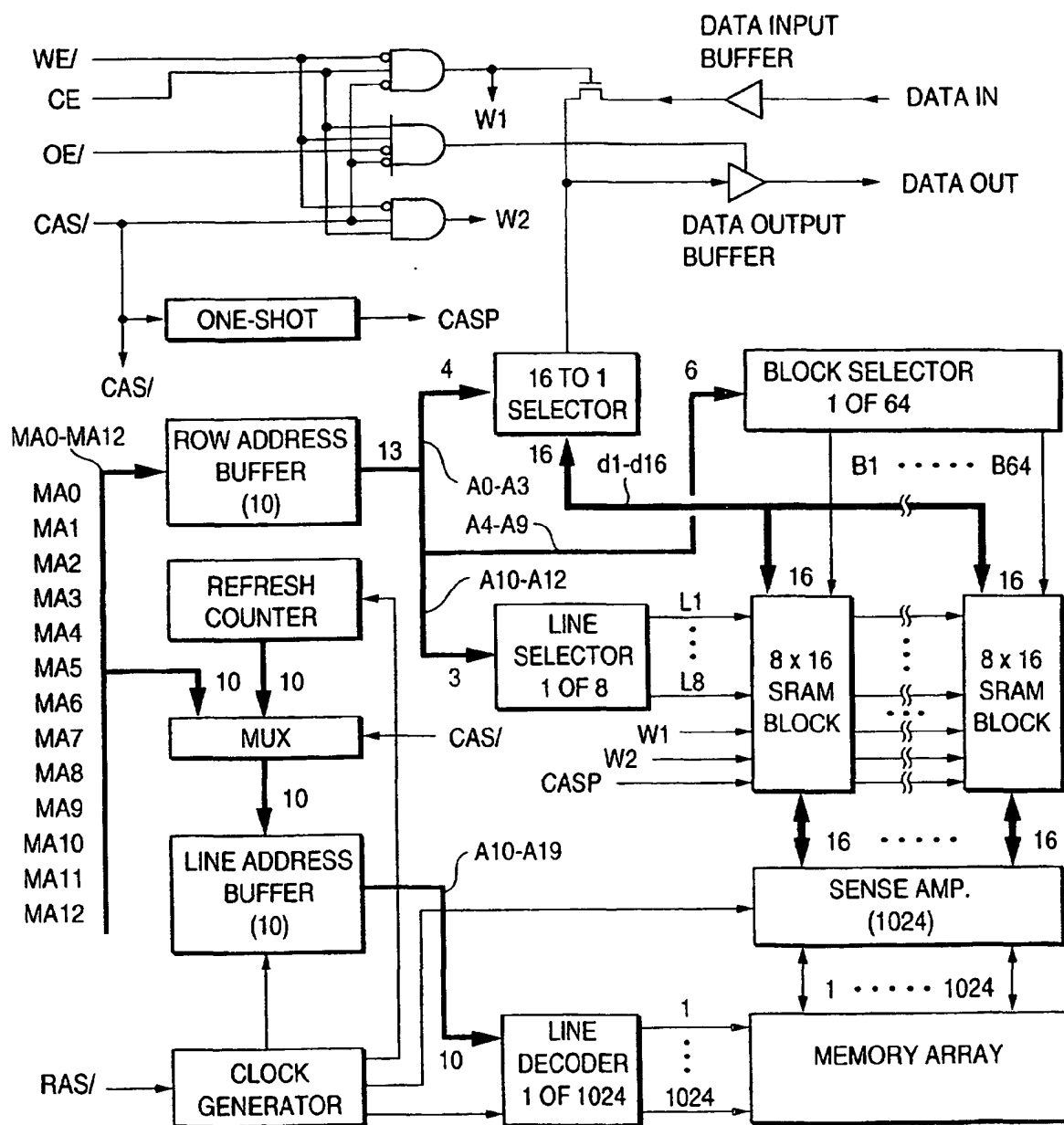


FIG. 97

PRIOR ART

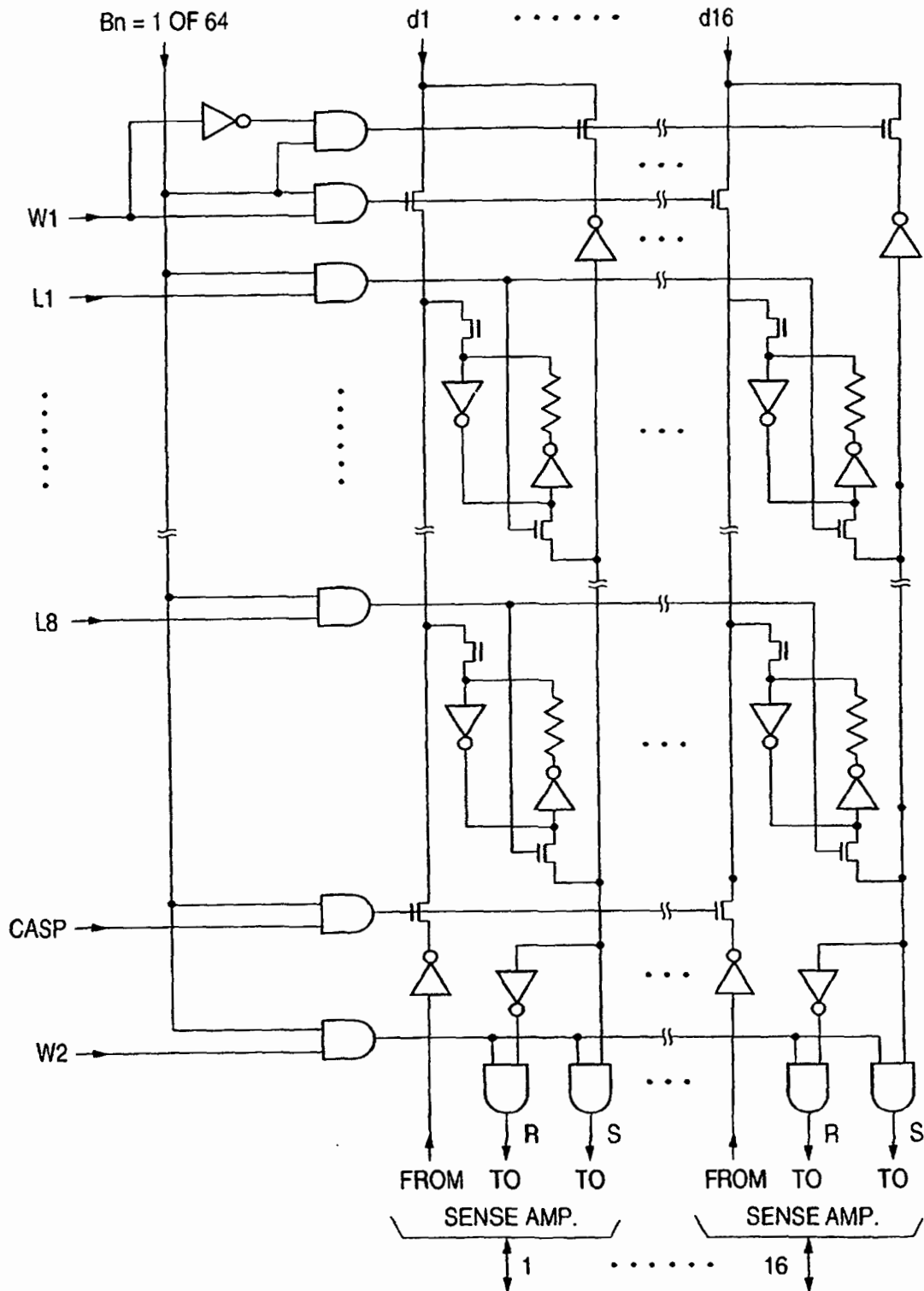


FIG. 98

PRIOR ART

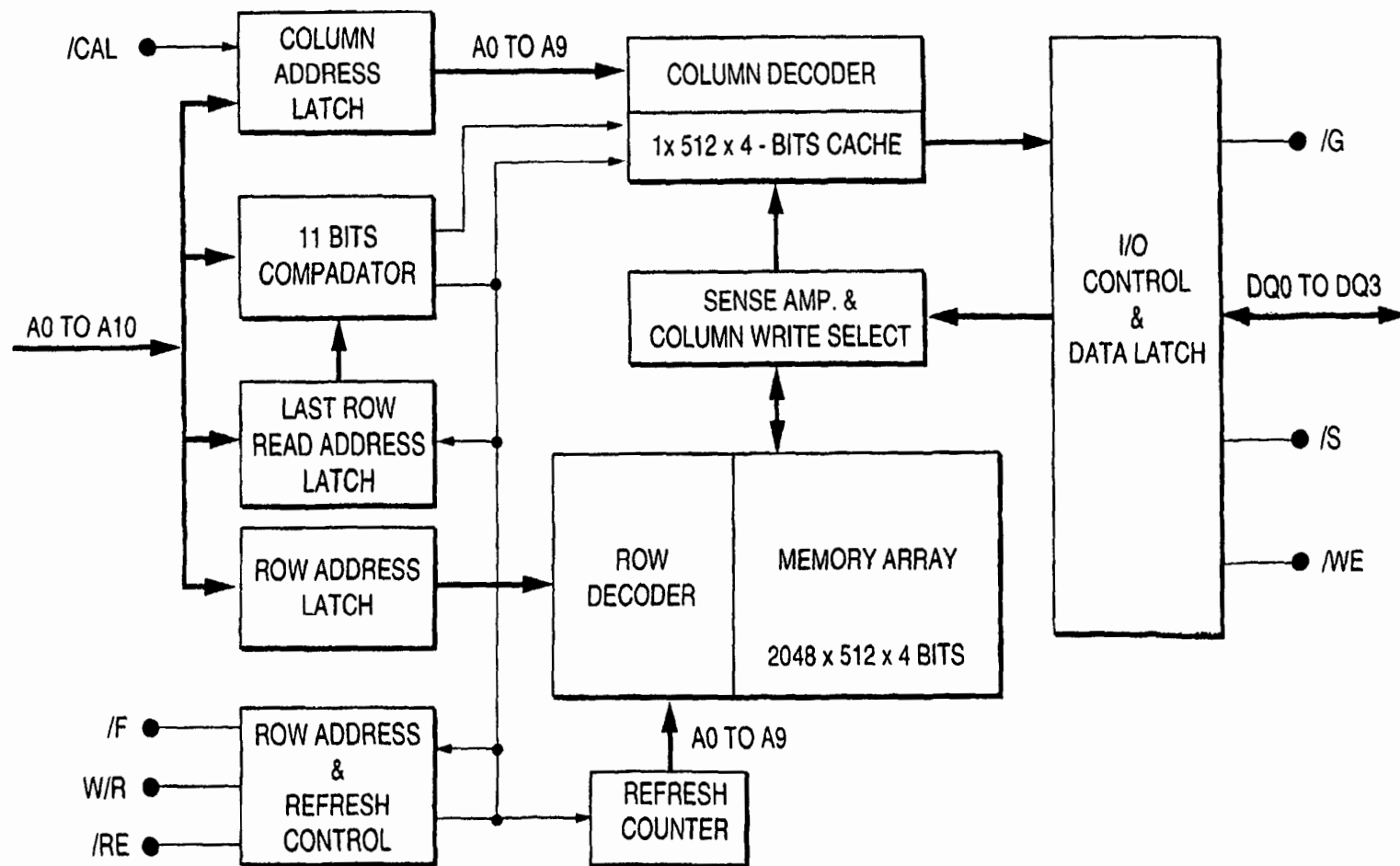


FIG. 99

PRIOR ART

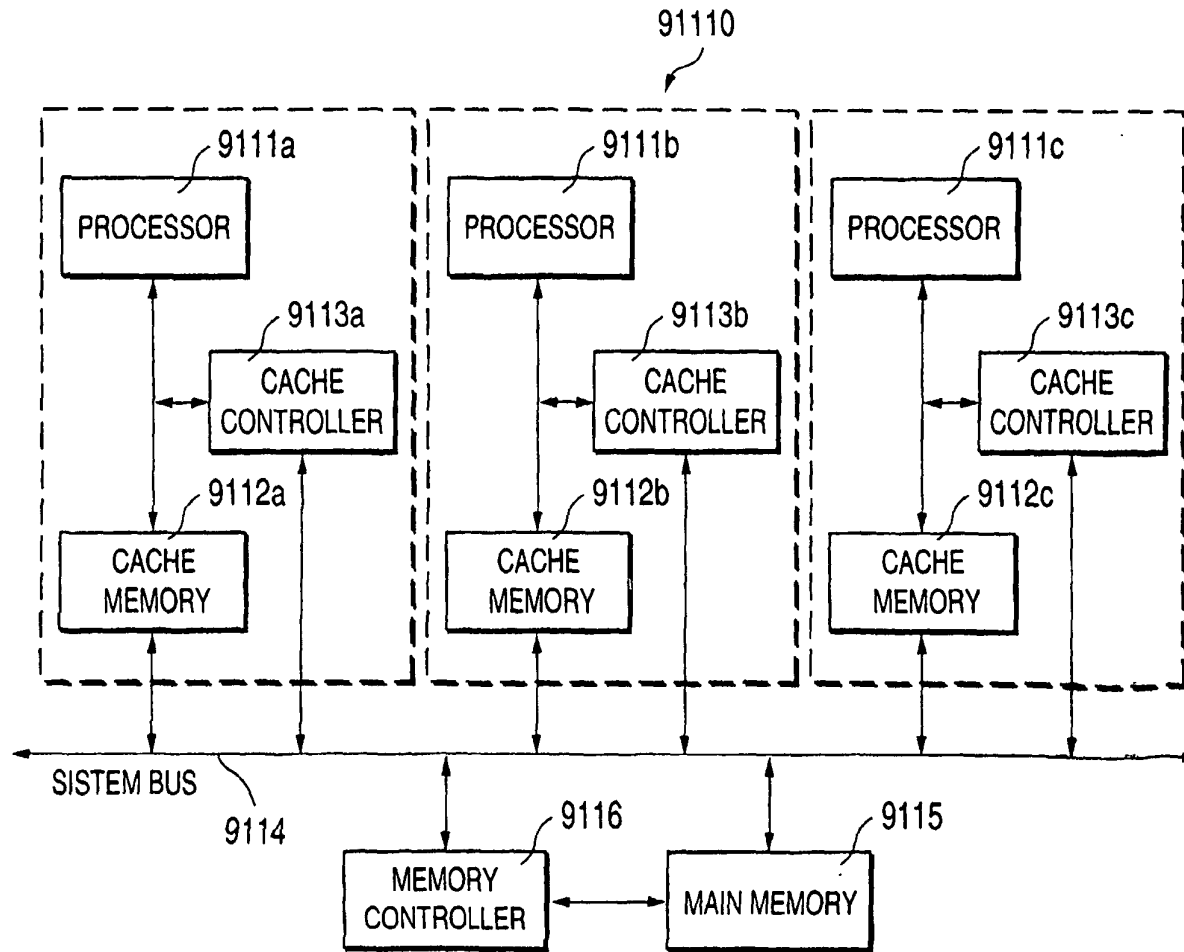


FIG. 100

PRIOR ART



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Priority: JP19950187365 [19950724]

Assignee: CANON INC; CANON KABUSHIKI KAISHA; キヤノン株式会社

Assignee^{std}: CANON KK

Inventor: 石川 祐司

Inventor^{std}: ISHIKAWA YUJI

International class⁸: G06F1/24; G06F1/26; G06F1/28; G06F12/16; G11C11/401; G11C11/403

Title: DRAM CONTROLLER
D R A M制御装置

Abstract:

PROBLEM TO BE SOLVED: To provide the DRAM controller in which a control circuit is integrated.

SOLUTION: A 1st reset signal is active till a voltage of a main power supply is a 1st threshold voltage or below or till a prescribed time elapses after the voltage exceeds the threshold level. A 2nd reset signal is active till a voltage of a monitor signal is a 2nd threshold voltage or below or till a prescribed time elapses after the voltage exceeds the threshold level. Power is supplied from the main power supply or a standby power supply to DRAMs 10, 11. The standby power supply is charged by the main power supply. A DRAM control means 8 is driven by the main power supply and transmits the DRAMs 10, 11 to a backup state when the 1st reset signal is active and a monitor voltage output is changed to be the 2nd threshold level or below. When the 1st reset signal is inactive, the monitor voltage output is set to a voltage in excess of the 2nd threshold level to restore the DRAMs 10, 11 from the backup state. The CPU 7 is driven by the main power supply and reset by the 2nd reset signal.

【要約】 【課題】 制御回路を集積化できるD RAM制御装置を提供すること。 【解決手段】 第1のリセット信号は、主電源の電圧が第1の閾値以下、または閾値を越えてから所定の時間が経過するまでアクティブになる。第2のリセット信号は監視電圧が第2の閾値以下、または閾値を越えてから所定の時間が経過するまでアクティブになる。DRAMには、主電源または予備電源から電力が供給される。予備電源は主電源により充電される。DRAM制御手段は主電源により駆動され、第1のリセット信号がアクティブになると、DRAMをバックアップ状態に遷移させ、その後監視電圧出力を第2の閾値以下に変化させる。第1のリセット信号がアクティブでなくなると監視電圧出力を第2の閾値を越える電圧にし、DRAMをバックアップ状態から復帰させる。CPUは主電源により駆動され、第2のリセット信号によりリセットされる。

Claims:

【特許請求の範囲】

[Claims]

1. (1)主電源の電圧が第1の閾値以下の 期間、および前記電圧が前記第1の閾値以下の電圧から 当該閾値を越えた電圧に変化してから第1の所定の時間 が経過するまでの期間に、第1のリセット信号をアクティブにし、他の期間に前記第1のリセット信号を非アクティブにする第1の電圧監視手段と、(2)監視電圧が 第2の閾値以下の期間、および前記監視電圧が前記第2 の閾値以下の電圧から当該閾値を越えた電圧に変化して から第2の所定の時間が経過するまでの期間に、第2の リセット信号をアクティブにし、他の期間に前記第2の リセット信号を非アクティブにする第2の電圧監視手段 と、(3)主電源が投入されている時に充電され、前記 主電源が投入されていないときに放電する予備電源と、(4) 前記主電源が投入されているときに前記主電源から電力が供給され、前記主電源が投入されていないとき に前記予備電源から電力が供給されるD RAMと、(5) 前記主電源により駆動されるDRAM制御手段であって、前記第1のリセット信号がアクティブになると、前記D RAMをバックアップ状態に遷移させるDRAM制御信号を出力し、その後に前記監視電圧を前記第2の閾値以下に変化させる手段と、前記第1のリセット信号がアクティブでなくなると、前記監視電圧を前記第2の閾値を越える電圧に変化させ、前記D RAMをバックアップ状態から復帰させるD RAM制御信号を出力する手段とを有するD RAM制御手段 と、(6)前記主電源により駆動され、前記第2のリセット信号によりリセットされるCPUとを備えたことを 特徴とするDRAM制御装置。

2. 前記DRAM制御手段は、前記第1のリ セット信号がアクティブになると、前記C P Uが前記D RAMをアクセスしないバス.タイミングで前記DRA Mをバックアップ状態に遷移させることを特徴とする請求項1に記載のD RAM制御装置。

3. 前記第1の所定の時間が前記第2の所定 の時間よりも短いことを特徴とする請求項1又は2に記載のDRAM制御装置。

4. 前記第1のリセット信号が、前記C P U のバス.ホールド要求入力に入力されていることを特徴 とする請求項1から3のいずれかに記載のD RAM制御装置。

1. (1) mains voltage of period, and the first voltage is less than the threshold value of the first threshold value or less of the voltage from the voltage exceeds the threshold value, from changes to the first predetermined time has elapsed, the first reset signal to the associative period and other non-the first reset signal to the first voltage monitoring means for monitoring voltage is the threshold value or less of the (2) the second period, and the threshold value or less of the monitoring voltage is the second voltage from the voltage exceeds the threshold value, from changes to the second predetermined time has elapsed, the second reset signal is activated, the other periods of the second reset signal to the second voltage monitoring means deactivating the main power supply is turned on, (3) when charged, the main power supply is turned on to discharge the standby power supply when it is not, (4) the main power supply is turned to the main power supply to power is supplied, the main power supply is turned on when it is not electric power is supplied from the standby power supply, (5) the main power supply D RAM and is driven by the control means, the first DRAM of the reset signal becomes active, the back D RAM to transition to the state control signal abbu DRAM, then the monitoring voltage to said second means to vary the threshold value to below the first of the reset signal becomes active, the before-mentioned monitoring voltage to said second voltage, the D exceeds the threshold value is changed, to return from the RAM to the backup state, and outputs a control signal D RA means M D, (6) RAM of the main power supply and control means driven by the second signal a second pldget is reset by the CPU (control device, characterized in that it comprises a DRAM.

2. The control means, the first DRAM set of the signal becomes active, D the RAM C P U is not access to the bath. M at the timing abbu DRA state to transition to the claim 1, wherein the D-RAM control device.

3. The first predetermined time is shorter than a predetermined time claim 1 or 2, characterized in that the DRAM control apparatus of

4 PU reset signal is input the C bus is input to the hold request, characterized in that according to any one of claims 1 to 3. D-RAM control device.

5. The standby power supply is capable of supplying power to the power signal indicating

Samsung Electronics Co., Ltd.

Ex. 1002, p. 814

5. 前記予備電源は、電力を供給できるか否 か示す電力信号を充電容量に応じて出力する出力手段を有し、前記D RAM制御手段は、前記第1のリセット信号が非 アクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ状態から復帰させる復帰制御を行うか、スタンバイ状態から起動させる起動制御を行うかを決定することを特徴とする請求項1から4のいずれかに記載のD RAM制御装置。

6. 前記予備電源は、電力を供給できるか否 か示す電力信号を充電容量に応じて出力する出力手段を有し、前記DRAM制御手段は、前記第1のリセット信号がアクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ。状態とするかスタンバイ状態とするかを決定することを特徴とする請求項1から5のいずれかに記載のDRAM制御装置。

whether or not the charging capacity an output means for outputting in accordance with the RAM, the D control means, said first when the reset signal becomes inactive, the power in response to a signal from the DRAM or backup state performing a return control for returning from the standby state to the start-up to determine whether the start-up control to claim 1, further characterized in that it is RAM of the control device D

6. The standby power supply is capable of supplying power to the power signal indicating whether or not the charging capacity an output means for outputting in accordance with the control means, the first DRAM reset signal indicates an inactive, in response to the power signal. DRAM backup State and the standby state, characterized in that to determine whether the claim 1, wherein control device according to any deviation of DRAM

Description:

【発明の詳細な説明】 【0001】 【発明の属する技術分野】 本発明は、DRAMのセルフリフレッシュモードを使ってバックアップするDRAM制御装置に関する。 【0002】 【従来の技術】 従来、DRAMをバックアップする手法としては、主電源が切断された時D RAMをセルフリフレッシュ■モードにするのが、もっとも一般的である。しかしながら、DRAMをセルフリフレッシュ■モードにするには、通常のアクセス時のRAS /CASシーケンスとは異なるシーケンスが要求される。しかも、通常のアクセスのシーケンスからセルフリフレッシュ.シーケンスへは、DRAMが要求する各種タイミング条件を満たすように移行しなければならない。主電源が低下したときに、アクセスのシーケンスを突然中断してしまうことは許されない。 【0003】 更に、バックアップ電源が供給されていた状態から主電源に切り替わった場合はセルフリフレッシュ-モードからの復帰シーケンスを実行し、バックアップ電源の供給がない状態から主電源が投入された場合はイニシャル■シーケンスとして所定期間RAS /CASを非アクティブにしなければならない場合もある。 【0004】 従来は、主電源で動作し通常のアクセス用のRAS /CASシー

Description of the invention] [0001] TECHNICAL FIELD [0001] The present invention is, DRAM self-refresh mode relates to a control device for backing up DRAM [0002] Conventionally, as a method to back up the main power supply DRAM is disconnected or the self-D RAM: the Walsh mode is the most common. However, DRAM a self-refresh mode, the normal, at the time of access to different sequence RAS/CAS sequence is required. Moreover, in the normal, from the sequence of the access to the DRAM self-refresh sequence is required to be less than the various timing conditions must move to. The main power supply is reduced, the sequence would be suddenly interrupted access is not allowed. [0003] In addition, the backup power is supplied from a state that has been switched to the main power supply - self-reflection return from the Ganassi Sequence-net instructions of the supply of power is not haptic abbu main power supply is turned on for a predetermined period of time as in the case of a non-RAS/CAS initial sequence must be activated. [0004] in the past, which run on mains power and RAS/CAS for normal access to output a logic control unit and a first power supply and a self-ganassi abbu work for the RAS/CAS 1842 to output a logic control unit and a second two RAS/CAS logic control unit outputs to the selector Samsung Electronics Co., Ltd.

ケンスを出力する第1のロジック制御部と、バックアップ電源でも動作するセルフリフレッシュ用のRAS/CASシーケンスを出力する第2のロジック制御部とを備え、2つのロジック制御部が出力するRAS/CASをセクタで切り代えてDRAMに与えていた。主電源の電圧の低下を検出すると、CPUのバス制御信号から各バスアクセスサイクルの切れ目を検出し、このタイミングで前記セクタのRAS/CAS出力信号を、前記第1のロジック制御部の出力から、第2のロジック制御部の出力に切り替えると共に、CPUをリセットしていた。主電源の投入時には、CPUのプログラム制御により、前記セクタを、主電源停止時とは逆に、第2のロジック制御部からの出力から、前記第1のロジック制御部の出力に切り替えていた。

【0005】 【発明が解決しようとする課題】 上記従来例では、バックアップ電源で、第2のロジック制御部にも電力を供給 特開平9-34806 する必要がある、電力消費量が多くなる。また、第2のロジック制御部は、バックアップ電源で動作させるため、ゲートアレイなどの集積回路の一部に取り込むことができず、ディスクリート部品で構成せざるをえない。このため部品点数が増え、基板面積が大きくなるという欠点があった。 【00 06】 そこで本発明は、従来必要とした第2のロジック制御部を不要とし、ゲートアレイなどの集積回路に制御回路を取り込むことを可能とすると共に、ソフトウェアによる制御を必要としないDRAM制御装置を提供することを目的とする。 【00 07】

【課題を解決するための手段】 このような目的を達成するために、請求項1に記載のDRAM制御装置は、(1)主電源の電圧が第1の閾値以下の期間、および前記電圧が前記第1の閾値以下の電圧から当該閾値を越えた電圧に変化してから第1の所定の時間が経過するまでの期間に、第1のリセット信号をアクティブにし、他の期間に前記第1のリセット信号を非アクティブにする第1の電圧監視手段と、(2)監視電圧が第2の閾値以下の期間、および前記監視電圧が前記第2の閾値以下の電圧から当該閾値を越えた電圧に変化してから第2の所定の時間が経過するまでの期間に、第2のリセット信号をアクティブにし、他の期間に前記第2のリセット信号を非アクティブにする第2の電圧監視手段と、(3)主電源が投入されている時に充電さ

has been given to the DRAM in the place of. The main power supply when it detects a drop in the voltage of the bus control signal CPU bus access cycle to detect a break from the RAS/CAS at this timing, the output signal of said selector, from the output of the first logic control unit the second control of the output of the logic of the CPU has been reset Cpu of the main power supply is turned on, the control of the selector of the stop from the main power supply, contrary to the time of the logic of the output from the second control unit, the first control section switches the output logic. [0005] The present invention is to provide a above-mentioned in the conventional example, the power supply, the second baffle abbu logic control unit to supply power to, it is necessary to JP-A 9-34806, the greater the power consumption. Further, the second logic control unit, the power supply the abbu operating a part of the integrated circuit such as a gate array, it is impossible to capture a discrete component, configuration c Therefore no choice but the substrate area increases, increasing the number of parts there was a drawback. 06 [00] the present invention, the conventionally required opening control unit of the second, and eliminates the need for the control circuit such as a gate array integrated circuit makes it possible to capture control by, and with reference to the DRAM, the software does not require a control device, and an object thereof is operable to provide [0007] [00 07 means for solving the problems] In order to achieve the above object, to the DRAM control device according to claim 1, wherein (1) mains voltage of first threshold voltage is less than or equal to the first period, and the before-mentioned threshold and less than or equal to a voltage from the voltage change exceeds the threshold value from the first predetermined time has elapsed, the first reset signal is activated, the other periods of the first reset signal to deactivate; and (2) the first voltage monitoring means for monitoring voltage is the second threshold value or less of the period, and the monitoring voltage is the second threshold value or less of the voltage from the voltage exceeds the threshold value, from changes to the second predetermined time has elapsed, the second reset signal is activated, the other periods of the deactivating the second reset signal to the second main power source voltage monitoring means (3) is turned on, is charged during the main power is not turned on, (4) when the standby power supply the main power source is turned is supplied with electric power from the main power

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Ex. 1002, p. 816

れ、前記主電源が投入されていないときに放電する予備電源と、(4)前記主電源が投入されているときに前記主電源から電力が供給され、前記主電源が投入されていないときに前記予備電源から電力が供給されるDRAMと、(5)前記主電源により駆動されるDRAM制御手段であって前記第1のリセット信号がアクティブになると、前記DRAMをバックアップ状態に遷移させるDRAM制御信号を出力し、その後前記監視電圧を前記第2の閾値以下に変化させる手段と前記第1のリセット信号がアクティブでなくなると、前記監視電圧を前記第2の閾値を越える電圧に変化させ、前記DRAMをバックアップ状態から復帰させるDRAM制御信号を出力する手段とを有するDRAM制御手段と、(6)前記主電源により駆動され、前記第2のリセット信号によりリセットされるCPUとを備えたことを特徴とする。【0008】請求項2に記載のDRAM制御装置は、前記DRAM制御手段が、前記第1のリセット信号がアクティブになると、前記CPUが前記DRAMをアクセスしないバス■タイミングで前記DRAMをバックアップ状態に遷移させることを特徴とする。【0009】請求項3に記載のDRAM制御装置は、前記第1の所定の時間が前記第2の所定の時間よりも短いことを特徴とする。【0010】請求項4に記載のDRAM制御装置は、前記第1のリセット信号が前記CPUのバス・ホールド要求入力に入力されていることを特徴とする。【0011】請求項5に記載のDRAM制御装置は、前記予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し前記DRAM制御手段は、前記第1のリセット信号が非アクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ状態から復帰させる復帰制御を行うか、スタンバイ状態から起動させる起動制御を行うかを決定することを特徴とする。

【0012】請求項6に記載のDRAM制御装置は、前記予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し前記DRAM制御手段は、前記第1のリセット信号がアクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ状態とするかスタンバイ状態とするかを決定することを特徴とする。【0013】請求項1に記載のDRAM制御装置において、主電源の電圧が第1の閾値以下の期間、

supply to the main power supply is turned on when it is not the standby power supply, and (5) electric power is supplied from the main power supply, DRAM is driven from the control unit D RAM set the first of the signal becomes active, the A M-up D R D in RAM to transition to the state, and thereafter, the outputs a control signal to the monitored voltage is changed to the second threshold and less than or reset means and the first signal is not active the the monitoring voltage to said second voltage variation exceeding the threshold value of the D-RAM and RAM return from the backup D-outputs a control signal to the control means and a means, (6) DRAM is driven by the main power supply, the second CPU is reset by a reset signal, characterized in that it comprises a [0021] 00 DRAM 08 of claim 2, wherein the control device, the control means, the first DRAM reset signal, wherein the processor is to access the DRAM and the DRAM on a bus that does not back up to transition to the state at the timing it features a. [0021] 00 DRAM 09 of claim 3, wherein the control device, the first predetermined time is shorter than a predetermined time it features a. [0010] DRAM controller as claimed in claim 4, the first reset signal is input, C P U bath. request is input to hold it features a. [0011] D-RAM of claim 5, wherein the control device, before-mentioned standby power supply can supply power power signal indicating whether or not the charge capacity in accordance with an output means for outputting the DRAM control means, said first when the reset signal in response to the power signal, to the state from the DRAM abbu stamper performing a return control for returning from the standby state, whether to perform a start control, characterized in that to determine. [0012] D-RAM of claim 6, wherein the control device, the power can be supplied to the standby power supply, power signal indicating whether or not the charging capacity an output means for outputting in accordance with the control means, the first DRAM of the reset signal becomes active when the Tsu and the power signal, in response to the haptic state DRAM abbu standby state, characterized in that to determine whether [0013] The control device of claim 1, wherein the main RAM smell D the voltage of the power supply period, and the first threshold value or less of the main power source from the voltage of the first voltage less than the threshold value exceeds the threshold value, from changes to the first predetermined time has elapsed, the first reset signal becomes active, the reset signal to the other

および主電源の電圧が第1の閾値以下の電圧から閾値を越えた電圧に変化してから第1の所定の時間が経過するまでの期間に、第1のリセット信号がアクティブになり、他の期間に第1のリセット信号が非アクティブになる。監視電圧が第2の閾値以下の期間、および監視電圧が第2の閾値以下の電圧から閾値を越えた電圧に変化してから第2の所定の時間が経過するまでの期間に、第2のリセット信号がアクティブになり、他の期間に第2のリセット信号が非アクティブになる。【0014】 DRAMには、主電源が投入されているときに主電源から電力が供給され、主電源が投入されていないときに予備電源から電力が供給される。この予備電源は主電源が投入されている時に充電され、主電源が投入されていないときに放電される。DRAM制御手段は主電源により駆動され、第1のリセット信号がアクティブになると、DRAMをバックアップ状態に遷移させるDRAM制御信号を出力し、その後に監視電圧を第2の閾値以下に変化させる。また第1のリセット信号がアクティブでなくなると、監視電圧を第2の閾値を超える電圧に変化させ、DRAMをバックアップ状態から復帰させるDRAM制御信号を出力する。CPUは主電源により駆動され、第2のリセット信号によりリセットされるので、監視電圧が第2の閾値以下の場合に、CPUの動作は強制的に停止される。

【0015】請求項2に記載のDRAM制御装置では、第1のリセット信号がアクティブになると、CPUがDRAMをアクセスしないバスタイミングでDRAMをバックアップ状態に遷移させる。

【0016】請求項3に記載のDRAM制御装置では、第1の所定の時間が第2の所定の時間よりも短Vなので、主電源の電圧が第1の閾値以下の電圧から閾値を越えた特開平9-34806電圧に変化してから第1のリセット信号が非アクティブになる時間の方が、監視電圧が第2の閾値以下の電圧から閾値を越えた電圧に変化してから第2のリセット信号が非アクティブになる時間より短い。【0017】請求項4に記載のDRAM制御装置では、第1のリセット信号がCPUのバス・ホールド要求入力に入力されている。このため、電源の電圧が第1の閾値以下の場合に、CPUにホールド要求が発行される。【0018】請求項5に記載のDRAM制御装置では、予備電源が電力を供給できるか否かを示す電力

periods first becomes inactive. For monitoring voltage is the second threshold value or less of the period, and the second threshold value or less of the monitoring voltage is the voltage from the voltage exceeds the threshold value, from changes to the second predetermined time has elapsed, the second reset signal is activated, the other periods, the second reset signal becomes active. [00] DRAM, the main power supply 14 is turned on from the main power supply and power is supplied to the main power supply is turned on when it is not electric power is supplied from the standby power supply. This preliminary power supply of the main power supply is turned on, the charged during the main power supply is not inserted, when discharged. Dram control means is the main power source is driven by the first reset signal is activated, the backup D-RAM to transition to the state, then the DRAM and outputs a control signal to the monitored voltage is changed to the second threshold value or less. Further, the first reset signal, the second cognitive monitoring voltage exceeding the threshold value of the voltage is changed to a back D RAM abbu recovered from, and outputs a control signal to DRAM Cpu of the main power supply, the second Ri by the drive is reset by a reset signal, the monitoring voltage is equal to or less than the second threshold, the PROCESSOR operation is forcibly stopped. [0015] The control device of claim 2, wherein the RAM, the first D of the reset signal becomes active, D C P U is not access timing in RAM bus back abbu to transition to the state. [0016] RAM of claim 3, wherein the control device D, the first predetermined time is shorter than the second predetermined time, since the main power supply voltage V > is a first threshold value or less of the voltage from the voltage exceeds the threshold value, JP-A 9-34806 from changes to the first reset signal becomes inactive, the monitoring voltage is time to the second threshold voltage below the voltage or exceeds the threshold value, from changes to the second reset signal becomes inactive, shorter than the time. [0017] D-RAM control device of claim 4, wherein, the first reset signal is input to the bath C P U hold request input. For this reason, the voltage of the power supply in the case of less than the first threshold value, and C P U, hold request is issued. [0018] D-RAM of claim 5, wherein the control device, the power can be supplied to the standby power supply indicating whether or not the output in accordance with the power signal to the charge capacity. Dram control means, the first of the set signal becomes inactive, Samsung Electronics Co., Ltd.

信号を充電容量に応じて出力する。DRAM制御手段は、第1のリセット信号が非アクティブとなったときに、電力信号に応じて、DRAMをバックアップ状態から復帰させる復帰制御を行うかスタンバイ状態から起動させる起動制御を行うかを決定する。【0019】請求項6に記載のDRAM制御装置では、予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する。DRAM制御手段は、第1のリセット信号がアクティブとなったときに、電力信号に応じてDRAMをバックアップ状態とするかスタンバイ状態とするかを決定する。【0020】【発明の実施の形態】以下、図面を参照して本発明の実施例を詳細に説明する。

【0021】(実施例1)図1は、本発明を説明するDRAMバックアップ回路のブロック図である。図1においてVccは主電源、VDBはバックアップ電源である。主電源Vccが供給されているときは、バックアップ電源VDBにはFET 6を介してVccから電力が供給される。【0022】図1において、1は第1の電圧監視IC、2は第2の電圧監視ICである。電圧監視ICは、一般的に非常に低い電源電圧での動作が保証されている。更に、本発明で用いる電圧監視ICは、以下の動作特性を持つ。【0023】(1)監視電圧Vrefが、第1の閾値以下から第1の閾値以上に上昇すると、所定時間の遅延後にリセット出力信号をHighレベルにする。【0024】(2)監視電圧Vrefが、第2の閾値以上から、第2の閾値以下に下降すると、リセット出力信号をLowレベルにする。【0025】このような特性を持つICとしては、例えば、富士通製MB3771などがある。RST*はリセット出力信号である。監視電圧入力Vrefの電圧が閾値以下の期間、及び監視電圧入力Vrefの電圧が閾値を越えた後の所定の期間、電圧監視ICはリセット出力信号RST*をLowレベルに保持する。【0026】第1の電圧監視ICは主電源の電圧を監視する。第1の電圧監視ICのリセット出力は、システムのリセットとしては用いず、DRAM制御ロジック回路に対するセルフリフレッシュモードへの移行を要求する信号として用いる。第2の電圧監視ICは、主電源の電圧ではなく、DRAM制御ロジック回路が出力するロジック出力の電圧を監視する。第2の電圧監視ICのリセット出力は、本システムのリセット信号として用いる。第2の電圧監視ICの閾値は、監視対象が

in response to a signal the power of the return from the DRAM abbu return state from the standby state to start the control to be performed to determine whether to perform start-up control. [0019] DRAM of claim 6, wherein the control device, the power can be supplied to the standby power supply signal to the charge and capacitance indicating whether or not the power generation function. Dram control means, the first of the reset signal becomes active when a DRAM power backup in response to the signal state and the standby state or to determine. [20] 00 [the embodiment of the invention] In the following, with reference to the accompanying drawings of the present invention implementation example will be described in detail. [0021] (Example 1) Figure 1, illustrating the present invention, is a block diagram of RAM backup circuit D Figure 1 is the main power source, the VDB to the backup power supply Vcc. When the main power supply Vcc is supplied to the backup power supply V via the FET 6 DB from Vcc power is supplied. [00] the first 22 in FIG. 1, 1, 2 is a second voltage monitoring voltage monitoring IC I C. Voltage monitoring IC is generally very low power supply voltage is guaranteed to operate with a. Further IC used in the present invention, the voltage monitoring of the operation of the following characteristics. [0021] (1) 00 23, the first monitoring voltage Vref is threshold value from the following the first threshold value rises above the predetermined time delay after a reset output signal to high level. [0021] (2) 00 24, the second monitoring voltage Vref is threshold value or more, the second threshold and less than or equal to the reset output signal to the low level. [0021] 0 0 2 5 having such a characteristic, for example, Fujitsu as 1C, there is such as a MB3771 The recess is a output signal. RST* pledget The voltage monitoring voltage input is less than the threshold value Vref monitored voltage input voltage period, and a threshold value Vref can have over a predetermined period of time after the voltage monitoring IC is reset output signal to the low level, and holds the RST* [0 0 6] the first of the voltage monitoring IC is to monitor the voltage of the main power supply. The reset output of the first voltage monitoring reset IC is not used, the system control as DRAM self-refresh mode logic circuitry, used as a signal to request the 1C second voltage monitoring of the main power supply is not a voltage output D R A M control logic circuit monitors the voltage of the output port, 1C of the second set output voltage monitoring of the

ロジック信号なので、低めに設定する。【0027】3は0R論理ゲートでありVDB電源で駆動される。4はN0R論理ゲートでありVDB電源で駆動される。【0028】5はバックアップ電源を供給する予備電源制御部である。予備電源制御部5は充電可能な2次電池を内蔵する。Vccが供給されているときにVccから2次電池へ充電電流が供給される。Vccが供給されていないときは、2次電池からの放電により、VDBにバックアップ電源を出力する。ALRMは2次電池の充電状態を表示するオープンコレクタ出力であり、Lでバックアップが可能であることを示し、Hで充電量が不足していることを現す。【0029】7は本システムを制御するCPUである。CPU7において、HLDREQ*は、CPUに対しタクトバスの解放を要求する入力信号。RST*はCPUのリセット入力信号。CKはCPUの駆動クロック出力。RD*は外部メモリの読みだしタイミングを制御する出力信号。WR*は外部メモリへの書き込みタイミングを制御する出力信号。ASTBは、アドレスとデータを時分割出力するA/Dバスから、アドレス値をラッチするタイミングを与える出力信号。A23~16は、24ビットのアドレス値の内の最上位8ビット出力信号。AD15~0は、アドレス値の下位16ビットと、16ビットデータとを時分割に入出力するシステムデータバスである。【0030】8は、CPU7からアクセスアドレスおよびタイミングを入力し、DRAM10、11のアクセスに必要な信号を出力するDRAM制御部である。DRAM制御部8において、ALRMは、予備電源制御部5が出力するバックアップの可否状態を現す入力信号である。RST0*は第1の電圧監視IC1が出力するリセット信号入力であり、Lで低電圧、Hで正常電圧を示す。RST0*がHの期間中、ALRMをラッチし、値を参照することで、セルフリフレッシュから復帰するかスタンバイするかを判断する。【0031】HRST*は、第2の電圧監視IC2の出力するリセット信号入力であり、Lでシステム■リセット中、Hでシステム動作中を示す。CKは、駆動クロック入力であり、このクロックに同期してDRAM制御信号が作成され出力される。RD*およびWR*は出力信号であり、DRAMの入力信号OE*およびWE*となる。ASTBは、アドレスとデータとが時分割多重して出力されるAD15~0から、アドレス値をラッチするタイミン

system is used as a reset signal. The threshold value of the second voltage monitoring IC logic signal, the monitoring target is set to be lower. [2 7 3 0 0], and VDB0R driven by the power logic gate. 4 is driven by the power, and VDB N0R logic gate. [0028] The standby power supply 5 supplies backup power to the control unit. The standby power supply control unit 5 has a built-in rechargeable secondary battery. Vcc is supplied to the secondary battery when the charging current to the Vcc is supplied. Vcc is supplied to the secondary battery, when it is not, the haptic by the discharge from the head abbu VDB output power. For displaying the state of charge of the secondary battery ALRM to oven-collector output, L is the abbu indicates that the amount of charge is insufficient, it is H. [0029] 7 is a CPU of the present system. Hldreq* CPU7, the bus of the CPU to request the release of evening urabe input signal. The CPU of the reset input signal RST*. The driving clock CK is a CPU. Rd* external memory is to control the timing of the reading of the output signal. Wr* writing to the external memory is output signal to control the timing. The address and the data to time ASTB output bus to latch the value of a / D from the priming signal output to provide an evening shower A23 is a 24-bok to 16 the 8-bit value among the address values of the output signal of the most significant. Yes, the address value AD1 5 to the low 16 bits of the 16-bit data to be input to and output data bus and time division system. [0030] 8 is a CPU7 timing from, and enter DRAM10 access address 11, and outputs a signal required to access the DRAM control unit. The control unit 8, the DRA M ALRM standby power supply control unit 5 is whether the output to the input signal abbu representing the state. I0 * R ST is a first reset voltage monitoring signal C1 is at a low voltage input, L voltage, H normal T0* ALRM RS during the period of the "H" is latched, the, refers to the value of the self-refresh and to whether or standby [1] HRST* 003 second voltage monitoring reset signal input I C2 in order, L H and reset, during system operation. Ck is the driving clock input, and DRAM control in synchronization with the clock signal is generated and output. Wr* RD* is called output signal, the input signal WE* OE* and DRAM. Astb are time-division multiplexed address and data output and a AD15 yes to latch the value to the address input. Thailand priming A 24-bit address A23 to 16 of JP-A 9-34806. at the top-level 8-bit input signal. Ad15 dress to the value Yes, further 16-bit I 6-bit input and output data of

グ入力である。A23～16は、24ビットのアドレス特開平9-34806 の内の最上位8ビットの入力信号。AD15～0は、アドレス値の下位16ビットを出力し、更に16ビットのデータを入出力するシステムデータバスである。【0032】 OFF*は、第2の電圧監視IC2のVref入力端子に接続する論理出力である。この出力を1とすることにより、第2の電圧監視ICは電源電圧が低下したと認識し、本システムのリセット信号reset1を出力する。RAS1*はDRAM1に対するRAS出力信号=RAS0*はDRAM0に対するRAS出力信号。CASH*は、DRAM1、0の16ビットデータの上位8バイトに対するCAS出力信号。CASL*は、DRAM1、0の16ビットデータの下位8バイトに対するCAS出力信号。OE*は、DRAMの読みだし信号。WE*はDRAMに対する書き込み信号。AX10～0は、DRAM1、0のロウアドレスおよびコラムアドレスを時分割多重して出力するDRAMアドレス出力である。【0033】 9は、バックアップ電源VDBで駆動する74HC157相当の2to1セクタである。SELは入力1A～4Aと1B～4Bのどちらを出力するかを選択する制御入力である。SELがLowの場合は1A～4Aが、Highの場合は1B～4Bが選択される。1A～4Aにはバックアップ電源供給部から出力される充電容量表示信号ALARMが入力されている。1B～4BにはDRAM制御ロジックから出力されるRAS/CAS信号が入力されている。ここでSELには2つの電圧監視ICの0R出力が入力されているので、2つの電圧監視ICのリセット出力が共にLowレベルのときのみ、ALARM信号がDRAMに供給される。

【0034】 1Y～4Yはセクタ9により選択された出力信号であり、RAS/CAS信号としてDRAMに供給される。ALARMは主電源でプルアップされ、バックアップ電源が供給可能なときはLowレベルとなり不可能な時はHighレベルとなる。セクタ9はバックアップ電源で駆動されている。【0035】 10および11は、バックアップ電源Vdbで駆動するワード構成のDRAMである。RAS*は、ロウアドレス・ストロブ入力、CASH*は上位バイト側のコラムアドレス・ストロブ入力、CASL*は下位バイト側のコラムアドレス・ストロブ入力である。OE*はデータ読み出しを制御する入力信号。WE*はデータ書き込みを制御する入力信号。AX10～0はアクセス・アドレス入力信号、D15～

the system data bus. [0 0], the second 32-OFF* voltage monitoring, connected to the input terminal of the first C2 Vre logic output. The second output of the voltage monitoring by the IC power supply voltage is lowered, it is recognized that the reset signal Reset1 to the output power of the present system. The output signal with respect to DRAM1+0 on RAS1* RAS is output with respect to the RAS Random-access RAS = Cash* DRAM1 of 16-bit data of the 0 bytes. CAS top 8 output signal. 6, 0, 1 DRAM1 CASL*-bit data of the lower 8 bytes. CAS output signal. Oe* DRAM read signal. We* with respect to the write signal of the DRAM. Ax10 Yes, yes to DRAM1 of the row address and a column address and outputs the DRAM address in time-division multiplexing. [9 0 0] of the backup power supply 33 to drive the 2To1 7 equivalent of the VDB 4HC157 selector. 1A~4A and 1B to 4 SEL input B to select whether to output either a control input. If the SEL is low, in the case of 1A~4A 1B~4B is a high is selected. The backup power supply unit 1A~4A the charge capacity ALARM is output from the display signal input. 1B~4B. RAS/CAS DR output from the AM control logic signal is input. Here, SEL 0 R two voltage monitoring IC output is input one of the voltage monitoring of the output are both low level 1C set only when the ALARM signal is supplied to the DRAM [0034] 1Y4Y selected by the selector 9 to output signal, the signal is supplied to RAS / CAS DRAM Alarm enable the main power source abbu abbu when power can be supplied at the time of the low level to the high level becomes impossible. The backup power supply is driven by the selector 9. [0021] 0 0 3 5 10 and 11 are driven by the backup power source Vdb word organization of DRAM. Ras*, the row address is input, the upper byte side and CASH* strobe of the CASL* RAM address strobe input the lower byte side of the column address strobe input. Oe* - read the input signals that control the evening. We* in the input signal for controlling the data write. Ax10 to the input signal, D15 Yes Yes dress to access the 16-bit data input output. In the above configuration, the gate 4 OR gate 9, R3, N0, 11 is a selector, DRAM10-up is driven by the power source Vdb [0 0] FIG. 2, the backup power supply 36 to supply the main power supply Vcc rises, the Vdb, in the case of a timing chart showing the operation of each part of. At this time, the DRAM refresh mode to the cell, and the process proceeds to the normal access mode In the initial state, the low level S E L signal selector 9 selects and outputs to the 1A~4a 1Y4Y of the input signal is output to the low level ALRM

○は、16ビットのデータ入出力である。以上の構成において、ORゲート3、N0 Rゲート4、セクタ9、DRAM10、11は、バックアップ電源Vdbで駆動される。【0036】図2は、バックアップ電源Vdbを供給中に主電源Vccが立ち上がった場合の、各部の動作を示したタイミングチャートである。このとき、DRAMはセルフリフレッシュモードから、通常アクセスモードに移行する。初期状態ではセクタ9のSEL信号はLowレベルなので、選択出力1Y~4Yには1A~4Aとして入力するLowレベルのALRM信号が出力される。すなわち、DRAM10、11に対するRAS、CAS信号のレベルは、Lowに保持される。【0037】時刻(2a)で、主電源Vccが上昇して第1の電圧監視IC1の閾値を越える。上昇途中は通常の論理回路の動作が保証されない。保証されない出力値を図2では「X」と表記する。DRAM制御部8のRAS1/○およびCASH/L*は、論理動作が可能な電源電圧になるとALRM信号と同一のレベルを出力する。ここではLowレベルを出力する。【0038】時刻(2a)からTd1時間経過した時刻(2b)で、reset 0信号がHighに変化する。これによりセクタ9は、予備電源制御部5から出力されるALRM信号から、DRAM制御部8から出力されるRAS1/0*、CASH/L*信号に出力を切り代える。両信号ともにLowレベルなので、DRAMはセルフリフレッシュモードを継続する。【0039】信号OFF*もLowレベルからHighレベルに変化し、第2の電圧監視IC2は遅延時間Td2の計測を開始する。OFF*信号は論理回路から生成されるので、Vccの立ち上がりでは不定状態になる。しかしながらTd1《Td2とすることで、不定状態の期間にOFF*の出力電圧レベルが第2の電圧監視ICの閾値を越えても、reset1はLowレベルを安定して保持することができる。NORゲート4の出力がLになるとPチャネルFET6は低インピーダンス状態となり、Vdb電源ラインには主電源Vccから電力が供給される。【0040】時刻(2b)からTd2時間遅れた時刻(2c)で、第2の電圧監視IC2のリセット出力reset1がLからHに変化する。この信号はCPUのリセット入出力に接続されているので、この時点からCPUが動作を開始する。reset1はDRAM制御部8にも入力されている。reset1がHighへ変化することにより、セルフリフレッシュモードからの復帰シーケ

Dram10, RAS, CAS, 11 with respect to the signal of the low level is maintained. [003] at the time the main power supply 7 (2) Vcc voltage monitoring IC1 rises, exceeding the threshold of the first. The middle rise is a normal operation of the logic circuit is not guaranteed. The output value is not guaranteed, in FIG. 2, "X" and the notation. The Cash/L* DRAM control unit 8 Yes and RAS1 and the logic operations ALRM power supply voltage signal of the same level and outputs. Here, Lo, and outputs the w level [0021] In the time T 0 0 3 8 2 d 1 (2b) from a) time period elapsed time, select the reset signal 0 is changed to High. This ensures the standby power supply control unit 5 selector 9, from the signal output from the control unit 8 ALRM DRAM that is output from the turn off the RAS1/0*, replaced by a Cash/L* signal Both Lo level signal both w, DRAM is self-refresh mode, to continue the: [0039] signal from the low level to the high level, also change OFF* and the second voltage monitoring IC a total of 2 d 2 the distance delay time T starts Off* signal because it is generated from the logic circuit at the rising edge of the Vcc is indeterminate state. "However we come, Td1 Td2 period, FF* indefinite state Yes the output voltage level of the second voltage monitoring IC reset1 exceeds the threshold value of the low level, to stably hold the, is not practical. The output of the NOR gate 4 and the P-ET6. LF becomes a low impedance state, the power supply line Vcc to the Vdb is the main power supply power is supplied. [0021] In the time T 0 0 4 0 2 2 d 2 from step b); c) time delay time, the second voltage monitoring reset output of L IC 2 changes to the H from reset1. This signal is input to the CPU reset Bok, from this point in time because it is connected to the CPU is to start the operation. Low reset1 control unit 8 is also input to the D-RAM. Reset1 is high, the cell refresh mode to be changed to the return sequence from the start. [1] The CPU 004 DRAM control unit 8 in synchronization with the clock, the time (2d) to the low level to the high level, RAS1/0* to change it This signal, via the selector 9, 11 is transmitted to the DRAM10 The DRAM control unit 8 2d, then, this time, to change to the low level to high Cash/L* This signal is also the selector 9, 11 via is transmitted to the DRAM10 As a result, the self-refresh mode M10, 11 ■ ■ DRA from returns to a normal, it is possible to access. [0042] FIG. 3 is the supply of the backup power supply is stopped when the Vdb with main power supply Vcc rises, in the case of a timing chart showing the operation of each unit The standby power supply control unit 5

ンスを開始する。【0041】 DRAM制御部8は、CPUのクロックに同期して時刻(2d)で、RAS1/0*をLowレベルからHighレベルに変化させる。この信号は、セクタ9を経由してDRAM10、11に伝わる。DRAM制御部8は、2dに続いて、今度はCASH/L*をLowレベルからHighに変化させる。この信号も、セクタ9を経由して、DRAM10、11に伝わる。これにより、DRAM10、11はセルフリフレッシュモードから復帰し、通常のアクセスが可能になる。【0042】図3は、バックアップ電源Vdbの供給が停止している時に主電源Vccが立ち上がった場合の、各部の動作を示すタイミングチャートである。予備電源制御部5が出力するオープンコレクタタイアのALRM信号は、主電源Vccが投入されると、プルアップ抵抗12に特開平9-34806よりHighとなる(3a)。この結果、NORゲート4の出力はLowレベルとなるため、Pch-FET6は低インピーダンス状態となり、VdbにはVccから電源が供給される。また、DRAM制御部8はALRM入力のHighをラッチし、これに従って、RAS/O及びCASH/L*出力をHとする。【0043】時刻(3a)からTd1時間経過した時刻(3b)で、第1の電圧監視IC1のリセット出力reset0がHighに変化する。この変化に対応して、DRAM制御部8はOFF*出力をHにする。これにより、第2の電圧監視IC2は、遅延時間Td2の計時を開始する。ORゲート3の出力SELもHighに変化するので、セクタ9の出力1Y~4Yは、ALRM信号から、DRAM制御部8からのRAS CAS信号に切り替わる。但し両者ともHighなので、出力信号は変化しない。

【0044】時刻(3b)からTd2時間経過した時刻(3c)で、第2の電圧監視IC2のリセット出力reset1がHighに変化する。これによりCPUはリセット状態が解除されて処理を開始する。【0045】時刻(3d)、(3e)では、CPUの駆動クロックCKに同期して、RASおよびCASを制御する。時刻(3a)でラッチしたALRM入力がスタンバイからの起動を示すHighなので、RAS1X0*およびCASH/L*はHighを保持する。これ以降、DRAM制御部8はCPU7のアクセスに応じて、DRAM10、11をアクセスする為のDRAM制御信号を出力する。【0046】図4は、主電源Vccが遮断され、バックアップ電源VDBによりDRAMがバックアップされる場合の動作を現すタイミングチャートである。この場合、

is output to the oven, and the ALRM collector of the signal, the main power supply Vcc is turned on, the resistance 12 in JP-A 9-34806 preamble abdu from high to (3a). As a result, the output of the NOR gate becomes low level 4, Pch-FET6, since the low-impedance state, the Vdb, power is supplied from Vcc. In addition, DRAM is input to a control unit 8 and the high ALRM, accordingly, the output of the Rasi/o and H and Cash/l* [0 0 4 3 3 d1] at time time period elapsed time T (3b) from a), the first voltage monitoring IC1 is High, the reset output of 0 is changed to the reset In response to this change is output to the DRAM control unit 8 H, OFF*. As a result, the second voltage monitoring IC2 is, to start the counting of the delay time T d 2. The output of the SEL 0 R gate 3 is also high, because the change in the output of the selector 9 to the DRA1Y4Y from the signal control unit 8 from the ALRM M is changed RAS CAS However, since both high output signal does not change. [0 0 3 2 44] at the time td time period elapsed time from step b) (3 c), the second voltage monitoring reset output of the t1 is I C 2 is changed to the high reset Thus CPU is in the reset state is released, to start the process. [0 0 4 5 - 3 - 3, d), e)] at time C P U in synchronization with the drive clock CK to control the RAS and CAS. (3a) input is latched by the standby time or ALRM indicating the activation of the high high and holds the L * RAS1X0* CASH/ Thereafter, the DRAM access control unit 8, in accordance with the C-DRAM10 PU7 access of DRAM, 11 and outputs a control signal in order [0] FIG. 4 is VCC of the main power supply 046 is cut off, the backup power supply is backed up, the VDB operation in a case where the DRAM is a timing chart representing the In this case, the main power supply Vcc to detect a decrease in the self-Ganassi: DRAM reflection mode migrated to. [0047] (4a), the first time the main power supply voltage monitoring IC1 is Vcc 0 detects the voltage drop, a low level signal reset. The low level signal is input to the DRAM control unit 8, the standby power supply control unit 5 from the power supply baffle ALRM-up signal is Low level, indicating a possible DR control unit 8, and AM CPU7 bus access that you monitor the sequence of the self-refresh mode can be migrated to the priming and to detect the caught in an evening shower This transition is carried out with respect to a timing detection signal, THE AMOUNT OF DRAM RAS, CAS capable short-destroy its data unauthorized in degrees and outputs the Mau \ stealth. [0 0 8 4 7 C P U] at time b, and bus cycle to access the DRAM and not from Thailand Mi, the self-refresh Samsung Electronics Co., Ltd.

主電源Vccの低下を検出し、DRAMをセルフリフレッシュ■モードに移行させる。【0047】時刻(4a)で、第1の電圧監視IC1は主電源Vccの電圧低下を検出し、信号reset 0をLowレベルにする。このLowレベル信号がDRAM制御部8に入力されると、予備電源制御部5からのALRM信号がバックアップ電源の供給可能を示すLowレベルなので、DRAM制御部8はCPU7のバスアクセスシーケンスを監視して、セルフリフレッシュ■モードに移行できるタイミングを検出する。この移行タイミング検出を行わないと、DRAMに対するRAS、CAS信号にDRAMの記憶データを破壊してしまう不正な短ノ、degrees ルスを出力してしまう可能性がある。【0048】時刻(4b)でCPU7のバス■アクセス■サイクルの中から、DRAMをアクセスしないタイミングを検出すると、セルフリフレッシュ■モードへの移行シーケンスを開始する。これ以後にCPU7がDRAMアクセスのバスサイクルを実行しても、無視する。DRAM制御部8は、このタイミングで、まず、CASH/L*の出力をLowレベルに固定する。【0049】時刻(4c)では、0尺八皿制御部8は1 S1/0*をLowレベルに固定する。これによりDRAMはセルフリフレッシュモードとなる。時刻(4d)では、DRAM制御部8は、第2の電圧監視IC2の監視対象であるVref入力となるOFF*出力をLowレベルとする。この結果時刻(4e)で、第2の電圧監視IC2のリセット出力reset1がLowレベルに変化する。この変化により、セクタ9の出力はDRAM制御部8からの入力から、予備電源制御部5からのALRM信号に切り替わる。但しいずれもLowレベルなので、DRAMはセルフリフレッシュ■モードを維持する。また、CPU7、DRAM制御部8のリセットとして作用する。【0050】図5は、主電源Vccが遮断されバックアップ電源Vdbも供給されない場合の、DRAM制御回路の動作を現すタイミングチャートである。この場合、主電源Vccの低下を検出しても、DRAMをセルフリフレッシュ■モードへ移行させない。時刻(5a)で、第1の電圧監視IC1は主電源Vccの電圧低下を検出し、信号reset 0をLowレベルにする。このLレベル信号がDRAM制御部8に入力されるが、予備電源制御部5からのALRM信号がバックアップ電源の供給不可能を示すHighにあることから、DRAM制御部8は、セルフリフレッシュ■モード

mode detects unhandled for the move to start the sequence line 7 is D C P U R A in this since M access be performed every series of the bus cycles, ignore. D R A M control unit 8 at this timing, first, the output to the low level, to fix the Cash/L* [0] at the time (4c) 049 0 tray 1 shakuhachi control unit 8 to the low level, to fix the s1/0* As a result, it D R A M is self-refresh mode. Time in DRAM control unit 8 (4d), the second voltage monitoring 2 monitors. I C becomes the input to the low level Vref output and an OFF* As a result, the second time (4 e) 2 voltage monitoring reset1 I C the reset output of the changes to the low level. By a change in the output of the selector 9 control unit 8 from the input of the DRAM to the standby power supply control unit 5 is changed from the ALRM However, DRAM is both low level, to maintain the self-refresh mode. Further, the control unit 8 CP of the reset U7, acts as DRAM [00] in FIG. 5, the main power supply 50 is cut off the power supply Vcc is also supplied to the back abbu DLAM Vdb, in the case of not the operation of the control circuit is a timing chart representing In this case, the main power supply Vcc by detecting a decrease in the reflection mode for the DRAM in self-and to not be migrated. (5 a), the first time C1 of the main power supply voltage monitoring I Vcc 0 detects the voltage drop, a low level signal reset. The L-level signal is input to the control unit 8 D R A M, the standby power supply control unit 5 from the power supply signal is abbu ALRM back, since it is possible high DRAM control unit 8 and the self-mode reflection and do not migrate to the Ganassi: [0021] At the time (5 0 0 51 b) backup. Power Supply Vdb is because it is not the time is different from the L * (4b) is fixed to the CASH/ High The power supply time of the Vdb Abbu (5c) is not supplied, the time (4c), unlike the fixed to the RAS1/0* to High. Time (4c) (5d), the time change in the same manner as in OFF* is to output to the low level, the second reset signal from the voltage monitoring IC to output. Time (3d), the second voltage monitoring reset1 I C2 output is low of the recess pldget change in level. This ensures the selector 9 control unit 8 the output of the DRAM input from the standby power supply control unit 5 is changed from the ALRM However, since the standby mode is also high to continue the DRAM is: [52] [00] in Example 1, another embodiment of the main power supply 0 voltage is lowered becomes low level, the reset in FIG. 4 or, as shown in FIG. 5, in a period running power-off sequence from the CPU to ignore the access to the DRAM For this reason, read CPU incorrect

ドには移行しない。【0051】時刻(5b)でバックアップ。電源Vdbが供給されていないので、時刻(4b)とは異なり、CASH/L*をHighに固定する。時刻(5c)ではバックアップ電源Vdbが供給されない、時刻(4c)とは異なり、RAS1/0*をHighに固定する。時刻(5d)では、時刻(4c)と同様にOFF*出力をLowレベルに変化させ、第2の電圧監視ICからリセット信号を出力させる。時刻(3d)により、第2の電圧監視IC2のリセット出力reset1がLowレベルに変化する。これにより、セクタ9の出力はDRAM制御部8からの入力から、予備電源制御部5からのALRM信号に切り替わる。但しいずれもHighなので、DRAMはスタンバイモードを継続する。【0052】〔他の実施例〕実施例1では、主電源の電圧が低下しreset0がLowレベルとなって、図4又は図5に示したパワーオフシーケンスを実行している期間に、CPUからDRAMへのアクセスを無視する。このためCPUは誤ったデータを読み取る。この結果、CPUは正常な動作を行えない。特にDRAMのアクセスがスタックからのポップ動作だった場合には暴走する。reset1がLowレベルになるとCPU7はリセット状態となるので暴走は停止するが、この間に他のメモリーの内容が書き換えられる危険がある。【0053】この危険を回避するため、第1の電圧監視ICのリセット出力をCPUに対するバスホールド要求信号として与える。これによりDRAMのセルフリフレッシュモードへの移行とほぼ同時にCPUが停止するので、アクセス不能となったDRAMから不定なデータを開平9-34806タを読み込んで誤った動作を行うことを防止することができる。なお、第1および第2の電圧監視ICは必ずしもICである必要はなく、ディスクリート部品で構成することもできる。【0054】以上の説明から明らかなように、主電源の供給が停止されると第1の電圧監視ICが主電源の電圧の低下を検出し、DRAM制御ロジックにセルフリフレッシュモードへの移行を要求する。DRAM制御ロジックは、CPUのバスアクセスサイクルの中からDRAMをアクセスしていないタイミングを検出し、RASCASをセルフリフレッシュモードとなるシーケンスで出力する。

【0055】次にDRAM制御ロジックは、第2の電圧監視ICからリセット信号を出力させるべく、第2の電圧監視ICのVref入力に接続されるデジタ

data As a result, CPU, can not be performed a normal operation. In particular, DRAM access operation from the stack in the case was a runaway potting. Reset CPU t1 is Low level, the reset state 7 is stopped, since the runaway shape during this time, other memory is rewritten, there is a risk of [53] The 00 in order to avoid the risk, the first voltage monitoring IC reset output request with respect to the bath. give as a signal hold. Thus, the legs and DRAM self-mode is to almost at the same time, CPU becomes inaccessible, JP-A 9-34806 from DRAM Day evening indefinite reads performs an operation mistake it is possible to prevent. It should be noted that the first and second voltage monitoring IC IC is always need not be a discrete component, it is also possible to horizontal form [0054] As is apparent from the above description, the main power supply is stopped, the supply of the main power supply and the first voltage monitoring IC detects the decrease of the voltage of self-reflection and control logic in the DRAM to request a transition to the mode. The DRAM access control logic on the PROCESSOR bus cycle to the DRAM no access to the RASCAS and detects the timing at which a self-refresh sequence. The Mode Output [0055] next second DRAM control logic is to output a reset signal from the voltage monitoring IC; i, C second conductive pressure monitoring Vref is connected to the input, to change the digital output signal to the low level, As a result, the second voltage monitoring IC outputs a reset signal, the system reset-like passive state. Two voltage monitoring of the reset since IC output is low, the selector ALRM and it outputs the signal. The discharge in accordance with the backup power supply if possible, the output power is low RAS/CAS to maintain the level. [56] The main power supply 00 is turned on, the control logic DRAM a RAS/CAS ALRM signal and the same level of the signal and outputs it as. First, the main power supply voltage monitoring to detect IC, reset output to High level, and, the selector signal from the output DRALRM AM subject is an output signal to be changed to the RAS/CAS Further, the DRAM control logic voltage monitoring with respect to the second digital output signal Vref IC to the high level. As a result, after a predetermined period of time through a second voltage monitoring reset output of 1C is released from the reset state, the system is brought into an operating state. [00] the reset output of the control logic 57 is also input to the DRAM self-refresh sequence, return from the start trigger of the sheet. Alrm return signal is

ル出力信号をLowレベルに変化させる。この結果、第2の電圧監視ICはリセット信号を出力し、本システムはリセット状態となる。2つの電圧監視ICのリセット出力がLowとなるので、セレクトはALRM信号を出力する。したがって、バックアップ電源が放電可能ならば、RAS/CAS出力はLowレベルを維持する。【0056】主電源が投入されると、DRAM制御ロジックはALRM信号と同一のレベルをRAS/CAS信号として出力する。第1の電圧監視ICが、主電源起動を検出し、リセット出力をHighレベルとすると、セレクトの出力対象が、ALRM信号からDRAM制御ロジックの出力するRAS/CAS信号に変化する。また、DRAM制御ロジックは、第2の電圧監視ICのVrefに対するデジタル出力信号をHighレベルとする。この結果、所定の時間経過後に、第2の電圧監視ICのリセット出力は解除され、本システムはリセット状態から動作状態になる。【0057】リセット出力は、DRAM制御ロジックにも入力され、セルフリフレッシュモードからの復帰シーケンスの起動トリガとなる。ALRM信号がLowレベルであれば、復帰シーケンスに従ってRAS/CASが制御される。ALRM信号がHighレベルの場合、即ちDRAMがバックアップされていない場合は、RAS/CAS共にHighレベルを出力する。これによりDRAMが要求するイニシャルモードが満たされる。【0058】【発明の効果】以上述べたように、本発明によれば、DRAMバックアップの為のタイミング制御を、主電源の電圧で動作する論理回路で行うので、ほとんどの回路を集積化できる。また、セルフリフレッシュモードへの移行、通常モードへの復帰ともに、論理回路だけで実行するので、ソフトウェアの負担がなくなる。さらに、主電源低下時、システムのリセットを行う前に、DRAMだけをアクセス不能としてしまうと、リセットまでの間にCPUが暴走して、SRAMなど他の保存すべきデータを破壊してしまう可能性があるが、本発明では、第1の電圧監視ICの出力するリセット出力を、CPUに対するバスホールド要求とすることにより、CPUの暴走を防ぐことができる。

【図面の簡単な説明】 【図1】本発明の実施例としてのDRAMバックアップ回路のブロック図である。【図2】バックアップ電源VDBの供給中に主電源Vccが立ち上がった場合の動作タイミングを

low, if the level of RAS/CAS is controlled in accordance with the sequence. Alrm signal is High level, that is, when the DRAM is, if it is not the RAS/CAS, and outputs the both high Bae Le As a result, requests for DRAM of a mode is satisfied. [0058] [Effect of the Invention] As described above, according to the present invention, timing control, D RAM backup to the main power supply for a logic circuit operating at a voltage of most of the circuit can be integrated, since the to. In addition, for the transition to the self-refresh mode of returning to the normal mode, the logic circuit, since both the burden on the software. Only is eliminated. Further, the main power supply drop time, the system only before resetting, DRAM as inaccessible until the reset CPU is runaway, such as base-out data from the SRAM to store, there is a possibility that destroy the, the present invention, the first to the output of the voltage monitoring reset output to the PROCESSOR 1C, by the bus hold request, it is possible to prevent the runaway of the CPU Brief Description of the Drawings FIG. 1 as an embodiment of the present invention is a block diagram of a DRAM of the backup circuit. Fig. 2 is a backup power supply of the main power supply Vcc during the supply of the VDB rises, timing chart showing the operation timing of when. Fig. 3 is a backup power supply during the interruption of the power supply Vcc is VDB, the main, the timing indicated by the operation in the case of rises Taingu is a Furochi chart. [Figure 4] after the cut-off of the main power supply Vcc is supplied, the backup power source VDB timing chart showing the operation timing - Bok. Fig. 5 is a main power supply after the interruption of the backup power supply Vcc is not supplied, the VDB is a timing chart showing the operation timing of the.

示すタイミングチャートである。【図3】バックアップ電源VDBの遮断中に、主電源Vccが立ち上がった場合の動作タイミングを示すタイミングチャートである。【図4】主電源Vccの遮断後、バックアップ電源VDBが供給される場合の動作タイミングを示すタイミングチャートである。【図5】主電源Vccの遮断後、バックアップ電源VDBも供給されない場合の動作タイミングを示すタイミングチャートである。

Cited by: JP11353243 A2; JP2000048559 A2; JP2000207292 A2; JP2002251316 A2; JP2005148827 A2; JP2006350859 A2; JP3727177 B2; JP4026585 B2; JP4136076 B2; JP4136150 B2; JP4817510 B2

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(71) 出願人 000001007

キヤノン株式会社

東京都大田区下丸子3丁目30番2号

(72) 発明者 石川 祐司

東京都大田区下丸子3丁目30番2号 キヤ
ノン株式会社内

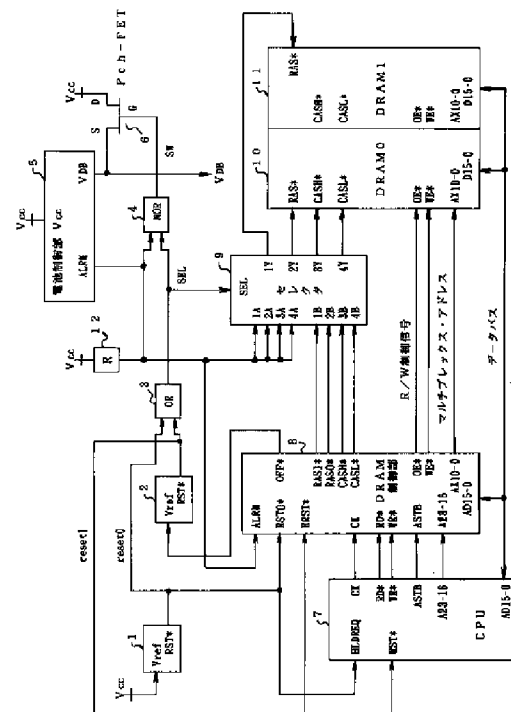
(74) 代理人 弁理士 谷 義一 (外1名)

(54) 【発明の名称】 DRAM制御装置

(57) 【要約】

【課題】 制御回路を集積化できるDRAM制御装置を提供すること。

【解決手段】 第1のリセット信号は、主電源の電圧が第1の閾値以下、または閾値を越えてから所定の時間が経過するまでアクティブになる。第2のリセット信号は監視電圧が第2の閾値以下、または閾値を越えてから所定の時間が経過するまでアクティブになる。DRAMには、主電源または予備電源から電力が供給される。予備電源は主電源により充電される。DRAM制御手段は主電源により駆動され、第1のリセット信号がアクティブになると、DRAMをバックアップ状態に移せ、その後監視電圧出力を第2の閾値以下に変化させる。第1のリセット信号がアクティブでなくなると監視電圧出力を第2の閾値を越える電圧にし、DRAMをバックアップ状態から復帰させる。CPUは主電源により駆動され、第2のリセット信号によりリセットされる。



【特許請求の範囲】

【請求項 1】 (1) 主電源の電圧が第 1 の閾値以下の期間、および前記電圧が前記第 1 の閾値以下の電圧から当該閾値を越えた電圧に変化してから第 1 の所定の時間が経過するまでの期間に、第 1 のリセット信号をアクティブにし、他の期間に前記第 1 のリセット信号を非アクティブにする第 1 の電圧監視手段と、(2) 監視電圧が第 2 の閾値以下の期間、および前記監視電圧が前記第 2 の閾値以下の電圧から当該閾値を越えた電圧に変化してから第 2 の所定の時間が経過するまでの期間に、第 2 のリセット信号をアクティブにし、他の期間に前記第 2 のリセット信号を非アクティブにする第 2 の電圧監視手段と、(3) 主電源が投入されている時に充電され、前記主電源が投入されていないときに放電する予備電源と、(4) 前記主電源が投入されているときに前記主電源から電力が供給され、前記主電源が投入されていないときに前記予備電源から電力が供給される DRAM と、(5) 前記主電源により駆動される DRAM 制御手段であって、前記第 1 のリセット信号がアクティブになると、前記 DRAM をバックアップ状態に遷移させる DRAM 制御信号を出力し、その後に前記監視電圧を前記第 2 の閾値以下に変化させる手段と、前記第 1 のリセット信号がアクティブでなくなると、前記監視電圧を前記第 2 の閾値を越える電圧に変化させ、前記 DRAM をバックアップ状態から復帰させる DRAM 制御信号を出力する手段とを有する DRAM 制御手段と、(6) 前記主電源により駆動され、前記第 2 のリセット信号によりリセットされる CPU とを備えたことを特徴とする DRAM 制御装置。

【請求項 2】 前記 DRAM 制御手段は、前記第 1 のリセット信号がアクティブになると、前記 CPU が前記 DRAM をアクセスしないバス・タイミングで前記 DRAM をバックアップ状態に遷移させることを特徴とする請求項 1 に記載の DRAM 制御装置。

【請求項 3】 前記第 1 の所定の時間が前記第 2 の所定の時間よりも短いことを特徴とする請求項 1 又は 2 に記載の DRAM 制御装置。

【請求項 4】 前記第 1 のリセット信号が、前記 CPU のバス・ホールド要求入力に入力されていることを特徴とする請求項 1 から 3 のいずれかに記載の DRAM 制御装置。

【請求項 5】 前記予備電源は、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し、前記 DRAM 制御手段は、前記第 1 のリセット信号が非アクティブとなったときに、前記電力信号に応じて、前記 DRAM をバックアップ状態から復帰させる復帰制御を行うか、スタンバイ状態から起動させる起動制御を行うかを決定することを特徴とする請求項 1 から 4 のい

れかに記載の DRAM 制御装置。

【請求項 6】 前記予備電源は、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し、

前記 DRAM 制御手段は、前記第 1 のリセット信号がアクティブとなったときに、前記電力信号に応じて、前記 DRAM をバックアップ状態とするかスタンバイ状態とするかを決定することを特徴とする請求項 1 から 5 のいずれかに記載の DRAM 制御装置。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、DRAM のセルフリフレッシュモードを使ってバックアップする DRAM 制御装置に関する。

【0002】

【従来の技術】従来、DRAM をバックアップする手法としては、主電源が切断された時 DRAM をセルフリフレッシュ・モードにするのが、もっとも一般的である。しかしながら、DRAM をセルフリフレッシュ・モードにするには、通常のアクセス時の RAS /CAS シーケンスとは異なるシーケンスが要求される。しかも、通常のアクセスのシーケンスからセルフリフレッシュ・シーケンスへは、DRAM が要求する各種タイミング条件を満たすように移行しなければならない。主電源が低下したときに、アクセスのシーケンスを突然中断してしまうことは許されない。

【0003】更に、バックアップ電源が供給されていた状態から主電源に切り替わった場合はセルフリフレッシュ・モードからの復帰シーケンスを実行し、バックアップ電源の供給がない状態から主電源が投入された場合はイニシャル・シーケンスとして所定期間 RAS /CAS を非アクティブにしなければならない場合もある。

【0004】従来は、主電源で動作し通常のアクセス用の RAS /CAS シーケンスを出力する第 1 のロジック制御部と、バックアップ電源でも動作するセルフリフレッシュ用の RAS /CAS シーケンスを出力する第 2 のロジック制御部とを備え、2 つのロジック制御部が出力する RAS /CAS をセレクトで切り代えて DRAM に与えていた。主電源の電圧の低下を検出すると、CPU のバス制御信号から各バスアクセスサイクルの切れ目を検出し、このタイミングで前記セレクトの RAS /CAS 出力信号を、前記第 1 のロジック制御部の出力から、第 2 のロジック制御部の出力に切り替えると共に、CPU をリセットしていた。主電源の投入時には、CPU のプログラム制御により、前記セレクトを、主電源停止時とは逆に、第 2 のロジック制御部からの出力から、前記第 1 のロジック制御部の出力に切り替えていた。

【0005】

【発明が解決しようとする課題】上記従来例では、バックアップ電源で、第 2 のロジック制御部にも電力を供給

する必要があり、電力消費量が多くなる。また、第2のロジック制御部は、バックアップ電源で動作させるため、ゲートアレイなどの集積回路の一部に取り込むことができず、ディスクリート部品で構成せざるをえない。このため部品点数が増え、基板面積が大きくなるという欠点があった。

【0006】そこで本発明は、従来必要とした第2のロジック制御部を不要とし、ゲートアレイなどの集積回路に制御回路を取り込むことを可能とすると共に、ソフトウェアによる制御を必要としないDRAM制御装置を提供することを目的とする。

【0007】

【課題を解決するための手段】このような目的を達成するために、請求項1に記載のDRAM制御装置は、

(1) 主電源の電圧が第1の閾値以下の期間、および前記電圧が前記第1の閾値以下の電圧から当該閾値を越えた電圧に変化してから第1の所定の時間が経過するまでの期間に、第1のリセット信号をアクティブにし、他の期間に前記第1のリセット信号を非アクティブにする第1の電圧監視手段と、(2) 監視電圧が第2の閾値以下の期間、および前記監視電圧が前記第2の閾値以下の電圧から当該閾値を越えた電圧に変化してから第2の所定の時間が経過するまでの期間に、第2のリセット信号をアクティブにし、他の期間に前記第2のリセット信号を非アクティブにする第2の電圧監視手段と、(3) 主電源が投入されている時に充電され、前記主電源が投入されていないときに放電する予備電源と、(4) 前記主電源が投入されているときに前記主電源から電力が供給され、前記主電源が投入されていないときに前記予備電源から電力が供給されるDRAMと、(5) 前記主電源により駆動されるDRAM制御手段であって前記第1のリセット信号がアクティブになると、前記DRAMをバックアップ状態に移移させるDRAM制御信号を出力し、その後前記監視電圧を前記第2の閾値以下に変化させる手段と前記第1のリセット信号がアクティブでなくなると、前記監視電圧を前記第2の閾値を越える電圧に変化させ、前記DRAMをバックアップ状態から復帰させるDRAM制御信号を出力する手段とを有するDRAM制御手段と、(6) 前記主電源により駆動され、前記第2のリセット信号によりリセットされるCPUとを備えたことを特徴とする。

【0008】請求項2に記載のDRAM制御装置は、前記DRAM制御手段が、前記第1のリセット信号がアクティブになると、前記CPUが前記DRAMをアクセスしないバス・タイミングで前記DRAMをバックアップ状態に移移させることを特徴とする。

【0009】請求項3に記載のDRAM制御装置は、前記第1の所定の時間が前記第2の所定の時間よりも短いことを特徴とする。

【0010】請求項4に記載のDRAM制御装置は、前

記第1のリセット信号が前記CPUのバス・ホールド要求入力に入力されていることを特徴とする。

【0011】請求項5に記載のDRAM制御装置は、前記予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し前記DRAM制御手段は、前記第1のリセット信号が非アクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ状態から復帰させる復帰制御を行うか、スタンバイ状態から起動させる起動制御を行うかを決定することを特徴とする。

【0012】請求項6に記載のDRAM制御装置は、前記予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する出力手段を有し前記DRAM制御手段は、前記第1のリセット信号がアクティブとなったときに、前記電力信号に応じて、前記DRAMをバックアップ状態とするかスタンバイ状態とするかを決定することを特徴とする。

【0013】請求項1に記載のDRAM制御装置において、主電源の電圧が第1の閾値以下の期間、および主電源の電圧が第1の閾値以下の電圧から閾値を越えた電圧に変化してから第1の所定の時間が経過するまでの期間に、第1のリセット信号がアクティブになり、他の期間に第1のリセット信号が非アクティブになる。監視電圧が第2の閾値以下の期間、および監視電圧が第2の閾値以下の電圧から閾値を越えた電圧に変化してから第2の所定の時間が経過するまでの期間に、第2のリセット信号がアクティブになり、他の期間に第2のリセット信号が非アクティブになる。

【0014】DRAMには、主電源が投入されているときに主電源から電力が供給され、主電源が投入されていないときに予備電源から電力が供給される。この予備電源は主電源が投入されている時に充電され、主電源が投入されていないときに放電される。DRAM制御手段は主電源により駆動され、第1のリセット信号がアクティブになると、DRAMをバックアップ状態に移移させるDRAM制御信号を出力し、その後監視電圧を第2の閾値以下に変化させる。また第1のリセット信号がアクティブでなくなると、監視電圧を第2の閾値を越える電圧に変化させ、DRAMをバックアップ状態から復帰させるDRAM制御信号を出力する。CPUは主電源により駆動され、第2のリセット信号によりリセットされるので、監視電圧が第2の閾値以下の場合に、CPUの動作は強制的に停止される。

【0015】請求項2に記載のDRAM制御装置では、第1のリセット信号がアクティブになると、CPUがDRAMをアクセスしないバス・タイミングでDRAMをバックアップ状態に移移させる。

【0016】請求項3に記載のDRAM制御装置では、第1の所定の時間が第2の所定の時間よりも短いので、主電源の電圧が第1の閾値以下の電圧から閾値を越えた

電圧に変化してから第1のリセット信号が非アクティブになる時間の方が、監視電圧が第2の閾値以下の電圧から閾値を越えた電圧に変化してから第2のリセット信号が非アクティブになる時間より短い。

【0017】請求項4に記載のDRAM制御装置では、第1のリセット信号がCPUのバス・ホールド要求入力に入力されている。このため、電源の電圧が第1の閾値以下の場合に、CPUにホールド要求が発行される。

【0018】請求項5に記載のDRAM制御装置では、予備電源が電力を供給できるか否かを示す電力信号を充電容量に応じて出力する。DRAM制御手段は、第1のリセット信号が非アクティブとなったときに、電力信号に応じて、DRAMをバックアップ状態から復帰させる復帰制御を行うかスタンバイ状態から起動させる起動制御を行うかを決定する。

【0019】請求項6に記載のDRAM制御装置では、予備電源が、電力を供給できるか否かを示す電力信号を充電容量に応じて出力する。DRAM制御手段は、第1のリセット信号がアクティブとなったときに、電力信号に応じてDRAMをバックアップ状態とするかスタンバイ状態とするかを決定する。

【0020】

【発明の実施の形態】以下、図面を参照して本発明の実施例を詳細に説明する。

【0021】（実施例1）図1は、本発明を説明するDRAMバックアップ回路のブロック図である。図1においてVccは主電源、VDBはバックアップ電源である。主電源Vccが供給されているときは、バックアップ電源VDBにはFET6を介してVccから電力が供給される。

【0022】図1において、1は第1の電圧監視IC、2は第2の電圧監視ICである。電圧監視ICは、一般的に非常に低い電源電圧での動作が保証されている。更に、本発明で用いる電圧監視ICは、以下の動作特性を持つ。

【0023】（1）監視電圧Vrefが、第1の閾値以下から第1の閾値以上に上昇すると、所定時間の遅延後にリセット出力信号をHighレベルにする。

【0024】（2）監視電圧Vrefが、第2の閾値以下から、第2の閾値以上に下降すると、リセット出力信号をLowレベルにする。

【0025】このような特性を持つICとしては、例えば、富士通製MB3771などがある。RST*はリセット出力信号である。監視電圧入力Vrefの電圧が閾値以下の期間、及び監視電圧入力Vrefの電圧が閾値を越えた後の所定の期間、電圧監視ICはリセット出力信号RST*をLowレベルに保持する。

【0026】第1の電圧監視ICは主電源の電圧を監視する。第1の電圧監視ICのリセット出力は、システムのリセットとしては用いず、DRAM制御ロジック回路に対するセルフリフレッシュ・モードへの移行を要求す

る信号として用いる。第2の電圧監視ICは、主電源の電圧ではなく、DRAM制御ロジック回路が出力するロジック出力の電圧を監視する。第2の電圧監視ICのリセット出力は、本システムのリセット信号として用いる。第2の電圧監視ICの閾値は、監視対象がロジック信号なので、低めに設定する。

【0027】3はOR論理ゲートでありVDB電源で駆動される。4はNOR論理ゲートでありVDB電源で駆動される。

【0028】5はバックアップ電源を供給する予備電源制御部である。予備電源制御部5は充電可能な2次電池を内蔵する。Vccが供給されているときにVccから2次電池へ充電電流が供給される。Vccが供給されていないときは、2次電池からの放電により、VDBにバックアップ電源を出力する。ALRMは2次電池の充電状態を表示するオープンコレクタ出力であり、Lでバックアップが可能であることを示し、Hで充電量が不足していることを現す。

【0029】7は本システムを制御するCPUである。CPU7において、HLDREQ*は、CPUに対し外部バスの解放を要求する入力信号。RST*はCPUのリセット入力信号。CKはCPUの駆動クロック出力。RD*は外部メモリの読みだしタイミングを制御する出力信号。WR*は外部メモリへの書き込みタイミングを制御する出力信号。ASTBIは、アドレスとデータを時分割出力するA/Dバスから、アドレス値をラッチするタイミングを与える出力信号。A23~16は、24ビットのアドレス値の内の最上位8ビット出力信号。AD15~0は、アドレス値の下位16ビットと、16ビットデータとを時分割に入出力するシステムデータバスである。

【0030】8は、CPU7からアクセスアドレスおよびタイミングを入力し、DRAM10、11のアクセスに必要な信号を出力するDRAM制御部である。DRAM制御部8において、ALRMは、予備電源制御部5が出力するバックアップの可否状態を現す入力信号である。RST0*は第1の電圧監視IC1が出力するリセット信号入力であり、Lで低電圧、Hで正常電圧を示す。RST0*がHの期間中、ALRMをラッチし、値を参照することで、セルフリフレッシュから復帰するかスタンバイするかを判断する。

【0031】HRST*は、第2の電圧監視IC2の出力するリセット信号入力であり、Lでシステム・リセット中、Hでシステム動作中を示す。CKは、駆動クロック入力であり、このクロックに同期してDRAM制御信号が作成され出力される。RD*およびWR*は出力信号であり、DRAMの入力信号OE*およびWE*となる。ASTBIは、アドレスとデータとが時分割多重して出力されるAD15~0から、アドレス値をラッチするタイミング入力である。A23~16は、24ビットのアドレス

の内の最上位 8 ビットの入力信号。AD 15~0 は、アドレス値の下位 16 ビットを出力し、更に 16 ビットのデータを入出力するシステムデータバスである。

【0032】OFF* は、第 2 の電圧監視 IC 2 の Vref 入力端子に接続する論理出力である。この出力を L とすることにより、第 2 の電圧監視 IC は電源電圧が低下したと認識し、本システムのリセット信号 reset 1 を出力する。RAS 1* は DRAM 1 に対する RAS 出力信号。RAS 0* は DRAM 0 に対する RAS 出力信号。CASH* は、DRAM 1、0 の 16 ビットデータの上位 8 バイトに対する CAS 出力信号。CASL* は、DRAM 1、0 の 16 ビットデータの下位 8 バイトに対する CAS 出力信号。OE* は、DRAM の読みだし信号。WE* は DRAM に対する書き込み信号。AX 10~0 は、DRAM 1、0 のロウアドレスおよびコラムアドレスを時分割多重して出力する DRAM アドレス出力である。

【0033】9 は、バックアップ電源 VDB で駆動する 74HC157 相当の 2 to 1 セレクタである。SEL は入力 1A~4A と 1B~4B のどちらを出力するかを選択する制御入力である。SEL が Low の場合は 1A~4A が、High の場合は 1B~4B が選択される。1A~4A にはバックアップ電源供給部から出力される充電容量表示信号 ALARM が入力されている。1B~4B には DRAM 制御ロジックから出力される RAS /CAS 信号が入力されている。ここで SEL には 2 つの電圧監視 IC の OR 出力が入力されているので、2 つの電圧監視 IC のリセット出力が共に Low レベルのときにのみ、ALARM 信号が DRAM に供給される。

【0034】1Y~4Y はセレクタ 9 により選択された出力信号であり、RAS /CAS 信号として DRAM に供給される。ALARM は主電源でプルアップされ、バックアップ電源が供給可能なときは Low レベルとなり不可能な時は High レベルとなる。セレクタ 9 はバックアップ電源で駆動されている。

【0035】10 および 11 は、バックアップ電源 Vdb で駆動するワード構成の DRAM である。RAS* は、ロウアドレス・ストロブ入力、CASH* は上位バイト側のコラムアドレス・ストロブ入力、CASL* は下位バイト側のコラムアドレス・ストロブ入力である。OE* はデータ読み出しを制御する入力信号。WE* はデータ書き込みを制御する入力信号。AX 10~0 はアクセス・アドレス入力信号、D 15~0 は、16 ビットのデータ入出力である。以上の構成において、OR ゲート 3、NOR ゲート 4、セレクタ 9、DRAM 10、11 は、バックアップ電源 Vdb で駆動される。

【0036】図 2 は、バックアップ電源 Vdb を供給中に主電源 Vcc が立ち上がった場合の、各部の動作を示したタイミングチャートである。このとき、DRAM はセルフ・リフレッシュ・モードから、通常アクセスモードに移行する。初期状態ではセレクタ 9 の SEL 信号は Low

レベルなので、選択出力 1Y~4Y には 1A~4A として入力する Low レベルの ALRM 信号が出力される。すなわち、DRAM 10、11 に対する RAS、CAS 信号のレベルは、Low に保持される。

【0037】時刻 (2a) で、主電源 Vcc が上昇して第 1 の電圧監視 IC 1 の閾値を越える。上昇途中は通常の論理回路の動作が保証されない。保証されない出力値を図 2 では「X」と表記する。DRAM 制御部 8 の RAS 1 /0* および CASH /L* は、論理動作が可能な電源電圧になると ALRM 信号と同一のレベルを出力する。ここでは Low レベルを出力する。

【0038】時刻 (2a) から Td1 時間経過した時刻 (2b) で、reset 0 信号が High に変化する。これによりセレクタ 9 は、予備電源制御部 5 から出力される ALRM 信号から、DRAM 制御部 8 から出力される RAS 1 /0*、CASH /L* 信号に出力を切り代える。両信号ともに Low レベルなので、DRAM はセルフ・リフレッシュ・モードを継続する。

【0039】信号 OFF* も Low レベルから High レベルに変化し、第 2 の電圧監視 IC 2 は遅延時間 Td2 の計測を開始する。OFF* 信号は論理回路から生成されるので、Vcc の立ち上がりでは不定状態になる。しかしながら Td1 < Td2 とすることで、不定状態の期間に OFF* の出力電圧レベルが第 2 の電圧監視 IC の閾値を越えても、reset 1 は Low レベルを安定して保持することができる。NOR ゲート 4 の出力が L になると P チャネル FET 6 は低インピーダンス状態となり、Vdb 電源ラインには主電源 Vcc から電力が供給される。

【0040】時刻 (2b) から Td2 時間遅れた時刻 (2c) で、第 2 の電圧監視 IC 2 のリセット出力 reset 1 が L から H に変化する。この信号は CPU のリセット入力に接続されているので、この時点から CPU が動作を開始する。reset 1 は DRAM 制御部 8 にも入力されている。reset 1 が High へ変化するることにより、セルフリフレッシュモードからの復帰シーケンスを開始する。

【0041】DRAM 制御部 8 は、CPU のクロックに同期して時刻 (2d) で、RAS 1 /0* を Low レベルから High レベルに変化させる。この信号は、セレクタ 9 を経由して DRAM 10、11 に伝わる。DRAM 制御部 8 は、2d に続いて、今度は CASH /L* を Low レベルから High に変化させる。この信号も、セレクタ 9 を経由して、DRAM 10、11 に伝わる。これにより、DRAM 10、11 はセルフ・リフレッシュ・モードから復帰し、通常のアクセスが可能になる。

【0042】図 3 は、バックアップ電源 Vdb の供給が停止している時に主電源 Vcc が立ち上がった場合の、各部の動作を示すタイミングチャートである。予備電源制御部 5 が出力するオープンコレクタ・タイプの ALRM 信号は、主電源 Vcc が投入されると、プルアップ抵抗 12 に

よりHighとなる(3a)。この結果、NORゲート4の出力はLowレベルとなるため、Pch-FET6は低インピーダンス状態となり、VdbにはVccから電源が供給される。また、DRAM制御部8はALRM入力のHighをラッチし、これに従って、RAS1/O*及びCASH/L*出力をHとする。

【0043】時刻(3a)からTd1時間経過した時刻(3b)で、第1の電圧監視IC1のリセット出力reset0がHighに変化する。この変化に対応して、DRAM制御部8はOFF*出力をHにする。これにより、第2の電圧監視IC2は、遅延時間Td2の計時を開始する。ORゲート3の出力SELもHighに変化するので、セクタ9の出力1Y~4Yは、ALRM信号から、DRAM制御部8からのRAS CAS信号に切り替わる。但し両者ともHighなので、出力信号は変化しない。

【0044】時刻(3b)からTd2時間経過した時刻(3c)で、第2の電圧監視IC2のリセット出力reset1がHighに変化する。これによりCPUはリセット状態が解除されて処理を開始する。

【0045】時刻(3d)、(3e)では、CPUの駆動クロックCKに同期して、RASおよびCASを制御する。時刻(3a)でラッチしたALRM入力がスタンバイからの起動を示すHighなので、RAS1/O*およびCASH/L*はHighを保持する。これ以降、DRAM制御部8はCPU7のアクセスに応じて、DRAM10、11をアクセスする為のDRAM制御信号を出力する。

【0046】図4は、主電源Vccが遮断され、バックアップ電源VDBによりDRAMがバックアップされる場合の動作を現すタイミングチャートである。この場合、主電源Vccの低下を検出し、DRAMをセルフリフレッシュ・モードに移行させる。

【0047】時刻(4a)で、第1の電圧監視IC1は主電源Vccの電圧低下を検出し、信号reset0をLowレベルにする。このLowレベル信号がDRAM制御部8に入力されると、予備電源制御部5からのALRM信号がバックアップ電源の供給可能を示すLowレベルなので、DRAM制御部8はCPU7のバスアクセス・シーケンスを監視して、セルフリフレッシュ・モードに移行できるタイミングを検出する。この移行タイミング検出を行わないと、DRAMに対するRAS、CAS信号にDRAMの記憶データを破壊してしまう不正な短パルスを出力してしまう可能性がある。

【0048】時刻(4b)でCPU7のバス・アクセス・サイクルの中から、DRAMをアクセスしないタイミングを検出すると、セルフリフレッシュ・モードへの移行シーケンスを開始する。これ以後にCPU7がDRAMアクセスのバスサイクルを実行しても、無視する。DRAM制御部8は、このタイミングで、まず、CASH/L*の出力をLowレベルに固定する。

【0049】時刻(4c)では、DRAM制御部8はRA

S1/O*をLowレベルに固定する。これによりDRAMはセルフリフレッシュモードとなる。時刻(4d)では、DRAM制御部8は、第2の電圧監視IC2の監視対象であるVref入力となるOFF*出力をLowレベルとする。この結果時刻(4e)で、第2の電圧監視IC2のリセット出力reset1がLowレベルに変化する。この変化により、セクタ9の出力はDRAM制御部8からの入力から、予備電源制御部5からのALRM信号に切り替わる。但しいずれもLowレベルなので、DRAMはセルフリフレッシュ・モードを維持する。また、CPU7、DRAM制御部8のリセットとして作用する。

【0050】図5は、主電源Vccが遮断されバックアップ電源Vdbも供給されない場合の、DRAM制御回路の動作を現すタイミングチャートである。この場合、主電源Vccの低下を検出しても、DRAMをセルフリフレッシュ・モードへ移行させない。時刻(5a)で、第1の電圧監視IC1は主電源Vccの電圧低下を検出し、信号reset0をLowレベルにする。このLowレベル信号がDRAM制御部8に入力されるが、予備電源制御部5からのALRM信号がバックアップ電源の供給不可能を示すHighにあることから、DRAM制御部8は、セルフリフレッシュ・モードには移行しない。

【0051】時刻(5b)でバックアップ電源Vdbが供給されていないので、時刻(4b)とは異なり、CASH/L*をHighに固定する。時刻(5c)ではバックアップ電源Vdbが供給されないで、時刻(4c)とは異なり、RAS1/O*をHighに固定する。時刻(5d)では、時刻(4c)と同様にOFF*出力をLowレベルに変化させ、第2の電圧監視ICからリセット信号を出力させる。時刻(5d)により、第2の電圧監視IC2のリセット出力reset1がLowレベルに変化する。これにより、セクタ9の出力はDRAM制御部8からの入力から、予備電源制御部5からのALRM信号に切り替わる。但しいずれもHighなので、DRAMはスタンバイ・モードを継続する。

【0052】〔他の実施例〕実施例1では、主電源の電圧が低下しreset0がLowレベルとなって、図4又は図5に示したパワーオフシーケンスを実行している期間に、CPUからDRAMへのアクセスを無視する。このためCPUは誤ったデータを読みとる。この結果、CPUは正常な動作を行えない。特にDRAMのアクセスがスタックからのポップ動作だった場合には暴走する。reset1がLowレベルになるとCPU7はリセット状態となるので暴走は停止するが、この間に他のメモリーの内容が書き換えられる危険がある。

【0053】この危険を回避するため、第1の電圧監視ICのリセット出力をCPUに対するバス・ホールド要求信号として与える。これによりDRAMのセルフリフレッシュ・モードへの移行とほぼ同時にCPUが停止するので、アクセス不能となったDRAMから不定なデー

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タを読み込んで誤った動作を行うことを防止することができる。なお、第1および第2の電圧監視ICは必ずしもICである必要はなく、ディスクリート部品で構成することもできる。

【0054】以上の説明から明らかなように、主電源の供給が停止されると第1の電圧監視ICが主電源の電圧の低下を検出し、DRAM制御ロジックにセルフリフレッシュ・モードへの移行を要求する。DRAM制御ロジックは、CPUのバスアクセス・サイクルの中からDRAMをアクセスしていないタイミングを検出し、RASCASをセルフリフレッシュ・モードとなるシーケンスで出力する。

【0055】次にDRAM制御ロジックは、第2の電圧監視ICからリセット信号を出力させるべく、第2の電圧監視ICのVref 入力に接続されるデジタル出力信号をLow レベルに変化させる。この結果、第2の電圧監視ICはリセット信号を出力し、本システムはリセット状態となる。2つの電圧監視ICのリセット出力がLowとなるので、セレクトはALRM信号を出力する。したがって、バックアップ電源が放電可能ならば、RAS /CAS 出力はLow レベルを維持する。

【0056】主電源が投入されると、DRAM制御ロジックはALRM信号と同一のレベルをRAS /CAS 信号として出力する。第1の電圧監視ICが、主電源起動を検出し、リセット出力をHighレベルとすると、セレクトの出力対象が、ALRM信号からDRAM制御ロジックの出力するRAS /CAS 信号に変化する。また、DRAM制御ロジックは、第2の電圧監視ICのVref に対するデジタル出力信号をHighレベルとする。この結果、所定の時間経過後に、第2の電圧監視ICのリセット出力は解除され、本システムはリセット状態から動作状態になる。

【0057】リセット出力は、DRAM制御ロジックにも入力され、セルフリフレッシュ・モードからの復帰シーケンスの起動トリガとなる。ALRM信号がLow レベルであれば、復帰シーケンスに従ってRAS /CAS が制御される。ALRM信号がHighレベルの場合、即ちDRAMがバックアップされていない場合は、RAS /CAS 共にHighレベルを出力する。これによりDRAMが要求するイニシャル・モードが満たされる。

【0058】

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【発明の効果】以上述べたように、本発明によれば、DRAMバックアップの為のタイミング制御を、主電源の電圧で動作する論理回路で行うので、ほとんどの回路を集積化できる。また、セルフリフレッシュ・モードへの移行、通常モードへの復帰ともに、論理回路だけで実行するので、ソフトウェアの負担がなくなる。さらに、主電源低下時、システムのリセットを行う前に、DRAMだけをアクセス不能としてしまうと、リセットまでの間にCPUが暴走して、SRAMなど他の保存すべきデータを破壊してしまう可能性があるが、本発明では、第1の電圧監視ICの出力するリセット出力を、CPUに対するバス・ホールド要求とすることにより、CPUの暴走を防ぐことができる。

【図面の簡単な説明】

【図1】本発明の実施例としてのDRAMバックアップ回路のブロック図である。

【図2】バックアップ電源VDBの供給中に主電源Vccが立ち上がった場合の動作タイミングを示すタイミングチャートである。

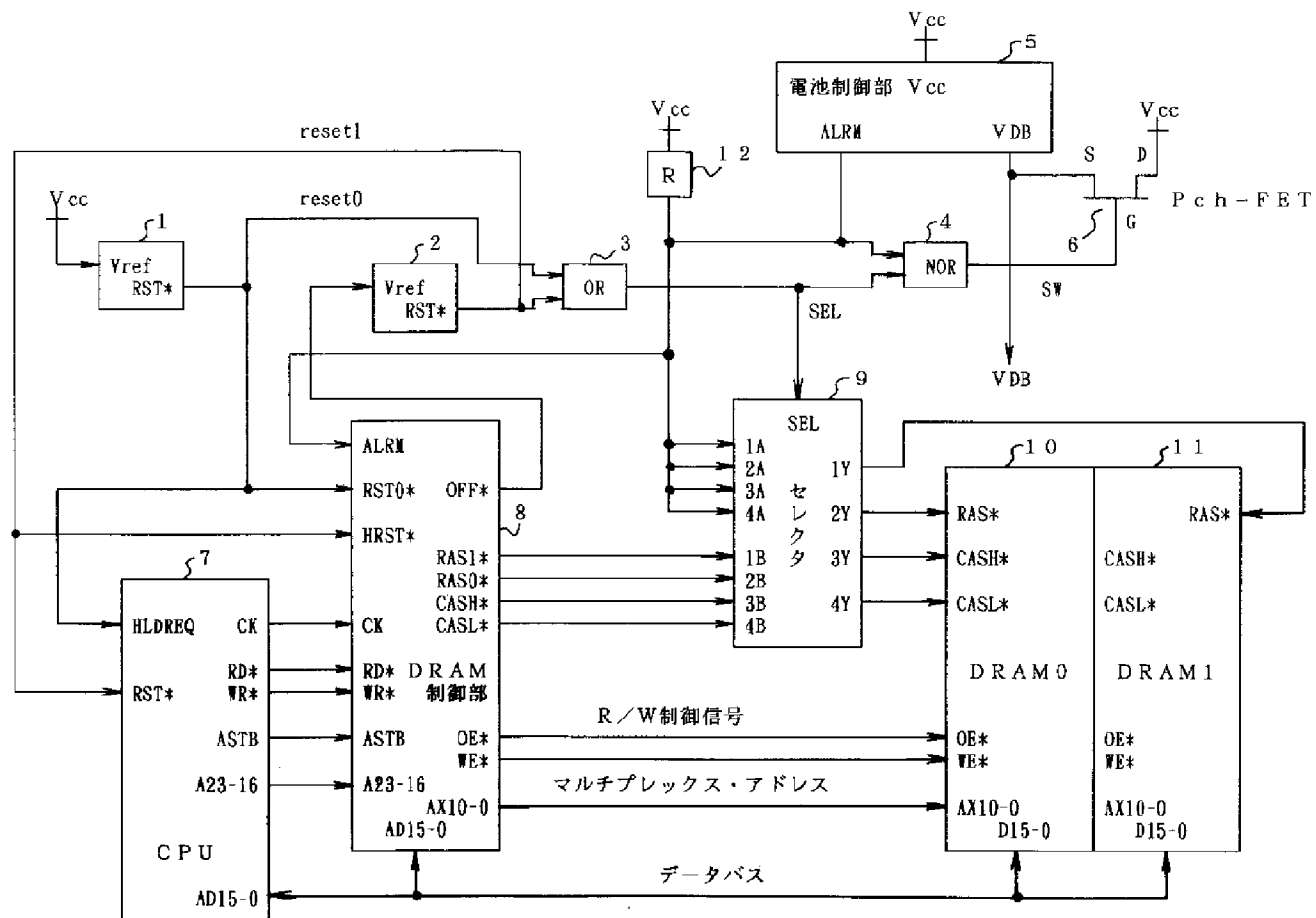
【図3】バックアップ電源VDBの遮断中に、主電源Vccが立ち上がった場合の動作タイミングを示すタイミングチャートである。

【図4】主電源Vccの遮断後、バックアップ電源VDBが供給される場合の動作タイミングを示すタイミングチャートである。

【図5】主電源Vccの遮断後、バックアップ電源VDBも供給されない場合の動作タイミングを示すタイミングチャートである。

【符号の説明】

- 1 第1の電圧監視IC
- 2 第2の電圧監視IC
- 3 OR論理ゲート
- 4 NOR論理ゲート
- 5 予備電源制御部
- 6 FET素子
- 7 CPU
- 8 DRAM制御部
- 9 セレクト
- 10 DRAM
- 11 DRAM

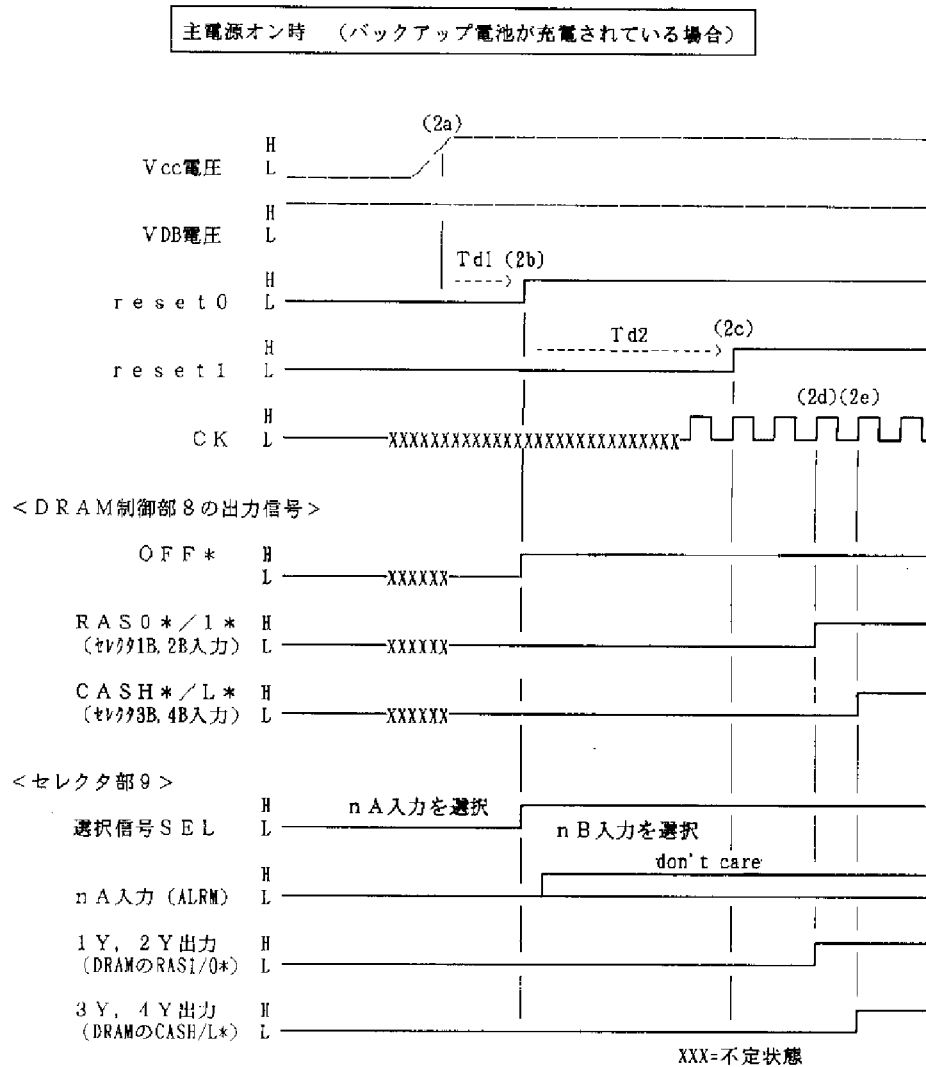


【図 1】

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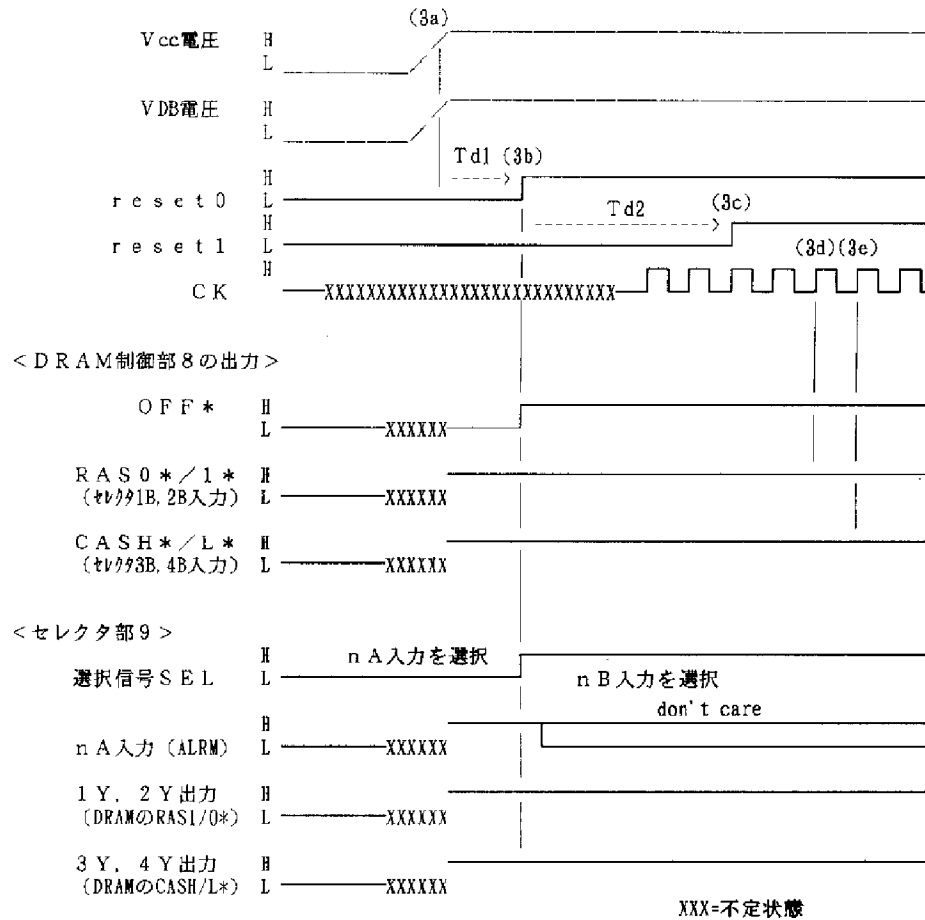
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【図2】

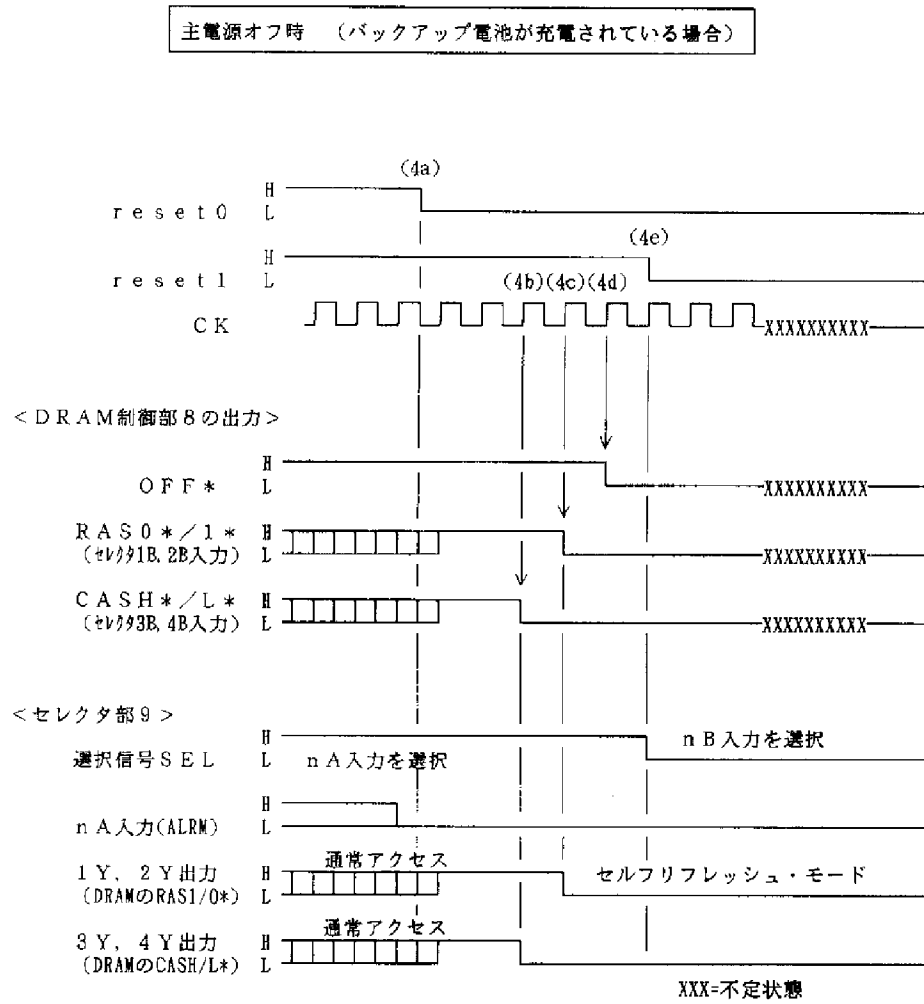


【図 3】

主電源オン時 (バックアップ電池が充電されていない場合)



【図4】



【図 5】

