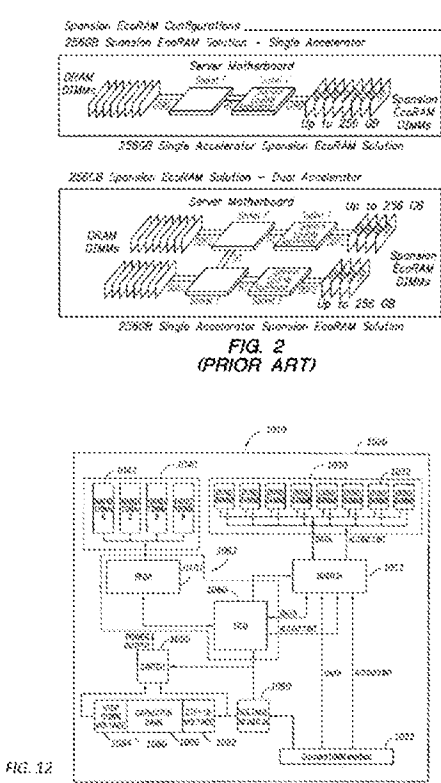
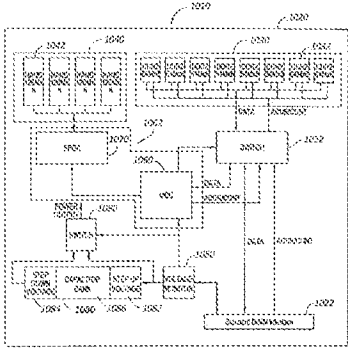


## Support for Claim Amendments

| Claim Element | Limitation                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | Support                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|---------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2.1           | A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, | <p>Para. [00123]</p> <p>“For example, <b>the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figure 2 and Fig. 12.</p>  <p><b>FIG. 2 (PRIOR ART)</b></p> <p><b>FIG. 12</b></p> |

|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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|  | <p>The memory socket of a computer system includes pins soldered onto the system board that provide electrical conduits for system power, data, and address and control signals from the system board to be electrically connected to corresponding edge connections of the edge connector 1022 when it is inserted into the memory socket.</p> <p>The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.</p> <p>The set of data conduits includes at least 72 data conduits.</p> <p>Para. [00122]</p> <p>“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>”.</p> <p>The embodiment of FIG. 13 shows nine x8 DRAM devices for a data bus bit width of 72:</p> |
|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|            |                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
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| <p>2.2</p> | <p>a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits</p> | <p>Para. [00123]</p> <p>“For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data</b>, address, and control <b>signals between the memory system 1010 and the host system . . .</b></p> <p>For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00124]</p> <p>“For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b>”</p> <p>This is showing a 64 bit wide DDR2 data bus, where each bit is sent in parallel. From the DDR2 Standard a POSITA would be aware that each data line is one bit wide as illustrated in FIG. 12:</p> <p>FIG. 12</p>  |
| <p>2.3</p> | <p>the DIMM comprising: a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:</p>                                                                                                                                                                                                             | <p>Para. [00122]</p> <p>“In certain embodiments, <b>the PCB 1020</b> has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) <b>form factor with a height</b> of 30 millimeters and <b>a width</b> of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters.”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                           |

|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2.4 | <p>an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:</p> <p>a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,</p> <p>a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and</p> <p>a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;</p> | <p>Para. [00123]</p> <p>“For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b>. For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector</b>.”</p> <p>When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.</p> <p>See also limitation 2.1.</p> |
| 2.5 | <p>a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | <p>Note respective power conduits (Vdd and gnd) of the set of power conduits of the Standard DIMM Interface 1022 are electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16, for example, in Fig. 12 the input voltage supply lines is shown electrically connected to the Voltage Monitor 1050.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |



conduct an input voltage when the system power is provided to the DIMM from the system board;

a set of data lines electrically coupled to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

FIG. 12

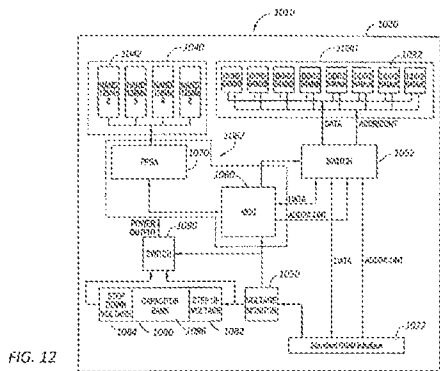
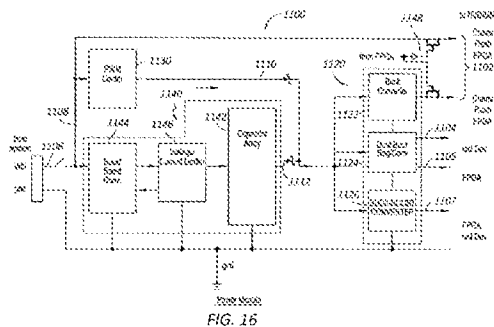


FIG. 16



For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd).

Para. [00124]

“For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises **eight 64Mx8 DDR2 SDRAM** elements 1032.”

Note, for example, the data lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12 are shown as 64-bit wide coupled to eight DDR2 SDRAM devices each of which having a bit width of 8-bit.

And

Para. [00172]

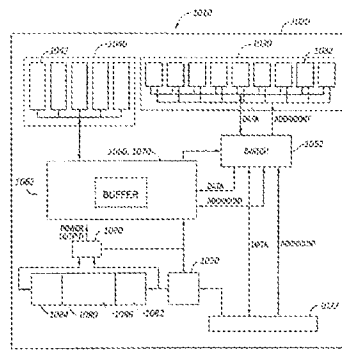
“In one embodiment, for example, the volatile memory subsystem 1030 comprises **a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example,**



a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to:

“FIG. 14 is a block diagram of an example memory module 1010 having **a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein.**”

FIG. 14

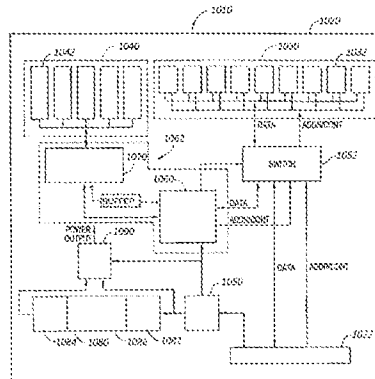


Para. [00172]

Para. [00178]

For example, FIG. 13 shows controller 1062 comprising a buffer:

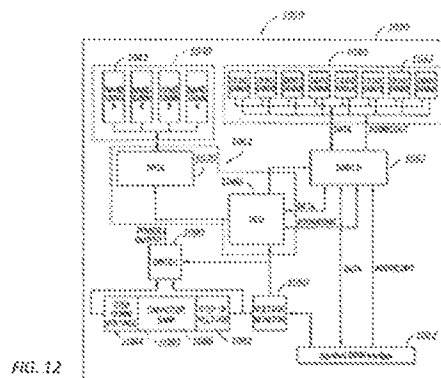
FIG. 13



Para. [00127]

“Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the **logic element 1070 comprises** an FPGA available from Lattice Semiconductor Corporation which includes **an internal flash**. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. **The internal flash can improve the speed of the memory system 1010 and save physical space**. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, **the logic element 1070 is a custom device**. In certain embodiments, **the logic element 1070 comprises various discrete electrical elements**, while in certain other embodiments, **the logic element 1070 comprises one or more integrated circuits**. FIG. 14 is a block diagram of an example memory module 1010 having **a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062** in accordance with certain embodiments described herein. **In certain embodiments, the controller 1062 includes one or more other components**. For example, in one embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.”

FIG. 12



|     |                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     |                                                                                                                                                                                                                        | <p>Para. [00133]</p> <p>“The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.” “In certain embodiments, <b>the voltage monitor circuit 1050 is part of the controller 1062</b> (e.g., part of the MCU 1060)” Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 2.7 | <p>compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and</p> <p>detect a trigger condition;</p>                                       | <p>Para. [00133]</p> <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 2.8 | <p>wherein, in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including:</p> <p>a first write operation to write a first set of data bits</p> | <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, <b>a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|     | <p>into a first portion of the data storage element;</p> <p>a second write operation to write a second set of data bits into a second portion of the data storage element, and subsequently; and subsequently</p> <p>a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;</p> | <p>Para. [00174]</p> <p>“In certain embodiments, <b>when the first and second data slices are written to the buffer in the controller 1062</b>, the controller 1062 <b>combines the first and second data slices 1630, 1640 into complete words or blocks of words</b> and <b>then writes each complete word or block of words to the non-volatile memory</b> subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.”</p> <p>Para. [00177]</p> <p>“In certain embodiments, <b>transferring each data word comprises storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem</b> 1040 in an operational block 1626.”</p>                                                                                                                                                                                                  |
| 2.9 | <p>wherein, when the system power is provided to the DIMM from the system board:</p> <p>the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and wherein:</p> <p>a specified operating voltage value is within a range of operating voltage values of the DIMM,</p> <p>the range of operating voltage values is bounded by an upper operating voltage value and a</p>                                                         | <p>For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | <p>lower operating voltage value,</p> <p>the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,</p> <p>the first threshold voltage corresponds to the lower operating voltage value, and</p> <p>the second threshold voltage corresponds to the upper operating voltage value;</p>                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2.10 | <p>a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and</p> | <p>FIG. 12</p> <p>Para. [00124]</p> <p><b>“Volatile memory elements 1032 compatible with certain embodiments described herein have packaging</b> which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data</p> |





and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively,

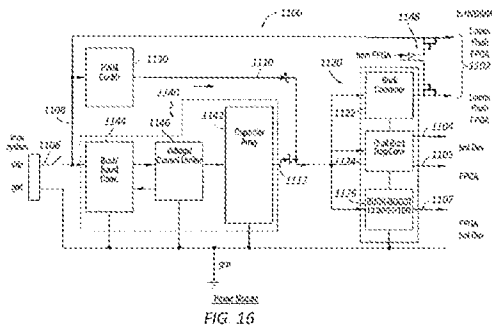
voltage 1102 is provided to the memory system 1010 from the input 1106 and **the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.**”

The conversion element 1120 is always powered from the system power through the first power element 1130 in either the first or second state, and the trigger condition here is the same as 2.8, above, disclosed in:

Para. [00130]

“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond **in response to a trigger condition.**”

FIG. 16



On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

Para. [00148]

“**The conversion element 1120 can comprise one or more buck converters** and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124,

|      |                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                          | <p>1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters</b>, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, <b>the conversion element 1120</b> receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and <b>reduces the input to an appropriate amount for powering various components of the memory system</b>. For example, <b>the buck- converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM)</b>, the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. <b>In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.</b>”</p> |
| 2.12 | <p>the set of components including:<br/>a first component electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;</p> | FIG. 16                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

a second component electrically connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;

a third component electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board;

and

a fourth component electrically connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;

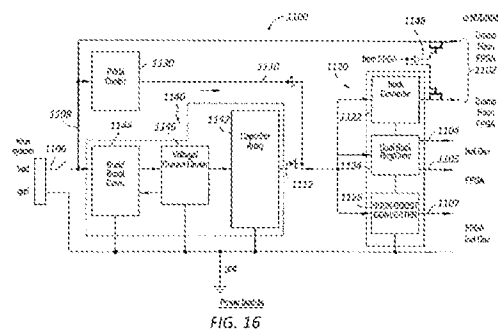


FIG. 12

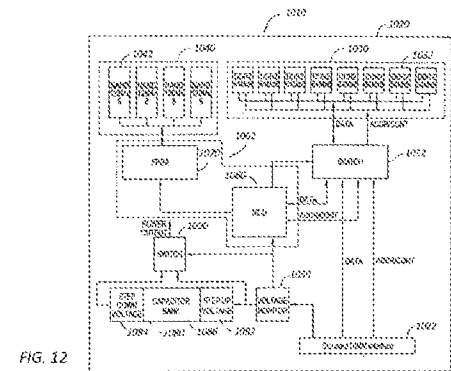


FIG. 12

On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

On the right, each of the DRAM are shown as being connected to the first regulated voltage, for example.

On the right, the isolation device is shown as being connected to the second regulated voltage, for example.

On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example.

On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:

Para. [00148]

“the other reduced **voltage 1105** is 1.2V and is used to **power the controller 1062** (e.g., FPGA). The subblock 1126 can provide yet

|      |                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                                                                                           | <p>another voltage 1107 to the memory system 1010. For example, the <b>voltage 1107</b> may be 3.3V and may be used to <b>power</b> both the <b>controller 1062</b> and <b>the at least one circuit 1052.</b>”</p> <p>As shown in FIG. 12, above, the controller 1062 includes the components <b>FPGA 1070</b>, and <b>the MCU 1060</b>, and thus needs two different voltages for each of the components 1070, 1060.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 2.13 | <p>wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit;</p>                                                                                                                                                                                                               | <p>Para. [00148]</p> <p>“The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.</b>”</p> <p>And</p> <p>Para. [00148]</p> <p>“In certain embodiments, <b>the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130</b> or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and <b>reduces the input to an appropriate amount for powering various components of the memory system.</b>”</p> |
| 2.14 |                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 2.15 | <p>wherein each component of the set of components:</p> <p>(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and</p> <p>(ii) when the system power is provided to the DIMM from the system board, is powered:</p> <ul style="list-style-type: none"> <li>only by one or more of the first, second,</li> </ul> | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |

|      |                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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|      | <p>third, and fourth converter circuits; and</p> <ul style="list-style-type: none"> <li>• only via the one or more of the first, second, third, and fourth regulated voltage lines;</li> </ul>                                                                                                                                   | <p>system power is received from couples power to each of the four converter circuits via voltage 1110.</p> <p>Para. [00145]</p> <p>“In a second state, <b>the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.</b>”</p> <p>Para. [00151]</p> <p>“The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. <b>During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem</b> in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.”</p> <p>The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.</p> |
| 2.16 | <p>wherein the plurality of DDR SDRAM packages includes:</p> <ul style="list-style-type: none"> <li>a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;</li> <li>a second group of at least four DDR</li> </ul> | <p>FIG. 21</p> <p>FIG. 21</p> <p>Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.</p> <p>Para. [00172]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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|  | <p>SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and</p> | <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from <b>two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology <b>including two DRAM segments 1630, 1640</b> for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from <b>the first DRAM segment 1630 and the second DRAM segment 1640</b> of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. <b>The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.</b>”</p> <p>Para. [00177]</p> <p>“In certain embodiments, transferring each data word comprises storing <b>a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624</b>, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p> <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.</p> |
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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | <p>Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.</p>                                                                                                                                                                                                                                                                                                                                   |
| 2.17 | <p>when the system power is provided to the DIMM from the system board:</p> <ul style="list-style-type: none"> <li>the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;</li> <li>the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit</li> </ul> | <p>Para. [00173]</p> <p>“In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode</b>.”</p> <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer.</p> |

|      |                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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|      | <p>DDR data signals in parallel via the integer number of data lines of the set of data lines; and</p> <ul style="list-style-type: none"> <li>the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and</li> </ul> | <p>Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”</p> <p>Para. [00182]</p> <p>“In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 2.18 | <p>wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.</p>                                                             | <p>Para. [00123]</p> <p>“The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>Para. [00178]</p> <p>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b>”</p> |
| 28   | <p>wherein the second component is further connected to the first regulated voltage line and is powered by the first</p>                                                                                                                                                                                  | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

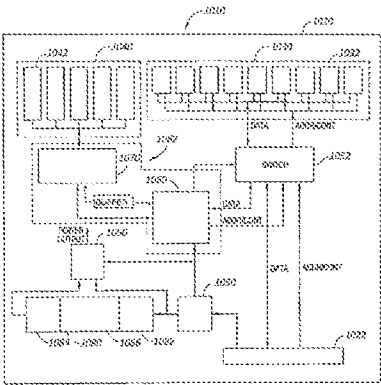
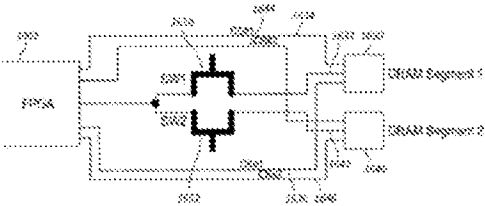


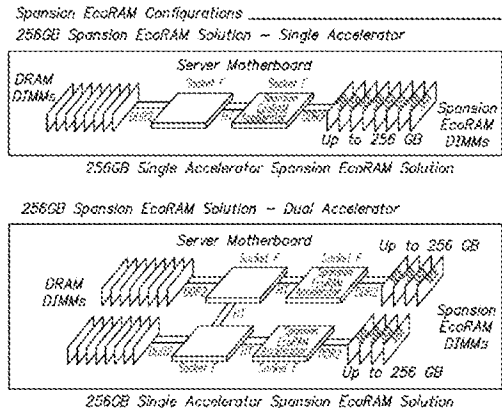


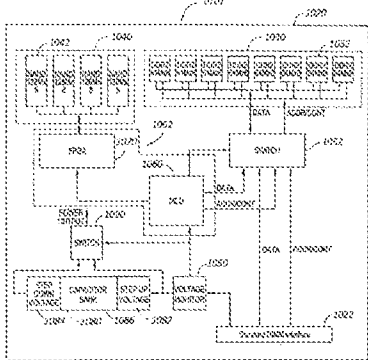
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|    |                                                                                                                                                                                                                                                                                                                               | <b>has a very low profile (VLP) form factor with a height of 18.3 millimeters.”</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 32 | wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations                                                                  | Para. [00178]<br>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”                                                                                                                                                                                                                                                                                                        |
| 33 | wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.                 | Para. [00179]<br>“In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer.”                                                                                                                                                                                                                                                                                         |
| 34 | wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.                                                                                                                                                                        | Para. [00149]<br>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are <b>not both powered using the first voltage 1102.</b> ”                                                                                                                                                                                                                                                                                                                                                                |
| 35 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to | Para. [00178]<br>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b> ”<br>Para. [00179]<br>“In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In |

|    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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|    | generate the third set of data bits based on the read first and second sets of data bits.                                                                                                                                                                                                                                                                                                                                                                                                                                       | certain other embodiments, the data word may comprise more than three portions.”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 36 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.                                                                                                                       | <p>Para. [00178]</p> <p>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>”</p> <p>Difference from Claim 35 is the read from the buffer is a plurality of steps in Claim 35, and one step here. Same sentence in Para. [00178] supports both scenarios.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 37 | wherein, prior to performing the third write operation, the logic element is further configured to perform (i) a first read operation of the plurality of read operations to read the first set of data bits from the first portion of the data storage element, and (ii) a second read operation of the plurality of read operations to read the second set of data bits from the second portion of the data storage element, and to generate the third set of data bits based on the read first and second sets of data bits. | <p>Para. [00178]</p> <p>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>”</p> <p>Difference from Claim 35 is the read from the buffer is <b>a plurality of steps in Claim 35, and specifically two steps here.</b> Same sentence in Para. [00178] supports both scenarios.</p> <p>Para. [00174]</p> <p>“In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040.”</p> <p>Reading a data word or a block of words to be written into the NVM.</p> |
| 38 | wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to                                                                                                                                                                                                                                                                                                                                                                                          | <p>Para. [00178]</p> <p>“In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, <b>reading a 32-bit block from the slice into the buffer,</b> and putting the 32-bit slice back into self-refresh. The 40-bit slice is then</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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|    | the detected trigger condition, one or more read operations.                                                                                                                                                                                 | brought out of self-refresh and <b>a 40-bit block from the slice is read into a buffer</b> . Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 39 | wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively. | Para. [00178]<br>“In the example embodiment, <b>the process of "slicing" the volatile memory</b> during a backup includes bringing the 32-bit slice out of self-refresh, <b>reading a 32-bit block from the slice into the buffer</b> , and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and <b>a 40-bit block from the slice is read into a buffer</b> . Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”                                                                                                                                                                                                                                                                                                                                                     |
| 40 | wherein the logic element is further configured to perform (i) first and second read operations of the one or more read operations, and (ii) subsequently, the first and second write operations.                                            | Para. [00178]<br>“In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. <b>The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b> ”<br><br>This makes clear that the read of the slices must happen before writing the slices into the buffer. |

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| 41 | <p>wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.</p> | <p>FIG. 13</p>  <p>FIG. 21</p>  <p>Para. [00172]</p> <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.”</p>                                                           |
| 42 | <p>wherein, in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.</p>                                                                                                                                                                                       | <p>Para. [00133]</p> <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 <b>transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p>                                                                                                                                                                                                                              |
| 43 | <p>wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and wherein, in response to the additional trigger</p>                                                           | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a <b>certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below a <b>specified operating voltage</b>. In certain embodiments, a <b>trigger condition</b> occurs when the voltage goes above a <b>certain threshold value</b>, such as, for example, 10 percent above a <b>specified operating voltage</b>. <b>In</b></p> |

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|      | condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.                                                                                                                                                                                                                                                                                                                                                                                                | <b>some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 44.1 | A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, | <p>Para. [00123]</p> <p>“For example, <b>the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.”</b></p> <p>Per the JEDEC DDR2 Standard, power is supplied from the socket to designated edge connections of the standard 240-pin DDR2 edge connector. A POSITA would be aware of this standard and the configuration of both the edge connector and the socket. For example, as shown in FIG. 2 of the disclosure:</p> <p>Figure 2</p>  <p><b>FIG. 2<br/>(PRIOR ART)</b></p> |
| 44.2 | a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are                                                                                                                                                                                                                                                                            | <p>Para. [00123]</p> <p>“For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system . . .</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

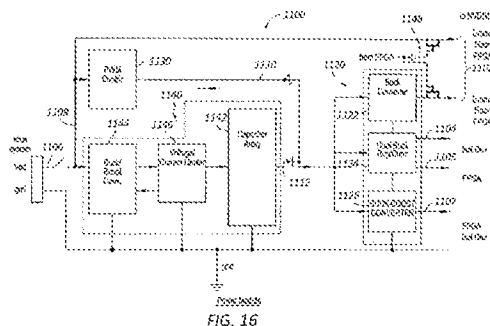
|      |                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
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|      | electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits                 | <p>For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00124]</p> <p>“For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b>”</p> <p>This is showing a 64 bit wide DDR2 data bus, where each bit is sent in parallel. From the DDR2 Standard a POSITA would be aware that each data line is one bit wide as illustrated in FIG. 12:</p> <p>FIG. 12</p>  <p>FIG. 12</p>                                                                                                                                                                                  |
| 44.3 | the DIMM comprising: a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including: | <p>Para. [00122]</p> <p>In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein.</p> |
| 44.4 | an interface having edge connections disposed along the width dimension and                                                               | <p>Para. [00123]</p> <p>“For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                 |
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|      | <p>configured to fit into the memory socket, the edge connections including:</p> <ul style="list-style-type: none"> <li>a first set of edge connections configured to be electrically connected to respective power conduits of the set of power conduits,</li> <li>a second set of edge connections each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and</li> <li>a third set of edge connections configured to be electrically connected to respective address and control conduits of the set of address and control conduits;</li> </ul> | <p><b>host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> |
| 44.5 | <p>a set of voltage supply lines electrically connected to the first set of edge connections, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;</p>                                                                                                                                                                                                                                                                                                                                                                                  | <p>FIG. 12</p> <p>FIG. 12</p>                                                                                                                                                                                                                                                                                   |



a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

FIG. 16



Note the data lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.

And

Para. [00172]

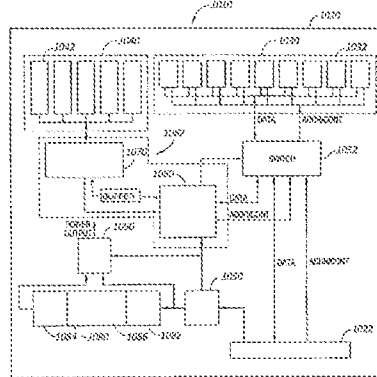
“In one embodiment, for example, the volatile memory subsystem 1030 comprises **a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

The embodiment of FIG. 13 shows nine x8 DRAM devices for a data bus bit width of 72:



a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and a voltage monitor circuit electrically connected to the input voltage supply and coupled to the logic element, the voltage monitor circuit configured to:

FIG. 13



Para. [00127]

“Referring to FIG. 12, in certain embodiments, **the logic element 1070** comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation **which includes an internal flash**. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. **The internal flash can improve the speed of the memory system 1010 and save physical space**. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, **the logic element 1070 comprises one or more integrated circuits**. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. **In certain embodiments, the controller 1062 includes one or more other components**. For example, in one embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.”

FIG. 13

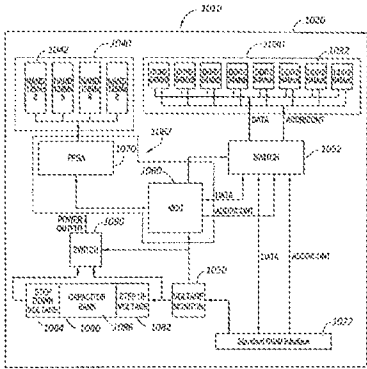


|      |                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | <p>second threshold voltage; and<br/>detect a trigger condition;</p>                                                                                                                                                                                                                                                                                                                                                                        | <p><b>portions of the controller 1062 upon detecting a power threshold condition.”</b></p> <p>Para. [00130]<br/>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p>                                                                                                                      |
| 44.8 | <p>wherein, in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including:</p> <ul style="list-style-type: none"> <li>a first write operation to write a first set of data bits into a first portion of the data storage element;</li> <li>a second write operation to write a second set of data bits into a second portion of the data storage element;</li> </ul> | <p>Para. [00130]<br/>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond <b>in response to a trigger condition.</b>”</p> <p>Para. [00177]<br/>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition</b> (e.g., a power failure) <b>occurs</b>. In certain embodiments, <b>transferring each data word comprises storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p> |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 44.9  | <p>wherein, when the system power is provided to the DIMM from the system board: the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and wherein:</p> <p>a specified operating voltage value is within a range of operating voltage values of the DIMM,</p> <p>the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value,</p> <p>the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,</p> <p>the first threshold voltage corresponds to the lower operating voltage value, and</p> <p>the second threshold voltage corresponds to the upper operating voltage value;</p> | <p>For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |
| 44.10 | a set of components coupled to the PCB, the set of components including a plurality of                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | FIG. 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and

FIG. 12



Para. [00124]

“**Volatile memory elements 1032 compatible with certain embodiments described herein have packaging** which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”

Para. [00172]

“In one embodiment, for example, the volatile memory subsystem 1030 comprises **a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

And

Para. [00122]

“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”

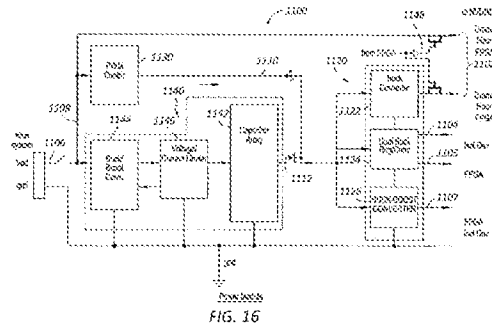
And

Para. [00124]

“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. **Types of DRAM elements 1032 compatible with certain embodiments described herein include,**

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <p>but are not limited to, <b>DDR, DDR2, DDR3, and synchronous DRAM (SDRAM)</b>. For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032</b>. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, <b>volatile memory elements 1032 having bit widths of 4, 8, 16, 32</b>, as well as other bit widths, are compatible with certain embodiments described herein.”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 44.11 | <p>first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively,</p> | <p>FIG. 16</p> <p>Para. [00145]</p> <p>“<b>The power module 1100 can be configured to be operated in at least three states</b> in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. <b>In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.</b>”</p> <p>And</p> <p>The trigger condition here is the same as 2.8, above, disclosed in: Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond <b>in response to a trigger condition.</b>”</p> <p>FIG. 16</p> |





On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

Para. [00148]

**“The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g.,**



|       |                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | DIMM from the system board;                                                                                                                          | <p>On the right, the isolation device is shown as being connected to the second regulated voltage, for example.</p> <p>On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example.</p> <p>On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:</p> <p>Para. [00148]</p> <p>“the other reduced <b>voltage 1105</b> is 1.2V and is used to <b>power the controller 1062</b> (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the <b>voltage 1107</b> may be 3.3V and may be used to <b>power</b> both the <b>controller 1062</b> and the at least one circuit 1052.”</p> <p>As shown in FIG. 12, above, the controller 1062 includes the components FPGA 1070, and the MCU 1060, and thus needs two different voltages for each of the components 1070, 1060.</p> |
| 44.13 | wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; | <p>Para. [00148]</p> <p>“The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.</b>”</p> <p>And</p> <p>Para. [00148]</p> <p>“In certain embodiments, <b>the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130</b> or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and <b>reduces the input to an appropriate amount for powering various components of the memory system.</b>”</p>                                                                                                                                                                    |
| 44.14 |                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

44.15

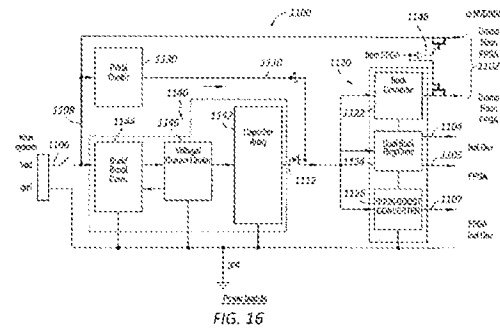
wherein each component  
of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) when the system power is provided to the DIMM from the system board, is powered:

- only by one or more of the first, second, third, and fourth converter circuits; and
- only via the one or more of the first, second, third, and fourth regulated voltage lines;

FIG. 16



On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides a voltage 1110 to each of the four converter circuits.

Para. [00145]

**“In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.”**

Para. [00151]

“For example, referring to FIG. 16, **a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.**”

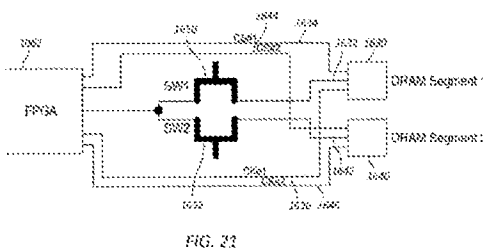
On the right side of the figure, the components are listed. The power provided to the PWM controller 1130 and from there to the converter circuits is the only power to the module. There is no alternative power source claimed.

44.16

wherein the plurality of  
DDR SDRAM packages  
includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

FIG. 21



Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.

|  |                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and</p> | <p>Para. [00172]</p> <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from <b>two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology <b>including two DRAM segments 1630, 1640</b> for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from <b>the first DRAM segment 1630 and the second DRAM segment 1640</b> of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. <b>The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.</b>”</p> <p>Para. [00177]</p> <p>“In certain embodiments, transferring each data word comprises storing <b>a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624</b>, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p> <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out</p> |
|--|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | <p>of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.</p>                                                                                                                                                                                 |
| 44.17 | <p>when the system power is provided to the DIMM from the system board:</p> <ul style="list-style-type: none"> <li>the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;</li> <li>the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an</li> </ul> | <p>Para. [00173]</p> <p>“In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode</b>.”</p> <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out</p> |

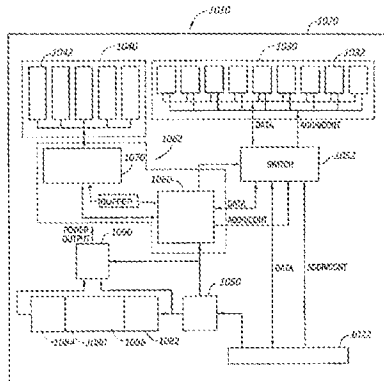
|       |                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | <p>integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and</p> <ul style="list-style-type: none"> <li>the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and</li> </ul> | <p>of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”</p> <p>Para. [00182]</p> <p>“In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| 44.18 | <p>wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.</p>                                                                                     | <p>Para. [00123]</p> <p>“The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC),</b> the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>Para. [00178]</p> <p>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b>”</p> |
| 45    | <p>wherein the plurality of write operations further includes a third</p>                                                                                                                                                                                                                                                         | <p>Para. [00177]</p> <p>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

|    |                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
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|    | <p>write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform at regular intervals of time all of the first and second write operations followed by the third write operation.</p>                | <p>1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p>                                                           |
| 46 | <p>wherein, the logic element is further configured to perform the third write operation by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.</p> | <p>Para. [00177]</p> <p>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>Para. [00178]</p> <p>“<b>The 32-bit and 40-bit slices are then combined into a 72-bit block</b> by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and <b>written into the non-volatile memory subsystem (e.g., flash).</b>”</p> |
| 47 | <p>wherein, prior to performing the third write operation, the logic element is further configured to generate</p>                                                                                                                                                                                                                      | <p>Para. [00178]</p> <p>“<b>The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062</b> and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

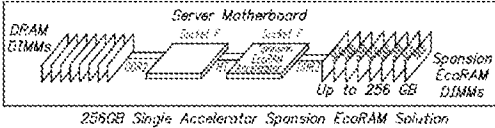
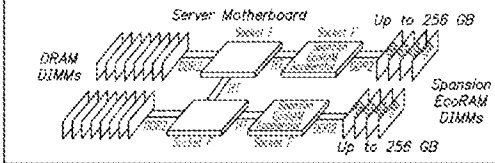


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|    | the third set of data bits based on groups of data bits stored in the data storage element.                                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 48 | wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.                                                                                                                                                                                                                                                                                                         | Para. [00149]<br>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are <b>not both powered using the first voltage 1102.</b> ”                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| 50 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits. | Para. [00130]<br>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”<br>Para. [00178]<br>“ <b>The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062</b> and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”                 |
| 51 | wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively.                                                                                              | Para. [00130]<br>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”<br>Para. [00178]<br>“The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, <b>the process of "slicing" the volatile memory during a backup</b> includes bringing the 32-bit slice out of self-refresh, <b>reading a</b> |

|    |                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
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|    |                                                                                                                                                                                                                                                                                                                                                          | <b>32-bit block from the slice into the buffer</b> , and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and <b>a 40-bit block from the slice is read into a buffer.</b> ”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| 52 | wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time a plurality of read operations.                                                                                                         | <p>Para. [00130]<br/>         “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> <p>Para. [00177]<br/>         “The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition (e.g., a power failure) occurs</b>. In certain embodiments, transferring each data word comprises <b>storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem</b> 1040 in an operational block 1626.”</p> |
| 53 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read data bits from the data storage element and to generate the third set of data bits based on the read data bits. | <p>Para. [00130]<br/>         “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> <p>Para. [00178]<br/>         “<b>The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062</b> and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>”</p>                                                                                                                                                                                                                                                                                                 |
| 54 | wherein the width dimension is 133.35 millimeters                                                                                                                                                                                                                                                                                                        | <p>Para. [00122]<br/>         “For example, the PCB I 020 can have a low profile (LP) form factor with a height of 30 millimeters and <b>a width of</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

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|    |                                                                                                                                                                                                                                                                                                                                                              | <p><b>133.35 millimeters.</b> In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB I 020 has a very low profile (VLP) form factor with a height of 18.3 millimeters.”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 55 | <p>wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.</p>                                                                                                                                                                                                                         | <p>Para. [00122]</p> <p>“<b>For example, the PCB I 020 can have a low profile (LP) form factor with a height of 30 millimeters</b> and a width of 133.35 millimeters. <b>In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB I 020 has a very low profile (VLP) form factor with a height of 18.3 millimeters.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 56 | <p>wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.</p> | <p>Para. [00177]</p> <p>“The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition (e.g., a power failure) occurs.</b> In certain embodiments, transferring each data word comprises <b>storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>FIG. 13</p>  <p>As can be seen in FIG. 13, the transfer from the DRAM occurs on a connection on the right side of the buffer, and the transfer to NVM will occur on a connection on the left side of the buffer.</p> |

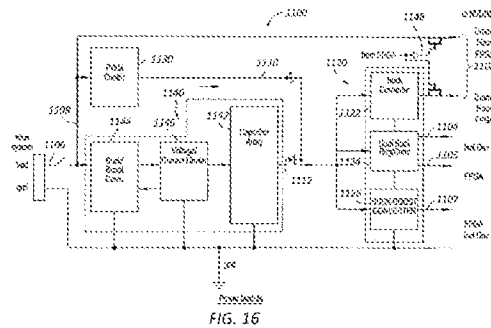
|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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| 57   | <p>wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.</p>                                                                                                               | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a <b>certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below a <b>specified operating voltage</b>. In certain embodiments, a <b>trigger condition</b> occurs when the voltage goes above a <b>certain threshold value</b>, such as, for example, 10 percent above a <b>specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>Para. [00133]</p> <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p> |
| 58.1 | <p>A dual in-line memory module (DIMM) configured to fit into a memory socket of a system board of a computer system, the memory socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits, wherein system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board,</p> | <p>Para. [00123]</p> <p>“For example, <b>the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b>. For example, the interface 1022 can comprise a <b>standard 240-pin DDR2 edge connector.</b>”</p> <p>Per the JEDEC DDR2 Standard, power is supplied from the socket to designated edge connections of the standard 240-pin DDR2 edge connector. A POSITA would be aware of this standard and the configuration of both the edge connector and the socket. For example, as shown in FIG. 2 of the disclosure:</p> <p>Figure 2</p>                                                                                                                                                               |

|      |                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
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|      |                                                                                                                                                                                                                                                                                                                                                              | <p><i>Sansion EcoRAM Configurations</i></p> <p><i>256GB Sansion EcoRAM Solution – Single Accelerator</i></p>  <p><i>256GB Single Accelerator Sansion EcoRAM Solution</i></p> <p><i>256GB Sansion EcoRAM Solution – Dual Accelerator</i></p>  <p><i>256GB Single Accelerator Sansion EcoRAM Solution</i></p> <p><b>FIG. 2</b><br/><b>(PRIOR ART)</b></p>                                                                                                                                                                                                                                                                                                                                                  |
| 58.2 | <p>a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits</p> | <p>Para. [00123]</p> <p>“For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data</b>, address, and control <b>signals between the memory system 1010 and the host system . . .</b></p> <p>For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00124]</p> <p>“For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b>”</p> <p>This is showing a 64 bit wide DDR2 data bus, were each bit is sent in parallel. From the DDR2 Standard a POSITA would be aware that each data line is one bit wide as illustrated in FIG. 12:</p> <p>FIG. 12</p> |





set of data lines includes at least 72 data lines; and  
a set of address and control lines electrically coupled to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;



Please note the input voltage supply line from the system on left is electrically connected to the PWM Controller 1130.

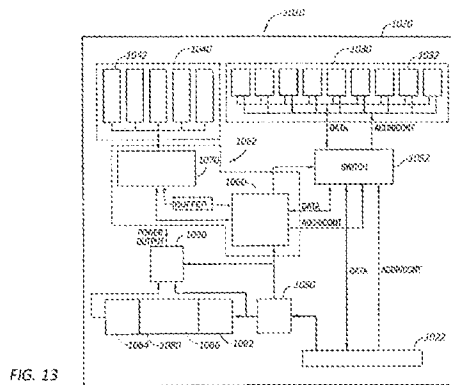
Note the data lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.

And

Para. [00172]

“In one embodiment, for example, the volatile memory subsystem 1030 comprises a **72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

The embodiment of FIG. 13 shows nine x8 DRAM devices for a data bus bit width of 72:



And

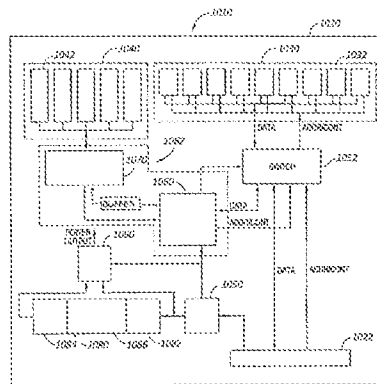




a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to:

compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, **the logic element 1070 comprises one or more integrated circuits.** FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. **In certain embodiments, the controller 1062 includes one or more other components.** For example, in one embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.”

FIG. 13



Para. [00127]

“FIG. 14 is a block diagram of an example memory module 1010 having **a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein.**”

FIG. 14



|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
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| 58.8 | <p>wherein, in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including:</p> <ul style="list-style-type: none"> <li>a first write operation to write a first set of data bits into a first portion of the data storage element;</li> <li>a second write operation to write a second set of data bits into a second portion of the data storage element;</li> </ul>                                                                                  | <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond <b>in response to a trigger condition.</b>”</p> <p>Para. [00177]</p> <p>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition</b> (e.g., a power failure) <b>occurs</b>. In certain embodiments, <b>transferring each data word comprises storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p>     |
| 58.9 | <p>wherein, when the system power is provided to the DIMM from the system board:</p> <ul style="list-style-type: none"> <li>the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and</li> </ul> <p>wherein:</p> <ul style="list-style-type: none"> <li>a specified operating voltage value is within a range of operating voltage values of the DIMM,</li> <li>the range of operating voltage values is bounded by an upper operating voltage value and a</li> </ul> | <p>For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
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|       | <p>lower operating voltage value,</p> <p>the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value,</p> <p>the first threshold voltage corresponds to the lower operating voltage value, and</p> <p>the second threshold voltage corresponds to the upper operating voltage value;</p>                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| 58.10 | <p>a set of components coupled to the PCB, the set of components including a plurality of DDR synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, each DDR SDRAM package of the plurality of DDR SDRAM packages having a bit width of m bits and configured to receive or output m 1-bit wide DDR data signals via respective m data lines of the set of data lines in response to address and control signals received via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and</p> | <p>FIG. 12</p> <p>FIG. 12</p> <p>Para. [00124]</p> <p><b>“Volatile memory elements 1032 compatible with certain embodiments described herein have packaging</b> which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data</p> |



and fourth voltage reducing circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the system power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively,

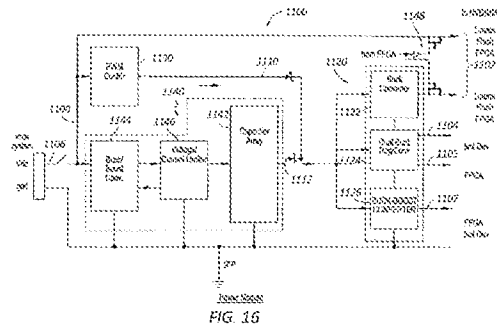
voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. **In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.**”

And

The trigger condition here is the same as 2.8, above, disclosed in: Para. [00130]

“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond **in response to a trigger condition.**”

FIG. 16



On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

Para. [00148]

“The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. **The sub-blocks may comprise various converter circuits** such

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|       |                                                                                                                                                                                                                                                                                                                                           | <p>as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, <b>the conversion element 1120</b> receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and <b>reduces the input to an appropriate amount for powering various components of the memory system.</b> For example, <b>the buck- converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment.</b> The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. <b>In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA).</b> The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”</p> |
| 58.12 | <p>the set of components including:<br/> a first component electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;<br/> a second component electrically connected to the second regulated voltage line and powered</p> | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |



|  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  | <p>by the second regulated voltage when the system power is provided to the DIMM from the system board;</p> <p>a third component electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board;</p> <p>and</p> <p>a fourth component electrically connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;</p> |
|--|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|



On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.

On the right, each of the DRAM are shown as being connected to the first regulated voltage, for example.

On the right, the isolation device is shown as being connected to the second regulated voltage, for example.

On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example.

On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:

Para. [00148]

“the other reduced **voltage 1105** is 1.2V and is used to **power the controller 1062** (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the **voltage 1107** may be 3.3V and may be used to **power** both the **controller 1062** and the at least one circuit 1052.”

As shown in FIG. 12, above, the controller 1062 includes the components FPGA 1070, and the MCU 1060, and thus needs two different voltages for each of the components 1070, 1060.



configured to electrically conduct a first chip select signal;  
a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

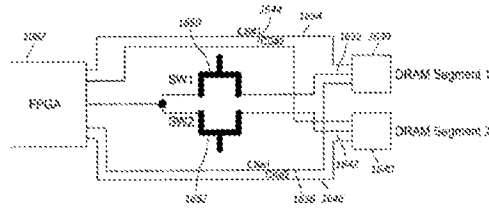


FIG. 21

Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.

Para. [00172]

“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from **two DRAM segments 1630, 1640** of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology **including two DRAM segments 1630, 1640** for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from **the first DRAM segment 1630 and the second DRAM segment 1640** of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. **The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.**”

Para. [00177]

“In certain embodiments, transferring each data word comprises storing **a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624**, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”

Para. [00178]

“**In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.** In certain embodiments, the buffer is included

|       |                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|-------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                                                                                                                                                       | <p>in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash)."</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.</p> |
| 58.16 | <p>when the system power is received by the controller:</p> <ul style="list-style-type: none"> <li>• the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;</li> <li>• the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-</li> </ul> | <p>Para. [00173]</p> <p>"In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode</b>."</p> <p>Para. [00178]</p> <p><b>"In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|-------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       | <p>bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and</p> <ul style="list-style-type: none"> <li>the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and</li> </ul> | <p>in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment."</p> <p>Para. [00182]</p> <p>"In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>"</p> |
| 58.17 | <p>wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.</p>                                                                                                                                                                                                                                                                                                                        | <p>Para. [00123]</p> <p>"The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>"</p> <p>Para. [00172]</p> <p>"In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC),</b> the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes."</p> <p>Para. [00178]</p>                                                                                                                                                                                                                                                                                                                                                    |

|    |                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|    |                                                                                                                                                                                                                                                                                                                                                                                  | <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.”</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 59 | <p>wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.</p> | <p>Para. [00177]</p> <p>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> |
| 60 | <p>wherein the logic element is further configured to perform the third write operation by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.</p>                                           | <p>Para. [00177]</p> <p>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p>                                                                                                                                                                                                                                                                                                                                                                                                       |

|    |                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 61 | wherein, in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.                                                                                                      | Para. [00133]<br>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b> ”                                                                                                                                                                                                                      |
| 62 | wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond a plurality of read operations prior to performing the first and second write operations.                       | Para. [00113]<br>“In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.”                                                              |
| 63 | wherein the logic element is further configured to perform a first and second read operations of the plurality of read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively. | [00172]<br><u>FIG. 21 schematically illustrates an example topology of <b>a connection to transfer data slices from two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a <b>controller 1062</b> of the memory system 1010.</u><br><u>The controller read first and second data slices (sets of data bits) from first and second groups of DDR SDRAM packages, and then write the first and second sets of data bits into the controller 1062 (data storage element).</u> |
| 64 | wherein the width dimension is 133.35 millimeters.                                                                                                                                                                                                        | Para. [00122]<br>“For example, the PCB I 020 can have a low profile (LP) form factor with a height of 30 millimeters and <b>a width of 133.35 millimeters</b> . In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB I 020 has a very low profile (VLP) form factor with a height of 18.3 millimeters.”                                                                                                |
| 65 | wherein the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.                                                                                                                             | Para. [00122]<br>“ <b>For example, the PCB I 020 can have a low profile (LP) form factor with a height of 30 millimeters</b> and a width of 133.35 millimeters. <b>In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50</b>                                                                                                                                                                                                                                       |

|    |                                                                                                                                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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|    |                                                                                                                                                                                                                                                                                                                                                                                          | <b>millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters.”</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 66 | wherein each of the first, second, and third voltage reducing circuits is a buck converter.                                                                                                                                                                                                                                                                                              | Para. [00148]<br><b>“The conversion element 1120 can comprise one or more buck converters</b> and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters</b> , boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.”                                        |
| 67 | wherein, when the system power is provided to the DIMM from the system board, the nonvolatile memory is not powered using the first regulated voltage.                                                                                                                                                                                                                                   | Para. [00149]<br><b>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.”</b>                                                                                                                                                                                                                                                                                                                                                                                                           |
| 68 | wherein, when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal. | Para. [00130]<br><b>“In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage.</b> For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage.</b> In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b> , such as, for example, 10 percent above <b>a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b> ” |



|                                   |                                       |  |                                                           |             |
|-----------------------------------|---------------------------------------|--|-----------------------------------------------------------|-------------|
| <b>Notice of References Cited</b> | Application/Control No.<br>17/582,797 |  | Applicant(s)/Patent Under<br>Reexamination<br>Chen et al. |             |
|                                   | Examiner<br>HASHEM FARROKH            |  | Art Unit<br>2138                                          | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

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|   | H |                                                  |                    |                   |                    |                   |
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|   | J |                                                  |                    |                   |                    |                   |
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**FOREIGN PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>YYYY-MM-DD | Country | Name | CPC Classification |
|---|---|--------------------------------------------------|--------------------|---------|------|--------------------|
|   | N |                                                  |                    |         |      |                    |
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**NON-PATENT DOCUMENTS**

| * |   | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in YYYY-MM-DD format are publication dates. Classifications may be US or foreign.

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|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------------------------|
| <b><i>Index of Claims</i></b><br> | <b>Application/Control No.</b><br>17/582,797 | <b>Applicant(s)/Patent Under Reexamination</b><br>Chen et al. |
|                                                                                                                    | <b>Examiner</b><br>HASHEM FARROKH            | <b>Art Unit</b><br>2138                                       |

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|---|-----------------|---|-------------------|---|---------------------|---|-----------------|
| ✓ | <b>Rejected</b> | - | <b>Cancelled</b>  | N | <b>Non-Elected</b>  | A | <b>Appeal</b>   |
| = | <b>Allowed</b>  | ÷ | <b>Restricted</b> | I | <b>Interference</b> | O | <b>Objected</b> |

| CLAIMS                                                                                                                                                                            |          |            |  |  |  |  |  |  |  |  |
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| <input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47 |          |            |  |  |  |  |  |  |  |  |
| CLAIM                                                                                                                                                                             |          | DATE       |  |  |  |  |  |  |  |  |
| Final                                                                                                                                                                             | Original | 01/19/2025 |  |  |  |  |  |  |  |  |
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|                                                                                                                                                                                   | 27       | -          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 28       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 29       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 30       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 31       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 32       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 33       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 34       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 35       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 36       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 37       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 38       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 39       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 40       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 41       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 42       | ✓          |  |  |  |  |  |  |  |  |

|                                                                                                                    |                                              |                                                               |
|--------------------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------------------------|
| <b><i>Index of Claims</i></b><br> | <b>Application/Control No.</b><br>17/582,797 | <b>Applicant(s)/Patent Under Reexamination</b><br>Chen et al. |
|                                                                                                                    | <b>Examiner</b><br>HASHEM FARROKH            | <b>Art Unit</b><br>2138                                       |

| CLAIM |          | DATE       |  |  |  |  |  |  |  |  |
|-------|----------|------------|--|--|--|--|--|--|--|--|
| Final | Original | 01/19/2025 |  |  |  |  |  |  |  |  |
|       | 43       | ✓          |  |  |  |  |  |  |  |  |
|       | 44       | ✓          |  |  |  |  |  |  |  |  |
|       | 45       | ✓          |  |  |  |  |  |  |  |  |
|       | 46       | ✓          |  |  |  |  |  |  |  |  |
|       | 47       | ✓          |  |  |  |  |  |  |  |  |
|       | 48       | ✓          |  |  |  |  |  |  |  |  |
|       | 49       | ✓          |  |  |  |  |  |  |  |  |
|       | 50       | ✓          |  |  |  |  |  |  |  |  |
|       | 51       | ✓          |  |  |  |  |  |  |  |  |
|       | 52       | ✓          |  |  |  |  |  |  |  |  |
|       | 53       | ✓          |  |  |  |  |  |  |  |  |
|       | 54       | ✓          |  |  |  |  |  |  |  |  |
|       | 55       | ✓          |  |  |  |  |  |  |  |  |
|       | 56       | ✓          |  |  |  |  |  |  |  |  |
|       | 57       | ✓          |  |  |  |  |  |  |  |  |
|       | 58       | ✓          |  |  |  |  |  |  |  |  |
|       | 59       | ✓          |  |  |  |  |  |  |  |  |
|       | 60       | ✓          |  |  |  |  |  |  |  |  |
|       | 61       | ✓          |  |  |  |  |  |  |  |  |
|       | 62       | ✓          |  |  |  |  |  |  |  |  |
|       | 63       | ✓          |  |  |  |  |  |  |  |  |
|       | 64       | ✓          |  |  |  |  |  |  |  |  |
|       | 65       | ✓          |  |  |  |  |  |  |  |  |
|       | 66       | ✓          |  |  |  |  |  |  |  |  |
|       | 67       | ✓          |  |  |  |  |  |  |  |  |
|       | 68       | ✓          |  |  |  |  |  |  |  |  |

|                                                                                                          |                                              |                                                               |
|----------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------------------------|
| <b>Search Notes</b><br> | <b>Application/Control No.</b><br>17/582,797 | <b>Applicant(s)/Patent Under Reexamination</b><br>Chen et al. |
|                                                                                                          | <b>Examiner</b><br>HASHEM FARROKH            | <b>Art Unit</b><br>2138                                       |

| CPC - Searched*                                                                                                                                                                                                                                                              |            |          |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------|
| Symbol                                                                                                                                                                                                                                                                       | Date       | Examiner |
| G06F1/185 OR G06F12/0246 OR G06F12/0638 OR G06F13/1694<br>OR G06F13/28 OR G06F13/4027 OR G06F13/4243 OR G06F2212/<br>205 OR G06F2212/7208 OR G06F3/0613 OR G06F3/0659 OR<br>G06F3/0685 OR G11C11/005 OR G11C11/409 OR G11C14/0018<br>OR G11C16/10 OR G11C7/1072 OR Y02D10/00 | 10/06/2022 | HF       |

| CPC Combination Sets - Searched* |      |          |
|----------------------------------|------|----------|
| Symbol                           | Date | Examiner |
|                                  |      |          |

| US Classification - Searched* |          |            |          |
|-------------------------------|----------|------------|----------|
| Class                         | Subclass | Date       | Examiner |
| 711                           | 110      | 10/06/2022 | HF       |
| 711                           | 110      | 11/01/2023 | HF       |

\* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

|                                                     |  |
|-----------------------------------------------------|--|
| /HASHEM FARROKH/<br>Primary Examiner, Art Unit 2138 |  |
|-----------------------------------------------------|--|

|                                                                                                                 |                                              |                                                               |
|-----------------------------------------------------------------------------------------------------------------|----------------------------------------------|---------------------------------------------------------------|
| <b><i>Search Notes</i></b><br> | <b>Application/Control No.</b><br>17/582,797 | <b>Applicant(s)/Patent Under Reexamination</b><br>Chen et al. |
|                                                                                                                 | <b>Examiner</b><br>HASHEM FARROKH            | <b>Art Unit</b><br>2138                                       |

| <b>Search Notes</b>                  |             |                 |
|--------------------------------------|-------------|-----------------|
| <b>Search Notes</b>                  | <b>Date</b> | <b>Examiner</b> |
| Inventor/Assignee Search             | 10/06/2022  | HF              |
| EAST Text, CPC, FACET Search         | 10/06/2022  | HF              |
| IP Search                            | 10/06/2022  | HF              |
| Google Search                        | 10/06/2022  | HF              |
| Inventor/Assignee Search Updated     | 07/07/2023  | HF              |
| EAST Text, CPC, FACET Search Updated | 07/07/2023  | HF              |
| Inventor/Assignee Search Updated     | 10/31/2023  | HF              |
| EAST Text, CPC, FACET Search Updated | 10/31/2023  | HF              |
| Inventor/Assignee Search Updated     | 02/22/2024  | HF              |
| EAST Text, CPC, FACET Search Updated | 02/22/2024  | HF              |
| Inventor/Assignee Search Updated     | 08/05/2024  | HF              |
| EAST Text, CPC, FACET Search Updated | 08/05/2024  | HF              |
| Inventor/Assignee Search Updated     | 01/19/2025  | HF              |
| EAST Text, CPC, FACET Search Updated | 01/19/2025  | HF              |

| <b>Interference Search</b> |                              |             |                 |
|----------------------------|------------------------------|-------------|-----------------|
| <b>US Class/CPC Symbol</b> | <b>US Subclass/CPC Group</b> | <b>Date</b> | <b>Examiner</b> |
| G06F3/0685                 | G06F3/00                     | 11/01/2023  | HF              |
| G06F13/28                  | G06F13/00                    | 11/01/2023  | HF              |
| G06F2212/205               | G06F2212/00                  | 11/01/2023  | HF              |

|                                                     |  |
|-----------------------------------------------------|--|
| /HASHEM FARROKH/<br>Primary Examiner, Art Unit 2138 |  |
|-----------------------------------------------------|--|

## PE2E SEARCH - Search History (Prior Art)

| Ref # | Hits | Search Query                                                                                                                                              | DBs                                                                                                                                                                                                                                                                                                                  | Default Operator | Plurals | British Equivalents | Time Stamp          |
|-------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------|---------|---------------------|---------------------|
| L92   | 51   | ("5563838" "6351827" "6418065" "6434044" "7034569" "7161820" "7166934" "7269764" "7426649" "7613880" "7644216" "7656735" "20090020608" "20090027844").pn. | (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)                                                                                                                                                                                                                                                           | OR               | ON      | ON                  | 2024/07/01 01:19 PM |
| L93   | 2    | 92 AND (buck near5 (conver\$3 OR regulat\$3))                                                                                                             | (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)                                                                                                                                                                                                                                                           | OR               | ON      | ON                  | 2024/07/01 01:25 PM |
| L94   | 16   | ("8301833").pn.                                                                                                                                           | (US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB)                                                                                                                                                                                                                                                           | OR               | ON      | ON                  | 2024/07/01 03:47 PM |
| L95   | 4    | ("11232054").pn.                                                                                                                                          | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR               | ON      | ON                  | 2024/07/01 05:00 PM |
| L96   | 2    | ("8874831").pn.                                                                                                                                           | (US-PGPUB; USPAT; USOCR; FIT (AU, AP, AT, BE, BG, BR, BY, CA, CH, CN, CS, CU, CZ, DD, DE, DK, EA, EE, EP, ES, FI, FR, GB, HR, HU, ID, IE, IL, IS, IT, JP, KR, LT, LU, LV, MA, OA, RU, SU, WO, MC, MD, MY, NL, NO, NZ, PH, PL, PT, RO, RS, SE, SG, SI, SK, TH, TN, TR, TW, UA, VN); FPRS; EPO; JPO; DERWENT; IBM_TDB) | OR               | ON      | ON                  | 2024/07/02 09:00 AM |
| L97   | 2    | ("8874831").pn.                                                                                                                                           | (US-PGPUB; USPAT; USOCR; FPRS; EPO;                                                                                                                                                                                                                                                                                  | OR               | ON      | ON                  | 2024/07/02 09:00 AM |

|      |      |                                                                                                                                                            |                                                                     |    |    |    |                        |
|------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|----|----|----|------------------------|
|      |      |                                                                                                                                                            | JPO; DERWENT;<br>IBM_TDB)                                           |    |    |    |                        |
| L99  | 2    | ("20060174140").pn.                                                                                                                                        | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/07/02<br>02:16 PM |
| L100 | 10   | ("7724604"<br>"20060080515"<br>"6856556").pn.                                                                                                              | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/07/02<br>02:24 PM |
| L101 | 4    | ("11232054").pn.                                                                                                                                           | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/07/03<br>10:03 AM |
| L102 | 4    | ("11232054").pn.                                                                                                                                           | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/07/30<br>10:26 AM |
| L103 | 2    | ("20070136523").pn.                                                                                                                                        | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>01:59 PM |
| L104 | 532  | periodic\$4 WITH<br>(backup OR replicat\$3<br>OR cop\$4) WITH<br>((non\$volatile OR flash)<br>near2 (memory OR<br>storage OR SSD))                         | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:30 PM |
| L105 | 2281 | periodic\$4 WITH<br>(backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3) WITH<br>((non\$volatile OR flash)<br>near2 (memory OR<br>storage OR SSD)) | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:31 PM |
| L106 | 97   | 105 AND (trigger\$3<br>near5 signal)                                                                                                                       | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:31 PM |
| L107 | 0    | 97 AND<br>(@ad<"20070601")                                                                                                                                 | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:32 PM |
| L108 | 410  | 105 AND<br>(@ad<"20070601")                                                                                                                                | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:32 PM |
| L109 | 13   | 106 AND<br>(@ad<"20070601")                                                                                                                                | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>02:33 PM |
| L110 | 55   | (backup OR replicat\$3<br>OR cop\$4 OR writ\$4                                                                                                             | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;                              | OR | ON | ON | 2024/08/02<br>04:48 PM |

|      |     |                                                                                                                                                                                                              |                                                                     |    |    |    |                        |
|------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|----|----|----|------------------------|
|      |     | OR sav\$3) WITH<br>((non\$volatile OR flash)<br>near2 (memory OR<br>storage OR SSD))<br>WITH milli\$1second                                                                                                  | JPO; DERWENT;<br>IBM_TDB)                                           |    |    |    |                        |
| L111 | 24  | 110 AND<br>(@ad<"20070601")                                                                                                                                                                                  | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:48 PM |
| L112 | 530 | (backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3 OR stor\$2)<br>WITH ((non\$volatile OR<br>flash) near2 (memory<br>OR storage OR SSD))<br>WITH (every OR each)<br>near5 (milli\$1second<br>OR ms) | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:51 PM |
| L113 | 143 | 112 AND<br>(@ad<"20070601")                                                                                                                                                                                  | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:52 PM |
| L114 | 71  | (backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3 OR stor\$2)<br>WITH ((non\$volatile OR<br>flash) near2 (memory<br>OR storage OR SSD))<br>WITH (every OR each)<br>ADJ (milli\$1second OR<br>ms)   | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:53 PM |
| L115 | 14  | 114 AND<br>(@ad<"20070601")                                                                                                                                                                                  | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:54 PM |
| L116 | 6   | (backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3 OR stor\$2)<br>WITH ((non\$volatile OR<br>flash) near2 (memory<br>OR storage OR SSD))<br>WITH (every OR each)<br>ADJ (milli\$1second)            | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:55 PM |
| L117 | 0   | 116 AND<br>(@ad<"20070601")                                                                                                                                                                                  | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>04:55 PM |
| L118 | 0   | periodic\$4 WITH<br>(backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3) WITH<br>((non\$volatile OR flash)<br>near2 (memory OR<br>storage OR SSD))                                                   | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON | ON | 2024/08/02<br>05:09 PM |



|      |     |                                                                                                                                                                           |                                                                     |    |     |    |                        |
|------|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|----|-----|----|------------------------|
|      |     | WITH millisecond                                                                                                                                                          |                                                                     |    |     |    |                        |
| L119 | 145 | periodic\$4 WITH<br>(backup OR replicat\$3<br>OR cop\$4 OR writ\$4<br>OR sav\$3) WITH<br>((non\$volatile OR flash)<br>near2 (memory OR<br>storage OR SSD))<br>WITH second | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:09 PM |
| L120 | 26  | 119 AND<br>(@ad<"20070601")                                                                                                                                               | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:09 PM |
| L121 | 0   | 120 AND dimm                                                                                                                                                              | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:19 PM |
| L122 | 19  | "backup may occur<br>every millisecond"                                                                                                                                   | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:39 PM |
| L123 | 0   | 122 AND<br>(@ad<"20070601")                                                                                                                                               | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:39 PM |
| L124 | 19  | (backup near5 occur<br>near5 every near5<br>millisecond)                                                                                                                  | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:40 PM |
| L125 | 19  | (backup near5 occur<br>near5 (every OR each<br>OR one) near5<br>millisecond)                                                                                              | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | ON  | ON | 2024/08/02<br>05:41 PM |
| L126 | 31  | (buck ADJ converters)<br>SAME (regulat\$3 near2<br>voltage) SAME ((printed<br>ADJ circuit ADJ board)<br>OR PCB)                                                           | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | OFF | ON | 2024/08/05<br>08:32 AM |
| L127 | 3   | ((buck ADJ converters)<br>SAME (regulat\$3 near2<br>voltage) SAME ((printed<br>ADJ circuit ADJ board)<br>OR PCB)).clm.                                                    | (US-PGPUB; USPAT;<br>USOCR; FPRS; EPO;<br>JPO; DERWENT;<br>IBM_TDB) | OR | OFF | ON | 2024/08/05<br>08:32 AM |
| L128 | 3   | 127 AND ("BHAKTA;<br>JAYESH".ine. OR<br>"CHEN; CHI-SHE".ine.<br>OR "MILTON; SCOTT<br>H.".ine. OR<br>"SOLOMON; JEFFREY<br>C.".ine.)                                        | (US-PGPUB; USPAT;<br>USOCR; IBM_TDB)                                | OR | ON  | ON | 2024/08/05<br>08:33 AM |
| L129 | 5   | 126 AND ("NETLIST,<br>INC.".ase.)                                                                                                                                         | (US-PGPUB; USPAT;<br>USOCR; IBM_TDB)                                | OR | ON  | ON | 2024/08/05<br>08:34 AM |
| L130 | 6   | 126 AND ((G06F1/185                                                                                                                                                       | (US-PGPUB; USPAT;                                                   | OR | ON  | ON | 2024/08/05             |

|  |  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                 |  |  |  |          |
|--|--|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--|--|--|----------|
|  |  | OR G06F12/0246 OR<br>G06F12/0638 OR<br>G06F13/1694 OR<br>G06F13/28 OR<br>G06F13/4027 OR<br>G06F13/4243 OR<br>G06F2212/205 OR<br>G06F2212/7208 OR<br>G06F3/0613 OR<br>G06F3/0659 OR<br>G06F3/0685 OR<br>G11C11/005 OR<br>G11C11/409 OR<br>G11C14/0018 OR<br>G11C16/10 OR<br>G11C7/1072 OR<br>Y02D10/00).cpc. OR<br>(711/110).ccls. OR<br>(G06F1/18 OR<br>G06F12/02 OR<br>G06F12/06 OR<br>G06F13/16 OR<br>G06F13/28 OR<br>G06F13/40 OR<br>G06F13/42 OR<br>G06F3/06 OR<br>G11C14/00 OR<br>G11C7/10).ipc.) | USOCR; IBM_TDB) |  |  |  | 08:35 AM |
|--|--|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|--|--|--|----------|

PE2E SEARCH - Search History (Interference)

There are no Interference searches to show.

|                                                                                                     |                        |                |            |
|-----------------------------------------------------------------------------------------------------|------------------------|----------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                | 17582797   |
|                                                                                                     | Filing Date            |                | 2022-01-24 |
|                                                                                                     | First Named Inventor   | Chi-She Chen   |            |
|                                                                                                     | Art Unit               | 2138           |            |
|                                                                                                     | Examiner Name          | HASHEM FARROKH |            |
|                                                                                                     | Attorney Docket Number | 022955-000090  |            |

| U.S.PATENTS       |         |               |                        |            |                                                 |                                                                        | Remove |
|-------------------|---------|---------------|------------------------|------------|-------------------------------------------------|------------------------------------------------------------------------|--------|
| Examiner Initial* | Cite No | Patent Number | Kind Code <sup>1</sup> | Issue Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |        |
|                   | 1       |               |                        |            |                                                 |                                                                        |        |

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| Examiner Initial*                   | Cite No | Publication Number | Kind Code <sup>1</sup> | Publication Date | Name of Patentee or Applicant of cited Document | Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear |        |
|                                     | 1       |                    |                        |                  |                                                 |                                                                        |        |

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|                                                                                                     | Filing Date            |                | 2022-01-24 |
|                                                                                                     | First Named Inventor   | Chi-She Chen   |            |
|                                                                                                     | Art Unit               | 2138           |            |
|                                                                                                     | Examiner Name          | HASHEM FARROKH |            |
|                                                                                                     | Attorney Docket Number | 022955-000090  |            |

|   |                                                                                                                                                                            |                          |
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|                                                                                                     | Attorney Docket Number | 022955-000090  |            |

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| Signature  | /Khaled Shami/ | Date (YYYY-MM-DD)   | 2024-10-01 |
| Name/Print | Khaled Shami   | Registration Number | 38745      |

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| 13 | Keller, S. J. (2006). The Physical Design of the ILLIAC 6 Supercomputing Platform (Doctoral dissertation, University of Illinois at Urbana-Champaign). See pages 12, 13 & highlighted sections.                                                                                                                                                                                     | <input type="checkbox"/> |
| 14 | Interstill (2004). Power Management Application Guide for Altera FPGAs. Retrieved from <a href="https://www.datasheetarchive.com/pdf/download.php?id=c9facaf95737a8327c7217bff086b497d4f48&amp;type=P&amp;term=buck%2520SDRAM">https://www.datasheetarchive.com/pdf/download.php?id=c9facaf95737a8327c7217bff086b497d4f48&amp;type=P&amp;term=buck%2520SDRAM</a> . See pages 4 & 9. | <input type="checkbox"/> |
| 15 | Summit (2006). Application Note 59. Retrieved from <a href="https://www.datasheetarchive.com/pdf/download.php?id=a7ccb0edb0c2b62d33ea2ca63eeb31b0884da8&amp;type=P&amp;term=buck%2520SDRAM">https://www.datasheetarchive.com/pdf/download.php?id=a7ccb0edb0c2b62d33ea2ca63eeb31b0884da8&amp;type=P&amp;term=buck%2520SDRAM</a> . See pages 1, 3 & 4.                                | <input type="checkbox"/> |
| 16 | <del>National Semiconductor (2007). Application note AN-1600. Retrieved from <a href="https://www.datasheetarchive.com/pdf/download.php?id=c08bde6d6162bdd65a909e9aa5fbce116b8c2c&amp;type=P&amp;term=buck%2520SDRAM">https://www.datasheetarchive.com/pdf/download.php?id=c08bde6d6162bdd65a909e9aa5fbce116b8c2c&amp;type=P&amp;term=buck%2520SDRAM</a>. See page 2.</del>         | <input type="checkbox"/> |
| 17 | Analog Devices (2006). TigerSHARC Embedded Processor ADSP-TS201S.                                                                                                                                                                                                                                                                                                                   | <input type="checkbox"/> |
| 18 | Renesas (2005). ISL6531 Datasheet.                                                                                                                                                                                                                                                                                                                                                  | <input type="checkbox"/> |
| 19 | Texas Instruments (2001). Designing for Small-Size, High Frequency Applications Using TPS546xx DC/DC Converters.                                                                                                                                                                                                                                                                    | <input type="checkbox"/> |
| 20 | Intersil (2002). Powering DDR Memory in Desktop Computers and Datacomm Systems. Retrieved from <a href="https://datasheet.datasheetarchive.com/originals/library/Datasheet-02/DSA0031945.pdf">https://datasheet.datasheetarchive.com/originals/library/Datasheet-02/DSA0031945.pdf</a>                                                                                              | <input type="checkbox"/> |
| 21 | Intel (2002). Mobile Intel® Pentium® 4 Processor-M and Intel® 845MP/845MZ Chipset Platform Design Guide.                                                                                                                                                                                                                                                                            | <input type="checkbox"/> |

**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**  
( Not for submission under 37 CFR 1.99)

|                        |               |
|------------------------|---------------|
| Application Number     | 17582797      |
| Filing Date            | 2022-01-24    |
| First Named Inventor   | CHEN          |
| Art Unit               | 2138          |
| Examiner Name          | FARROKH       |
| Attorney Docket Number | 022955-000090 |

|    |                                                                                                                                                                                                                                                                                                                          |                          |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| 22 | Asus (2001). A7V133 A7V133-C jumperfree PC133/VC133 200/266MHz FSB AGP Pro/4X Socket A Motherboard User's Manual.                                                                                                                                                                                                        | <input type="checkbox"/> |
| 23 | Trescases, O. (2007). Integrated Power-Supplies for Portable Applications.                                                                                                                                                                                                                                               | <input type="checkbox"/> |
| 24 | Van Schaik, C. F. (2002). The Development of a Node for a Hardware Reconfigurable Parallel Processor (Master's thesis, University of Cape Town).                                                                                                                                                                         | <input type="checkbox"/> |
| 25 | <del>Boroyevich, D. (2004). Power Electronics Building Blocks, "Plug-and-Play", Hardware and Software Control Architectures. VIRGINIA POLYTECHNIC INST AND STATE UNIV BLACKSBURG OFFICE OF SPONSORED PROGRAMS.</del>                                                                                                     | <input type="checkbox"/> |
| 26 | McPartland, R. J., Loeper, D. J., Higgins, F. P., Singh, R., MacDonald, G., Komoriya, G., ... & Leung, C. W. (2000, May). SRAM Embedded Memory with Low Cost, FLASH EEPROM-Switch-Controlled Redundancy. In Proceedings of the IEEE 2000 Custom Integrated Circuits Conference (Cat. No. 00CH37044) (pp. 287-289). IEEE. | <input type="checkbox"/> |
| 27 | Crisp, R. (1997). Direct Rambus Technology: The New Main Memory Standard. IEEE Micro, 17(6), 18-28. PC2-4200/PC2-3200 DDR2                                                                                                                                                                                               | <input type="checkbox"/> |
| 28 | PC2-4200/PC2-3200 DDR2 Registered Mini-DIMM. (December 2006). Design Spec Rev. 2.0. Retrievable from <a href="https://www.jedec.org/standards-documents/docs/module-42014">https://www.jedec.org/standards-documents/docs/module-42014</a>                                                                               | <input type="checkbox"/> |

If you wish to add additional non-patent literature document citation information please click the Add button

**EXAMINER SIGNATURE**

|                    |                  |                 |            |
|--------------------|------------------|-----------------|------------|
| Examiner Signature | /HASHEM FARROKH/ | Date Considered | 01/16/2025 |
|--------------------|------------------|-----------------|------------|

\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

<sup>1</sup> See Kind Codes of USPTO Patent Documents at [www.USPTO.GOV](http://www.USPTO.GOV) or MPEP 901.04. <sup>2</sup> Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>3</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>4</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. <sup>5</sup> Applicant is to place a check mark here if English language translation is attached.

|                                                                                                     |                        |               |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |               | 17582797   |
|                                                                                                     | Filing Date            |               | 2022-01-24 |
|                                                                                                     | First Named Inventor   | CHEN          |            |
|                                                                                                     | Art Unit               | 2138          |            |
|                                                                                                     | Examiner Name          | FARROKH       |            |
|                                                                                                     | Attorney Docket Number | 022955-000090 |            |

### CERTIFICATION STATEMENT

Please see 37 CFR 1.97(e) to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

**OR**

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☒ A certification statement is not submitted herewith.

### FEE

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

### COPIES

☐ An identification of an earlier application pursuant to 37 CFR 1.98 (d) (1) is attached.

### SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

|            |                |                     |            |
|------------|----------------|---------------------|------------|
| Signature  | /Khaled Shami/ | Date (YYYY-MM-DD)   | 2024-09-24 |
| Name/Print | Khaled Shami   | Registration Number | 38745      |

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.





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| APPLICATION NO.                     | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-------------------------------------|-------------|----------------------|---------------------|------------------|
| 17/582,797                          | 01/24/2022  | Chi-She Chen         | 022955-000090       | 3546             |
| 151145                              | 7590        | 01/24/2025           | EXAMINER            |                  |
| Vorys, Sater, Seymour and Pease LLP |             |                      | FARROKH, HASHEM     |                  |
| 1909 K Street, NW                   |             |                      | ART UNIT            |                  |
| 9th Floor                           |             |                      | PAPER NUMBER        |                  |
| Washington, DC 20006-1152           |             |                      | 2138                |                  |
|                                     |             |                      | NOTIFICATION DATE   |                  |
|                                     |             |                      | DELIVERY MODE       |                  |
|                                     |             |                      | 01/24/2025          |                  |
|                                     |             |                      | ELECTRONIC          |                  |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com  
mvmessinger@vorys.com  
vorys\_docketing@cardinal-ip.com



**DETAIL ACTION**

**Notice of Pre-AIA or AIA Status**

1. *The present application, filed on or after March 16, 2013, is being examined under the first inventor to file provisions of the AIA.*
2. *This office action is in response to the communication filed on 10/01/2024. There are a total of 42 claims pending in the application. Claim 2 has been amended; claims 1 and 3-27 have been canceled; and claims 28-68 have been added.*

**INFORMATION CONCERNING IDS:**

3. *The information disclosure statements (IDS') submitted on 09/24/2024 and 10/01/2024 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the Examiner. The IDS listed documents marked by lined-through have not been considered by the Examiner, because a copy documents have not been provided.*

**INFORMATION CONCERNING CLAIMS:**

**Claim Rejections - 35 USC § 112**

*The following is a quotation of the first paragraph of 35 U.S.C. 112(a):*

*(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.*

*The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:*

*The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.*

4. *Claims 2 and 28-68 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.*

*The independent claim 2 recites, in part, the limitation(s):*

- “the memory-socket including a set of power conduits, a set of data conduits including at least 72 data conduits, and a set of address and control conduits”.
  
- “a 1-bit wide double data rate (DDR) data signal is electrically conducted between the system board”
  
- “wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines”
  
- “in response to the detected trigger condition, the logic element is configured to perform a plurality of write operations, including: a first write operation to write a first set of data bits into a first portion of the data storage element; a second write

operation to write a second set of data bits into a second portion of the data storage element; and subsequently a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;”

- “the trigger condition occurs when the input voltage goes above both the first and second threshold voltages”
- “wherein: a specified operating voltage value is within a range of operating voltage values of the DIMM, the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value”
- “each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the system board”
- “wherein, when the system power is provided to the DIMM from the system board:

the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein: a specified operating voltage value is within a range of operating voltage values of the DIMM,  
the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value

- "when the system power is provided to the DIMM from the system board:  
the first and second groups of DDR SDRAM packages are configured to be **accessible and not in self-refresh mode**;

the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and

the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits."

*The claimed specification fails to describe/support the limitation(s) as claimed.*

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5. *Independent claims 44 and 58 recite similar limitations as presented above with respect to the independent claim 2.*

6. *Dependent claims 28-43, 45-67 and 68 are rejected at least by virtue their dependency from their respected claim.*

**35 USC 112(b) or 35 USC 112 (pre-AIA), Second Paragraph**

*The following is a quotation of 35 U.S.C. 112(b):*

*(b) CONCLUSION.—The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the inventor or a joint inventor regards as the invention.*

*The following is a quotation of 35 U.S.C. 112 (pre-AIA), second paragraph:*

*The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.*

*Claims 2, 44, and 58 are rejected under 35 U.S.C. 112(b) or 35 U.S.C. 112 (pre-AIA), second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the inventor or a joint inventor (or for applications subject to pre-AIA 35 U.S.C. 112, the applicant), regards as the invention.*

7. *The independent claim 2, in part, recite the limitation:*

*“trigger condition occurs when the **input voltage goes above both the first and second threshold voltages**” (emphasis added).*

*The specification appears to recite trigger condition occurs when input voltage is above a first threshold voltage and below a second threshold votage.*

8. *The independent claim 2, in part, recite the limitation:*

“the first and second groups of DDR SDRAM packages are configured to be **accessible and not in self-refresh mode**” (*emphasis added*).

*It is not clear what is meant by phrase “accessible and not self-refresh mode”.*

*Does that mean that both groups may be in self-refresh and no access to either group possible or only one group at a time can be in the self-refresh mode?*

*The independent claims 44 and 58 recites a similar limitations and are rejected on the same ground of limitations. The dependent claims 28-43, 45-57, and 59-68 are rejected at least based on their dependency from their respected independent claims.*

### **Response to Remarks**

*Applicant arguments have been fully considered but they have not been persuasive. Page 22-27 of the Remarks recites the newly amended independent claim 2. Page 27-28 recite the status of claim rejection as related to previous office action. On page 30-31, the Remarks make references to ¶ 0002 of Harris. The ¶ 0002 of Harris is background portion of the specification (e.g., refers to related art prior to Harris invention). ¶ 0003 Harris discusses the solution is a power distributed system in which the DIMM modules (e.g., board) receives external input voltage and generate a plurality of on-board regulated voltages to be supplied or provided to memory devices (e.g., DIMMs, see paragraph ¶ 0009 of Harris). Contrary to the Applicant arguments, the external input voltage regulated by VRM module 102 and supplied to the DRAM devices 110-1 to 110-N (e.g., DIMM, see ¶ 0009 and Figs. 1A and 1b of Harris) . In addition Harris DIMM may comprise any type of Double Data Rate (DDR) devices. Page 33 of*



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*the Remarks recites ¶ 0019 of the Remarks and highlight some portions of the paragraph and concludes that Harris cannot read on claim 2. Applicant argues:*

**“As the Office Action acknowledges, the memory module 100A of Harris receives its power through an external source. (“Fig. 1B Harris shows a block diagram of memory module 100B comprising DRAM devices 110, inputs a plurality voltages 120 from external (sic) source and generates a plurality of regulated voltages 106 and 108,”** Office Action, p. 5, 11. 3-5, emphasis added).

**Applicant respectfully maintains that Harris expressly teaches away from providing power to any memory module assembly via the memory socket from the system board of the computer system.”** (*Emphasis added, bolded portion*).

*The Examiner respectfully disagrees. Fig. 1A or 1B Harris teaches receiving input voltage(s) from an external voltage source (line(s) of 104 or 120s) and converting to the regulated voltages Vdd 108 and Vcc 106 using the voltage regulator module 102. Fig. 1B of Harris shows receiving voltages from a plurality of external voltage sources (e.g., lines), and converting to the regulated voltages Vdd 108 and Vcc 104 using a plurality of voltage regulator modules 122 (and logic 124). Harris discloses:*

**“[0014] FIG. 1B is a block diagram of voltage distribution system for a memory module 100B according to another embodiment. It should be apparent to one skilled in the art that the voltage distribution system for memory module 100B is essentially similar to the system shown in FIG. 1A, but for the redundancy implementation of local voltage conversion. A plurality of on-board VRMs 122-K, K=1, 2, . . . , N, are provided as part of the memory assembly/module 100B wherein each VRM is operable with an independent voltage supply path for locally converting an external supply voltage into appropriate local voltage levels. Reference numerals 120-1 through 120-K refer to K supply voltage paths which may be coupled to various voltage sources provided within the electronic system (e.g., a computer system) (not shown). It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore**

**unknown voltage supplies, either regulated or unregulated, and even including variable voltages.**

[0015] A **suitable logic module 124 is provided for selecting among the plurality of like voltage outputs from the VRMs 122-K in order to energize the V.sub.dd and V.sub.cc paths 108, 106, respectively.** In one implementation, a wired-OR arrangement is operable to **select from K voltage outputs (e.g., from K V.sub.dd outputs or from K V.sub.cc outputs) to power the appropriate local voltage supply path, i.e., the V.sub.dd and V.sub.cc paths.** As described previously, the V.sub.dd path 108 is coupled to each of the DRAM devices 110-1 through 110-N and the V.sub.cc path 106 is coupled to the buffer/logic component 112 of the memory assembly module 100B.” (Pars. 0014-0015, *emphasis added*).

*Fig. 3 of Harris shows a plurality of DIMM board or module with withs a plurality edge pins to be attached or coupled to memory controller via DIMM connector (.e.g., Par. 0019 OF Harris). Fig. 4 of Harris shows a computer system 400 comprising a plurality of memory modules 410 connected to memory controller 408 via memory link 411. Fig. 4 also shows that each of memory module comprise a local voltage regulator 412 for receiving input voltage from the external memory controller and converting it to regulated voltages used by each DIMM module of the plurality of DIMM modules. As showed in Figs. 3-4 of Harris, all of the communication between the computer system and the memory modules including external power voltage source or lines provided via edge pins and the DIMM connectors. Applicant argues that Harris expressly teaches away, apparently assuming that that there is no socket (e.g., connector). Applicant make numerous references to ¶ 0002 of Harris, which, as noted above, is a portion of background information. The Examiner respectfully disagrees with the Applicant that Harris teaches away, even if power was not provided through connector (e.g., socket). Harris teaches external voltage(s) are received by DIMM boards or modules and converted to regulated voltage(s) required by operating DIMMs.*

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*Page 28 of the Remarks states “support for all of the below amendments has been provided in the attachment accompanying this paper. The support is provided by claim number in a table within the attachment.” The Examiner respectfully submits that no support provided for the newly added amendments. The support means that the claimed specification describes/supports by pointing to portion(s) of the specification that describes/supports the newly added limitations. There is no table within the provided applicant’s Remarks that relates the limitations to claimed specification. Applicant describes various limitations in the claims without referring to the portions of specification that describes or supports them. The rejections under 35 USC 112, indicate at least some of the added new limitation not described/supported as is required to comply with written description requirement.*

*The arguments regarding the limitations associated with self-refresh subject is a newly introduced subject matter is considered moot. Although, as rejected under 112, there are some ambiguities in claim limitations that need clarification or modification.*

*Regarding the plurality Buck converted and voltage values, as previously noted, Harris teaches one or more regulated supply (e.g., Figs. 1A and 1B of Harris) to provide regulated voltages used by DIMM. The information regarding the type of voltage regulators such as buck converters and specific voltage values, as referred to in the previous office action, has been provided in the document “Trial Termination or final written description” or “Trial-Term”. For example page 23 of trial teaches how to combine (e.g., map) the teaching of Harris and FBDIMM standards to achieve require voltage values. The Trial-Term documents also describes that single and dual package*

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*buck converters were available before the time the Harris' invention filed, one having ordinary in the art would have been motivated to modify the DIMM board or module taught by Harris to include buck converters as voltage regulators. Regarding triggering voltage variation or fault, the combination of references should be considered.*

*For example, Harris teaches a power system supply voltage of +12V with a wide tolerance +/-15%. For an input supply source voltage 12V with +/-15%, The voltage range for DIMM to properly operates is from 10V to 13.8V. It means the DIMM module with an operating voltage  $\leq 10.2$  or an operating voltage  $\geq 13.8$  may fail (e.g., causes triggering condition). Amidi teaches a variation in a power supply may be detected and means has been provided to switch to the backup power supply (e.g., see claim 19, Figs. 5-6 of Amidi). In summary, the Examiner respectfully submit that combination or reference relied on previous office action teach or render obvious the pre-amended limitations. The current set of claims (e.g., newly amended and added claims) recite some limitations not described/supported by the claim specification.*

### **Conclusion**

*Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

*A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.*

*Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.*

*If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Tim Vo can be reached on (571)272-3642. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer*

*Art Unit: 2138*

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*/HASHEM FARROKH/*

*Primary Examiner, Art Unit 2138*



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| APPLICATION NO.                     | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 17/582,797                          | 01/24/2022  | Chi-She Chen         | 022955-000090       | 3546             |
| 151145                              | 7590        | 03/10/2025           | EXAMINER            |                  |
| Vorys, Sater, Seymour and Pease LLP |             |                      | FARROKH, HASHEM     |                  |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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|                                                     |                                      |                                    |                                                  |                              |
|-----------------------------------------------------|--------------------------------------|------------------------------------|--------------------------------------------------|------------------------------|
| <b><i>Applicant-Initiated Interview Summary</i></b> | <b>Application No.</b><br>17/582,797 | <b>Applicant(s)</b><br>Chen et al. |                                                  |                              |
|                                                     | <b>Examiner</b><br>HASHEM<br>FARROKH | <b>Art Unit</b><br>2138            | <b>AIA (First Inventor to File) Status</b><br>No | <b>Page</b><br><b>1 of 1</b> |

| <b>All Participants</b> (applicant, applicants representative, PTO personnel) | <b>Title</b>     | <b>Type</b> |
|-------------------------------------------------------------------------------|------------------|-------------|
| HASHEM FARROKH                                                                | Primary Examiner | Telephonic  |
| Khalid Shami                                                                  | Attorney         |             |

**Date of Interview:** 05 March 2025

**Issues Discussed:**

**35 U.S.C. 112**

An applicant initiated interview with (the Applicant Mr. Khaled Shami Reg. # 38,745), was conducted on 03/05/2025. The interview was in response to the previous office action mailed 01/24/2025. The purpose of the interview was to clarify the rejections under 35 USC 112(a) first paragraph, as not complying with written description requirement. During the interview, agreement reached that applicant would provide a table that map claims limitations to the portions of the claimed specification that describe/support them.

☒ Attachment

|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |  |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|
| /HASHEM FARROKH/<br>Primary Examiner, Art Unit 2138                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |  |
| <p><b>Applicant is reminded that a complete written statement as to the substance of the interview must be made of record in the application file. It is the applicants responsibility to provide the written statement, unless the interview was initiated by the Examiner and the Examiner has indicated that a written summary will be provided. See MPEP 713.04</b></p> <p>Please further see:<br/>MPEP 713.04<br/>Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews, paragraph (b)<br/>37 CFR § 1.2 Business to be transacted in writing</p> |  |

**Applicant recordation instructions:** The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview.

**Examiner recordation instructions:** Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.



FOR DISCUSSION PURPOSES ONLY

Proposed Claim Amendments (Marked-Up)

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket~~ slot connector of a system board of a ~~host computer~~ system, the memory ~~socket~~ slot connector including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board;~~ a 1 bit wide double data rate (DDR) data signal ~~signals is electrically conducted between the system board~~ host system and the DIMM ~~are transferred via the memory socket by each data conduit of the set of data conduits, and address and control signals are delivered electrically conducted from the host system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:~~

~~a printed circuit board (PCB) having a form factor with a width dimension and a height dimension, the PCB including:~~

~~an interface~~ having edge connections ~~disposed along the width dimension and~~ configured to fit into the memory ~~socket~~ slot connector of the host system, the edge connections including:

a first set of edge connections configured to be electrically connected to ~~respective power conduits of the set of power conduits and operable to deliver to the DIMM power from power rails of at the host system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM;~~

a second set of edge connections ~~each of which~~ is configured to ~~electrically conduct a 1 bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and~~

a third set of edge connections configured to be electrically connected to

respective address and control conduits of the set of address and control conduits[[:]]

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM, ~~the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board;~~

a set of data lines electrically ~~coupled~~ connected to respective edge connections of the second set of edge connections, wherein each data line of the set of data lines is configured to electrically conduct a 1 bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and

a set of address and control lines electrically ~~coupled~~ connected to respective edge connections of the third set of edge connections and configured to electrically conduct address and control signals;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and ~~electrically connected to the~~ to an input voltage supply line of the set of voltage supply lines, the controller configured to receive the input voltage via the input voltage supply line, the controller including:

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits;~~

~~a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and~~

~~a voltage monitor circuit electrically connected to the input voltage supply line and coupled to the logic element, the voltage monitor circuit configured to: (i) monitor and compare the input voltage supplied via the input voltage supply line to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and (ii) generate a trigger signal upon detecting~~ detect a trigger condition; and (iii) transmit the trigger signal to

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at least one other portion of the controller, wherein the controller is configured to perform, in response to the detected trigger condition signal, the logic element is configured to perform a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations;

wherein, when the system power is provided to the DIMM from the system board:

the trigger condition occurs when the input voltage exceeds a first threshold voltage goes above both the first and second threshold voltages; and

wherein:

a specified operating voltage value is within a range of operating voltage values of the DIMM;

the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value;

the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value;

the first threshold voltage corresponds to the lower operating voltage value; and

the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR-SDRAM) packages devices coupled to the set of address and control lines and to the set of data lines, each the DDR SDRAM package of the plurality of DDR-SDRAM packages having a bit width of m bits and configured devices being operable to receive or output m-1 bit wide DDR data signals via respective m data lines of the set of data lines in response to based on address and control signals

received ~~from the host system via address and control lines of the set of address and control lines, wherein m is equal to four or eight; and~~

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line; ~~and each of the first, second, third, and fourth converter circuits configured to, in response to the detected trigger condition, receive power supplied by the input voltage supply line when the system power is provided to the DIMM from the input voltage supply line and to deliver power system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively,~~

~~wherein the set of components includes~~including:

a first component ~~configured to receive power via at least electrically connected to the first regulated voltage line and powered by the first regulated voltage when the system power is provided to the DIMM from the system board;~~

a second component ~~configured to receive power via at least electrically connected to the second regulated voltage line and powered by the second regulated voltage when the system power is provided to the DIMM from the system board;~~

a third component ~~configured to receive power via at least electrically connected to the third regulated voltage line and powered by the third regulated voltage when the system power is provided to the DIMM from the system board; and~~

a fourth component electrically ~~configured to receive power via at least connected to the fourth regulated voltage line and powered by the fourth regulated voltage when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) ~~receives power when the system power is provided to the DIMM from the system board, is powered;~~

only by one or more of the first, second, third, and fourth converter circuits; and only via the one or more of the first, second, third, and fourth regulated voltage lines;

~~wherein the DIMM is configurable to operate in any of a plurality of states including a first state and a second state, wherein the controller is further configured to control power delivery to one or more components of the set of components for the DIMM to operate in the first state or the second state, whereby power to the set of components via the first, second, third, and fourth regulated voltage lines is turned on when the DIMM is operating in the first state, and whereby power to the first component via the first regulated voltage line is turned off and power to the second, third, and fourth components via the second, third and fourth regulated voltage lines is turned on when the DIMM is operating in the second state~~

~~wherein the plurality of DDR SDRAM packages includes:~~

~~a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;~~

~~a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and~~

~~when the system power is provided to the DIMM from the system board:~~

- ~~• the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;~~
- ~~• the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and~~
- ~~• the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data~~

~~signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and~~

- ~~• wherein the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.~~

3 – 27. (Canceled)

~~28.~~ (Currently Amended) The DIMM of claim 2, wherein the ~~second component is~~ further connected to the first regulated voltage line and is powered by the first and second regulated voltages when the system power is provided to the DIMM from the system board plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;
- the at least 40 1-bit wide DDR data signals include at least 32 1-bit

wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals; and

the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

29. (Currently Amended) The DIMM of claim 2, wherein the controller further includes:  
data storage element is a buffer configured to store the plurality of data bits or a First In First Out (FIFO) buffer configured to store the plurality of data bits.

a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Currently Amended) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage, the PCB has a form factor with a width and a height dimension, and wherein the width dimension is 133.35 millimeters.

31. (Currently Amended) The DIMM of claim 30, wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages, the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.

32. (Currently Amended) The DIMM of claim 312, wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based

~~on a combination of the first and second sets of data bits written during the first and second write operations, a specified operating voltage value is within a range of operating voltage values of the DIMM.~~

33. (Currently Amended) The DIMM of claim ~~32~~, wherein, ~~prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations, the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM.~~

34. (Currently Amended) The DIMM of claim 2, wherein, when power from the power rails of the host system is provided to the DIMM~~the system power is provided to the DIMM from the system board~~, the nonvolatile memory is not powered using the first regulated voltage.

35. (Currently Amended) The DIMM of claim ~~2~~ 29, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger ~~condition~~signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger ~~condition~~signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Currently Amended) The DIMM of claim ~~235~~, wherein, ~~prior to performing the third write operation, the logic element is further configured to perform (i) a first read operation of the plurality of read operations to read the first set of data bits from the first portion of the data storage element, and (ii) a second read operation of the plurality of read operations to read the second set of data bits from the second portion of the data storage element, and to generate the~~



~~third set of data bits based on the read first and second sets of data bits; each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.~~

38. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger ~~condition~~ signal, one or more read operations.

39. (Previously Presented) The DIMM of claim 38, wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM ~~packages~~ devices, respectively.

40. (Currently Amended) The DIMM of claim ~~33~~ 38, wherein the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value. ~~the logic element is further configured to perform (i) first and second read operations of the one or more read operations, and (ii) subsequently, the first and second write operations.~~

41. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Currently Amended) The DIMM of claim ~~29~~ 2, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits, ~~in response to the detected trigger condition,~~ the voltage monitor circuit is further configured to generate and transmit a trigger signal.

43. (Currently Amended) The DIMM of claim ~~24~~ 0, wherein, when power from the power rails of the host system is provided to the DIMM ~~the system power is provided to the DIMM from the system board~~, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket~~ slot connector of a host system board of a computer system, the memory ~~socket~~ slot connector including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board, a 1 bit wide double data rate (DDR) data signals are transferred is electrically conducted between the host system board and the DIMM via the memory socket by each data conduit of the set of data conduits, and address and control signals are delivered from the host system electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits, the DIMM comprising:~~

a printed circuit board (PCB) having ~~a form factor with a width dimension and a height dimension, the PCB~~ edge connections configured to fit into the memory slot connector of the host system, the edge connections including:

~~an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:~~

a first set of edge connections configured to be electrically connected to ~~respective power conduits~~ of the set of power conduits and operable to deliver the DIMM power from the power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM.

a second set of edge connections ~~each of which is~~ configured to ~~electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and~~

a third set of edge connections configured to be electrically connected to ~~respective address and control conduits of the set of address and control conduits~~[[:]],

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power

rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board[[:]]

a set of data lines electrically ~~coupled to respective edge connections of~~ connected to the second set of edge connections, ~~wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; and~~

a set of address and control lines electrically ~~coupled to respective edge connections of~~ electrically connected to the third set of edge connections and ~~configured to electrically conduct address and control signals;~~

a controller ~~including coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power and the input voltage via the input voltage supply line, the controller including:~~

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits; and~~

~~a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and~~

a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and electrically connected to the an input voltage supply line of the set of voltage supply lines, and coupled to the logic element; the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line; and
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller, wherein, compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage; and  
~~detect a trigger condition;~~

~~wherein, in response to the detected trigger condition, the logic element<sub>2</sub>~~  
in response to the detected trigger condition, the controller is configured to  
periodically perform<sub>2</sub> at regular intervals of time<sub>2</sub> a plurality of write operations,  
including[[:]]

a first write operation to write a first set of data bits into a first portion of  
the data storage element; and

a second write operation to write a second set of data bits into a second  
portion of the data storage element;

~~wherein, when the system power is provided to the DIMM from the system board:~~

- ~~• the trigger condition occurs when the input voltage goes above both  
the first and second threshold voltages; and~~

~~wherein:~~

- ~~• a specified operating voltage value is within a range of operating  
voltage values of the DIMM;~~
- ~~• the range of operating voltage values is bounded by an upper operating  
voltage value and a lower operating voltage value;~~
- ~~• the lower operating voltage value is below the specified operating  
voltage value of the DIMM and the upper operating voltage value is  
above the specified operating voltage value;~~
- ~~• the first threshold voltage corresponds to the lower operating voltage  
value, and~~
- ~~• the second threshold voltage corresponds to the upper operating  
voltage value;~~

a set of components coupled to the PCB, the set of components including a  
plurality of double data rate (DDR) synchronous dynamic random access memory (DDR  
SDRAM) packages-devices coupled to the set of address and control lines and to the set of  
data lines, ~~the each DDR SDRAM package of the plurality of DDR SDRAM packages~~  
~~having a bit width of m bits and configured devices being operable to receive or output m~~  
~~1-bit wide DDR data signals via respective m data lines of the set of data lines based on~~  
~~response to address and control signals received from the host system via the set of~~  
address and control lines via address and control lines of the set of address and control  
~~lines, wherein m is equal to four or eight; and~~

first, second, third, and fourth converters ~~circuits~~ coupled to the PCB and to the input voltage supply line, ~~each of the first, second, third, and fourth converter circuits~~ and configured to, ~~in response to the detected trigger condition,~~ receive power ~~supplied by~~ from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines, ~~when the system power is provided to the DIMM from the system board, the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and (ii) output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltages lines, respectively, wherein the set of components includes including:~~

a first component ~~electrically connected to the first regulated voltage line and powered by~~ configured to receive power via the first regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a second component ~~electrically connected to the second regulated voltage line and powered by~~ configured to receive power via the second regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a third component ~~electrically connected to the third regulated voltage line and powered by~~ configured to receive power via the third regulated voltage line ~~when the system power is provided to the DIMM from the system board; and~~

a fourth component ~~electrically connected to the fourth regulated voltage line and powered by~~ configured to receive power via the fourth regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power ~~when the system power is provided to the DIMM from the system board, is powered:~~

- ~~only by one or more of the first, second, third, and fourth converter circuits; and~~

only via the one or more of the first, second, third, and fourth regulated voltage

lines;

wherein the plurality of DDR SDRAM packages includes:

a first group of at least five DDR SDRAM packages that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM packages that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

when the system power is provided to the DIMM from the system board:

- the first and second groups of DDR SDRAM packages are configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output 40 1-bit wide DDR data signals in parallel via 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error correcting code (ECC) data signals; and

wherein the sum of the 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory socket, and the total number of data conduits is at least 72 data conduits.

45. (Currently Amended) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

the plurality of write operations further includes a third write operation subsequent to the first and second write operations; and wherein, in response to the detected trigger condition, the logic

~~element is further configured to periodically perform at regular intervals of time all of the first and second write operations followed by the third write operation.~~

46. (Currently Amended) The DIMM of claim 44~~5~~, ~~wherein, the logic element is further configured to perform the third write operation by writing a third set of data bits from the data~~

~~storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations~~ wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector ~~socket~~, and the total number of data conduits is at least 72 data conduits.

47. (Currently Amended) The DIMM of claim 45, ~~wherein, prior to performing the third write operation, the logic element is further configured to generate the third set of data bits based on groups of data bits stored in the data storage element~~ the logic element is further configured to perform a second write operation to write a second set of data bits into a second portion of the

data storage element.

48. (Previously Presented) The DIMM of claim 44, wherein, when ~~the system~~ power is provided to the DIMM from the power rails of the host system board, the nonvolatile memory is not powered using the first regulated voltage.

49. (Currently Amended) The DIMM of claim 474, wherein, ~~in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal~~ the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Currently Amended) The DIMM of claim 496, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Currently Amended) The DIMM of claim 474, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM ~~packages~~ devices, respectively.

52. (Currently Amended) The DIMM of claim 44, wherein, ~~prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time a plurality of read operations~~ when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including



a first threshold voltage and a second threshold voltage.

53. (Currently Amended) The DIMM of claim 5246, wherein, ~~prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read data bits from the data storage element and to generate the third set of data bits based on the read data bits~~ when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

54. (Currently Amended) The DIMM of claim 5344, wherein a specified operating voltage value is within a range of operating voltage values of the DIMM, ~~the width dimension is 133.35 millimeters.~~

55. (Currently Amended) The DIMM of claim 54, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM, ~~the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.~~

56. (Currently Amended) The DIMM of claim 495, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Currently Amended) The DIMM of claim 5544, wherein, ~~when the system power is provided to the DIMM from the system board, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and~~

~~wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal~~ the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds

to the upper operating voltage value.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory ~~socket slot connector~~ of a ~~host system board of a computer system~~, the memory ~~socket slot connector~~ including a set of power conduits, a set of data conduits ~~including at least 72 data conduits~~, and a set of address and control conduits, wherein ~~system power from the system board is provided to the DIMM via the memory socket by the set of power conduits and the DIMM is configured to operate using only the provided system power from the system board~~, a 1-bit wide double data rate (DDR) data signals are transferred ~~dis electrically conducted~~ between the ~~host system board~~ and the DIMM via ~~the memory socket by each data conduit of the set of data conduits~~, and ~~address and control signals are delivered from the host system electrically conducted from the system board to the DIMM via the memory socket by the set of address and control conduits~~, the DIMM comprising:

a printed circuit board (PCB) having ~~a form factor with a width dimension and a height dimension~~, the PCB edge connections configured to fit into the memory slot connector of the host system, the edge connections including:

~~an interface having edge connections disposed along the width dimension and configured to fit into the memory socket, the edge connections including:~~

a first set of edge connections configured to be electrically connected to ~~respective power conduits of the set of power conduits and operable to deliver the DIMM power from the power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM.~~

a second set of edge connections ~~each of which is configured to electrically conduct a 1-bit wide DDR data signal and to be electrically connected to a respective data conduit of the set of data conduits, and~~

a third set of edge connections configured to be electrically connected to ~~respective address and control conduits of the set of address and control conduits[;].~~

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the

first set of edge connections of the DIMM, the set of voltage supply lines including an input voltage supply line to electrically conduct an input voltage when the system power is provided to the DIMM from the system board[::]

a set of data lines electrically ~~coupled to respective edge connections of~~ connected to the second set of edge connections, ~~wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines~~[::] and

a set of address and control lines electrically ~~coupled to respective edge connections of~~ connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines and configured to electrically conduct address and control signals;

a controller ~~including coupled to the PCB and electrically connected to the input voltage supply line, the controller configured to receive the system power and the input voltage via the input voltage supply line, the controller including:~~

~~nonvolatile memory;~~

~~a data storage element configured to store a plurality of data bits; and~~

~~a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element; and~~

a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and electrically connected to the input voltage supply line of the set of voltage supply lines and coupled to the logic element; the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line; and
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller, wherein the compare the input voltage to a plurality of threshold voltages including a first threshold voltage and a second

threshold voltage; and

detect a trigger condition;

wherein, in response to the detected trigger condition, the logic element controller is configured to ~~periodically perform every millisecond~~, in response to the trigger signal, a plurality of write operations, including:

a first write operation to write a first set of data bits into a first portion of the data storage element; and

a second write operation to write a second set of data bits into a second portion of the data storage element;

wherein, when the system power is provided to the DIMM from the system board:

- the trigger condition occurs when the input voltage goes above both the first and second threshold voltages; and

wherein:

- a specified operating voltage value is within a range of operating voltage values of the DIMM;
- the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value;
- the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value;
- the first threshold voltage corresponds to the lower operating voltage value; and
- the second threshold voltage corresponds to the upper operating voltage value;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (DDR SDRAM) packages coupled to the set of address and control lines and to the set of data lines, ~~the each DDR SDRAM package of the plurality of DDR SDRAM packages~~ having a bit width of m bits and ~~configured devices being operable~~ to receive or output m 1-bit wide DDR data signals via ~~respective m data lines of the set of data lines based on~~ response to address and control signals received from the host system via the set of address and control lines ~~via address and control lines of the set of address and control~~

lines, wherein  $m$  is equal to four or eight; and

first, second, third, and fourth ~~voltage reducing circuits~~ converter circuits coupled to the PCB and to the input voltage supply line, ~~each of the first, second, third, and fourth converter circuits~~ and configured to, ~~in response to the detected trigger condition,~~ receive power ~~supplied by~~ from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines, ~~when the system power is provided to the DIMM from the system board,~~ the first, second, third, and fourth converter circuits configured to (i) generate first, second, third, and fourth regulated voltages, respectively, from the power supplied by the input voltage supply line, and

(ii) ~~output the first, second, third, and fourth regulated voltages via first, second, third, and fourth regulated voltage lines, respectively,~~ wherein the set of components ~~includes~~ including:

a first component ~~electrically connected to the first regulated voltage line and powered by~~ configured to receive power via the first regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a second component ~~electrically connected to the second regulated voltage line and powered by~~ configured to receive power via the second regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

a third component ~~electrically connected to the third regulated voltage line and powered by~~ configured to receive power via the third regulated voltage line ~~when the system power is provided to the DIMM from the system board; and~~

a fourth component ~~electrically connected to the fourth regulated voltage line and powered by~~ configured to receive power via the fourth regulated voltage line ~~when the system power is provided to the DIMM from the system board;~~

~~wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit; and~~

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power ~~when the system power is provided to the DIMM from the system board, is powered;~~

- ~~only by one or more of the first, second, third, and fourth~~

converter circuits; and  
only via the one or more of the first, second, third, and fourth  
regulated voltage lines;

wherein the plurality of DDR SDRAM ~~packages~~ devices includes:

a first group of at least five DDR SDRAM ~~packages~~ devices that are each  
connected to a first chip select line configured to electrically conduct a first chip  
select signal; and

a second group of at least four DDR SDRAM ~~packages~~ devices that are each  
connected to a second chip select line configured to electrically conduct a second  
chip select signal; and

~~when the system power is provided to the DIMM from the system board:~~

- ~~• the first and second groups of DDR SDRAM packages are is-~~  
~~configured to be accessible and not in self refresh mode;~~
- ~~• the first group of DDR SDRAM packages is configured to be-~~  
~~enabled, in response to the first chip select signal, to receive or output~~  
~~40 1 bit wide DDR data signals in parallel via 40 data lines of the set~~  
~~of data lines independently of whether the second group of DDR~~  
~~SDRAM packages is enabled, in response to the second chip select~~  
~~signal, to receive or output an integer number of 1 bit DDR data~~  
~~signals in parallel via the integer number of data lines of the set of data~~  
~~lines; and~~
- ~~• the 40 1 bit wide DDR data signals include 32 1 bit wide DDR data~~  
~~signals and eight 1 bit wide DDR error correcting code (ECC) data~~  
~~signals; and~~

~~wherein the sum of the 40 data lines and the integer number of data lines~~  
~~matches a total number of data conduits of the set of data conduits of the memory~~  
~~socket, and the total number of data conduits is at least 72 data conduits.~~

59. (Currently Amended) The DIMM of claim 586, ~~wherein the plurality of write~~  
~~operations further includes a third write operation subsequent to the first and second write~~  
~~operations; and wherein, in response to the detected trigger condition, the logic element is~~

~~further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.~~

wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector ~~socket~~, and the total number of data conduits is at least 72 data conduits

60. (Currently Amended) The DIMM of claim 527, wherein the logic element is further configured to perform ~~the a~~ third write operation by subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Currently Amended) The DIMM of claim 560, wherein, ~~in response to the detected trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal~~ the logic element is further configured to perform, prior to the first write operation and the second write operation, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Currently Amended) The DIMM of claim 586, wherein, ~~in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond a plurality of read operations prior to performing the first and second write~~

operations when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.

63. (Currently Amended) The DIMM of claim ~~586~~60, wherein ~~the logic element is further configured to perform a first and second read operations of the plurality of read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM packages, respectively~~ when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Currently Amended) The DIMM of claim ~~563~~, wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages. ~~the width dimension is 133.35 millimeters.~~

65. (Currently Amended) The DIMM of claim ~~642~~, wherein a specified operating voltage value is within a range of operating voltage values of the DIMM. ~~the height dimension is selected from one of a plurality of profiles ranging from 18.3 millimeters to 50 millimeters.~~

66. (Currently Amended) The DIMM of claim ~~586~~, wherein each of the first, second, and third ~~voltage reducing~~converter circuits is a buck converter.

67. (Currently Amended) The DIMM of claim ~~586~~, wherein, when ~~the system power is provided to the DIMM from the power rails of the host system board,~~ the nonvolatile memory is not powered using the first regulated voltage.

68. (Currently Amended) The DIMM of claim ~~6358~~, wherein, when ~~the system power is provided to the DIMM from the power rails of the host system board,~~ an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.



**Proposed Claim Amendments (Clean)**

1. (Canceled)

2. (Currently amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals are delivered from the host system to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and

(iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the host system via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line; and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component electrically configured to receive power via at least the fourth regulated voltage line; and

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.

3– 27. (Canceled)

28. (Currently Amended) The DIMM of claim 2, wherein the plurality of DDR

SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and

wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;
- the at least 40 1-bit wide DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals; and

the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

29. (Currently Amended) The DIMM of claim 2, wherein the controller further includes:

a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically

communicate with the nonvolatile memory and the data storage element, and wherein the write operation conducted by the controller in response to the trigger signal includes:

a first write operation to write a first set of data bits into a first portion of the data storage element;

a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

30. (Currently Amended) The DIMM of claim 2, wherein when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

31. (Currently Amended) The DIMM of claim 30, wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

32. (Currently Amended) The DIMM of claim 31, wherein a specified operating voltage value is within a range of operating voltage values of the DIMM.

33. (Currently Amended) The DIMM of claim 32, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM.

34. (Currently Amended) The DIMM of claim 2, wherein, when power from the power rails of the host system is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

35. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

36. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

37. (Currently Amended) The DIMM of claim 2, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

38. (Currently Amended) The DIMM of claim 29, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger signal, one or more read operations.

39. (Currently amended) The DIMM of claim 38, wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

40. (Currently Amended) The DIMM of claim 33, wherein the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value.

41. (Currently Amended) The DIMM of claim 29, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

42. (Currently Amended) The DIMM of claim 29, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

43. (Currently Amended) The DIMM of claim 40, wherein, when power from the power rails of the host system is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

44. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the host system ~~board~~ and the DIMM via the set of data conduits, and control signals are delivered from the host system to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,

and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
- (ii) generate a trigger signal upon detecting a trigger condition; and
- (iii) transmit the trigger signal to at least one other portion of the controller,

wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the host system via the set of address and control lines; and

first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via the first regulated voltage line;  
a second component configured to receive power via the second regulated voltage line;

a third component configured to receive power via the third regulated voltage line;

and

a fourth component electrically configured to receive power via the fourth regulated

voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.

45. (Currently Amended) The DIMM of claim 44, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

46. (Currently Amended) The DIMM of claim 44, wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and
- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and



wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

47. (Currently Amended) The DIMM of claim 45, wherein the logic element is further configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

48. (Currently Amended) The DIMM of claim 44, wherein, when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.

49. (Currently Amended) The DIMM of claim 47, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

50. (Currently Amended) The DIMM of claim 49, wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

51. (Currently Amended) The DIMM of claim 47, wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

52. (Currently Amended) The DIMM of claim 44, wherein when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input

voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

53. (Currently Amended) The DIMM of claim 52, wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

54. (Currently Amended) The DIMM of claim 53, wherein a specified operating voltage value is within a range of operating voltage values of the DIMM.

55. (Currently Amended) The DIMM of claim 54, wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM.

56. (Currently Amended) The DIMM of claim 49, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

57. (Currently Amended) The DIMM of claim 55, wherein the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value.

58. (Currently Amended) A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the host system and the DIMM via the set of data conduits, and control signals are delivered from the host system set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the host

system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM,

a second set of edge connections configured to be electrically connected to the set of data conduits,

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections,  
and

a set of address and control lines electrically connected to the third set of edge connections, wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines;

a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

- (i) monitor an input voltage supplied via the input voltage supply line;
  - (ii) generate a trigger signal upon detecting a trigger condition; and
  - (iii) transmit the trigger signal to at least one other portion of the controller,
- wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the data storage element;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM-devices being operable to receive or output data signals via the set of data lines based on-address and control signals received from the host system via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

- a first component configured to receive power via the first regulated voltage line;
- a second component configured to receive power via the second regulated voltage line;
- a third component configured to receive power via the third regulated voltage line;
- and
- a fourth component electrically configured to receive power via the fourth regulated voltage line;

wherein each component of the set of components:

- (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
- (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

wherein the plurality of DDR SDRAM devices includes:

- a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and
- a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal.

59. (Currently Amended) The DIMM of claim 58, wherein when power from the power rails of the host system is provided to the DIMM:

- each group of the first and second groups of DDR SDRAM is configured to be accessible and not in self-refresh mode;
- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of

whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and

- the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

60. (Currently Amended) The DIMM of claim 59, wherein the logic element is further configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

61. (Currently Amended) The DIMM of claim 60, wherein the logic element is further configured to perform, prior to the first write operation and the second write operation, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

62. (Currently Amended) The DIMM of claim 58, wherein when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.

63. (Currently Amended) The DIMM of claim 58, when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

64. (Currently Amended) The DIMM of claim 63, wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages.

65. (Currently Amended) The DIMM of claim 64, wherein a specified operating

voltage value is within a range of operating voltage values of the DIMM.

66. (Currently Amended) The DIMM of claim 58, wherein each of the first, second, and third converter circuits is a buck converter.

67. (Currently Amended) The DIMM of claim 58, wherein, when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.

68. (Currently Amended) The DIMM of claim 63, wherein, when power is provided to the DIMM from the power rails of the host system, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and

wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal.

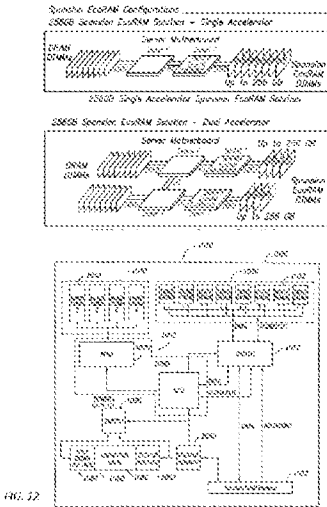
**Support Table for Claim Amendments**

| <b>Claim<br/>Element</b> | <b>Limitation</b> | <b>Support</b> |
|--------------------------|-------------------|----------------|
|--------------------------|-------------------|----------------|

2.1

A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals are delivered from the host system to the DIMM via the set of address and control conduits

Para. [00123]  
“For example, **the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system.** The interface 1022 of certain embodiments **provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.** For example, the interface 1022 can comprise **a standard 240-pin DDR2 edge connector.**”  
Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figure 2 and Fig.



12.

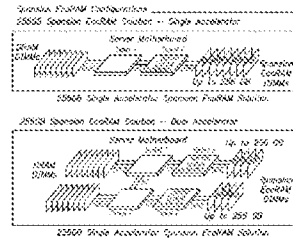
The memory socket of a computer system includes pins soldered onto the system board that provide electrical conduits for system power, data, and address and control signals from the system board to be electrically connected to



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|  |  | <p>corresponding edge connections of the edge connector 1022 when it is inserted into the memory socket.</p> <p>Para. [00123]</p> <p>“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).</p> <p>For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system . . .</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.”</b></p> |
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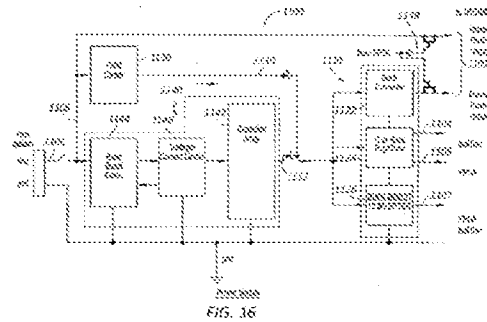
|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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| 2.2 | <p>the DIMM comprising:<br/> a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:<br/> a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM,</p> <p>a second set of edge connections configured to be electrically connected to the set of data conduits, and</p> <p>a third set of edge connections configured to be electrically connected to the set of address and control conduits,</p> | <p>Para. [00123]</p> <p>“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).</p> <p>For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.”</b></p> <p>This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector.</p> <p>When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.</p> |
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Fig. 2 which shows the DIMM in the socket on the



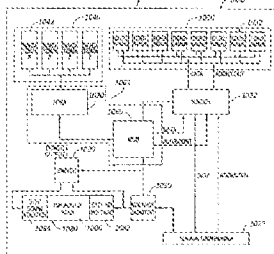
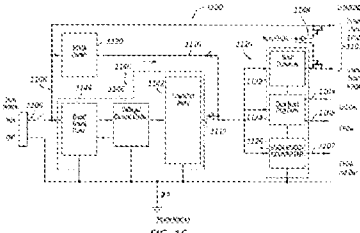
motherboard:

Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.



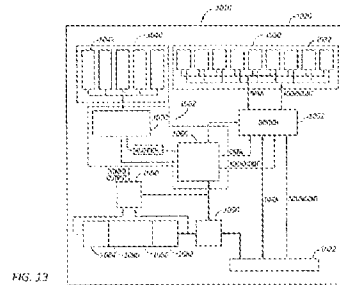
The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.

See also limitation 2.1.

|            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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| <p>2.3</p> | <p>a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM</p> <p>a set of data lines electrically coupled to the second set of edge connections, and</p> <p>a set of address and control lines electrically to the third set of edge connections,</p> | <p>Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16. For example, in Fig. 12 the input voltage supply lines are shown electrically connected to the Voltage Monitor 1050.</p> <p>FIG. 12</p>  <p>FIG. 16</p>  <p>For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd).</p> <p>Para. [00124]</p> |
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|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | <p>“For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises <b>eight 64Mx8 DDR2 SDRAM</b> elements 1032.”</p> <p>Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 2.4 | <p>a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;</p> | <p>The current application specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16.</p> <p>A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178.</p> <p>Para. [00172]</p> <p>“In certain embodiments, <b>the controller 1062 comprises a buffer (not shown) which is configured to store data</b> from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).”</p> <p>Para. [00178]</p> <p>“For example, in one embodiment, the <b>buffer is a first-in, first-out buffer implemented in the controller 1062</b> which comprises an FPGA.”</p> |

For example, FIG. 13 shows controller 1062 comprising a buffer:



Para. [00133]

“The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.”

“In certain embodiments, **the voltage monitor circuit 1050 is part of the controller 1062** (e.g., part of the MCU 1060)”

Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070

Para. [00133]

“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and **the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.**”

Para. [00130]

“In certain embodiments, the trigger condition occurs when the memory system 1010 **detects** that the **system voltage** is below **a certain threshold voltage**. For example, in one embodiment, the threshold voltage is 10 percent below **a specified operating voltage**. In certain embodiments, **a trigger condition** occurs when the voltage goes above **a certain threshold value**, such as,

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|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | <p>for example, 10 percent above a <b>specified operating voltage</b>. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 2.5 | <p>a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the host system via the set of address and control lines;</p> | <p>FIG. 12</p>                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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|     |                                                                                                                                                                                                                                                                          | <p>of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>And</p> <p>Para. [00122]</p> <p>“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”</p> <p>And</p> <p>Para. [00124]</p> <p>“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. <b>Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM).</b> For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b> The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, <b>volatile memory elements 1032 having bit widths of 4, 8, 16, 32,</b> as well as other bit widths, are compatible with certain embodiments described herein.”</p> |
| 2.6 | <p>first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines</p> | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

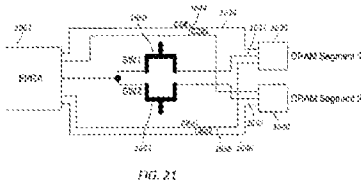


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|  | <p>On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck convertor 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.</p> <p>Para. [00148]</p> <p><b>“The conversion element 1120 can comprise one or more buck converters</b> and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters</b>, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, <b>the conversion element 1120</b> receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and <b>reduces the input to an appropriate amount for powering various components of the memory system</b>. For example, <b>the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g.,</b></p> |
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|     |                                                                                                                                                                                                                                                                                                                                                                                                                                                             | flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. <b>In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.”</b> |
| 2.7 | wherein the set of components includes:<br>a first component configured to receive power via at least the first regulated voltage line;<br>a second component configured to receive power via at least the second regulated voltage line;<br>a third component configured to receive power via at least the third regulated voltage line; and<br>a fourth component electrically configured to receive power via at least the fourth regulated voltage line | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |

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|     |                                                                                                                                                                                                                                                                       | <p>regulated voltage lines 1102, 1104, 1105, and 1107, respectively.</p> <p>On the right, each of the DRAM are shown as being connected to the first regulated voltage, for example.</p> <p>On the right, the isolation device is shown as being connected to the second regulated voltage, for example.</p> <p>On the right, the FPGA 1070 is shown as being connected to the third regulated voltage, for example.</p> <p>On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:</p> <p>Para. [00148]</p> <p>“the other reduced <b>voltage 1105</b> is 1.2V and is used to <b>power the controller 1062</b> (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the <b>voltage 1107</b> may be 3.3V and may be used to <b>power both the controller 1062 and the at least one circuit 1052.</b>”</p> <p>As shown in FIG. 12, above, the controller 1062 includes the components <b>FPGA 1070</b>, and <b>the MCU 1060</b>, and thus needs two different voltages for each of the components 1070, 1060.</p> |
| 2.8 | <p>wherein each component of the set of components:</p> <p>(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and</p> <p>(ii) receives power only via the one or more of the first, second, third, and</p> | <p>FIG. 16</p> <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |

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| fourth regulated voltage lines | <p>On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 that, when the system power is received, couples power to each of the four converter circuits via voltage 1110.</p> <p>Para. [00145]<br/>“In a second state, <b>the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.</b>”</p> <p>Para. [00151]<br/>“The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. <b>During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem</b> in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.”</p> <p>The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.</p> |
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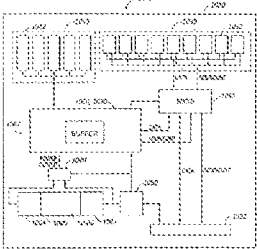
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| <p>28.1</p> | <p>wherein the plurality of DDR SDRAM devices includes:<br/>a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;<br/>a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal; and</p> | <p>FIG. 21</p>  <p>Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.</p> <p>Para. [00172]</p> <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from <b>two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology <b>including two DRAM segments 1630, 1640</b> for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from <b>the first DRAM segment 1630 and the second DRAM segment 1640</b> of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. <b>The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.</b>”</p> <p>Para. [00177]</p> <p>“In certain embodiments, transferring each data word comprises storing <b>a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624,</b> and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p> |
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|  | <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126].</p> |
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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | If x4 are used, the number of DRAM are correspondingly more.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| 28.2 | <p>when power from the power rails of the host system is provided to the DIMM:</p> <ul style="list-style-type: none"> <li>each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;</li> <li>the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines;</li> <li>the at least 40 1-bit wide DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit wide DDR error-correcting code (ECC) data signals</li> </ul> | <p>Para. [00173]</p> <p>“In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode.</b>”</p> <p>Para. [00178]</p> <p>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”</p> <p>Para. [00182]</p> |

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|      |                                                                                                                                                                                                                                               | <p>“In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 28.3 | <p>the sum of the 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.</p> | <p>Para. [00123]</p> <p>“The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00172]</p> <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>Para. [00178]</p> <p>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b>”</p> |
| 29.1 | <p>a data storage element configured to store a plurality of data bits and a logic element coupled to the nonvolatile memory and the data storage</p>                                                                                         | <p>The current application specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

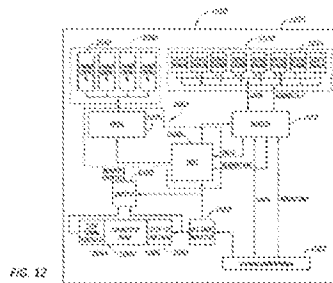


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|  | <p>element and configured to electrically communicate with the nonvolatile memory and the data storage element,</p> | <p>1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16.</p> <p>Para. [00127]</p> <p>“FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein.”</p> <p>FIG. 14</p>  <p>A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178.</p> <p>Para. [00172]</p> <p>“In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).”</p> <p>Para. [00178]</p> |
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|  | <p>“For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA.”</p> <p>For example, FIG. 13 shows controller 1062 comprising a buffer:</p> <p>Para. [00127]</p> <p>“Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the <b>logic element 1070 comprises</b> an FPGA available from Lattice Semiconductor Corporation which includes <b>an internal flash</b>. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. <b>The internal flash can improve the speed of the memory system 1010 and save physical space.</b> Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, <b>the logic element 1070 is a custom device</b>. In certain embodiments, <b>the logic element 1070 comprises various discrete electrical elements</b>, while in certain other embodiments, <b>the logic element 1070 comprises one or more integrated circuits</b>. FIG. 14 is a block diagram of an example memory module 1010 having <b>a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062</b> in accordance with certain embodiments described herein. <b>In certain embodiments, the controller 1062 includes one or more other components</b>. For example, in one embodiment, an FPGA without an internal flash is used</p> |
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and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.”

FIG. 12



29.2

a first write operation to write a first set of data bits into a first portion of the data storage element; a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations

Para. [00130]

“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, **a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.**”

Para. [00174]

"In certain embodiments, **when the first and second data slices are written to the buffer in the controller 1062**, the controller 1062 **combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040**. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030."

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|    |                                                                                | <p>Para. [00177]</p> <p>“In certain embodiments, <b>transferring each data word comprises storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |
| 30 | when power is provided to the DIMM from the power rails of the host system the | <p>Para. [00133]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

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|    | <p>voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage</p>                               | <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 31 | <p>when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages</p> | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

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|    |                                                                                                                                             | <p><b>occurs when the voltage goes below a threshold or above another threshold.”</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 32 | wherein a specified operating voltage value is within a range of operating voltage values of the DIMM                                       | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |
| 33 | wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |

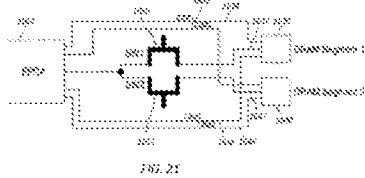
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|    | operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM.                                                                                                                                                                                             | <p>example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>"</p> <p>The first threshold and second threshold are the same as above, supported by "a threshold" and "another threshold" in the last line. The "10 percent" in the "the threshold voltage is 10 percent below a specified operating voltage" and the "10 percent" in the "above a specified operating voltage" support the lower operating voltage value, and the upper operating voltage value.</p> |
| 34 | wherein, when power from the power rails of the host system is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.                                                                                                                                                                                                                    | <p>Para. [00149]</p> <p>"In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are <b>not both powered using the first voltage 1102.</b>"</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 35 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read | <p>Para. [00178]</p> <p>"The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>"</p> <p>Para. [00178]</p> <p>"The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>"</p> <p>Para. [00179]</p>                                                                                                                                                                                                            |

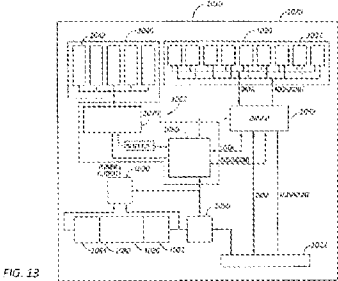
|    |                                                                                                                                                                                                                                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
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|    | first and second sets of data bits.                                                                                                                                                                                                                                                                                                                                                                    | “In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 35 | wherein, prior to performing the third write operation, the logic element is further configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits. | <p>Para. [00178]</p> <p>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>”</p> <p>Difference from Claim 35 is the read from the buffer is a <b>plurality of steps in Claim 35, and specifically two steps here</b>. Same sentence in Para. [00178] supports both scenarios.</p> <p>Para. [00174]</p> <p>“In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040.”</p> <p>Reading a data word or a block of words to be written into the NVM.</p> |
| 37 | wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.                                                                                                                                                                                                                                                   | <p>Para. [00148]</p> <p>“The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |



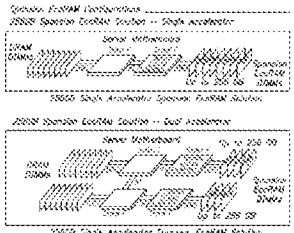
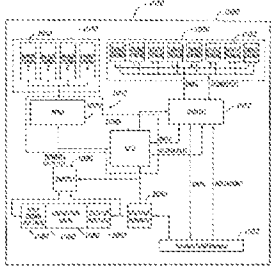
|    |                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
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|    |                                                                                                                                                                                                                                                    | <p><b>providing various voltage values to the memory system 1010.”</b></p> <p>And</p> <p>Para. [00148]</p> <p>“In certain embodiments, <b>the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system.”</b></p>                                                                                                                                                                                                |
| 38 | <p>wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger signal, one or more read operations.</p>                                            | <p>Para. [00178]</p> <p>“The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is <b>read from the buffer and written into the non-volatile memory subsystem (e.g., flash).</b>”</p> <p>Para. [00179]</p> <p>“In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.”</p> |
| 39 | <p>wherein the logic element is further configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.</p> | <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, <b>a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.</b>”</p> <p>Para. [00174]</p>                                                                                                                                                                                                                                                    |

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|    |                                                                                                                                                                          | <p>“In certain embodiments, <b>when the first and second data slices are written to the buffer in the controller 1062</b>, the controller 1062 <b>combines the first and second data slices 1630, 1640 into complete words or blocks of words</b> and <b>then writes each complete word or block of words to the non-volatile memory subsystem 1040</b>. In certain embodiments, this process is called “slicing” the volatile memory subsystem 1030.”</p> <p>Para. [00177]</p> <p>“In certain embodiments, <b>transferring each data word comprises storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p>            |
| 40 | wherein the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value. | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating</p> |

|    |                                                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
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|    |                                                                                                                                                                                                                                                                                                                                                    | voltage” support the lower operating voltage value, and the upper operating voltage value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 41 | <p>wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.</p> | <p>FIG. 21</p>  <p>Para. [00172]<br/>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.”</p> <p>Para. [00177]<br/>“The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition (e.g., a power failure) occurs</b>. In certain embodiments, transferring each data word comprises <b>storing a first portion (also referred to as a slice) of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>FIG. 13</p> |

|    |                                                                                                                                                                                        |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
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|    |                                                                                                                                                                                        |  <p>FIG. 13</p> <p>As can be seen in FIG. 13, the transfer from the DRAM occurs on a connection on the right side of the buffer, and the transfer to NVM will occur on a connection on the left side of the buffer.</p>                                                                                                                                                                                                                                                                                                                                                      |
| 42 | <p>wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.</p> | <p>A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178.</p> <p>Para. [00172]</p> <p>“In certain embodiments, <b>the controller 1062 comprises a buffer</b> (not shown) <b>which is configured to store data</b> from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).”</p> <p>Para. [00178]</p> <p>“For example, in one embodiment, the <b>buffer is a first-in, first-out buffer implemented in the controller 1062</b> which comprises an FPGA.”</p> <p>For example, FIG. 13 shows controller 1062 comprising a buffer:</p> |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
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|      |                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 43.1 | <p>wherein, when power from the power rails of the host system is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and the input voltage is below the second threshold; and</p> <p>wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.</p> | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> |
| 44.1 | <p>A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the host system and the DIMM are</p>                                                                                                            | <p>Para. [00123]</p> <p>“For example, <b>the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b>. For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p>                                                                                                                                                                                   |

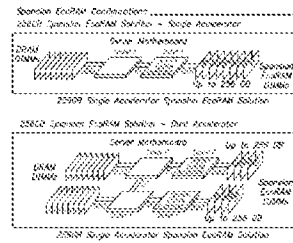
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|  | <p>transferred via the set of data conduits, and control signals are delivered from the host system to the DIMM via the set of address and control conduits</p> | <p>Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figure 2 and Fig. 12.</p>  <p>FIG. 2<br/>PRIOR ART</p> <p>The memory socket of a computer system includes pins soldered onto the system board that provide electrical conduits for system power, data, and address and control signals from the system board to be electrically connected to</p>  <p>FIG. 12</p> <p>corresponding edge connections of the edge connector 1022 when it is inserted into the memory socket.</p> <p>Para. [00123]<br/>“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).</p> |
|  |                                                                                                                                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | For example, the interface 1022 can comprise a <b>plurality of edge connections which fit into a corresponding slot connector of the host system</b> . The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b> . . . For example, the interface 1022 can comprise a <b>standard 240-pin DDR2 edge connector</b> .”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 44.2 | <p>the DIMM comprising:</p> <p style="padding-left: 40px;">a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:</p> <p style="padding-left: 80px;">a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM,</p> <p style="padding-left: 80px;">a second set of edge connections configured to be electrically connected to the set of data conduits, and</p> | <p>Para. [00123]</p> <p>“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).</p> <p>For example, the interface 1022 can comprise a <b>plurality of edge connections which fit into a corresponding slot connector of the host system</b>. The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b>. For example, the interface 1022 can comprise a <b>standard 240-pin DDR2 edge connector</b>.”</p> <p>This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector.</p> <p>When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to</p> |

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

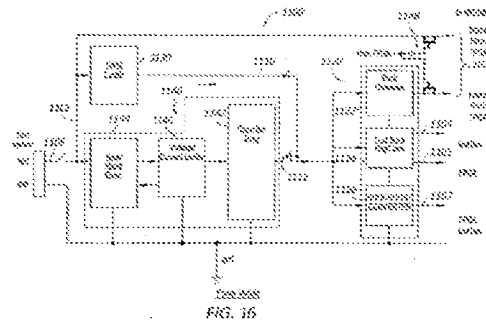
the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.

Fig. 2 which shows the DIMM in the socket on the

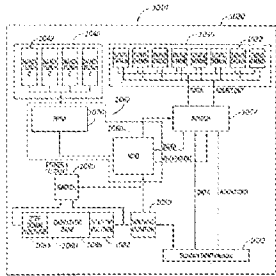
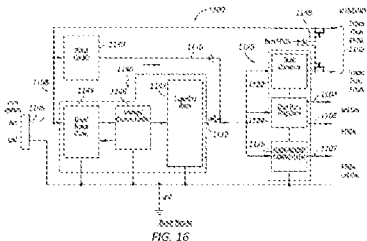


motherboard:

Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.



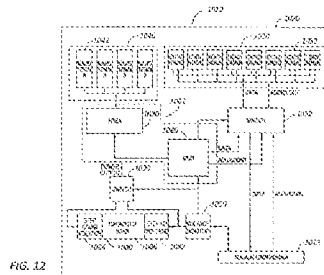


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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | See also limitation 2.1.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 44.3 | <p>a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM</p> <p>a set of data lines electrically coupled to the second set of edge connections, and</p> <p>a set of address and control lines electrically to the third set of edge connections ,</p> | <p>Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16. For example, in Fig. 12 the input voltage supply lines is shown electrically connected to the Voltage Monitor 1050.</p> <p>FIG. 12</p>  <p>FIG. 16</p>  <p>For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd).</p> |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | <p>Para. [00124]</p> <p>“For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises <b>eight 64Mx8 DDR2 SDRAM</b> elements 1032.”</p> <p>Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 44.4 | <p>a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;</p> | <p>The current application specification discloses a controller 1062 designed to seamlessly integrate with various other components described within the memory system 1010 that enhances performance (speed), efficiency and reduces cost. The controller 1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16.</p> <p>A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178.</p> <p>Para. [00172]</p> <p>“In certain embodiments, <b>the controller 1062 comprises a buffer (not shown) which is configured to store data</b> from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).”</p> <p>Para. [00133]</p> <p>“The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.”</p> |

|      |                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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|      |                                                                                                                           | <p>“In certain embodiments, <b>the voltage monitor circuit 1050 is part of the controller 1062</b> (e.g., part of the MCU 1060)”</p> <p>Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070</p> <p>Para. [00133]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. <b>For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.</b>”Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 44.5 | a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous | FIG. 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the host system via the set of address and control lines;



Para. [00124]  
**“Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”**

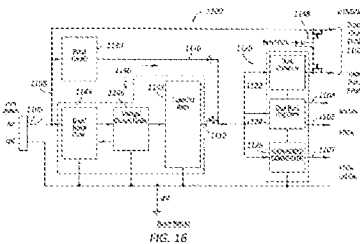
Para. [00172]  
 “In one embodiment, for example, the volatile memory subsystem 1030 comprises **a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)**, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

And

Para. [00122]  
 “In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”

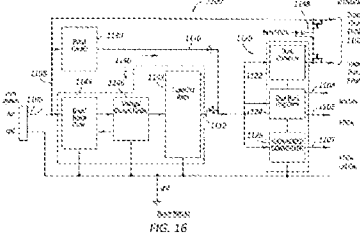
And

Para. [00124]

|      |                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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|      |                                                                                                                                                                                                                                                                  | <p>“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. <b>Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM).</b> For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b> The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, <b>volatile memory elements 1032 having bit widths of 4, 8, 16, 32,</b> as well as other bit widths, are compatible with certain embodiments described herein.”</p> |
| 44.6 | <p>first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines</p> | <p>FIG. 16</p>  <p>On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 which provides power to the four converter circuits. Buck converter 1122, dual buck converter 1124, and buck-boost converter 1126 provide regulated voltages on the regulated voltage lines 1102, 1104, 1105, and 1107, respectively.</p> <p>Para. [00148]</p> <p>“<b>The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters.</b> The conversion element 1120 may comprise a plurality of</p>                                                                                   |

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|  | <p>sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck- converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and</b></p> |
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On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the

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|      |                                                                                                                                                                                                                                                                                                       | <p>embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:</p> <p>Para. [00148]</p> <p>“the other reduced <b>voltage 1105</b> is 1.2V and is used to <b>power the controller 1062</b> (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the <b>voltage 1107</b> may be 3.3V and may be used to <b>power both the controller 1062 and the at least one circuit 1052.</b>”</p> <p>As shown in FIG. 12, above, the controller 1062 includes the components <b>FPGA 1070</b>, and <b>the MCU 1060</b>, and thus needs two different voltages for each of the components 1070, 1060.</p> |
| 44.8 | <p>wherein each component of the set of components:</p> <p>(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and</p> <p>(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines.</p> | <p>FIG. 16</p>  <p>On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 that, when the system power is received, couples power to each of the four converter circuits via voltage 1110.</p> <p>Para. [00145]</p> <p>“In a second state, <b>the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.</b>”</p>                                                                                                |



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|    |                                                                                                                                                                                                                                                                                | <p>Para. [00151]</p> <p>“The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. <b>During the second condition</b>, the method 1200 <b>comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem</b> in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.”</p> <p>The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.</p> |
| 45 | <p>wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.</p> | <p>Para. [00127]</p> <p>“FIG. 14 is a block diagram of an example memory module 1010 having <b>a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein.</b>”</p> <p>FIG. 14</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

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| 46.1 | <p>wherein the plurality of DDR SDRAM devices includes:</p> <p style="padding-left: 40px;">a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;</p> <p style="padding-left: 40px;">a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;</p> | <p>FIG. 21</p> <p>FIG. 21</p> <p>Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.</p> <p>Para. [00172]</p> <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from <b>two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology <b>including two DRAM segments 1630, 1640</b> for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from <b>the first DRAM segment 1630 and the second DRAM segment 1640</b> of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. <b>The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKE signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.</b>”</p> <p>Para. [00177]</p> <p>“In certain embodiments, transferring each data word comprises storing <b>a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire</b></p> |
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|  | <p>data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</p> <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or “slice”) may comprise 40 bits of the data word, and the second portion (or “slice”) may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as “slicing” the volatile memory during a backup operation. In the example embodiment, the process of “slicing” the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM</p> |
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|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | (5+4) as shown in FIG. 13 and discussed in Para. [00126].<br>If x4 are used, the number of DRAM are correspondingly more                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| 46.2 | <p>wherein when power from the power rails of the host system is provided to the DIMM:</p> <ul style="list-style-type: none"> <li>each group of the first and second groups of DDR SDRAM devices is configured to be accessible and not in self-refresh mode;</li> <li>the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an</li> </ul> | <p>Para. [00173]<br/>“In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode.</b>”</p> <p>Para. [00178]<br/>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”</p> <p>Para. [00182]</p> |

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|      | <p>integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and</p> <ul style="list-style-type: none"> <li>the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and</li> </ul> | <p>“In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 46.3 | <p>wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.</p>                                                                            | <p>Para. [00123]<br/>         “The interface 1022 of certain embodiments <b>provides a conduit for</b> power voltage as well as <b>data</b>, address, and control <b>signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>Para. [00172]<br/>         “In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>Para. [00178]</p> |

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|    |                                                                                                                                                                                  | <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.”</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
| 47 | <p>wherein the logic element is further configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.</p> | <p>Para. [00174]</p> <p><b>“In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.”</b></p> <p>Para. [00177]</p> <p><b>“In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.”</b></p> <p>For the chain of system power electrical connection to the controller, see 2.1, 2.4, 2.5, and 2.6 above.</p> |
| 48 | <p>wherein, when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.</p>             | <p>Para. [00149]</p> <p><b>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.”</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

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| 49 | <p>wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory, wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and wherein, in response to the detected trigger condition, the logic element is further configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.</p> | <p>Para. [00177]<br/>         “In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.”</p> <p>Para. [00130]<br/>         “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> |
| 50 | <p>wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of</p>                                                                                                                                                                                                    | <p>Para. [00130]<br/>         “In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> <p>Para. [00178]<br/>         “The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, <b>the process of "slicing" the volatile memory during a backup</b> includes bringing the 32-bit slice</p>                                                                                                                                                                                                                                                                                                                                                                                                                     |

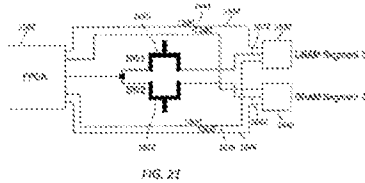
|    |                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
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|    | data bits based on the read first and second sets of data bits, respectively.                                                                                                                                                                                                                                                                                     | out of self-refresh, <b>reading a 32-bit block from the slice into the buffer</b> , and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and <b>a 40-bit block from the slice is read into a buffer.</b> ”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 51 | wherein, prior to performing the first and second write operations, the logic element is further configured to perform, in response to the detected trigger condition, periodically at regular intervals of time, one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively. | <p>Para. [00130]</p> <p>“In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition.”</p> <p>Para. [00177]</p> <p>“The memory system 1010 may enter the second mode of operation, for example, <b>when a trigger condition (e.g., a power failure) occurs</b>. In certain embodiments, transferring each data word comprises <b>storing a first portion</b> (also referred to as a slice) <b>of the data word in a buffer</b> in an operational block 1622, <b>storing a second portion of the data word in the buffer</b> in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem</b> 1040 in an operational block 1626.”</p> |
| 52 | wherein when power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.                                                                                                                | <p>Para. [00133]</p> <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p> <p>Para. [00130]</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |



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|    |                                                                                                                                                                                                     | <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 53 | wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above both the first and the second threshold voltages. | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b></p>                                                                                                                                                                                                                                     |
| 54 | wherein a specified operating voltage value is within a range of operating voltage values of the DIMM.                                                                                              | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |

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|    |                                                                                                                                                                                                                                                                                                                                         | <p>voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p>                                                                                                                                                                                                                                                                                                                                                                 |
| 55 | <p>wherein the range of operating voltage values is bounded by an upper operating voltage value and a lower operating voltage value, the lower operating voltage value is below the specified operating voltage value of the DIMM and the upper operating voltage value is above the specified operating voltage value of the DIMM.</p> | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |
| 56 | <p>wherein the third write operation comprises a transfer of the first and second set of data bits</p>                                                                                                                                                                                                                                  | <p>FIG. 21</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

from the data storage element to the nonvolatile memory via a first connection, and wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.



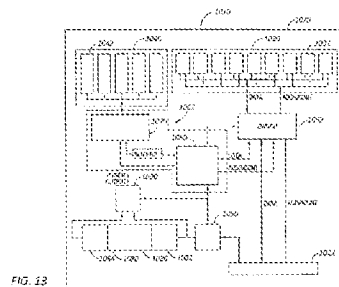
Para. [00172]

“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.”

Para. [00177]

“The memory system 1010 may enter the second mode of operation, for example, **when a trigger condition (e.g., a power failure) occurs**. In certain embodiments, transferring each data word comprises **storing a first portion** (also referred to as a slice) **of the data word in a buffer** in an operational block 1622, **storing a second portion of the data word in the buffer** in an operational block 1624, and **writing the entire data word from the buffer to the non-volatile memory subsystem 1040** in an operational block 1626.”

FIG. 13

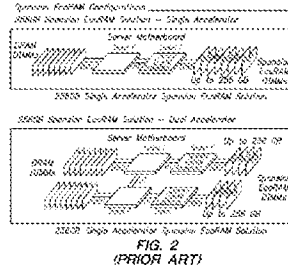


As can be seen in FIG. 13, the transfer from the DRAM occurs on a connection on the right side of the buffer, and

|      |                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                                                                                                     | the transfer to NVM will occur on a connection on the left side of the buffer.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 57   | wherein the first threshold voltage corresponds to the lower operating voltage value, and the second threshold voltage corresponds to the upper operating voltage value.                                                                                                                                                                                                            | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |
| 58.1 | A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a host system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals between the host system and the DIMM are transferred via the set of data conduits, and control signals are delivered from | <p>Para. [00123]</p> <p>“For example, <b>the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

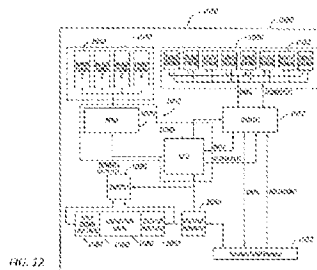
the host system to the DIMM via the set of address and control conduits

Dual in-line memory module (DIMM) has an edge connector 1022 that includes edge connections for power, data, and address and control signals designed to fit into a memory socket of a computer system. See Figure 2 and Fig.



12.

The memory socket of a computer system includes pins soldered onto the system board that provide electrical conduits for system power, data, and address and control signals from the system board to be electrically connected to corresponding edge connections of the edge connector 1022



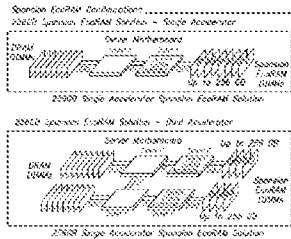
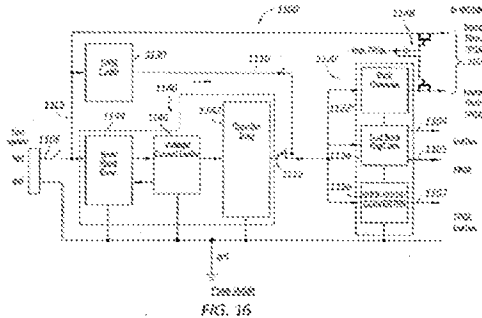
when it is inserted into the memory socket.

Para. [00123]

“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).

For example, the interface 1022 can comprise a **plurality of edge connections which fit into a corresponding slot connector of the host system.** The interface 1022 of certain

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system</b> . . . For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b> ”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 58.2 | <p>the DIMM comprising:</p> <p style="padding-left: 40px;">a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the host system, the edge connections including:</p> <p style="padding-left: 80px;">a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the host system via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the host system is the only power received by the DIMM,</p> <p style="padding-left: 80px;">a second set of edge connections configured to be electrically connected to the set of data conduits, and</p> <p style="padding-left: 40px;">a third set of edge connections configured to</p> | <p>Para. [00123]</p> <p>“The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown).</p> <p>For example, the interface 1022 can comprise <b>a plurality of edge connections which fit into a corresponding slot connector of the host system.</b> The interface 1022 of certain embodiments <b>provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>”</p> <p>This paragraph describes the contact of the edge connections and the slot connector, as well as a JEDEC standard 240 pin DDR2 edge connector. The JEDEC standard specifies what voltages the system voltage regulator is to provide to which pins in the slot, which are then passed on to the edge connector.</p> <p>When the interface 1022 edge connector is inserted into the memory socket of the computer system, edge connections will mate with corresponding conduits and an electrical connection is established for system power, data, and address and control signals to be electrically conducted to the edge connections on the PCB, and PCB traces also called lines allow signals and power/voltage to be electrically conducted on the PCB.</p> |

|      |                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|------|-----------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      | be electrically connected to the set of address and control conduits,                         | <p>Fig. 2 which shows the DIMM in the socket on the</p>  <p>FIG. 2<br/>(PRIOR ART)</p> <p>motherboard:</p> <p>Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply lines on the PCB, as shown in Fig. 16.</p>  <p>FIG. 16</p> <p>The DIMM operates using only the system power provided from the system board, for example as specified and is well known in the JEDEC standard 240-pin DDR2 edge connector.</p> |
| 58.3 | a set of voltage supply lines electrically connected to the first set of edge connections and | <p>Note the power rails (Vdd and Gnd) of the host system coupled to the Standard DIMM Interface 1022 and electrically connected to the input voltage and ground supply</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

configured to receive the power delivered to the DIMM from the power rails of the host system by way of the memory slot connector of the host system and the first set of edge connections of the DIMM

a set of data lines electrically coupled to the second set of edge connections, and

a set of address and control lines electrically coupled to the third set of edge connections,

lines on the PCB, as shown in Fig. 12, Fig. 13, Fig. 14 and Fig. 16. For example, in Fig. 12 the input voltage supply lines is shown electrically connected to the Voltage Monitor 1050.

FIG. 12

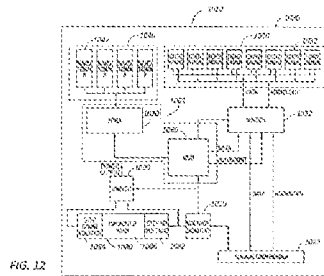
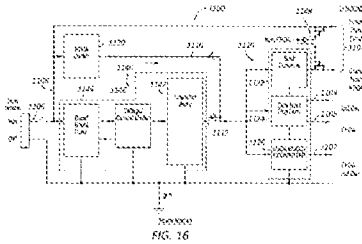


FIG. 16



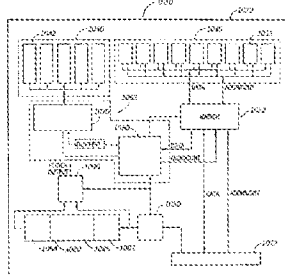
For example, respective power conduits (Vdd and gnd) of the set of power conduits of the memory socket are labeled “from system”, on left of Fig. 16, are electrically connected via a set of voltage supply lines to the PWM Controller 1130, and the ground supply line (gnd).

Para. [00124]

“For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises **eight 64Mx8 DDR2 SDRAM** elements 1032.”



|      |                                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                                    | Note also the address and control lines from the Standard DIMM Interface 1022 coupled to the DRAM 1030 through the Switch 1052 in FIG. 12.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 58.4 | wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection, wherein each data line of the set of data lines is configured to electrically conduct a 1-bit wide DDR data signal, and wherein the set of data lines includes at least 72 data lines; | <p>Para. [00178]</p> <p><b>“In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or “slice”) may comprise 40 bits of the data word, and the second portion (or “slice”) may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as “slicing” the volatile memory during a backup operation. In the example embodiment, the process of “slicing” the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment.”</p> <p>Para. [00182]</p> <p><b>“In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.”</b></p> <p>And</p> <p>Para. [00172]</p> |

|      |                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                     | <p>“In one embodiment, for example, the volatile memory subsystem 1030 comprises a <b>72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”</p> <p>The embodiment of FIG. 13 shows nine x8 DRAM devices for a data bus bit width of 72:</p>  <p>FIG. 13</p> <p>And</p> <p>Para. [00122]</p> <p>“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”</p> |
| 58.5 | a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied | <p>1062 comprises a microcontroller unit (MCU) 1060, logic element 1070, buffer, voltage monitor circuit 1050, and one or more additional components. Logic element 1070 comprises internal nonvolatile memory, one or more integrated circuits and various discrete electrical elements. The controller 1062 receives system power from the standard DIMM interface 1022. For example, support is</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the data storage element;

found in at least [00127], [00133], and [00172]; and Fig. 12, Fig. 13, Fig. 14, and Fig. 16.

A buffer (data storage element) is shown in Fig. 13 and Fig. 14, and disclosed to store data in at least 172, and 178.

Para. [00172]

“In certain embodiments, **the controller 1062 comprises a buffer (not shown) which is configured to store data** from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO).”

Para. [00178]

“For example, in one embodiment, the **buffer is a first-in, first-out buffer implemented in the controller 1062** which comprises an FPGA.”

For example, FIG. 13 shows controller 1062 comprising a buffer:

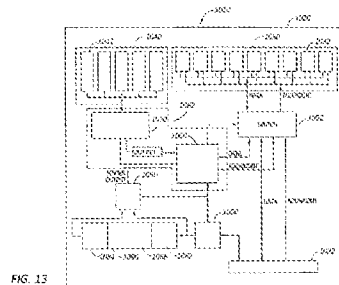


FIG. 13

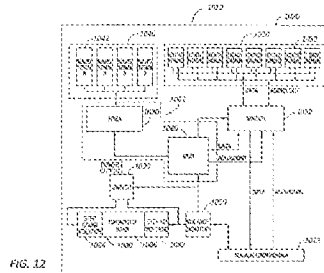
Para. [00133]

“The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022.”

“In certain embodiments, **the voltage monitor circuit 1050 is part of the controller 1062** (e.g., part of the MCU 1060)”

|      |                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                               | <p>Fig. 14 depicts the voltage monitoring circuit 1050 receiving the input voltage via interface 1022 and coupled to the logic element 1070</p> <p>Para. [00133]</p> <p>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b>”</p> <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b>”</p> <p>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.”</p> |
| 58.6 | a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data | FIG. 12                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |

lines, the DDR SDRAM-devices being operable to receive or output data signals via the set of data lines based on-address and control signals received from the host system via the set of address and control lines;



Para. [00124]

**“Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).”**

Para. [00172]

“In one embodiment, for example, the volatile memory subsystem 1030 comprises a **72-bit data bus** (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”

And

Para. [00122]

“In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein.”

And

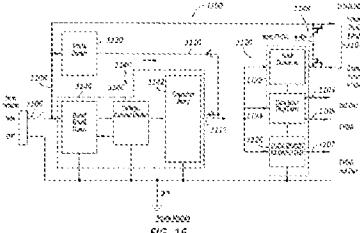
Para. [00124]

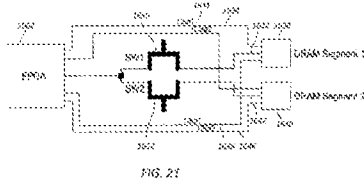
|      |                                                                                                                                                                                                                                                                          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                          | <p>“In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. <b>Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and synchronous DRAM (SDRAM).</b> For example, in the block diagram of FIG. 12, <b>the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032.</b> The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, <b>volatile memory elements 1032 having bit widths of 4, 8, 16, 32,</b> as well as other bit widths, are compatible with certain embodiments described herein.”</p> |
| 58.7 | <p>first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines</p> | <p>FIG. 16</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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|--|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|  |  | <p>The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system. For example, the buck- converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and</b></p> |
|--|--|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|

On the right, the MCU 1060 is shown as also being connected to the fourth regulated voltage, as is shown in the



|      |                                                                                                                                                                                                                                                                                                      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                      | <p>embodiment of FIG. 12, the MCU 1060 is part of the controller 1062. This is further specified in the text of the disclosure:</p> <p>Para. [00148]</p> <p>“the other reduced <b>voltage 1105</b> is 1.2V and is used to <b>power the controller 1062</b> (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the <b>voltage 1107</b> may be 3.3V and may be used to <b>power both the controller 1062 and the at least one circuit 1052.</b>”</p> <p>As shown in FIG. 12, above, the controller 1062 includes the components <b>FPGA 1070</b>, and <b>the MCU 1060</b>, and thus needs two different voltages for each of the components 1070, 1060</p> |
| 58.9 | <p>wherein each component of the set of components:</p> <p>(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and</p> <p>(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines</p> | <p>FIG. 16</p>  <p>On the left of the figure, system power (Vdd) is provided on the input voltage supply line 1106 to the PWM controller 1130 that, when the system power is received, couples power to each of the four converter circuits via voltage 1110.</p> <p>Para. [00145]</p> <p>“In a second state, <b>the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120.</b>”</p> <p>Para. [00151]</p>                                                                           |

|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
|-------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|       |                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | <p>“The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. <b>During the second condition</b>, the method 1200 comprises <b>providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem</b> in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.”</p> <p>The system power is provided to the PWM controller 1130 and from there to the four converter circuits (conversion element 1120) is the only power to the module. In the second state all components are powered from the power supplied from one or more of the four converter circuits via one or more of the four regulated voltages. There is no alternative power source claimed.</p> |
| 58.10 | <p>wherein the plurality of DDR SDRAM devices includes:</p> <ul style="list-style-type: none"> <li>a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;</li> <li>a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal</li> </ul> | <p>FIG. 21</p>  <p>Chip Select 1 and Chip Select 2 going to each group is shown in FIG. 21 above.</p> <p>Para. [00172]</p> <p>“FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from <b>two DRAM segments 1630, 1640</b> of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology <b>including two DRAM segments 1630, 1640</b> for</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                     |

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|  | <p>the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from <b>the first DRAM segment 1630 and the second DRAM segment 1640</b> of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. <b>The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062.</b>"</p> <p>Para. [00177]</p> <p>"In certain embodiments, transferring each data word comprises storing <b>a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624,</b> and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626."</p> <p>Para. [00178]</p> <p><b>"In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the</p> |
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|      |                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|      |                                                                                                                                                                                                                                                                                                                                                                           | <p>32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).”</p> <p>This claim is limited to x4 and x8 DRAM. When using x8, it takes five DRAM to receive or output 40 bits. The remaining bits in the word are 32, which means it would take four x8 DRAM to complete receiving or outputting the word. Thus, you have a module with a total of nine DRAM (5+4) as shown in FIG. 13 and discussed in Para. [00126]. If x4 are used, the number of DRAM are correspondingly more.</p> |
| 59.1 | <p>wherein when power from the power rails of the host system is provided to the DIMM:</p> <ul style="list-style-type: none"> <li>each group of the first and second groups of DDR SDRAM is configured to be accessible and not in self-refresh mode;</li> <li>the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip</li> </ul> | <p>Para. [00173]</p> <p>“In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are <b>not accessible when they are in self-refresh mode</b>, and <b>maintain stored information and are accessible when they are in active mode.</b>”</p> <p>Para. [00178]</p> <p>“<b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> In certain embodiments, the buffer is included in the</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                             |

|      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
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|      | <p>select signal, to receive or output at least 40 1-bit wide DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via the integer number of data lines of the set of data lines; and</p> <ul style="list-style-type: none"> <li>the at least 40 1-bit wide DDR data signals include 32 1-bit wide DDR data signals and eight 1-bit wide DDR error-correcting code (ECC) data signals; and</li> </ul> | <p>controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The 40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment."</p> <p>Para. [00182]</p> <p>"In certain other embodiments, <b>the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.</b>"</p> |
| 59.2 | <p>wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits</p>                                                                                                                                                                                                                                                                                                                                                                                                       | <p>Para. [00123]</p> <p>"The interface 1022 of certain embodiments <b>provides a conduit for</b> power voltage as well as <b>data</b>, address, and control <b>signals between the memory system 1010 and the host system.</b> For example, the interface 1022 can comprise <b>a standard 240-pin DDR2 edge connector.</b>"</p> <p>Para. [00172]</p> <p>"In one embodiment, for example, the volatile memory subsystem 1030 comprises <b>a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC)</b>, the first data slice from the</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

|    |                                                                                                                                                                                                                                                                                                                                                                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
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|    | is at least 72 data conduits.                                                                                                                                                                                                                                                                                                                                                     | first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.”<br>Para. [00178]<br>“ <b>In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word.</b> ”                                                                                    |
| 60 | wherein the logic element is further configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations. | Para. [00177]<br>“In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and <b>writing the entire data word from the buffer to the non-volatile memory subsystem 1040</b> in an operational block 1626.” |
| 61 | wherein the logic element is further configured to perform, prior to the first write operation and the second write operation, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.                                                                                            | [00172]<br><u>FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010.</u><br><u>The controller read first and second data slices (sets of data bits) from first and second groups of DDR SDRAM packages, and then write the first and second sets of data bits into the controller 1062 (data storage element).</u>                                                                                                                                                                          |

|    |                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |
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| 62 | wherein when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.                                                                                   | Para. [00149]<br>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are <b>not both powered using the first voltage 1102.</b> ”                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
| 63 | when the power is provided to the DIMM from the power rails of the host system the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage. | Para. [00133]<br>“In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and <b>the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.</b> ”<br>Para. [00130]<br>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a <b>certain threshold voltage</b> . For example, in one embodiment, the threshold voltage is 10 percent below a <b>specified operating voltage</b> . In certain embodiments, a <b>trigger condition</b> occurs when the voltage goes above a <b>certain threshold value</b> , such as, for example, 10 percent above a <b>specified operating voltage</b> . <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b> ”<br>The system voltage provides support for the input voltage. The “a threshold” in the last sentence provides support for “a first threshold” and the “another threshold,” also in the last sentence provides support for the “a second threshold.” |
| 64 | wherein when power is provided to the DIMM from the power rails of the host system the trigger condition occurs when the input voltage goes above                                                                                              | Para. [00130]<br>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |

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|    | both the first and the second threshold voltages.                                                      | <p>percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p>                                                                                                                                                                                                                                                        |
| 65 | wherein a specified operating voltage value is within a range of operating voltage values of the DIMM. | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, 10 percent above a specified operating voltage. <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.</b></p> <p>The first threshold and second threshold are the same as above, supported by “a threshold” and “another threshold” in the last line. The “10 percent” in the “the threshold voltage is 10 percent below a specified operating voltage” and the “10 percent” in the “above a specified operating voltage” support the lower operating voltage value, and the upper operating voltage value.</p> |



|    |                                                                                                                                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
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| 66 | wherein each of the first, second, and third converter circuits is a buck converter.                                                                                                    | <p>Para. [00148]</p> <p>“The conversion element 1120 may comprise a plurality of sub- blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. <b>The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010.</b>”</p> <p>And</p> <p>Para. [00148]</p> <p>“In certain embodiments, <b>the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate amount for powering various components of the memory system.</b>”</p> |
| 67 | wherein, when power is provided to the DIMM from the power rails of the host system, the nonvolatile memory is not powered using the first regulated voltage.                           | <p>Para. [00149]</p> <p>“In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are <b>not both powered using the first voltage 1102.</b>”</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 68 | wherein, when power is provided to the DIMM from the power rails of the host system, an additional trigger condition occurs when the input voltage is above the first threshold and the | <p>Para. [00130]</p> <p>“In certain embodiments, the trigger condition occurs when the memory system 1010 <b>detects</b> that the <b>system voltage</b> is below <b>a certain threshold voltage</b>. For example, in one embodiment, the threshold voltage is 10 percent below <b>a specified operating voltage</b>. In certain embodiments, <b>a trigger condition</b> occurs when the voltage goes above <b>a certain threshold value</b>, such as, for example, 10 percent above <b>a specified operating voltage</b>.</p>                                                                                                                                                                                                                                                                                                                                                       |

|  |                                                                                                                                                                                                         |                                                                                                                             |
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|  | input voltage is below the second threshold; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a trigger signal. | <b>In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.”</b> |
|--|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------|



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## ELECTRONIC PAYMENT RECEIPT

APPLICATION #  
**17/582,797**

RECEIPT DATE / TIME  
**03/24/2025 04:10:05 PM Z ET**

ATTORNEY DOCKET #  
**022955-000090**

### Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

### Application Information

APPLICATION TYPE Utility - Nonprovisional Application  
under 35 USC 111(a)

PATENT # -

CONFIRMATION # 3546

FILED BY LISA MARGARET ELLIOTT

PATENT CENTER # 69710469

AUTHORIZED BY Khaled Shami

CUSTOMER # 151145

FILING DATE 01/24/2022

CORRESPONDENCE ADDRESS -

FIRST NAMED INVENTOR Chi-She Chen

### Payment Information

PAYMENT METHOD  
DA / 220585

PAYMENT TRANSACTION ID  
E20253NG10277610

PAYMENT AUTHORIZED BY  
LISA MARGARET ELLIOTT

| FEE CODE             | DESCRIPTION                                                                            | ITEM PRICE(\$) | QUANTITY | ITEM TOTAL(\$)    |
|----------------------|----------------------------------------------------------------------------------------|----------------|----------|-------------------|
| 1820                 | REQUEST FOR CONTINUED EXAMINATION (RCE)- 2ND AND SUBSEQUENT REQUEST (SEE 37 CFR 1.114) | 2860.00        | 1        | 2860.00           |
| <b>TOTAL AMOUNT:</b> |                                                                                        |                |          | <b>\$2,860.00</b> |

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

#### New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

#### National Stage of an International Application under 35 U.S.C. 371

Samsung Electronics Co., Ltd.  
Ex. 1002, p. 1391

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

## REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL (Submitted Only via EFS-Web)

|                      |              |             |            |                               |                |          |      |
|----------------------|--------------|-------------|------------|-------------------------------|----------------|----------|------|
| Application Number   | 17582797     | Filing Date | 2022-01-24 | Docket Number (if applicable) | 022955-000090  | Art Unit | 2138 |
| First Named Inventor | Chi-She Chen |             |            | Examiner Name                 | HASHEM FARROKH |          |      |

**This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.**

Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at [WWW.USPTO.GOV](http://WWW.USPTO.GOV)

### SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on \_\_\_\_\_

☐ Other \_\_\_\_\_

☒ Enclosed

☒ Amendment/Reply

☐ Information Disclosure Statement (IDS)

☐ Affidavit(s)/ Declaration(s)

☒ Other Appendix A - Claim Support Table; Appendix B - Clean Copy of Amended Claims

### MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months \_\_\_\_\_  
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other \_\_\_\_\_

### FEES

**The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**

☒ The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 220585

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

| Signature of Registered U.S. Patent Practitioner |                |                     |            |
|--------------------------------------------------|----------------|---------------------|------------|
| Signature                                        | /Khaled Shami/ | Date (YYYY-MM-DD)   | 2025-03-24 |
| Name                                             | Khaled Shami   | Registration Number | 38745      |

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

*If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.*

## Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.



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## ELECTRONIC ACKNOWLEDGEMENT RECEIPT

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ATTORNEY DOCKET #  
**022955-000090**

### Title of Invention

MEMORY WITH ON-MODULE POWER MANAGEMENT

### Application Information

|                           |                                                             |                         |                       |
|---------------------------|-------------------------------------------------------------|-------------------------|-----------------------|
| APPLICATION TYPE          | Utility - Nonprovisional Application<br>under 35 USC 111(a) | PATENT #                | -                     |
| CONFIRMATION #            | 3546                                                        | FILED BY                | LISA MARGARET ELLIOTT |
| PATENT CENTER #           | 69710469                                                    | FILING DATE             | 01/24/2022            |
| CUSTOMER #                | 151145                                                      | FIRST NAMED<br>INVENTOR | Chi-She Chen          |
| CORRESPONDENCE<br>ADDRESS | -                                                           | AUTHORIZED BY           | Khaled Shami          |

### Documents

**TOTAL DOCUMENTS: 2**

| DOCUMENT                                                      | PAGES | DESCRIPTION                                                                                                                           | SIZE<br>(KB) |
|---------------------------------------------------------------|-------|---------------------------------------------------------------------------------------------------------------------------------------|--------------|
| RCE - 022955-90.pdf                                           | 3     | Request for Continued Examination (RCE)                                                                                               | 1631 KB      |
| Resp to 1-24-25 FOA w<br>Appendix A and B - 022955-<br>90.pdf | 99    | Amendment<br>Submitted/Entered with Filing<br>of Continued Prosecution<br>Application (CPA)/Request for<br>Continued Examination(RCE) | 2459 KB      |

### Digest

| DOCUMENT            | MESSAGE DIGEST(SHA-512)                                                                                |
|---------------------|--------------------------------------------------------------------------------------------------------|
| RCE - 022955-90.pdf | DB1FC70920753464AC76BD959DA2078658A2B02721B0211B9<br>107C08E09C817B1A56279487F8202F9CFE3E98A3234C9B137 |

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DE433596459B9DE0E180ADDF57610B

Resp to 1-24-25 FOA w  
Appendix A and B - 022955-  
90.pdf

D7BC46D7161D95C3014355A0629AE46E079BDD4342FD77BE  
3F65A401DD9DA0B804934A15DCEE10B16C6D80DCAB6D4349  
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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.