UNITED STATES PATENT APPLICATION

FOR

TITLE

FLASH-DRAM HYBRID MEMORY MODULE

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Flash-DRAM Hybrid Memory Module

PRIORITY CLAIM

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, titled "HIGH-DENSITY DIMMS", and is a continuation-in-part (CIP) of US patent application serial no. 12/240,916, filed September 29, 2008, titled "NON-VOLATILE MEMORY MODULE", the contents of both of which are incorporated herein by reference in their entirety.

TECHNICAL FIELD

[0002] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0003] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

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[0004] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as 'finance transactions' (for example, point-of-service, inter-bank transaction, stock market transaction), 'scientific computation' (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), 'medical diagnostics' (for example, diagnostics based on the fuzzy logic, medical data processing), 'simple information sharing and searching' (for example, web search, retail store website, company home page), 'email' (information distribution and archive), 'security service', 'entertainment' (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0005] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process

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cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0006] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM . The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MBs for the EcoRAM vs. 104MBs for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™), which occupies one of the server's CPU sockets is

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used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0007] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0008] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0009] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

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OVERVIEW

[0010] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0011] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0012] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring,

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and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0013] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0014] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0015] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0016] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0017] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

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[0018] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0019] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0020] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0021] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0022] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

[0023] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0024] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the

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memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0025] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0026] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0027] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0028] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0029] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

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[0030] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0031] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0032] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0033] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0034] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0035] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0036] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0037] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0038] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0039] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0040] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0041] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0042] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

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[0043] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0044] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0045] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0046] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0047] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0048] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0049] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

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[0050] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0051] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0052] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0053] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0054] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0055] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a

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value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0056] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0057] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0059] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0060] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

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[0061] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0062] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0063] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

BRIEF DESCRIPTION OF THE DRAWINGS

[0064] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0065] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

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FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

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DESCRIPTION OF EXAMPLE EMBODIMENTS

[0066] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0067] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0068] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those

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of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only Memory), EEPROM (Electrically Eraseable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0069] The term "exemplary" where used herein is intended to mean "serving as an example, instance or illustration." Any embodiment described herein as "exemplary" is not necessarily to be construed as preferred or advantageous over other embodiments.

[0070] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0071] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction,

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scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0072] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0073] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type

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of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0074] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to

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the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0075] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0076] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400'supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that

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the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0077] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0078] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0079] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain

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embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0080] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion,

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Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0081] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0082] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be

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configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH 510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0083] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0084] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information

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from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0085] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

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[0086] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0087] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0088] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to

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CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received form MCH 510.

[0089] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0090] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[0091] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort <u>its operation in order to execute the operation initiated by the MCH.</u> However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502

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may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[0092] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash–DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[0093] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM) 801. As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 803 and the other for the DRAM memory DRAM 805. The MCH 810 treats the DRAM 805 and Flash 803 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However,

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the on-DIMM data path 807 between Flash 803 and DRAM 805 allows for direct data transfer to occur between the Flash 803 and the DRAM 805 in response to control information from Ctrl 830. In this embodiment, this data transfer mechanism provides direct support for executing commands from the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 803 to the DRAM 805. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[0094] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and

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DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[0095] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[0096] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory

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space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[0097] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information

to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[0098] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[0099] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906

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and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502 monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00100] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks

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numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1060 field, a Block address 1050 field, a Plane address 1040, a Page address 1030, and a group of least significant address bits A_0A_1 1020. The Plane address 1040 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00101] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00102] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400μs, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such

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that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00103] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

((#of blocks per bank)/(ratio of 'Flash_block_write_time' to 'Flash_read_time'))*((Block usage time)/('Flash_block_write_time'))

[00104] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00105] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

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[00106] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

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CLAIMS

What is claimed is:

1. A memory module couplable to a memory controller of a host system, comprising:

a non-volatile memory subsystem;

a data manager coupled to the non-volatile memory subsystem;

a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and

a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

2. The memory module of claim 1, wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

3. The memory module of claim 1, wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

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4. The memory module of claim 3, wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

5. The memory module of claim 1, wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

6. The memory module of claim 1, wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

7. The memory module of claim 6, wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

8. The memory module of claim 7, wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

9. The memory module of claim 1, wherein the volatile memory subsystem comprises DRAM memory.

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10. The memory module of claim 7, wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

11. The memory module of claim 6, wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

12. The memory module of 11, wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

13. A method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems, the method comprising:

receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem;

identifying a data path to be used for transferring data to or from the memory module using the received control information; and

using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

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14. The method of claim 13, further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

15. The method of claim 13, further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

16. The memory module of claim 13, wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

17. The method of claim 15, further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

18. The method of claim 13, further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

19. The method of claim 18, further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

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20. The method of claim 13, further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

21. The method of claim 13, further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

22. The method of claim 21, wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

23. The method of claim 21, wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

24. The method of claim 13, further comprising:

operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system;

operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency.

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ABSTRACT

A memory module that is couplable to a memory controller hub (MCH) of a host system includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive read/write commands from the MCH and to direct transfer of data between any two or more of the MCH, the volatile memory subsystem, and the non-volatile memory subsystem based on the commands.

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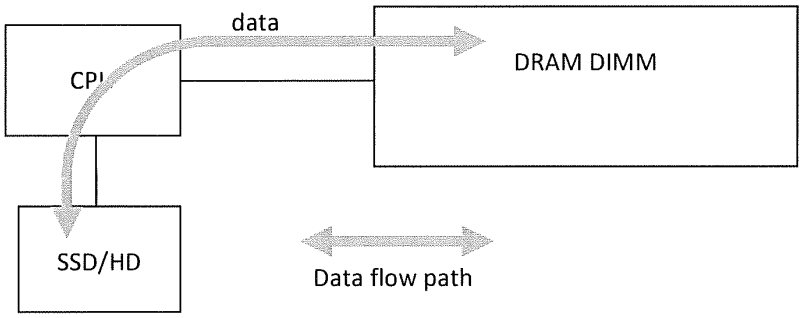


FIG. 1
(PRIOR ART)

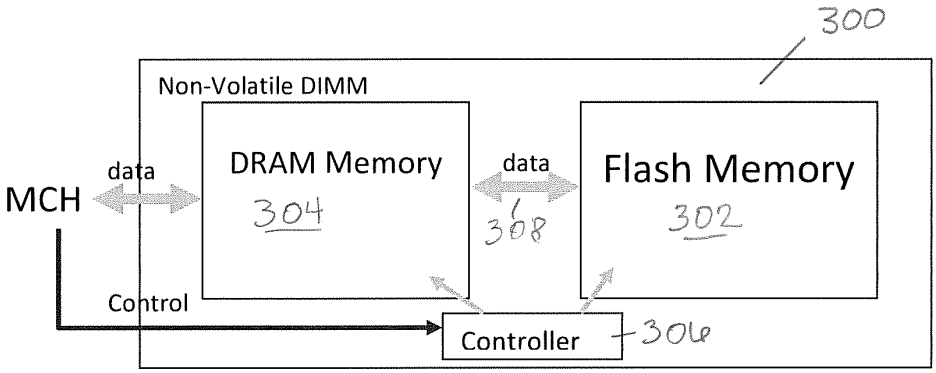
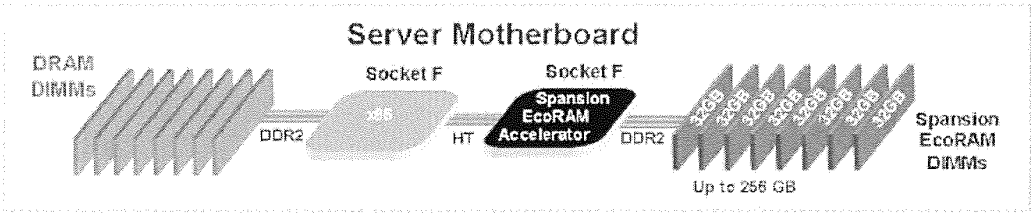


FIG. 3A

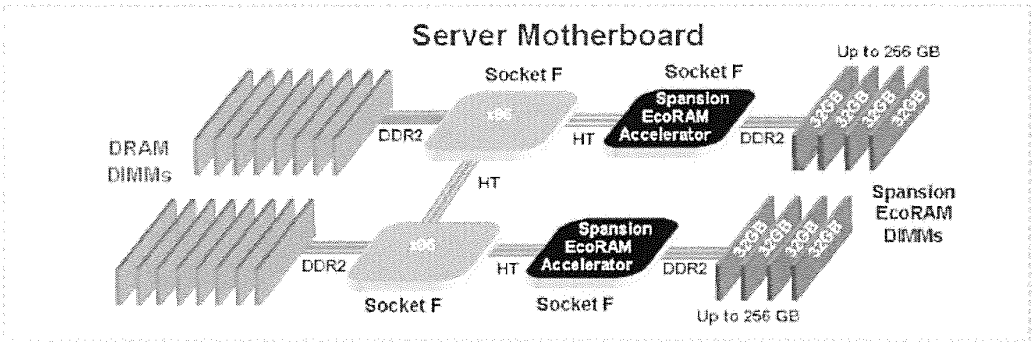
Spansion EcoRAM Configurations

256GB Spansion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

256 GB Spanison EcoRAM Solution – Dual Accelerator



256GB Dual Accelerator Spansion EcoRAM Solution

FIG. 2
(PRIOR ART)

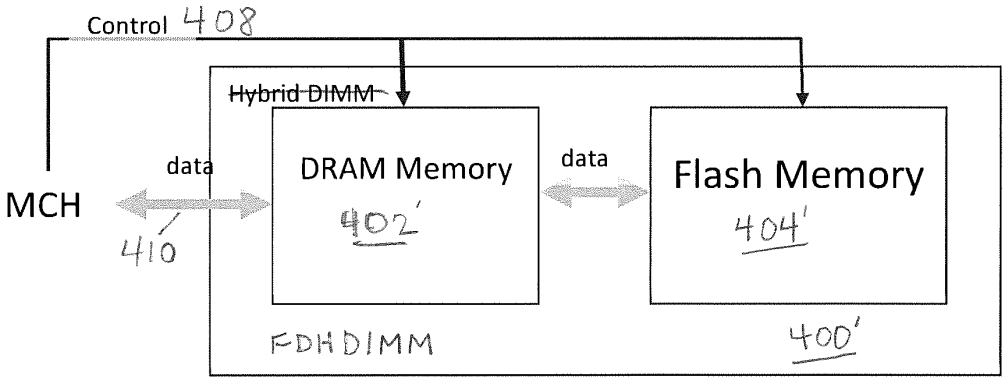


FIG. 4B

FIG. 3B

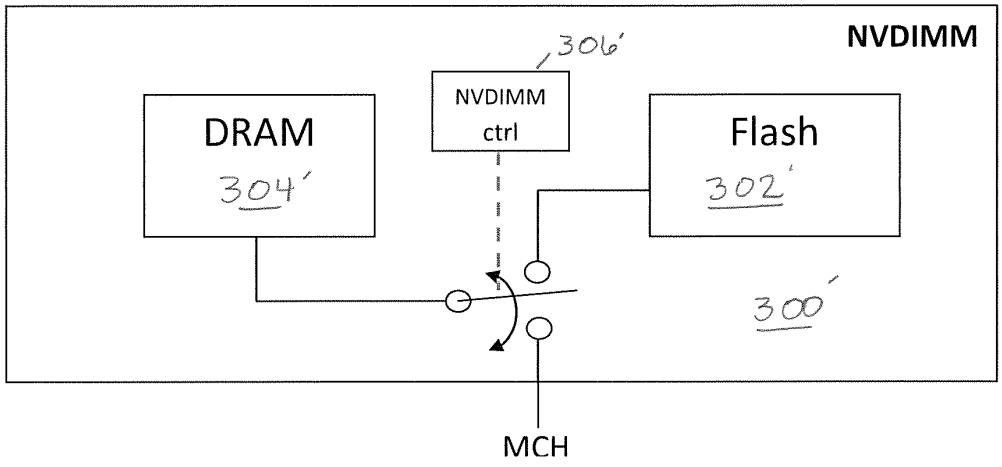
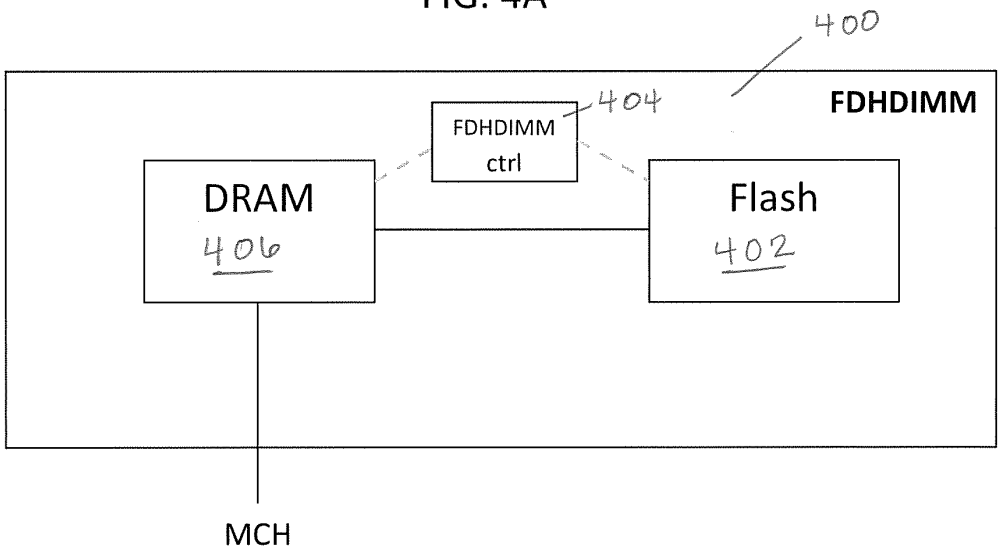

NVDIMM
306'
NVDIMM
ctrl
DRAM
304'
Flash
302'
300'
MCH

FIG. 4A


400
FDHDIMM
404
FDHDIMM
ctrl
DRAM
406
Flash
402
MCH

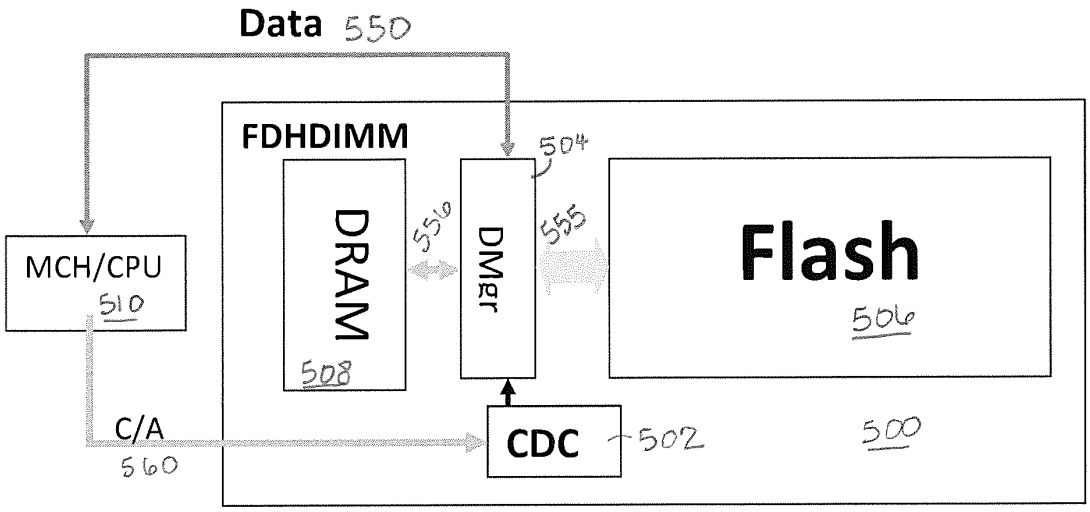

Data 550
FDHDIMM
504
DRAM
508
550
DMgr
555
Flash
506
MCH/CPU
510
C/A
560
CDC
502
500

FIG. 5A

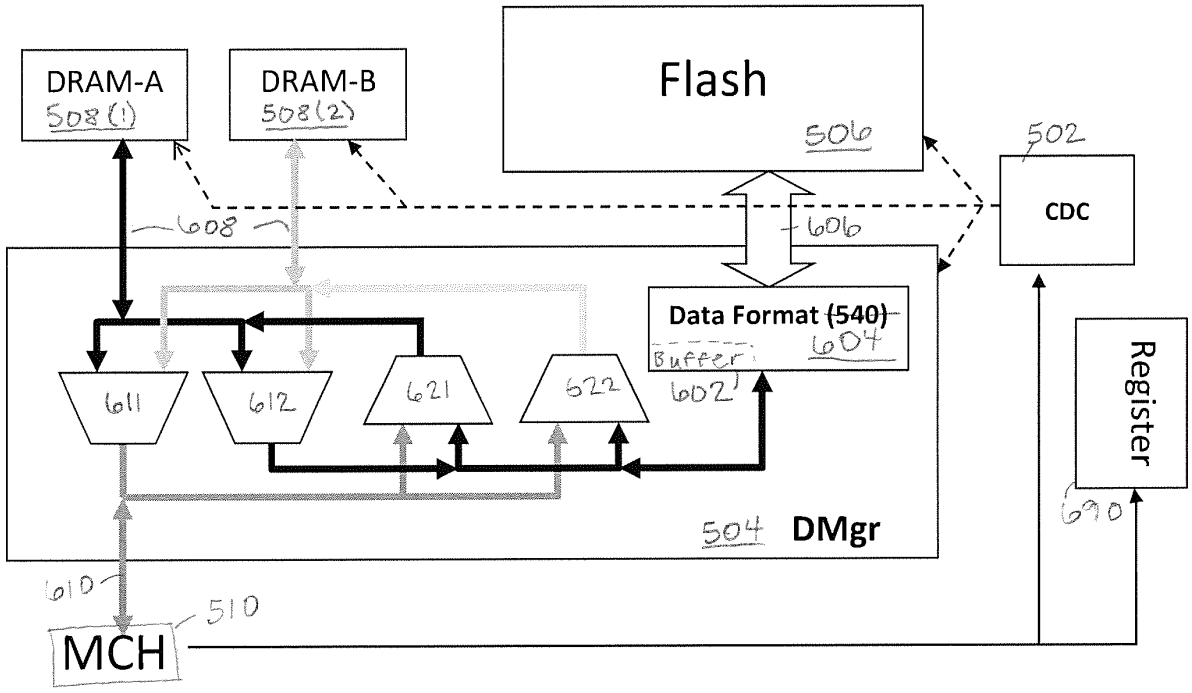
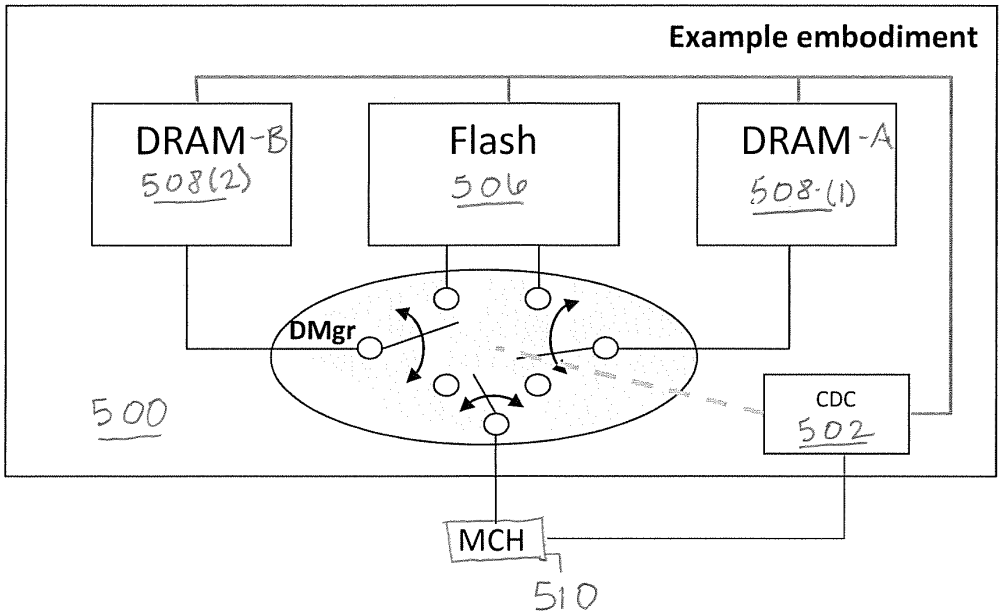

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
502
CDC
608
606
Data Format (540)
604
Buffer
602
611
612
621
622
Register
690
504 DMgr
610
510
MCH

FIG. 6

FIG. 5B


Example embodiment
DRAM-B
508(2)
Flash
506
DRAM-A
508-(1)
DMgr
500
CDC
502
MCH
510

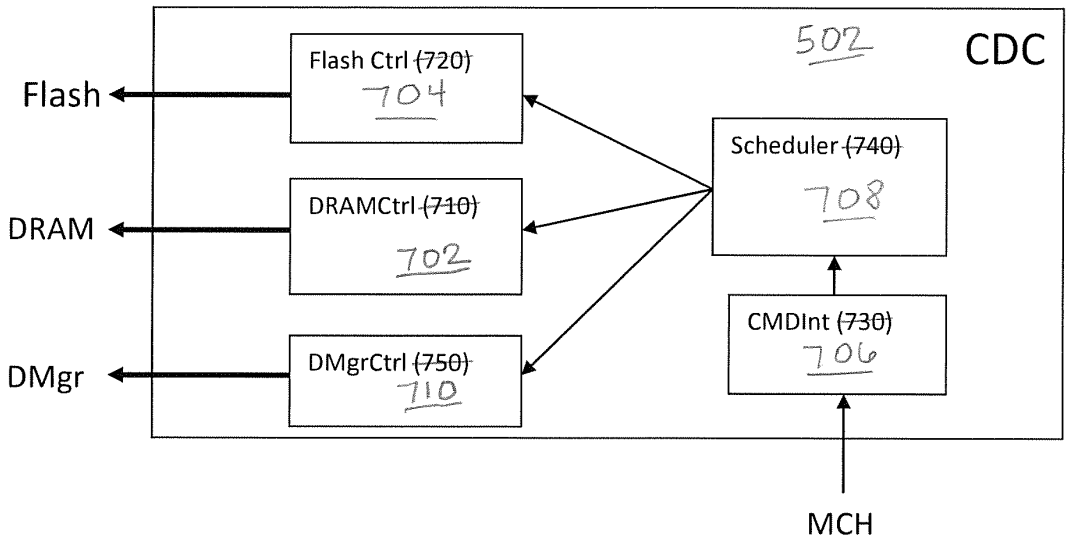


FIG. 7

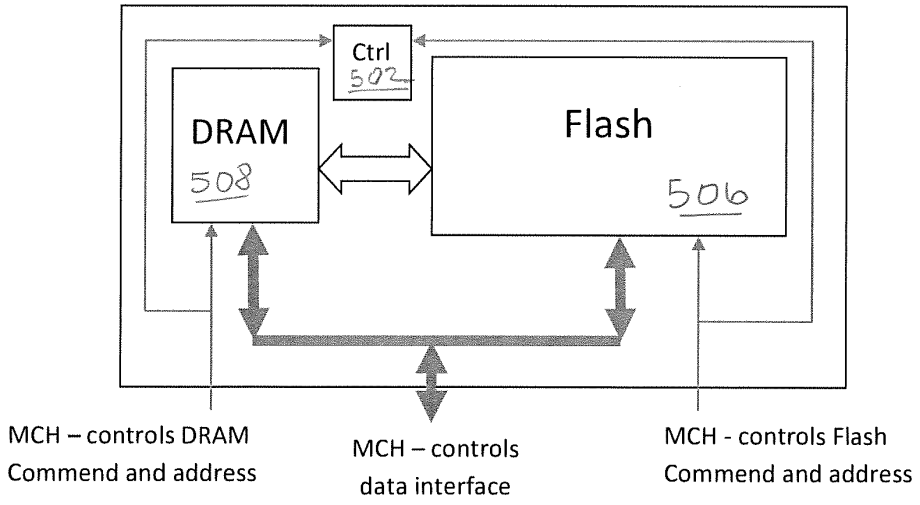


Figure 8A

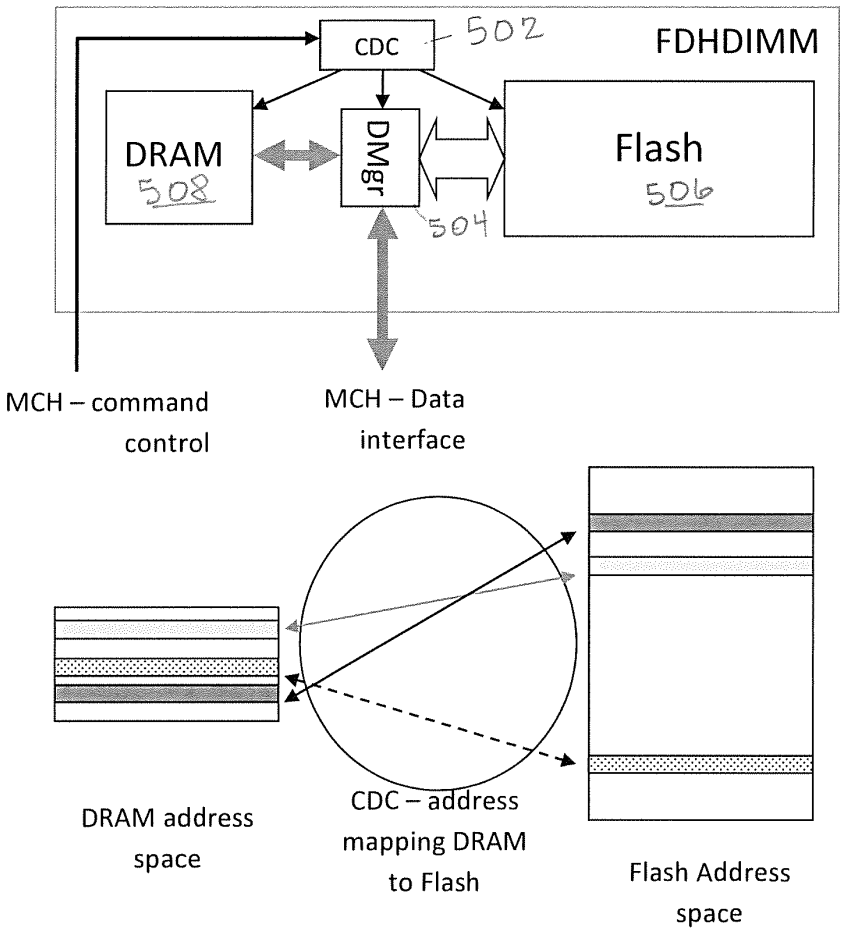

CDC
502
FDHDIMM
DRAM
508
DMgr
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

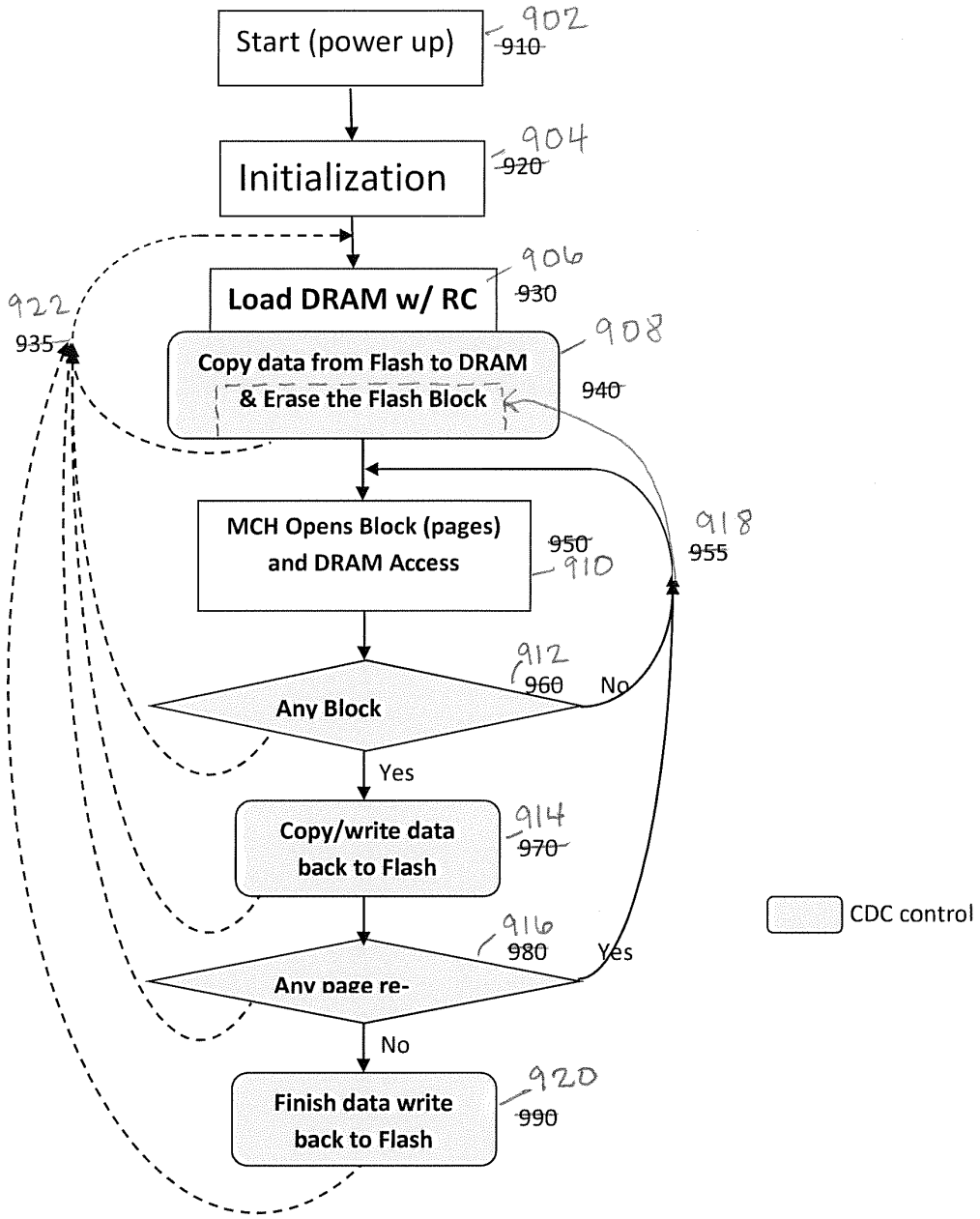

Start (power up)
902
910
Initialization
904
920
Load DRAM w/ RC
906
930
922
935
Copy data from Flash to DRAM
& Erase the Flash Block
908
940
MCH Opens Block (pages)
and DRAM Access
950
910
918
955
Any Block
912
960
No
Yes
Copy/write data
back to Flash
914
970
Any page re-
916
980
Yes
No
Finish data write
back to Flash
920
990
CDC control

FIG. 9

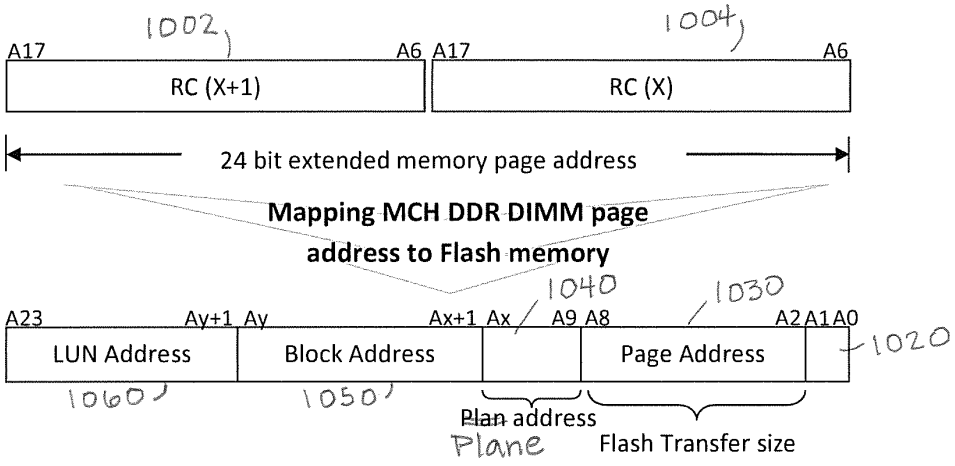

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1040
1030
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1
A0
1020
LUN Address
Block Address
Page Address
1060
1050
~~Plan~~ address
Plane
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr-time to rd-time ratio	Avg block use time (sec)	Flash write ~~tine~~ time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	062453-010
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.
This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Hyun		Lee	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Ladera Ranch	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i: US

Mailing Address of Applicant:

Address 1	21 THALIA ST		
Address 2			
City	Ladera Ranch	State/Province	CA
Postal Code	92694	Country i	US

Applicant 2 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Walnut	State/Province	CA	Country of Residence i	US

Citizenship under 37 CFR 1.41(b) i: TW

Mailing Address of Applicant:

Address 1	944 Crystal Water Lane		
Address 2			
City	Walnut	State/Province	CA
Postal Code	91789	Country i	US

Applicant 3 Remove

Applicant Authority ◉ Inventor ◯ Legal Representative under 35 U.S.C. 117 ◯ Party of Interest under 35 U.S.C. 118

Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	

Residence Information (Select One) ◉ US Residency ◯ Non US Residency ◯ Active US Military Service

City	Irvine	State/Province	CA	Country of Residence i	US

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	062453-010
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Citizenship under 37 CFR 1.41(b) i	US		
Mailing Address of Applicant:			
Address 1	6 Silver Fir		
Address 2			
City	Irvine	**State/Province**	CA
Postal Code	92604	**Country**i	US

Applicant 4 Remove

Applicant Authority	◉ Inventor	◯ Legal Representative under 35 U.S.C. 117	◯ Party of Interest under 35 U.S.C. 118	
Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Scott		Milton	
Residence Information (Select One)	◉ US Residency	◯ Non US Residency	◯ Active US Military Service	
City	Irvine	**State/Province**	CA	**Country of Residence** i US
Citizenship under 37 CFR 1.41(b) i	US			
Mailing Address of Applicant:				
Address 1	49 Statehouse Place			
Address 2				
City	Irvine	**State/Province**	CA	
Postal Code	92602	**Country**i	US	

Applicant 5 Remove

Applicant Authority	◉ Inventor	◯ Legal Representative under 35 U.S.C. 117	◯ Party of Interest under 35 U.S.C. 118	
Prefix	**Given Name**	**Middle Name**	**Family Name**	**Suffix**
	Jayesh		Bhakta	
Residence Information (Select One)	◉ US Residency	◯ Non US Residency	◯ Active US Military Service	
City	Cerritos	**State/Province**	CA	**Country of Residence** i US
Citizenship under 37 CFR 1.41(b) i	US			
Mailing Address of Applicant:				
Address 1	12220 Rose Street			
Address 2				
City	Cerritos	**State/Province**	CA	
Postal Code	90703	**Country**i	US	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button. Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.
For further information see 37 CFR 1.33(a).

☐ **An Address is being provided for the correspondence Information of this application.**

Customer Number	46188

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	062453-010
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Email Address		Add Email	Remove Email

Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	062453-010	**Small Entity Status Claimed**	☐
Application Type	Nonprovisional		
Subject Matter	Utility		
Suggested Class (if any)		**Sub Class (if any)**	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	10	**Suggested Figure for Publication (if any)**	

Publication Information:

☐	Request Early Publication (Fee required at time of Request 37 CFR 1.219)
☐	**Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S. C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32).
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Please Select One:	◉ Customer Number	◯ US Patent Practitioner	◯ Limited Recognition (37 CFR 11.9)
Customer Number	46188		

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This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	non provisional of	61512871	2011-07-28
Prior Application Status	Pending		Remove
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)
	Continuation in part of	12240916	2008-09-29

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	062453-010
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

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Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove

Application Number	Country i	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			◯ Yes ◯ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button. Add

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1 Remove

If the Assignee is an Organization check here. ☒

Organization Name	Netlist, Inc.		
Mailing Address Information:			
Address 1	51 Discovery, Suite 150		
Address 2			
City	Irvine	**State/Province**	CA
Country i	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the **Add** button. Add

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/			Date (YYYY-MM-DD)	2012-07-26
First Name	Khaled	Last Name	Shami	Registration Number	38745

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Application Data Sheet 37 CFR 1.76	Attorney Docket Number	062453-010
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

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Electronic Patent Application Fee Transmittal

Application Number:	
Filing Date:	
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Utility application filing	1011	1	380	380
Utility Search Fee	1111	1	620	620
Utility Examination Fee	1311	1	250	250
Pages:				
Claims:				
Claims in excess of 20	1202	4	60	240
Miscellaneous-Filing:				
Petition:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
			Total in USD ($)	**1490**

Electronic Acknowledgement Receipt

EFS ID:	13353335
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	26-JUL-2012
Filing Date:	
Time Stamp:	19:31:36
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$1490
RAM confirmation Number	6870
Deposit Account	503557
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_010_Spec.pdf	202079 c60dd948101904d70a8443a4a64c47ae69da3e71	yes	44
	Multipart Description/PDF files in .zip description				
	Document Description		**Start**	**End**	
	Specification		1	37	
	Claims		38	43	
	Abstract		44	44	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	062453_010_Drawings.pdf	190034 073f5c7db3f6af50483c4ffbc3e361c5806bb3acf	no	10
Warnings:					
Information:					
3	Application Data Sheet	data_sheet.pdf	1537065 c32664fd53e98c643bf5c173e5101bfce57e9255	no	6
Warnings:					
Information:					
4	Fee Worksheet (SB06)	fee-info.pdf	36510 9f8fce9ec382ceb6b6db27f9144ce79078ff5de5	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	1965688		

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

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If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/559,476	07/26/2012	2189	1490	062453-010	24	2

CONFIRMATION NO. 1046

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

FILING RECEIPT

OC000000055837050

Date Mailed: 08/13/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: None

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008

Foreign Applications (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.)

If Required, Foreign Filing License Granted: 08/07/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/559,476**

Projected Publication Date: To Be Determined - pending completion of Missing Parts

Non-Publication Request: No

Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as

set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/559,476

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	380
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 60 =	240
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1490

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/559,476	07/26/2012	Hyun Lee	062453-010

CONFIRMATION NO. 1046

FORMALITIES LETTER

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

OC000000055837051

Date Mailed: 08/13/2012

NOTICE TO FILE MISSING PARTS OF NONPROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(b)

Filing Date Granted

Items Required To Avoid Abandonment:

An application number and filing date have been accorded to this application. The item(s) indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The oath or declaration is missing.
  A properly signed oath or declaration in compliance with 37 CFR 1.63, identifying the application by the above Application Number and Filing Date, is required.
  Note: If a petition under 37 CFR 1.47 is being filed, an oath or declaration in compliance with 37 CFR 1.63 signed by all available joint inventors, or if no inventor is available by a party with sufficient proprietary interest, is required.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- A surcharge (for late submission of filing fee, search fee, examination fee or oath or declaration) as set forth in 37 CFR 1.16(f) of $**130** for a non-small entity, must be submitted.

SUMMARY OF FEES DUE:

Total fee(s) required within **TWO MONTHS** from the date of this Notice is $**130** for a non-small entity
- $**130** Surcharge.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 70

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at http://www.uspto.gov/ebc.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/eggolla/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee.	CONFIRMATION NO.: 1046
APPLICATION NO.:	13/559,476	
FILING DATE:	July 26, 2012	
TITLE:	FLASH-DRAM HYBRID MEMORY MODULE	
EXAMINER:	unassigned	
ART UNIT:	unassigned	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Remarks begin on page **3** of this paper.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 72

In the Specification

Please amend paragraph [0001] as follows:

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, ~~titled "HIGH-DENSITY DIMMS",~~ and of U.S. patent application serial 13/559,476, filed July 26, 2012,~~and~~which is a continuation-in-part (CIP) of US patent application serial no. 12/240,916, filed September 29, 2008 ~~, titled "NON-VOLATILE MEMORY MODULE"~~which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of ~~both~~all of which are incorporated herein by reference in their entirety.

This application may also be considered to be related to co-pending U.S. patent application serial no. 13/536,173, filed on June 28, 2012, and commonly owned herewith.

REMARKS

The specification has been amended to more accurately reflect priority and related application information.

Early consideration and allowance of this application is earnestly solicited.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: August 20, 2012

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
FAX. (650) 320-7701

Samsung Electronics Co., Ltd.
Ex. 1009, p. 74

Electronic Acknowledgement Receipt

EFS ID:	13539422
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	20-AUG-2012
Filing Date:	26-JUL-2012
Time Stamp:	18:21:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_010_Prelim_amendment.pdf	116869 078f71fa178386ecc77a09770b11ebcf0f28bc89	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3
Warnings:			
Information:			
	Total Files Size (in bytes):	116869	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4420821		1983-12-13	Hoffman	
	2	4449205		1984-05-15	Hoffman	
	3	5519663		1996-05-21	Harper, Jr. et al.	
	4	6158015		2000-12-05	Klein	
	5	6336174	B1	2002-01-01	Li et al.	
	6	6336176	B1	2002-01-01	Leyda et al.	
	7	6487623	B1	2002-11-26	Emerson et al.	
	8	6658507	B1	2003-12-02	Chan	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

	9	6799244	B2	2004-09-28	Tanaka et al.	
	10	7409590	B2	2008-08-05	Moshayedi et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020083368	A1	2002-06-27	Abe et al.	
	2	20040190210	A1	2004-09-30	Leete	
	3	20070192627	A1	2007-08-16	Oshikiri	
	4	20080195806	A1	2008-08-14	Cope	

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	1							☐

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action in U.S. Patent Application No. 12/240,916, mailed April 3, 2012.	☐
	2	Office Action in U.S. Patent Application No. 12/240,916, mailed February 1, 2012.	☐
	3	Office Action in U.S. Patent Application No. 12/240,916, mailed July 29, 2011.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2012-09-27
Name/Print	Khaled Shami	Registration Number	38,745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt

EFS ID:	13853673
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Tadas Narauskas
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	27-SEP-2012
Filing Date:	26-JUL-2012
Time Stamp:	14:19:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	062453-010_IDS_FORM.pdf	613227 6d6b8421757a2e96e22bbcda22ffe7e3b557d812	no	5

Warnings:

Information:

2	Non Patent Literature	OA_12240916_02-01-2012.pdf	478286 4c543efdb9b4cbd435ce0fe9eff687d64b283f53	no	14
Warnings:					
Information:					
3	Non Patent Literature	OA_12240916_04-03-2012.pdf	414082 45d9b1f93055200016b162ea2b824edecfefaf2a	no	12
Warnings:					
Information:					
4	Non Patent Literature	OA_12240916_07-29-2011.pdf	264654 1c9f68a01a64c8fec8e2c0d219a52aaa9c284d60	no	8
Warnings:					
Information:					
		Total Files Size (in bytes):	1770249		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

DECLARATION & POWER OF ATTORNEY

As a below-named inventor, I hereby declare that:

My correct city and state of residence, my post office address and my citizenship are stated below next to my name.

I believe myself to be an original and joint inventor of the subject matter which is disclosed and claimed and for which a patent is sought on the invention entitled:

"FLASH-DRAM HYBRID MEMORY MODULE"

The specification of this subject matter:

□ is attached hereto.
x was filed on July 26, 2012 as United States Application Number 13/559,476
x and was amended on August 20, 2012 (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified patent application, including the claims, as amended by any amendment(s) referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

PRIOR FOREIGN APPLICATION(S)			Priority Claimed		Certified Copy Attached?	
Number	Country	Month/Day/Year Filed	Yes	No	Yes	No
Number	Country	Month/Day/Year Filed	Yes	No	Yes	No

I hereby appoint practitioners associated with **Customer Number 46188** as attorneys of record with full power of substitution and revocation, to prosecute this application and transact all business in the United States Patent and Trademark Office connected therewith. If this application is assigned by me I agree and understand that the above-named attorneys will represent the assignee and not me.

Please send all correspondence and direct all telephone calls to the address associated with **Customer Number 46188**.

I, the undersigned, declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

FULL NAME OF INVENTOR 1	**FIRST Name**	**MIDDLE Initial(s)**	**LAST Name**
	HUYN		LEE
RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	LADERA RANCH	CALIFORNIA	US

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	21 THALIA ST.	LADERA RANCH	CA	92694

SIGNATURE	Date
	11/12/2012.

FULL NAME OF INVENTOR 2	FIRST Name	MIDDLE Initial(s)	LAST Name
	CHI-SHE		CHEN

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	WALNUT	CALIFORNIA	TW

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	944 CRYSTAL WATER LANE	WALNUT	CA	91789

SIGNATURE	Date
	Sep. 09, 2012

FULL NAME OF INVENTOR 3	FIRST Name	MIDDLE Initial(s)	LAST Name
	JEFFREY	C.	SOLOMON

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	IRVINE	CALIFORNIA	US

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	6 SILVER FIR	IRVINE	CA	92604

SIGNATURE	Date

FULL NAME OF INVENTOR 2	FIRST Name	MIDDLE Initial(s)	LAST Name
	CHI-SHE		CHEN

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	WALNUT	CALIFORNIA	TW

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	944 CRYSTAL WATER LANE	WALNUT	CA	91789

SIGNATURE	Date

FULL NAME OF INVENTOR 3	FIRST Name	MIDDLE Initial(s)	LAST Name
	JEFFREY	C.	SOLOMON

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	IRVINE	CALIFORNIA	US

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	16 SILVER FIR	IRVINE	CA	92604

SIGNATURE	Date
Jeffrey Solomon	11-12-2012

FULL NAME OF Name INVENTOR 4	FIRST Name	MIDDLE Initial(s)	LAST
SCOTT			MILTON

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	IRVINE	CALIFORNIA	US

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	49 STATEHOUSE PLACE	IRVINE	CA	92602

SIGNATURE	Date
Scott H. Milton	09/06/12

FULL NAME OF Name INVENTOR 5	FIRST Name	MIDDLE Initial(s)	LAST
JAYESH			BHAKTA

RESIDENCE AND CITIZENSHIP	City	State or Foreign Country	Country of Citizenship
	CERRITOS	CALIFORNIA	US

POST OFFICE ADDRESS	Number and Street	City	State or Country	Zip Code
	12220 ROSE STREET	CERRITOS	CA	90703

SIGNATURE	Date
Jayesh Bhakta	9/6/12

37 C.F.R. §1.56
Duty to disclose information material to patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1,97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and
(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or
(2) It refutes, or is inconsistent with, a position the applicant takes in:
(i) Opposing an argument of unpatentability relied on by the Office, or
(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;
(2) Each attorney or agent who prepares or prosecutes the application; and
(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.

Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late filing fee for oath or declaration	1051	1	130	130
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension - 1 month with $0 paid	1251	1	150	150
Miscellaneous:				
			Total in USD ($)	**280**

Electronic Acknowledgement Receipt

EFS ID:	14212528
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	13-NOV-2012
Filing Date:	26-JUL-2012
Time Stamp:	13:27:04
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$280
RAM confirmation Number	20035
Deposit Account	503557
Authorized User	
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Oath or Declaration filed	062453_010_Dec_and_POA.pdf	539426 6546714f83a331355ba19d601961fe0506dc5c84	no	6
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32225 63dc82500c4030088f04c95b9b587daca31c087e	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	571651	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

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<u>National Stage of an International Application under 35 U.S.C. 371</u>
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<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

U.S.PATENTS Remove

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8301833		2012-10-30	Chen et al.	

If you wish to add additional U.S. Patent citation information please click the Add button. Add

U.S.PATENT APPLICATION PUBLICATIONS Remove

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080104344		2008-05-01	Shimozono et al.	
	2	20100274953		2010-10-28	Lee et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button. Add

FOREIGN PATENT DOCUMENTS Remove

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button Add

NON-PATENT LITERATURE DOCUMENTS Remove

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report and Written Opinion in PCT/US12/48750, dated October 10, 2012	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2012-12-11
Name/Print	Khaled Shami	Registration Number	38,745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

KS

RECEIVED

OCT 15 2012

NIXON PEABODY LLP

PATENT COOPERATION TREATY

From the INTERNATIONAL SEARCHING AUTHORITY

To: Khaled Shami
P.O. Box 60610
Palo Alto, CA 94306
United States of America

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)* 10 OCT 2012
Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US12/48750	International filing date *(day/month/year)* 28 July 2012 (28.07.2012)
Applicant Netlist, Inc.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

   Filing of amendments and statement under Article 19:
   The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

   When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

   Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

   For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

   ☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

   ☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

   The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

   Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

   Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

   In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

   For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

RECEIVED

OCT 15 2012

NIXON PEABODY LLP

From the INTERNATIONAL SEARCHING AUTHORITY

To: Khaled Shami
P.O. Box 60610
Palo Alto, CA 94306
United States of America

PCT

NOTIFICATION OF TRANSMITTAL OF THE INTERNATIONAL SEARCH REPORT AND THE WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY, OR THE DECLARATION

(PCT Rule 44.1)

	Date of mailing *(day/month/year)*
Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION** See paragraphs 1 and 4 below
International application No. PCT/US12/48750	International filing date *(day/month/year)* 28 July 2012 (28.07.2012)
Applicant Netlist, Inc.	

1. ☒ The applicant is hereby notified that the international search report and the written opinion of the International Searching Authority have been established and are transmitted herewith.

Filing of amendments and statement under Article 19:
The applicant is entitled, if he so wishes, to amend the claims of the international application (see Rule 46):

When? The time limit for filing such amendments is normally two months from the date of transmittal of the international search report.

Where? Directly to the International Bureau of WIPO, 34 chemin des Colombettes 1211 Geneva 20, Switzerland, Facsimile No.: +41 22 338 82 70

For more detailed instructions, see *PCT Applicant's Guide*, International Phase, paragraphs 9.004 – 9.011.

2. ☐ The applicant is hereby notified that no international search report will be established and that the declaration under Article 17(2)(a) to that effect and the written opinion of the International Searching Authority are transmitted herewith.

3. ☐ **With regard to any protest** against payment of (an) additional fee(s) under Rule 40.2, the applicant is notified that:

☐ the protest together with the decision thereon has been transmitted to the International Bureau together with any request to forward the texts of both the protest and the decision thereon to the designated Offices.

☐ no decision has been made yet on the protest; the applicant will be notified as soon as a decision is made.

4. **Reminders**

The applicant may submit comments on an informal basis on the written opinion of the International Searching Authority to the International Bureau. The International Bureau will send a copy of such comments to all designated Offices unless an international preliminary examination report has been or is to be established. Following the expiration of 30 months from the priority date, these comments will also be made available to the public.

Shortly after the expiration of **18 months** from the priority date, the international application will be published by the International Bureau. If the applicant wishes to avoid or postpone publication, a notice of withdrawal of the international application, or of the priority claim, must reach the International Bureau before the completion of the technical preparations for international publication (Rules 90*bis*.1 and 90*bis*.3).

Within **19 months** from the priority date, but only in respect of some designated Offices, a demand for international preliminary examination must be filed if the applicant wishes to postpone the entry into the national phase **until 30 months** from the priority date (in some Offices even later); otherwise, the applicant must, **within 20 months** from the priority date, perform the prescribed acts for entry into the national phase before those designated Offices.

In respect of other designated Offices, the time limit of **30 months** (or later) will apply even if no demand is filed within 19 months.

For details about the applicable time limits, Office by Office, see www.wipo.int/pct/en/texts/time_limits.html and the *PCT Applicant's Guide*, National Chapters.

Name and mailing address of the ISA/ Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer Shane Thomas PCT Helpdesk: 571-272-4300 Telephone No. PCT OSP: 571-272-7774

Form PCT/ISA/220 (July 2010)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL SEARCH REPORT

(PCT Article 18 and Rules 43 and 44)

Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION**	see Form PCT/ISA/220 as well as, where applicable, item 5 below.
International application No. PCT/US12/48750	International filing date *(day/month/year)* 28 July 2012 (28.07.2012)	(Earliest) Priority Date *(day/month/year)* 28 July 2011 (28.07.2011)
Applicant Netlist, Inc.		

This international search report has been prepared by this International Searching Authority and is transmitted to the applicant according to Article 18. A copy is being transmitted to the International Bureau.

This international search report consists of a total of 2 sheets.

☐ It is also accompanied by a copy of each prior art document cited in this report.

1. **Basis of the report**
   a. With regard to the **language**, the international search was carried out on the basis of:
      ☒ the international application in the language in which it was filed.
      ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).
   b. ☐ This international search report has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43.6*bis*(a)).
   c. ☐ With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, see Box No. I.
2. ☐ **Certain claims were found unsearchable** (see Box No. II).
3. ☐ **Unity of invention is lacking** (see Box No. III).
4. With regard to the **title**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established by this Authority to read as follows:
5. With regard to the **abstract**,
   ☒ the text is approved as submitted by the applicant.
   ☐ the text has been established, according to Rule 38.2, by this Authority as it appears in Box No. IV. The applicant may, within one month from the date of mailing of this international search report, submit comments to this Authority.
6. With regard to the **drawings**,
   a. the figure of the **drawings** to be published with the abstract is Figure No. 5
      ☒ as suggested by the applicant.
      ☐ as selected by this Authority, because the applicant failed to suggest a figure.
      ☐ as selected by this Authority, because this figure better characterizes the invention.
   b. ☐ none of the figures is to be published with the abstract.

Form PCT/ISA/210 (first sheet) (July 2009)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US12/48750

A. CLASSIFICATION OF SUBJECT MATTER
IPC(8) - G06F 12/00 (2012.01)
USPC - 711/118, 103
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC(8): G06F 12/00, 12/08, 13/16 (2012.01)
USPC: 711/170, 104, 118, 103

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
MicroPatent (US-G, US-A, EP-A, EP-B, WO, JP-bib, DE-C,B, DE-A, DE-T, DE-U, GB-A, FR-A); DialogPRO; IEEE/IEEEXplore; Google/Google Scholar; IP.com; volatile, non-volatile, memory, controller, manager, performance, frequency, clock, plural, multiple, port, segment, subset

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X -- Y	US 2008/0104344 A1, (SHIMOZONO, N., et al.), May 1, 2008, figures 19, paragraphs [0017], [0053], [0055], [0057], [0061], [0065], [0067], [0080]	1-6, 9, 11-15, 18-23 ---------- 7, 8, 10, 16, 17, 24
Y	US 2010/0274953 A1, (LEE, T., et al.), October 28, 2010, figures 1, 2, 4B, 10, paragraphs [0005], [0007], [0046], [0053], [0058], [0062], [0065], [0066], [0071], [0080], [0115]	7, 8, 10, 16, 17, 24

☐ Further documents are listed in the continuation of Box C. ☐

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
21 September 2012 (21.09.2012)	10 OCT 2012
Name and mailing address of the ISA/US Mail Stop PCT, Attn: ISA/US, Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	Authorized officer: Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/210 (second sheet) (July 2009)

KS

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: Khaled Shami
P.O. Box 60610
Palo Alto, CA 94306
United States of America

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	10 OCT 2012
Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US12/48750	28 July 2012 (28.07.2012)	28 July 2011 (28.07.2011)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 12/00 (2012.01)
USPC - 711/118, 103

Applicant Netlist, Inc.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1 *bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Fom PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	21 September 2012 (21.09.2012)	Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [x] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:

   a. (means)
   - [ ] on paper
   - [ ] in electronic form

   b. (time)
   - [ ] in the international application as filed
   - [ ] together with the international application in electronic form
   - [ ] subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

Samsung Electronics Co., Ltd.
Ex. 1009, p. 103

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	7, 8, 10, 16, 17, 24	YES
	Claims	1-6, 9, 11-15, 18-23	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-24	NO
Industrial applicability (IA)	Claims	1-24	YES
	Claims	NONE	NO

2. Citations and explanations:

Claims 1-6, 9, 11-15 and 18-23 lack novelty under PCT Article 33(2) as being anticipated by US 2008/0104344 A1, SHIMOZONO, N., et al (hereinafter 'Shimozono').

As per Claim 1, Shimozono discloses a memory module (storage system 101 (a memory module), Figure 19, paragraph [0053]) couplable to a memory controller of a host system (is connected to storage system input/output (memory controller) of host 200 through front end I/F 307, Figure 19, paragraphs [0017] and [0080]), comprising: a non-volatile memory subsystem (non-volatile memory 313 (non-volatile memory subsystem), NM, Figure 19, paragraph [0055]); a data manager coupled to the non-volatile memory subsystem (microprocessor 303, MP, comprising the functionality of a data manager, is connected to non-volatile memory 313, through switch 309, SW, Figure 19, paragraph [0055]); a volatile memory subsystem coupled to the data manager (cache memory 311, CM, is volatile memory (a volatile memory subsystem) connected to microprocessor 303 through switch 309, SW, Figure 19, paragraphs [0055] and [0057]) and operable to exchange data with the non-volatile memory subsystem by way of the data manager (microprocessor 303 can copy data on the volatile memory, CM311, to the non-volatile memory 313, paragraphs [0055], [0057], [0065]); and a controller operable to receive commands from the memory controller (controller 301 communicates with the storage system input/output (the memory controller) of host 200 and uses microprocessor 303 to process read and write commands, paragraphs [0017], [0055], [0056], [0061]) and to direct (i) operation of the non-volatile memory subsystem (processes read and write commands with non-volatile memory 313, paragraphs [0055], [0065], [0067]), (ii) operation of the volatile memory subsystem (processes read and write commands with volatile memory 311, paragraphs [0055], [0057], [0065], [0067]), and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller (based on a read command from the storage system input/output (memory controller) of host 200, transmits data between volatile memory 311 and non-volatile memory 313 with the storage system input/output of host 200, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 2, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller (microprocessor 303 (the data manager) processes commands received from the storage system input/output (the memory controller) of host 200 and allocates the volatile memory into a fixed length segment size (controls data buffer size), paragraphs [0017], [0057], [0061], [0114]).

As per Claim 3, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller (microprocessor 303 (the data manager) specifies the access address information from the read and write commands of the storage system input/output (the memory controller) of host 200 and controls the transmission of data (controls data traffic) between volatile memory 311, non-volatile memory 313, and the storage system input/output of host 200, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 4, Shimozono discloses the memory module of claim 3; additionally, Shimozono discloses wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer (microprocessor 303 processes host 200 commands indicating the type of command, transfer address, and transfer length (data transfer size), paragraphs [0055], [0061], [0083]).

As per Claim 5, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module (the host 200 through the storage system input/output (the memory controller) can control the memory regions of volatile sub-regions (a first memory address space of the volatile memory subsystem) and non-volatile sub-regions (a second memory address space of the non-volatile memory subsystem), in units called host volumes when the microprocessor executes commands from the controller 301 regarding the configuration of the memory regions, paragraph [0017], [0055]-[0059], [0086], [0102]).

As per Claim 6, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager is configured as a bidirectional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems (microprocessor 303 (the data manager) provides read and write command processing with the storage system input/output of host 200 by utilizing one or more ports (two or more sets of data ports) to the volatile cache memory of the multiplexed storage devices (a bidirectional data transfer fabric), paragraphs [0017], [0061], [0077], claim 15).
-***-Continued Within the Next Supplemental Box-***-

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
-***-Continued from Box No. V: Citations and Explanations-***-

As per Claim 9, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the volatile memory subsystem comprises DRAM memory (CM 311 is volatile memory may be DRAM, Dynamic Random Access Memory, paragraph [0057]).

As per Claim 11, Shimozono discloses the memory module of claim 6; additionally, Shimozono discloses wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller (microprocessor 303 (the data manager) processes volatile memory 311 and non-volatile memory 313 commands between the storage system input/output (the memory controller) of host 200, using Fiber Channel Protocol, Ethernet and iSCSI, Internet Small Computer System Interface, protocols (a data format module to format data), paragraphs [0017], [0057], [0061], [0077], [0078]).

As per Claim 12, Shimozono discloses the memory module of 11; additionally, Shimozono discloses wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem (microprocessor 303 (the data manager) copies volatile memory 311 to the non-volatile cache region 391 (data buffer for buffering data) of the non-volatile memory 313, Figure 19, paragraphs [0055], [0057], [0068]).

As per Claim 13, Shimozono discloses a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems (a process of receiving commands on storage system 101 (a memory module) from storage system input/output (a memory controller) of host 200 and reading or writing data to volatile memory 311 and non-volatile memory 313, Figure 19, paragraph [0017], [0055], [0057], [0061]), the method comprising: receiving control information from the memory controller (commands are transceived between the storage system input/output (the memory controller) of host 200 and storage system 101 using a selected protocol, paragraphs [0017], [0077]-[0079]), wherein the control information is received using a protocol of the volatile memory subsystem (using the protocol, the storage system 101 provides volatile memory, CM 311 sub-regions, for processing read and write commands and data, paragraphs [0057], [0065], [0067] [0077]); identifying a data path to be used for transferring data to or from the memory module using the received control information (microprocessor 303 specifies access address information (identifying a data path) from the read and write commands sent from storage system input/output (the memory controller) of host 200, paragraph [0017], [0055], [0065], [0067]); and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path (storage system 101 (the memory module) comprises controller 301 and using microprocessor 303, recognized as comprising the functionality of a data manager, specifies access address information (the identified data path) and transmits data between volatile memory 311 and non-volatile memory 313 with the storage system input/output (the memory controller) of host 200, Figure 19, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 14, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data (microprocessor 303 (the data manager) processes commands received from the storage system input/output (the memory controller) of host 200 and allocates the volatile memory into a fixed length segment size (controls data buffer size), paragraphs [0017], [0057], [0061], [0114]).

As per Claim 15, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising operating the data manager as a bidirectional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems (microprocessor 303 (the data manager) provides read and write command processing with the storage system input/output of host 200 by utilizing one or more ports (two or more sets of data ports) to the volatile cache memory of the multiplexed storage devices (a bidirectional data transfer fabric), paragraphs [0017], [0061], [0077], claim 15).

As per Claim 18, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller (microprocessor 303 (the data manager) copies data from volatile memory 311 to non-volatile memory 313 and to volatile memory from non-volatile memory 313 (directing transfer of data bi-directionally) using the access address information from the storage system input/output (the memory controller) of host 200, [0017], [0055]-[0058]).

As per Claim 19, Shimozono discloses the method of claim 18; additionally, Shimozono discloses further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem (microprocessor 303 processes the commands received from the storage system input/output (the memory controller) of host 200 in volatile memory 311 and copy the data to non-volatile memory 313 by executing the specific computer program, paragraphs [0017], [0055], [0057], [0061], [0065]).

As per Claim 20, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and nonvolatile memory subsystems (controller 301 comprises an access control unit in storage system 101 and when executed by microprocessor 303, allows memory to be used (memory access control), Figure 19, paragraphs [0014] and [0055]).

As per Claim 21, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value (the host 200 through the storage system input/output (the memory controller) can control the memory regions of volatile sub-regions and non-volatile sub-regions (configure memory space) in units called host volumes through the microprocessor executing commands from the controller 301 regarding the configuration of the memory regions, paragraph [0017], [0055]-[0059], [0086], [0102]).
-***-Continued Within the Next Supplemental Box-***-

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
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-***-Continued from Previous Supplemental Box-***-

As per Claim 22, Shimozono discloses the method of claim 21; additionally, Shimozono discloses wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller (controller 301 executes a program with microprocessor 303 to control volatile memory 311 or non-volatile memory 313 sub-region address information (configures the memory space using a first portion of the memory subsystem) in storage system 101 (the memory module) by converting the access address information designated in an access address command (the controller presents a unified memory space) from the storage system input/output (the memory controller) of host 200, Figure 19, paragraphs [0017], [0055], [0057], [0058]).

As per Claim 23, Shimozono discloses the method of claim 21; additionally, Shimozono discloses wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific (microprocessor executes the controller 301 cache control program 454 to control the forming of volatile memory 311 sub-region in storage system 101 (configures the memory space in the memory module), based on the command processing program 451 and the RAID control program 453 (instructions that are application-specific), Figures 3 and 19, paragraphs [0057], [0102]-[0106]).

Claims 7, 8, 10, 16, 17 and 24 lack an inventive step under PCT Article 33(3) as being obvious over Shimozono in view of US 2010/0274953 A1, LEE, T., et al (hereinafter 'Lee').

As per Claim 7, Shimozono discloses the memory module of claim 6. Shimozono does not disclose wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments. Lee discloses wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments (the memory system of solid state disk 120 comprises a non-volatile, flash memory interface 240 connected to a plurality of non-volatile flash memory devices groups 123 through 125 (non-volatile memory subsystem), each containing memory devices (one or more memory segments), Figures 1 and 2, paragraphs [0007] and [0046]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

As per Claim 8, Shimozono, in combination with Lee, discloses the memory module of claim 7; additionally, Lee discloses wherein each memory segment comprises at least one memory circuit, memory device, or memory die (each of the memory device groups 123 through 125 contains memory devices MEM_11 through MEM_1m, which may be NAND flash memory devices, Figure 3, paragraphs [0058] and [0071]).

As per Claim 10, Shimozono, in combination with Lee, discloses the memory module of claim 7; additionally, Lee discloses wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems (solid state disk controller 121 (the data manager) can activate some or all (independently and/or concurrently) of the channels (one set of data ports) to the non-volatile memory devices (non-volatile memory subsystem) for read and write transfer control, paragraphs [0053] and [0062]).

As per Claim 16, Shimozono discloses the memory module of claim 13. Shimozono does not disclose wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments. Lee discloses wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments (the memory system of solid state disk 120 comprises a non-volatile, flash memory interface 240 connected to a plurality of non-volatile flash memory devices groups 123 through 125 (non-volatile memory subsystem), each containing memory devices (one or more memory segments), Figures 1 and 2, paragraphs [0007] and [0046]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

As per Claim 17, Shimozono discloses the method of claim 15. Shimozono does not disclose further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or nonvolatile memory subsystems. Lee discloses further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or nonvolatile memory subsystems (solid state disk controller 121 (the data manager) can activate some or all (independently and/or concurrently) of the channels (one set of data ports) to the non-volatile memory devices (non-volatile memory subsystem) for read and write transfer control, paragraphs [0053] and [0062]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

-***-Continued Within the Next Supplemental Box-***-

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:

-***-Continued from Previous Supplemental Box-***-

As per Claim 24, Shimozono discloses the method of claim 13. Shimozono does not disclose further comprising: operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency. Lee discloses further comprising: operating the volatile memory subsystem at a first clock frequency, when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system (SDRAM, volatile buffer memory 522 (the volatile memory subsystem) clock frequencies, fb, (a first clock frequency) are controlled by different internal clock signals in the solid state disk 520 (the memory system) when temporarily storing data involving read and write operations with host 510 (the host system), Figures 4B and 10, paragraphs [0065], [0080], [0115]); operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem (the flash clock frequency, fi, (a second clock frequency) controls the rate of the non-volatile flash interface 240 for exchanging data between the SDRAM volatile buffer memory 122 (the volatile memory subsystem) and the non-volatile flash memory device groups (non-volatile memory subsystem), Figure 4B, paragraphs [0005], [0066], [0080]); and operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency (solid state disk (the memory system) controller 121 can adjust the clock frequency driving SDRAM volatile memory 122 (the volatile memory subsystem) by lowering its clock frequency (the third clock frequency being less than the first clock frequency) to reduce its power consumption, when activating some or all of the non-volatile flash memory device groups (the second mode of operation), paragraphs [0005], [0053], [0065]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of selective component clock frequencies. The suggestion/motivation for doing so would have been to provide a method to lower clock frequencies of selective components to enable better power consumption and redirect the limited available power to other storage components to ensure proper data storage and retention.

Claims 1-24 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

Electronic Acknowledgement Receipt

EFS ID:	14430454
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	10-DEC-2012
Filing Date:	26-JUL-2012
Time Stamp:	19:25:20
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453_010_preliminary_2.pdf	115826 3af9e0a4c1857da157bf9ae528c0ba4df3e9d7f9	yes	3

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Specification	2	2
	Applicant Arguments/Remarks Made in an Amendment	3	3

Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	062453-010_IDS_FORM.pdf	612328 fc61e91c21cd5d37de2144fd901556a94dcecfd7	no	4
Warnings:					
Information:					
3	Non Patent Literature	062453_0011_ISR.pdf	1134384 2ec404a332aec427be1b2f18b7d1df7a3581fd41	no	10
Warnings:					
Information:					
		Total Files Size (in bytes):	1862538		

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

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If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee	CONFIRMATION NO.: 1046
APPLICATION NO.:	13/559,476	
FILING DATE:	July 26, 2012	
TITLE:	FLASH-DRAM HYBRID MEMORY MODULE	
EXAMINER:	unassigned	
ART UNIT:	2189	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

Please amend the above-identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Remarks begin on page **3** of this paper.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 110

In the Specification

Please amend paragraph [0001] as follows:

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, and ~~of U.S. patent application serial 13/559,476, filed July 26, 2012,which is a continuation-in-part (CIP)~~ of US patent application serial no. 12/240,916, filed September 29, 2008 which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

This application may also be considered to be related to co-pending U.S. patent application serial no. 13/536,173, filed on June 28, 2012, and commonly owned herewith.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 111

REMARKS

The specification has been amended to more accurately reflect priority and related application information.

Early consideration and allowance of this application is earnestly solicited.

Please charge any additional required fees, including those necessary to obtain extensions of time to render timely the filing of the instant Amendment and/or Reply to Office Action, or credit any overpayment not otherwise credited, to our deposit account no. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: December 10, 2012

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
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Samsung Electronics Co., Ltd.
Ex. 1009, p. 112

PTO/SB/06 (07-06)
Approved for use through 1/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number	Filing Date	
13/559,476	07/26/2012	☐ To be Mailed

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY ☐ RATE ($)	SMALL ENTITY FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =		OR	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =			X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT 12/10/2012

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 24	Minus	** 20	= 4	X $ =		OR	X $62=	248
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $ =		OR	X $250=	0
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	**248**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE ($)	SMALL ENTITY ADDITIONAL FEE ($)	OR	OTHER THAN SMALL ENTITY RATE ($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =		OR	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =		OR	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))									
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

Legal Instrument Examiner:
/ANDREW JAMES JR/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/559,476

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	390
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 62 =	248
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1508

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)	OR	RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

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United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/559,476	07/26/2012	2189	1620	062453-010	24	2

CONFIRMATION NO. 1046

UPDATED FILING RECEIPT

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

OC000000058127441

Date Mailed: 12/20/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 46188

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/07/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/559,476**

Projected Publication Date: Perfected

Non-Publication Request: No

Early Publication Request: No
Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/559,476	07/26/2012	2188	1620	062453-010	24	2

CONFIRMATION NO. 1046

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46188
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OC000000058127441

Date Mailed: 12/28/2012

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NETLIST, INC., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 46188

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If Required, Foreign Filing License Granted: 08/07/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/559,476**

Projected Publication Date: 04/04/2013

Non-Publication Request: No

Early Publication Request: No
Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage, facilitate, and accelerate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/559,476

APPLICATION AS FILED - PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY FEE($)
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	390
SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A	620
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	250
TOTAL CLAIMS (37 CFR 1.16(i))	24 minus 20 =	* 4			OR	x 62 =	248
INDEPENDENT CLAIMS (37 CFR 1.16(h))	2 minus 3 =	*				x 250 =	0.00
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1508

APPLICATION AS AMENDED - PART II

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	SMALL ENTITY RATE($)	SMALL ENTITY ADDITIONAL FEE($)	OR	OTHER THAN SMALL ENTITY RATE($)	OTHER THAN SMALL ENTITY ADDITIONAL FEE($)
AMENDMENT A	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT A	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT A	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT A	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

		(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE($)	ADDITIONAL FEE($)		RATE($)	ADDITIONAL FEE($)
AMENDMENT B	Total (37 CFR 1.16(i))	*	Minus	**	=	x =		OR	x =	
AMENDMENT B	Independent (37 CFR 1.16(h))	*	Minus	***	=	x =		OR	x =	
AMENDMENT B	Application Size Fee (37 CFR 1.16(s))									
AMENDMENT B	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/559,476	07/26/2012	Hyun Lee	062453-010

CONFIRMATION NO. 1046

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

PUBLICATION NOTICE

OC000000060250294

Title:FLASH-DRAM HYBRID MEMORY MODULE

Publication No.US-2013-0086309-A1
Publication Date:04/04/2013

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently http://www.uspto.gov/patft/.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently http://pair.uspto.gov/. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Managment, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee.	CONFIRMATION NO.: 1046
APPLICATION NO.:	13/559,476	
FILING DATE:	July 26, 2012	
TITLE:	FLASH-DRAM HYBRID MEMORY MODULE	
EXAMINER:	Reginald Glenwood Bragdon	
ART UNIT:	2189	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST TO CORRECT FILING RECEIPT

Sir:

Our office received the attached filing receipt for the above-identified case. Pursuant to the Supplemental Amendments filed August 20, 2012 and December 10, 2012, please amend the Filing Receipt to reflect the correct domestic priority application numbers as follows:

This application claims the benefit of 61/512,871, 07/28/11,
and of 12/240,916, 9/29/2008
which is a continuation of 12/131,873, 6/2/08,
which claims the benefit of 60/941,586, 6/1/07

(see attached copy of the filing receipt with the changes shown on a second page).

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: April 19, 2013

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
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Samsung Electronics Co., Ltd.
Ex. 1009, p. 123

UNITED STATES PATENT AND TRADEMARK OFFICE

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United States Patent and Trademark Office
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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/559,476	07/26/2012	2188	1620	062453-010	24	2

CONFIRMATION NO. 1046

UPDATED FILING RECEIPT

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

OC000000058127441

Date Mailed: 12/28/2012

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 46188

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833

See attached comments

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

In the Specification

(August 20, 2012)

Please amend paragraph [0001] as follows:

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, and of U.S. patent application serial 13/559,476, filed July 26, 2012,which is a continuation-in-part (CIP) of US patent application serial no. 12/240,916, filed September 29, 2008 which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

This application may also be considered to be related to co-pending U.S. patent application serial no. 13/536,173, filed on June 28, 2012, and commonly owned herewith.

(December 10, 2012)

Please amend paragraph [0001] as follows:

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, and of US patent application serial no. 12/240,916, filed September 29, 2008 which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

This application may also be considered to be related to co-pending U.S. patent application serial no. 13/536,173, filed on June 28, 2012, and commonly owned herewith.

Electronic Acknowledgement Receipt

EFS ID:	15570410
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	19-APR-2013
Filing Date:	26-JUL-2012
Time Stamp:	19:29:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Corrected Filing Receipt	062453_010_req_corr_fr.pdf	216375 b8198dcc59f6e2cdd908413f392fe6fdbe78524d	no	3

Warnings:

Information:

Total Files Size (in bytes):	216375

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	TOT CLAIMS	IND CLAIMS
13/559,476	07/26/2012	2189	1620	062453-010	24	2

CONFIRMATION NO. 1046

CORRECTED FILING RECEIPT

46188
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

OC000000060633652

Date Mailed: 04/29/2013

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Inventor(s)

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

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Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Assignment For Published Patent Application

NETLIST, INC., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 46188

Domestic Priority data as claimed by applicant

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see http://www.uspto.gov for more information.) - None.
Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

If Required, Foreign Filing License Granted: 08/07/2012

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 13/559,476**

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

711

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications:

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at http://www.uspto.gov/web/offices/pac/doc/general/index.html.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, http://www.stopfakes.gov. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER

Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

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The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

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SelectUSA

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The U.S. offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to promote and facilitate business investment. SelectUSA provides information assistance to the international investor community; serves as an ombudsman for existing and potential investors; advocates on behalf of U.S. cities, states, and regions competing for global investment; and counsels U.S. economic development organizations on investment attraction best practices. To learn more about why the United States is the best country in the world to develop technology, manufacture products, deliver services, and grow your business, visit http://www.SelectUSA.gov or call +1-202-482-6800.

PTO/SB/08a (01-10)
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U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120204079	A1	2012-08-09	Takefman et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1					.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

	1		☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]See Kind Codes of USPTO Patent Documents at www.USPTO.GOVor MPEP 901.04. [2]Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5]Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2013-05-21
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Electronic Acknowledgement Receipt

EFS ID:	15836017
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Yang (Aaron) Zhang
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	21-MAY-2013
Filing Date:	26-JUL-2012
Time Stamp:	18:13:18
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	062453_010_IDS__ss.pdf	92624 31353328bf4773c808095aa170dfd6004929350c	no	3

Warnings:

Information:

This is not an USPTO supplied IDS fillable form	
Total Files Size (in bytes):	92624

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New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5675725		1997-10-07	Malcolm	
	2	7111142		2006-09-19	Spencer et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1					.		☐

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NON-PATENT LITERATURE DOCUMENTS

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	U.S. Office Action in U.S. Application No. 13/536,173, mailed on April 15, 2013.	☐
	2	Notice of Allowance in U.S. Application No. 12/240,916 dated September 17, 2012.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]See Kind Codes of USPTO Patent Documents at www.USPTO.GOVor MPEP 901.04. [2]Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5]Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2013-07-12
Name/Print	Khaled Shami	Registration Number	38745

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Electronic Acknowledgement Receipt

EFS ID:	16307297
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Yang (Aaron) Zhang
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	12-JUL-2013
Filing Date:	26-JUL-2012
Time Stamp:	18:20:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	062453_010_IDS__JUL_12_2013__ss.pdf	93341 400c5940d490964376e3aa3f0c62fb832c2c62d3	no	3

Warnings:

Information:

This is not an USPTO supplied IDS fillable form					
2	Non Patent Literature	OA__003__APR_15_2013.pdf	361822 95898d369cdbcda76d8d225741008677ab4d4f82	no	10
Warnings:					
Information:					
3	Non Patent Literature	NoA__002__SEP_17_2012.pdf	387574 f51e469063c3f9737f844e1fc95d514c7846b2da	no	7
Warnings:					
Information:					
			Total Files Size (in bytes):	842737	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee et al.	
SERIAL NO.:	13/559,476	CONFIRMATION NO: 1046
FILING DATE:	July 26, 2012	
TITLE:	Flash-DRAM Hybrid Memory Module	
EXAMINER:	Elmore, Stephen C.	
ART UNIT:	2188	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the above-identified application as follows:

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page **2**.

Remarks begin on page **7** of this paper.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 141

In the Claims

The following Listing of Claims replaces all prior versions in the application:

LISTING OF CLAIMS

1. (Currently Amended) A memory module couplable to a memory controller of a host system, comprising:

a non-volatile memory subsystem;

a data manager coupled to the non-volatile memory subsystem;

a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and

a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein:

at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and

the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

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Ex. 1009, p. 142

2. (Previously Presented) The memory module of claim 1, wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

3. (Previously Presented) The memory module of claim 1, wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

4. (Previously Presented) The memory module of claim 3, wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

5. (Previously Presented) The memory module of claim 1, wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

6-8. (Cancelled)

9. (Previously Presented) The memory module of claim 1, wherein the volatile memory subsystem comprises DRAM memory.

10-12. (Cancelled)

13. (Currently Amended) A method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems, the method comprising:

receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem;

identifying a data path to be used for transferring data to or from the memory module using the received control information; ~~and~~

using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path;

operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports, wherein a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystems, and a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem;

operating the two or more sets of data ports to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems based on control information received from the controller of the memory module; and

using the controller of the memory module to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem.

14. (Previously Presented) The method of claim 13, further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

15. (Cancelled)

16. (Previously Presented) The memory module of claim 13, wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

17. (Cancelled)

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Ex. 1009, p. 144

18. (Previously Presented) The method of claim 13, further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

19. (Previously Presented) The method of claim 18, further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

20. (Cancelled)

21. (Previously Presented) The method of claim 13, further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

22. (Previously Presented) The method of claim 21, wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

23. (Previously Presented) The method of claim 21, wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

24. (Currently Amended) The method of claim 13, further comprising:

operating the volatile memory subsystem at a first clock frequency when the memory ~~system~~ module is in a first mode of operation in which data is communicated between the volatile memory subsystem and the ~~host system~~memory controller;

operating the non-volatile memory subsystem at a second clock frequency when the memory ~~system~~ module is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

operating the volatile memory subsystem at a third clock frequency when the memory ~~system~~ module is in the second mode of operation, the third clock frequency being less than the first clock frequency.

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Ex. 1009, p. 146

REMARKS

Applicants have amended Claims 1, 13 and 24 and have cancelled Claims 6-8, 10-12, 15, 17 and 20. Applicants reserve the right to further pursue the cancelled claims in a continuation and/or divisional application as well as for appeal purposes. Early consideration and allowance of this application are earnestly solicited.

The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to deposit account No. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: March 28, 2014

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
FAX (650) 320-7701

Samsung Electronics Co., Ltd.
Ex. 1009, p. 147

Electronic Acknowledgement Receipt

EFS ID:	18619309
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Monica Pizarro
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	28-MAR-2014
Filing Date:	26-JUL-2012
Time Stamp:	20:13:57
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		062453-010_Preliminary_Amendment.pdf	99801 931544b89091d35af0ad5f98a298b9cffe157300	yes	7

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Preliminary Amendment	1	1
	Claims	2	6
	Applicant Arguments/Remarks Made in an Amendment	7	7
Warnings:			
Information:			
	Total Files Size (in bytes):	99801	

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PTO/SB/06 (09-11)
Approved for use through 1/31/2014. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875	Application or Docket Number 13/559,476	Filing Date 07/26/2012	☐ To be Mailed

ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO

APPLICATION AS FILED – PART I

FOR	(Column 1) NUMBER FILED	(Column 2) NUMBER EXTRA	RATE ($)	FEE ($)
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A	
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A	
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A	
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X $ =	
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X $ =	
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is $310 ($155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).			
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))				
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL	

APPLICATION AS AMENDED – PART II

AMENDMENT

03/28/2014	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	* 15	Minus	** 24	= 0	X $80 =	0
Independent (37 CFR 1.16(h))	* 2	Minus	***3	= 0	X $420 =	0
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	**0**

AMENDMENT

	(Column 1) CLAIMS REMAINING AFTER AMENDMENT		(Column 2) HIGHEST NUMBER PREVIOUSLY PAID FOR	(Column 3) PRESENT EXTRA	RATE ($)	ADDITIONAL FEE ($)
Total (37 CFR 1.16(i))	*	Minus	**	=	X $ =	
Independent (37 CFR 1.16(h))	*	Minus	***	=	X $ =	
☐ Application Size Fee (37 CFR 1.16(s))						
☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))						
					TOTAL ADD'L FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

LIE
/DOROTHY BELL/

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If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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NOTICE OF ALLOWANCE AND FEE(S) DUE

46188 7590 05/06/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/06/2014

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/06/2014

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
Ex. 1009, p. 151

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46188 7590 05/06/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	$960	$0	$0	$960	08/06/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELMORE, STEPHEN C	2188	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ❑ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ❑ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1_____
2_____
3_____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE (B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ❑ Individual ❑ Corporation or other private group entity ❑ Government

4a. The following fee(s) are submitted:
- ❑ Issue Fee
- ❑ Publication Fee (No small entity discount permitted)
- ❑ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ❑ A check is enclosed.
- ❑ Payment by credit card. Form PTO-2038 is attached.
- ❑ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ❑ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ❑ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ❑ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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Ex. 1009, p. 152

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

46188 7590 05/06/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 05/06/2014

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

PTOL-85 (Rev. 02/11)

Samsung Electronics Co., Ltd.
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OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/559,476	Applicant(s) LEE ET AL.	
	Examiner STEPHEN ELMORE	Art Unit 2188	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Application filed 7/26/2012*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5,9,13,14,16,18,19 and 21-24*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date See Continuation Sheet
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☒ Examiner's Statement of Reasons for Allowance
7. ☐ Other _____.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

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Ex. 1009, p. 155

Continuation of Attachment(s) 2. Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date: 9/27/12, 12/10/12, 5/21/13, 7/12/13.

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Ex. 1009, p. 156

EXAMINER'S COMMENT and REASONS FOR ALLOWANCE

The present application is being examined under the pre-AIA first to invent provisions.

Priority

Applicant's claim for the benefit of one or more prior-filed applications under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged. However, Applicant has not complied with one or more conditions for receiving the benefit of an earlier filing date under 35 U.S.C. 119(e) or 120 as follows: the inventive entity of each of the prior-filed applications is/are not the same inventive entity of the present application. Prior filed provisional application 61/512871 has single inventor, Hyun Lee (a distinct inventive entity), and prior filed CIP application 12/240916 has four inventors: Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (a different distinct inventive entity), while the present application has five inventors: Hyun Lee, Chi-She Chen, Jeffrey Solomon, Scott Milton, and Jayesh Bhakta (another different distinct inventive entity). The priority date granted to the examination of the present application is 7/26/2012.

Drawings

The drawings Figures 2, 8B, and 9 filed on 7/26/2012 are objected-to subject to correction of the informalities indicated below. In order to avoid abandonment of this application, correction is required in reply to the Office action. The correction will not be held in abeyance.

Figure 2 is objected to because graphic shading elements in the figure obscure text in the drawing.

Figure 8B is objected-to because the multiple drawing elements composed of graphical shading are unidentified.

Figure 9 is objected-to because flowchart element 916 contains an incomplete descriptive labeling/statement.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

In independent claims 1 and 13 the following features taken **in combination with** the remaining limitations of the independent claim are not found in and/or are not obvious in view of the closest prior art of record, Song et al., US 8,102,614,

Claim 1,

"a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein: at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data

manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem" and *"a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller";*

Claim 13,

"*identifying a data path to be used for transferring data to or from the memory module using the received control information; and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path; operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports, wherein a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystems, and a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem; operating the two or more sets of data ports to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems based on control information received from the controller of the memory module"* and *"using the controller of the memory module to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem".*

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN ELMORE whose telephone number is (571)272-4436. The examiner can normally be reached on Mon-Fri from 9:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

April 20, 2014

Notice of References Cited	Application/Control No. 13/559,476	Applicant(s)/Patent Under Reexamination LEE ET AL.	
	Examiner STEPHEN ELMORE	Art Unit 2188	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,577,213 A	11-1996	Avery et al.	710/100
*	B	US-5,619,644 A	04-1997	Crockett et al.	714/45
*	C	US-6,269,382 B1	07-2001	Cabrera et al.	1/1
*	D	US-6,691,209 B1	02-2004	O'Connell, Mark Andrew	711/114
*	E	US-2007/0136523 A1	06-2007	Bonella et al.	711/113
*	F	US-8,086,955 B2	12-2011	Zhou et al.	715/234
*	G	US-2011/0320804 A1	12-2011	Chan et al.	713/150
*	H	US-8,102,614 B2	01-2012	Song et al.	360/31
*	I	US-8,412,879 B2	04-2013	Chang et al.	711/103
*	J	US-2014/0059170 A1	02-2014	Gasparakis et al.	709/217
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

Receipt date: 12/10/2012

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

13559476 - GAU: 2188

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	8301833		2012-10-30	Chen et al.	
If you wish to add additional U.S. Patent citation information please click the Add button.						Add

U.S.PATENT APPLICATION PUBLICATIONS						Remove
Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20080104344		2008-05-01	Shimozono et al.	
	2	20100274953		2010-10-28	Lee et al.	
If you wish to add additional U.S. Published Application citation information please click the Add button.						Add

FOREIGN PATENT DOCUMENTS								Remove
Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐
If you wish to add additional Foreign Patent Document citation information please click the Add button								Add

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

Receipt date: 12/10/2012	Application Number	13559476 13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	International Search Report and Written Opinion in PCT/US12/48750, dated October 10, 2012 pp 1-10.	☐

If you wish to add additional non-patent literature document citation information please click the Add button Add

EXAMINER SIGNATURE

Examiner Signature	/Stephen Elmore/	Date Considered	04/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

EFS Web 2.1.17 ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

Receipt date: 12/10/2012	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name		
	Attorney Docket Number	062453-010	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2012-12-11
Name/Print	Khaled Shami	Registration Number	38,745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

CPC								
Symbol							Type	Version
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CPC Combination Sets								
Symbol							Type	Set	Ranking	Version
			/							
			/							

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	4/20/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

Part of Paper No. 20140420

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
711	103	G	0	6	F	12 / 02 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	111	112	114	154	156
365	185.33				

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	4/20/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

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Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1														
	2														
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NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	4/20/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

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Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

CPC- SEARCHED		
Symbol	**Date**	**Examiner**

CPC COMBINATION SETS - SEARCHED		
Symbol	**Date**	**Examiner**

US CLASSIFICATION SEARCHED			
Class	**Subclass**	**Date**	**Examiner**
711	103, 111, 112, 114, 154, 156	4/20/2014	SE
365	185.33	4/20/2014	SE

SEARCH NOTES		
Search Notes	**Date**	**Examiner**
EAST	4/20/2014	SE
Inventor Name Search for DP	4/20/2014	SE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	**US Subclass / CPC Group**	**Date**	**Examiner**
711	103	4/20/2014	SE
PGPUB Searched		4/20/2014	SE

Samsung Electronics Co., Ltd.
Ex. 1009, p. 169

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4420821		1983-12-13	Hoffman	
	2	4449205		1984-05-15	Hoffman	
	3	5519663		1996-05-21	Harper, Jr. et al.	
	4	6158015		2000-12-05	Klein	
	5	6336174	B1	2002-01-01	Li et al.	
	6	6336176	B1	2002-01-01	Leyda et al.	
	7	6487623	B1	2002-11-26	Emerson et al.	
	8	6658507	B1	2003-12-02	Chan	

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Receipt date: 09/27/2012	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name		
	Attorney Docket Number	062453-010	

	9	6799244	B2	2004-09-28	Tanaka et al.	
	10	7409590	B2	2008-08-05	Moshayedi et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20020083368	A1	2002-06-27	Abe et al.	
	2	20040190210	A1	2004-09-30	Leete	
	3	20070192627	A1	2007-08-16	Oshikiri	
	4	20080195806	A1	2008-08-14	Cope	

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Receipt date: 09/27/2012	Application Number	13559476 13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	
	Attorney Docket Number	062453-010

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	Office Action in U.S. Patent Application No. 12/240,916, mailed April 3, 2012. pp 1-12.	☐
	2	Office Action in U.S. Patent Application No. 12/240,916, mailed February 1, 2012. pp 1-14.	☐
	3	Office Action in U.S. Patent Application No. 12/240,916, mailed July 29, 2011. pp 1-8.	☐

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Examiner Signature	/Stephen Elmore/	Date Considered	04/20/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 09/27/2012	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name		
	Attorney Docket Number	062453-010	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2012-09-27
Name/Print	Khaled Shami	Registration Number	38,745

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BIB DATA SHEET

CONFIRMATION NO. 1046

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/559,476	07/26/2012 RULE	711	2188	062453-010

APPLICANTS

INVENTORS

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

**** FOREIGN APPLICATIONS ****************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ****

08/07/2012

		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
Foreign Priority claimed ☐ Yes ☑ No 35 USC 119(a-d) conditions met ☐ Yes ☑ No Verified and Acknowledged /STEPHEN C ELMORE/ Examiner's Signature	☐ Met after Allowance Initials	CA	10	24	2

ADDRESS

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306
UNITED STATES

TITLE

FLASH-DRAM HYBRID MEMORY MODULE

FILING FEE RECEIVED		
1620	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	8720	711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:03
L2	2611	365/185.33.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:04
L3	18749	711/111,112,114,154,156.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:04
L4	28259	1 or 2 or 3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:04
L5	4365	hybrid near3 memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:14
L6	522	data adj manager and controller and memory adj controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:15
L7	6	5 and 6	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:15
L8	3	7 and ((@pd or @ad)<"20120726")	US-	OR	ON	2014/04/20

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB			19:16
L9	2	(US-20070136523-$).did. or (US-8412879-$).did.	US-PGPUB; USPAT	OR	ON	2014/04/20 19:18
L10	154543	(format$3 near3 data) with (transfer or transferred or transferring or move or moved or moving or transmitted or transmission or write or written or writing or store or stored or storing)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:22
L11	79	6 and 10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:23
L12	1	5 and 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:23
L13	2	4 and 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:23
L14	344	(bi-direction or bi-directional) near3 fabric	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:25
L15	1	14 with (data adj manager)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:25
L16	17	(data near3 (port or input-output or I/O or IO)) and 11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:27
L17	1	5 and 16	US-PGPUB; USPAT;	OR	ON	2014/04/20 19:27

			USOCR; FPRS; EPO; JPO; IBM_TDB			
L18	14	16 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:27
L19	0	4 and 18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:29
L20	14	6 and 18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:30
L21	0	14 and 20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:30
L22	0	5 and 20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:30
L23	28107	(control adj information or control adj data or control adj meta-data or control adj metadata) near3 controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:32
L24	1	((control adj information or control adj data or control adj meta-data or control adj metadata) near3 controller) and 16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:33
L25	1	6 and 23 and 10 and 4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:33
L26	1	6 and 23 and 10	US-	OR	ON	2014/04/20

			PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB			19:33
L27	6	6 and 23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:33
L28	5305	((Hyun) near2 (Lee)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/20 19:35
L29	11	((Chi-She) near2 (Chen)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/20 19:35
L30	89	((Jeffrey) near2 (Solomon)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/20 19:35
L31	154	((Scott) near2 (Milton)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/20 19:35
L32	76	((Jayesh) near2 (Bhakta)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/04/20 19:35
L42	1	(data adj manager same controller same memory adj controller) and 5 and (10 or 14)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:39
L47	503	(hybrid near3 memory).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:43
L48	2	6 and 47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:43
L49	0	48 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2014/04/20 19:43

			IBM_TDB			
L50	2	(data adj manager and memory adj controller) and 47	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:44
L51	0	50 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:44
L52	1	(data adj manager) and 47 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:44
L53	36	("20080195806" | "6658507" | "5675725" | "20040190210" | "6336176" | "7409590" | "20100274953" | "6336174" | "5519663" | "6487623" | "20080104344" | "4420821" | "6799244" | "20020083368" | "4449205" | "8301833" | "7111142" | "20070192627" | "6158015" | "20120204079").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:46
L54	1	6 and 53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/04/20 19:46

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L33	12	((Chi-She) near2 (Chen)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:36
L34	89	((Jeffrey) near2 (Solomon)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:36
L35	110	((Scott) near2 (Milton)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:36
L36	77	((Jayesh) near2 (Bhakta)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:36
L37	5310	((Hyun) near2 (Lee)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:36
L38	5528	33 or 34 or 35 or 36 or 37	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:37
L40	6	(data adj manager with controller with memory adj controller).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:38
L41	1	38 and 40	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:38

Samsung Electronics Co., Ltd.
Ex. 1009, p. 180

L44	11629	(data adj path or memory adj segment).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:40
L45	36	38 and 44	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:41
L46	1	40 and 45	US-PGPUB; USPAT; UPAD	OR	ON	2014/04/20 19:41

4/20/2014 7:47:30 PM
C:\Users\selmore\Documents\EAST\Workspaces\13559476.wsp

Samsung Electronics Co., Ltd.
Ex. 1009, p. 181

Receipt date: 05/21/2013

13559476 - GAU: 2188

Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1					

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U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20120204079	A1	2012-08-09	Takefman et al.	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1					.		☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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Receipt date: 05/21/2013	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

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EXAMINER SIGNATURE

Examiner Signature	/Stephen Elmore/	Date Considered	04/20/2014

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Receipt date: 05/21/2013	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2013-05-21
Name/Print	Khaled Shami	Registration Number	38745

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
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	Attorney Docket Number	062453-010

U.S.PATENTS

Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5675725		1997-10-07	Malcolm	
	2	7111142		2006-09-19	Spencer et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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Receipt date: 07/12/2013	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99**)	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	U.S. Office Action in U.S. Application No. 13/536,173, mailed on April 15, 2013. pp 1-10.	☐
	2	Notice of Allowance in U.S. Application No. 12/240,916 dated September 17, 2012. pp 1-7.	☐

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Examiner Signature	/Stephen Elmore/	Date Considered	04/29/2014

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	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2013-07-12
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Doc code: IDS
Doc description: Information Disclosure Statement (IDS) Filed

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Approved for use through 07/31/2012. OMB 0651-0031
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
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NON-PATENT LITERATURE DOCUMENTS			Remove
Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

	1	Office Action in U.S. Patent Application No. 14/173,219, mailed March 13, 2014.	☐
	2	Office Action in U.S. Patent Application No. 14/173,242, mailed March 14, 2014.	☐

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	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

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☒ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-05-20
Name/Print	Khaled Shami	Registration Number	38745

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Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Tiffany Weeks
Attorney Docket Number:	062453-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	19070990
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Tiffany Weeks
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	20-MAY-2014
Filing Date:	26-JUL-2012
Time Stamp:	13:09:32
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	10597
Deposit Account	503557
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1	Information Disclosure Statement (IDS) Form (SB08)	062453-010_IDS_dated_05-20-2014_US_Certify.pdf	584336 287a75239810988fd443f4152cdc9939cf164c12	no	4
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2	Non Patent Literature	OA_14173219_03_13_2014.pdf	234253 c0a3c9a61fe5d7ac4bbaa13398360b4025a240a2	no	7
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4	Fee Worksheet (SB06)	fee-info.pdf	30324 648fc6349613b6c0a17d2417b1b5fb0a78dc319b	no	2
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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

	1	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed April 3, 2014.	☐

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Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-05-20
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PATENT COOPERATION TREATY

ADVANCE E-MAIL

PCT

From the INTERNATIONAL BUREAU

To:

SHAMI, Khaled
P.O. Box 60610
Palo Alto, CA 94306
ETATS-UNIS D'AMERIQUE

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

Date of mailing *(day/month/year)* 03 April 2014 (03.04.2014)	
Applicant's or agent's file reference 062453-0011	**IMPORTANT NOTICE**

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2012/048750	28 July 2012 (28.07.2012)	28 July 2011 (28.07.2011)

Applicant
NETLIST, INC. et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Yukari Nakamura e-mail: pt07.pct@wipo.int

Form PCT/IB/326 (January 2004)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2012/048750	International filing date *(day/month/year)* 28 July 2012 (28.07.2012)	Priority date *(day/month/year)* 28 July 2011 (28.07.2011)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant NETLIST, INC.		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 7 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 25 March 2014 (25.03.2014)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland Facsimile No. +41 22 338 82 70	Authorized officer Yukari Nakamura e-mail: pt07.pct@wipo.int

Form PCT/IB/373 (January 2004)

PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To: Khaled Shami
P.O. Box 60610
Palo Alto, CA 94306
United States of America

PCT

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	10 OCT 2012
Applicant's or agent's file reference 062453-0011	**FOR FURTHER ACTION** See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US12/48750	28 July 2012 (28.07.2012)	28 July 2011 (28.07.2011)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 12/00 (2012.01)
USPC - 711/118, 103

Applicant Netlist, Inc.

1. This opinion contains indications relating to the following items:

- [x] Box No. I Basis of the opinion
- [ ] Box No. II Priority
- [ ] Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- [ ] Box No. IV Lack of unity of invention
- [x] Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- [ ] Box No. VI Certain documents cited
- [ ] Box No. VII Certain defects in the international application
- [ ] Box No. VIII Certain observations on the international application

2. **FURTHER ACTION**

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1 *bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Fom PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	21 September 2012 (21.09.2012)	Shane Thomas PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (July 2011)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Box No. I Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:
   - [x] the international application in the language in which it was filed.
   - [ ] a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. [ ] This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under Rule 91 (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of a sequence listing filed or furnished:
   a. (means)
   - [ ] on paper
   - [ ] in electronic form

   b. (time)
   - [ ] in the international application as filed
   - [ ] together with the international application in electronic form
   - [ ] subsequently to this Authority for the purposes of search

4. [ ] In addition, in the case that more than one version or copy of a sequence listing has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	7, 8, 10, 16, 17, 24	YES
	Claims	1-6, 9, 11-15, 18-23	NO
Inventive step (IS)	Claims	NONE	YES
	Claims	1-24	NO
Industrial applicability (IA)	Claims	1-24	YES
	Claims	NONE	NO

2. Citations and explanations:

Claims 1-6, 9, 11-15 and 18-23 lack novelty under PCT Article 33(2) as being anticipated by US 2008/0104344 A1, SHIMOZONO, N., et al (hereinafter 'Shimozono').

As per Claim 1, Shimozono discloses a memory module (storage system 101 (a memory module), Figure 19, paragraph [0053]) couplable to a memory controller of a host system (is connected to storage system input/output (memory controller) of host 200 through front end I/F 307, Figure 19, paragraphs [0017] and [0080]), comprising: a non-volatile memory subsystem (non-volatile memory 313 (non-volatile memory subsystem), NM, Figure 19, paragraph [0055]); a data manager coupled to the non-volatile memory subsystem (microprocessor 303, MP, comprising the functionality of a data manager, is connected to non-volatile memory 313, through switch 309, SW, Figure 19, paragraph [0055]); a volatile memory subsystem coupled to the data manager (cache memory 311, CM, is volatile memory (a volatile memory subsystem) connected to microprocessor 303 through switch 309, SW, Figure 19, paragraphs [0055] and [0057]) and operable to exchange data with the non-volatile memory subsystem by way of the data manager (microprocessor 303 can copy data on the volatile memory, CM311, to the non-volatile memory 313, paragraphs [0055], [0057], [0065]); and a controller operable to receive commands from the memory controller (controller 301 communicates with the storage system input/output (the memory controller) of host 200 and uses microprocessor 303 to process read and write commands, paragraphs [0017], [0055], [0056], [0061]) and to direct (i) operation of the non-volatile memory subsystem (processes read and write commands with non-volatile memory 313, paragraphs [0055], [0065], [0067]), (ii) operation of the volatile memory subsystem (processes read and write commands with volatile memory 311, paragraphs [0055], [0057], [0065], [0067]), and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller (based on a read command from the storage system input/output (memory controller) of host 200, transmits data between volatile memory 311 and non-volatile memory 313 with the storage system input/output of host 200, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 2, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller (microprocessor 303 (the data manager) processes commands received from the storage system input/output (the memory controller) of host 200 and allocates the volatile memory into a fixed length segment size (controls data buffer size), paragraphs [0017], [0057], [0061], [0114]).

As per Claim 3, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller (microprocessor 303 (the data manager) specifies the access address information from the read and write commands of the storage system input/output (the memory controller) of host 200 and controls the transmission of data (controls data traffic) between volatile memory 311, non-volatile memory 313, and the storage system input/output of host 200, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 4, Shimozono discloses the memory module of claim 3; additionally, Shimozono discloses wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer (microprocessor 303 processes host 200 commands indicating the type of command, transfer address, and transfer length (data transfer size), paragraphs [0055], [0061], [0083]).

As per Claim 5, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module (the host 200 through the storage system input/output (the memory controller) can control the memory regions of volatile sub-regions (a first memory address space of the volatile memory subsystem) and non-volatile sub-regions (a second memory address space of the non-volatile memory subsystem), in units called host volumes when the microprocessor executes commands from the controller 301 regarding the configuration of the memory regions, paragraph [0017], [0055]-[0059], [0086], [0102]).

As per Claim 6, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the data manager is configured as a bidirectional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems (microprocessor 303 (the data manager) provides read and write command processing with the storage system input/output of host 200 by utilizing one or more ports (two or more sets of data ports) to the volatile cache memory of the multiplexed storage devices (a bidirectional data transfer fabric), paragraphs [0017], [0061], [0077], claim 15).
-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Supplemental Box

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-***-Continued from Box No. V: Citations and Explanations-***-

As per Claim 9, Shimozono discloses the memory module of claim 1; additionally, Shimozono discloses wherein the volatile memory subsystem comprises DRAM memory (CM 311 is volatile memory may be DRAM, Dynamic Random Access Memory, paragraph [0057]).

As per Claim 11, Shimozono discloses the memory module of claim 6; additionally, Shimozono discloses wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller (microprocessor 303 (the data manager) processes volatile memory 311 and non-volatile memory 313 commands between the storage system input/output (the memory controller) of host 200, using Fiber Channel Protocol, Ethernet and iSCSI, Internet Small Computer System Interface, protocols (a data format module to format data), paragraphs [0017], [0057], [0061], [0077], [0078]).

As per Claim 12, Shimozono discloses the memory module of 11; additionally, Shimozono discloses wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem (microprocessor 303 (the data manager) copies volatile memory 311 to the non-volatile cache region 391 (data buffer for buffering data) of the non-volatile memory 313, Figure 19, paragraphs [0055], [0057], [0068]).

As per Claim 13, Shimozono discloses a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems (a process of receiving commands on storage system 101 (a memory module) from storage system input/output (a memory controller) of host 200 and reading or writing data to volatile memory 311 and non-volatile memory 313, Figure 19, paragraph [0017], [0055], [0057], [0061]), the method comprising: receiving control information from the memory controller (commands are transceived between the storage system input/output (the memory controller) of host 200 and storage system 101 using a selected protocol, paragraphs [0017], [0077]-[0079]), wherein the control information is received using a protocol of the volatile memory subsystem (using the protocol, the storage system 101 provides volatile memory, CM 311 sub-regions, for processing read and write commands and data, paragraphs [0057], [0065], [0067] [0077]); identifying a data path to be used for transferring data to or from the memory module using the received control information (microprocessor 303 specifies access address information (identifying a data path) from the read and write commands sent from storage system input/output (the memory controller) of host 200, paragraph [0017], [0055], [0065], [0067]); and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path (storage system 101 (the memory module) comprises controller 301 and using microprocessor 303, recognized as comprising the functionality of a data manager, specifies access address information (the identified data path) and transmits data between volatile memory 311 and non-volatile memory 313 with the storage system input/output (the memory controller) of host 200, Figure 19, paragraphs [0017], [0055], [0057], [0065], [0067]).

As per Claim 14, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data (microprocessor 303 (the data manager) processes commands received from the storage system input/output (the memory controller) of host 200 and allocates the volatile memory into a fixed length segment size (controls data buffer size), paragraphs [0017], [0057], [0061], [0114]).

As per Claim 15, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising operating the data manager as a bidirectional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems (microprocessor 303 (the data manager) provides read and write command processing with the storage system input/output of host 200 by utilizing one or more ports (two or more sets of data ports) to the volatile cache memory of the multiplexed storage devices (a bidirectional data transfer fabric), paragraphs [0017], [0061], [0077], claim 15).

As per Claim 18, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller (microprocessor 303 (the data manager) copies data from volatile memory 311 to non-volatile memory 313 and to volatile memory from non-volatile memory 313 (directing transfer of data bi-directionally) using the access address information from the storage system input/output (the memory controller) of host 200, [0017], [0055]-[0058]).

As per Claim 19, Shimozono discloses the method of claim 18; additionally, Shimozono discloses further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem (microprocessor 303 processes the commands received from the storage system input/output (the memory controller) of host 200 in volatile memory 311 and copy the data to non-volatile memory 313 by executing the specific computer program, paragraphs [0017], [0055], [0057], [0061], [0065]).

As per Claim 20, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and nonvolatile memory subsystems (controller 301 comprises an access control unit in storage system 101 and when executed by microprocessor 303, allows memory to be used (memory access control), Figure 19, paragraphs [0014] and [0055]).

As per Claim 21, Shimozono discloses the method of claim 13; additionally, Shimozono discloses further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value (the host 200 through the storage system input/output (the memory controller) can control the memory regions of volatile sub-regions and non-volatile sub-regions (configure memory space) in units called host volumes through the microprocessor executing commands from the controller 301 regarding the configuration of the memory regions, paragraph [0017], [0055]-[0059], [0086], [0102]).
-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Supplemental Box

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Continuation of:

-***-Continued from Previous Supplemental Box-***-

As per Claim 22, Shimozono discloses the method of claim 21; additionally, Shimozono discloses wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller (controller 301 executes a program with microprocessor 303 to control volatile memory 311 or non-volatile memory 313 sub-region address information (configures the memory space using a first portion of the memory subsystem) in storage system 101 (the memory module) by converting the access address information designated in an access address command (the controller presents a unified memory space) from the storage system input/output (the memory controller) of host 200, Figure 19, paragraphs [0017], [0055], [0057], [0058]).

As per Claim 23, Shimozono discloses the method of claim 21; additionally, Shimozono discloses wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific (microprocessor executes the controller 301 cache control program 454 to control the forming of volatile memory 311 sub-region in storage system 101 (configures the memory space in the memory module), based on the command processing program 451 and the RAID control program 453 (instructions that are application-specific), Figures 3 and 19, paragraphs [0057], [0102]-[0106]).

Claims 7, 8, 10, 16, 17 and 24 lack an inventive step under PCT Article 33(3) as being obvious over Shimozono in view of US 2010/0274953 A1, LEE, T., et al (hereinafter 'Lee').

As per Claim 7, Shimozono discloses the memory module of claim 6. Shimozono does not disclose wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments. Lee discloses wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments (the memory system of solid state disk 120 comprises a non-volatile, flash memory interface 240 connected to a plurality of non-volatile flash memory devices groups 123 through 125 (non-volatile memory subsystem), each containing memory devices (one or more memory segments), Figures 1 and 2, paragraphs [0007] and [0046]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

As per Claim 8, Shimozono, in combination with Lee, discloses the memory module of claim 7; additionally, Lee discloses wherein each memory segment comprises at least one memory circuit, memory device, or memory die (each of the memory device groups 123 through 125 contains memory devices MEM_11 through MEM_1m, which may be NAND flash memory devices, Figure 3, paragraphs [0058] and [0071]).

As per Claim 10, Shimozono, in combination with Lee, discloses the memory module of claim 7; additionally, Lee discloses wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems (solid state disk controller 121 (the data manager) can activate some or all (independently and/or concurrently) of the channels (one set of data ports) to the non-volatile memory devices (non-volatile memory subsystem) for read and write transfer control, paragraphs [0053] and [0062]).

As per Claim 16, Shimozono discloses the memory module of claim 13. Shimozono does not disclose wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments. Lee discloses wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments (the memory system of solid state disk 120 comprises a non-volatile, flash memory interface 240 connected to a plurality of non-volatile flash memory devices groups 123 through 125 (non-volatile memory subsystem), each containing memory devices (one or more memory segments), Figures 1 and 2, paragraphs [0007] and [0046]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

As per Claim 17, Shimozono discloses the method of claim 15. Shimozono does not disclose further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or nonvolatile memory subsystems. Lee discloses further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or nonvolatile memory subsystems (solid state disk controller 121 (the data manager) can activate some or all (independently and/or concurrently) of the channels (one set of data ports) to the non-volatile memory devices (non-volatile memory subsystem) for read and write transfer control, paragraphs [0053] and [0062]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of more granular control of memory storage functions. The suggestion/motivation for doing so would have been to provide a process to selectively activate memory channels and adjust the degree of interleaving of the activated channels to provide a more efficient and reliable memory access.

-***-Continued Within the Next Supplemental Box-***-

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US12/48750

Supplemental Box

In case **the space in any of the preceding boxes is not sufficient.**
Continuation of:
-***-Continued from Previous Supplemental Box-***-

As per Claim 24, Shimozono discloses the method of claim 13. Shimozono does not disclose further comprising: operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system; operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency. Lee discloses further comprising: operating the volatile memory subsystem at a first clock frequency, when the memory system is in a first mode of operation in which data is communicated between the volatile memory subsystem and the host system (SDRAM, volatile buffer memory 522 (the volatile memory subsystem) clock frequencies, fb, (a first clock frequency) are controlled by different internal clock signals in the solid state disk 520 (the memory system) when temporarily storing data involving read and write operations with host 510 (the host system), Figures 4B and 10, paragraphs [0065], [0080], [0115]); operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem (the flash clock frequency, fi, (a second clock frequency) controls the rate of the non-volatile flash interface 240 for exchanging data between the SDRAM volatile buffer memory 122 (the volatile memory subsystem) and the non-volatile flash memory device groups (non-volatile memory subsystem), Figure 4B, paragraphs [0005], [0066], [0080]); and operating the volatile memory subsystem at a third clock frequency when the memory system is in the second mode of operation, the third clock frequency being less than the first clock frequency (solid state disk (the memory system) controller 121 can adjust the clock frequency driving SDRAM volatile memory 122 (the volatile memory subsystem) by lowering its clock frequency (the third clock frequency being less than the first clock frequency) to reduce its power consumption, when activating some or all of the non-volatile flash memory device groups (the second mode of operation), paragraphs [0005], [0053], [0065]). At the time of the invention, it would have been obvious to one of ordinary skill in the art, having the teachings of Shimozono and Lee before him or her, to modify the volatile cache and non-volatile storage system and method of Shimozono to include the data storage performance system and method of Lee because of selective component clock frequencies. The suggestion/motivation for doing so would have been to provide a method to lower clock frequencies of selective components to enable better power consumption and redirect the limited available power to other storage components to ensure proper data storage and retention.

Claims 1-24 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.

Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Tiffany Weeks
Attorney Docket Number:	062453-010

Filed as Large Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
		Total in USD ($)		**180**

Electronic Acknowledgement Receipt

EFS ID:	19071082
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Tiffany Weeks
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	20-MAY-2014
Filing Date:	26-JUL-2012
Time Stamp:	13:26:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$180
RAM confirmation Number	10803
Deposit Account	503557
Authorized User	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)

1	Information Disclosure Statement (IDS) Form (SB08)	062453-010_IDS_dated_05-20-2014_Foreign_Certify.pdf	590758 9c766ce4d9580852d24f74af71bfd361a1845618	no	4
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	IPRP_PCTUS1248750_mailed_04_03_2014.pdf	494897 b8a072d0cdcedbc842ace7cc23fed63e2dc5e795	no	8
Warnings:					
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3	Fee Worksheet (SB06)	fee-info.pdf	30325 45e625d91703c76c66e8af7b92a2deb40ee1fae6	no	2
Warnings:					
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			Total Files Size (in bytes):	1115980	

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

46188 7590 05/23/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
05/23/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/559,476	LEE ET AL.	
	Examiner	Art Unit	
	STEPHEN ELMORE	2188	

All participants (applicant, applicant's representative, PTO personnel):

(1) *STEPHEN ELMORE*. (3)_____.

(2) *Mr Khaled Shami, Reg. No. 38,745*. (4)_____.

Date of Interview: *16 May 2014*.

Type: ☒ Telephonic ☐ Video Conference
☐ Personal [copy given to: ☐ applicant ☐ applicant's representative]

Exhibit shown or demonstration conducted: ☐ Yes ☒ No.
If Yes, brief description: _____.

Issues Discussed ☐101 ☐112 ☐102 ☐103 ☒Others
(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *None*.

Identification of prior art discussed: *None*.

Substance of Interview
(For each issue discussed, provide a detailed description and indicate if agreement was reached. Some topics may include: identification or clarification of a reference or a portion thereof, claim interpretation, proposed amendments, arguments of any applied references etc...)

This interview summary pertains to Applicant's claim for priority based on prior provisional application 61/512,871, filed 7/28/2011, and on prior application 12/240,916, filed 9/29/2008. The Examiner and Applicant's representative reached agreement that the present application is entitled to the benefit of the priority dates claimed above.

Applicant recordation instructions: The formal written reply to the last Office action must include the substance of the interview. (See MPEP section 713.04). If a reply to the last Office action has already been filed, applicant is given a non-extendable period of the longer of one month or thirty days from this interview date, or the mailing date of this interview summary form, whichever is later, to file a statement of the substance of the interview

Examiner recordation instructions: Examiners must summarize the substance of any interview of record. A complete and proper recordation of the substance of an interview should include the items listed in MPEP 713.04 for complete and proper recordation including the identification of the general thrust of each argument or issue discussed, a general indication of any other pertinent matters discussed regarding patentability and the general results or outcome of the interview, to include an indication as to whether or not agreement was reached on the issues raised.

☐ Attachment

/STEPHEN ELMORE/ Primary Examiner, Art Unit 2188	

Samsung Electronics Co., Ltd.
Ex. 1009, p. 213

Summary of Record of Interview Requirements

Manual of Patent Examining Procedure (MPEP), Section 713.04, Substance of Interview Must be Made of Record
A complete written statement as to the substance of any face-to-face, video conference, or telephone interview with regard to an application must be made of record in the application whether or not an agreement with the examiner was reached at the interview.

Title 37 Code of Federal Regulations (CFR) § 1.133 Interviews
Paragraph (b)

In every instance where reconsideration is requested in view of an interview with an examiner, a complete written statement of the reasons presented at the interview as warranting favorable action must be filed by the applicant. An interview does not remove the necessity for reply to Office action as specified in §§ 1.111, 1.135. (35 U.S.C. 132)

37 CFR §1.2 Business to be transacted in writing.
All business with the Patent or Trademark Office should be transacted in writing. The personal attendance of applicants or their attorneys or agents at the Patent and Trademark Office is unnecessary. The action of the Patent and Trademark Office will be based exclusively on the written record in the Office. No attention will be paid to any alleged oral promise, stipulation, or understanding in relation to which there is disagreement or doubt.

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Examiners must complete an Interview Summary Form for each interview held where a matter of substance has been discussed during the interview by checking the appropriate boxes and filling in the blanks. Discussions regarding only procedural matters, directed solely to restriction requirements for which interview recordation is otherwise provided for in Section 812.01 of the Manual of Patent Examining Procedure, or pointing out typographical errors or unreadable script in Office actions or the like, are excluded from the interview recordation procedures below. Where the substance of an interview is completely recorded in an Examiners Amendment, no separate Interview Summary Record is required.

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The Form provides for recordation of the following information:
- Application Number (Series Code and Serial Number)
- Name of applicant
- Name of examiner
- Date of interview
- Type of interview (telephonic, video-conference, or personal)
- Name of participant(s) (applicant, attorney or agent, examiner, other PTO personnel, etc.)
- An indication whether or not an exhibit was shown or a demonstration conducted
- An identification of the specific prior art discussed
- An indication whether an agreement was reached and if so, a description of the general nature of the agreement (may be by attachment of a copy of amendments or claims agreed as being allowable). Note: Agreement as to allowability is tentative and does not restrict further action by the examiner to the contrary.
- The signature of the examiner who conducted the interview (if Form is not an attachment to a signed Office action)

It is desirable that the examiner orally remind the applicant of his or her obligation to record the substance of the interview of each case. It should be noted, however, that the Interview Summary Form will not normally be considered a complete and proper recordation of the interview unless it includes, or is supplemented by the applicant or the examiner to include, all of the applicable items required below concerning the substance of the interview.

A complete and proper recordation of the substance of any interview should include at least the following applicable items:
1) A brief description of the nature of any exhibit shown or any demonstration conducted,
2) an identification of the claims discussed,
3) an identification of the specific prior art discussed,
4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
5) a brief identification of the general thrust of the principal arguments presented to the examiner,
   (The identification of arguments need not be lengthy or elaborate. A verbatim or highly detailed description of the arguments is not required. The identification of the arguments is sufficient if the general nature or thrust of the principal arguments made to the examiner can be understood in the context of the application file. Of course, the applicant may desire to emphasize and fully describe those arguments which he or she feels were or might be persuasive to the examiner.)
6) a general indication of any other pertinent matters discussed, and
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Examiner to Check for Accuracy

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UNITED STATES DEPARTMENT OF COMMERCE
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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
13/559,476	26 July, 2012	LEE ET AL.	062453-010

		EXAMINER	
Nixon Peabody LLP P.O. Box 60610 Palo Alto, CA 94306		STEPHEN ELMORE	
		ART UNIT	PAPER
		2188	20140516

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The Applicant-Initiated Interview held on 5/16/2014 (see attached PTOL-413) confirms the determination that the present application is entitled to Applicant's claim for priority based on prior provisional application 61/512,871, filed 7/28/2011, and on prior application 12/240,916, filed 9/29/2008.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

PTO-90C (Rev.04-03)

Applicant-Initiated Interview Summary	Application No.	Applicant(s)	
	13/559,476	LEE ET AL.	
	Examiner	Art Unit	
	STEPHEN ELMORE	2188	

All participants (applicant, applicant's representative, PTO personnel):

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(2) *Mr Khaled Shami, Reg. No. 38,745*. (4)_____.

Date of Interview: *16 May 2014*.

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If Yes, brief description: _____.

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(For each of the checked box(es) above, please describe below the issue and detailed description of the discussion)

Claim(s) discussed: *None*.

Identification of prior art discussed: *None*.

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☐ Attachment

/STEPHEN ELMORE/ Primary Examiner, Art Unit 2188	

Samsung Electronics Co., Ltd.
Ex. 1009, p. 216

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4) an identification of the principal proposed amendments of a substantive nature discussed, unless these are already described on the Interview Summary Form completed by the Examiner,
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

46188 7590 06/24/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
06/24/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

PTOL-90A (Rev. 04/07)

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 13559476
Applicant : Lee
Filing Date : 07/26/2012
Date Mailed : 06/24/2014

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The application is not in compliance with 37 CFR 1.78, as indicated in the attachment. The consequences of failure to respond within the above-identified time period are set forth in the attachment.

Even if the Office has recognized a benefit claim and has entered it into the Office's database and included it on applicant's filing receipt, the benefit claim is not a proper benefit claim unless the reference in compliance with 37 CFR 1.78 is included, depending upon the application's filing date and as indicated in the attachment, in an application data sheet or in the first sentence(s) of the specification and all other requirements are met.

See attachment.

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Kam Sin/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 13559476

APPLICATION FILED PRIOR TO SEPTEMBER 16, 2012, NOT IN COMPLIANCE WITH 37 CFR 1.78

[X] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification does not indicate the relationship (continuation, division, continuation-in-part) to the prior U.S. nonprovisional application or international application designating the U.S. See document coded SPEC dated 12/10/2012, listing application number(s) 12/240916.

[ ] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification following the title does not provide the U.S. nonprovisional application number (series code and serial number) or, with respect to an international PCT application designating the U.S., it provides the international application number or international filing date but not both. See document coded dated , in which the following is missing: .

[ ] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification following the title shows an incorrect, incomplete, or illegible U.S. nonprovisional application number, international PCT application number, or international PCT filing date. See document coded dated , in which the following error was made: .

[ ] The 37 CFR 1.78(a)(2) reference to the prior U.S. nonprovisional application or international application designating the U.S. is not present on an application data sheet or in the first sentence(s) of the specification following the title, thus removing the validating link under 35 U.S.C. 119(a)-(d) to a prior foreign application or under 35 U.S.C. 119(e) to a prior U.S. provisional application.

[ ] The 37 CFR 1.78(a)(2) reference to the prior U.S. nonprovisional application or international application designating the U.S. is not present on an application data sheet or in the first sentence(s) of the specification following the title.

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application is not present on an application data sheet or in first sentence(s) of the specification following the title.

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application on an application data sheet or in first sentence(s) of the specification following the title does not provide the provisional application number (series code and serial number). See document coded dated , in which the following is missing: .

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application on an application data sheet or in first sentence(s) of the specification following the title shows an incorrect, incomplete, or illegible U.S. provisional application number. See document coded dated , in which the following error was made: .

[ ] Other: .

HOW TO RESPOND

A proper response to this notice would include any one of: (1) a supplemental Application Data Sheet (ADS) pursuant to 37 CFR 1.76(c) which provides benefit information that complies with 37 CFR 1.78(a)(2) or 37 CFR 1.78(a)(5); (2) an amendment to the first sentence(s) of the specification which provides benefit information that complies with 37 CFR 1.78(a)(2) or 37 CFR 1.78(a)(5); or (3) a petition filed pursuant to the provisions of 37 CFR 1.78(a)(3) or 37 CFR 1.78(a)(6) if the benefit information from the document identified above by code and date does not accurately reflect the benefits under 35 U.S.C. 119(e), 120, 121 or 365(c) as claimed by applicant (a grantable petition would include either a supplemental ADS or an amendment to the first sentence(s) of the specification as required by 37 CFR 1.78(a)(3)(i) or 37 CFR 1.78(a)(6)(i)). Such amendments to the specification or supplemental ADS submission may be filed after payment of the issue fee if limited to informalities noted herein. See Waiver of 37 CFR 1.312 for Document Required by Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004).

WARNING: If Applicant fails to timely submit a proper response, the benefit information will be deleted and the patent will be printed without the benefit information present.

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United States Patent and Trademark Office
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

46188 7590 07/02/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
07/02/2014	ELECTRONIC

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patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Samsung Electronics Co., Ltd.
Ex. 1009, p. 221

UNITED STATES DEPARTMENT OF COMMERCE
U.S. Patent and Trademark Office
Address : COMMISSIONER FOR PATENTS
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Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
13/559,476	26 July, 2012	LEE ET AL.	062453-010

		EXAMINER	
Nixon Peabody LLP P.O. Box 60610 Palo Alto, CA 94306		STEPHEN ELMORE	
		ART UNIT	PAPER
		2188	20140627

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

The two IDS documents filed 5/20/2014 have been entered and considered. A copy of each signed IDS is enclosed.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

PTO-90C (Rev.04-03)

PTO/SB/08a (01-10)
Approved for use through 07/31/2012. OMB 0651-0031
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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

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Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1					.		☐
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

Receipt date: 05/20/2014	Application Number	13559476 13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26
	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

	1	International Preliminary Report on Patentabillity in PCT/US12/48750, mailed April 3, 2014. pp. 1-8.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Stephen Elmore/	Date Considered	06/27/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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Receipt date: 05/20/2014	Application Number	13559476	13559476 - GAU: 2188
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	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☒ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-05-20
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these record s.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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	First Named Inventor	Hyun Lee
	Art Unit	2189
	Examiner Name	Bragdon, Reginald Glenwood
	Attorney Docket Number	062453-010

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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]

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Receipt date: 05/20/2014	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (**Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

	1	Office Action in U.S. Patent Application No. 14/173,219, mailed March 13, 2014. pp. 1-7.	☐
	2	Office Action in U.S. Patent Application No. 14/173,242, mailed March 14, 2014. pp. 1-7.	☐

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EXAMINER SIGNATURE

Examiner Signature	/Stephen Elmore/	Date Considered	06/27/2014

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[1] See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. [2] Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3] For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4] Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5] Applicant is to place a check mark here if English language translation is attached.

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	First Named Inventor	Hyun Lee	
	Art Unit	2189	
	Examiner Name	Bragdon, Reginald Glenwood	
	Attorney Docket Number	062453-010	

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OR

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☒ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-05-20
Name/Print	Khaled Shami	Registration Number	38745

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ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: Mail **Mail Stop ISSUE FEE**
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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

46188 7590 05/06/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	~~$960~~ $480	$0	$0	~~$960~~ $480	08/06/2014

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELMORE, STEPHEN C	2188	711-103000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Nixon Peabody LLP
2 Khaled Shami
3

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE: NETLIST, INC.
(B) RESIDENCE: (CITY and STATE OR COUNTRY): IRVINE, CA

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:
- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)
- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 50-3557 (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)
- ☐ Applicant certifying micro entity status. See 37 CFR 1.29 — NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
- ☒ Applicant asserting small entity status. See 37 CFR 1.27 — NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
- ☐ Applicant changing to regular undiscounted fee status. — NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Khaled Shami/ Date August 6, 2014
Typed or printed name Khaled Shami Registration No. 38,745

PTOL-85 Part B (10-13) Approved for use through 10/31/2013. OMB 0651-0033 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Samsung Electronics Co., Ltd.
Ex. 1009, p. 231

Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-010

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Utility Appl Issue Fee	2501	1	480	480
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Miscellaneous:				
		Total in USD ($)		**480**

Electronic Acknowledgement Receipt

EFS ID:	19789878
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	06-AUG-2014
Filing Date:	26-JUL-2012
Time Stamp:	14:04:03
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$480
RAM confirmation Number	253
Deposit Account	503557
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Post Allowance Communication - Incoming	062453-010_resp_to_correct_appln_papers.pdf	202616 634082c521e1918897b8c655035f807a4d9d40de	no	5
Warnings:					
Information:					
2	Drawings-only black and white line drawings	062453-010_Drawings1.pdf	192592 57b191387c053dfc8143ba94f099f34dff324b85	no	10
Warnings:					
Information:					
3	Post Allowance Communication - Incoming	062453-010_comments_on_allowance.pdf	84400 4c26bbc2a6f090adc584030db8ba9553090401f5	no	2
Warnings:					
Information:					
4	Issue Fee Payment (PTO-85B)	062453_010_IF_Pment.pdf	114304 4500842d284d9f045028b33ab2db645e47cfd640	no	1
Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	30036 1733fb7e5f200424bbebd1e7a82b731313bb049a	no	2
Warnings:					
Information:					
		Total Files Size (in bytes):	623948		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee et al.	
SERIAL NO.:	13/559,476	CONFIRMATION NO: 1046
FILING DATE:	July 26, 2012	
TITLE:	Flash-DRAM Hybrid Memory Module	
EXAMINER:	Elmore, Stephen C.	
ART UNIT:	2188	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Dear Sir:

This paper is responsive to the notice mailed June 24, 2014. Please amend the above-identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Remarks begin on page **3** of this paper.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 236

In the Specification

Please amend paragraph [0001] as follows:

[0001] This application claims the benefit of provisional patent application serial no. 61/512,871, filed July 28, 2011, and is a continuation-in-part of US patent application serial no. 12/240,916, filed September 29, 2008 which is a continuation of U.S. patent application serial no. 12/131,873, filed June 2, 2008, which claims the benefit of U.S. provisional patent application serial no. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

This application may also be considered to be related to co-pending U.S. patent application serial no. 13/536,173, filed on June 28, 2012, and commonly owned herewith.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 237

REMARKS

In response to the Notice to File Corrected Application Papers mailed June 24, 2014, Applicants amend the specification as set out in the Amendments of the Specification section herein to include an amended paragraph [0001] to amend the priority listing for the purposes of improving the readability of the application. Applicants added no new matter through the amendment.

Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: August 6, 2014

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
FAX (650) 320-7701

Samsung Electronics Co., Ltd.
Ex. 1009, p. 238

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Application No. : 13559476
Applicant : Lee
Filing Date : 07/26/2012
Date Mailed : 06/24/2014

NOTICE TO FILE CORRECTED APPLICATION PAPERS

Notice of Allowance Mailed

This application has been accorded an Allowance Date and is being prepared for issuance. The application, however, is incomplete for the reasons below.

Applicant is given two (2) months from the mail date of this Notice within which to respond. This time period for reply is extendable under 37 CFR 1.136(a) for only TWO additional MONTHS.

The application is not in compliance with 37 CFR 1.78, as indicated in the attachment. The consequences of failure to respond within the above-identified time period are set forth in the attachment.

Even if the Office has recognized a benefit claim and has entered it into the Office's database and included it on applicant's filing receipt, the benefit claim is not a proper benefit claim unless the reference in compliance with 37 CFR 1.78 is included, depending upon the application's filing date and as indicated in the attachment, in an application data sheet or in the first sentence(s) of the specification and all other requirements are met.

See attachment.

A copy of this notice MUST be returned with the reply. Please address response to "Mail Stop Issue Fee, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450".

/Kam Sin/
Publication Branch
Office of Data Management
(571) 272-4200

Application No. 13559476

APPLICATION FILED PRIOR TO SEPTEMBER 16, 2012, NOT IN COMPLIANCE WITH 37 CFR 1.78

[X] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification does not indicate the relationship (continuation, division, continuation-in-part) to the prior U.S. nonprovisional application or international application designating the U.S. See document coded SPEC dated 12/10/2012, listing application number(s) 12/240916.

[ ] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification following the title does not provide the U.S. nonprovisional application number (series code and serial number) or, with respect to an international PCT application designating the U.S., it provides the international application number or international filing date but not both. See document coded dated , in which the following is missing: .

[ ] The 37 CFR 1.78(a)(2) reference on the application data sheet or in the first sentence(s) of the specification following the title shows an incorrect, incomplete, or illegible U.S. nonprovisional application number, international PCT application number, or international PCT filing date. See document coded dated , in which the following error was made: .

[ ] The 37 CFR 1.78(a)(2) reference to the prior U.S. nonprovisional application or international application designating the U.S. is not present on an application data sheet or in the first sentence(s) of the specification following the title, thus removing the validating link under 35 U.S.C. 119(a)-(d) to a prior foreign application or under 35 U.S.C. 119(e) to a prior U.S. provisional application.

[ ] The 37 CFR 1.78(a)(2) reference to the prior U.S. nonprovisional application or international application designating the U.S. is not present on an application data sheet or in the first sentence(s) of the specification following the title.

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application is not present on an application data sheet or in first sentence(s) of the specification following the title.

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application on an application data sheet or in first sentence(s) of the specification following the title does not provide the provisional application number (series code and serial number). See document coded dated , in which the following is missing: .

[ ] The 37 CFR 1.78(a)(5) reference to the prior U.S. provisional application on an application data sheet or in first sentence(s) of the specification following the title shows an incorrect, incomplete, or illegible U.S. provisional application number. See document coded dated , in which the following error was made: .

[ ] Other: .

HOW TO RESPOND

A proper response to this notice would include any one of: (1) a supplemental Application Data Sheet (ADS) pursuant to 37 CFR 1.76(c) which provides benefit information that complies with 37 CFR 1.78(a)(2) or 37 CFR 1.78(a)(5); (2) an amendment to the first sentence(s) of the specification which provides benefit information that complies with 37 CFR 1.78(a)(2) or 37 CFR 1.78(a)(5); or (3) a petition filed pursuant to the provisions of 37 CFR 1.78(a)(3) or 37 CFR 1.78(a)(6) if the benefit information from the document identified above by code and date does not accurately reflect the benefits under 35 U.S.C. 119(e), 120, 121 or 365(c) as claimed by applicant (a grantable petition would include either a supplemental ADS or an amendment to the first sentence(s) of the specification as required by 37 CFR 1.78(a)(3)(i) or 37 CFR 1.78(a)(6)(i)). Such amendments to the specification or supplemental ADS submission may be filed after payment of the issue fee if limited to informalities noted herein. See Waiver of 37 CFR 1.312 for Document Required by Office of Patent Publication, 1280 Off. Gaz. Patent Office 918 (March 23, 2004).

WARNING: If Applicant fails to timely submit a proper response, the benefit information will be deleted and the patent will be printed without the benefit information present.

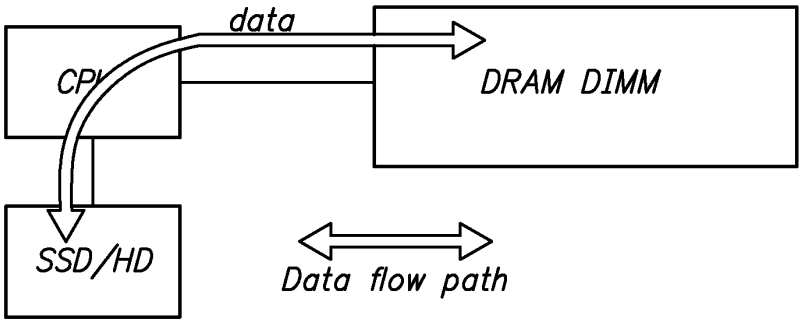


FIG. 1
(PRIOR ART)

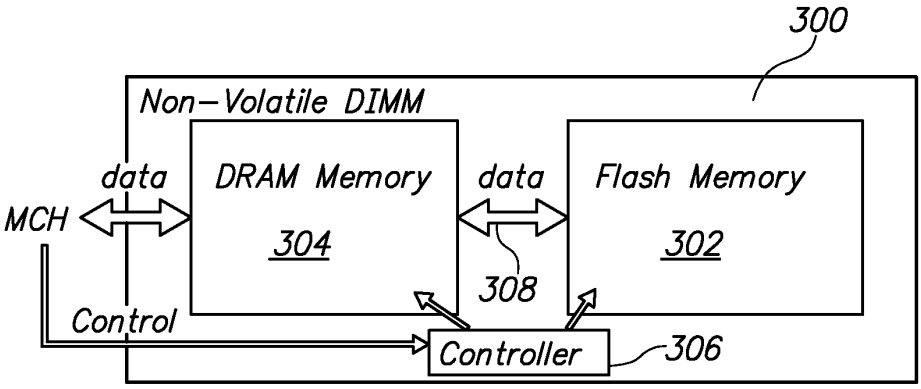
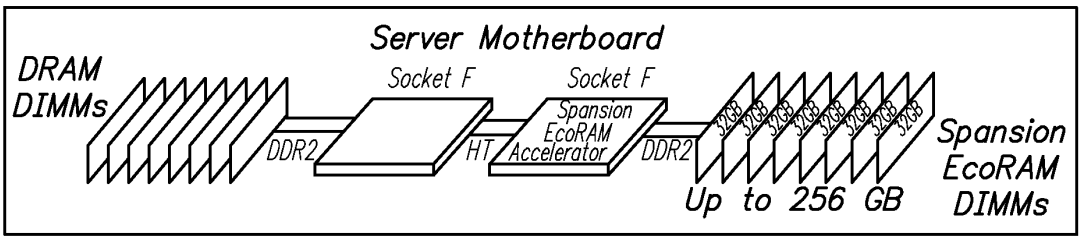


FIG. 3A

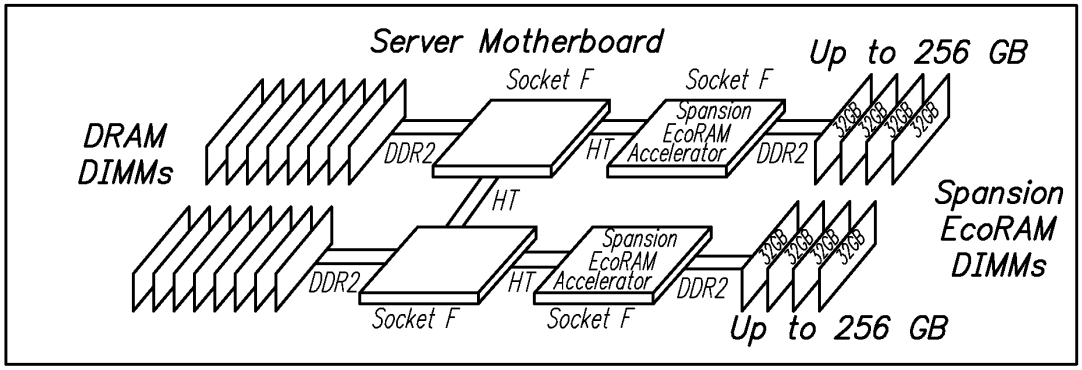
Spansion EcoRAM Configurations

256GB Spansion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

256GB Spansion EcoRAM Solution – Dual Accelerator



256GB Single Accelerator Spansion EcoRAM Solution

FIG. 2
(PRIOR ART)

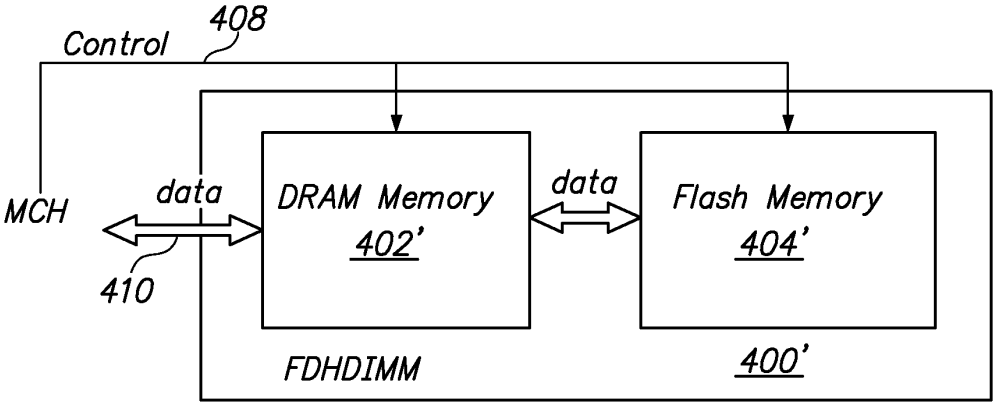


FIG. 4B

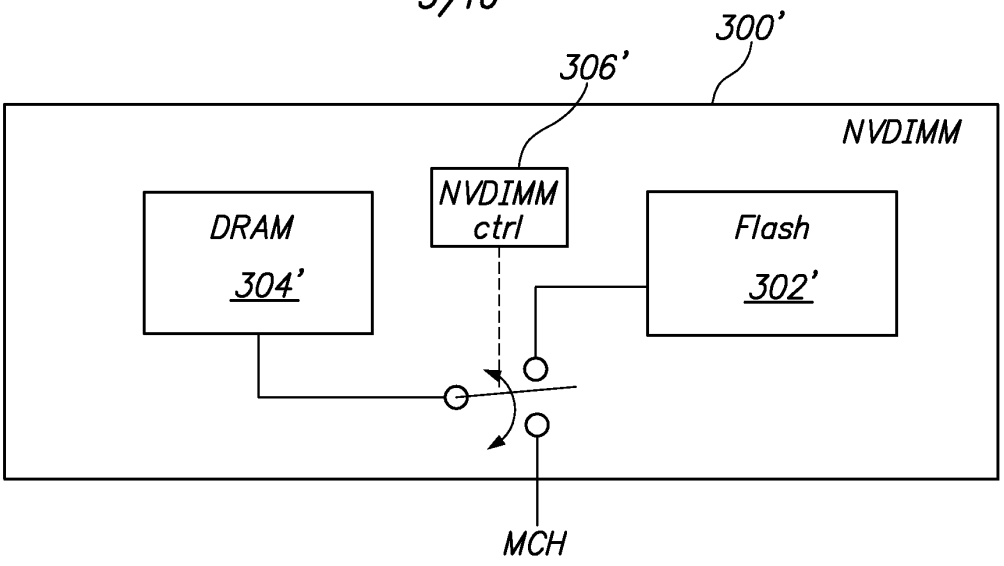

300'
306'
NVDIMM
NVDIMM ctrl
DRAM
304'
Flash
302'
MCH

FIG. 3B

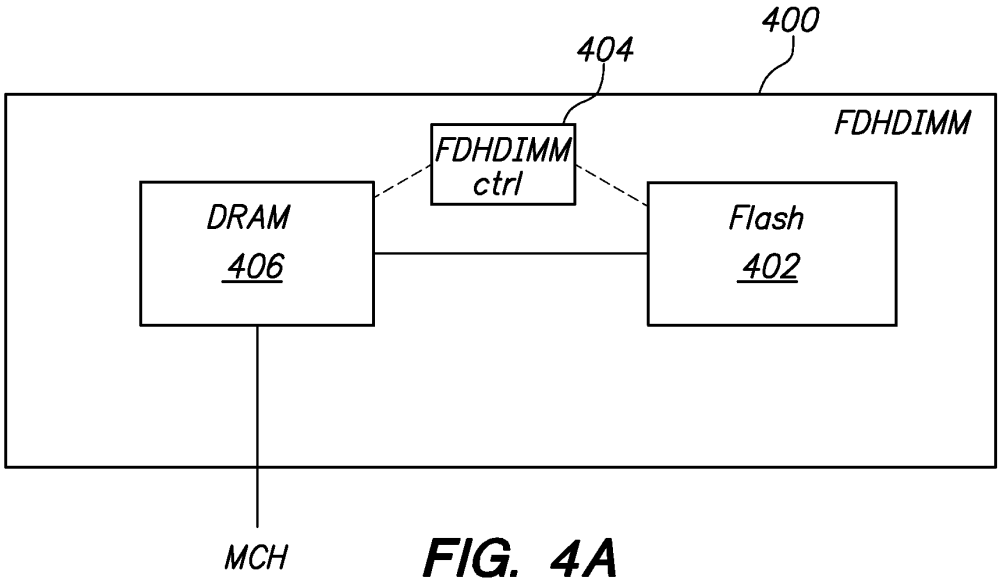

400
404
FDHDIMM
FDHDIMM ctrl
DRAM
406
Flash
402
MCH

FIG. 4A

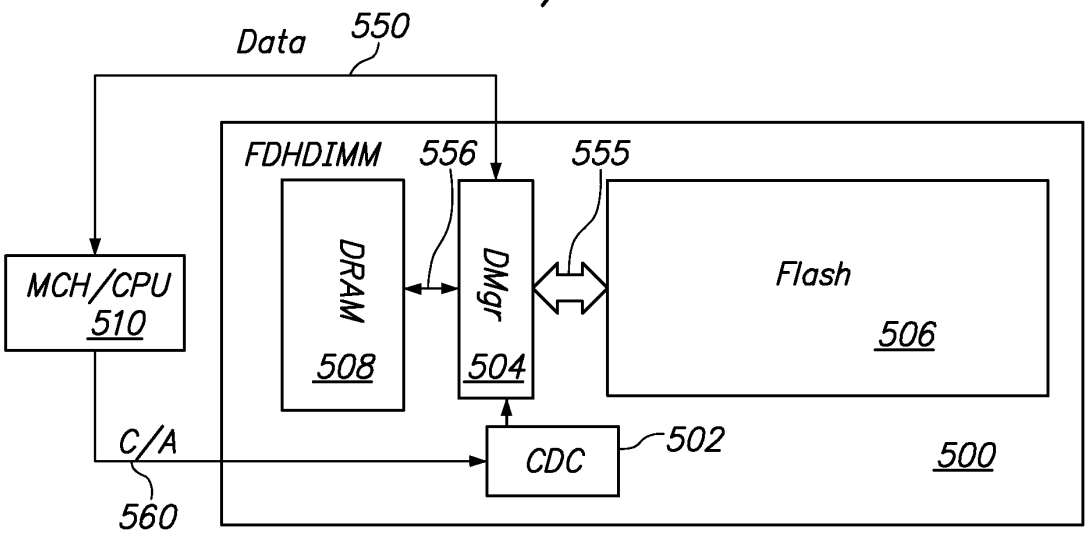

Data
550
FDHDIMM
556
555
MCH/CPU
510
DRAM
508
DMgr
504
Flash
506
C/A
560
CDC
502
500

FIG. 5A

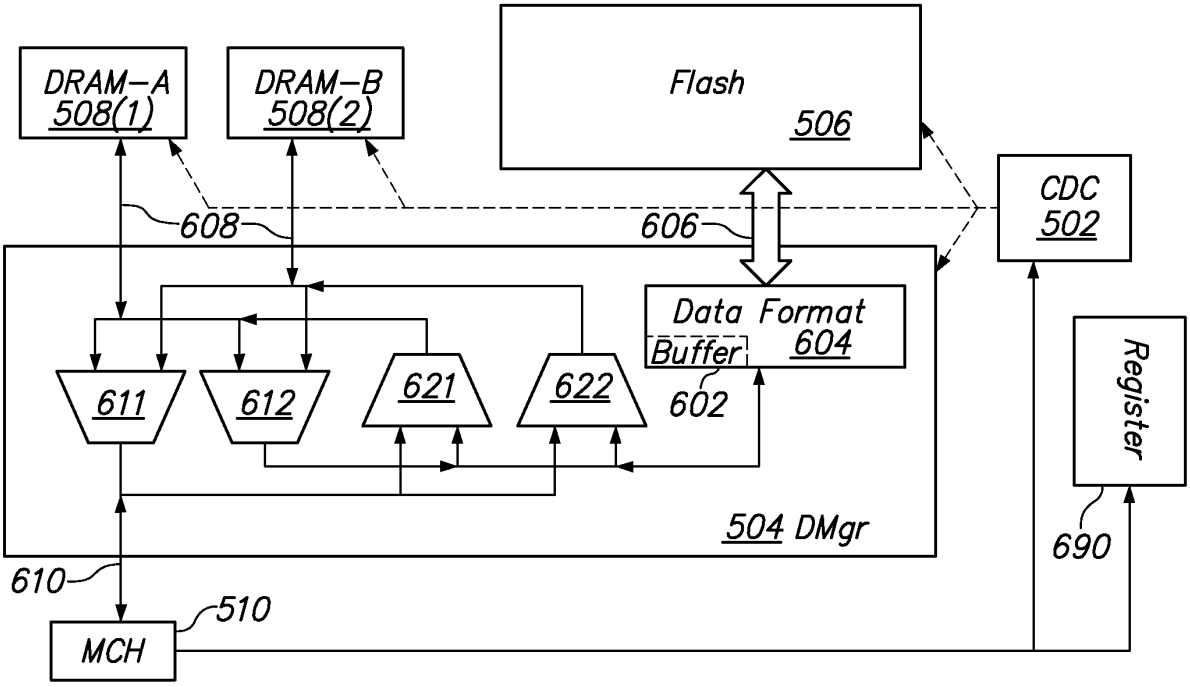

DRAM-A
508(1)
DRAM-B
508(2)
Flash
506
CDC
502
608
606
Data Format
604
Buffer
602
611
612
621
622
Register
504 DMgr
690
610
510
MCH

FIG. 6

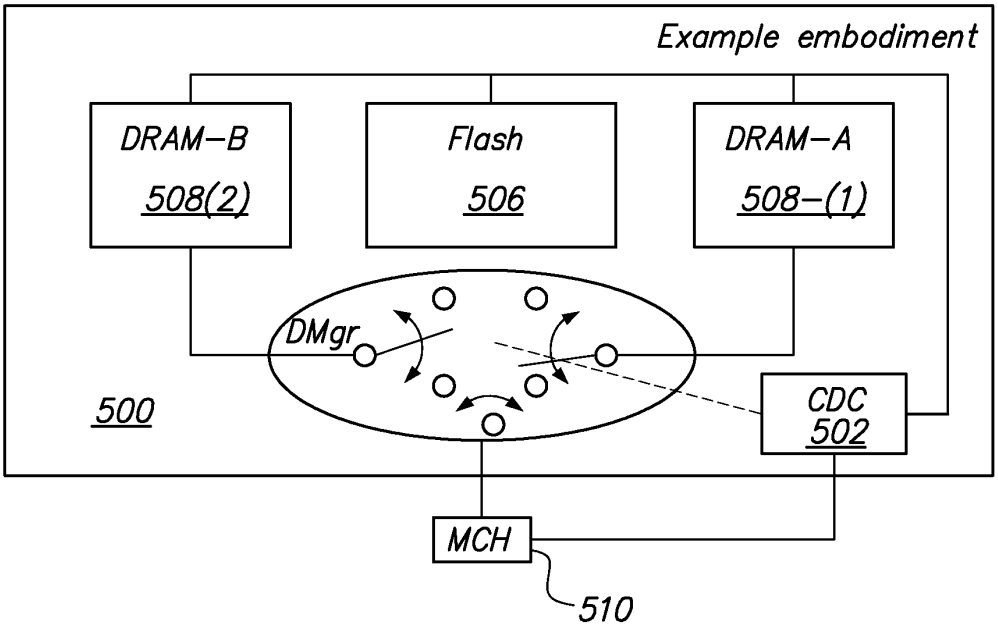

Example embodiment
DRAM–B
508(2)
Flash
506
DRAM–A
508–(1)
DMgr
500
CDC
502
MCH
510

FIG. 5B

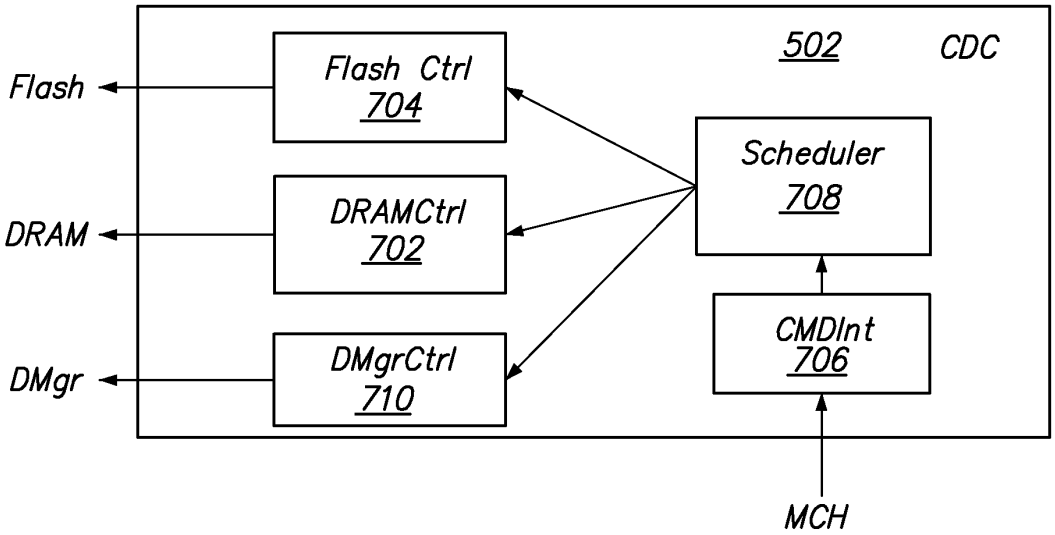

502
CDC
Flash
Flash Ctrl
704
DRAM
DRAMCtrl
702
DMgr
DMgrCtrl
710
Scheduler
708
CMDInt
706
MCH

FIG. 7

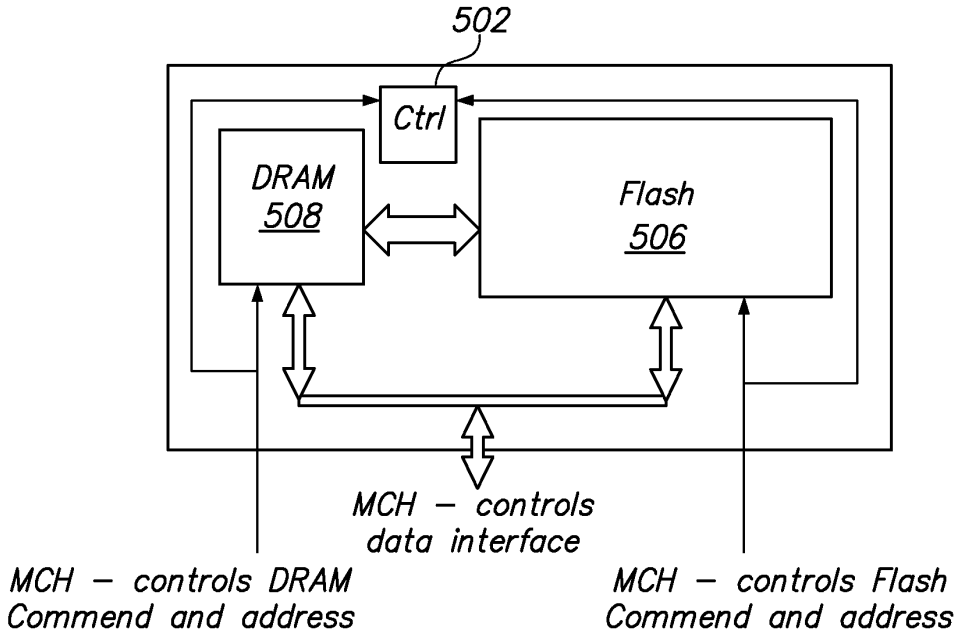

502
Ctrl
DRAM
508
Flash
506
MCH – controls
data interface
MCH – controls DRAM
Commend and address
MCH – controls Flash
Commend and address

FIG. 8A

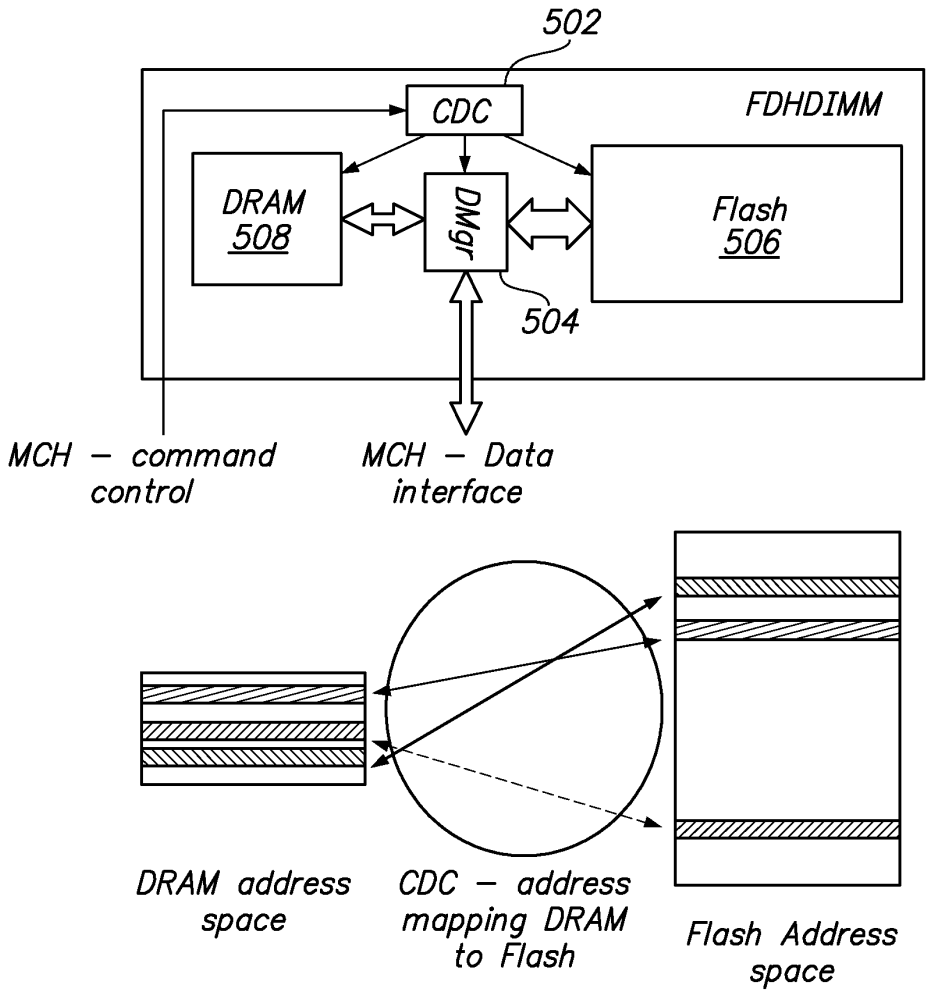

502
CDC
FDHDIMM
DRAM
508
DMgr
Flash
506
504
MCH – command control
MCH – Data interface
DRAM address space
CDC – address mapping DRAM to Flash
Flash Address space

FIG. 8B

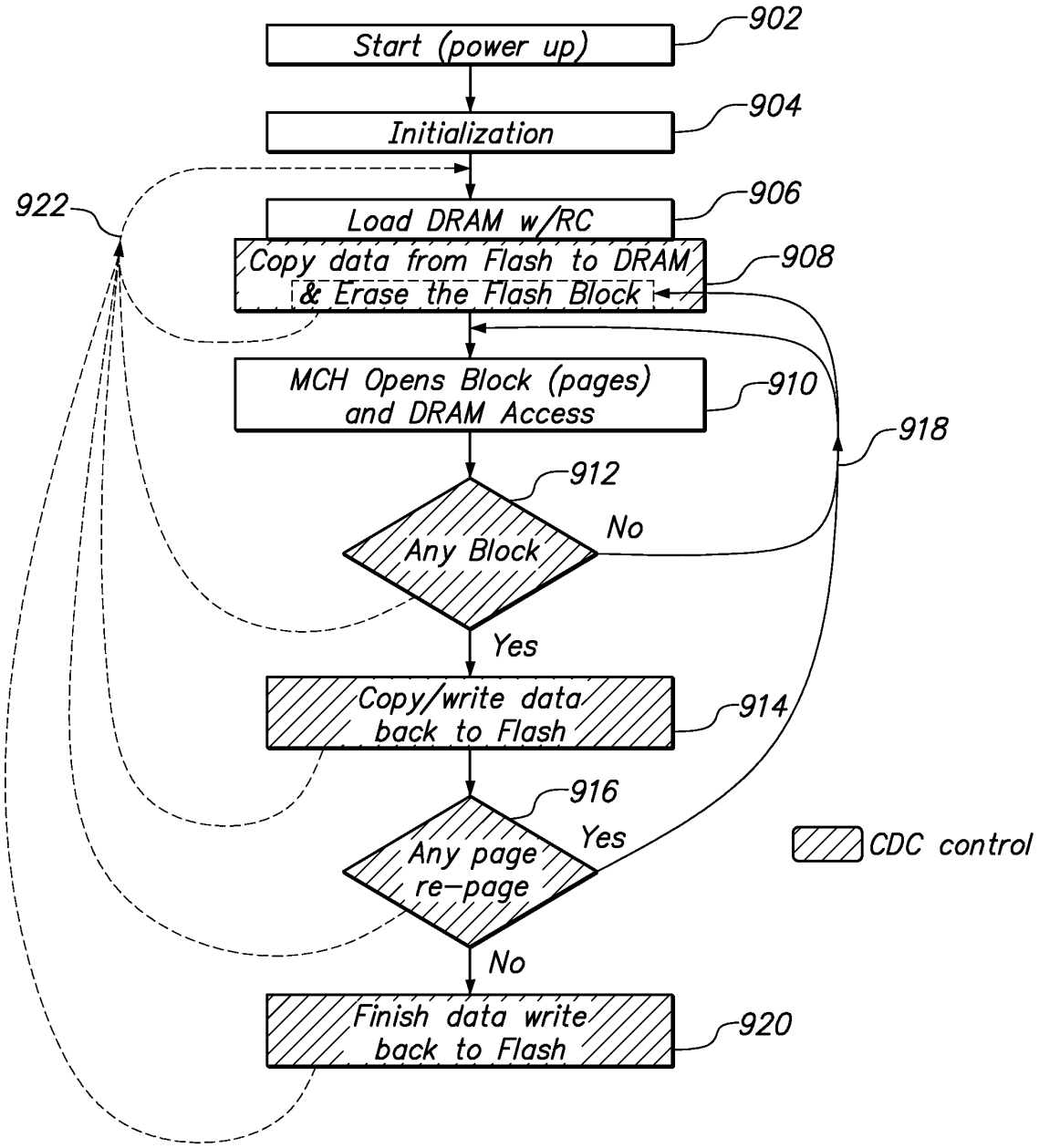

Start (power up)
902
Initialization
904
Load DRAM w/RC
906
Copy data from Flash to DRAM
& Erase the Flash Block
908
922
MCH Opens Block (pages)
and DRAM Access
910
918
912
Any Block
No
Yes
Copy/write data
back to Flash
914
916
Any page
re-page
Yes
No
Finish data write
back to Flash
920
CDC control

FIG. 9

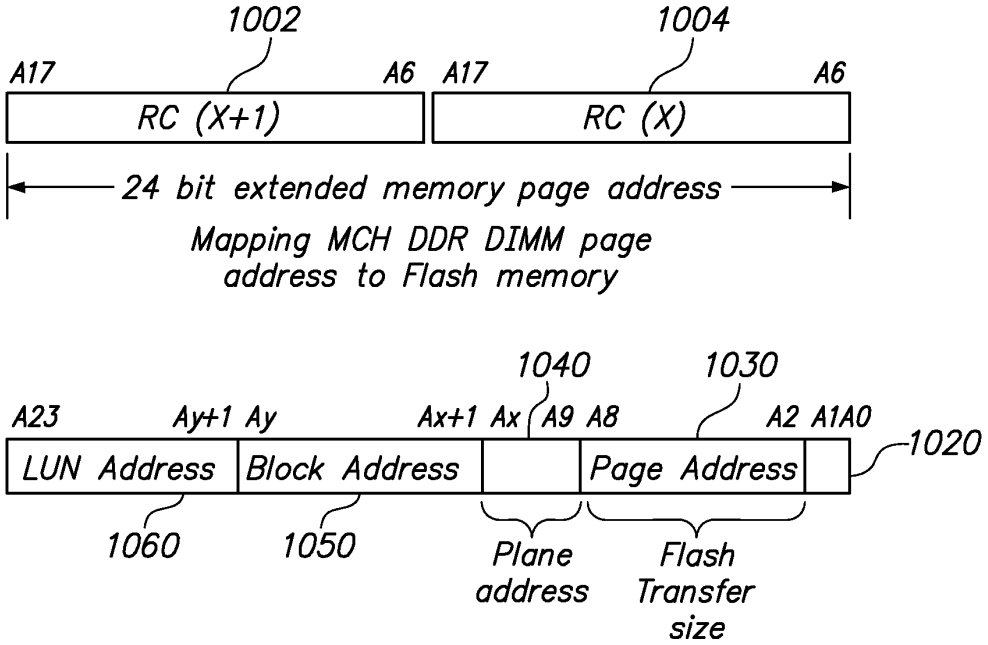

1002
1004
A17
A6
A17
A6
RC (X+1)
RC (X)
24 bit extended memory page address
Mapping MCH DDR DIMM page address to Flash memory
1040
1030
A23
Ay+1
Ay
Ax+1
Ax
A9
A8
A2
A1A0
1020
LUN Address
Block Address
Page Address
1060
1050
Plane address
Flash Transfer size

FIG. 10

DRAM density (GB)	# of blocks per bank	Flash wr–time to rd–time ratio	Avg block use time (sec)	Flash write time (sec)	Max allowed Closed Blk in queue to be written back to Flash
1	250	55	1.00E–03	2.00E–02	0
1	250	55	1.00E–02	2.00E–02	2
1	250	55	2.00E–02	2.00E–02	5
1	250	55	5.00E–02	2.00E–02	11
2	500	55	1.00E–03	2.00E–02	0
2	500	55	1.00E–02	2.00E–02	5
2	500	55	2.00E–02	2.00E–02	9
2	500	55	5.00E–02	2.00E–02	23
4	1000	55	1.00E–03	2.00E–02	1
4	1000	55	1.00E–02	2.00E–02	9
4	1000	55	2.00E–02	2.00E–02	18
4	1000	55	5.00E–02	2.00E–02	45

FIG. 11

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee et al.	
SERIAL NO.:	13/559,476	CONFIRMATION NO: 1046
FILING DATE:	July 26, 2012	
TITLE:	Flash-DRAM Hybrid Memory Module	
EXAMINER:	Elmore, Stephen C.	
ART UNIT:	2188	

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPLICANT'S COMMENTS ON REASONS FOR ALLOWANCE

These comments are responsive to the Notice of Allowance, mailed on May 6, 2014.

Applicant gratefully acknowledges the indication of allowance of Claims 1-5, 9, 13, 14, 16, 18, 19 and 21-24. Applicant respectfully urges that additional and/or alternative reasons for allowance may exist apart from those advanced by the Examiner and the Applicant, and these reasons may each be independently sufficient to establish the patentability of the allowed claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 251

Please charge any additional required fee or credit any overpayment to our Deposit Account number 50-3557.

Respectfully submitted,
NIXON PEABODY LLP

Dated: August 6, 2014

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

NIXON PEABODY LLP
P.O. BOX 60610
PALO ALTO, CA 94306
TEL. (650) 320-7700
FAX (650) 320-7701

Samsung Electronics Co., Ltd.
Ex. 1009, p. 252

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	09/16/2014	8838886	062453-010	1046

46188 7590 08/27/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 176 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

The United States represents the largest, most dynamic marketplace in the world and is an unparalleled location for business investment, innovation, and commercialization of new technologies. The USA offers tremendous resources and advantages for those who invest and manufacture goods here. Through SelectUSA, our nation works to encourage and facilitate business investment. To learn more about why the USA is the best country in the world to develop technology, manufacture products, and grow your business, visit SelectUSA.gov.

IR103 (Rev. 10/09)

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

REQUEST FOR CONTINUED EXAMINATION(RCE)TRANSMITTAL
(Submitted Only via EFS-Web)

Application Number	13559476	Filing Date	2012-08-26	Docket Number (if applicable)	062453-010	Art Unit	2188
First Named Inventor	Hyun LEE			Examiner Name	Stephen C. ELMORE		

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. The Instruction Sheet for this form is located at WWW.USPTO.GOV

SUBMISSION REQUIRED UNDER 37 CFR 1.114

Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

☐ Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

- ☐ Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____
- ☐ Other _____

☒ Enclosed

- ☐ Amendment/Reply
- ☒ Information Disclosure Statement (IDS)
- ☐ Affidavit(s)/ Declaration(s)
- ☒ Other Certification and Request for Consideration of the Information Disclosure Statement Filed After Payment of Issue Fee Under the QPIDS Pilot Program

MISCELLANEOUS

☐ Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of months _____
(Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

☐ Other _____

FEES

☒ **The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.**
The Director is hereby authorized to charge any underpayment of fees, or credit any overpayments, to Deposit Account No 503557

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

☒ Patent Practitioner Signature

☐ Applicant Signature

PTO/SB/30EFS (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Signature of Registered U.S. Patent Practitioner			
Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-09-05
Name	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: QPIDS.REQ
Document Description: Quick Path Information Disclosure Statement

PTO/SB/09 (08-14)

CERTIFICATION AND REQUEST FOR CONSIDERATION OF AN INFORMATION DISCLOSURE STATEMENT FILED AFTER PAYMENT OF THE ISSUE FEE UNDER THE QPIDS PILOT PROGRAM

Non-Provisional Application Number: 13/559,476	Filing Date: 2012-08-26
First Named Inventor: Hyun LEE	Title of Invention: FLASH-DRAM HYBRID MEMORY MODULE

THE UNDERSIGNED HEREBY CERTIFIES AND REQUESTS THE FOLLOWING FOR THE ABOVE-IDENTIFIED APPLICATION.

1. Consideration is requested of the information disclosure statement (IDS) submitted herewith, which is being filed after payment of the issue fee.
2. Check the box next to the appropriate selection:

   ☐ Each item of information contained in the IDS was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the IDS. See 37 CFR 1.97(e)(1).

   OR

   ☑ No item of information contained in the IDS was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the IDS was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the IDS. See 37 CFR 1.97(e)(2).
3. Please charge the IDS fee set forth in 37 CFR 1.17(p) to Deposit Account No. 50-3557.
4. A Petition to Withdraw from Issue After Payment of the Issue Fee (37 CFR 1.313(c)(2)), including the petition fee set forth in 37 CFR 1.17(h), is submitted herewith as a **Web-based ePetition**.
   WARNING: Do not submit the petition as a follow-on paper via EFS-Web. Submit the petition as a Web-based ePetition by signing on to EFS-Web as a registered user, selecting the radio button next to "Existing application/patent," and then selecting the radio button next to "ePetition (for automatic processing and immediate grant, if all petitions requirements are met)." Failure to use the Web-based ePetition interface will result in automatic entry of the RCE.
5. A request for continued examination (RCE) under 37 CFR 1.114 and the RCE fee under 37 CFR 1.17(e) are submitted herewith.
6. The RCE will be treated as a "conditional" RCE. In the event the examiner determines that any item of information contained in the IDS necessitates the reopening of prosecution in the application, the undersigned understands that (i) the RCE will be processed and treated as an RCE under 37 CFR 1.114 and therefore (ii) the IDS fee under 37 CFR 1.17(p) will be returned in accordance with 37 CFR 1.97(b)(4). In the event that no item of information in the IDS necessitates reopening prosecution, the undersigned understands that the RCE will not be processed and the RCE fee under 37 CFR 1.17(e) will be returned.
7. This certification and request is being filed as a **Web-based ePetition** and is not accompanied by an amendment to the application. Inclusion of an amendment will result in automatic entry of the RCE.

Signature /Khaled Shami/	Date 2014-09-05
Name (Print/Typed) Khaled Shami	Practitioner Registration Number (If applicable) 38,745

Note: *Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required in accordance with 37 CFR 1.33 and 11.18. Please see 37 CFR 1.4(d) for the form of the signature. If necessary, submit multiple forms for more than one signature, see below.**

☐ *Total of _____ forms are submitted.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

Privacy Act Statement

The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Doc Code: PET.AUTO Document Description: Petition automatically granted by EFS-Web	PTO/SB/140 U.S. Patent and Trademark Office Department of Commerce

Electronic Petition Request	**PETITION TO WITHDRAW AN APPLICATION FROM ISSUE AFTER PAYMENT OF THE ISSUE FEE UNDER 37 CFR 1.313(c)**
Application Number	13559476
Filing Date	26-Jul-2012
First Named Inventor	Hyun Lee
Art Unit	2188
Examiner Name	STEPHEN ELMORE
Attorney Docket Number	062453-010
Title	FLASH-DRAM HYBRID MEMORY MODULE

An application may be withdrawn from issue for further action upon petition by the applicant. To request that the Office withdraw an application from issue, applicant must file a petition under this section including the fee set forth in § 1.17(h) and a showing of good and sufficient reasons why withdrawal of the application from issue is necessary.

APPLICANT HEREBY PETITIONS TO WITHDRAW THIS APPLICATION FROM ISSUE UNDER 37 CFR 1.313(c).

A grantable petition requires the following items:
(1) Petition fee; and
(2) One of the following reasons:
(a) Unpatentability of one or more claims, which must be accompanied by an unequivocal statement that one or more claims are unpatentable, an amendment to such claim or claims, and an explanation as to how the amendment causes such claim or claims to be patentable;
(b) Consideration of a request for continued examination in compliance with § 1.114 (for a utility or plant application only); or
(c) Express abandonment of the application. Such express abandonment may be in favor of a continuing application, but not a CPA under 37 CFR 1.53(d).

Petition Fee

- (●) Small Entity
- ( ) Micro Entity
- ( ) Regular Undiscounted

Reason for withdrawal from issue

○ One or more claims are unpatentable ◉ Consideration of a request for continued examination (RCE) (List of Required Documents and Fees) ○ Applicant hereby expressly abandons the instant application (any attorney/agent signing for this reason must have power of attorney pursuant to 37 CFR 1.32(b)).
RCE request,submission, and fee. ☐ I certify, in accordance with 37 CFR 1.4(d)(4) that : The RCE request ,submission, and fee have already been filed in the above-identified application on ☒ Are attached.
THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ◉ An attorney or agent registered to practice before the Patent and Trademark Office who has been given power of attorney in this application. ○ An attorney or agent registered to practice before the Patent and Trademark Office, acting in a representative capacity. ○ A sole inventor ○ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ○ A joint inventor; all of whom are signing this e-petition

Signature	/Khaled Shami/
Name	Khaled Shami
Registration Number	38745

Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-010

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Petition Fee-37CFR 1.17(h) (Group II)	2464	1	70	70
Request for Continued Examination	2801	1	600	600
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Extension-of-Time:				
Miscellaneous:				
		Total in USD ($)		**670**

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

Decision Date : September 5, 2014

In re Application of :

Hyun Lee

Application No : 13559476

Filed : 26-Jul-2012

Attorney Docket No : 062453-010

DECISION ON PETITION

UNDER CFR 1.313(c)(2)

This is an electronic decision on the petition under 37 CFR 1.313(c)(2), filed September 5, 2014 to withdraw the above-identified application from issue after payment of the issue fee.

The petition is **GRANTED.**

The above-identified application is withdrawn from issue for consideration of a submission under 37 CFR 1.114 (request for continued examination). See 37 CFR 1.313(c)(2).

Petitioner is advised that the issue fee paid in this application cannot be refunded. If, however, this application is again allowed, petitioner may request that it be applied towards the issue fee required by the new Notice of Allowance.

Telephone inquiries concerning this decision should be directed to the Patent Electronic Business Center (EBC) at 866-217-9197.

This application file is being referred to Technology Center AU 2188 for processing of the request for continuing examination under 37 CFR 1.114 .

Office of Petitions

Electronic Acknowledgement Receipt	
EFS ID:	20055150
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	05-SEP-2014
Filing Date:	26-JUL-2012
Time Stamp:	11:59:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$670
RAM confirmation Number	9407
Deposit Account	503557
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Continued Examination (RCE)	RCE.pdf	722759 ae884bd7800065e952966a7ff6f3915abf883705	no	3
Warnings:					
Information:					
2	Transmittal Letter	QPIDS_petition.pdf	153108 28f1d8909a9c172ac30a3e9c43b5399353b64e38	no	2
Warnings:					
Information:					
3	Quick Path Information Disclosure Statement	062453-010_IDS_1_of_2_dated_09-05-2014_f.pdf	78148 903ebadb3aed372a1303dcd39ef1adc8727fb96a	no	5
Warnings:					
Information:					
4	Quick Path Information Disclosure Statement	062453-010_IDS_2_of_2_dated_09-05-2014_f.pdf	93863 6e72ed352d12a52522df07e75b4cd4a048aaf264	no	9
Warnings:					
Information:					
5	Petition automatically granted by EFS	petition-request.pdf	31539 76ceeff4418beb957ebbcb605aa6403823e739b2	no	2
Warnings:					
Information:					
6	Fee Worksheet (SB06)	fee-info.pdf	32092 b334a2148d09e043df5e6c7757ea1daae3f782fc	no	2
Warnings:					
Information:					
			Total Files Size (in bytes):	1111509	

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt

EFS ID:	20052493
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	05-SEP-2014
Filing Date:	26-JUL-2012
Time Stamp:	12:01:24
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	JEDEC21-C.pdf	427496 724cded39aa33581516ae1037c08fd3bf329c93f	no	18

Warnings:

Information:

2	Non Patent Literature	Diablo_INVALIDITY_CONTENTIONS_Redacted_Part_1_of_3.pdf	9884128 ec5b633b40e4756a29424f7fa5ca97b58b088f1b	no	128
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Information:					
3	Non Patent Literature	Diablo_INVALIDITY_CONTENTIONS_Redacted_Part_2_of_3.pdf	10136012 18b6a42976e212855c703752512ca902516defb7	no	126
Warnings:					
Information:					
4	Non Patent Literature	Diablo_INVALIDITY_CONTENTIONS_Redacted_Part_3_of_3.pdf	11441351 7bc10674dc6a234e3c80540f0a1b1f65dece277d	no	124
Warnings:					
Information:					
5	Non Patent Literature	Diablo_INVALIDITY_CONTENTIONS_REGULAR_NO_Exhibits.pdf	5190188 85187f818e0160cf5f2916865bb21d51401d485e	no	56
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Information:					
6	Non Patent Literature	Smart_Storage_INVALIDITY_CONTENTIONS_Redacted_Part_1_of_4.pdf	12866211 313b061a2da26af1aebde5694835b2402f47b636	no	169
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Information:					
7	Non Patent Literature	Smart_Storage_INVALIDITY_CONTENTIONS_Redacted_Part_2_of_4.pdf	15887104 4e959ae0063c21547a778c161be8594d1ab69928	no	147
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Information:					
8	Non Patent Literature	Smart_Storage_INVALIDITY_CONTENTIONS_Redacted_Part_3_of_4.pdf	15486864 e3f7e686ed97f40abba5a4ad2060a36c6bf2211f	no	132
Warnings:					
Information:					
9	Non Patent Literature	Smart_Storage_INVALIDITY_CONTENTIONS_Redacted_Part_4_of_4.pdf	12151878 9d26b7c7e5418869758a265b3082c2e8b1062dfc	no	136
Warnings:					
Information:					
10	Non Patent Literature	Smart_Storage_INVALIDITY_CONTENTIONS_REGULAR_NO_Exhibits.pdf	6094810 207dc6742575898e259c398f62262b52fa4c4191	no	100
Warnings:					
Information:					

11	Non Patent Literature	Bruce_Synchronous_DRAM_Architectures_Organizations.pdf	2373997 b906ef4334b40d2cd451a2eba77b45f0d8ec95d7	no	22
Warnings:					
Information:					
12	Non Patent Literature	David_Fully_Buffered_DIMM.pdf	21697487 0d141cc8b1e95f74cb83556fe08a8082d23e4628	no	36
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
13	Non Patent Literature	Horowitz_The_Art_of_Electronics.pdf	1277181 5888c452b6dfcec9affe0fe1af52fc3b1217dea4	no	15
Warnings:					
Information:					
14	Non Patent Literature	Innis_MPC8560_PowerQUICCIII_Compact_Flash_Interface_Design.pdf	2723361 9393028aeabc43a647a8984d424aab67abe24706	no	24
Warnings:					
Information:					
15	Non Patent Literature	Jacob_Memory_Systems_Cache_DRAM_Disk.pdf	1576215 b8c7166a007a5ad79a9ec15fbb674e383bbbb24c	no	15
Warnings:					
Information:					
16	Non Patent Literature	Jandhyala_Design_For_Test_Analysis_Buffered_DRAM_DIMM_IEEE_Semiconductor_Group.pdf	1434512 682e1320112a3bb7b6fc2df93eb39d12c6e2c0fe	no	15
Warnings:					
Information:					
17	Non Patent Literature	JEDEC_Double_Data_Rate_DDR_SDRAM_Spec.pdf	8467564 739ebc109a9560e511bdc8840f525c49b5564c52	no	82
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18	Non Patent Literature	JEDEC_Standard_FBDIMM_Specification_JESD205.pdf	12289532 f3dacdb47071656d8c7779389ee99b774c128824	no	129
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19	Non Patent Literature	Mutnuary_Analysis_of_Fully_Buffered_DIMM_Interface.pdf	824400 f1b6d894ce374d5e806a1cab688eac4913b2f42c	no	6

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20	Non Patent Literature	SanDISK_INTERPARTES_Review_8516187_Part_1_of_3.pdf	9699421 25edd77e348ee128475459042b74895b6464a1a9	no	124
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21	Non Patent Literature	SanDISK_INTERPARTES_Review_8516187_Part_2_of_3.pdf	7539544 c9a0cbefec79cd8574244f9fff270149ff3434f	no	124
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22	Non Patent Literature	SanDISK_INTERPARTES_Review_8516187_Part_3_of_3.pdf	7508670 6de44c254e0beb4c1c9e095bcc7b12829972f55c	no	114
Warnings:					
Information:					
23	Non Patent Literature	SanDISK_INTERPARTES_Review_8301833_Part_2_of_3.pdf	9155369 c83ddd990594309cddb3d9179ca72cdfc2a7db17	no	125
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24	Non Patent Literature	SanDISK_INTERPARTES_Review_8301833_Part_3_of_3.pdf	8284508 5e9f05073b305f95d19a84d7af453465d87ae95c	no	113
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25	Non Patent Literature	SanDISK_INTERPARTES_Review_8301833_Part_1_of_3.pdf	7612188 497ade5addaf2abd59619da5489ebbb5b4f39e59	no	113
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Information:					
26	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_1_of_8.pdf	18923000 e14bd3f4cc4742eb004baf2e58cad996eb66c1fc	no	121
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Information:					
27	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_2_of_8.pdf	21016670 b35816a70cd850f5b74a55f5955baa37d128796a	no	123
Warnings:					
Information:					
28	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_3_of_8.pdf	26015708 0cbbd7bef6932f07e45dd0391358ba39c43e1d9e	no	157

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29	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_4_of_8.pdf	21329680 4f33260f71a465f46583d8dffefa3efc590a66fa	no	137
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Information:					
30	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_5_of_8.pdf	17570496 71d44640c7678d1d15fb04f0df7352a1b56a123d	no	168
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31	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_6_of_8.pdf	10894604 c46f8ee941b9d03ef97286f152adf61ecdcfc894	no	85
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32	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_7_of_8.pdf	10806690 8319af8149ecf885cf355ef9c2902a4c4ffd6128	no	105
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Information:					
33	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8516187_Part_8_of_8.pdf	23006724 2454df0b12bcb3bf2af7f5db4ecb0d13cc463e25	no	70
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Information:					
34	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_1_of_6.pdf	2943276 0eae3bcb323c8eeea9ac128302b3bfd282bef22f	no	128
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35	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_2_of_6.pdf	1592771 7db414d586461d49d795a0074e6ca21a7f527a00	no	128
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Information:					
36	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_3_of_6.pdf	2861988 ea27acb6dc3af76bd4c96e0630eee61c3b14d804	no	128
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Information:					
37	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_4_of_6.pdf	10558618 3ba030454c84a4ba38a06d6bb514747a206d1dd6	no	179

Warnings:					
Information:					
38	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_6_of_6.pdf	8657521 66702e5024d2cebbcdd3e4861beb519a033b67aa	no	50
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Information:					
39	Non Patent Literature	SMART_Inter_PARTES_Petition_For_Review_8301833_Part_5_of_6.pdf	17071395 29098017e13051156e02cc6e8121d90e18272e3f	no	155
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Information:					
40	Non Patent Literature	Using_Two_Chip_Selects_to_Enable_Quad_Rank.pdf	884607 fa05e52784c65f8589e83895079c6beedf600c5a	no	2
Warnings:					
Information:					
41	Non Patent Literature	MetaRAM_Develops_New_Technology_SNDK-NET-0000386.pdf	483215 0e5597e9f10d47f0e88c0c2b9cff6985892615 41	no	3
Warnings:					
Information:					
42	Non Patent Literature	HYNIX_240pin_DDR2_MetaSDRAM_SNDK-NET-0000389.pdf	2020886 35fd594dcd6ae3924af0b0c6982e2f11d496daf5	no	32
Warnings:					
Information:					
43	Non Patent Literature	NPL_WONG_1998-2001_BIOS_Optimization_Guide_67_pages.pdf	1301358 80901a3dd53f5efd3af6a97c1e01c961334626af	no	67
Warnings:					
Information:					
44	Non Patent Literature	ANS_1988_Dictionary_Electrical_Electrical_Terms_pp_215_722_964_1103.pdf	1504338 5ce54aeb84f7e2c1f02be0ab4029d93f1c75d2bb	no	6
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45	Non Patent Literature	Websters_New_College_Dictionary_2001_pp_259_1115.pdf	969448 2a2f89e3ffcfe1e1ec9747fa5562256114858cd5	no	4
Warnings:					
Information:					

46	Non Patent Literature	Out_Of_Stealth_Mode_Start_Up_Storage_Newsletter_SNDK-NET-0000361.pdf	2727068 94d7509cfc790659409ee276bf946c6f90e5abe8	no	8
Warnings:					
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47	Non Patent Literature	JEDEC_Configurations_For_Solid_State_Std_21-C_Release_9_August_1999.pdf	21706341 e00b93ebef389deae120f48b7d629935d40c36ee	no	114
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			Total Files Size (in bytes):	426876393	

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<u>New Applications Under 35 U.S.C. 111</u>
If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

<u>National Stage of an International Application under 35 U.S.C. 371</u>
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

<u>New International Application Filed with the USPTO as a Receiving Office</u>
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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PATENT AND TRADEMARK OFFICE

PATENT WITHDRAWAL NOTICE

DATE WITHDRAWN	WITHDRAWAL NUMBER
9/9/2014	26649

The following application has been **WITHDRAWN** from the

9/16/2014 issue.

SERIAL NO.	PATENT NUMBER
13559476	8838886

TITLE

FLASH-DRAM HYBRID MEMORY MODULE

NAME AND ADDRESS

HYUN LEE
Ladera Ranch, CA

REASON FOR WITHDRAWAL

Auto-petition to withdraw - Granted
-

APPROVED

/Kimberly Terrell/, Manager

Patent Publication Branch
Office of Data Management

FORM PTO-302 -- (REV. 05-2009)

U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	07/26/2012	Hyun Lee	062453-010	1046

46188 7590 09/29/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

EXAMINER
ELMORE, STEPHEN C

ART UNIT	PAPER NUMBER
2188	

NOTIFICATION DATE	DELIVERY MODE
09/29/2014	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

patentsv@nixonpeabody.com
ocastanon@nixonpeabody.com

Samsung Electronics Co., Ltd.
Ex. 1009, p. 277

Corrected Notice of Allowability	Application No. 13/559,476	Applicant(s) LEE ET AL.	
	Examiner STEPHEN ELMORE	Art Unit 2188	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *See Continuation Sheet*.
   ☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on_____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are *1-5,9,13,14,16,18,19 and 21-24*. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov .
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

   Certified copies:

   a) ☐ All b) ☐ Some *c) ☐ None of the:
   1. ☐ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/5/2014 and 9/5/2014
3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
4. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
5. ☒ Examiner's Amendment/Comment
6. ☐ Examiner's Statement of Reasons for Allowance
7. ☒ Other *Response to Rule 312 Amendment (PTOL-271)*.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

Samsung Electronics Co., Ltd.
Ex. 1009, p. 278

Continuation of Item 1. This communication is responsive to : the Petition to Withdraw an Application From Issue Under 37 CFR 1.313(c) and QPIDS Pilot Program submission both filed 9/5/2014, and Rule 312 Amendment and Replacement Drawings both filed 8/6/2014.

Samsung Electronics Co., Ltd.
Ex. 1009, p. 279

The present application is being examined under the pre-AIA first to invent provisions.

Drawings

The replacement drawings were received on 8/6/2014. These drawings are approved.

Information Disclosure Statement

The two (2) IDS [PTOL-1449's] submitted 9/5/2014 includes listed publications that have been "lined-through" because the listings fail to comply with 37 CFR § 1.98 (b)(5), which requires the following information: publisher, author (if any), title, relevant pages of the publication, date, and place of publication.

Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609.05(a).

A copy of the submitted PTOL-1449(s) otherwise initialed and dated by the examiner is attached to the instant office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to STEPHEN ELMORE whose telephone number is (571)272-4436. The examiner can normally be reached on Mon-Fri from 9:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571) 272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

September 19, 2014

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	LEE, Hyun
	Art Unit	2188
	Examiner Name	ELMORE, STEPHEN C
	Attorney Docket Number	062453-010 2 of 2

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	2043099		1936-02-02	Hanna	
	2	3562555		1971-02-09	Ahrons	
	3	3916390		1975-10-28	Chang et al.	
	4	4234920		1980-11-18	Van Ness et al.	
	5	5430742		1995-07-04	Jeddeloh et al.	
	6	5563839		1996-10-08	Herdt et al.	
	7	5870350		1999-02-09	Bertin et al.	
	8	5874995		1999-02-23	Naimpally et al.	

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Receipt date: 09/05/2014	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

	9	5890192		1999-03-30	Lee et al.	
	10	5953215		1999-09-14	Karabatsos	
	11	6023421		2000-02-08	Clinton et al.	
	12	6112310		2000-08-29	Jun et al.	
	13	6216247	B1	2001-04-10	Creta et al.	
	14	6459647	B1	2002-10-01	Kengeri	
	15	6769081	B1	2004-07-27	Parulkar	
	16	6799241	B2	2004-09-28	Kahn et al.	
	17	6487102	B1	2002-11-26	Halbert et al.	
	18	6948029	B2	2005-09-20	Yano	
	19	7053470	B1	2006-05-30	Sellers et al.	

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	First Named Inventor	LEE, Hyun	
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	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

	20	7089412	B2	2006-08-08	Chen	
	21	7102391	B1	2006-09-05	Sun et al.	
	22	7155627	B2	2006-12-26	Matsui	
	23	7200021	B2	2007-04-03	Raghuram	
	24	7234099	B2	2007-06-19	Gower et al.	
	25	7409491	B2	2008-12-05	Doblar et al.	
	26	7818488	B2	2010-10-19	Park et al.	
	27	8233303	B2	2012-07-31	Best et al.	
	28	4965828		1990-10-23	Ergott, Jr. et al.	
	29	5519831	A	1996-05-21	Holzhammer	

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	First Named Inventor	LEE, Hyun	
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	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20040163027	A1	2004-08-19	MacLaren et al.	
	2	20050044302	A1	2005-02-25	Pauley et al.	
	3	20050060488	A1	2005-03-17	Poechmueller	
	4	20050132250	A1	2005-06-16	Hansen et al.	
	5	20060080515	A1	2006-04-13	Spiers et al.	
	6	20090031099	A1	2009-01-29	Sartore	

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FOREIGN PATENT DOCUMENTS

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Receipt date: 09/05/2014	Application Number	13559476	13559476 - GAU: 2188
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	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T5
	1	Bruce, J., "Synchronous DRAM Architectures, Organizations, and Alternate Technologies", Electrical and Computer Enginnering Dept., Univ. of Maryland, December 10, 2002, 22 pages.	☐
	2	David, H. et al., "Fully Buffered DIMM (FB-DIMM) Design Considerations", Intel Developer Forum, Intel Corp., February 18, 2004, 36 pages.	☐
	3	Horowitz, P. et al., "The Art of Electronics", Cambridge Univesity Press 2nd Ed. 1989, pp. 471, 495-496.	☐
	4	Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.	☐
	5	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322.	☐
	6	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, August 13014, 1996, 15 pages.	☐
	7	JEDEC Standard, Double Data Rate (DDR): SDRAM Specification: JESD79C (Revision JESD79B), March 2003, pp. 1-75.	☐
	8	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification: JESD205, JEDEC SOLID STATE TECH. ASSOC., March 2007, pp. 1-129.	☐
	9	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp, xSeries eServer Development, 2006 Electronic Components and Technology Conference, pp. 203-208.	☐
	10	Petition for Inter Partes Review of U.S. Patent No. 8,546,187 (on behalf of SanDisk, Corp.), filed June 19, 2014.	☐

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	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

	11	~~Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed June 20, 2014.~~	☐
	12	~~Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.~~	☐
	13	~~Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed August 22, 2014.~~	☐
	14	"Using Two Chip Selects to Enable Quad Rank", an IP.com Prior Art Database Technical Disclosure, IP.com Electronic Publication: December 17, 2005, 2 pages.	☐
	15	"Out of Stealth Mode, Start-Up MetaRAM Unveils New Technology That Quadruples DRAM Capacity", Press Release edited by Storage Newsletter on February 28, 2008 at StorageNewsLetter.com, 8 pages.	☐
	16	"MetaRAM Develops New Technology That Quadruples Memory Capacity of Servers and Workstations; Reduces Price by Up to 90 Percent", Press Release provided by MetaRAM and published on MarketWired.com, February 25, 2008, 3 pages.	☐
	17	"240pin DDR2 MetaSDRAM Registered DIMM based on 1 GB version C", Hynix Semiconductor, Product Description Rev. 0.2, September 2008, 32 pages.	☐
	18	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21–C, Release 9, August 1999, 114 pages.	☐
	19	WONG, A. "The BIOS Optimization Guide", Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.	☐
	20	American National Standard Dictionary of Electrical and Electrical Terms, IEEE, Fourth Edition, Revised, ANS/IEEE Std 100-1988, Institute of Electrical Engineers, November 3, 1988, pp. 215, 722, 964 and 1103.	☐
	21	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 259, 1115.	☐

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

Receipt date: 09/05/2014	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

If you wish to add additional non-patent literature document citation information please click the Add button			
EXAMINER SIGNATURE			
Examiner Signature	/Stephen Elmore/	Date Considered	09/24/2014
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

[1]See Kind Codes of USPTO Patent Documents at www.USPTO.GOVor MPEP 901.04. [2]Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5]Applicant is to place a check mark here if English language translation is attached.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

Receipt date: 09/05/2014	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 2 of 2	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-09-05
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.

2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.

3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.

4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).

5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.

6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).

7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.

8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.

9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /S.E./

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	9438	711/103.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L2	2687	365/185.33.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L3	19492	711/111,112,114,154,156.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L4	29661	L1 or L2 or L3	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L5	4794	hybrid near3 memory	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L6	566	data adj manager and controller and memory adj controller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L7	9	L5 and L6	US-PGPUB; USPAT;	OR	ON	2014/09/19 17:48

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			USOCR; FPRS; EPO; JPO; IBM_TDB			
L8	3	L7 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L9	2	(US-20070136523-$).did. or (US-8412879-$).did.	US-PGPUB; USPAT	OR	ON	2014/09/19 17:48
L10	162084	(format$3 near3 data) with (transfer or transferred or transferring or move or moved or moving or transmitted or transmission or write or written or writing or store or stored or storing)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L11	83	L6 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L12	1	L5 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L13	3	L4 and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L14	349	(bi-direction or bi-directional) near3 fabric	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L15	1	L14 with (data adj manager)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2014/09/19 17:48

			EPO; JPO; IBM_TDB			
L16	19	(data near3 (port or input-output or I/O or IO)) and L11	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L17	1	L5 and L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L18	15	L16 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L19	0	L4 and L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L20	15	L6 and L18	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L21	0	L14 and L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L22	0	L5 and L20	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L23	29572	(control adj information or control adj data or control adj meta-data or control	US-PGPUB;	OR	ON	2014/09/19 17:48

		adj metadata) near3 controller	USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB			
L24	1	((control adj information or control adj data or control adj meta-data or control adj metadata) near3 controller) and L16	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L25	1	L6 and L23 and L10 and L4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L26	1	L6 and L23 and L10	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L27	7	L6 and L23	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L28	5655	((Hyun) near2 (Lee)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/09/19 17:48
L29	14	((Chi-She) near2 (Chen)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/09/19 17:48
L30	94	((Jeffrey) near2 (Solomon)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/09/19 17:48
L31	158	((Scott) near2 (Milton)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/09/19 17:48
L32	80	((Jayesh) near2 (Bhakta)).INV.	US-PGPUB; USPAT; USOCR	OR	ON	2014/09/19 17:48
L33	1	(data adj manager same controller same memory adj controller) and L5 and (L10	US-PGPUB;	OR	ON	2014/09/19 17:48

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Ex. 1009, p. 294

		or L14)	USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB			
L34	539	(hybrid near3 memory).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L35	5	L6 and L34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L36	0	L35 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L37	5	(data adj manager and memory adj controller) and L34	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L38	0	L37 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L39	1	(data adj manager) and L34 and ((@pd or @ad)<"20120726")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L40	37	("20080195806" | "6658507" | "5675725" | "20040190210" | "6336176" | "7409590" | "20100274953" | "6336174" | "5519663" | "6487623" | "20080104344" | "4420821" | "6799244" | "20020083368" | "4449205" | "8301833" | "7111142" | "20070192627" | "6158015" | "20120204079").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48

L41	1	L6 and L40	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:48
L53	109	("2043099" | "20030158995" | "20040163027" | "20050044302" | "20050060488" | "20050132250" | "20050141273" | "20060039197" | "20060069896" | "20060080515" | "20060294295" | "20090031099" | "3562555" | "3916390" | "4234920" | "4965828" | "5430742" | "5519831" | "5563839" | "5870350" | "5874995" | "5890192" | "5953215" | "6023421" | "6112310" | "6145068" | "6199142" | "6216247" | "6421279" | "6459647" | "6487102" | "6769081" | "6799241" | "6944042" | "6948029" | "6952368" | "7053470" | "7062618" | "7089412" | "7102391" | "7155627" | "7200021" | "7234099" | "7409491" | "7411859" | "7421552" | "7467251" | "7600142" | "7716411" | "7818488" | "8233303").PN.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:52
L54	0	14 and 53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:52
L55	0	16 and 53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:52
L56	0	6 and 53	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; IBM_TDB	OR	ON	2014/09/19 17:53

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L42	15	((Chi-She) near2 (Chen)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L43	94	((Jeffrey) near2 (Solomon)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L44	114	((Scott) near2 (Milton)).INV.	US-PGPUB;	OR	ON	2014/09/19

			USPAT; UPAD			17:48
L45	81	((Jayesh) near2 (Bhakta)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L46	5660	((Hyun) near2 (Lee)).INV.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L47	5883	L42 or L43 or L44 or L45 or L46	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L48	6	(data adj manager with controller with memory adj controller).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L49	1	L47 and L48	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L50	12077	(data adj path or memory adj segment).clm.	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L51	38	L47 and L50	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48
L52	1	L48 and L51	US-PGPUB; USPAT; UPAD	OR	ON	2014/09/19 17:48

9/ 19/ 2014 5:53:35 PM
C:\ Users\ selmore\ Documents\ EAST\ Workspaces\ 13559476.wsp

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Ex. 1009, p. 297

Response to Rule 312 Communication	Application No.	Applicant(s)
	13/559,476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

1. ☒ The amendment filed on *06 August 2014* under 37 CFR 1.312 has been considered, and has been:

   a) ☐ entered.

   b) ☒ entered as directed to matters of form not affecting the scope of the invention.

   c) ☐ disapproved because the amendment was filed after the payment of the issue fee.
   Any amendment filed after the date the issue fee is paid must be accompanied by a petition under 37 CFR 1.313(c)(1) and the required fee to withdraw the application from issue.

   d) ☐ disapproved. See explanation below.

   e) ☐ entered in part. See explanation below.

/STEPHEN ELMORE/
Primary Examiner, Art Unit 2188

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Ex. 1009, p. 298

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)		
	Application Number	13559476
	Filing Date	2012-07-26
	First Named Inventor	LEE, Hyun
	Art Unit	2188
	Examiner Name	ELMORE, STEPHEN C
	Attorney Docket Number	062453-010 1 of 2

U.S.PATENTS						
Examiner Initial*	Cite No	Patent Number	Kind Code[1]	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6145068		2000-11-07	Lewis	
	2	6199142		2001-03-06	Saulsbury et al.	
	3	6421279		2002-07-16	Tobita et al.	
	4	6944042		2005-09-13	Komatsuzaki	
	5	6952368		2005-10-04	Miura et al.	
	6	7062618		2006-06-13	Tsunoda et al.	
	7	7411859		2008-08-12	Sohn et al.	
	8	7421552		2008-09-02	Long	

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Receipt date: 09/05/2014	Application Number	13559476	13559476 - GAU: 2188
INFORMATION DISCLOSURE STATEMENT BY APPLICANT **(Not for submission under 37 CFR 1.99)**	Filing Date	2012-07-26	
	First Named Inventor	LEE, Hyun	
	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 1 of 2	

	9	7467251		2008-12-16	Park et al.	
	10	7600142		1990-10-17	Groos	
	11	7716411		2010-05-11	Panabaker et al.	

If you wish to add additional U.S. Patent citation information please click the Add button.

U.S.PATENT APPLICATION PUBLICATIONS

Examiner Initial*	Cite No	Publication Number	Kind Code[1]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	20030158995		2003-08-21	Lee et al.	
	2	20050141273		2005-06-30	Park et al.	
	3	20060039197		2006-02-23	Khouri et al.	
	4	20060069896		2006-03-30	Sanders	
	5	20060294295		2006-12-28	Fukuzo	

If you wish to add additional U.S. Published Application citation information please click the Add button.

FOREIGN PATENT DOCUMENTS

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	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 1 of 2	

Examiner Initial*	Cite No	Foreign Document Number[3]	Country Code[2] ¡	Kind Code[4]	Publication Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	T[5]
	1							☐

If you wish to add additional Foreign Patent Document citation information please click the Add button

NON-PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T[5]
	1	JEDEC Standard 21–C, "Configurations for Solid State Memories," pp. 4.5.5–1 to 4.5.5–18.	☐
	2	Diablo Technologies, Inc.'s Invalidity Contentions, Case No. 13-CV-05889 YGR, dated June 6, 2014.	☐
	3	Smart Storage Systems, Inc's Invalidity Contentions, Case No. 4:13-cv-05889-YGR, dated June 6, 2014.	☐

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature	/Stephen Elmore/	Date Considered	09/22/2014

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

[1]See Kind Codes of USPTO Patent Documents at www.USPTO.GOVor MPEP 901.04. [2]Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). [3]For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. [4]Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. [5]Applicant is to place a check mark here if English language translation is attached.

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	Art Unit	2188	
	Examiner Name	ELMORE, STEPHEN C	
	Attorney Docket Number	062453-010 1 of 2	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2014-09-05
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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BIB DATA SHEET

CONFIRMATION NO. 1046

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/559,476	07/26/2012 RULE	711	2188	062453-010

APPLICANTS

INVENTORS

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

**** CONTINUING DATA ***************************

This appln claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

**** FOREIGN APPLICATIONS ****************************

**** IF REQUIRED, FOREIGN FILING LICENSE GRANTED **** ** SMALL ENTITY **
08/07/2012

Foreign Priority claimed	☐ Yes ☑ No		STATE OR COUNTRY	SHEETS DRAWINGS	TOTAL CLAIMS	INDEPENDENT CLAIMS
35 USC 119(a-d) conditions met	☐ Yes ☑ No	☐ Met after Allowance	CA	10	24	2
Verified and Acknowledged	/STEPHEN C ELMORE/ Examiner's Signature	Initials				

ADDRESS

Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306
UNITED STATES

TITLE

FLASH-DRAM HYBRID MEMORY MODULE

FILING FEE RECEIVED		
1620	FEES: Authority has been given in Paper No._____ to charge/credit DEPOSIT ACCOUNT No._____ for following:	☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____ ☐ Credit

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

CPC						
Symbol					**Type**	**Version**
G06F		12	/	0246	F	2013-01-01
G06F		1	/	185	I	2013-01-01
G06F		2212	/	205	A	2013-01-01
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CPC Combination Sets							
Symbol				**Type**	**Set**	**Ranking**	**Version**
			/				
			/				

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	9/19/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

Part of Paper No. 20140919

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

US ORIGINAL CLASSIFICATION		INTERNATIONAL CLASSIFICATION									
CLASS	SUBCLASS	CLAIMED					NON-CLAIMED				
711	103	G	0	6	F	12 / 02 (2006.01.01)					

CROSS REFERENCE(S)					
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
711	111	112	114	154	156
365	185.33				

NONE (Assistant Examiner)	(Date)	Total Claims Allowed: 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	9/19/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

Part of Paper No. 20140919

Issue Classification	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

☒ **Claims renumbered in the same order as presented by applicant** ☐ **CPA** ☐ **T.D.** ☐ **R.1.47**

Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1														
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	19														
	21														
	22														
	23														
	24														

NONE (Assistant Examiner)	(Date)	**Total Claims Allowed:** 15	
/STEPHEN ELMORE/ Primary Examiner.Art Unit 2188 (Primary Examiner)	9/19/2014 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

U.S. Patent and Trademark Office

Part of Paper No. 20140919

Search Notes	Application/Control No.	Applicant(s)/Patent Under Reexamination
	13559476	LEE ET AL.
	Examiner	**Art Unit**
	STEPHEN ELMORE	2188

CPC- SEARCHED

Symbol	Date	Examiner

CPC COMBINATION SETS - SEARCHED

Symbol	Date	Examiner

US CLASSIFICATION SEARCHED

Class	Subclass	Date	Examiner
711	103, 111, 112, 114, 154, 156	4/20/2014	SE
365	185.33	4/20/2014	SE
Search Updated		9/19/2014	SE

SEARCH NOTES

Search Notes	Date	Examiner
EAST	4/20/2014	SE
Inventor Name Search for DP	4/20/2014	SE
Search Updated	9/19/2014	SE

INTERFERENCE SEARCH

US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
711	103	4/20/2014	SE
PGPUB Searched		4/20/2014	SE
Search Updated		9/19/2014	SE

OK TO ENTER: /S.E./

/S.E./ 09/19/2014

Docket No.: 062453-010

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Hyun Lee et al.	
SERIAL NO.:	13/559,476	CONFIRMATION NO: 1046
FILING DATE:	July 26, 2012	
TITLE:	Flash-DRAM Hybrid Memory Module	
EXAMINER:	Elmore, Stephen C.	
ART UNIT:	2188	

Mail Stop Issue Fee
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE TO NOTICE TO FILE CORRECTED APPLICATION PAPERS

Dear Sir:

This paper is responsive to the notice mailed June 24, 2014. Please amend the above-identified application as follows:

Amendments to the Specification begin on page **2** of this paper.

Remarks begin on page **3** of this paper.

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Ex. 1009, p. 309

Electronic Acknowledgement Receipt

EFS ID:	20055150
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Pamela Wilson
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	05-SEP-2014
Filing Date:	26-JUL-2012
Time Stamp:	11:59:48
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	$670
RAM confirmation Number	9407
Deposit Account	503557
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Charge any Additional Fees required under 37 C.F.R. Section 1.20 (Post Issuance fees)

Charge any Additional Fees required under 37 C.F.R. Section 1.21 (Miscellaneous fees and charges)

Electronic Patent Application Fee Transmittal

Application Number:	13559476
Filing Date:	26-Jul-2012
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Filer:	Khaled Shami/Pamela Wilson
Attorney Docket Number:	062453-010

Filed as Small Entity

Utility under 35 USC 111(a) Filing Fees

Description	Fee Code	Quantity	Amount	Sub-Total in USD($)
Basic Filing:				
Petition Fee-37CFR 1.17(h) (Group II)	2464	1	70	70
Request for Continued Examination	2801	1	600	600
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Adjustment date: 09/29/2014 SDIRETA1 13559476
09/05/2014 INTEFSW 00009407 503557
02 FC:2801 600.00 CR

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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/559,476	10/28/2014	8874831	062453-010	1046

46188 7590 10/08/2014
Nixon Peabody LLP
P.O. Box 60610
Palo Alto, CA 94306

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The Patent Term Adjustment is 176 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (http://pair.uspto.gov).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site http://pair.uspto.gov for additional applicants):

Hyun Lee, Ladera Ranch, CA;
Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

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IR103 (Rev. 10/09)

Trials@uspto.gov
571-272-7822

Paper 7
Entered: July 21, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00692
Patent 8,874,831 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges.*

CLEMENTS, *Administrative Patent Judge.*

DECISION
Instituting *Inter Partes* Review
35 U.S.C. § 314 and 37 C.F.R. § 42.108

I. INTRODUCTION

SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") filed a Petition requesting *inter partes* review of claims 1–15 ("the challenged claims") of U.S. Patent No. 8,874,831 B2 (Ex. 1001, "the '831 patent"). Paper 1 ("Pet."). Netlist, Inc. ("Patent Owner") filed a Preliminary Response. Paper 6 ("Prelim. Resp."). We review the Petition pursuant to 35 U.S.C. § 314, which provides that an *inter partes* review may be authorized only if "the information presented in the petition . . . and any [preliminary] response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); 37 C.F.R. § 42.4(a).

Upon consideration of the Petition and the Preliminary Response, we determine that the information presented by Petitioner establishes that there is a reasonable likelihood that Petitioner would prevail in showing the unpatentability of at least one of the challenged claims of the '831 patent. Accordingly, pursuant to 35 U.S.C. § 314, we institute an *inter partes* review of claims 1–15 of the '831 patent.

A. Related Proceedings

The '831 patent is involved in *Netlist, Inc. v. Smart Modular Technologies, Inc. et al,* Case No. 2:13-cv-02613 (E.D. Cal.). Paper 4, 3. Related patents have been asserted in *Netlist, Inc. v. SMART Modular Technologies, Inc.*, Case No. 8-13-cv-00996 (C.D. Cal.), *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03916 (N.D. Cal.), *Diablo Technologies, Inc. v. Netlist, Inc.*, Case No. 4-13-cv-03901 (N.D. Cal.), and *Netlist, Inc. v. Smart Modular Technologies, Inc.*, 4-13-cv-05889

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(N.D. Cal.). Pet. 2. Related patents are also the subject of *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00982 (PTAB) (institution denied), *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-00994 (PTAB) (institution denied), *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01370 (PTAB) (institution denied); *Smart Modular Technologies, Inc. v. Netlist, Inc.*, Case No. IPR2014-01371 (PTAB) (institution denied), *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00587 (PTAB) (instituted June 22, 2017), and *SK hynix Inc., et al. v. Netlist, Inc.*, Case No. IPR2017-00649 (PTAB). Pet. 2; Paper 4, 3.

B. The '831 patent

The '831 patent, titled "Flash-Dram Hybrid Memory Module," issued October 28, 2014, from U.S. Patent Application No. 13/559,476. Ex. 1001 at [54], [45], [21]. The '831 patent generally relates to a memory module with a non-volatile memory, a volatile memory, and a data manager through which the volatile memory and non-volatile memory may exchange data, and a controller to receive read/write commands from a memory controller hub ("MCH") and transfer data between any two or more of the MCH, volatile memory, and non-volatile memory. *Id.* at Abstract. Figure 4A is reproduced below.

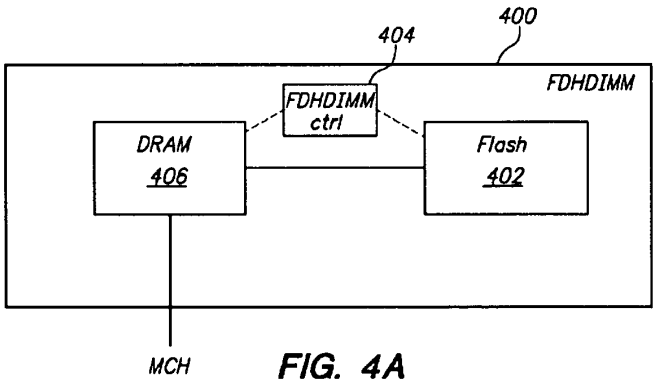

FIG. 4A

Figure 4A is a block diagram of a Flash-DRAM hybrid dynamic random access memory dual in-line memory module (DIMM). In this embodiment, volatile memory subsystem 406 (e.g. DRAM) is used as a data buffer such that data from Flash memory 402 is transferred to DRAM 406 at the Flash access speed, and buffered or collected into DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. *Id.* at 9:15–21. Similarly, when the MCH transfers data to DRAM 406, controller 404 manages the data transfer from DRAM 406 to Flash 402. *Id.* at 9:21–23.

Figure 5 is reproduced below.

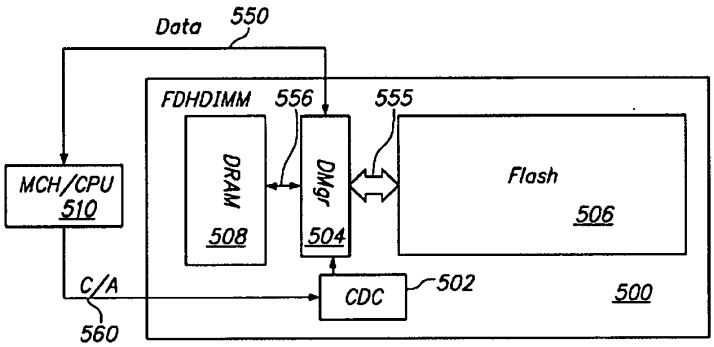

FIG. 5A

Figure 5A is a block diagram of memory module 500 in accordance with certain embodiments. Ex. 1001, 7:7–8. As shown in Figure 5, memory module 500 includes two on-module intermediary components: controller (CDC) 502 and data manager (DMgr) 504. *Id.* at 10:35–46. These components "manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510." *Id.* at 10:49–53. "In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM

memory from/to MCH 510." *Id.* at 10:54–56. "In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction." *Id.* at 11:18–21.

Figure 6 is reproduced below.

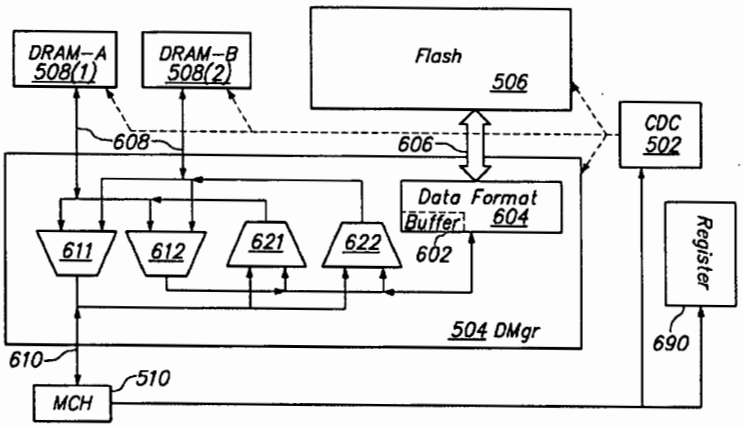

FIG. 6

Figure 6 is a block diagram showing some details of data manager 504. Ex. 1001, 7:11–12. "In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric." *Id.* at 12:1–3. "For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508." *Id.* at 12:3–5. "Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506." *Id.* at 12:5–8. "Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B)." *Id.* at 12:8–11.

C. Illustrative Claim

Of the challenged claims, claims 1 and 7 are independent, claims 2–6 depend, directly or indirectly, from claim 1, and claims 8–15 depend, directly or indirectly, from claim 7. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A memory module couplable to a memory controller of a host system, comprising:
>
> a non-volatile memory subsystem;
>
> a data manager coupled to the non-volatile memory subsystem;
>
> a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and
>
> a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein:
>
> at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and
>
> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a

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> data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Ex. 1001, 17:44–18:13.

D. Evidence Relied Upon

Petitioner relies upon the following prior art references:

Best	US 2010/0110748 A1	May 6, 2010	Ex. 1006
Roy	US 6,065,092	May 16, 2000	Ex. 1008
Tsunoda	US 2003/0028733 A1	Feb. 6, 2003	Ex. 1009
Ashmore	US 2006/0212651 A1	Sept. 21, 2006	Ex. 1011
Bonella	US 2007/0136523 A1	June 14, 2007	Ex. 1013
Roohparvar	US 2005/0273548 A1	Dec. 8, 2005	Ex. 1019

Pet. 3. Petitioner also relies upon the Declaration of Ron Maltiel ("Maltiel Decl.") (Ex. 1003).

E. Asserted Grounds of Unpatentability

Petitioner asserts that the challenged claims are unpatentable based on the following grounds (Pet. 3):

Reference(s)	**Basis**	**Claim(s) challenged**
Best	§ 102	1–14
Best and Roy	§ 103	1–14
Best and Tsunoda, with or without Roy	§ 103	2 and 8
Best and Roohparvar, with or without Roy	§ 103	5 and 12–14
Best and Bonella, with or without Roy	§ 103	15
Best, Bonella, and Ashmore, with or without Roy	§ 103	15

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Ex. 1009, p. 319

Petitioner also relies upon the Declaration of Ron Maltiel. Ex. 1003 ("Maltiel Decl.").

II. ANALYSIS

A. Claim Construction

In an *inter partes* review, a claim in an unexpired patent shall be given its broadest reasonable construction in light of the specification of the patent in which it appears. 37 C.F.R. § 42.100(b). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

Petitioner proposes constructions for "bi-directional data transfer fabric," "set of data ports," "format data," and "operable at a . . . clock frequency." Pet. 10–14. Patent Owner argues that no construction is necessary for "bi-directional data transfer fabric," "set of data ports," and "operable at a . . . clock frequency." Prelim. Resp. 21–24. Patent Owner proposes a different construction of "format data," and offers constructions

for the terms "memory module," "memory address mapping," "address domain conversion," and "data width modulation." *Id.* at 21, 23–28. On this record, and for purposes of this Decision, we determine that only the term "memory module" requires express construction.

1. "memory module" (claim 1)

Petitioner does not propose a construction for "memory module." Patent Owner contends that "memory module" should be construed to mean "a carrier that contains one or more memory chips." Prelim. Resp. 21. Specifically, Patent Owner contends that a "memory module" is a removable circuit board and does not refer to an integrated circuit by itself. *Id.* (citing Ex. 2001 (Microsoft Computer Dictionary, 5th ed.), 334 ("**memory module** *n.* A removable circuit board, cartridge, or other carrier that contains one or more RAM memory chips."); *see also* Prelim. Resp. 32–33 (arguing that Best's integrated circuit package is not a "memory module" because it is not a circuit board). Patent Owner also relies upon our construction of "memory module" in a prior proceeding involving a different patent to mean "a carrier that contains one or more memory chips." *Id.* (citing *Diablo Technologies, Inc. v. Netlist, Inc.*, Case IPR2014-00882 (PTAB Dec. 14, 2015) (Paper 33 ("882 FWD"), 8–11 (construing "memory module" as used in U.S. Patent No. 7,881,150 B2) ("the '150 patent")).

The '831 patent does not define a "memory module." The '831 patent depicts a memory module 500 in Figures 5A and 5B, and describes how "[i]n certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor" (Ex. 1001, 10:28–31), but the '831 patent also expressly contemplates other form factors (*see, e.g., id.* at 10:32–34 ("it is to be

understood that in both structure and operation [memory module 500] may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B"), 10:46–49 ("While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well.").

Moreover, our construction of "memory module" in IPR2014-00882 is informative, but not dispositive, because the '150 patent has a different Specification than the '831 patent, and our construction in that case was based, in part, on disclosures in the '150 patent that are not found in the '831 patent. *See, e.g.,* 882 FWD, 10 (citing teachings of a printed circuit board on which memory devices are mounted). The '831 patent, in contrast, does not use the terms "printed circuit board" or "circuit board" even once, much less limit explicitly a "memory module" to a removable printed circuit board, as Patent Owner suggests. Because the '831 patent is open-ended regarding the form factor that a "memory module" may take, and because it makes no mention of a printed circuit board, much less a removable printed circuit board, we also are not persuaded by Patent Owner's extrinsic evidence (Ex. 2001) such that we should import such a limitation into our construction of this term.

On this record, and for purposes of this decision, we construe "memory module" to mean "a carrier that contains one or more memory chips," where "carrier" encompasses an integrated circuit package.

B. Claims 1–14: Anticipation by Best

Petitioner argues that the claims 1–14 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Best. Pet. 11–35. In light of the

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arguments and evidence of record, we are persuaded that Petitioner has established a reasonable likelihood that the claims 1–14 are unpatentable as anticipated by Best.

1. Best (Ex. 1006)

Best is directed to a hybrid volatile and non-volatile memory device. Ex. 1006, Abstract. Specifically, Best discloses "[a]composite, hybrid memory device including a first storage die having an array of volatile storage cells and a second storage die having an array of non-volatile storage cells disposed within an integrated circuit package." *Id.* "The hybrid memory device includes a shared interface circuit to receive memory access commands directed to the first storage die and the second storage die and to convey read and write data between an external data path and the first and second storage dice." *Id.*

Figure 2 of Best is reproduced below.

FIG. 2

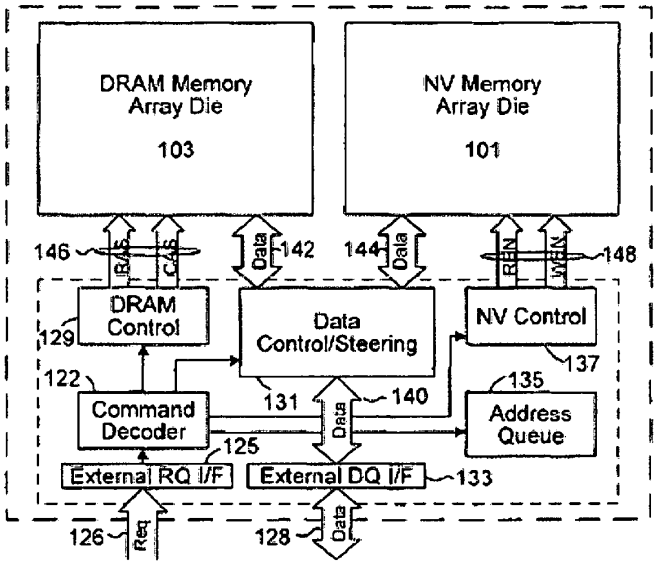

Figure 2 illustrates an embodiment of a hybrid, composite memory device with shared interface circuitry, volatile memory, and non-volatile memory. *Id.* ¶ 17. "[T]he shared interface circuitry includes an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." *Id.* "[I]ncoming control signals and addresses . . . are received in the external request interface 125 via control/address (CA) path 126, reformatted as necessary (e.g., deserialized to form a parallel command word and one or more address values) and then forwarded to the command decoder 122." *Id.* "The command decoder 122 in turn forwards address to the address queue 135 and stores memory access commands." *Id.* "[M]emory access operations may be automatically directed to either the volatile storage die or non-volatile storage die according to the memory address to be accessed." *Id.* "[C]ommand decoder 122 outputs, from the head of the command queue, an enable signal and corresponding memory access control signals to the DRAM control circuit 129 and NV control circuit 137." *Id.* ¶ 18. "[D]ata control/steering circuit 131 is used to control the transfer of data between a shared internal data bus and dedicated internal data buses associated with the volatile and non-volatile storage dice, respectively." *Id.* ¶ 20.

Figure 3 of Best is reproduced below.

FIG. 3

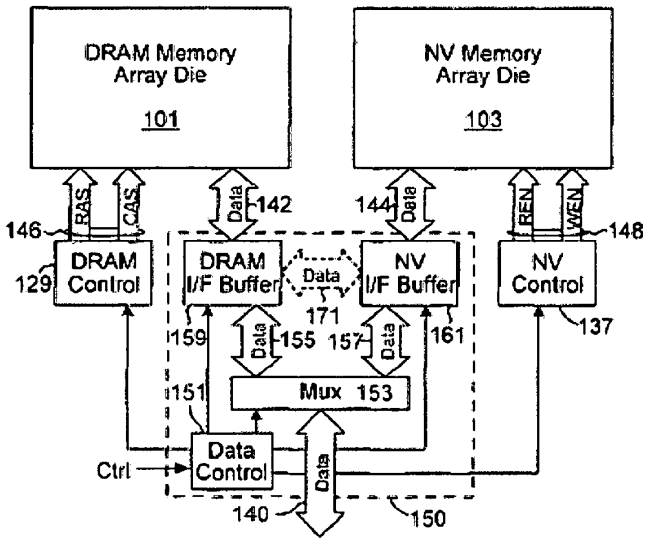

Figure 3 illustrates an embodiment of a data control/steering circuit 150 that may be used to implement the data control/steering circuit 131 of Figure 2. *Id.* ¶ 21. "[D]ata control circuit 151 receives control signals from the command decoder that indicate the direction of data flow during a memory access operation (read or write) and whether the volatile or non-volatile storage die is the target of the memory access." *Id.*

2. *Independent claims 1 and 7*

Claim 1 recites "[a] memory module couplable to a memory controller of a host system." Petitioner relies upon Best's disclosure of "a 'hybrid composite memory device having non-volatile and volatile memories implemented in distinct integrated circuit (IC) dice that are packaged together and accessed through a shared interface.'" Pet. 20 (quoting Ex. 1006 ¶ 12). Claim 1 further recites "a non-volatile memory subsystem."

Petitioner relies upon Best's disclosure of a Flash memory. Pet. 21. Claim 1 further recites "a data manager coupled to the non-volatile memory subsystem." Petitioner relies upon Best's data control/steering circuit in combination with the external interface. Pet. 21–22 (citing Ex. 1006, Figure 3). Claim 1 further recites "a volatile memory subsystem." Petitioner relies upon Best's disclosure of a DRAM. Pet. 22–23. Claim 1 further recites "a controller." Petitioner relies upon Best's command decoder 122, which receives "incoming control signals and addresses" and directs operation of the volatile and non-volatile memories by "output[ting] . . . an enable signal and corresponding memory access control signals to the DRAM control circuit . . . and NV control circuit," and transfers data between the memories and memory controller. Pet. 23–24 (citing Ex. 1006 ¶¶ 17–19, 21, 29). Claim 1 further recites "at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments." Petitioner relies upon Best's disclosure that "the volatile and non-volatile memories [are] implemented by a DRAM die 103 and Flash memory die 101, respectively," each of which, according to Petitioner, is a memory segment. Pet. 24–25. Claim 1 further recites

> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

Petitioner relies upon Best's disclosure of an interface to the primary volatile data path 142 between data control/steering circuit 150 and DRAM 101 ("a first set of data ports . . . coupled to the volatile memory subsystem"), and of an

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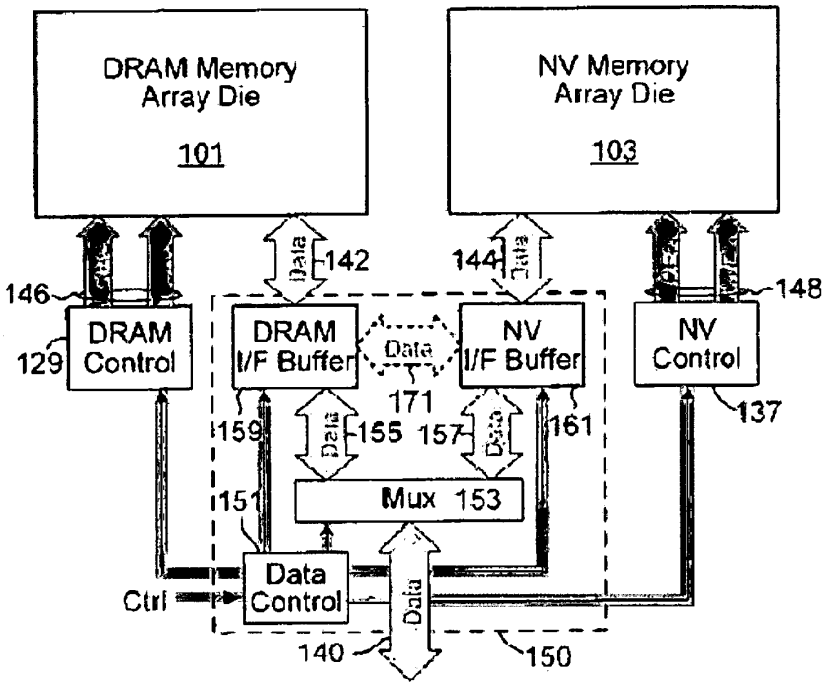
interface to primary non-volatile data path 144 between data control steering circuit 150 and NV memory 103 ("a second set of data ports . . . coupled to the non-volatile memory subsystem"). Pet. 25–26. Petitioner contends that each set of interconnections is "bi-directional" because data can flow in either direction, and illustrates the point with an annotated version of Figure 3, reproduced below:

FIG. 3



Finally, claim 1 recites

> the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Petitioner relies upon Best's disclosure of "non-volatile-storage-die interface buffer 161" as the recited "data buffer" (Pet. 27–28), and relies

upon Best's disclosure of logic for serializing/deserializing within data steering/control circuit and the external data interface as the recited "data format module" (*id.* at 28–30). We are persuaded that Petitioner's citations support its contentions.

We also are persuaded that Petitioner's citations support its contentions with respect to claim 7, for which Petitioner relies upon largely the same disclosures in Best (Pet. 38–43).

Patent Owner argues that Best does not disclose a "memory module" because it is implemented on a single integrated circuit package—i.e., a single chip. Prelim. Resp. 32–33. This argument is not persuasive, however, because it is based upon Patent Owner's proposed construction of "memory module," which we do not adopt. Because our broadest reasonable construction of "memory module," as discussed above, encompasses an integrated circuit package, we are persuaded that Best discloses this limitation.

Patent Owner also argues that "neither [Best's interface to the single volatile data path 142 nor its interface to the single nonvolatile data path 144 is] a 'set of data ports' because each interface is to a single data bus." Prelim. Resp. 33–34. This argument also is not persuasive. Patent Owner argues that no construction is necessary for the phrase "set of data ports." Prelim. Resp. 23. The claims require that the "first set of data ports" is "coupled to the volatile memory subsystem," and that the "second set of data ports" is "coupled to the non-volatile memory subsystem." The '831 patent explicitly describes non-volatile memory subsystem 506 as coupled to a single data bus, i.e., data bus 606. Ex. 1001, Fig. 6, 12:58 ("wide data bus

606 coupled to the Flash memory 506"). As a result, we are not persuaded that "set of data ports" excludes a single data bus, as disclosed by Best.

3. Dependent claims 2–6 and 8–14

We have reviewed Petitioner's explanations and supporting evidence regarding dependent claims 2–6 and 8–14, and find them persuasive. *See* Pet. 30–49. Patent Owner does not argue separately these claims. Based on the record before us, Petitioner has demonstrated a reasonable likelihood that it would prevail on its assertion that claims 2–6 and 8–14 are anticipated by Best.

4. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–14 are unpatentable as anticipated by Best.

C. Claim 1–14: Obviousness over Best[1]

As discussed above, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–14 are unpatentable as anticipated by Best. Inasmuch as "anticipation is the epitome of obviousness" (*In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002)) and because there is no evidence of objective indicia of non-obviousness on the record, we determine that Petitioner has also established a reasonable likelihood of prevailing in showing that claims 1–14 would have been obvious over Best.

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[1] Although Petitioner challenges claims 1–14 as obvious over "Best in view of Roy" (Pet. 3), its other obviousness challenges are "with or without Roy" (*id.*). We, therefore, interpret the Petition to allege that claims 1–14 also are obvious over Best alone.

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D. Claims 1–14: Obviousness over Best and Roy

Petitioner argues that claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Best and Roy. Pet. 49–53. In light of the arguments and evidence of record, we are persuaded that Petitioner has established a reasonable likelihood that the claims 1–14 are unpatentable as obvious over the combination of Best and Roy.

1. Roy (Ex. 1008)

Roy is directed generally to an "independent and cooperative multichannel memory architecture" that includes a plurality of independent channels between a master device and one or more memory clusters. Ex. 1008, Abstract. Figure 1 of Roy is reproduced below.

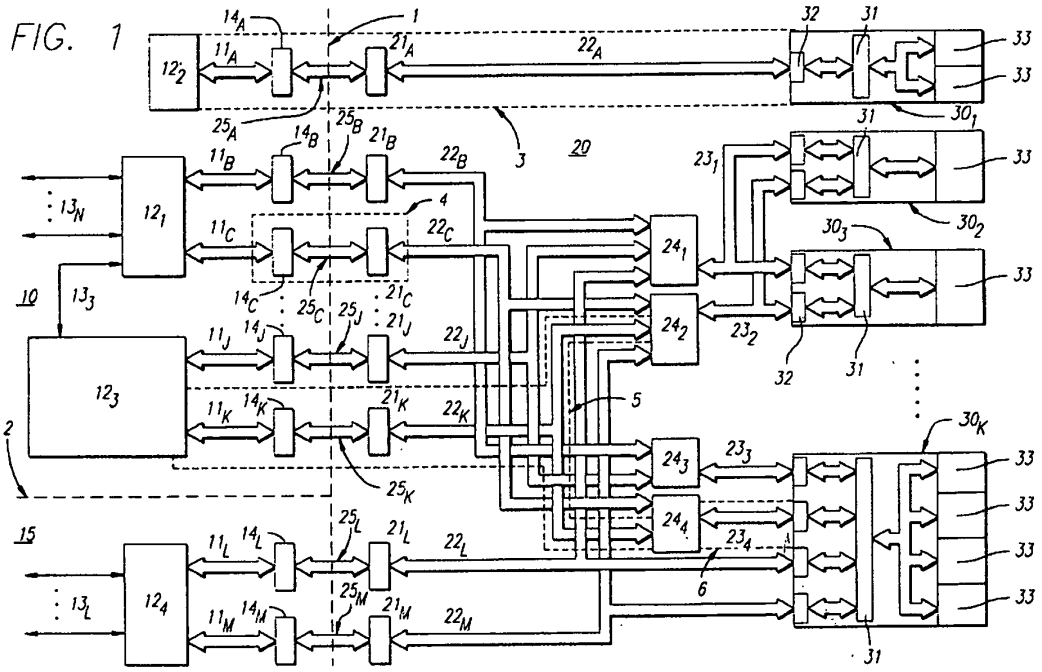
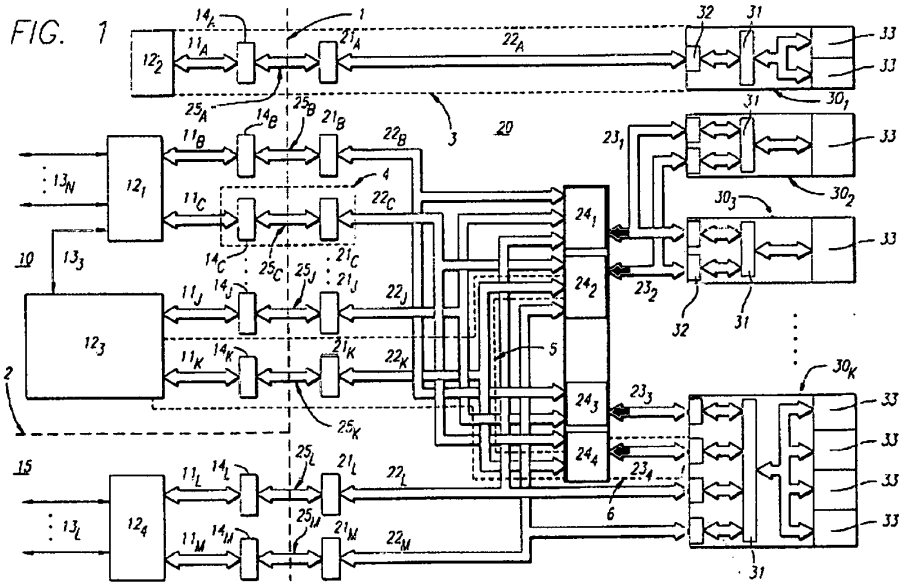


Figure 1 of Roy is a system level block diagram of a multichannel memory architecture disclosed in Roy. *Id.* at 7:59–60. As shown, "memory device 20 further includes multiplexer units 24_{1-4} which couple individual ones of a

plurality of the channels to one or more of the memory clusters 30." *Id.* at 11:52–54.

2. *Claims 1 and 7*

Independent claims 1 and 7 recite "a bi-directional data transfer fabric [having/with] two or more sets of data ports." Petitioner argues that, if this phrase is construed to require two or more independent read/write paths to each of the volatile and non-volatile memory subsystems, such a feature was taught by Roy. Pet. 49–51. In particular, Petitioner relies upon Roy's teaching of multiplexers 24_{1-4} ("a bi-directional data transfer fabric"), their interfaces to buses 23_{1-4} ("two or more sets of data ports"), some of which are coupled to memory cluster 30_3 ("a first set . . . coupled to") and others of which are coupled to memory cluster 30_K ("a second set . . . coupled to"). Pet. 50–51. Petitioner also annotates Figure 1 of Roy to indicate multiplexers (red), interfaces (green), and memory clusters to which they are coupled (yellow):



Id. at 50.

With respect to why a person of ordinary skill in the art would have modified Best in view of Roy, Petitioner argues:

> One of ordinary skill in the art would have been motivated to implement this architecture for all the reasons Roy describes, including allowing independent and simultaneous transactions, Ex. 1008, 7:37-40, and increased performance by providing a wide effective channel, *id.*, 7:45-49; Ex. 1003, ¶173. Roy also teaches that a multichannel architecture provides substantial flexibility. Ex. 1008, 9:30-42; Ex. 1003, ¶173.
>
> Roy discloses that "nearly identical address and control information" can be applied to each channel such that "[s]ubsequent transfer[s] of data on each of these channels can be synchronized to provide an effectively wider channel." Ex. 1008, 10:28-32. This provides particular motivation to combine with Best in light of Best's disclosure that "multiple non-volatile storage dice and/or multiple volatile storage dice may be ... selected ... based on incoming address and/or control signals." Ex. 1006, ¶15; Ex. 1003, ¶174.
>
> Best suggests such a modification through his disclosure of overlapping and pipelined memory operations. Ex. 1006, ¶18. One of ordinary skill would understand that multiple channels allow for further overlapping or pipelining of operations, such as allowing Best to write data from volatile to non-volatile memory as part of the "Shadow Mode" operation while allowing the host to simultaneously write data to volatile memory, thus improving the operation and responsiveness of the system. Ex. 1003, ¶175.
>
> Modifying Best to use a multichannel architecture such as Roy's would have been an arrangement of old elements (Best's hybrid memory, Roy's multichannel architecture) with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, Best's system with a multichannel architecture. Ex. 1003, ¶176. Multichannel architectures were known in the art, and using one in Best would have involved only routine skill to implement the functionality described by Roy. *Id.*

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> Such a modification would have therefore been obvious. *Id.*, ¶¶176, 240.

Pet. 56–53. On this record, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2017) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Additionally, Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." Prelim. Resp. 35. We are not persuaded by that argument for the reasons discussed above.

3. Dependent claims 2–6 and 8–14

For dependent claims 2–6 and 8–14, Petitioner relies upon its explanations and supporting evidence from Ground 1. *See* Pet. 49–53. Patent Owner does not argue separately dependent claims 2–6 and 8–14. Based on the record before us, Petitioner has demonstrated a reasonable likelihood that it would prevail on its assertion that claims 2–6 and 8–14 would have been obvious over Best and Roy.

4. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claims 1–14 are unpatentable as obvious over the combination of Best and Roy.

E. Claim 15: Obviousness over Best, Mills, and Bonella, with or without Roy

Petitioner argues that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without

Roy.[2] Pet. 57–68. In light of the arguments and evidence of record, we are persuaded that Petitioner has established a reasonable likelihood that the claim 15 is unpatentable as obvious over the combination of Best and Bonella, and over the combination of Best, Roy, and Bonella.

1. Bonella (Ex. 1013)

Bonella describes "A memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system." Ex. 1013, Abstract. Bonella teaches that, "[t]he memory module controller . . . is 'Power State Aware.'" *Id.* ¶ 45. At "Power Level 4," Bonella's controller "reduces power by limiting the DRAM performance and the PCIe transaction performance." *Id.* ¶ 48. Bonella teaches that "[r]education of power in the DRAM can be accomplished" by "reduc[ing] the frequency in which the DRAM is operating," which "reduces power and, in general, produces no noticeable decrease in system performance." *Id.* ¶ 49.

2. Claim 15

Claim 15 recites

> operating the volatile memory subsystem at a first clock frequency when the memory module is in a first mode of operation in which data is communicated between the volatile memory subsystem and the memory controller;

Ex. 1001, 20:12–15. Petitioner relies upon Best's teaching of a conventional DRAM, which one of ordinary skill in the art would have understood operates at a first clock frequency. Pet. 58–60.

---

[2] Although Petitioner does not include Mills (Ex. 1010) explicitly in its ground (Pet. 3), we include it here because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

Claim 15 further recites

> operating the non-volatile memory subsystem at a second clock frequency when the memory module is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem; and

Ex. 1001, 20:16–20. Petitioner concedes that Best does not explicitly disclose this limitation, but relies upon Mills' teaching of a synchronous flash interface to argue that it would have been obvious to include this functionality in Best. Pet. 61 (citing Ex. 1010). Specifically, Petitioner argues that Mills teaches "a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency." *Id.* at 62.

With respect to why a person of ordinary skill in the art would have combined Best and Mills, Petitioner argues

> it would have been obvious to one of ordinary skill in the art to employ a synchronous flash memory, such as disclosed in Mills, in the system of Best because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, the non-volatile storage of data. . . .
>
> A skilled artisan would have been motivated to make such a combination because, as Mills explains, a synchronous flash interface "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." Ex. 1010, 17:6-9. In the context of Best, restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory, and reduced sequential read access times during other operations or uses of Best's Flash memory, motivating one of ordinary skill in the art to use a synchronous interface generally. Ex. 1003, ¶299.

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> [O]ne of ordinary skill in the art would have therefore understood Best to suggest modification to work with any known Flash interface, including Mills' synchronous Flash interface. Ex. 1003, ¶300.

Pet. 62–64.

Patent Owner argues that Petitioner's reason to combine Mills and Best is insufficient because it "fails to show that Mills' interface provides any improvement for Best's write flushing to the alleged NVMS." This argument is not persuasive. Prelim. Resp. 36–40. Petitioner contends that there is an advantage when restoring, i.e., reading, data from the non-volatile memory, not when writing data to the non-volatile memory. Patent Owner does not explain why an advantage during reading would not be sufficient motivation. Patent Owner does not explain, for example, why a person of ordinary skill in the art would not make the proposed modification unless it also improved Best's write flushing.

Patent Owner also argues that the proposed modification adds complexity and consumes a large amount of power. *Id.* at 38–40 (citing Ex. 1010, 16:49–59). The portion of Mills on which Patent Owner relies, however, relates only to the embodiment of Figure 3. Petitioner is not relying solely upon Mills' teachings with respect to Figure 3. Petitioner is relying, for example, upon Mills' teachings with respect to Figure 6, which relies upon "a single flash memory chip" (Ex. 1010, 16:63) rather than the "at least two flash memory chips" in Figure 3. *See, e.g.,* Pet. 61 (citing 16:60–63). On this record, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *Kahn*, 441 F.3d at 988).

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Finally, claim 15 recites

> operating the volatile memory subsystem at a third clock frequency when the memory module is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 20:21–24. Petitioner concedes that Best does not explicitly disclose this limitation, but argues that "(1) reducing power during volatile to non-volatile flush operations prompted by a power loss was a well-known technique, and (2) one known way to reduce the power consumption of DRAM devices was to reduce their frequency of operation." Pet. 64–65 (citing Ex. 1011; Ex. 1013). As for why a person of ordinary skill in the art would have modified Best in view of this knowledge, Petitioner states

> One of ordinary skill in the art would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss. A skilled artisan would have been motivated to perform this power reduction technique for all the reasons that were known in the art: e.g., decreasing the risk of data loss due to insufficient backup power (Ex. 1011, ¶7) and enabling the use of a smaller-sized backup power source (Ex. 1012, 4:54-64). Reducing power consumption during write flushing in response to a power loss would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore). Ex. 1003, ¶307
>
> . . .
>
> One of ordinary skill in the art would also have found it obvious to reduce power consumption during Best's write flushing in response to a power loss using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella.

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Pet. 66–67. On this record, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *Kahn*, 441 F.3d at 988).

Patent Owner additionally argues that Petitioner fails to show evidence of the volatile memory subsystem operation at a "third clock frequency" during the "second mode." Prelim. Resp. 40–43. Patent Owner argues that "[n]one of the references, however, teaches a reduction of the frequency of operation of DRAM devices prompted by the power loss" and "no one single reference, however, teaches all three requirements." *Id.* at 41–42. This argument is not persuasive because Petitioner is relying upon the combination of the references. Nonobviousness cannot be established by attacking references individually where, as here, the ground of unpatentability is based upon the teachings of *a combination* of references. *In re Keller,* 642 F.2d 413, 426 (CCPA 1981). Rather, the test for obviousness is whether the combination of references, taken as a whole, would have suggested the patentee's invention to a person of ordinary skill in the art. *In re Merck & Co., Inc.,* 800 F.2d 1091, 1097 (Fed. Cir. 1986).

Patent Owner also argues that Bonella teaches that "a reduction in the DRAM operation frequency would result in a write flush taking longer to complete" and "the total amount of power required for the write flush would not change." Prelim. Resp. 42–43. At this stage of the proceeding, however, this attorney argument is unsupported by evidence and is, therefore, also unpersuasive.

3. Conclusion

On this record, we are persuaded that Petitioner has established a reasonable likelihood that it would prevail in showing that claim 15 is unpatentable as obvious over the combination of Best, Mills, and Bonella, with or without Roy.

F. Other Grounds

Petitioner argues that (1) claims 2 and 8 are unpatentable under 35 U.S.C. § 103 as obvious over Best and Tsunoda, with or without Roy (Pet. 53–54); (2) claims 5 and 12–14 are unpatentable under 35 U.S.C. § 103 as obvious over Best and Roohparvar, with or without Roy (*id.* at 55–57); and (3) claim 15 is unpatentable under 35 U.S.C. § 103 as obvious over Best, Bonella, and Ashmore, with or without Roy (*id.* at 68–69). The Board's rules for AIA *inter partes* proceedings, including those pertaining to institution, are "construed to secure the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1(b); *accord* 35 U.S.C. § 316(b) (regulations for AIA *inter partes* proceedings take into account "the efficient administration of the Office" and "the ability of the Office to timely complete [instituted] proceedings"). We institute an *inter partes* review of claims 1–15 based on the grounds discussed above. We exercise our discretion not to institute a review based on these other grounds. *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed . . . on all or some of the grounds of unpatentability asserted for each claim"); 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1368 (Fed. Cir. 2016) ("[U]nder [37 C.F.R. § 42.108(a)], it is clear that the Board

may choose to institute some grounds and not institute others as part of its comprehensive institution decision.").

III. CONCLUSION

For the foregoing reasons, we are persuaded that Petitioner has demonstrated that there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–15 of the '831 patent. At this stage of the proceeding, we have not made a final determination with respect to the patentability of these challenged claims or to the construction of any claim term.

IV. ORDER

Accordingly, it is

ORDERED that pursuant to 35 U.S.C. § 314, an *inter partes* review is hereby instituted on the following grounds:

1. claims 1–14 under 35 U.S.C. § 102 as anticipated by Best;
2. claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best;
3. claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best and Roy;
4. claim 15 under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without Roy;

FURTHER ORDERED that no other grounds are authorized for this *inter partes* review other than those specifically identified above; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(d), and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial commences on the entry date of this Decision.

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Samsung Electronics Co., Ltd.
Ex. 1009, p. 341

PTO/SB/80 (11-08)
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I hereby appoint:

☑ Practitioners associated with the Customer Number: 151145

OR

☐ Practitioner(s) named below (if more than ten patent practitioners are to be named, then a customer number must be used):

Name	Registration Number	Name	Registration Number

as attorney(s) or agent(s) to represent the undersigned before the United States Patent and Trademark Office (USPTO) in connection with any and all patent applications assigned only to the undersigned according to the USPTO assignment records or assignment documents attached to this form in accordance with 37 CFR 3.73(b).

Please change the correspondence address for the application identified in the attached statement under 37 CFR 3.73(b) to:

☑ The address associated with Customer Number: 151145

OR

☐ Firm or Individual Name			
Address			
City		State	Zip
Country			
Telephone		Email	

Assignee Name and Address:

Netlist, Inc.
175 Technology Drive, Suite 150
Irvine, CA 92618

A copy of this form, together with a statement under 37 CFR 3.73(b) (Form PTO/SB/96 or equivalent) is required to be filed in each application in which this form is used. The statement under 37 CFR 3.73(b) may be completed by one of the practitioners appointed in this form if the appointed practitioner is authorized to act on behalf of the assignee, and must identify the application in which this Power of Attorney is to be filed.

SIGNATURE of Assignee of Record

The individual whose signature and title is supplied below is authorized to act on behalf of the assignee

Signature	[signature]	Date	12/5/17
Name	Noel B. Whitley	Telephone	949-639-0115
Title	VP, IP & Licensing		

This collection of information is required by 37 CFR 1.31, 1.32 and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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STATEMENT UNDER 37 CFR 3.73(b)

Applicant/Patent Owner: Hyun Lee et al.

Application No./Patent No.: 13/559,476 Filed/Issue Date: 07-26-2012

Titled:
FLASH-DRAM HYBRID MEMORY MODULE

Netlist, Inc. , a Corporation
(Name of Assignee) (Type of Assignee, e.g., corporation, partnership, university, government agency, etc.

states that it is:

1. ☒ the assignee of the entire right, title, and interest in;

2. ☐ an assignee of less than the entire right, title, and interest in
(The extent (by percentage) of its ownership interest is _____ %); or

3. ☐ the assignee of an undivided interest in the entirety of (a complete assignment from one of the joint inventors was made)

the patent application/patent identified above, by virtue of either:

A. ☒ An assignment from the inventor(s) of the patent application/patent identified above. The assignment was recorded in the United States Patent and Trademark Office at Reel 029843, Frame 0824, or for which a copy therefore is attached.

OR

B. ☐ A chain of title from the inventor(s), of the patent application/patent identified above, to the current assignee as follows:

1. From: _____ To: _____
The document was recorded in the United States Patent and Trademark Office at
Reel _____, Frame _____, or for which a copy thereof is attached.

2. From: _____ To: _____
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☐ Additional documents in the chain of title are listed on a supplemental sheet(s).

☐ As required by 37 CFR 3.73(b)(1)(i), the documentary evidence of the chain of title from the original owner to the assignee was, or concurrently is being, submitted for recordation pursuant to 37 CFR 3.11.

[NOTE: A separate copy (*i.e.*, a true copy of the original assignment document(s)) must be submitted to Assignment Division in accordance with 37 CFR Part 3, to record the assignment in the records of the USPTO. See MPEP 302.08]

The undersigned (whose title is supplied below) is authorized to act on behalf of the assignee.

/Khaled Shami/ December 8, 2017
Signature Date

Khaled Shami, Reg. No. 38,745 Attorney for Assignee
Printed or Typed Name Title

This collection of information is required by 37 CFR 3.73(b). The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Acknowledgement Receipt

EFS ID:	31175292
Application Number:	13559476
International Application Number:	
Confirmation Number:	1046
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Hyun Lee
Customer Number:	46188
Filer:	Khaled Shami/Casey Berger
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	062453-010
Receipt Date:	08-DEC-2017
Filing Date:	26-JUL-2012
Time Stamp:	15:55:21
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		00160010004_POA373.pdf	942088 b32c7c289974d43a421126e88f69d7eb2203ef89	yes	2

	Multipart Description/PDF files in .zip description		
	Document Description	**Start**	**End**
	Power of Attorney	1	1
	Assignee showing of ownership per 37 CFR 3.73	2	2

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If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.
National Stage of an International Application under 35 U.S.C. 371
If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.
New International Application Filed with the USPTO as a Receiving Office
If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/559,476	07/26/2012	Hyun Lee	062453-010

CONFIRMATION NO. 1046

POWER OF ATTORNEY NOTICE

46188
Nixon Peabody LLP
P.O. Box 26769
San Francisco, CA 94126

OC000000096083146

Date Mailed: 12/14/2017

NOTICE REGARDING CHANGE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/08/2017.

- The Power of Attorney to you in this application has been revoked by the assignee who has intervened as provided by 37 CFR 3.71. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sleutchit/

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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
13/559,476	07/26/2012	Hyun Lee	062453-010

CONFIRMATION NO. 1046

POA ACCEPTANCE LETTER

151145
Shami Messinger PLLC
1000 Potomac Street NW
Fifth Floor
Washington, DC 20007

OC000000096083404

Date Mailed: 12/14/2017

NOTICE OF ACCEPTANCE OF POWER OF ATTORNEY

This is in response to the Power of Attorney filed 12/08/2017.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Questions about the contents of this notice and the requirements it sets forth should be directed to the Office of Data Management, Application Assistance Unit, at **(571) 272-4000** or **(571) 272-4200** or **1-888-786-0101**.

/sleutchit/

Trials@uspto.gov
571-272-7822

Paper 25
Entered: July 5, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2017-00692
Patent 8,874,831 B2

Before STEPHEN C. SIU, MATTHEW R. CLEMENTS, and
SHEILA F. McSHANE, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, SK hynix Inc., SK hynix America Inc. and SK hynix memory solutions Inc. ("Petitioner") challenges claims 1–15 ("the challenged claims") of U.S. Patent No. 8,874,831 B2 (Ex. 1001, "the '831 patent"), owned by Netlist, Inc. ("Patent Owner"). We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable. Petitioner's Motion to Exclude is *dismissed.*

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–15 of the '831 patent. Paper 1 ("Pet."). Patent Owner filed a Preliminary Response. Paper 6. On July 21, 2017, we instituted *inter partes* review of (1) claims 1–14 of the '831 patent as unpatentable under 35 U.S.C. § 102[1] as anticipated by Best;[2] (2) claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best; (3) claims 1–14 under 35 U.S.C. § 103(a) as obvious over Best and Roy;[3] and (4) claim 15 over Bowie under 35 U.S.C. § 103(a) as obvious

---

[1] The Leahy-Smith America Invents Act, Pub. L. No. 112–29, 125 Stat. 284 (2011) ("AIA"), amended 35 U.S.C. §§ 102 and 103. Because the '831 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

[2] U.S. Patent Publication No. 2010/0110748 A1 (Ex. 1006, "Best").

[3] U.S. Patent No. 6,065,092 (Ex. 1008, "Roy").

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over Best, Mills,[4,5] and Bonella,[6] with or without Roy. Paper 7 ("Inst. Dec."), 28.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 12, "PO Resp."), to which Petitioner filed a Reply (Paper 15, "Reply"). Petitioner filed a Motion to Exclude (Paper 17). Patent Owner filed an Opposition (Paper 20) to which Petitioner filed a Reply (Paper 22).

On April 24, 2018, we held a hearing and a transcript of the hearing is included in the record. Paper 24 ("Tr.").

On May 3, 2018, following the Supreme Court's decision in *SAS Inst., Inv. v. Iancu*, 138 S. Ct. 1348 (2018), we issued an Order (Paper 23) modifying our Institution Decision to include review of all challenged claims and all grounds presented in the Petition, including these grounds on which we had previously not instituted (Pet. 3, 28):

References	**Basis**	**Claim(s) challenged**
Best and Tsunoda, with or without Roy	§ 103	2 and 8
Best and Roohparvar,[7] with or without Roy	§ 103	5 and 12–14
Best, Mills,[8] Bonella, and Ashmore, with or without Roy	§ 103	15

[4] U.S. Patent No. 6,026,465 (Ex. 1010, "Mills").

[5] Although Petitioner does not include Mills (Ex. 1010) explicitly in its ground (Pet. 3), we include it because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

[6] U.S. Patent Publication No. 2007/0136523 A1 (Ex. 1013, "Bonella").

[7] U.S. Patent Publication No. 2005/0273548 A1 (Ex. 1019, "Roohparvar").

[8] Although Petitioner does not include Mills (Ex. 1010) explicitly in its

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In our order, we also stated that, "If, after conferring, the parties wish to submit further briefing, the parties must, within one week of the date of this Order, request a conference call with the panel to seek authorization for such briefing." Paper 23, 2. Neither party requested a conference call with the panel.

B. Related Proceedings

The parties indicate that the '831 patent is the subject of several district court cases and related *inter partes* reviews. Pet. 2; Paper 4, 3.

C. The '831 patent (Ex. 1001)

The '831 patent, titled "Flash-Dram Hybrid Memory Module," issued October 28, 2014, from U.S. Patent Application No. 13/559,476. Ex. 1001 at [54], [45], [21]. The '831 patent generally relates to a memory module with a non-volatile memory, a volatile memory, and a data manager through which the volatile memory and non-volatile memory may exchange data, and a controller to receive read/write commands from a memory controller hub ("MCH") and transfer data between any two or more of the MCH, volatile memory, and non-volatile memory. *Id.* at Abstract.

---

ground (Pet. 3), we include it because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

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Figure 4A is reproduced below.

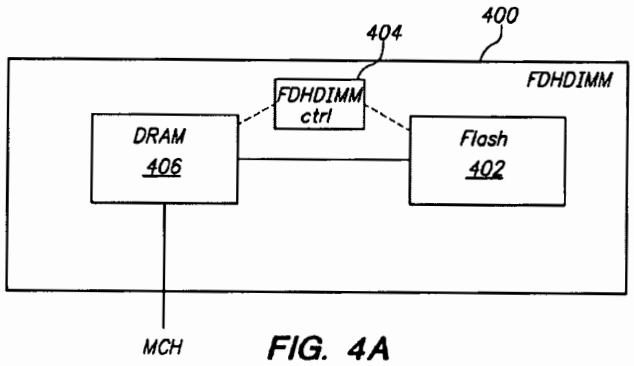

FIG. 4A

Figure 4A is a block diagram of a Flash-DRAM hybrid dynamic random access memory dual in-line memory module (DIMM). In this embodiment, volatile memory subsystem 406 (e.g. DRAM) is used as a data buffer such that data from Flash memory 402 is transferred to DRAM 406 at the Flash access speed, and buffered or collected into DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. *Id.* at 9:15–21. Similarly, when the MCH transfers data to DRAM 406, controller 404 manages the data transfer from DRAM 406 to Flash 402. *Id.* at 9:21–23.

Figure 5A is reproduced below.

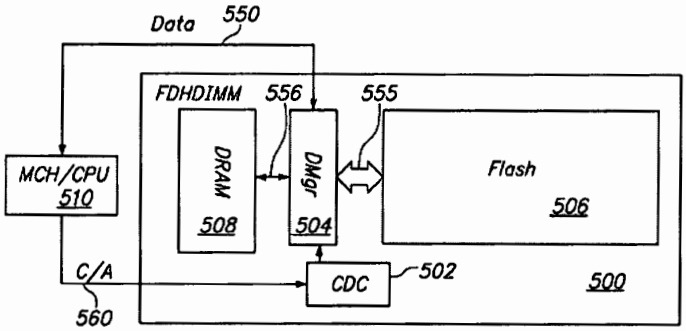

FIG. 5A

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Figure 5A is a block diagram of memory module 500 in accordance with certain embodiments. Ex. 1001, 7:7–8. As shown in Figure 5, memory module 500 includes two on-module intermediary components: controller (CDC) 502 and data manager (DMgr) 504. *Id.* at 10:35–46. These components "manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510." *Id.* at 10:49–53. "In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510." *Id.* at 10:54–56. "In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction." *Id.* at 11:18–21.

Figure 6 is reproduced below.

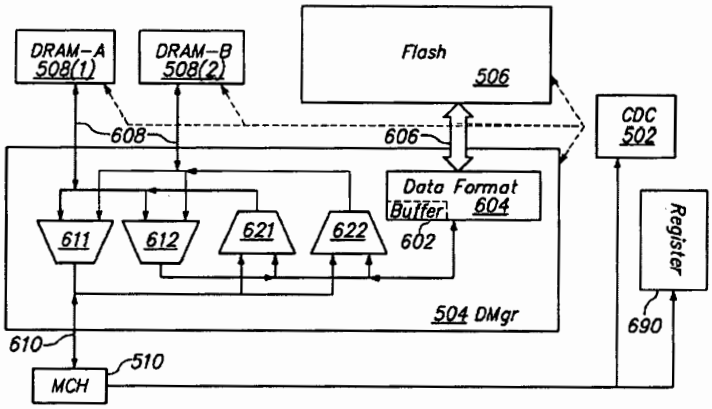

FIG. 6

Figure 6 is a block diagram showing some details of data manager 504. Ex. 1001, 7:11–12. "In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric." *Id.* at 12:1–3. "For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM

508." *Id.* at 12:3–5. "Multiplexers 611 and 612 provide controllable data paths from any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506." *Id.* at 12:5–8. "Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B)." *Id.* at 12:8–11.

D. Illustrative Claim

Of the challenged claims, claims 1 and 7 are independent, claims 2–6 depend, directly or indirectly, from claim 1, and claims 8–15 depend, directly or indirectly, from claim 7. Independent claim 1 is illustrative of the challenged claims and is reproduced below:

> 1. A memory module couplable to a memory controller of a host system, comprising:
>
> a non-volatile memory subsystem;
>
> a data manager coupled to the non-volatile memory subsystem;
>
> a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and
>
> a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein:
>
> at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and

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> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Ex. 1001, 17:44–18:13.

E. Instituted Grounds of Unpatentability

Petitioner asserted that the challenged claims are unpatentable based on the following grounds (Pet. 3), and trial has been instituted on these grounds (*see supra* Section I.A):

Reference(s)	**Basis**	**Claim(s) challenged**
Best	§ 102	1–14
Best and Roy	§ 103	1–14
Best and Tsunoda, with or without Roy	§ 103	2 and 8
Best and Roohparvar, with or without Roy	§ 103	5 and 12–14
Best, Mills,[9] and Bonella, with or without Roy	§ 103	15
Best, Mills,[10] Bonella, and Ashmore, with or without Roy	§ 103	15

[9] Petitioner does not include Mills (Ex. 1010) explicitly (Pet. 3), but the analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

[10] *See* n.9, above.

II. ANALYSIS

A. Claim Construction

We interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definition for a claim term must be set forth in the specification with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). We must be careful not to read a particular embodiment appearing in the written description into the claim if the claim language is broader than the embodiment. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993). Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

1. "memory module"

Each independent claim recites a "memory module." Petitioner did not propose a construction for "memory module" in the Petition. Patent Owner argued, in its Preliminary Response, that "memory module" should be construed to mean "a carrier that contains one or more chips." Prelim. Resp. 21. In our Decision on Institution, we construed "memory module" to mean "a carrier that contains one or more memory chips," where "carrier"

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encompasses an integrated circuit package. Inst. Dec. 9–10. We observed that

> The '831 patent does not define a "memory module." The '831 patent depicts a memory module 500 in Figures 5A and 5B, and describes how "[i]n certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor" (Ex. 1001, 10:28–31), but the '831 patent also expressly contemplates other form factors (*see, e.g., id.* at 10:32–34 ("it is to be understood that in both structure and operation [memory module 500] may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B"), 10:46–49 ("While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well.").

Id.

In its Patent Owner Response, Patent Owner argues that "memory module" should be construed to mean "one or more memory segments on a printed circuit board" ("PCB"). PO Resp. 14–34. According to Patent Owner, "[e]very embodiment of a 'memory module' disclosed by the '831 patent comprises a PCB" and its proposed construction "parallels how the term 'memory module' is used by those in the industry and standards bodies." *Id.* at 15. Specifically, Patent Owner annotates Figure 5A, arguing that it shows "a PCB (yellow)":

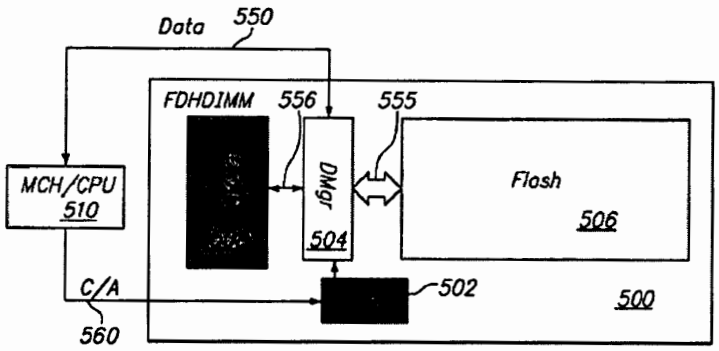

FIG. 5A

PO Resp. 16; *see also id.* at 20–23 ("Because the '831 specification only discloses embodiments including memory segments on a PCB, the claimed 'memory module' should be construed to cover such embodiments."). These arguments are not persuasive because the '831 patent does *not* describe 500, or any other embodiment, as a PCB. Instead, the '831 patent refers to 500 only as a "module." Ex. 1001, 10:14–15.

Patent Owner also argues that the '831 patent "repeatedly and consistently describes 'memory modules' as having a Dual In-Line Memory Module ('DIMM') form factor." PO Resp. 17. As Petitioner points out, however, claims are not limited to the embodiments described in the Specification. Pet. Reply 3–4 (citing *ACUMED LLC v. Stryker Corp.*, 483 F.3d 800, 805 (Fed. Cir. 2007)). Moreover, as we noted above, the '831 patent expressly contemplates other form factors for its "module" and, therefore, does not limit "module" to a DIMM form factor. *See, e.g.*, Ex. 1001, 10:32–49. The '831 patent states, for example

> These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for

> integration known to those skilled in the art to achieve a specific design, application, or economic goal.

Id. at 10:36–43.

For the same reasons, we are unpersuaded by Patent Owner's argument that boilerplate language cannot be used to broaden claims beyond what is disclosed in the Specification. PO Resp. 23–26.[11] The '831 patent's disclosure that "[w]hile the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well" (Ex. 1001, 10:46–49), is not mere boilerplate.

Patent Owner also relies upon disclosure in U.S. Patent Application No. 12/240,916 ("the '916 application"), of which the '831 patent is a continuation-in-part. PO Resp. 17–19; Ex. 1001 [63]. The '916 patent explicitly describes an embodiment in which memory system 10 comprises PCB 20. Ex. 2018 ¶ 31. This argument is not persuasive, however, because when the application leading to the '831 patent was filed, all references to "printed circuit board," "PCB," or even "board," were deleted from the Specification and the more generic word "module" was used instead. That the applicant for the '831 patent *removed* the words "PCB" and "printed circuit board" from the '916 application and used only the word "module" instead suggests, if anything, that applicant intended "module" *not* to be limited to a PCB.

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[11] Patent Owner's citation to the "ID at 5–6" and the quote in parenthetical (Pet. 23–24) appears to be a citation to our Institution Decision in IPR2017-00560, not to our Institution Decision in this proceeding. Pet. Reply 10–11.

Patent Owner also relies upon a Final Written Decision in *Diablo Techs., Inc. v. Netlist, Inc.*, Case No. IPR2014-00882, concerning U.S. Patent 7,881,150 ("the '150 patent"). PO Resp. 26–27; Ex. 2021. Patent Owner's reliance on this decision is not persuasive, however, because the '150 patent is not related to the '831 patent and the Specification for the '150 patent is different from the Specification of the '831 patent. For example, the '150 patent explicitly discloses a printed circuit board, whereas the '831 patent does not.

Patent Owner also relies upon extrinsic evidence as support for its proposed construction. PO Resp. 27–31. There is no doubt that the DIMM form factor, including a PCB, was well-known. The issue, however, is whether the applicant for the '831 patent intended the term "memory module" to require a PCB. In light of the intrinsic evidence that the applicant deleted the words "printed circuit board" and "PCB" from the Specification, explicitly contemplated non-DIMM form factors, and even contemplated a controller and data manager "integrated with other memory devices" (Ex. 1001, 10:39–40), Patent Owner's extrinsic evidence does not persuade us that applicant intended "memory module" to require a PCB.

Patent Owner also argues that our preliminary determination that "carrier" encompasses an integrated circuit package is overly broad because (a) the '831 patent "does not describe any IC package comprising a PCB" and (b) it lacks any support from the industry or standards bodies. PO Resp. 33–34. We disagree. As discussed, the '831 patent explicitly contemplates integrating the controller and data manager "with other memory devices, for example in a three dimensional stack, or in any one of several other possible

expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal." Ex. 1001, 10:36–43.

Finally, Patent Owner argues, with respect to Best, that our construction "requires two layers of IC packages, in which a first IC package (the Board's 'carrier') contains one or more second IC packages (the Board's memory chips)." PO Resp. 39. Petitioner counters that "[t]he Board's construction does no such thing." Pet. Reply 18–19. We agree with Petitioner. Patent Owner's argument is predicated upon the erroneous assertion that "[e]ach memory chip in the Board's 'carrier' requires a different IC package (*i.e.*, a second IC package) that encloses at least one memory die." PO Resp. 39. Each memory chip does *not* require its own integrated circuit package. On the contrary, it may be, as Best discloses, a die enclosed with another die in a single IC package.

Having considered the arguments and evidence, we maintain our construction of "memory module" to mean "a carrier that contains one or more memory chips," where "carrier" encompasses an integrated circuit package.

B. Level of Ordinary Skill in the Art

Petitioner contends that a hypothetical person of ordinary skill in the art, with respect to and at the time of the'831 patent, "would be a person with a Bachelor's degree in materials science, electrical engineering, computer engineering, computer science, or in a related field and at least one year of experience with the design or development of semiconductor non-volatile memory circuitry or systems." Pet. 7; Ex. 1003 ¶¶ 55–56.

Patent Owner contends that such a person "would have been a person with a Bachelor's degree in electrical and/or computer engineering and at

least five years of industry experience designing memory devices and controllers" but that "[a] Master of Science degree in electrical and/or computer engineering would substitute for two years of industry experience" and "[a] Doctorate degree in electrical and/or computer engineering would substitute for four years of industry experience." PO Resp. 43; Ex. 2016 ¶ 32.

Patent Owner argues that a degree in material science would *not* be equivalent to a degree in electrical and/or computer engineering, and that Petitioner's expert, Mr. Maltiel, who has only a degree in materials science, is not competent to testify to the understanding of a person of ordinary skill in the art. PO Resp. 43–44. Patent Owner did not, however, move to exclude the testimony of Mr. Maltiel. To the extent Patent Owner is arguing that we should accord Mr. Maltiel's testimony little to no weight based on his qualifications, we decline to do so. After earning three degrees, Mr. Maltiel joined Intel in 1980 to work on the first commercial non-volatile EEPROM devices and, therefore, had 27 years of industry experience as of the earliest priority date to which the '831 patent could be entitled. Ex. 1003 ¶¶ 3–9. Mr. Maltiel was recognized as a Senior Member of the IEEE in 2008 and is a named inventor on six United States patents covering various aspects of memory devices, including for combining non-volatile and DRAM memories. *Id.* ¶¶ 10–12. As a result, we are persuaded that Mr. Maltiel is qualified to testify as to the understanding of a person of ordinary skill in the art at the time of the '831 patent.

Otherwise, we determine that no express finding on a specific corresponding level of technical education and experience is necessary. Here, the level of ordinary skill in the art is reflected by the prior art of

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record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Whether to Give Weight to Mr. Maltiel's Testimony

Patent Owner argues that Mr. Maltiel's testimony should be given no weight because it is neither reliable nor credible. PO Resp. 41–42; *see also id.* at 62–64. In support of the argument, Patent Owner directs attention to portions of Dr. Maltiel's cross examination testimony where he allegedly (1) "contradicted himself on critical matters;" (2) "made a number of statements that are simply incorrect;" and (3) "concede[d] that he did not consider the complete intrinsic record, including the '916 patent application." *Id.*

Petitioner counters that Mr. Maltiel is qualified, reliable, and credible. Pet. Reply 24–25.

We have reviewed the arguments provided by Patent Owner and determine such arguments are insufficient to have Mr. Maltiel's declaration excluded in its entirety. Rather, it is within our discretion to assign the appropriate weight to be accorded evidence. *See* 37 C.F.R. § 42.65(a); *see also, e.g.*, *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); and *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its]

discretion."). Based on the record before us, we are not persuaded that we should give the entirety of Mr. Maltiel's declaration no weight.

D. The Parties' Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that (1) claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best; (2) claims 1–14 under 35 U.S.C. § 103(a) are obvious over Best; (3) claims 1–14 under 35 U.S.C. § 103(a) are obvious over Best and Roy; and (4) claim 15 over Bowie under 35 U.S.C. § 103(a) is obvious over Best, Mills, and Bonella, with or without Roy. Inst. Dec. 28. We subsequently instituted on the remaining grounds asserted by Petitioner. Paper 23. We must now determine whether Petitioner has established by a preponderance of the evidence that claims 1–15 are unpatentable over the cited prior art. 35 U.S.C. § 316(e). We previously instructed Patent Owner that "any arguments for patentability not raised in the [Patent Owner Response] will be deemed waived." Paper 3, 3; *see also* 37 C.F.R. § 42.23(a) ("Any material fact not specifically denied may be considered admitted."); *In re Nuvasive, Inc.*, 842 F.3d 1376, 1379–1382 (Fed. Cir. 2016) (holding Patent Owner waived an argument addressed in Preliminary Response by not raising the same argument in the Patent Owner Response). Additionally, the Board's Trial Practice Guide states that the Patent Owner Response "should identify all the involved claims that are believed to be patentable and state the basis for that belief." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,766 (Aug. 14, 2012).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability

contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations that Patent Owner contests in the Patent Owner Response are addressed below.

E. Claims 1–14: Anticipation by Best

Petitioner argues that claims 1–14 are unpatentable under 35 U.S.C. § 102(e) as anticipated by Best. Pet. 20–49.

1. Principles of Law

To establish anticipation, "all of the elements and limitations of the claim must be shown in a single prior reference, arranged as in the claim." *Karsten Mfg. Corp. v. Cleveland Golf Co.*, 242 F.3d 1376, 1383 (Fed. Cir. 2001). When evaluating a single prior art reference in the context of anticipation, the reference must be "considered together with the knowledge of one of ordinary skill in the pertinent art." *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994) (citing *In re Samour*, 571 F.2d 559, 562 (CCPA 1978)). "'[T]he dispositive question regarding anticipation[, therefore, i]s whether *one skilled in the art* would reasonably understand or infer from the [prior art reference's] teaching' that every claim element was disclosed in that single reference." *Dayco Prods., Inc. v. Total Containment, Inc.*, 329 F.3d 1358, 1368 (Fed. Cir. 2003) (alterations in original) (quoting *In re Baxter Travenol Labs.*, 952 F.2d 388, 390 (Fed. Cir. 1991)). We analyze

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this asserted ground based on anticipation with the principles stated above in mind.

2. Best Overview

Best is directed to a hybrid volatile and non-volatile memory device. Ex. 1006, Abstract. Specifically, Best discloses "[a]composite, hybrid memory device including a first storage die having an array of volatile storage cells and a second storage die having an array of non-volatile storage cells disposed within an integrated circuit package." *Id.* "The hybrid memory device includes a shared interface circuit to receive memory access commands directed to the first storage die and the second storage die and to convey read and write data between an external data path and the first and second storage dice." *Id.*

Figure 2 of Best is reproduced below.

FIG. 2

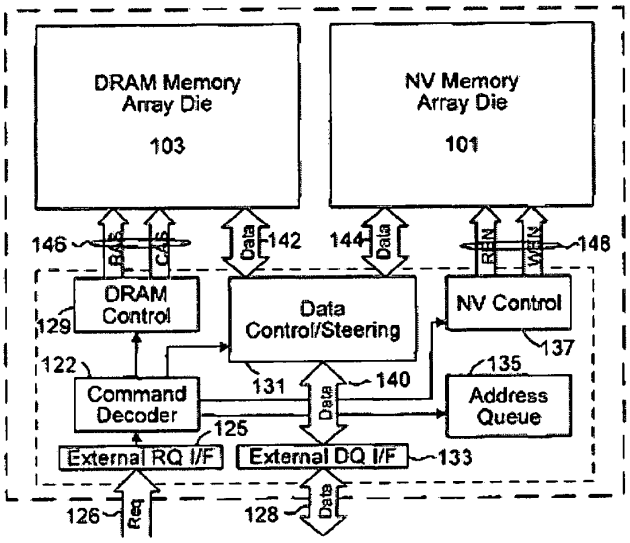

Figure 2 illustrates an embodiment of a hybrid, composite memory device with shared interface circuitry, volatile memory, and non-volatile memory.

Id. ¶ 17. "[T]he shared interface circuitry includes an external request interface 125, external data interface 133, command decoder 122, address queue 135, DRAM control circuit 129, Flash control circuit 137, and data control/steering circuit 131." *Id.* "[I]ncoming control signals and addresses . . . are received in the external request interface 125 via control/address (CA) path 126, reformatted as necessary (e.g., deserialized to form a parallel command word and one or more address values) and then forwarded to the command decoder 122." *Id.* "The command decoder 122 in turn forwards address to the address queue 135 and stores memory access commands." *Id.* "[M]emory access operations may be automatically directed to either the volatile storage die or non-volatile storage die according to the memory address to be accessed." *Id.* "[C]ommand decoder 122 outputs, from the head of the command queue, an enable signal and corresponding memory access control signals to the DRAM control circuit 129 and NV control circuit 137." *Id.* ¶ 18. "[D]ata control/steering circuit 131 is used to control the transfer of data between a shared internal data bus and dedicated internal data buses associated with the volatile and non-volatile storage dice, respectively." *Id.* ¶ 20.

Figure 3 of Best is reproduced below.

FIG. 3

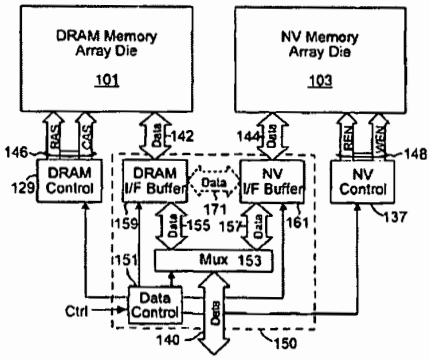

Figure 3 illustrates an embodiment of a data control/steering circuit 150 that may be used to implement the data control/steering circuit 131 of Figure 2. *Id.* ¶ 21. "[D]ata control circuit 151 receives control signals from the command decoder that indicate the direction of data flow during a memory access operation (read or write) and whether the volatile or non-volatile storage die is the target of the memory access." *Id.*

3. Petitioner's Initial Positions

Petitioner contends that Best anticipates claims 1–14 of the '831 patent. Pet. 20–49. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claims 1–14, and we adopt Petitioner's contentions discussed below as our own.

For example, Claim 1 recites "[a] memory module couplable to a memory controller of a host system." Petitioner relies upon Best's disclosure of "a 'hybrid composite memory device having non-volatile and volatile memories implemented in distinct integrated circuit (IC) dice that are packaged together and accessed through a shared interface.'" Pet. 20 (quoting Ex. 1006 ¶ 12). In light of our construction of "memory module" to mean "a carrier that contains one or more memory chips," where "carrier" encompasses an integrated circuit package, we are persuaded by Petitioner's showing and find that Best's integrated circuit package containing first and second storage die teaches the recited "memory module."

Claim 1 further recites "a non-volatile memory subsystem." Petitioner relies upon Best's disclosure of a Flash memory. Pet. 21. We are

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persuaded by Petitioner's showing and find that Best's Flash memory teaches the recited "non-volatile memory subsystem."

Claim 1 further recites "a data manager coupled to the non-volatile memory subsystem." Petitioner relies upon Best's data control/steering circuit in combination with the external interface. Pet. 21–22 (citing Ex. 1006, Figure 3). We are persuaded by Petitioner's showing and find that Best's data control/steering circuit in combination with the external interface teaches the recited "data manager."

Claim 1 further recites "a volatile memory subsystem." Petitioner relies upon Best's disclosure of a DRAM. Pet. 22–23. We are persuaded by Petitioner's showing and find that Best's DRAM teaches this limitation.

Claim 1 further recites "a controller." Petitioner relies upon Best's command decoder 122, which receives "incoming control signals and addresses" and directs operation of the volatile and non-volatile memories by "output[ting] . . . an enable signal and corresponding memory access control signals to the DRAM control circuit . . . and NV control circuit," and transfers data between the memories and memory controller. Pet. 23–24 (citing Ex. 1006 ¶¶ 17–19, 21, 29). We are persuaded by Petitioner's showing and find that Best's command decoder 122 teaches the recited "controller."

Claim 1 further recites "at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments." Petitioner relies upon Best's disclosure that "the volatile and non-volatile memories [are] implemented by a DRAM die 103 and Flash memory die 101, respectively," each of which, according to Petitioner, is a memory segment. Pet. 24–25. We are persuaded by Petitioner's showing and find that Best's

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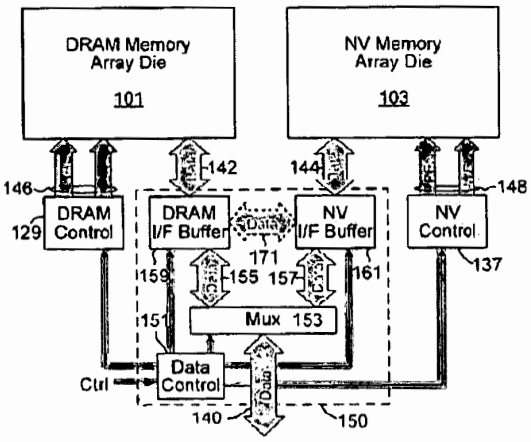
DRAM die 103 and Flash memory die 101 teach the recited "one or more memory segments."

Claim 1 further recites

> the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

Petitioner relies upon Best's disclosure of an interface to the primary volatile data path 142 between data control/steering circuit 150 and DRAM 101 ("a first set of data ports . . . coupled to the volatile memory subsystem"), and of an interface to primary non-volatile data path 144 between data control steering circuit 150 and NV memory 103 ("a second set of data ports . . . coupled to the non-volatile memory subsystem"). Pet. 25–26. Petitioner contends that each set of interconnections is "bi-directional" because data can flow in either direction, and illustrates the point with an annotated version of Figure 3, reproduced below:

FIG. 3



We are persuaded by Petitioner's showing and find that Best's interfaces to primary volatile data path 142 and to primary non-volatile data path 144, respectively, as illustrated in annotated Figure 3 above, teach the recited "two or more sets of data ports."

Finally, claim 1 recites

> the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

Petitioner relies upon Best's disclosure of "non-volatile-storage-die interface buffer 161" as the recited "data buffer" (Pet. 27–28), and relies upon Best's disclosure of logic for serializing/deserializing within data steering/control circuit and the external data interface as the recited "data format module" (*id.* at 28–30). We are persuaded by Petitioner's showing and find that Best's non-volatile-storage-die interface buffer 161 teaches the recited "data buffer."

We also are persuaded that Petitioner's citations support its contentions with respect to claim 7, for which Petitioner relies upon largely the same disclosures in Best (Pet. 38–43).

Petitioner has provided a similar detailed analysis of claims 2–6 and 8–14. Pet. 30–37, 44–49. Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claims 1–14 are unpatentable under 35 U.S.C. § 102 as anticipated by Best.

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4. Patent Owner's Assertions Concerning Best

Patent Owner argues that Best does not disclose a "memory module" because it is implemented on a single integrated circuit package—i.e., a single chip. PO Resp. 34–41. Specifically, Patent Owner argues that (1) Petitioner's expert testified that a "memory module" and an "IC package" are "totally different terms;" (2) Best's dual-die chip teaches away from a memory module; (3) Best does not teach an IC package within another IC package; and (4) Best does not teach a PCB. *Id.*

Petitioner counters that (1) Mr. Maltiel testified specifically that Best's specific disclosure of an IC package teaches a "memory module" as a person of ordinary skill in the art would have understood it; and (2) Patent Owner's alleged "teaching away" is irrelevant in an anticipation analysis. Pet. Reply 17–18. We agree.

Moreover, Patent Owner's remaining arguments are not persuasive because they are based upon Patent Owner's proposed construction of "memory module," which we do not adopt for the reasons discussed above. Because our broadest reasonable construction of "memory module" encompasses an integrated circuit package and because Best discloses an integrated circuit package with two die, we are persuaded that Best discloses this limitation.

Patent Owner does not separately argue claims 2–14.

5. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best.

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F. Claim 1–14: Obviousness over Best

Although Petitioner challenges claims 1–14 as obvious over "Best in view of Roy" (Pet. 3), its other obviousness challenges are "with or without Roy" (*id.*). We, therefore, interpret the Petition to allege that claims 1–14 also are obvious over Best alone.

As discussed above, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1–14 are unpatentable as anticipated by Best. Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

Inasmuch as "anticipation is the epitome of obviousness" (*In re McDaniel*, 293 F.3d 1379, 1385 (Fed. Cir. 2002)) and because there is no evidence of objective indicia of non-obviousness on the record, we determine that Petitioner has also established, by a preponderance of the evidence, that claims 1–14 would have been obvious over Best.

G. Claims 1–14: Obviousness over Best and Roy

Petitioner argues that claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Best and Roy. Pet. 49–53.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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KSR Int'l Co. v. Teleflex Inc., 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness (i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Roy Overview

Roy is directed generally to an "independent and cooperative multichannel memory architecture" that includes a plurality of independent channels between a master device and one or more memory clusters. Ex. 1008, Abstract. Figure 1 of Roy is reproduced below.

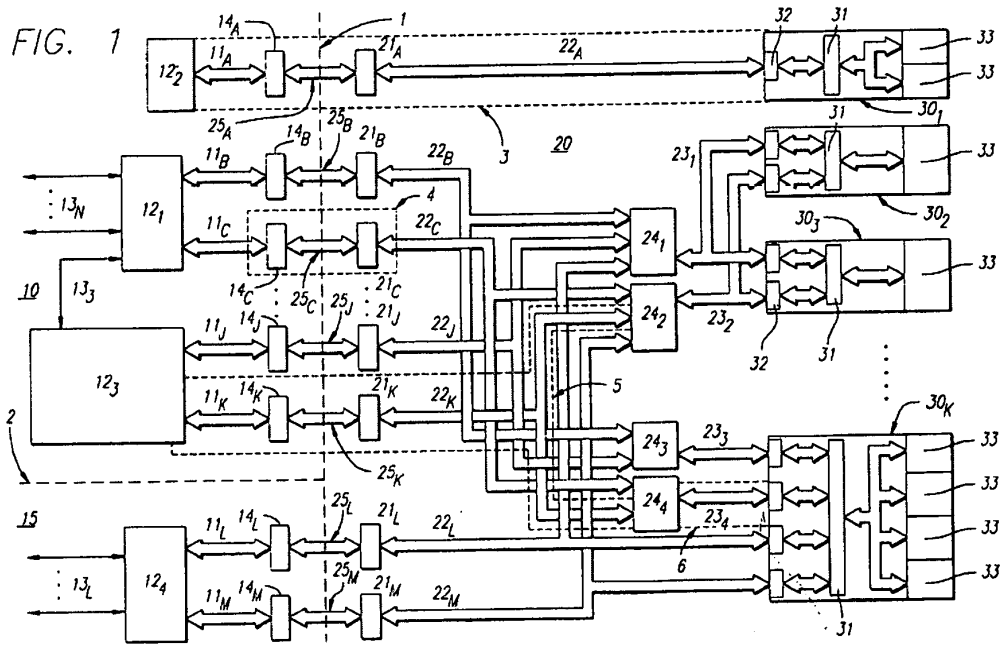

Figure 1 of Roy is a system level block diagram of a multichannel memory architecture disclosed in Roy. *Id.* at 7:59–60. As shown, "memory device 20 further includes multiplexer units 24_{1-4} which couple individual ones of a plurality of the channels to one or more of the memory clusters 30." *Id.* at 11:52–54.

3. Analysis

Petitioner contends that, to the extent the claims require "two or more" independent read or write paths to the "volatile memory subsystem" and "non-volatile memory subsystem," a combination of Best and Roy would have rendered obvious claims 1–14 of the '831 patent. Pet. 49–53. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claims 1–14, and we adopt Petitioner's contentions discussed below as our own.

For example, independent claims 1 and 7 recite "a bi-directional data transfer fabric [having/with] two or more sets of data ports." Petitioner argues that, if this phrase is construed to require two or more independent read/write paths to each of the volatile and non-volatile memory subsystems, such a feature was taught by Roy. Pet. 49–51. In particular, Petitioner relies upon Roy's teaching of multiplexers 24_{1-4} ("a bi-directional data transfer fabric"), their interfaces to buses 23_{1-4} ("two or more sets of data ports"), some of which are coupled to memory cluster 30_3 ("a first set . . . coupled to") and others of which are coupled to memory cluster 30_K ("a second set . . . coupled to"). Pet. 50–51. Petitioner also annotates Figure 1 of Roy to

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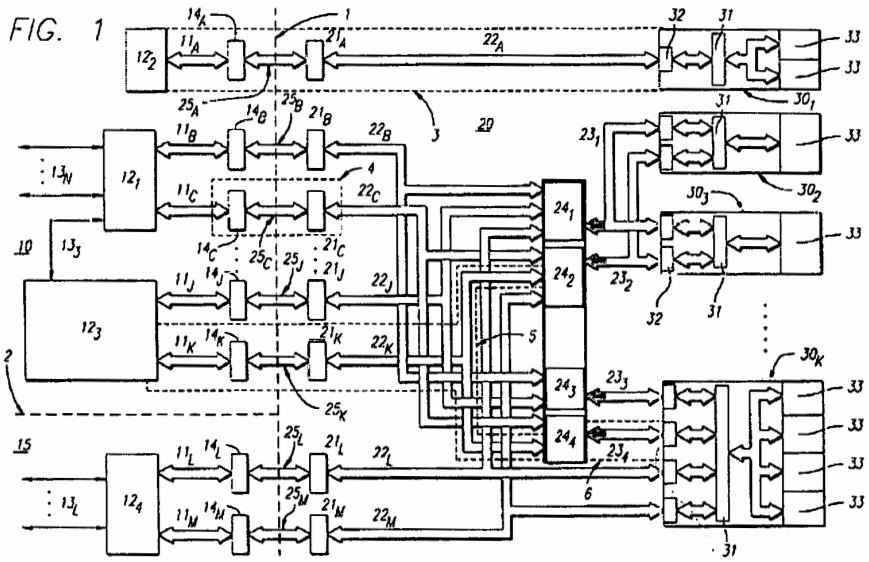
indicate multiplexers (red), interfaces (green), and memory clusters to which they are coupled (yellow):



Id. at 50. An annotated version of Figure 1 of Roy is reproduced above.

We are persuaded by Petitioner's showing and find that Roy's multiplexers 24_{1-4}, buses 23_{1-4}, memory cluster 30_3, and memory cluster 30_K teach the recited "bi-directional data transfer fabric."

With respect to why a person of ordinary skill in the art would have modified Best in view of Roy, Petitioner argues:

> One of ordinary skill in the art would have been motivated to implement this architecture for all the reasons Roy describes, including allowing independent and simultaneous transactions, Ex. 1008, 7:37-40, and increased performance by providing a wide effective channel, *id.*, 7:45-49; Ex. 1003, ¶173. Roy also teaches that a multichannel architecture provides substantial flexibility. Ex. 1008, 9:30-42; Ex. 1003, ¶173.
>
> Roy discloses that "nearly identical address and control information" can be applied to each channel such that "[s]ubsequent transfer[s] of data on each of these channels can be synchronized to provide an effectively wider channel." Ex.

> 1008, 10:28-32. This provides particular motivation to combine with Best in light of Best's disclosure that "multiple non-volatile storage dice and/or multiple volatile storage dice may be ... selected ... based on incoming address and/or control signals." Ex. 1006, ¶15; Ex. 1003, ¶174.
>
> Best suggests such a modification through his disclosure of overlapping and pipelined memory operations. Ex. 1006, ¶18. One of ordinary skill would understand that multiple channels allow for further overlapping or pipelining of operations, such as allowing Best to write data from volatile to non-volatile memory as part of the "Shadow Mode" operation while allowing the host to simultaneously write data to volatile memory, thus improving the operation and responsiveness of the system. Ex. 1003, ¶175.
>
> Modifying Best to use a multichannel architecture such as Roy's would have been an arrangement of old elements (Best's hybrid memory, Roy's multichannel architecture) with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, Best's system with a multichannel architecture. Ex. 1003, ¶176. Multichannel architectures were known in the art, and using one in Best would have involved only routine skill to implement the functionality described by Roy. *Id.* Such a modification would have therefore been obvious. *Id.*, ¶¶176, 240.

Pet. 56–53. We determine that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2017) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

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Having considered the arguments and evidence, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy.

4. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy.

H. Claim 15: Obviousness over Best, Mills, and Bonella, with or without Roy

Petitioner argues that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without Roy.[12] Pet. 57–69.

1. Bonella Overview

Bonella describes "A memory module including a volatile memory, a non-volatile memory, and a controller that provides address, data, and control interfaces to the memories and to a host system." Ex. 1013, Abstract. Bonella teaches that, "[t]he memory module controller . . . is 'Power State Aware.'" *Id.* ¶ 45. At "Power Level 4," Bonella's controller "reduces power by limiting the DRAM performance and the PCIe transaction performance." *Id.* ¶ 48. Bonella teaches that "[r]eduction of power in the DRAM can be accomplished" by "reduc[ing] the frequency in

[12] Although Petitioner does not include Mills (Ex. 1010) explicitly in its ground (Pet. 3), we include it here because Petitioner's analysis relies upon it (*id.* at 61–64) for teaching part of a limitation.

which the DRAM is operating," which "reduces power and, in general, produces no noticeable decrease in system performance." *Id.* ¶ 49.

2. Petitioner's Initial Contentions

Petitioner contends that claim 15 of the '831 patent is unpatentable as obvious over the combination of Best, Mills, and Bonella, and over the combination of Best, Mills, Roy, and Bonella. Pet. 57–68. We have reviewed the Petition, Patent Owner's Response, and Petitioner's Reply, as well as the relevant evidence discussed in those papers and other record papers, and are persuaded that the record establishes Petitioner's contentions for claim 15, and we adopt Petitioner's contentions discussed below as our own.

i. "first clock frequency"

For example, claim 15 recites

> operating the volatile memory subsystem at a first clock frequency when the memory module is in a first mode of operation in which data is communicated between the volatile memory subsystem and the memory controller;

Ex. 1001, 20:12–15. Petitioner relies upon Best's teaching of a conventional DRAM, which one of ordinary skill in the art would have understood operates at a first clock frequency. Pet. 58–60. We are persuaded by Petitioner's showing and find that a person of ordinary skill in the art would have understood that Best's DRAM operates at a first clock frequency.

ii. "second clock frequency"

Claim 15 further recites

> operating the non-volatile memory subsystem at a second clock frequency when the memory module is in a second mode of operation in which data is communicated between the volatile memory subsystem and the non-volatile memory subsystem;

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Ex. 1001, 20:16–20. Petitioner concedes that Best does not explicitly disclose this limitation, but relies upon Mills' teaching of a synchronous flash interface to argue that it would have been obvious to include this functionality in Best. Pet. 61 (citing Ex. 1010). Specifically, Petitioner argues that Mills teaches "a synchronous Flash interface where read and write operations are synchronized to the rising edge of a clock signal provided to the device and operating at a particular frequency." *Id.* at 62. Petitioner also argues that "[a]s combined, Best's Flash interface would conform to Mills' synchronous Flash protocol and include a separate clock signal that controls read and write operations." *Id.* at 63. We are persuaded by Petitioner's showing and find that Mills teaches a synchronous Flash interface operating on a separate clock.

With respect to why a person of ordinary skill in the art would have combined Best and Mills, Petitioner argues

> it would have been obvious to one of ordinary skill in the art to employ a synchronous flash memory, such as disclosed in Mills, in the system of Best because to do so would have been merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement, *i.e.*, the non-volatile storage of data. . . .
>
> A skilled artisan would have been motivated to make such a combination because, as Mills explains, a synchronous flash interface "creates an average access time for sequential read accesses that is significantly less than the access time of an asynchronous flash device." Ex. 1010, 17:6-9. In the context of Best, restoring data from the non-volatile flash memory would therefore have been faster by use of a synchronous flash memory, and reduced sequential read access times during other operations or uses of Best's Flash memory, motivating one of ordinary skill

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> in the art to use a synchronous interface generally. Ex. 1003, ¶ 299.
>
> [O]ne of ordinary skill in the art would have therefore understood Best to suggest modification to work with any known Flash interface, including Mills' synchronous Flash interface. Ex. 1003, ¶300.

Pet. 62–64. We determine that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2017) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

iii. "third clock frequency"

Finally, claim 15 recites

> operating the volatile memory subsystem at a third clock frequency when the memory module is in the second mode of operation, the third clock frequency being less than the first clock frequency.

Ex. 1001, 20:21–24. Petitioner concedes that Best does not explicitly disclose this limitation, but argues that Bonella teaches reducing DRAM operational frequency to reduce power. Pet. 66–67 (citing Ex. 1013 ¶ 50). The cited portion of Bonella teaches

> An improved power saving option is to slow the operating frequency of the device down and restrict the number of requests being serviced by the ExpressCard interface. By doing this a significant savings in power can be achieved. Voltage can be reduced to the DRAM, frequency is reduced to the DRAM, and the number of cycle requests to the DRAM are reduced making the device function in a very lower power state while maintaining a reasonable system performance level.

Ex. 1013 ¶ 50. We are persuaded by Petitioner's showing and find that Bonella teaches operating DRAM at a reduced frequency (i.e., the recited

"third clock frequency . . . less than the first clock frequency") to conserve power (i.e., in the recited "second mode of operation").

As for why a person of ordinary skill in the art would have modified Best in view of this knowledge, Petitioner states "(1) reducing power during volatile to non-volatile flush operations prompted by a power loss was a well-known technique, and (2) one known way to reduce the power consumption of DRAM devices was to reduce their frequency of operation." Pet. 64–65 (citing Ex. 1011; Ex. 1013). As evidence that reducing power during volatile to non-volatile flush operations was well-known, Petitioner cites U.S. Patent Publication 2006/0212651 A1 (Ex. 1011, "Ashmore"), which "reduc[es] battery power consumption during a main power loss to reduce the likelihood of loss of user write-cached data in a write-caching mass storage controller" and U.S. Patent No. 7,421,552 (Ex. 1012, "Long"), which discloses that "if there is a loss of primary power 34, ... provid[ing] a significantly slower clock signal to ... the controller 40 while the controller 40 moves data from the volatile-memory storage cache 42 to the flash-based memory vault 44." Pet. 65. As evidence that reducing power consumption of a DRAM by reducing its frequency of operation was well-known, Petitioner cites Bonella, which "explains that one way to reduce the power consumption of the memory module is to slow or reduce the operating frequency of the DRAM." Pet. 66. Petitioner further states that

> One of ordinary skill in the art would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss. A skilled artisan would have been motivated to perform this power reduction technique for all the reasons that were known in the art: e.g., decreasing the risk of data loss due to insufficient backup power (Ex. 1011, ¶7) and enabling the use of a smaller-sized backup power source (Ex.

> 1012, 4:54-64). Reducing power consumption during write flushing in response to a power loss would also have been the arrangement of old elements, each performing the same function it had been known to perform, in a way that yields no more than one of ordinary skill in the art would expect from such an arrangement (reducing power consumption during a power loss event, as suggested by Long and Ashmore). Ex. 1003, ¶307
>
> . . .
>
> One of ordinary skill in the art would also have found it obvious to reduce power consumption during Best's write flushing in response to a power loss using any known or conventional means, and would have also considered power consumption reduction techniques other than those of Ashmore and Long to obtain the same benefits, including those described in Bonella.

Pet. 66–67. On this record, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning that would support the legal conclusion of obviousness. *See KSR*, 550 U.S. at 418 (citing *Kahn*, 441 F.3d at 988).

Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, that claim 15 is unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, and over the combination of Best, Mills, Roy, and Bonella.

3. Patent Owner's Assertions Concerning the References

Patent Owner relies upon the same argument as for Ground 1—i.e., that Best does not teach a "memory module"—and argues that the Petition fails to show that Roy teaches a "memory module." PO Resp. 45. We are not persuaded by that argument for the reasons discussed above.

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Patent Owner also argues that claim 15 is not obvious in view of Bonella's Power Level 4. PO Resp. 46–47. Specifically, Patent Owner argues that Bonella does not indicate "what frequency the DRAM is operating at during a power loss" because "there is no suggestion in Bonella about what frequency the DRAM runs at when powered by the UPS battery." *Id.* at 46. Thus, concludes Patent Owner, Petitioner "fails to show evidence that operating in a 'power saving' mode prior to Bonella's 'power loss algorithm' has any effect on the clock frequencies during the 'power loss algorithm.'" *Id.* at 47.

Petitioner counters that it is relying upon Bonella's teaching to reduce power consumption by reducing DRAM operating frequency, not upon Bonella's Power Level 4 as a whole. Pet. Reply 21–22.

We agree with Petitioner. The Petition relies upon Bonella's teaching that reducing the operating frequency of a DRAM reduces power, and argues that a person of ordinary skill in the art would have known how, and been motivated, to apply that teaching to Best to reduce the power consumption of Best's DRAM during a power loss (i.e., in the "second mode of operation" recited in claim 15, when data is flushed from volatile memory subsystem to non-volatile memory subsystem) by operating it at a slower frequency (i.e., the "third clock frequency" recited in claim 15). Pet. 64–68. Although Bonella teaches frequency reduction in the context of Power Level 4, we are persuaded that a person of ordinary skill in the art would have known how to apply that teaching independent of the other aspects of Power Level 4 (e.g., limiting PCIe transaction performance). Pet. Reply 22.

Patent Owner also argues that claim 15 is not obvious in view of Petitioner's cited scenarios. PO Resp. 47–54. Specifically, Patent Owner

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characterizes Petitioner's proposed combination as comprising "two scenarios [that] are independent of each other," one in which power is reduced to devices other than the volatile memory subsystem during a power loss, and another in which power is reduced to the volatile memory subsystem during normal operation (i.e., *not* during a power loss). *Id.* at 48. According to Patent Owner, Long teaches away from, and Ashmore does not teach, the "third clock frequency." PO Resp. 49–52.

These arguments are not persuasive because Petitioner relies upon Bonella, not upon Ashmore and Long, for teaching a "third clock frequency." Patent Owner also constructs a hypothetical system based on teachings of Ashmore, Long, and Bonella that is *not* relied upon by Petitioner and concludes that its hypothetical combination "does not reduce the DRAM clock frequency during power loss mode as Petitioner asserts." *Id.* at 52–53. This argument also is not persuasive because Petitioner is relying upon Long and Ashmore as evidence of what a person of ordinary skill in the art would have known and been motivated by (Pet. 65–68), not for teaching the "third clock frequency," much less for collateral teachings about the specific components in Long and Ashmore to which power is reduced during a power loss. Similarly, Petitioner relies upon Bonella's teaching that DRAM power consumption can be reduced by slowing the operating frequency down (Pet. 66–67 (Ex. 1013 ¶¶ 49–50), not upon Bonella's teaching of a power-loss algorithm.

Patent Owner also argues that "Bonella does not teach that power (or frequency) is reduced during a power loss." *Id.* at 56. This argument is misplaced, however, because Petitioner is not relying upon Bonella to show power reducing frequency *during a power loss*. Petitioner is relying upon

Bonella's teaching that DRAM power consumption can be reduced by slowing the operating frequency down (Pet. 66–67 (Ex. 1013 ¶¶ 49–50)), and arguing that "[o]ne of ordinary skill in the art would have been motivated to reduce the power consumption during Best's write flushing in response to a power loss" (*id.* at 66).

Finally, Patent Owner argues a person of ordinary skill in the art would not have been motivated to combine Best with Bonella to "enable[e] the use of a smaller-sized backup power source," as Petitioner contends (Pet. 66), because "[a person of ordinary skill in the art] would know that Petitioner's power reduction will not reduce the required battery capacity or increase the amount of data that can be transferred." PO Resp. 60. Specifically, Patent Owner argues that "reducing the clock frequency . . . reduces power dissipation but simply spreads the task out over time, thereby consuming the same total energy." *Id.* at 61. Thus, according to Patent Owner, "because Petitioner's power reduction technique extends the time required to back up the DRAM, energy requirements are not reduced." *Id.* at 62.

Petitioner counters that Patent Owner's argument "ignores the energy consumption of an idle DRAM as it transfers data to a much-slower Flash memory." Pet. Reply 22. Petitioner highlights Mr. Maltiel's testimony that "the transfer of data between DRAM and FLASH could not occur faster than the speed of the FLASH, which in the case of Best would be substantially slower than the DRAM." Pet. Reply 23 (quoting Ex. 1003 ¶ 312). Patent Owner's declarant, Dr. Baker, testified that "accessing the memory in the big flash array takes considerably longer -- microseconds, as I testified -- than accessing memory in a DRAM, which could take, say, 10 to 50

nanoseconds, for example. So the access portion in a DRAM is considerably faster." Ex. 1020, 15:14–19. Thus, according to Petitioner, reducing the operating frequency of the DRAM does *not* extend the time required to flush the DRAM to the Flash as long as the operating frequency of the DRAM is still faster than that of the Flash. *Id.* at 23–24.

We agree with Petitioner. Patent Owner's argument assumes that the time to flush the DRAM to the Flash is directly proportional to the operating frequency of the DRAM. That process, however, is actually limited by the much slower operating frequency of the Flash memory. Ex. 1003 ¶ 312. We are persuaded by the arguments and evidence that a person of ordinary skill in the art would have known that reducing the operating frequency of the DRAM would enable the use of a smaller-sized backup power source because doing so reduces power consumption without extending the time required to flush the DRAM to the Flash.

4. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claim 15 of the '831 patent are unpatentable under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, and over Best, Mills, Roy, and Bonella.

I. Other Grounds

Because claims 1–14 are unpatentable over Best, with or without Roy, and because claim 15 is unpatentable over Best, Mills, and Bonella, or Best, Mills, Roy, and Bonella, we need not reach Petitioner's other grounds for unpatentability of these claims.

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J. Petitioner's Motion to Exclude

Petitioner filed a Motion to Exclude (Paper 17). Patent Owner filed an Opposition (Paper 20, "Opp."), and Petitioner filed a Reply in support of its Motion (Paper 22). As movant, Petitioner has the burden of proof to establish that it is entitled to the requested relief. *See* 37 C.F.R. § 42.20(c).

We decline to assess the merits of Petitioner's Motion to Exclude. Even without excluding the identified evidence, we have concluded that Petitioner has demonstrated, by a preponderance of the evidence, that the challenged claims are unpatentable. Accordingly, Petitioner's Motion to Exclude is dismissed.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that (1) claims 1–14 of the '831 patent are unpatentable under 35 U.S.C. § 102 as anticipated by Best; (2) claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best; (3) claims 1–14 are unpatentable under 35 U.S.C. § 103(a) as obvious over Best and Roy; and (4) claim 15 is unpatentable over Bowie under 35 U.S.C. § 103(a) as obvious over Best, Mills, and Bonella, with or without Roy.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–15 of the '831 patent are held *unpatentable*;

FURTHER ORDERED that Petitioner's Motion to Exclude is *dismissed*; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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Acknowledgement of Loss of Entitlement to Entity Status Discount

The entity status change request below filed through Private PAIR on 07/09/2018 has been accepted.

CERTIFICATIONS:

Change of Entity Status:

X Applicant changing to regular undiscounted fee status.
NOTE: Checking this box will be taken to be notification of loss of entitlement to small or micro entity status, as applicable.

This portion must be completed by the signatory or signatories making the entity status change in accordance with 37 CFR 1.4(d)(4).

Signature:	/Khaled Shami/
Name:	Khaled Shami
Registration Number:	38745

(12) **INTER PARTES REVIEW CERTIFICATE** (1756th)

United States Patent
Lee et al.

(10) **Number: US 8,874,831 K1**
(45) **Certificate Issued: May 12, 2020**

(54) **FLASH-DRAM HYBRID MEMORY MODULE**

(75) Inventors: **Hyun Lee**; **Chi-She Chen**; **Jeffrey C. Solomon**; **Scott Milton**; **Jayesh Bhakta**

(73) Assignee: **NETLIST, INC.**

Trial Number:

IPR2017-00692 filed Jan. 17, 2017

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Filed: **Jul. 26, 2012**

The results of IPR2017-00692 are reflected in this inter partes review certificate under 35 U.S.C. 318(b).

INTER PARTES REVIEW CERTIFICATE
U.S. Patent 8,874,831 K1
Trial No. IPR2017-00692
Certificate Issued May 12, 2020

AS A RESULT OF THE INTER PARTES REVIEW PROCEEDING, IT HAS BEEN DETERMINED THAT:

Claims **1-15** are cancelled.

* * * * *