

**CERTIFICATION AND REQUEST FOR PRIORITIZED EXAMINATION
UNDER 37 CFR 1.102(e) (Page 1 of 1)**

First Named Inventor:	Chi-She Chen	Nonprovisional Application Number (if known):	
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE		

APPLICANT HEREBY CERTIFIES THE FOLLOWING AND REQUESTS PRIORITIZED EXAMINATION FOR THE ABOVE-IDENTIFIED APPLICATION.

1. The processing fee set forth in 37 CFR 1.17(i)(1) and the prioritized examination fee set forth in 37 CFR 1.17(c) have been filed with the request. The publication fee requirement is met because that fee, set forth in 37 CFR 1.18(d), is currently \$0. The basic filing fee, search fee, and examination fee are filed with the request or have been already been paid. I understand that any required excess claims fees or application size fee must be paid for the application.
2. I understand that the application may not contain, or be amended to contain, more than four independent claims, more than thirty total claims, or any multiple dependent claims, and that any request for an extension of time will cause an outstanding Track I request to be dismissed.
3. The applicable box is checked below:

I. ☒ Original Application (Track One) - Prioritized Examination under § 1.102(e)(1)

- i. (a) The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a). This certification and request is being filed with the utility application via EFS-Web.
---OR---
(b) The application is an original nonprovisional plant application filed under 35 U.S.C. 111(a). This certification and request is being filed with the plant application in paper.
- ii. An executed inventor's oath or declaration under 37 CFR 1.63 or 37 CFR 1.64 for each inventor, or the application data sheet meeting the conditions specified in 37 CFR 1.53(f)(3)(i) is filed with the application.

II. ☐ Request for Continued Examination - Prioritized Examination under § 1.102(e)(2)

- i. A request for continued examination has been filed with, or prior to, this form.
- ii. If the application is a utility application, this certification and request is being filed via EFS-Web.
- iii. The application is an original nonprovisional utility application filed under 35 U.S.C. 111(a), or is a national stage entry under 35 U.S.C. 371.
- iv. This certification and request is being filed prior to the mailing of a first Office action responsive to the request for continued examination.
- v. No prior request for continued examination has been granted prioritized examination status under 37 CFR 1.102(e)(2).

Signature /Khaled Shami/	Date May 24 2021
Name (Print/Typed) Khaled Shami	Practitioner Registration Number 38,745

Note: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. Submit multiple forms if more than one signature is required.*

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I hereby revoke all previous powers of attorney given in the application identified in either the attached transmittal letter or the boxes below.

Application Number	Filing Date

(Note: The boxes above may be left blank if information is provided on form PTO/AIA/82A.)

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151145

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I am the Applicant (if the Applicant is a juristic entity, list the Applicant name in the box):

Netlist, Inc.

- ☐ Inventor or Joint Inventor (title not required below)
- ☐ Legal Representative of a Deceased or Legally Incapacitated Inventor (title not required below)
- ☒ Assignee or Person to Whom the Inventor is Under an Obligation to Assign (provide signer's title if applicant is a juristic entity)
- ☐ Person Who Otherwise Shows Sufficient Proprietary Interest (e.g., a petition under 37 CFR 1.46(b)(2) was granted in the application or is concurrently being filed with this document) (provide signer's title if applicant is a juristic entity)

SIGNATURE of Applicant for Patent

The undersigned (whose title is supplied below) is authorized to act on behalf of the applicant (e.g., where the applicant is a juristic entity).

Signature

Date (Optional)

12/5/17

Name

Noel B. Whitley

Title

VP, IP & Licensing

NOTE: Signature - This form must be signed by the applicant in accordance with 37 CFR 1.33. See 37 CFR 1.4 for signature requirements and certifications. If more than one applicant, use multiple forms.

☐ Total of forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Ex. 1052, p. 3

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Application Number	61/798,956
Filing Date	03-15-2013
First Named Inventor	Scott H. Milton
Title	HYBRID MEMORY SYSTEM WITH CONFIGURABLE ERROR THRESHOLD PARAMETERS
Art Unit	Not assigned
Examiner Name	Not assigned
Attorney Docket Number	0016.0020000

SIGNATURE of Applicant or Patent Practitioner

Signature	/Khaled Shami/	Date (Optional)	
Name	Khaled Shami	Registration Number	38,745
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

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*Total of _____ forms are submitted.

This collection of information is required by 37 CFR 1.131, 1.32, and 1.33. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 3 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 17/138,766, filed December 30, 2020, titled "Flash-Dram Hybrid Memory", now U.S. Patent No. 11,016,918, which is a continuation of U.S. Patent Application No. 15/934,416, filed March 23, 2018, titled "Flash-Dram Hybrid Memory Module," which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled "Flash-Dram Hybrid Memory Module," now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled "Non-Volatile Memory Module," now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

[0002] This application may be considered related to U.S. Patent Application No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed February 5, 2014, which is a continuation of U.S. Patent Application 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Patent 8,677,060, issued

March 18, 2014, which is a continuation of U.S. Patent Application 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed June 28, 2012, now U.S. Patent 8,516,187, issued August 20, 2013, which is a divisional of U.S. Patent Application 12/240,916, titled "Non-Volatile Memory Module," filed September 29, 2008, now U.S. Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007, the contents of which are incorporated by reference herein in their entirety.

[0003] This application may also be considered related to U.S. Patent Application No. 15/000,834, filed January 19, 2016 (abandoned), which is a continuation of U.S. Patent Application No. 14/489,332, filed September 17, 2014, now U.S. Patent No. 9,269,437, which is a continuation of U.S. Patent Application No. 14/173,219, filed February 5, 2014, now U.S. Patent No. 8,904,099, which is a continuation of U.S. Patent Application No. 13/905,048, filed May 29, 2013, now U.S. Patent No. 6,671,243, which is a continuation U.S. Patent Application 13/536,173 above.

[0004] This application may also be considered related to U.S. Patent Application No. 15/924,866, (abandoned), which is a continuation of U.S. Patent Application No. 14/489,281, filed September 17, 2014, now U.S. Patent No. 9,921,762, which is a continuation of U.S. Patent Application No. 13/625,563, filed September 24, 2012, now U.S. Patent No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed September 23, 2011.

TECHNICAL FIELD

[0005] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0006] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0007] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as ‘finance transactions’ (for example, point-of-service, inter-bank transaction, stock market transaction), ‘scientific computation’ (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), ‘medical diagnostics’ (for example, diagnostics based on the fuzzy logic, medical data processing), ‘simple information sharing and searching’ (for example, web search, retail store website, company home page), ‘email’ (information distribution and archive), ‘security service’, ‘entertainment’ (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high

speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0008] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0009] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM. The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a

data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MB/s for the EcoRAM vs. 104MB/s for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™, which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0010] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0011] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash

DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0012] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

[0013] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0014] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0015] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

[0016] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0017] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0018] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0019] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0020] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0021] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0022] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0023] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0024] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0025] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0026] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0027] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0028] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

[0029] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0030] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0031] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0032] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0033] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0034] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0035] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0036] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0037] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0038] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0039] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0040] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0041] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0042] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0043] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0044] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0045] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0046] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0047] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0048] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0049] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0050] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0051] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0052] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0053] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0054] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0055] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0056] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0057] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0059] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0060] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0061] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0062] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0063] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0064] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0065] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0066] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0067] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0068] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0069] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

[0070] Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to

allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

[0071] Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

[0072] Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0073] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0074] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. 12 is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. 13 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. 14 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. 15A-15C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. 16 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

FIG. 17 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. 18 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. 19 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. 20 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. 22 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0075] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to

implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0076] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0077] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only

Memory), EEPROM (Electrically Erasable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0078] The term “exemplary” where used herein is intended to mean “serving as an example, instance or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments.

[0079] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0080] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0081] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0082] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or

commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0083] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0084] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0085] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400' supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then

the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0086] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0087] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0088] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory

module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0089] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In

the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0090] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0091] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH

510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0092] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0093] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the

DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0094] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0095] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate

and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0096] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0097] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or

provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510.

[0098] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0099] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[00100] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[00101] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash-DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[00102] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 506 and the other for the DRAM memory DRAM 508. The MCH treats the DRAM 508 and Flash 506 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash 506 and DRAM 508 allows for direct data transfer to occur between the Flash 506 and the DRAM 508 in response to control information from Ctrl 502. In this embodiment, this data transfer mechanism provides direct support for executing commands from

the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 506 to the DRAM 508. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[00103] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[00104] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[00105] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a

first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[00106] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[00107] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[00108] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502

monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00109] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1061

field, a Block address 1051 field, a Plane address 1041, a Page address 1031, and a group of least significant address bits A_0A_1 1021. The Plane address 1041 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00110] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00111] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400 μ s, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash

memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00112] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

$$((\text{\#of blocks per bank})/(\text{ratio of 'Flash_block_write_time' to 'Flash_read_time'})) * (\text{Block usage time})/(\text{'Flash_block_write_time'})$$

[00113] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00114] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00115] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up

the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[00116] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[00117] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor

array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[00118] In certain embodiments, the power module transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[00119] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[00120] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[00121] FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory

subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.

[00122] In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 1010 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for

example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[00123] In certain preferred embodiments, the memory system 1010 is in electrical communication with the host system. In other embodiments, the memory system 1010 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system 1010 can be in communication with a disk controller of a computer system, for example. The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.

[00124] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem 1040 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 1030. In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and

synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00125] In certain embodiments, the second plurality of non-volatile memory elements 1042 comprises one or more flash memory elements. Types of flash memory elements 1042 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. 12, the second memory bank 1040 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 1042. In addition, nonvolatile memory elements 1042 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 1042 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00126] FIG. 13 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 1030 with nine volatile memory elements

1032 and a non-volatile memory subsystem 1040 with five non-volatile memory elements 1042 in accordance with certain embodiments described herein. The additional memory element 1032 of the first memory bank 1030 and the additional memory element 1042 of the second memory bank 1040 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 1030 comprises other numbers of volatile memory elements 1032 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 1040 comprises other numbers of nonvolatile memory elements 1042 (e.g., 2, 3, more than 5).

[00127] Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one

embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.

[00128] In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system.

[00129] In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one

or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150.

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash “mirror” to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 1010 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example,

1010 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[00131] As schematically illustrated by FIGS. 12 and 13, in certain embodiments, the controller 1062 may comprise a microcontroller unit (MCU) 1060 and a logic element 1070. In certain embodiments, the MCU 1060 provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 and the nonvolatile memory subsystem 1040. The MCU 1060 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. 12 and 13, the logic element 1070 of certain embodiments is in electrical communication with the non-volatile memory subsystem 1040 and the MCU 1060. The logic element 1070 can provide signal level translation between the volatile memory elements 1032 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 1042 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 1070 is also programmed to perform address/address translation between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 1042 because of their superior read speed and compact structure.

[00132] The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the

volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[00133] The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.

[00134] The isolation or operational decoupling of the volatile memory subsystem 1030 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 1010 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 1030. For example, in one embodiment during such periods of operation, the controller 1062 and the nonvolatile memory subsystem 1040 do not add a significant capacitive load to the volatile memory system 1030 when the memory system 1010 is in the first state. In certain such embodiments, the capacitive load of the controller 1062 and the non-volatile memory subsystem 1040 do not significantly affect the signals propagating between the volatile memory subsystem 1030 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 1052 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 1052 comprises other types of isolation devices.

[00135] Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. In certain embodiments, the memory system 1010 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 1010 enters the second state in response to a trigger condition. In certain embodiments, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory

subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.

[00136] In certain embodiments, the second power supply 1080 does not comprise a battery. Because a battery is not used, the second power supply 1080 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. 12-14, the second power supply 1080 comprises a step-up transformer 1082, a step-down transformer 1084, and a capacitor bank 1086 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 1080 is configured to power the volatile memory subsystem 1030 for less than thirty minutes. In certain embodiments, the second power supply 1080 may comprise a battery. For example, in certain embodiments, the second power supply 1080 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 1030 for no more than thirty minutes.

[00137] In certain embodiments, the capacitor bank 1086 of the second power supply 1080 is charged by the first power supply while the memory system 1010 is in the first state. As a result, the second power supply 1080 is fully charged when the memory system 1010 enters the second state. The memory system 1010 and the second power supply 1080 may be located on the same printed circuit board 1020. In other embodiments, the second power supply 1080 may not be on

the same printed circuit board 1020 and may be tethered to the printed circuit board 1020, for example.

[00138] When operating in the first state, in certain embodiments, the step-up transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the step-down transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. 12-14, the memory module 1010 further comprises a switch 1090 (e.g., FET switch) that switches power provided to the controller 1062, the volatile memory subsystem 1030, and the non-volatile memory subsystem 1040, between the power from the second power supply 1080 and the power from the first power supply (e.g., system power) received via the interface 1022. For example, the switch 1090 may switch from the first power supply to the second power supply 1080 when the voltage monitor 1050 detects a low voltage condition. The switch 1090 of certain embodiments advantageously ensures that the volatile memory elements 1032 and non-volatile memory elements 1042 are powered long enough for the data to be transferred from the volatile memory elements 1032 and stored in the non-volatile memory elements 1042. In certain embodiments, after the data transfer is complete, the switch 1090 then switches back to the first power supply and the controller 1062 transmits a signal to the at least one circuit 1052 to operatively decouple the controller 1062 from the volatile memory subsystem 1030, such that the memory system 1010 reenters the first state.

[00139] When the memory system 1010 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 via the

controller 1062. The host system can then resume accessing the volatile memory subsystem 1030 of the memory module 1010. In certain embodiments, after the memory system 1010 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 1030 rather than the non-volatile memory subsystem 1040 because the volatile memory elements 1032 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 1030 to the nonvolatile memory bank 1040, or from the non-volatile memory bank 1040 to the volatile memory bank 1030, takes less than one minute per GB.

[00140] In certain embodiments, the memory system 1010 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 1010 copies the entire contents of the volatile memory subsystem 1030 into the nonvolatile memory subsystem 1040 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are copied back into the volatile memory subsystem 1030 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 1040 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 1010. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 1010 and can improve the performance of the memory system 1010. In certain other embodiments, the entire contents of the volatile memory subsystem 1030 are not copied into the non-volatile memory subsystem 1040 on each backup operation, but only a partial copy is performed. In certain embodiments, other

management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 1040 are performed in the controller 1062.

[00141] The memory system 1010 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 1030 which then writes the data to non-volatile storage which is not part of the memory system 1010, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 1010 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 1010 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 1010 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 1010 may be operated as a write-through cache or as some other type of cache.

[00142] FIG. 16 schematically illustrates an example power module 1100 of the memory system 1010 in accordance with certain embodiments described herein. The power module 1100 provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. In certain embodiments, the power module 1100 comprises one or more of the components described above with respect to FIG. 12. For example, in certain embodiments, the power module 1100 includes the second power supply 1080 and the switch 1090.

[00143] The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110.

[00144] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106.

[00145] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element

1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120.

[00146] In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.

[00147] In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For

example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142.

[00148] The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate

amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.

[00149] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.

[00150] FIG. 17 is a flowchart of an example method 1200 of providing a first voltage 1102 and a second voltage 1104 to a memory system 1010 including volatile and nonvolatile memory subsystems 1030, 1040. While the method 1200 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-15, other memory systems are also compatible with embodiments of the method 1200. During a first condition, the method 1200

comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 and providing the second voltage 1104 to the memory system 1010 from a first power subsystem in operational block 1210. For example, in one embodiment, the first power subsystem comprises the first power element 1130 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, other first power subsystems are used.

[00151] The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.

[00152] The method 1200 further comprises charging a second power subsystem in operational block 1240. In certain embodiments, the second power subsystem comprises the second power element 1140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 1140 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, some other second power subsystem is used.

[00153] The method 1200 further comprises detecting a third condition in an operational block 1250 and during the third condition, providing the first voltage 1102 and the second

voltage 1104 to the memory system 1010 from the second power subsystem 1140 in an operational block 1260. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 1200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 1140 is charged before detecting the second condition.

[00154] In certain embodiments, the memory system 1010 comprises a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 1010 also comprises a controller 1062 operatively coupled to the volatile memory subsystem 1030 and operatively coupled to the non-volatile memory subsystem 1040. The controller 1062 can be configured to allow data to be communicated between the volatile memory subsystem 1030 and the host system when the memory system 1010 is operating in a first state and to allow data to be communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040 when the memory system 1010 is operating in a second state.

[00155] Although the memory system 1010 having extra storage capacity of the non-volatile memory subsystem 1040 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In various embodiments, there may be at least 200, 300, or 400 percent more

storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In other embodiments, the non-volatile memory subsystem 1040 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 1030. In some embodiments, the non-volatile memory subsystem 1040 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 1030. In one embodiment, the non-volatile memory subsystem 1040 includes less than 100 percent more storage capacity than does the volatile memory subsystem 1030.

[00156] The extra storage capacity of the non-volatile memory subsystem 1040 can be used to improve the backup capability of the memory system 1010. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 1040 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem 1040 allows the volatile memory subsystem 1030 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to backup the volatile memory subsystem 1030 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 1030 is copied to a first, previously erased portion of the nonvolatile memory subsystem 1040 via the controller 1062. Since the non-volatile memory subsystem 1040 has more storage capacity than does the volatile memory subsystem 1030, there is a second portion of the non-volatile memory subsystem 1040 which does not have data from the volatile memory subsystem 1030 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 1062 of the memory system 1010 restores the data to the volatile memory subsystem 1030 by copying the backed-up data from the non-volatile memory

subsystem 40 back to the volatile memory subsystem 1030. After the data is restored, the memory system 1010 erases the non-volatile memory subsystem 1040. While the first portion of the non-volatile memory subsystem 1040 is being erased, it may be temporarily inaccessible.

[00157] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 1040 is completely erased, the volatile memory subsystem 1030 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 1040 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 1040, the memory system 1010 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 1040.

[00158] FIG. 18 is a flowchart of an example method 1300 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. In certain embodiments, the non-volatile memory subsystem 1040 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 1300 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-14, the method 1300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 1310, the method 1300 comprises communicating data between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation. The method 1300 further comprises storing a first copy of data from the

volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a first time when the memory system 1010 is in a second mode of operation in an operational block 1320.

[00159] In an operational block 1330, the method 1300 comprises restoring the first copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030. The method 1300 further comprises erasing the first copy of data from the non-volatile memory subsystem 1040 in an operational block 1340. The method further comprises storing a second copy of data from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a second time when the memory system 1010 is in the second mode of operation in an operational block 1350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 1040.

[00160] In some embodiments, the memory system 1010 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 1040. The method 1300 can also include restoring the second copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 in an operational block 1360. The operational blocks of method 1300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem 1030 at operational block 1360 before the first copy of data is completely erased in the operational block 1340.

[00161] FIG. 19 schematically illustrates an example clock distribution topology 1400 of a memory system 1010 in accordance with certain embodiments described herein. The clock

distribution topology 1400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 1010. A clock source 1402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 1402 may feed a clock generator 1404 which provides a clock signal 1406 to the controller 1062, which may be an FPGA. In one embodiment, the clock generator 1404 generates a 125 MHz clock signal 1406. The controller 1062 receives the clock signal 1406 and uses it to clock the controller 1062 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 1062.

[00162] The clock signal 1406 can also be input into a clock divider 1410 which produces a frequency-divided version of the clock signal 1406. In an example embodiment, the clock divider 1410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 1406. A non-volatile memory phase-locked loop (PLL) block 1412 can be included (e.g., in the controller 1062) which distributes a series of clock signals to the non-volatile memory subsystem 1040 and to associated control logic. For example, a series of clock signals 1414 can be sent from the controller 1062 to the non-volatile memory subsystem 1040. Another clock signal 1416 can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem 1040. For example, the clock signal 1416 may clock the portion of the controller 1062 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 1040. A feedback clock signal 1418 is fed back into the non-volatile memory PLL block 1412. In one embodiment, the PLL block 1412 compares the feedback clock 1418 to the reference clock 1411 and varies the phase and frequency of its output until the reference 1411 and feedback 1418 clocks are phase and frequency matched.

[00163] A version of the clock signal 1406 such as the backup clock signal 1408 may be sent from the controller to the volatile memory subsystem 1030. The clock signal 1408 may be, for example, a differential version of the clock signal 1406. As described herein, the backup clock signal 1408 may be used to clock the volatile memory subsystem 1030 when the memory system 1010 is backing up the data from the volatile memory subsystem 1030 into the non-volatile memory subsystem 1040. In certain embodiments, the backup clock signal 1408 may also be used to clock the volatile memory subsystem 1030 when the memory system 1010 is copying the backed-up data back into the volatile memory subsystem 1030 from the nonvolatile memory subsystem 1040 (also referred to as restoring the volatile memory subsystem 1030). The volatile memory subsystem 1030 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the nonvolatile memory subsystem 1040 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 1030 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 1030 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 1010.

[00164] In one embodiment, the backup clock 1408 and the volatile memory system clock signal 1420 are received by a multiplexer 1422, as schematically illustrated by FIG. 19. The multiplexer 1422 can output either the volatile memory system clock signal 1420 or the backup clock signal 1408 depending on the backup state of the memory system 1010. For example, when the memory system 1010 is not performing a backup or restore operation and is

communicating with the host system (e.g., normal operation), the volatile memory system clock signal 1420 may be provided by the multiplexer 422 to the volatile memory PLL block 1424. When the memory system 1010 is performing a backup (or restore) operation, the backup clock signal 1408 may be provided.

[00165] The volatile memory PLL block 1424 receives the volatile memory reference clock signal 1423 from the multiplexer 1422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 1030 and associated control logic. For example, in one embodiment, the PLL block 1424 generates a series of clock signals 1426 which clock the volatile memory elements 1032. A clock signal 1428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal 1430 may be sent to the controller 1062. A feedback clock signal 1432 is fed back into the volatile memory PLL block 1424. In one embodiment, the PLL block 1424 compares the feedback clock signal 1432 to the reference clock signal 1423 and varies the phase and frequency of its output until the reference clock signal 1423 and the feedback clock signal 1432 clocks are phase and frequency matched.

[00166] The clock signal 1430 may be used by the controller 1062 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 1030. For example, control logic in the controller 1062 may be used to control the volatile memory subsystem 1030 during a backup or restore operation. The clock signal 1430 may be used as a reference clock signal for the PLL block 1434 which can generate one or more clocks 1438 used by logic in the controller 1062. For example, the PLL block 1434 may generate one or more clock signals 1438 used to drive logic circuitry associated with

controlling the volatile memory subsystem 1030. In certain embodiments, the PLL block 1434 includes a feedback clock signal 1436 and operates in a similar manner to other PLL blocks described herein.

[00167] The clock signal 1430 may be used as a reference clock signal for the PLL block 1440 which may generate one or more clock signals used by a sub-block 1442 to generate one or more other clock signals 1444. In one embodiment, for example, the volatile memory subsystem 1030 comprises DDR2 SDRAM elements and the sub-block 1442 generates one or more DDR2 compatible clock signals 1444. A feedback clock signal 1446 is fed back into the PLL block 1440. In certain embodiments, the PLL block 1440 operates in a similar manner to other PLL blocks described herein.

[00168] While described with respect to the example embodiment of FIG. 19, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 1030 operates on the volatile memory clock signal 1420 and there is no backup clock signal 1408. In some embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a restore operation and not during a backup operation.

[00169] FIG. 20 is a flowchart of an example method 1500 of controlling a memory system 1010 operatively coupled to a host system. Although described with respect to the memory

system 1010 described herein, the method 1500 is compatible with other memory systems. The memory system 1010 may include a clock distribution topology 1400 similar to the one described above with respect to FIG. 19 or another clock distribution topology. The memory system 1010 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 1040.

[00170] In an operational block 1510, the method 1500 comprises operating the volatile memory subsystem 1030 at a first frequency when the memory system 1010 is in a first mode of operation in which data is communicated between the volatile memory subsystem 1030 and the host system. In an operational block 1520, the method 1500 comprises operating the non-volatile memory subsystem 1040 at a second frequency when the memory system 1010 is in a second mode of operation in which data is communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. The method 1500 further comprises operating the volatile memory subsystem 1030 at a third frequency in an operational block 1530 when the memory system 1010 is in the second mode of operation. In certain embodiments, the memory system 1010 is not powered by a battery when it is in the second mode of operation. The memory system 1010 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

[00171] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 1010.

[00172] FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062. In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 1630, 1640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice

from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[00173] In certain embodiments, the switches 1650, 1652 can each be selectively switched to selectively operatively couple the data lines 1632, 1642, respectively from the first and second DRAM segments 1630, 1640 to the controller 1062. The chip select lines 1634, 1644 enable the first and second DRAM segments 1630, 1640, respectively, of the volatile memory subsystem 1030, and the self-refresh lines 1636, 1646 toggle the first and second DRAM segments 1630, 1640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[00174] In certain embodiments, when the memory system 1010 is backing up the volatile memory system 1030, data slices from only one of the two DRAM segments 1630, 1640 at a time are sent to the controller 1062. For example, when the first slice is being written to the controller 1062 during a back-up, the controller 1062 sends a signal via the CKe line 1636 to the first DRAM segment 1630 to put the first DRAM segment 1630 in active mode. In certain embodiments, the data slice from the first DRAM segment 1630 for multiple words (e.g., a block of words) is written to the controller 1062 before writing the second data slice from the second DRAM segment 1640 to the controller 1062. While the first data slice is being written to the controller 1062, the controller 1062 also sends a signal via the CKe line 1646 to put the second DRAM segment 1640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 1062, the controller 1062 puts the first DRAM segment 1630

into self-refresh mode by sending a signal via the CKe line 1636 to the first DRAM segment 1640. The controller 1062 also puts the second DRAM segment 1640 into active mode by sending a signal via the CKe line 1646 to the DRAM segment 1640. The second slice for a word or for a block of words is written to the controller 1062. In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.

[00175] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1042 write each backed-up data word to the controller 1062 which writes a first slice of the data word to the volatile memory subsystem 1030 and then a second slice of the data word to the volatile memory subsystem 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00176] FIG. 22 is a flowchart of an example method 1600 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. Although described with respect to the memory system 1010 described herein with respect to FIGS. 12-14 and 21, the method 1600 is compatible with other memory systems. The method 1600 comprises communicating data words between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation in an operational block 1610. For example, the memory

system 1010 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[00177] In an operational block 1620, the method further comprises transferring data words from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 when the memory system 1010 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.

[00178] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The

40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[00179] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[00180] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1040 write each backed-up data word to the controller 1062 which writes a first portion of the data word to the volatile memory subsystem 1030 and then a second portion of the data word to the volatile memory 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00181] The method 1600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem 1030 comprises DRAM elements, only the slice of the DRAM which is currently being accessed

(e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 1600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[00182] In addition, the connection between the DRAM elements and the controller 1062 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 1062 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 1062 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 1030. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[00183] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

CLAIMS

What is claimed is:

1. A memory module comprising:
 - a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
 - a first buck converter configured to provide a first regulated voltage having a first voltage amplitude;
 - a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;
 - a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;
 - a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and
 - a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:
 - a plurality of synchronous dynamic random access memory (SDRAM) devices coupled to the first regulated voltage, and
 - at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein one of the second and fourth voltage amplitudes is less than the other one of the second and fourth voltage amplitudes.

ABSTRACT

In certain embodiments, a memory module includes a printed circuit board (PCB) having an interface that couples it to a host system for provision of power, data, address and control signals. First, second, and third buck converters receive a pre-regulated input voltage and produce first, second and third regulated voltages. A converter circuit reduces the pre-regulated input voltage to provide a fourth regulated voltage. Synchronous dynamic random access memory (SDRAM) devices are coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, and a voltage monitor circuit monitors an input voltage and produces a signal in response to the input voltage having a voltage amplitude that is greater than a threshold voltage.

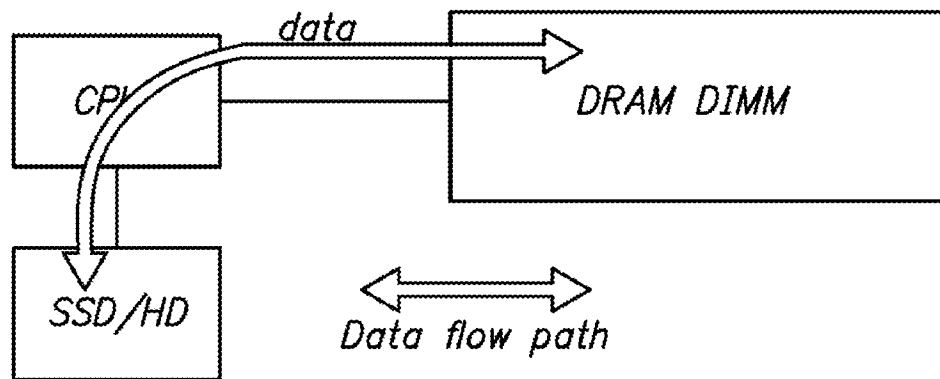


FIG. 1
(PRIOR ART)

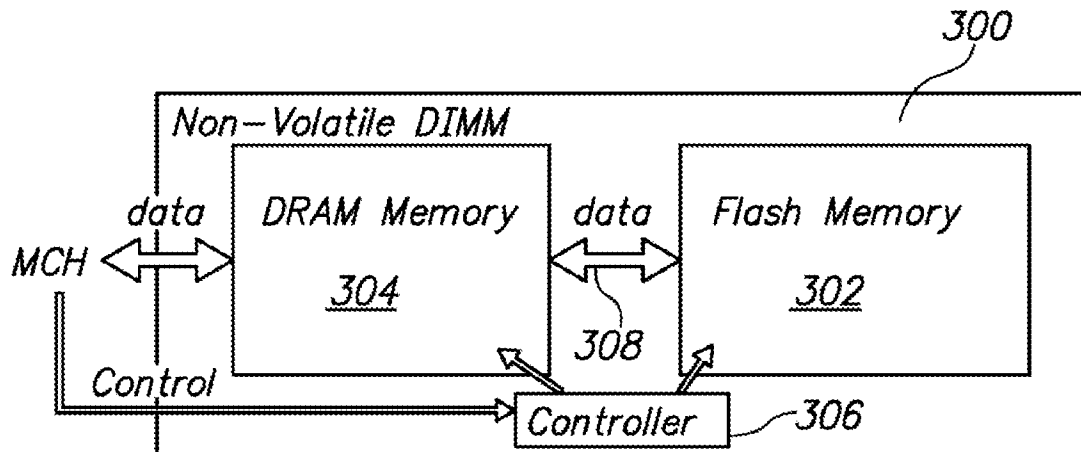
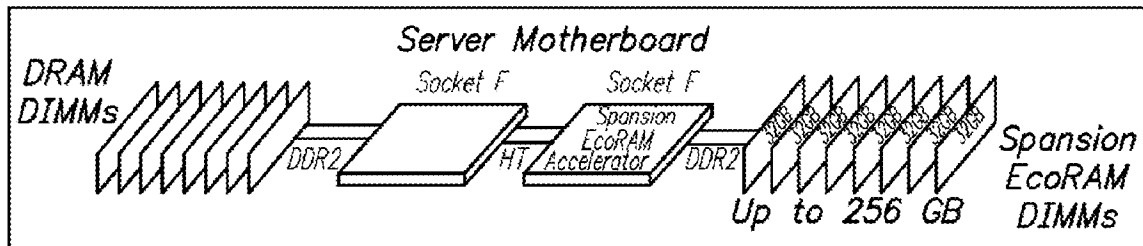


FIG. 3A

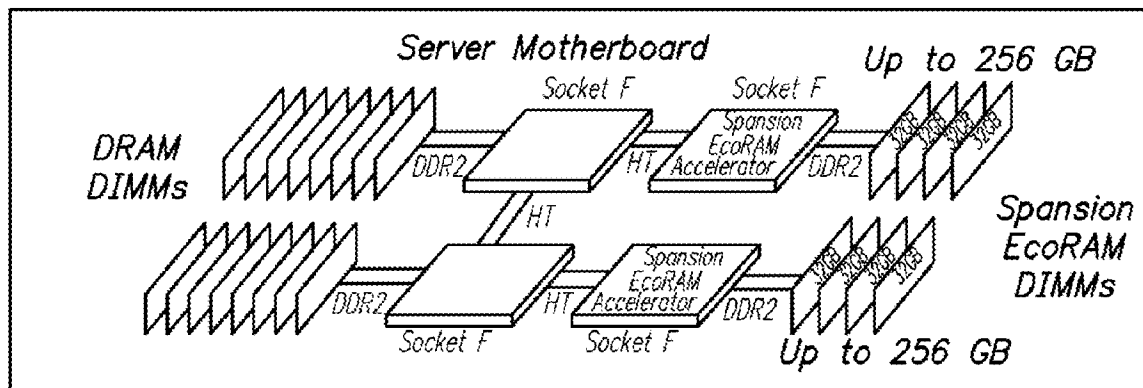
Spancion EcoRAM Configurations

256GB Spancion EcoRAM Solution – Single Accelerator



256GB Single Accelerator Spancion EcoRAM Solution

256GB Spancion EcoRAM Solution – Dual Accelerator



256GB Single Accelerator Spancion EcoRAM Solution

FIG. 2
(PRIOR ART)

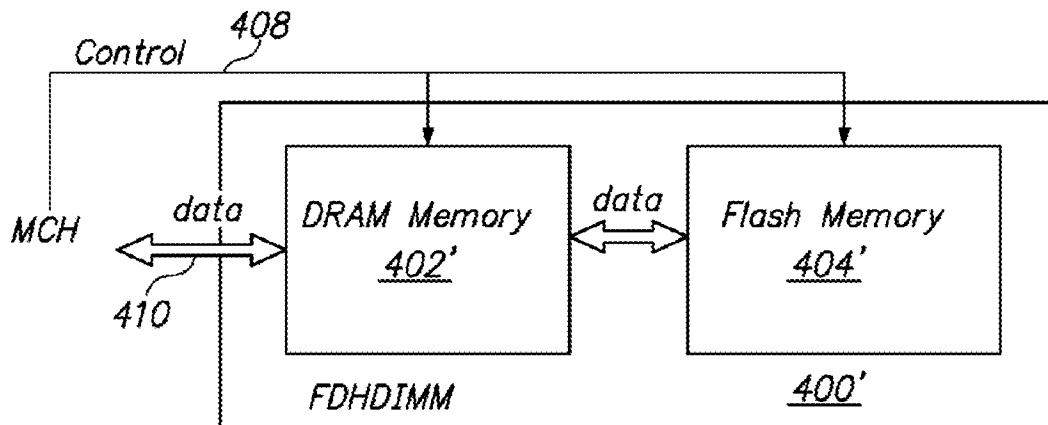


FIG. 4B

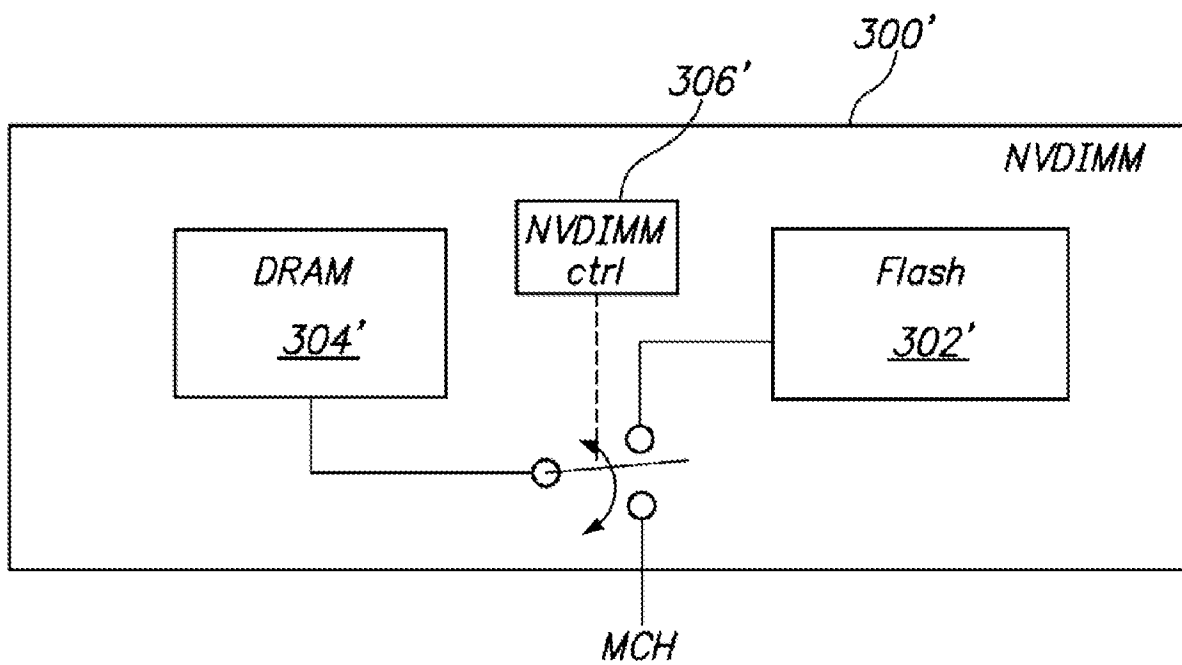


FIG. 3B

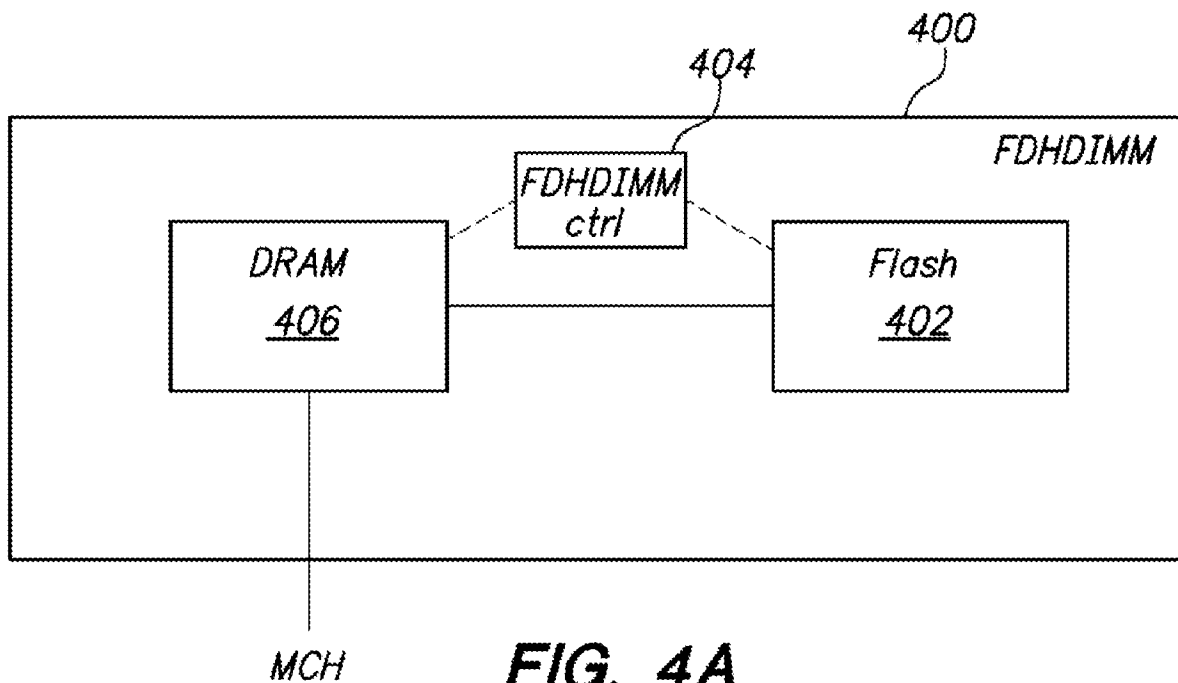


FIG. 4A

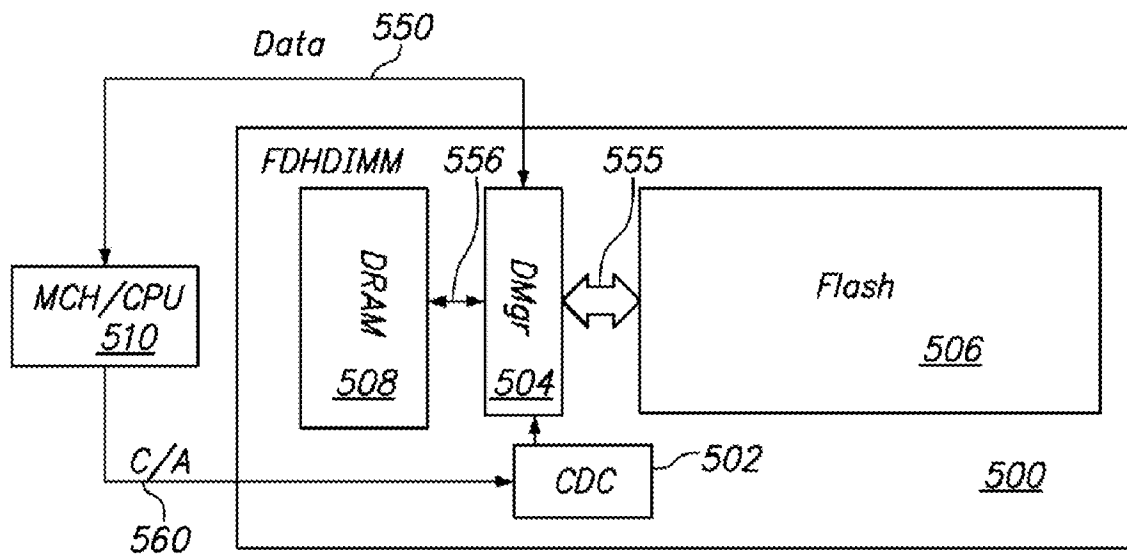


FIG. 5A

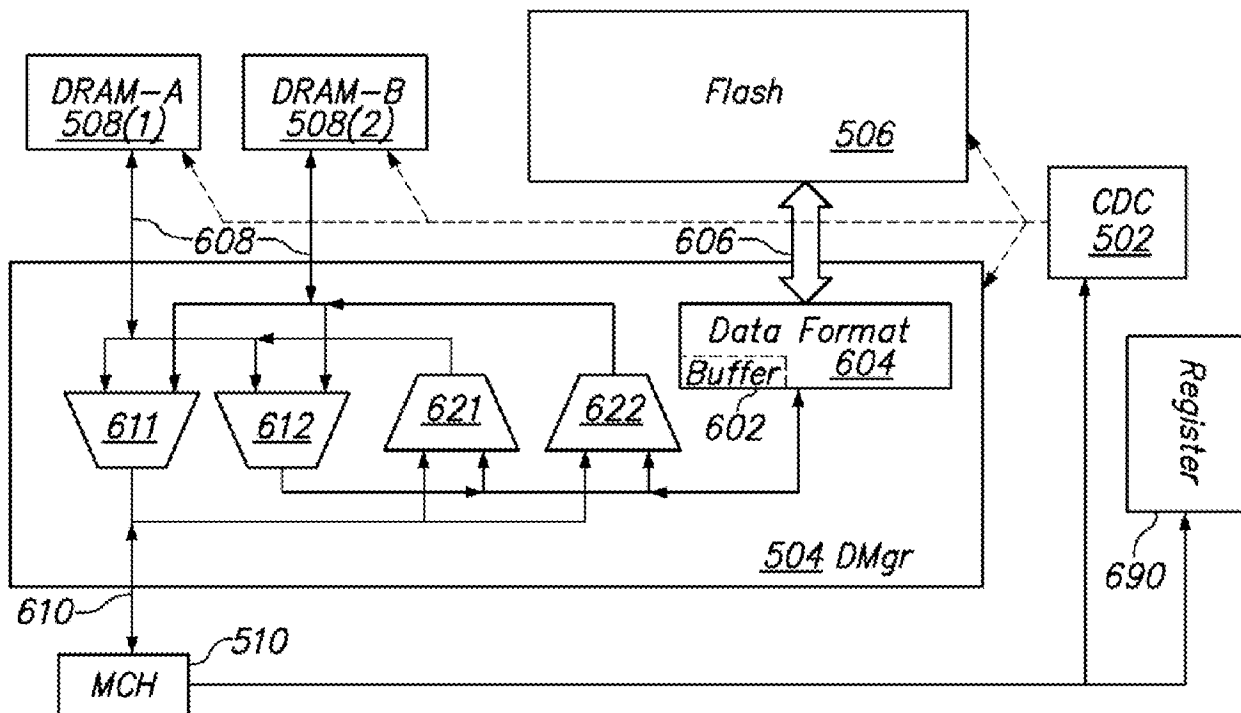


FIG. 6

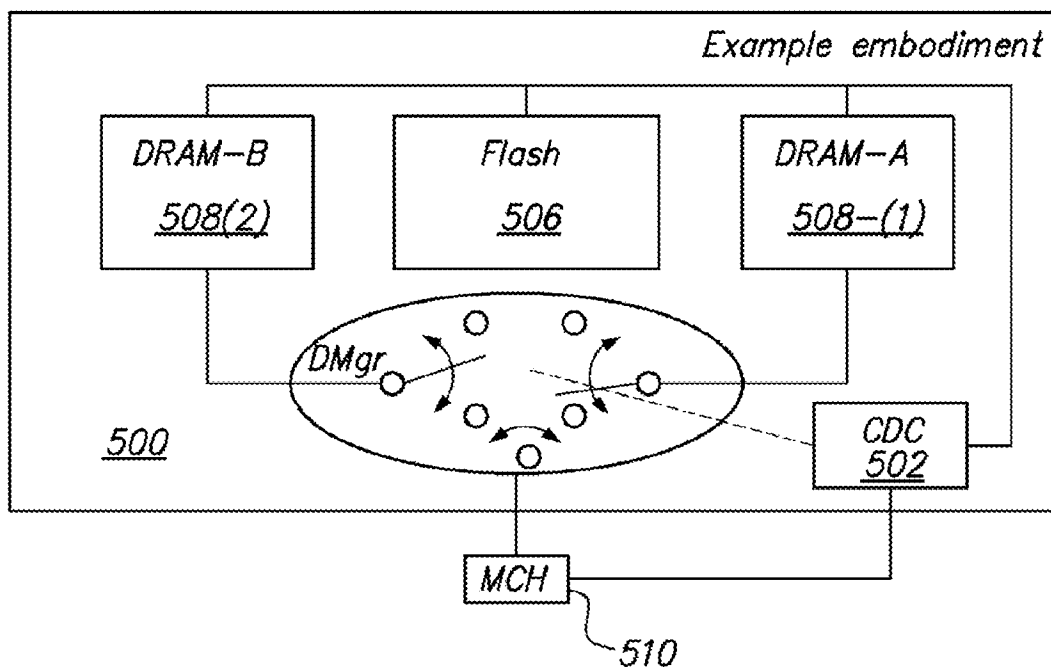


FIG. 5B

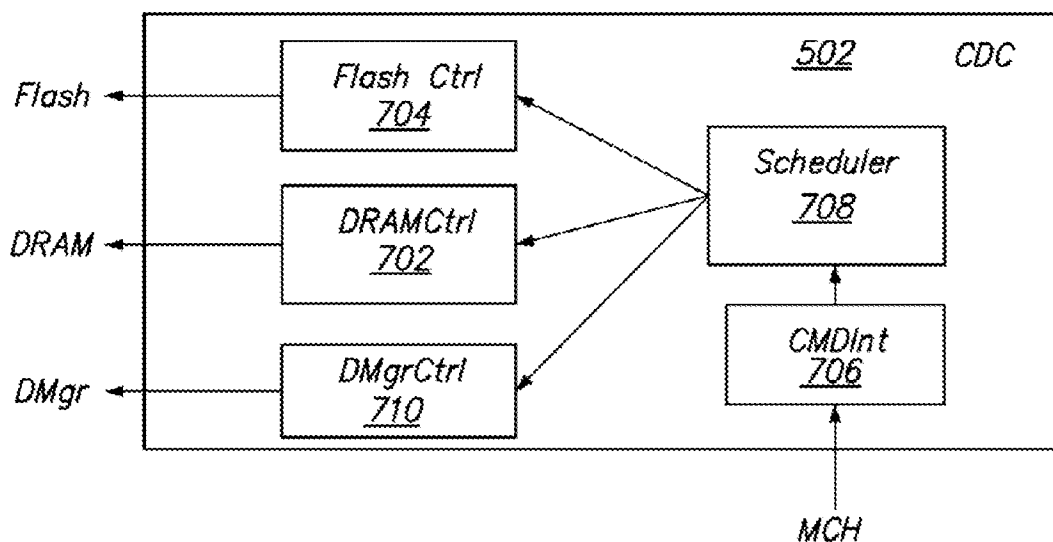


FIG. 7

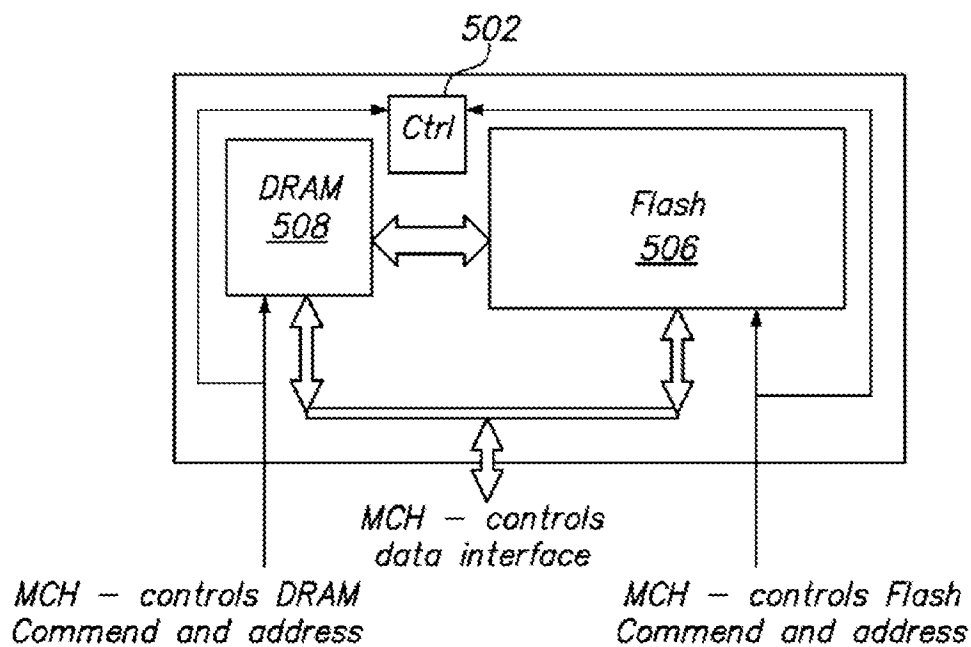


FIG. 8A

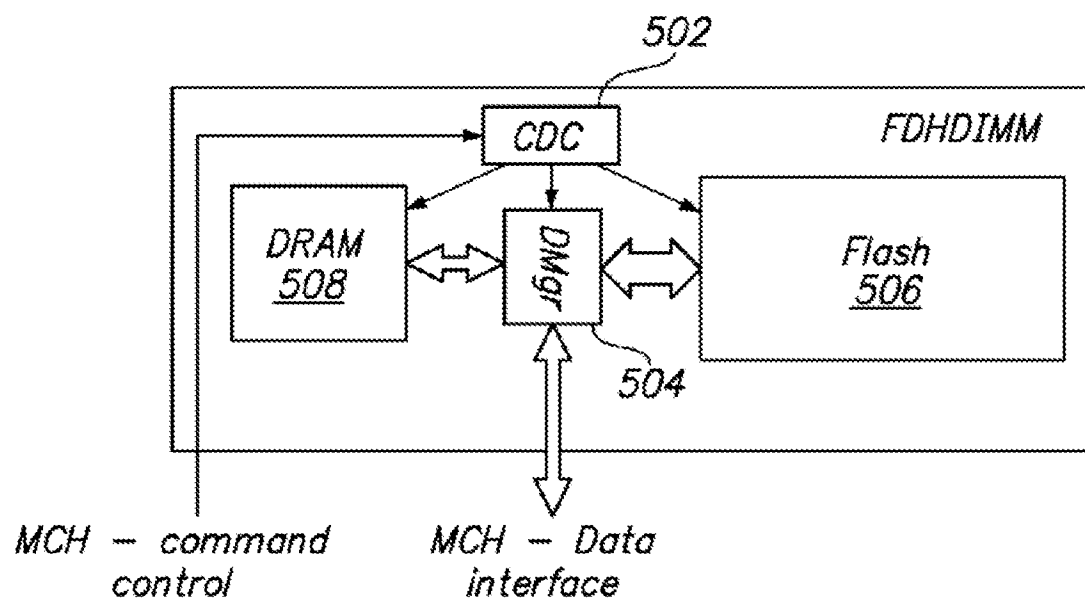
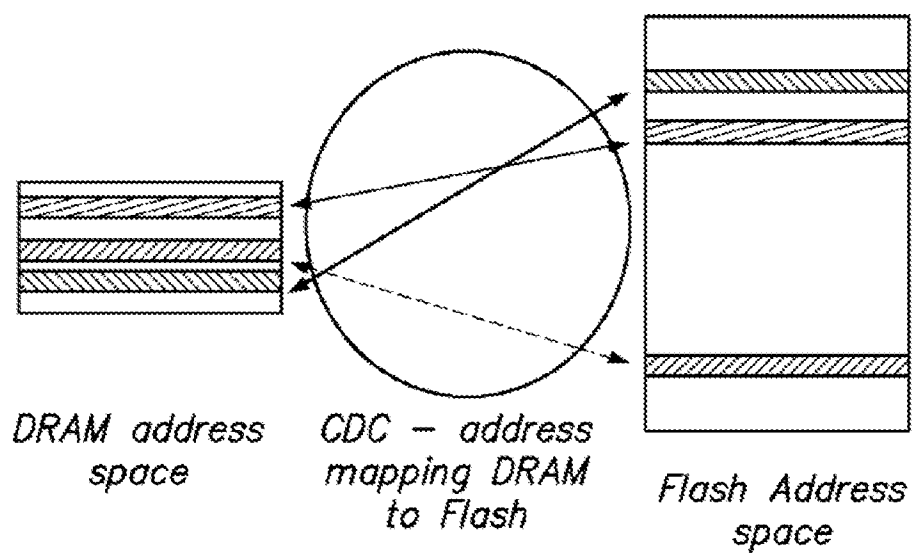


FIG. 8B

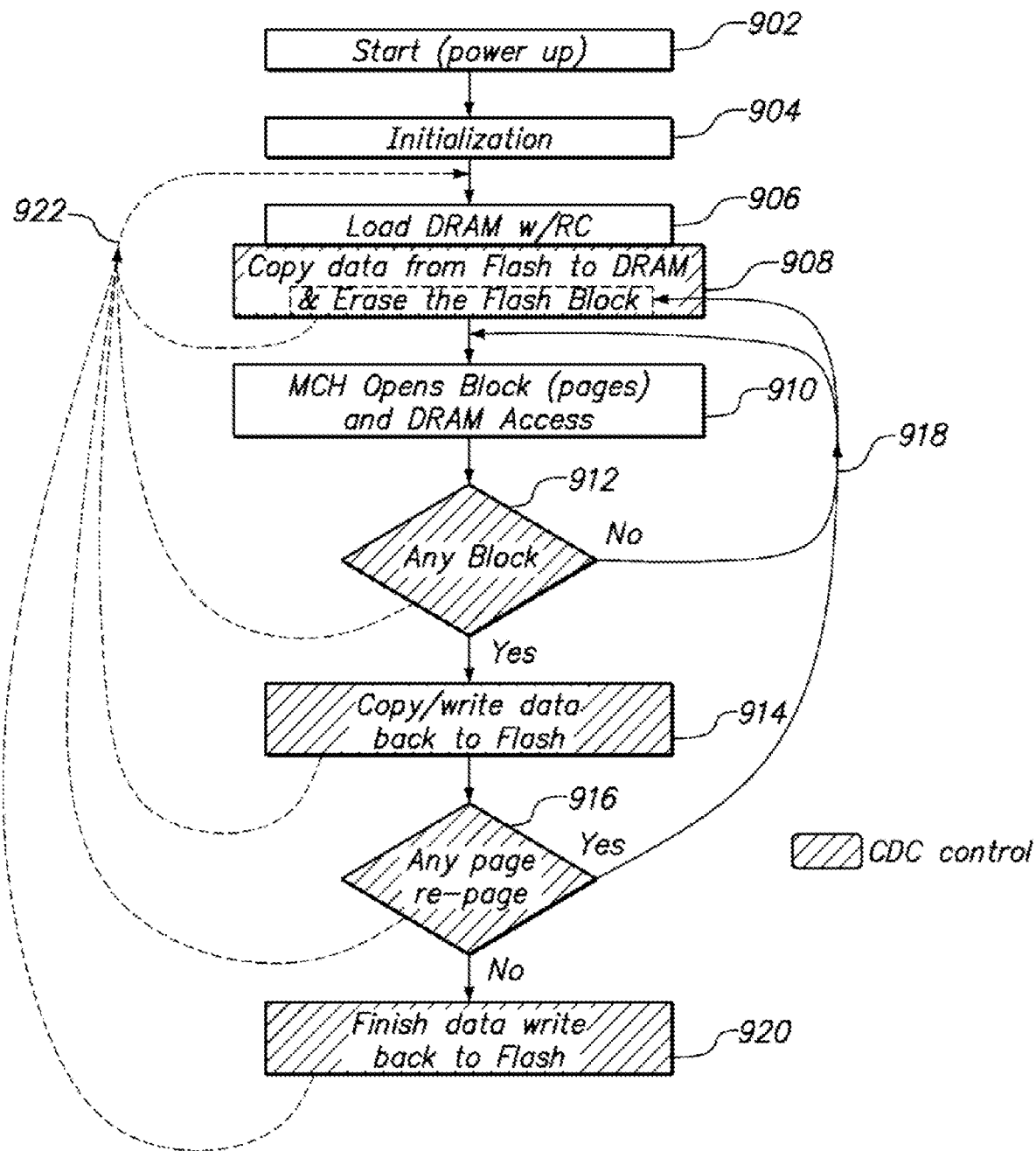


FIG. 9

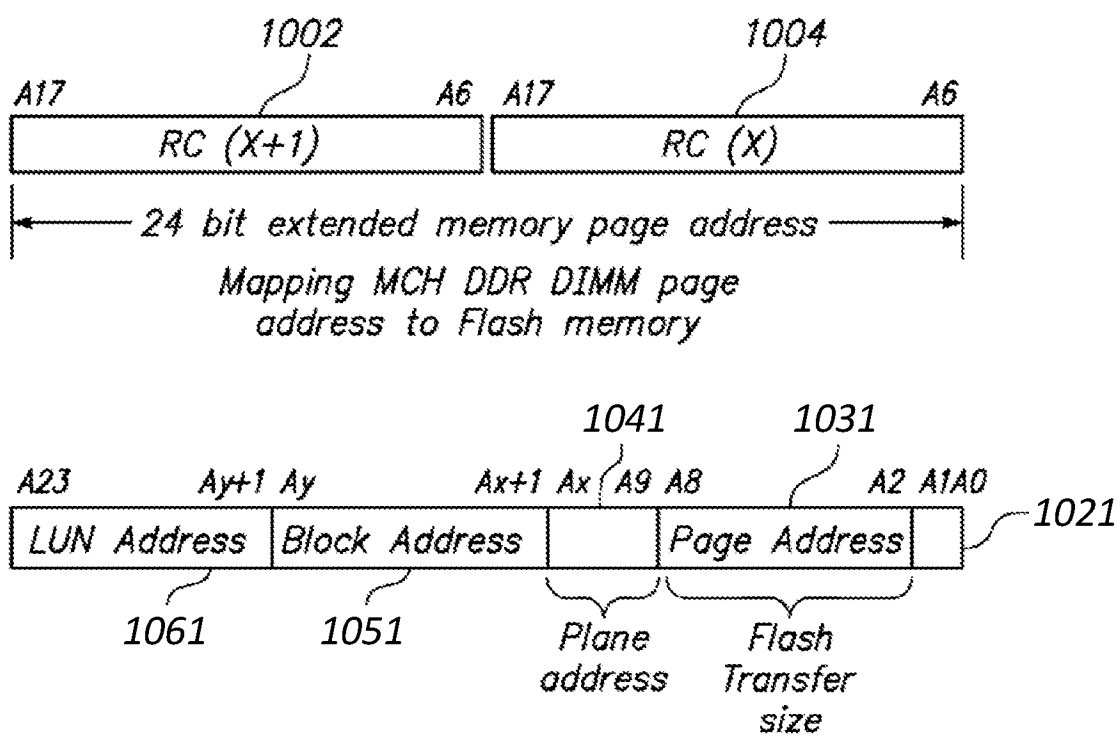


FIG. 10

<i>DRAM density (GB)</i>	<i># of blocks per bank</i>	<i>Flash wr-time to rd-time ratio</i>	<i>Avg block use time (sec)</i>	<i>Flash write time (sec)</i>	<i>Max allowed Closed Blk in queue to be written back to Flash</i>
1	250	55	1.00E-03	2.00E-02	0
1	250	55	1.00E-02	2.00E-02	2
1	250	55	2.00E-02	2.00E-02	5
1	250	55	5.00E-02	2.00E-02	11
2	500	55	1.00E-03	2.00E-02	0
2	500	55	1.00E-02	2.00E-02	5
2	500	55	2.00E-02	2.00E-02	9
2	500	55	5.00E-02	2.00E-02	23
4	1000	55	1.00E-03	2.00E-02	1
4	1000	55	1.00E-02	2.00E-02	9
4	1000	55	2.00E-02	2.00E-02	18
4	1000	55	5.00E-02	2.00E-02	45

FIG. 11

FIG. 12

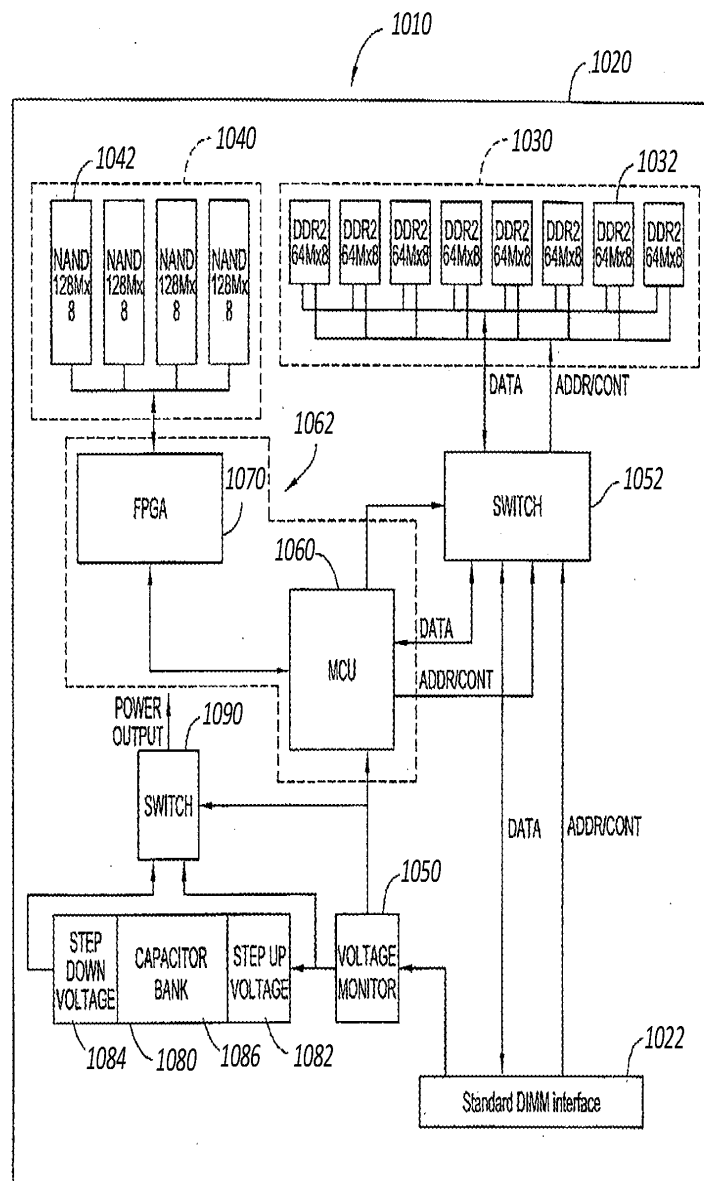


FIG. 13

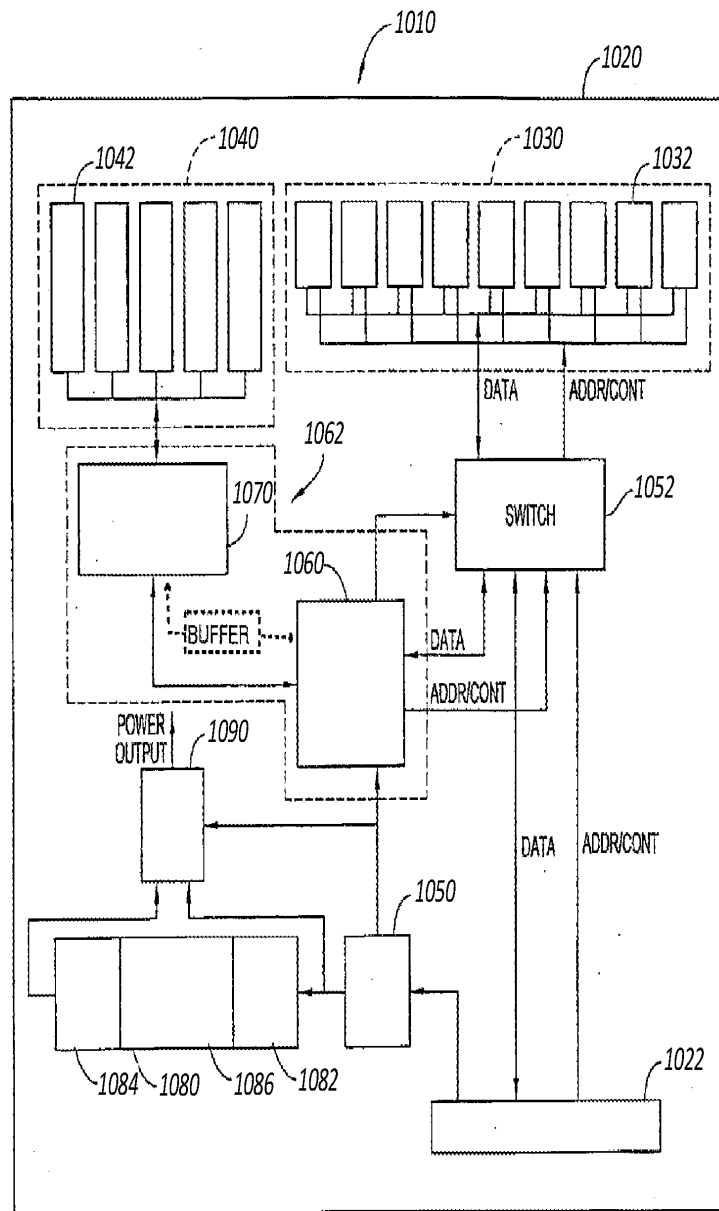
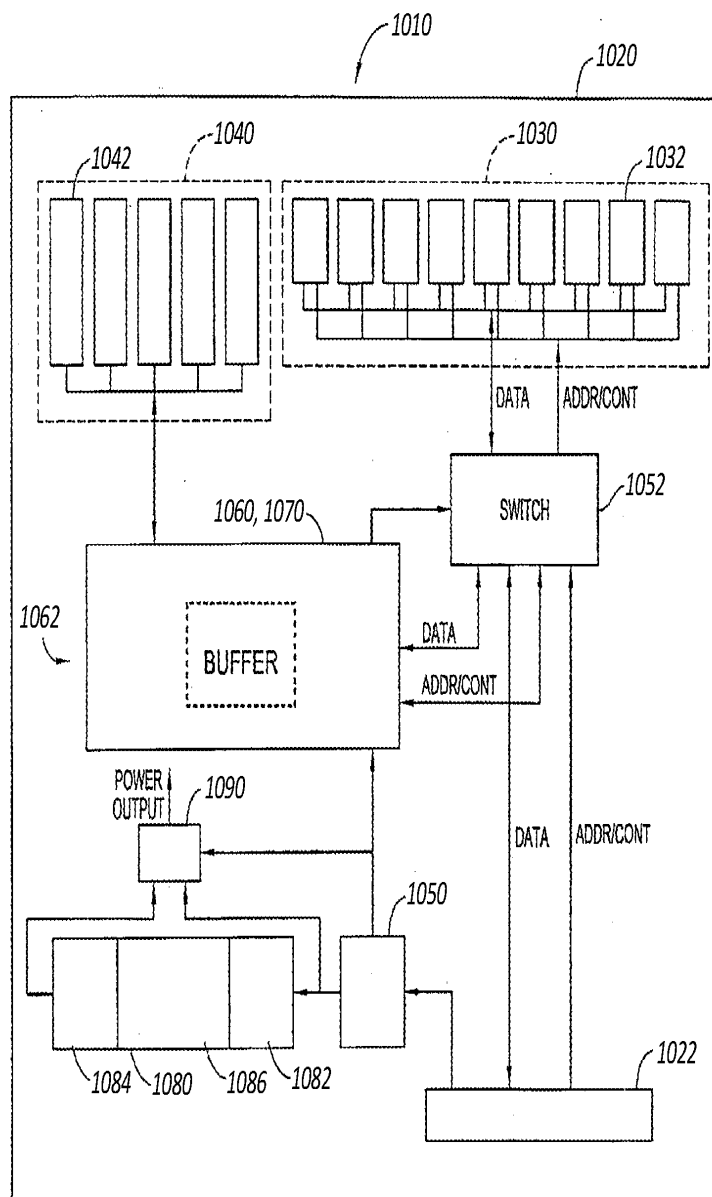


FIG. 14



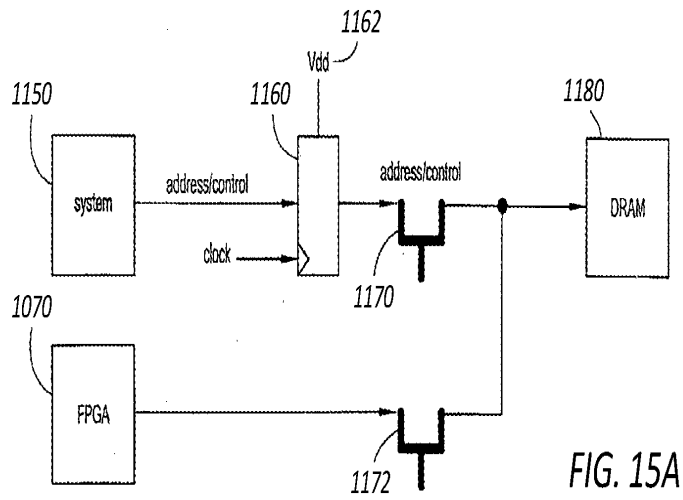


FIG. 15A

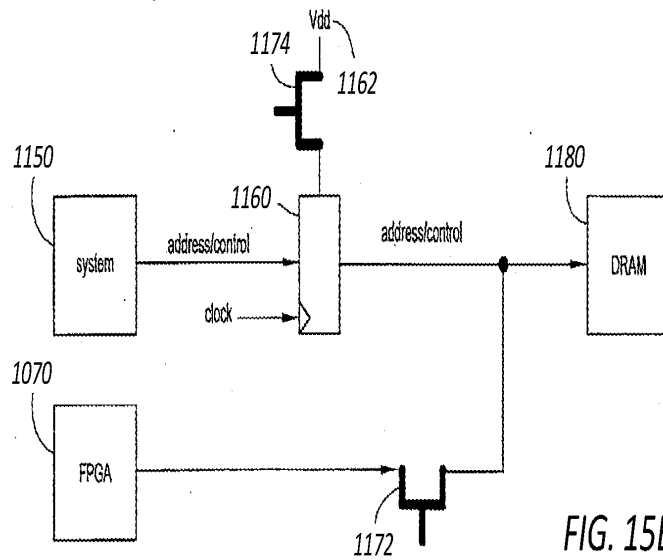


FIG. 15B

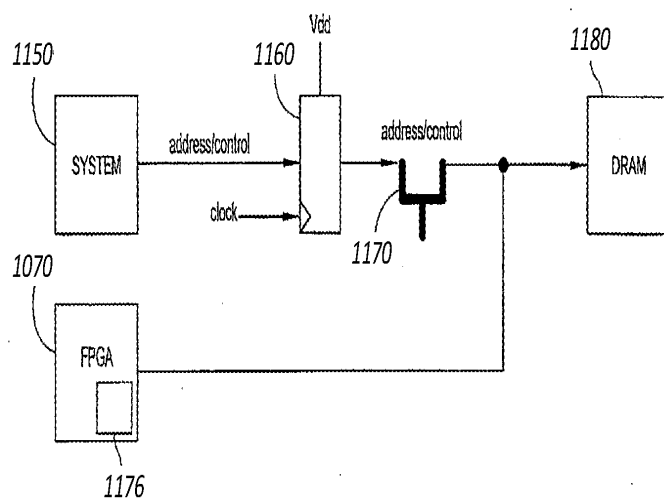


FIG. 15C

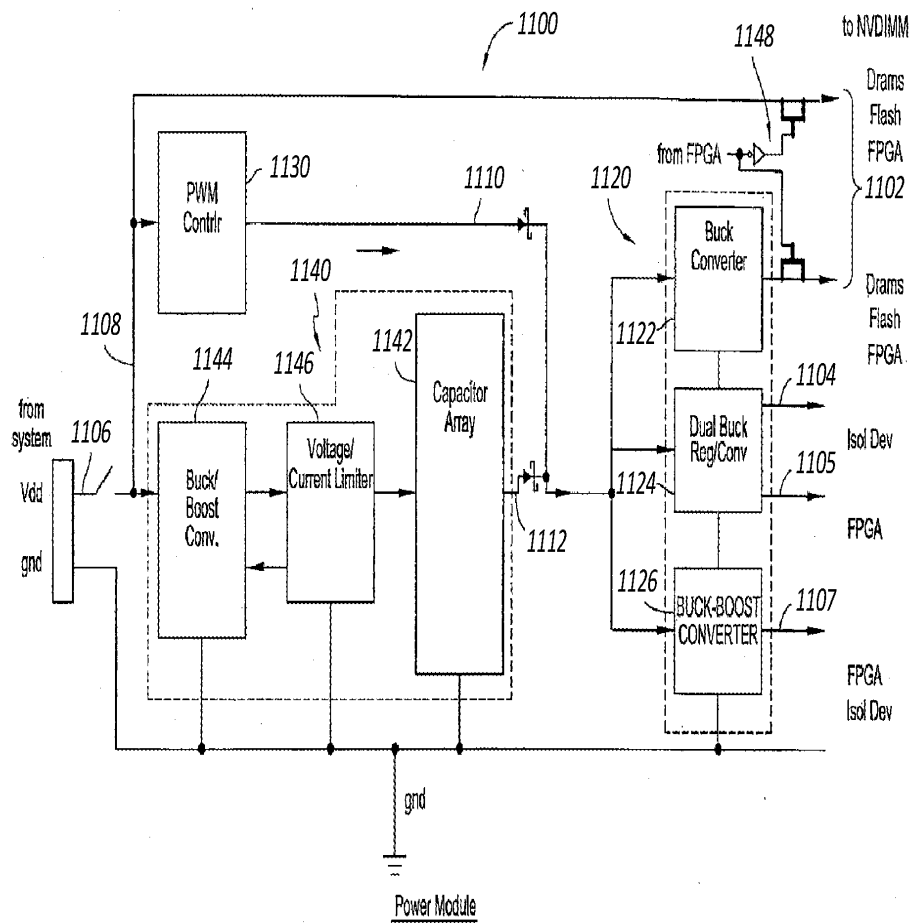


FIG. 16

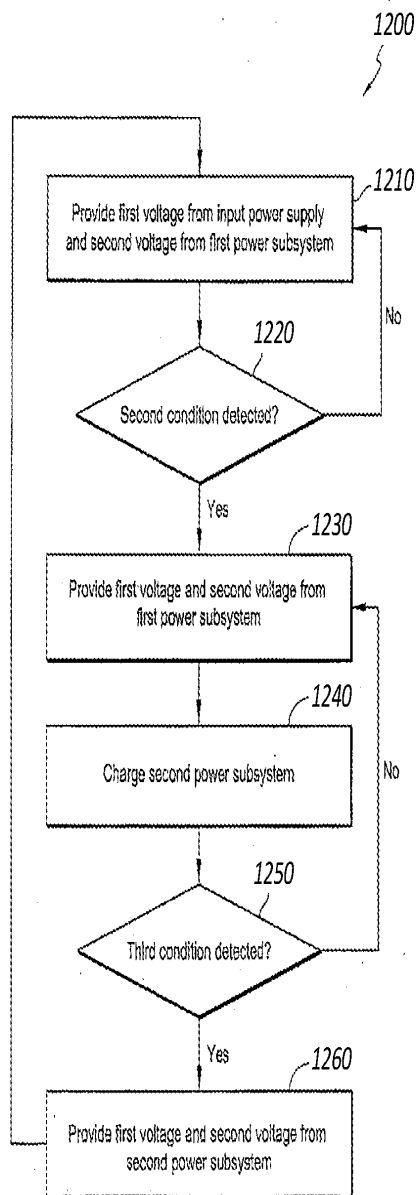


FIG. 17

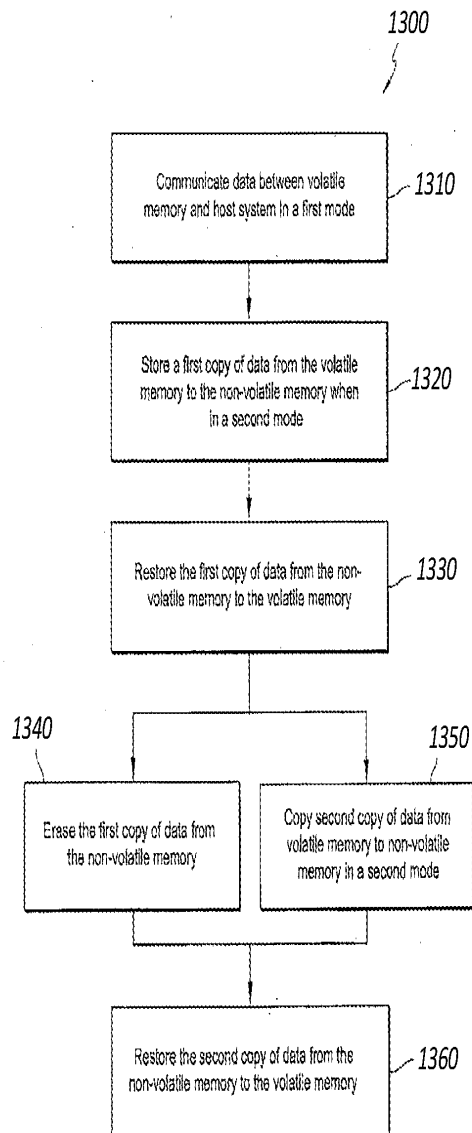
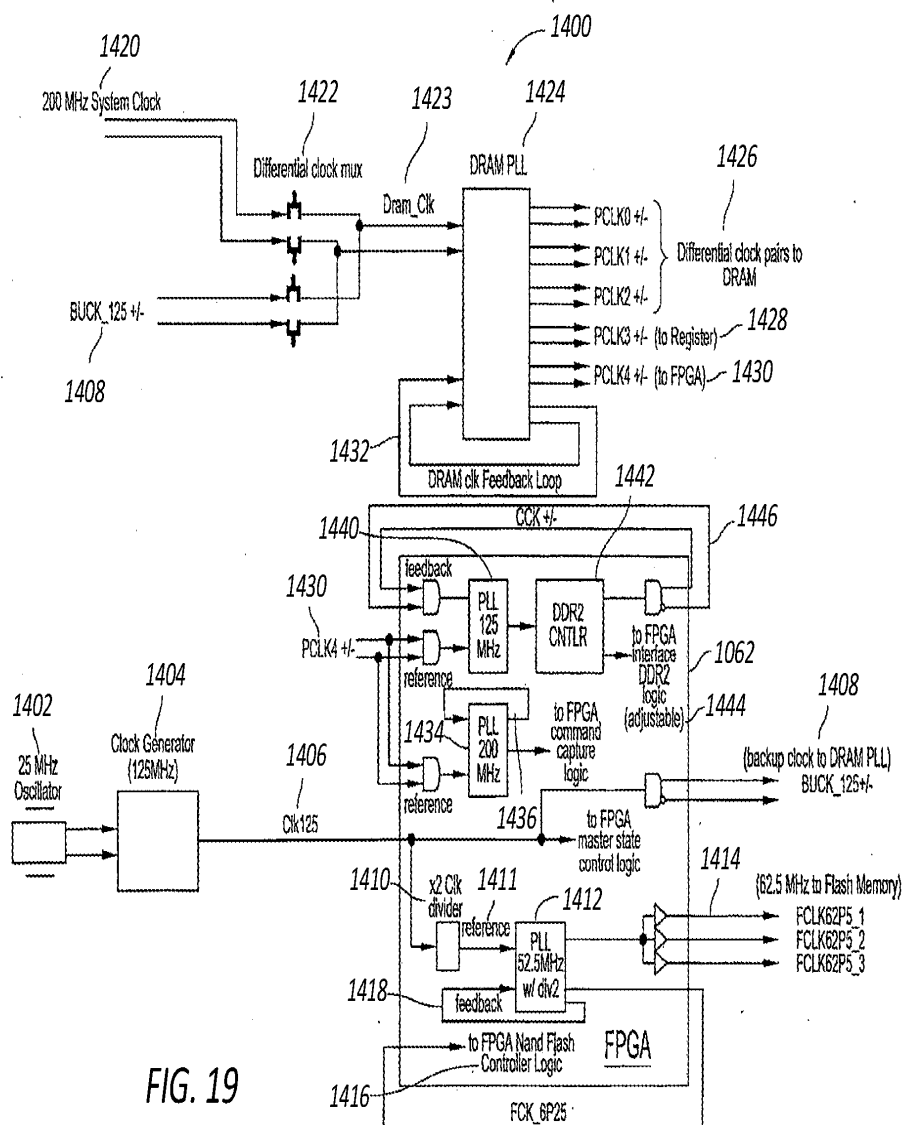


FIG. 18



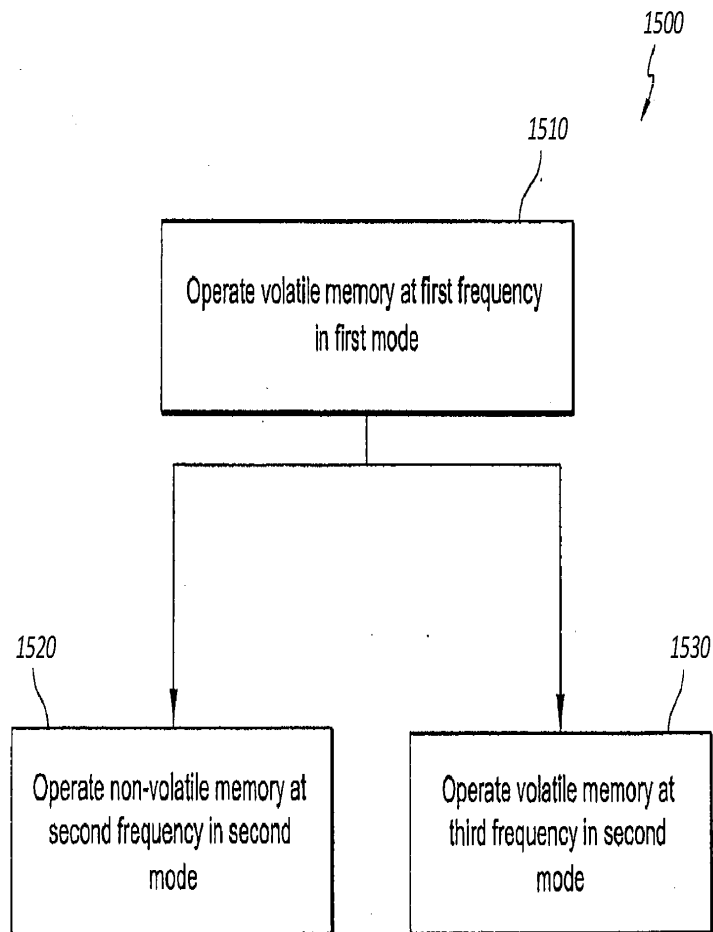


FIG. 20

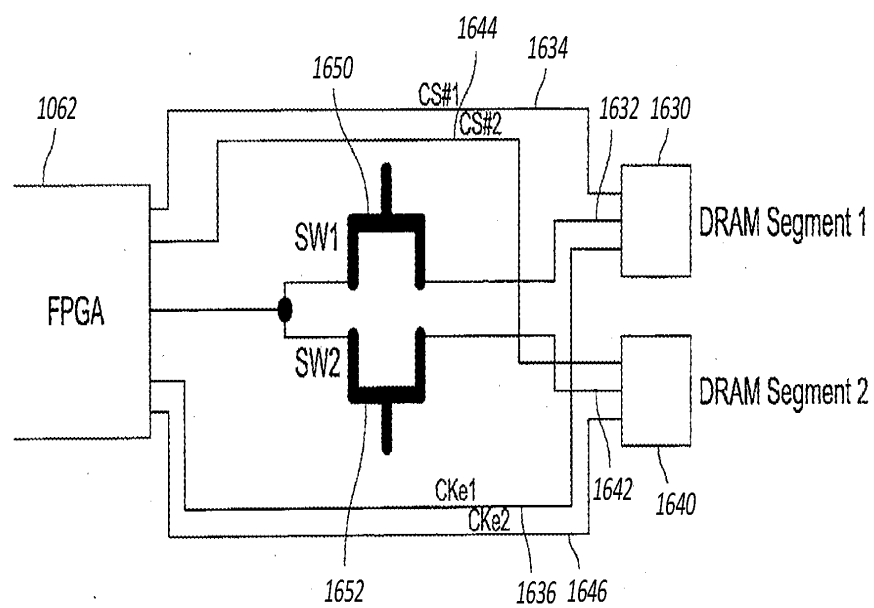


FIG. 21

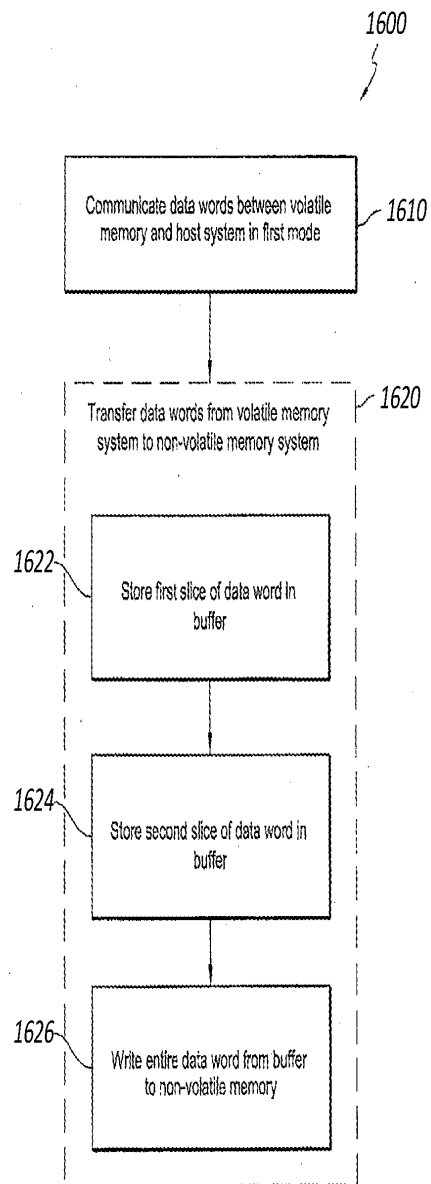


FIG. 22

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DECLARATION (37 CFR 1.63) FOR UTILITY OR DESIGN APPLICATION USING AN APPLICATION DATA SHEET (37 CFR 1.76)

Title of
Invention

FLASH-DRAM HYBRID MEMORY MODULE

As the below named inventor, I hereby declare that:

This declaration
is directed to:

☐

The attached application, or

☒

United States application or PCT international application number 14/489269

filed on September 17, 2014

The above-identified application was made or authorized to be made by me.

I believe that I am the original inventor or an original joint inventor of a claimed invention in the application.

I hereby acknowledge that any willful false statement made in this declaration is punishable under 18 U.S.C. 1001 by fine or imprisonment of not more than five (5) years, or both.

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LEGAL NAME OF INVENTOR

Inventor: Chi-She Chen

Date (Optional): Oct-17-2014

Signature: Chi-She Chen

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LEGAL NAME OF INVENTOR

Inventor: Jeffrey C. Solomon

Date (Optional) : _____

Signature: _____

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LEGAL NAME OF INVENTOR

Inventor: Scott H. Milton

Date (Optional): 10/17/2014

Signature: Scott H. Milton

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This declaration
is directed to:☐

The attached application, or

☒United States application or PCT international application number 14/489269filed on September 17, 2014

The above-identified application was made or authorized to be made by me.

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LEGAL NAME OF INVENTOR

Inventor: Jayesh BhaktaDate (Optional): 9-17-2014Signature: Jayesh Bhakta

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Application Number	TBA
Filing Date	TBA
First Named Inventor	Chi-She Chen
Title	FLASH-DRAM HYBRID MEMORY MODULE
Art Unit	TBA
Examiner Name	TBA
Attorney Docket Number	0016.001000I

SIGNATURE of Applicant or Patent Practitioner

Signature	/Khaled Shami/	Date (Optional)	
Name	Khaled Shami	Registration Number	38,745
Title (if Applicant is a juristic entity)			
Applicant Name (if Applicant is a juristic entity)			

NOTE: This form must be signed in accordance with 37 CFR 1.33. See 37 CFR 1.4(d) for signature requirements and certifications. If more than one applicant, use multiple forms.

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*Total of _____ forms are submitted.

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Electronic Patent Application Fee Transmittal

Application Number:				
Filing Date:				
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE			
First Named Inventor/Applicant Name:	Chi-She Chen			
Filer:	Khaled Shami/Susanh Perez			
Attorney Docket Number:	0016.001000I			
Filed as Large Entity				
Filing Fees for Track I Prioritized Examination - Nonprovisional Application under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
UTILITY APPLICATION FILING	1011	1	320	320
UTILITY SEARCH FEE	1111	1	700	700
UTILITY EXAMINATION FEE	1311	1	800	800
REQUEST FOR PRIORITIZED EXAMINATION	1817	1	4200	4200
Pages:				
Claims:				
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
PUBL. FEE- EARLY, VOLUNTARY, OR NORMAL	1504	1	0	0
PROCESSING FEE, EXCEPT PROV. APPLS.	1830	1	140	140
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				6160

Electronic Acknowledgement Receipt

EFS ID:	42797786
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Susanh Perez
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.0010001
Receipt Date:	24-MAY-2021
Filing Date:	
Time Stamp:	12:48:16
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	CARD
Payment was successfully received in RAM	\$6160
RAM confirmation Number	E20215NC51133944
Deposit Account	602034
Authorized User	Susanh Perez

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

37 CFR 1.16 (National application filing, search, and examination fees)

37 CFR 1.17 (Patent application and reexamination processing fees)

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37 CFR 1.19 (Document supply fees)
 37 CFR 1.20 (Post Issuance fees)
 37 CFR 1.21 (Miscellaneous fees and charges)

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Application Data Sheet	WebADS.pdf	173072	no	9
			024d0527756718ace8c8a6cf42912cad2b8d5f29		
Warnings:					
Information:					
2	TrackOne Request	0016001000I_TrackOneRequestForm_aia0424.pdf	130205	no	2
			f2be939f4d6bd7e584b64396a50033dece7c2cf5		
Warnings:					
Information:					
3	Power of Attorney	Signed_POA.pdf	880737	no	2
			6f585b39d647761dfeedc57b98cfd2a5aa8c777d		
Warnings:					
The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
4		Application__0016001000I.pdf	476233	yes	77
			cbe99cd93ea85fac43989e7379f23180614092d9		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	75	
	Claims		76	76	
	Abstract		77	77	
Warnings:					
Information:					

5	Drawings-only black and white line drawings	Drwgs_0016001000l.pdf	4488651 4c32d20e5adfe5f5d06f6f4363693e2715b8f18c	no	22
Warnings: The page size in the PDF is too large. The pages should be 8.5 x 11 or A4. If this PDF is submitted, the pages will be resized upon entry into the Image File Wrapper and may affect subsequent processing					
Information:					
6	Oath or Declaration filed	Inventors_Oath.pdf	372159 f091bc0e76caeabd5677e65b65d09f9c9b91d709	no	4
Warnings: Information:					
7	Transmittal Letter	POA_Transmittal_0016001000l.pdf	187769 eac6b27617adc227e82c9cf0957012218f329cf4	no	1
Warnings: Information:					
8	Fee Worksheet (SB06)	fee-info.pdf	39956 a9257abd068e08cce3929f6c0af7380317cb7eb5	no	2
Warnings: Information:					
Total Files Size (in bytes):			6748782		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		
<p>The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76.</p> <p>This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.</p>			

Secrecy Order 37 CFR 5.2:

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)
--

Inventor Information:

Inventor 1				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Chi-She		Chen	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Walnut	State/Province	CA	Country of Residence ⁱ US
Mailing Address of Inventor:				
Address 1		944 Crystal Water Lane		
Address 2				
City	Walnut	State/Province	CA	
Postal Code	91789	Country ⁱ	US	
Inventor 2				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Jeffrey	C.	Solomon	
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City	Irvine	State/Province	CA	Country of Residence ⁱ US
Mailing Address of Inventor:				
Address 1		6 Silver Fir		
Address 2				
City	Irvine	State/Province	CA	
Postal Code	92604	Country ⁱ	US	
Inventor 3				
Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Scott	H.	Milton Samsung Electronics Co., Ltd.	

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Residence Information (Select One)		☒ US Residency	☐ Non US Residency	☐ Active US Military Service
City	Irvine	State/Province	CA	Country of Residence ⁱ
US				

Mailing Address of Inventor:

Address 1	49 Statehouse Place			
Address 2				
City	Irvine	State/Province	CA	
Postal Code	92602	Country ⁱ	US	

Inventor 4

Legal Name				
Prefix	Given Name	Middle Name	Family Name	Suffix
	Jayesh		Bhakta	

Residence Information (Select One)		☒ US Residency	☐ Non US Residency	☐ Active US Military Service
City	Cerritos	State/Province	CA	Country of Residence ⁱ
US				

Mailing Address of Inventor:

Address 1	12220 Rose Street			
Address 2				
City	Cerritos	State/Province	CA	
Postal Code	90703	Country ⁱ	US	

All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the **Add** button.

Add

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below.	
For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	151145
Email Address	
	<div>Add Email</div> <div>Remove Email</div>

Application Information:

Title of the Invention	FLASH-DRAM HYBRID MEMORY MODULE		
Attorney Docket Number	0016.001000I	Small Entity Status Claimed	☐
Application Type			
Subject Matter			
Total Number of Drawing Sheets (if any)	22	Suggested Figure for Publication (if any)	

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Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Filing By Reference:

Only complete this section when filing an application by reference under 35 U.S.C. 111(c) and 37 CFR 1.57(a). Do not complete this section if application papers including a specification and any drawings are being filed. Any domestic benefit or foreign priority information must be provided in the appropriate section(s) below (i.e., "Domestic Benefit/National Stage Information" and "Foreign Priority Information").

For the purposes of a filing date under 37 CFR 1.53(b), the description and any drawings of the present application are replaced by this reference to the previously filed application, subject to conditions and requirements of 37 CFR 1.57(a).

Application number of the previously filed application	Filing date (YYYY-MM-DD)	Intellectual Property Authority or Country

Publication Information:

☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

☐ **Request Not to Publish.** I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Either enter Customer Number or complete the Representative Name section below. If both sections are completed the customer Number will be used for the Representative Information during processing.

Please Select One:						☒ Customer Number	☐ US Patent Practitioner	☐ Limited Recognition (37 CFR 11.9)
Customer Number		151145						
Prefix	Given Name	Middle Name	Family Name	Suffix	<div>Remove</div>			
Registration Number								
Prefix	Given Name	Middle Name	Family Name	Suffix	<div>Remove</div>			
Registration Number								
Additional Representative Information blocks may be generated within this form by selecting the Add button.								

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, 365(c), or 386(c) or indicate National Stage entry from a PCT application. Providing benefit claim information in the Application Data Sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78.

When referring to the current application, please leave the "Application Number" field blank.

Prior Application Status		Pending		Remove	
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
	Continuation of		17138766	2020-12-30	

Prior Application Status		Pending		Remove	
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
17138766	Continuation of		15934416	2018-03-23	

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
15934416	Continuation of	14840865	2015-08-31	9928186	2018-03-27

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14840865	Continuation of	14489269	2014-09-17	9158684	2015-10-13

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
14489269	Continuation of	13559476	2012-07-26	8874831	2014-10-28

Prior Application Status		Pending		Remove	
Application Number	Continuity Type		Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)	
13559476	Claims benefit of provisional		61512871	2011-07-28	

Prior Application Status		Patented		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)	Patent Number	Issue Date (YYYY-MM-DD)
13559476	Continuation in part of	12240916	2008-09-29	8301833	2012-10-30

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Prior Application Status	Abandoned	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12240916	Continuation of	12131873	2008-06-02
Prior Application Status	Pending	Remove	
Application Number	Continuity Type	Prior Application Number	Filing or 371(c) Date (YYYY-MM-DD)
12131873	Claims benefit of provisional	60941586	2007-06-01
Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the Add button.			

Foreign Priority Information:

This section allows for the applicant to claim priority to a foreign application. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55. When priority is claimed to a foreign application that is eligible for retrieval under the priority document exchange program (PDX) the information will be used by the Office to automatically attempt retrieval pursuant to 37 CFR 1.55(i)(1) and (2). Under the PDX program, applicant bears the ultimate responsibility for ensuring that a copy of the foreign application is received by the Office from the participating foreign intellectual property office, or a certified copy of the foreign priority application is filed, within the time period specified in 37 CFR 1.55(g)(1).

Application Number	Country ⁱ	Filing Date (YYYY-MM-DD)	Access Code ⁱ (if applicable)
Additional Foreign Priority Data may be generated within this form by selecting the Add button.			

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications

☐ This application (1) claims priority to or the benefit of an application filed before March 16, 2013 and (2) also contains, or contained at any time, a claim to a claimed invention that has an effective filing date on or after March 16, 2013. NOTE: By providing this statement under 37 CFR 1.55 or 1.78, this application, with a filing date on or after March 16, 2013, will be examined under the first inventor to file provisions of the AIA.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76	Attorney Docket Number	0016.001000I
	Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	

Authorization or Opt-Out of Authorization to Permit Access:

When this Application Data Sheet is properly signed and filed with the application, applicant has provided written authority to permit a participating foreign intellectual property (IP) office access to the instant application-as-filed (see paragraph A in subsection 1 below) and the European Patent Office (EPO) access to any search results from the instant application (see paragraph B in subsection 1 below).

Should applicant choose not to provide an authorization identified in subsection 1 below, applicant **must opt-out** of the authorization by checking the corresponding box A or B or both in subsection 2 below.

NOTE: This section of the Application Data Sheet is **ONLY** reviewed and processed with the **INITIAL** filing of an application. After the initial filing of an application, an Application Data Sheet cannot be used to provide or rescind authorization for access by a foreign IP office(s). Instead, Form PTO/SB/39 or PTO/SB/69 must be used as appropriate.

1. Authorization to Permit Access by a Foreign Intellectual Property Office(s)

A. Priority Document Exchange (PDX) - Unless box A in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the European Patent Office (EPO), the Japan Patent Office (JPO), the Korean Intellectual Property Office (KIPO), the State Intellectual Property Office of the People's Republic of China (SIPO), the World Intellectual Property Organization (WIPO), and any other foreign intellectual property office participating with the USPTO in a bilateral or multilateral priority document exchange agreement in which a foreign application claiming priority to the instant patent application is filed, access to: (1) the instant patent application-as-filed and its related bibliographic data, (2) any foreign or domestic application to which priority or benefit is claimed by the instant application and its related bibliographic data, and (3) the date of filing of this Authorization. See 37 CFR 1.14(h)(1).

B. Search Results from U.S. Application to EPO - Unless box B in subsection 2 (opt-out of authorization) is checked, the undersigned hereby **grants the USPTO authority** to provide the EPO access to the bibliographic data and search results from the instant patent application when a European patent application claiming priority to the instant patent application is filed. See 37 CFR 1.14(h)(2).

The applicant is reminded that the EPO's Rule 141(1) EPC (European Patent Convention) requires applicants to submit a copy of search results from the instant application without delay in a European patent application that claims priority to the instant application.

2. Opt-Out of Authorizations to Permit Access by a Foreign Intellectual Property Office(s)

☐ A. Applicant **DOES NOT** authorize the USPTO to permit a participating foreign IP office access to the instant application-as-filed. If this box is checked, the USPTO will not be providing a participating foreign IP office with any documents and information identified in subsection 1A above.

☐ B. Applicant **DOES NOT** authorize the USPTO to transmit to the EPO any search results from the instant patent application. If this box is checked, the USPTO will not be providing the EPO with search results from the instant application.

NOTE: Once the application has published or is otherwise publicly available, the USPTO may provide access to the application in accordance with 37 CFR 1.14.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Applicant Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Applicant 1

If the applicant is the inventor (or the remaining joint inventor or inventors under 37 CFR 1.45), this section should not be completed. The information to be provided in this section is the name and address of the legal representative who is the applicant under 37 CFR 1.43; or the name and address of the assignee, person to whom the inventor is under an obligation to assign the invention, or person who otherwise shows sufficient proprietary interest in the matter who is the applicant under 37 CFR 1.46. If the applicant is an applicant under 37 CFR 1.46 (assignee, person to whom the inventor is obligated to assign, or person who otherwise shows sufficient proprietary interest) together with one or more joint inventors, then the joint inventor or inventors who are also the applicant should be identified in this section.

[Clear](#)

☐ Assignee
☐ Legal Representative under 35 U.S.C. 117
☐ Joint Inventor

☐ Person to whom the inventor is obligated to assign.
☐ Person who shows sufficient proprietary interest

If applicant is the legal representative, indicate the authority to file the patent application, the inventor is:

Name of the Deceased or Legally Incapacitated Inventor:

If the Applicant is an Organization check here. ☒

Organization Name Netlist, Inc.

Mailing Address Information For Applicant:

Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	State/Province	CA
Country ⁱ	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			

Additional Applicant Data may be generated within this form by selecting the Add button.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Assignee Information including Non-Applicant Assignee Information:

Providing assignment information in this section does not substitute for compliance with any requirement of part 3 of Title 37 of CFR to have an assignment recorded by the Office.

Assignee 1			
Complete this section if assignee information, including non-applicant assignee information, is desired to be included on the patent application publication. An assignee-applicant identified in the "Applicant Information" section will appear on the patent application publication as an applicant. For an assignee-applicant, complete this section only if identification as an assignee is also desired on the patent application publication.			
If the Assignee or Non-Applicant Assignee is an Organization check here. ☒			
Organization Name	Netlist, Inc.		
Mailing Address Information For Assignee including Non-Applicant Assignee:			
Address 1	175 Technology Drive		
Address 2	Suite 150		
City	Irvine	State/Province	CA
Country i	US	Postal Code	92618
Phone Number		Fax Number	
Email Address			
Additional Assignee or Non-Applicant Assignee Data may be generated within this form by selecting the Add button.			

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	0016.001000I
		Application Number	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE		

Signature:

NOTE: This Application Data Sheet must be signed in accordance with 37 CFR 1.33(b). **However, if this Application Data Sheet is submitted with the INITIAL filing of the application and either box A or B is not checked in subsection 2 of the "Authorization or Opt-Out of Authorization to Permit Access" section, then this form must also be signed in accordance with 37 CFR 1.14(c).**

This Application Data Sheet **must** be signed by a patent practitioner if one or more of the applicants is a **juristic entity** (e.g., corporation or association). If the applicant is two or more joint inventors, this form must be signed by a patent practitioner, **all** joint inventors who are the applicant, or one or more joint inventor-applicants who have been given power of attorney (e.g., see USPTO Form PTO/AIA/81) on behalf of **all** joint inventor-applicants.

See 37 CFR 1.4(d) for the manner of making signatures and certifications.

Signature	/Khaled Shami/			Date (YYYY-MM-DD)	
First Name	Khaled	Last Name	Shami	Registration Number	38745
Additional Signature may be generated within this form by selecting the Add button.					

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875						Application or Docket Number 17/328,019				
APPLICATION AS FILED - PART I										
(Column 1)		(Column 2)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY				
FOR	NUMBER FILED	NUMBER EXTRA	RATE(\$)	FEE(\$)		RATE(\$)	FEE(\$)			
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A	320			
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A	N/A			N/A	700			
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A	800			
TOTAL CLAIMS (37 CFR 1.16(j))	1	minus 20 = *			OR	x 100 =	0.00			
INDEPENDENT CLAIMS (37 CFR 1.16(h))	1	minus 3 = *				x 480 =	0.00			
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).						0.00			
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))							0.00			
* If the difference in column 1 is less than zero, enter "0" in column 2.			TOTAL			TOTAL	1820			
APPLICATION AS AMENDED - PART II										
(Column 1)		(Column 2)		(Column 3)		SMALL ENTITY		OR OTHER THAN SMALL ENTITY		
AMENDMENT A		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
AMENDMENT B		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE(\$)	ADDITIONAL FEE(\$)		RATE(\$)	ADDITIONAL FEE(\$)
	Total (37 CFR 1.16(i))	*	Minus	**	=	x	=	OR	x	=
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x	=	OR	x	=
	Application Size Fee (37 CFR 1.16(s))							OR		
	FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))							OR		
						TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest found in the appropriate box in column 1.										



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Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
17/328,019	05/24/2021		1820	0016.001000I	1	1

CONFIRMATION NO. 6552

FILING RECEIPT



0000000125973892

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

Date Mailed: 06/02/2021

Receipt is acknowledged of this non-provisional utility patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF FIRST INVENTOR, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection.

Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please submit a written request for a corrected Filing Receipt, including a properly marked-up ADS showing the changes with strike-through for deletions and underlining for additions. If you received a "Notice to File Missing Parts" or other Notice requiring a response for this application, please submit any request for correction to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections provided that the request is grantable.

Inventor(s)

Chi-She Chen, Walnut, CA;
Jeffrey C. Solomon, Irvine, CA;
Scott H. Milton, Irvine, CA;
Jayesh Bhakta, Cerritos, CA;

Applicant(s)

Netlist, Inc., Irvine, CA

Assignment For Published Patent Application

Netlist, Inc., Irvine, CA

Power of Attorney: The patent practitioners associated with Customer Number 151145

Domestic Priority data as claimed by applicant

This application is a CON of 17/138,766 12/30/2020 PAT 11016918
which is a CON of 15/934,416 03/23/2018
which is a CON of 14/840,865 08/31/2015 PAT 9928186
which is a CON of 14/489,269 09/17/2014 PAT 9158684
which is a CON of 13/559,476 07/26/2012 PAT 8874831
which claims benefit of 61/512,871 07/28/2011
and is a CIP of 12/240,916 09/29/2008 PAT 8301833
which is a CON of 12/131,873 06/02/2008 ABN
which claims benefit of 60/941,586 06/01/2007

Foreign Applications for which priority is claimed (You may be eligible to benefit from the **Patent Prosecution Highway** program at the USPTO. Please see <http://www.uspto.gov> for more information.) - None.

Foreign application information must be provided in an Application Data Sheet in order to constitute a claim to foreign priority. See 37 CFR 1.55 and 1.76.

Permission to Access Application via Priority Document Exchange: Yes

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The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 17/328,019**

Projected Publication Date: 09/09/2021

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Early Publication Request: No

Title

FLASH-DRAM HYBRID MEMORY MODULE

Preliminary Class

Statement under 37 CFR 1.55 or 1.78 for AIA (First Inventor to File) Transition Applications: No

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 6552

APPLICATION NO: 17/328,019

ART UNIT: Unassigned

FILING DATE: 05/024/2021

EXAMINER: Unassigned

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Commissioner:

Applicants respectfully request amendment of this application as directed herein.

Amendments to the Specification begin on page 2.

Amendments to the Claims, if any, are reflected in the Listing of Claims beginning on page 3.

Remarks begin on page 9.

It is not believed that extensions of time are required beyond those that may otherwise be provided for in documents accompanying this paper. However, if additional extensions of time are necessary to prevent abandonment of this Application, then such extensions of time are hereby petitioned under 37 C.F.R. § 1.136(a), and any additional fees required to continue prosecution or appeal of this Application (including issue fee, fees for net addition of claims or forwarding to appeal) are hereby authorized to be charged to our Deposit Account No. 60-2034.

In the Specification

Please amend paragraph [00130] as follows:

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash “mirror” to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is **[[1010]] 10** percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example, **[[1010]] 10** percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)

2. (New) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and a first circuit that is coupled to the plurality of synchronous dynamic random access memory (SDRAM) devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.

3. (New) The memory module of claim 2, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.

4. (New) The memory module of claim 2, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.

5. (New) The memory module of claim 2, further comprising:

a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the predetermined threshold voltage is ten percent below a specified operating voltage.

6. (New) The memory module of claim 2, further comprising:

a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the predetermined threshold voltage is ten percent above a specified operating voltage.

7. (New) The memory module of claim 2, further comprising:

a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

8. (New) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a predetermined threshold voltage, and wherein the predetermined threshold voltage is above a specified operating voltage.

9. (New) The memory module of claim 8, wherein the predetermined threshold voltage is ten percent above the specified operating voltage.

10. (New) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a predetermined threshold voltage, and wherein the

predetermined threshold voltage is below a specified operating voltage.

11. (New) The memory module of claim 10, wherein the predetermined threshold voltage is ten percent below the specified operating voltage.

12. (New) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.

13. (New) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.

14. (New) The memory module of claim 2, wherein the voltage conversion circuit includes at least three buck converters.

15. (New) The memory module of claim 14, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.

16. (New) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages;

a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect a change in the input voltage, wherein, in response to the voltage

monitor detecting a change in the input voltage, the memory module transitions from a first operable state to a second operable state.

17. (New) The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage, and wherein the first predetermined threshold voltage is ten percent above a specified operating voltage, and the second predetermined threshold voltage is ten percent below the specified operating voltage.

18. (New) The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

19. (New) The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.

20. (New) The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.

21. (New) The memory module of claim 16, further comprising:

a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit, wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage, wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion

circuit via the output using the first pre-regulated voltage, and wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.

22. (New) The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.

23. (New) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

a voltage conversion circuit configured to provide a plurality of regulated voltages;

a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting a change in the input voltage.

24. (New) The memory module of claim 23, wherein, in response to the voltage monitor circuit detecting a change in the input voltage, the memory module transitions from a first state of operation to a second state of operation.

25. (New) The memory module of claim 24, wherein, in the first state of operation, the voltage conversion circuit provides the first regulated voltage to the SDRAM devices using a first pre-regulated voltage, and wherein, in the second state of operation, the voltage conversion circuit provides the first regulated voltage to the SDRAM devices using a second pre-regulated voltage.

26. (New) The memory module of claim 23, wherein the voltage monitor circuit is

configured to detect the input voltage being above a first predetermined threshold voltage.

27. (New) The memory module of claim 26, wherein the first predetermined threshold voltage is ten percent above a specified operating voltage.

28. (New) The memory module of claim 23, wherein the voltage monitor circuit is configured to detect the input voltage being below a second predetermined threshold voltage.

29. (New) The memory module of claim 28, wherein the second predetermined threshold voltage is ten percent below a specified operating voltage.

30. (New) The memory module of claim 25, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.

31. (New) The memory module of claim 30, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.

REMARKS

Entry of the foregoing amendment prior to substantive examination is respectfully requested. The pending claims subject to examination are 2 – 31, of which 2, 16, and 23 are independent.

Specification

The specification has been amended in order to correct a minor typographical error. Specifically, the numeral “1010” appearing in paragraph [00130]. Support for this change can be found in ancestor application 12/240,916, from which priority is claimed and whose contents are incorporated in the instant application by reference in their entirety. No new matter has been introduced.

Canceled Claims

Claim 1 has been canceled without prejudice or disclaimer of the subject matter contained therein.

Newly-Added Claims

Claims 2 – 31 have been added to further particularly point out and distinctly claim the subject matter of the claimed arrangement.

Conclusion

In view of the preceding discussion, Applicants respectfully urge that the claims of the present application define patentable subject matter and should be passed to allowance.

If the Examiner believes that a telephone call would help advance prosecution of the present application, the Examiner is kindly invited to call the undersigned attorney at the number below.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

Dated: June 4, 2021

/Khaled Shami/
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Reg. No. 38,745

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Electronic Acknowledgement Receipt

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Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Susanh Perez
Filer Authorized By:	Khaled Shami
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Time Stamp:	20:17:42
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Specification	Substitute_Spec_Annotated_016001000I.pdf	963765 ef6ffe8adf9dadddfedd9133c59e6b6fa04dcb017	no	75

Warnings:

Samsung Electronics Co., Ltd.

Ex. 1052, p. 138

Information:					
2	Specification	Substitute_Spec_Clean_0016001000l.pdf	1024741 138d5fdf9ccfb9975df8227aaf1f4b2ac13925e7	no	75
Warnings:					
Information:					
3		Preliminary_Amendment_FV_0016001000l.pdf	155598 be56600b31b7caef3acaa1e762c6a76e69db9cbb	yes	10
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Preliminary Amendment		1	1	
	Specification		2	2	
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	Applicant Arguments/Remarks Made in an Amendment		9	10	
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SUBSTITUTE SPECIFICATION (ANNOTATED)

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 17/138,766, filed December 30, 2020, titled “Flash-Dram Hybrid Memory”, now U.S. Patent No. 11,016,918, which is a continuation of U.S. Patent Application No. 15/934,416, filed March 23, 2018, titled “Flash-Dram Hybrid Memory Module,” which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled “Non-Volatile Memory Module,” now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

[0002] This application may be considered related to U.S. Patent Application No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed February 5, 2014, which is a continuation of U.S. Patent Application 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Patent 8,677,060, issued

March 18, 2014, which is a continuation of U.S. Patent Application 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed June 28, 2012, now U.S. Patent 8,516,187, issued August 20, 2013, which is a divisional of U.S. Patent Application 12/240,916, titled "Non-Volatile Memory Module," filed September 29, 2008, now U.S. Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007, the contents of which are incorporated by reference herein in their entirety.

[0003] This application may also be considered related to U.S. Patent Application No. 15/000,834, filed January 19, 2016 (abandoned), which is a continuation of U.S. Patent Application No. 14/489,332, filed September 17, 2014, now U.S. Patent No. 9,269,437, which is a continuation of U.S. Patent Application No. 14/173,219, filed February 5, 2014, now U.S. Patent No. 8,904,099, which is a continuation of U.S. Patent Application No. 13/905,048, filed May 29, 2013, now U.S. Patent No. 6,671,243, which is a continuation U.S. Patent Application 13/536,173 above.

[0004] This application may also be considered related to U.S. Patent Application No. 15/924,866, (abandoned), which is a continuation of U.S. Patent Application No. 14/489,281, filed September 17, 2014, now U.S. Patent No. 9,921,762, which is a continuation of U.S. Patent Application No. 13/625,563, filed September 24, 2012, now U.S. Patent No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed September 23, 2011.

TECHNICAL FIELD

[0005] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0006] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0007] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as ‘finance transactions’ (for example, point-of-service, inter-bank transaction, stock market transaction), ‘scientific computation’ (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), ‘medical diagnostics’ (for example, diagnostics based on the fuzzy logic, medical data processing), ‘simple information sharing and searching’ (for example, web search, retail store website, company home page), ‘email’ (information distribution and archive), ‘security service’, ‘entertainment’ (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high

speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0008] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0009] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM. The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a

data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MB/s for the EcoRAM vs. 104MB/s for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™, which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0010] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0011] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash

DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0012] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

[0013] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0014] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0015] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

[0016] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0017] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0018] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0019] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0020] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0021] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0022] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0023] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0024] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0025] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0026] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0027] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0028] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

[0029] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0030] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0031] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0032] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0033] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0034] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0035] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0036] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0037] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0038] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0039] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0040] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0041] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0042] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0043] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0044] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0045] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0046] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0047] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0048] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0049] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0050] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0051] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0052] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0053] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0054] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0055] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0056] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0057] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0059] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0060] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0061] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0062] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0063] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0064] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0065] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0066] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0067] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0068] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0069] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

[0070] Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to

allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

[0071] Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

[0072] Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0073] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0074] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. 12 is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. 13 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. 14 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. 15A-15C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. 16 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

FIG. 17 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. 18 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. 19 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. 20 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. 22 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0075] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to

implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0076] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0077] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only

Memory), EEPROM (Electrically Erasable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0078] The term “exemplary” where used herein is intended to mean “serving as an example, instance or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments.

[0079] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0080] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0081] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0082] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or

commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0083] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0084] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0085] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400' supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then

the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0086] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0087] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0088] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory

module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0089] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In

the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0090] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0091] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH

510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0092] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0093] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the

DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0094] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0095] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate

and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0096] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0097] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or

provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510.

[0098] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0099] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[00100] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[00101] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash-DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[00102] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 506 and the other for the DRAM memory DRAM 508. The MCH treats the DRAM 508 and Flash 506 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash 506 and DRAM 508 allows for direct data transfer to occur between the Flash 506 and the DRAM 508 in response to control information from Ctrl 502. In this embodiment, this data transfer mechanism provides direct support for executing commands from

the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 506 to the DRAM 508. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[00103] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[00104] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[00105] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a

first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[00106] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[00107] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[00108] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502

monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00109] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1061

field, a Block address 1051 field, a Plane address 1041, a Page address 1031, and a group of least significant address bits A_0A_1 1021. The Plane address 1041 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00110] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00111] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400 μ s, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash

memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00112] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

$$((\text{\#of blocks per bank})/(\text{ratio of 'Flash_block_write_time' to 'Flash_read_time'})) * (\text{Block usage time})/(\text{'Flash_block_write_time'})$$

[00113] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00114] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00115] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up

the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[00116] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[00117] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor

array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[00118] In certain embodiments, the power module transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[00119] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[00120] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[00121] FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory

subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.

[00122] In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 1010 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for

example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[00123] In certain preferred embodiments, the memory system 1010 is in electrical communication with the host system. In other embodiments, the memory system 1010 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system 1010 can be in communication with a disk controller of a computer system, for example. The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.

[00124] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem 1040 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 1030. In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and

synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00125] In certain embodiments, the second plurality of non-volatile memory elements 1042 comprises one or more flash memory elements. Types of flash memory elements 1042 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. 12, the second memory bank 1040 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 1042. In addition, nonvolatile memory elements 1042 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 1042 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00126] FIG. 13 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 1030 with nine volatile memory elements

1032 and a non-volatile memory subsystem 1040 with five non-volatile memory elements 1042 in accordance with certain embodiments described herein. The additional memory element 1032 of the first memory bank 1030 and the additional memory element 1042 of the second memory bank 1040 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 1030 comprises other numbers of volatile memory elements 1032 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 1040 comprises other numbers of nonvolatile memory elements 1042 (e.g., 2, 3, more than 5).

[00127] Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one

embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.

[00128] In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system.

[00129] In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one

or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150.

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash “mirror” to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is ~~1010~~ 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example,

~~1010~~ **10** percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[00131] As schematically illustrated by FIGS. 12 and 13, in certain embodiments, the controller 1062 may comprise a microcontroller unit (MCU) 1060 and a logic element 1070. In certain embodiments, the MCU 1060 provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 and the nonvolatile memory subsystem 1040. The MCU 1060 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. 12 and 13, the logic element 1070 of certain embodiments is in electrical communication with the non-volatile memory subsystem 1040 and the MCU 1060. The logic element 1070 can provide signal level translation between the volatile memory elements 1032 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 1042 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 1070 is also programmed to perform address/address translation between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 1042 because of their superior read speed and compact structure.

[00132] The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the

volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[00133] The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.

[00134] The isolation or operational decoupling of the volatile memory subsystem 1030 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 1010 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 1030. For example, in one embodiment during such periods of operation, the controller 1062 and the nonvolatile memory subsystem 1040 do not add a significant capacitive load to the volatile memory system 1030 when the memory system 1010 is in the first state. In certain such embodiments, the capacitive load of the controller 1062 and the non-volatile memory subsystem 1040 do not significantly affect the signals propagating between the volatile memory subsystem 1030 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 1052 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 1052 comprises other types of isolation devices.

[00135] Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. In certain embodiments, the memory system 1010 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 1010 enters the second state in response to a trigger condition. In certain embodiments, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory

subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.

[00136] In certain embodiments, the second power supply 1080 does not comprise a battery. Because a battery is not used, the second power supply 1080 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. 12-14, the second power supply 1080 comprises a step-up transformer 1082, a step-down transformer 1084, and a capacitor bank 1086 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 1080 is configured to power the volatile memory subsystem 1030 for less than thirty minutes. In certain embodiments, the second power supply 1080 may comprise a battery. For example, in certain embodiments, the second power supply 1080 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 1030 for no more than thirty minutes.

[00137] In certain embodiments, the capacitor bank 1086 of the second power supply 1080 is charged by the first power supply while the memory system 1010 is in the first state. As a result, the second power supply 1080 is fully charged when the memory system 1010 enters the second state. The memory system 1010 and the second power supply 1080 may be located on the same printed circuit board 1020. In other embodiments, the second power supply 1080 may not be on

the same printed circuit board 1020 and may be tethered to the printed circuit board 1020, for example.

[00138] When operating in the first state, in certain embodiments, the step-up transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the step-down transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. 12-14, the memory module 1010 further comprises a switch 1090 (e.g., FET switch) that switches power provided to the controller 1062, the volatile memory subsystem 1030, and the non-volatile memory subsystem 1040, between the power from the second power supply 1080 and the power from the first power supply (e.g., system power) received via the interface 1022. For example, the switch 1090 may switch from the first power supply to the second power supply 1080 when the voltage monitor 1050 detects a low voltage condition. The switch 1090 of certain embodiments advantageously ensures that the volatile memory elements 1032 and non-volatile memory elements 1042 are powered long enough for the data to be transferred from the volatile memory elements 1032 and stored in the non-volatile memory elements 1042. In certain embodiments, after the data transfer is complete, the switch 1090 then switches back to the first power supply and the controller 1062 transmits a signal to the at least one circuit 1052 to operatively decouple the controller 1062 from the volatile memory subsystem 1030, such that the memory system 1010 reenters the first state.

[00139] When the memory system 1010 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 via the

controller 1062. The host system can then resume accessing the volatile memory subsystem 1030 of the memory module 1010. In certain embodiments, after the memory system 1010 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 1030 rather than the non-volatile memory subsystem 1040 because the volatile memory elements 1032 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 1030 to the nonvolatile memory bank 1040, or from the non-volatile memory bank 1040 to the volatile memory bank 1030, takes less than one minute per GB.

[00140] In certain embodiments, the memory system 1010 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 1010 copies the entire contents of the volatile memory subsystem 1030 into the nonvolatile memory subsystem 1040 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are copied back into the volatile memory subsystem 1030 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 1040 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 1010. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 1010 and can improve the performance of the memory system 1010. In certain other embodiments, the entire contents of the volatile memory subsystem 1030 are not copied into the non-volatile memory subsystem 1040 on each backup operation, but only a partial copy is performed. In certain embodiments, other

management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 1040 are performed in the controller 1062.

[00141] The memory system 1010 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 1030 which then writes the data to non-volatile storage which is not part of the memory system 1010, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 1010 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 1010 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 1010 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 1010 may be operated as a write-through cache or as some other type of cache.

[00142] FIG. 16 schematically illustrates an example power module 1100 of the memory system 1010 in accordance with certain embodiments described herein. The power module 1100 provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. In certain embodiments, the power module 1100 comprises one or more of the components described above with respect to FIG. 12. For example, in certain embodiments, the power module 1100 includes the second power supply 1080 and the switch 1090.

[00143] The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110.

[00144] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106.

[00145] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element

1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120.

[00146] In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.

[00147] In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For

example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142.

[00148] The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate

amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.

[00149] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.

[00150] FIG. 17 is a flowchart of an example method 1200 of providing a first voltage 1102 and a second voltage 1104 to a memory system 1010 including volatile and nonvolatile memory subsystems 1030, 1040. While the method 1200 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-15, other memory systems are also compatible with embodiments of the method 1200. During a first condition, the method 1200

comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 and providing the second voltage 1104 to the memory system 1010 from a first power subsystem in operational block 1210. For example, in one embodiment, the first power subsystem comprises the first power element 1130 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, other first power subsystems are used.

[00151] The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.

[00152] The method 1200 further comprises charging a second power subsystem in operational block 1240. In certain embodiments, the second power subsystem comprises the second power element 1140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 1140 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, some other second power subsystem is used.

[00153] The method 1200 further comprises detecting a third condition in an operational block 1250 and during the third condition, providing the first voltage 1102 and the second

voltage 1104 to the memory system 1010 from the second power subsystem 1140 in an operational block 1260. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 1200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 1140 is charged before detecting the second condition.

[00154] In certain embodiments, the memory system 1010 comprises a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 1010 also comprises a controller 1062 operatively coupled to the volatile memory subsystem 1030 and operatively coupled to the non-volatile memory subsystem 1040. The controller 1062 can be configured to allow data to be communicated between the volatile memory subsystem 1030 and the host system when the memory system 1010 is operating in a first state and to allow data to be communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040 when the memory system 1010 is operating in a second state.

[00155] Although the memory system 1010 having extra storage capacity of the non-volatile memory subsystem 1040 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In various embodiments, there may be at least 200, 300, or 400 percent more

storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In other embodiments, the non-volatile memory subsystem 1040 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 1030. In some embodiments, the non-volatile memory subsystem 1040 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 1030. In one embodiment, the non-volatile memory subsystem 1040 includes less than 100 percent more storage capacity than does the volatile memory subsystem 1030.

[00156] The extra storage capacity of the non-volatile memory subsystem 1040 can be used to improve the backup capability of the memory system 1010. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 1040 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem 1040 allows the volatile memory subsystem 1030 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to backup the volatile memory subsystem 1030 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 1030 is copied to a first, previously erased portion of the nonvolatile memory subsystem 1040 via the controller 1062. Since the non-volatile memory subsystem 1040 has more storage capacity than does the volatile memory subsystem 1030, there is a second portion of the non-volatile memory subsystem 1040 which does not have data from the volatile memory subsystem 1030 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 1062 of the memory system 1010 restores the data to the volatile memory subsystem 1030 by copying the backed-up data from the non-volatile memory

subsystem 40 back to the volatile memory subsystem 1030. After the data is restored, the memory system 1010 erases the non-volatile memory subsystem 1040. While the first portion of the non-volatile memory subsystem 1040 is being erased, it may be temporarily inaccessible.

[00157] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 1040 is completely erased, the volatile memory subsystem 1030 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 1040 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 1040, the memory system 1010 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 1040.

[00158] FIG. 18 is a flowchart of an example method 1300 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. In certain embodiments, the non-volatile memory subsystem 1040 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 1300 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-14, the method 1300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 1310, the method 1300 comprises communicating data between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation. The method 1300 further comprises storing a first copy of data from the

volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a first time when the memory system 1010 is in a second mode of operation in an operational block 1320.

[00159] In an operational block 1330, the method 1300 comprises restoring the first copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030. The method 1300 further comprises erasing the first copy of data from the non-volatile memory subsystem 1040 in an operational block 1340. The method further comprises storing a second copy of data from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a second time when the memory system 1010 is in the second mode of operation in an operational block 1350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 1040.

[00160] In some embodiments, the memory system 1010 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 1040. The method 1300 can also include restoring the second copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 in an operational block 1360. The operational blocks of method 1300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem 1030 at operational block 1360 before the first copy of data is completely erased in the operational block 1340.

[00161] FIG. 19 schematically illustrates an example clock distribution topology 1400 of a memory system 1010 in accordance with certain embodiments described herein. The clock

distribution topology 1400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 1010. A clock source 1402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 1402 may feed a clock generator 1404 which provides a clock signal 1406 to the controller 1062, which may be an FPGA. In one embodiment, the clock generator 1404 generates a 125 MHz clock signal 1406. The controller 1062 receives the clock signal 1406 and uses it to clock the controller 1062 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 1062.

[00162] The clock signal 1406 can also be input into a clock divider 1410 which produces a frequency-divided version of the clock signal 1406. In an example embodiment, the clock divider 1410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 1406. A non-volatile memory phase-locked loop (PLL) block 1412 can be included (e.g., in the controller 1062) which distributes a series of clock signals to the non-volatile memory subsystem 1040 and to associated control logic. For example, a series of clock signals 1414 can be sent from the controller 1062 to the non-volatile memory subsystem 1040. Another clock signal 1416 can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem 1040. For example, the clock signal 1416 may clock the portion of the controller 1062 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 1040. A feedback clock signal 1418 is fed back into the non-volatile memory PLL block 1412. In one embodiment, the PLL block 1412 compares the feedback clock 1418 to the reference clock 1411 and varies the phase and frequency of its output until the reference 1411 and feedback 1418 clocks are phase and frequency matched.

[00163] A version of the clock signal 1406 such as the backup clock signal 1408 may be sent from the controller to the volatile memory subsystem 1030. The clock signal 1408 may be, for example, a differential version of the clock signal 1406. As described herein, the backup clock signal 1408 may be used to clock the volatile memory subsystem 1030 when the memory system 1010 is backing up the data from the volatile memory subsystem 1030 into the non-volatile memory subsystem 1040. In certain embodiments, the backup clock signal 1408 may also be used to clock the volatile memory subsystem 1030 when the memory system 1010 is copying the backed-up data back into the volatile memory subsystem 1030 from the nonvolatile memory subsystem 1040 (also referred to as restoring the volatile memory subsystem 1030). The volatile memory subsystem 1030 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the nonvolatile memory subsystem 1040 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 1030 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 1030 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 1010.

[00164] In one embodiment, the backup clock 1408 and the volatile memory system clock signal 1420 are received by a multiplexer 1422, as schematically illustrated by FIG. 19. The multiplexer 1422 can output either the volatile memory system clock signal 1420 or the backup clock signal 1408 depending on the backup state of the memory system 1010. For example, when the memory system 1010 is not performing a backup or restore operation and is

communicating with the host system (e.g., normal operation), the volatile memory system clock signal 1420 may be provided by the multiplexer 422 to the volatile memory PLL block 1424. When the memory system 1010 is performing a backup (or restore) operation, the backup clock signal 1408 may be provided.

[00165] The volatile memory PLL block 1424 receives the volatile memory reference clock signal 1423 from the multiplexer 1422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 1030 and associated control logic. For example, in one embodiment, the PLL block 1424 generates a series of clock signals 1426 which clock the volatile memory elements 1032. A clock signal 1428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal 1430 may be sent to the controller 1062. A feedback clock signal 1432 is fed back into the volatile memory PLL block 1424. In one embodiment, the PLL block 1424 compares the feedback clock signal 1432 to the reference clock signal 1423 and varies the phase and frequency of its output until the reference clock signal 1423 and the feedback clock signal 1432 clocks are phase and frequency matched.

[00166] The clock signal 1430 may be used by the controller 1062 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 1030. For example, control logic in the controller 1062 may be used to control the volatile memory subsystem 1030 during a backup or restore operation. The clock signal 1430 may be used as a reference clock signal for the PLL block 1434 which can generate one or more clocks 1438 used by logic in the controller 1062. For example, the PLL block 1434 may generate one or more clock signals 1438 used to drive logic circuitry associated with

controlling the volatile memory subsystem 1030. In certain embodiments, the PLL block 1434 includes a feedback clock signal 1436 and operates in a similar manner to other PLL blocks described herein.

[00167] The clock signal 1430 may be used as a reference clock signal for the PLL block 1440 which may generate one or more clock signals used by a sub-block 1442 to generate one or more other clock signals 1444. In one embodiment, for example, the volatile memory subsystem 1030 comprises DDR2 SDRAM elements and the sub-block 1442 generates one or more DDR2 compatible clock signals 1444. A feedback clock signal 1446 is fed back into the PLL block 1440. In certain embodiments, the PLL block 1440 operates in a similar manner to other PLL blocks described herein.

[00168] While described with respect to the example embodiment of FIG. 19, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 1030 operates on the volatile memory clock signal 1420 and there is no backup clock signal 1408. In some embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a restore operation and not during a backup operation.

[00169] FIG. 20 is a flowchart of an example method 1500 of controlling a memory system 1010 operatively coupled to a host system. Although described with respect to the memory

system 1010 described herein, the method 1500 is compatible with other memory systems. The memory system 1010 may include a clock distribution topology 1400 similar to the one described above with respect to FIG. 19 or another clock distribution topology. The memory system 1010 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 1040.

[00170] In an operational block 1510, the method 1500 comprises operating the volatile memory subsystem 1030 at a first frequency when the memory system 1010 is in a first mode of operation in which data is communicated between the volatile memory subsystem 1030 and the host system. In an operational block 1520, the method 1500 comprises operating the non-volatile memory subsystem 1040 at a second frequency when the memory system 1010 is in a second mode of operation in which data is communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. The method 1500 further comprises operating the volatile memory subsystem 1030 at a third frequency in an operational block 1530 when the memory system 1010 is in the second mode of operation. In certain embodiments, the memory system 1010 is not powered by a battery when it is in the second mode of operation. The memory system 1010 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

[00171] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 1010.

[00172] FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKe signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062. In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 1630, 1640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice

from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[00173] In certain embodiments, the switches 1650, 1652 can each be selectively switched to selectively operatively couple the data lines 1632, 1642, respectively from the first and second DRAM segments 1630, 1640 to the controller 1062. The chip select lines 1634, 1644 enable the first and second DRAM segments 1630, 1640, respectively, of the volatile memory subsystem 1030, and the self-refresh lines 1636, 1646 toggle the first and second DRAM segments 1630, 1640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[00174] In certain embodiments, when the memory system 1010 is backing up the volatile memory system 1030, data slices from only one of the two DRAM segments 1630, 1640 at a time are sent to the controller 1062. For example, when the first slice is being written to the controller 1062 during a back-up, the controller 1062 sends a signal via the CKe line 1636 to the first DRAM segment 1630 to put the first DRAM segment 1630 in active mode. In certain embodiments, the data slice from the first DRAM segment 1630 for multiple words (e.g., a block of words) is written to the controller 1062 before writing the second data slice from the second DRAM segment 1640 to the controller 1062. While the first data slice is being written to the controller 1062, the controller 1062 also sends a signal via the CKe line 1646 to put the second DRAM segment 1640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 1062, the controller 1062 puts the first DRAM segment 1630

into self-refresh mode by sending a signal via the CKe line 1636 to the first DRAM segment 1640. The controller 1062 also puts the second DRAM segment 1640 into active mode by sending a signal via the CKe line 1646 to the DRAM segment 1640. The second slice for a word or for a block of words is written to the controller 1062. In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.

[00175] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1042 write each backed-up data word to the controller 1062 which writes a first slice of the data word to the volatile memory subsystem 1030 and then a second slice of the data word to the volatile memory subsystem 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00176] FIG. 22 is a flowchart of an example method 1600 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. Although described with respect to the memory system 1010 described herein with respect to FIGS. 12-14 and 21, the method 1600 is compatible with other memory systems. The method 1600 comprises communicating data words between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation in an operational block 1610. For example, the memory

system 1010 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[00177] In an operational block 1620, the method further comprises transferring data words from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 when the memory system 1010 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.

[00178] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The

40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[00179] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[00180] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1040 write each backed-up data word to the controller 1062 which writes a first portion of the data word to the volatile memory subsystem 1030 and then a second portion of the data word to the volatile memory 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00181] The method 1600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem 1030 comprises DRAM elements, only the slice of the DRAM which is currently being accessed

(e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 1600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[00182] In addition, the connection between the DRAM elements and the controller 1062 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 1062 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 1062 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 1030. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[00183] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

SUBSTITUTE SPECIFICATION (CLEAN)

FLASH-DRAM HYBRID MEMORY MODULE

PRIORITY CLAIM

[0001] This application is a continuation of U.S. Patent Application No. 17/138,766, filed December 30, 2020, titled “Flash-Dram Hybrid Memory”, now U.S. Patent No. 11,016,918, which is a continuation of U.S. Patent Application No. 15/934,416, filed March 23, 2018, titled “Flash-Dram Hybrid Memory Module,” which is a continuation of U.S. Patent Application No. 14/840,865, filed August 31, 2015, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 9,928,186, which is a continuation of U.S. Patent Application No. 14/489,269, filed September 17, 2014, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 9,158,684, which is a continuation of U.S. Patent Application No. 13/559,476, filed July 26, 2012, titled “Flash-Dram Hybrid Memory Module,” now U.S. Patent No. 8,874,831, which claims the benefit of U. S. Provisional Patent Application No. 61/512,871, filed July 28, 2011, and is a continuation-in-part of U.S. Patent Application No. 12/240,916, filed September 29, 2008, titled “Non-Volatile Memory Module,” now U.S. Patent No. 8,301,833, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, which claims the benefit of U. S. Provisional Patent Application No. 60/941,586, filed June 1, 2007, the contents of all of which are incorporated herein by reference in their entirety.

[0002] This application may be considered related to U.S. Patent Application No. 14/173,242, titled "Isolation Switching For Backup Of Registered Memory," filed February 5, 2014, which is a continuation of U.S. Patent Application 13/905,053, titled "Isolation Switching For Backup Of Registered Memory," filed May 29, 2013, now U.S. Patent 8,677,060, issued

March 18, 2014, which is a continuation of U.S. Patent Application 13/536,173, titled "Data Transfer Scheme For Non-Volatile Memory Module," filed June 28, 2012, now U.S. Patent 8,516,187, issued August 20, 2013, which is a divisional of U.S. Patent Application 12/240,916, titled "Non-Volatile Memory Module," filed September 29, 2008, now U.S. Patent No. 8,301,833, issued October 30, 2012, which is a continuation of U.S. Patent Application No. 12/131,873, filed June 2, 2008, now abandoned, which claims the benefit of U.S. Provisional Application No. 60/941,586, filed June 1, 2007, the contents of which are incorporated by reference herein in their entirety.

[0003] This application may also be considered related to U.S. Patent Application No. 15/000,834, filed January 19, 2016 (abandoned), which is a continuation of U.S. Patent Application No. 14/489,332, filed September 17, 2014, now U.S. Patent No. 9,269,437, which is a continuation of U.S. Patent Application No. 14/173,219, filed February 5, 2014, now U.S. Patent No. 8,904,099, which is a continuation of U.S. Patent Application No. 13/905,048, filed May 29, 2013, now U.S. Patent No. 6,671,243, which is a continuation U.S. Patent Application 13/536,173 above.

[0004] This application may also be considered related to U.S. Patent Application No. 15/924,866, (abandoned), which is a continuation of U.S. Patent Application No. 14/489,281, filed September 17, 2014, now U.S. Patent No. 9,921,762, which is a continuation of U.S. Patent Application No. 13/625,563, filed September 24, 2012, now U.S. Patent No. 8,904,098, which claims the benefit of U.S. Provisional Application No. 61/583,775, filed September 23, 2011.

TECHNICAL FIELD

[0005] The present disclosure relates generally to computer memory devices, and more particularly, to devices that employ different types of memory devices such as combinations of Flash and random access memories.

BACKGROUND

[0006] As technology advances and the usage of portable computing devices, such as tablet notebook computers, increases, more data needs to be transferred among data centers and to/from end users. In many cases, data centers are built by clustering multiple servers that are networked to increase performance.

[0007] Although there are many types of networked servers that are specific to the types applications envisioned, the basic concept is generally to increase server performance by dynamically allocating computing and storage resources. In recent years, server technology has evolved to be specific to particular applications such as ‘finance transactions’ (for example, point-of-service, inter-bank transaction, stock market transaction), ‘scientific computation’ (for example, fluid dynamic for automobile and ship design, weather prediction, oil and gas expeditions), ‘medical diagnostics’ (for example, diagnostics based on the fuzzy logic, medical data processing), ‘simple information sharing and searching’ (for example, web search, retail store website, company home page), ‘email’ (information distribution and archive), ‘security service’, ‘entertainment’ (for example, video-on-demand), and so on. However, all of these applications suffer from the same information transfer bottleneck due to the inability of a high

speed CPU (central processing unit) to efficiently transfer data in and out of relatively slower speed storage or memory subsystems, particularly since data transfers typically pass through the CPU input/output (I/O) channels.

[0008] The data transfer limitations by the CPU are exemplified by the arrangement shown in FIG. 1, and apply to data transfers between main storage (for example the hard disk (HD) or solid state drive (SSD) and the memory subsystems (for example DRAM DIMM (Dynamic Random Access Memory Dual In-line Memory Module) connected to the front side bus (FSB)). In arrangements such as that of FIG. 1, the SSD/HD and DRAM DIMM of a conventional memory arrangement are connected to the CPU via separate memory control ports (not shown). FIG. 1 specifically shows, through the double-headed arrow, the data flow path between the computer or server main storage (SSD/HD) to the DRAM DIMMs. Since the SSD/HD data I/O and the DRAM DIMM data I/O are controlled by the CPU, the CPU needs to allocate its process cycles to control these I/Os, which may include the IRQ (Interrupt Request) service which the CPU performs periodically. As will be appreciated, the more time a CPU allocates to controlling the data transfer traffic, the less time the CPU has to perform other tasks. Therefore, the overall performance of a server will deteriorate with the increased amount of time the CPU has to expend in performing data transfer.

[0009] There have been various approaches to increase the data transfer throughput rates from/to the main storage, such as SSD/HD, to local storage, such as DRAM DIMM. In one example as illustrated in FIG. 2, EcoRAM™ developed by Spansion provides a storage SSD based system that assumes a physical form factor of a DIMM. The EcoRAM™ is populated with Flash memories and a relatively small memory capacity using DRAMs which serve as a

data buffer. This arrangement is capable of delivering higher throughput rate than a standard SSD based system since the EcoRAM™ is connected to the CPU (central processing unit) via a high speed interface, such as the HT (Hyper Transport) interface, while an SSD/HD is typically connected via SATA (serial AT attachment), USB (universal serial bus), or PCI Express (peripheral component interface express). For example, the read random access throughput rate of EcoRAM™ is near 3GB/s compared with 400MB/s for a NAND SSD memory subsystem using the standard PCI Express-based. This is a 7.5X performance improvement. However, the performance improvement for write random access throughput rate is less than 2X (197MB/s for the EcoRAM vs. 104MB/s for NAND SSD). This is mainly due to the fact that the write speed is cannot be faster than the NAND Flash write access time. Figure 2 is an example of EcoRAM™ using SSD with the form factor of a standard DIMM such that it can be connected to the FSB (front side bus). However, due to the interface protocol difference between DRAM and Flash, an interface device, EcoRAM Accelerator™, which occupies one of the server's CPU sockets is used, and hence further reducing server's performance by reducing the number of available CPU sockets available, and in turn reducing the overall computation efficiency. The server's performance will further suffer due to the limited utilization of the CPU bus due to the large difference in the data transfer throughput rate between read and write operations.

[0010] The EcoRAM™ architecture enables the CPU to view the Flash DIMM controller chip as another processor with a large size of memory available for CPU access.

[0011] In general, the access speed of a Flash based system is limited by four items: the read/write speed of the Flash memory, the CPU's FSB bus speed and efficiency, the Flash

DIMM controller's inherent latency, and the HT interconnect speed and efficiency which is dependent on the HT interface controller in the CPU and Flash DIMM controller chip.

[0012] The published results indicate that these shortcomings are evident in that the maximum throughput rate is 1.56 GBs for the read operation and 104 MBs for the write operation. These access rates are 25% of the DRAM read access speed, and 1.7% of the DRAM access speed at 400MHz operation. The disparity in the access speed (15 to 1) between the read operation and write operation highlight a major disadvantage of this architecture. The discrepancy of the access speed between this type of architecture and JEDEC standard DRAM DIMM is expected to grow wider as the DRAM memory technology advances much faster than the Flash memory.

[0013] Certain types of memory modules comprise a plurality of dynamic random-access memory (DRAM) devices mounted on a printed circuit board (PCB). These memory modules are typically mounted in a memory slot or socket of a computer system (e.g., a server system or a personal computer) and are accessed by the computer system to provide volatile memory to the computer system.

[0014] Volatile memory generally maintains stored information only when it is powered. Batteries have been used to provide power to volatile memory during power failures or interruptions. However, batteries may require maintenance, may need to be replaced, are not environmentally friendly, and the status of batteries can be difficult to monitor.

[0015] Non-volatile memory can generally maintain stored information while power is not applied to the non-volatile memory. In certain circumstances, it can therefore be useful to backup volatile memory using non-volatile memory.

OVERVIEW

[0016] Described herein is a memory module couplable to a memory controller of a host system. The memory module includes a non-volatile memory subsystem, a data manager coupled to the non-volatile memory subsystem, a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager, and a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller.

[0017] Also described herein is a method for managing a memory module by a memory controller, the memory module including volatile and non-volatile memory subsystems. The method includes receiving control information from the memory controller, wherein the control information is received using a protocol of the volatile memory subsystem. The method further includes identifying a data path to be used for transferring data to or from the memory module using the received control information, and using a data manager and a controller of the memory module to transfer data between any two or more of the memory controller, the volatile memory

subsystem, and the non-volatile memory subsystem based on at least one of the received control information and the identified data path.

[0018] Also described herein is a memory module wherein the data manager is operable to control one or more of data flow rate, data transfer size, data buffer size, data error monitoring, and data error correction in response to receiving at least one of a control signal and control information from the controller.

[0019] Also described herein is a memory module wherein the data manager controls data traffic between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on instructions received from the controller.

[0020] Also described herein is a memory module wherein data traffic control relates to any one or more of data flow rate, data transfer size, data buffer size, data transfer bit width, formatting information, direction of data flow, and the starting time of data transfer.

[0021] Also described herein is a memory module wherein the controller configures at least one of a first memory address space of the volatile memory subsystem and a second memory address space of the non-volatile memory subsystem in response to at least one of a received command from the memory controller and memory address space initialization information of the memory module.

[0022] Also described herein is a memory module wherein the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0023] Also described herein is a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0024] Also described herein is a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0025] Also described herein is a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0026] Also described herein is a memory module wherein the non-volatile memory subsystem comprises flash memory.

[0027] Also described herein is a memory module wherein at least one set of data ports is operated by the data manager to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0028] Also described herein is a memory module wherein the data manager and controller are configured to effect data transfer between the memory controller and the non-volatile memory subsystem in response to memory access commands received by the controller from the memory controller.

[0029] Also described herein is a memory module wherein the volatile memory subsystem is operable as a buffer for the data transfer between the memory controller and non-volatile memory.

[0030] Also described herein is a memory module wherein the data manager further includes a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.

[0031] Also described herein is a memory module wherein the data manager further includes a data buffer for buffering data delivered to or from the non-volatile memory subsystem.

[0032] Also described herein is a memory module wherein the controller is operable to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0033] Also described herein is a memory module wherein the controller is configured to effect operation with the host system in accordance with a prescribed protocol.

[0034] Also described herein is a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0035] Also described herein is a memory module wherein the controller is operable to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0036] Also described herein is a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0037] Also described herein is a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0038] Also described herein is a memory module wherein the controller is operable to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0039] Also described herein is a memory module wherein the controller includes a volatile memory control module, a non-volatile memory control module, data manager control module, a command interpreter module, and a scheduler module.

[0040] Also described herein is a memory module wherein commands from the volatile memory control module to the volatile memory subsystem are subordinated to commands from the memory controller to the controller.

[0041] Also described herein is a memory module wherein the controller effects pre-fetching of data from the non-volatile to the volatile memory.

[0042] Also described herein is a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0043] Also described herein is a memory module wherein the controller is operable to initiate a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0044] Also described herein is a memory module wherein, if the closed block is re-opened, the controller is operable to abort the copy operation and to erase the target block from the non-volatile memory subsystem.

[0045] Also described herein is a method for managing a memory module wherein the transfer of data includes a bidirectional transfer of data between the non-volatile and the volatile memory subsystems.

[0046] Also described herein is a method for managing a memory module further comprising operating the data manager to control one or more of data flow rate, data transfer size, data width size, data buffer size, data error monitoring, data error correction, and the starting time of the transfer of data.

[0047] Also described herein is a method for managing a memory module further comprising operating the data manager to control data traffic between the memory controller and at least one of the volatile and non-volatile memory subsystems.

[0048] Also described herein is a method for managing a memory module wherein data traffic control relates to any one or more of data transfer size, formatting information, direction of data flow, and the starting time of the transfer of data.

[0049] Also described herein is a method for managing a memory module wherein data traffic control by the data manager is based on instructions received from the controller.

[0050] Also described herein is a method for managing a memory module further comprising operating the data manager as a bi-directional data transfer fabric with two or more sets of data ports coupled to any one of the volatile and non-volatile memory subsystems.

[0051] Also described herein is a method for managing a memory module wherein at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments.

[0052] Also described herein is a method for managing a memory module wherein each memory segment comprises at least one memory circuit, memory device, or memory die.

[0053] Also described herein is a method for managing a memory module wherein the volatile memory subsystem comprises DRAM memory.

[0054] Also described herein is a method for managing a memory module wherein the non-volatile memory subsystem comprises Flash memory.

[0055] Also described herein is a method for managing a memory module further comprising operating the data ports to independently and/or concurrently transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems.

[0056] Also described herein is a method for managing a memory module further comprising directing transfer of data bi-directionally between the volatile and non-volatile memory subsystems using the data manager and in response to memory access commands received by the controller from the memory controller.

[0057] Also described herein is a method for managing a memory module further comprising buffering the data transferred between the memory controller and non-volatile memory subsystem using the volatile memory subsystem.

[0058] Also described herein is a method for managing a memory module further comprising using the controller to perform one or more of memory address translation, memory address mapping, address domain conversion, memory access control, data error correction, and data width modulation between the volatile and non-volatile memory subsystems.

[0059] Also described herein is a method for managing a memory module further comprising using the controller to effect communication with a host system by the volatile memory subsystem in accordance with a prescribed protocol.

[0060] Also described herein is a method for managing a memory module wherein the prescribed protocol is selected from one or more of DDR, DDR2, DDR3, and DDR4 protocols.

[0061] Also described herein is a method for managing a memory module further comprising using the controller to configure memory space in the memory module based on at least one of a command received from the memory controller, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a first portion of the non-volatile memory subsystem, and a timing value.

[0062] Also described herein is a method for managing a memory module wherein the controller configures the memory space of the memory module using at least a first portion of the volatile memory subsystem and a first portion of the non-volatile memory subsystem, and the controller presents a unified memory space to the memory controller.

[0063] Also described herein is a method for managing a memory module wherein the controller configures the memory space in the memory module using partitioning instructions that are application-specific.

[0064] Also described herein is a method for managing a memory module further comprising using the controller to copy booting information from the non-volatile to the volatile memory subsystem during power up.

[0065] Also described herein is a method for managing a memory module wherein the controller includes a volatile memory control module, the method further comprising generating

commands by the volatile memory control module in response to commands from the memory controller, and transmitting the generated commands to the volatile memory subsystem.

[0066] Also described herein is a method for managing a memory module further comprising pre-fetching of data from the non-volatile memory subsystem to the volatile memory subsystem.

[0067] Also described herein is a method for managing a memory module wherein the pre-fetching is initiated by the memory controller writing an address of requested data into a register of the controller.

[0068] Also described herein is a method for managing a memory module further comprising initiating a copy operation of data of a closed block in the volatile memory subsystem to a target block in the non-volatile memory subsystem.

[0069] Also described herein is a method for managing a memory module further comprising aborting the copy operation when the closed block of the volatile memory subsystem is re-opened, and erasing the target block in the non-volatile memory subsystem.

[0070] Also described herein is a memory system having a volatile memory subsystem, a non-volatile memory subsystem, a controller coupled to the non-volatile memory subsystem, and a circuit coupled to the volatile memory subsystem, to the controller, and to a host system. In a first mode of operation, the circuit is operable to selectively isolate the controller from the volatile memory subsystem, and to selectively couple the volatile memory subsystem to the host system to allow data to be communicated between the volatile memory subsystem and the host system. In a second mode of operation, the circuit is operable to selectively couple the controller to the volatile memory subsystem to

allow data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem using the controller, and the circuit is operable to selectively isolate the volatile memory subsystem from the host system.

[0071] Also described herein is a method for operating a memory system. The method includes coupling a circuit to a host system, a volatile memory subsystem, and a controller, wherein the controller is coupled to a non-volatile memory subsystem. In a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, the circuit is used to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, the circuit is used to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

[0072] Also described herein is a nontransitory computer readable storage medium storing one or more programs configured to be executed by one or more computing devices. The programs, when executing on the one or more computing devices, cause a circuit that is coupled to a host system, to a volatile memory subsystem, and to a controller that is coupled to a nonvolatile memory subsystem, to perform a method in which, in a first mode of operation that allows data to be communicated between the volatile memory subsystem and the host system, operating the circuit to (i) selectively isolate the controller from the volatile memory subsystem, and (ii) selectively couple the volatile memory subsystem to the host system. In a second mode of operation that allows data to be communicated between the volatile memory subsystem and the nonvolatile memory subsystem via the controller, operating the circuit to (i) selectively couple the controller to the volatile memory subsystem, and (ii) selectively isolate the volatile memory subsystem from the host system.

BRIEF DESCRIPTION OF THE DRAWINGS

[0073] The accompanying drawings, which are incorporated into and constitute a part of this specification, illustrate one or more examples of embodiments and, together with the description of example embodiments, serve to explain the principles and implementations of the embodiments.

[0074] In the drawings:

FIG. 1 is a block diagram illustrating the path of data transfer, via a CPU, of a conventional memory arrangement;

FIG. 2 is a block diagram of a known EcoRAM™ architecture;

FIGS. 3A and 3B are block diagrams of a non-volatile memory DIMM or NVDIMM;

FIGS. 4A and 4B are block diagrams of a Flash-DRAM hybrid DIMM or FDHDIMM;

FIG. 5A is a block diagram of a memory module 500 in accordance with certain embodiments described herein;

FIG. 5B is a block diagram showing some functionality of a memory module such as that shown in FIG. 5A;

FIG. 6 is a block diagram showing some details of the data manager (DMgr);

FIG. 7 is a functional block diagram of the on-module controller (CDC);

FIG. 8A is a block diagram showing more details of the prior art Flash-DRAM hybrid DIMM (FDHDIMM) of FIGS. 4A and 4B;

FIG. 8B is a block diagram of a Flash-DRAM hybrid DIMM (FDHDIMM) in accordance with certain embodiments disclosed herein;

FIG. 9 is a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM;

FIG. 10 is a block diagram showing an example of mapping of DRAM address space to Flash memory address space; and

FIG. 11 is a table showing estimates of the maximum allowed closed blocks in a queue to be written back to Flash memory for different DRAM densities using various average block use time.

FIG. 12 is a block diagram of an example memory system compatible with certain embodiments described herein.

FIG. 13 is a block diagram of an example memory module with ECC (error-correcting code) having a volatile memory subsystem with nine volatile memory elements and a non-volatile memory subsystem with five non-volatile memory elements in accordance with certain embodiments described herein.

FIG. 14 is a block diagram of an example memory module having a microcontroller unit and logic element integrated into a single device in accordance with certain embodiments described herein.

FIGS. 15A-15C schematically illustrate example embodiments of memory systems having volatile memory subsystems comprising registered dual in-line memory modules in accordance with certain embodiments described herein.

FIG. 16 schematically illustrates an example power module of a memory system in accordance with certain embodiments described herein.

FIG. 17 is a flowchart of an example method of providing a first voltage and a second voltage to a memory system including volatile and non-volatile memory subsystems.

FIG. 18 is a flowchart of an example method of controlling a memory system operatively coupled to a host system and which includes at least 100 percent more storage capacity in non-volatile memory than in volatile memory.

FIG. 19 schematically illustrates an example clock distribution topology of a memory system in accordance with certain embodiments described herein.

FIG. 20 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including operating a volatile memory subsystem at a reduced rate in a back-up mode.

FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments of a volatile memory subsystem of a memory system to a controller of the memory system.

FIG. 22 is a flowchart of an example method of controlling a memory system operatively coupled to a host system, the method including backing up and/or restoring a volatile memory subsystem in slices.

DESCRIPTION OF EXAMPLE EMBODIMENTS

[0075] Example embodiments are described herein in the context of a system of computers, servers, controllers, memory modules, hard disk drives and software. Those of ordinary skill in the art will realize that the following description is illustrative only and is not intended to be in any way limiting. Other embodiments will readily suggest themselves to such skilled persons having the benefit of this disclosure. Reference will now be made in detail to

implementations of the example embodiments as illustrated in the accompanying drawings. The same reference indicators will be used to the extent possible throughout the drawings and the following description to refer to the same or like items.

[0076] In the interest of clarity, not all of the routine features of the implementations described herein are shown and described. It will, of course, be appreciated that in the development of any such actual implementation, numerous implementation-specific decisions must be made in order to achieve the developer's specific goals, such as compliance with application- and business-related constraints, and that these specific goals will vary from one implementation to another and from one developer to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of engineering for those of ordinary skill in the art having the benefit of this disclosure.

[0077] In accordance with this disclosure, the components, process steps, and/or data structures described herein may be implemented using various types of operating systems, computing platforms, computer programs, and/or general purpose machines. In addition, those of ordinary skill in the art will recognize that devices of a less general purpose nature, such as hardwired devices, field programmable gate arrays (FPGAs), application specific integrated circuits (ASICs), or the like, may also be used without departing from the scope and spirit of the inventive concepts disclosed herein. Where a method comprising a series of process steps is implemented by a computer or a machine and those process steps can be stored as a series of instructions readable by the machine, they may be stored on a tangible medium such as a computer memory device (e.g., ROM (Read Only Memory), PROM (Programmable Read Only

Memory), EEPROM (Electrically Erasable Programmable Read Only Memory), Flash memory, Jump Drive, and the like), magnetic storage medium (e.g., tape, magnetic disk drive, and the like), optical storage medium (e.g., CD-ROM, DVD-ROM, paper card, paper tape and the like) and other types of program memory.

[0078] The term “exemplary” where used herein is intended to mean “serving as an example, instance or illustration.” Any embodiment described herein as “exemplary” is not necessarily to be construed as preferred or advantageous over other embodiments.

[0079] Disclosed herein are arrangements for improving memory access rates and addressing the high disparity (15 to 1 ratio) between the read and write data throughput rates. In one arrangement, a Flash-DRAM-hybrid DIMM (FDHDIMM) with integrated Flash and DRAM is used. Methods for controlling such an arrangement are described.

[0080] In certain embodiments, the actual memory density (size or capacity) of the DIMM and/or the ratio of DRAM memory to Flash memory are configurable for optimal use with a particular application (for example, POS, inter-bank transaction, stock market transaction, scientific computation such as fluid dynamics for automobile and ship design, weather prediction, oil and gas expeditions, medical diagnostics such as diagnostics based on the fuzzy logic, medical data processing, simple information sharing and searching such as web search, retail store website, company home page, email or information distribution and archive, security service, and entertainment such as video-on-demand).

[0081] In certain embodiments, the device contains a high density Flash memory with a low density DRAM, wherein the DRAM is used as a data buffer for read/write operation. The Flash serves as the main memory. Certain embodiments described herein overcome the needs of having a long separation period between an Activate command (may be referred to as RAS) and a corresponding read or write command (may be referred to as first CAS command).

[0082] In accordance with one embodiment, described with reference to FIGS. 3A and 3B, a memory system 300 includes a non-volatile (for example Flash) memory subsystem 302 and a volatile (for example DRAM) memory subsystem 304. The examples of FIGS. 3A and 3B are directed to architectures of a non-volatile DIMM (NVDIMM) NVDIMM system that may use a power subsystem (not shown) that can include a battery or a capacitor as a means for energy storage to copy DRAM memory data into Flash memory when power loss occurs, is detected, or is anticipated to occur during operation. When normal power is restored, a restore NVDIMM operation is initiated and the data stored in the Flash memory is properly restored to the DRAM memory. In this architecture, the density of the Flash is about the same as the DRAM memory size or within a few multiples, although in some applications it may be higher. This type of architecture may also be used to provide non-volatile storage that is connected to the FSB (front side bus) to support RAID (Redundant Array of Independent Disks) based systems or other type of operations. An NVDIMM controller 306 receives and interprets commands from the system memory controller hub (MCH). The NVDIMM controller 306 control the NVDIMM DRAM and Flash memory operations. In FIG. 3A, the DRAM 304 communicates data with the MCH, while an internal bus 308 is used for data transfer between the DRAM and Flash memory subsystems. In FIG. 3B, the NVDIMM controller 306' of NVDIMM 300' monitors events or

commands and enables data transfer to occur in a first mode between the DRAM 304' and Flash 302' or in a second mode between the DRAM and the MCH.

[0083] In accordance with one embodiment, a general architecture for a Flash and DRAM hybrid DIMM (FDHDIMM) system 400 is shown in FIG. 4A. The FDHDIMM interfaces with an MCH (memory controller hub) to operate and behave as a high density DIMM, wherein the MCH interfaces with the non-volatile memory subsystem (for example Flash) 402 is controlled by an FDHDIMM controller 404. Although the MCH interfaces with the Flash via the FDHDIMM controller, the FDHDIMM overall performance is governed by the Flash access time. The volatile memory subsystem (for example DRAM) 406 is primarily used as a data buffer or a temporary storage location such that data from the Flash memory 402 is transferred to the DRAM 406 at the Flash access speed, and buffered or collected into the DRAM 406, which then transfers the buffered data to the MCH based on the access time of DRAM. Similarly, when the MCH transfers data to the DRAM 406, the FDHDIMM controller 404 manages the data transfer from the DRAM 406 to the Flash 402. Since the Flash memory access speed (both read and write) is relatively slower than DRAM, (e.g. for example a few hundred microseconds for read access), the average data throughput rate of FDHDIMM 400 is limited by the Flash access speed. The DRAM 406 serves as a data buffer stage that buffers the MCH read or write data. Thus, the DRAM 406 serves as a temporary storage for the data to be transferred from/to the Flash 402. Furthermore, in accordance with one embodiment, the MCH recognizes the physical density of an FDHDIMM operating as a high density DIMM as the density of Flash alone.

[0084] In accordance with one embodiment, a read operation can be performed by the MCH by sending an activate command (may be simply referred to as RAS, or row address strobe) to the FDHDIMM 400 to conduct a pre-fetch read data operation from the Flash 402 to the DRAM 406, with the pre-fetch data size being for example a page (1KB or 2KB, or may be programmable to any size). The MCH then sends a read command (may be simply referred to as CAS, or column address strobe) to read the data out input of the DRAM. In this embodiment, the data transfer from Flash to DRAM occurs at Flash access speed rates, while data transfer from DRAM to MCH occurs at DRAM access speed rates. In this example, data latency and throughput rates are the same as any DRAM operation as long as the read operations are executed onto the pages that were opened with the activate command previously sent to pre-fetch data from the Flash to DRAM. Thus, a longer separation time period between the RAS (e.g. Activate command) and the first CAS (column address strobe e.g. read or write command) is required to account for the time it takes to pre-fetch data from the Flash to DRAM.

[0085] An example of FDHDIMM operating as a DDR DIMM with SSD is shown in FIG. 4B, wherein the FDHDIMM 400' supports two different interface interpretations to the MCH. In the first interface interpretation, the MCH views the FDHDIMM 400' as a combination of DRAM DIMM and SSD (not illustrated). In this mode the MCH needs to manage two address spaces, one for the DRAMs 402' and one for the Flash 404'. The MCH is coupled to, and controls, both of the DRAM and Flash memory subsystems. One advantage of this mode is that the CPU does not need to be in the data path when data is moved from DRAM to Flash or from Flash to DRAM. In the second interface interpretation, the MCH views the FDHDIMM 400' as an on-DIMM Flash with the SSD in an extended memory space that is behind the DRAM space. Thus, in this mode, the MCH physically fetches data from the SSD to the DDR DRAM and then

the DRAM sends the data to the MCH. Since all data movement occurs on the FDHDIMM, this mode will provide better performance than if the data were to be moved through or via the CPU.

[0086] In accordance with one embodiment and as shown in FIG. 4B, the FDHDIMM 400' receives control signals 408 from the MCH, where the control signals may include one or more control signals specifically for the DRAM 402' operation and one or more control signals specifically for the Flash 404' operation. In this embodiment, the MCH or CPU is coupled to the FDHDIMM via a single data bus interface 410 which couples the MCH to the DRAM.

[0087] FIGS. 5A and 5B are block diagrams of a memory module 500 that is couplable to a host system (not shown). The host system may be a server or any other system comprising a memory system controller or an MCH for providing and controlling the read/write access to one or more memory systems, wherein each memory system may include a plurality of memory subsystems, a plurality of memory devices, or at least one memory module. The term "read/write access" means the ability of the MCH to interface with a memory system or subsystem in order to write data into it or read data from it, depending on the particular requirement at a particular time.

[0088] In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory subsystem which may be integrated with other components of a host system. In certain embodiments, memory module 500 is a Flash-DRAM hybrid memory module that has the DIMM (dual-inline memory module) form factor, and may be referred to as a FDHDIMM, although it is to be understood that in both structure and operation it may be different from the FDHDIMM discussed above and described with reference to FIGS. 4A and 4B. Memory

module 500 includes two on-module intermediary components: a controller and a data manager. These on-module intermediary components may be physically separate components, circuits, or modules, or they may be integrated onto a single integrated circuit or device, or integrated with other memory devices, for example in a three dimensional stack, or in any one of several other possible expedients for integration known to those skilled in the art to achieve a specific design, application, or economic goal. In the case of a DIMM, these on-module intermediary components are an on-DIMM Controller (CDC) 502 and an on-DIMM data manager (DMgr) 504. While the DIMM form factor will predominate the discussion herein, it should be understood that this is for illustrative purposes only and memory systems using other form factors are contemplated as well. CDC 502 and data manager DMgr 504 are operative to manage the interface between a non-volatile memory subsystem such as a Flash 506, a volatile memory subsystem such as a DRAM 508, and a host system represented by MCH 510.

[0089] In certain embodiments, CDC 502 controls the read/write access to/from Flash memory 506 from/to DRAM memory 508, and to/from DRAM memory from/to MCH 510. Read/write access between DRAM 508, Flash 506 and MCH 510 may be referred to herein generally as communication, wherein control and address information C/A 560 is sent from MCH 510 to CDC 502, and possible data transfers follow as indicated by Data 550, Data 555, and/or Data 556. In certain embodiments, the CDC 502 performs specific functions for memory address transformation, such as address translation, mapping, or address domain conversion, Flash access control, data error correction, manipulation of data width or data formatting or data modulation between the Flash memory and DRAM, and so on. In certain embodiments, the CDC 502 ensures that memory module 500 provides transparent operation to the MCH in accordance with certain industry standards, such as DDR, DDR2, DDR3, DDR4 protocols. In

the arrangement shown in FIGS. 5A and 5B, there is no direct access from the MCH 510 to the Flash 506 memory subsystem. Thus in accordance with certain embodiments, the Flash access speed has minimal impact on the overall FDHDIMM access speed. In the schematic illustration of FIG. 5B and in accordance with one embodiment, the CDC controller 502 receives standard DDR commands from the MCH, interprets, and produces commands and/or control signals to control the operation of the Data manager (DMgr), the Flash memory and the DRAM memory. The DMgr controls the data path routing amongst DRAMs, Flash and MCH, as detailed below. The data path routing control signals are independently operated without any exclusivity.

[0090] An exemplary role of DMgr 504 is described with reference to FIG. 6. In certain embodiments and in response to communication from CDC 502, DMgr 504 provides a variety of functions to control data flow rate, data transfer size, data buffer size, data error monitoring or data error correction. For example, these functions or operations can be performed on-the-fly (while data is being transferred via the DMgr 504) or performed on buffered or stored data in DRAM or a buffer. In addition, one role of DMgr 504 is to provide interoperability among various memory subsystems or components and/or MCH 510.

[0091] In one embodiment, an exemplary host system operation begins with initialization. The CDC 502 receives a first command from the MCH 510 to initialize FDHDIMM 500 using a certain memory space. The memory space as would be controlled by MCH 510 can be configured or programmed during initialization or after initialization has completed. The MCH 510 can partition or parse the memory space in various ways that are optimized for a particular application that the host system needs to run or execute. In one embodiment, the CDC 502 maps the actual physical Flash 506 and DRAM 508 memory space using the information sent by MCH

510 via the first command. In one embodiment, the CDC 502 maps the memory address space of any one of the Flash 506 and DRAM 508 memory subsystems using memory address space information that is received from the host system, stored in a register within FDHDIMM 500, or stored in a memory location of a non-volatile memory subsystem, for example a portion of Flash 506 or a separate non-volatile memory subsystem. In one embodiment, the memory address space information corresponds to a portion of initialization information of the FDHDIMM 500.

[0092] In one embodiment, MCH 510 may send a command to restore a certain amount of data information from Flash 506 to DRAM 508. The CDC 502 provides control information to DMgr 504 to appropriately copy the necessary information from Flash 506 to the DRAM 508. This operation can provide support for various host system booting operations and/or a special host system power up operation.

[0093] In one embodiment, MCH 510 sends a command which may include various fields comprising control information regarding data transfer size, data format options, and/or startup time. CDC 502 receives and interprets the command and provides control signals to DMgr 504 to control the data traffic between the Flash 506, the DRAM 508, and the MCH 510. For example, DMgr 504 receives the data transfer size, formatting information, direction of data flow (via one or more multiplexers such as 611, 612, 621, 622 as detailed below), and the starting time of the actual data transfer from CDC 502. DMgr 504 may also receive additional control information from the CDC 502 to establish a data flow path and/or to correctly establish the data transfer fabric. In certain embodiments, DMgr 504 also functions as a bi-directional data transfer fabric. For example, DMgr 504 may have more than 2 sets of data ports facing the Flash 506 and the DRAM 508. Multiplexers 611 and 612 provide controllable data paths from any one of the

DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B) to any one of the MCH 510 and the Flash 506. Similarly multiplexers 621 and 622 provide controllable data paths from any one of the MCH and the Flash memory to any one of the DRAMs 508(1) and 508(2) (DRAM-A and DRAM-B). In one embodiment, DRAM 508(1) is a segment of DRAM 508, while in other embodiments, DRAM 508(1) is a separate DRAM memory subsystem. It will be understood that each memory segment can comprise one or more memory circuits, a memory devices, and/or memory integrated circuits. Of course other configurations for DRAM 508 are possible, and other data transfer fabrics using complex data paths and suitable types of multiplexing logic are contemplated.

[0094] In accordance with one embodiment, the two sets of multiplexors 611, 612 and 621, 622 allow independent data transfer to Flash 506 from DRAM-A 508(1) and DRAM-B 508(2). For example, in response to one or more control signals or a command from CDC 502, DMgr 504 can transfer data from DRAM-A 508(1) to MCH 510, via multiplexer 611, at the same time as from DRAM-B 508(2) to the Flash 506, via multiplexer 612; or data is transferred from DRAM-B 508(2) to MCH 510, via multiplexer 611, and simultaneously data is transferred from the Flash 506 to DRAM-A 508(1), via multiplexer 621. Further, in the same way that data can be transferred to or from the DRAM in both device-wide or segment-by-segment fashion, data can be transferred to or from the flash memory in device-wide or segment-by-segment fashion, and the flash memory can be addressed and accessed accordingly.

[0095] In accordance with one embodiment the illustrated arrangement of data transfer fabric of DMgr 504 also allows the CDC 502 to control data transfer from the Flash memory to the MCH by buffering the data from the Flash 506 using a buffer 602, and matching the data rate

and/or data format of MCH 510. The buffer 602 is shown in FIG. 6 as a portion of a data format module 604; however, buffer 602 may also be a distributed buffer such that one buffer is used for each one of the set of multiplexer logic elements shown as multiplexers 611, 612, 621, and 622. Various buffer arrangements may be used, such as a programmable size buffer to meet the requirement of a given system design requirement, for example the disparity between read/write access time; or overall system performance, for example latency. In certain embodiments, the buffer 604 may introduce one or more clock cycle delays into a data communication path between MCH 510, DRAM 508, and Flash 506.

[0096] In certain embodiments, data format module 604 contains a data formatting subsystem (not shown) to enable DMgr 504 to format and perform data transfer in accordance with control information received from CDC502. Data buffer 604 of data format module 602, discussed above, also supports a wide data bus 606 coupled to the Flash memory 506 operating at a first frequency, while receiving data from DRAM 508 using a relatively smaller width data bus 608 operating at a second frequency, the second frequency being larger than the first frequency in certain embodiments. The buffer 602 is designed to match the data flow rate between the DRAM 508 and the Flash 506.

[0097] A register 690 provides the ability to register commands received from MCH 510 via C/A 560 (FIG. 5A). The register 690 may communicate these commands to CDC 502 and/or to the DRAM 508 and/or Flash 506. The register 690 communicates these registered commands to CDC 502 for processing. The register 690 may also include multiple registers (not shown), such that it can provide the ability to register multiple commands, a sequence of commands, or

provide a pipeline delay stage for buffering and providing a controlled execution of certain commands received from MCH 510.

[0098] In certain embodiments, the register 690 may register commands from MCH 510 and transmit the registered commands to DRAM 508 and/or Flash 506 memory subsystems. In certain embodiments, the CDC 502 monitors commands received from MCH 510, via control and address bus C/A 560, and provides appropriate control information to DMgr 504, DRAM 508, or Flash 506 to execute these commands and perform data transfer operations between MCH 510 and FDHDIMM 500 via MCH data bus 610.

[0099] FIG. 7 illustrates a functional block diagram of the CDC 502. In certain embodiments, the major functional blocks of the CDC 502 are a DRAM control block DRAMCtrl 702, Flash control block FlashCtrl 704, MCH command interpreter CmdInt 706, DRAM-Flash interface scheduler Scheduler 708, and DMgr control block (DMgrCtrl) 710.

[00100] In accordance with one embodiment, DRAMCtrl 702 generates DRAM commands that are independent from the commands issued by the MCH 510. In accordance with one embodiment, when the MCH 510 initiates a read/write operation from/to the same DRAM 508 that is currently executing a command from the DRAMCtrl 702, then the CDC 502 may choose to instruct DRAMCtrl 702 to abort its operation in order to execute the operation initiated by the MCH. However, the CDC 502 may also pipeline the operation so that it causes DRAMCtrl 702 to either halt or complete its current operation prior to executing that of the MCH. The CDC 502 may also instruct DRAMCtrl 702 to resume its operation once the command from MCH 510 is completed.

[00101] In accordance with one embodiment, the FlashCtrl 704 generates appropriate Flash commands for the proper read/write operations. The CmdInt 706 intercepts commands received from MCH 510 and generates the appropriate control information and control signals and transmit them to the appropriate FDHDIMM functional block. For example, CmdInt 706 issues an interrupt signal to the DRAMCtrl 702 when the MCH issues a command that collides (conflicts) with the currently executing or pending commands that DRAMCtrl 702 has initiated independently from MCH 510, thus subordinating these commands to those from the MCH. The Scheduler 708 schedules the Flash-DRAM interface operation such that there is no resource conflict in the DMgr 504. In accordance with one embodiment, the Scheduler 708 assigns time slots for the DRAMCtrl 702 and FlashCtrl 704 operation based on the current status and the pending command received or to be received from the MCH. The DMgrCtrl 710 generates and sends appropriate control information and control signals for the proper operation and control of the data transfer fabric to enable or disable data paths between Flash 506, DRAM 508, and the MCH 510.

[00102] FIG. 8A is a block diagram showing a Flash-DRAM hybrid DIMM (FDHDIMM). As seen from FIG. 8A, this Flash-DRAM hybrid DIMM requires two separate and independent address buses to separately control the address spaces: one for the Flash memory Flash 506 and the other for the DRAM memory DRAM 508. The MCH treats the DRAM 508 and Flash 506 as separate memory subsystems, for example DRAM and SSD/HD memory subsystems. The memory in each address space is controlled directly by the MCH. However, the on-DIMM data path between Flash 506 and DRAM 508 allows for direct data transfer to occur between the Flash 506 and the DRAM 508 in response to control information from Ctrl 502. In this embodiment, this data transfer mechanism provides direct support for executing commands from

the MCH without having the MCH directly controlling the data transfer, and thus improving data transfer performance from Flash 506 to the DRAM 508. However, the MCH needs to manage two address spaces and two different memory protocols simultaneously. Moreover, the MCH needs to map the DRAM memory space into the Flash memory space, and the data interface time suffers due to the difference in the data access time between the Flash memory and the DRAM memory.

[00103] In accordance with one embodiment, a memory space mapping of a Flash-DRAM hybrid DIMM is shown in FIG. 8B. A memory controller of a host system (not shown) controls both of the DRAM 508 address space and the Flash 506 address space using a single unified address space. The CDC 502 receives memory access commands from the MCH and generates control information for appropriate mapping and data transfer between Flash and DRAM memory subsystem to properly carry out the memory access commands. In one embodiment, the memory controller of the host system views the large Flash memory space as a DRAM memory space, and accesses this unified memory space with a standard DDR (double data rate) protocol used for accessing DRAM. The unified memory space in this case can exhibit overlapping memory address space between the Flash 506 and the DRAM 508. The overlapping memory address space may be used as a temporary storage or buffer for data transfer between the Flash 506 and the DRAM 508. For example, the DRAM memory space may hold a copy of data from the selected Flash memory space such that the MCH can access this data normally via DDR memory access commands. The CDC 502 controls the operation of the Flash 506 and DRAM 508 memory subsystems in response to commands received from a memory controller of a host system.

[00104] In one embodiment, the unified memory space corresponds to a contiguous address space comprising a first portion of the address space of the Flash 506 and a first portion of the address space of the DRAM 508. The first portion of the address space of the Flash 506 can be determined via a first programmable register holding a first value corresponding to the desired Flash memory size to be used. Similarly, the first portion of the address space of the DRAM 508 can be determined via a second programmable register holding a second value corresponding to the desired DRAM memory size to be used. In one embodiment, any one of the first portion of the address space of the Flash 506 and the first portion of the address space of the DRAM 508 is determined via a first value corresponding to a desired performance or memory size, the first value being received by the CDC 502 via a command sent by memory controller of the host system.

[00105] In accordance with one embodiment, a flow diagram directed to the transfer of data from Flash memory to DRAM memory and vice versa in an exemplary FDHDIMM is shown in Fig. 9. In certain embodiments, data transfer from the Flash 506 to the DRAM 508 occurs in accordance with memory access commands which the CDC 502 receives from the memory controller of the host system. In certain embodiments, the CDC 502 controls the data transfer from the DRAM 508 to the Flash 506 so as to avoid conflict with any memory operation that is currently being executed. For example, when all the pages in a particular DRAM memory block are closed. The CDC 502 partitions the DRAM memory space into a number of blocks for the purpose of optimally supporting the desired application. The controller can configure memory space in the memory module based on at least one of one or more commands received from the MCH, instructions received from the MCH, a programmable value written into a register, a value corresponding to a first portion of the volatile memory subsystem, a value corresponding to a

first portion of the non-volatile memory subsystem, and a timing value. Furthermore, the block size can be configurable by the memory controller of the host system, such that the number pages in a block can be optimized to support a particular application or a task. Furthermore, the block size may be configured on-the-fly, e.g. CDC 502 can receive instruction regarding a desired block size from the memory controller via a memory command, or via a programmable value.

[00106] In certain embodiments, a memory controller can access the memory module using a standard access protocol, such as JEDEC's DDR DRAM, by sending a memory access command to the CDC 502 which in turn determines what type of a data transfer operation it is and the corresponding target address where the data information is stored, e.g. data information is stored in the DRAM 508 or Flash 506 memory subsystems. In response to a read operation, if the CDC 502 determines that data information, e.g. a page (or block), does not reside in the DRAM 508 but resides in Flash 506, then the CDC 502 initiates and controls all necessary data transfer operations from Flash 506 to DRAM 508 and subsequently to the memory controller. In one embodiment, once the CDC 502 completes the data transfer operation of the requested data information from the Flash 506 to the DRAM 508, the CDC 502 alerts the memory controller to retrieve the data information from the DRAM 508. In on embodiment, the memory controller initiates the copying of data information from Flash 506 to DRAM 508 by writing, into a register in the CDC 502, the target Flash address along with a valid block size. The CDC 502 in turn, executes appropriate operations and generates control information to copy the data information to the DRAM 508. Consequently, the memory controller can access or retrieve the data information using standard memory access commands or protocol.

[00107] An exemplary flow chart is shown in FIG. 9, a starting step or power up 902, is followed by an initialization step 904, the memory controller initiates, at step 906, a data move from the Flash 506 to the DRAM 508 by writing target address and size, to a control register in the CDC 502, which then copies, at 908, data information from the Flash 506 to the DRAM 508 and erases the block in the Flash. Erasing the data information from Flash may be accomplished independently from (or concurrently with) other steps that CDC 502 performs in this flow chart, i.e. other steps can be executed concurrently with the Erase the Flash block step. Once the data information or a block of data information is thus moved to the DRAM 508, the memory controller can operate on this data block using standard memory access protocol or commands at 910. The CDC 502 checks, at 912, if any of the DRAM 508 blocks, or copied blocks, are closed. If the memory controller closed any open blocks in DRAM 508, then the CDC 502 initiate a Flash write to write the closed block from the DRAM 508 to the Flash 506, at 914. In addition, the memory controller, at 916, reopens the closed block that is currently being written into the Flash 506, then the CDC 502 stops the Flash write operation and erases the Flash block which was being written to, as shown at 918. Otherwise, the CDC 502 continues and completes the writing operation to the Flash at 920.

[00108] The dashed lines in FIG. 9 indicate independent or parallel activities that can be performed by the CDC 502. At any time the CDC 502 receives a DRAM load command from a memory controller which writes a Flash target address and/or block size information into the RC register(s) at 922, as described above, then the CDC 502 executes a load DRAM w/RC step 906 and initiates another branch (or a thread) of activities that includes steps 908 – 922. In one embodiment, the CDC 502 controls the data transfer operations between DRAM 508 and Flash 506 such that the Flash 506 is completely hidden from the memory controller. The CDC 502

monitors all memory access commands sent by the memory controller using standard DRAM protocol and appropriately configures and manipulate both Flash 506 and DRAM 508 memory subsystems to perform the requested memory access operation and thus achieve the desired results. The memory controller does not interface directly with the Flash memory subsystem. Instead, the memory controller interfaces with the CDC 502 and/or DMgr 504 as shown in Fig. 5 and Fig. 6. Moreover, the memory controller may use one or more protocol, such as DDR, DDR2, DDR3, DDR4 protocols or the like.

[00109] In accordance with one embodiment, an example of mapping a DRAM address space to Flash memory address space is shown in FIG. 10. Two sets (1002, 1004) of address bits AD6 to AD17, forming a 24 bit extended memory page address, are allocated for the block address. For example, assuming a Block size of 256K Bytes, then a 24-bit block address space (using the two sets of AD6 to AD17 1002 and 1004) would enable access to 4TB of Flash memory storage space. If a memory module has 1GB of DRAM storage capacity, then it can hold approximately 4K Blocks of data in the DRAM memory, each Block comprise 256 K Bytes of data. The DRAM address space, corresponding to the 4K blocks, can be assigned to different virtual ranks and banks, where the number of virtual ranks and banks is configurable and can be manipulated to meet a specific design or performance needs. For example, if a 1G Bytes memory module is configured to comprise two ranks with eight banks per rank, then each bank would hold two hundred fifty (250) blocks or the equivalent of 62 M Bytes or 62K pages, where each page correspond to a 1K Bytes. Other configurations using different page, block, banks, or ranks numbers may also be used. Furthermore, an exemplary mapping of 24-bit DDR DIMM block address to Flash memory address, using Block addressing as described above, is shown in Fig. 10. The 24-bit can be decomposed into fields, such as a logical unit number LUN address 1061

field, a Block address 1051 field, a Plane address 1041, a Page address 1031, and a group of least significant address bits A_0A_1 1021. The Plane address 1041 is a sub address of the block address, and it may be used to support multiple page IO so as to improve Flash memory subsystem operation. In this example, it is understood that different number of bits may be allocated to each field of the 24-bit

[00110] The CDC 502 manages the block write-back operation by queuing the blocks that are ready to be written back to the Flash memory. As described above, if any page in a queued block for a write operation is reopened, then the CDC 502 will stop the queued block write operation, and remove the block from the queue. Once all the pages in a block are closed, then the CDC 502 restarts the write-back operation and queue the block for a write operation.

[00111] In accordance with one embodiment, an exemplary read operation from Flash 506 to DRAM 508 can be performed in approximately 400 μ s, while a write operation from DRAM 508 to Flash 506 can be performed in approximately 22ms resulting in a read to write ratio of 55 to 1. Therefore, if the average time a host system's memory controller spends accessing data information in a Block of DRAM is about 22ms (that is the duration that a Block comprises one or more pages that are open), then the block write-back operation from DRAM to Flash would not impact performance and hence the disparity between read and write access may be completely hidden from the memory controller. If the block usage time is 11ms instead of 22ms, then the CDC 502 control the data transfer operation between DRAM 508 and Flash 506 such that there are no more than 9 closed blocks in the queue to be written-back to the Flash memory, hence approximately an average of 100ms can be maintained for a standard DDR DRAM operation. Moreover, the number of closed Blocks in the queue to be written-back to the Flash

memory subsystem varies with the average block usage time and the desired performance for a specific host system or for a specific application running using the host system resources.

[00112] Consequently, the maximum number of closed Blocks to be written-back to Flash can be approximated to be

$$((\text{\#of blocks per bank})/(\text{ratio of 'Flash_block_write_time' to 'Flash_read_time'})) * (\text{Block usage time})/(\text{'Flash_block_write_time'})$$

[00113] In order to maintain less than 100ms time period for queued write-back Blocks, then using a Flash memory subsystem having 22ms write access time per Block would results in a maximum number of four Blocks to be queued for write operation to Flash 506. Therefore, on average approximately 88ms (= 22ms * 4) for blocks means that each bank should not have more than four Blocks that need to be written back to the Flash 506.

[00114] The above equation also indicates that bigger DRAM memory space can support shorter block usage times. For example, 2GB of DRAM memory allows the 8 closed blocks to be written-back to Flash. The table in FIG. 11 provides an estimation of the maximum allowed closed blocks in the queue to be written back to the Flash memory for different DRAM density using various average block use time.

[00115] Certain embodiments described herein include a memory system which can communicate with a host system such as a disk controller of a computer system. The memory system can include volatile and non-volatile memory, and a controller. The controller backs up

the volatile memory using the non-volatile memory in the event of a trigger condition. Trigger conditions can include, for example, a power failure, power reduction, request by the host system, etc. In order to power the system in the event of a power failure or reduction, the memory system can include a secondary power source which does not comprise a battery and may include, for example, a capacitor or capacitor array.

[00116] In certain embodiments, the memory system can be configured such that the operation of the volatile memory is not adversely affected by the non-volatile memory or by the controller when the volatile memory is interacting with the host system. For example, one or more isolation devices may isolate the non-volatile memory and the controller from the volatile memory when the volatile memory is interacting with the host system and may allow communication between the volatile memory and the non-volatile memory when the data of the volatile memory is being restored or backed-up. This configuration generally protects the operation of the volatile memory when isolated while providing backup and restore capability in the event of a trigger condition, such as a power failure.

[00117] In certain embodiments described herein, the memory system includes a power module which provides power to the various components of the memory system from different sources based on a state of the memory system in relation to a trigger condition (e.g., a power failure). The power module may switch the source of the power to the various components in order to efficiently provide power in the event of the power failure. For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor

array). In the event of a power failure or other trigger condition, the power module may power the volatile memory elements using the previously charged secondary power source.

[00118] In certain embodiments, the power module transitions relatively smoothly from powering the volatile memory with system power to powering it with the secondary power source. For example, the power system may power volatile memory with a third power source from the time the memory system detects that power failure is likely to occur until the time the memory system detects that the power failure has actually occurred.

[00119] In certain embodiments, the volatile memory system can be operated at a reduced frequency during backup and/or restore operations which can improve the efficiency of the system and save power. In some embodiments, during backup and/or restore operations, the volatile memory communicates with the non-volatile memory by writing and/or reading data words in bit-wise slices instead of by writing entire words at once. In certain embodiments, when each slice is being written to or read from the volatile memory the unused slice(s) of volatile memory is not active, which can reduce the power consumption of the system.

[00120] In yet other embodiments, the non-volatile memory can include at least 100 percent more storage capacity than the volatile memory. This configuration can allow the memory system to efficiently handle subsequent trigger conditions.

[00121] FIG. 12 is a block diagram of an example memory system 1010 compatible with certain embodiments described herein. The memory system 1010 can be coupled to a host computer system and can include a volatile memory subsystem 1030, a non-volatile memory

subsystem 1040, and a controller 1062 operatively coupled to the non-volatile memory subsystem 1040. In certain embodiments, the memory system 1010 includes at least one circuit 1052 configured to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030.

[00122] In certain embodiments, the memory system 1010 comprises a memory module. The memory system 1010 may comprise a printed-circuit board (PCB) 1020. In certain embodiments, the memory system 1010 has a memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, or 8-GB. Other volatile memory capacities are also compatible with certain embodiments described herein. In certain embodiments, the memory system 1010 has a non-volatile memory capacity of 512-MB, 1-GB, 2-GB, 4-GB, 8-GB, 16-GB, or 32-GB. Other non-volatile memory capacities are also compatible with certain embodiments described herein. In addition, memory systems 1010 having widths of 4 bytes, 8 bytes, 16 bytes, 32 bytes, or 32 bits, 64 bits, 128 bits, 256 bits, as well as other widths (in bytes or in bits), are compatible with embodiments described herein. In certain embodiments, the PCB 1020 has an industry-standard form factor. For example, the PCB 1020 can have a low profile (LP) form factor with a height of 30 millimeters and a width of 133.35 millimeters. In certain other embodiments, the PCB 1020 has a very high profile (VHP) form factor with a height of 50 millimeters or more. In certain other embodiments, the PCB 1020 has a very low profile (VLP) form factor with a height of 18.3 millimeters. Other form factors including, but not limited to, small-outline (SO-DIMM), unbuffered (UDIMM), registered (RDIMM), fully-buffered (FBDIMM), miniDIMM, mini-RDIMM, VLP mini-DIMM, micro-DIMM, and SRAM DIMM are also compatible with certain embodiments described herein. For example, in other embodiments, certain non-DIMM form factors are possible such as, for

example, single in-line memory module (SIMM), multi-media card (MMC), and small computer system interface (SCSI).

[00123] In certain preferred embodiments, the memory system 1010 is in electrical communication with the host system. In other embodiments, the memory system 1010 may communicate with a host system using some other type of communication, such as, for example, optical communication. Examples of host systems include, but are not limited to, blade servers, 1U servers, personal computers (PCs), and other applications in which space is constrained or limited. The memory system 1010 can be in communication with a disk controller of a computer system, for example. The PCB 1020 can comprise an interface 1022 that is configured to be in electrical communication with the host system (not shown). For example, the interface 1022 can comprise a plurality of edge connections which fit into a corresponding slot connector of the host system. The interface 1022 of certain embodiments provides a conduit for power voltage as well as data, address, and control signals between the memory system 1010 and the host system. For example, the interface 1022 can comprise a standard 240-pin DDR2 edge connector.

[00124] The volatile memory subsystem 1030 comprises a plurality of volatile memory elements 1032 and the non-volatile memory subsystem 1040 comprises a plurality of non-volatile memory elements 1042. Certain embodiments described herein advantageously provide nonvolatile storage via the non-volatile memory subsystem 1040 in addition to high-performance (e.g., high speed) storage via the volatile memory subsystem 1030. In certain embodiments, the first plurality of volatile memory elements 1032 comprises two or more dynamic random-access memory (DRAM) elements. Types of DRAM elements 1032 compatible with certain embodiments described herein include, but are not limited to, DDR, DDR2, DDR3, and

synchronous DRAM (SDRAM). For example, in the block diagram of FIG. 12, the first memory bank 1030 comprises eight 64Mx8 DDR2 SDRAM elements 1032. The volatile memory elements 1032 may comprise other types of memory elements such as static random-access memory (SRAM). In addition, volatile memory elements 1032 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Volatile memory elements 1032 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BGA), fine-pitch BGA (FBOA), micro-BOA (1.1,BGA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00125] In certain embodiments, the second plurality of non-volatile memory elements 1042 comprises one or more flash memory elements. Types of flash memory elements 1042 compatible with certain embodiments described herein include, but are not limited to, NOR flash, NAND flash, ONE-NAND flash, and multi-level cell (MLC). For example, in the block diagram of FIG. 12, the second memory bank 1040 comprises 512 MB of flash memory organized as four 128Mbx8 NAND flash memory elements 1042. In addition, nonvolatile memory elements 1042 having bit widths of 4, 8, 16, 32, as well as other bit widths, are compatible with certain embodiments described herein. Non-volatile memory elements 1042 compatible with certain embodiments described herein have packaging which include, but are not limited to, thin small-outline package (TSOP), ball-grid-array (BOA), fine-pitch BOA (FBGA), micro-BOA (POA), mini-BGA (mBGA), and chip-scale packaging (CSP).

[00126] FIG. 13 is a block diagram of an example memory module 10 with ECC (error-correcting code) having a volatile memory subsystem 1030 with nine volatile memory elements

1032 and a non-volatile memory subsystem 1040 with five non-volatile memory elements 1042 in accordance with certain embodiments described herein. The additional memory element 1032 of the first memory bank 1030 and the additional memory element 1042 of the second memory bank 1040 provide the ECC capability. In certain other embodiments, the volatile memory subsystem 1030 comprises other numbers of volatile memory elements 1032 (e.g., 2, 3, 4, 5, 6, 7, more than 9). In certain embodiments, the non-volatile memory subsystem 1040 comprises other numbers of nonvolatile memory elements 1042 (e.g., 2, 3, more than 5).

[00127] Referring to FIG. 12, in certain embodiments, the logic element 1070 comprises a field-programmable gate array (FPGA). In certain embodiments, the logic element 1070 comprises an FPGA available from Lattice Semiconductor Corporation which includes an internal flash. In certain other embodiments, the logic element 1070 comprises an FPOA available from another vendor. The internal flash can improve the speed of the memory system 1010 and save physical space. Other types of logic elements 1070 compatible with certain embodiments described herein include, but are not limited to, a programmable-logic device (PLD), an application-specific integrated circuit (ASIC), a custom-designed semiconductor device, a complex programmable logic device (CPLD). In certain embodiments, the logic element 1070 is a custom device. In certain embodiments, the logic element 1070 comprises various discrete electrical elements, while in certain other embodiments, the logic element 1070 comprises one or more integrated circuits. FIG. 14 is a block diagram of an example memory module 1010 having a microcontroller unit 1060 and logic element 1070 integrated into a single controller 1062 in accordance with certain embodiments described herein. In certain embodiments, the controller 1062 includes one or more other components. For example, in one

embodiment, an FPGA without an internal flash is used and the controller 1062 includes a separate flash memory component which stores configuration information to program the FPGA.

[00128] In certain embodiments, the at least one circuit 1052 comprises one or more switches coupled to the volatile memory subsystem 1030, to the controller 1062, and to the host computer (e.g., via the interface 1022, as schematically illustrated by FIGS. 12-14). The one or more switches are responsive to signals (e.g., from the controller 1062) to selectively operatively decouple the controller 1062 from the volatile memory subsystem 1030 and to selectively operatively couple the controller 1062 to the volatile memory subsystem 1030. In addition, in certain embodiments, the at least one circuit 1052 selectively operatively couples and decouples the volatile memory subsystem 1030 and the host system.

[00129] In certain embodiments, the volatile memory subsystem 1030 can comprise a registered DIMM subsystem comprising one or more registers 1160 and a plurality of DRAM elements 1180, as schematically illustrated by FIG. 15A. In certain such embodiments, the at least one circuit 1052 can comprise one or more switches 1172 coupled to the controller 1062 (e.g., logic element 1070) and to the volatile memory subsystem 1030 which can be actuated to couple and decouple the controller 1062 to and from the volatile memory subsystem 1030, respectively. The memory system 1010 further comprises one or more switches 1170 coupled to the one or more registers 1160 and to the plurality of DRAM elements 1180 as schematically illustrated by FIG. 15A. The one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. In certain other embodiments, as schematically illustrated by FIG. 15B, the one or more switches 1174 are also coupled to the one or more registers 1160 and to a power source 1162 for the one

or more registers 1160. The one or more switches 1174 can be selectively switched to turn power on or off to the one or more registers 1160, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150. As schematically illustrated by FIG. 15C, in certain embodiments the at least one circuit 1052 comprises a dynamic on-die termination (ODT) 1176 circuit of the logic element 1070. For example, the logic element 1070 can comprise a dynamic ODT circuit 1176 which selectively operatively couples and decouples the logic element 1070 to and from the volatile memory subsystem 1030, respectively. In addition, and similar to the example embodiment of FIG. 15A described above, the one or more switches 1170 can be selectively switched, thereby selectively operatively coupling the volatile memory subsystem 1030 to the host system 1150.

[00130] Certain embodiments described herein utilize the non-volatile memory subsystem 1040 as a flash “mirror” to provide backup of the volatile memory subsystem 1030 in the event of certain system conditions. For example, the non-volatile memory subsystem 1040 may backup the volatile memory subsystem 1030 in the event of a trigger condition, such as, for example, a power failure or power reduction or a request from the host system. In one embodiment, the nonvolatile memory subsystem 1040 holds intermediate data results in a noisy system environment when the host computer system is engaged in a long computation. In certain embodiments, a backup may be performed on a regular basis. For example, in one embodiment, the backup may occur every millisecond in response to a trigger condition. In certain embodiments, the trigger condition occurs when the memory system 1010 detects that the system voltage is below a certain threshold voltage. For example, in one embodiment, the threshold voltage is 10 percent below a specified operating voltage. In certain embodiments, a trigger condition occurs when the voltage goes above a certain threshold value, such as, for example,

10 percent above a specified operating voltage. In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold. In various embodiments, a backup and/or restore operation may occur in reboot and/or non-reboot trigger conditions.

[00131] As schematically illustrated by FIGS. 12 and 13, in certain embodiments, the controller 1062 may comprise a microcontroller unit (MCU) 1060 and a logic element 1070. In certain embodiments, the MCU 1060 provides memory management for the non-volatile memory subsystem 1040 and controls data transfer between the volatile memory subsystem 30 and the nonvolatile memory subsystem 1040. The MCU 1060 of certain embodiments comprises a 16-bit microcontroller, although other types of microcontrollers are also compatible with certain embodiments described herein. As schematically illustrated by FIGS. 12 and 13, the logic element 1070 of certain embodiments is in electrical communication with the non-volatile memory subsystem 1040 and the MCU 1060. The logic element 1070 can provide signal level translation between the volatile memory elements 1032 (e.g., 1.8V SSTL-2 for DDR2 SDRAM elements) and the non-volatile memory elements 1042 (e.g., 3V TTL for NAND flash memory elements). In certain embodiments, the logic element 1070 is also programmed to perform address/address translation between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. In certain preferred embodiments, 1-NAND type flash are used for the non-volatile memory elements 1042 because of their superior read speed and compact structure.

[00132] The memory system 1010 of certain embodiments is configured to be operated in at least two states. The at least two states can comprise a first state in which the controller 1062 and the non-volatile memory subsystem 1040 are operatively decoupled (e.g., isolated) from the

volatile memory subsystem 1030 by the at least one circuit 1052 and a second state in which the volatile memory subsystem 1030 is operatively coupled to the controller 1062 to allow data to be communicated between the volatile memory subsystem 1030 and the nonvolatile memory subsystem 1040 via the controller 1062. The memory system 1010 may transition from the first state to the second state in response to a trigger condition, such as when the memory system 1010 detects that there is a power interruption (e.g., power failure or reduction) or a system hang-up.

[00133] The memory system 1010 may further comprise a voltage monitor 1050. The voltage monitor circuit 1050 monitors the voltage supplied by the host system via the interface 1022. Upon detecting a low voltage condition (e.g., due to a power interruption to the host system), the voltage monitor circuit 1050 may transmit a signal to the controller 1062 indicative of the detected condition. The controller 1062 of certain embodiments responds to the signal from the voltage monitor circuit 1050 by transmitting a signal to the at least one circuit 1052 to operatively couple the controller to the volatile memory system 1030, such that the memory system 1010 enters the second state. For example, the voltage monitor 1050 may send a signal to the MCU 1060 which responds by accessing the data on the volatile memory system 1030 and by executing a write cycle on the nonvolatile memory subsystem 1040. During this write cycle, data is read from the volatile memory subsystem 1030 and is transferred to the non-volatile memory subsystem 1040 via the MCU 1060. In certain embodiments, the voltage monitor circuit 1050 is part of the controller 1062 (e.g., part of the MCU 1060) and the voltage monitor circuit 1050 transmits a signal to the other portions of the controller 1062 upon detecting a power threshold condition.

[00134] The isolation or operational decoupling of the volatile memory subsystem 1030 from the non-volatile memory subsystem in the first state can preserve the integrity of the operation of the memory system 1010 during periods of operation in which signals (e.g., data) are transmitted between the host system and the volatile memory subsystem 1030. For example, in one embodiment during such periods of operation, the controller 1062 and the nonvolatile memory subsystem 1040 do not add a significant capacitive load to the volatile memory system 1030 when the memory system 1010 is in the first state. In certain such embodiments, the capacitive load of the controller 1062 and the non-volatile memory subsystem 1040 do not significantly affect the signals propagating between the volatile memory subsystem 1030 and the host system. This can be particularly advantageous in relatively high-speed memory systems where loading effects can be significant. In one preferred embodiment, the at least one circuit 1052 comprises an FSA1208 Low-Power, Eight-Port, Hi-Speed Isolation Switch from Fairchild Semiconductor. In other embodiments, the at least one circuit 1052 comprises other types of isolation devices.

[00135] Power may be supplied to the volatile memory subsystem 1030 from a first power supply (e.g., a system power supply) when the memory system 1010 is in the first state and from a second power supply 1080 when the memory system 1010 is in the second state. In certain embodiments, the memory system 1010 is in the first state when no trigger condition (e.g., a power failure) is present and the memory system 1010 enters the second state in response to a trigger condition. In certain embodiments, the memory system 1010 has a third state in which the controller 1062 is operatively decoupled from the volatile memory subsystem 1030 and power is supplied to the volatile memory subsystem 1030 from a third power supply (not shown). For example, in one embodiment the third power supply may provide power to the volatile memory

subsystem 1030 when the memory system 1010 detects that a trigger condition is likely to occur but has not yet occurred.

[00136] In certain embodiments, the second power supply 1080 does not comprise a battery. Because a battery is not used, the second power supply 1080 of certain embodiments may be relatively easy to maintain, does not generally need to be replaced, and is relatively environmentally friendly. In certain embodiments, as schematically illustrated by FIGS. 12-14, the second power supply 1080 comprises a step-up transformer 1082, a step-down transformer 1084, and a capacitor bank 1086 comprising one or more capacitors (e.g., double-layer capacitors). In one example embodiment, capacitors may take about three to four minutes to charge and about two minutes to discharge. In other embodiments, the one or more capacitors may take a longer time or a shorter time to charge and/or discharge. For example, in certain embodiments, the second power supply 1080 is configured to power the volatile memory subsystem 1030 for less than thirty minutes. In certain embodiments, the second power supply 1080 may comprise a battery. For example, in certain embodiments, the second power supply 1080 comprises a battery and one or more capacitors and is configured to power the volatile memory subsystem 1030 for no more than thirty minutes.

[00137] In certain embodiments, the capacitor bank 1086 of the second power supply 1080 is charged by the first power supply while the memory system 1010 is in the first state. As a result, the second power supply 1080 is fully charged when the memory system 1010 enters the second state. The memory system 1010 and the second power supply 1080 may be located on the same printed circuit board 1020. In other embodiments, the second power supply 1080 may not be on

the same printed circuit board 1020 and may be tethered to the printed circuit board 1020, for example.

[00138] When operating in the first state, in certain embodiments, the step-up transformer 1082 keeps the capacitor bank 1086 charged at a peak value. In certain embodiments, the step-down transformer 1084 acts as a voltage regulator to ensure that regulated voltages are supplied to the memory elements (e.g., 1.8V to the volatile DRAM elements 1032 and 3.0V to the non-volatile flash memory elements 1042) when operating in the second state (e.g., during power down). In certain embodiments, as schematically illustrated by FIGS. 12-14, the memory module 1010 further comprises a switch 1090 (e.g., FET switch) that switches power provided to the controller 1062, the volatile memory subsystem 1030, and the non-volatile memory subsystem 1040, between the power from the second power supply 1080 and the power from the first power supply (e.g., system power) received via the interface 1022. For example, the switch 1090 may switch from the first power supply to the second power supply 1080 when the voltage monitor 1050 detects a low voltage condition. The switch 1090 of certain embodiments advantageously ensures that the volatile memory elements 1032 and non-volatile memory elements 1042 are powered long enough for the data to be transferred from the volatile memory elements 1032 and stored in the non-volatile memory elements 1042. In certain embodiments, after the data transfer is complete, the switch 1090 then switches back to the first power supply and the controller 1062 transmits a signal to the at least one circuit 1052 to operatively decouple the controller 1062 from the volatile memory subsystem 1030, such that the memory system 1010 reenters the first state.

[00139] When the memory system 1010 re-enters the first state, data may be transferred back from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 via the

controller 1062. The host system can then resume accessing the volatile memory subsystem 1030 of the memory module 1010. In certain embodiments, after the memory system 1010 enters or re-enters the first state (e.g., after power is restored), the host system accesses the volatile memory subsystem 1030 rather than the non-volatile memory subsystem 1040 because the volatile memory elements 1032 have superior read/write characteristics. In certain embodiments, the transfer of data from the volatile memory bank 1030 to the nonvolatile memory bank 1040, or from the non-volatile memory bank 1040 to the volatile memory bank 1030, takes less than one minute per GB.

[00140] In certain embodiments, the memory system 1010 protects the operation of the volatile memory when communicating with the host-system and provides backup and restore capability in the event of a trigger condition such as a power failure. In certain embodiments, the memory system 1010 copies the entire contents of the volatile memory subsystem 1030 into the nonvolatile memory subsystem 1040 on each backup operation. Moreover, in certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are copied back into the volatile memory subsystem 1030 on each restore operation. In certain embodiments, the entire contents of the non-volatile memory subsystem 1040 are accessed for each backup and/or restore operation, such that the non-volatile memory subsystem 1040 (e.g., flash memory subsystem) is used generally uniformly across its memory space and wear-leveling is not performed by the memory system 1010. In certain embodiments, avoiding wear-leveling can decrease cost and complexity of the memory system 1010 and can improve the performance of the memory system 1010. In certain other embodiments, the entire contents of the volatile memory subsystem 1030 are not copied into the non-volatile memory subsystem 1040 on each backup operation, but only a partial copy is performed. In certain embodiments, other

management capabilities such as bad-block management and error management for the flash memory elements of the non-volatile memory subsystem 1040 are performed in the controller 1062.

[00141] The memory system 1010 generally operates as a write-back cache in certain embodiments. For example, in one embodiment, the host system (e.g., a disk controller) writes data to the volatile memory subsystem 1030 which then writes the data to non-volatile storage which is not part of the memory system 1010, such as, for example, a hard disk. The disk controller may wait for an acknowledgment signal from the memory system 1010 indicating that the data has been written to the hard disk or is otherwise secure. The memory system 1010 of certain embodiments can decrease delays in the system operation by indicating that the data has been written to the hard disk before it has actually done so. In certain embodiments, the memory system 1010 will still be able to recover the data efficiently in the event of a power outage because of the backup and restore capabilities described herein. In certain other embodiments, the memory system 1010 may be operated as a write-through cache or as some other type of cache.

[00142] FIG. 16 schematically illustrates an example power module 1100 of the memory system 1010 in accordance with certain embodiments described herein. The power module 1100 provides power to the various components of the memory system 1010 using different elements based on a state of the memory system 1010 in relation to a trigger condition. In certain embodiments, the power module 1100 comprises one or more of the components described above with respect to FIG. 12. For example, in certain embodiments, the power module 1100 includes the second power supply 1080 and the switch 1090.

[00143] The power module 1100 provides a plurality of voltages to the memory system 1010 comprising non-volatile and volatile memory subsystems 1030, 1040. The plurality of voltages comprises at least a first voltage 1102 and a second voltage 1104. The power module 1100 comprises an input 1106 providing a third voltage 1108 to the power module 1100 and a voltage conversion element 1120 configured to provide the second voltage 1104 to the memory system 1010. The power module 1100 further comprises a first power element 1130 configured to selectively provide a fourth voltage 1110 to the conversion element 1120. In certain embodiments, the first power element 1130 comprises a pulse-width modulation power controller. For example, in one example embodiment, the first power element 1130 is configured to receive a 1.8V input system voltage as the third voltage 1108 and to output a modulated 5V output as the fourth voltage 1110.

[00144] The power module 1100 further comprises a second power element 1140 can be configured to selectively provide a fifth voltage 1112 to the conversion element 1120. The power module 1100 can be configured to selectively provide the first voltage 1102 to the memory system 1010 either from the conversion element 1120 or from the input 1106.

[00145] The power module 1100 can be configured to be operated in at least three states in certain embodiments. In a first state, the first voltage 1102 is provided to the memory system 1010 from the input 1106 and the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130. In a second state, the fourth voltage 1110 is provided to the conversion element 1120 from the first power element 1130 and the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120. In the third state, the fifth voltage 1112 is provided to the conversion element 1120 from the second power element

1140 and the first voltage 1104 is provided to the memory system 1010 from the conversion element 1120.

[00146] In certain embodiments, the power module 1100 transitions from the first state to the second state upon detecting that a trigger condition is likely to occur and transitions from the second state to the third state upon detecting that the trigger condition has occurred. For example, the power module 1100 may transition to the second state when it detects that a power failure is about to occur and transitions to the third state when it detects that the power failure has occurred. In certain embodiments, providing the first voltage 1102 in the second state from the first power element 1130 rather than from the input 1106 allows a smoother transition from the first state to the third state. For example, in certain embodiments, providing the first voltage 1102 from the first power element 1130 has capacitive and other smoothing effects. In addition, switching the point of power transition to be between the conversion element 1120 and the first and second power elements 1130, 1140 (e.g., the sources of the pre-regulated fourth voltage 1110 in the second state and the pre-regulated fifth voltage 1112 in the third state) can smooth out potential voltage spikes.

[00147] In certain embodiments, the second power element 1140 does not comprise a battery and may comprise one or more capacitors. For example, as schematically illustrated in FIG. 16, the second power element 1140 comprises a capacitor array 1142, a buck-boost converter 1144 which adjusts the voltage for charging the capacitor array and a voltage/current limiter 1146 which limits the charge current to the capacitor array 1142 and stops charging the capacitor array 1142 when it has reached a certain charge voltage. In one example embodiment, the capacitor array 1142 comprises two 50 farad capacitors capable of holding a total charge of 4.6V. For

example, in one example embodiment, the buck-boost converter 1144 receives a 1.8V system voltage (first voltage 1108) and boosts the voltage to 4.3V which is outputted to the voltage current limiter 1146. The voltage/current limiter 1146 limits the current going to the capacitor array 1142 to 1A and stops charging the array 1142 when it is charged to 4.3V. Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the second power element 1140 may include alternative embodiments. For example, different components and/or different value components may be used. For example, in other embodiments, a pure boost converter may be used instead of a buck-boost converter. In another embodiment, only one capacitor may be used instead of a capacitor array 1142.

[00148] The conversion element 1120 can comprise one or more buck converters and/or one or more buck-boost converters. The conversion element 1120 may comprise a plurality of sub-blocks 1122, 1124, 1126 as schematically illustrated by FIG. 16, which can provide more voltages in addition to the second voltage 1104 to the memory system 1010. The sub-blocks may comprise various converter circuits such as buck-converters, boost converters, and buck-boost converter circuits for providing various voltage values to the memory system 1010. For example, in one embodiment, sub-block 1122 comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter as schematically illustrated by FIG. 16. Various other components for the sub-blocks 1122, 1124, 1126 of the conversion element 1120 are also compatible with certain embodiments described herein. In certain embodiments, the conversion element 1120 receives as input either the fourth voltage 1110 from the first power element 1130 or the fifth voltage 1112 from the second power element 1140, depending on the state of the power module 1100, and reduces the input to an appropriate

amount for powering various components of the memory system. For example, the buck-converter of sub-block 1122 can provide 1.8V at 2A for about 60 seconds to the volatile memory elements 1032 (e.g., DRAM), the non-volatile memory elements 1042 (e.g., flash), and the controller 1062 (e.g., an FPGA) in one embodiment. The sub-block 1124 can provide the second voltage 1104 as well as another reduced voltage 1105 to the memory system 1010. In one example embodiment, the second voltage 1104 is 2.5V and is used to power the at least one circuit 1052 (e.g., isolation device) and the other reduced voltage 1105 is 1.2V and is used to power the controller 1062 (e.g., FPGA). The subblock 1126 can provide yet another voltage 1107 to the memory system 1010. For example, the voltage 1107 may be 3.3V and may be used to power both the controller 1062 and the at least one circuit 1052.

[00149] Although described with respect to certain example embodiments, one of ordinary skill will recognize from the disclosure herein that the conversion element 1120 may include alternative embodiments. For example, there may be more or less sub-blocks which may comprise other types of converters (e.g., pure boost converters) or which may produce different voltage values. In one embodiment, the volatile memory elements 1032 and nonvolatile memory elements 1042 are powered using independent voltages and are not both powered using the first voltage 1102.

[00150] FIG. 17 is a flowchart of an example method 1200 of providing a first voltage 1102 and a second voltage 1104 to a memory system 1010 including volatile and nonvolatile memory subsystems 1030, 1040. While the method 1200 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-15, other memory systems are also compatible with embodiments of the method 1200. During a first condition, the method 1200

comprises providing the first voltage 1102 to the memory system 1010 from an input power supply 1106 and providing the second voltage 1104 to the memory system 1010 from a first power subsystem in operational block 1210. For example, in one embodiment, the first power subsystem comprises the first power element 1130 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, other first power subsystems are used.

[00151] The method 1200 further comprises detecting a second condition in operational block 1220. In certain embodiments, detecting the second condition comprises detecting that a trigger condition is likely to occur. During the second condition, the method 1200 comprises providing the first voltage 1102 and the second voltage 1104 to the memory system 1010 from the first power subsystem in an operational block 1230. For example, referring to FIG. 16, a switch 1148 can be toggled to provide the first voltage 1102 from the conversion element 1120 rather than from the input power supply.

[00152] The method 1200 further comprises charging a second power subsystem in operational block 1240. In certain embodiments, the second power subsystem comprises the second power element 1140 or another power supply that does not comprise a battery. For example, in one embodiment, the second power subsystem comprises the second power element 1140 and the voltage conversion element 1120 described above with respect to FIG. 16. In other embodiments, some other second power subsystem is used.

[00153] The method 1200 further comprises detecting a third condition in an operational block 1250 and during the third condition, providing the first voltage 1102 and the second

voltage 1104 to the memory system 1010 from the second power subsystem 1140 in an operational block 1260. In certain embodiments, detecting the third condition comprises detecting that the trigger condition has occurred. The trigger condition may comprise various conditions described herein. In various embodiments, for example, the trigger condition comprises a power reduction, power failure, or system hang-up. The operational blocks of the method 1200 may be performed in different orders in various embodiments. For example, in certain embodiments, the second power subsystem 1140 is charged before detecting the second condition.

[00154] In certain embodiments, the memory system 1010 comprises a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040 comprising at least 100 percent more storage capacity than does the volatile memory subsystem. The memory system 1010 also comprises a controller 1062 operatively coupled to the volatile memory subsystem 1030 and operatively coupled to the non-volatile memory subsystem 1040. The controller 1062 can be configured to allow data to be communicated between the volatile memory subsystem 1030 and the host system when the memory system 1010 is operating in a first state and to allow data to be communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040 when the memory system 1010 is operating in a second state.

[00155] Although the memory system 1010 having extra storage capacity of the non-volatile memory subsystem 1040 has been described with respect to certain embodiments, alternative configurations exist. For example, in certain embodiments, there may be more than 100 percent more storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In various embodiments, there may be at least 200, 300, or 400 percent more

storage capacity in the non-volatile memory subsystem 1040 than in the volatile memory subsystem 1030. In other embodiments, the non-volatile memory subsystem 1040 includes at least some other integer multiples of the storage capacity of the volatile memory subsystem 1030. In some embodiments, the non-volatile memory subsystem 1040 includes a non-integer multiple of the storage capacity of the volatile memory subsystem 1030. In one embodiment, the non-volatile memory subsystem 1040 includes less than 100 percent more storage capacity than does the volatile memory subsystem 1030.

[00156] The extra storage capacity of the non-volatile memory subsystem 1040 can be used to improve the backup capability of the memory system 1010. In certain embodiments in which data can only be written to portions of the non-volatile memory subsystem 1040 which do not contain data (e.g., portions which have been erased), the extra storage capacity of the nonvolatile memory subsystem 1040 allows the volatile memory subsystem 1030 to be backed up in the event of a subsequent power failure or other trigger event. For example, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to backup the volatile memory subsystem 1030 efficiently in the event of multiple trigger conditions (e.g., power failures). In the event of a first power failure, for example, the data in the volatile memory system 1030 is copied to a first, previously erased portion of the nonvolatile memory subsystem 1040 via the controller 1062. Since the non-volatile memory subsystem 1040 has more storage capacity than does the volatile memory subsystem 1030, there is a second portion of the non-volatile memory subsystem 1040 which does not have data from the volatile memory subsystem 1030 copied to it and which remains free of data (e.g., erased). Once system power is restored, the controller 1062 of the memory system 1010 restores the data to the volatile memory subsystem 1030 by copying the backed-up data from the non-volatile memory

subsystem 40 back to the volatile memory subsystem 1030. After the data is restored, the memory system 1010 erases the non-volatile memory subsystem 1040. While the first portion of the non-volatile memory subsystem 1040 is being erased, it may be temporarily inaccessible.

[00157] If a subsequent power failure occurs before the first portion of the non-volatile memory subsystem 1040 is completely erased, the volatile memory subsystem 1030 can be backed-up or stored again in the second portion of the non-volatile memory subsystem 1040 as described herein. In certain embodiments, the extra storage capacity of the non-volatile memory subsystem 1040 may allow the memory system 1010 to operate more efficiently. For example, because of the extra storage capacity of the non-volatile memory subsystem 1040, the memory system 1010 can handle a higher frequency of trigger events that is not limited by the erase time of the non-volatile memory subsystem 1040.

[00158] FIG. 18 is a flowchart of an example method 1300 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. In certain embodiments, the non-volatile memory subsystem 1040 comprises at least 100 percent more storage capacity than does the volatile memory subsystem 30 as described herein. While the method 1300 is described herein by reference to the memory system 1010 schematically illustrated by FIGS. 12-14, the method 1300 can be practiced using other memory systems in accordance with certain embodiments described herein. In an operational block 1310, the method 1300 comprises communicating data between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation. The method 1300 further comprises storing a first copy of data from the

volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a first time when the memory system 1010 is in a second mode of operation in an operational block 1320.

[00159] In an operational block 1330, the method 1300 comprises restoring the first copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030. The method 1300 further comprises erasing the first copy of data from the non-volatile memory subsystem 1040 in an operational block 1340. The method further comprises storing a second copy of data from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 at a second time when the memory system 1010 is in the second mode of operation in an operational block 1350. Storing the second copy begins before the first copy is completely erased from the non-volatile memory subsystem 1040.

[00160] In some embodiments, the memory system 1010 enters the second mode of operation in response to a trigger condition, such as a power failure. In certain embodiments, the first copy of data and the second copy of data are stored in separate portions of the nonvolatile memory subsystem 1040. The method 1300 can also include restoring the second copy of data from the non-volatile memory subsystem 1040 to the volatile memory subsystem 1030 in an operational block 1360. The operational blocks of method 1300 referred to herein may be performed in different orders in various embodiments. For example, in some embodiments, the second copy of data is restored to the volatile memory subsystem 1030 at operational block 1360 before the first copy of data is completely erased in the operational block 1340.

[00161] FIG. 19 schematically illustrates an example clock distribution topology 1400 of a memory system 1010 in accordance with certain embodiments described herein. The clock

distribution topology 1400 generally illustrates the creation and routing of the clock signals provided to the various components of the memory system 1010. A clock source 1402 such as, for example, a 25 MHz oscillator, generates a clock signal. The clock source 1402 may feed a clock generator 1404 which provides a clock signal 1406 to the controller 1062, which may be an FPGA. In one embodiment, the clock generator 1404 generates a 125 MHz clock signal 1406. The controller 1062 receives the clock signal 1406 and uses it to clock the controller 1062 master state control logic. For example, the master state control logic may control the general operation of an FPGA controller 1062.

[00162] The clock signal 1406 can also be input into a clock divider 1410 which produces a frequency-divided version of the clock signal 1406. In an example embodiment, the clock divider 1410 is a divide by two clock divider and produces a 62.5 MHz clock signal in response to the 125 MHz clock signal 1406. A non-volatile memory phase-locked loop (PLL) block 1412 can be included (e.g., in the controller 1062) which distributes a series of clock signals to the non-volatile memory subsystem 1040 and to associated control logic. For example, a series of clock signals 1414 can be sent from the controller 1062 to the non-volatile memory subsystem 1040. Another clock signal 1416 can be used by the controller logic which is dedicated to controlling the non-volatile memory subsystem 1040. For example, the clock signal 1416 may clock the portion of the controller 1062 which is dedicated to generating address and/or control lines for the non-volatile memory subsystem 1040. A feedback clock signal 1418 is fed back into the non-volatile memory PLL block 1412. In one embodiment, the PLL block 1412 compares the feedback clock 1418 to the reference clock 1411 and varies the phase and frequency of its output until the reference 1411 and feedback 1418 clocks are phase and frequency matched.

[00163] A version of the clock signal 1406 such as the backup clock signal 1408 may be sent from the controller to the volatile memory subsystem 1030. The clock signal 1408 may be, for example, a differential version of the clock signal 1406. As described herein, the backup clock signal 1408 may be used to clock the volatile memory subsystem 1030 when the memory system 1010 is backing up the data from the volatile memory subsystem 1030 into the non-volatile memory subsystem 1040. In certain embodiments, the backup clock signal 1408 may also be used to clock the volatile memory subsystem 1030 when the memory system 1010 is copying the backed-up data back into the volatile memory subsystem 1030 from the nonvolatile memory subsystem 1040 (also referred to as restoring the volatile memory subsystem 1030). The volatile memory subsystem 1030 may normally be run at a higher frequency (e.g., DRAM running at 400MHz) than the nonvolatile memory subsystem 1040 (e.g., flash memory running at 62.5MHz) when communicating with the host system (e.g., when no trigger condition is present). However, in certain embodiments the volatile memory subsystem 1030 may be operated at a reduced frequency (e.g., at twice the frequency of the non-volatile memory subsystem 1040) without introducing significant delay into the system during backup operation and/or restore operations. Running the volatile memory subsystem 1030 at the reduced frequency during a backup and/or restore operation may advantageously reduce overall power consumption of the memory system 1010.

[00164] In one embodiment, the backup clock 1408 and the volatile memory system clock signal 1420 are received by a multiplexer 1422, as schematically illustrated by FIG. 19. The multiplexer 1422 can output either the volatile memory system clock signal 1420 or the backup clock signal 1408 depending on the backup state of the memory system 1010. For example, when the memory system 1010 is not performing a backup or restore operation and is

communicating with the host system (e.g., normal operation), the volatile memory system clock signal 1420 may be provided by the multiplexer 422 to the volatile memory PLL block 1424. When the memory system 1010 is performing a backup (or restore) operation, the backup clock signal 1408 may be provided.

[00165] The volatile memory PLL block 1424 receives the volatile memory reference clock signal 1423 from the multiplexer 1422 and can generate a series of clock signals which are distributed to the volatile memory subsystem 1030 and associated control logic. For example, in one embodiment, the PLL block 1424 generates a series of clock signals 1426 which clock the volatile memory elements 1032. A clock signal 1428 may be used to clock control logic associated with the volatile memory elements, such as one or more registers (e.g., the one or more registers of a registered DIMM). Another clock signal 1430 may be sent to the controller 1062. A feedback clock signal 1432 is fed back into the volatile memory PLL block 1424. In one embodiment, the PLL block 1424 compares the feedback clock signal 1432 to the reference clock signal 1423 and varies the phase and frequency of its output until the reference clock signal 1423 and the feedback clock signal 1432 clocks are phase and frequency matched.

[00166] The clock signal 1430 may be used by the controller 1062 to generate and distribute clock signals which will be used by controller logic which is configured to control the volatile memory subsystem 1030. For example, control logic in the controller 1062 may be used to control the volatile memory subsystem 1030 during a backup or restore operation. The clock signal 1430 may be used as a reference clock signal for the PLL block 1434 which can generate one or more clocks 1438 used by logic in the controller 1062. For example, the PLL block 1434 may generate one or more clock signals 1438 used to drive logic circuitry associated with

controlling the volatile memory subsystem 1030. In certain embodiments, the PLL block 1434 includes a feedback clock signal 1436 and operates in a similar manner to other PLL blocks described herein.

[00167] The clock signal 1430 may be used as a reference clock signal for the PLL block 1440 which may generate one or more clock signals used by a sub-block 1442 to generate one or more other clock signals 1444. In one embodiment, for example, the volatile memory subsystem 1030 comprises DDR2 SDRAM elements and the sub-block 1442 generates one or more DDR2 compatible clock signals 1444. A feedback clock signal 1446 is fed back into the PLL block 1440. In certain embodiments, the PLL block 1440 operates in a similar manner to other PLL blocks described herein.

[00168] While described with respect to the example embodiment of FIG. 19, various alternative clock distribution topologies are possible. For example, one or more of the clock signals have a different frequency in various other embodiments. In some embodiments, one or more of the clocks shown as differential signals are single ended signals. In one embodiment, the volatile memory subsystem 1030 operates on the volatile memory clock signal 1420 and there is no backup clock signal 1408. In some embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a backup operation and not during a restore operation. In other embodiments, the volatile memory subsystem 1030 is operated at a reduced frequency during a restore operation and not during a backup operation.

[00169] FIG. 20 is a flowchart of an example method 1500 of controlling a memory system 1010 operatively coupled to a host system. Although described with respect to the memory

system 1010 described herein, the method 1500 is compatible with other memory systems. The memory system 1010 may include a clock distribution topology 1400 similar to the one described above with respect to FIG. 19 or another clock distribution topology. The memory system 1010 can include a volatile memory subsystem 30 and a non-volatile memory subsystem 1040.

[00170] In an operational block 1510, the method 1500 comprises operating the volatile memory subsystem 1030 at a first frequency when the memory system 1010 is in a first mode of operation in which data is communicated between the volatile memory subsystem 1030 and the host system. In an operational block 1520, the method 1500 comprises operating the non-volatile memory subsystem 1040 at a second frequency when the memory system 1010 is in a second mode of operation in which data is communicated between the volatile memory subsystem 1030 and the non-volatile memory subsystem 1040. The method 1500 further comprises operating the volatile memory subsystem 1030 at a third frequency in an operational block 1530 when the memory system 1010 is in the second mode of operation. In certain embodiments, the memory system 1010 is not powered by a battery when it is in the second mode of operation. The memory system 1010 may switch from the first mode of operation to the second mode of operation in response to a trigger condition. The trigger condition may be any trigger condition described herein such as, for example, a power failure condition. In certain embodiments, the second mode of operation includes both backup and restore operations as described herein. In other embodiments, the second mode of operation includes backup operations but not restore operations. In yet other embodiments, the second mode of operation includes restore operations but not backup operations.

[00171] The third frequency can be less than the first frequency. For example, the third frequency can be approximately equal to the second frequency. In certain embodiments, the reduced frequency operation is an optional mode. In yet other embodiments, the first, second and/or third frequencies are configurable by a user or by the memory system 1010.

[00172] FIG. 21 schematically illustrates an example topology of a connection to transfer data slices from two DRAM segments 1630, 1640 of a volatile memory subsystem 1030 of a memory system 1010 to a controller 1062 of the memory system 1010. While the example of FIG. 21 shows a topology including two DRAM segments 1630, 1640 for the purposes of illustration, each address location of the volatile memory subsystem 1030 comprises more than the two segments in certain embodiments. The data lines 1632, 1642 from the first DRAM segment 1630 and the second DRAM segment 1640 of the volatile memory subsystem 1030 are coupled to switches 1650, 1652 which are coupled to the controller 1062 (e.g., logic element 1070) of the memory system 1010. The chip select lines 1634, 1644 and the self-refresh lines 1636, 1646 (e.g., CKE signals) of the first and second DRAM segments 1630, 1640, respectively, are coupled to the controller 1062. In certain embodiments, the controller 1062 comprises a buffer (not shown) which is configured to store data from the volatile memory subsystem 1030. In certain embodiments, the buffer is a first-in, first out buffer (FIFO). In certain embodiments, data slices from each DRAM segment 1630, 1640 comprise a portion of the volatile memory subsystem data bus. In one embodiment, for example, the volatile memory subsystem 1030 comprises a 72-bit data bus (e.g., each data word at each addressable location is 72 bits wide and includes, for example, 64 bits of accessible SDRAM and 8 bits of ECC), the first data slice from the first DRAM segment 1630 may comprise 40 bits of the data word, and the second data slice

from the second DRAM segment 1640 may comprise the remaining 32 bits of the data word. Certain other embodiments comprise data buses and/or data slices of different sizes.

[00173] In certain embodiments, the switches 1650, 1652 can each be selectively switched to selectively operatively couple the data lines 1632, 1642, respectively from the first and second DRAM segments 1630, 1640 to the controller 1062. The chip select lines 1634, 1644 enable the first and second DRAM segments 1630, 1640, respectively, of the volatile memory subsystem 1030, and the self-refresh lines 1636, 1646 toggle the first and second DRAM segments 1630, 1640, respectively, from self-refresh mode to active mode. In certain embodiments, the first and second DRAM segments 1630, 1640 maintain stored information but are not accessible when they are in self-refresh mode, and maintain stored information and are accessible when they are in active mode.

[00174] In certain embodiments, when the memory system 1010 is backing up the volatile memory system 1030, data slices from only one of the two DRAM segments 1630, 1640 at a time are sent to the controller 1062. For example, when the first slice is being written to the controller 1062 during a back-up, the controller 1062 sends a signal via the CKe line 1636 to the first DRAM segment 1630 to put the first DRAM segment 1630 in active mode. In certain embodiments, the data slice from the first DRAM segment 1630 for multiple words (e.g., a block of words) is written to the controller 1062 before writing the second data slice from the second DRAM segment 1640 to the controller 1062. While the first data slice is being written to the controller 1062, the controller 1062 also sends a signal via the CKe line 1646 to put the second DRAM segment 1640 in self-refresh mode. Once the first data slice for one word or for a block of words is written to the controller 1062, the controller 1062 puts the first DRAM segment 1630

into self-refresh mode by sending a signal via the CKe line 1636 to the first DRAM segment 1640. The controller 1062 also puts the second DRAM segment 1640 into active mode by sending a signal via the CKe line 1646 to the DRAM segment 1640. The second slice for a word or for a block of words is written to the controller 1062. In certain embodiments, when the first and second data slices are written to the buffer in the controller 1062, the controller 1062 combines the first and second data slices 1630, 1640 into complete words or blocks of words and then writes each complete word or block of words to the non-volatile memory subsystem 1040. In certain embodiments, this process is called "slicing" the volatile memory subsystem 1030.

[00175] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1042 write each backed-up data word to the controller 1062 which writes a first slice of the data word to the volatile memory subsystem 1030 and then a second slice of the data word to the volatile memory subsystem 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00176] FIG. 22 is a flowchart of an example method 1600 of controlling a memory system 1010 operatively coupled to a host system and which includes a volatile memory subsystem 1030 and a non-volatile memory subsystem 1040. Although described with respect to the memory system 1010 described herein with respect to FIGS. 12-14 and 21, the method 1600 is compatible with other memory systems. The method 1600 comprises communicating data words between the volatile memory subsystem 1030 and the host system when the memory system 1010 is in a first mode of operation in an operational block 1610. For example, the memory

system 1010 may be in the first mode of operation when no trigger condition has occurred and the memory system is not performing a backup and/or restore operation or is not being powered by a secondary power supply.

[00177] In an operational block 1620, the method further comprises transferring data words from the volatile memory subsystem 1030 to the non-volatile memory subsystem 1040 when the memory system 1010 is in a second mode of operation. In certain embodiments, each data word comprises the data stored in a particular address of the memory system 1010. The memory system 1010 may enter the second mode of operation, for example, when a trigger condition (e.g., a power failure) occurs. In certain embodiments, transferring each data word comprises storing a first portion (also referred to as a slice) of the data word in a buffer in an operational block 1622, storing a second portion of the data word in the buffer in an operational block 1624, and writing the entire data word from the buffer to the non-volatile memory subsystem 1040 in an operational block 1626.

[00178] In one example embodiment, the data word may be a 72 bit data word (e.g., 64 bits of accessible SDRAM and 8 bits of ECC), the first portion (or "slice") may comprise 40 bits of the data word, and the second portion (or "slice") may comprise the remaining 32 bits of the data word. In certain embodiments, the buffer is included in the controller 1062. For example, in one embodiment, the buffer is a first-in, first-out buffer implemented in the controller 1062 which comprises an FPGA. The method 1600 may generally be referred to as "slicing" the volatile memory during a backup operation. In the example embodiment, the process of "slicing" the volatile memory during a backup includes bringing the 32-bit slice out of self-refresh, reading a 32-bit block from the slice into the buffer, and putting the 32-bit slice back into self-refresh. The

40-bit slice is then brought out of self-refresh and a 40-bit block from the slice is read into a buffer. Each block may comprise a portion of multiple words. For example, each 32-bit block may comprise 32-bit portions of multiple 72-bit words. In other embodiments, each block comprises a portion of a single word. The 40-bit slice is then put back into self-refresh in the example embodiment. The 32-bit and 40-bit slices are then combined into a 72-bit block by the controller 1062 and ECC detection/correction is performed on each 72-bit word as it is read from the buffer and written into the non-volatile memory subsystem (e.g., flash).

[00179] In some embodiments, the entire data word may comprise more than two portions. For example, the entire data word may comprise three portions instead of two and transferring each data word further comprises storing a third portion of each data word in the buffer. In certain other embodiments, the data word may comprise more than three portions.

[00180] In certain embodiments, the data may be sliced in a restore operation as well as, or instead of, during a backup operation. For example, in one embodiment, the nonvolatile memory elements 1040 write each backed-up data word to the controller 1062 which writes a first portion of the data word to the volatile memory subsystem 1030 and then a second portion of the data word to the volatile memory 1030. In certain embodiments, slicing the volatile memory subsystem 1030 during a restore operation may be performed in a manner generally inverse to slicing the volatile memory subsystem 1030 during a backup operation.

[00181] The method 1600 can advantageously provide significant power savings and can lead to other advantages. For example, in one embodiment where the volatile memory subsystem 1030 comprises DRAM elements, only the slice of the DRAM which is currently being accessed

(e.g., written to the buffer) during a backup is configured in full-operational mode. The slice or slices that are not being accessed may be put in self-refresh mode. Because DRAM in self-refresh mode uses significantly less power than DRAM in full-operational mode, the method 1600 can allow significant power savings. In certain embodiments, each slice of the DRAM includes a separate self-refresh enable (e.g., CKe) signal which allows each slice to be accessed independently.

[00182] In addition, the connection between the DRAM elements and the controller 1062 may be as large as the largest slice instead of as large as the data bus. In the example embodiment, the connection between the controller 1062 and the DRAM may be 40 bits instead of 72 bits. As a result, pins on the controller 1062 may be used for other purposes or a smaller controller may be used due to the relatively low number of pin-outs used to connect to the volatile memory subsystem 1030. In certain other embodiments, the full width of the data bus is connected between the volatile memory subsystem 1030 and the controller 1062 but only a portion of it is used during slicing operations. For example, in some embodiments, memory slicing is an optional mode.

[00183] While embodiments and applications have been shown and described, it would be apparent to those skilled in the art having the benefit of this disclosure that many more modifications than mentioned above are possible without departing from the inventive concepts disclosed herein. The invention, therefore, is not to be restricted except in the spirit of the appended claims.

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PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/328,019		Filing Date 05/24/2021		☐ To be Mailed				
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO												
APPLICATION AS FILED - PART I												
		(Column 1)	(Column 2)									
FOR		NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)					
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A	N/A		N/A							
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A	N/A		N/A							
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A	N/A		N/A							
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *		x \$100 =								
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *		x \$480 =								
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).										
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))												
* If the difference in column 1 is less than zero, enter "0" in column 2.					TOTAL							
APPLICATION AS AMENDED - PART II												
		(Column 1)		(Column 2)	(Column 3)							
AMENDMENT	06/04/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)				
	Total (37 CFR 1.16(i))	* 30	Minus	** 20	= 10	x \$100 =		1000				
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0	x \$480 =		0				
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
								TOTAL ADD'L FEE		1000		
		(Column 1)		(Column 2)	(Column 3)							
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)				
	Total (37 CFR 1.16(i))	*	Minus	**	=	x \$0 =						
	Independent (37 CFR 1.16(h))	*	Minus	***	=	x \$0 =						
	☐ Application Size Fee (37 CFR 1.16(s))											
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))											
								TOTAL ADD'L FEE				
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.						LDRC						
** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".						/EVA V GILLIS/						
*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".												
The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.												

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	Attorney Docket Number		0016.0010001

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**INFORMATION DISCLOSURE
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Application Number	17328019
Filing Date	2021-05-24
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Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
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	5	Amendment and Reply to Office Action, SanDisk Corporation v. Netlist, Application No. 13/536,173, IPR2014-00982 (PTAB), dated May 21, 2013, 24 pages.	
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	7	American Heritage Dictionary of the English Language, Third Ed., Houghton Mifflin Company, Boston, MA, 1996, 7 pages.	
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10	Annotated added to Russel Jacob Baker Deposition, Exhibit 1027, p.79, Patent No. 8, 671,243, Case No. IPR-2017-00587 (PTAB), filed December 18, 2017, 1 page.
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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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10	Notice of Allowance in U.S. Appl. No. 12/240,916 dated Sep. 17, 2012, pp. 1-7.
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14	Notice of Allowance in U.S. Appl. No. 13/559,476, dated Sep. 29, 2014.
15	Notice of Allowance in U.S. Appl. No. 13/905,048, dated Dec. 19, 2013, 8 pages.
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45	Out of Stealth Mode, Start-Up MetaRAM Unveils New Technology That Quadruples DRAM Capacity, Press Release edited by Storage Newsletter on Feb. 28, 2008 at StorageNewsLetter.com, 8 pages.
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47	Patent Owner's Listing of New Arguments and Evidence in Petitioners' Reply, Patent No. 8,671,243, Case No. IPR2017-00587 (PTAB), filed Jan. 29, 2018, 6 pages.
48	Patent Owner's Opposition to Petitioners' Motion to Exclude, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed April 2, 2018, 2017, 11 pages.
49	Patent Owner's Preliminary Response, Patent Number: 8,516,187, Case IPR2014-01371 (PTAB), filed Dec. 16, 2014, 66 pages.
50	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), Paper 8, dated October 2, 2014, 60 pages.

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17328019
	Filing Date		2021-05-24
	First Named Inventor	Chi-She Chen	
	Art Unit		
	Examiner Name		
	Attorney Docket Number		0016.0010001

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**INFORMATION DISCLOSURE
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Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
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Attorney Docket Number	0016.001000I	

1	Exhibit, Application As Filed, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), 52 pages
2	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-3, filed March 17, 2015, 23 pages.
3	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-4, filed March 17, 2015, 20 pages.
4	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-5, filed March 17, 2015, 28 pages.
5	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-9, filed March 17, 2015, 17 pages.
6	Exhibit 12, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-7, filed March 17, 2015, 17 pages.
7	Exhibit 9, Email from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-17, filed March 10, 2015, 6 pages.
8	Exhibit, Institution of Inter Partes Review, Sandisk Corporation v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 316-9, filed March 24, 2015, 29 pages.
9	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.
10	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.
11	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-2, filed March 17, 2015, 23 pages.

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12	Exhibit, Letter from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-16, filed March 10, 2015, 3 pages.
13	Exhibit, Letter sent via email on December 6, 2013, Case 4:13-cv-03901-YGR Document 53-2, filed January 6, 2014
14	Exhibit, Order Denying Defendant's Motion to Stay Pending Inter Partes Review (Doc.59), The Procter and Gamble Company v. Team Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 316-6, filed March 24, 2015, 10 pages.
15	Exhibit, Patent Public Advisory Committee Quarterly Meeting, Appeals Statistics USPTO, Case No. 4:13-cv-05889-YGR Document 309-8, filed March 17, 2015, 23 pages.
16	Exhibit, Reporter's Transcript of Proceedings, Netlist, Inc v. Smart Modular Technologies, Inc., et al., Case 4:13-cv-05889-YGR Document 316-3, filed March 24, 2015, 15 pages.
17	Exhibit, Transcript of Official Electronic Sound Recording Proceeding, Netlist v. Smart Modular Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 305-7, filed March 10, 2015, 10 pages.
18	Extended European Search Report for European Application No. 12 817 751.6, dated Jun. 9, 2015.
19	File History for U.S. Appl. No. 12/240,916, filed Sep. 29, 2008, 320 pages.
20	File History for U.S. Appl. No. 13/905,048, filed May 29, 2013, 181 pages.
21	File History for U.S. Appl. No. 60/941,586, filed Jun. 1, 2007, 23 pages.
22	File History U.S. Pat. No. 8,671,243.

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23	Final Office Action, dated Jun. 15, 2016, dated in U.S. Appl. No. 14/489,281, 10 pages.
24	Final Office Action, dated Jun. 15, 2016, issued in U.S. Appl. No. 14/489,281, 10 pages.
25	Final Office Action, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-0099-1007 (PTAB), dated February 1, 2012, 13 pages
26	Final Written Decision, Patent 8,671,243, IPR2017-00587-34, Paper No. 34, entered June 20, 2018, 53 pages.
27	Final Written Decision, Patent 8,874,831, IPR2017-00692, Paper No. 25, entered July 5, 2018, 42 pages.
28	Final Written Decision, US Patent No. 7,881,150, Case No. Case IPR2014-00882, (PTAB), Paper 33, filed December 14, 2015, 51 pages.
29	First Amended Complaint for Patent Infringement, Netlist Inc. v Smart Modular Tech, Inc., et al., Case 8:13-cv-00996-DOC-JPR, Document 5, filed Aug. 23, 2013, 99 pages.
30	Hasan, J. et al. Efficient Use of Memory Bandwidth to Improve Network Processor Throughput, Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA'03), IEEE, 2003, 12 pages.
31	Horowitz, P. et al., "The Art of Electronics", Cambridge University Press 2nd Ed. 1989, pp. 471, 495-496.
32	Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.
33	Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18), 2003, 100 pages.

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34	Inter Partes Review No. IPR2017-00692 (PTAB), Patent No. 8,874,831, filed July 26, 2012, 78 pages.
35	Inter Partes Review of U.S. Patent No. 8,874,831, Case IPR2017-00692 (PTAB), filed July 26, 2012, Paper No. 1, 78 pages.
36	International Preliminary Report on Patentability in PCT/US12/48750, mailed Apr. 3, 2014.
37	International Preliminary Report on Patentability in PCT/US12/48750, mailed Apr. 3, 2014, pp. 1-8.
38	International Search Report and Written Opinion in PCT/US12/48750, dated Oct. 10, 2012, pp. 1-10.
39	ISSCC 2006 / SESSION 7 / NON-VOLATILE MEMORY / 7.7, IEEE International Solid-State Circuits Conference, 2006, 10 pages.
40	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322, 58 pages.
41	Jandhyala, S. et al., "Design-For-Test Analysis of a Buffered SDRAM DIMM", Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, Aug. 13014, 1996, 15 pages.
42	JEDEC Definition of DIMM, Exhibit 1029, IPR No. 2017-00587, December 18, 2017, 2 pages.
43	JEDEC Global Standard for the Microelectronics Industry, Why JEDEC Standards Matter, 2014, 1 page.
44	JEDEC Standard 21-C, "Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18.

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45	JEDEC Standard No. 21-C (Release 17), Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3), 60 pages.
46	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, Aug. 1999, 114 pages.
47	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) Jan. 2005, 113 pages.
48	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79, Jun. 2000, 77 pages.
49	JEDEC Standard, Double Data Rate (DDR): SDRAM Specification: JESD79C (Revision JESD79B), Mar. 2003, pp. 1-75.
50	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification: JESD205, JEDEC Solid State Tech. Assoc., Mar. 2007, 129 pages.

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Name/Print	Khaled Shami	Registration Number	38745

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Attorney Docket Number	0016.001000I

1	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Patent Number: 8,516,187, IPR2014-00982 (PTAB), dated September 26, 2014, 57 pages.
2	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,301,833, Case No. IPR2017-00649 (PTAB), filed May 1, 2017, 67 pages.
3	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed May 1, 2017, 48 pages.
4	Patent Owner's Preliminary Response, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, Case IPR2014-01370 (PTAB), filed Dec. 16, 2014, 66 pages.
5	Patent Owner's Response, Patent No. 8,671,243, Case No. IPR2017-00587-12 (PTAB), filed Oct. 13, 2017, 80 pages.
6	Patent Owner's Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692-12 (PTAB), filed Nov. 10, 2017, 77 pages.
7	Patterson et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998), 71 pages.
8	Petition for Inter Partes Review of Claims 1-30 of US.PATENT No. 8,301,833, IPR2014-01370 (PTAB), filed August 22, 2014, 68 pages.
9	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.
10	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
11	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833, filed Sep. 29, 2008.

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12	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.
13	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
14	Petition for Inter Partes Review of U.S. Pat. No. 8,671,243, filed May 29, 2013.
15	Petition for Inter Partes Review of U.S. Pat. No. 8,874,831, filed Jul. 26, 2012.
16	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.
17	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
18	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.
19	Petition for Inter Partes Review of US Patent 8,516,187, IPR2014-00982 (PTAB), dated June 19, 2014, 67 pages.
20	Petition for Inter Partes Review of US Patent No. 8,671,243, Case No. IPR2017-00587-1(PTAB), May 29, 2013, 82 pages.
21	Petition for Inter Partes Review, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), filed June 20, 2014, 69 pages.
22	Petition for Inter Parties Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.

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23	Petition for Inter Parties Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 192014.
24	Petitioners Demonstratives, SK hynix Inc., et al., v. Netlist, Inc., U.S. Patent No. 8,671,243, IPR2017-00587-1037, 89 pages.
25	Petitioners' Reply in Support of Its Motion to Exclude, U.S. Patent No. 8,874,831, Case No. IPR2017-00692, filed April 9, 2018, 8 pages.
26	Petitioners' Reply to Patent Owner's Response, Inter Partes Review No. IPR2017-00587-16, Patent No. 8,671,243, filed Jan. 12, 2018, 38 pages.
27	Petitioners' Reply, U.S. Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), Paper No. 15, filed March 2, 2018, 35 pages.
28	Petitioners' Request for Hearing, U.S. Patent No. 8,301,833, Case No. Case No. IPR2017-00649-2020 (PTAB), Paper No. 8, entered Aug, 23, 2017, 18 pages.
29	Prosecution History, Application No. 12,240,916, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date April 13, 2009, 320 pages.
30	Prosecution History, Application No. 13,559,476, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date Sep. 5, 2014, 312 pages.
31	Prosecution History, Provisional Application No. 60/941,586, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1005 (PTAB), received date Oct. 15, 2012, 23 pages.
32	Provisional Application for Advance Dynamic Disk Memory Module, Specification, SK hynix Inc., V. Netlist, Inc., Case No. IPR2017-00649-1006 (PTAB), dated Dec. 8, 2005, 53 pages.
33	Provisional Application No. 60/912,321 filed Apr. 17, 2007.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.001000I

34	Provisional Application No. 60/941,586 filed Jun. 1, 2007.
35	Requirement for Restriction Election, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994-1003 (PTAB), dated March 31, 2019, 7 pages.
36	Restriction Requirement in U.S. Appl. No. 12/240,916, dated Mar. 31, 2011.
37	Second Amended Answer and Counterclaims to Plaintiff's Complaint for Declaratory Judgment, Diablo Technologies, Inc. v. Netlist, Inc., Case No. 4:13-CV-03901 (NDCA), YGR, filed February 17, 2014, 21 pages.
38	Smart Storage Systems, Inc's Invalidity Contentions, Netlist, Inc. v Smart Storage Systems, et al., Case No. 4:13-cv-05889-YGR, dated Jun. 6, 2014, 538 pages.
39	Supplemental Declaration of Daniel E. Alberti in Response to Court Order [Docket No. 361] in Support of Motion to Withdraw as Counsel of Record, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 362, filed September 5, 2018, 3 pages.
40	Supplemental Declaration of Ronald H. Spuhler, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-1, filed March 10, 2015, 2 pages.
41	Supplemental Declaration of Steven J. Corr, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 309, filed March 17, 2015, 3 pages.
42	Switches - D&T Online, Switches, http://wiki.dtonline.org , Exhibit 1022, Case No. IPR2017-00587, accessed October 13, 2017, 3 pages.
43	U.S. Appl. No. 60/912,321, filed Apr. 17, 2007.
44	U.S. Office Action in U.S. Appl. No. 13/536,173, mailed on Apr. 15, 2013, pp. 1-10.

**INFORMATION DISCLOSURE
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Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
Art Unit		
Examiner Name		
Attorney Docket Number	0016.001000I	

45	Updated Joint Case Management Statement, Case No. 4:13-cv-03916-YGR (NDCA), Document 53, filed Jan. 6, 2014.
46	US Patent Application No. 12/240,916, Case No. IPR2017-00692-2018 (PTAB), dated Sep. 29, 2008, 52 pages.
47	US Patent Application No. 60/912,321, Case No. No. IPR2017-00692-1007 (PTAB), filed April 17, 2017, 42 pages.
48	Using Two Chip Selects to Enable Quad Rank, an IP.com Prior Art Database Technical Disclosure, IP.com Electronic Publication: Dec. 17, 2005, 2 pages.
49	Videotaped Deposition of Russel Jacob Baker, Patent No. 8,671,243, Case Nos. IPR2017-00587-1030 (PTAB), filed December 18, 2017, 268 pages.
50	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 257, 259; 1114,1115, Exhibit 1017, IPR2014-01370 (PTAB), Smart Modular Tech v Netlist Inc, Patent No. 8,301,833, Sep. 22, 2014, 5 pages.

If you wish to add additional non-patent literature document citation information please click the Add button

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Examiner Signature		Date Considered	
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17328019
	Filing Date	2021-05-24
	First Named Inventor	Chi-She Chen
	Art Unit	
	Examiner Name	
	Attorney Docket Number	0016.0010001

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(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.001000I

1	Wong, A., The BIOS Optimization Guide, Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.
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Filing Date	2021-05-24
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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONFIRMATION NO.: 6552

SERIAL NO.: 17/328,019

ART UNIT: 2135

FILING DATE: 05-24-2021

EXAMINER: TBA

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

**Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Commissioner:

Notice of Related Litigation and/or Proceedings

Pursuant to MPEP 2001.06(c), Applicant notifies the Patent and Trademark Office of litigation and proceedings involving U.S. Patents related to the current patent application, the subject matter of which may be related to the present patent application.

Appendix A lists results of a Cases Search. The Cases Search was performed on June 16, 2021, on the Docket Navigator™ search tool for patent cases involving commonly-owned U.S. Patents No. 8,301,833, 8,516,187, 8,671,243, and 8,874,831. The Cases Search covered forums including U.S. federal courts, ITC, and PTAB. The Cases Search results presented includes information output by the search tool for the following fields: Case, Case Filing Date, Case Status Case Terminated, and Case Name.

Notification of the cases and proceedings identified in the attached Notice in no way operates as an admission that documents cited or filed in those cases and proceedings are material to the

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The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 60-2034.

Respectfully submitted,

SHAMI MESSINGER PLLC

Dated: June 22, 2021

/Khaled Shami/
Khaled Shami
Reg. No. 38,745

SHAMI MESSINGER PLLC
1000 Wisconsin Ave N.W., Suite 200
Washington, D.C. 20007
Tel: 202-516-6900

Cases

12 Results

Patents: 8301833, 8516187, 8671243, 8874831

	Case	Case Filing Date	Case Status	Case Termination Date	Case Name
	Netlist, Inc. v. Micron Technology, Inc. et al 6-21-cv-00430 (WDTX)	Apr. 28, 2021	Active		Netlist, Inc. v. Micron Technology, Inc. et al
	<u>Number</u> 8301833	<u>Inventor</u> Chen	<u>Name</u> Non-volatile memory module		
	SK hynix Inc. et al v. Netlist, Inc. IPR2017-00692 (PTAB)	Jan. 17, 2017	Terminated	Jul. 05, 2018	SK hynix Inc. et al v. Netlist, Inc.
	<u>Number</u> 8874831	<u>Inventor</u> Lee	<u>Name</u> Flash-DRAM hybrid memory module		
	SK hynix Inc. v. Netlist, Inc. IPR2017-00649 (PTAB)	Jan. 13, 2017	Terminated	May. 29, 2018	SK hynix Inc. v. Netlist, Inc.
	<u>Number</u> 8301833	<u>Inventor</u> Chen	<u>Name</u> Non-volatile memory module		
	SK hynix Inc. et al v. Netlist, Inc. IPR2017-00587 (PTAB)	Jan. 06, 2017	Terminated	Jun. 20, 2018	SK hynix Inc. et al v. Netlist, Inc.
	<u>Number</u> 8671243	<u>Inventor</u> Chen	<u>Name</u> Isolation switching for backup memory		
	SMART Modular Technologies Inc. v. Netlist, Inc. IPR2014-01370 (PTAB)	Aug. 23, 2014	Terminated	Apr. 30, 2015	SMART Modular Technologies Inc. v. Netlist, Inc.
	<u>Number</u> 8301833	<u>Inventor</u> Chen	<u>Name</u> Non-volatile memory module		
	SMART Modular Technologies Inc. v. Netlist, Inc. IPR2014-01371 (PTAB)	Aug. 23, 2014	Terminated	Apr. 30, 2015	SMART Modular Technologies Inc. v. Netlist, Inc.
	<u>Number</u> 8516187	<u>Inventor</u> Chen	<u>Name</u> Data transfer scheme for non-volatile memory module		
	SanDisk Corporation v. Netlist, Inc. IPR2014-00994 (PTAB)	Jun. 20, 2014	Terminated	Jun. 02, 2015	SanDisk Corporation v. Netlist, Inc.
	<u>Number</u> 8301833	<u>Inventor</u> Chen	<u>Name</u> Non-volatile memory module		
	SanDisk Corporation v. Netlist, Inc. IPR2014-00982 (PTAB)	Jun. 19, 2014	Terminated	Jun. 03, 2015	SanDisk Corporation v. Netlist, Inc.
	<u>Number</u> 8516187	<u>Inventor</u> Chen	<u>Name</u> Data transfer scheme for non-volatile memory module		
	Netlist, Inc. v. Smart Modular Technologies, Inc. et al 4-13-cv-05889 (NDCA)	Dec. 19, 2013	Terminated	May. 19, 2020	Netlist, Inc. v. Smart Modular Technologies, Inc. et al
	<u>Number</u> 7381150	<u>Inventor</u> Solomon	<u>Name</u> Circuit providing load isolation and memory domain translation for memory module		
	8001434	Lee	Memory board with self-testing capability		
	8081536	Solomon	Circuit for memory module		
	8301833	Chen	Non-volatile memory module		
	8359501	Lee	Memory board with self-testing capability		
	8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module		
	8516187	Chen	Data transfer scheme for non-volatile memory module		

	Diablo Technologies, Inc. v. Netlist, Inc. 4-13-cv-03901 (NDCA)	Aug. 23, 2013	Terminated	Apr. 08, 2014	Diablo Technologies, Inc. v. Netlist, Inc.
	<u>Number</u>	<u>Inventor</u>	<u>Name</u>		
	7881150	Solomon	Circuit providing load isolation and memory domain translation for memory module		
	8001434	Lee	Memory board with self-testing capability		
	8081536	Solomon	Circuit for memory module		
	8301833	Chen	Non-volatile memory module		
	8359501	Lee	Memory board with self-testing capability		
	8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module		
	8516187	Chen	Data transfer scheme for non-volatile memory module		
	Smart Modular Technologies, Inc. v. Netlist, Inc. 4-13-cv-03916 (NDCA)	Aug. 23, 2013	Terminated	Feb. 12, 2014	Smart Modular Technologies, Inc. v. Netlist, Inc.
	<u>Number</u>	<u>Inventor</u>	<u>Name</u>		
	8001434	Lee	Memory board with self-testing capability		
	8301833	Chen	Non-volatile memory module		
	8359501	Lee	Memory board with self-testing capability		
	8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module		
	8516187	Chen	Data transfer scheme for non-volatile memory module		
	Netlist, Inc. v. Smart Modular Technologies, Inc. 8-13-cv-00996 (CDCA)	Jul. 01, 2013	Terminated	Dec. 23, 2013	Netlist, Inc. v. Smart Modular Technologies, Inc.
	<u>Number</u>	<u>Inventor</u>	<u>Name</u>		
	8001434	Lee	Memory board with self-testing capability		
	8301833	Chen	Non-volatile memory module		
	8359501	Lee	Memory board with self-testing capability		
	8516185	Lee	System and method utilizing distributed byte-wise buffers on a memory module		
	8516187	Chen	Data transfer scheme for non-volatile memory module		

Electronic Acknowledgement Receipt

EFS ID:	43017467
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Susanh Perez
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	0016.0010001
Receipt Date:	22-JUN-2021
Filing Date:	24-MAY-2021
Time Stamp:	13:55:05
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	NPL2_1_OF_5_240pin_DDR2_ MetaSDRAM_Registered_DIMM .pdf	1937315 ce8d661768da4826c666025788c3c0f254d bdd54	no	32

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Samsung Electronics Co., Ltd.

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Information:					
2	Non Patent Literature	NPL4_1_OF_5_Amazoncom_search_for_memory_module_downloaded_oct_12_2017.pdf	886882	no	6
			4ce418ee7dfc288864a1c0c0e70cfc25d3f73f20		
Warnings:					
Information:					
3	Non Patent Literature	NPL8_1_OF_5_American_National_Standard_Dictionary_of_Electrical_Terms.pdf	1669432	no	6
			bace5d872a5904a2bc1f9cb3165cdc84d7e34ec0		
Warnings:					
Information:					
4	Non Patent Literature	NPL9_1_OF_5_Annotated_added_to_Russel_Jacob_Baker_Deposition_Exhibit_1026.pdf	174992	no	1
			a853db46bf1006bcbcf41fbcd10270a2053547a1		
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5	Non Patent Literature	NPL10_1_OF_5_Annotated_added_to_Russel_Jacob_Baker_Deposition_Exhibit_1027.pdf	173996	no	1
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Warnings:					
Information:					
6	Non Patent Literature	NPL11_1_OF_5_Annotated_added_to_Russel_Jacob_Baker_Deposition_Exhibit_1028.pdf	1310232	no	1
			7437b919cf8d136e27a31f76284fac9952e0462a		
Warnings:					
Information:					
7	Non Patent Literature	NPL13_1_OF_5_Bonella_Provisional_Application_for_Advance .pdf	2290471	no	53
			d8b0cc758ee1868dee5989da5001719dced46e47		
Warnings:					
Information:					
8	Non Patent Literature	NPL14_1_OF_5_Bruce_Synchronous_DRAM_Architectures_Organizations.pdf	2371060	no	22
			d9f314453c9cb4d99edbb43dde5334a7d87d04a7		
Warnings:					
Information:					

9	Non Patent Literature	NPL15_1_OF_5_Catsoulis_Designing_Embedded_Hardware.pdf	6720819	no	67
			5eda2233c917c4a752f612c2602ea3bffa90d		
Warnings:					
Information:					
10	Non Patent Literature	NPL20_1_OF_5_Chiappetta_Kingston_Launches_667_MHz_DDR2SO_DIMM_Memory.pdf	471952	no	3
			471992d6253a7cc0e25737d32114d553e8975d94		
Warnings:					
Information:					
11	Non Patent Literature	NPL21_1_OF_5_Copy_of_Notice_of_Final_Rejection_KR.pdf	80109	no	4
			b728e511b3dc6439a8e2d2693cfd8949dc0742c9		
Warnings:					
Information:					
12	Non Patent Literature	NPL22_1_OF_5_Copy_of_Notice_of_Submission_of_Opinion_KR.pdf	251796	no	6
			be5637c443deb85bf0c710cffe14470f107e2fb		
Warnings:					
Information:					
13	Non Patent Literature	NPL27_1_OF_5_David_H_Fully_Buffered_DIMM_FBDIMM_Design_Considerations.pdf	21690036	no	36
			32dc0eecefd0948a38e40f3119035873399013d6		
Warnings:					
Information:					
14	Non Patent Literature	NPL28_1_OF_5_Decision_Denying_Institution_of_Inter_Parties_Review_PTAB_IPR2017_00649_7_july242017.pdf	247510	no	17
			9dac6f19e96b6e02365cf94f1ef630734ef54fb4		
Warnings:					
Information:					
15	Non Patent Literature	NPL34_1_OF_5_Decision_Instituting_Inter_Parties_Review_PTAB_IPR2017-00692_7.pdf	763751	no	29
			8388eddb68ce58cbb56e925c409f71e9e8f8428e		
Warnings:					
Information:					

16	Non Patent Literature	NPL46_1_OF_5_Netlist_v_Smart_Storage_System_v_DiabloTechnologies_invalidity_CaseNo_413cv05889.pdf	10600473	no	109
			7ff547c9fc85d5fd7bec808fed93062f58202ecb		
Warnings:					
Information:					
17	Non Patent Literature	NPL48_1_OF_5_ElmhurstD_A18_V_128MB_125MHZ_Multilevel_Cell.pdf	740560	no	5
			40dd6ef368ac56b46c56d21f43715db359cedb19		
Warnings:					
Information:					
18	Non Patent Literature	NPL49_1_OF_5_Ex_1004_IPR2017_00587_Ron_Maltiel_CV.pdf	300416	no	7
			70012dbe1f7712db39f15d1a9fb21d4df3f78fd6		
Warnings:					
Information:					
19	Non Patent Literature	NPL6_2_OF_5_Exhibit_12_Decision_Denying_Institution_of_Inter_Parties_Review.pdf	362253	no	17
			3b3ba8fe0c7ad56d8260ea95f8ab3587d1de9a43		
Warnings:					
Information:					
20	Non Patent Literature	NPL7_2_OF_5_Exhibit_9_Email_from_Defendants_Counsel.pdf	156463	no	6
			7156668594dd36fe0b9c4a88f0faa3fcc14d4ad8		
Warnings:					
Information:					
21	Non Patent Literature	NPL50_2_OF_5_JEDEC_Standard_FBDIMM_Specification_DDR2.pdf	2344051	no	129
			db293ffbe725ade4e3f3ab6c1ce382f647026fd4		
Warnings:					
Information:					
22	Non Patent Literature	NPL4_3_OF_5_MetaRAM_Develops_New_Technology.pdf	468176	no	3
			4328a50092b9eaa86184718f0f199ed050648ee8		
Warnings:					
Information:					

23	Non Patent Literature	NPL9_3_OF_5_MutnuaryB_Analysis_of_Fully_Buffered_DIMM.pdf	1450795	no	7
			90ed23396568e94f53b629d3a89e55bc8a75f15a		
Warnings:					
Information:					
24	Non Patent Literature	NPL19_3_OF_5_NOA_Appl_17138766_3_24_2021_H.pdf	556204	no	10
			c8c4fe8e16429c6e676080274d74624a8fa32e79		
Warnings:					
Information:					
25	Non Patent Literature	NPL34_3_OF_5_OA_Appl_15934416_4_2_2021_G.pdf	969167	no	21
			f1a17ef0d2bcbdf6f4baa6a4033161f7c90c5012		
Warnings:					
Information:					
26	Non Patent Literature	NPL35_3_OF_5_OA_Appl_15934416_01_1_2021_G.pdf	717993	no	17
			4e2d25b2a6b9fd247caac69eba5bba16c959214		
Warnings:					
Information:					
27	Non Patent Literature	NPL36_3_OF_5_OA_Appl_15934416_3_21_2019_G.pdf	285453	no	8
			672fd95e97bbe2d460ac977d82feb41d422cc9b		
Warnings:					
Information:					
28	Non Patent Literature	NPL37_3_OF_5_OA_Appl_15934416_10_15_2019_G.pdf	530932	no	13
			51b901ebae274156ab09a4237a46d90c04e8ff97		
Warnings:					
Information:					
29	Non Patent Literature	NPL38_3_OF_5_OA_Appl_17138766_3_2_2021_H.pdf	285267	no	7
			528f1b024af4f1e0b968f17737480fc5be88571d		
Warnings:					
Information:					

30	Non Patent Literature	NPL44_3_OF_5_Order_Grants_Joint_Stipulation_of_Dismissal_NDCA_413cv05889_382.pdf	148422	no	2
			422360fc5dbf01591feed500869b237c3f3eb469		
Warnings:					
Information:					
31	Non Patent Literature	NPL45_3_OF_5_Out_of_Stealth_Mode_Start_Up_MetaRAM.pdf	1334942	no	8
			5c7d9d8fe4818842dda24d11196890b0eeacefae		
Warnings:					
Information:					
32	Non Patent Literature	NPL7_4_OF_5_Patterson_Computer_Organization_Design.pdf	8238976	no	71
			d044b81ddd753851a154eb8f952d0b300749a9e2		
Warnings:					
Information:					
33	Non Patent Literature	NPL39_4_OF_5_SUPPLEMENTAL_DECLARATION_OF_DANIEL_E_ALBERTI.pdf	109313	no	3
			77f4287eeb2bbd7947e187654dd6793d0700efad		
Warnings:					
Information:					
34	Non Patent Literature	NPL41_4_OF_5_SUPPLEMENTAL_DECLARATION_OF_STEVEN_J_CORRINSUPPORTOFSANDISK_case413cv058889.pdf	158968	no	3
			42bd7fe1a87c3c30babf4f8291a78d46eace669b		
Warnings:					
Information:					
35	Non Patent Literature	NPL42_4_OF_5_Switches_DT_Online_PTAB_IPR2017_00587_Ex2022.pdf	281887	no	3
			8044caa534879385fab9e6464d26e0aaaa0df6a		
Warnings:					
Information:					
36	Non Patent Literature	NPL48_4_OF_5_Using_Two_Chip_Selects_to_Enable_Quad_Rank.pdf	888238	no	2
			1b9858d81175a80c455ee67862df1d1017caff88		
Warnings:					
Information:					

37	Non Patent Literature	NPL50_4_OF_5_Websters_II_N ew_College_Dictionary.pdf	1024387	no	5
			cb1c81e2f7d6c1541b69d0ae98fd9427cb6 b2f21		
Warnings:					
Information:					
38	Non Patent Literature	NPL1_5_OF_5_Wong_The_BIO S_Optimization_Guide.pdf	787615	no	67
			cd04636e98d8e56918b7797cffbc3846f7e1 3436		
Warnings:					
Information:					
39	Non Patent Literature	NPL26_1_OF_5_Data_Sheet_7 4F257A_Quad_2_line.pdf	619266	no	10
			772ef88ead2870395603d3ae9e29fca8b30f 13e9		
Warnings:					
Information:					
40	Non Patent Literature	NPL50_1_OF_5_Exhibit_1_Clai m_Chart_Comparing_Netlists_ USPatent8001434.pdf	1401054	no	21
			bb30e92bbe043471a3c3b7a3da6850d524 e4c154		
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41	Non Patent Literature	NPL1_2_OF_5_Exhibit_Applica tion_As_Filed_PTAB_IPR2014_ 00994_1002.pdf	2777777	no	52
			19e4392842cc718b71b14bdc781e13628d 412597		
Warnings:					
Information:					
42	Non Patent Literature	NPL33_3_OF_5_Intel_18Volt_I ntel_StrataFlash.pdf	2219680	no	100
			7dae7d8451dd339fcab19182c5aff50352c6 f974		
Warnings:					
Information:					
43	Non Patent Literature	NPL32_2_OF_5_Innis_MPC856 0_PowerQUICC.pdf	505730	no	25
			f3b5a1e20dd4b4057b7e2a680ad1708ddd 72a9ee		
Warnings:					
Information:					

44	Non Patent Literature	NPL31_2_OF_5_Horowitz_The_Art_of_Electronics.pdf	691449	no	4
			9f78ad8989060f44b8d5e02cf2fa9e2fbc34362		
Warnings:					
Information:					
45	Information Disclosure Statement (IDS) Form (SB08)	IDS_20210616_0016001000I_1_OF_5.pdf	1061397	no	24
			67a733d6c7ac529a199dbbf7928e8ab13f07da5f		
Warnings:					
Information:					
46	Information Disclosure Statement (IDS) Form (SB08)	IDS_20210616_0016001000I_2_OF_5.pdf	1055801	no	8
			bd07e5548e5c87270596960461c6fc15c5460ae6		
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47	Information Disclosure Statement (IDS) Form (SB08)	IDS_20210616_0016001000I_3_OF_5.pdf	1055262	no	8
			bede53bf1c6dc9cbf2b71378cd342580066c3863		
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48	Information Disclosure Statement (IDS) Form (SB08)	IDS_20210616_0016001000I_4_OF_5.pdf	1055559	no	8
			02dd4e7652f10548a659ad7f6154c4053e2b8ebf		
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49	Information Disclosure Statement (IDS) Form (SB08)	IDS_20210616_0016001000I_5 _OF_5.pdf	1053095 4a1d301c647eda4454b731968036dc6e6aa dc0ba	no	4
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A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
50	Notice of concurrent proceedings / decisions	001600100I_Notice_of_Related _Litigation_and_AppendixA. pdf	214700 72ef1ad15c4c855443de4edcefd2c98fae88 db7a	no	4
Warnings:					
Information:					
Total Files Size (in bytes):			87492074		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	0016.001000I	6552
151145	7590	07/21/2021	EXAMINER	
Shami Messinger PLLC			CENTRAL, DOCKET	
1000 Wisconsin Ave. NW			ART UNIT	
Suite 200			PAPER NUMBER	
Washington, DC 20007			OPAP	
			NOTIFICATION DATE	DELIVERY MODE
			07/21/2021	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

khaled@shamimessinger.com
mike@shamimessinger.com
stephanie@shamimessinger.com

<i>Decision Granting Request for Prioritized Examination (Track I)</i>	Application No. 17/328,019	Applicant(s) Chen et al.	
	Examiner TERRI S JOHNSON	Art Unit OPET	AIA (FITF) Status No
<p>1. THE REQUEST FILED <u>24 May 2021</u> IS GRANTED .</p> <p>The above-identified application has met the requirements for prioritized examination</p> <p>A. ☒ for an original nonprovisional application (Track I).</p> <p>B. ☐ for an application undergoing continued examination (RCE).</p> <p>2. The above-identified application will undergo prioritized examination. The application will be accorded special status throughout its entire course of prosecution until one of the following occurs:</p> <p>A. filing a <u>petition for extension of time</u> to extend the time period for filing a reply;</p> <p>B. filing an <u>amendment to amend the application to contain more than four independent claims, more than thirty total claims</u>, or a multiple dependent claim;</p> <p>C. filing a <u>request for continued examination</u> ;</p> <p>D. filing a notice of appeal;</p> <p>E. filing a request for suspension of action;</p> <p>F. mailing of a notice of allowance;</p> <p>G. mailing of a final Office action;</p> <p>H. completion of examination as defined in 37 CFR 41.102; or</p> <p>I. abandonment of the application.</p> <p>Telephone inquiries with regard to this decision should be directed to TERRI JOHNSON at (571)272-2991. In his/her absence, calls may be directed to Petition Help Desk at (571) 272-3282.</p>			
/TERRI S JOHNSON/ Paralegal Specialist, OPET			



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APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
17/328,019	05/24/2021	Chi-She Chen	0016.001000I

CONFIRMATION NO. 6552

PUBLICATION NOTICE



OC000000128292336

151145
Shami Messinger PLLC
1000 Wisconsin Ave. NW
Suite 200
Washington, DC 20007

Title:FLASH-DRAM HYBRID MEMORY MODULE

Publication No.US-2021-0279194-A1

Publication Date:09/09/2021

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Public Records Division. The Public Records Division can be reached by telephone at (571) 272-3150 or (800) 972-6382, by facsimile at (571) 273-3250, by mail addressed to the United States Patent and Trademark Office, Public Records Division, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <https://portal.uspto.gov/pair/PublicPair>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	0016.001000I	6552
151145	7590	09/27/2021	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW			ART UNIT	
9th Floor			PAPER NUMBER	
Washington, DC 20006-1152			2135	
			NOTIFICATION DATE	DELIVERY MODE
			09/27/2021	ELECTRONIC

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Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

kshami@vorys.com
mvmessinger@vorys.com
vorys_docketing@cardinal-ip.com

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

The instant application having application No. 17/328,019 has a total of 30 claims pending in the application; there are 3 independent claim and 27 dependent claims, all of which are ready for examination by the examiner.

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

Information Disclosure Statement

*As required by **M.P.E.P. 2001.06(b)** and **37 C.F.R. 1.98(d)**, since the instant application has been identified as a continuation application of an earlier filed application and is relied upon for an earlier filing date under **35 U.S.C. 120**, the examiner has reviewed the prior art cited in the earlier related application as required by **M.P.E.P. 707.05** and **904** and as stated in **M.P.E.P. 2001.06(b)**, no separate citation of the same prior art need be made by the applicants in the instant application.*

INFORMATION CONCERNING IDS:

The information disclosure statements (IDS') submitted on 06/22/2021 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements have been considered by the Examiner. However, the documents marked by lined-through have not been considered by because either copy of the documents

were not provided or the documents weren't readily identifiable from the IDS description of the corresponding documents.

INFORMATION CONCERNING CLAIMS:

Claim Interpretation

Claim limitations in this application do not use the word "means" (or "step"), thus, they are not being interpreted under 35 U.S.C. 112(f) or pre-AIA 35 U.S.C. 112, sixth paragraph.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112(a):

(a) IN GENERAL.—The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor or joint inventor of carrying out the invention.

The following is a quotation of the first paragraph of pre-AIA 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. *Claims 20, 22, and 30-31 are rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-AIA), first paragraph, as failing to comply with the written description requirement.*

The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor or

a joint inventor, or for applications subject to pre-AIA 35 U.S.C. 112, the inventor(s), at the time the application was filed, had possession of the claimed invention.

2. *Claim 20 recites the limitation(s):*

“wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and **wherein the circuit includes a second diode having a second input and a second output,** the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.” *(Emphasis added).*

3. *Claim 22 recites the limitation(s):*

“wherein the first circuit includes **a first diode** coupled between the first input and the output and **a second diode** coupled between the second input and the output.”

4. *Claim 30 recites the limitation(s):*

“wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via **a first diode.**” *(Emphasis added).*

5. *Claim 31 recites the limitation(s):*

“wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via **a second diode.**” *(Emphasis added).*

The claimed specification does not appear to describe or support the above limitations as claimed.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at

least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP § 2146 et seq. for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For

more information about eTerminal Disclaimers, refer to

www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

6. Claims 2-15, 23, and 26 -29 are rejected on the ground of nonstatutory double patenting as being unpatentable over claims 1-30 of U.S. Patent No. 11,016,918 B2.

Although the claims at issue are not identical, they are not patentably distinct from each other because although, the language and order of limitations in claims are slightly different (e.g., see table below), they are not patentably distinct from each other.

7. Claim 2 of instant application (Application No. 17/328,019) is compared to claim 1 of Patent No. 11,016,918 B2 in the following table:

Patent No. 11,016,918 B2	Application No. 17/328,019
Claim 1: A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;	Claim 2: A memory module comprising: a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;

<p>a first buck converter configured to provide a first regulated voltage having a first voltage amplitude; a second buck converter configured to provide a second regulated voltage having a second voltage amplitude; a third buck converter configured to provide a third regulated voltage having a third voltage amplitude; a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and</p> <p>a plurality of components coupled to the PCB, each component of the plurality of components coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages,</p> <p>the plurality of components comprising: a plurality of synchronous dynamic random access memory (SDRAM)</p>	<p>a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages;</p> <p>a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages,</p> <p>the plurality of components including</p>
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<p>devices coupled to the first regulated voltage,</p> <p>and at least one circuit coupled between a first portion of the plurality of edge connections and the plurality of SDRAM devices, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii) output a second plurality of address and control signals to the plurality of SDRAM devices, the at least one circuit coupled to both the second regulated voltage and the fourth regulated voltage, wherein a first one of the second and fourth voltage amplitudes is less than a second one of the second and fourth voltage amplitudes.</p>	<p>a plurality of synchronous dynamic random access memory (SDRAM) devices</p> <p>and a first circuit that is coupled to the plurality of synchronous dynamic random access memory (SDRAM) devices and to a first set of edge connections of the plurality of edge connections,</p> <p>wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.</p>
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Allowable Subject Matter

Claims 16-19 and 21 are allowed.

Claims 24-25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

8. *The prior art of record does not disclose or suggest the distinct features “the voltage monitor circuit configured to detect a change in the input voltage, wherein, in response to the voltage monitor detecting a change in the input voltage, the memory module transitions from a first operable state to a second operable state”, as recited in the independent claim 16. Claims 17-19 and 21 are dependent from the independent claim 16.*

9. *The prior art of record does not disclose or suggest the distinct features “wherein, in response to the voltage monitor circuit detecting a change in the input voltage, the memory module transitions from a first state of operation to a second state of operation”, as recited in the independent claim 24. Claim 25 is dependent from claim 24.*

Conclusion

The prior art made of record and not relied upon are as follows:

1. *Chen et al. (US 20120271990 A1).*
2. *Bates (US 20070136523 A1).*
3. *Prete et al. (US 20080126624 A1).*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached Monday through Friday from 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/HASHEM FARROKH/
Primary Examiner, Art Unit 2135*

September 22, 2021

Notice of References Cited	Application/Control No. 17/328,019		Applicant(s)/Patent Under Reexamination Chen et al.	
	Examiner HASHEM FARROKH		Art Unit 2135	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-20120271990-A1	10-2012	Chen; Chi-She	G06F12/00	711/103
*	B	US-20070136523-A1	06-2007	Bonella; Randy M.	G06F9/4401	711/113
*	C	US-20080126624-A1	05-2008	Prete; Edoardo	G11C7/106	710/53
	D					
	E					
	F					
	G					
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	I					
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

<i>Index of Claims</i> 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	09/22/2021								
	1	-								
	2	✓								
	3	✓								
	4	✓								
	5	✓								
	6	✓								
	7	✓								
	8	✓								
	9	✓								
	10	✓								
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	21	=								
	22	✓								
	23	✓								
	24	O								
	25	O								
	26	✓								
	27	✓								
	28	✓								
	29	✓								
	30	✓								
	31	✓								

Search Notes 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

CPC - Searched*		
Symbol	Date	Examiner
G11C7/1072; G11C14/0018; G06F12/0246; G06F13/4243; G06F13/1694; G06F3/0659; G06F13/4027; G06F12/0638; G06F13/28; G06F1/185; G06F2212/205; G06F2212/7208; G06F3/0685; Y02D10/00	09/22/2021	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	09/22/2021	HF

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Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	09/22/2021	HF
EAST Text Search	09/22/2021	HF
IP Search	09/22/2021	HF
Google Search	09/22/2021	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17328019
	Filing Date	2021-05-24
	First Named Inventor	Chi-She Chen
	Art Unit	2135
	Examiner Name	Hashem Farrokh
	Attorney Docket Number	0016.0010001

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
Art Unit		
Examiner Name		
Attorney Docket Number	0016.0010001	

1	Joint Status Report Regarding Inter Partes Review, <i>Nollist v. Smart Storage Systems, Inc. et al.</i>, Case No. 4:13-CV-05889-YGR (NDCA), filed August 17, 2018, 4 pages.
2	Material Science & Engineering, Department of Material Science and Engineering, Stanford University, Exhibit 2011, Case No. IPR2017-00692, 2 pages.
3	Merriam-Webster's Collegiate Dictionary, Eleventh Ed., Merriam-Webster Corporation, Springfield, MA, 2003, 7 pages.
4	MetaRAM Develops New Technology That Quadruples Memory Capacity of Servers and Workstations; Reduces Price by Up to 90 Percent, Press Release provided by MetaRAM and published on MarketWired.com, Feb. 25, 2008, 3 pages.
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9	Mutnuary, B. et al., "Analysis of Fully Buffered DIMM Interface in High-speed Server Applications", IBM Corp, xSeries eServer Development, 2006 Electronic Components and Technology Conferencepp. 203-208.
10	Notice of Allowance in U.S. Appl. No. 12/240,916 dated Sep. 17, 2012, pp. 1-7.
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First Named Inventor	Chi-She Chen
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Attorney Docket Number	0016.001000I

12	Notice of Allowance in U.S. Appl. No. 13/536,173, dated Jul. 2, 2013.
13	Notice of Allowance in U.S. Appl. No. 13/559,476, dated May 6, 2014.
14	Notice of Allowance in U.S. Appl. No. 13/559,476, dated Sep. 29, 2014.
15	Notice of Allowance in U.S. Appl. No. 13/905,048, dated Dec. 19, 2013, 8 pages.
16	Notice of Allowance in U.S. Appl. No. 13/905,053, dated Dec. 11, 2013.
17	Notice of Allowance in U.S. Appl. No. 14/173,219 dated Jul. 7, 2014.
18	Notice of Allowance in U.S. Appl. No. 14/489,269, dated Oct. 8, 2015.
19	Notice of Allowance in U.S. Appl. No. 17/138,766, dated Mar. 24, 2021, 10 pages.
20	Notice of Allowance, SanDisk Corporation v. Netlist, Application No. 13/536,173, IPR2014-00982 (PTAB), dated July 2, 2013, 8 pages.
21	Office Action dated Aug. 19, 2016 of the Chinese Patent Application No. 201280047758.X, 9 pages.
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23	Office Action in U.S. Appl. No. 12/240,916, mailed Feb. 1, 2012.
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27	Office Action in U.S. Appl. No. 13/625,563, dated Aug. 5, 2013.
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29	Office Action in U.S. Appl. No. 13/905,048, dated Aug. 1, 2013.
30	Office Action in U.S. Appl. No. 13/905,053, dated Aug. 1, 2013.
31	Office Action in U.S. Appl. No. 14/173,219, dated Mar. 13, 2014.
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34	Office Action in U.S. Appl. No. 15/934,416, dated on Apr. 2, 2020, 21 pages.
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39	Office Action in U.S. Application No. 12/240,916, dated Feb. 1, 2012, 14 pages.
40	Office Action in U.S. Application No. 14/173,242, dated March 14, 2014, 7 pages.
41	Office Action, Application 12/240,916, IPR2014-0099-1005 (PTAB), dated July 29, 2011, 8 pages.
42	Office Action, Application 12/240,916, IPR2014-0099-1010 (PTAB), dated April 3, 2012, 11 pages.
43	Office Action, Application No. 13/536,173, IPR2014-00982 (PTAB), dated April 15, 2013, 9 pages.
44	Order Granting Joint Stipulation of Dismissal, Nollist v. Smart Storage Systems, Inc. et al., Case No. 4:13-cv-05889-YGR (NDCA), filed May 15, 2020, 2 pages.

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Examiner Name	
Attorney Docket Number	0016.0010001

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46	Patent Owner's Demonstratives, Patent Number: 8,671,243, Case No. IPR 2017-00587-2023, (PTAB), 57 pages.
47	Patent Owner's Listing of New Arguments and Evidence in Petitioners' Reply, Patent No. 8,671,243, Case No. IPR2017-00587 (PTAB), filed Jan. 29, 2018, 6 pages.
48	Patent Owner's Opposition to Petitioners' Motion to Exclude, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed April 2, 2018, 2017, 11 pages.
49	Patent Owner's Preliminary Response, Patent Number: 8,516,187, Case IPR2014-01371 (PTAB), filed Dec. 16, 2014, 66 pages.
50	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), Paper 8, dated October 2, 2014, 60 pages.

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EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	09/21/2021
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S413	4	"11016918".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/16 11:29
S414	1	"17328019"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/16 11:41
S415	3	"17138766"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/16 15:36
S416	380	((printed adj circuit adj board) or PCB) with (plurality near2 edge near2 connections)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 10:01
S417	10,693	((synchronous adj dynamic adj random adj access adj memory) or SDRAM) near2 (devices or chips or dies)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 10:05
S418	7,653	(regulated near2 voltages)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 10:06

S419	6	S417 same S418	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 10:06
S420	16	"8301833".pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 10:08
S421	31	"12131873"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 10:12
S422	3	S419 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 10:24
S423	3	S416 same S417	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 10:47
S424	33	S416 and S417	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/09/20 11:03
S425	4	S424 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:03

S426	4	S425 and voltage	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:06
S427	0	S425 and (regulat\$3 near2 voltage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:08
S428	3	((printed adj circuit adj board) or PCB) with (plurality near2 edge near2 connections) same SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:09
S429	7,625	(board same SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:10
S430	43	S418 and S429	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:10
S431	19	S430 and connector	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:10
S432	19	S431 and (regulat\$3 near2 voltage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:11

S433	2	S432 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/20 11:11
S434	220	("2043099" "3562555" "3916390" "4234920" "4607332" "4658204" "4884242" "4965828" "4420821" "4449205" "4882709" "5430742" "5444664" "5630096" "5757712" "58749955490155" "5519663" "5519831" "55638395917213" "5619644" "5675725" "5799200" "5813029" "5870350" "5890192" "5953215" "5991885" "6721860" "6026465" "6065092" "6216247" "6421279" "6614685" "6721212" "6799241" "6816982" "69106356948029" "6023421" "6112310" "6145068" "6158015" "6199142" "6269382" "6336174" "6336176" "6363450" "6459647" "6487102" "6487623").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 12:28
S435	281	("6571244" "6658507" "6691209" "6693840" "6769081" "6799244" "6810513" "6839774" "6944042" "6952368" "7062618" "7107480" "7136978" "7421552" "7467251" "7600142" "7881150" "7952179" "7053470" "7089412" "7102391" "7111142" "7155627" "7200021" "7234099" "7353325" "7409491" "7409590" "7411859" "7519754" "7613877" "7716411" "7818488" "7873750" "8001434" "8081536" "8301833" "8874831" "8086955" "8102614" "8214616" "8233303" "8407395" "8412879" "8516187" "8671243" "8677060" "8880791" "8904098" "8904099" "9043677" "9158684" "9361250" "9436600" "9921762" "20020053944" "20020083368" "20020199061" "20030028733" "20030076726" "20030158995" "20030204776" "20030210601").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:14
S436	101	("20030147297" "20030206478" "20030137881" "20040163027" "20040088508" "20040190210"	US-PGPUB; USPAT; USOCR;	OR	ON	2021/09/21 14:34

		"20050044302" "20050060488" "20050132250" "20050141273" "20050144418" "20050185472" "20050204091" "20050249011" "20050273548" "20060080515" "20060126369" "20060294295" "20060039197" "20060069896" "20060212651" "20070276995" "20070070669" "20070136523" "20070147115" "20070192627" "20070255898" "20070288683" "20080126690" "20080104344" "20080126624" "20080147968" "20080189479" "20080195806" "20080235443" "20080291727" "20090235038" "20090031099" "20100122200" "20100110748" "20100274953" "20100322020" "20110078496" "20110161569").pn.	FPRS; EPO; JPO; DERWENT; IBM_TDB			
S437	34	("20110320804" "20120110417" "20120271990" "20120117402" "20120204079" "20120265952" "20120317433" "20130019076" "20130086309" "20130254456" "20140059170" "20140156919" "20140156920" "20150058701").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:39
S438	72	((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:42
S439	220	("2043099" "3562555" "3916390" "4234920" "4607332" "4658204" "4884242" "4965828" "4420821" "4449205" "4882709" "5430742" "5444664" "5630096" "5757712" "58749955490155" "5519663" "5519831" "55638395917213" "5619644" "5675725" "5799200" "5813029" "5870350" "5890192" "5953215" "5991885" "6721860" "6026465" "6065092" "6216247" "6421279" "6614685" "6721212" "6799241" "6816982" "69106356948029" "6023421" "6112310" "6145068" "6158015" "6199142" "6269382" "6336174" "6336176" "6363450" "6459647" "6487102" "6487623").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:43

S440	13	S438 and (S439 or S435 or S436 or S437)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:43
S441	0	S440 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/21 14:47
S442	1,356	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S443	79	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S444	75	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S445	36	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S446	39	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16

S447	37	((transfer\$3 or cop\$4 or transmi\$5 or retriev\$3 or read\$3) near5 ?DRAM near5 (flash or non\$1volatile)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S448	0	S447 and (S442 or S443 or S444 or S445 or S446)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:16
S449	12,048	(transfer\$4 or cop\$4 or transmi\$5 or mov\$3) with data with (non\$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:18
S450	226	NETLIST.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:18
S451	21	S449 and S450	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:18
S452	4	((((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:21
S453	72	((((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:22

S454	3	S452 and (S442 or S443 or S444 or S445 or S446)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:23
S455	59	S450 and S453	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:23
S456	3	S455 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:24
S457	15	S455 and (regulat\$3 near2 voltage)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:25
S458	0	S457 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:26
S459	48	S453 AND ((G11C7/1072 OR G11C14/0018 OR G06F12/0246 OR G06F13/4243 OR G06F13/1694 OR G06F3/0659 OR G06F13/4027 OR G06F12/0638 OR G06F13/28 OR G06F1/185 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0685 OR Y02D10/00).CPC. OR (711/110).CCLS. OR (G06F13/16 OR G06F3/06 OR G06F12/02 OR G06F13/42 OR G06F12/06 OR G06F13/40 OR G06F13/28 OR G06F1/18 OR G11C7/10 OR G11C14/00).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 10:47
S460	2	S459 and (@ad<"20070601")	US-PGPUB; USPAT;	OR	ON	2021/09/22 10:47

			USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			
S461	1	(respons\$3 or based or according or "when") with (voltage adj monitor) with (detect\$3 or sens\$3 or recogniz\$3) with (chang\$3 or transit\$3) with (input adj voltage) with (memory adj module) with (transition\$3 or chang\$3) with (first adj (state or status or condition) adj operation) with (second adj (state or status or condition) adj operation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 12:02
S462	1	(respons\$3 or based or according or "when") same (voltage adj monitor) same (detect\$3 or sens\$3 or recogniz\$3) same (chang\$3 or transit\$3) same (input adj voltage) same (memory adj module) same (transition\$3 or chang\$3) same (first adj (state or status or condition) adj operation) same (second adj (state or status or condition) adj operation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 12:04
S463	1	(respons\$3 or based or according or "when") same (voltage adj monitor) same (detect\$3 or sens\$3 or recogniz\$3) same (chang\$3 or transit\$3) same (input adj voltage) same (memory or storage) same (transition\$3 or chang\$3) same (first adj (state or status or condition) adj operation) same (second adj (state or status or condition) adj operation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 12:06
S464	1	(respons\$3 or based or according or "when") same (voltage adj monitor) same (detect\$3 or sens\$3 or recogniz\$3) same (chang\$3 or transit\$3) same (input adj voltage) same (memory or storage) same ((transition\$3 or chang\$3) near5 ((state or status or condition) adj operation))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/09/22 12:08

9/22/2021 12:32:08 PM

C:\Users\hfarrokh\Documents\EAST\Workspaces\15934416.wsp

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17328019
	Filing Date		2021-05-24
	First Named Inventor		Chi-She Chen
	Art Unit		2135
	Examiner Name	Hashem Farrokh	
	Attorney Docket Number		0016.0010001

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
Art Unit		
Examiner Name		
Attorney Docket Number	0016.0010001	

1	Wong, A., The BIOS Optimization Guide, Adrian's Rojak Pot, Rev. 6.2, 1998-2001, 67 pages.
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Examiner Signature	/HASHEM FARROKH/	Date Considered	09/21/2021
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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CHANG NAI-SHUNG (1)

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MICRON TECH INC (25)

MWI VETERINARY SUPPLY ... (1)

INTEL CORP (196)

More Visuals

1. Mother board and computer system capable of flexibly using synchronous dynamic random access memory and double data rate dynamic random access memory

A mother board and a computer system capable of flexibly using the SDRAM and the DDRAM. The mother board has several memory module slots, a voltage comparator, a clock generator and a chip set. Each of the memory module slots comprises a reference voltage pin, and the reference voltage pins of the...

CURRENT ASSIGNEES: VIA TECH INC
US6813157 | US PATENTS | 02-NOV-2004

2. Mother board and computer system capable of flexibly using synchronous dynamic random access memory and double data rate dynamic random access memory

A mother board and a computer system capable of flexibly using the SDRAM and the DDRAM. The mother board has several memory module slots, a voltage comparator, a clock generator and a chip set. Each of the memory module slots comprises a reference voltage pin, and the reference voltage pins of the...

CURRENT ASSIGNEES: CHANG NAI-SHUNG
US20020196650 | US APPLICATIONS | 26-DEC-2002

3. Mother board and computer system capable of flexibly using synchronous dynamic random access memory and double data rate dynamic random access memory

A mother board and a computer system capable of flexibly using the SDRAM and the DDRAM. The mother board has several memory module slots, a voltage comparator, a clock generator and a chip set. Each of the memory module slots comprises a reference voltage pin, and the reference voltage pins of the...

CURRENT ASSIGNEES: VIA TECH INC
US6424555 | US PATENTS | 23-JUL-2002

4. Mainboard and computer system using elastic memory and double rate memory

The present invention relates to mainboard and computer system with elastic synchronous DRAM and double data rate DRAM. By means of setting voltage regulator and several terminal resistors in terminal circuit module, the present invention has decreased printed circuit board area and production cost...

CURRENT ASSIGNEES: VIA TECH INC
CN1365036A | CHINA APPLICATIONS | 21-AUG-2002

5. Terminating circuit module used in a computer system

Result #1

PREV

NEXT

Doc code: IDS

PTO/SB/08a (02-18)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 11/30/2020. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	2135
Examiner Name	Hashem Farrokh
Attorney Docket Number	0016.0010001

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	2	3562555	A	1971-02-09	Ahrons	Entire Document
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32	Decision Denying Institution of Inter Partes Review, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, IPR2014-01370 (PTAB), Paper 13, entered March 13, 2015, 19 pages.
33	Decision Instituting Inter Partes Review, Patent 8,671,243, Case No. IPR2017-00587-7(PTAB), Paper No. 7, entered June 22, 2017, 40 pages.
34	Decision Instituting Inter Partes Review, Patent 8,874,831, Case No. IPR2017-00692-7(PTAB), Paper No. 7, entered July 21, 2017, 29 pages.
35	Declaration of R. Jacob Baker, Patent No. 8,874,831, Case IPR2017-00692-2016 (PTAB), filed Nov. 10, 2017, 72 pages.
36	Declaration of R. Jacob Baker, Patent Number: 8,671,243, Case IPR2017-00587-2016 (PTAB), filed October 13, 2019, 109 pages.
37	Declaration of Dr. Nader Bagherzadeh, Patent No. 8,516,187, IPR2014-01371 (PTAB), filed September 22, 2014, 306 pages.
38	Declaration of Jeff McMullen, Netlist, Inc. v. Diablo Technologies, Inc., Case No. 4: I 3-CV-05889-YGR (NDCA), Document 362-1, filed September 5, 2018, 3 pages.
39	Declaration of Paul Min, In Inter Partes Review of U.S. Patent No. 8,301,833, IPR2014-00994-1020 (PTAB), filed September 29, 2008, 215 pages.
40	Declaration of Paul Min, In Inter Partes Review of U.S. Patent No. 8,516,187, IPR2014-00982-1013 (PTAB), filed June 28, 2012, pages 240.
41	Declaration of Ron Maltiel, Patent No. 8,671,243, No. IPR2017-00587-1003 (PTAB), filed May 29, 2013, 131 pages.
42	Declaration of Ron Maltiel, Patent No. 8,874,831, No. IPR2017-00692-1003 (PTAB), filed July 26, 2012 29, 172 pages.

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Application Number		17328019
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First Named Inventor	Chi-She Chen	
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43	Declaration of Steven J. Corr, Netlist, Inc. v. SMART Storage Systems, Inc., et al., Case 4:13-cv-05889-YGR (NDCA), Document 305-8, filed March 10, 2015, 3 pages.
44	Deposition of Baker, Exhibit 1030, p.78, Patent No. 8, 671,243, SK hynix Inc., et al. v. Netlist, Inc., Case No. IPR-2017-00587 (PTAB), filed December 18, 2017, 268 pages.
45	Deposition of Ron Maltiel, Patent No. 8874831, Case No. IPR2017-00692-2010 (PTAB), dated Sep. 27, 2017, 155 pages.
46	Netlist v Smart Storage System and Diablo Technologies, Inc.'s Invalidity Contentions, Case No. 13-CV-05889 YGR, dated Jun. 6, 2014, 109 pages.
47	Drawing by R. Jacob Bake regarding Address of Dram and Flash, Patent Number: 8,671,243, Case IPR2017-00587-1023 (PTAB), filed December 18, 2017, 1 page.
48	Elmhurst, D. et al., A 1.8-V 128-Mb 125-MHz Multilevel Cell Flash Memory With Flexible Read While Write, IEEE Journal of Solid-State Circuits, Vol. 38, No. 11, Nov. 2003, 5 pages.
49	Ex. 1004—IPR2017-00587 Ron Maltiel CV, 7 pages.
50	Exhibit 1: Claim Chart Comparing Netlist's US Patent No. 8,001,434 to Smart Storage Ulltradimm, Case4:13-cv-05889-YGR Document 193-1, filed Apr. 10, 2014, 21 pages.

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A memory module includes a circuit board having socket mating contacts at a socket interface and VRM contacts at a VRM interface. Memory devices are coupled ...

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US8151009B2 - Serial connection external interface from printed ...

A translator of an apparatus in an example through a serial connection external interface of a printed circuit board (PCB) communicates between a serial ...

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US20050093120A1 - Detachable on package voltage regulation ...

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Printed circuit board - Wikipedia

A printed circuit board (PCB) is a laminated sandwich structure of conductive and insulating layers. PCBs have two complementary functions.

Missing: plurality | Must include: plurality

<https://www.nxp.com/docs/application-note/AN2826.pdf>

AN2826: DDR-SDRAM Layout Considerations for MCF547x ...

This application note discusses the critical parts of a DDR SDRAM memory sub-system design, particularly those related to printed circuit board (PCB) layout. 1.

20 pages

<https://www.gerberlabs.com/what-is-a-printed-circuit-board/>

What is a Printed Circuit Board (PCB) | Gerber Labs

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Missing: SDRAM regulators

<https://www.electromaker.io/blog/article/what-is-a-pcb/>

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<https://www.xilinx.com/support/documentation/UG583.pdf>

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	First Named Inventor	Chi-She Chen	
	Art Unit	2135	
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Attorney Docket Number	0016.0010001	

1	Exhibit, Application As Filed, Sandisk Corporation v. Netlist, Inc., Patent 8,304,833, IPR2014-00004 (PTAB), 52 pages.
2	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-3, filed March 17, 2015, 23 pages.
3	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-4, filed March 17, 2015, 20 pages.
4	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-5, filed March 17, 2015, 28 pages.
5	Exhibit, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-9, filed March 17, 2015, 17 pages.
6	Exhibit 12, Decision Denying Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-7, filed March 17, 2015, 17 pages.
7	Exhibit 9, Email from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-17, filed March 10, 2015, 6 pages.
8	Exhibit, Institution of Inter Partes Review, Sandisk Corporation v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 316-9, filed March 24, 2015, 29 pages.
9	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.
10	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-1, filed March 17, 2015, 22 pages.
11	Exhibit, Institution of Inter Partes Review, Smart Modular Technologies, Inc. v. Netlist, Inc., Case No. 4:13-cv-05889-YGR Document 309-2, filed March 17, 2015, 23 pages.

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12	Exhibit, Letter from Defendant's Counsel, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-16, filed March 10, 2015, 3 pages.
13	Exhibit, Letter sent via email on December 6, 2013, Case 4:13-cv-03901-YGR Document 53-2, filed January 6, 2014
14	Exhibit, Order Denying Defendant's Motion to Stay Pending Inter Partes Review (Doc.59), The Procter and Gamble Company v. Team Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 316-6, filed March 24, 2015, 10 pages.
15	Exhibit, Patent Public Advisory Committee Quarterly Meeting, Appeals Statistics USPTO, Case No. 4:13-cv-05889-YGR Document 309-8, filed March 17, 2015, 23 pages.
16	Exhibit, Reporter's Transcript of Proceedings, Netlist, Inc v. Smart Modular Technologies, Inc., et al., Case 4:13-cv-05889-YGR Document 316-3, filed March 24, 2015, 15 pages.
17	Exhibit, Transcript of Official Electronic Sound Recording Proceeding, Netlist v. Smart Modular Technologies, Inc, et al., Case 4:13-cv-05889-YGR Document 305-7, filed March 10, 2015, 10 pages.
18	Extended European Search Report for European Application No. 12 817 751.6, dated Jun. 9, 2015.
19	File History for U.S. Appl. No. 12/240,046, filed Sep. 20, 2008, 320 pages.
20	File History for U.S. Appl. No. 13/005,048, filed May 20, 2013, 181 pages.
21	File History for U.S. Appl. No. 60/941,586, filed Jun. 1, 2007, 23 pages.
22	File History U.S. Pat. No. 8,674,243.

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23	Final Office Action, dated Jun. 15, 2016, dated in U.S. Appl. No. 14/489,281, 16 pages.
24	Final Office Action, dated Jun. 15, 2016, issued in U.S. Appl. No. 14/489,281, 16 pages.
25	Final Office Action, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-0699-1007 (PTAB), dated February 1, 2012, 13 pages
26	Final Written Decision, Patent 8,674,243, IPR2017-00587-34, Paper No. 34, entered June 26, 2018, 53 pages.
27	Final Written Decision, Patent 8,874,831, IPR2017-00692, Paper No. 25, entered July 5, 2018, 42 pages.
28	Final Written Decision, US Patent No. 7,881,150, Case No. Case IPR2014-06882, (PTAB), Paper 33, filed December 14, 2015, 51 pages.
29	First Amended Complaint for Patent Infringement, Netlist Inc. v Smart Modular Tech, Inc., et al., Case 8:13-cv-00996-DOC-JPR, Document 5, filed Aug. 23, 2013, 99 pages.
30	Hasan, J. et al. Efficient Use of Memory Bandwidth to Improve Network Processor Throughput, Proceedings of the 30th Annual International Symposium on Computer Architecture (ISCA'03), IEEE, 2003, 12 pages.
31	Horowitz, P. et al., "The Art of Electronics", Cambridge University Press 2nd Ed. 1989, pp. 471, 495-496.
32	Innis, J., "MPC8560 PowerQUICC III Compact Flash Interface Design", Freescale Semiconductor, Inc., 2004-2006, pp. 1-23.
33	Intel 1.8 Volt Intel StrataFlash Wireless Memory (L18), 2003, 100 pages.

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34	Inter Partes Review No. IPR2017-00692 (PTAB), Patent No. 8,874,831, filed July 26, 2012, 78 pages.
35	Inter Partes Review of U.S. Patent No. 8,874,831, Case IPR2017-00692 (PTAB), filed July 26, 2012, Paper No. 1, 78 pages.
36	International Preliminary Report on Patentability in PCT/US12/48750, mailed Apr. 3, 2014.
37	International Preliminary Report on Patentability in PCT/US12/48750, mailed Apr. 3, 2014, pp. 1-8.
38	International Search Report and Written Opinion in PCT/US12/48750, dated Oct. 10, 2012, pp. 1-10.
39	ISSCC 2006 / SESSION 7 / NON-VOLATILE MEMORY / 7.7, IEEE International Solid State Circuits Conference, 2006, 10 pages.
40	Jacob, B., "Memory Systems Cache, DRAM, Disk", Morgan Kaufman Publishers, Burlington, MA, 2008, Preface and Ch. 7 pp. 315-322, 58 pages.
41	Jandhvala, S. et al. "Design-For-Test Analysis of a Buffered SDRAM DIMM". Semiconductor Group, Texas Instruments, Proceedings of International Workshop in Memory Technology, Design and Testing, Singapore, Aug. 13014, 1996, 15 pages.
42	JEDEC Definition of DIMM, Exhibit 1029, IPR No. 2017-00587, December 18, 2017, 2 pages.
43	JEDEC Global Standard for the Microelectronics Industry, Why JEDEC Standards Matter, 2014, 1 page.
44	JEDEC Standard 21-G, "Configurations for Solid State Memories," pp. 4.5.5-1 to 4.5.5-18.

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45	JEDEC Standard No. 21-C (Release 17), Annex J: Serial Presence Detects for DDR2 SDRAM (Revision 1.3), 60 pages.
46	JEDEC Standard, "Configurations for Solid State Memories", JEDEC Standard 21-C, Release 9, Aug. 1999, 144 pages.
47	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (Revision of JESD79-2A) Jan. 2006, 143 pages.
48	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79, Jun. 2006, 77 pages.
49	JEDEC Standard, Double Data Rate (DDR): SDRAM Specification: JESD79C (Revision JESD79B), Mar. 2003, pp. 1-75.
50	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification: JESD205, JEDEC Solid State Tech. Assoc., Mar. 2007, 129 pages.

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		17328019
	Filing Date		2021-05-24
	First Named Inventor	Chi-She Chen	
	Art Unit	2135	
	Examiner Name	Hashem Farrokh	
	Attorney Docket Number	0016.0010001	

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
Art Unit		
Examiner Name		
Attorney Docket Number	0016.0010001	

1	Patent Owner's Preliminary Response, SanDisk Corporation v. Netlist, Patent Number: 8,516,187, IPR2014-00982 (PTAB), dated September 26, 2014, 57 pages.
2	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,301,833, Case No. IPR2017-00649 (PTAB), filed May 1, 2017, 67 pages.
3	Patent Owner's Preliminary Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), filed May 1, 2017, 48 pages.
4	Patent Owner's Preliminary Response, Smart Modular Tech v Netlist Inc., Patent No. 8,301,833, Case IPR2014-01370 (PTAB), filed Dec. 16, 2014, 66 pages.
5	Patent Owner's Response, Patent No. 8,671,243, Case No. IPR2017-00587-12 (PTAB), filed Oct. 13, 2017, 80 pages.
6	Patent Owner's Response, SK hynix Inc., et al., v. Netlist, Patent No. 8,874,831, Case No. IPR2017-00692-12 (PTAB), filed Nov. 10, 2017, 77 pages.
7	Patterson et al., "Computer Organization & Design: The Hardware/Software Interface" Morgan Kaufmann Publishers, Inc. (1998), 71 pages.
8	Petition for Inter Partes Review of Claims 1-30 of U.S. PATENT No. 8,301,833, IPR2014-01370 (PTAB), filed August 22, 2014, 68 pages.
9	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.
10	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
11	Petition for Inter Partes Review of U.S. Pat. No. 8,301,833, filed Sep. 29, 2008.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number		17328019
Filing Date		2021-05-24
First Named Inventor	Chi-She Chen	
Art Unit		
Examiner Name		
Attorney Docket Number	0016.0010001	

12	Petition for Inter Partes Review of U.S. Pat. No. 8,510,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.
13	Petition for Inter Partes Review of U.S. Pat. No. 8,516,187 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
14	Petition for Inter Partes Review of U.S. Pat. No. 8,671,243, filed May 29, 2013.
15	Petition for Inter Partes Review of U.S. Pat. No. 8,874,834, filed Jul. 26, 2012.
16	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.
17	Petition for Inter Partes Review of U.S. Patent No. 8,301,833 (on behalf of SMART Modular Technologies, Inc.), filed Aug. 22, 2014.
18	Petition for Inter Partes Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 10, 2014.
19	Petition for Inter Partes Review of U.S. Patent 8,516,187, IPR2014-00982 (PTAB), dated June 10, 2014, 67 pages.
20	Petition for Inter Partes Review of US Patent No. 8,671,243, Case No. IPR2017-00587-1 (PTAB), May 29, 2013, 82 pages.
21	Petition for Inter Partes Review, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994 (PTAB), filed June 20, 2014, 69 pages.
22	Petition for Inter Parties Review of U.S. Patent No. 8,301,833 (on behalf of SanDisk, Corp.), filed Jun. 20, 2014.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

23	Petition for Inter Parties Review of U.S. Patent No. 8,516,187 (on behalf of SanDisk, Corp.), filed Jun. 19, 2014.
24	Petitioners Demonstratives, SK hynix Inc., et al., v. Netlist, Inc., U.S. Patent No. 8,671,243, IPR2017-00587-1037, 89 pages.
25	Petitioners' Reply in Support of Its Motion to Exclude, U.S. Patent No. 8,874,831, Case No. IPR2017-00692, filed April 9, 2018, 8 pages.
26	Petitioners' Reply to Patent Owner's Response, Inter Parties Review No. IPR2017-00587-16, Patent No. 8,671,243, filed Jan. 12, 2018, 38 pages.
27	Petitioners' Reply, U.S. Patent No. 8,874,831, Case No. IPR2017-00692 (PTAB), Paper No. 15, filed March 2, 2018, 35 pages.
28	Petitioners' Request for Hearing, U.S. Patent No. 8,301,833, Case No. Case No. IPR2017-00649-2020 (PTAB), Paper No. 8, entered Aug. 23, 2017, 18 pages.
29	Prosecution History, Application No. 12,240,916, U.S. Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date April 13, 2009, 320 pages.
30	Prosecution History, Application No. 13,559,470, US Patent No. 8,301,833, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1002 (PTAB), received date Sep. 5, 2014, 312 pages.
31	Prosecution History, Provisional Application No. 60/941,586, SK hynix Inc v Netlist Inc, Case No. IPR2017-00649-1005 (PTAB), received date Oct. 15, 2012, 23 pages.
32	Provisional Application for Advance Dynamic Disk Memory Module, Specification, SK hynix Inc., V. Netlist, Inc., Case No. IPR2017-00649-1006 (PTAB), dated Dec. 8, 2005, 53 pages.
33	Provisional Application No. 60/912,321 filed Apr. 17, 2007.

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Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

34	Provisional Application No. 60/941,586 filed Jun. 1, 2007.
35	Requirement for Restriction Election, SanDisk Corporation v. Netlist, Inc., Patent 8,301,833, IPR2014-00994, 1003 (PTAB), dated March 31, 2019, 7 pages.
36	Restriction Requirement in U.S. Appl. No. 12/240,916, dated Mar. 31, 2011.
37	Second Amended Answer and Counterclaims to Plaintiffs Complaint for Declaratory Judgment, Diablo Technologies, Inc. v. Netlist, Inc., Case No. 4:13-CV-03901 (NDCA), YGR, filed February 17, 2014, 21 pages.
38	Smart Storage Systems, Inc.'s Invalidity Contentions, Netlist, Inc. v. Smart Storage Systems, et al., Case No. 4:13-cv-05889-YGR, dated Jun. 6, 2014, 538 pages.
39	Supplemental Declaration of Daniel E. Alberti in Response to Court Order [Docket No. 361] in Support of Motion to Withdraw as Counsel of Record, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 362, filed September 5, 2018, 3 pages.
40	Supplemental Declaration of Ronald H. Spuhler, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 305-1, filed March 10, 2015, 2 pages.
41	Supplemental Declaration of Steven J. Corr, Netlist v. Smart Storage Systems, Inc. et. al., Case 4:13-cv-05889-YGR Document 309, filed March 17, 2015, 3 pages.
42	Switches - D&T Online, Switches, http://wiki.dtonline.org , Exhibit 1022, Case No. IPR2017-00587, accessed October 13, 2017, 3 pages.
43	U.S. Appl. No. 60/942,321, filed Apr. 17, 2007.
44	U.S. Office Action in U.S. Appl. No. 13/536,173, mailed on Apr. 15, 2013, pp. 1-10.

**INFORMATION DISCLOSURE
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Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

45	Updated Joint Case Management Statement, Case No. 4:13-cv-03916-YGP (NDCA), Document 53, filed Jan. 6, 2014.
46	US Patent Application No. 12/240,916, Case No. IPR2017-00692-2018 (PTAB), dated Sep. 29, 2008, 52 pages.
47	US Patent Application No. 60/912,321, Case No. No. IPR2017-00692-1007 (PTAB), filed April 17, 2017, 42 pages.
48	Using Two Chip Selects to Enable Quad Rank, an IP.com Prior Art Database Technical Disclosure, IP.com Electronic Publication: Dec. 17, 2005, 2 pages.
49	Videotaped Deposition of Russel Jacob Baker, Patent No. 8,671,243, Case Nos. IPR2017-00587-1030 (PTAB), filed December 18, 2017, 268 pages.
50	Webster's II New College Dictionary, Houghton Mifflin Company, Boston, MA, 2001, pp. 257, 259; 1114,1115, Exhibit 1017, IPR2014-01370 (PTAB), Smart Modular Tech v Netlist Inc, Patent No. 8,301,833, Sep. 22, 2014, 5 pages.

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Examiner Signature	/HASHEM FARROKH/	Date Considered	09/21/2021
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen
Art Unit	
Examiner Name	
Attorney Docket Number	0016.0010001

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Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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OR

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See attached certification statement.

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Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-06-22
Name/Print	Khaled Shami	Registration Number	38745

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Electronic Petition Request	TERMINAL DISCLAIMER TO OBIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Application Number	17328019	
Filing Date	24-May-2021	
First Named Inventor	Chi-She Chen	
Attorney Docket Number	022955-000047	
Title of Invention	FLASH-DRAM HYBRID MEMORY MODULE	
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Samsung Electronics Co., Ltd.

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Applicant claims the following fee status: ☐ Small Entity ☐ Micro Entity ☒ Regular Undiscounted	
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THIS PORTION MUST BE COMPLETED BY THE SIGNATORY OR SIGNATORIES I certify, in accordance with 37 CFR 1.4(d)(4) that I am: ☒ An attorney or agent registered to practice before the Patent and Trademark Office who is of record in this application Registration Number <u>38745</u> ☐ A sole inventor ☐ A joint inventor; I certify that I am authorized to sign this submission on behalf of all of the inventors as evidenced by the power of attorney in the application ☐ A joint inventor; all of whom are signing this request	
Signature	/Khaled Shami/
Name	Khaled Shami

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Electronic Patent Application Fee Transmittal

Application Number:	17328019			
Filing Date:	24-May-2021			
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE			
First Named Inventor/Applicant Name:	Chi-She Chen			
Filer:	Khaled Shami/Yayoi Bourne			
Attorney Docket Number:	022955-000047			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	1814	1	170	170
Pages:				
Claims:				
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Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 17328019

Filing Date: 24-May-2021

Applicant/Patent under Reexamination: Chen

Electronic Terminal Disclaimer filed on November 19, 2021

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EFS ID:	44332141
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000047
Receipt Date:	19-NOV-2021
Filing Date:	24-MAY-2021
Time Stamp:	17:23:37
Application Type:	Utility under 35 USC 111(a)

Payment information:

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<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Netlist, Inc.

CONF. NO: 6552

APPLICATION NO: 17/328,019

ART UNIT: 2135

FILING DATE: 05/24/2021

EXAMINER: HASHEM FARROKH

TITLE: FLASH-DRAM HYBRID MEMORY MODULE

AMENDMENT AND RESPONSE

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Non-Final Office Action dated September 27, 2021, making a response due on or before December 27, 2021. Accordingly, this paper is timely filed.

Amendments to the Claims begin on page 2 of this paper.

Remarks begin on page 9 of this paper.

A Conclusion appears at page 13 of this paper.

LISTING OF CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Canceled)
2. (Currently Amended) A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and a first circuit that is coupled to the plurality of ~~synchronous dynamic random access memory (SDRAM)~~ devices and to a first set of edge connections of the plurality of edge connections, wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.
3. (Previously presented) The memory module of claim 2, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.
4. (Previously presented) The memory module of claim 2, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.

5. (Currently Amended) The memory module of claim 2, further comprising:
a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal ~~the predetermined threshold voltage is ten percent below a specified operating voltage.~~

6. (Currently Amended) The memory module of claim 2, further comprising:
a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage, wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal ~~the predetermined threshold voltage is ten percent above a specified operating voltage.~~

7. (Previously presented) The memory module of claim 2, further comprising:
a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections, wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

8. (Currently Amended) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and wherein the first predetermined threshold voltage is above a specified operating voltage.

9. (Currently Amended) The memory module of claim 8, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage.

10. (Currently Amended) The memory module of claim ~~[[7]]~~8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, ~~and wherein the second predetermined threshold voltage is below a the specified operating voltage, and wherein the memory module transitions from a first operable state to a second operable state in response to the signal.~~

11. (Currently Amended) The memory module of claim 10, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage.

12. (Previously presented) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.

13. (Previously presented) The memory module of claim 7, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.

14. (Canceled)

15. (Currently Amended) The memory module of claim ~~[[14]]~~2, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.

16. (Currently Amended) A memory module comprising:
a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;
a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory

(SDRAM) devices, the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.

17. (Currently Amended) The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage, ~~and wherein the first predetermined threshold voltage is ten percent above a specified operating voltage, and the second predetermined threshold voltage is ten percent below the specified operating voltage.~~

18. (Previously presented) The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

19. (Previously presented) The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.

20. (Previously presented) The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.

21. (Previously presented) The memory module of claim 16, further comprising:

a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit, wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage, wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage, and wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.

22. (Previously presented) The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.

23. (Currently Amended) A memory module comprising:

a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;

a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and

a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and wherein the one or more operations include a write operation to transfer data into non-volatile memory.

24. (Currently Amended) The memory module of claim 23, wherein, in response to

the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state of operation of operation to a second operable state of operation of operation.

25. (Currently Amended) The memory module of claim 24, wherein, in the first operable state of operation of operation, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and wherein, in the second operable state of operation of operation, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.

26. (Currently Amended) The memory module of claim 23, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

27. (Currently Amended) The memory module of claim 26, wherein the first predetermined threshold voltage is ~~ten percent ten percent~~ above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

28 - 29. (Canceled)

30. (Previously presented) The memory module of claim 25, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.

31. (Previously presented) The memory module of claim 30, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.

32. (New) The memory module of claim 5, further comprising:
a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

33. (New) The memory module of claim 6, further comprising:
a controller coupled to the voltage monitor circuit; wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
34. (New) The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.

REMARKS

The Non-Final Office Action issued September 27, 2021, has been carefully considered.

Reconsideration in view of the following remarks is respectfully requested.

Claims 2, 5-6, 8-11, 15-17, 23-27 have been amended, and claims 32-34 have been added.

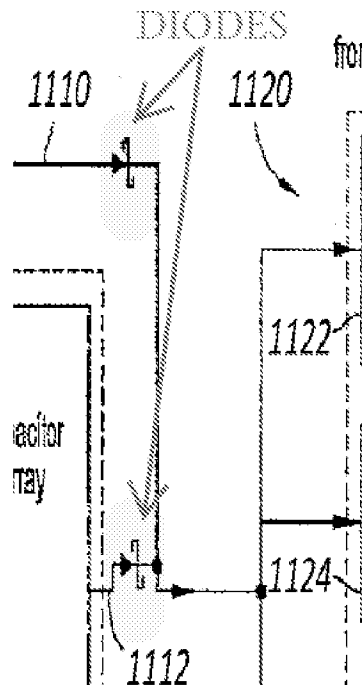
Claim Interpretation

Applicant acknowledges that the Examiner is not interpreting the claims under 35 USC 112(f), or under pre-AIA paragraph six.

Rejection under 35 USC 112

Claims 20, 22, and 30-31 stand rejected under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph, as allegedly failing to comply with the written description requirement. According to the Office Action, the “claimed specification does not appear to describe or support” the claimed first and second diodes.

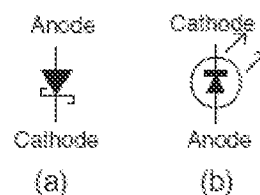
Applicant respectfully disagrees, and directs the Examiner’s attention to FIG. 16, and specifically to the symbols therein highlighted below, which represent diodes as is known in the electrical arts.



Referring for example to Chapter 5 of the Practical Electronics Handbook, Sixth Edition, 2007, it illustrates, in FIG. 5.4, a Schottky diode as follows:

Figure 5.4

Symbols: (a) Schottky diode, (b) LED.



It will be appreciated that the symbols highlighted in FIG. 16 are identical to those in the Practical Electronics Handbook that are used to represent a Schottky diode, and the drawings therefore illustrate the claimed diodes. Namely, in FIG. 16, and consistently with the claims, one diode is depicted having an input coupled to a pre-regulated fourth voltage 1110 from first power conversion element 1130 and an output coupled to voltage conversion element 1120; and another diode is depicted having an input coupled to a pre-regulated fifth voltage 1112 from second power element 1140 and an output coupled to voltage conversion element 1120.¹ The MPEP states that the fundamental inquiry behind compliance with the written description requirement (under 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph) “is whether the specification conveys with reasonable clarity to those skilled in the art that, as of the filing date sought, applicant was in possession of the invention as now claimed. See, e.g., *Vas-Cath, Inc. v. Mahurkar*, 935 F.2d 1555, 1563-64, 19 USPQ2d 1111, 1117 (Fed. Cir. 1991).”² The MPEP then explains that “An applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, **figures**, **diagrams**, and formulas that fully set forth the claimed invention. (Relying on *Lockwood v. Am. Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997), emphasis added).³

For these reasons at least, Applicant respectfully maintains that claims 20, 22, and 30-31 are in compliance with 35 U.S.C. 112(a) or 35 U.S.C. 112 (pre-A/A), first paragraph, and the rejection should be withdrawn.

Double Patenting

Timely submitted herewith is a Terminal Disclaimer over U.S. Patent No. 11,016,918 overcoming the alleged non-statutory double patenting rejection of claims 2-15, 23, and 26 -29.

Newly-Added Claims

Claims 32-34 have been added to further particularly point out and distinctly claim the subject matter of the claimed arrangement.

¹ See parenthetical clause at end of paragraph [00146] expressly characterizing the voltages 1110 and 1112 as “pre-regulated.”

² MPEP 2163.02 Standard for Determining Compliance With the Written Description Requirement

³ *Id.*

Comments on the Statement of Reasons for the Indication of Allowable Subject Matter

Applicant gratefully acknowledges the indication that claims 16-19 are 21 are allowed and that claim 24-25 contain allowable subject matter. Of these allowed and allowable claims, claims 16-17 and 24-25 have been amended, and Applicant respectfully maintains that they continue to be allowable at least for the reasons cited by the Examiner. Further, pursuant to 37 C.F.R. § 1.104, Applicant respectfully submits the instant statement commenting on the Examiner's reasons for allowance.

Applicant maintains that additional and/or alternative reasons for allowance may exist apart from those expressed by the Examiner and the Applicant, and these reasons may be independently sufficient to establish the patentability of each of the allowed dependent or independent claims.

Applicant respectfully reserves the right to introduce, articulate, or otherwise comment on any such additional reasons for allowance as may be appropriate in any future proceedings concerning the one or more claimed embodiments.

To the extent that the Examiner's reasons for allowance are inconsistent with applicable case law, statutes, and regulations, Applicant respectfully disagrees with them. Furthermore, Applicant does not admit to any characterization or limitation of the claims or to any characterization of a reference by the Examiner, particularly any that are inconsistent with the language of the claims considered in their entirety and including all of their constituent limitations.

Conclusion

In view of the foregoing, Applicant submits that the application is in condition for immediate allowance. Early notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned attorney if it is believed that such contact will expedite the prosecution of the application.

In the event this paper is not timely filed, Applicant petitions for an appropriate extension of time. Please charge any fee deficiency or credit any overpayment to Deposit Account No. 22-0585.

Respectfully submitted,

VORYS, SATER, SEYMOUR and PEASE LLP

/Khaled Shami/
Khaled Shami, Registration No. 38745
Customer No.: 151145

Date: November 19, 2021

VORYS, SATER, SEYMOUR and PEASE LLP

1909 K Street, NW, 9th Floor
Washington, DC 20006-1152
Tel: (202) 467-8800

Electronic Acknowledgement Receipt

EFS ID:	44332358
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000047
Receipt Date:	19-NOV-2021
Filing Date:	24-MAY-2021
Time Stamp:	17:26:21
Application Type:	Utility under 35 USC 111(a)

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	Multipart Description/PDF files in .zip description		
	Document Description	Start	End
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1
	Claims	2	8
	Applicant Arguments/Remarks Made in an Amendment	9	13

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New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875				Application or Docket Number 17/328,019		Filing Date 05/24/2021		☐ To be Mailed			
ENTITY: ☒ LARGE ☐ SMALL ☐ MICRO											
APPLICATION AS FILED - PART I											
		(Column 1)		(Column 2)							
FOR		NUMBER FILED		NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))		N/A		N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))		N/A		N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))		N/A		N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(i))		minus 20 = *				x \$100 =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))		minus 3 = *				x \$480 =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))		If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))											
* If the difference in column 1 is less than zero, enter "0" in column 2.						TOTAL					
APPLICATION AS AMENDED - PART II											
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	11/19/2021	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 30	Minus	** 30	= 0			x \$100 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	*** 3	= 0			x \$480 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE		0	
		(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR		PRESENT EXTRA		RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=			x \$0 =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=			x \$0 =			
	☐ Application Size Fee (37 CFR 1.16(s))										
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
								TOTAL ADD'L FEE			
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This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17328019
	Filing Date	2021-05-24
	First Named Inventor	Chi-She Chen, et al.
	Art Unit	2135
	Examiner Name	HASHEM FARROKH
	Attorney Docket Number	022955-000047

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen, et al.
Art Unit	2135
Examiner Name	HASHEM FARROKH
Attorney Docket Number	022955-000047

1	<p>an R. Sinclair and John Dunton, Practical Electronics Handbook, Sixth Edition 2007, ELSEVIER, <http://al-marefah.blogspot.com>, retrieved from the Internet November 18, 2021</p>
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If you wish to add additional non-patent literature document citation information please click the Add button

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EXAMINER SIGNATURE

Examiner Signature		Date Considered	
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen, et al.
Art Unit	2135
Examiner Name	HASHEM FARROKH
Attorney Docket Number	022955-000047

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-11-22
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal

Application Number:	17328019			
Filing Date:	24-May-2021			
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE			
First Named Inventor/Applicant Name:	Chi-She Chen			
Filer:	Khaled Shami/Yayoi Bourne			
Attorney Docket Number:	022955-000047			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	1806	1	260	260
Total in USD (\$)				260

Electronic Acknowledgement Receipt

EFS ID:	44342728
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000047
Receipt Date:	22-NOV-2021
Filing Date:	24-MAY-2021
Time Stamp:	15:41:47
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$260
RAM confirmation Number	E2021ALF42182208
Deposit Account	
Authorized User	

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:

Samsung Electronics Co., Ltd.

Ex. 1052, p. 468

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	022955-000047-IDS6-SB08.pdf	1041828	no	4
			fb71bac4e9b043ffb842a49f47066ff677bb10ccf		
Warnings:					
Information:					
A U.S. Patent Number Citation or a U.S. Publication Number Citation is required in the Information Disclosure Statement (IDS) form for autoloading of data into USPTO systems. You may remove the form to add the required data in order to correct the Informational Message if you are citing U.S. References. If you chose not to include U.S. References, the image of the form will be processed and be made available within the Image File Wrapper (IFW) system. However, no data will be extracted from this form. Any additional data such as Foreign Patent Documents or Non Patent Literature will be manually reviewed and keyed into USPTO systems.					
2	Non Patent Literature	Chapter5_practical_electronics_handbook_sixth_edition.pdf	807816	no	84
			50c00ca37f885e0f9a6bd5155f774d5543f73b6b		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	37865	no	2
			3370a6da9c7d4f0a0de929fabe365dd7c27d585a		
Warnings:					
Information:					
Total Files Size (in bytes):			1887509		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

151145 7590 12/10/2021
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

EXAMINER	
FARROKH, HASHEM	
ART UNIT	PAPER NUMBER
2135	

DATE MAILED: 12/10/2021

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/10/2022

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Maintenance fees are due in utility patents issuing on applications filed on or after Dec. 12, 1980. It is patentee's responsibility to ensure timely payment of maintenance fees when due. More information is available at www.uspto.gov/PatentMaintenanceFees.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

By mail, send to: Mail Stop ISSUE FEE
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

151145 7590 12/10/2021
Vorys, Sater, Seymour and Pease LLP
 1909 K Street, NW
 9th Floor
 Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

	(Typed or printed name)
	(Signature)
	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/10/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH, HASHEM	2135	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

1 _____

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) : ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☐ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. _____

5. **Change in Entity Status** (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552
151145	7590	12/10/2021	EXAMINER	
Vorys, Sater, Seymour and Pease LLP			FARROKH, HASHEM	
1909 K Street, NW				
9th Floor			ART UNIT	
Washington, DC 20006-1152			PAPER NUMBER	
			2135	
DATE MAILED: 12/10/2021				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 30 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 17/328,019	Applicant(s) Chen et al.	
	Examiner HASHEM FARROKH	Art Unit 2135	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 11/199/2021.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are 2-13,15-27 and 30-34. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

a) ☐ All b) ☐ Some* c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. ____.

3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: ____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date ____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>11/22/2021</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.
--	--

/HASHEM FARROKH/
Primary Examiner, Art Unit 2135

Notice of Pre-AIA or AIA Status

The present application is being examined under the pre-AIA first to invent provisions.

Terminal Disclaimer

1. *The terminal disclaimer filed on 11/19/2021 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of Application 17/138,766 now US patent 11,016,918 has been reviewed and is accepted. The terminal disclaimer has been recorded.*

INFORMATION CONCERNING IDS:

2. *The information disclosure statement (IDS) submitted on 11/22/2021 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement has been considered by the examiner.*

Allowable Subject Matter

3. *Claims 2-13, 15-27, and 30-34 allowed.*

The following is an examiner's statement of reasons for allowance:

4. *The prior art of record does not teach or suggest the distinct features "a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three*

regulated voltages”, recited in the independent claims 2 and 23. The dependent claims 3-13, 15, and 32-33 are allowed by virtue of their dependency from the independent claim 2. The dependent claims 24-27 and 30-31 are allowed by virtue of their dependency from the independent claim 23.

5. The prior art of record does not teach or suggest the distinct features “a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state”, recited in the independent claim 16. The dependent claims 17-22 and 34 are allowed by virtue of their dependency from the independent claim 16.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

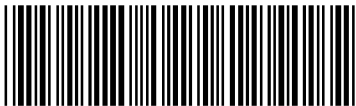
Any inquiry concerning this communication or earlier communications from the examiner should be directed to HASHEM FARROKH whose telephone number is (571)272-4193. The examiner can normally be reached on 8:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Sanjiv Shah can be reached on (571)272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. For questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

*/HASHEM FARROKH/
Primary Examiner, Art Unit 2135*

November 30, 2021

Issue Classification 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

CPC						
Symbol					Type	Version
G06F	/	13	/	28	F	2013-01-01
G06F	/	12	/	0246	I	2013-01-01
G06F	/	13	/	1694	I	2013-01-01
G06F	/	1	/	185	I	2013-01-01
G06F	/	12	/	0638	I	2013-01-01
G06F	/	13	/	4243	I	2013-01-01
G11C	/	7	/	1072	I	2013-01-01
G11C	/	14	/	0018	I	2013-01-01
G06F	/	3	/	0613	I	2013-01-01
G06F	/	3	/	0659	I	2013-01-01
G06F	/	3	/	0685	I	2013-01-01
G06F	/	13	/	4027	I	2013-01-01
G06F	/	2212	/	205	A	2013-01-01
G06F	/	2212	/	7208	A	2013-01-01

CPC Combination Sets				
Symbol	Type	Set	Ranking	Version
/				

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	30 November 2021	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	6

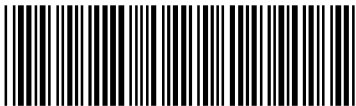
Issue Classification 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06F	/	13	/ 28
NON-CLAIMED			
/	/		

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
711	110

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135 (Primary Examiner)	30 November 2021 (Date)	O.G. Print Claim(s) 1	O.G. Print Figure 6

Issue Classification 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☒ T.D.
 ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
	1	11	10	19	19		28								
1	2	12	11	20	20		29								
2	3	13	12	21	21	27	30								
3	4	14	13	22	22	28	31								
4	5		14	24	23	5	32								
6	6	15	15	25	24	7	33								
8	7	16	16	26	25	23	34								
9	8	17	17	29	26										
10	9	18	18	30	27										

NONE (Assistant Examiner) _____ (Date) _____		Total Claims Allowed: 30	
/HASHEM FARROKH/ Primary Examiner, Art Unit 2135 (Primary Examiner) _____ (Date) _____		30 November 2021 (Date)	O.G. Print Claim(s) 1 O.G. Print Figure 6

<i>Search Notes</i> 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

CPC - Searched*		
Symbol	Date	Examiner
G11C7/1072; G11C14/0018; G06F12/0246; G06F13/4243; G06F13/1694; G06F3/0659; G06F13/4027; G06F12/0638; G06F13/28; G06F1/185; G06F2212/205; G06F2212/7208; G06F3/0685; Y02D10/00	09/22/2021	HF
G11C7/1072; G11C14/0018; G06F12/0246; G06F13/4243; G06F13/1694; G06F3/0659; G06F13/4027; G06F12/0638; G06F13/28; G06F2212/205; G06F2212/7208; G06F3/0613; G06F3/0685; Y02D10/00	11/30/2021	HF

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
711	110	09/22/2021	HF
711	110	11/30/2021	HF

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	
---	--

<i>Search Notes</i> 	Application/Control No. 17/328,019	Applicant(s)/Patent Under Reexamination Chen et al.
	Examiner HASHEM FARROKH	Art Unit 2135

Search Notes		
Search Notes	Date	Examiner
Inventor/Assignee Search	09/22/2021	HF
EAST Text Search	09/22/2021	HF
IP Search	09/22/2021	HF
Google Search	09/22/2021	HF
Inventor/Assignee Search Updated	11/30/2021	HF
EAST Text Search Updated	11/30/2021	HF

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
G11C7/1072	G11C7/00	11/30/2021	HF
G06F13/1694	G06F13/00	11/30/2021	HF
G06F2212/205	G06F2212/00	11/30/2021	HF

/HASHEM FARROKH/ Primary Examiner, Art Unit 2135	
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EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	72	((((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 14:02
L2	48	L1 AND ((G11C7/1072 OR G11C14/0018 OR G06F12/0246 OR G06F13/4243 OR G06F13/1694 OR G06F3/0659 OR G06F13/4027 OR G06F12/0638 OR G06F13/28 OR G06F1/185 OR G06F2212/205 OR G06F2212/7208 OR G06F3/0685 OR Y02D10/00).CPC. OR (711/110).CCLS. OR (G06F13/16 OR G06F3/06 OR G06F12/02 OR G06F13/42 OR G06F12/06 OR G06F13/40 OR G06F13/28 OR G06F1/18 OR G11C7/10 OR G11C14/00).IPCR.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 14:02

11/30/2021 2:04:19 PM

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BIB DATA SHEET

CONFIRMATION NO. 6552

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
17/328,019	05/24/2021	711	2135	022955-000047		
APPLICANTS Netlist, Inc., Irvine, CA INVENTORS Chi-She Chen, Walnut, CA; Jeffrey C. Solomon, Irvine, CA; Scott H. Milton, Irvine, CA; Jayesh Bhakta, Cerritos, CA;						
** CONTINUING DATA ***** This application is a CON of 17/138,766 12/30/2020 PAT 11016918 which is a CON of 15/934,416 03/23/2018 ABN which is a CON of 14/840,865 08/31/2015 PAT 9928186 which is a CON of 14/489,269 09/17/2014 PAT 9158684 which is a CON of 13/559,476 07/26/2012 PAT 8874831 which claims benefit of 61/512,871 07/28/2011 and is a CIP of 12/240,916 09/29/2008 PAT 8301833 which is a CON of 12/131,873 06/02/2008 ABN which claims benefit of 60/941,586 06/01/2007						
** FOREIGN APPLICATIONS *****						
** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/28/2021						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/HASHEM FARROKH/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY CA	SHEETS DRAWINGS 22	TOTAL CLAIMS 30	INDEPENDENT CLAIMS 3
ADDRESS Vorys, Sater, Seymour and Pease LLP 1909 K Street, NW 9th Floor Washington, DC 20006-1152 UNITED STATES						
TITLE FLASH-DRAM HYBRID MEMORY MODULE						
FILING FEE RECEIVED 1820	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			☐ All Fees ☐ 1.16 Fees (Filing) ☐ 1.17 Fees (Processing Ext. of time) ☐ 1.18 Fees (Issue) ☐ Other _____		

☐ Credit

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S465	1	(respons\$3 or based or according or "when") with (voltage adj monitor) with (detect\$3 or sens\$3 or recogniz\$3) with (chang\$3 or transit\$3) with (input adj voltage) with (memory adj module) with (transition\$3 or chang\$3) with (first adj (state or status or condition) adj operation)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 09:36
S466	11	((printed adj circuit adj board) or PCB) with (regulat\$3 near2 voltages) with (buck near2 converters)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 10:20
S467	2	S466 and (@ad<"20070601")	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 10:23
S468	0	((printed adj circuit adj board) or PCB) with (regulat\$3 near2 voltages) with (buck near2 converters)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/11/30 10:24
S469	3	((printed adj circuit adj board) or PCB) same (regulat\$3 near2 voltages) same (buck near2 converters)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2021/11/30 10:27
S470	1,361	Lee-Hyun.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S471	79	Chen-Chi-She.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/11/30 11:46

			DERWENT; IBM_TDB			
S472	75	Solomon-Jeffrey-C.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S473	36	Milton-Scott-H.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S474	41	Bhakta-Jayesh.in.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S475	4	((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S476	3	S475 and (S470 or S471 or S472 or S473 or S474)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:46
S477	12,186	(transfer\$4 or cop\$4 or transmi\$5 or mov\$3) with data with (non\$1volatile or flash or SSD or NVM) with (volatile or ?RAM or ?DRAM memory).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:48
S478	229	NETLIST.as.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:48
S479	22	S477 and S478	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO;	OR	ON	2021/11/30 11:48

			DERWENT; IBM_TDB			
S480	72	((((printed adj circuit adj board) or PCB) and (plurality near2 edge near2 connections) and SDRAM)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2021/11/30 11:52

11/30/2021 1:56:11 PM

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	17328019
	Filing Date	2021-05-24
	First Named Inventor	Chi-She Chen, et al.
	Art Unit	2135
	Examiner Name	HASHEM FARROKH
	Attorney Docket Number	022955-000047

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen, et al.
Art Unit	2135
Examiner Name	HASHEM FARROKH
Attorney Docket Number	022955-000047

1	<p>an R. Sinclair and John Dunton, Practical Electronics Handbook, Sixth Edition 2007, ELSEVIER, <http://al-marefah.blogspot.com>, retrieved from the Internet November 18, 2021</p>
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EXAMINER SIGNATURE

Examiner Signature	/HASHEM FARROKH/	Date Considered	11/30/2021
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	17328019
Filing Date	2021-05-24
First Named Inventor	Chi-She Chen, et al.
Art Unit	2135
Examiner Name	HASHEM FARROKH
Attorney Docket Number	022955-000047

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Khaled Shami/	Date (YYYY-MM-DD)	2021-11-22
Name/Print	Khaled Shami	Registration Number	38745

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The information provided by you in this form will be subject to the following routine uses:

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2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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Complete and send this form, together with applicable fee(s), by mail or fax, or via EFS-Web.

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Alexandria, Virginia 22313-1450

By fax, send to: (571)-273-2885

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

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Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

(51145) 7590 12/10/2021
Vorys, Sater, Seymour and Pease LLP
1909 K Street, NW
9th Floor
Washington, DC 20006-1152

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being transmitted to the USPTO via EFS-Web or by facsimile to (571) 273-2885, on the date below.

(Typed or printed name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	05/24/2021	Chi-She Chen	022955-000047	6552

TITLE OF INVENTION: FLASH-DRAM HYBRID MEMORY MODULE

APPLN. TYPE	ENTIFY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	UNDISCOUNTED	\$1200	\$0.00	\$0.00	\$1200	03/10/2022

EXAMINER	ART UNIT	CLASS-SUBCLASS
FARROKH. HASHEM	2135	711-110000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

2. For printing on the patent front page, list

(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,

(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Vorys, Sater, Seymour and Pease LLP

2. _____

3. _____

☐ Change of correspondence address (or Change of Correspondence Address form PTO/AIA/122 or PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/AIA/47 or PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document must have been previously recorded, or filed for recordation, as set forth in 37 CFR 3.11 and 37 CFR 3.81(a). Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

NETLIST, INC.

IRVINE, CALIFORNIA

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. Fees submitted: ☒ Issue Fee ☐ Publication Fee (if required) ☐ Advance Order - # of Copies _____

4b. Method of Payment: (Please first reapply any previously paid fee shown above)

☐ Electronic Payment via EFS-Web ☐ Enclosed check ☐ Non-electronic payment by credit card (Attach form PTO-2038)

☒ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment to Deposit Account No. 220585

5. Change in Entity Status (from status indicated above)

☐ Applicant certifying micro entity status. See 37 CFR 1.29

☐ Applicant asserting small entity status. See 37 CFR 1.27

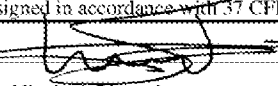
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature: 

Date December 11, 2021

Typed or printed name Khaled Shami

Registration No. 38745

Electronic Patent Application Fee Transmittal

Application Number:	17328019			
Filing Date:	24-May-2021			
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE			
First Named Inventor/Applicant Name:	Chi-She Chen			
Filer:	Khaled Shami/Yayoi Bourne			
Attorney Docket Number:	022955-000047			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	1501	1	1200	1200

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1200

Electronic Acknowledgement Receipt

EFS ID:	44492396
Application Number:	17328019
International Application Number:	
Confirmation Number:	6552
Title of Invention:	FLASH-DRAM HYBRID MEMORY MODULE
First Named Inventor/Applicant Name:	Chi-She Chen
Customer Number:	151145
Filer:	Khaled Shami/Yayoi Bourne
Filer Authorized By:	Khaled Shami
Attorney Docket Number:	022955-000047
Receipt Date:	11-DEC-2021
Filing Date:	24-MAY-2021
Time Stamp:	09:58:23
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 1200
RAM confirmation Number	E2021BA058351021
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Ex. 1052, p. 497

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	IFTransmittal.pdf	1521478	no	1
			f6bb439a0cb580c525070081789fbc9c642b0f4c		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	37643	no	2
			a7aa19502086d62deb034f9db9337ce137e14146		
Warnings:					
Information:					
Total Files Size (in bytes):			1559121		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

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9th Floor
Washington, DC 20006-1152



**Courtesy Reminder for
Application Serial No: 17/328,019**

Attorney Docket No: 022955-000047

Customer Number: 151145

Date of Electronic Notification: 12/10/2021

This is a courtesy reminder that new correspondence is available for this application. If you have not done so already, please review the correspondence. The official date of notification of the outgoing correspondence will be indicated on the form PTOL-90 accompanying the correspondence.

An email notification regarding the correspondence was sent to the following email address(es) associated with your customer number:

kshami@vorys.com

vmessinger@vorys.com

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To view your correspondence online or update your email addresses, please visit us anytime at **<https://ppair-my.uspto.gov/pair/PrivatePair>**.

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Ex. 1052, p. 499



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
17/328,019	01/25/2022	11232054	022955-000047	6552

151145 7590 01/05/2022

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ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

INVENTOR(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional inventors):

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APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Netlist, Inc., Irvine, CA

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