

UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

- - -

SAMSUNG ELECTRONICS CO., LTD,
Petitioner

vs.

NETLIST, INC.,
Patent Owner

IPR2022-00996

Patent 11,016,918

IPR2022-00999

Patent 11,232,054

Deposition of WILLIAM MANGIONE-SMITH, PH.D.

Monday, June 12, 2023

Job No.: J9759315

Pages 1 - 245

Reported by: Gail L. Verbano

BA, RDR CRR, CSR-CA No. 8635

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8 Whereupon, the remote video-recorded
9 deposition of WILLIAM MANGIONE-SMITH, PH.D., was
10 held via videoconference on Monday, June 12,
11 2023, beginning at approximately 9:06 a.m.,
12 Pacific Time, the proceedings being recorded
13 stenographically by Gail Verbano, Registered
14 Diplomate Reporter, Certified Realtime Reporter,
15 Certified Shorthand Reporter, and transcribed
16 under her direction.
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I N D E X

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DEPONENT:	EXAMINATION	PAGE
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	By Attorney Chandler	226

E X H I B I T S

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Exhibit 1076	Red-line comparison of the	17
	declarations of	
	Dr. Mangione-Smith (165 pages)	
Exhibit 1077	Netlist PowerPoint	81
	presentation, Technology	
	Tutorial" in re: 337-TA-1023,	
	5-8-17 (CDX-200.1 to .14)	
Exhibit 1078	Data sheet for ADP1821	138
	Step-Down DC-to-DC controller	
	(24 pages)	

PREVIOUSLY MARKED EXHIBITS REFERENCED:

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Exhibit 10018

Exhibit 100345

Exhibit 102323

Exhibit 102424

Exhibit 102525

Exhibit 102626

Exhibit 102727

Exhibit 102828

Exhibit 103830

Exhibit 1042228

Exhibit 104569

Exhibit 104669

Exhibit 1048127

Exhibit 1058107

Exhibit 1062129

Exhibit 2012192

Exhibit 201369

Exhibit 201646

Exhibit 202948

Exhibit 203118

Exhibit 2032141

Exhibit 2035165

Exhibit 2038180

1 PREVIOUSLY MARKED EXHIBITS REFERENCED:

2 NUMBER PAGE

3 Exhibit 204496

4 Exhibit 2045102

5 Exhibit 204669

6 Exhibit 206118

7 Exhibit 2101170

8

9 QUESTIONS INSTRUCTED NOT TO ANSWER:

10 PAGE LINE

11 (None)

12

13 REQUEST FOR PRODUCTION OF DOCUMENTS

14 PAGE LINE

15 (None)

16

17 QUESTIONS MARKED

18 PAGE LINE

19 (None)

20

21

22 REPORTER'S NOTE:

23 QUOTATION MARKS ARE USED FOR CLARITY AND DO NOT NECESSARILY

24 REFLECT A DIRECT QUOTE.

25

1 --000--

2 P R O C E E D I N G S

3 --000--

08:20:32

4 THE VIDEOGRAPHER: Good morning. We're
5 now on the record at 9:06 a.m. Pacific Time on
6 June 12th, 2023.

09:06:25

09:06:26

09:06:30

7 This begins the videoconference

09:06:33

8 deposition of Dr. William Mangione-Smith --

09:06:35

9 excuse me -- taken in the matter of Samsung

09:06:39

10 Electronics Company, Limited, versus Netlist,

09:06:42

11 Incorporated, filed in the Patent and Trial

09:06:45

12 Appeal Board, United States Patent and Trademark

09:06:50

13 Office, Case Number IPR2022-00996, and Case

09:06:53

14 Number IPR2022-00999.

09:07:06

15 My name is Dana Bachman. I'm your

09:07:15

16 videographer today. Our court reporter is Gail

09:07:17

17 Verbano. We're both representing Esquire

09:07:19

18 Deposition Solutions.

09:07:21

19 Will everyone present please identify

09:07:23

20 themselves, beginning with the noticing attorney.

09:07:25

21 ATTORNEY CHANDLER: Good morning. This

09:07:28

22 is Ted Chandler from Baker Botts on behalf of the

09:07:29

23 Petitioner, Samsung Electronics Co., Limited; and

09:07:32

24 with me are my colleagues, Dr. Ferenc Pazmandi

09:07:36

25 and Dr. Leon Wong.

09:07:39

1 ATTORNEY LINDSAY: And this is Jonathan 09:07:43
2 Lindsay with Irell & Manella for Patent Owner 09:07:44
3 Netlist, Inc., defending Dr. Mangione-Smith; and 09:07:48
4 with me is my colleague, Dr. Annita Zhong. 09:07:53
5 THE VIDEOGRAPHER: Thank you very much. 09:07:58
6 Madam Reporter, would you please swear 09:07:59
7 in our witness. 09:08:01
8 09:08:13
9 Whereupon, 09:08:13
10 WILLIAM MANGIONE-SMITH, PH.D., 09:08:14
11 being first duly sworn or affirmed to testify to the 09:08:14
12 truth, the whole truth, and nothing but the truth, 09:08:14
13 was examined and testified as follows: 09:08:14
14 09:08:14
15 EXAMINATION 09:08:14
16 BY ATTORNEY CHANDLER: 09:08:13
17 Q. Good morning. Please state your name 09:08:17
18 for the record. 09:08:18
19 A. William Henry Mangione-Smith. 09:08:19
20 Q. Dr. Mangione-Smith, were you retained 09:08:24
21 by Netlist to provide opinions in these two cases 09:08:25
22 related to Netlist's '918 and '054 patents? 09:08:29
23 A. Yes, I was. 09:08:37
24
25

1	(Exhibit Number 1001 was previously	09:08:37
2	marked for identification.)	09:08:37
3	BY ATTORNEY CHANDLER:	09:08:37
4	Q. And the '918 patent has been marked as	09:08:37
5	Exhibit 1001 in IPR2022-00996 and is U.S. Patent	09:08:40
6	Number 11,016,918; correct?	09:08:47
7	A. Yes.	09:08:57
8	Q. And the '054 patent is marked as	09:08:57
9	Exhibit 1001 in IPR - , and is number	09:08:59
10	11,232,054; correct?	09:09:05
11	A. Yes, that's correct.	09:09:10
12	Q. And where are you physically located	09:09:13
13	right now?	09:09:14
14	A. My home office in Kirkland, Washington.	09:09:15
15	Q. Given that this is a remote deposition,	09:09:25
16	meaning we're not in the same physical room	09:09:27
17	together, there are a few questions I need to	09:09:29
18	ask, starting with: Is there anyone else in the	09:09:31
19	room with you right now?	09:09:33
20	A. No.	09:09:35
21	Q. And given that I cannot see the room	09:09:36
22	that you're in, will you please let me know if	09:09:38
23	someone enters the room that you're in at any	09:09:41
24	time before this deposition ends?	09:09:43
25	A. Yes, I will.	09:09:47

1 Q. Did you bring anything with you to your
2 deposition today?

3 A. No, I did not.

4 Q. Do you have any, for example, printed
5 copies of any of the exhibits or declarations
6 from these two cases in front of you?

7 A. No, I do not.

8 Q. And are you looking at anything on your
9 screen besides the video feed and the PDF
10 exhibits that I've been sending to you through
11 the chat?

12 A. Just a folder with the PDFs, getting
13 ready to open them.

14 Q. And to be clear, do you have any PDFs
15 of the exhibits that you're looking at that have
16 any notes on them that haven't been shared with
17 me?

18 A. No, I do not.

19 Q. We will take breaks throughout your
20 deposition today, but I wanted to remind you that
21 during those breaks, under the rules governing
22 these two cases, you should not consult with your
23 counsel about the substance of your testimony
24 during the breaks while I'm taking your
25 testimony.

1	Understood?	09:11:08
2	A. Yes, that's understood.	09:11:09
3	Q. And during the deposition, I would ask	09:11:12
4	that you do not look things up on the internet or	09:11:14
5	do other things on the computer or on your phone	09:11:17
6	that we cannot see on camera.	09:11:20
7	Understood?	09:11:23
8	A. I'm sorry. Could you repeat that	09:11:23
9	question.	09:11:24
10	Q. I would ask, during the deposition,	09:11:26
11	that you do not look things up on the internet or	09:11:27
12	do things on the computer or on your phone that	09:11:30
13	we cannot see on the camera.	09:11:36
14	Do you understand?	09:11:38
15	A. Assuming you mean while on the record,	09:11:39
16	yes, I understand that.	09:11:41
17	Q. Correct.	09:11:47
18	And you understand that during your	09:11:47
19	deposition you should not be emailing or texting	09:11:49
20	other people?	09:11:51
21	A. Yes.	09:11:51
22	Q. Do you have any questions for me about	09:11:52
23	the procedure for today's deposition?	09:11:54
24	A. No, I do not.	09:11:57
25	Q. And you understand that this is two	09:12:01

1 depositions for two cases being taken at the same
2 time, and so it's possible that we may extend
3 into a second day, starting tomorrow at
4 9:00 a.m.?

5 A. Yes, that's my understanding.

6 Q. What did Netlist ask you to do in these
7 two IPRs?

8 A. They asked me to review the
9 documentation that had been produced prior to my
10 review, and to consider -- to determine what I
11 thought of the arguments that were made regarding
12 invalidity.

13 Q. Did anyone help you with your work in
14 these two matters?

15 A. "Help" is a very broad term.
16 Certainly, for example, people sent me PDFs and
17 sent me the documents. It's likely that -- it's
18 possible, I wouldn't even say "likely," that
19 somebody said, "Hey, you may want to focus on
20 this section as a priority." I don't remember
21 that happening, but for the most part, I'd say
22 no, nobody really helped me with my work on this.

23 Q. And when you say that people sent you
24 PDFs or people may have asked you to focus, are
25 you referring to the attorneys at the Irell &

1 Manella firm, or are there other people you're 09:13:29
2 referring to? 09:13:32

3 A. Those were the only people I would have 09:13:35
4 been referring to -- that I was referring to, 09:13:36
5 yes. 09:13:39

6 Q. Is there anyone besides the attorneys 09:13:39
7 at the Irell & Manella firm that you interacted 09:13:45
8 with for purposes of forming your opinions in 09:13:50
9 this matter? 09:13:54

10 A. It's possible. I have interacted with 09:14:04
11 Dr. Thomas Barr. I don't recall that 09:14:08
12 specifically being with regards to my efforts on 09:14:12
13 the IPR, though. 09:14:15

14 Q. And who is Dr. Thomas Barr? I'm not 09:14:17
15 familiar with him. 09:14:21

16 A. He's a -- he's a Ph.D. at Irell, and my 09:14:23
17 understanding is he's not an attorney. But as I 09:14:25
18 said, I don't remember anything specific with 09:14:33
19 regards to the IPR efforts where I interacted 09:14:35
20 with him. 09:14:38

21 Q. And outside of people at Irell, was 09:14:39
22 there anyone else that you interacted with for 09:14:41
23 purposes of forming your opinions in these two 09:14:44
24 IPRs? 09:14:46

25 A. Not that I recall as I sit here today. 09:14:51

1 Q. And what did you do to prepare for 09:14:55
2 today's deposition and tomorrow's deposition? 09:14:58

3 A. Well, I reviewed my declaration, and 09:15:03
4 the materials -- some of the materials that I 09:15:05
5 was -- I'm sorry. 09:15:08

6 I reviewed my declarations, the two, 09:15:08
7 and the materials that they cited. And there 09:15:10
8 were, I think, three different phone calls with 09:15:18
9 counsel at Irell to discuss issues that may come 09:15:23
10 up today and tomorrow. 09:15:28

11 Q. And who attended those phone calls? 09:15:32

12 A. That would be Jonathan Lindsay and 09:15:35
13 Dr. Annita Zhong. 09:15:38

14 Q. Anyone else? 09:15:40

15 A. Nope. Well, and myself, clearly, yeah. 09:15:42

16 Q. And approximately how long were those 09:15:49
17 three phone calls? 09:15:51

18 A. Probably seven or eight hours in total. 09:15:56

19 Q. And in the last few weeks, about how 09:16:00
20 many hours in total did you prepare on your own 09:16:05
21 for the deposition today and tomorrow in these 09:16:08
22 two IPRs? 09:16:11

23 A. It's hard to say. Probably -- I would 09:16:19
24 estimate another 10 to 14 hours. 09:16:22

25 Q. So in total, approximately 20 hours of 09:16:30

1	preparation for the deposition today and	09:16:32
2	tomorrow; is that fair?	09:16:35
3	A. Over the last two weeks, yes. Yeah.	09:16:36
4	Q. Approximately how many hours in total	09:16:46
5	have you spent working on these two IPRs?	09:16:47
6	A. I don't have an estimate with regards	09:16:52
7	to that.	09:16:53
8	I've worked on, as I'm sure you're	09:16:56
9	aware, a couple of other matters for Netlist. So	09:16:58
10	I don't have any -- I have no estimate in my head	09:17:02
11	that I feel comfortable making as I sit here.	09:17:07
12	Q. In the past year and a half,	09:17:13
13	approximately how many hours in total have you	09:17:17
14	worked on all of the matters for Netlist?	09:17:20
15	ATTORNEY LINDSAY: Objection; form.	09:17:28
16	THE WITNESS: I can't reasonably make	09:17:31
17	any reliable estimate as I sit here on this. I	09:17:33
18	would have to review my billing statements.	09:17:35
19	BY ATTORNEY CHANDLER:	09:17:39
20	Q. Be fair to say at least a couple of	09:17:40
21	hundred hours over the past year and a half	09:17:41
22	you've worked for -- on the matters for Netlist?	09:17:44
23	Is that fair?	09:17:47
24	ATTORNEY LINDSAY: Objection; form.	09:17:48
25	THE WITNESS: I wouldn't say that. As	09:17:51

1	I sit here, I'm not comfortable providing any	09:17:52
2	estimate.	09:17:54
3	BY ATTORNEY CHANDLER:	09:17:57
4	Q. How much are you charging Netlist per	09:17:58
5	hour for your time spent on these two IPRs?	09:18:00
6	A. My current rate that I ask new clients	09:18:03
7	for is 750. I don't recall if Netlist -- and I	09:18:07
8	don't increase that over time, even for matters	09:18:15
9	that take multiple years. So I don't recall	09:18:18
10	exactly when Netlist and I -- when Netlist	09:18:20
11	engaged me through Irell, but it's probably	09:18:24
12	between 650 and \$750 an hour.	09:18:28
13	Q. And over the past year and a half,	09:18:39
14	would it be fair to say that you have billed	09:18:41
15	Netlist in excess of \$100,000 for the time spent	09:18:44
16	working on Netlist matters?	09:18:49
17	A. Possibly. As I suggested though, I'm	09:18:52
18	not really comfortable making any estimate off	09:18:54
19	the top of my head. There is a number that I	09:19:00
20	have billed them for that can be determined	09:19:01
21	precisely.	09:19:04
22	Q. By you; correct?	09:19:08
23	A. Sure. By me, presumably by Irell or	09:19:11
24	Netlist.	09:19:14
25	Q. Approximately how many times have you	09:19:17

1 been deposed before?

09:19:19

2 A. Oh, too many times. Too many times
3 this year. Probably more than 20 different
4 matters. Certainly more than 20 days.

09:19:24

09:19:26

09:19:30

5 Q. And have you testified at trial before?

09:19:41

6 A. Yes, I have.

09:19:43

7 Q. How many times?

09:19:44

8 A. I've testified mostly at trial at the
9 ITC. I've also testified in front of a jury at
10 least three times. I thought it was four, but
11 recently I went back to look and it might only be
12 three.

09:19:46

09:19:51

09:19:58

09:20:00

09:20:02

13 Q. I want to talk about your declarations
14 and your CV. And actually I want to introduce a
15 new exhibit, which is a red-line comparison of
16 your two declarations. So really just a way for
17 any of us to see the differences more quickly.
18 So I'll mark that as Exhibit 1076 in both IPRs.

09:20:11

09:20:15

09:20:21

09:20:26

09:20:32

09:20:39

19 (Whereupon, Exhibit Number 1076 was
20 marked for identification in both
21 IPR cases and are attached hereto.)

09:20:39

09:20:39

09:20:39

22 ATTORNEY CHANDLER: And I'll send the
23 same document twice, one for the first IPR and
24 one for the second IPR. That is the same
25 document, just with a different stamp on the

09:20:39

09:20:48

09:20:52

09:20:55

1 bottom right. Let me know when you have
2 Exhibit 1076.

09:20:58

09:21:00

3 And to be more precise, Exhibit 1076 is
4 a computer-generated red-line comparing your
5 declaration in IPR2022-00999, marked as
6 Exhibit 2061 to your declaration; and
7 IPR2022-00996 marked as Exhibit 2031.

09:21:06

09:21:09

09:21:11

09:21:16

09:21:20

8 (Exhibit Numbers 2031 and 2061 were
9 previously marked for
10 identification.)

09:21:27

09:21:27

09:21:27

11 THE WITNESS: All right. I have the
12 '054 downloaded and the '918 is downloading now.
13 And which one would you like me to open first?

09:21:35

09:21:36

09:21:39

14 BY ATTORNEY CHANDLER:

09:21:43

15 Q. They're the same, so either one.

09:21:43

16 A. Okay. It's just the file sizes are
17 different.

09:21:45

09:21:48

18 Q. I think the stamp -- it should be a
19 function of the stamping.

09:21:49

09:21:53

20 A. Okay, I have it opened.

09:22:02

21 Q. And just as a general matter, is it
22 fair to say that there's similarities between
23 your two declarations and the two IPRs, as shown
24 in the red-line, as marked as Exhibit 1076?

09:22:06

09:22:08

09:22:13

09:22:15

25 A. Sure.

09:22:18

1	Q. Look at your CV at the end of your	09:22:23
2	declaration, so either Exhibit 2031 in	09:22:29
3	IPR2022-00996 or Exhibit 2061 in IPR2022-00999.	09:22:35
4	At the end of both of those declarations is what	09:22:42
5	I believe is your CV; correct?	09:22:47
6	A. Yes.	09:23:00
7	Q. Does the CV at the end of your expert	09:23:01
8	declaration in the two IPRs list all of your	09:23:04
9	prior expert engagements in which you were either	09:23:07
10	deposed or testified at trial?	09:23:10
11	A. It is intended to include that	09:23:14
12	information, yes.	09:23:17
13	Q. When did you start your work for	09:23:25
14	Netlist in these two IPRs?	09:23:27
15	A. I don't know for sure. Likely sometime	09:23:38
16	mid last year.	09:23:42
17	Q. So approximately a year ago?	09:23:48
18	A. That's -- yes, that's an estimate.	09:23:50
19	It's probably -- yeah.	09:23:52
20	Q. And do you have your two expert	09:23:58
21	declarations on the screen in front of you?	09:24:01
22	A. Yes, I do.	09:24:06
23	Q. Are your expert declarations marked as	09:24:07
24	Exhibit 2031, for the '918 patent, and	09:24:17
25	Exhibit 2061, for the '054 patent, complete?	09:24:20

1 Meaning, do they provide a complete statement of 09:24:23
2 all the opinions that you intend to express in 09:24:26
3 each IPR along with the basis and the reasons for 09:24:28
4 those opinions? 09:24:32

5 A. I don't understand the question of what 09:24:35
6 I intend to express or state. So it's what I've 09:24:38
7 intended to state in these declarations. 09:24:41

8 Q. And you've reviewed the declarations. 09:24:45
9 And my question is: In your perspective, are the 09:24:46
10 two complete? Meaning do they provide a complete 09:24:53
11 statement of all of the opinions that you intend 09:24:57
12 to express in each IPR along with the basis and 09:24:59
13 the reasons for those opinions? 09:25:03

14 A. Again, it sounds like either you're 09:25:10
15 asking me if they're complete with regards to 09:25:11
16 what I intended to state within them; and the 09:25:14
17 answer would be sure, yeah, they are. 09:25:19

18 But if you're asking me about opinions 09:25:22
19 that I intend to state regarding -- in the 09:25:24
20 context of the IPR in the future, I don't have 09:25:28
21 any particular expectations of stating any more 09:25:30
22 opinions. 09:25:33

23 Q. Are your expert declarations, marked as 09:25:36
24 Exhibit 2031, in IPR2022-00996, and Exhibit 2061, 09:25:39
25 in IPR 202022-0999, accurate? Meaning, they do 09:25:48

1 not have any mistakes?

09:25:54

2 A. Well, there likely are mistakes. I
3 don't know of any -- there almost certainly are
4 mistakes. There always seem to be.

09:26:04

09:26:09

09:26:12

5 I don't know of any material -- any
6 mistakes that are really material to
7 understanding my opinions, with one exception.

09:26:15

09:26:18

09:26:24

8 There was a place -- my recollection
9 is, there was one place where I had stated an
10 opinion fairly clearly three or four times, and
11 then in one sentence I said, "It's clear that
12 this is not supported." And the "not" was in
13 error.

09:26:31

09:26:35

09:26:39

09:26:44

09:26:48

09:26:52

14 But I think that -- I don't recall
15 exactly where that was. And reviewing the
16 context, I believe that my intention was clear.

09:26:54

09:26:55

09:27:00

17 Q. And could you generally describe the
18 opinion that you stated three or four times, to
19 help us more easily identify the error where
20 later you said "not supported" when, in fact, you
21 intended to say that something was supported? So
22 for example, what generally do you recall the
23 discussion concerned?

09:27:07

09:27:13

09:27:15

09:27:22

09:27:24

09:27:27

09:27:31

24 A. Yeah, I can try to -- that's something
25 that I could try to review during a break. But

09:27:34

09:27:38

1	as I sit here, no, I don't recall -- I wouldn't	09:27:43
2	even point you more closely, Oh, it's generally	09:27:46
3	related to this piece of prior art.	09:27:49
4	But as I said, I don't believe that the	09:27:53
5	error would have confused somebody reviewing it	09:27:59
6	with regards to what my opinions are.	09:28:04
7	Q. Are there any other errors that you	09:28:09
8	recall in your two declarations that you came	09:28:15
9	across during the time you spent in the last	09:28:17
10	couple of weeks preparing for today's deposition?	09:28:21
11	A. No.	09:28:26
12	Q. Have you carefully read Netlists '918	09:28:34
13	patent, marked as Exhibit 1001 in IPR2022-00996?	09:28:37
14	A. What was the exhibit number, please?	09:28:45
15	Again, sorry.	09:28:47
16	Q. 1001 in IPR2022-00996.	09:28:50
17	A. Sure. Yes, I have.	09:28:57
18	Q. Do you believe you understand Netlist's	09:28:59
19	'918 patent?	09:29:03
20	A. I believe I have an understanding of	09:29:04
21	it, yes.	09:29:05
22	Q. Do you believe you understand the	09:29:07
23	figures in Netlist's '918 patent?	09:29:08
24	A. I believe I have an understanding of	09:29:13
25	the figures, yes.	09:29:14

1 Q. And you believe you understand the 09:29:16
2 claims at the end of '918 patent? 09:29:18

3 A. I believe I have an understanding of 09:29:23
4 the claims, yes. 09:29:24

5 Q. Have you carefully read Netlist's '054 09:29:25
6 patent, marked as Exhibit 1001 in the second IPR, 09:29:29
7 number IPR2022-00999? 09:29:35

8 A. Yes. 09:29:44

9 Q. Do you believe you understand the '054 09:29:44
10 patent? 09:29:47

11 A. Yes, I have an understanding of it. Is 09:29:50
12 that -- I'm sorry. Never mind. I found it. 09:29:52

13 Okay. Yes, I have an understanding of 09:29:57
14 it. 09:29:59

15 Q. And it's fair to say the '918 and the 09:30:00
16 '054 patent, they have the same specifications 09:30:02
17 and figures; correct? 09:30:05

18 A. Yes, that's my understanding. Yeah. 09:30:08

19 Q. And you believe that you understand the 09:30:11
20 claims at the end of the '054 patent? 09:30:13

21 A. Yes, I believe I have an understanding 09:30:17
22 of the claims at the end of the '054 patent. 09:30:19

23 (Exhibit Number 1023 was previously
24 marked for identification.)
25

1 BY ATTORNEY CHANDLER:

09:30:22

2 Q. Could you please turn to Exhibit 1023,
3 which is the same in both IPRs, and let me know
4 when you're there.

09:30:23

09:30:26

09:30:29

5 A. Yes. This is the Harris application,
6 and I have it opened in front of me.

09:30:40

09:30:44

7 Q. Have you carefully read the Harris
8 prior art reference marked, as Exhibit 1023 in
9 both IPRs?

09:30:46

09:30:48

09:30:50

10 A. I have read the Harris patent
11 application with a focus on the elements that
12 were relied upon in making arguments in the
13 context of the IPR. But Harris is fairly short,
14 so I don't know that there's nothing of anything
15 beyond that that's disclosed in it.

09:30:54

09:30:56

09:31:00

09:31:06

09:31:08

09:31:13

16 Q. Do you believe you understand the
17 Harris prior art reference marked as Exhibit 1023
18 in both IPRs?

09:31:15

09:31:16

09:31:18

19 A. I have an understanding of it, yeah.
20 (Exhibit Number 1024 was previously
21 marked for identification.)

09:31:21

09:31:24

09:31:24

22 BY ATTORNEY CHANDLER:

09:31:24

23 Q. Please turn to Exhibit 1024, which is
24 the same in both IPRs, and let me know when you
25 have that in front of you.

09:31:24

09:31:26

09:31:28

1 A. Yes, this is the '604 Amidi reference. 09:31:40
2 I have it in front of me now. 09:31:45
3 Sorry, Amidi. 09:31:49
4 Q. Amida, A-M-I-D-I; correct? 09:31:51
5 A. Yes, sir. 09:31:54
6 Q. Have you carefully read the Amidi prior 09:31:54
7 art reference, marked as Exhibit 1024 in both 09:31:56
8 IPRs? 09:31:59
9 A. Yes, I have with a particular focus on 09:32:02
10 the elements that were cited and relied upon by 09:32:04
11 others to make arguments in this IPR. 09:32:11
12 Q. And do you believe that you understand 09:32:15
13 the Amidi prior art reference, marked as 09:32:19
14 Exhibit 1024 in both IPRs? 09:32:21
15 A. I believe I have an understanding of 09:32:25
16 it, yes. 09:32:26
17 (Exhibit Number 1025 was previously 09:32:27
18 marked for identification.) 09:32:27
19 BY ATTORNEY CHANDLER: 09:32:28
20 Q. Please pull up Exhibit 1025, which is 09:32:28
21 the same in both IPRs, and let me know when 09:32:30
22 you're there. 09:32:33
23 A. Yes, sir, I'm there. 09:32:49
24 Q. Have you carefully read the Spiers 09:32:50
25 prior art reference, marked as Exhibit 1025 in 09:32:53

1 both IPRs? 09:32:57

2 A. I have reviewed Spiers with a 09:32:58

3 particular emphasis on the arguments made by 09:33:01

4 Dr. Wolfe and any others regarding its relevance 09:33:04

5 in this IPR. 09:33:07

6 Q. And do you believe you understand the 09:33:09

7 Spiers prior art reference, marked as 09:33:10

8 Exhibit 1025 in both IPRs? 09:33:13

9 A. I believe I have an understanding of 09:33:18

10 it, yes. 09:33:19

11 (Exhibit Number 1026 was previously 09:33:19

12 marked for identification.) 09:33:19

13 BY ATTORNEY CHANDLER: 09:33:19

14 Q. Please turn to Exhibit 1026. Let me 09:33:19

15 know when you're there. 09:33:22

16 A. I am there. 09:33:33

17 Q. Have you carefully read the JEDEC 09:33:34

18 JESD79-2B DDR2 SDRAM specification dated 09:33:38

19 January 2005, marked as Exhibit 1026 in both 09:33:49

20 IPRs? 09:33:55

21 A. I have reviewed this document 09:33:58

22 specifically in the regards to -- in regards to 09:34:00

23 the way in which it was relied upon by Dr. Wolfe 09:34:02

24 and potentially others in the context of this 09:34:08

25 IPR. 09:34:11

1 Q. And do you believe that you understand 09:34:13
2 the JEDEC JESD79-2BDD DDR2 SDRAM specification 09:34:14
3 dated January 2005, marked as Exhibit 1026 in 09:34:23
4 both IPRs? 09:34:26

5 A. I have an understanding of it. There 09:34:28
6 are many elements of this document, in 09:34:31
7 particular, that, in my opinion, are not relevant 09:34:33
8 to the IPR arguments; but I have an understanding 09:34:37
9 of it, yes. 09:34:41

10 (Exhibit Number 1027 was previously 09:34:41
11 marked for identification.) 09:34:41

12 BY ATTORNEY CHANDLER: 09:34:41

13 Q. Please turn to Exhibit 1027, which is 09:34:41
14 the same in both IPRs. Let me know when you're 09:34:44
15 there. 09:34:46

16 A. I have it opened in front of me. 09:34:53

17 Q. Have you carefully read the JEDEC 09:34:56
18 JESD82-20 FBDIMM, advanced memory buffer standard 09:34:57
19 dated March 2007, marked as Exhibit 1027 in both 09:35:07
20 IPRs? 09:35:14

21 A. I have carefully read and reviewed the 09:35:15
22 elements of this document that were cited and 09:35:18
23 relied upon by Dr. Wolfe and others in the 09:35:22
24 context of this IPR. 09:35:25

25 I'm sorry. I gave you the impression I 09:35:27

1 had stopped speaking. 09:35:30

2 Q. Do you believe that you understand the 09:35:32

3 JEDEC JESD82-20 FBDIMM advanced memory buffer 09:35:35

4 standard dated March 2007, marked as Exhibit 1027 09:35:42

5 in both IPRs? 09:35:46

6 A. I believe I have an understanding of 09:35:50

7 this document, particularly in the context of how 09:35:52

8 it has been relied upon by Dr. Wolfe and others 09:35:57

9 in this IPR. 09:36:00

10 (Exhibit Number 1028 was previously 09:36:01

11 marked for identification.) 09:36:01

12 ATTORNEY CHANDLER: Please turn to 09:36:04

13 Exhibit 1028, which is the same in both IPRs, and 09:36:05

14 let me know when you're there. 09:36:08

15 A. I am there. 09:36:16

16 Q. Have you carefully read the JEDEC 09:36:17

17 JESD205 DDR2 SDRAM fully buffered DIMM design 09:36:19

18 specification dated March 2007, marked as 09:36:29

19 Exhibit 1028 in both IPRs? 09:36:34

20 A. Yes, I believe I have. This document 09:36:39

21 looks a little odd. I don't think it -- I don't 09:36:46

22 recall if it matches exactly what I reviewed or 09:36:48

23 not. 09:36:50

24 The reason I say it's odd is there's 09:36:51

25 a -- there's a PDF enabled comment in the bottom 09:36:53

1 left. If that was in the PDF that I reviewed -- 09:36:56
2 I'm not saying it wasn't. I just don't recall. 09:37:00

3 But setting aside that issue, I did 09:37:02
4 review this document; and I have an understanding 09:37:07
5 of it specifically in the context of how it has 09:37:11
6 been relied upon by Dr. Wolfe and others in their 09:37:14
7 arguments regarding this IPR. 09:37:19

8 Q. And just for clarity, you referred to a 09:37:24
9 comment in the PDF. Is there any content to that 09:37:26
10 comment that you're referring to? 09:37:34

11 A. There is, not that is meaningful to me. 09:37:36
12 It says "Unmarked sent by" and then in uppercase, 09:37:38
13 SLIQUORI. 09:37:42

14 I -- I have no idea what that means. 09:37:47

15 Q. I think what that means is that when 09:37:49
16 this was stamped by a paralegal, their name may 09:37:52
17 have appeared. 09:37:55

18 A. It doesn't -- it -- certainly doesn't 09:37:57
19 seem to be meaningful and relevant to my analysis 09:38:00
20 at all. You know, it just makes me wonder if 09:38:04
21 there's any comments or anything else later on in 09:38:07
22 the document, but I have no reason to think there 09:38:09
23 is. 09:38:11

24 Q. And I'm not aware of any. Again, I 09:38:13
25 think that may be tied to the stamped 09:38:18

1 "Exhibit 1028" in the bottom right. But if you 09:38:21
2 do come across a comment that you think suggests 09:38:24
3 that an attorney was leaving comments in the 09:38:28
4 document, let me know. But as far as I know, 09:38:36
5 there shouldn't be anything like that in there. 09:38:37
6 Understood? 09:38:39
7 A. Understood. 09:38:40
8 Q. And for clarity, do you believe you 09:38:43
9 understand that JEDEC JESD205 DDR2 SDRAM fully 09:38:45
10 buffered DIMM design specification dated 09:38:51
11 March 2007, marked as Exhibit 1028 in both IPRs? 09:38:55
12 A. I believe I have an understanding of 09:39:02
13 it, particularly in regards to how it was relied 09:39:04
14 upon by Dr. Wolfe and others in the context of 09:39:09
15 this IPR. 09:39:13
16 (Exhibit Number 1038 was previously 09:39:13
17 marked for identification.) 09:39:13
18 BY ATTORNEY CHANDLER: 09:39:14
19 Q. Please turn to Exhibit 1038, which is 09:39:18
20 the same in both IPRs, and let me know when 09:39:20
21 you're there. 09:39:22
22 A. This appears to be the Hajeck 09:39:30
23 reference. And I have it opened in front of me 09:39:33
24 now. 09:39:35
25 Q. And before we go further, that was a 09:39:35

1 question I had, is how you would pronounce the
2 name. But to be clear, the name is spelled
3 H-A-J-E-C-K; correct?

09:39:42

09:39:44

09:39:47

4 A. Yes, sir. And if you know how to
5 pronounce it correctly with any confidence, I'd
6 be happy to take some advice on that. I
7 hesitate, but I'm not sure.

09:39:53

09:39:54

09:39:56

09:40:00

8 Q. I'm not sure either. It could be
9 "Hajeck."

09:40:01

09:40:05

10 A. Yeah.

09:40:06

11 Q. Have you carefully read the Hajeck
12 prior art reference, marked as Exhibit 1038 in
13 both IPRs?

09:40:11

09:40:14

09:40:16

14 A. I have, particularly with regards to
15 the -- how it's been relied upon by Dr. Wolfe and
16 others in the context of this IPR.

09:40:20

09:40:22

09:40:27

17 Q. And do you believe that you understand
18 the Hajeck prior art reference marked as
19 Exhibit 1038 in both IPRs?

09:40:28

09:40:31

09:40:33

20 A. I believe I have an understanding,
21 particularly with regards to how Dr. Wolfe and
22 others have relied upon it in forming their
23 opinions in the context of this IPR.

09:40:40

09:40:42

09:40:45

09:40:47

24 Q. Okay. You can put most of those
25 exhibits to the side for now and put back your

09:40:49

09:40:56

1	two expert declarations. I'm not sure how you	09:40:59
2	have your screen organized, but to the extent	09:41:02
3	that helps, I'm going to move to a slightly	09:41:04
4	different topic. And just let me know when	09:41:07
5	you're organized and ready to proceed.	09:41:09
6	A. I'm ready when you are. Thank you,	09:41:13
7	though.	09:41:15
8	Q. I'd like to ask you some questions	09:41:19
9	about the hypothetical person of ordinary skill	09:41:20
10	in the art, starting with the relevant time frame	09:41:23
11	for such a person. So that's just sort of	09:41:28
12	background of some of the questions I'm going to	09:41:32
13	be asking you.	09:41:34
14	So do you -- do you have that	09:41:35
15	background in mind?	09:41:37
16	A. Sure.	09:41:39
17	Q. To start, please turn to paragraph 22	09:41:42
18	in both of your expert declarations and let me	09:41:45
19	know when you're there. I believe that	09:41:49
20	paragraph 22 is substantially the same in both	09:41:51
21	expert declarations. And if it's helpful to you,	09:41:56
22	you could look at the red-line that I marked as	09:42:00
23	Exhibit 1076 to see any slight differences.	09:42:03
24	A. I have paragraph 22 of the -- yes --	09:42:09
25	well, I was going to mention, I guess it's the	09:42:14

1 '918 version in front of me on the screen. 09:42:18

2 Q. And if you want, you can pull up 09:42:23

3 paragraph 22 of the other declaration, the '054 09:42:26

4 declaration. I don't think there's any 09:42:28

5 difference that's material, so I'd like to cover 09:42:33

6 both of them at the same time, but I also don't 09:42:37

7 want you to be uncomfortable covering both at the 09:42:40

8 same time, so ... 09:42:47

9 A. Fair enough. I'll go to the red-line 09:42:48

10 version that you provided then. 09:42:50

11 Okay. I have that opened in front of 09:43:04

12 me. And there certainly is nothing relevant that 09:43:05

13 differs between the two of them with regards to 09:43:09

14 this paragraph I see. 09:43:11

15 Q. Now, Samsung's expert, Dr. Wolfe, 09:43:15

16 expressed the opinion in his declarations that 09:43:18

17 the effective filing date for the '918 and '054 09:43:20

18 patents was no earlier than June 2nd, 2008. 09:43:27

19 And my question for you is whether you 09:43:32

20 expressed any opinion disagreeing with Dr. Wolfe 09:43:34

21 on that point. And to be clear, I didn't see any 09:43:40

22 opinion in your expert declarations disagreeing 09:43:44

23 with Dr. Wolfe on this point, but if you do 09:43:47

24 disagree with Dr. Wolfe on this point, please let 09:43:50

25 me know now. 09:43:52

1 ATTORNEY LINDSAY: Objection; form. 09:43:55

2 THE WITNESS: As I sit here today, 09:44:02

3 having not memorized both reports, I will say 09:44:03

4 that I don't recall taking a contrary position to 09:44:06

5 Dr. Wolfe. 09:44:10

6 BY ATTORNEY CHANDLER: 09:44:10

7 Q. And so, in particular, your expert 09:44:11

8 declarations do not express the opinion that the 09:44:15

9 '918 and '054 patents are entitled to an 09:44:19

10 effective filing date of June 1st, 2007; 09:44:22

11 correct? 09:44:27

12 A. So I don't see the date 2007 appearing 09:44:40

13 in the context of a priority date in the red-line 09:44:44

14 document. And so as I sit here, I don't recall 09:44:49

15 taking that position, but I guess it's possible 09:44:55

16 it's in some portion of my declaration that 09:44:57

17 avoided search or that I simply don't recall. 09:45:00

18 But as I sit here today, I don't recall 09:45:02

19 taking such a position. 09:45:05

20 Q. And to be clear, I don't think you did 09:45:07

21 either; and I searched both your declarations for 09:45:09

22 2007 and did not see any reference to any opinion 09:45:11

23 by you that the patents were entitled to an 09:45:18

24 effective filing date any time in 2007, but I 09:45:21

25 just wanted to double-check to make sure that I 09:45:27

1	wasn't missing anything.	09:45:30
2	Understood?	09:45:32
3	A. Yes. And just to be clear, I'm only	09:45:32
4	referring to the context of these documents for	09:45:37
5	the IPR, yeah.	09:45:39
6	Q. In your two expert declarations for	09:45:44
7	these two IPRs, in paragraph 22 you assumed a	09:45:47
8	date of invention in 2008, consistent with	09:45:53
9	Dr. Wolfe; correct?	09:45:57
10	ATTORNEY LINDSAY: Objection; form.	09:45:58
11	THE WITNESS: Well, there you go.	09:46:21
12	There's an error in paragraph 23, although it's	09:46:22
13	just a formatting error on page 12.	09:46:24
14	But setting that aside, yeah, on	09:46:29
15	paragraph 23, I say I've adopted his	09:46:35
16	understanding as to the level of skill in the	09:46:39
17	relevant field at the time of the invention.	09:46:42
18	I generally try to refrain from	09:46:47
19	referring to something as "prior art," just	09:46:50
20	because there's enough odd little legal aspects	09:46:53
21	of what makes something prior art that are not	09:46:57
22	technical. And in matters like this, I try to	09:47:00
23	just review the technical documents and the	09:47:05
24	opinions expressed around them and leave the	09:47:08
25	question of whether they actually are prior art	09:47:11

1 to someone else. 09:47:14

2 BY ATTORNEY CHANDLER: 09:47:16

3 Q. And just for clarity, I wasn't talking 09:47:16

4 about prior art per se. I was talking about the 09:47:20

5 effective filing date of the '918 and '054 09:47:24

6 patents. 09:47:28

7 A. Yes, understood. I was just using that 09:47:28

8 as a place to jump forward, perhaps, or 09:47:30

9 anticipate and to say, you know, if the date 09:47:34

10 was -- was actually 2007, it wouldn't have 09:47:37

11 changed my analysis, because I tend to just look 09:47:41

12 at the art put in front of me and read the 09:47:45

13 arguments made around it. 09:47:51

14 Q. And you referred to some sort of error 09:47:54

15 in paragraph 23. What were you pointing to as 09:47:55

16 the mistake or typo or formatting error? 09:47:58

17 A. So the red-line version that I'm 09:48:02

18 looking at, the -- there's a -- the first 09:48:04

19 sentence at the top of page -- that's labeled 09:48:08

20 page 12 is -- carries over from the previous 09:48:12

21 page. And after -- it says "I express" -- 09:48:18

22 "noting that none of the opinions I express 09:48:21

23 herein," the next line says "would," and then a 09:48:24

24 new line begins. 09:48:28

25 So there's no content difference. It's 09:48:30

1 just a formatting error.

09:48:32

2 Q. Understood. And for clarity,
3 Exhibit 1076 was computer-generated, and so there
4 may be formatting errors through 1076, that is
5 likely not the only one.

09:48:38

09:48:39

09:48:43

09:48:46

6 A. Sure. Understood. Since it's not
7 marked in red or blue, I am willing to assume
8 it's a formatting error in both originals. It
9 may not be, but I don't think it matters
10 substantially to any of us.

09:48:51

09:48:54

09:48:58

09:49:01

09:49:06

11 Q. Correct. I think what it is is simply
12 a page break in the original declaration.

09:49:07

09:49:09

13 A. That makes sense. Thank you.

09:49:14

14 Q. Unless stated otherwise, could you
15 please answer my questions today from the
16 perspective of a person of ordinary skill in the
17 art as of June 2nd, 2008?

09:49:21

09:49:23

09:49:25

09:49:29

18 A. Yes, I will endeavor to do so.

09:49:35

19 Q. And could you also please answer my
20 questions today in a way that is consistent with
21 the ordinary and accustomed meaning of words to a
22 person of ordinary skill in the art as of
23 June 2nd, 2008?

09:49:38

09:49:41

09:49:45

09:49:52

09:49:54

24 A. Yes, I will endeavor to do so.

09:49:58

25 Q. When did you first do any work for

09:50:01

1	Netlist?	09:50:05
2	ATTORNEY LINDSAY: Objection; form.	09:50:10
3	THE WITNESS: That was several years	09:50:11
4	ago in a matter at the ITC. That was the first	09:50:12
5	time I worked for them.	09:50:18
6	BY ATTORNEY CHANDLER:	09:50:23
7	Q. And besides the ITC matter, have there	09:50:27
8	been other matters that you've worked on for	09:50:29
9	Netlist over the past few years?	09:50:32
10	ATTORNEY LINDSAY: Objection; form.	09:50:36
11	THE WITNESS: Yes. My recollection was	09:50:38
12	that there were two different ITC matters; and	09:50:40
13	then there was a district court matter that I did	09:50:45
14	a very small amount of work for subsequent to	09:50:51
15	those two ITC matters. Both -- or all three of	09:50:55
16	these were several years ago.	09:51:01
17	BY ATTORNEY CHANDLER:	09:51:03
18	Q. And in your CV at the end of your	09:51:04
19	expert declarations, if I understand correctly,	09:51:07
20	the ITC matter that you're referring to was in	09:51:10
21	2017; is that correct? The case number	09:51:20
22	337-TA-1023?	09:51:23
23	A. I could go back -- I could flip forward	09:51:29
24	if you want me to exactly verify it, but that	09:51:33
25	sounds right. They were two different ITC	09:51:35

1 matters, and I was working on both of them 09:51:38
2 through Mintz Levin. 09:51:41

3 Q. And if it's helpful, you can just 09:51:45
4 search for 337-TA-1023 in either of your expert 09:51:49
5 declarations, I think you'll find it. 09:51:54
6 Understood? 09:51:56

7 A. Yes. Oddly enough, no. I -- but -- as 09:51:58
8 I said, I -- I'm -- have no problem with 09:52:03
9 accepting that representation there -- okay. 09:52:08

10 Yeah, the red-line version wasn't 09:52:14
11 searchable to find it, but I've got it with -- 09:52:19
12 looking at one of the declarations directly. 09:52:21

13 Q. Before you were first engaged by 09:52:25
14 Netlist around 2017, did you know any of the 09:52:26
15 named inventors on the '918 and '054 patents who 09:52:31
16 are identified as Chi)She Chan -- that's spelled 09:52:36
17 C-H-I dash S-H-E Chan. Second inventor is 09:52:41
18 Jeffrey C. Solomon. Third inventor is Scott H. 09:52:48
19 Milton. And fourth inventor listed is Jayesh 09:52:53
20 Bhakta. J-A-Y-E-S-H, last name B-H-A-K-T-A. 09:52:57

21 A. Not that I recall as I sit here today. 09:53:09
22 It's certainly more than possible that I met them 09:53:12
23 at some place and simply don't recall. 09:53:16

24 Q. And that was my next question: Have 09:53:20
25 you ever met any of the named inventors on the 09:53:21

1 '918 and '054 patents, to your recollection?

09:53:25

2 A. Not that I recall, no.

09:53:28

3 Oh, I'm sorry. I -- I assume you meant
4 prior -- well, I have met Mr. Milton in the
5 context of litigation.

09:53:31

09:53:36

09:53:40

6 Q. Recently?

09:53:44

7 A. Yeah, yeah.

09:53:45

8 Q. All right. But before that, you don't
9 recall ever meeting him; is that fair?

09:53:46

09:53:48

10 A. Yes, that's fair.

09:53:52

11 Q. When do you believe was the first time
12 that you had heard of the named inventors of the
13 '918 and '054 patents?

09:53:56

09:53:57

09:54:02

14 A. The first time that I can recall
15 hearing of the named inventors is when the
16 patents were presented to me, or for my review.

09:54:09

09:54:10

09:54:13

17 Q. So within the last year, approximately;
18 is that fair?

09:54:24

09:54:26

19 A. Yes, like within the last year.

09:54:33

20 Q. In Exhibit 2031, your declaration in
21 the '918 patent, you had mentioned you thought
22 there was a typo. And I'm wondering if it's on
23 page 63 in paragraph 103. Last sentence,
24 where -- as written it says "A POSITA, would not
25 have used an LDO, not a buck converter."

09:54:42

09:54:45

09:54:56

09:55:04

09:55:15

09:55:21

41

1	A. You said that was paragraph 103?	09:55:27
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2	Q. Correct.	09:55:31
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3	A. Okay.	09:55:32
---	----------	----------

4	Q. Exhibit 1031 in IPR - .	09:55:33
---	----------------------------	----------

5	And there may not be a corresponding	09:56:00
---	--------------------------------------	----------

6 paragraph in the other declaration. 09:56:03

7	A. I think that's right. Certainly	09:56:05
---	------------------------------------	----------

8 immediately on the face of it, where the 09:56:09

9	structure is, well, he's got two options and a	09:56:11
---	--	----------

10	POSITA would not have used either of them.	09:56:14
----	--	----------

11	So yes, that is, I believe, the spot	09:56:16
----	--------------------------------------	----------

12	that I'm recalling.	09:56:20
----	---------------------	----------

13	Q. For clarity, you believe that the last	09:56:22
----	---	----------

14	sentence of paragraph 103 of Exhibit 2031 in	09:56:26
----	--	----------

15	IPR2022-00996 should read, "Thus, a POSITA would	09:56:32
----	--	----------

16	have used an LDO, not a buck converter"?	09:56:41
----	--	----------

17	A. Yes.	09:56:49
----	---------	----------

18	Q. And it goes on.	09:56:50
----	--------------------	----------

19	A. That's correct. And what's probably	09:56:51
----	--	----------

20	apparent to the court reporter, LDO is all	09:56:56
----	--	----------

21	uppercase and stands for "linear dropout."	09:56:59
----	--	----------

22	Q. Could you please turn to paragraph 10	09:57:09
----	--	----------

23	in your two expert declarations, which I believe	09:57:11
----	--	----------

24	is substantially the same in both. And let me	09:57:15
----	---	----------

25	know when you're there.	09:57:19
----	-------------------------	----------

1 A. All right. I'm there. 09:57:24

2 Q. Netlist retained another expert named 09:57:27

3 Dr. Khatri for these two IPRs, spelled 09:57:30

4 K-H-A-T-R-I; correct? 09:57:34

5 A. Yes, that is my understanding. 09:57:39

6 Q. And Dr. Khatri submitted expert 09:57:43

7 declarations on behalf of Netlist in these two 09:57:47

8 IPRs; correct? 09:57:50

9 A. Yeah, that is my understanding. 09:57:51

10 Q. Do you have any disagreements with any 09:57:55

11 of Dr. Khatri's opinions in these two IPRs? 09:57:57

12 A. Likely. I don't have a list of them, 09:58:07

13 though, as I sit here. 09:58:09

14 Q. And why do you say "likely"? 09:58:14

15 A. Because in my experience -- these are 09:58:17

16 detailed, complex, technical concepts, and in my 09:58:22

17 experience, experts tend to not agree completely, 09:58:29

18 even though on the same side. 09:58:34

19 So I don't have anything in particular 09:58:39

20 to point to, but I wasn't looking for places in 09:58:40

21 any of his -- any of the materials that he 09:58:45

22 sourced for points of disagreement. 09:58:49

23 Q. But as stated in paragraph 10 of your 09:58:53

24 two expert declarations, you did review 09:58:56

25 Dr. Khatri's declarations; correct? 09:59:00

1 A. Yes. 09:59:03

2 Q. And there were at least portions of 09:59:07
3 Dr. Khatri's declaration that you adopted and, I 09:59:12
4 assume, agreed with; correct? 09:59:14

5 A. Yes. At the second sentence of 09:59:17
6 paragraph 10, I say, "Because of significant 09:59:22
7 overlap with points that I make throughout my 09:59:24
8 report, in some instances I have adopted his 09:59:26
9 positions as my own." 09:59:30

10 But that was only after doing my own 09:59:31
11 review and forming my own opinions. 09:59:36

12 Q. And my question is: When you reviewed 09:59:40
13 the declaration submitted by Dr. Khatri, were 09:59:42
14 there any opinions expressed by him that you 09:59:47
15 disagreed with? 09:59:50

16 ATTORNEY LINDSAY: Objection; asked and 09:59:51
17 answered. 09:59:51

18 THE WITNESS: Yeah, I think that was 09:59:54
19 the same question you asked a moment ago. And I 09:59:55
20 would say likely, but nothing that I can identify 09:59:58
21 as I sit here. Nothing that I recall thinking, 10:00:01
22 Oh, this is -- this is an important point where 10:00:10
23 we disagree. 10:00:12

24 I'm just saying "likely" because I 10:00:13
25 expressed a lot of opinions, as did he. There's 10:00:16

1 probably something where I would disagree with
2 him.

3 BY ATTORNEY CHANDLER:

4 Q. Do you know, Dr. Khatri?

5 A. I don't believe so. Much like the
6 inventors on the -- on the patents at hand, I
7 guess, I would be willing to say I may have run
8 across him in the past. I have no particular
9 recollection of him individually.

10 Q. Are you willing to vouch for Dr. Khatri
11 as an expert?

12 ATTORNEY LINDSAY: Objection; form.

13 THE WITNESS: No. I have no particular
14 opinions regarding his qualifications one way or
15 another. I'm sure when I reviewed his
16 declaration, out of some interest, I looked
17 further into his background; but I don't recall
18 forming any opinions on that one way or another.
19 He could be a perfectly fine, highly qualified
20 individual or not. I don't have an opinion.

21 BY ATTORNEY CHANDLER:

22 Q. And to be clear, you don't have an
23 opinion on whether all of Dr. Khatri's opinions
24 are correct; is that fair?

25 A. I don't think I've taken a position on

1 whether all of the opinions that he had 10:01:52
2 previously expressed in the context of these IPRs 10:01:54
3 are correct. 10:01:58

4 Q. Could you go to paragraph 22 in your 10:02:07
5 two expert declarations and let me know when 10:02:09
6 you're there? 10:02:11

7 A. Okay, I'm there. 10:02:16

8 Q. And then below paragraph 22 in 10:02:17
9 paragraph 23, of your two expert declarations, to 10:02:19
10 be clear, you do not dispute Dr. Wolfe's 10:02:25
11 definition of a person of ordinary skill in the 10:02:29
12 art as of 2008; correct? 10:02:31

13 (Exhibit Number 1003 was previously
14 marked for identification.)

15 BY ATTORNEY CHANDLER: 10:02:39

16 Q. And I'm referring to the paragraphs in 10:02:39
17 Dr. Wolfe's declarations that you cited in 10:02:43
18 paragraph 22, which are Exhibit 1003, 10:02:46
19 paragraph 67 for IPR 2022-00996, involving the 10:02:50
20 '918 patent; and Exhibit 1003, paragraph 61, for 10:02:56
21 IPR2022-00999 involving the '054 patent. 10:03:02

22 A. I don't recall disagreeing with 10:03:13
23 Dr. Wolfe regarding what a person of ordinary 10:03:18
24 skill in the art would be for either of these two 10:03:23
25 patents. In my experience, while we have 10:03:26

1 disagreed quite a bit on a number technical
2 questions, complex technical matters, Dr. Wolfe
3 is a thorough professional.

4 (Exhibit Number 2016 was previously
5 marked for identification.)

6 BY ATTORNEY CHANDLER:

7 Q. Could you turn to Exhibit 2016 and let
8 me know when you have it. And I believe it's the
9 same in both IPRs. And, you know, maybe for the
10 benefit of the court reporter, I'll put it in the
11 chat so she can follow along.

12 A. Yes, I have it opened in front of me.

13 Q. Are you familiar with Exhibit 2016?

14 A. I have a familiarity with it, yes.

15 Q. Please turn to page 3 of Exhibit 2016,
16 and let me know when you're there.

17 A. All right. I'm there with you.

18 Q. Page 3 of Exhibit 2016 in both IPRs
19 describes different variations of the PCI bus
20 specification; correct?

21 A. Yes. It refers to Conventional PCI,
22 PCI-X, and PCI Express.

23 Q. And these those variations of the PCI
24 bus specification, labeled Conventional PCI,
25 PCI-X, and PCI Express those existed and were

1 known before the '918 and '054 patents were filed 10:05:36
2 in 2008; correct? 10:05:39

3 A. Yeah, I believe so. Particularly with 10:05:43
4 regards to PCI Express, as this document states, 10:05:50
5 its available -- availability "is expected in 10:05:55
6 2004." I don't recall exactly when it became 10:06:01
7 available. 10:06:05

8 However, at least at the time of this 10:06:05
9 document, there was certainly an understanding of 10:06:08
10 what PCI Express was, predating the -- the 2008 10:06:11
11 date. 10:06:16

12 Q. And Exhibit 2016 is from the year 2006; 10:06:18
13 correct? 10:06:23

14 A. I would be surprised, I guess. Let me 10:06:29
15 see. 10:06:31

16 Where is the -- can you point me to a 10:06:36
17 date for this? 10:06:38

18 Q. Sure. Last page on the left, 10:06:39
19 December 2006. 10:06:44

20 A. It does say 2006. I don't know why it 10:06:49
21 would say "PCI Express is expected in 2004" in a 10:06:51
22 document that was written two years later. But I 10:06:57
23 do see that it says 2006. 10:07:00

24 Q. But to be clear, a Conventional PCI, 10:07:04
25 that was known well before 2008; correct? 10:07:08

1 A. Yes. 10:07:14

2 Q. And PCI-X was also well known before 10:07:15

3 2008; correct? 10:07:26

4 A. Yes, I believe that's the case. 10:07:29

5 Q. And at least the initial Version 1.0 of 10:07:31

6 PCI Express released back in 2002, that would 10:07:36

7 have also predated the '918 and '054 patents 10:07:44

8 filed in 2008; correct? 10:07:49

9 A. That -- that date that they reference 10:07:51

10 PCI Express Revision 1.0 in 2002 certainly does 10:07:56

11 predate 2008. 10:08:05

12 Q. And the Conventional PCI specification 10:08:06

13 was revised with Revision 2.2 and 2.3 and 3.0, 10:08:10

14 and all of those revisions were well before 2008; 10:08:21

15 correct? 10:08:28

16 A. This document shows some of those 10:08:32

17 dates, not all of them. But given that the 10:08:34

18 document was either written prior to 2004, based 10:08:37

19 on my comment -- or what it says regarding PCI 10:08:40

20 Express, or in 2006, as we saw the last page, I 10:08:45

21 would agree with you, those would have to have 10:08:52

22 been available prior to 2008. 10:08:56

23 (Exhibit Number 2029 was previously

24 marked for identification.)

25

1 BY ATTORNEY CHANDLER:

10:09:01

2 Q. Could you turn to Exhibit 2029, which
3 is the same in both IPRs. Let me know when
4 you're there. And I'll also put it in the chat
5 for everyone's convenience.

10:09:01

10:09:04

10:09:11

10:09:13

6 A. Okay. Would now be a good time to take
7 a break if you're changing documents? Or if you
8 would prefer to finish up questioning along the
9 lines of PCI for a few minutes, I'm certainly
10 fine with that wall.

10:09:22

10:09:25

10:09:28

10:09:31

10:09:35

11 Q. Yeah, let's do that and then we'll take
12 a break.

10:09:38

10:09:41

13 A. Okay.

10:09:41

14 Q. Do you have Exhibit 2029 in front of
15 you?

10:09:42

10:09:44

16 A. Yes, I do.

10:09:44

17 Q. And do you recognize Exhibit 2029?

10:09:46

18 A. Yes, I believe so.

10:09:50

19 Q. Exhibit 2029, in both IPRs, is a PCI
20 Technology Overview dated February 2003; correct?

10:09:53

10:09:57

21 A. Yes, sir, it is.

10:10:04

22 Q. And turn to page 5 of Exhibit 2029.
23 Let me know when you're there.

10:10:06

10:10:10

24 A. I am there.

10:10:12

25 Q. And so page 5 of Exhibit 2029 also

10:10:14

1 provides some dates concerning Conventional PCI,
2 PCI-X and PCI Express; correct?

3 A. Yes, sir, I see that.

4 Q. So Conventional PCI Version 1.0 was
5 proposed in 1991; and then we got a Version 2.0
6 in 1993, a Version 2.1 in 1995, and a Version 2.3
7 in 2002; correct?

8 A. Yes, sir, that's what the document
9 says.

10 Q. And PCI-X Version 1.0 was approved in
11 1999, and Version 2.0 was approved in 2002;
12 correct?

13 A. Yes, sir, that's what the document
14 states.

15 Q. And PCI Express Version 1.0 was
16 approved in 2002; correct?

17 A. Yes, sir, the document states that.

18 Q. And are the statements in the document
19 consistent with your understanding of the time
20 frame of Conventional PCI, PCI-X and PCI Express?

21 A. I would say they're not inconsistent.
22 I don't have any particular recollection of the
23 various revisions.

24 Q. But you don't have any reason to
25 disagree with the dates shown on page 5 of

1 Exhibit 2029; is that fair?

10:11:48

2 A. That's fair. I don't have any
3 particular position to say they're accurate or
4 inaccurate. It's not -- the dates are not
5 inconsistent with what I would expect.

10:11:50

10:11:52

10:11:55

10:11:58

6 Q. And this is a document that you cited;
7 correct?

10:12:01

10:12:05

8 A. I believe so, yeah.

10:12:06

9 Q. And you relied upon it; right?

10:12:09

10 A. I'd have to go back and see where I
11 reference, but that's likely the case, yeah.

10:12:11

10:12:13

12 Q. Turn to page 6 of Exhibit 2029.

10:12:19

13 A. I'm there.

10:12:24

14 Q. This page 6 of 2029 discusses some of
15 the functionality of Conventional PCI; is that
16 fair?

10:12:27

10:12:33

10:12:39

17 A. Yes, sir.

10:12:40

18 Q. And it looks like somebody highlighted,
19 on page 6 of Exhibit 2029, that Conventional PCI
20 has a throughput of 532 megabytes per second;
21 correct?

10:12:41

10:12:44

10:12:49

10:12:57

22 A. Yes, for a 64-bit PCI 2.1 slot.

10:13:01

23 Q. And does that sound accurate to you,
24 that Conventional PCI had a throughput of 532
25 megabytes per second for the 64-bit slot?

10:13:06

10:13:10

10:13:18

1 A. Sure, yes. 10:13:23

2 Q. Turn to page 8 of Exhibit 2029. Let me 10:13:25

3 know when you're there. 10:13:31

4 A. I'm there. 10:13:32

5 Q. And page 8 provides a description of 10:13:33

6 PCI-X Version 1.0; correct? 10:13:41

7 A. Yes, sir, that's correct. 10:13:46

8 Q. And PCI-X is based on the existing PCI 10:13:51

9 architecture; correct? 10:14:03

10 A. That is what the document states. 10:14:06

11 Q. It's fully backwards-compatible; 10:14:09

12 correct? 10:14:13

13 ATTORNEY LINDSAY: Objection; form. 10:14:14

14 BY ATTORNEY CHANDLER: 10:14:15

15 Q. PCI-X is fully backwards-compatible 10:14:20

16 with Conventional PCI slots; correct? 10:14:26

17 ATTORNEY LINDSAY: Objection; form. 10:14:29

18 THE WITNESS: That is what the document 10:14:33

19 states. I'm only a little unsure, because it 10:14:35

20 also states that there's no support for a 10:14:39

21 5-volt-only board, which would suggest to me that 10:14:43

22 it's at least not backwardly compatible for those 10:14:48

23 boards. 10:14:53

24 But other than that, it does say that 10:14:53

25 it's fully backwards compatible, yeah. 10:14:56

1 BY ATTORNEY CHANDLER:

10:14:58

2 Q. And if you look back on page 6 of
3 Exhibit 2029, the Conventional PCI could operate
4 at 3.3 volts or 5 volts; correct?

10:14:59

10:15:02

10:15:07

5 A. I'm not sure. Are you referring to the
6 reference at the bottom with regards to PCI 2.3?

10:15:25

10:15:28

7 Q. PCI -- PCI 2.1 supported both 3.3 volts
8 and 5 volts; correct?

10:15:33

10:15:43

9 A. Yes, that's what it says. Yeah.

10:15:45

10 Q. And then the later version of the
11 Conventional PCI, Version 2.3, only supported a
12 3.3-volt power supply; correct?

10:15:48

10:15:51

10:16:00

13 A. Well, it says it doesn't support
14 5-volt-only adapters, which may mean that the
15 adapters have to be 5 and 3.3, or 3.3.

10:16:06

10:16:08

10:16:13

16 But the combination of the comment
17 on -- regarding there being 5-volt boards, in the
18 context of 2.1, suggests to me that PCI-X is not
19 fully compatible because there were 5-volt-only
20 boards, and yet they're saying they don't support
21 5-volt only boards.

10:16:19

10:16:23

10:16:28

10:16:35

10:16:40

10:16:42

22 But I don't know of any other place
23 where it would appear that they are not fully
24 backwards compatible.

10:16:44

10:16:46

10:16:50

25 Q. Page 8 of Exhibit 2021 [sic] teaches

10:16:52

1 that PCI-X was backwards compatible with the 10:16:55
2 slots for Conventional PCI boards; correct? 10:17:01
3 A. For many of them. But, again, it says 10:17:19
4 that there's no support for the 5-volt-only board 10:17:22
5 slots, boards that would go in those slots. 10:17:26
6 Q. PCI-X uses 3.3 volts; correct? 10:17:33
7 A. Yes, PCI-X 1.0 uses 3.3 volts. 10:17:45
8 Q. And PCI-X 1.0 had two speed grades, 10:17:50
9 66 megahertz and 133 megahertz; correct? 10:17:57
10 A. Yeah, it -- well, it says that it 10:18:02
11 provides two speed grades, 66 megahertz and 133. 10:18:20
12 But in the bullet point above that, it also says 10:18:27
13 that it supports conventional 33-megahertz PCI 10:18:32
14 adapters. 10:18:36
15 Q. Right. So it's backwards-compatible 10:18:45
16 with slower adapters; but it also can operate at 10:18:47
17 the higher speed if the computer supports that; 10:18:51
18 is that fair? 10:18:57
19 A. Yeah, that's my understanding. I was 10:18:58
20 just pointing out that it's not limited to just 10:18:59
21 those speeds, but it does indicate that it 10:19:02
22 supports those speeds of 66 megahertz and 10:19:05
23 133 megahertz. 10:19:07
24 Q. And a PCI-X was targeted at high-end 10:19:23
25 data networking and storage network applications; 10:19:29

1 correct? 10:19:32

2 A. That's what the bullet point at the 10:19:36
3 bottom of page 8 says. That would be consistent 10:19:37
4 with my recollection at the time. I just -- I 10:19:43
5 don't know that the PCI standards body officially 10:19:46
6 took that position. But that is consistent with 10:19:51
7 my understanding of what they were trying to 10:19:55
8 achieve. 10:19:57

9 Q. And what were you doing at the time 10:19:59
10 back then? 10:20:01

11 A. In -- so this was 2003. 2003, I was 10:20:02
12 teaching electrical engineering at UCLA. 10:20:08

13 Q. And did you ever use PCI cards back 10:20:12
14 then? 10:20:19

15 A. Yes. PCI cards were very widely used 10:20:21
16 at the time. 10:20:25

17 I don't recall making use of PCI-X, you 10:20:27
18 know. But in many situations, we would just 10:20:31
19 generate specifications for a computer needed in 10:20:37
20 the lab, and it would come as specified. May 10:20:40
21 have had a PCI-X board, but I don't recall. 10:20:44

22 Q. And you indicated that the statement at 10:20:47
23 the bottom of page 8 of Exhibit 2029, that PCI-X 10:20:50
24 was "Targeted at high-end data networking and 10:20:54
25 storage network applications" was consistent with 10:21:02

1 your recollection back in 2003.

10:21:05

2 What are you referring to with respect
3 to your recollection in 2003?

10:21:06

10:21:07

4 A. My understanding of what PCI-X was
5 developed to support.

10:21:12

10:21:18

6 Q. Can you explain that a little more.
7 I'm just a little unclear what you're referring
8 to.

10:21:23

10:21:25

10:21:28

9 A. Yeah. My recollection was that PCI-X
10 was developed to support, higher-end,
11 higher-speed-requirement transfers than typically
12 found in the industry at the time, in general;
13 and, in particular, typically identified as
14 required for servicing the, I would say, consumer
15 market.

10:21:28

10:21:32

10:21:39

10:21:46

10:21:48

10:21:52

10:21:59

16 Q. So if I understand what you're saying,
17 your recollection is that a PCI-X was targeted at
18 higher-end applications, not for consumers? Is
19 that what you're saying? Like, something faster
20 than what a consumer would need?

10:22:04

10:22:06

10:22:13

10:22:20

10:22:26

21 ATTORNEY LINDSAY: Objection; misstates
22 prior testimony.

10:22:28

10:22:30

23 BY ATTORNEY CHANDLER:

10:22:32

24 Q. I'm just trying to understand what you
25 said.

10:22:32

10:22:34

1 A. Yeah, at least at that time. 10:22:34

2 However, you know, what technology that 10:22:37

3 often is -- oftentimes, technology that's 10:22:40

4 developed for higher -- what's considered a 10:22:43

5 higher-performance situation at the time of 10:22:47

6 development migrates down into the consumer 10:22:50

7 market. And we've seen that time and time again. 10:22:55

8 But, yeah, my recollection is, at the 10:22:59

9 time when PCI-X was introduced, they were talking 10:23:03

10 about it generally being a higher-cost, 10:23:06

11 higher-performance set of technologies to service 10:23:11

12 more, I guess I would say, server-oriented 10:23:15

13 contexts. 10:23:25

14 Q. And what are examples you recall of 10:23:26

15 high-end data networking or storage network 10:23:30

16 applications? 10:23:36

17 A. So a storage network application would 10:23:37

18 be something where there was like a hard disk 10:23:39

19 that I was accessing fairly regularly that was 10:23:46

20 not physically attached to my -- directly 10:23:55

21 attached to my computer but was somewhere else on 10:23:57

22 the network. In which case, the higher 10:24:00

23 throughput of PCI-X likely would have been 10:24:06

24 attractive. 10:24:09

25 Q. Could you turn to page 9 of 10:24:11

1	Exhibit 2029. Let me know when.	10:24:14
2	A. All right, I'm there.	10:24:18
3	Q. So there was a second version of PCI-X	10:24:21
4	referred to as PCI-X 2.0; correct?	10:24:25
5	A. Yes, that's correct.	10:24:34
6	Q. And it was still intended to be	10:24:35
7	backwards-compatible; is that fair?	10:24:39
8	A. Yes, I see that.	10:24:42
9	Q. And PCI-X 2.0 provided two additional	10:24:44
10	speeds grades -- 266 megahertz for a throughput	10:24:50
11	of 2.13 gigabytes per second, and 533 megahertz	10:24:56
12	for a throughput of 4.26 gigabytes per second --	10:25:03
13	correct?	10:25:07
14	A. Yes. I see that.	10:25:08
15	Q. And the bottom of page 9 of	10:25:11
16	Exhibit 2029 indicates that that bandwidth would	10:25:15
17	be "sufficient to support new breed of cutting	10:25:18
18	edge technologies," such as 10-gigabyte Ethernet	10:25:21
19	and some other technologies; correct?	10:25:26
20	A. Yes, I see that.	10:25:31
21	Q. And then page 10 of Exhibit 2029 graphs	10:25:33
22	the throughput in gigabytes-per-second for	10:25:41
23	different versions of Conventional PCI and PCI-X	10:25:52
24	in purple; correct?	10:26:01
25	A. Yes, that's correct.	10:26:07

1 Q. And then in green and yellow on page 10
2 of Exhibit 2029 there's graphed the throughput of
3 some other technologies, including Ethernet and a
4 few other things; correct?

5 A. Yes, that's correct.

6 Q. And, for example, what's the technology
7 shown in green on page 10 of Exhibit 2029?

8 A. So that's labeled U160 and then the
9 acronym, in uppercase, SCSCI, which is typically
10 pronounced "scuzzy." And that is generally what
11 was considered a interface technology for storage
12 devices.

13 Q. And I gather the point of the graph on
14 page 10 of Exhibit 2029 is that there are
15 versions of PCI and PCI-X that have a throughput
16 in gigabytes per second greater than Ethernet and
17 SCSCI and something called InfiniBand; is that
18 fair?

19 A. Yes. I think the purpose of this graph
20 is to show that PCI-X could be used in systems
21 that use any of those technologies without
22 necessarily being a bottleneck and the limiting
23 factor in system performance.

24 Q. Go to page 14. This talks about the
25 future of PCI-X. Let me know when you're there.

1	A. I'm there.	10:28:15
2	Q. So page 14 of Exhibit 2029 indicates,	10:28:20
3	as of February 2003, that there was the	10:28:24
4	expectation that there would be a Version 3.0 of	10:28:29
5	the PCI-X specification; correct?	10:28:31
6	A. Yes, that's correct.	10:28:38
7	Q. And that PCI-X 3.0 was in development	10:28:42
8	and intended to provide 1066-megahertz data rate	10:28:45
9	with 8.5 gigabytes-per-second bandwidth; is that	10:28:54
10	fair?	10:28:59
11	A. Yes, I see that statement on this page.	10:29:00
12	Q. And then if you turn to page 16 of	10:29:06
13	Exhibit 2029, that page refers to the third	10:29:08
14	variation that we discussed earlier referred to	10:29:13
15	as PCI Express; correct?	10:29:20
16	A. Yes, sir, I see that.	10:29:25
17	Q. And so PCI Express is described as	10:29:30
18	essentially a serialized, packetized version of	10:29:34
19	PCI; correct?	10:29:39
20	A. Yes, sir, I see that.	10:29:43
21	Q. And how would you explain to a	10:29:43
22	layperson what a serialized, packetized version	10:29:46
23	of PCI is?	10:29:49
24	A. Well, what it's -- it's serialized in	10:29:55
25	the sense that some of the control signals	10:29:57

1 that -- some of the information carried over 10:30:02
2 varies -- 10:30:11

3 I have to ask, is that noise in the 10:30:11
4 background apparent to anybody? If it is, I 10:30:14
5 could close my window. 10:30:16

6 Q. I thought you were talking about the 10:30:19
7 noise outside my window. But I guess there's 10:30:21
8 noise outside your window too? 10:30:24

9 A. There is. Actually, give me just a 10:30:26
10 second. I'm going to close it for my own 10:30:27
11 satisfaction. 10:30:30

12 Q. All right. I was just reading about 10:30:30
13 how noise outside windows could lead to early 10:30:34
14 heart attacks. 10:30:38

15 A. All right. So it's -- 10:30:40

16 Q. So to be clear, the question was: How 10:30:41
17 would you explain to a layperson what a 10:30:43
18 serialized, packetized version of PCI is? Which 10:30:45
19 is how page 16 of Exhibit 2029 refers to PCI 10:30:49
20 Express. 10:30:54

21 A. Yeah, so the original PCI had a set of 10:30:56
22 signal pins on an edge connector, and one of the 10:31:02
23 things that -- each of which carried a specific 10:31:07
24 type of information. 10:31:14

25 One of the things that PCI Express 10:31:15

1 changed from that was to take the information on 10:31:18
2 those various signal pins and send them over a 10:31:23
3 new set of signal pins that -- a reduced set of 10:31:28
4 signal pins, in what we call a serialized manner. 10:31:31

5 So, for example, if there were 16 bits 10:31:36
6 of -- 16 physical control signal pins on the 10:31:40
7 original PCI -- and I don't recall exactly how 10:31:46
8 many signals there were -- but you could take the 10:31:48
9 information that was conventionally sent over 10:31:52
10 those 16 signal wires and send them over one 10:31:56
11 signal wire using 16 different clock cycles, 10:32:01
12 setting them one after the another. So, in 10:32:05
13 essence, you could require fewer signal wires, 10:32:10
14 signal pins. 10:32:13

15 Q. Or if I understand correctly what 10:32:18
16 page 16 of Exhibit 2029 is describing, in the 10:32:20
17 alternative, you could essentially get a higher 10:32:22
18 throughput by using more lanes, is the term that 10:32:27
19 it uses? Is that fair? 10:32:34

20 ATTORNEY LINDSAY: Objection; form. 10:32:36

21 THE WITNESS: Sure. So that's -- in 10:32:40
22 the -- in the simplest form, you would take those 10:32:41
23 16 signals and send the data that was 10:32:47
24 communicated over them over a single signal wire, 10:32:52
25 signal pin; but you could also -- and it would 10:32:56

1 take 16 clock cycles.

10:33:00

2 You could also choose to use two signal
3 wires, in which case it would only take eight; or
4 four, in which case, it would only take four
5 clock cycles.

10:33:03

10:33:05

10:33:09

10:33:14

6 And the question of going from one to
7 two -- I don't think anybody did three. But one
8 to two to four is generally referred to as
9 changing the number of lanes in use.

10:33:15

10:33:17

10:33:20

10:33:23

10 BY ATTORNEY CHANDLER:

10:33:26

11 Q. And was this something that you
12 personally worked with back in the early 2000s as
13 part of your work as a professor?

10:33:26

10:33:29

10:33:33

14 A. Sure, I did have some familiarity with
15 that. But the general concept of using
16 serialized packet communication was -- that's
17 very widely known. That's how the internet
18 operates, for example.

10:33:38

10:33:41

10:33:48

10:33:52

10:33:55

19 Its application to PCI Express I was
20 familiar with at the time of 2003. I began
21 working with it, that particular aspect, very
22 closely probably in late 2005.

10:33:56

10:34:01

10:34:06

10:34:11

23 Q. Okay. Are you done -- are you done
24 with that answer?

10:34:20

10:34:23

25 A. Yes.

10:34:24

1 ATTORNEY CHANDLER: Why don't we take a 10:34:25
2 break. 10:34:26
3 THE WITNESS: All right. 10:34:28
4 ATTORNEY CHANDLER: Go off the record? 10:34:29
5 ATTORNEY LINDSAY: Certainly. 10:34:32
6 THE VIDEOGRAPHER: Off the record at 10:34:33
7 10:34 a.m. Pacific Time. 10:34:34
8 (Recess taken from 10:34 a.m. to
9 10:47 a.m.)
10 THE VIDEOGRAPHER: On the record at 10:47:25
11 10:47 a.m. Pacific Time. 10:47:26
12 BY ATTORNEY CHANDLER: 10:47:29
13 Q. And Dr. Mangione-Smith, just to 10:47:31
14 confirm, during the break, you did not talk with 10:47:34
15 your counsel or anyone else about the substance 10:47:37
16 of your testimony; correct? 10:47:38
17 A. That's correct, I did not. 10:47:42
18 Q. And are there any corrections or 10:47:44
19 clarifications you'd like to make to any of your 10:47:46
20 testimony earlier today? 10:47:50
21 A. No, there are not. 10:47:56
22 Q. Now, Dr. Mangione-Smith, you and 10:47:57
23 Dr. Wolfe and Dr. Khatri all cited to various 10:48:06
24 JEDEC standards; correct? 10:48:10
25 A. Yes, sir. 10:48:16

1 Q. And you do not disagree with 10:48:16
2 Dr. Wolfe's opinion that a person of ordinary 10:48:23
3 skill in the art would have known about JEDEC 10:48:25
4 standards applicable to memory modules; is that 10:48:28
5 correct? 10:48:30

6 A. Yes. It's -- it's a deeper question to 10:48:34
7 think about which standards they would be 10:48:37
8 familiar with; but they would certainly be 10:48:39
9 familiar with JEDEC in the large. 10:48:42

10 Q. And so if you can pull up Exhibit 1026. 10:48:46
11 Let me know when you have it. 10:48:56

12 A. All right. I have it in front of me. 10:49:07

13 Q. You do not dispute that a person of 10:49:09
14 ordinary skill in the art would have known about 10:49:11
15 Exhibit 1026, the JEDEC standard for DDR2 SDRAM 10:49:15
16 memory devices labeled JESD79-2B, dated 10:49:25
17 January 2005; correct? 10:49:32

18 A. I don't have an opinion on that one way 10:49:39
19 or the other. So yes, I guess to that extent, I 10:49:42
20 don't disagree with that. I'm not sure I agree 10:49:45
21 with that position either. 10:49:48

22 Q. But to be clear, you're not disputing 10:49:50
23 Dr. Wolfe's position on that; right? 10:49:52

24 A. Yes, that's -- I believe that to be 10:49:54
25 accurate. 10:49:58

1 Q. Look at Exhibit 1027. Let me know when 10:49:59
2 you have it. And it's the same in both IPRs. 10:50:04

3 A. Yes, I have it. 10:50:09

4 Q. You do not dispute that a person of 10:50:10
5 ordinary skill in the art would have known by 10:50:11
6 Exhibit 1027, the JEDEC standard JESD82-20 for 10:50:13
7 FBDIMM advanced memory buffer, dated March 2007; 10:50:22
8 correct? 10:50:28

9 A. I have no position one way or another 10:50:30
10 regarding whether they would have -- a person of 10:50:33
11 ordinary skill in the art would have been 10:50:36
12 familiar with this. They certainly -- such a 10:50:37
13 person certainly would have been familiar with 10:50:41
14 JEDEC in general, and this material would have 10:50:43
15 been available to them. 10:50:46

16 So I'm not disputing his position that 10:50:47
17 it would have -- that this particular document 10:50:50
18 would have been known. I'm just not sure I agree 10:50:51
19 with it. 10:50:55

20 Q. I'm a little unclear about the last 10:51:02
21 part of your answer when you say I'm just not 10:51:04
22 sure I agree with "it." What is the "it"? 10:51:08

23 A. Thank you. As I finished that, I 10:51:13
24 realized it was unclear. 10:51:15

25 I'm not sure I agree with his opinion 10:51:16

1 that a person of ordinary skill in the art would 10:51:20
2 have been familiar with this particular document. 10:51:22
3 I'm not disputing it or accepting it one way or 10:51:29
4 another. 10:51:31

5 Q. But it would have been available to a 10:51:33
6 person of ordinary skill in the art; is that 10:51:37
7 fair? 10:51:37

8 ATTORNEY LINDSAY: Objection; form. 10:51:39

9 THE WITNESS: Yeah -- yes, that is my 10:51:43
10 understanding. 10:51:44

11 BY ATTORNEY CHANDLER: 10:51:47

12 Q. And to be clear, when you and I use the 10:51:48
13 phrase "person of ordinary skill in the art," 10:51:51
14 we're not referring to any actual human being; 10:51:54
15 this is a hypothetical person of ordinary skill 10:51:57
16 in the art; correct? 10:52:00

17 A. Yes, that's correct. 10:52:05

18 Q. And you understand that the 10:52:08
19 hypothetical person of ordinary skill in the art 10:52:09
20 is assumed to know about all of the prior art in 10:52:11
21 the relevant field of art, as of the date of the 10:52:17
22 invention; is that fair? 10:52:21

23 ATTORNEY LINDSAY: Objection; calls for 10:52:24
24 a legal conclusion. 10:52:24

25 THE WITNESS: Yeah, I don't know if the 10:52:28

1 standards are written precisely that way, but 10:52:30
2 that sounds roughly like it matches my 10:52:33
3 understanding, sure. 10:52:35

4 BY ATTORNEY CHANDLER: 10:52:38

5 Q. Right. And so with that understanding, 10:52:38
6 you do not dispute that a hypothetical person of 10:52:42
7 ordinary skill in the art would have known about 10:52:45
8 Exhibit 1026, the JESD79-2B standards, and 10:52:53
9 Exhibit 1027, the JESD82-20 standard; correct? 10:53:00

10 ATTORNEY LINDSAY: Objection; calls for 10:53:07
11 a legal conclusion, form. 10:53:07

12 THE WITNESS: Yeah, I think that's -- 10:53:11
13 when we discussed this just a few minutes ago, I 10:53:13
14 don't recall disagreeing or disagreeing with 10:53:17
15 Dr. Wolfe's statement there. As I sit here 10:53:23
16 today, I'm not of the opinion that, Oh, a POSITA 10:53:26
17 would not have been familiar with this or that 10:53:31
18 particularly they would have. 10:53:34

19 BY ATTORNEY CHANDLER: 10:53:41

20 Q. Look at Exhibit 1028. Let me know when 10:53:41
21 you have it in front of you. It's the same in 10:53:44
22 both IPRs. 10:53:47

23 A. Yes, I see it. 10:53:53

24 Q. Do you dispute that a hypothetical 10:53:53
25 person of ordinary skill in the art would have 10:53:57

1 known about Exhibit 1028, the JEDEC standard 10:53:58
2 JESD205, dated March 2007, for DDR2 SDRAM fully 10:54:02
3 buffered DIMM; correct? 10:54:15

4 ATTORNEY LINDSAY: Objection; calls for 10:54:16
5 a legal conclusion and form. 10:54:16

6 THE WITNESS: I don't recall taking a 10:54:21
7 position disagreeing with that, with the notion 10:54:23
8 that a person of ordinary skill in the art would 10:54:27
9 have been familiar with this specification. But 10:54:30
10 at the same time, I don't recall taking a 10:54:37
11 position agreeing with that notion. And I 10:54:38
12 don't -- so -- I don't disagree with it as I sit 10:54:40
13 here today. 10:54:45

14 (Exhibit Numbers 1045, 1046, 2013 10:54:46
15 and 2046 were previously marked for 10:54:46
16 identification.) 10:54:46

17 BY ATTORNEY CHANDLER: 10:54:50

18 Q. And pull up Exhibit 1045. Let me know 10:54:50
19 you have it. I'll put it in the chat as well and 10:54:56
20 make it easier. And I'll also put some other 10:54:58
21 exhibits in the chat, such as Exhibit 1046. And 10:55:04
22 I'll also put in Exhibit 2013. And also 10:55:13
23 Exhibit 2046. 10:55:19

24 Let me know when you have those four 10:55:26
25 exhibits in front of you, either from your own 10:55:27

1 computer or through the chat. 10:55:29

2 A. So I have them all downloaded, or 10:55:40
3 downloading, and I have 1045 open in front of me 10:55:45
4 at the moment. 10:55:48

5 Q. We can probably cover all four at once. 10:55:49
6 Why don't you go ahead and open Exhibit 1046, 10:55:52
7 Exhibit 2013, and Exhibit 2046. Those four 10:55:54
8 exhibits are all the same in both IPRs, and just 10:55:59
9 let me know when you have them, and we can cover 10:56:01
10 them in one fell swoop when you're ready. 10:56:03

11 A. All right. 10:56:18

12 Q. You do not dispute that a person of 10:56:22
13 ordinary skill in the art would have known about 10:56:24
14 the following four exhibits: Exhibit 1045 in 10:56:25
15 both IPRs, which is the JEDEC standard JESD79 for 10:56:29
16 double data rate (DDR) SDRAM dated June 2000; 10:56:36
17 Exhibit 1046, the JESD79-3A JEDEC standard for 10:56:45
18 DDR3 SDRAM; Exhibit 2013, the JEDEC standard 10:56:52
19 Number 21-C for SDRAM unbuffered SO-DIMM dated 10:56:58
20 2001; and Exhibit 2046, the JEDEC standard number 10:57:08
21 21-C for SDRAM unbuffered SO-DIMM Revision 2.5, 10:57:13
22 Release 18; correct? 10:57:19

23 A. I was following you, I think, until the 10:57:27
24 last one. What was the last exhibit? Was that 10:57:29
25 1046? 10:57:32

1	Q.	2046.	10:57:34
2	A.	2046. Give me just a moment.	10:57:35
3	Q.	Exhibit 2046 dated July 2008.	10:57:56
4		Do you have it?	10:58:00
5	A.	Yes, I have it. And yes, I would -- I	10:58:01
6		don't think I've taken the position that a person	10:58:05
7		of ordinary skill in the art would not have had	10:58:07
8		access to and -- and understanding of these four	10:58:15
9		documents.	10:58:21
10	Q.	Turn to Exhibit 1045, and let me know	10:58:23
11		when you have it in front of you. And, again,	10:58:27
12		that's the JEDEC standard JESD79 dated June 2000.	10:58:30
13	A.	I have it opened in front of me now.	10:58:42
14	Q.	So Exhibit 1045 in both IPRs is the	10:58:43
15		JEDEC standard JESD79 for double data rate (DDR)	10:58:46
16		SDRAM memory dated June 2000; correct?	10:58:52
17	A.	Yes, that's correct.	10:59:00
18	Q.	And that's sometimes referred to as the	10:59:01
19		DDR1 standard; is that fair?	10:59:08
20	A.	I don't recall that, but probably. It	10:59:10
21		appears to be the first -- yeah.	10:59:14
22	Q.	Turn to page 1, as stamped in the	10:59:18
23		bottom right of Exhibit 1045. It's the fifth	10:59:23
24		page of the PDF file. And let me know when	10:59:29
25		you're there.	10:59:34

1	A. Yes, I'm there.	10:59:36
2	Q. And as shown in the left side of page 1	10:59:39
3	of Exhibit 1045 directly above the heading	10:59:43
4	"General Description," DDR1 SDRAM memory devices	10:59:47
5	could use a VDDQ voltage of 2.5 volts, and a VDD	10:59:55
6	voltage of 3.3 volts; correct?	11:00:08
7	A. Yes, I see that.	11:00:14
8	Q. And then if you turn to page 3 of	11:00:19
9	Exhibit 1045, as shown on the bottom of page 3 of	11:00:21
10	Exhibit 1045, DDR1 SDRAM memory devices could be	11:00:28
11	x4, x8 or x16; correct?	11:00:36
12	And that's spelled x-8, x-4, or x-16;	11:00:42
13	correct?	11:00:47
14	A. Yes, I see that notation on the address	11:00:50
15	assignment table to the right-hand side.	11:00:53
16	Q. And also in the bottom heading;	11:00:55
17	correct?	11:00:57
18	A. Yes, I see it there as well, yeah.	11:00:59
19	Q. And briefly, how would you explain what	11:01:02
20	x4, x8 and x16, what those terms mean?	11:01:05
21	A. Typically, that means whether there are	11:01:11
22	four sets of communication lines or eight or	11:01:15
23	sixteen.	11:01:19
24	Q. For a given memory chip?	11:01:21
25	A. Sure.	11:01:26

1	Q. Please turn to Exhibit 1026. Let me	11:01:27
2	know when you're there.	11:01:30
3	A. I'm there.	11:01:39
4	Q. So Exhibit 1026 in both IPRs is the	11:01:40
5	JEDEC standard, JESD79-2B for DDR2 SDRAM memory	11:01:43
6	devices dated January 2005; correct?	11:01:50
7	A. Yes, I see that designation.	11:01:54
8	Q. And this standard is sometimes referred	11:01:56
9	to as the DDR2 standard; is that fair?	11:01:59
10	A. Yes, that's fair. In fact, it refers	11:02:03
11	to itself as DDR2, yeah.	11:02:07
12	Q. And turning to page 6, as stamped in	11:02:09
13	bottom right of Exhibit 1026. Let me know when	11:02:13
14	you're there. It's the 14th page of the PDF	11:02:17
15	file.	11:02:20
16	A. Okay, I'm there.	11:02:22
17	Q. As shown at the bottom of page 6 of	11:02:26
18	Exhibit 1026, DDR2 SDRAM memory devices could use	11:02:28
19	a VDDQ voltage of 1.8 volts; correct?	11:02:34
20	A. It says that the power supply should be	11:02:45
21	1.8 volts plus or minus .1 volts.	11:02:48
22	Q. And, in particular, the VDDQ power	11:02:53
23	supply should be 1.8 volts plus or minus	11:02:57
24	0.1 volts; correct?	11:03:01
25	A. Yes, sir, that's correct.	11:03:05

1 Q. And then on the top of the next page,
2 page 7 of Exhibit 1026, DDR2 SDRAM memory devices
3 could use a VDD voltage of 1.8 volts; correct?

4 A. Yes. It says 1.8 volts, again, plus or
5 minus .1 volts.

6 Q. And if you go back to page 6 of
7 Exhibit 1026, at the bottom of that page it shows
8 that DDR2 SDRAM memory devices could use a VDDL
9 voltage of 1.8 volts; correct?

10 A. Yes. Again, like the VDDQ, it lists
11 the power supply as 1.8 volts plus or minus .1
12 volt.

13 Q. And then if you turn back to page 1 of
14 Exhibit 1026, as stamped in the bottom right,
15 which is the ninth page of the PDF file -- let me
16 know when you're there.

17 A. Yes, I'm there.

18 Q. As shown in the bottom of pages 1, 2,
19 and 3 of Exhibit 1026, DDR2 SDRAM memory devices
20 could be x4, x8 or x16; correct?

21 A. Yes, that is what it appears to show.

22 Q. And as shown on the bottom of pages 4
23 and 5 of Exhibit 1026, DDR2 SDRAM memory devices
24 could also be stacked/dual-die x4 or x8 memory
25 devices; is that correct?

75

1	A. At the bottom on page 4 it says	11:05:36
2	"Figure 4--stacked/dual-die DDR2 SDRAM x4," and	11:05:39
3	then on page 5 it says x8.	11:05:50
4	Q. Are you done or --	11:05:59
5	A. Yes, I am.	11:06:01
6	Q. What is stacked/dual-die?	11:06:03
7	A. Typically, that means that the dies are	11:06:08
8	stacked on top of each other physically.	11:06:12
9	Q. And in what circumstances would you	11:06:16
10	want to use a stacked/dual-die memory device?	11:06:18
11	A. Sorry. There's a fellow who was making	11:06:25
12	the noise earlier outside my window.	11:06:28
13	When you wanted to increase the	11:06:33
14	capacity of the memory system.	11:06:36
15	Q. And could you explain that a little	11:06:41
16	more.	11:06:42
17	A. Sure. The physical space on a DIMM	11:06:44
18	would require a certain amount of space, a	11:06:48
19	rectangle or, typically, a square -- I guess it's	11:06:53
20	rectangular -- for one of these integrated	11:06:58
21	circuits. If they were stacked, you've now	11:07:03
22	doubled the amount of memory stored in the same	11:07:09
23	amount of physical space -- two-dimensional	11:07:12
24	physical space. It certainly has a little	11:07:15
25	additional height.	11:07:17

1	Q.	Please turn to Exhibit 1046. Let me	11:07:19
2		know when you're there. It's the same exhibit in	11:07:21
3		both IPRs.	11:07:30
4	A.	I have it opened in front of me now.	11:07:31
5	Q.	Exhibit 1046 is the JEDEC standard	11:07:33
6		JESD79-3A for DDR3 SDRAM memory devices dated	11:07:35
7		September 2007; correct?	11:07:43
8	A.	Yes. I see those designations on the	11:07:45
9		first page of that exhibit.	11:07:49
10	Q.	And this is sometimes referred to as	11:07:51
11		the DDR3 standard; is that fair?	11:07:53
12	A.	Yes, sir, that's fair.	11:07:57
13	Q.	And turn to page 10 of Exhibit 1046 as	11:08:02
14		stamped in the bottom right, which is the 24th	11:08:09
15		page of the PDF file. Let me know when you're	11:08:13
16		there.	11:08:16
17	A.	I am there.	11:08:17
18	Q.	As shown in the middle of page 10 of	11:08:18
19		Exhibit 1046, DDR3 SDRAM memory devices could use	11:08:20
20		a VDDQ voltage of 1.5 volts plus or minus	11:08:26
21		.075 volts, as well as a VDD voltage of 1.5 volts	11:08:37
22		plus or minus 0.075 volts; correct?	11:08:45
23	A.	Yes, I see that.	11:08:51
24	Q.	And if you turn back to page 3 of	11:08:54
25		Exhibit 1046 -- let me know when you're there.	11:08:57

1 This is the 17th page of the PDF file.

11:09:00

2 A. I'm there.

11:09:04

3 Q. As shown at the top of pages 3 to 5 of
4 Exhibit 1046, DDR3 SDRAM memory devices could be
5 x4, x8 or x16; correct?

11:09:06

11:09:10

11:09:18

6 A. Those pages indicate what are called
7 ball assignments for x4, x8 and x16.

11:09:36

11:09:39

8 Q. For DDR3 SDRAM memory devices; correct?

11:09:44

9 A. Yes, sir, that's correct.

11:09:49

10 Q. And then as shown at the top of pages 6
11 to 8 of Exhibit 1046, DDR3 SDRAM memory devices
12 could also be stacked/dual-die, x4, x8 or x16
13 memory devices; is that correct?

11:09:52

11:09:55

11:10:04

11:10:09

14 A. Yes, Section 2.4 refers to
15 stacked/dual-die x4, 2.5 refers to
16 stacked/dual-die DDR3 SDRAM x8, and 2.6 refers to
17 stacked/dual-die DDR3 SDRAM x16.

11:10:21

11:10:28

11:10:34

11:10:41

18 Q. Okay. So now I want to step back and
19 ask you sort of a bigger-picture question about
20 these JEDEC standards for DDR1, DDR2 and DDR3.

11:10:47

11:10:50

11:10:56

21 So you have that in mind as a
22 background to the next question I'm going to ask
23 you?

11:11:01

11:11:04

11:11:06

24 A. I do.

11:11:08

25 Q. So as we just discussed, the voltages

11:11:10

1 required by the JEDEC standard got lower with 11:11:14
2 each new generation of the standard as we went 11:11:19
3 from DDR1 to DDR2 to DDR3; correct? 11:11:23

4 A. Yeah, I believe that to be the case, 11:11:29
5 sure. 11:11:32

6 Q. So in 2000 the JEDEC standard required 11:11:34
7 voltages of 2.5 volts and 3.3 volts for DDR1 11:11:37
8 SDRAM memory devices. Then by 2005 JEDEC lowered 11:11:43
9 the voltages to 1.8 volt for DDR2 SDRAM memory 11:11:48
10 devices. And then by 2007 JEDEC lowered the 11:11:54
11 voltages to 1.5 volts for DDR3 SDRAM memory 11:11:57
12 devices. 11:12:03

13 Is that fair? 11:12:06

14 A. That sounds right. 11:12:07

15 Q. So what's the benefit of using a lower 11:12:09
16 voltage with memory devices? 11:12:12

17 ATTORNEY LINDSAY: Objection; form. 11:12:19

18 THE WITNESS: In general -- well, there 11:12:20
19 are benefits and there are downsides. In 11:12:22
20 general, all things being equal, a lower voltage 11:12:28
21 will result in less power consumption. 11:12:31

22 BY ATTORNEY CHANDLER: 11:12:38

23 Q. Is that your understanding of why each 11:12:44
24 new generation of the JEDEC standard, as it went 11:12:48
25 from DDR1 to DDR2 to DDR3, used a lower voltage 11:12:53

1 to result in less power consumption? 11:12:58

2 A. I wasn't part of the -- any of the 11:13:06
3 JEDEC standards committees, so that's consistent 11:13:09
4 with my expectation of why they did that. I 11:13:17
5 don't really know -- well, various parties have 11:13:20
6 commented on that being a benefit, but I don't 11:13:25
7 recall what the -- I don't know what the 11:13:29
8 committee overall said they were doing that for. 11:13:32

9 Q. So if I understand what you're saying 11:13:37
10 is, you weren't personally involved so you don't 11:13:39
11 personally know what the reasoning was of JEDEC 11:13:42
12 lowering the voltage; but your understanding, as 11:13:45
13 a technical matter, is that a consequence of the 11:13:48
14 voltage getting lower with each version of the 11:13:51
15 JEDEC standard, as you go from DDR1 to DDR2 to 11:13:56
16 DDR3, is that the result would be less power 11:14:00
17 consumption? 11:14:05

18 ATTORNEY LINDSAY: Objection; form. 11:14:07

19 THE WITNESS: I would go farther than 11:14:13
20 that. As I said, all things being equal, 11:14:14
21 lowering the voltage will reduce [sic] in 11:14:18
22 lowering the power consumption, and that's 11:14:22
23 just -- that's an incredibly consistent fact, 11:14:25
24 motivation in the industry. 11:14:33

25 I assume that is part of what motivated 11:14:36

1	JEDEC. I just don't know for sure, not having	11:14:39
2	been there.	11:14:43
3	BY ATTORNEY CHANDLER:	11:14:44
4	Q. All right. I want to move to a	11:14:44
5	slightly different topic. Let me know when	11:14:51
6	you're ready.	11:14:55
7	A. Okay.	11:14:56
8	Q. Do you believe that a person of	11:15:00
9	ordinary skill in the art knew about DIMM memory	11:15:01
10	modules.	11:15:05
11	It's the acronym DIMM, all caps.	11:15:06
12	A. Sure.	11:15:12
13	Q. And did a person of ordinary skill in	11:15:13
14	the art know about RDIMM memory modules?	11:15:15
15	A. Yes, I believe so.	11:15:21
16	Q. And did a person of ordinary skill in	11:15:23
17	the art know about DDR3 LRDIMM memory modules?	11:15:27
18	A. I would expect so, assuming that the	11:15:37
19	introductory date for DDR3 LRDIMM was prior to	11:15:41
20	the date of invention. I don't know that it's	11:15:47
21	not. I just don't recall exactly what that date	11:15:50
22	was.	11:15:52
23	Q. And do you believe a person of ordinary	11:15:53
24	skill in the art would have known about FBDIMM	11:15:54
25	memory modules, as described, for example, in	11:16:00

1 some of the exhibits that we looked at earlier, 11:16:05
2 such as Exhibit 1028 and Exhibit 1027? 11:16:08

3 A. Yes. I believe it likely that a person 11:16:21
4 of ordinary skill in the art, this hypothetical 11:16:24
5 person, would be familiar with FBDIMMs. 11:16:27

6 ATTORNEY CHANDLER: Okay. I'd like to 11:16:32
7 mark a new exhibit as Exhibit 1077. It will be 11:16:33
8 the same document both IPRs, but I'll send it to 11:16:40
9 you twice, the only difference being the stamp in 11:16:45
10 the bottom right that shows the case number. But 11:16:49
11 otherwise, the documents are the same and the 11:16:54
12 page numbers are the same. 11:16:56

13 (Whereupon, Exhibit Number 1077 was 11:16:32
14 marked for identification in both 11:16:32
15 IPR cases and are attached 11:16:32
16 hereto.) 11:16:32

17 BY ATTORNEY CHANDLER: 11:16:57

18 Q. Let me know when you have Exhibit 1077 11:16:58
19 in the chat. 11:17:00

20 A. Yes, I have it in front of me. 11:17:18

21 Q. Exhibit 1077 is Netlist's Technology 11:17:20
22 Tutorial in the ITC case where you were providing 11:17:22
23 expert testimony for Netlist about memory 11:17:27
24 modules; correct? 11:17:31

25 ATTORNEY LINDSAY: Objection; outside 11:17:33

1 the scope of direct. 11:17:33
2 THE WITNESS: Yes, I believe that to be 11:17:41
3 the case. 11:17:42
4 BY ATTORNEY CHANDLER: 11:17:43
5 Q. Please turn to page 2 of Exhibit 1077. 11:17:44
6 Let me know when you're there. 11:17:47
7 A. I am there. 11:17:50
8 Q. Does page 2 of Exhibit 1077 show a 11:17:53
9 picture of a DIMM, which is to say a dual in-line 11:17:55
10 memory module? 11:18:01
11 ATTORNEY LINDSAY: Objection; outside 11:18:02
12 the scope of direct. 11:18:02
13 THE WITNESS: It appears to, although I 11:18:10
14 will say I don't recall if I saw this document at 11:18:12
15 all during the trial. But it appears to be 11:18:15
16 indicating that the hyper cloud memory device, 11:18:19
17 identified in it, is a memory module; and then it 11:18:24
18 says memory modules are called "dual in-line" 11:18:27
19 memory modules because there are in-line 11:18:32
20 connections on each side of the module. 11:18:35
21 BY ATTORNEY CHANDLER: 11:18:38
22 Q. Turn to page 3 of Exhibit 1077, and let 11:18:39
23 me know when you're there. 11:18:42
24 A. I'm there. 11:18:44
25 Q. Do you agree that SDRAM memory devices 11:18:45

1	emerged in the 1990s and have been standardized	11:18:50
2	by JEDEC?	11:18:54
3	ATTORNEY LINDSAY: Objection; outside	11:18:55
4	the scope of direct.	11:18:55
5	THE WITNESS: I don't have an opinion	11:19:08
6	on that one way or another.	11:19:09
7	BY ATTORNEY CHANDLER:	11:19:11
8	Q. Do you agree that SDRAM has evolved in	11:19:11
9	several generations, including DDR, DDR2, DDR3	11:19:16
10	and currently DDR4?	11:19:19
11	ATTORNEY LINDSAY: Objection; outside	11:19:22
12	the scope of direct.	11:19:22
13	THE WITNESS: Yes, I am familiar with	11:19:27
14	that evolution of the various SDRAM products.	11:19:29
15	BY ATTORNEY CHANDLER:	11:19:35
16	Q. From DDR1 through DDR3, and then more	11:19:38
17	recently DDR 4; correct?	11:19:43
18	ATTORNEY LINDSAY: Objection; outside	11:19:45
19	the scope of direct.	11:19:45
20	THE WITNESS: Yes, that's correct.	11:19:49
21	BY ATTORNEY CHANDLER:	11:19:52
22	Q. Turn to page 4 of Exhibit 1077.	11:19:52
23	Do you agree that SDRAM contains	11:19:56
24	several sections called banks, with a B?	11:20:00
25	ATTORNEY LINDSAY: Objection; outside	11:20:04

1 the scope of direct.

11:20:04

2 THE WITNESS: Yes, that is a

11:20:09

3 conventional design of SDRAM chips.

11:20:10

4 BY ATTORNEY CHANDLER:

11:20:14

5 Q. Do you agree that each bank within an
6 SDRAM consists of rows and columns of memory?

11:20:14

11:20:17

7 ATTORNEY LINDSAY: Objection; outside
8 the scope of direct.

11:20:22

11:20:22

9 THE WITNESS: That is the general
10 structure of most SDRAM that I'm familiar with.

11:20:26

11:20:28

11 I'm not sure that it is a consistent structure
12 across all SDRAM. And as I said, I don't recall
13 if I ever actually reviewed this document during
14 trial.

11:20:31

11:20:35

11:20:38

11:20:44

15 BY ATTORNEY CHANDLER:

11:20:45

16 Q. But it would at least be common, based
17 on your experience, for SDRAM to have rows and
18 columns of memory; is that fair?

11:20:46

11:20:47

11:20:50

19 A. Yes, it would be common for SDRAM to
20 have -- SDRAM banks to have rows and columns.

11:20:54

11:20:59

21 Q. Please turn to page 5 of Exhibit 1077.
22 Let me know when you're there.

11:21:05

11:21:09

23 A. I am there.

11:21:12

24 Q. Do you agree that a rank is a set of
25 DRAMs that are written to or read from together?

11:21:14

11:21:16

1 ATTORNEY LINDSAY: Objection; outside 11:21:20
2 the scope of direct. 11:21:20
3 THE WITNESS: Yes, that is my 11:21:29
4 understanding of how the term "rank" is used, in 11:21:29
5 general. 11:21:32
6 BY ATTORNEY CHANDLER: 11:21:32
7 Q. And do you agree that DQ refers to a 11:21:32
8 data signal? 11:21:37
9 ATTORNEY LINDSAY: Objection; outside 11:21:39
10 the scope of direct. 11:21:39
11 THE WITNESS: Yeah, as indicated here, 11:21:43
12 DQ is showing a data signal coming from or going 11:21:48
13 to a memory controller. 11:21:52
14 BY ATTORNEY CHANDLER: 11:21:55
15 Q. So in the example on page 5 of 11:21:55
16 Exhibit 1077, there are two ranks shown, 11:22:00
17 highlighted in green and red, where each rank 11:22:04
18 comprises eight DRAM memory devices, and each 11:22:08
19 DRAM memory device is 8 bits wide, resulting in 11:22:14
20 each rank of memory devices having a total bit 11:22:18
21 width of 64 bites; is that fair? 11:22:23
22 ATTORNEY LINDSAY: Objection; outside 11:22:29
23 the scope of direct. 11:22:29
24 THE WITNESS: Yes, I believe that to be 11:22:33
25 a fair characterization of what's shown here on 11:22:34

1 page 5 of this tutorial.

11:22:37

2 BY ATTORNEY CHANDLER:

11:22:38

3 Q. Turn to page 6 of Exhibit 1077. Let me
4 know when you're there.

11:22:39

11:22:41

5 A. Okay I'm there.

11:22:45

6 Q. Do you agree that DQS refers to the
7 data strobe signal?

11:22:46

11:22:49

8 ATTORNEY LINDSAY: Objection; outside
9 the scope of direct.

11:22:52

11:22:52

10 THE WITNESS: Yes, it does.

11:22:55

11 BY ATTORNEY CHANDLER:

11:22:57

12 Q. And do you agree that DDR2 memory
13 devices have a clock speed that's approximately
14 twice as fast as the clock speed of DDR1 memory
15 devices?

11:22:57

11:23:01

11:23:05

11:23:08

16 ATTORNEY LINDSAY: Objection; outside
17 the scope of direct.

11:23:10

11:23:10

18 THE WITNESS: Yeah, here it's showing
19 the clock period or DDR1 at 5 nanoseconds, and
20 then DDR2 at 2.5 nanoseconds. And so since the
21 clock period has been cut in half, the clock
22 frequency has doubled.

11:23:14

11:23:16

11:23:21

11:23:26

11:23:29

23 BY ATTORNEY CHANDLER:

11:23:31

24 Q. And do you agree that DDR3 memory
25 devices use a clock speed that's approximately

11:23:31

11:23:33

1	twice as fast as the clock speed for DDR2 memory	11:23:36
2	devices?	11:23:40
3	ATTORNEY LINDSAY: Objection; outside	11:23:42
4	the scope of direct.	11:23:42
5	THE WITNESS: Yes, this -- this slide	11:23:46
6	indicates that DDR3 has a clock period of 1.25	11:23:47
7	nanoseconds, which is half of that for DDR2; and	11:23:53
8	thus, its frequency would be double.	11:23:58
9	BY ATTORNEY CHANDLER:	11:24:05
10	Q. So going from DDR1 to DDR2 to DDR3, the	11:24:05
11	clock speed got faster with each new generation;	11:24:10
12	is that fair?	11:24:12
13	ATTORNEY LINDSAY: Objection; outside	11:24:16
14	the scope of direct.	11:24:16
15	THE WITNESS: Yes, I think that is fair	11:24:17
16	to say. That's what this slide shows.	11:24:19
17	BY ATTORNEY CHANDLER:	11:24:22
18	Q. What's the benefit of using a faster	11:24:22
19	clock speed with memory devices?	11:24:24
20	ATTORNEY LINDSAY: Objection; outside	11:24:27
21	the scope of direct.	11:24:27
22	THE WITNESS: It depends. I would say,	11:24:32
23	all things being equal, if you increase the clock	11:24:34
24	speed, you will increase the performance of the	11:24:39
25	device.	11:24:41

1 However, these are very complex, 11:24:44
2 technical engineering jobs, and so -- technical 11:24:48
3 engineering challenges, rather. And so you can 11:24:54
4 very rarely meet the clock frequency that -- at 11:25:00
5 which you would like to operate and have to make 11:25:05
6 some sacrifices. 11:25:07

7 BY ATTORNEY CHANDLER: 11:25:12

8 Q. Did the performance of DDR memory 11:25:19
9 devices improve going from the DDR1 generation to 11:25:25
10 the DDR2 generation to the DDR3 generation? And 11:25:28
11 if so, in what regards? 11:25:34

12 ATTORNEY LINDSAY: Objection; form. 11:25:36

13 THE WITNESS: Well, there's a broad set 11:25:40
14 of what I would call performance characteristics 11:25:42
15 for these devices. I don't know that I could say 11:25:44
16 that they all improved; but certainly the 11:25:48
17 bandwidth, which is the rate at which you could 11:25:55
18 move data on to and off of the chips, did improve 11:25:59
19 as you progress from, for example, DDR1 to DDR2 11:26:04
20 to DDR3. 11:26:08

21 BY ATTORNEY CHANDLER: 11:26:13

22 Q. And we were talking a little while ago 11:26:13
23 about the power consumption and the voltage 11:26:17
24 levels as you move from DDR1 to DDR2 to DDR3. 11:26:24
25 Were there improvements in that regard as well? 11:26:28

1 A. So as we saw, the voltage levels on 11:26:33
2 some of the signals did indeed reduce, and -- 11:26:36
3 over that evolutionary path from DDR1 to DDR2 and 11:26:41
4 DDR3. 11:26:47

5 And as I said, all things being equal, 11:26:49
6 I would expect the power consumption to similarly 11:26:53
7 have been reduced, but I don't know for sure that 11:26:57
8 the overall consumption -- the reductions that 11:27:01
9 would be made -- that would be desired or 11:27:05
10 anticipated with all other things being equal, 11:27:08
11 were actually achievable. 11:27:10

12 Q. Can you turn to page 7 of Exhibit 1077. 11:27:15
13 Let me know when you're there. 11:27:18

14 A. Okay. Yes, I'm there. 11:27:24

15 Q. Do you agree that page 7 of 11:27:26
16 Exhibit 1077 illustrates an unbuffered DIMM, also 11:27:27
17 known as a UDIMM? 11:27:33

18 ATTORNEY LINDSAY: Objection; outside 11:27:37
19 the scope of direct. 11:27:37

20 THE WITNESS: Yes, this slide appears 11:27:39
21 to be displaying a UDIMM. 11:27:43

22 BY ATTORNEY CHANDLER: 11:27:45

23 Q. And in your opinion, did a person of 11:27:46
24 ordinary skill in the art know about UDIMM memory 11:27:48
25 modules? 11:27:52

1 A. A hypothetical person of ordinary skill 11:27:57
2 in the art may very well have been aware of the 11:27:59
3 concept of UDIMMs. 11:28:02
4 Q. Using this illustration on page 7 of 11:28:04
5 Exhibit 1077, how would you explain to a 11:28:08
6 layperson what a UDIMM memory module is? 11:28:10
7 ATTORNEY LINDSAY: Objection; outside 11:28:13
8 the scope of direct. 11:28:13
9 THE WITNESS: I generally would not 11:28:17
10 attempt to make such an explanation. 11:28:20
11 BY ATTORNEY CHANDLER: 11:28:24
12 Q. How would you explain to a person of 11:28:25
13 ordinary skill in the art what a UDIMM memory 11:28:29
14 module is, using page 7 of Exhibit 1077? 11:28:33
15 ATTORNEY LINDSAY: Objection; outside 11:28:37
16 the scope of direct. 11:28:37
17 THE WITNESS: I'm not ready to do that 11:28:43
18 on the fly, other than saying a UDIMM is a DIMM 11:28:45
19 that is now missing certain buffers. 11:28:49
20 BY ATTORNEY CHANDLER: 11:28:59
21 Q. On the memory module? 11:29:00
22 A. Yes. 11:29:01
23 Q. Turn to page 8 of Exhibit 1077. Let me 11:29:05
24 know when you're there. 11:29:09
25 A. I am there. 11:29:10

1 Q. Do you agree that page 8 of 11:29:11
2 Exhibit 1077 illustrates a registered DIMM, also 11:29:12
3 known as an RDIMM? 11:29:16
4 ATTORNEY LINDSAY: Objection; outside 11:29:19
5 the scope of direct. 11:29:19
6 THE WITNESS: Page 8 has a title that 11:29:23
7 says "Evolution of DIMMs: JEDEC Registered 11:29:25
8 DIMM," and then in parentheses "RDIMM." 11:29:31
9 So it's labeled as illustrating aspects 11:29:34
10 of RDIMMs. 11:29:37
11 BY ATTORNEY CHANDLER: 11:29:39
12 Q. And in your opinion, would a person of 11:29:40
13 ordinary skill in the art have known about RDIMM 11:29:41
14 memory modules? 11:29:46
15 ATTORNEY LINDSAY: Objection; outside 11:29:47
16 the scope of direct. 11:29:47
17 THE WITNESS: I think a person of 11:29:51
18 ordinary skill in the art may very well have 11:29:52
19 been -- a hypothetical person of ordinary skill 11:29:55
20 in the art may very well have been familiar with 11:29:57
21 the concept of RDIMMs. 11:30:02
22 BY ATTORNEY CHANDLER: 11:30:04
23 Q. And using the illustration on page 8 of 11:30:04
24 Exhibit 1077, how would you explain the concept 11:30:08
25 of RDIMMs? 11:30:10

1 ATTORNEY LINDSAY: Objection; outside 11:30:13
2 the scope of direct. 11:30:13
3 THE WITNESS: I would begin and end by 11:30:19
4 saying that there's a new element that's been 11:30:22
5 added, compared to previous DIMM design, and 11:30:25
6 that's called a register or RCD. And that's 11:30:29
7 shown in this figure as sitting between some of 11:30:40
8 the control and address signals of the memory 11:30:42
9 controller and the various DRAM chips. 11:30:49
10 BY ATTORNEY CHANDLER: 11:30:55
11 Q. So an RDIMM has a register for control 11:31:00
12 and address signals from the memory controller 11:31:13
13 but not for data signals from the memory 11:31:16
14 controller; is that fair? 11:31:21
15 ATTORNEY LINDSAY: Objection; 11:31:22
16 foundation, outside the scope of direct. 11:31:22
17 THE WITNESS: I think that that's 11:31:28
18 generally accurate, as depicted here on the 11:31:29
19 slide, yep. 11:31:32
20 BY ATTORNEY CHANDLER: 11:31:33
21 Q. What's the benefit of using a register 11:31:34
22 on the memory module for address and control 11:31:36
23 signals? 11:31:41
24 ATTORNEY LINDSAY: Objection; outside 11:31:42
25 the scope of direct. 11:31:42

1 THE WITNESS: I'm not sure that I know 11:31:48
2 the full set of benefits that would review -- I 11:31:48
3 would identify, let alone what JEDEC specifically 11:31:53
4 identified. 11:31:58

5 However, as a basic design approach, 11:31:59
6 adding the register will add a delay into the 11:32:02
7 DIMM for getting commands. However, it will 11:32:09
8 reduce what we refer to as the load of those 11:32:14
9 signal wires, such that the clock rate has an 11:32:19
10 opportunity to be increased -- the clock 11:32:22
11 frequency. 11:32:25

12 So in general, this -- an approach like 11:32:25
13 this is used to increase the clock frequency and 11:32:29
14 improve performance in that way, although the 11:32:36
15 ultimate time, the final time for any particular 11:32:40
16 access to the DRAM might increase. 11:32:42

17 BY ATTORNEY CHANDLER: 11:32:50

18 Q. Are you saying that the net result can 11:32:51
19 be a positive impact on performance if there's a 11:32:54
20 register on the memory module? 11:32:59

21 A. I'm more saying it can be a positive 11:33:03
22 impact on performance with regards to the overall 11:33:06
23 throughput of the memory system: How much data 11:33:10
24 per unit time I can move on to or off of. It can 11:33:14
25 have a negative impact on performance with 11:33:19

1 regards to any one individual read or write 11:33:21
2 transaction. 11:33:27

3 Q. But the overall impact with respect to 11:33:29
4 throughput could be a positive impact with 11:33:33
5 respect to performance; is that fair? 11:33:38

6 ATTORNEY LINDSAY: Objection; outside 11:33:40
7 the scope of direct, form. 11:33:40

8 THE WITNESS: I would say, again, with 11:33:49
9 respect to throughput, an approach like this is 11:33:50
10 being done to increase throughput. I wouldn't -- 11:33:52
11 I just don't understand how to use the concept of 11:33:56
12 "overall." 11:33:59

13 The throughput and latency are just two 11:34:02
14 different things. Sometimes -- and by "latency" 11:34:05
15 I mean the time it takes to do one particular 11:34:10
16 read or write. 11:34:13

17 They're both important, but for the 11:34:15
18 most part, I think that DIMMs tend to focus on 11:34:17
19 throughput as opposed to latency. 11:34:24

20 BY ATTORNEY CHANDLER: 11:34:26

21 Q. And you mentioned a moment ago "load." 11:34:26
22 What is load? 11:34:29

23 ATTORNEY LINDSAY: Outside the scope of 11:34:31
24 direct. 11:34:31

25 THE WITNESS: So "load" can mean quite 11:34:36

1 a number of different things. 11:34:39

2 In this context, what I was referring 11:34:40
3 to is, I guess I would say, the amount of 11:34:42
4 electrical interconnect that is attached to a 11:34:52
5 component that needs to drive a signal over that 11:34:59
6 interconnect. 11:35:02

7 So, for example, the memory controller 11:35:04
8 is sending address and control signals to the 11:35:05
9 DIMM. The load would be related to how long the 11:35:10
10 wires are, all the wires that are connected to it 11:35:16
11 and other electrical properties of those specific 11:35:19
12 wires. 11:35:21

13 BY ATTORNEY CHANDLER: 11:35:23

14 Q. When you put a register on the memory 11:35:28
15 module, as shown with an RDIMM, what changes if 11:35:30
16 any does the register make to the address command 11:35:39
17 and clock signals that are sent from the memory 11:35:47
18 controller to the memory module? 11:35:50

19 ATTORNEY LINDSAY: Objection; outside 11:35:53
20 the scope of direct, and form. 11:35:53

21 THE WITNESS: Well, as an initial 11:36:00
22 matter, I would say that while I agree that it is 11:36:02
23 not uncommon in RDIMMs to refer to that as that 11:36:05
24 block as "register," it's also referred to as the 11:36:09
25 RCD, which, I think, is more accurate. It's -- 11:36:13

1 and I only say that because it's -- it's much 11:36:16
2 more than the concept of a -- what I would say is 11:36:19
3 just a register. 11:36:23

4 And then with regards to what sort of 11:36:27
5 changes it makes on the various signals -- I 11:36:29
6 guess I would say there's a set of signal pins 11:36:37
7 that are connected from the memory controller 11:36:40
8 across signal wires that are connected from the 11:36:45
9 memory controller to the register over the pins 11:36:48
10 of the DIMM, and then it produces a different set 11:36:52
11 of signals -- signal wires that come out of the 11:36:56
12 register and are sent to the various DRAM 11:37:01
13 modules. 11:37:05

14 (Exhibit Number 2044 was previously
15 marked for identification.)

16 BY ATTORNEY CHANDLER: 11:37:06

17 Q. Please turn to Exhibit 2044, and let me 11:37:11
18 know when you're there. It's the same exhibit in 11:37:16
19 both IPRs; and I will also put it in the chat for 11:37:19
20 everyone if that helps. 11:37:24

21 A. Okay, I have it opened in front of me 11:37:48
22 now. 11:37:49

23 Q. Exhibit 2044 in both IPRs is a data 11:37:50
24 sheet for an RDIMM memory module similar to 11:37:55
25 what's shown on page 8 of Exhibit 1077; correct? 11:38:00

1 A. Yes. I believe so. 11:38:07
2 Q. Please turn to page 9 of Exhibit 1077. 11:38:21
3 Let me know when you're there. 11:38:26
4 A. All right. I'm on page 9. 11:38:45
5 Q. Does page 9 of Exhibit 1077 illustrate 11:38:47
6 a fully buffered DIMM, also known as an FBDIMM? 11:38:50
7 ATTORNEY LINDSAY: Objection; outside 11:38:57
8 the scope of direct. 11:38:57
9 THE WITNESS: I'm sorry. We're in 11:39:06
10 Exhibit 2044 on page 9; right? 11:39:08
11 BY ATTORNEY CHANDLER: 11:39:12
12 Q. No. 11:39:12
13 A. Sorry. 11:39:13
14 Q. Exhibit 1077, page 9. 11:39:16
15 A. Ah, okay. 11:39:21
16 Q. So does page 9 of Exhibit 1077 11:39:26
17 illustrate a fully buffered DIMM, also known as 11:39:29
18 an FBDIMM? 11:39:31
19 A. So that slide is labeled "Evolution of 11:39:36
20 DIMMs: Fully buffered DIMM (FBDIMM)." 11:39:40
21 And then there's an illustration below 11:39:46
22 that which I expect was an attempt to illustrate 11:39:48
23 some of the major characteristics, architectural 11:39:52
24 structures of an FBDIMM. 11:39:55
25 Q. And how would you explain some of the 11:39:59

1 major characteristics of the architectural 11:40:03
2 structure of an FBDIMM? 11:40:08
3 ATTORNEY LINDSAY: Objection; outside 11:40:10
4 the scope of direct. 11:40:10
5 THE WITNESS: I would say that with an 11:40:18
6 FBDIMM, all of the signals, from address command 11:40:20
7 and clock and control, and the data signals and 11:40:24
8 the DQSS are directed first to a block called the 11:40:28
9 AMB and, thus, electrically separated or isolated 11:40:34
10 from the DRAM circuits themselves. 11:40:42
11 BY ATTORNEY CHANDLER: 11:40:46
12 Q. And what does AMB stand for? Does it 11:40:47
13 stand for advanced memory buffer, as I believe 11:40:50
14 shown in one of the JEDEC standards we looked at; 11:40:55
15 a little earlier? 11:40:58
16 ATTORNEY LINDSAY: Objection; form. 11:41:00
17 THE WITNESS: Yes -- yes, sir, that's 11:41:03
18 my recollection. 11:41:05
19 BY ATTORNEY CHANDLER: 11:41:06
20 Q. And what's the benefit of buffering 11:41:06
21 data lines on a memory module? 11:41:09
22 A. Well, one benefit -- one -- I'm not 11:41:21
23 sure what the benefit is in this context, to be 11:41:30
24 quite honest with you. 11:41:35
25 Q. Just generally speaking -- 11:41:36

1 A. So I would say, generally speaking,
2 buffering the data lines is not going to reduce
3 the load on a single DIMM, as opposed to what we
4 saw previously with the address comment and clock
5 signals.

11:41:46
11:41:51
11:41:58
11:42:05
11:42:11

6 However, the length of those -- of the
7 electrical traces between the memory controller
8 and the AMB is likely to be smaller, shorter and,
9 again, might present the opportunity for having
10 the FBDIMM running at a faster clock frequency
11 with the result of some increased latency.

11:42:12
11:42:16
11:42:20
11:42:29
11:42:33
11:42:38

12 Although now that I think about it,
13 there would be a benefit of reducing the load in
14 a multirank FBDIMM. I don't recall whether
15 FBDIMMs were offered with multiple ranks or not,
16 but assuming they were, it would provide that
17 benefit as well.

11:42:43
11:42:44
11:42:46
11:42:51
11:42:54
11:42:56

18 Q. Turn to page 10 of Exhibit 1077. Let
19 me know when you're there.

11:43:12
11:43:15

20 A. Okay, I'm.

11:43:21

21 Q. Do you agree that page 10 of
22 Exhibit 1077 illustrates a DDR3 LRDIMM memory
23 module?

11:43:22
11:43:23
11:43:28

24 ATTORNEY LINDSAY: Outside the scope of
25 direct.

11:43:30
11:43:30

1 THE WITNESS: I would certainly agree 11:43:37
2 that it's labeled "Evolution of DIMMs: JEDEC 11:43:38
3 DDR3 LRDIMM (Gen. 1)", and then below that 11:43:44
4 heading on the slide there is a box labeled "DDR3 11:43:48
5 LRDIMM." 11:43:54
6 BY ATTORNEY CHANDLER: 11:43:57
7 Q. What are some of the primary 11:43:58
8 characteristics of a DDR3 LRDIMM memory module, 11:44:00
9 as shown on page 10 of Exhibit 1077? 11:44:04
10 A. Well, again, it's showing all of the 11:44:12
11 signals from the memory controller being buffered 11:44:14
12 or registered. 11:44:19
13 Q. And that could improve throughput, if I 11:44:25
14 understand your prior testimony, by reducing 11:44:32
15 electrical load; is that fair? 11:44:35
16 A. All things being equal -- of course, 11:44:42
17 things are never equal between two different 11:44:44
18 designs. But as a basic engineering approach, it 11:44:46
19 could -- would likely result in reduced load, 11:44:53
20 which could result in increased throughput. 11:44:58
21 Q. What is an SO-DIMM? 11:45:05
22 ATTORNEY LINDSAY: Objection; outside 11:45:12
23 the scope of direct. 11:45:12
24 THE WITNESS: Yeah, my recollection is 11:45:14
25 that SO is "small outline" but I don't recall for 11:45:15

1 sure. It's a form of DIMM that is typically used 11:45:22
2 in small form-factor devices. 11:45:27

3 BY ATTORNEY CHANDLER: 11:45:36

4 Q. Please turn to Exhibit 2046. Let me 11:45:37
5 know when you're there. 11:45:40

6 A. Okay, I'm there. 11:45:47

7 Q. Exhibit 2046, which is the same in both 11:45:48
8 IPRs, is the JEDEC standards for SO-DIMM memory 11:45:52
9 modules; is that correct? 11:46:02

10 A. It's the standard for DDR2 SDRAM 11:46:06
11 unbuffered SO-DIMM memory modules. 11:46:10

12 Q. As of July 2008; correct? 11:46:15

13 A. Yes, this is Revision 2.5 as of 11:46:19
14 July 2008. 11:46:22

15 Q. Turn to the page number in the upper 11:46:26
16 right 4.20.11-23, which I believe is the 23rd 11:46:31
17 page of the PDF file. Let me know when you're 11:46:39
18 there. And this is, again, Exhibit 2046. 11:46:40

19 A. Yes, I'm there. 11:46:49

20 Q. Page 4.20.11-23 of Exhibit 2046 11:46:50
21 illustrates an SO-DIMM memory module; correct? 11:46:57

22 A. Yeah, it appears to be describing 11:47:12
23 form-factor elements of what they refer to as raw 11:47:16
24 cards E and F. 11:47:23

25 Q. And I believe you said earlier this is 11:47:24

1 an unbuffered SO-DIMM, meaning that on 11:47:26
2 page 4.20.11-23 of Exhibit 2046 there's no 11:47:31
3 register or RCD or buffer shown on the SO-DIMM 11:47:38
4 memory model; is that fair? 11:47:44
5 A. There's no buffer or RCD shown in these 11:47:49
6 figures. I really don't know. Previously, I was 11:47:55
7 just saying that the document is captured 11:48:00
8 unbuffered -- is captioned, rather, "unbuffered." 11:48:03
9 So I assume that that applies to all of the cards 11:48:07
10 and DIMMs in the document. 11:48:12
11 (Exhibit Number 2045 was previously
12 marked for identification.)
13 BY ATTORNEY CHANDLER: 11:48:18
14 Q. Turn to Exhibit 2045. Let me know when 11:48:18
15 you're there. I'll also put it in the chat. 11:48:21
16 A. All right. I have it in front of me. 11:48:43
17 Q. Exhibit 2045 is a data sheet for a DDR2 11:48:48
18 SDRAM SODIMM memory module; correct? 11:48:54
19 A. Yes, that appears to be what it is. 11:49:01
20 That's how it's labeled. I don't recall if I 11:49:03
21 reviewed this or not, as I sit here. But that is 11:49:06
22 indeed how it's labeled. 11:49:10
23 Q. And the figure on the cover page of 11:49:12
24 Exhibit 2045 is similar to the figure that we 11:49:18
25 just looked at on page 4.20.11-23 of 11:49:23

1	Exhibit 2046; is that fair?	11:49:34
2	A. Yeah, it certainly has similarities.	11:49:44
3	Q. And the SODIMM in Exhibit 2046 is	11:49:50
4	similar to the SODIMM in Exhibit 2045 in that	11:50:04
5	they both appear to be unbuffered memory modules;	11:50:07
6	is that fair?	11:50:14
7	A. I would say that they don't appear	11:50:18
8	to -- the figures there don't appear to show	11:50:20
9	buffering. I would certainly agree with that.	11:50:23
10	ATTORNEY CHANDLER: All right. I'm	11:50:32
11	thinking of taking a break. It's 11:50. Why	11:50:33
12	don't we go off the record and we can discuss the	11:50:36
13	length of the break.	11:50:38
14	THE VIDEOGRAPHER: Off the record at	11:50:39
15	11:50 a.m. Pacific Time.	11:50:40
16	(Recess taken from 11:50 a.m. to	
17	11:58 a.m.)	
18	THE VIDEOGRAPHER: On the record at	11:58:29
19	11:58 a.m. Pacific Time.	11:58:30
20	BY ATTORNEY CHANDLER:	11:58:34
21	Q. And Dr. Mangione-Smith, what is a buck	11:58:37
22	converter?	11:58:40
23	A. A buck converter is a particular form	11:58:44
24	of switching voltage regulator.	11:58:47
25	Q. And how would you explain to someone	11:58:55

1 what a buck converter does?

11:58:57

2 A. Well, there are a number of different
3 types of buck converters; but oftentimes, what it
4 does is it will -- a buck converter will be used
5 to take a particular voltage and convert it to a
6 lower voltage as needed; or potentially, a higher
7 voltage buck boost convert will increase the
8 voltage.

11:59:04

11:59:07

11:59:12

11:59:16

11:59:21

11:59:25

11:59:30

9 Q. And that was my next question: What is
10 a boost converter?

11:59:31

11:59:33

11 A. Well, there you go: It's a -- it's a
12 converter that uses buck converter techniques to
13 increase the output voltage. So if the input
14 voltage is five volts and you need 20 volts, you
15 could design a buck boost converter to produce
16 the necessary 20-volt output.

11:59:35

11:59:41

11:59:45

11:59:48

11:59:51

11:59:55

17 Q. And is there something called a "boost
18 buck converter"?

12:00:01

12:00:04

19 A. There might be. I would assume it's
20 the same as a buck boost converter, but possibly
21 those two terms, there are people that use them
22 both ways, yeah.

12:00:08

12:00:11

12:00:16

12:00:18

23 Q. All right. Would you agree that buck
24 converters were known in the art by the time of
25 the '918 and '054 patents?

12:00:19

12:00:21

12:00:24

1	A. Yes. For example, I was familiar with	12:00:29
2	them at least as -- back in the 1996 time frame.	12:00:33
3	Q. And would your answer be the same for	12:00:41
4	boost converters and boost buck converters?	12:00:44
5	A. Generally, yes, those were known	12:00:49
6	concepts.	12:00:51
7	Q. You mentioned a moment ago the word	12:00:54
8	"switching," I believe.	12:01:02
9	A. Yes.	12:01:03
10	Q. Could you explain a little bit more	12:01:10
11	what the relationship is between a buck converter	12:01:11
12	and a switching voltage regulator.	12:01:13
13	A. A buck converter is one example of a	12:01:19
14	switching voltage regulator.	12:01:21
15	Q. And how does a buck converter work? At	12:01:24
16	a high level.	12:01:30
17	A. At a high level, a buck converter has a	12:01:33
18	switching element that takes an input voltage and	12:01:36
19	switches on or off; and then typically has a	12:01:40
20	capacitor on an output that allows the switched	12:01:46
21	voltage to be integrated and averaged over time	12:01:53
22	to achieve a lower voltage.	12:01:57
23	Q. Are you familiar with something called	12:02:06
24	a pulse width modulation circuit or PWM, as in	12:02:08
25	Mary?	12:02:16

1 A. Yes, I am. 12:02:16

2 Q. What's a pulse width modulation circuit 12:02:17

3 and what's its relevance to buck converters? 12:02:22

4 A. A PWM is a circuit that switches -- is 12:02:25

5 a circuit where the output, at least in my 12:02:32

6 experience, switches at a fixed frequency, but 12:02:37

7 the -- the duty cycle of the switching changes. 12:02:40

8 And by that what I mean is the 12:02:46

9 on-time -- if it's switching, it spends some time 12:02:50

10 on and some time off. For a 50 percent duty 12:02:52

11 cycle, the on time would be equal to the off 12:02:57

12 time. For a 25 percent duty cycle, the on time 12:03:00

13 would be one quarter of the time and the off time 12:03:04

14 would be three-quarters, for example. 12:03:09

15 Q. And does changing the on and off time 12:03:11

16 of the PWM circuit change the output voltage? 12:03:18

17 A. Well, PWMs are used in a wide variety 12:03:26

18 of situations. So they are not just used for 12:03:29

19 voltage control at all. 12:03:33

20 However, if you, again, introduce some 12:03:35

21 sort of capacitance on the output that would 12:03:39

22 average out the voltage, then yes, a PWM could be 12:03:43

23 used to control the output voltage. 12:03:47

24 Q. And what is an inductor? 12:04:04

25 A. An inductor is generally a -- it's a 12:04:07

1	circuit that has electromagnetic properties. And	12:04:18
2	the simplest example would be a coil of wire.	12:04:22
3	Q. And what's the relevance of an	12:04:30
4	inductor, if any, to a buck converter?	12:04:32
5	A. Buck converters typically make use of	12:04:38
6	inductors in their design.	12:04:42
7	Q. And so at a high level, how does a buck	12:04:46
8	converter use an inductor and a PWM circuit to	12:04:50
9	convert an input voltage to an output voltage?	12:04:56
10	A. So the capacitor that I mentioned	12:05:00
11	previously generally has the effect of smoothing	12:05:03
12	out variations in voltage; and an inductor	12:05:09
13	generally has the effect of smoothing out changes	12:05:13
14	in current.	12:05:17
15	(Exhibit Number 1058 was previously	12:05:20
16	marked for identification.)	12:05:20
17	BY ATTORNEY CHANDLER:	12:05:23
18	Q. Could you look at Exhibit 1058, which I	12:05:24
19	just put in the chat. Let me know when you're	12:05:27
20	there.	12:05:29
21	A. All right, I have it.	12:06:03
22	Q. Exhibit 1058, which is the same in both	12:06:04
23	IPRs, is a textbook by John D. Lenk titled	12:06:06
24	"Simplified Design of Switching Power Supplies";	12:06:12
25	correct?	12:06:15

1	A. Yes, that's correct.	12:06:23
2	Q. Did you personally use this textbook	12:06:23
3	when you were teaching?	12:06:27
4	A. No.	12:06:30
5	Q. Turn to page 5 of Exhibit 105. Let me	12:06:34
6	know when you're there.	12:06:38
7	A. I am there.	12:06:40
8	Q. Page 5 of Exhibit 1058 shows a buck	12:06:44
9	converter in the middle section of the page;	12:06:46
10	correct?	12:06:53
11	A. Yes, that's correct.	12:06:54
12	Q. And above it is a boost converter, and	12:06:57
13	below is a buck boost converter; correct?	12:07:00
14	A. Yes, that's correct.	12:07:04
15	Q. So focusing for a moment on the buck	12:07:05
16	converter on page 5 of Exhibit 1058, could you	12:07:08
17	identify the inductor, the capacitor and where	12:07:15
18	the PWM circuit would be.	12:07:21
19	A. So the -- an inductor is drawn -- is	12:07:26
20	illustrated, by people of ordinary skill in the	12:07:33
21	art, in circuits of this sort as sort of the	12:07:36
22	lines that have little bumps in them, in this	12:07:41
23	case, four bumps, which are really originally, I	12:07:45
24	believe, intended to be illustrative of a coil in	12:07:49
25	a wire.	12:07:56

1 And then a capacitor is shown in this 12:07:58
2 circuitry as a horizontally straight line with a 12:08:03
3 horizontally slightly curved line right below it, 12:08:12
4 or, I guess, in one of the illustrations right 12:08:16
5 above it. 12:08:19

6 And then if the PWM is meant to be 12:08:21
7 illustrated in here, I think that only leaves the 12:08:26
8 control section block to serve as that role. 12:08:29

9 Q. And using the buck converter circuit 12:08:37
10 illustrated on page 5 of Exhibit 1058, how would 12:08:42
11 you explain at a high level how the circuit 12:08:47
12 works? Where does the electricity voltage come 12:08:50
13 from, where does it go, and what happens in 12:08:54
14 between? 12:08:57

15 ATTORNEY LINDSAY: Objection; form. 12:08:58

16 THE WITNESS: I'm just referring to 12:09:00
17 reading the standard conventions of electrical 12:09:21
18 circuits. I don't recall reviewing Lenk at all 12:09:23
19 or, in particular, referring to this. But if I 12:09:26
20 have, it's been a little while. 12:09:30

21 The -- there are two terminals shown on 12:09:33
22 the -- well, let's start with the left-hand side. 12:09:36

23 The left-hand side shows a battery, 12:09:42
24 which is where -- which produces a certain 12:09:47
25 voltage and a certain current, and that's with 12:09:51

1 four different lines -- long one, short one, long 12:09:54
2 one, short one -- stacked on top of each other; 12:09:58
3 and terminals that are labeled positive and 12:10:00
4 negative. 12:10:02

5 And then the current would flow out of 12:10:06
6 the battery, go through the various circuit 12:10:08
7 elements, and eventually be provided to other 12:10:11
8 circuitry on the right-hand side, where there are 12:10:16
9 terminals labeled V-out, with a plus and a minus 12:10:22
10 above and below them. 12:10:28

11 This is a particular kind of set of 12:10:30
12 switching regulators in that it's designed to 12:10:35
13 work with a battery power supply. 12:10:39

14 BY ATTORNEY CHANDLER: 12:10:46

15 Q. And could you briefly explain how the 12:10:48
16 voltage conversion is accomplished using the 12:10:50
17 circuitry shown on page 5 of Exhibit 105 labeled 12:10:58
18 buck converter. 12:11:04

19 A. Sure. At a very high level, the 12:11:08
20 circuitry shows a switch in the -- along the top 12:11:13
21 edge to the left of the inductor that we saw. 12:11:17

22 That switch is going to selectively 12:11:22
23 couple the rest of the circuitry to the V-batt 12:11:28
24 voltage power supply, at which point the output 12:11:34
25 of that will be connected to the inductor that's 12:11:39

1 shown along the top, as well as the capacitor on 12:11:43
2 the right-hand side; and those two circuit 12:11:47
3 elements will result in the final output voltage 12:11:53
4 that is produced on the far right-hand side, the 12:11:57
5 V-out signal. 12:12:01

6 Q. And you may have said it. So the 12:12:07
7 switch you're referring to is sort of to the left 12:12:23
8 of the inductor and got an up arrow, and below it 12:12:29
9 a horizontal line? 12:12:32

10 A. That's right. That's a particular form 12:12:34
11 of transistor. 12:12:35

12 Q. And then what's the black triangle with 12:12:38
13 the horizontal line going up the middle of the 12:12:42
14 buck converter circuit? 12:12:51

15 A. Yeah, that's called a diode. In its 12:12:51
16 simplest form, and most common form, a diode will 12:12:54
17 only allow current to flow in one direction. 12:12:59

18 Q. What's a LDO linear regulator? 12:13:05

19 A. An LDO, low dropout regulator, is a 12:13:14
20 different form of voltage converter, voltage 12:13:19
21 regulator. 12:13:23

22 Q. And does LDO stand for "low dropout"? 12:13:24

23 A. Yes. 12:13:28

24 Q. And at a high level, how does an LDO 12:13:29
25 linear regulator work? 12:13:35

1 A. Well, the general form -- I guess I 12:13:36
2 would take a step back and say, there's less 12:13:39
3 agreement on a general form -- general 12:13:44
4 architecture of an LDO compared to something like 12:13:48
5 a buck converter or a switching converter. 12:13:53

6 An LDO could be something as simple as 12:13:58
7 a single resistor -- excuse me -- and, in fact, a 12:14:01
8 simple resistor could be nothing more than an 12:14:08
9 electrical wire. But LDOs can also get quite a 12:14:11
10 bit more -- they generally are quite a bit more 12:14:16
11 complicated. 12:14:20

12 Q. And what were some of the trade-offs 12:14:22
13 that were known at the time between using a buck 12:14:24
14 converter and an LDO linear regulator? 12:14:27

15 A. Well, in general, a buck converter 12:14:37
16 might achieve what's referred to as higher 12:14:41
17 efficiency, which is to say, all of these voltage 12:14:49
18 regulators, voltage converters that we're talking 12:14:52
19 about have some amount of electrical power that 12:14:55
20 goes in, and a smaller amount of electrical power 12:14:58
21 that's made available on the output. There's 12:15:02
22 always entropy. There's always loss. 12:15:05

23 So in general, the -- it's understood 12:15:09
24 that something like a switch regulator will have 12:15:12
25 better efficiency than LDOs generally. On the 12:15:16

1 plus side, they tend to be able to support 12:15:25
2 greater current draw. 12:15:27

3 Now, an LDO, while it has lower -- 12:15:30
4 while it may have lower efficacy and not be able 12:15:37
5 to support, in general, comparable current draw 12:15:40
6 as a switching regulator, as I suggested, they're 12:15:45
7 much simpler circuits. So they tend to be much 12:15:50
8 smaller, require less space on a board or inside 12:15:54
9 an integrated circumstance. They will cost less. 12:16:00

10 And so if the performance requirements 12:16:05
11 of a particular need are well-matched to either 12:16:10
12 an LDO or a buck converter, one would be inclined 12:16:17
13 to go with a buck converter because of the other 12:16:21
14 benefits, in comparison, that I just mentioned. 12:16:23

15 Q. And was all of what you just described 12:16:27
16 just now known at the time of the '918 and '054 12:16:30
17 patents? 12:16:35

18 A. Yes. I believe a POSITA would have 12:16:37
19 known those factors. 12:16:42

20 Q. Is there a way to calculate the rough 12:16:43
21 efficiency of an LDO regulator if you know what 12:16:48
22 the input voltage is and the output voltage is? 12:16:51

23 A. If you know what the input voltage and 12:16:58
24 current is, and the output voltage and current, 12:17:00
25 you can calculate the efficiency. 12:17:03

1 Q. So we try to use round numbers, but 12:17:10
2 keeping in mind that I'm not an electrical 12:17:15
3 engineer, if the input is 10 volts and one amp, 12:17:18
4 and the output is 1 volt and one amp, what would 12:17:21
5 be the rough efficiency? 12:17:27

6 A. Well, I'm generally reluctant to do 12:17:31
7 even simple math on the spot, but I believe that 12:17:34
8 would be a 10 percent efficiency. 12:17:38

9 Q. And what would happen to the other 12:17:42
10 90 percent in that example -- in that 12:17:48
11 hypothetical example? Where would it go? 12:17:50

12 A. That depends on the particular design 12:17:54
13 of the LDO. 12:17:56

14 In general -- excuse me -- it's lost to 12:17:57
15 the rest of the system. In practice, there 12:18:02
16 are -- there are ways to recover some of that 12:18:06
17 energy. 12:18:10

18 Q. And when you say that it's lost to the 12:18:19
19 system, is one way that an LDO linear regulator 12:18:31
20 loses energy to the system by way of heat? 12:18:45

21 A. That is one way that LDOs -- that is 12:18:53
22 one way that often happens for certain LDO 12:19:00
23 designs, for them to lose energy. And that's -- 12:19:04
24 that heat is often a source of reduced 12:19:07
25 efficiency. But you could imagine then attaching 12:19:11

1 something like a thermal couple on top of the LDO 12:19:15
2 in an attempt to recover some of that energy. 12:19:19

3 But as a first rule, it's lost to the 12:19:24
4 voltage regulator, the converter, the LDO, even 12:19:29
5 if it can be recovered for use elsewhere. 12:19:34

6 Q. I want to move to a new topic, which 12:19:43
7 would probably take 20 minutes, or if you prefer, 12:19:44
8 we could break for lunch. What would you prefer? 12:19:49

9 A. I think I would prefer to break for 12:19:52
10 lunch. 12:19:54

11 ATTORNEY CHANDLER: All right. Let's 12:19:54
12 do that, and we'll go off the record and we'll 12:19:54
13 pick a time to come back. 12:19:57

14 THE VIDEOGRAPHER: Off the record at 12:19:59
15 12:19 p.m. Pacific Time. 12:20:00

16 (Luncheon recess taken from 12:55
17 p.m. to 12:56 p.m.)

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PROCEEDINGS

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THE VIDEOGRAPHER: On the record at
12:56 p.m. Pacific Time.

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12:57:40

CONTINUED EXAMINATION

BY ATTORNEY CHANDLER:

Q. And Dr. Mangione-Smith, do you have any corrections or clarifications you'd like to make to your testimony earlier today?

A. No, sir.

Q. Could you please turn to page 10 of your expert declarations. And there's a Figure 16 from the patent that you annotated in both of your expert declarations that I'd like to ask you some questions about. Just let me know when you have it in front of you.

A. You said page 10; correct?

Q. Yes.

A. Yes, okay.

Q. So on page 10 of your expert declaration, you've annotated Figure 16 of the

1 '918 and '054 patents; correct? 12:57:44

2 A. Yes. 12:57:47

3 Q. Is Figure 16 an embodiment of the 12:57:48

4 claims of the '918 and '054 patents? 12:57:53

5 A. I don't know. I haven't really 12:58:01

6 considered that. I guess it might be. It's 12:58:03

7 likely it's referred to as an embodiment of the 12:58:08

8 specification. 12:58:12

9 Q. Figure 16 of the '918 and '054 patents 12:58:17

10 shows, on the right side, a buck converter 12:58:21

11 labeled 1122; correct? 12:58:24

12 A. Yes, that's correct. 12:58:30

13 Q. And if you have the patent marked as 12:58:31

14 Exhibit 1001, and you search for 1122, you will 12:58:40

15 see that the buck converter labeled 1122 can 12:58:47

16 output 1.8 volts to the DRAM, to the nonvolatile 12:58:54

17 memory, and to the FPGA; correct? 12:59:02

18 A. Can you tell me where you're looking? 12:59:09

19 I'm searching the patent and whatever OCR'd it 12:59:11

20 was not finding that. 12:59:14

21 Q. Sure. So if you look at the '918 12:59:21

22 patent, Column 29 around line 40, for example. 12:59:25

23 A. Okay. 12:59:29

24 Yeah, I see that. 12:59:48

25 Q. And Figure 16 of the '918 and '054 12:59:53

1	patents also shows, on the right side, a dual	12:59:58
2	buck converter labeled 1124; correct?	01:00:01
3	A. Yes, that's correct.	01:00:08
4	Q. And if you search for "1124" in the	01:00:13
5	'918 and '054 patents, you will see that the dual	01:00:15
6	buck converter, labeled 1124 can output 2.5 volts	01:00:18
7	on 1104 to an isolation device, and 1.8 volts on	01:00:27
8	1105 to the FPGA; correct?	01:00:34
9	A. Yeah. So in Column 29 it says, in one	01:00:58
10	example embodiment, the second voltage, 1104 is	01:01:03
11	2.5 volts and is used to power at least one	01:01:11
12	circuit 1052, e.g., an isolation device; and the	01:01:15
13	other reduced voltage 1105 is 1.2 volts and is	01:01:23
14	used to power the controller 1062, e.g., FPGA.	01:01:28
15	And FPGA stands for field programmable	01:01:39
16	gate array.	01:01:45
17	Q. Figure 16 of the '918 and '054 patents	01:01:46
18	also shows in the right a buck boost converter	01:01:49
19	labeled 1126; correct?	01:01:53
20	A. Yes, it does.	01:01:57
21	Q. And if you search for 1126 in the '918	01:01:58
22	and '054 patents, you will see that the buck	01:02:02
23	boost converter labeled 1126 can output 3.3 volts	01:02:05
24	on line 1107 to the FPGA and to an isolation	01:02:11
25	device; correct? As shown on the right side of	01:02:17

1	Figure 16.	01:02:30
2	A. Okay, yes, I was looking through the	01:02:35
3	text.	01:02:36
4	It does show 1107 going to the FPGA and	01:02:39
5	an isolation device.	01:02:43
6	Q. Does Figure 16 show diodes?	01:02:45
7	A. Yes, it does.	01:02:55
8	Q. And how would you describe where the	01:02:58
9	diodes are shown in Figure 16 of the '918 and	01:03:00
10	'054 patents?	01:03:04
11	A. I believe it's showing them. I believe	01:03:05
12	the line 1110, which I've highlighted in purple,	01:03:09
13	has a diode in it along the horizontal span of	01:03:18
14	it. That's not the conventional sort of	01:03:23
15	universal symbol for a diode, but my recollection	01:03:30
16	is that it represents a particular form of diode.	01:03:34
17	Q. And is there a second diode in	01:03:38
18	Figure 16 of the '918 and '054 patents	01:03:40
19	illustrated?	01:03:44
20	A. Yeah, there's at least the same circuit	01:03:45
21	component, illustrated on line 1112 below that.	01:03:47
22	Q. And at a high level, what would the	01:03:54
23	diode accomplish in Figure 16 of the '918 and	01:03:59
24	'054 patents?	01:04:04
25	A. Well, I only recall what diodes do, in	01:04:07

1 general. I don't -- as I suggested, don't recall 01:04:09
2 that. It's a particular stylized form of diode 01:04:12
3 and how it differentiates from a diode in 01:04:18
4 general. 01:04:20

5 However, a diode, in general, is used 01:04:22
6 to make sure the current only flows in one 01:04:26
7 direction. So, for example, it would avoid 01:04:28
8 having current flow from the capacitor array into 01:04:33
9 the PWM controller. 01:04:37

10 Q. Could you look at Claim 13 of the '918 01:04:55
11 patent. Let me know when you're there. 01:04:58

12 A. I'm there. 01:05:11

13 Q. Claim 13 refers to a power input 01:05:14
14 voltage coupled with the first, second and third 01:05:18
15 buck converters and the converter circuit; 01:05:22
16 correct? 01:05:23

17 A. Yes. 01:05:28

18 Q. And does Figure 16 show the first, 01:05:30
19 second and third buck converter and a converter 01:05:38
20 circuit? 01:05:42

21 A. It may have. I haven't gone to the 01:05:46
22 effort to map Claim 13 on to Figure 16. It does 01:05:48
23 show three buck converters. 01:05:52

24 Q. And does Figure 16 show an input 01:05:59
25 voltage coupled to the buck converters? 01:06:02

1	A.	It shows an input voltage that is	01:06:12
2		conditionally connected to the buck converters.	01:06:17
3	Q.	And what are you pointing to?	01:06:20
4	A.	The -- what appears to be a switch,	01:06:24
5		although it may be labeling the wire 1106.	01:06:27
6	Q.	And I think you said conditionally	01:06:32
7		connected to the buck converters. What do you	01:06:34
8		mean by that?	01:06:36
9	A.	It's a switch. It can be opened or	01:06:37
10		closed.	01:06:39
11	Q.	So if I understand what you're saying,	01:06:42
12		in Figure 16, when 1106 is connected to the wire	01:06:44
13		directly to the right of it, that would be the	01:06:57
14		input voltage coupled to the three buck	01:07:05
15		converters on the right side of Figure 16?	01:07:08
16	A.	I'm sorry. Could you repeat the	01:07:14
17		question.	01:07:15
18	Q.	It's probably easier if you just	01:07:17
19		explain it to me.	01:07:20
20	A.	Okay. Yeah, when the switch is closed,	01:07:21
21		we would say the line 1106 is connected, at least	01:07:26
22		indirectly, through to the buck converters.	01:07:34
23	Q.	I guess what I was trying to clarify	01:07:39
24		is, the switch that you're pointing to is, I	01:07:41
25		guess, sort of right next to the label 1106?	01:07:45

1 A. That's correct. 01:07:49

2 Q. So in Figure 16, the input voltage, 01:07:58

3 1106, is not directly connected to the three buck 01:08:00

4 converters; it goes through another component, 01:08:05

5 either 1130 or 1140; is that correct? And 1140 01:08:10

6 is sort of the big dashed line that you've 01:08:19

7 highlighted in blue. 01:08:23

8 A. Yeah, I think it's only connected 01:08:26

9 indirectly through 1130. 01:08:29

10 Q. So what is 1130 and what does it do? 01:08:37

11 A. It's labeled PWM controller. 01:08:40

12 Q. And what is that and what does it do? 01:08:45

13 A. It controls the pulse width modulation 01:08:48

14 that we discussed previously. 01:08:53

15 Q. And what's the effect that PWM 01:08:55

16 controller 1130 has on the input voltage 1106? 01:09:04

17 A. To be honest with you, I don't recall. 01:09:15

18 I'd have to go back and read the description of 01:09:17

19 exactly -- because there are multiple different 01:09:20

20 architectures that could be used. 01:09:24

21 And as I have explained, unfortunately, 01:09:28

22 these PDFs for the patents are only somewhat 01:09:31

23 searchable. When I search for "1130," I got 01:09:37

24 nothing. Although maybe -- well, "PWM" only 01:09:41

25 shows me the Figure 16. 01:09:45

1	So I could bring up a text version	01:09:53
2	on -- of the patent just by going to	01:09:57
3	Google Patents, but I don't want to go to another	01:10:02
4	reference unless that works for you.	01:10:07
5	Q. It does. I'm happy to have you use	01:10:13
6	Google Patents. I want you to just use it as a	01:10:15
7	tool and then direct to me where it shows up in	01:10:18
8	the column and line. That was 1001, but I get	01:10:21
9	your point about text searching. So --	01:10:26
10	A. "1130" pops all over -- well, not all	01:10:34
11	over but quite a few locations. I'm kind of	01:10:39
12	shocked that the searching fails.	01:10:43
13	Q. For what it's worth, when I search	01:10:47
14	"1130" in my version of Exhibit 1001, I get 11	01:10:48
15	hits. So I don't know if you're using a	01:10:56
16	different version of the patent. But, you know,	01:10:58
17	in the chat I think I sent you Exhibit 1001. I	01:11:00
18	can send it again if you'd like.	01:11:04
19	A. Are you looking at -- for the '054 or	01:11:06
20	the '918?	01:11:09
21	Q. '918.	01:11:11
22	A. So am I. "1130." I get nothing.	01:11:13
23	Other than -- well, I get nothing.	01:11:20
24	Q. I'll send it to you again. It's not	01:11:27
25	critical. We'll deal with it, but I don't want	01:11:31

1 you to be frustrated with the search 01:11:34
2 capabilities. 01:11:36
3 A. It gives me the same thing. It may be 01:12:20
4 the Adobe Acrobat as opposed to the Macintosh 01:12:23
5 default reader. 01:12:27
6 Some very strange reason, Acrobat finds 01:12:29
7 everything just fine. So -- I've never seen that 01:12:57
8 behavior before, but I'll go forward with it. 01:13:00
9 Q. Okay. Do you recall thinking about 01:13:03
10 what 1130 does, or are you indicating to me that 01:13:05
11 you would need to read it in the first instance 01:13:10
12 now? 01:13:14
13 A. Well, I just want to read it and review 01:13:15
14 my -- my recollection. It's not -- doesn't 01:13:17
15 appear to be a long stretch, a couple of 01:13:20
16 paragraphs. Does that make sense? 01:13:22
17 Q. Maybe we'll come back to 1130. Let me 01:13:30
18 keep going. And if you feel like we need to come 01:13:33
19 back to 1130 to answer a later question, let me 01:13:36
20 know. Fair enough? 01:13:39
21 A. Sure. 01:13:41
22 Q. What's a dual buck converter? 01:13:41
23 A. A dual buck converter is a buck 01:13:46
24 converter that produces two different output 01:13:50
25 voltages. 01:13:55

1	Q. And do you see Claim 2 of the '918	01:13:55
2	patent indicates that two buck converters can	01:13:59
3	operate as a dual buck converter; correct?	01:14:01
4	A. Yes, that's my recollection. Yep.	01:14:07
5	Q. So how do two buck converters operate	01:14:09
6	as a dual buck converter?	01:14:13
7	A. They provide two separate voltage	01:14:19
8	outputs.	01:14:22
9	Q. What's the difference between two buck	01:14:26
10	converters that are separate from each other and	01:14:29
11	two buck converters operating as a dual buck	01:14:31
12	converter?	01:14:34
13	A. Well, in this case, it provides better	01:14:41
14	isolation on the output.	01:14:46
15	Q. And when you state "in this case," what	01:14:50
16	case are you referring to?	01:14:53
17	A. The dual buck converter configuration.	01:14:54
18	Q. And can you explain it a little bit	01:14:58
19	more, your answer. "It provides better	01:15:04
20	isolation."	01:15:07
21	What's "it," and what do you mean by	01:15:08
22	"better isolation"?	01:15:11
23	A. This configuration provides better	01:15:13
24	isolation between the two output voltages. My	01:15:14
25	recollection is there's also an opportunity to	01:15:21

1 save some components. 01:15:23

2 Q. And what's the opportunity to save 01:15:26
3 components with a dual buck converter that you're 01:15:31
4 referring to? 01:15:33

5 A. That's just my recollection. It wasn't 01:15:36
6 an essential part of my analysis, so -- that's my 01:15:38
7 recollection. But I don't recall the details to 01:15:40
8 go into it further. 01:15:43

9 Q. So big picture, what are the benefits 01:15:47
10 of a dual buck converter versus two separate buck 01:15:48
11 converters? 01:15:51

12 A. Depends on the specific design. Don't 01:15:55
13 have a general opinion to state that would apply 01:15:58
14 to both. 01:16:03

15 Q. Were dual buck converters known before 01:16:06
16 the '918 and '054 patents? 01:16:07

17 A. Sure. I don't believe the inventor 01:16:14
18 took the position that they invented the concept. 01:16:19

19 Q. If you're using a dual buck converter, 01:16:22
20 can you turn off one of the two buck converters 01:16:24
21 while continuing to use the other buck converter? 01:16:26

22 A. Possibly. It depends on the specific 01:16:34
23 design. 01:16:36

24 Q. If two buck converters can operate as a 01:16:38
25 dual buck converter, is it possible for three 01:16:41

1 buck converters to operate as a triple buck 01:16:44
2 converter? 01:16:47
3 A. Haven't considered the question. 01:16:50
4 Q. And would your answer be the same for 01:16:54
5 whether four buck converters can operate as a 01:17:01
6 quad buck converter? 01:17:03
7 A. Yes. I've run into the basic concept 01:17:07
8 of dual buck converters in the past. I haven't 01:17:11
9 run across the concept of a triple or a quad, but 01:17:16
10 that doesn't mean that people haven't used such 01:17:20
11 structures in the past. 01:17:24
12 (Exhibit Number 1048 was previously 01:17:25
13 marked for identification.) 01:17:25
14 BY ATTORNEY CHANDLER: 01:17:29
15 Q. Could you pull up Exhibit 1048, and let 01:17:29
16 me know when you have it in front of you. And 01:17:35
17 for everyone's benefit, I will put it in the 01:17:39
18 chat. 01:17:42
19 Do you have Exhibit 1048? 01:18:02
20 A. I do. 01:18:05
21 Q. Exhibit 1048 is titled "DC-DC converter 01:18:10
22 specification for MPD4S014S"; correct? 01:18:16
23 A. Yes. That's correct. 01:18:29
24 Is this one of the prior art elements 01:18:32
25 that I testified to? Do you know? As I sit 01:18:33

1 here, I don't recall seeing this. 01:18:40

2 Q. Well, it's certainly one of the 01:18:43
3 exhibits Dr. Wolfe testified about, so you would 01:18:44
4 have seen it there. 01:18:49

5 A. Fair enough. 01:18:50

6 Q. And that -- I mean, it appears you cite 01:18:51
7 to it as well in your declaration. 01:18:56

8 A. Thank you. Okay. 01:18:59

9 Q. Could you go to page 2 of Exhibit 1048. 01:19:01
10 Let me know when you're there. 01:19:04

11 A. Yes, I'm there. 01:19:11

12 Q. Page 2 of Exhibit 1048 shows a block 01:19:11
13 diagram that's similar to the diagram we 01:19:14
14 discussed earlier on page 5 of Exhibit 1058, for 01:19:16
15 a buck converter; is that fair? 01:19:22

16 A. It has some elements that are similar 01:19:30
17 to it and some elements that are quite a bit 01:19:32
18 different. 01:19:34

19 Q. And that's what I wanted to ask you 01:19:35
20 about. 01:19:38

21 Does page 2 of Exhibit 1048 show a 01:19:41
22 circuit with two buck converters outputting two 01:19:46
23 regulated voltages labeled V-out1 and V-out2? 01:19:50

24 A. So it shows -- let's see. It does show 01:20:09
25 V-out1 and V-out2. And it shows a control 01:20:14

1 circuit controlling the -- controlling switches, 01:20:21
2 switching transistors, as I mentioned before. 01:20:26
3 Between V-in and the two V-outs, sure, 01:20:32
4 the basic architecture looks comparable. 01:20:39
5 Q. Comparable to the buck converter 01:20:47
6 circuit we discussed previously on page 5 of 01:20:49
7 Exhibit 1058; is that fair? 01:20:52
8 A. Yes, that's correct. 01:20:53
9 Q. And how many inductors are shown in the 01:20:56
10 circuit on page 2 of Exhibit 1048? 01:20:59
11 A. There are two inductors, illustrated in 01:21:03
12 the circuit, this block diagram on page 2. 01:21:06
13 Q. Does page 2 of Exhibit 1048 show two 01:21:13
14 buck converters operating as a dual buck 01:21:20
15 converter? 01:21:22
16 A. It does not label that as a dual buck 01:21:27
17 converter. In fact, it doesn't label it as a 01:21:29
18 buck converter, but it is indeed two buck 01:21:35
19 converters. 01:21:37
20 Q. With two regulated output voltages? 01:21:43
21 A. Pardon me? 01:21:52
22 Q. With two regulated output voltages; 01:21:54
23 correct? 01:21:56
24 A. Yes, that's correct. 01:21:59
25

1 (Exhibit Number 1062 was previously
2 marked for identification.)

3 BY ATTORNEY CHANDLER:

01:22:10

4 Q. Why don't you put that aside. And turn
5 to Exhibit 1062 and let me know when you have it.
6 And I'll also try to put it in the chat for you.

01:22:10

01:22:35

01:22:39

7 Do you have Exhibit 1062?

01:23:10

8 A. It has just downloaded. And I have it
9 open now.

01:23:12

01:23:17

10 Q. Exhibit 1062 in both IPRs is a
11 publication by "Analog Devices" named "Analog
12 Dialogue" dated 2006, as shown in the upper left
13 corner of the cover page; correct?

01:23:19

01:23:25

01:23:31

01:23:35

14 A. Yes, that's correct.

01:23:39

15 Q. Please go to page 13 of Exhibit 1062.
16 And probably the easiest thing to find what I
17 will be referring to is to search for the phrase
18 "Core" with a hyphen -- C-O-R-E hyphen. And let
19 me know when you have found that on page 13.

01:23:43

01:23:47

01:23:55

01:23:57

01:24:06

20 A. I have it.

01:24:07

21 Q. So page 13 of Exhibit 1062 states,
22 "Many high-performance ICs now require multiple
23 voltages. For example, separate core- and I/O
24 voltages are standard for many devices."

01:24:11

01:24:14

01:24:19

01:24:25

25 Did I read that accurately?

01:24:28

1 A. Yes, I did. 01:24:32

2 Q. What's the core voltage for a device 01:24:33
3 and what's the I/O voltage for a device? 01:24:36

4 A. There isn't necessarily a core voltage 01:24:41
5 or an I/O voltage. It's possible that they're 01:24:44
6 referring to devices that have a processor core 01:24:47
7 and some off-chip I/O. But there are many 01:24:54
8 high-performance ICs that don't have anything 01:24:59
9 that I would refer to as "core" in comparison to 01:25:02
10 I/O. 01:25:08

11 Q. In the situation where there is a core 01:25:16
12 voltage and a separate I/O voltage, why is that? 01:25:18

13 A. You're asking about a hypothetical 01:25:28
14 system that's not in play or consideration. 01:25:29
15 There -- in my review for these IPRs, there might 01:25:35
16 be many reasons for having them separate. There 01:25:42
17 would be many reasons for having them combined. 01:25:47
18 It depends on the details of the design goals 01:25:50
19 that the engineers are trying to match to meet. 01:25:52

20 Q. So this statement on page 13 of 01:26:00
21 Exhibit 1062 that we just looked at indicates 01:26:05
22 that it's standard for many devices to have 01:26:09
23 separate core and I/O voltages. 01:26:15

24 Do you agree with that? 01:26:18

25 A. I don't know. I don't have an opinion 01:26:26

1 on that one way or another.

01:26:28

2 It's likely that the vast majority of
3 high-performance -- I guess I'm inclined to
4 disagree with it. The vast majority of
5 high-performance integrated systems -- for
6 example, in computers of the sort that I think we
7 are talking about -- would not have cores within
8 them.

01:26:31

01:26:38

01:26:40

01:26:43

01:26:45

01:26:49

01:26:55

9 Q. Do you agree that many high-performance
10 integrated circuits at the time required multiple
11 voltages?

01:27:02

01:27:04

01:27:09

12 A. Many high-performance integrated
13 circuits at the time would make use of multiple
14 voltages, assuming we're talking about voltages
15 being introduced from the outside.

01:27:15

01:27:18

01:27:21

01:27:27

16 However, many high-performance
17 integrated circuits that required multiple
18 voltages, internal, were able to generate them
19 from a single external voltage source. There's a
20 wide range of design options.

01:27:29

01:27:32

01:27:35

01:27:38

01:27:43

21 Q. Turn to page 14 of Exhibit 1062. Let
22 me know when you're there.

01:27:48

01:27:52

23 A. Okay, I'm there.

01:27:57

24 Q. The top of page 14 of Exhibit 1062
25 states, "Figure 2 shows how basic sequencing can

01:27:59

01:28:03

1 be implemented with discrete components." 01:28:08
2 Correct? 01:28:13
3 A. Yes. Figure 2 shows "Basic discrete 01:28:20
4 sequencing for a four-supply system." 01:28:24
5 Q. And that paragraph goes on to refer to 01:28:28
6 a resister capacity (RC) combination; correct? 01:28:31
7 A. Yes. 01:28:40
8 Q. What is a resister capacitor (RC) 01:28:41
9 combination? 01:28:46
10 A. It's a combination of a resister and a 01:28:46
11 capacitor. 01:28:48
12 Q. What does that do? 01:28:50
13 A. It depends on how exactly it's 01:28:51
14 configured and what the various capabilities -- 01:28:53
15 the -- what's the term I'm looking for? -- the 01:28:59
16 specific resisters and capacitors that are in 01:29:03
17 use. 01:29:06
18 In this situation, they're using it, 01:29:09
19 they say, to slowly ramp the gate voltage of the 01:29:12
20 end channel FET, F-E-T, in series with the 5-volt 01:29:16
21 supply. 01:29:26
22 Q. And Figure 2 shows LDO linear 01:29:28
23 regulators being used; correct? 01:29:36
24 A. Figure 2 shows two blocks that are 01:29:40
25 labeled ADP3330 LDO, and ADP3333 LDO. 01:29:43

1 Q. And those are described in the 01:29:55
2 paragraph above as low dropout (LDO) regulators; 01:29:56
3 correct? 01:30:03

4 A. That's correct. 01:30:03

5 Q. And those would be an example of what 01:30:04
6 we were discussing earlier with respect to LDO 01:30:09
7 linear regulators; would that be fair? 01:30:15

8 A. I believe that they are, yes, LDO 01:30:18
9 linear regulators. 01:30:21

10 Q. The next paragraph on page 14 of 01:30:27
11 Exhibit 1062 states: 01:30:29

12 "This simple, low-cost approach to 01:30:32
13 sequencing power supplies uses little 01:30:34
14 board area and is perfectly acceptable 01:30:37
15 in many applications. It is suitable 01:30:39
16 for systems where cost is the primary 01:30:41
17 driver, the sequencing requirements are 01:30:44
18 simple, and the accuracy of the 01:30:47
19 sequencing circuit is not critical." 01:30:49

20 Did I read that accurately? 01:30:51

21 A. Yes, I believe you did. 01:30:57

22 Q. And then the following paragraph of 01:30:59
23 page 14 of Exhibit 1062 states: 01:31:00

24 "But many situations require more 01:31:04
25 accuracy than is available with RC lag 01:31:07

1 circuits. In addition, this simple 01:31:12
2 solution does not permit faults to be 01:31:15
3 dealt with in a structured way (e.g., a 01:31:17
4 5-volt supply failure will eventually 01:31:21
5 bring down the other rails)."
6 Did I read that accurately? 01:31:27
7 A. Yes, you did. 01:31:30
8 Q. And then if we turn to page 15 of 01:31:33
9 Exhibit 1062. Let me know when you're there. 01:31:37
10 A. I'm there. 01:31:46
11 Q. In the second paragraph on the top left 01:31:46
12 side of page 15 of Exhibit 1062, it states: 01:31:48
13 "In systems with four or more 01:31:54
14 voltages, it may make sense to use a 01:31:57
15 centralized device to manage the power 01:32:00
16 supplies. An example of this approach 01:32:03
17 can be seen in Figure 4."
18 Did I read that accurately? 01:32:07
19 A. Yes, you did. 01:32:09
20 Q. Are the statements that I just read on 01:32:11
21 pages 14 and 15 of Exhibit 1062, are those 01:32:13
22 consistent with your general understanding of 01:32:17
23 power supplies? 01:32:23
24 A. Yeah, they're not inconsistent. Of 01:32:26
25 course, there are a number of qualifications in 01:32:28

1	the language directly. These are examples that,	01:32:30
2	as it says, may make sense.	01:32:35
3	Q. And at the top of page 15 of	01:32:47
4	Exhibit 1062, do you see there's a gray box for	01:32:50
5	circuit labeled ADP1821?	01:32:54
6	A. Yes, I see that.	01:32:58
7	Q. ADP1821 is not an LDO layer regulator;	01:33:07
8	correct?	01:33:12
9	A. I don't recall. It would appear not to	01:33:16
10	be, but I don't recall.	01:33:19
11	Q. That top circuit labeled ADP1821 takes	01:33:25
12	an input of 12 volts and steps it down to an	01:33:28
13	output of 3.3 volts; is that correct?	01:33:31
14	A. That is how it's labeled.	01:33:35
15	Q. And then below that is a second circuit	01:33:38
16	in gray labeled ADP1821 that takes an input of	01:33:43
17	12 volts and steps it down to an output of	01:33:47
18	2.5 volts; correct?	01:33:50
19	A. Yes, that's correct.	01:33:57
20	Q. And that circuit is not indicated as	01:33:57
21	being an LDO linear regulator; correct?	01:34:02
22	A. Not in this figure. I don't recall	01:34:09
23	anything more specific about the 1821 circuits.	01:34:11
24	Q. And then there's a third circuit in	01:34:16
25	gray labeled ADP1821 that takes an input voltage	01:34:20

1 of 12 volts and steps it down to an output of 01:34:24
2 0.9 volts; correct? 01:34:28
3 A. Yes, that is what the figure shows. 01:34:33
4 Q. And that circuit is also not indicated 01:34:34
5 as being an LDO linear regulator; correct? 01:34:40
6 A. I think that's correct. It's shown as 01:34:46
7 a DC-to-CD converter, but it's not labeled as an 01:34:49
8 LDO or a buck converter or anything more. 01:34:54
9 Q. And I think you mentioned it 01:35:12
10 previously, but if you could briefly explain it 01:35:14
11 to me, since I'm not an expert in the field, 01:35:22
12 what's the relationship between a switching 01:35:23
13 regulator and a buck converter? 01:35:25
14 A. A buck converter is an example -- is an 01:35:27
15 instance of a switching regulator. 01:35:29
16 Q. And is the -- the distinction that a 01:35:33
17 switching regulator could either increase the 01:35:36
18 voltage or decrease the voltage, but a buck 01:35:39
19 converter requires decreasing the voltage? 01:35:42
20 A. It depends on the particular switching 01:35:46
21 regulator you build. But, in general, I don't 01:35:51
22 think that's clearly a wrong distinction. 01:35:56
23 So, for example, a buck boost converter 01:35:58
24 does boost the voltage, and it is also a 01:36:01
25 switching regulator. 01:36:03

1 Q. Is ADP1821 a switching regulator that 01:36:07
2 is shown in -- on this page to be acting like a 01:36:13
3 buck converter in that the output voltage is 01:36:22
4 lower than the input voltage? 01:36:25

5 A. Well, it does show that the output 01:36:30
6 voltage is less than the input voltage, but that 01:36:35
7 element is consistent with an LDO as well. I was 01:36:36
8 trying to find a description of what 1821 was 01:36:41
9 further than that, and wasn't finding much. 01:36:43

10 ATTORNEY CHANDLER: Let me mark a new 01:36:53
11 exhibit. It will be Exhibit 1078. I'll put it 01:36:55
12 in the chat. 01:36:58

13 And as I did before, I'm going to mark 01:37:02
14 it in both IPRs, so I'm sending you two versions 01:37:04
15 of it. It's the same document. The only 01:37:06
16 difference is the stamp in the bottom right is 01:37:09
17 different to reflect the two different IPR 01:37:12
18 numbers. 01:37:15

19 So let me know when you've got 01:37:16
20 Exhibit 1078 in front of you. 01:37:17

21 (Whereupon, Exhibit Number 1078 was
22 marked for identification in both
23 IPR cases and are attached hereto.)

24 THE WITNESS: I have the '918 version 01:37:26
25 available in front of me. 01:37:29

1 BY ATTORNEY CHANDLER: 01:37:30

2 Q. Exhibit 1078 is the data sheet for the 01:37:31

3 ADP1821 step down DC-to-DC controller; correct? 01:37:36

4 A. Yes. 01:37:42

5 Q. And in the bottom left of the cover 01:37:45

6 page of Exhibit 1078, does that show the ADP1821 01:37:50

7 being used? 01:37:56

8 ATTORNEY LINDSAY: Objection -- sorry, 01:38:02

9 I thought you were done. 01:38:05

10 BY ATTORNEY CHANDLER: 01:38:09

11 Q. Does the bottom left of the cover page 01:38:09

12 of Exhibit 1078 show that ADP1821 being used in a 01:38:11

13 way that would be consistent with a buck 01:38:17

14 converter? 01:38:20

15 ATTORNEY LINDSAY: Objection; outside 01:38:22

16 the scope of direct. 01:38:22

17 THE WITNESS: Yeah, I don't recall 01:38:29

18 reviewing this particular part of this document. 01:38:30

19 It does appear that there are structural elements 01:38:33

20 that are in common with a much simpler buck 01:38:39

21 converter circuitry that we've seen previously. 01:38:45

22 BY ATTORNEY CHANDLER: 01:38:47

23 Q. And in the upper right of the cover 01:38:48

24 page of Exhibit 1078, under "General Description" 01:38:50

25 it states, "The ADP1821 is a versatile and 01:38:54

1	inexpensive synchronous pulse width moderated	01:38:59
2	(PWM) voltage-mode step down controller."	01:39:03
3	Did I read that accurately?	01:39:08
4	A. Yeah.	01:39:10
5	ATTORNEY LINDSAY: Objection; outside	01:39:11
6	the scope of direct.	01:39:11
7	BY ATTORNEY CHANDLER:	01:39:16
8	Q. Could you say your answer again,	01:39:16
9	please, Dr. Mangione-Smith.	01:39:18
10	A. Yes, you read that accurately.	01:39:20
11	Q. And would that general description be	01:39:21
12	consistent with a buck converter?	01:39:24
13	ATTORNEY LINDSAY: Objection; outside	01:39:27
14	the scope of direct.	01:39:27
15	THE WITNESS: No.	01:39:38
16	BY ATTORNEY CHANDLER:	01:39:39
17	Q. In particular, the controller that can	01:39:39
18	be used for a buck converter; correct?	01:39:42
19	ATTORNEY LINDSAY: Objection; outside	01:39:47
20	the scope of direct, form.	01:39:47
21	THE WITNESS: Yeah, it's not	01:39:50
22	inconsistent with the controller that could be	01:39:52
23	used with a buck converter, I would agree with	01:39:53
24	that.	01:39:58
25		

1 BY ATTORNEY CHANDLER:

01:40:10

2 Q. And on page 1 of Exhibit 1078, in the
3 third paragraph under "General Description," it
4 states, "The ADP1821 operates as a
5 pin-selectable, fixed switching frequency of
6 either 300 kilohertz or 600 kilohertz, minimizing
7 external component size and cost."

01:40:10

01:40:17

01:40:20

01:40:23

01:40:28

01:40:35

8 Did I read that accurately?

01:40:36

9 ATTORNEY LINDSAY: Objection; outside
10 the scope of direct.

01:40:38

01:40:38

11 THE WITNESS: You did. Yes, you read
12 that accurately.

01:40:40

01:40:42

13 BY ATTORNEY CHANDLER:

01:40:43

14 Q. So would it be fair to say that ADP1821
15 can be a switching controller, which would be
16 consistent with use in a buck converter?

01:40:47

01:40:53

01:40:58

17 ATTORNEY LINDSAY: Objection; outside
18 the scope of direct.

01:41:03

01:41:03

19 THE WITNESS: It's indicating that it
20 operates at two different switching frequencies;
21 and it indicates in that figure that it can be
22 used in a context of what I believe is a buck
23 converter. So -- yeah.

01:41:08

01:41:11

01:41:17

01:41:23

01:41:28

24

25

1 (Exhibit Number 2032 was previously
2 marked for identification.)

3 BY ATTORNEY CHANDLER:

4 Q. You can put that aside. Let me show
5 you a different example, Exhibit 2032. I'll put
6 it in the chat for ease of reference. Let me
7 know when you have it.

8 A. All right. I have it opened in front
9 of me.

10 Q. Exhibit 2032 in both IPRs is the Claim
11 Construction Order in the Eastern District of
12 Texas Civil Action 2:21-CV-00463 filed
13 December 14th, 2022, as shown in the top of the
14 first page of that exhibit; correct?

15 A. Yes, sir, I see that.

16 Q. Please turn to page 34 of Exhibit 2032.
17 Let me know when you're there.

18 A. I'm sorry. Which page?

19 Q. 34, second-to-last.

20 A. Okay.

21 Q. Pages 34 and 35 of Exhibit 2032 provide
22 the claim constructions adopted by the Court in
23 the Eastern District of Texas for several claim
24 terms in the '918 and '054 patents; correct?

25 A. Yes.

1	Q. Do you disagree with any of the claim	01:43:20
2	constructions adopted by the Court in the Eastern	01:43:22
3	District of Texas for the '918 and '054 patents?	01:43:25
4	A. No, I don't.	01:43:34
5	Q. In your opinion, are any of the claim	01:43:35
6	constructions adopted by the Court in the Eastern	01:43:38
7	District of Texas for the '918 and '054 patents	01:43:41
8	either too broad or too narrow?	01:43:46
9	A. I don't have an opinion on this. I	01:43:52
10	don't disagree with them, and for the most part,	01:43:55
11	I haven't considered whether or not they might	01:43:59
12	have benefited from some refinement in one	01:44:01
13	direction or the other.	01:44:06
14	Q. Do you believe that the board, in these	01:44:11
15	two IPRs proceedings, should change any of the	01:44:13
16	claim constructions adopted by the Court in the	01:44:17
17	Eastern District of Texas for the '918 and '054	01:44:20
18	patents?	01:44:22
19	ATTORNEY LINDSAY: Objection; calls for	01:44:24
20	legal reasoning.	01:44:27
21	THE WITNESS: Yeah, I don't have an	01:44:28
22	opinion on that. I'm not providing advice that,	01:44:29
23	in my opinion, one or more of the constructions	01:44:35
24	is wrong.	01:44:37
25	It's my understanding, not being a	01:44:42

1	lawyer, that constructions of this nature are	01:44:44
2	oftentimes useful evidence for the board to	01:44:48
3	consider; but I don't even know -- I don't think	01:44:50
4	it's controlling, but I'm not sure of that.	01:44:55
5	BY ATTORNEY CHANDLER:	01:44:59
6	Q. And to be clear, I'm not trying to ask	01:44:59
7	you for a legal opinion of, you know, whether	01:45:01
8	it's controlling or not controlling.	01:45:04
9	What I'm trying to get at is, from your	01:45:06
10	technical standpoint, whether there's anything	01:45:09
11	from a technical standpoint that you think the	01:45:12
12	board ought to change with respect to any of the	01:45:14
13	claim constructions adopted by the Court in the	01:45:19
14	Eastern District of Texas for the '918 and '054	01:45:22
15	patents, given the issues presented in these two	01:45:25
16	IPRs?	01:45:30
17	A. No. I don't have an opinion or advice	01:45:36
18	along those lines for the board.	01:45:39
19	Q. I'd like to ask you about the meaning	01:45:44
20	of a claim term that was not construed by the	01:45:46
21	Court in the Eastern District of Texas, okay?	01:45:50
22	Understood that I'm moving on to a slightly	01:45:57
23	different topic now?	01:46:00
24	A. Yes.	01:46:03
25	Q. In Claim 1 of the '918 patent there is	01:46:06

1 the claim term "converter circuit"; correct? 01:46:08

2 A. Yes. Let me reorient and get that in 01:46:14
3 front of me. 01:46:18

4 Q. And the way the claim is structured is, 01:46:19
5 there's a paragraph for the first buck converter, 01:46:21
6 and then second buck converter, and then third 01:46:24
7 buck converter, and then there's the claim term 01:46:28
8 "converter circuit." 01:46:31

9 Do you see that claim language in 01:46:32
10 Claim 1 of the '918 patent? 01:46:34

11 A. No, I don't. Obviously -- just give me 01:46:51
12 a moment to find the file. 01:46:54

13 Q. I think you had it open in Acrobat, was 01:47:09
14 my recollection. 01:47:11

15 A. That's probably what happened, and then 01:47:12
16 I closed it in Preview, which is what I normally 01:47:13
17 go to. 01:47:17

18 Yes, okay. I've got it now. Thank 01:47:18
19 you. 01:47:19

20 Q. All right. In Column 38 of the '918 01:47:19
21 patent, it shows Claim 1, and there's sort of 01:47:22
22 paragraphs or indentations, and you see that 01:47:26
23 there's a first buck converter, and then there's 01:47:29
24 a second buck converter, and there's a third buck 01:47:31
25 converter; and then there is a converter circuit. 01:47:33

1	A. Yes.	01:47:38
2	Q. In your opinion, does the claim	01:47:41
3	language "converter circuit" in the claims of the	01:47:41
4	'918 patent require a buck converter?	01:47:46
5	A. No.	01:47:52
6	Q. In your opinion, can a linear regulator	01:47:53
7	satisfy the claim language "converter circuit" in	01:47:57
8	the claims of the '918 patent?	01:48:00
9	A. A linear regulator by virtue of	01:48:06
10	converting from an unregulated to a regulated	01:48:09
11	voltage is, in fact, a converter circuit.	01:48:14
12	Q. So in your opinion, an LDO linear	01:48:19
13	regulator can satisfy the claim language	01:48:24
14	"converter circuit" in the claims of the '918	01:48:26
15	patent?	01:48:30
16	A. Yes, that's right.	01:48:33
17	Q. All right. I want to talk now about	01:48:43
18	Figure 12 of the '918 and '054 patents. It's	01:48:48
19	shown in paragraph 19 of your expert declaration,	01:48:53
20	so you're welcome to look there, if you would	01:48:57
21	like to see Figure 12. Actually, it's probably	01:49:00
22	easiest if you just go there because you've got	01:49:06
23	some description of Figure 12 that may be	01:49:08
24	helpful. So why don't you turn to paragraph 19	01:49:11
25	of your expert declarations. Let me know when	01:49:14

1	you're there.	01:49:16
2	A. Okay, I'm there.	01:49:23
3	Q. And I believe your discussion in	01:49:24
4	paragraph 19 is materially the same in both of	01:49:27
5	your expert declarations, so I'll sort of cover	01:49:30
6	both expert declarations at the same time on this	01:49:35
7	point, if that's all right with you.	01:49:37
8	A. That's all right with me.	01:49:40
9	Q. Is Figure 12 of the '918 and '054	01:49:47
10	patents an embodiment of the claims of the '918	01:49:48
11	and '054 patents?	01:49:53
12	A. It may be. It depends. I haven't	01:49:59
13	looked to see if it's an embodiment -- it's an	01:50:02
14	embodiment of the inventions that the inventors	01:50:07
15	believe that they created. I haven't looked to	01:50:10
16	see if it constitutes an embodiment of any	01:50:15
17	particular claim, let alone all of them.	01:50:17
18	Q. In figure 12 of the '918 and '054	01:50:22
19	patents, there is a controller 1062 sort of on	01:50:23
20	the left-hand side shown with dashed lines that	01:50:30
21	go around FPGA 1070 and microcontroller unit	01:50:34
22	1060; correct?	01:50:41
23	A. Yes; is that correct.	01:50:48
24	Q. And you explain in paragraph 19 of your	01:50:49
25	expert declarations that it's also possible that	01:50:51

1	FPGA 1070 may be integrated with the	01:50:57
2	microcontroller 1060; correct?	01:50:59
3	A. Yes.	01:51:06
4	Q. And you explain that the	01:51:06
5	microcontroller 1060 provides memory management	01:51:06
6	and controls the data transfer between the	01:51:10
7	nonvolatile memory 1040, shown in the upper left	01:51:14
8	of Figure 12, and the volatile memory 1030, shown	01:51:18
9	in the upper right of Figure 12; correct?	01:51:22
10	A. Yes, you read that correctly.	01:51:29
11	Q. And you go on to explain that the FPGA	01:51:35
12	logic element 1070 provides some signal level	01:51:38
13	translation and address translation between the	01:51:42
14	volatile memory and the nonvolatile memory;	01:51:45
15	correct?	01:51:47
16	A. Yes, that's correct.	01:51:49
17	Q. And then you go on to explain that the	01:51:53
18	volatile memory can be 1.8 volts and the	01:51:55
19	nonvolatile memory can be 3 volts; correct?	01:51:59
20	A. Yes, that's correct.	01:52:02
21	Q. And when you say that the FPGA logic	01:52:11
22	element 1070 provides signal-level translation	01:52:13
23	between the volatile memory and the nonvolatile	01:52:16
24	memory, what do you mean by "signal-level	01:52:18
25	translation?	01:52:22

1 A. At a minimum, it's going to provide 01:52:25
2 voltage translation between the two. 01:52:28
3 Q. And what do you mean by "voltage 01:52:32
4 translation"? 01:52:35
5 A. Well, as you just discussed, one 01:52:35
6 example would be the SDRAM's operating at 01:52:42
7 1.8 volts and the NAND flash operating at 01:52:49
8 3 volts. 01:52:53
9 Q. And can you explain it a little bit 01:52:57
10 more. So I get that they're two voltages, but 01:52:59
11 then what does the final logic element 1070 do as 01:53:03
12 part of signal level translation? 01:53:07
13 A. It operates at one point -- interfaces 01:53:10
14 between the 1.8-volt side of the system and the 01:53:15
15 3-volt side of the system. 01:53:18
16 Q. So the FPGA 1070 would have one 01:53:30
17 interface at 1.8 volts for the volatile memory in 01:53:35
18 the upper right of Figure 12, marked as 1030; and 01:53:42
19 then it would have a second interface operating 01:53:45
20 at 3 volts for the nonvolatile memory, in the 01:53:47
21 upper left of Figure 12, marked as 1040; is that 01:53:53
22 fair? 01:53:58
23 A. That's what I'm suggesting, that this 01:54:00
24 embodiment could support such a design. 01:54:02
25 On the other hand, it could be the case 01:54:05

1 that the MCU 1060 is also operating at 3 volts, 01:54:06
2 in which case that voltage level translation 01:54:15
3 wouldn't necessarily need to be done by the FPGA. 01:54:18

4 Q. But in at least one embodiment, the 01:54:27
5 logic element 1070 -- the FPGA would provide the 01:54:28
6 voltage translation; is that fair? 01:54:33

7 A. I believe that that's -- that matches 01:54:38
8 my recollection of what the patent discloses, 01:54:40
9 yeah. 01:54:42

10 (Simultaneous cross-talk.) 01:54:47

11 (Clarification by reporter.) 01:54:54

12 BY ATTORNEY CHANDLER: 01:54:54

13 Q. Sorry. My question was: That's what 01:54:55
14 you quote; correct? 01:54:57

15 And I could make it a better question, 01:55:01
16 which is: At the bottom of page 8 of your 01:55:03
17 declaration, you quote from the patent where it 01:55:09
18 states, that the logic element 1070, which is the 01:55:13
19 FPGA, can provide signal-level translation 01:55:17
20 between the volatile memory, and that's what is 01:55:21
21 1.8 volts, and the nonvolatile memory, which 01:55:26
22 could be 3 volts; correct? 01:55:31

23 A. Yes. It provides that that's an 01:55:33
24 example of what it can do. 01:55:35

25 Q. Please turn to Exhibit 1027. Let me 01:55:38

1 know when you're there.

01:55:41

2 A. Okay.

01:55:56

3 Q. Exhibit 1027 we've looked at before.

01:55:57

4 But this, just to be sure we're on the same page,

01:55:59

5 is the JESD82-20 JEDEC standard for FBDIMM

01:56:03

6 advanced memory buffer dated March 2007; correct?

01:56:09

7 A. Yes, that's correct.

01:56:15

8 Q. Please turn to page 1 of Exhibit 1027,

01:56:16

9 as shown in the bottom right stamp. It's, I

01:56:19

10 believe, the 13th page of the PDF file. Let me

01:56:25

11 know when you're there.

01:56:29

12 A. I am there now.

01:56:31

13 Q. Section 1.1 of Exhibit 1027 states that

01:56:33

14 the AMB on an FBDIMM, quote, supports DDR2 SDRAM

01:56:37

15 main memory, end quote; correct?

01:56:47

16 A. Yes.

01:56:55

17 Q. And DDR2 SDRAM main memory is what we

01:56:55

18 discussed in Exhibit 1026, the JEDEC standard

01:57:01

19 JSD79-2B; is that fair?

01:57:10

20 A. We did discuss the JEDEC standard

01:57:15

21 previously. I don't remember which exhibit it

01:57:19

22 is, but I'm happy to assume that that's the

01:57:21

23 correct reference.

01:57:25

24 Q. So in other words, if FB did not use

01:57:29

25 memory devices that are unique to FBDIMMs, it

01:57:33

1	uses the same DDR2 SDRAM memory that can be used	01:57:36
2	on other types of DIMM memory modules; correct?	01:57:42
3	ATTORNEY LINDSAY: Objection; form.	01:57:46
4	THE WITNESS: It does say it supports	01:57:51
5	DDR2 SDRAM main memory, yes.	01:57:53
6	BY ATTORNEY CHANDLER:	01:57:56
7	Q. And that's a JEDEC standard type of	01:57:56
8	memory that can be used on different types of	01:57:59
9	DIMM memory modules, it's not limited to FBDIMMs;	01:58:03
10	correct? For example, we looked at, I guess, an	01:58:08
11	RDIMM standard for DDR2 and an SODIMM memory	01:58:12
12	module for DDR2; correct?	01:58:16
13	A. Yes, that's correct.	01:58:20
14	Q. Section 1.1 of Exhibit 1027 states, on	01:58:27
15	the third line, that, quote:	01:58:30
16	"All memory control for the DRAM	01:58:34
17	resides in the host, including memory	01:58:37
18	request initiation, timing, refresh,	01:58:42
19	scrubbing, sparing, configuration	01:58:45
20	access, and power management."	01:58:49
21	Did I read that accurately?	01:58:53
22	A. Yes, it says that.	01:58:55
23	Q. So when you have an FBDIMM memory	01:59:07
24	module, it is the host computer that maintains	01:59:09
25	the ultimate control over the DDR2 SDRAM memory	01:59:18

1	devices on the memory module; is that fair?	01:59:24
2	A. I wouldn't say that.	01:59:30
3	Q. The memory control for the DDR2 SDRAM	01:59:38
4	memory devices on an FBDIMM resides in the host	01:59:42
5	computer; correct?	01:59:46
6	A. I wouldn't agree with that.	01:59:51
7	Q. Isn't that what we just read?	01:59:52
8	A. Yes.	01:59:54
9	Q. All -- all memory control for the DRAM	01:59:54
10	resides in the host?	01:59:58
11	A. Yes, that is what we just read.	02:00:02
12	Q. And to be clear, are you agreeing with	02:00:04
13	that statement or disagreeing with that	02:00:06
14	statement?	02:00:07
15	A. I'm disagreeing with that statement.	02:00:09
16	Q. Okay. So in forming your opinions in	02:00:10
17	this matter, you did not agree with the	02:00:14
18	statement, on the third line of Section 1.1 of	02:00:19
19	Exhibit 1027; is that fair?	02:00:23
20	A. No, I wouldn't say that.	02:00:26
21	Q. But to be clear, you disagree with the	02:00:38
22	statement that all memory control for the DRAM	02:00:39
23	resides in the host?	02:00:44
24	A. Yes, that's correct.	02:00:46
25	Q. You think that's a typo in	02:00:51

1	Exhibit 1027?	02:00:53
2	A. I have no idea.	02:00:55
3	Q. Page 1 of Exhibit 1027 in the middle of	02:01:01
4	Section 1.2.1, do you see there's the bullet	02:01:05
5	point that begins with the word "Acts"?	02:01:17
6	A. Yes.	02:01:19
7	Q. So page 1 of Exhibit 1027 in the middle	02:01:22
8	of Section 1.2.1 states that "The AMB on an	02:01:25
9	FBDIMM, quote, acts as DRAM memory buffer for all	02:01:32
10	read, write and configuration accesses addressed	02:01:38
11	to the DIMM," end quote; correct?	02:01:42
12	A. Yes, I see that.	02:01:48
13	Q. So would it be fair to say that if you	02:01:51
14	have an FBDIMM, the host computer can send read	02:01:52
15	and write commands to the AMB on the FBDIMM?	02:01:56
16	A. So I would generally be a little bit	02:02:14
17	more precise and say the memory controller on the	02:02:16
18	host.	02:02:21
19	But, sure, if the typical memory	02:02:21
20	controller is configured -- if a reference to the	02:02:24
21	host computer is meant to include that, then yes,	02:02:28
22	that memory controller sends read and write and	02:02:31
23	configuration access addresses to the DIMM.	02:02:35
24	Q. So going back to the sentence that we	02:02:41
25	were discussing a moment ago that you disagreed	02:02:45

1 with, where Section 1.1 of Exhibit 1027 states 02:02:48
2 that "All memory control for the DRAM resides in 02:02:54
3 the host," would you agree with that statement if 02:02:58
4 it were clarified to be that all memory control 02:03:03
5 for the DRAM resides in the memory controller in 02:03:06
6 the host? 02:03:12

7 A. No, I would not. 02:03:13

8 Q. When a memory controller in the host 02:03:19
9 sends a read and write commands to the AMB on the 02:03:21
10 FBDIMM, would those read and write commands 02:03:25
11 include address information for the read and 02:03:33
12 write commands? 02:03:35

13 A. They would typically include address 02:03:42
14 information for the read and write commands. 02:03:44

15 Q. If you turn to paragraph 31 of your 02:03:46
16 expert declaration -- and again, I believe it's 02:03:48
17 the same in both, so I'll just refer to 02:03:53
18 paragraph 31 generically to refer to both of your 02:03:57
19 expert declarations. And let me know when you're 02:04:00
20 there. 02:04:01

21 A. I'm there. 02:04:06

22 Q. In paragraph 31 of your expert 02:04:23
23 declaration you state in the first sentence that 02:04:24
24 an "FBDIMM uses packetized serial signaling to 02:04:27
25 exchange data, address and control information 02:04:32

1	with the host."	02:04:33
2	Correct?	02:04:35
3	A. Yes, you read that accurately.	02:04:37
4	Q. So when the host computer wants to send	02:04:40
5	a read or write command to an FBDIMM, that read	02:04:43
6	or write command and the associated address	02:04:47
7	information is sent as packetized serial signals;	02:04:50
8	correct?	02:04:56
9	A. Yes, that's correct.	02:04:57
10	Q. And similarly, when the host computer	02:05:01
11	wants to send data to an FBDIMM that data is sent	02:05:03
12	as packetized serial signals; correct?	02:05:08
13	A. Yes, that's correct.	02:05:15
14	Q. And then in the fourth line of	02:05:16
15	paragraph 31 of your declarations, you explain	02:05:20
16	that the AMB on the FBDIMM receives the data	02:05:28
17	address and control information that was sent by	02:05:32
18	the host computer using packetized serial	02:05:34
19	signals; and the AMB decodes that information and	02:05:37
20	generates the data address and control signals	02:05:42
21	needed by the DDR2 SDRAM memory devices; correct?	02:05:45
22	A. Yes, that's correct. That's what it	02:05:50
23	says.	02:05:54
24	Q. And you believe that's an accurate	02:05:56
25	description of how the AMB and the FBDIMM works?	02:06:00

1	A. Yes, I do.	02:06:03
2	ATTORNEY CHANDLER: Let's take a break.	02:06:17
3	THE WITNESS: Okay.	02:06:20
4	ATTORNEY CHANDLER: Maybe five minutes?	02:06:24
5	ATTORNEY LINDSAY: That works for me.	02:06:26
6	THE WITNESS: Sounds good.	02:06:28
7	THE VIDEOGRAPHER: Off the record at	02:06:29
8	2:06 p.m. Pacific Time.	02:06:30
9	(Recess taken from 2:06 p.m. to	
10	2:17 p.m.)	
11	THE VIDEOGRAPHER: On the record at	02:17:14
12	2:17 p.m. Pacific Time.	02:17:15
13	BY ATTORNEY CHANDLER:	02:17:17
14	Q. Please turn to paragraph 59 of your	02:17:19
15	report expert declaration, which I believe is the	02:17:21
16	same in both.	02:17:24
17	A. Okay, I am there.	02:17:38
18	Q. In paragraph 59 of your expert	02:17:38
19	declaration you talk about the Harris reference	02:17:40
20	marked as Exhibit 1023; correct?	02:17:42
21	A. Yes, that's correct.	02:17:48
22	Q. In paragraph 59 your expert	02:17:49
23	declarations you have reprinted Figure 1A of	02:17:51
24	Harris, and then you have drawn little edge	02:17:54
25	connections along the bottom of the memory module	02:17:56

1 shown in Figure 1A; correct? 02:18:01

2 A. Yes, that's correct. 02:18:06

3 Q. And then you state that, in your 02:18:07

4 opinion, Harris' DIMM memory module would receive 02:18:09

5 the external voltage source from a side connector 02:18:12

6 instead of the edge connections along the bottom 02:18:18

7 of the memory module; correct? 02:18:21

8 A. Yes, that's correct. 02:18:26

9 Q. So to be clear, is your opinion that 02:18:28

10 Harris only teaches receiving an external voltage 02:18:31

11 source from a side connector, or do you believe 02:18:35

12 that Harris includes other teachings besides just 02:18:38

13 Figure 1A in isolation where the external 02:18:41

14 voltage source can be connected to an edge 02:18:45

15 connection along the bottom of Harris' memory 02:18:49

16 module? 02:18:52

17 ATTORNEY LINDSAY: Objection; form. 02:18:54

18 THE WITNESS: So my recollection is 02:18:55

19 that Harris is very clear that its intent is to 02:18:56

20 allow the removal of voltage supply pins along 02:19:00

21 the edge connectors; and that the voltage comes 02:19:07

22 from an external source. So yes, it -- if they 02:19:11

23 remove the voltage pins and then add back in the 02:19:14

24 voltage pins, they would not achieve the benefit 02:19:19

25 of their design intent. 02:19:22

1 BY ATTORNEY CHANDLER: 02:19:25

2 Q. I'm a little confused by your logic 02:19:25
3 right there, and I'm also a little unclear if 02:19:28
4 that answered my question. 02:19:33

5 So Harris teaches reducing the number 02:19:35
6 of voltage pins; correct? 02:19:44

7 A. Yes, that's correct. 02:19:47

8 Q. So I'm not trying to ask about how many 02:19:52
9 voltage pins there are in Harris' memory module. 02:19:57
10 For now I'm focused on the question of whether, 02:20:01
11 in your opinion, the voltage going to Harris' 02:20:04
12 memory module can only come from a side connector 02:20:09
13 or, in your opinion, are there embodiments of 02:20:12
14 Harris where the voltage can come from at least 02:20:17
15 one of the edge connectors along the bottom of 02:20:25
16 memory module? 02:20:28

17 A. I don't recall that being disclosed. 02:20:33
18 If you want to point me to something, maybe I 02:20:34
19 could comment on it. 02:20:37

20 Certainly, when I said the side -- the 02:20:39
21 voltage supply could have come from either side 02:20:46
22 or the top or the backside, or the front side as 02:20:48
23 well. I wasn't intending to make a distinction 02:20:51
24 between those different options. 02:20:55

25 Q. I just want to be clear about your 02:20:58

1	opinion.	02:21:00
2	So your opinion is that the voltage	02:21:00
3	going Harris' memory module could basically enter	02:21:02
4	the memory module anywhere other than the edge	02:21:06
5	connections along the bottom of the memory module	02:21:11
6	that plug into the host system; correct?	02:21:14
7	ATTORNEY LINDSAY: Objection; form,	02:21:17
8	misstates prior testimony.	02:21:19
9	THE WITNESS: Yeah, I don't recall if	02:21:20
10	Harris proposes an embodiment -- they might, in	02:21:22
11	which case, I'm sure we'll discuss it -- that	02:21:28
12	they suggest comes over those pins. However,	02:21:30
13	Harris is clear that one of its main objectives	02:21:35
14	is to remove those pins.	02:21:39
15	So lots of people say, Well, our	02:21:42
16	invention is turning to the left; here's an	02:21:45
17	embodiment where we turn to the right.	02:21:47
18	Okay, that doesn't make any sense, but	02:21:49
19	you could say whatever you want.	02:21:52
20	That was a bad analogy. I apologize.	02:21:54
21	I make terrible analogies on the fly.	02:21:56
22	BY ATTORNEY CHANDLER:	02:22:00
23	Q. You understand that Dr. Wolfe's opinion	02:22:00
24	is that Harris does teach that the voltage can	02:22:02
25	come on the edge connections along the bottom of	02:22:05

1 the memory module; and then you have this long 02:22:10
2 discussion where you disagree with that; right? 02:22:12

3 A. Yeah, that's my recollection. 02:22:16

4 Q. And the question, though, I'm trying to 02:22:20
5 crystallize for both myself and for the Board is 02:22:25
6 whether it's your position that Harris' invention 02:22:28
7 could never ever be practiced using a memory 02:22:35
8 module that receives power from the edge 02:22:38
9 connections along the bottom of the memory module 02:22:43
10 that plugs into the host system. 02:22:45

11 ATTORNEY LINDSAY: Objection form. 02:22:51

12 THE WITNESS: Yeah, at least for the 02:22:52
13 reasons that it's fundamentally contrary to what 02:22:54
14 Harris teaches as a benefit and a design goal; 02:23:00
15 but as well, in such a situation, the power 02:23:02
16 supply wouldn't be an external voltage supply. 02:23:09

17 BY ATTORNEY CHANDLER: 02:23:12

18 Q. And that's your opinion that you used 02:23:14
19 when forming your nonobviousness conclusions; 02:23:16
20 correct? 02:23:23

21 ATTORNEY LINDSAY: Objection; form. 02:23:23

22 THE WITNESS: I did use those opinions 02:23:28
23 when forming my response to Dr. Wolfe's 02:23:29
24 arguments, yeah. 02:23:35
25

1 BY ATTORNEY CHANDLER:

02:23:37

2 Q. And did you form any opinions about
3 Harris where you accepted Dr. Wolfe's conclusion
4 that Harris does teach voltage being supplied to
5 Harris' memory module along the bottom edge of
6 the memory module through the edge connections
7 that plug into the host system?

02:23:37

02:23:39

02:23:42

02:23:50

02:23:56

02:24:00

8 A. Possibly. I haven't memorized my
9 report. If you want to focus me on a particular
10 area, I'd be happy to review that.

02:24:04

02:24:07

02:24:12

11 Q. I don't believe you did, which is why
12 I'm asking you.

02:24:14

02:24:15

13 A. Yeah, yeah. As I sit here today, I
14 don't recall taking that -- assuming that
15 position and then making further arguments. But
16 if I did and I simply don't recall -- if I
17 recalled, I would point you to it.

02:24:16

02:24:19

02:24:22

02:24:26

02:24:28

18 Q. You would agree, though, that it's very
19 common for a memory module to receive power from
20 the edge connections along the bottom of the
21 memory module that plugs into the host system;
22 right?

02:24:31

02:24:33

02:24:35

02:24:38

02:24:40

23 A. Yes. That's the standard approach, and
24 Harris is teaching an innovation that's contrary
25 to the standard.

02:24:43

02:24:45

02:24:49

1	Q.	According to you, but not Dr. Wolfe;	02:24:50
2		right?	02:24:53
3	A.	According -- no, literally according to	02:24:55
4		the technical standards, he's saying that it's	02:24:57
5		possible; but he's not saying that that's a	02:25:02
6		standard approach.	02:25:04
7		I think, for example, if I remember	02:25:09
8		right, there was a discussion of taking the power	02:25:10
9		supply from the memory controller, and I think he	02:25:12
10		was asked if he was aware of anybody doing that.	02:25:15
11		He said no.	02:25:19
12		So I don't think that he took the	02:25:19
13		approach that any such design was standard.	02:25:23
14	Q.	I think that may have confused you.	02:25:30
15	A.	It's happened.	02:25:32
16	Q.	You would agree that it's very common	02:25:36
17		for a memory module to receive power from the	02:25:38
18		edge connections along the bottom of the memory	02:25:41
19		module that plugs into the host system; right?	02:25:44
20	A.	Yes, that is standard approach. But	02:25:50
21		Harris directly, in my opinion, teaches against	02:25:55
22		that.	02:25:59
23	Q.	And you understand that Dr. Wolfe has a	02:26:01
24		different opinion about what Harris teaches with	02:26:05
25		respect to whether or not the voltage going to	02:26:07

1 Harris' memory module can come through the edge 02:26:14
2 connections along the bottom that are plugged 02:26:17
3 into the host system? That's a sort of 02:26:18
4 fundamental dispute between you and Dr. Wolfe; 02:26:22
5 fair? 02:26:25

6 A. I'm sorry. Could you repeat the 02:26:31
7 question. 02:26:32

8 Q. You understand that Dr. Wolfe has a 02:26:33
9 different opinion than you do about whether 02:26:35
10 Harris teaches whether or not the voltage going 02:26:38
11 to Harris' memory module can be supplied through 02:26:45
12 the edge connections along the bottom of the 02:26:50
13 memory module that plug into the host system? 02:26:53

14 A. I don't know that we actually have a 02:27:03
15 disagreement about whether or not Harris teaches 02:27:04
16 that. 02:27:06

17 My recollection is he said that he 02:27:08
18 thought it could be used that way, but I may just 02:27:10
19 be misremembering how tightly his arguments 02:27:15
20 were -- how tight his arguments were. 02:27:18

21 Q. Do you see on paragraph 59 of your 02:27:22
22 expert declaration you've got a photograph of a 02:27:28
23 BBvault? 02:27:31

24 A. Yes, I see that. 02:27:34

25 Q. Could you please pull up Exhibit 2035 02:27:35

1 and let me know when you're there. And I'll also 02:27:42
2 put it in the chat for ease of reference. 02:27:44
3 (Exhibit Number 2035 was previously
4 marked for identification.)
5 BY ATTORNEY CHANDLER: 02:28:04
6 Q. All right. Do you have Exhibit 2035? 02:28:04
7 A. I do. I'm trying to get it opened -- 02:28:08
8 okay, there it is. 02:28:11
9 All right. Yes, I see it. 02:28:15
10 Q. Last page of Exhibit 2035 it shows 02:28:19
11 BBvault, which you reference in paragraph 59 of 02:28:25
12 your declarations; correct? 02:28:28
13 A. Yes, that's correct. 02:28:34
14 Q. BBvault is a memory module that was 02:28:34
15 released back in 2005; correct? 02:28:36
16 A. Yes, that's correct. 02:28:41
17 Q. And the side connection on the BBvault 02:28:42
18 memory module connects to a battery backup; 02:28:46
19 correct? 02:28:50
20 A. Yes. 02:28:54
21 Q. And in addition to that side connection 02:28:55
22 on BBvault, there is also edge connections along 02:28:58
23 the bottom of the memory module that permit 02:29:02
24 BBvault to plug in to a host system and receive 02:29:06
25 power along the edge connections on the bottom of 02:29:10

1 the memory module; correct? 02:29:18

2 A. Yes, that's correct. 02:29:19

3 Q. So the side connection on the BBvault 02:29:21

4 memory is for battery backup, while the edge 02:29:24

5 connections along the bottom of the memory module 02:29:27

6 are for power from the host system; correct? 02:29:29

7 A. Yes. The side connections are -- go to 02:29:35

8 the battery backup and are used when the power 02:29:38

9 coming in from the host system along the edge 02:29:44

10 connectors is not used. 02:29:47

11 Q. And this was known by 2005; correct? 02:29:51

12 A. Yes. 02:29:57

13 Q. So it was known by 2005 that the memory 02:29:57

14 module would have both edge connections along the 02:30:00

15 bottom of the memory module to receive power from 02:30:02

16 the host system, as well as side connections to 02:30:04

17 connect to a battery backup in the event that the 02:30:07

18 host system loses power; correct? 02:30:10

19 A. Yes, but not of the nature that Harris 02:30:17

20 discloses. 02:30:21

21 Q. But that was taught, including by 02:30:33

22 BBvault in 2005; correct? 02:30:37

23 ATTORNEY LINDSAY: Objection; form. 02:30:38

24 THE WITNESS: BBvault showed that -- 02:30:42

25 disclosed a system that could operate using the 02:30:45

1	standard power supply over an edge connector, as	02:30:52
2	well as switch away from that to a power supply	02:30:56
3	that's attached over a side connector.	02:31:04
4	BY ATTORNEY CHANDLER:	02:31:06
5	Q. And the side connector, that's the	02:31:07
6	battery backup?	02:31:09
7	A. Yes, that's correct.	02:31:11
8	Q. Could you pull up the Harris reference,	02:31:16
9	marked as Exhibit 1023. Let me know when you	02:31:17
10	have it in front of you again.	02:31:24
11	A. All right, I have it.	02:31:30
12	Q. Look at Figure 3 of Harris, marked as	02:31:40
13	Exhibit 1023. Let me know when you have it in	02:31:42
14	front of you.	02:31:48
15	A. I have it in front of me.	02:31:49
16	Q. Figure 3 is an embodiment of Harris'	02:31:51
17	invention; correct?	02:31:53
18	A. Likely. I don't recall for sure.	02:31:56
19	Q. Paragraph 7 of Harris confirms that	02:32:01
20	Figure 3 is an embodiment of his invention;	02:32:04
21	correct?	02:32:08
22	A. Yes.	02:32:18
23	Q. And Figure 3 of Harris shows a memory	02:32:18
24	controller 302 that's part of the host system;	02:32:23
25	correct?	02:32:26

1	A. Yes, that's correct.	02:32:29
2	Q. And Figure 3 of Harris shows several	02:32:31
3	memory modules 306 with edge connections along	02:32:34
4	the bottom of those memory modules to plug in to	02:32:38
5	the host system; correct?	02:32:44
6	A. Yes, that's correct.	02:32:49
7	Q. The edge connections in the memory	02:32:49
8	module, shown in Figure 3 of Harris, are used to	02:32:52
9	connect to the memory controller in 302 that's	02:32:56
10	part of the host system; correct?	02:33:00
11	A. I believe so, yeah. Sure.	02:33:05
12	Q. The memory modules in Figure 3 of	02:33:07
13	Harris do not show any connections on the side of	02:33:10
14	the memory module for receiving power; correct?	02:33:14
15	A. That's correct.	02:33:19
16	Q. And paragraph 17 of Harris describes	02:33:21
17	Figure 3; correct?	02:33:25
18	A. It begins -- referring to Figure 3,	02:33:32
19	yeah.	02:33:34
20	Q. And the last two sentences of	02:33:35
21	paragraph 17 of Harris, marked as Exhibit 1023,	02:33:40
22	state, with reference to Figure 3:	02:33:45
23	"Although not explicitly shown in	02:33:49
24	this figure, each memory board also	02:33:52
25	receives a supply voltage that is	02:33:54

1	locally converted by an on-board VRM for	02:33:57
2	powering the DRAM and buffer components	02:34:04
3	therein. In one arrangement, the supply	02:34:07
4	voltage may be sourced from the memory	02:34:10
5	controller 302 or from a separate	02:34:13
6	voltage source."	02:34:17
7	Did I read that accurately?	02:34:19
8	A. You did.	02:34:22
9	Q. In Figure 3 of Harris, the memory	02:34:24
10	modules can receive power from the host system	02:34:28
11	using the edge connections along the bottom of	02:34:32
12	the memory module; correct?	02:34:36
13	A. I don't believe so.	02:34:40
14	Q. So you disagree with that statement?	02:34:41
15	A. Sure.	02:34:45
16	Harris teaches -- Harris suggests that	02:34:47
17	the memory controller can provide power. No	02:34:49
18	memory controller that I'm familiar with does	02:34:55
19	that. The -- my recollection, as I said, was	02:34:57
20	that Dr. Wolfe is unfamiliar with any such memory	02:35:00
21	controller. But furthermore, Harris	02:35:06
22	fundamentally doesn't work.	02:35:09
23	So it doesn't matter to me much, if the	02:35:11
24	power supply -- if they say the power comes from	02:35:14
25	the memory controller or not. It's just a broken	02:35:18

1	design.	02:35:24
2	Q. When you say "Harris fundamentally	02:35:25
3	doesn't work," where does Harris say that he	02:35:27
4	fundamentally doesn't work?	02:35:33
5	A. I'm saying Harris is a fundamentally	02:35:37
6	broken design and cannot work the way it's --	02:35:41
7	Q. Yeah. I'm sorry. "Cannot work the	02:35:44
8	way," and then I cut you off. I apologize.	02:35:47
9	A. It's quite all right.	02:35:50
10	Cannot work the way it's disclosed.	02:35:51
11	(Exhibit Number 2101 was previously	
12	marked for identification.)	
13	BY ATTORNEY CHANDLER:	02:35:53
14	Q. Please turn to Exhibit 2101, and let me	02:35:56
15	know when you're there. And I will also put it	02:36:01
16	in the chat.	02:36:04
17	All right. Do you have Exhibit 2101 in	02:36:38
18	front of you?	02:36:41
19	A. It was larger and taking a little	02:36:42
20	longer to download, but yes, I have it now.	02:36:43
21	Q. Are you familiar with Exhibit 2101?	02:36:46
22	A. Yes, I have seen it before.	02:36:49
23	Q. Exhibit 2101 is an exhibit that you	02:36:52
24	cite that describes FBDIMMs; correct?	02:36:56
25	A. That matches my recollection.	02:37:01

1	Q. Please turn to page 4 of Exhibit 2101	02:37:06
2	and let me know when you're there.	02:37:09
3	A. I am there.	02:37:12
4	Q. Page 4 of Exhibit 2101 shows FBDIMM	02:37:14
5	memory modules connected to a memory controller	02:37:19
6	in the host system using edge connections along	02:37:23
7	the bottom of the memory modules; correct?	02:37:26
8	A. Yes, that's correct.	02:37:30
9	Q. FBDIMM memory modules receive power	02:37:33
10	from the host system using edge connections along	02:37:36
11	the bottom of the memory module; correct?	02:37:40
12	A. Yes, that's correct.	02:37:45
13	Q. And page 4 of Exhibit 2101 is nearly	02:37:47
14	identical to Figure 3 of Harris, marked as	02:37:54
15	Exhibit 1023; correct?	02:37:59
16	A. It has many structural elements that	02:38:01
17	are identical, yes.	02:38:04
18	Q. Please turn to page 21 of Exhibit 2101.	02:38:06
19	Let me know when you're there.	02:38:11
20	A. Okay, I'm there.	02:38:19
21	Q. Both page 21 and 22 of Exhibit 2101	02:38:20
22	refer to a, quote, "key" on the bottom edge of	02:38:27
23	the FBDIMM memory module; correct?	02:38:32
24	A. Yes.	02:38:45
25	Q. And what is meant by a "key" here on	02:38:46

1 pages 21 and 22, Exhibit 2101?

02:38:48

2 A. Well, in this context, a key is
3 referring to a physical structure that would
4 either accept two elements to be mated together
5 or to block them so that you, for example,
6 couldn't put a DIMM into the wrong slot that
7 didn't match it. That's the intent, in general.

02:38:53

02:38:55

02:39:02

02:39:05

02:39:08

02:39:13

8 Q. And so to be clear, what's the purpose
9 of a key along the bottom edge of the memory
10 module?

02:39:18

02:39:20

02:39:22

11 A. That's -- I think I just answered that
12 question: It's -- they want to make sure that
13 you couldn't insert the wrong DIMM into a slot
14 that didn't match or support it.

02:39:25

02:39:27

02:39:30

02:39:34

15 Q. And was it common to use a key along
16 the bottom edge of a memory module?

02:39:37

02:39:40

17 A. It wasn't uncommon in the context of
18 JEDEC memory modules, or memory modules falling
19 under various JEDEC specifications. I think keys
20 of one form or another were always used, but I'm
21 not positive.

02:39:48

02:39:53

02:39:58

02:40:02

02:40:05

22 Q. Could you turn back to Exhibit 2016
23 that we looked at earlier this morning about PCI
24 bus variations. And let me know when you have
25 that exhibit.

02:40:05

02:40:11

02:40:16

02:40:19

1	A. I have it.	02:40:22
2	Q. Page 6 of Exhibit 2016 at the top shows	02:40:25
3	another example of using a key along the bottom	02:40:29
4	edge of the module; correct?	02:40:35
5	A. Yes, it does.	02:40:40
6	Q. And this would be another example, as	02:40:43
7	you explained, that the key is designed to make	02:40:46
8	sure that you don't insert the module into the	02:40:50
9	wrong slot on the computer; is that fair?	02:40:58
10	A. Yes. So for example, as we were	02:41:04
11	discussing before, I think it was PCI-X said that	02:41:06
12	they're completely backward compatible. But this	02:41:11
13	shows that while PCI-X runs at 3.3 volts and	02:41:14
14	possibly 5, it physically could not accept a	02:41:20
15	5-volt-only slot because the 3.3-volt key is not	02:41:25
16	cut out.	02:41:29
17	Q. So in this example, on page 6 of	02:41:35
18	Exhibit 2016, the module labeled 5-volt, which is	02:41:38
19	the second from the top, would not fit into a	02:41:44
20	slot with the 3.3-volt key; correct?	02:41:48
21	A. That's correct. If the key slot --	02:41:58
22	it's -- I'm not sure if the tradition is to refer	02:42:00
23	to the key itself as the slot or the tab that	02:42:04
24	goes into it. But if that slot is not cut out on	02:42:07
25	the card, there'll be some piece of plastic that	02:42:09

1 physically blocks it from being inserted. 02:42:14

2 Q. And to avoid confusion, I think you and 02:42:16

3 I started to use "slot" in two different ways. 02:42:21

4 So normally I would think of "slot" as 02:42:25

5 the full length that the card would plug into, 02:42:27

6 and I would think of the key as more of a little 02:42:33

7 notch. Is that -- 02:42:36

8 A. Yeah, I didn't realize, but you're 02:42:37

9 right, I was using the term "slot" in two 02:42:39

10 different ways, yeah. 02:42:42

11 Q. So the -- the little key is a notch on 02:42:44

12 the bottom edge of the module that can be used to 02:42:46

13 prevent you from inserting the module into the 02:42:52

14 wrong slot on the host computer; correct? 02:42:57

15 A. That's right. Thinking about this now, 02:43:06

16 it seems to me that the literal "key" should 02:43:09

17 probably be the little plastic tab, and this 02:43:13

18 would be the keyhole. But I've never heard 02:43:16

19 anybody call it a keyhole or anything like that. 02:43:19

20 Q. Let's turn back to Harris, 02:43:21

21 Exhibit 1023. Let me know when you're there. 02:43:24

22 A. I have it opened now. 02:43:30

23 Q. So at the end of paragraph 13 of 02:43:42

24 Harris, marked as Exhibit 1023, he states, quote: 02:43:44

25 "By way of an additional variation 02:43:52

1 in implementation, the form factor
2 associated with the memory assembly
3 module 100A may be suitably modified
4 (e.g., removing the board's connector
5 keyway) so as to ensure that a memory
6 assembly module embodying the teachings
7 of the present disclosure is not
8 interchangeable with the standard DIMM,
9 thereby preventing any accidental
10 damage," end quote.

11 Did I read that accurately?

12 A. Yes, you did.

13 Q. Is the keyway, referenced in
14 paragraph 13 of Harris, marked as Exhibit 1023,
15 the same concept as the key that we were just
16 discussing on page 6 of Exhibit 2016?

17 A. I believe so.

18 Q. And also the same concept described on
19 pages 21 and 22 of Exhibit 2101; is that correct?

20 A. Yes, I believe so.

21 Q. All right. Can you turn back to
22 Exhibit 2032, and let me know when you're there.

23 A. I'm sorry. 2032?

24 Q. Yes. That's the Claim Construction
25 Order in the Eastern District of Texas?

1	A. Yes, I'm there now.	02:45:33
2	Q. And please go to page 23 of	02:45:35
3	Exhibit 2032, and let me know when you're there.	02:45:39
4	A. Okay. I'm there.	02:45:45
5	Q. Do you see in the upper left of page 23	02:45:52
6	of Exhibit 2032 that Netlist's construction for	02:45:56
7	the first, second, third, fourth regulated	02:46:02
8	voltage:	02:46:08
9	"Is plain and ordinary meaning to a	02:46:08
10	person of ordinary skill in the art in	02:46:12
11	light of the specification (that is,	02:46:13
12	first, second, third and fourth voltages	02:46:15
13	that are adjusted within tolerance to a	02:46:20
14	particular voltage level)."	02:46:24
15	Do you see that?	02:46:27
16	A. Yes, I see that.	02:46:29
17	Q. Do you disagree with Netlist's proposed	02:46:32
18	construction here?	02:46:36
19	A. Only to the extent that it's my	02:46:38
20	understanding that one can -- so typically either	02:46:40
21	offer a construction or say "plain and ordinary	02:46:46
22	meaning."	02:46:49
23	They say "plain and ordinary meaning."	02:46:51
24	As I understand it, that's the construction.	02:46:53
25	Now, the judge obviously doesn't have to accept	02:47:01

1 that one way or another.

02:47:03

2 Q. Do you agree that the plain and
3 ordinary meaning of a regulated voltage is a
4 voltage that is adjusted within tolerance to a
5 particular voltage level?

02:47:08

02:47:09

02:47:13

02:47:17

6 A. Speaking -- no, I wouldn't say, in
7 general, that's necessarily an accurate -- the
8 correct construction for a regulated voltage.

02:47:25

02:47:26

02:47:32

9 Q. And so -- I mean, that's what Netlist
10 proposed here, and that's what I'm trying to
11 understand, is whether you agree or disagree with
12 that.

02:47:34

02:47:39

02:47:41

02:47:43

13 A. Yeah, I think that that's -- I agree
14 with their construction, which is plain and
15 ordinary meaning. I would not step up and agree
16 with the subsequent parenthetical comments. They
17 don't seem right to me, but that's because I'm
18 inclined to, in my mind, try to test and think if
19 there's an exception to a construction that I can
20 imagine, but I haven't conducted a full analysis.

02:47:44

02:47:54

02:47:56

02:48:00

02:48:06

02:48:10

02:48:14

02:48:18

21 I think the construction should be
22 plain and ordinary meaning, and the Court agreed.

02:48:21

02:48:23

23 Q. But how would you explain to somebody
24 like myself, who is not a person of ordinary
25 skill in the art, or to someone like the judges

02:48:28

02:48:30

02:48:34

1 and the Board here, what is the plain and 02:48:37
2 ordinary meaning of a regulated voltage? 02:48:39
3 A. The plain and ordinary meaning is that 02:48:45
4 the voltage input is regulated. The voltage 02:48:47
5 output is a regulated voltage sourced from its 02:48:56
6 input. 02:49:04
7 Q. And what does -- it's not entirely 02:49:04
8 helpful to me to use the word "regulated" both in 02:49:07
9 the claim language and in your definition of the 02:49:11
10 claim language. 02:49:13
11 So how else would you explain the 02:49:14
12 concept of a regulated voltage? 02:49:16
13 ATTORNEY LINDSAY: Objection; form, 02:49:21
14 asked and answered. 02:49:22
15 THE WITNESS: Yeah, I wouldn't be 02:49:24
16 inclined necessarily to go further. I mean, I 02:49:28
17 would -- I would give an example. 02:49:32
18 For example, it says -- the 02:49:35
19 parenthetical says "the voltages are adjusted, 02:49:37
20 within tolerance, to a particular voltage level." 02:49:46
21 A voltage could be regulated without 02:49:53
22 being within any particular tolerance at all and 02:49:58
23 it could still be classified as a regulated 02:50:01
24 voltage. 02:50:04
25

1 BY ATTORNEY CHANDLER:

02:50:05

2 Q. How would that differ from an
3 unregulated voltage?

02:50:05

02:50:09

4 A. It could differ quite a bit. An
5 unregulated voltage could be totally
6 unpredictable in its time-varying
7 characteristics.

02:50:10

02:50:12

02:50:15

02:50:19

8 A regulated voltage could be completely
9 predictable in its time-varying characteristics
10 without falling within any particular
11 predetermined voltage tolerance.

02:50:21

02:50:23

02:50:28

02:50:30

12 Q. So if I understand, you're sort of
13 expanding the possible scope of regulated voltage
14 to be broader than just a voltage that's adjusted
15 within tolerance to a particular voltage level;
16 is that fair?

02:50:39

02:50:44

02:50:50

02:50:55

02:50:57

17 A. Yeah, that's -- that's fair. It's not
18 that I'm saying this -- right, they're
19 essentially saying, i.e. for a second, third.
20 That, I disagree with. If it was "e.g.," sure.

02:50:59

02:51:01

02:51:06

02:51:09

21 Q. Okay. So to be clear, in your opinion,
22 a voltage that is adjusted within tolerance to a
23 particular voltage level is an example of a
24 regulated voltage but it may not be the full
25 scope of all the examples of what might be a

02:51:13

02:51:18

02:51:21

02:51:24

02:51:26

1 regulated voltage. 02:51:30

2 Is that accurate? Does that accurately 02:51:31

3 capture your opinion? 02:51:34

4 A. Yes. I would say that's a good 02:51:38

5 characterization. That's what I was trying to 02:51:41

6 get at. 02:51:43

7 (Exhibit Number 2038 was previously

8 marked for identification.)

9 BY ATTORNEY CHANDLER: 02:51:46

10 Q. Could you turn to Exhibit 2038. Let me 02:51:51

11 know when you have that. And I'll also put it in 02:51:54

12 the chat for ease of reference. 02:51:58

13 A. Okay. I have it opened in front of me. 02:52:16

14 Q. Exhibit 2038, which is the same in both 02:52:19

15 IPRs, is the ATX12V Power Supply Design Guide, 02:52:22

16 Version 2.2, dated March 2005; correct? 02:52:28

17 A. Yes. 02:52:32

18 Q. And then please go to page 8 of 02:52:34

19 Exhibit 2038. Let me know when you're there. 02:52:41

20 A. I am there. 02:52:43

21 Q. Page 8 of Exhibit 2038 states at the 02:52:44

22 top, under the heading 1.1 "Scope": 02:52:47

23 "This document provides design 02:52:53

24 suggestions and reference specifications 02:52:55

25 for a family of power supplies that 02:52:59

1 comply with the ATX specification 02:53:02
2 Version 2.03 for motherboards and 02:53:04
3 chassis." 02:53:08
4 Did I read that accurately? 02:53:10
5 A. Yes, you did. 02:53:13
6 Q. So this Exhibit 2038 concerns power 02:53:15
7 supplies that can be used on the motherboard of a 02:53:21
8 computer system; is that fair? 02:53:25
9 A. Yes. ATX is a particular form factor. 02:53:29
10 And so there are ATX motherboards, and this is 02:53:33
11 saying a power supply that would fit physically 02:53:39
12 into a ATX chassis and provide suitable 02:53:42
13 electrical requirements for an ATX motherboard 02:53:46
14 has these specifications. 02:53:51
15 Q. And is the ATX form factor -- is that 02:53:52
16 commonly used in sort of the mini tower computers 02:53:59
17 that some of us might be familiar with? 02:54:04
18 A. Yeah, that's my recollection. 02:54:08
19 Q. Under Section 1.2, on page 8 of 02:54:12
20 Exhibit 2038, this document indicates that the 02:54:16
21 power supply on the motherboard is 12 volts; 02:54:22
22 correct? 02:54:27
23 A. It indicates that there is a 12-volt 02:54:35
24 output, provided that -- well, there has to be a 02:54:40
25 12-volt output, that has to be provided by the 02:54:44

1	power supply, yeah.	02:54:48
2	Q. Please turn to page 13 of Exhibit 2038.	02:54:49
3	Let me know when you're there.	02:54:53
4	A. I am there.	02:55:00
5	Q. Under Section 3.2.1 on page 13 of	02:55:01
6	Exhibit 2038, The document states, quote, "The DC	02:55:04
7	output voltages shall remain within the	02:55:11
8	regulation ranges shown in Table 2," end quote.	02:55:13
9	Did I read that accurately?	02:55:18
10	A. Yes.	02:55:19
11	Q. And then Table 2 of Exhibit 2038 is	02:55:21
12	showing regulated voltages; correct?	02:55:25
13	A. Yes, that's correct.	02:55:31
14	Q. These are not unregulated voltages,	02:55:32
15	these are regulated voltages; correct?	02:55:35
16	A. Yes, they were labeled "regulated	02:55:37
17	voltages."	02:55:41
18	Q. And, for example, Footnote 1 to Table 2	02:55:41
19	on page 13 of Exhibit 2038 states that the	02:55:45
20	regulated range of the 12-volt power supply is	02:55:48
21	plus or minus 10 percent; correct?	02:55:52
22	A. Yes.	02:55:57
23	Q. So this would be an example of a	02:55:58
24	12-volt output that can vary by plus or minus	02:56:04
25	10 percent and still be a regulated voltage;	02:56:08

1 fair? 02:56:12

2 A. Yes, within the definition of 02:56:12

3 "regulated" used here. 02:56:14

4 Q. Can you turn back to Harris, marked 02:56:16

5 Exhibit 1023. Let me know when you're there. 02:56:21

6 A. I have it open now. 02:56:28

7 Q. In paragraph 13 of Harris, he refers to 02:56:32

8 a 12-volt power supply with a tolerance around 02:56:40

9 plus or minus 15 percent; correct? 02:56:48

10 A. He does refer to the 12-volt plus or 02:57:11

11 minus 15 percent. I just want to review the rest 02:57:14

12 of the context there. 02:57:17

13 (Witness reviews document.) 02:57:25

14 A. Yes, he is referring to 12-volt power 02:57:58

15 supply with a tolerance of plus or minus 02:58:03

16 15 percent. 02:58:09

17 Q. In Harris, the 12-volt power supply 02:58:10

18 with a tolerance of plus or minus 15 percent 02:58:13

19 could be a regulated voltage; correct? 02:58:16

20 A. It is regulated at least to that 02:58:22

21 extent, yes. The only reason I have that 02:58:24

22 caveat -- it's probably not material here -- it's 02:58:27

23 a matter of perspective. From the point of view 02:58:31

24 of the power supply, it is regulated to operate 02:58:34

25 within those boundaries. Someone else consuming 02:58:37

1 that power who cannot directly operate within 02:58:41
2 that range might consider it unregulated. It's 02:58:45
3 just a matter of perspective. 02:58:48

4 Q. But it would satisfy the definition of 02:58:59
5 "regulated voltage" we were describing earlier, 02:59:00
6 which, my understanding was your opinion was 02:59:03
7 broad enough to include a voltage that's adjusted 02:59:08
8 within tolerance to a particular voltage level; 02:59:13
9 is that fair? 02:59:15

10 A. Sure. From the point of view of that 02:59:18
11 power supply, that is regulated voltage. 02:59:20

12 Q. Could you please turn to paragraph 103 02:59:27
13 of your declaration, marked as Exhibit 2061, 02:59:40
14 which is substantially similar to paragraph 105 02:59:46
15 of your declaration marked as Exhibit 2031. And 02:59:49
16 actually, let me just make sure I've got that 02:59:57
17 straight. 03:00:02

18 Unfortunately, your two declarations 03:00:06
19 start to diverge towards the back. 03:00:08

20 A. Yeah, I've got 2031 of the '918 open. 03:00:11
21 Do you want to give me the paragraph number for 03:00:17
22 that again, and maybe that's just quicker? 03:00:19

23 Q. Yeah. Paragraph 105. 03:00:22

24 A. Okay. 03:00:25

25 Q. And so I want to ask you about 03:00:30

1 paragraphs 105, 106 and 107 in Exhibit 2031, 03:00:32
2 which are substantially identical to paragraphs 03:00:36
3 103, 104, 105 in your other declaration, marked 03:00:40
4 as Exhibit 2061. The first thing you should 03:00:43
5 probably do, is just -- you don't have to read 03:00:50
6 every word, but just quickly look at 105, 106, 03:00:52
7 107 to get generally oriented, and then I'll have 03:00:57
8 some specific questions for you when you're 03:01:02
9 ready. 03:01:05

10 (Witness reviews document.) 03:01:40

11 A. Okay. 03:02:04

12 Q. So in these paragraphs of your expert 03:02:10
13 declaration, you're discussing Harris' disclosure 03:02:14
14 of a redundant power supply. 03:02:19

15 A. Yes, that's correct. Yeah. Sorry, I 03:02:25
16 cut you off. 03:02:27

17 Q. Is that generally fair? 03:02:29

18 A. Yes. 03:02:31

19 Q. So in the embodiment of Harris, marked 03:02:32
20 as Exhibit 1023, where he talks about a redundant 03:02:35
21 power supply, in my mind, there are two possible 03:02:40
22 ways, in general, to think about a redundant 03:02:52
23 power supply; and I want to understand your 03:02:57
24 interpretation of what Harris is referring to 03:03:01
25 when he makes reference to a redundant power 03:03:05

1	supply.	03:03:10
2	So one interpretation, in my mind, at	03:03:11
3	least -- and I'm not suggesting that either one	03:03:14
4	of these interpretations is the correct	03:03:16
5	interpretation of Harris; I'm just trying to,	03:03:19
6	from a general standpoint, understand your	03:03:23
7	opinions.	03:03:31
8	So one way that I might understand sort	03:03:33
9	of your opinions about Harris and the redundant	03:03:37
10	implementation, is that Harris is talking about	03:03:40
11	at least two different voltage sources going into	03:03:47
12	his memory module, both of which ultimately	03:03:52
13	connect to a plug in the wall that, you know, has	03:03:59
14	electricity; but like many things in life, one of	03:04:03
15	those two voltage sources can have some circuit	03:04:11
16	that fails.	03:04:18
17	Even though the wall is still supplying	03:04:23
18	electricity, it's possible that one of those	03:04:27
19	voltage sources fails, in which case, there would	03:04:30
20	be this second redundant voltage source that	03:04:35
21	would continue to supply power to Harris. So in	03:04:41
22	my mind, that's sort of one way to understand	03:04:46
23	what you're talking about.	03:04:50
24	But then there's also a different way,	03:04:52
25	potentially, to understand what you're talking	03:04:55

1	about, and I want to get clarity as to what	03:04:56
2	you're -- what you believe you're talking about.	03:04:59
3	And the different way of understanding	03:05:01
4	what you're talking about is that the redundancy	03:05:03
5	implementation in Harris is essentially like a	03:05:10
6	battery backup, and that even if the wall outlet	03:05:14
7	loses power -- so in other words, your whole	03:05:21
8	neighborhood loses power -- the redundancy	03:05:24
9	implementation taught by Harris would have	03:05:30
10	essentially a battery backup from the side that	03:05:32
11	continues to supply power no matter what.	03:05:35
12	Do you understand those two possible	03:05:40
13	characterizations of your discussion of Harris'	03:05:48
14	redundancy implementation?	03:05:55
15	ATTORNEY LINDSAY: Objection; form.	03:05:56
16	THE WITNESS: Yes, I think I understand	03:05:59
17	the distinction that you're suggesting.	03:06:01
18	BY ATTORNEY CHANDLER:	03:06:04
19	Q. And what did you intend, in	03:06:04
20	paragraphs 105 through 107 of Exhibit 2031 and	03:06:08
21	paragraphs 103 through 105 of Exhibit 2061, when	03:06:14
22	describing Harris' redundancy implementation with	03:06:19
23	respect to those two sort of different	03:06:25
24	characterizations that I just laid out?	03:06:28
25	A. I was referring to both.	03:06:34

1 It seems to me, without having any 03:06:38
2 market data, the more likely instance is along 03:06:39
3 the lines of the second example you gave with, 03:06:46
4 you know, maybe one is plugged into the wall and 03:06:49
5 the second is a large battery uninterruptible 03:06:51
6 power supply. 03:06:57

7 On the other hand, there's no reason 03:06:58
8 why it couldn't be two wall outlet plugs. 03:06:59

9 Q. Could you look at Figure 1A of Harris. 03:07:21
10 And I guess it's probably easiest just to look at 03:07:31
11 Exhibit 1023 directly. So let me know when you 03:07:36
12 have that in front of you. 03:07:40

13 A. I have it open now and am closing in on 03:07:41
14 1A. 03:07:45

15 All right. There's 1A. 03:07:46

16 Q. In Figure 1A of Harris, do you see that 03:07:48
17 there is a line -- there is a horizontal line 03:07:51
18 labeled 106 labeled Vcc; and then there is below 03:07:56
19 it another horizontal line labeled Vdd? 03:08:02

20 A. Yes, I see that. 03:08:07

21 Q. And then in paragraph 10 of Harris, do 03:08:08
22 you see that he refers, at the bottom of the page 03:08:15
23 where paragraph 10 begins, to Vdd and Vcc paths 03:08:22
24 108 and 106? 03:08:30

25 A. Yes, I see that. 03:08:33

1 Q. In your opinion, can either or both Vdd 03:08:39
2 and Vcc paths 108 and 106 include more than one 03:08:43
3 voltage along more than one wire? 03:08:59

4 ATTORNEY LINDSAY: Objection. 03:09:05

5 BY ATTORNEY CHANDLER: 03:09:05

6 Q. Or, in your opinion -- or, in your 03:09:10
7 opinion, is the Vdd path limited to only a single 03:09:08
8 wire with a single voltage, and the Vcc path is 03:09:14
9 limited to a single wire with a single voltage? 03:09:17

10 ATTORNEY LINDSAY: Objection; form. 03:09:24

11 THE WITNESS: Well, I would say, me 03:09:27
12 reading this figure, 106 and 108 are limited to a 03:09:32
13 single -- single voltage; and I would call that a 03:09:43
14 single logical wire or path. 03:09:45

15 You'll see that, however, line 108 03:09:50
16 splits out and goes to the individual DRAMs. So 03:09:54
17 one might consider those to be -- well, they're 03:09:58
18 certainly separate paths. One might consider 03:10:02
19 those to be at least separate wire segments. And 03:10:05
20 furthermore, there may be, you know, two versions 03:10:09
21 of 108, which go to half the DRAMs and half the 03:10:14
22 other one. 03:10:18

23 My understanding, though, is that there 03:10:19
24 is just the one voltage, Vdd. 03:10:22
25

1 BY ATTORNEY CHANDLER:

03:10:24

2 Q. And that's the way you interpreted
3 Harris, that Vdd would only be functionally one
4 wire with one voltage, even if it's a couple of
5 wires that split in various places. But
6 functionally, Vdd is just one wire, one voltage?

03:10:24

03:10:26

03:10:33

03:10:39

03:10:42

7 A. Yes.

03:10:48

8 Q. And same for Vcc?

03:10:48

9 A. Yes. It's not uncommon on large
10 circuits to have the same input voltage from one
11 single source -- well, typically on larger
12 circuits, they'll go into multiple locations,
13 even on the same chip -- we think of that as one
14 input power supply.

03:10:55

03:10:57

03:11:01

03:11:04

03:11:06

03:11:11

15 Q. But to be clear, in my experience, you
16 know, paths can include multiple wires traveling
17 next to each other, and those multiple wires
18 could have, you know, different voltages on them.
19 And I just want to -- I mean, as a general
20 matter, that's fair; right?

03:11:16

03:11:18

03:11:24

03:11:27

03:11:30

03:11:35

21 ATTORNEY LINDSAY: Objection; form.

03:11:37

22 BY ATTORNEY CHANDLER:

03:11:40

23 Q. And I just want to make sure that I'm
24 understanding your opinion that, in the example
25 of Harris, you're interpreting the path as being

03:11:40

03:11:43

03:11:44

1 narrowed to one voltage on essentially what could 03:11:52
2 be conceived as one wire. 03:11:59

3 A. Yeah, so if I understood your question, 03:12:05
4 you were asking about a path having neighboring 03:12:11
5 wires that are at different voltages. 03:12:19

6 Q. Yeah. 03:12:21

7 A. So, for example, if we look at the 03:12:22
8 portions of 106 and 108 that go horizontal. 03:12:23

9 Q. Yeah, or we can just focus on 106 to 03:12:29
10 sort of remove ambiguity. 03:12:33

11 A. Well, so I guess that's where I'm 03:12:35
12 confused. 03:12:37

13 106 is only going to have one voltage. 03:12:38
14 It could be running parallel for quite a while to 03:12:40
15 108, which has a separate voltage; but 106 will 03:12:43
16 only have one voltage at any particular instance 03:12:47
17 in time. 03:12:49

18 Q. But that's why -- I just want to 03:12:55
19 clarify: That's your opinion, that 106 will only 03:12:56
20 have one voltage at any instance in time? 03:12:59

21 A. Yes, that's my opinion. 03:13:04

22 Now, with one caveat, at very 03:13:05
23 high-speed situations, the voltage of one end of 03:13:09
24 the wire will be slightly different in an 03:13:14
25 instance of time from the other end of the wire; 03:13:16

1 but we're not dealing with situations like that 03:13:19
2 in this context. 03:13:23
3 (Exhibit Number 2012 was previously
4 marked for identification.)
5 BY ATTORNEY CHANDLER: 03:13:27
6 Q. Could you turn to Exhibit 2012 and let 03:13:27
7 me know when you have it. I'll also put it in 03:13:31
8 the chat for convenience. 03:13:33
9 A. I'm downloading it and opening it up. 03:13:42
10 It seems we've been going for about an 03:13:45
11 hour. Is this a good place to take a break? 03:13:47
12 Q. Why don't we -- I think it's been a 03:13:57
13 little less than an hour. I don't think it will 03:13:57
14 take too long to talk about this document, so why 03:13:58
15 don't we knock it out, since you've got it in 03:14:01
16 front of you, and then we'll take a break. 03:14:03
17 A. That sounds fair enough to me. 03:14:05
18 Q. All right. Do you have Exhibit 2012 03:14:08
19 open in front of you? 03:14:10
20 A. I do. 03:14:12
21 Q. And do you recognize Exhibit 2012? 03:14:14
22 A. Yes. 03:14:18
23 Q. Exhibit 2012 is titled "DDr2 Memories, 03:14:22
24 Comparison and Overview;" correct? 03:14:29
25 A. Yes, it is. 03:14:30

1	Q. And in the upper right of the first	03:14:31
2	page, Exhibit 2012 shows something that we were	03:14:36
3	discussing a little earlier today, which is that,	03:14:41
4	as you move from DDR1 to DDR2 to DDR3, the	03:14:44
5	voltage levels got lower, going from 2.5 volts to	03:14:49
6	1.8 volts to 1.5 volts; correct?	03:14:56
7	A. Yes, that's correct.	03:15:00
8	Q. And Exhibit 2012 states that as a	03:15:01
9	result, that produced less heat and provided more	03:15:04
10	efficiency in power management than the earlier	03:15:10
11	SDRAM chipsets that used 3.3-volt; correct?	03:15:13
12	A. Yes, I see that.	03:15:19
13	Q. And that's consistent with your	03:15:20
14	understanding?	03:15:22
15	A. Sure.	03:15:24
16	Q. On the second page of Exhibit 2012, in	03:15:26
17	the bottom right, you see that there's	03:15:29
18	Figure 2.0.1?	03:15:32
19	A. Yes, I see that.	03:15:37
20	Q. And you see that there's reference to	03:15:38
21	VTT, in both the upper half of Figure 2.0.1 and	03:15:43
22	the bottom half of Figure 2.0.1?	03:15:48
23	A. Yes, I see that.	03:15:52
24	Q. In this Figure 2.0.1 on the second page	03:15:57
25	of Exhibit 2012, VTT is a termination voltage for	03:15:59

1 the DQ data lines; is that fair? 03:16:06

2 A. Yes, that's accurate. 03:16:13

3 Q. And then if you go to the third page of 03:16:15

4 Exhibit 2012, on the bottom left under the 03:16:21

5 heading "VTT and VREF Considerations" -- 03:16:29

6 A. Yes. 03:16:34

7 Q. I guess there's some yellow 03:16:35

8 highlighting, which I didn't put there; someone 03:16:37

9 else put there. 03:16:39

10 But after the yellow highlighting, it 03:16:41

11 states, as I think you just said, each data line 03:16:43

12 is connected to VTT; correct? 03:16:46

13 A. Yes. 03:16:52

14 Q. And that's consistent with Figure 2.0.1 03:16:52

15 on the previous page? 03:16:56

16 A. Yes. 03:16:59

17 Q. And then on the last page of 03:16:59

18 Exhibit 2012, do you see in the upper left 03:17:02

19 there's a heading "Power Sequencing Violations"? 03:17:08

20 It's directly under the table. There's a little 03:17:18

21 heading that says "Power Sequencing Violations." 03:17:20

22 A. Yeah, got it. 03:17:23

23 Q. And so the last page of Exhibit 2012, 03:17:25

24 under the heading Power Sequencing Violations, 03:17:27

25 states, "DDR memories must be powered up in a 03:17:31

1 specific manner. Any violation of the power-up 03:17:35
2 sequencing will result in undefined operations." 03:17:37
3 Did I read that accurately? 03:17:41
4 A. Yes, you did. 03:17:43
5 Q. Is that consistent with your 03:17:45
6 understanding of DDR memories? 03:17:47
7 A. Yes, it is. 03:17:54
8 ATTORNEY CHANDLER: Why don't we take a 03:17:56
9 break. Off the record. 03:17:58
10 THE VIDEOGRAPHER: Off the record at 03:18:02
11 3:17 p.m. Pacific Time. 03:18:03
12 (Recess taken from 3:17 p.m. to
13 3:29 p.m.)
14 THE VIDEOGRAPHER: On the record at 03:29:29
15 3:29 p.m. Pacific Time. 03:29:30
16 BY ATTORNEY CHANDLER: 03:29:32
17 Q. All right. Could you pull up the 03:29:35
18 Hajeck reference, which was -- which I sent to 03:29:41
19 you previously. It's marked as Exhibit 1038. 03:29:44
20 And if you need it in the chat again, let me 03:29:48
21 know. 03:29:50
22 A. No, I have it opened in front of me 03:29:54
23 now. 03:29:56
24 Q. All right. And you've reviewed the 03:30:03
25 Hajeck reference, marked as Exhibit 1038; 03:30:07

1	correct?	03:30:09
2	A. Yes.	03:30:11
3	Q. And please turn to Column 3 of Hajeck	03:30:15
4	around -- starting around line 30.	03:30:20
5	A. I'm there. And upon reflection, I	03:30:25
6	think your pronunciation is likely closer than	03:30:27
7	mine.	03:30:31
8	Q. I wasn't even thinking about it, but	03:30:37
9	all right.	03:30:40
10	So in Column 3, starting around line 30	03:30:52
11	of Hajeck marked as Exhibit 1038, he teaches a	03:30:55
12	voltage detection circuit 48 that's responsible	03:31:00
13	for detecting anomalies in the power signal V-in	03:31:03
14	supplied by the host on line 36; correct?	03:31:09
15	A. Yes, that's correct.	03:31:15
16	Q. And the power anomalies that Hajeck's	03:31:18
17	voltage detection circuit 48 can detect include	03:31:22
18	both when the voltage V-in falls below a certain	03:31:26
19	level, such as 2.6 or 2.7 volts, and also when	03:31:34
20	the voltage exceeds a certain level; correct?	03:31:38
21	A. Yes, I see that.	03:31:58
22	Q. It says -- it would be fair to say that	03:32:00
23	it was known at the time that detection circuits	03:32:03
24	could detect both of those cases when the voltage	03:32:08
25	drops too low or spikes too high?	03:32:12

1	A. Yes.	03:32:18
2	Q. And then at the top of Column 3 of	03:32:20
3	Hajeck, starting around line 5 of Column 3, he	03:32:23
4	describes that there could be a brief	03:32:35
5	interpretation, a drop, an increase or a spike in	03:32:40
6	the voltage V-in supplied by the host 32;	03:32:45
7	correct?	03:32:51
8	A. Yes, I see that.	03:32:52
9	Q. And do you agree that's a fair	03:32:58
10	characterization of things that might happen to a	03:33:00
11	power supply, that the power could have a brief	03:33:05
12	interruption or drop or increase or spike?	03:33:09
13	A. Yes, I do.	03:33:11
14	Q. And then Hajeck goes on to say that the	03:33:14
15	charge pump is preferably designed to protect	03:33:19
16	against sustained voltage drops. In one	03:33:26
17	embodiment, the charge pump is capable of	03:33:31
18	maintaining V-reg at 4.5 volts indefinitely so	03:33:34
19	long as V-in exceeds 0.7 volts; correct?	03:33:43
20	A. Yes, that's correct.	03:33:49
21	Q. And so to be clear, Hajeck is not	03:33:51
22	saying that he has magical way of providing	03:33:53
23	indefinite power when the electricity goes out	03:34:05
24	forever. Instead, what he's referring to is, as	03:34:12
25	long as you have some electricity coming in to	03:34:15

1	the system that's at least 0.7 volts, in his	03:34:19
2	invention, the charge pump can maintain V-reg at	03:34:26
3	5.4 volts indefinitely; is that fair?	03:34:32
4	A. Yes, that fairly characterizes what	03:34:36
5	he's saying here.	03:34:40
6	Q. Could you turn to Exhibit 2101 again,	03:34:41
7	which I believe we spoke about a little bit	03:34:47
8	earlier. Let me know when you have that in front	03:34:55
9	of you.	03:34:56
10	A. I have it open now.	03:35:01
11	Q. Exhibit 2101 is the Fully Buffered DIMM	03:35:02
12	Design Considerations document that you relied	03:35:06
13	upon; correct?	03:35:12
14	A. Yes, that's correct.	03:35:15
15	Q. Could you turn to page 14 of	03:35:17
16	Exhibit 2101. Let me know when you're there.	03:35:24
17	A. I am there.	03:35:28
18	Q. Page 14 of Exhibit 2101 shows an FBDIMM	03:35:29
19	plugged into a riser board that's plugged into a	03:35:37
20	PCI Express slot on the host system that connects	03:35:41
21	to the memory controller; is that correct?	03:35:47
22	A. Yes, I see that.	03:35:50
23	Q. And is that consistent with your	03:35:53
24	recollection of PCI Express, that it would be	03:35:55
25	possible to insert a memory module, like an	03:35:57

1	FBDIMM, into a PCI Express slot?	03:36:00
2	ATTORNEY LINDSAY: Objection; outside	03:36:05
3	the scope of direct, form.	03:36:05
4	THE WITNESS: Hadn't really considered	03:36:17
5	it in much detail. I don't believe that that's	03:36:19
6	accurate, or at least completely accurate, but I	03:36:20
7	hadn't really considered that aspect.	03:36:26
8	BY ATTORNEY CHANDLER:	03:36:28
9	Q. So that's what page 14 of Exhibit 2101	03:36:29
10	shows, is that the FBDIMM can use the PCI Express	03:36:32
11	slot to connect to the memory controller;	03:36:40
12	correct?	03:36:42
13	ATTORNEY LINDSAY: Objection; outside	03:36:44
14	the scope of direct.	03:36:44
15	THE WITNESS: It is showing such a	03:36:47
16	topology, as it says. I don't know that it's	03:36:52
17	actually suggesting that it would be a	03:36:59
18	PCI Express fully conformant slot as opposed to	03:37:01
19	simply a -- physical characteristics. There	03:37:07
20	certainly are enough -- well, I guess I'll leave	03:37:11
21	that part alone -- or whether there's any active	03:37:14
22	components on the riser board doing any physical	03:37:17
23	or electric translation.	03:37:23
24	So yeah, that's suggesting, the	03:37:28
25	simplified view there, that, in essence the	03:37:32

1 FBDIMM could be plugged into a PCI Express slot, 03:37:35
2 and I know that's not the case. 03:37:40
3 So yeah, I could imagine one could 03:37:43
4 build a system that had a lot of these 03:37:47
5 characteristics. But there's an awful lot of 03:37:49
6 details that are missing, some of which would 03:37:50
7 make -- if you chose wrong, make this not work. 03:37:51
8 BY ATTORNEY CHANDLER: 03:37:54
9 Q. Could you continue to the Spiers 03:37:55
10 reference, which is Exhibit 1025. 03:37:58
11 A. Yes, I have that open in front of me. 03:38:10
12 Q. And you have reviewed the Spiers 03:38:12
13 reference; correct? 03:38:15
14 A. Yes, I have. 03:38:18
15 Q. And in your expert declaration, marked 03:38:19
16 as Exhibit 2031, could you turn to paragraph 134, 03:38:26
17 which also, in your other expert declaration, is 03:38:39
18 also paragraph 134. 03:39:05
19 A. Yes, I am there. 03:39:06
20 Q. In your opinion, a person of ordinary 03:39:12
21 skill in the art would understand that Spiers 03:39:13
22 requires five voltages; is that fair? Or I 03:39:18
23 should say at least five voltages. 03:39:28
24 A. Can you narrow it down to where you're 03:39:32
25 looking -- I'm sorry. 03:39:35

1 Q. In your opinion, a person of ordinary 03:39:38
2 skill in the art reading Spiers would understand 03:39:40
3 that Spiers requires at least five voltages, 03:39:42
4 which you have numbered 1 through 5; is that 03:39:47
5 fair? 03:39:50

6 And I may have -- you know, I know 03:39:57
7 what's going on, which is a little confusing. 03:40:05

8 Your numbering -- paragraph numbering 03:40:08
9 restarts in your declaration. So there are two 03:40:10
10 paragraph 134s. 03:40:15

11 A. I think I noticed that previously as 03:40:16
12 well. Which page are you on? How about that? 03:40:19

13 Q. Page 86 of Exhibit 2031, which is also 03:40:24
14 page 80 of Exhibit 2061 -- well, shucks. 03:40:32

15 The page number is inconsistent in 03:40:42
16 Exhibit 2061. In Exhibit 2061 it would be 03:40:45
17 page 81, using the stamp in the bottom right 03:40:48
18 corner of Exhibit 2061. 03:40:51

19 A. I'm on 2031. So if we can just 03:40:53
20 localize to that, hopefully we'll reduce the 03:40:57
21 number of confusions based on the renumbering. 03:41:00

22 Q. And I -- I believe that your opinions 03:41:02
23 are materially the same in this regard in the two 03:41:07
24 expert declarations. 03:41:12

25 So on pages 86, carrying over to 87, 03:41:13

1	Exhibit 2031, you express the opinion that a	03:41:18
2	person of ordinary skill in the art, reading	03:41:23
3	Spiers, would understand that at least five	03:41:26
4	voltages are required, which you have numbered 1	03:41:30
5	through 5; correct?	03:41:34
6	A. Yes, that's correct.	03:41:35
7	Q. The first voltage is the operating	03:41:41
8	voltage for the volatile memory; correct?	03:41:43
9	A. Correct.	03:41:47
10	Q. Second voltage is the operating voltage	03:41:48
11	of the nonvolatile memory; correct?	03:41:50
12	A. Correct.	03:41:54
13	Q. The third voltage is the voltage for	03:41:54
14	the bus I/O between the FPGA and the volatile	03:41:57
15	memory; correct?	03:42:03
16	A. That's correct.	03:42:05
17	Q. And the fourth voltage is the voltage	03:42:07
18	of the bus I/O between the FPGA and the	03:42:09
19	nonvolatile memory; correct?	03:42:11
20	A. Correct.	03:42:14
21	Q. And the fifth voltage is the voltage	03:42:15
22	required for the FPGA core, which you indicate is	03:42:21
23	1.8 volts in this example; is that correct?	03:42:25
24	A. That's correct.	03:42:30
25	Q. Now, as we discussed earlier today, at	03:42:40

1	the time of the invention, there was known in the	03:42:45
2	art different types of volatile memory, including	03:42:49
3	DDR1, DDR2, DDR3, and others, that operated at	03:42:55
4	different voltages; is that fair?	03:43:01
5	A. Yes, that's fair.	03:43:06
6	Q. And similarly, nonvolatile memory --	03:43:08
7	there also was known in the art at the time	03:43:11
8	different types of nonvolatile memory that could	03:43:17
9	operate at different voltages; is that fair?	03:43:21
10	A. Yes, that's correct.	03:43:28
11	Q. And there was also known in the art at	03:43:29
12	the time different FPGAs that could operate at	03:43:34
13	different voltages; correct?	03:43:39
14	A. That's correct. A number of different	03:43:44
15	types of FPGAs were known, operating at very	03:43:47
16	different voltage levels.	03:43:50
17	Q. All right. Could you go back to	03:43:52
18	Spiers, which is Exhibit 1025, and let me know	03:43:55
19	when you've got it back up.	03:44:04
20	A. I have it open.	03:44:10
21	Q. And it may actually be useful to use	03:44:50
22	your annotation of Spiers, in paragraph 46 of	03:44:53
23	your declarations, where you annotate Figure 5 of	03:45:01
24	Spiers.	03:45:12
25	(Clarification by reporter.)	03:45:20

1	Q. Do you have that annotation in mind,	03:45:22
2	Dr. Mangione-Smith?	03:45:27
3	A. Yeah. This was paragraph 133, 134? Is	03:45:27
4	that what you're referring to?	03:45:33
5	Q. No, paragraph 46 in both of your expert	03:45:34
6	declarations. You provide an annotated color	03:45:39
7	version of Figure 5 of Spiers.	03:45:42
8	A. Yeah, I actually think it's the same	03:45:52
9	figure that I just reproduce later on. But we're	03:45:54
10	in the same place now, in any case.	03:45:57
11	Q. Does Spiers teach an input voltage that	03:46:01
12	can be 5 volts?	03:46:07
13	A. You mean an input voltage to the whole	03:46:15
14	PCI card, I assume?	03:46:18
15	Q. Yeah, coming across the edge	03:46:20
16	connections, which I think are 172.	03:46:22
17	A. Yeah. I believe those are -- at	03:46:27
18	that -- right, we've seen that as 5 volts or	03:46:30
19	3.3 volts in some circumstances. So sure.	03:46:34
20	Q. And that's what I was getting at, is --	03:46:38
21	I guess Spiers is a type of PCI card, meaning	03:46:40
22	that the standard voltages for PCI cards included	03:46:44
23	5 volts and 3.3 volts coming across the edge	03:46:50
24	connections at the bottom of memory module; is	03:46:55
25	that fair?	03:46:59

4	Q. And if you sort of really zoom in, into	03:47:09
5	your annotation of Figure 5, 202 is a 5-volt	03:47:13
6	detector; is that correct?	03:47:20

8	Q. And what does that do?	03:47:31
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14	Q. Well, if it's helpful to you, if you'd	03:47:48
15	turn back to Spiers, Exhibit 1025, at the bottom	03:47:50
16	of page 19, carrying over to the top of page 20,	03:47:53
17	which is paragraph 37, Spiers talks about that	03:47:57
18	element. And why don't you take a look and then	03:48:02
19	explain to me what you think is going on there.	03:48:06

21	A. You said 135, going on top of -- I'm	03:49:01
22	sorry. Did you say --	03:49:04

23	Q. Paragraph 37 of Spiers, marked as	03:49:10
24	Exhibit 1025, which starts at the bottom of	03:49:12
25	page 19 of the exhibit and carries to the top of	03:49:15

1 page 20 of the exhibit, it refers to 202 and 03:49:18
2 talks about it a little. If you've had an 03:49:22
3 opportunity to look at that, could you tell us 03:49:26
4 your understanding of what Spiers is disclosing 03:49:29
5 there. 03:49:31

6 A. I'll do that now. I apologize. I was 03:49:31
7 looking at 137, which then carries over to the 03:49:33
8 next -- I'm sorry. I was referring to 135 -- the 03:49:36
9 day is getting late. Let me catch my breath. 03:49:40

10 I had been reviewing paragraph 35, 03:49:43
11 which carries over to the next column, not 03:49:46
12 paragraph 37. But I will, now that I'm correctly 03:49:49
13 oriented, do that, look at 37. 03:49:53

14 (Witness reviews document.) 03:49:59

15 A. Sure. So it's receiving power, I guess 03:50:46
16 I would say, over the PCI bus during normal 03:50:49
17 operations. And then there's this 5-volt PCI 03:50:56
18 detector element 202, which is used to determine 03:51:01
19 when to switch over to the capacitor array. 03:51:04

20 Q. Okay. So I want to focus for now 03:51:10
21 during normal operation, when the host system has 03:51:14
22 power and there's not a power outage. 03:51:20

23 So do you have that in mind? 03:51:23

24 A. Understood. 03:51:24

25 Q. And I'm looking now at your annotation 03:51:27

1 of Figure 5 of Spiers, which shows a FPGA 03:51:29
2 processor 198 in red, some NAND flash in green, 03:51:37
3 and some SDRAM in yellow. 03:51:41

4 Do you see all of that? 03:51:49

5 A. Yes, I do. 03:51:50

6 Q. And I think, as we discussed a moment 03:51:51
7 ago, when you're talking about the 5 volts that 03:51:59
8 Spiers would need, the FPGA processor 198 would 03:52:06
9 need 1.8 volts; is that correct? 03:52:10

10 A. Yes. 03:52:17

11 Q. And then the SDRAM, that could be 03:52:17
12 3.3 volts; is that correct? 03:52:24

13 A. That's my recollection, yes. 03:52:29

14 Q. So during normal operation, Spiers 03:52:31
15 would need to take the 5-volt input from the host 03:52:33
16 system and step it down to 3.3 volts for the 03:52:40
17 SDRAM; is that fair? 03:52:43

18 A. Yes. 03:52:47

19 Q. And similarly, the NAND flash in 03:52:48
20 green -- remind me, is that 3 volts, 3.3 volts or 03:52:54
21 a different voltage? 03:53:00

22 A. I don't recall how they characterized 03:53:03
23 it. And, of course, over the years there have 03:53:05
24 been different voltage settings. So I'm sorry, I 03:53:08
25 don't recall what voltage was assigned for the 03:53:14

1	NAND flash.	03:53:19
2	Q. Would it be fair that either 3 or	03:53:21
3	3.3 volts would be a common voltage for NAND	03:53:24
4	flash?	03:53:27
5	A. Yes.	03:53:29
6	Q. And so during normal operations, Spiers	03:53:29
7	would need to step down the 5-volt input to	03:53:32
8	either 3 or 3.3 volts to work with the voltage of	03:53:37
9	the NAND flash?	03:53:44
10	A. Yes.	03:53:45
11	Q. Okay. Could you look at Figure 3 of	03:53:52
12	Spiers, so -- in Exhibit 1025.	03:53:55
13	A. Okay, I have that.	03:54:16
14	Q. All right. Figure 3 shows storage	03:54:18
15	controller 132 at the top; a bus 128 in the	03:54:20
16	middle; a storage device 140 in the bottom left	03:54:26
17	that includes a write-back cache 148; and a	03:54:31
18	backup device 144 in the bottom right; correct?	03:54:35
19	A. Yes, that's correct.	03:54:40
20	Q. And Figure 5 of Spiers corresponds to	03:54:47
21	the backup device 144 in Figure 3; is that fair?	03:54:52
22	A. Yes, that's my recollection.	03:54:59
23	Q. And so Figure 5 in Spiers is separate	03:55:03
24	from the write-back cache 148 in Figure 3; is	03:55:07
25	that accurate?	03:55:12

1	A. Yes, that's accurate.	03:55:15
2	Q. Dr. Mangione-Smith, Netlist did not	03:55:30
3	invent SDRAM memory devices; correct? Those were	03:55:33
4	known before the '918 and '054 patents?	03:55:38
5	A. Yes, that's correct. Synchronous DRAM	03:55:42
6	devices were known prior to those two patents.	03:55:47
7	Q. Netlist did not invent DDR1 SDRAM	03:55:50
8	memory devices; correct?	03:55:56
9	A. To the best of my knowledge, they did	03:55:59
10	not -- they don't claim to have invented DDR1	03:56:01
11	memory.	03:56:05
12	Q. And Netlist did not invent DDR or DDR3	03:56:08
13	SDRAM memory devices either; correct?	03:56:12
14	A. Not by themselves, no. I don't believe	03:56:20
15	they claim to have invented those.	03:56:22
16	Q. And Netlist did not invent nonvolatile	03:56:24
17	memory; correct?	03:56:28
18	A. I think that's true. In general,	03:56:31
19	nonvolatile memory was known prior to either of	03:56:34
20	the two inventions at issue here.	03:56:37
21	Q. Netlist did not invent the printed	03:56:44
22	circuit board or the memory module; correct?	03:56:47
23	A. That is correct.	03:56:52
24	Q. Netlist did not invent edge connections	03:56:55
25	on a memory module to plug into a host computer;	03:56:57

1	correct?	03:57:01
2	A. That's correct. The notion of edge	03:57:05
3	connections to connect a module to a host	03:57:07
4	computer were known prior to the priority dates	03:57:11
5	of these two patents at issue.	03:57:15
6	Q. Netlist did not invent buffered DIMM	03:57:20
7	memory modules; correct? Those existed before,	03:57:25
8	such as FBDIMM; right?	03:57:32
9	A. Sure. FBDIMM were known before.	03:57:35
10	Q. Netlist did not invent the RDIMM memory	03:57:40
11	module; correct?	03:57:45
12	A. Netlist did not invent all aspects of	03:57:47
13	the RDIMM on their own, that's true.	03:57:50
14	Q. Netlist did not invent buck converters;	03:57:53
15	correct?	03:57:56
16	A. To the best of my knowledge, Netlist	03:58:00
17	did not invent the concept of buck converters.	03:58:02
18	Q. Netlist did not invent dual buck	03:58:08
19	converters; correct?	03:58:11
20	A. I would say that is correct, to the	03:58:14
21	best of my knowledge.	03:58:16
22	Q. Netlist did not invent LDO linear	03:58:17
23	regulators; correct?	03:58:22
24	A. That's correct to the best of my	03:58:25
25	knowledge, they did not.	03:58:28

1 Q. Netlist was not the first to put a 03:58:29
2 voltage converter on a DIMM memory module; 03:58:32
3 correct? For example, Harris did that earlier; 03:58:36
4 correct? 03:58:43

5 A. Harris talked about it. I don't know 03:58:48
6 if Harris actually -- you said they were not the 03:58:53
7 first to do that. Harris talked about the 03:58:57
8 concept. I don't know if Harris actually did 03:59:02
9 what he talked about at all. 03:59:08

10 But also, there was the BBvault product 03:59:11
11 which -- I don't remember the date, but that was 03:59:20
12 much earlier than the two patents, I believe. 03:59:22
13 Well, I don't recall that date. 03:59:25

14 I don't know whether they were the 03:59:26
15 first to put a voltage converter on a memory 03:59:28
16 module or not. 03:59:30

17 Q. Netlist did not invent a circuit for 03:59:33
18 detecting and protecting against overvoltage 03:59:37
19 conditions; correct? 03:59:45

20 A. The concept of overvoltage detection 03:59:49
21 and circuitry for implementing that function was 03:59:53
22 known, certainly, prior to the priority date of 03:59:57
23 the two patents at issue here. 04:00:01

24 Q. And similarly, Netlist did not invent 04:00:06
25 undervoltage protection; correct? 04:00:12

1	A. Yes. I would give a similar answer	04:00:15
2	compared to the one I gave for overvoltage.	04:00:19
3	Q. Do you have any corrections or	04:00:28
4	clarifications you would like to make to any of	04:00:29
5	your testimony earlier today?	04:00:32
6	A. Not that occurs to me as I sit here.	04:00:39
7	ATTORNEY CHANDLER: All right. Then I	04:00:41
8	pass the witness.	04:00:42
9	ATTORNEY LINDSAY: Okay. I'm going to	04:00:45
10	need a little time. Take 15 minutes and then see	04:00:46
11	how it goes.	04:00:53
12	ATTORNEY CHANDLER: Okay. Sounds good.	04:00:55
13	THE VIDEOGRAPHER: Off the record,	04:00:57
14	Counsel? Off the record at 4:00 p.m. Pacific	04:00:58
15	Time.	04:01:02
16	ATTORNEY CHANDLER: We would like the	04:11:38
17	final transcript by Thursday, June 15th.	04:11:40
18	THE COURT REPORTER: And you want the	04:11:59
19	rough draft?	04:11:59
20	ATTORNEY CHANDLER: Yeah, that's sort	04:12:01
21	of less important. You don't have to spend that	04:12:02
22	much time on it, but yeah, we'll take a rough.	04:12:04
23	(Recess taken from 4:00 p.m. to	
24	4:41 p.m.)	
25	THE VIDEOGRAPHER: On the record at	04:41:43

1 4:41 p.m. Pacific Time.

04:41:44

2

04:41:46

3

EXAMINATION

04:41:46

4

BY ATTORNEY LINDSAY:

04:41:47

5

Q. Dr. Mangione-Smith, can you turn to

04:41:50

6

your declaration. It's paragraph 31. I'm in the

04:41:51

7

Exhibit 2031 for the '918, but it's the same in

04:41:58

8

either one.

04:42:04

9

A. I've got that open. Which paragraph

04:42:06

10

did you say? Sorry.

04:42:08

11

Q. 31.

04:42:11

12

A. 31, okay. Yes, I'm there.

04:42:12

13

Q. Okay. Do you recall discussing this

04:42:18

14

paragraph earlier today?

04:42:23

15

A. Yes, I do.

04:42:25

16

Q. The first sentence, does that read,

04:42:28

17

"FBDIMM uses packetized serial signaling to

04:42:31

18

exchange data, address and control information

04:42:37

19

with the host"?

04:42:39

20

A. Yes, sir, that's what it says.

04:42:47

21

Q. And skipping over the next sentence,

04:42:49

22

I'm going to read the third sentence, and it

04:42:50

23

says, "This is evident from the pinout of the

04:42:53

24

DIMM."

04:42:56

25

Did I read that correctly?

04:42:56

1	A. Yes, you did.	04:43:00
2	Q. Okay. And then the next sentence I'll	04:43:01
3	read, and you let me know if I read it correctly.	04:43:05
4	It says: "As such, the AMB receives data,	04:43:07
5	address and control information, decodes it, and	04:43:12
6	generates the data, address, and control signals	04:43:15
7	needed by the DDR2 SDRAMs."	04:43:17
8	A. Yes, you read that correctly.	04:43:20
9	Q. Okay. On the next page -- it's the	04:43:26
10	same paragraph, there's a table entitled	04:43:33
11	"Advanced Memory Buffer Pin Description."	04:43:35
12	A. Yes, I see that.	04:43:39
13	ATTORNEY CHANDLER: I'm sorry.	04:43:42
14	Objection; outside the scope of cross.	04:43:43
15	BY ATTORNEY LINDSAY:	04:43:45
16	Q. What is this table describing?	04:43:46
17	ATTORNEY CHANDLER: Objection; outside	04:43:49
18	the scope of cross.	04:43:49
19	THE WITNESS: This table is describing	04:43:53
20	a number of pins that are used to move signals	04:43:56
21	between the host memory controller and the	04:44:02
22	FBDIMM.	04:44:05
23	BY ATTORNEY LINDSAY:	04:44:08
24	Q. Are there any pins that are dedicated	04:44:08
25	to data signals shown in the table in -- that you	04:44:10

1	just described?	04:44:17
2	ATTORNEY CHANDLER: Objection; outside	04:44:19
3	the scope of cross.	04:44:19
4	THE WITNESS: No, I don't believe so.	04:44:24
5	BY ATTORNEY LINDSAY:	04:44:26
6	Q. Are there any dedicated address pins in	04:44:27
7	the table that you just described?	04:44:30
8	ATTORNEY CHANDLER: Objection; outside	04:44:35
9	the scope of cross.	04:44:35
10	THE WITNESS: No. There are no	04:44:38
11	dedicated address signal pins shown in this	04:44:40
12	table.	04:44:43
13	BY ATTORNEY LINDSAY:	04:44:44
14	Q. And are there any dedicated control	04:44:47
15	signal pins shown in the table?	04:44:50
16	ATTORNEY CHANDLER: Objection; outside	04:44:54
17	the scope of cross.	04:44:54
18	THE WITNESS: No, there are no	04:44:57
19	dedicated control signal pins shown in this	04:44:58
20	table.	04:45:01
21	BY ATTORNEY LINDSAY:	04:45:03
22	Q. Okay. So if I could just go back up to	04:45:03
23	the paragraph we were reading a moment ago, go to	04:45:05
24	the next sentence. I want to get your	04:45:09
25	understanding of this next sentence. And I'll	04:45:14

1 read it. It says, "This can be seen from the 04:45:17
2 fact that the pin description for the AMB, there 04:45:19
3 are dedicated pins for data, address or control 04:45:22
4 under the heading for 'FBDIMM Channel Signals'. " 04:45:25
5 A. I'm sorry. Where were you reading? 04:45:32
6 From the previous page? 04:45:35
7 Q. Yes, from page 15, paragraph 31. The 04:45:36
8 same paragraph we were reading from a moment ago. 04:45:42
9 A. Yes, I see that. 04:45:50
10 Q. Okay. So you just -- you just talked 04:45:52
11 about the table below this paragraph, that this 04:45:58
12 paragraph is describing. Was that your intent? 04:46:01
13 ATTORNEY CHANDLER: Objection; leading. 04:46:09
14 THE WITNESS: No, because there are 04:46:10
15 signals coming -- there are pins coming in to the 04:46:16
16 AMB and then the decoded signal pins going out. 04:46:20
17 So there are dedicated address control 04:46:28
18 and signal pins that exit the AMD but not that 04:46:33
19 enter into them. 04:46:41
20 BY ATTORNEY LINDSAY: 04:46:41
21 Q. Right. What I'm trying to get at is if 04:46:42
22 there's a typo in the sentence that I read a 04:46:45
23 moment ago. 04:46:47
24 A. Yeah, I'm trying to get to that too, by 04:46:48
25 taking a step away from it and describing in a 04:46:50

1 larger sense what I meant to say. 04:46:53

2 Yeah, it appears to me -- I say that it 04:47:07
3 receives and decodes the address, data, and 04:47:17
4 control information, and thus -- right. There 04:47:24
5 are -- there are no -- it should have said the 04:47:40
6 information is exchanged between the AMB, and the 04:47:42
7 host, not the signals exchanged between the AMB 04:47:47
8 and the host. 04:47:50

9 Q. Okay. Thank you. 04:47:55

10 A. And if I could just add, I think an 04:47:56
11 answer or two before I said "AMD" by mistake, and 04:48:01
12 it should have been AMB. 04:48:05

13 Q. Okay. And then in paragraph 32, if you 04:48:10
14 would scroll down and describe for me briefly 04:48:11
15 what you see in this table. 04:48:17

16 ATTORNEY CHANDLER: Objection; outside 04:48:22
17 the scope of cross, and leading. 04:48:22

18 THE WITNESS: This table is showing the 04:48:29
19 signals used to interface to a DDR2 memory 04:48:31
20 device, including specific data lines, address 04:48:36
21 lines, and various control lines. 04:48:42

22 BY ATTORNEY LINDSAY: 04:48:46

23 Q. So is it the case that this -- strike 04:48:47
24 that. 04:48:49

25 Does this table show dedicated data, 04:48:50

1 control, and address signals? 04:48:55

2 A. Yes. It shows dedicated data, control, 04:49:07
3 and address signals from the AMB to the DDR2 04:49:09
4 memory devices. 04:49:17

5 Q. Okay. Earlier today Mr. Chandler asked 04:49:24
6 you a question and you gave an answer. I was 04:49:34
7 just going to read it so that we're all on the 04:49:37
8 same page. 04:49:41

9 The question: "And how would you 04:49:45
10 explain some of the major characteristics of the 04:49:48
11 architecture structure of an FBDIMM?" 04:49:50

12 "I would say that with an FBDIMM, 04:49:53
13 all of the signals from the address 04:49:57
14 command and clock and control and the 04:49:59
15 data signals and the DQSs are directed 04:50:01
16 first to a block called the AMD and 04:50:05
17 thus -- sorry -- AMB -- and thus, 04:50:08
18 electrically separated or isolated from 04:50:11
19 the DRAM circuits themselves." 04:50:14

20 Do you recall that? 04:50:21

21 A. Yes, I recall that. 04:50:22

22 Q. Is it the case that -- can you explain 04:50:28
23 to us what you meant by that, since it seems to 04:50:34
24 be discussing signals rather than the information 04:50:41
25 you just described. 04:50:43

1	ATTORNEY CHANDLER: Objection; leading.	04:50:44
2	THE WITNESS: Yes. What I meant, and	04:50:47
3	what I think in most of the other places I've	04:50:49
4	been consistent in expressing, is that the	04:50:53
5	address, data, and control information is being	04:50:56
6	sent from the host to the AMB but not over	04:50:58
7	address, data, control signals, signal pins.	04:51:06
8	It's being translated into another set of signals	04:51:15
9	received by the AMB and then, as I mentioned,	04:51:18
10	decoded and translated back into a specific set	04:51:21
11	of signals for the DDR2 SDRAM.	04:51:26
12	BY ATTORNEY LINDSAY:	04:51:34
13	Q. Okay. And I just want to go to another	04:51:34
14	question to see if we can clarify your answer	04:51:38
15	here as well.	04:51:44
16	The question was: "So when the host	04:51:45
17	computer wants to send a read or write command	04:51:48
18	for, if I remember DIMM, that read or write	04:51:52
19	command" -- rough translation here -- "and the	04:51:56
20	associated address information is sent as	04:51:59
21	packetized serial signals; correct?"	04:52:02
22	Answer: "Yes, that's correct."	04:52:06
23	What did you understand Mr. Chandler's	04:52:12
24	question to be asking?	04:52:15
25	ATTORNEY CHANDLER: Objection; leading.	04:52:19

1	THE WITNESS: Yeah, I was thinking	04:52:23
2	about the information contained for the address,	04:52:24
3	data, and control. They're sent over a set of	04:52:27
4	signal wires, but it's signal wires that are not	04:52:34
5	dedicated to address, data or control but are	04:52:39
6	used for a wide variety of purposes.	04:52:41
7	So the information passes over that,	04:52:45
8	and then signals carrying that information are	04:52:48
9	regenerated and sent on to the DDR2 SDRAM chips.	04:52:52
10	BY ATTORNEY LINDSAY:	04:53:01
11	Q. Okay. Thank you. Can we go over to,	04:53:01
12	now, Exhibit 1027.	04:53:05
13	A. Yes, I have 1027, the FBDIMM document,	04:53:25
14	opened in front of me.	04:53:28
15	Q. On page 1, Mr. Chandler asked you about	04:53:31
16	your opinion on a sentence earlier today. I just	04:53:34
17	want to read the sentence first.	04:53:38
18	"All memory control for the DRAM	04:53:42
19	resides in the host, including memory	04:53:45
20	request initiation, timing, refresh,	04:53:47
21	scrubbing, sparing -- or sparring --	04:53:51
22	configuration access and power	04:53:54
23	management."	04:53:56
24	Do you remember discussing that	04:53:58
25	sentence with Mr. Chandler?	04:53:59

1	A. Yes, I do.	04:54:01
2	Q. Did you indicate you didn't agree with	04:54:06
3	that sentence?	04:54:08
4	A. Yeah.	04:54:13
5	Q. And why is that?	04:54:14
6	A. Well, the host communicates to the DRAM	04:54:16
7	through the AMB. And so if the AMB is -- is	04:54:23
8	misconfigured not to take some particular action,	04:54:29
9	it doesn't matter what the host says; the -- that	04:54:33
10	won't -- that action won't be taken. If the AMB	04:54:36
11	is in some way faulty or operating outside of its	04:54:39
12	design range -- maybe the temperature is too	04:54:47
13	hot -- it will not interpret those commands from	04:54:50
14	the host correctly and cause the correct set of	04:54:54
15	steps to occur on the DIMM.	04:55:01
16	So while it's true that I think the	04:55:03
17	vast majority, if not all, of the actions --	04:55:10
18	well, let me just say, the vast majority of the	04:55:12
19	actions, the commands, will originate from the	04:55:15
20	host controller, just doing a -- starting a read	04:55:17
21	or write operation, the most common operations,	04:55:20
22	the AMB plays a fundamental role in controlling	04:55:23
23	them as well. That was all I meant.	04:55:28
24	Q. Okay. Let's move to Exhibit 1048 if we	04:55:34
25	can. And I'm looking at page 2 of 1048.	04:55:40

1	A. Yes, I have that open in front of me.	04:55:50
2	Q. There's a block diagram that's	04:55:55
3	called -- it's under the number 6 and it just	04:55:58
4	says "Block Diagram."	04:56:00
5	You recall discussing this earlier	04:56:02
6	today?	04:56:03
7	A. Yeah, I do.	04:56:04
8	Q. How many input voltages are being	04:56:08
9	provided to this -- this circuitry?	04:56:10
10	ATTORNEY CHANDLER: Objection; leading,	04:56:18
11	and outside the scope of direct.	04:56:18
12	THE WITNESS: So as I read it, it's got	04:56:24
13	two different input voltages, one going to the	04:56:26
14	top circuitry and being used to generate V-out1;	04:56:32
15	and one going to the bottom and being used, in	04:56:40
16	part, to generate V-out2.	04:56:44
17	BY ATTORNEY LINDSAY:	04:56:50
18	Q. The circuitry in the middle of that	04:56:54
19	diagram is receiving one input voltage and	04:56:57
20	outputting two output voltages.	04:57:07
21	Is that a fair characterization?	04:57:12
22	ATTORNEY CHANDLER: Objection to form;	04:57:15
23	and objection, leading.	04:57:15
24	THE WITNESS: Yes, it is.	04:57:18
25		

1	BY ATTORNEY LINDSAY:	04:57:19
2	Q. The circuitry that's in the middle of	04:57:22
3	the block diagram is outputting how many	04:57:23
4	voltages?	04:57:27
5	ATTORNEY CHANDLER: Same objections;	04:57:32
6	form and leading.	04:57:32
7	THE WITNESS: It's outputting something	04:57:35
8	labeled V-out2; and then that output also goes	04:57:37
9	through 2.5-volt LDO to generate V-out3.	04:57:43
10	BY ATTORNEY LINDSAY:	04:57:49
11	Q. Did you testify earlier today that that	04:57:50
12	middle circuitry was -- resembled a buck	04:57:52
13	converter?	04:57:57
14	A. Yes, I believe I did.	04:58:01
15	Q. And in this example, this buck	04:58:06
16	converter circuitry is receiving one input	04:58:08
17	voltage and outputting two output voltages?	04:58:12
18	ATTORNEY CHANDLER: Objection; form and	04:58:17
19	leading.	04:58:18
20	THE WITNESS: Yes, it's receiving one	04:58:20
21	input voltage, and it's producing two output	04:58:22
22	voltages.	04:58:26
23	BY ATTORNEY LINDSAY:	04:58:37
24	Q. I want to turn to a different exhibit,	04:58:37
25	Exhibit 2101. And I'm looking at page 14.	04:58:41

1	A. Yes, I'm there with you.	04:58:55
2	Q. Does this slide show a memory module?	04:59:03
3	A. Yes, it appears to. It points to an	04:59:10
4	FBDIMM, which would be an example of a memory	04:59:12
5	module.	04:59:15
6	Q. Is the memory riser board part of that	04:59:20
7	memory module?	04:59:25
8	ATTORNEY CHANDLER: Objection; form.	04:59:28
9	THE WITNESS: No, it's not.	04:59:30
10	BY ATTORNEY LINDSAY:	04:59:34
11	Q. I want to turn back to your	04:59:51
12	declaration. And I'm looking at paragraph 80	04:59:56
13	of -- this is Exhibit 2031, but it's the same in	04:59:57
14	the other one, I believe.	05:00:01
15	A. Okay. I'm at paragraph 80 of	05:00:14
16	Exhibit 2031.	05:00:17
17	Q. Just give you a second to -- to recall	05:00:26
18	the paragraph.	05:00:33
19	ATTORNEY CHANDLER: Objection as	05:00:37
20	outside the scope and leading.	05:00:39
21	THE WITNESS: Yes, I see it.	05:00:40
22	BY ATTORNEY LINDSAY:	05:00:45
23	Q. In the first sentence it states that	05:00:46
24	"it was known for a single buck converter to	05:00:49
25	generate four outputs."	05:00:52

1	ATTORNEY CHANDLER: Objection; outside	05:00:57
2	the scope of cross, and leading.	05:00:57
3	THE WITNESS: Yes, I see that.	05:01:01
4	BY ATTORNEY LINDSAY:	05:01:02
5	Q. Do you provide a couple of citations,	05:01:04
6	then, for that statement?	05:01:06
7	ATTORNEY CHANDLER: Objection; outside	05:01:11
8	the scope -- sorry -- objection; outside the	05:01:11
9	scope of cross, and leading.	05:01:13
10	THE WITNESS: Sorry about that.	05:01:16
11	Yes, it -- there are a couple of	05:01:17
12	examples and further discussion of a four-output	05:01:19
13	buck converter.	05:01:25
14	BY ATTORNEY LINDSAY:	05:01:26
15	Q. And this would have been before the	05:01:32
16	time of invention of the '918 and '054 patent?	05:01:36
17	ATTORNEY CHANDLER: Objection; outside	05:01:44
18	the scope of cross, and leading.	05:01:44
19	THE WITNESS: Yes, that's my	05:01:49
20	recollection.	05:01:51
21	ATTORNEY LINDSAY: Okay. I don't have	05:01:51
22	any other questions.	05:01:55
23	ATTORNEY CHANDLER: Let's go off the	05:01:59
24	record, please.	05:02:00
25	THE VIDEOGRAPHER: Off the record at	05:02:04

1	5:01 p.m. Pacific Time.	05:02:05
2	(Recess taken from 5:01 p.m. to	
3	5:15 p.m.)	
4	THE VIDEOGRAPHER: On the record at	05:15:43
5	5:15 p.m. Pacific Time.	05:15:44
6		05:15:45
7	FURTHER EXAMINATION	05:15:45
8	BY ATTORNEY CHANDLER:	05:15:46
9	Q. Dr. Mangione-Smith, when I was asking	05:15:48
10	you questions throughout the morning and	05:15:49
11	afternoon, I gave you the opportunity several	05:15:53
12	times to let me know if you had any corrections	05:15:55
13	or clarifications; correct?	05:16:00
14	A. Yes.	05:16:06
15	Q. And you did not provide me any	05:16:06
16	corrections or clarifications when I asked you if	05:16:08
17	you had any corrections or clarifications;	05:16:14
18	correct?	05:16:16
19	A. That's my recollection, yes.	05:16:17
20	Q. And in preparation for your deposition	05:16:19
21	today, you spent approximately 20 hours in the	05:16:21
22	last week or two preparing; right?	05:16:25
23	A. Yes, I believe that's what I said	05:16:28
24	earlier in the day.	05:16:30
25	Q. And you felt that you were well	05:16:31

1 prepared for your deposition to give me your best
2 testimony in response to the questions I asked
3 you this morning and afternoon; correct?

05:16:34

05:16:40

05:16:42

4 A. Yes. But I think, as we saw in a few
5 circumstances, I tripped over paragraph 135 or 35
6 and 37. But yes, I felt prepared enough to give
7 you my best and honest effort.

05:16:48

05:16:51

05:16:56

05:16:59

8 Q. And after I finished asking my
9 questions, you spoke with counsel for Netlist on
10 the telephone; right?

05:17:03

05:17:07

05:17:11

11 ATTORNEY LINDSAY: Just caution the
12 witness not to discuss the substance of any
13 conversations with counsel. You can answer as to
14 the fact that a discussion may or may not have
15 occurred but not to the substance of that
16 conversation.

05:17:13

05:17:14

05:17:16

05:17:19

05:17:22

05:17:25

17 THE WITNESS: Yes, there was a
18 discussion over the telephone.

05:17:27

05:17:28

19 BY ATTORNEY CHANDLER:

05:17:30

20 Q. And it lasted for approximately 30
21 minutes or so; is that fair?

05:17:31

05:17:33

22 A. I thought it was shorter than that, but
23 to be honest with you, I'm not sure.

05:17:37

05:17:39

24 Q. And then after that discussion you had
25 with counsel for Netlist, we went back on the

05:17:42

05:17:45

1 record and counsel for Netlist asked you redirect 05:17:49
2 questions; and as part of your redirect 05:17:52
3 testimony, you changed some of the things that 05:17:56
4 you had told me earlier in the day; correct? 05:17:58

5 A. Yes. My recollection is that he read a 05:18:03
6 couple of examples of the answers I had given 05:18:08
7 that gave me an opportunity to consider whether I 05:18:11
8 had stumbled over a phrase or something, sure. 05:18:17

9 (Exhibit Number 1042 was previously 05:19:17
10 marked for identification.) 05:19:17

11 BY ATTORNEY CHANDLER: 05:18:20

12 Q. Could you pull up two exhibits, and 05:18:21
13 it's probably going to help to put them side by 05:18:27
14 side. 05:18:29

15 The first is Exhibit 1048, page 2; and 05:18:30
16 the second is Exhibit 1042, and -- which -- both 05:18:39
17 of those exhibits are the same in the two IPRs. 05:18:51
18 And I'll put Exhibit 1042 in the chat, in case 05:18:57
19 you don't have it handy. 05:19:02

20 A. Great. 05:19:04

21 Q. And what may be helpful to you is, 05:19:07
22 first, let me know when you have the two exhibits 05:19:08
23 up, and we'll go from there. 05:19:15

24 A. Yes, I have them open. 05:19:29

25 Q. All right. So Exhibit 1048 is the data 05:19:35

1	sheet for the MPD4S014S DC-to-DC converter;	05:19:41
2	correct?	05:19:53
3	A. That's correct.	05:19:56
4	Q. And how would you pronounce the name of	05:19:59
5	that manufacturer of that part that's shown at	05:20:01
6	the bottom of the page there?	05:20:03
7	A. I always thought it was "Murata," but	05:20:06
8	don't really know for sure.	05:20:09
9	Q. But it's spelled M-U-R-A-T-A?	05:20:11
10	A. Yes.	05:20:14
11	Q. And then Exhibit 1042 is another	05:20:15
12	document from Murata titled "Power Supply	05:20:25
13	Reference Guide for Xilinx FPGAs"; correct?	05:20:30
14	ATTORNEY LINDSAY: Objection; outside	05:20:36
15	the scope of redirect.	05:20:36
16	THE WITNESS: Yes, that's correct.	05:20:39
17	BY ATTORNEY CHANDLER:	05:20:40
18	Q. Please turn to page 16 of Exhibit 1042,	05:20:43
19	and let me know when you're there.	05:20:47
20	A. I'm at page 16 now.	05:20:57
21	Q. Of Exhibit 1042?	05:21:00
22	A. Yes.	05:21:03
23	Q. And. Are you also at page 2 of	05:21:03
24	Exhibit 1048?	05:21:08
25	A. Yes, I am.	05:21:09

1	Q. So page 16 of Exhibit 1042 shows an	05:21:14
2	example of using the MPD4S014S DC-to-DC converter	05:21:19
3	that's described in Exhibit 1048, including	05:21:33
4	page 2 of Exhibit 1048; is that fair?	05:21:40
5	ATTORNEY LINDSAY: Objection; outside	05:21:44
6	the scope of redirect.	05:21:44
7	THE WITNESS: Yes, it appears to be.	05:21:47
8	BY ATTORNEY CHANDLER:	05:21:53
9	Q. And as shown in Exhibit 1042 of page	05:21:53
10	16, V-in, for the MPD4S014S circuit shown on	05:21:57
11	page 2 of Exhibit 1048, can be the same for the	05:22:07
12	two buck converters; correct?	05:22:13
13	ATTORNEY LINDSAY: Objection; outside	05:22:16
14	the scope of redirect.	05:22:16
15	THE WITNESS: What do you mean "can be	05:22:20
16	the same"?	05:22:22
17	BY ATTORNEY CHANDLER:	05:22:24
18	Q. The same voltage.	05:22:25
19	ATTORNEY LINDSAY: Objection; outside	05:22:30
20	the scope of redirect.	05:22:30
21	THE WITNESS: Where do you see that?	05:22:36
22	BY ATTORNEY CHANDLER:	05:22:38
23	Q. So on page 16 of Exhibit 1042, on the	05:22:38
24	left, there's just one V-in, which is the supply;	05:22:41
25	right?	05:22:45

1 ATTORNEY LINDSAY: Objection; outside 05:22:46
2 the scope of redirect. 05:22:46
3 THE WITNESS: Yes, I see that. 05:22:49
4 BY ATTORNEY CHANDLER: 05:22:50
5 Q. So in other words, nothing requires 05:22:51
6 that V-in, on page 2 of Exhibit 1048, be 05:22:55
7 different for the top buck converter and the 05:23:00
8 second buck converter underneath it. V-in could 05:23:05
9 be the same signal, just going to two different 05:23:08
10 places; correct? As shown, for example, on 05:23:13
11 page 16 of Exhibit 1042. 05:23:16
12 ATTORNEY LINDSAY: Objection; form, 05:23:19
13 outside the scope of redirect. 05:23:20
14 THE WITNESS: Page 16 on 1042 shows an 05:23:25
15 input pin called V-in. It doesn't show if it's 05:23:30
16 the one that's connected to -- using the -- what 05:23:35
17 I think I've referred to as the upper circuit to 05:23:39
18 generate V-out1, or if it's used in connection 05:23:42
19 with the lower circuit for V-out2 and V-out3. I 05:23:46
20 don't know which one it's connected to. 05:23:53
21 BY ATTORNEY CHANDLER: 05:23:55
22 Q. It can be connected to both; right? It 05:23:55
23 could be the same voltage input for both? 05:23:57
24 ATTORNEY LINDSAY: Objection; outside 05:24:02
25 the scope of redirect. 05:24:02

1 THE WITNESS: It could be. It could be 05:24:06
2 connected to ground directly. These things could 05:24:07
3 be externally wired up just about any way. But 05:24:10
4 this isn't showing me what that V-in is going to 05:24:14
5 in the context of the circuit we looked at on 05:24:18
6 page 2 of the other document, the 1048. 05:24:21
7 BY ATTORNEY CHANDLER: 05:24:27
8 Q. I just want to be clear that you're not 05:24:27
9 saying that, on page 2 of Exhibit 1048, that the 05:24:29
10 V-ins have to be separate and unrelated inputs; 05:24:32
11 they could -- it's possible that V-in could be 05:24:40
12 the same input for both what we've been referring 05:24:44
13 to as the top buck converter and then the second 05:24:48
14 buck converter below it; is that fair? 05:24:53
15 ATTORNEY LINDSAY: Objection; form. 05:24:55
16 THE WITNESS: Well, we know that 05:24:58
17 they're separate pins, so they certainly can be 05:24:59
18 separate and independent. Whether they can be 05:25:05
19 the same or not, I guess perhaps it could, sure. 05:25:11
20 BY ATTORNEY CHANDLER: 05:25:14
21 Q. And then with respect to V-out3, which 05:25:15
22 is shown, again, both on page 16 of Exhibit 1042 05:25:20
23 as well as page 2 of Exhibit 1048 -- do you see 05:25:26
24 V-out3? 05:25:33
25 A. I do. 05:25:35

1 ATTORNEY LINDSAY: Objection; outside 05:25:37
2 the scope of direct. 05:25:37
3 BY ATTORNEY CHANDLER: 05:25:39
4 Q. There's no requirement that V-out3, 05:25:40
5 which is connected to the LDO, be used in the 05:25:46
6 buck converter that's shown on page 2 of 05:25:58
7 Exhibit 1048 and referred to as well on page 16 05:26:02
8 of Exhibit 1042; correct? 05:26:06
9 ATTORNEY LINDSAY: Objection; form, 05:26:09
10 outside the scope of redirect. 05:26:11
11 THE WITNESS: There's no requirement 05:26:14
12 that any of those outputs be used, let alone 05:26:15
13 the -- you're right, there's no requirement that 05:26:20
14 V-out3 or V-out2 or V-out1 be used. 05:26:23
15 BY ATTORNEY CHANDLER: 05:26:27
16 Q. And as shown on page 16 of 05:26:28
17 Exhibit 1042, you could have one supply voltage 05:26:30
18 coming in and two regulated voltages coming out 05:26:37
19 on V-out1 from the top buck converter and V-out2 05:26:46
20 from the second buck converter; correct? 05:26:52
21 ATTORNEY LINDSAY: Objection; outside 05:26:57
22 the scope of direct. 05:26:57
23 THE WITNESS: Well, again, I would 05:27:00
24 disagree with that, only to the extent that the 05:27:01
25 circuit on page 16 doesn't make it clear which 05:27:08

1 V-in is connected to anything, let alone what 05:27:12
2 happens with the other V-in. 05:27:17
3 BY ATTORNEY CHANDLER: 05:27:19
4 Q. There's only one supply voltage that's 05:27:19
5 referenced; right? There's one wire or one path, 05:27:24
6 as we described previously? 05:27:28
7 ATTORNEY LINDSAY: Objection; outside 05:27:31
8 the scope of direct. 05:27:31
9 THE WITNESS: Sure. There's only one 05:27:36
10 shown on the top left side. If there was only 05:27:38
11 one that was wired up that way, they wouldn't be 05:27:41
12 able to generate either V-out1 or V-out2 at all. 05:27:45
13 BY ATTORNEY CHANDLER: 05:27:53
14 Q. And as we discussed a moment ago, the 05:27:53
15 same supply voltage could go to both the V-in for 05:27:55
16 the top buck converter, shown on page 2 of 05:28:02
17 Exhibit 1048, as well as the V-in for the second 05:28:06
18 buck converter, and then it would work; correct? 05:28:12
19 ATTORNEY LINDSAY: Objection; outside 05:28:15
20 the scope of direct. 05:28:15
21 THE WITNESS: I don't think so. As I 05:28:19
22 look at this, it's showing the input pins, at 05:28:20
23 least some of them, and the output pins on this 05:28:23
24 particular product. 05:28:27
25 There are two different V-in pins. If 05:28:31

1 you only use one, you can only power the 05:28:34
2 components that are connected to that V-in. If 05:28:38
3 it had said something like -- I don't know. I 05:28:42
4 don't know. 05:28:46

5 They should show two different V-in 05:28:48
6 pins. 05:28:51

7 BY ATTORNEY CHANDLER: 05:28:59

8 Q. They show two different V-in pins on 05:29:00
9 page 2 of Exhibit 1048. But those two pins can 05:29:03
10 get the same signal; right? Same supply voltage? 05:29:08

11 ATTORNEY LINDSAY: Objection; form. 05:29:13

12 THE WITNESS: I believe conceptually 05:29:16
13 they could. Then, you know, if that was the case 05:29:21
14 for the usage, the figure in 1042 on page 16, I 05:29:22
15 would expect it to show V-in1, V-in2 or V-in with 05:29:33
16 the pin numbers or something showing them 05:29:41
17 connected together. But it doesn't. 05:29:43

18 BY ATTORNEY CHANDLER: 05:29:50

19 Q. And so in the situation that I've been 05:29:52
20 describing, where the same supply voltage is 05:29:54
21 provided to the V-in pin for the top buck 05:29:57
22 converter as well as the second buck converter, 05:30:03
23 in that situation, the circuit on page 2 of 05:30:05
24 Exhibit 1048 would work properly to output two 05:30:13
25 regulated voltages, identified as V-out1, which 05:30:18

1 could be, for example, 1.8 volts, as shown on 05:30:22
2 page 16 of Exhibit 1042; as well as the second 05:30:28
3 regulated output voltage, V-out2, which could be 05:30:32
4 3.3 volts, as shown, for example, on page 16 of 05:30:36
5 Exhibit 1042; correct? 05:30:40

6 ATTORNEY LINDSAY: Objection; form, 05:30:43
7 outside the scope of redirect. 05:30:45

8 THE WITNESS: I've got no reason to 05:30:50
9 think that if the circuit as depicted on page 2 05:30:51
10 of 1048 -- that it could be wired up in a way 05:30:58
11 that would produce the output voltages shown on 05:31:01
12 page 16 of 1042. It just doesn't seem to be 05:31:07
13 wired up that way. 05:31:15

14 BY ATTORNEY CHANDLER: 05:31:16

15 Q. And if you look at page 7 of 05:31:19
16 Exhibit 1048 at the top, that also shows a single 05:31:22
17 V-in being used to produce two V-outs; correct? 05:31:30

18 ATTORNEY LINDSAY: Objection; outside 05:31:37
19 the scope of redirect. 05:31:37

20 THE WITNESS: It shows a single line -- 05:31:47
21 single pin called V-in. And it shows a V-out1, 05:31:49
22 V-out2, and V-out3. However, I don't recall 05:32:01
23 Dr. Wolfe analyzing this part of the circuit. 05:32:10
24 And to be honest with you, I don't recall the 05:32:12
25 details of how it operates. 05:32:14

1	BY ATTORNEY CHANDLER:	05:32:19
2	Q. That's the same circuit that we've been	05:32:20
3	discussing in Exhibit 1048 though; right?	05:32:21
4	ATTORNEY LINDSAY: Objection; outside	05:32:26
5	the scope of redirect.	05:32:27
6	THE WITNESS: No, it's not.	05:32:28
7	BY ATTORNEY CHANDLER:	05:32:34
8	Q. That's the MPD4S014S?	05:32:35
9	ATTORNEY LINDSAY: Objection; outside	05:32:40
10	the scope of redirect.	05:32:40
11	THE WITNESS: Sure. We've looked at	05:32:43
12	the circuit -- circuitry inside the product on	05:32:44
13	Figure 2; and then on -- I'm sorry. It was --	05:32:49
14	which page? Page 7.	05:32:56
15	We don't see anything about the	05:33:00
16	circuitry inside. We see circuitry on the	05:33:02
17	outside.	05:33:05
18	BY ATTORNEY CHANDLER:	05:33:07
19	Q. We see pins; right? We see the -- the	05:33:07
20	V-in for MPD47014S [sic], which is the same	05:33:10
21	circuit we've been discussing on page 2 of	05:33:21
22	Exhibit 1048; right?	05:33:23
23	ATTORNEY LINDSAY: Objection; outside	05:33:25
24	the scope of redirect, form.	05:33:25
25	THE WITNESS: We do see a pin for V-in,	05:33:28

1	yeah.	05:33:31
2	BY ATTORNEY CHANDLER:	05:33:32
3	Q. And there's only one voltage shown, or	05:33:32
4	one path, as you've described it earlier, coming	05:33:37
5	in to V-in on page 7 of Exhibit 1048, similar to	05:33:41
6	page 16 of Exhibit 1042; correct?	05:33:47
7	A. I'm not sure --	05:33:51
8	ATTORNEY LINDSAY: Objection --	05:33:52
9	objection; outside the scope of redirect. Sorry.	05:33:54
10	THE WITNESS: So, yeah, it is showing a	05:33:58
11	variable V-in supply on the far left, which then	05:34:00
12	goes up and enters into the pin labeled V-in.	05:34:04
13	Just the one, I agree, yeah.	05:34:09
14	BY ATTORNEY CHANDLER:	05:34:13
15	Q. And then at least two outputs, at least	05:34:13
16	V-out1 and V-out2 on both page 7 of 1048 and	05:34:24
17	page 16 of Exhibit 1042?	05:34:29
18	ATTORNEY LINDSAY: Objection; outside	05:34:32
19	the scope of redirect.	05:34:32
20	THE WITNESS: Page 7 shows three	05:34:35
21	outputs, and page 16 of the 1042 shows three	05:34:38
22	outputs, V-out1 through 3.	05:34:43
23	BY ATTORNEY CHANDLER:	05:34:46
24	Q. And V-out3, though, is not used in	05:34:47
25	page 16 of Exhibit 1042; correct?	05:34:49

1	ATTORNEY LINDSAY: Objection; outside	05:34:54
2	the scope of the redirect.	05:34:54
3	THE WITNESS: That's correct.	05:34:58
4	BY ATTORNEY CHANDLER:	05:35:05
5	Q. Do you have any corrections or	05:35:06
6	clarifications you'd like to make?	05:35:07
7	A. Not that I noticed.	05:35:10
8	ATTORNEY CHANDLER: All right. Then	05:35:11
9	that will conclude the deposition. Thank you.	05:35:12
10	THE VIDEOGRAPHER: Counsel, would you	05:35:19
11	like us to conclude the video deposition?	05:35:20
12	ATTORNEY LINDSAY: Yes.	05:35:22
13	ATTORNEY CHANDLER: Yeah, it was	05:35:27
14	unanimous.	05:35:28
15	THE VIDEOGRAPHER: Before I do, I just	05:35:29
16	need to ask, does anyone need the copy of the	05:35:31
17	video?	05:35:33
18	ATTORNEY CHANDLER: Yes, we will take a	05:35:33
19	copy. No particular rush that I know of.	05:35:36
20	THE VIDEOGRAPHER: Thank you. This	05:35:46
21	concludes today's deposition of Dr. William	05:35:47
22	Mangione-Smith. We're off the video record at	05:35:51
23	5:35 p.m. Pacific Time on June 12th, 2023.	05:35:53
24		
25		

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--o0o--
(Whereupon, at 5:35 p.m. Pacific Time, the
proceedings concluded.)
--o0o--

05:35:58
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CERTIFICATE OF SHORTHAND REPORTER

I, Gail Inghram, Registered Diplomate
Reporter, Certified Realtime Reporter, California
Certified Shorthand Reporter No, 8635, and Notary
Public, the officer before whom the foregoing
proceedings were taken, do hereby certify that
the foregoing transcript is a true and correct
record of the proceedings; that said proceedings
were taken by me stenographically and thereafter
reduced to typewriting under my supervision; and
that I am neither counsel for, related to, nor
employed by any of the parties to this case and
have no interest, financial or otherwise, in its
outcome.

Gail Inghram Verbano

GAIL INGRAM, BA, RDR, CRR, CA-CSR 8635

1 WILLIAM MANGIONE-SMITH, PH.D.

05:35:58

2
3 RE: Samsung v. Netlist June 12, 2023 , WILLIAM
4 MANGIONE-SMITH, PH.D.

05:35:58

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5 The above-referenced transcript has been completed by
6 Esquire Deposition Solutions and review of the transcript is
7 being handled as follows:

05:35:58

05:35:58

05:35:58

8 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Contact
9 Esquire Deposition to schedule a time to review the original
10 transcript at a Esquire Deposition office.

05:35:58

05:35:58

05:35:58

11 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Locked .PDF
12 Transcript - The witness should review the transcript and
13 make any necessary corrections on the errata pages included
14 below, notating the page and line number of the corrections.
15 The witness should then sign and date the errata and penalty
16 of perjury pages and return the completed pages to all
17 appearing counsel within the period of time determined at
18 the deposition or provided by the Code of Civil Procedure.

05:35:58

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19 ___Waiving the CA Code of Civil Procedure per Stipulation of
20 Counsel - Original transcript to be released for signature
21 as determined at the deposition.

05:35:58

05:35:58

05:35:58

22 ___Signature Waived - Reading and Signature was waived at
23 the time of the deposition.

05:35:58

05:35:58

24 ___Federal Read and Sign Requested (FRCP 30(e)(1)(B) -
25 Locked .PDF Transcript - The witness should review the

05:35:58

05:35:58

1 transcript and make any necessary corrections on the errata 05:35:58
2 pages included below, notating the page and line number of 05:35:58
3 the corrections. The witness should then sign and date the 05:35:58
4 errata and penalty of perjury pages and return the completed 05:35:58
5 pages to all appearing counsel within the period of time 05:35:58
6 determined at the deposition or provided by the Federal 05:35:58
7 Rules. 05:35:58
8 XX___Federal Read and Sign Not Requested - Reading and 05:35:58
9 Signature was not requested before the completion of the 05:35:58
10 deposition. 05:35:58

E R R A T A

I wish to make the following changes,

for the following reasons:

Page Line

_____ CHANGE: _____

REASON: _____

_____ CHANGE: _____

REASON: _____

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REASON: _____

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REASON: _____

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REASON: _____

_____ CHANGE: _____

REASON: _____

1		05:35:58
2		05:35:58
3	I, WILLIAM MANGIONE-SMITH, PH.D., do	05:35:58
4	hereby certify:	05:35:58
5	That I have read the foregoing	05:35:58
6	deposition;	05:35:58
7	That I have made such changes in form	05:35:58
8	and/or substance to the within deposition as	05:35:58
9	might be necessary to render the same true and	05:35:58
10	correct;	05:35:58
11	That having made such changes thereon,	05:35:58
12	I hereby subscribe my name to the deposition.	05:35:58
13	I declare, under penalty of perjury,	05:35:58
14	that the foregoing is true and correct.	05:35:58
15	Executed this _____ day of	05:35:58
16	_____, 2023, at _____.	05:35:58
17	(City)	05:35:58
18	_____.	05:35:58
19	(State)	05:35:58
20		05:35:58
21	_____	05:35:58
22	WILLIAM MANGIONE-SMITH, PH.D.	05:35:58
23		
24		
25		