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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co. Ltd.	Case No. IPR2022-00996
Petitioner,	Patent No. 11,016,918
vs.	
Netlist, Inc.,	Case No. IPR2022-00999
Patent Owner.	Patent No. 11,232,054

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VIDEOCONFERENCE DEPOSITION OF ANDREW WOLFE, Ph.D.

Thursday, March 16, 2023

Volume I (Pages 1 - 199)

Reported Remotely and Stenographically by:
JANIS JENNINGS, CSR No. 3942, CLR, CCRR
Job No. 5807753

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DEPOSITION OF ANDREW WOLFE, Ph.D.,
appearing remotely, located in Santa Clara,
California, taken on behalf of the Petitioner,
beginning at 9:06 a.m., on Thursday, March 16, 2023,
sworn remotely by Janis Jennings, Certified Shorthand
Reporter No. 3942, CCRR, located in the City of
Walnut Creek, County of Contra Costa, State of
California.

1
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I N D E X

WITNESS	PAGE
ANDREW WOLFE, Ph.D.	
VOLUME I (Pages 1 - 199)	
EXAMINATION BY MS. ZHONG	5

E X H I B I T S

EXHIBIT	PAGE
Exhibit 2101 Intel Developer Forum "Fully Buffered DIMM (FB-DIMM) Design Considerations" dated 2/18/04	41

1 THURSDAY, MARCH 16, 2023; 9:06 A.M.

2

3 ANDREW WOLFE, Ph.D.,

4 the witness herein, was sworn and

5 testified as follows:

6

7 EXAMINATION 08:54

8 BY MS. ZHONG: 08:54

9 Q. Good morning, Dr. Wolfe. 08:54

10 A. How are you? 09:07

11 Q. Can you please -- good. 09:07

12 Can you please state your full name for the 09:07

13 record? 09:07

14 A. Andrew Wolfe. 09:07

15 Q. Okay. Dr. Wolfe, you're familiar with fully 09:07

16 buffered dual in-line memory modules; correct? 09:07

17 (Clarification requested by Reporter.) 09:07

18 BY MS. ZHONG: 09:07

19 Q. Dr. Wolfe, you are familiar with fully 09:07

20 buffered dual in-line memory modules; correct? 09:07

21 A. I'm familiar with that term as it is used in 09:07

22 certain JEDEC standards. 09:07

23 Q. And fully buffered dual in-line memory 09:07

24 modules are abbreviated as FB-DIMM; correct? 09:08

25 A. Sometimes they are. 09:08

Page 5

1 Q. Okay. So if I use the abbreviation FB-DIMM, 09:08
2 can we agree that I am referring to the fully 09:08
3 buffered dual in-line memory modules? 09:08
4 A. As specified in the JEDEC specifications? 09:08
5 Q. Sure. 09:08
6 A. Okay. 09:08
7 Q. And FB-DIMM includes a buffer on a memory 09:08
8 module; correct? 09:08
9 A. Yes, as that's defined in the JEDEC 09:08
10 specification, yes. 09:08
11 Q. Okay. And that buffer is referred to as an 09:08
12 advanced memory buffer or AMB; correct? 09:08
13 A. In some cases it is. 09:08
14 Q. The AMB receives information from a memory 09:08
15 controller of a host system; is that correct? 09:08
16 A. Under certain circumstances that can be 09:09
17 true. 09:09
18 Q. Under what circumstances it is not true? 09:09
19 A. Well, if you buy an FB-DIMM and it's still 09:09
20 in the box, it doesn't receive anything from any 09:09
21 memory controller. You have to install it in a 09:09
22 computer system and you have to configure the 09:09
23 computer system properly and you have to operate the 09:09
24 computer system. 09:09
25 Q. Okay. So when the FB-DIMM is inserted into 09:09

1 a memory slot of a properly configured computer 09:09
2 system, the AMB will receive information from the 09:09
3 memory controller of the host system; is that 09:09
4 correct? 09:09
5 A. It needs a little bit more than that. It 09:09
6 actually needs to be -- the computer system needs to 09:09
7 be operating, and it needs to be programmed to 09:09
8 interact with that particular memory module. 09:10
9 Q. Okay. So assume that if the FB-DIMM is 09:10
10 inserted into a memory slot, a properly configured 09:10
11 computer system that is operating and that is 09:10
12 programmed to interact with the particular memory 09:10
13 module, the MB receives information from the memory 09:10
14 controller of that host system; is that correct? 09:10
15 A. That would normally be true. 09:10
16 Q. Okay. And what information is received by 09:10
17 the AMB from the memory controller in that 09:10
18 situation? 09:10
19 A. Let me look at the specification. 09:10
20 Q. When you say "specification," which exhibit 09:10
21 are you referring to? 09:10
22 A. 1027. 09:10
23 Q. 1027? 09:10
24 A. Yes. 09:10
25 Q. Okay. And that's JSD82-20; is that correct? 09:10

1	A.	Yes.	09:11
2	Q.	Okay.	09:11
3	A.	The AMB receives clocks, it receives address	09:11
4		command bits, and it receives data and data strobe	09:11
5		signals.	09:11
6	Q.	Where are you looking at?	09:11
7	A.	I'm looking at Figure 1.1.	09:11
8	Q.	And which page?	09:11
9	A.	3.	09:11
10	Q.	Page 3.	09:11
11		And you are referring to the output on the	09:11
12		DDR I/O side; is that correct?	09:11
13	A.	Correct. That's where it outputs the	09:11
14		information that is received over what are called	09:12
15		northbound/southbound links.	09:12
16	Q.	What information -- I'm asking what	09:12
17		information it is received.	09:12
18	A.	Well, that's the information that's	09:12
19		received. It's received over the northbound and	09:12
20		southbound links in an encoded form.	09:12
21	Q.	Why don't you take a look at Exhibit 1028.	09:12
22	A.	Okay.	09:12
23	Q.	Can you take a look at pages 11 and 12 of	09:12
24		Exhibit 1028.	09:12
25	A.	Yes.	09:13

Page 8

1 Q. Where are the address pins? 09:13

2 A. I didn't say there were address pins. The 09:13

3 pins are the northbound and southbound lanes. The 09:13

4 information that gets conveyed does include 09:13

5 addresses. 09:13

6 Q. So there are no address pins or control 09:13

7 pins? 09:13

8 MR. CHANDLER: Object to form. Object to 09:13

9 form. 09:13

10 THE WITNESS: There are no pins -- well -- 09:13

11 DEPOSITION REPORTER: Excuse me, Mr. Wolfe. 09:14

12 I'm sorry to interrupt. I'm getting an audio 09:14

13 feedback from somebody. Can we go off the record 09:14

14 real quick and let's see where it is coming from, 09:14

15 please. 09:14

16 MS. ZHONG: Sure. 09:14

17 (Off the record.) 09:14

18 BY MS. ZHONG: 09:15

19 Q. So there are no address pins or control 09:15

20 pins; is that correct, Dr. Wolfe? 09:15

21 MR. CHANDLER: Object to form. 09:15

22 THE WITNESS: No. I think that that would 09:15

23 be misleading. There are no pins that have those 09:15

24 specific names and there are no -- when you talk 09:15

25 about -- pins on the DIMM? Is that the question? 09:15

1 BY MS. ZHONG: 09:15

2 Q. Correct. 09:15

3 A. Yeah. There are no DIMM pins that have 09:15

4 those specific names, but there are pins, the 09:15

5 northbound and southbound lanes, that carry that 09:15

6 information so they perform that function. 09:15

7 Q. And the address and the control information 09:15

8 are sent as serialized packets; is that correct? 09:15

9 A. Serialized packets? They -- yes. They 09:16

10 are -- the information is sent to the advanced 09:16

11 memory buffer in the form of serialized packets. 09:16

12 Q. Okay. So unlike the most common DIMMs with 09:16

13 the dedicated second address and the control pins, 09:16

14 the FB-DIMM does not have dedicated address and 09:16

15 control pins; is that correct? 09:16

16 MR. CHANDLER: Object to form. 09:16

17 THE WITNESS: I want to be clear. When we 09:16

18 talk about the most common DIMMs, I assume we are 09:16

19 talking about unbuffered DIMMs of some type and, of 09:16

20 course, there are a number of different types that 09:16

21 were known at the time of the filing of these 09:16

22 patents. There are more types known today. 09:16

23 Those generally have pins that are used for 09:17

24 address and control, but there are often pins that 09:17

25 are shared between address functions and control 09:17

1 functions. So to that extent, they are not 09:17
2 dedicated to one or the other. 09:17
3 But as I explained before, the northbound 09:17
4 and southbound lanes on the fully buffered DIMM are 09:17
5 used for address and control communications, but 09:17
6 they are also used for data communications. 09:17
7 BY MS. ZHONG: 09:17
8 Q. Okay. So in the most common DIMMs, such as 09:17
9 RDIMMs, or registered DIMMs, SODIMMs, small outlined 09:17
10 DIMMS and the output DIMM connection -- 09:18
11 (Clarification requested by Reporter.) 09:18
12 BY MS. ZHONG: 09:18
13 Q. -- SODIMMs, or small outlined DIMMs, and 09:18
14 unbuffered DIMMs. Small outlined DIMMs, yeah, 09:18
15 SODIMMs, and unbuffered DIMMs or UDIMMs. 09:18
16 So in those DIMMs, data is not sent on the 09:18
17 same pins as for address signals; is that correct? 09:18
18 MR. CHANDLER: Objection to form. 09:18
19 THE WITNESS: Of course, there are many 09:18
20 different generations of those DIMM types at 09:18
21 different times and each one has its own 09:18
22 specification, so I would need to review them all to 09:18
23 give you an absolute answer. 09:18
24 But my recollection is that, generally, 09:19
25 there are separate pins that are used for data 09:19

1 communication as opposed to the pins that are used 09:19
2 for address and commands. 09:19
3 BY MS. ZHONG: 09:19
4 Q. Okay. But in FB-DIMMs, they are sent on the 09:19
5 same pins as for command and address; is that 09:19
6 correct? 09:19
7 MR. CHANDLER: Objection. Form. 09:19
8 THE WITNESS: Between the host computer and 09:19
9 the FB-DIMM, that is the case. 09:19
10 BY MS. ZHONG: 09:19
11 Q. Okay. What's an FB-DIMM? That's only for 09:19
12 the DDR2; correct? There are no DDR3 FB-DIMMs as 09:19
13 far as you know? 09:19
14 A. I don't recall one way or the other. There 09:19
15 certainly is a DDR2 FB-DIMM. 09:19
16 Q. Does your declaration rely on DDR3 FB-DIMMs? 09:19
17 A. Not that I can recall. 09:20
18 Q. And there are no DDR4 FB-DIMMs; correct? 09:20
19 A. I don't recall referring to any in my 09:20
20 declaration. 09:20
21 Q. Okay. So your declaration only referred to 09:20
22 a DDR2 FB-DIMM? 09:20
23 A. As far as I can recall right now. 09:20
24 Q. Okay. What is a termination voltage? 09:20
25 A. In general? 09:20

1 Q. For use with -- let me withdraw and ask. 09:20
2 Is a termination voltage used in connection 09:20
3 with a DDR2 FB-DIMM? 09:20
4 A. I believe it is, yes. 09:20
5 Q. Okay. What is it used for? 09:20
6 MR. CHANDLER: Objection. Form. 09:21
7 THE WITNESS: It's used to provide power to 09:21
8 signal termination networks. 09:21
9 BY MS. ZHONG: 09:21
10 Q. What does "signal termination" mean? 09:21
11 A. What does -- as I used it in that previous 09:21
12 phrase? 09:21
13 Q. Correct. 09:21
14 A. When a high-speed signal passes over a wire 09:21
15 that has what we call transmission line properties, 09:21
16 there is potential for that signal to reflect back 09:21
17 from the end of the wire. 09:21
18 Q. Uh-huh.
19 A. We can reduce those reflections using what's 09:21
20 called a termination network, and in many cases, 09:22
21 that termination network is powered. 09:22
22 Q. So termination -- signal termination is not 09:22
23 required if you have a low-speed signal; is that 09:22
24 correct? 09:22
25 MR. CHANDLER: Objection. Form. 09:22

1 THE WITNESS: It depends on the 09:22
2 characteristics of the -- of the wiring and the 09:22
3 voltages that are used and the wiring properties and 09:22
4 what your definition of low speed is. 09:22
5 The speed of the signal with respect to 09:22
6 termination requirements has to do with the spectral 09:22
7 distribution of the energy, and that is primarily 09:22
8 reflected by the signal transition speed, not the 09:22
9 total amount of data that's being communicated. 09:23
10 BY MS. ZHONG: 09:23
11 Q. So in DDR2 FB-DIMM, what signals are the 09:23
12 termination voltage used to terminate? 09:23
13 A. The VTT voltage is used to terminate the 09:23
14 signals going to the DRAM chips. I would have to go 09:23
15 through the spec very carefully to figure out if 09:23
16 there were other places where it's used. 09:23
17 Q. Why don't you take a look at Exhibit 1028, 09:23
18 page 11, and the pin name for VTT as well as the 09:23
19 corresponding description. 09:24
20 A. I see that. 09:24
21 Q. So which signals are used to terminate with 09:24
22 VTT? 09:24
23 A. Well, as I said, I -- the ones that I recall 09:24
24 are address command and clock signals to the DRAMs, 09:24
25 but I would have to look very carefully at the 09:24

1 specification to see if there were any others. 09:24
2 That's the one that's documented on, for example, 09:24
3 page 15 or page 14. 09:24
4 Q. So if -- in FB-DIMM, if address command 09:24
5 signal information is transmitted on the same -- 09:24
6 through the same pin as for data, how can VTT be 09:24
7 selectively terminating the address command and 09:25
8 clock signals but not the data? 09:25
9 MR. CHANDLER: Objection. Form. 09:25
10 THE WITNESS: Are you referring to something 09:25
11 in my declaration? 09:25
12 BY MS. ZHONG: 09:25
13 Q. I'm just asking you. 09:25
14 A. So you're asking me about an unmodified 09:25
15 FB-DIMM? 09:25
16 Q. Correct. 09:25
17 A. I'm sorry. Can I hear the question one more 09:27
18 time? 09:27
19 Q. In FB-DIMM, you said that the address and 09:27
20 command information is transmitted on the same pins 09:27
21 as for data; correct? 09:27
22 MR. CHANDLER: Object to form. 09:27
23 THE WITNESS: From the host, that is true. 09:27
24 Not to the DRAMs. 09:27
25 / / / 09:27

1 BY MS. ZHONG: 09:27

2 Q. Okay. So how can the FTT be used 09:27

3 to selectively terminate the address and command 09:27

4 information signals but not the data signals? 09:27

5 MR. CHANDLER: Objection. Form. And I 09:27

6 think you said "FTT." 09:27

7 (Clarification requested by Reporter.) 09:28

8 MS. ZHONG: FTT -- VTT. 09:28

9 MR. CHANDLER: Even with that correction, 09:28

10 objection to form. 09:28

11 THE WITNESS: So VTT can be used to 09:28

12 selectively enable termination between the AMB and 09:28

13 the DRAMs on the address and command signals without 09:28

14 impacting the termination of the data signals. 09:28

15 BY MS. ZHONG: 09:28

16 Q. So where on the termination resistors placed 09:28

17 between the FTT pins and the address command clock 09:28

18 signals to the DRAM, or they are terminated on the 09:29

19 motherboard? 09:29

20 MR. CHANDLER: Objection. Form. 09:29

21 THE WITNESS: Usually there is a termination 09:29

22 on each end, but there would be termination near the 09:29

23 DRAMs for the address control signals. There are 09:29

24 numerous other places where there's termination, but 09:29

25 I believe on FB-DIMM, the other terminations would 09:29

1 primarily be on-chip terminations. 09:29
2 BY MS. ZHONG: 09:29
3 Q. The on-chip terminations is not part of the 09:29
4 F -- VTT; correct? 09:29
5 MR. CHANDLER: Objection. Form. 09:29
6 THE WITNESS: On an unmodified FB-DIMM, I 09:29
7 believe that's correct. 09:30
8 BY MS. ZHONG: 09:30
9 Q. And in the modified Harris FB-DIMM, how 09:30
10 would that differ? 09:30
11 Let me withdraw and ask it this way. In 09:30
12 your declaration, you didn't say that the FTT -- let 09:30
13 me withdraw and ask. 09:30
14 In your declaration, you do not say that the 09:30
15 VTT would operate any differently in the Harris 09:30
16 FB-DIMM and the JEDEC-compliant FB-DIMM; correct? 09:30
17 A. Well, no. I think that there are certain 09:31
18 teachings from the FB-DIMM that are taken into 09:31
19 account into Harris, but I explained what the 09:31
20 combination would be and how Harris would be 09:31
21 modified in the declaration for the [simultaneous 09:31
22 speakers] --
23 Q. Did you contend -- did you contend that VTT 09:31
24 would be used for online -- on-die termination? 09:31
25 A. I don't recall everything that's in the 09:31

1 declaration. It's quite large, but the focus 09:31
2 appears to be for DRAM termination for VTT in the 09:32
3 embodiment that I'm looking at right now for grounds 09:32
4 2D and 3D. 09:32
5 Q. When you say for "DRAM termination," is it 09:32
6 for the on-die termination? 09:32
7 A. I don't believe so. There is a resistor 09:32
8 shown in the drawings. 09:32
9 Q. Okay. So for the modified Harris, the VTT 09:32
10 is used in the same manner as in the -- for the 09:32
11 JEDEC-compliant FB-DIMM -- 09:32
12 A. No, actually I --
13 Q. -- [Simultaneous speakers] command a clock's
14 signal to the DRAM -- 09:32
15 (Clarification requested by Reporter.) 09:32
16 BY MS. ZHONG: 09:32
17 Q. So in your declaration, the VTT is used in 09:33
18 the same set manner for the modified Harris FB-DIMM 09:33
19 as for the JEDEC-compliant FB-DIMM, which is for the 09:33
20 termination of the address command and clock signals 09:33
21 to the DDR2 devices; is that correct? 09:33
22 A. No, I think that's an overgeneralization. 09:33
23 Again, there are many different grounds that are 09:33
24 presented in the declaration. We'd have to go 09:33
25 through them all carefully. 09:33

1 But, for example, I do see that certainly 09:33
2 some of the grounds refer to DDR3 and some of the 09:33
3 grounds refer to a VTT voltage of 0.9 volts, which I 09:33
4 recall is the on-ground -- or the on-die termination 09:34
5 voltage. 09:34
6 Q. For Harris, you used a DDR3 combination? 09:34
7 A. Let me look. 09:34
8 Q. Are you confusing that with Spiers? 09:34
9 A. Let me look at the various combinations 09:34
10 here. Oh, I'm sorry. I may have these backwards. 09:34
11 For Harris, I have DDR2 combinations that do 09:34
12 show a variety of different VTTs, so those would be 09:35
13 used for a variety of different purposes. 09:35
14 Q. When you say "a variety of VTTs," which 09:35
15 paragraph are you referring to? 09:35
16 A. So in paragraph 247, I talk about a VTT of 09:36
17 1.2 volts and also of .9 volts. I'm sorry, 1.25 09:36
18 volts and .9 volts. 09:36
19 Q. Paragraph 247? 09:36
20 A. Yes. 09:36
21 Q. VTT is half of VDDQ; correct? 09:36
22 A. In some instances, it is. 09:36
23 Q. In which instance is -- it is not? 09:36
24 A. I believe in the instance of DDR2 SDRAM, it 09:36
25 can just be .9 volts independently of VDDQ. 09:37

1 Q. What is VDDQ in DDR2? 09:37
2 A. I'm sorry. I didn't get -- 09:37
3 Q. Let me withdraw and ask. 09:37
4 What is VDDQ for DDR2? 09:37
5 A. It's one of the power supply voltages. 09:37
6 Q. What's the value? 09:37
7 MR. CHANDLER: Objection to form. 09:37
8 THE WITNESS: It's 1.8 volts plus or minus 09:38
9 0.1 volts. 09:38
10 BY MS. ZHONG: 09:38
11 Q. And half of that is 0.9; correct? 09:38
12 A. It is. 09:38
13 Q. Okay. So the 0.9 volt VTT is half of the 09:38
14 DDR2 SDRAM, as you stated in paragraph 247; correct?
15 A. That nominal -- 09:38
16 (Clarification requested by Reporter.) 09:38
17 BY MS. ZHONG:
18 Q. Is half of the VDDQ for DDR2. 09:38
19 MR. CHANDLER: Objection. Form. 09:38
20 THE WITNESS: At the nominal value, that's 09:38
21 true. 09:38
22 MS. ZHONG: VDDQ is one word, VDDQ, as 09:38
23 letter Q. 09:38
24 MR. CHANDLER: And sometimes it's shown as 09:38
25 subscript. It doesn't have to be, but -- so the V 09:39

1 is always capitalized and then the letters after it, 09:39
2 like "TT" and "DD" or "DDQ" are sometimes shown as 09:39
3 subscript. 09:39
4 MS. ZHONG: Yeah, it's probably easier for 09:39
5 you just to type them all as like capitalized 09:39
6 letters. 09:39
7 DEPOSITION REPORTER: Thank you. I 09:39
8 appreciate that. 09:39
9 BY MS. ZHONG: 09:39
10 Q. And which SDRAMs have a VDD or VDDQ of 09:39
11 2.5 volts? 09:39
12 A. I don't recall them all off the top of my 09:39
13 head. 09:39
14 Q. That's DDR; correct? Why don't you take a 09:39
15 look at your paragraph 246. 09:40
16 A. For certain DDR devices. 09:40
17 Q. So do you remember -- do you see like your 09:40
18 quote for different generations, there's 3.3 volt, 09:40
19 2.5 volt, 1.8 volt and a 1.5 volts? 09:40
20 A. I do. 09:40
21 Q. So the -- so the 3.3 is for SDR SDRAM, 2.5 09:40
22 is for DDR1, 1.8V is for DDR2, and 1.5V is for DDR3; 09:40
23 correct? 09:40
24 A. For at least some examples of these, that's 09:40
25 true. 09:40

1 Q. Okay. You're not aware of any DDR1 FB-DIMM, 09:40
2 are you? 09:41
3 A. Not off the top of my head, no. 09:41
4 Q. Okay. And you certainly didn't cite any 09:41
5 JEDEC standards for DDR1 FB-DIMM; correct? 09:41
6 A. I did not. 09:41
7 Q. And you're not aware of any DDR1 FB-DIMM; 09:41
8 correct? 09:41
9 A. I don't recall one right now. 09:41
10 Q. And as far as you know, is FB-DIMM first 09:41
11 developed for DDR2? 09:41
12 MR. CHANDLER: Objection. Form. 09:41
13 THE WITNESS: That particular specification, 09:41
14 JESD82-20, was first developed for DDR2, as far as I 09:41
15 know. 09:41
16 BY MS. ZHONG: 09:42
17 Q. Now, for the memory controller to send data, 09:42
18 address or command or clock information to an AMB, 09:42
19 there needs to be some power to drive those signals 09:42
20 from the memory controller to the AMB; is that 09:42
21 correct? 09:42
22 A. That's strangely phrased. Any electrical 09:42
23 signal that goes from one place to another requires 09:42
24 some energy. 09:42
25 Q. So why don't we take a look at Figure 3 of 09:42

1	Harris.	09:42
2	A. I will pull it up.	09:42
3	Q. And Harris is Exhibit 1023.	09:43
4	A. Okay.	09:43
5	Q. Okay. So in Figure 3 of Harris, it is shown	09:43
6	that certain information can flow from the memory	09:43
7	controller to the buffer on the DIMM; correct?	09:43
8	A. Yes.	09:43
9	Q. And for that information to flow from the	09:43
10	memory controller to the buffer, electrical energy	09:43
11	needs to be applied to drive that information from	09:43
12	the memory controller to the buffer; is that	09:43
13	correct?	09:43
14	A. Electrical energy needs to be present.	09:43
15	Ordinarily, a person of ordinary skill would	09:43
16	understand that both the DRAM, DIMM and the memory	09:43
17	controller would have a power source.	09:43
18	Q. Okay. So power and voltages will be applied	09:44
19	to the memory controller, including for the -- the	09:44
20	signal lines that's connecting between the memory	09:44
21	controller to the buffer to drive those information;	09:44
22	is that correct?	09:44
23	MR. CHANDLER: Objection. Form.	09:44
24	THE WITNESS: Again, I'm not sure I	09:44
25	understand your language. The memory controller	09:44

1 would ordinarily be understood to have a power 09:44
2 supply -- 09:44
3 BY MS. ZHONG:
4 Q. Okay.
5 A. -- that powers the circuits on the memory 09:44
6 controller. 09:44
7 Q. Okay. And is that still the case for 09:44
8 modified -- let me withdraw and ask. 09:44
9 Instead of using JEDEC-compliant FB-DIMM, if 09:44
10 you use Harris FB-DIMM, does the memory controller 09:45
11 still have a power supply that powers the circuit on 09:45
12 the memory controller? 09:45
13 A. Under ordinary operation, the memory 09:45
14 controller would have a source of power, whether 09:45
15 that's continuous power or switched power, whether 09:45
16 it is a single voltage or multiple voltages, there 09:45
17 would be a source of power to the memory controller. 09:45
18 Q. Okay. And so regardless whether we use 09:45
19 Harris FB-DIMM or the JEDEC-compliant FB-DIMM, the 09:45
20 memory controller will have its own power source -- 09:45
21 power supply; is that right? 09:45
22 MR. CHANDLER: Objection. Form. 09:45
23 THE WITNESS: No, that's not what I said. 09:45
24 It will have a power supply. It need not always be 09:45
25 independent from the power supply to the FB-DIMMs or 09:45

1 to any DIMMs. 09:46

2 BY MS. ZHONG: 09:46

3 Q. So in the case of -- so are you saying that 09:46

4 if we use Harris FB-DIMM, the -- let me just ask you 09:46

5 this question. 09:46

6 You proposed like in one configuration the 09:46

7 FB-DIMM will have a battery power as a backup power; 09:46

8 correct? 09:46

9 A. Yes. Well, the -- the modified FB-DIMM as 09:46

10 described in my declaration. 09:47

11 Q. So are you saying that that battery power on 09:47

12 the DIMM can also be used somehow to operate the 09:47

13 memory controller? 09:47

14 A. No. I don't think I said that. I mean, it 09:47

15 might be possible, but that's not a situation I 09:47

16 proposed. 09:47

17 Q. Okay. 09:47

18 A. When you're talking about the memory 09:47

19 controller, I assume you're talking about a standard 09:47

20 host memory controller for a standard FB-DIMM 09:47

21 because that's what we started talking about. 09:47

22 Q. What about if you use Harris FB-DIMM, what 09:47

23 kind of memory controller -- you did not propose 09:48

24 modification of a memory controller, did you? 09:48

25 A. Let me look through all the claims. 09:48

1 I did not propose modification to a host 09:49
2 memory controller, but there are -- there is logic 09:49
3 that controls memory separately on the -- on the 09:49
4 Harris embodiments. 09:49
5 Q. And that logic is on the memory module; 09:49
6 correct? 09:49
7 A. Correct. 09:49
8 Q. Okay. It's not on the host side. 09:49
9 A. Correct. The logic that I was referring to 09:49
10 is not on the host computer. 09:49
11 Q. Okay. So what will be the voltage applied 09:49
12 to the southbound signal lines between the memory 09:50
13 controller and the AMB buffer? 09:50
14 A. In what circumstances? 09:50
15 Q. When you have a FB-DIMM that's inserted into 09:50
16 a host computer. 09:50
17 A. An unmodified FB-DIMM? 09:50
18 Q. We can start there. 09:50
19 A. Can I hear the first question again? 09:50
20 Q. What will be the voltage applied to the 09:50
21 southbound signal lines going from the memory 09:50
22 controller to the buffer? 09:50
23 A. It depends on what the signal is, but they 09:50
24 would nominally vary between zero and 1.5 volts. 09:51
25 Q. Why 1.5 volts? Aren't DDR2 VDD and a VDDQ 09:51

1 voltage level is 1.8 volts? 09:51

2 A. I thought you asked me about the southbound 09:51

3 signal levels voltages. 09:51

4 Q. That's correct. 09:51

5 Is that voltage level different than the 09:51

6 DDR2 signal levels? 09:52

7 A. It's described as a 1.5 volt high-speed 09:52

8 differential point-to-point link so... 09:52

9 Q. Can you tell me where -- which exhibit? 09:52

10 A. On Exhibit 1028 at page 9. 09:52

11 Q. That's the AMB VCC, VCC FBD, or where 09:52

12 exactly? 09:52

13 A. The buffer interface. 09:52

14 Q. Page 9? 09:52

15 A. Yes. 09:52

16 Q. And the product description? 09:53

17 A. Product family attributes. 09:53

18 Q. Are you talking about supply voltage 09:53

19 nominal? 09:53

20 A. No. Buffer interface. 09:53

21 Q. Okay. And that buffer interface refers to 09:53

22 the interface between the memory controller and the 09:53

23 AMB? 09:53

24 A. Between the host memory controller and the 09:53

25 AMB, that would be my understanding, yes. 09:53

Page 27

1 Q. Okay. And is that still the same voltage 09:53
2 level where there is the Harris modified FB-DIMM? 09:53
3 MR. CHANDLER: Objection. Form. 09:54
4 THE WITNESS: I don't think the signal 09:54
5 voltage levels matter in my analysis of the modified 09:54
6 Harris FB-DIMM. 09:54
7 BY MS. ZHONG: 09:54
8 Q. So the answer to my question is yes, it is 09:54
9 the same and remains the same? 09:54
10 MR. CHANDLER: Objection. Form. 09:54
11 THE WITNESS: No. No. My answer is that it 09:54
12 wasn't relevant to my analysis. I don't think there 09:54
13 are any claims that I can recall that talked about 09:54
14 the magnitude of the signaling voltage. 09:54
15 BY MS. ZHONG: 09:54
16 Q. Dr. Wolfe, I'm not asking you whether you 09:54
17 think it matters or not. Just answer my question. 09:54
18 I want to get the facts -- 09:54
19 A. Yes.
20 Q. -- did you assert that the signal levels
21 would be different between the memory controller -- 09:55
22 (Clarification requested by Reporter.) 09:55
23 BY MS. ZHONG: 09:55
24 Q. Dr. Wolfe, did you claim that the signal 09:55
25 voltage levels would be different between the memory 09:55

1 controller and the buffer of Harris FB-DIMM? 09:55

2 A. I don't recall opining on the signal level 09:55

3 voltages between the host memory controller and the 09:55

4 FB-DIMM in my analysis. 09:55

5 Q. Does VTT track the signal level of the 09:55

6 memory controller -- let me withdraw and ask. 09:56

7 Why don't you take a look at Exhibit 1026. 09:56

8 A. Okay. 09:56

9 Q. And let's go to Table 16 -- 09:56

10 A. Table 16? 09:56

11 Q. -- which says -- yeah. Page 49. 09:56

12 A. Okay. 09:56

13 Q. Table 16, note 4, it says: 09:56

14 "VTT of transmitting device must track 09:56

15 VRAM of receiving device." 09:56

16 Do you see that? 09:56

17 A. I do. 09:56

18 Q. So in the case of FB-DIMM communicating with 09:56

19 a host system and where the VTT is used to terminate 09:57

20 the address and command signals, what is a 09:57

21 transmitting device in that instance? 09:57

22 A. I think that these questions don't make any 09:57

23 sense. This document talks about the communications 09:57

24 to the DDR2 DRAM chip -- 09:57

25 Q. Uh-huh.

1 A. -- not between a host computer and the 09:57
2 advanced memory buffer on a FB-DIMM. So this -- 09:57
3 this table and, in fact, this document aren't even 09:57
4 relevant to that communication. 09:57
5 Q. I'm not asking you that. I'm asking a 09:57
6 different question. 09:57
7 What is a transmitting device in note 4 here 09:57
8 if VTT for an FB-DIMM is used to terminate the 09:57
9 address command and clock signals of the DRAM? 09:58
10 A. It would be -- it would be whatever device 09:58
11 is directly connected to the DDR2 DRAM chip in 09:58
12 question for the purpose of sending, I believe in 09:58
13 this case, data, but possibly address commands as 09:58
14 well. 09:58
15 Q. Okay. VTT in FB-DIMM is used to terminate 09:58
16 the address command and clock signals; correct? 09:58
17 MR. CHANDLER: Object to form. 09:58
18 THE WITNESS: It is used to terminate those 09:58
19 signals in the communication between the advanced 09:58
20 memory buffer and the DDR2 chips. 09:58
21 BY MS. ZHONG: 09:58
22 Q. So is the transmitting device for the 09:58
23 address, command and clock signals the AMB then? 09:59
24 A. If one were to apply note 4 to a fully 09:59
25 buffered DIMM, then the transmitting device would be 09:59

1 the AMB on particular wires. 09:59

2 MS. ZHONG: Can we take a five-minute break? 10:00

3 DEPOSITION REPORTER: We're off the record. 10:00

4 (Off the record.) 10:00

5 BY MS. ZHONG: 10:12

6 Q. Dr. Wolfe, your declaration cites to 10:12

7 JESD79-2B, which is Exhibit 1026; correct? 10:12

8 A. It is one of the things that it cites to, 10:13

9 yes. 10:13

10 Q. How does that exhibit relate to JESD205, 10:13

11 which is Exhibit 1026? 10:13

12 MR. CHANDLER: Objection. Form. 10:13

13 THE WITNESS: From the perspective of the 10:13

14 JEDEC standards, the DRAM chips that are described 10:13

15 on page 9 of Exhibit 1028 would be further described 10:13

16 in detail in Exhibit 1026. 10:13

17 BY MS. ZHONG: 10:13

18 Q. And is it your contention that in Harris, or 10:13

19 whatever the modification you applied to Harris, 10:13

20 those DRAM chips in Harris would comply with 10:14

21 JESD79-2B? 10:14

22 MR. CHANDLER: Objection. Form. 10:14

23 THE WITNESS: Not necessarily. Harris talks 10:14

24 about DDR, DDR2 and DDR3. It talks about various 10:14

25 kinds of DIMMs, including FB-DIMMs. Harris is very 10:14

1 open that his teaching can be used in a variety of 10:14
2 different memory configurations, so there would 10:14
3 be -- the 1028 -- exhibits 1028 and 1026 are 10:14
4 exemplary of some portion of the scope of Harris' 10:14
5 teachings, but certainly not -- certainly Harris is 10:14
6 not limited to those particular kinds of devices. 10:14
7 BY MS. ZHONG: 10:14
8 Q. And are you relying on DDR1 FB-DIMM? 10:14
9 A. I'm not relying on a particular standard 10:14
10 device called a DDR1 FB-DIMM, but I am relying on 10:15
11 Harris' teachings that say that the teachings from 10:15
12 various DIMM standards can be combined in various 10:15
13 ways and still be consistent with Harris' teachings. 10:15
14 Q. So for claim No. 1, can you point me to 10:15
15 anywhere that you relied on a non-DDR2 standard? 10:15
16 MR. CHANDLER: Objection. Form. 10:15
17 THE WITNESS: So for example, in paragraph 10:15
18 239, I quote Harris where he explains that the 10:16
19 memory devices on the memory module can be of any 10:16
20 known or heretofore unknown DDR time, for example, 10:16
21 DDR2. And I think, in general, I've referred to a 10:17
22 number of portions in Harris that explain Harris' 10:17
23 broad view of memory. 10:17
24 I also, in paragraph 246, quote Harris' 10:17
25 range of power supplies, which we noted earlier, 10:17

1 ordinarily apply to various generations of memory. 10:17
2 So those are some examples. 10:17
3 The specific detailed examples that I used 10:17
4 illustratively for Harris Claim 1 are based on DDR2, 10:17
5 and then I referred to Harris' explanations of how 10:17
6 his teachings may be interpreted more broadly. 10:17
7 BY MS. ZHONG: 10:17
8 Q. Okay. In fact, you are not aware of any 10:17
9 FB-DIMMs that use DDR, DDR3 or DDR4; correct? 10:18
10 MR. CHANDLER: Objection. Form. 10:18
11 THE WITNESS: Well, since we agreed that for 10:18
12 this deposition, FB-DIMM refers to JESD82-20 that 10:18
13 would be correct. I'm not familiar with any 10:18
14 JESD79 -- I'm sorry, JESD82-20-compliant FB-DIMMs 10:18
15 that use memory other than DDR2. 10:18
16 BY MS. ZHONG: 10:18
17 Q. Are you aware of any -- let me withdraw and 10:18
18 ask. 10:18
19 Are you aware of any modified FB-DIMM that 10:18
20 uses DDR, DDR3 or DDR4? 10:18
21 A. I think Harris teaches that one can modify 10:18
22 and combine the teachings of various DIMM structures 10:19
23 with various memory structures, so that's one place 10:19
24 where it's true. 10:19
25 And then there are successor technologies. 10:19

1 They're not JESD82-20-compliant, but there are 10:19
2 successor registered DIMMs or buffered DIMM 10:19
3 technologies that correspond to DDR3 and DDR4. 10:19
4 Q. And are you aware of -- let me withdraw and 10:19
5 ask you this question. 10:19
6 Did you provide any examples of those other 10:19
7 FB-DIMMs? 10:19
8 MR. CHANDLER: Objection. Form. 10:20
9 THE WITNESS: Well, I'll repeat what I said. 10:20
10 I provided a discussion of the teachings of Harris 10:20
11 in combination with the JESD82-20 FB-DIMM standard, 10:20
12 and then I referenced the teachings in Harris that 10:20
13 would encourage one to modify those DIMMs to use 10:20
14 other forms of DDR memory. 10:20
15 So to that extent, I used that as an 10:20
16 example, but I have not provided any illustrations 10:20
17 or voltage mappings that correspond to those 10:20
18 particular examples. 10:20
19 BY MS. ZHONG: 10:20
20 Q. Okay. So your voltage mapping is based on 10:20
21 the voltages specified in JESD82-20 or JESD205. 10:20
22 Fair? 10:21
23 A. The exemplary voltage mappings with respect 10:21
24 to Harris are based on those two standards, but as I 10:21
25 said, I also refer to alternative voltages and quote 10:21

1 Harris as to where he introduces those. 10:21

2 Q. You did not provide a separate VCC voltage 10:21

3 for example; correct, other than 1.5 volts? 10:21

4 MR. CHANDLER: Objection. Form. 10:21

5 THE WITNESS: That's not true. In paragraph 10:21

6 254, I note that Harris explains that the 10:21

7 appropriate voltage levels for the VCC path depend 10:21

8 on the buffer and DIMM technology, such as from 0.5 10:21

9 volts to 3.5 volts. 10:21

10 BY MS. ZHONG: 10:22

11 Q. How many regulators are used in the 10:23

12 standard -- let me just withdraw and re-ask. 10:23

13 Do you know how many voltage regulators are 10:23

14 used on the host motherboard to generate VDD, VDDQ 10:23

15 and VDDL? 10:23

16 A. I think it varies from motherboard to 10:23

17 motherboard. 10:23

18 Q. And in the JEDEC-compliant FB-DIMM, there 10:24

19 are no separate DIMM pins for VDD, VDDQ and VDDL; is 10:24

20 that correct? 10:24

21 MR. CHANDLER: Objection. Form. 10:24

22 THE WITNESS: I missed a word there. In the 10:24

23 what compliant? 10:24

24 BY MS. ZHONG: 10:24

25 Q. In the JEDEC-compliant FB-DIMMs, there are 10:24

1 no separate pins for VDD, VDDQ and VDDL; is that 10:24
2 correct? 10:24
3 MR. CHANDLER: Objection. Form. 10:24
4 THE WITNESS: I believe that is correct. 10:24
5 Those would be derived on the module. 10:25
6 BY MS. ZHONG: 10:25
7 Q. So the power supply or the voltage supply 10:25
8 for VDD, VDDL and VDDQ are all derived from the same 10:25
9 input pins? 10:25
10 MR. CHANDLER: Objection. Form. 10:25
11 THE WITNESS: On an unmodified FB-DIMM, that 10:25
12 would be correct. On the combination that I 10:25
13 proposed in the Harris-combined grounds, they would 10:25
14 all be derived from the, for example, 12-volt input 10:25
15 pin. 10:26
16 BY MS. ZHONG: 10:26
17 Q. Okay. So on the standard JEDEC-compliant 10:26
18 FB-DIMM, there are -- how do you say it -- traces or 10:26
19 distribution network to distribute the voltage input 10:26
20 from VDD pins to the respective pins on the DRAM for 10:26
21 VDD, VDDQ and VDDL; correct? 10:26
22 MR. CHANDLER: Objection. Form. 10:26
23 THE WITNESS: Any particular unmodified 10:27
24 JEDEC-compliant FB-DIMM would have a wiring network 10:27
25 for the distribution of the VDD, VDDQ and VDDL 10:27

1 signals. 10:27

2 BY MS. ZHONG: 10:27

3 Q. And a POSITA can take advantage of those 10:27

4 pre-existing wiring network to provide the voltage 10:27

5 for the VDD, VDDQ and VDDL signals with Harris 10:28

6 12-volt external power source; is that correct? 10:28

7 MR. CHANDLER: Objection. Form. 10:28

8 A. No. One would not use an unmodified 10:28

9 FB-DIMM's wiring structure with Harris. Harris 10:28

10 teaches a voltage regulator module that generates a 10:28

11 separate VDD, which could then be used. 10:28

12 BY MS. ZHONG:

13 Q. So once the 1.8 voltage is generated with 10:28

14 the on-module regulator, a POSITA can use the 10:28

15 existing wiring network to connect that 1.8-volt 10:28

16 voltage to a VDD, VDDQ and a VDDL signal pin on the 10:28

17 DRAM; is that correct? 10:29

18 MR. CHANDLER: Objection. Form. 10:29

19 THE WITNESS: No, I think that would be 10:29

20 impractical. One would certainly learn from it. 10:29

21 One would understand how to build a power wiring 10:29

22 network of their own, but because there is a 10:29

23 separate voltage regulator module, one would build 10:29

24 their own connections to that voltage regulator 10:29

25 module. That's an ordinary engineering task and 10:29

1 well within the capabilities of a POSITA, and a 10:29
2 POSITA would understand how to do that based on the 10:29
3 teachings of Harris with a single voltage -- or a 10:29
4 single physical connection to VDDQ, VDDL and VDD or 10:29
5 with the three discrete connections. 10:29
6 BY MS. ZHONG: 10:29
7 Q. What do you mean by "a single physical 10:29
8 connection to VDDQ, VDDL and VDD"? 10:30
9 A. There could be a single output from the 10:30
10 voltage regulator module that connects to all three 10:30
11 of those sets of inputs on the DRAMs through a 10:30
12 wiring network, or there could be three distinct 10:30
13 outputs on the voltage regulator module. Either one
14 is acceptable and either one is within the skill of 10:30
15 a person of ordinary skill in the art. 10:30
16 Q. But whether it's a single connection or 10:30
17 three discrete connection, you just use one 10:30
18 regulator to generate the output; is that correct? 10:30
19 MR. CHANDLER: Objection. Form. 10:31
20 THE WITNESS: Not necessarily. It is 10:31
21 certainly well within the skill set of a person of 10:31
22 ordinary skill in the art to generate 1.8 volts with 10:31
23 a single regulator or to generate multiple 1.8 volts 10:31
24 supplies with multiple regulators. 10:31
25 / / / 10:31

1 BY MS. ZHONG: 10:31

2 Q. When would you use multiple regulators to 10:31

3 generate multiple 1.8 volts output? 10:31

4 A. It would be an ordinary design decision. 10:31

5 One might do it when they want to sequence the 10:31

6 power, one might want to do it when they turn the 10:31

7 power on and off independently, or one may do it 10:31

8 simply because it's more cost effective to use 10:31

9 multiple small regulators than one large regulator. 10:31

10 It's a design choice. 10:32

11 Q. Okay. So in the standard FB-DIMM, VDD, VDDQ 10:32

12 and VDDL are all connected to the same power source 10:32

13 from the VDD pins; correct? 10:32

14 A. In an unmodified -- 10:32

15 MR. CHANDLER: Objection. Form. 10:32

16 THE WITNESS: In an unmodified standard 10:32

17 FB-DIMM, that would likely be the case. 10:32

18 BY MS. ZHONG: 10:32

19 Q. Okay. And so in that unmodified standard 10:32

20 FB-DIMM, is there ability to sequence the power? 10:32

21 A. Not between the three different FDD-derived 10:32

22 power lines, there would not be. There would be an 10:33

23 ability to sequence other power sources. 10:33

24 Q. Okay. And so among VDD, VDDQ and the VDDL, 10:33

25 in an unmodified standard FB-DIMM, they cannot be 10:33

1 turned on and off independently; is that right? 10:33

2 MR. CHANDLER: Objection. Form. 10:33

3 THE WITNESS: My understanding is that an 10:33

4 unmodified standard FB-DIMM, the VDD would be turned 10:33

5 on or off always. 10:33

6 BY MS. ZHONG: 10:33

7 Q. Okay. And does Harris suggest that in its 10:33

8 modified FB-DIMM, the powering sequence for VDD, 10:34

9 VDDQ and a VDDL should be modified? 10:34

10 MR. CHANDLER: Objection. Form. 10:34

11 THE WITNESS: I don't think it suggests one 10:34

12 way or the other. 10:34

13 BY MS. ZHONG: 10:34

14 Q. It doesn't -- Harris doesn't say -- it 10:34

15 doesn't suggest expressly that it will be desirable 10:34

16 to sequence VDD, VDDQ and a VDDL; correct? 10:34

17 MR. CHANDLER: Objection. Form. 10:34

18 THE WITNESS: Not that I can recall at this 10:34

19 moment. 10:34

20 BY MS. ZHONG: 10:34

21 Q. Okay. And did Harris expressly suggest or 10:34

22 disclose pinning VDD, VDDQ and VDDL independently? 10:34

23 A. I don't recall it having -- I don't recall 10:35

24 it specifying one way or the other. 10:35

25 Q. Okay. Do you have access to Exhibit Share? 10:35

1 A. Yes. 10:36
2 Q. Can you search for an Exhibit 2101. 10:36
3 A. Did you recently update it? 10:36
4 Q. Yeah. 10:36
5 A. Okay. 10:36
6 Q. You may have to refresh the folder. 10:36
7 A. Yep. Hold on. Let me -- 10:36
8 MR. CHANDLER: Is this a new exhibit or is 10:36
9 this one that was premarked? 10:37
10 MS. ZHONG: Yes. It was starting with 2100 10:37
11 and then later, I just introduced it. 10:37
12 MR. CHANDLER: Just one moment, please, 10:37
13 then. Okay. I've got it, 2101. 10:37
14 (Exhibit 2101 introduced as an Exhibit
15 on the record.) 10:37
16 BY MS. ZHONG: 10:37
17 Q. Okay. Exhibit 2101 is a deck of slides with 10:37
18 the title "Fully Buffered DIMM (FB-DIMM) Design 10:37
19 Consideration," dated February 18, 2004, by Intel. 10:37
20 Do you see that? 10:38
21 A. I see that's how it's marked. 10:38
22 MR. CHANDLER: Annita, I apologize. Can we 10:38
23 go off the record? My colleague is having trouble 10:38
24 with the Exhibit Share. 10:38
25 MS. ZHONG: Okay. 10:38

1 DEPOSITION REPORTER: We are off the record. 10:38
2 (Off the record.) 10:45
3 BY MS. ZHONG: 10:45
4 Q. So, Dr. Wolfe, can you please go to page 27 10:45
5 of this Exhibit 2101. 10:45
6 A. Okay. 10:46
7 Q. By the way, have you seen this document 10:46
8 before? 10:46
9 A. Not that I can recall. 10:46
10 Q. On page 27 -- 10:46
11 MR. CHANDLER: Based on -- 10:46
12 MS. ZHONG: Sorry.
13 MR. CHANDLER: Sorry, Annita, based on that, 10:46
14 we would object to the exhibit as hearsay and 10:46
15 lacking authentication, and I don't believe it 10:46
16 relates to any exhibit that either expert introduced 10:46
17 as part of their declaration. I apologize. 10:46
18 Go ahead. 10:46
19 BY MS. ZHONG: 10:46
20 Q. Are you on page -- okay. 10:46
21 Are you on page 27, Dr. Wolfe? 10:46
22 A. Yes. 10:46
23 Q. Do you see the third bullet point? 10:46
24 A. Yes. 10:47
25 Q. Okay. So according to this presentation by 10:47

Page 42

1 Intel, three regulators are used, one for the 1.8 10:47
2 volts, one for the 0.9 volts and the one for the 1.5 10:47
3 volts; correct? 10:47
4 A. I would take exception with the word "used." 10:47
5 This appears, from what I can see, to be a 10:47
6 preliminary proposal that predates JEDEC. To that 10:47
7 extent, it does say that three voltage regulators 10:47
8 are used, but it doesn't say that only three voltage 10:47
9 regulators are used. 10:47
10 If one actually looks at the actual JESD205 10:47
11 specification, it's very clear that in the actual 10:47
12 JEDEC specification, there are four voltages that 10:47
13 would require four voltage regulators in most 10:48
14 situations. 10:48
15 Q. And when you say "four voltage regulators," 10:48
16 what is the fourth one? 10:48
17 A. VDDSPD is clearly recited as an additional 10:48
18 voltage in JEDEC standard 205, and then as I said in 10:48
19 my report, it would also be obvious, although not 10:48
20 required, to use more than one regulator for a 10:48
21 specific voltage when it's being used for multiple 10:48
22 purposes. 10:48
23 Q. Now, Intel knows DDR2 would have VDD, VDDQ 10:48
24 and VDDL; correct? 10:48
25 A. Presumably somebody at Intel does. 10:48

1 Q. Okay. And even though Intel knows that 10:48
2 there are three different voltage pins for DDR2, as 10:48
3 far as 1.8 volt is concerned, they are only stating 10:49
4 that it is using one voltage regulator; right? 10:49
5 MR. CHANDLER: Object to form. 10:49
6 THE WITNESS: As a minimum perhaps. I mean, 10:49
7 clearly, they haven't listed all the voltage 10:49
8 regulators here. We know that by looking at the 10:49
9 standard. 10:49
10 So at a minimum, I would think you would 10:49
11 only need one 1.8-volt voltage regulator, but as I 10:49
12 stated, it would be obvious if you were using more 10:49
13 than 1.8 volts for more than one purpose that you 10:49
14 could also use more than one 1.8-volt regulator. 10:49
15 BY MS. ZHONG: 10:49
16 Q. And it would also be obvious not to use -- 10:49
17 would it be obvious to use only a single voltage 10:49
18 regulator for the 1.8 volts? 10:49
19 A. Under certain circumstances, yes, depending 10:49
20 on exactly what the details of the design were. I 10:49
21 think both would be obvious solutions. 10:49
22 Q. Okay. And under what circumstances would 10:50
23 different voltage regulators be used -- let me 10:50
24 withdraw and ask. 10:50
25 You mentioned earlier you would use 10:50

1 different -- separate voltage regulators if you want 10:50
2 to sequence the power supply differently, if you 10:50
3 want to turn them on and off independently, or for a 10:50
4 power efficiency reason; right? 10:50
5 A. I think I also mentioned cost efficiency. 10:50
6 Q. Okay.
7 A. And of course, the other reason would be to 10:50
8 eliminate cross-coupling of noise. 10:50
9 Q. When you say "cost efficiency," what exactly 10:50
10 do you mean? 10:50
11 A. Depending on the circumstances, two smaller 10:50
12 regulators can sometimes be cheaper than one larger 10:50
13 one. 10:51
14 Q. Why? Two small regulators would be cheaper 10:51
15 than one large one? 10:51
16 A. It depends on the circumstances. But for 10:51
17 example, you may need a smaller -- small inductors 10:51
18 can be cheaper than large inductors, small
19 capacitors --
20 (Clarification requested by Reporter.) 10:51
21 THE WITNESS: Right. It can be that certain 10:51
22 support components are cheaper when they're smaller, 10:51
23 even less than half the price. It can also be that 10:51
24 the packaging of a low-power regulator can be much 10:51
25 less costly than a higher power regulator. 10:51

1 It can have to do with physical size. If 10:51
2 you've got spacing constraints or you have space 10:51
3 available in two different spots on the DIMM, but 10:51
4 you can't combine that space into a single spot. 10:51
5 So it's a number of ordinary engineering 10:52
6 factors that you would consider that would allow you 10:52
7 in a situation where you have two different things 10:52
8 that are being supplied by the same voltage to 10:52
9 consider the ordinary options of using one supply 10:52
10 for both or two supplies. 10:52
11 BY MS. ZHONG: 10:52
12 Q. And where in your declaration is that 10:52
13 analyzed? 10:52
14 A. I don't recall. 10:52
15 Q. You don't recall? Okay. 10:52
16 A. I certainly discuss it in paragraph 256 with 10:52
17 respect to VCC and VCC FBD, but I don't -- and it's 10:53
18 the same issue, but I don't recall where or if it's 10:53
19 discussed with respect to VDD. 10:53
20 Q. Where is the cost efficiency discussed? 10:53
21 A. I simply refer to it as "efficiency." I 10:53
22 don't break that out in this particular paragraph to 10:53
23 cost and power efficiency. 10:53
24 Q. Now, Harris does not suggest having VCC and 10:53
25 VCC FBDs separately; correct? 10:54

1 MR. CHANDLER: Objection. Form. 10:54

2 THE WITNESS: I don't recall Harris 10:54

3 specifically saying that. I attributed that to 10:54

4 the knowledge of a person who was very skilled 10:54

5 in the art. 10:54

6 BY MS. ZHONG: 10:54

7 Q. Okay. And is there a sequencing requirement 10:54

8 for VCC and VCC FBD anywhere in the standard or in 10:54

9 Harris? 10:55

10 A. I don't recall. 10:55

11 Q. Okay. Is there a requirement for separately 10:55

12 or independently turning VCC and VCC FBD on in the 10:55

13 standard? 10:55

14 A. I don't recall whether that is required by 10:55

15 the standard or not. 10:55

16 Q. Are VCC and VCC FBD used to supply use for 10:55

17 analog and digital applications -- let me withdraw 10:55

18 and ask. 10:55

19 Is one of the VCC and VCC FBD used for 10:55

20 analog application and the other one used for 10:55

21 digital application? 10:55

22 MR. CHANDLER: Objection. Form. 10:56

23 THE WITNESS: Whether or not those are the 10:56

24 best words is a bit of a judgment call. One is used 10:56

25 for I/O and one is used for core operation. 10:56

1 Because high-speed I/Os typically have 10:56
2 analog properties, it is known in the art to have 10:56
3 separate power supplies for high-speed I/Os because 10:56
4 they suffer from the same noise-coupling problems as 10:56
5 analog circuits. 10:57
6 BY MS. ZHONG: 10:57
7 Q. But instead FB-DIMM, a single-power supply 10:57
8 is used to supply both the VCC and the VCC FBD; 10:57
9 correct? 10:57
10 MR. CHANDLER: Objection. Form. 10:57
11 THE WITNESS: I don't know that that's 10:57
12 necessarily true. They are listed as separate power 10:57
13 supplies. They are supplied through separate pins. 10:57
14 That would indicate to me that the system designers, 10:57
15 at least explicitly had given the option of 10:57
16 segregating them. 10:57
17 BY MS. ZHONG:
18 Q. In the standard FB-DIMMs, there are no 10:57
19 separate pins for VCC and VCC FBD; correct? 10:57
20 MR. CHANDLER: Objection. Form. 10:58
21 THE WITNESS: Not on the DIMM itself, but on 10:58
22 the AMB chip, they are separated and, therefore, 10:58
23 they could be separated and separately supplied. 10:58
24 BY MS. ZHONG: 10:58
25 Q. And have you seen any designs in which 10:58

1 different regulators are used to supply VCC and 10:58
2 VCC FBD? 10:58
3 A. Not for an unmodified FB-DIMM, but I believe 10:58
4 that that's what's taught by the references that I 10:58
5 cited in my declaration. 10:58
6 Q. Which reference are you referring to? 10:58
7 A. I think when you combine Harris with JEDEC, 10:58
8 and Harris talks about the idea that you can have 10:59
9 various kinds of DRAM and various kinds of DIMMs, I 10:59
10 think that would encourage one to look at the 10:59
11 natural obvious variations of a -- of a DIMM. 10:59
12 And because JDESD82-20 specifies that VCC 10:59
13 and VCC FBD have separate pins and separate 10:59
14 functions, it would be obvious for one to separate 10:59
15 the power supplies for them. 10:59
16 Q. Does Harris mention using separate 10:59
17 regulators for even VCC and VDD? 11:00
18 A. Not by itself. But in combination with 11:00
19 those other references, including JEDEC 82-20, it 11:00
20 would be obvious. 11:00
21 Q. Harris does not suggest using separate 11:00
22 regulators for VCC and VDD; correct? 11:00
23 A. For VCC and VDD? 11:00
24 MR. CHANDLER: Objection. Form. 11:00
25 THE WITNESS: I believe it does. There are 11:00

1 separate outputs from the voltage regulator module 11:00
2 and I think a person of ordinary skill would 11:00
3 understand them to be separate regulators in Harris. 11:00
4 BY MS. ZHONG: 11:00
5 Q. So if there are different voltage outputs 11:00
6 from a regulator module, then they necessarily are 11:00
7 from different regulators? 11:00
8 A. Not necessarily, but that would be the most 11:00
9 common way to implement them. 11:01
10 Q. Okay. And if you look at paragraph 10 of 11:01
11 Harris, which is Exhibit 1023, on page 8 of 11:01
12 paragraph 10, it states: 11:01
13 "Preferably, a high-frequency 11:01
14 switching and voltage converter 11:01
15 capable of generating tightly- 11:01
16 controlled voltage levels may be 11:01
17 implemented as the on-board VRM 102 11:01
18 for purposes of the present patent 11:01
19 disclosure." 11:01
20 Do you see that? 11:01
21 A. I do see that. 11:01
22 Q. It says "a high frequency switching voltage 11:01
23 converter"; right? 11:02
24 MR. CHANDLER: Objection. Form. 11:02
25 THE WITNESS: That is what it says in that 11:02

1 paragraph. But if you look -- 11:02

2 BY MS. ZHONG:

3 Q. Okay.

4 A. -- at Figure 1A, it shows one module and 11:02

5 Figure 1B shows plural voltage regulator modules, so 11:02

6 I think it's clear that there is a contemplation of 11:02

7 more than one. 11:02

8 And I also think that it's very clear that a 11:02

9 person of ordinary skill would understand that 11:02

10 generating two voltages with two voltage regulators 11:02

11 is obvious. 11:02

12 Q. Isn't it the case that for Figure 1B, there 11:02

13 are different voltage sources; correct? 11:02

14 A. Yes. 11:02

15 MR. CHANDLER: Objection. 11:02

16 BY MS. ZHONG: 11:02

17 Q. So each voltage regulator module corresponds 11:02

18 to one voltage source; correct? 11:02

19 MR. CHANDLER: Objection to form. 11:02

20 THE WITNESS: Well, it says they refer to 11:02

21 K voltage paths, and if you look at Figure 1B, the 11:03

22 Ks are in the outputs as well as the inputs so... 11:03

23 BY MS. ZHONG: 11:03

24 Q. So if you look at paragraph -- let's see, 11:03

25 paragraph 14, and in particular, look at the 11:03

1 right-hand column starting on the fourth line. 11:03
2 "A plurality of on-board VRMs." 11:03
3 "VRMs" refers to voltage regulation -- 11:03
4 regulator modules; correct? 11:03
5 A. Yes. 11:03
6 Q. Okay. 11:03
7 "A plurality of on-board VRMs 22-K, 11:03
8 K=1,2...N, are provided as part of 11:03
9 the memory/assembly module 100B 11:03
10 wherein each VRM is operable with an 11:03
11 independent voltage supply path for 11:04
12 locally converting an external supply 11:04
13 voltage into appropriate local 11:04
14 voltage levels." 11:04
15 Correct? 11:04
16 A. Yes. 11:04
17 Q. So each VRM is associated with a different 11:04
18 voltage supply path; correct? 11:04
19 MR. CHANDLER: Objection. Form. 11:04
20 BY MS. ZHONG: 11:05
21 Q. Dr. Wolfe? 11:05
22 A. I'm sorry. Is there a pending question? I 11:05
23 thought I answered it. 11:05
24 Q. Yeah. Yeah. So I said each VRM is 11:05
25 associated with a different voltage supply path; 11:05

1 correct? 11:05

2 MR. CHANDLER: Objection. Form. 11:05

3 THE WITNESS: That is what it says, yes. 11:05

4 BY MS. ZHONG: 11:05

5 Q. Okay. And but for each voltage path, both 11:05

6 VCC and VDD are generated; correct? 11:05

7 A. They are generated and they are generated by 11:05

8 the same module, but not necessarily by the same 11:05

9 regulator. It does say, for example, that the VDD 11:05

10 and VCC power supply rails are rendered independent 11:05

11 from external voltage sources. That would suggest 11:05

12 to me that they are separately rendered. 11:06

13 But certainly, it would at least be obvious 11:06

14 to do that. A voltage regulation regulator module, 11:06

15 I think, can contain more than one regulator. 11:06

16 Q. Okay. And but it was well known at the time 11:06

17 of the invention that you can have a single-voltage 11:06

18 converter to generate two different voltage levels; 11:06

19 correct? 11:06

20 MR. CHANDLER: Objection. Form. 11:06

21 THE WITNESS: It was possible under some 11:06

22 circumstances, but certainly not the most common 11:06

23 thing to do. Normally, if you need to generate 11:06

24 multiple output voltages, you would use multiple 11:06

25 regulators, especially in a high-current situation 11:06

1 like this one. 11:06

2 BY MS. ZHONG: 11:06

3 Q. Okay. Where space is a concern, would there 11:06

4 be advantage of having a single-voltage regulator to 11:06

5 generate two different voltages? 11:07

6 A. Unlikely because a regulator that generates 11:07

7 multiple voltages is more complicated than a 11:07

8 regulator that generates one. 11:07

9 Q. But if it's implemented ICs, it would still 11:07

10 be smaller; right, and -- 11:07

11 A. Not necessarily, because almost all 11:07

12 regulators require some external components as well, 11:07

13 and those tend to multiply with -- based on the 11:07

14 number of voltages that are being supported. 11:07

15 Q. But you will need the same number of 11:07

16 external components whether you use three regulators 11:07

17 or one regulator. Isn't that the case? 11:07

18 A. You might -- you would have to look at the 11:07

19 particular circumstances. You might need the same 11:07

20 number of external components and you would likely 11:07

21 need the same number of pins. So, generally, one 11:08

22 would not deal with the circuit level complexity of 11:08

23 trying to support multiple voltages with a single 11:08

24 regulator. 11:08

25 Q. When would you use a single regulator to 11:08

1 generate different voltage levels? 11:08

2 A. I think that there are certain circumstances 11:08

3 where the voltages need to closely track each other, 11:08

4 where one might consider that as an option. But as 11:08

5 I said, it's unusual. It's not the normal approach 11:08

6 to multiple power supply voltages in a computer 11:08

7 system in my experience. 11:08

8 Q. So, for example, if VTT needs to track a VDD 11:08

9 closely, it would make sense to have a single 11:08

10 regulator to generate them both? 11:08

11 A. It would be one option. But one can also 11:08

12 simply couple the feedback from the two and use 11:09

13 separate regulators. Both are well known options. 11:09

14 Q. Is a pulse-width modulator voltage converter 11:09

15 synonym to a buck converter? 11:09

16 MR. CHANDLER: Objection. Form. And I 11:09

17 didn't quite hear all the words either. 11:09

18 DEPOSITION REPORTER: Ms. Zhong, I didn't 11:09

19 get all the words either. 11:09

20 BY MS. ZHONG: 11:09

21 Q. So is a pulse-width modulated converter a 11:09

22 synonym to a buck converter? 11:09

23 MR. CHANDLER: And you are saying width, 11:10

24 pulse, w-i-d-t-h, pulse width modulator? 11:10

25 MS. ZHONG: Pulse width, yes, yes. 11:10

1 MR. CHANDLER: I get it. 11:10

2 THE WITNESS: In my experience, those are 11:10

3 not synonyms, but in this context, pulse-width 11:10

4 modulated controller is referring to a buck 11:10

5 converter because it is referring to a switching 11:10

6 down converter from a 12-volt supply to a .5 to 11:10

7 3.5-volt supply, and one would understand a 11:10

8 pulse-width modulated voltage converter that inverts 11:10

9 between those particular voltages in this particular 11:10

10 kind of a system to be a buck converter. 11:10

11 BY MS. ZHONG:

12 Q. Can a switching regulator be a switched or a 11:10

13 switching capacitor regulator? 11:11

14 MR. CHANDLER: Objection. Form. 11:11

15 DEPOSITION REPORTER: Excuse me.

16 "Objection, form," and what was after that,

17 Mr. Chandler?

18 MR. CHANDLER: Just a cough after objection, 11:11

19 form. 11:11

20 MS. ZHONG: Janis, it's capacitor, not 11:11

21 compass. 11:11

22 THE WITNESS: I don't believe that a switch 11:11

23 capacitor regulator would be suitable for this kind 11:11

24 of a system, and it certainly would not be one that 11:11

25 a person of ordinary skill would think that Harris 11:11

1 is referring to. 11:11

2 BY MS. ZHONG: 11:11

3 Q. Why not? 11:11

4 A. Because to provide high currents, such a 11:11

5 system would be -- would require a very large 11:11

6 capacitor and wouldn't be suitable for positioning 11:11

7 on a -- on a DIMM. 11:11

8 An ordinary buck converter at this time was 11:12

9 cheap, it was efficient, it was what was commonly 11:12

10 used for voltage-down conversion in computer 11:12

11 systems. It was available off-the-shelf and, in 11:12

12 particular, it was available in designs that had 11:12

13 been pre-tuned to supply voltages to memory modules. 11:12

14 So I think that that would clearly have been 11:12

15 the first thought of a person of ordinary skill in 11:12

16 reading this paragraph. 11:12

17 Q. And what was the efficiency of buck 11:12

18 convertors at the time of the invention? 11:12

19 A. It varies from situation to situation. But 11:12

20 typically, in the 80 to 98 percent range. 11:12

21 Q. And what is the basis for that? 11:12

22 A. My recollection. 11:12

23 Q. Are there any data sheets backing up that 11:13

24 recollection? 11:13

25 MR. CHANDLER: Objection. Form. 11:13

1 THE WITNESS: As I said, it would depend on 11:13
2 the particular situation. We did cite to some data 11:13
3 sheets. I don't remember [simultaneous speakers] -- 11:13
4 DEPOSITION REPORTER: Excuse me, I need one
5 at a time. 11:13
6 MS. ZHONG: I don't know what you were 11:13
7 referring to. 11:13
8 DEPOSITION REPORTER: You started speaking 11:13
9 in the middle of the answer. So I lost a couple 11:13
10 words is what happened. 11:13
11 MS. ZHONG: That's okay. 11:13
12 BY MS. ZHONG: 11:13
13 Q. Did you cite any data sheets that is 11:13
14 specific for the FB-DIMM application? 11:13
15 A. I cited data sheets to show that appropriate 11:13
16 regulators were available, not for the specific 11:14
17 purpose of citing efficiency numbers. 11:14
18 Q. Okay. So for the particular regulators you 11:14
19 cited, what were the efficiencies? 11:14
20 MR. CHANDLER: Objection. Form. 11:14
21 THE WITNESS: Again, it would depend on the 11:14
22 circumstances. Let me see if they're disclosed 11:14
23 here. 11:14
24 So if we look at Exhibit 1040 -- 11:14
25 / / / 11:15

1 BY MS. ZHONG: 11:15

2 Q. Uh-huh. 11:15

3 A. -- on page 23. 11:15

4 Q. Page 23. Hold on. Okay. 11:15

5 A. There is a graph that shows that, for 11:15

6 example, an output current of 1 amp, the 11:15

7 efficiency -- 11:15

8 Q. Uh-huh.

9 A. -- is approximately 95 percent from a 11:15

10 12-volt input. 11:15

11 Q. Okay. For this one, do you see an input 11:15

12 overvoltage regulation anywhere? 11:15

13 MR. CHANDLER: Objection. Form. 11:15

14 THE WITNESS: Yes. Figure 15 shows an 11:15

15 overvoltage protection threshold. 11:15

16 BY MS. ZHONG: 11:15

17 Q. That's for the output, I believe. 11:16

18 A. It says "V-in." Let's see. Oh, that's a 11:16

19 voltage output. 11:16

20 Q. I see UVLO, which is for the undervoltage 11:16

21 lockout on the input side. I see the undervoltage 11:16

22 protection, overvoltage protection on the output 11:16

23 side, but I don't see a corresponding overvoltage 11:16

24 protection on the input side. 11:16

25 So, for example, on page 4, if you look at 11:16

1 the electrical characteristics. 11:17

2 A. Yeah, that's where I'm at. I believe that 11:17

3 this particular device has an undervoltage input 11:17

4 protection and an overcurrent input protection. 11:17

5 Q. But not overvoltage input -- there is no 11:17

6 input voltage overvoltage protection as far as you 11:17

7 can tell; correct? 11:17

8 A. At the moment, I don't see one disclosed. 11:17

9 Q. What would be the reason for not having 11:17

10 input voltage overvoltage protection? 11:17

11 A. It may be that for this particular design, 11:17

12 they felt that overcurrent protection was more 11:18

13 important. 11:18

14 Q. But why would they have an undervoltage -- 11:18

15 why would they have an undervoltage input -- let me 11:18

16 try again. 11:18

17 Why would they have an input undervoltage 11:18

18 lockout, but not the overvoltage lockout? 11:18

19 A. It's possible by having an output 11:18

20 overvoltage and undervoltage protection, they can 11:18

21 reduce the need for an input overvoltage protection 11:18

22 because they're still protecting the circuits on the 11:18

23 other side. That if an overvoltage at the input 11:18

24 causes an overvoltage at the output or an 11:19

25 undervoltage at the output, it will still be 11:19

1 detected and, therefore, it's not necessary to 11:19
2 monitor it separately in this particular device. 11:19
3 Q. Okay. Can you take a look at Exhibit 1041 11:19
4 as well, and let me know whether you see an input 11:19
5 overvoltage protection or lockout in this particular 11:19
6 case. 11:19
7 A. I believe this particular one works in the 11:20
8 same way, where it has an overcurrent protection on 11:20
9 the input, and overvoltage and undervoltage 11:20
10 protections on the output, and an undervoltage 11:20
11 protection on the input. And for this particular 11:20
12 device, it determined that those are sufficient. 11:20
13 Q. Okay. Now, let's go back to Harris. 11:20
14 A. Okay. 11:20
15 Q. Is an LDO a buck converter? 11:20
16 A. I don't think it's clear from the disclosure 11:21
17 in Harris. There are buck converters that are 11:21
18 called low dropout buck converters, so that may be 11:21
19 what he's referring to. That's a possibility. 11:21
20 BY MS. ZHONG: 11:21
21 Q. But LDOs usually refer to linear regulators? 11:21
22 A. LDOs usually refer to linear regulators, but 11:21
23 again, not always. If you look at data sheets from 11:21
24 buck converters, some of them are described as LDO. 11:21
25 When the words converter's used, that usually 11:21

1 suggests to me it is a switching converter. 11:22

2 I'm not really familiar with linear 11:22

3 regulators being called inverters very often or, 11:22

4 actually, at all off the top of my head. 11:22

5 So I think, most likely, he's talking about 11:22

6 a low dropout buck converter there, but it wasn't 11:22

7 something that really made a difference to my 11:22

8 opinion one way or the other. 11:22

9 Q. And do host system usually supply 11:22

10 unregulated supply voltages? 11:22

11 A. Usually? I mean, it depends what the system 11:22

12 is. In PCs, it's more common to supply regulated 11:22

13 voltages or in modern computers in general, it is 11:22

14 more common to supply regulated voltages, but -- 11:22

15 Q. Are you aware -- 11:23

16 A. -- but I am aware of times in the past where 11:23

17 computers supplied an unregulated voltage into a 11:23

18 module. 11:23

19 Q. So at the time of the invention -- let me 11:23

20 withdraw and ask you this question. 11:23

21 So for computers designed to work with 11:23

22 FB-DIMMs, do those computer system supply regulated 11:23

23 voltages or unregulated voltages to the FB-DIMM? 11:23

24 A. All the ones I'm familiar with supply 11:23

25 regulated voltages. 11:23

1 Q. Okay. What about the PSU units on the 11:23
2 computer systems, do they output regulated or 11:23
3 unregulated voltages? 11:24
4 MR. CHANDLER: Objection. Form. 11:24
5 THE WITNESS: In the kinds of computer 11:24
6 systems that would use a FB-DIMM, in my experience, 11:24
7 those are regulated voltages coming out of the power 11:24
8 supply unit. 11:24
9 BY MS. ZHONG: 11:24
10 Q. Okay. What is a regulated supply voltage 11:24
11 versus an unregulated supply voltage? Let me 11:24
12 withdraw and ask. 11:24
13 A. Yeah.
14 Q. So what is the difference between a 11:24
15 regulated versus an unregulated supply voltage? 11:24
16 A. Yeah. Let me answer this very, very 11:24
17 carefully because the -- it's tied to the idea that 11:24
18 nothing is perfect. 11:24
19 Q. Okay. 11:24
20 A. But, typically, an unregulated supply 11:24
21 voltage would vary its output roughly in proportion 11:25
22 to variations in the input voltage. So if the input 11:25
23 voltage changed by 5 percent, the output voltage 11:25
24 would change by 5 percent. 11:25
25 A regulated voltage means that we have 11:25

1 attempted to make the output voltage not vary when 11:25
2 the input voltage varies, but in practice, there 11:25
3 would still be some variation, just much less than 11:25
4 in an unregulated system. 11:25
5 Q. So in the regulated -- let me put it this 11:25
6 way. 11:25
7 For a regulator to provide a regulated 11:25
8 supply voltage, there is usually a feedback loop to 11:26
9 make sure that the output stays within a tightly 11:26
10 controlled range -- 11:26
11 MR. CHANDLER: Objection. Form.
12 BY MS. ZHONG:
13 Q. -- is that right? 11:26
14 MR. CHANDLER: Objection. Form. 11:26
15 THE WITNESS: Often, there's a feedback 11:26
16 loop. It's not necessary that there be a feedback 11:26
17 loop as long as there is some type of a reference or 11:26
18 some type of -- of decoupling between input 11:26
19 variations and output variations. 11:26
20 A feedback loop allows one to maintain 11:26
21 regulation as the current varies and most modern 11:26
22 voltage-regulated systems would include that 11:26
23 capability. 11:26
24 BY MS. ZHONG: 11:26
25 Q. So are feedback loops used in unregulated -- 11:26

1 let me withdraw and ask. 11:26

2 So are feedback loops used to provide the 11:26

3 unregulated supply of voltages? 11:27

4 MR. CHANDLER: Objection. Form. 11:27

5 THE WITNESS: They could be, but I would not 11:27

6 think that that's very common. Again, the feedback 11:27

7 is somewhat separate from the fact or absence of 11:27

8 regulation. A feedback loop is used to maintain 11:27

9 stability in light of current variations, 11:27

10 temperature changes, and other factors. 11:27

11 BY MS. ZHONG: 11:27

12 Q. Okay. So to you, the main difference 11:27

13 between regulated and unregulated voltage is whether 11:27

14 there is coupling or decoupling between the input 11:27

15 voltage variation and the output voltage variation; 11:28

16 is that correct? 11:28

17 A. Yes, with the understanding that there's 11:28

18 always some coupling. It's whether or not it's 11:28

19 being substantially reduced, whether or not the 11:28

20 circuit is attempting to maintain a fixed output 11:28

21 voltage despite potential variations in the input 11:28

22 voltage. 11:28

23 Q. Okay. So if, as in Harris, the supply 11:28

24 voltage has a plus-minus 15 percent margin, does 11:28

25 that indicate to a POSITA that this is an 11:28

1 unregulated voltage source? 11:28

2 A. Not necessarily. It could just be a 11:28

3 regulated voltage source that doesn't have precise 11:29

4 regulation. But in any case, Harris specifically 11:29

5 tells us that it supports both regulated and 11:29

6 unregulated voltage input sources. 11:29

7 Q. Harris mentions external power source in, 11:29

8 for example, Figure 1A; correct? 11:29

9 A. External voltage source. 11:29

10 Q. What is "external voltage source"? 11:29

11 A. It's one that comes from off the DIMM. 11:29

12 Q. So in your mind, a voltage source that comes 11:29

13 from the host is also an external voltage source? 11:30

14 A. With respect to Harris' figures, I would 11:30

15 think that's correct. 11:30

16 Q. And so when Harris mentions external source 11:30

17 path 104, to you that just means a path to a voltage 11:30

18 source that's off the DIMM; is that correct? 11:30

19 A. Yes. 11:30

20 (Clarification requested by Reporter.) 11:30

21 BY MS. ZHONG: 11:30

22 Q. So external source path 104 in Harris, to 11:31

23 you, does not mean there is something that means an 11:31

24 internal source path in Harris; is that right? 11:31

25 MR. CHANDLER: Objection to form. 11:31

1 THE WITNESS: I'm sorry. I missed some 11:31
2 words. 11:31
3 BY MS. ZHONG:
4 Q. So if you have an external source path, then 11:31
5 one would think of there is going to be an internal 11:31
6 source path as well; correct? 11:31
7 MR. CHANDLER: Objection. Form. 11:31
8 THE WITNESS: Not necessarily, but I do 11:31
9 believe that with respect to Harris' drawings, 104 11:31
10 is an external voltage and 106 and 108 are internal 11:31
11 voltages. 11:31
12 BY MS. ZHONG: 11:31
13 Q. So to you, internal voltage source path will 11:31
14 be 106 and 108? 11:31
15 MR. CHANDLER: Objection. Form. 11:31
16 THE WITNESS: Those would be examples of 11:31
17 what a person of ordinary skill might call an 11:31
18 internal voltage source on those drawings. 11:32
19 BY MS. ZHONG: 11:32
20 Q. Where in Harris does it disclose that the 11:32
21 external voltage source comes from host system? 11:32
22 A. Well, I think there's a couple things that 11:32
23 push us in that direction. 11:33
24 Q. Okay. 11:33
25 A. One is that Harris tells us that these are 11:33

1	supplied on the DIMM pins. And normally, all the	11:33
2	pins to a DIMM connect to the host. So that would	11:34
3	lead one to expect that voltage to come from the	11:34
4	host.	11:34
5	Secondly, there are claims on a computer	11:34
6	system that describe that voltage that would be	11:34
7	indicative. In general, the discussion of the	11:34
8	external voltage source is in the context of a	11:34
9	memory board assembly. So, again, that would lead	11:34
10	one to think that it's external from the memory	11:34
11	board assembly and not necessarily external from	11:34
12	anything else.	11:34
13	And then on top of all that, I think there	11:34
14	is just some commonsense that anyone who's designed	11:34
15	or built a computer understands that there is	11:34
16	typically a single-power supply, the host power	11:35
17	supply, and that for both safety and convenience	11:35
18	reasons, memories are powered from the host power	11:35
19	supply, that it would be very difficult to make a	11:35
20	safe and reliable system where memories were not	11:35
21	powered by the computer system.	11:35
22	Q. Are you familiar with NV DIMMs?	11:35
23	A. I am familiar with the concept of an	11:35
24	NV DIMM, but I don't know the details of the	11:36
25	specification.	11:36

1 Q. Do you know if NV DIMMs usually includes a 11:36
2 plug to which a power module is connected? 11:36
3 A. I'm not familiar with those details. 11:36
4 MR. CHANDLER: Objection. Form. 11:36
5 BY MS. ZHONG: 11:36
6 Q. And do you know that NV DIMM, the power 11:36
7 module actually supplies the -- can supply power to 11:36
8 the NV DIMM through that plug? 11:36
9 MR. CHANDLER: Objection. Form. 11:36
10 THE WITNESS: Again, I'm not familiar with 11:36
11 the details of that specification, but even if that 11:36
12 were the case, I'm not sure I would consider that 11:36
13 power supply to be separate and not part of the host 11:36
14 computer. 11:36
15 BY MS. ZHONG: 11:37
16 Q. Even if that power module does not draw 11:37
17 power from the host? 11:37
18 A. I'd have to look at the details, but -- 11:37
19 Q. Even if the power supply, for example, comes 11:37
20 from a capacitor or a battery? 11:37
21 A. Again, I'd have to look at the details. But 11:37
22 certainly, there is battery power in most computers. 11:37
23 That's part of the host system. The battery in my 11:37
24 laptop is part of the host system. 11:37
25 MR. CHANDLER: I had an objection to the 11:37

1 form of the question. 11:37

2 BY MS. ZHONG:

3 Q. And you have no idea where the -- how in the 11:37

4 NV system -- let me withdraw that question. 11:37

5 So you basically have not considered how the 11:38

6 NV DIMMs can be powered; correct? 11:38

7 MR. CHANDLER: Objection. Form. 11:38

8 THE WITNESS: With respect to this 11:38

9 declaration, I have not considered anything about 11:38

10 the NV DIMMs. 11:38

11 BY MS. ZHONG: 11:38

12 Q. Okay. And can you look at paragraph 19 of 11:38

13 Harris. What does Harris mean when it says the 11:38

14 system board power supply and associated voltage 11:39

15 planes are eliminated? 11:39

16 A. It means the specific voltage planes that 11:39

17 are otherwise necessary to supply VDD and VCC to 11:39

18 memory modules in certain prior art systems. 11:39

19 Q. So, for example, the 1.8 volt, the 1.5 volt 11:39

20 voltage rails are removed from the motherboard? Is 11:39

21 that what Harris means? 11:39

22 A. He doesn't get quite that specific, but he 11:39

23 means that the specific highly regulated memory 11:40

24 specific power rails need not be generated on the 11:40

25 motherboard. They can be generated locally on the 11:40

1 DIMM module. 11:40

2 Q. Okay. And specifically, he mentions the VCC 11:40

3 and the VDD; correct? 11:40

4 A. Yes, with reference to the memory module. 11:40

5 There are lots of VCCs and VDDs in a computer 11:40

6 system. He is specifically talking about the ones 11:40

7 on the memory module in a particular example. 11:40

8 As I've noted before, he also explains how 11:40

9 this could be useful to many other systems that have 11:40

10 different names for memories -- for memory voltages. 11:40

11 Q. Okay. So for the FB-DIMM example that you 11:40

12 relied on, what this sentence means is that the 11:40

13 1.8-volt power supply and the 1.5V power supply for 11:40

14 the FB-DIMM module, those power supplies and the 11:41

15 associated power planes are eliminated; is that 11:41

16 right? 11:41

17 MR. CHANDLER: Objection. Form. 11:41

18 THE WITNESS: It means that for purposes of 11:41

19 supplying memory chips on the DIMMs with power, that 11:41

20 can be done locally and need not be done in a 11:41

21 specifically low-voltage regulated form on the 11:41

22 motherboard. 11:41

23 Obviously, one would have to look at the 11:41

24 totality of the situation to see whether or not 11:41

25 there are other things on the motherboard that 11:41

1 require similar voltages and whether or not those 11:42
2 voltages had been shared with memory in a prior 11:42
3 design or whether they'd been distinct from memory 11:42
4 in a prior design. 11:42
5 BY MS. ZHONG: 11:42
6 Q. Now, Harris does not expressly state 11:42
7 generating VTT locally; correct? 11:42
8 A. Correct. One would have to look at Harris 11:42
9 in light of the other memory technologies that he 11:42
10 references. 11:42
11 Q. Okay. Harris -- a POSITA would be aware of 11:42
12 the usage of VDD -- VTT pins on a standard-compliant 11:42
13 FB-DIMM; correct? 11:42
14 MR. CHANDLER: Objection. Form. 11:42
15 THE WITNESS: Yes. A person of ordinary 11:42
16 skill would have been familiar with the VTT pins on 11:42
17 a standard JESD 205-compliant FB-DIMM. 11:43
18 BY MS. ZHONG:
19 Q. Okay. So Harris would presumably be aware 11:43
20 of that as well; correct? 11:43
21 A. Presumably, yes. 11:43
22 Q. Okay. Any reason for not generating VTT 11:43
23 locally on the DIMM board? 11:43
24 MR. CHANDLER: Objection. Form. 11:43
25 THE WITNESS: I think if you read Harris and 11:43

1 the FB-DIMM standard together, it's clear that it 11:43
2 would be preferable to do it locally. 11:43
3 BY MS. ZHONG: 11:43
4 Q. Any reason for not doing it locally? 11:43
5 A. It would depend on particular circumstances. 11:43
6 Because it has to track VDD in the standard, I think 11:43
7 it would be preferable to do it locally. 11:44
8 Q. When you say "it has to track VDD in the 11:44
9 standard," are you referring to the VDD of the DRAM? 11:44
10 A. Yes. The VDD in the DRAM would generally 11:44
11 have a relationship with the VTT. 11:44
12 May I -- give me a second. I will look at 11:44
13 Harris again. 11:44
14 Yeah. I think the subject just doesn't come 11:44
15 up in Harris. One would have to combine the 11:44
16 teachings. 11:45
17 Harris describes in paragraph 9 -- I think 11:45
18 that his teachings are broad enough to apply both to 11:45
19 memory technologies that have a separate VTT voltage 11:45
20 and those that don't. And that's why I think he 11:45
21 relies on the reader to determine how many voltages 11:45
22 need to be generated on the DIMM in a particular 11:45
23 embodiment. 11:45
24 Q. So at the time of the invention, are you 11:45
25 aware of any DIMMs that don't use VTT? 11:45

1 A. I believe older ones like S -- like single 11:46
2 data rate did not use VTT, if I recall correctly. 11:46
3 Q. Why don't they use VTT? 11:46
4 A. I'd have to go back and look. At one point, 11:46
5 termination was not required. And then later on, 11:46
6 separate termination voltages weren't used. A less 11:46
7 efficient method was used in which VDD was used 11:46
8 directly for termination. 11:46
9 But in any case, the teaching of Harris is 11:46
10 that you would convert the externally supplied 11:46
11 voltage into appropriate local voltage levels, and 11:46
12 he lists DDR2, DDR3 as examples. So a person of 11:46
13 ordinary skill would know what the appropriate 11:46
14 voltage levels are for those technologies. 11:46
15 Q. You say that "at one point, termination was 11:47
16 not required." 11:47
17 Why was that? 11:47
18 A. The signals were very slow. 11:47
19 Q. What do you mean by "slow"? 11:47
20 A. They had very slow rise and fall times. 11:47
21 In -- decades ago, it wasn't necessary to terminate 11:47
22 every signal. And as I mentioned, in some cases, 11:47
23 on-chip termination without separate termination 11:47
24 voltage was sufficient, although less efficient. 11:47
25 Q. So SDR falls into that category? 11:47

1 A. From what I can recall off the top of my 11:47
2 head. I would have to go back and look at the spec 11:47
3 to remember exactly when it changed. 11:47
4 Q. So as far as you recall, FDRs don't need a 11:47
5 VTT? 11:48
6 A. As far as I can recall right now, yes. 11:48
7 Q. What is the current draw for SPD? 11:48
8 MR. CHANDLER: Objection. Form.
9 THE WITNESS: How much current does it 11:48
10 draw? 11:48
11 BY MS. ZHONG: 11:48
12 Q. Yes, for the SPD on the FB-DIMM. 11:48
13 A. I don't see a specification. 11:48
14 Q. Do you have any -- based on your knowledge, 11:49
15 what is the general range of the current draw for 11:50
16 the SPD? 11:50
17 A. I wouldn't speculate. I would go find a 11:50
18 data sheet if I needed an example. 11:50
19 Q. Do you have any sense as to the range? 11:50
20 A. I wouldn't want to speculate. 11:50
21 Q. Is it tens of milliamps? 11:50
22 A. That's possible, but I don't know, not 11:50
23 without looking at a reference. 11:50
24 Q. Are you aware of any buck converter used for 11:50
25 generating the voltage used to operate the SPD? 11:50

1 MR. CHANDLER: Objection. Form. 11:50

2 THE WITNESS: In an actual product? 11:50

3 BY MS. ZHONG: 11:50

4 Q. Did you cite any data sheets that's for 11:50

5 generating the SPD supply voltage? 11:51

6 A. Well, the SPD is 3.3 volts. Let me look. I 11:51

7 think that some of the data -- buck converter data 11:51

8 sheets that I -- 11:51

9 Q. But are they -- did they say they are 11:51

10 designed for use with SPD? 11:51

11 A. I don't think they specifically mention it. 11:51

12 I mean, in general, power generation chips don't 11:51

13 specify a particular component. Engineers use 11:51

14 voltage and current specifications to choose an 11:51

15 appropriate voltage regulator. 11:51

16 The regulator in Exhibit 1048, for example, 11:51

17 puts out appropriate voltages, and that's what a 11:52

18 person of ordinary skill would do is they would 11:52

19 simply look for something that's suitable. 11:52

20 Q. Are you aware of any use -- are you aware of 11:52

21 any computer system designs in which a buck 11:52

22 regulator is used to generate the VDD for the SPD? 11:52

23 A. I haven't looked one way or another in 11:52

24 actual designs. 11:52

25 Q. Okay. Do you know what kind of regulator is 11:52

1 used to generate a VDD SPD in the DDR5 DIMM modules? 11:52

2 A. No, not without referring to specifications. 11:52

3 Q. Would it you surprise that a linear LDO 11:52

4 regulator is used to generate VDDSPD? 11:53

5 MR. CHANDLER: Objection. Outside the scope 11:53

6 of direct. 11:53

7 THE WITNESS: It would not surprise me. 11:53

8 There are a range of voltages and currents where a 11:53

9 person of ordinary skill would understand that 11:53

10 either a buck converter or an LDO might be -- 11:53

11 regulator might be suitable, and they would make the 11:53

12 decision between them based on factors such as cost, 11:53

13 size, efficiency, heat generation, and other 11:53

14 factors. 11:53

15 BY MS. ZHONG: 11:53

16 Q. Does it surprise you that even though 11:53

17 DDR5 -- let me withdraw. 11:53

18 Does it surprise you that even though DDR5 11:53

19 DIMMs use a power management IC that includes 11:54

20 multiple buck converters, it would use a linear 11:54

21 regulator for generating a 1.8-volt needed to power 11:54

22 the SPD from a 12-volt input voltage? 11:54

23 MR. CHANDLER: Objection. Outside the scope 11:54

24 of direct. 11:54

25 THE WITNESS: No. It doesn't surprise me. 11:54

1 After looking at all the engineering considerations 11:54
2 it's quite possible that the implementer of that 11:54
3 module decided not to use a buck converter and to 11:54
4 use a linear regulator instead, likely because of 11:54
5 cost concerns. 11:54
6 BY MS. ZHONG: 11:54
7 Q. And what other reasons for not using a buck 11:54
8 converter? 11:54
9 MR. CHANDLER: Objection. Outside the scope 11:54
10 of direct. 11:54
11 THE WITNESS: It would depend on the details 11:54
12 of that particular implementation. But in my 11:54
13 experience, in a modern computer system, even where 11:55
14 a buck converter might be suitable, oftentimes it's 11:55
15 not selected and an LDO regulator is selected 11:55
16 instead for cost reasons or for space reasons. 11:55
17 BY MS. ZHONG: 11:55
18 Q. And an LDO is selected over a buck 11:55
19 converter, especially when the current is low; 11:55
20 correct? 11:55
21 MR. CHANDLER: Objection. Form. 11:55
22 THE WITNESS: It can be either way, right. 11:55
23 So, you know, a cell phone in sleep mode uses very, 11:55
24 very low currents and yet would typically use a 11:55
25 buck -- a buck converter because of the efficiency. 11:55

1 It's a host of things that are taken into 11:55
2 consideration, and there are many situations where 11:56
3 either one is suitable, but there are different 11:56
4 costs, there are different size constraints, there 11:56
5 are different efficiency levels, and one makes -- 11:56
6 uses one's engineering judgment to decide between 11:56
7 two common alternatives. 11:56
8 BY MS. ZHONG: 11:56
9 Q. The fact is you are not aware of any usage 11:56
10 of a buck converter to generate VDDSPD in a computer 11:56
11 system; correct? 11:56
12 MR. CHANDLER: Objection. Form. 11:56
13 THE WITNESS: As I said, I haven't looked so 11:56
14 I'm not aware, but that's primarily because I 11:56
15 haven't looked. 11:56
16 BY MS. ZHONG: 11:56
17 Q. You basically did not cite an example where 11:56
18 a buck converter is used to generate VDDSPD; 11:56
19 correct? 11:56
20 A. Not in an actual computer system, but what I 11:56
21 did cite is the availability of suitable buck 11:56
22 converters to do so that would have been known to a 11:57
23 person of ordinary skill in the art at the time. 11:57
24 Q. So it is your position that as long as a 11:57
25 voltage regulator outputs the right voltage range, 11:57

1	then it can be used with the SPD?	11:57
2	A. No. I would -- it's a narrower -- no.	11:57
3	That's not right.	11:57
4	Q. Okay.	11:57
5	A. You know, there are a number of things that	11:57
6	have to be considered. I've talked about them.	11:57
7	It's the voltage, the current, the size, and noise	11:57
8	levels. And in this particular case, I identified	11:57
9	that a person of ordinary skill in the art would	11:57
10	have known of buck converters that were suitable to	11:57
11	generate the SPD at the time.	11:57
12	Q. What is the noise level required for	11:57
13	operating VDDSPD?	11:58
14	A. We would have to look at the specific	11:58
15	components. But, typically, it's something on the	11:58
16	order of plus/minus 5 percent.	11:58
17	Q. Where is that analyzed?	11:58
18	A. It would be on the EEPROM data sheet for the	11:58
19	SPD.	11:58
20	Q. Did you cite any SPD data sheets?	11:58
21	A. No.	11:58
22	Q. What is the current requirement for the SPD?	11:58
23	A. I think you asked me that already and I told	11:58
24	you that I didn't know off the top of my head.	11:58
25	Q. And what is the size requirement for usage	11:58

1 with the SPD? 11:58

2 A. That would depend on a particular DIMM 11:59

3 design, but certainly the small chips that I cited 11:59

4 to are suitable. 11:59

5 Q. And where is that analyzed, specifically for 11:59

6 SPD? 11:59

7 A. Where in my declaration? 11:59

8 Q. Correct. 11:59

9 A. Paragraph 286 -- 11:59

10 Q. Okay.

11 A. -- when I cite back to a number of other 12:01

12 things. 12:01

13 Q. Uh-huh. Can you tell me which one's 12:01

14 specific for the SPD? 12:01

15 DEPOSITION REPORTER: Excuse me. Did you 12:01

16 object, Mr. Chandler? 12:01

17 MR. CHANDLER: Just coughing. 12:01

18 THE WITNESS: There's only two sentences 12:01

19 there that's specific to a skilled artisan would 12:01

20 have understood it would have been obvious to 12:01

21 implement the high-frequency switching converter in 12:01

22 Harris for SPD as a buck converter. And then I 12:01

23 refer -- 12:01

24 Q. Uh-huh.

25 A. -- to paragraph 236, 146 to 149, where I 12:01

1 explain reasoning and then also to a bunch of other 12:01
2 exhibits. 12:02
3 (Clarification requested by Reporter.)
4 THE WITNESS: My reasoning and a bunch of 12:02
5 other references. 12:02
6 BY MS. ZHONG: 12:02
7 Q. Okay. So do any of the references you cited 12:02
8 refer specifically to SPD? 12:02
9 A. I don't recall if they refer to it by name. 12:02
10 I would be happy to look at each one if you'd like. 12:02
11 Q. Sure.
12 A. What they do is they refer to a range of 12:02
13 voltages and currents that would be suitable to 12:02
14 provide the voltage for an SPD, as I explained 12:02
15 earlier in the declaration, including in paragraph 12:02
16 236. 12:02
17 Q. Okay. So let's look at 146 to 149. I don't 12:03
18 see any analysis with respect to SPD. 12:03
19 A. Well, the relevancy is it explains that a 12:03
20 buck converter can be used to step down a voltage 12:03
21 from a higher voltage to a lower voltage. And in 12:03
22 the examples that I provided for Harris, the input 12:03
23 voltage would be 12 volts, and the output voltage 12:03
24 would be 3.3 volts and, therefore, a buck converter 12:03
25 would generally be suitable. 12:03

1 Q. Okay. So but you did not look specifically 12:03
2 for the operating condition for SPD in the FB-DIMM; 12:04
3 correct? 12:04
4 MR. CHANDLER: Objection. Form. 12:04
5 THE WITNESS: That's not correct. I looked 12:04
6 for buck converters that could produce 3.3 volts at 12:04
7 sufficient currents to support a -- a SP-DIMM. 12:04
8 BY MS. ZHONG:
9 Q. For FB-DIMM in general, but not for the 12:04
10 specific operating conditions for the SPD on the 12:04
11 FB-DIMM; correct? I don't see the word "SPD" 12:04
12 appearing anywhere in those paragraphs in paragraph 12:04
13 236. 12:04
14 MR. CHANDLER: Objection. Form. 12:05
15 THE WITNESS: It's not -- the words are not 12:05
16 in that paragraph. The words show up later when I 12:05
17 talk about the VSPD and refer back to those 12:05
18 paragraphs because those paragraphs explain how a 12:05
19 buck converter can be used to generate a step-down 12:05
20 voltage from 12 volts, such as a 3.3V voltage. 12:05
21 And I believe the other citation actually 12:05
22 specifically points to those ranges. And the -- 12:05
23 let's see. And then I gave examples of chips that 12:05
24 were known at the time that could supply a 3.3-volt 12:05
25 output. 12:05

1 BY MS. ZHONG: 12:05

2 Q. Okay. My question is very simple. None of 12:05

3 those are specific for SPD; correct? It's just a 12:05

4 general concept as to when buck converters can be 12:05

5 used and that there are buck converters than can 12:05

6 convert 12-volt to 3.3-volt; correct? 12:06

7 A. In those particular paragraphs. Later on, I 12:06

8 explain how those paragraphs are used to explain the 12:06

9 reasons why one would supply VSPD using a buck 12:06

10 converter. 12:06

11 Q. And it's based on the general explanation 12:06

12 that's not specific for SPD; right, when you are 12:06

13 referring back to those paragraphs? 12:06

14 A. When I refer back, yes, I refer back to a 12:06

15 general explanation because as I explained before, 12:06

16 the way that a person of ordinary skill chooses a 12:06

17 power supply or a voltage regulator is not based on 12:06

18 it being labeled for a particular use. It's based 12:06

19 on it having the appropriate characteristics to make 12:07

20 it suitable for that use. 12:07

21 Q. Okay. But you have no idea what is a 12:07

22 suitable size, current, for example, for the SPD; 12:07

23 right? 12:07

24 MR. CHANDLER: Objection. Form. 12:07

25 THE WITNESS: No. That's not true. I mean, 12:07

1 certainly, I can -- I know how big a DIMM is and I 12:07
2 know that DIMMs can vary somewhat in size, so I can 12:07
3 determine what's an appropriate size. And I have 12:07
4 looked at those exemplary chips. They are all the 12:07
5 appropriate size. I know the appropriate voltage at 12:07
6 3.3 volts. And I know just in general that an SPD 12:07
7 needs a reasonably small current. It does not need 12:07
8 amps of current, so that tells me that these 12:07
9 particular power supply units are -- buck converters 12:07
10 are suitable as well. 12:07
11 BY MS. ZHONG: 12:08
12 Q. And what's the range of the current needed 12:08
13 by the SPD? 12:08
14 A. I don't know exactly, but we looked, for 12:08
15 example, at the one part before and saw that it 12:08
16 could supply a voltage efficiently at 1 ampere; I 12:08
17 would expect an SPD to be significantly below that. 12:08
18 It also was able to supply current much less than 12:08
19 1 ampere so... 12:08
20 Q. Why do you say "significantly below 1 amp"? 12:08
21 What is significantly below 1 amp? 12:08
22 A. Let me see if I can find that graph again. 12:08
23 It seems to go down to maybe .02 amps. That's just 12:08
24 a question of how far down they measured it. I'm 12:08
25 sure it could potentially work even below that as 12:08

1 well. 12:09

2 MR. CHANDLER: Could I ask what exhibit the 12:09

3 two of you are looking at? 12:09

4 THE WITNESS: I'm looking at 1040. 12:09

5 BY MS. ZHONG: 12:09

6 Q. 1040. Which page? 23? 12:09

7 A. Yes. 12:09

8 Q. And about 0.02 amp, the efficiency is about 12:09

9 20 percent? Maybe 22? 12:09

10 A. Ballpark. It goes up -- 12:09

11 Q. Okay. 12:09

12 A. -- very quickly there. 12:09

13 Q. Okay. So if you use a linear regulator 12:09

14 that's 3.3 volts output and 12 volts input, that's 12:10

15 25 percent, 26 percent efficiency at least; right? 12:10

16 A. Not at least. At most actually. 12:10

17 Q. That's 25 percent efficiency, 3.3 divided by 12:10

18 12 volts. That's the efficiency for the LDOs; 12:10

19 right? 12:10

20 A. Yes, but there's also references -- there 12:10

21 are other current paths in the chip. So it will be 12:10

22 somewhat less than that. Probably not a lot less 12:10

23 than that. 12:10

24 Q. Okay. And it will be the same for the buck 12:10

25 converters; right? Whatever -- the 20 percent 12:10

1 that's shown here, that's for the -- that's the 12:10
2 upper limit, that's not the lower limit? 12:10
3 A. No. I believe that's typical for this 12:10
4 particular -- 12:10
5 MR. CHANDLER: Object to form. 12:10
6 THE WITNESS: -- so, yeah, that's typical 12:10
7 for this particular chip and at that particular 12:11
8 current, it could be a wash. That's a possibility 12:11
9 for this particular chip. 12:11
10 BY MS. ZHONG: 12:11
11 Q. And is it usually the case when you have a 12:11
12 very -- in the low load situation, the efficiency of 12:11
13 the buck converter drops off pretty quickly? 12:11
14 A. Yes. 12:11
15 MR. CHANDLER: Object to form. 12:11
16 THE WITNESS: But low load is different for 12:11
17 each buck converter. There would be other buck 12:11
18 converters that would be optimized for much lower 12:11
19 currents, so they would be much more efficient at 12:11
20 .02 amps. 12:11
21 BY MS. ZHONG: 12:11
22 Q. Okay. Have you cited the ones that's much 12:11
23 more efficient at the amps and milliamps range, like 12:11
24 the 20 milliamps, 30 milliamp range ones? 12:12
25 So for example, 1041, what would be 12:12

1 efficiency at the low load situation? 12:12

2 A. Well, I don't know that that's provided in 12:12

3 the specification -- 12:12

4 Q. Okay. As a designer, if the load at the 12:12

5 peak is 20 to 30 milliamp, would you use the buck 12:13

6 converter showing in Exhibit 1040, or would you just 12:13

7 use a new regulator in that case? 12:13

8 A. Either one would be obvious. 12:13

9 Q. I'm asking you as a designer, which one 12:13

10 would you choose? 12:13

11 A. I would have to consider other factors 12:13

12 including price and supply chain availability and 12:13

13 other characteristics. 12:13

14 Q. A buck converter is usually more expensive 12:13

15 than a linear LDO regulator; right? 12:13

16 MR. CHANDLER: Objection to form. And I 12:13

17 couldn't hear you. 12:13

18 THE WITNESS: Not necessarily. You know, it 12:13

19 really depends on what point in time and what 12:13

20 particular regulator and what its capabilities are. 12:14

21 BY MS. ZHONG: 12:14

22 Q. So the buck regulator in Exhibit 1040 versus 12:14

23 an LDO that drops 12 volts down to 3.3 volts? 12:14

24 A. I haven't done a comprehensive cost 12:14

25 analysis. 12:14

1 Q. Okay. Certainly, the LDO design would take 12:14
2 up less space; correct? 12:14
3 MR. CHANDLER: Objection -- 12:14
4 THE WITNESS: Not necessarily. 12:14
5 (Clarification requested by Reporter.)
6 MR. CHANDLER: Object to form. 12:14
7 BY MS. ZHONG: 12:14
8 Q. Why not? 12:14
9 A. It depends on the external components, the 12:14
10 packaging. You have to actually do the analysis. 12:14
11 Both are viable solutions and, again, since buck 12:15
12 converters, especially low current buck converters, 12:15
13 are designed for some very small battery powered 12:15
14 systems like cell phones, or even smaller things, 12:15
15 they often can be extremely small. 12:15
16 Q. The linear regulators, you don't even need 12:15
17 external components like capacitors -- like 12:15
18 inductors; right? 12:15
19 A. You don't need inductors, but you do 12:15
20 generally need capacitors and they can be just as 12:15
21 large. 12:15
22 Q. And inductors are pretty large; right? 12:15
23 A. It depends on the value of the inductor and 12:15
24 the particular situation. 12:15
25 Q. Have you ever used a buck converter with an 12:15

1 efficiency of 20 to 30 percent when you have an LDO 12:16
2 available? 12:16
3 MR. CHANDLER: Objection to form. 12:16
4 THE WITNESS: I think I probably have. 12:16
5 BY MS. ZHONG: 12:16
6 Q. When the usage is always 20 to 30 percent 12:16
7 efficiency for the buck converters in a memory 12:16
8 system? 12:16
9 A. Well, I don't think that I have an example 12:16
10 that is -- that is that narrow. 12:16
11 Q. Okay. And you certainly have not used a 12:16
12 buck converter that's with a 20 to 30 percent 12:16
13 efficiency to supply voltage for SPD; correct? 12:16
14 A. No. I have not personally designed the 12:16
15 power supply for an SPD. 12:16
16 Q. And you are not aware of any usage of a buck 12:17
17 converter that is operating at a 20 to 30 percent 12:17
18 efficiency for supplying a voltage to SPD; correct? 12:17
19 A. I can't point to one off the top of my head. 12:17
20 Q. And can you point to an example where a buck 12:17
21 converter that's operating on 20 to 30 percent 12:17
22 efficiency is used in a memory system? 12:17
23 MR. CHANDLER: Objection to form. 12:17
24 THE WITNESS: That's not an analysis I've 12:17
25 performed, no. 12:17

1 MS. ZHONG: Okay. It's 12:17 right now. Do 12:17
2 you want to take your lunch break? 12:17
3 DEPOSITION REPORTER: Why don't we go off 12:17
4 the record. 12:17
5 MS. ZHONG: Sure. 12:17
6 (Lunch recess.) 12:17
7 BY MS. ZHONG:
8 Q. Good afternoon, Dr. Wolfe. 13:02
9 You are not aware of any computer systems 13:02
10 suitable for use with FB-DIMM that provides 13:03
11 unregulated supply voltage; is that correct? 13:03
12 A. No. They all provide unregulated supply 13:03
13 voltage somewhere. 13:03
14 Q. Okay. So you are not aware of any computer 13:03
15 system suitable for use with FB-DIMMs that provide 13:03
16 unregulated supply voltages to FB-DIMM; is that 13:03
17 correct? 13:03
18 A. You are asking about computer systems that 13:03
19 are in production? 13:03
20 Q. At the time of the invention, are you -- let 13:03
21 me withdraw and ask. 13:03
22 Are you aware of any computer systems at the 13:03
23 time of the invention that are suitable for use with 13:04
24 FB-DIMM that provides unregulated supply voltages 13:04
25 for the memory systems? 13:04

1 computer systems? 13:06

2 Q. Yes. 13:06

3 A. Not off the top of my head. I haven't -- I 13:06

4 don't recall the specifications to that level of 13:06

5 detail. Lots of computer systems had 12-volt power 13:06

6 rails with some variation, but I don't recall the 13:06

7 exact specification for a particular computer from 13:06

8 that long ago. 13:06

9 Q. Is it typical for the 12-volt power rails to 13:06

10 have a plus/minus 15 percent variations in the 13:06

11 computer systems at the time of the invention? 13:07

12 A. It depends what your environment is. In an 13:07

13 automotive environment, that would have been 13:07

14 typical. In a desktop computer or a server 13:07

15 environment, the variation typically would have been 13:07

16 less, but they would have been within the plus or 13:07

17 minus 15 percent. 13:07

18 Q. FB-DIMMs are not used in automotive 13:07

19 environment as far as you know; correct? 13:07

20 A. Not as far as I know, no. 13:07

21 Q. And what is a typical variation for the 13:07

22 12-volt voltage supply in service at the time of the 13:07

23 invention? 13:08

24 A. I'm sure there's variation throughout the 13:08

25 industry. I think plus or minus 5 percent or plus 13:08

1 or minus 10 percent on a 12-volt rail would have 13:08
2 been typical, but there could have been others. 13:08
3 Q. Okay. And that -- is the answer the same 13:08
4 for a PC system? 13:08
5 A. At that time, yes. For a normal desktop PC, 13:08
6 those would be more typical variations. 13:08
7 Q. Okay. But FB-DIMMs are usually -- let me 13:08
8 put it this way. 13:08
9 FB-DIMMs are designed for use in server 13:08
10 systems; right? 13:08
11 A. I think they're primarily intended for 13:08
12 servers and high-end workstations. 13:08
13 Q. And the high-end workstations will have 13:08
14 plus/minus 5 percent variation for a 12-volt rail; 13:09
15 is that right? 13:09
16 MR. CHANDLER: Object to form. 13:09
17 THE WITNESS: Some of them could. Some of 13:09
18 them might have a different tolerance. 13:09
19 BY MS. ZHONG: 13:09
20 Q. So for a high-end workstation with a 12-volt 13:09
21 power rail, the tolerance is the 5 to 10 percent you 13:09
22 mentioned before; correct? 13:09
23 MR. CHANDLER: Objection to form. 13:09
24 THE WITNESS: That would be most common. 13:09
25 But as I said, there would be variation among 13:09

1	manufacturers.	13:09
2	BY MS. ZHONG:	13:09
3	Q. Certainly you're not aware of any server	13:09
4	systems or high-end workstations that are used with	13:10
5	FB-DIMMs with a 12-volt power rail and a plus/minus	13:10
6	15 percent voltage sway; is that correct?	13:10
7	A. I'm not specifically aware of a physical	13:10
8	system that has those exact specifications.	13:10
9	Q. And I just want to confirm that your	13:10
10	declaration does not propose any modification to the	13:10
11	host controller or memory controller in the modified	13:11
12	Harris system; correct?	13:11
13	A. It does not suggest any modifications to the	13:11
14	host computer or to the host computer memory	13:11
15	controller.	13:11
16	Q. And in the server systems and workstation	13:11
17	systems that you are aware of at the time of the	13:11
18	invention, those systems provide regulated power	13:11
19	rails to the memory systems; correct?	13:12
20	MR. CHANDLER: Object to form.	13:12
21	THE WITNESS: That's generally the case.	13:12
22	Again, I'm not -- I'm not familiar off the top of my	13:12
23	head with every system, but usually memory is	13:12
24	supplied with regulated power.	13:12
25	/ / /	13:12

1	BY MS. ZHONG:	13:12
2	Q. Can you pull up Harris Exhibit 1023 and	13:12
3	paragraph 2.	13:12
4	A. Okay.	13:12
5	Q. And do you see the sentence that says:	13:12
6	"To cope with power requirements,	13:12
7	industry standard memory modules, e.g.,	13:13
8	Dual In-line Memory Modules, populated	13:13
9	with dynamic random access memory	13:13
10	devices..."	13:13
11	Do you see that sentence?	13:13
12	A. I do.	13:13
13	Q. So this sentence states that instead of the	13:13
14	memory modules, the DIMMs are powered supply rails	13:13
15	from the host system?	13:13
16	MR. CHANDLER: Objection to form.	13:13
17	THE WITNESS: Yes, in a sense. It says that	13:13
18	they are powered from the system board or main	13:13
19	board, which would be part of the host system.	13:13
20	BY MS. ZHONG:	13:13
21	Q. Okay. And can you take a look at that	13:13
22	paragraph 11.	13:13
23	A. Okay.	13:14
24	Q. There's a sentence that says:	13:14
25	"Since the VDD and VCC power supply	13:14

1 rails are rendered independent from
2 external voltage sources..."

3 Do you see that sentence? 13:14

4 A. I do. 13:14

5 Q. What does that sentence mean? 13:14

6 A. I think it means two things. I think it 13:14
7 means that in this proposed module, rather than VDD 13:14
8 and VCC being directly drawn from the host system, 13:14
9 they are rendered on the module, on the memory 13:14
10 module from a voltage that is external to the memory 13:14
11 module, and that each of those two are done 13:14
12 independently. 13:14

13 Q. If you use a single regulator to generate 13:14
14 both VDD and VCC on the DIMM, can the two voltages 13:15
15 be rendered independent from external voltage 13:15
16 sources? 13:15

17 MR. CHANDLER: Objection. Form. 13:15

18 THE WITNESS: It would depend on the 13:15
19 characteristics of that regulator. And I think it 13:15
20 would also be somewhat semantics as to whether or 13:15
21 not you called it a single regulator. If it has two 13:16
22 outputs -- we would have to look at it, but most 13:16
23 engineers would treat it as two regulators if it had 13:16
24 two outputs at two different voltages or a dual 13:16
25 regulator, not just a simple regulator. 13:16

1 And, of course, as I said before, the most 13:17
2 straightforward approach to generating two different 13:17
3 output voltages is to use two regulators. 13:17
4 BY MS. ZHONG: 13:17
5 Q. Do you have Exhibit 2004 with you? 13:17
6 A. I can find it. I have it. I have not read 13:17
7 it. 13:17
8 Q. Would you consider a single inductor 13:17
9 multiple output regulator to be multiple buck 13:17
10 converters or a single buck converter? 13:18
11 A. I'd have to study the functionality more. 13:18
12 Q. In general, each buck converter would have a 13:18
13 corresponding inductor; correct? 13:18
14 A. In the most straightforward but -- 13:18
15 MR. CHANDLER: Objection to form. 13:18
16 THE WITNESS: In the most straightforward 13:18
17 implementation, yes, the -- each converter would be 13:18
18 distinct. 13:18
19 BY MS. ZHONG: 13:18
20 Q. Okay. And have you -- do you have 13:18
21 Exhibit 2003 [verbatim] with you? 13:18
22 A. Yeah. Unfortunately, I messed up my screen 13:18
23 a little bit. Give me a second. Again, yes, I have 13:19
24 it. I have not read it. 13:19
25 Q. Okay. So you have no opinion as to whether 13:19

1 a four-output single inducted DC-DC buck converter 13:19
2 would be regarded as a single buck converter or 13:19
3 multiple buck converters? 13:19
4 MR. CHANDLER: Object to form. 13:19
5 THE WITNESS: No. Not at this time, no. 13:19
6 BY MS. ZHONG: 13:19
7 Q. Now, assuming you're using a single inductor 13:19
8 multiple output buck converter to generate VDD and 13:19
9 VCC -- 13:19
10 A. Uh-huh. 13:19
11 Q. -- would the resulting VDD and the VCC be 13:19
12 generated independent from the external voltage 13:19
13 source? 13:20
14 A. I think it depends on the actual design of 13:20
15 the converter. 13:20
16 Q. Can you specify what you mean by that? 13:20
17 A. I don't think I can say without looking at 13:20
18 the actual circuit in its operation whether or not 13:20
19 the two voltages are being independently generated 13:20
20 or dependently generated. Again, it wasn't 13:20
21 something I had to consider because the most 13:20
22 straightforward approach in light of the teachings 13:20
23 would be to simply have two converters. 13:20
24 Q. Okay. But VDD and the VCC will be 13:20
25 independent from the external voltage source; right? 13:20

1	A.	That is what Harris teaches, yes.	13:20
2	Q.	Okay. And if you use a single conductor	13:20
3		multiple output buck converter, the locally	13:21
4		generated voltage would be independent from the	13:21
5		voltage source that's supplied to the DIMM; is	13:21
6		that correct?	13:21
7	MR. CHANDLER:	Objection. Form.	13:21
8	THE WITNESS:	Yeah. I think it depends on	13:21
9		the specific circuit, but I think that could be	13:21
10		true.	13:21
11	BY MS. ZHONG:		13:21
12	Q.	And can you take a look at paragraph 12 of	13:22
13		Harris.	13:22
14	A.	Yes.	13:22
15	Q.	What is paragraph 12 describing?	13:22
16	A.	Paragraph 12 describes the standard FBD	13:23
17		modules' power pins and the alternative of having	13:23
18		12-volt pins on Harris' module. The implication is	13:23
19		that they're the same kind of pins, but that they	13:23
20		use a different voltage and a different number	13:23
21		required, and you can calculate that number based on	13:23
22		how many memory devices you have on your DIMM.	13:23
23	Q.	Is Harris proposing to replace both the	13:23
24		power pins and the ground pins with the 12-volt	13:23
25		supply pins?	13:23

1 MR. CHANDLER: Objection. Form. 13:23

2 THE WITNESS: He's not completely clear. He 13:23

3 certainly is replacing the power pins with the 13:24

4 12-volt supply pins. I think he is suggesting that 13:24

5 there may be cases where the number of grounds can 13:24

6 be reduced, but that is not really critical to his 13:24

7 invention. 13:24

8 BY MS. ZHONG: 13:24

9 Q. So if in the modified Harris, the ground 13:24

10 pins are no longer there, would there be a ground 13:24

11 loop issue in which the FB-DIMM would have a ground 13:24

12 reference than the motherboard? 13:25

13 A. I don't think he's suggesting that the 13:25

14 ground pins are not there. He certainly talks about 13:25

15 associating ground returns. I think that a person 13:25

16 of ordinary skill might understand that one may not 13:25

17 need as many ground pins if one does not have as 13:25

18 many power pins, but certainly one would still need 13:25

19 associated ground returns. 13:25

20 Q. Would it be a problem if the FB-DIMM 13:25

21 receives 12-volt voltage supply while the memory 13:25

22 controller is receiving, say, 1.5 volt supply needed 13:25

23 to drive the signal lines? 13:26

24 A. No. No, as long as they share a ground and 13:26

25 as long as the signals are provided at the 13:26

1 appropriate voltages, the original source of power 13:26
2 is not particularly relevant. 13:26
3 Q. So they have to share -- the motherboard and 13:26
4 the DIMM have to share a common ground? 13:26
5 A. Yes, or they need to use differential 13:26
6 signaling. Different generations did it different 13:26
7 ways. 13:26
8 Q. So for FB-DIMM, would differential signaling 13:26
9 work? 13:26
10 A. The FB-DIMMs have a shared ground. 13:26
11 Q. What do you mean by "FB-DIMMs have a shared 13:27
12 ground"? 13:27
13 A. There are VSS pins, that's the ground, that 13:27
14 are connected to the motherboard ground, and there 13:27
15 are 80 of them and the memory controller would also 13:27
16 share that same ground reference. 13:27
17 Q. What about in Harris, the modified Harris? 13:27
18 A. It would still share a ground. 13:27
19 Q. How, if you replace all the ground as well? 13:27
20 A. As I said, I don't think you replace all the 13:28
21 ground. I don't think there would be any reason to 13:28
22 replace all the ground. Nobody who understands 13:28
23 electrical engineering would think that Harris says 13:28
24 you should provide power but not provide a 13:28
25 corresponding ground. 13:28

1 Q. But Harris says there are a total of 13:28
2 72 pins that provide a power supply interface for up 13:28
3 to two x4 DRAM ranks and the buffer logic; right? 13:28
4 A. Yes. 13:29
5 (Clarification requested by Reporter.)
6 MS. ZHONG: If you just look at the 13:29
7 exhibit, you should be able to find it. 13:29
8 MR. CHANDLER: It is paragraph 12? 13:29
9 MS. ZHONG: Yes. 13:29
10 BY MS. ZHONG: 13:29
11 Q. And the 72 pins include both the VDD VCC 13:29
12 pins and the ground pins; right? 13:29
13 A. Give me one second. Yes, but that's only a 13:29
14 subset of the total ground pins on the module. 13:30
15 Q. What other ground pins are there? 13:30
16 A. Well, if we look at page 11 of Exhibit 1028, 13:30
17 you can see that a standard FB-DIMM has 80 ground 13:30
18 pins to go along with 36 -- actually, 37 if you 13:30
19 include SPD, power pins. I believe that the 72 he 13:30
20 was talking to -- talking about was the 36 power 13:30
21 pins, which do include the VTT pins, and 36 of the 13:31
22 80 ground pins. But there would still be 44 13:31
23 remaining ground pins. 13:31
24 Q. So you think that when Harris is referring 13:31
25 to the VDD pins, it includes both what the FB-DIMM 13:31

1 specification calls the VTT and VDD pins? 13:32

2 A. I think so because he says there's 28 of 13:32

3 them -- 13:32

4 Q. Okay.

5 A. -- and the specification has 24 VDDs and 13:32

6 4 VTTs. 13:32

7 Q. Okay. And he shows a single outlet for -- 13:32

8 of 28 of the VDD voltage level; right? 13:32

9 MR. CHANDLER: Objection. Form. 13:32

10 THE WITNESS: No. I think he only 13:32

11 illustrates 24 of them and just hasn't illustrated 13:32

12 the other four in his drawings. 13:32

13 BY MS. ZHONG: 13:32

14 Q. He only mentions 1 VDD; right? He never 13:32

15 differentiated VDD and VTT; correct? 13:32

16 MR. CHANDLER: Objection. Form. 13:32

17 THE WITNESS: Well, he refers to the 13:32

18 standard FB-DIMM and he refers to 28 pins. That 13:32

19 includes the FTT pins -- or the VTT pins -- I'm 13:32

20 sorry, a person of ordinary skill would understand

21 that. But in his drawings, he does simplify things.

22 He draws a single VDD, a single VCC, and does not

23 actually draw the VTT. 13:33

24 BY MS. ZHONG: 13:33

25 Q. Okay. When was Harris filed? 13:33

1 A. When was Harris filed? January 31, 2005. 13:33

2 Q. And when is the specification adopted? 13:33

3 A. The version I have was adopted in 2007. 13:33

4 Q. And do you have an idea what was the 13:33

5 proposal at the time when Harris filed its 13:33

6 application for FB-DIMM, how many VDD pins there are 13:33

7 in that version? 13:33

8 A. No, I don't know all the previous versions. 13:33

9 But there is a version log in -- at the end of the 13:33

10 JEDEC document that does show that VTT pins were 13:34

11 added in a very early version, or at least some 13:34

12 additional VTT pins were added in a very early 13:34

13 version. 13:34

14 Q. Uh-huh. How many VCC pins -- VDD pins were 13:34

15 there in the early versions? 13:34

16 A. I don't know. I don't have that version. 13:34

17 Q. Okay. And do you know when each of the 13:34

18 version was adopted? 13:34

19 A. I don't have those dates in front of me. 13:34

20 But, again, I considered what a person of ordinary 13:34

21 skill would have understood at the time of the 13:34

22 filing of the patents currently being examined. 13:34

23 Q. And did you say anywhere that -- in your 13:34

24 declaration that Harris lumped the VDD and the VTT 13:34

25 pins together? 13:35

1	A. I don't recall.	13:35
2	Q. Is it that you don't recall or that you	13:35
3	never so opined?	13:35
4	MR. CHANDLER: Objection to form.	13:35
5	THE WITNESS: I don't recall.	13:35
6	BY MS. ZHONG:	13:35
7	Q. Now, SDRAMs -- DDR2 SDRAMs don't really have	13:35
8	a VTT pin; correct?	13:35
9	A. Say that again.	13:35
10	Q. DDR2 SDRAMs do not have VTT pins; correct?	13:35
11	MR. CHANDLER: Objection to form.	13:36
12	THE WITNESS: That's correct. The chip	13:36
13	itself does not have a VTT pin.	13:36
14	BY MS. ZHONG:	13:36
15	Q. Is VTT and VREF the same thing?	13:36
16	A. They don't perform the same function. It	13:36
17	may be that in some systems they are connected	13:36
18	together.	13:36
19	Q. What different functions do they perform?	13:36
20	A. VTT is for the purpose of terminating the	13:36
21	signal. VREF is used to compare the voltages from	13:37
22	the incoming signal to determine whether or not it	13:37
23	is a 0 or 1.	13:37
24	Q. Are you aware of any memory modules in which	13:37
25	VREF and VTT are supplied from the same power rail?	13:37

1 And in those dozens of -- in those dozen of 13:39
2 memory systems, are there both VTT and VREF? 13:39
3 A. I don't believe so. Not that I can recall. 13:39
4 Q. In which systems there are no VTTs? 13:39
5 MR. CHANDLER: Object to form. 13:39
6 THE WITNESS: I can't recall off the top of 13:40
7 my head. Most of them were more than 25 years ago. 13:40
8 BY MS. ZHONG: 13:40
9 Q. And back in those days, were VTTs commonly 13:40
10 used to terminate the signals for DRAMs? 13:40
11 A. On large systems they were, on smaller 13:40
12 systems they were not. 13:40
13 Q. How do you define large systems? 13:40
14 A. Again, it would be a complex analysis based 13:40
15 on simulations. But generally, it would be based 13:40
16 primarily on the length of the wires between the 13:40
17 memory controller and the memory. That would have 13:40
18 to be considered in light of the -- of the signal 13:41
19 transition speeds. 13:41
20 Q. Okay. So in the case of FB-DIMM, Harris' 13:41
21 FB-DIMM, where I believe you said the transmitting 13:41
22 device for the address command and clock signals 13:41
23 would be the un-DIMM AMB buffer; right? 13:41
24 A. With respect to the one particular statement 13:41
25 that you asked me about, yes. 13:41

1 Q. Okay. And the receiving device will be the 13:41
2 DRAM on the FB-DIMM; right? 13:41

3 A. With respect to that one particular 13:42
4 statement, that would be true. 13:42

5 Q. Okay. And for the potential wide length 13:42
6 between the transmitting device AMB and the 13:42
7 receiving device FB-DIMM, would that wide length be 13:42
8 sufficiently long that a VTT would be required? 13:42

9 A. I think in that particular case, in order to 13:42
10 be compliant with the relevant JEDEC standards, a 13:42
11 VTT is required independent of whether or not it's 13:43
12 hypothetically required. 13:43

13 Q. Well, Harris is not JEDEC compliant; 13:43
14 correct? 13:43

15 MR. CHANDLER: Object to form. 13:43

16 THE WITNESS: Harris need not be JEDEC 13:43
17 compliant, but he certainly refers us to a number of 13:43
18 JEDEC-compliant memories that he believes are 13:43
19 compatible with his system, including the FB-DIMM, 13:43
20 the standard FB-DIMM, which we know has two 13:43
21 termination networks, one on each side, both of 13:43
22 which are connected to VTT. 13:43

23 BY MS. ZHONG: 13:43

24 Q. Where does Harris say if FB-DIMM is JEDEC 13:43
25 compliant? 13:43

1 A. As a person of ordinary skill in the art, 13:43
2 when he refers to a standard FBD module and refers 13:43
3 to numerous DDR standards, I would understand that 13:44
4 to include JEDEC standard FB-DIMMs. And when he 13:44
5 gives specific numbers of pins that correspond to 13:44
6 the JEDEC FBD standard, that would reinforce that 13:44
7 understanding. 13:44
8 Q. In the standard-compliant FB-DIMM and DDR2, 13:44
9 VTT is not supplied to the DRAM; correct? 13:45
10 MR. CHANDLER: Objection. Form. 13:45
11 THE WITNESS: In that situation, it would 13:45
12 not be supplied to the DRAM chips, but would be 13:45
13 connected to a termination network that is connected 13:45
14 to DRAM pins on the DRAM chips. 13:45
15 BY MS. ZHONG: 13:45
16 Q. Which DRAM pins would those termination 13:45
17 networks be connected to? 13:45
18 A. I believe the address pins. 13:45
19 Q. Where is that stated in FB-DIMM standard or 13:45
20 the DDR2 SDRAM standard? 13:45
21 A. I believe that's shown on page 77, for 13:46
22 example. 13:47
23 Q. Of which exhibit? 13:47
24 A. Of Exhibit 1028. 13:47
25 Q. Okay. 13:47

1 A. The AMB output is connected through TLs. 13:47
2 "TL" stands for transmission line, and essentially 13:47
3 it means a wire on the printed circuit board, which 13:47
4 connect to the SDRAMs, and I believe in this 13:47
5 particular case, to the address pins, and then 13:47
6 connect through resistor R1, which is exemplary, to 13:48
7 VTT. 13:48
8 Actually, on page 74, there's a drawing 13:48
9 that's similar that is specific to address and 13:48
10 command. There are other similar drawings as well. 13:48
11 Q. Will you go to page 29 of Exhibit 1028. 13:49
12 A. Okay. 13:49
13 Q. Let me know when you are there. 13:49
14 A. I'm there. 13:49
15 Q. Okay. Do you see the heading "FB-DIMM 13:49
16 Channel Signals"? 13:49
17 A. Yes. 13:49
18 Q. Are the signals listed below that heading 13:49
19 the signals received by AMB from the memory 13:49
20 controller? 13:49
21 A. The first 10 lines are. Now, they may not 13:49
22 be coming from the memory controller. They may be 13:50
23 coming from another FB-DIMM depending on how the 13:50
24 FB-DIMM has been placed. 13:50
25 Q. So let's say this is a FB-DIMM that's 13:50

1 connected with the host system, the first in the 13:50
2 daisy chain. 13:50
3 A. Okay. 13:50
4 Q. So are those signals listed under the 13:50
5 heading the ones received from the memory 13:50
6 controller? 13:50
7 A. No. Depending on how it's connected, some 13:50
8 of them would be received from the memory controller 13:50
9 and some of them would be potentially output to the 13:50
10 next FB-DIMM. 13:50
11 Q. Okay. So which are the ones -- which 13:50
12 signals are received by AMB from the DIMM 13:51
13 connectors? 13:51
14 A. So the host of the first DIMM next to the 13:51
15 northbound out and the southbound in -- I'm sorry. 13:52
16 What page were we on for the original -- 13:52
17 Q. 29. 13:52
18 A. -- that's page 29? 13:52
19 Q. Yeah. 13:52
20 A. So I believe that the system clock input 13:52
21 would be connected. I'd have to do some more 13:52
22 looking to understand which is primary and which is 13:52
23 secondary. I believe the primary connections, the 13:52
24 next four, are the ones that would be connected to 13:52
25 the host and the secondary connections would be 13:52

Page 112

1 connected downstream. 13:53

2 Q. Okay. So assuming that you are correct that 13:53

3 the primary are the ones connected from the -- are 13:53

4 the ones received from the connectors, then the 13:53

5 information received by the AMB are the ones from 13:53

6 the system clock input, the first two lines, as well 13:53

7 as primary southbound data positive lines and 13:53

8 primary southbound data negative lines; is that 13:53

9 right? 13:53

10 A. I believe that's correct. 13:53

11 Q. And the signals that are outputted to the 13:53

12 DDR2, those are listed under the DDR2 interface 13:53

13 signals; is that right? 13:53

14 A. Yes. Although a few of the ones at the 13:53

15 bottom are not actually connected to the DDR chips. 13:54

16 Q. Okay. But the -- for example, the address, 13:54

17 the bank address, the command signals, chip select 13:54

18 and the clock, those are outputted from the AMB to 13:54

19 the DDR; correct? 13:54

20 A. On an FB-DIMM, yes. 13:54

21 Q. What is your understanding of SDRAM? 13:54

22 MR. CHANDLER: Objection. Form. 13:55

23 THE WITNESS: My understanding of SDRAM? 13:55

24 BY MS. ZHONG: 13:55

25 Q. Yeah. 13:55

1 A. It depends -- it depends on the context. 13:55
2 Generally, it refers to any synchronous dynamic 13:55
3 random access memory, but in some contexts, it can 13:55
4 be more specific. 13:55
5 Q. So generally, you would not limit it to just 13:55
6 the SDR SDRAM; is that right? 13:55
7 A. Generally, I would not. And particularly 13:55
8 with respect to these patents, I would not. These 13:55
9 patents claim SDRAM, and I think if you read them in 13:55
10 light of the specification, they clearly intended to 13:56
11 be broader than simply single data rate. 13:56
12 Q. So in the context of '918 and '054, it is 13:56
13 pretty clear to you the SDRAM is not limited to the 13:56
14 SDR, the first generation SDRAM; is that right? 13:56
15 A. I think it's clear to me. 13:56
16 Q. Okay. You think that would be clear to a 13:56
17 POSITA. 13:56
18 A. I do. It is a legal determination, but I 13:56
19 think it would be clear to a POSITA in light of the 13:56
20 specification. 13:56
21 Q. What is a portion of the DIMM connectors via 13:57
22 which the AMB receives address and control 13:57
23 information? 13:57
24 A. It would receive it from its primary 13:57
25 southbound data lines. 13:57

1 Q. And so what is a portion of the DIMM 13:57
2 connectors via which data will be received? 13:57
3 A. The same. Those lines perform both 13:57
4 functions on a F -- on a standard FB-DIMM. 13:57
5 Q. Is that also same for PCI card? 13:57
6 A. Oh, there are a bunch of different PCI 13:57
7 standards. Let me see if I can remember. 13:58
8 Q. I'm talking about the one you cited in your 13:58
9 declaration, which I believe is Exhibit 1031. 13:58
10 A. My recollection is that on PCI commands have 13:58
11 separate pins and address and data share pins. 13:58
12 Q. Okay. So is it correct then that for the 13:58
13 PCI specification you relied on, with that PCI card, 13:58
14 at least, the addresses are sent in one cycle and 13:58
15 data are sent in separate cycles over the same pins? 13:58
16 A. For -- yes, for PCI revision 2.2, that would 13:59
17 be true. 13:59
18 Q. What is your understanding of voltage 13:59
19 independent FBD design that's referenced in 13:59
20 paragraph 12 of Harris? 13:59
21 A. I think that just means a fully buffered 13:59
22 DIMM design that generates its supply voltages 13:59
23 on-board from a larger off-DIMM supply voltage. 14:00
24 Q. Why is the voltage independent? 14:00
25 A. Because it doesn't really matter whether the 14:00

1 input voltage is 10 volts or 12 volts or 15; the 14:00
2 regulators would still produce the proper operating 14:00
3 voltages. 14:00
4 Q. And is that also -- and take a look at 14:00
5 paragraph 19 with the sentence stating "...the 14:00
6 technology-independent voltage distribution scheme 14:00
7 disclosed herein..."
8 Take a look at that sentence. 14:00
9 A. Yes. 14:00
10 Q. What does it mean by 14:00
11 "technology-independent"? 14:00
12 A. I think it means that when a new DRAM 14:00
13 technology comes out, as they had historically done 14:01
14 every so many years, and used a different supply 14:01
15 voltage or a different combination of supply 14:01
16 voltages, they could be plugged into the same DIMM 14:01
17 slots because of this decoupling between the actual 14:01
18 memory voltages and the voltage supplied by the 14:01
19 slot. 14:01
20 Q. And paragraph 19 also mentions "elimination 14:01
21 of system board-specific power supply or regulator 14:01
22 output." 14:01
23 Do you see that? 14:01
24 A. I do. 14:01
25 Q. What is a system board power supply that is 14:01

1 being eliminated? 14:01

2 A. In this case, it's the supplies such as the 14:01

3 memory VDD and the memory VCC that are specific to a 14:01

4 particular generation of memory chips. Those can be 14:01

5 supplied on the DIMM rather than being supplied from 14:02

6 the motherboard. 14:02

7 Q. Okay. And paragraph 13 mentions the 14:02

8 connector keyway. What is a connector keyway? 14:02

9 A. It's just a little notch in the connector 14:02

10 that shows you that your memory module is somehow 14:02

11 different from another memory module, so that you 14:02

12 can't inadvertently plug it into the wrong machine. 14:02

13 Q. So why does it desire to make sure that the 14:02

14 modified Harris is not interchangeable with a 14:02

15 standard FB-DIMM? 14:03

16 A. Because a standard FB-DIMM doesn't supply 14:03

17 12 volts and does supply other voltages. He's 14:03

18 changed the definition of certain pins in his 14:03

19 proposal, so he wouldn't want you to plug it into a 14:03

20 motherboard that was not aware that the 14:03

21 functionality of certain pins had changed. 14:03

22 Q. And what does he mean by the "design 14:03

23 requirements for bypass/hold-up capacitors may be 14:03

24 relaxed or minimized"? 14:03

25 A. Bypass capacitors are capacitors that are 14:04

1 placed very close to a circuit, or in this case a 14:04
2 chip, to provide a reservoir of electrical charge so 14:04
3 that smaller peak currents can be pulled from the 14:04
4 original power supply. If you don't have that, you 14:04
5 can get voltage dips or other kinds of spikes in the 14:04
6 voltage. 14:04

7 Q. When --

8 A. The larger the current you're using in a -- 14:04
9 in a transient way, and the longer the distance 14:04
10 between the power supply and the chip that's 14:04
11 consuming the current, the greater the need for 14:05
12 bypass capacitors. 14:05

13 So by moving the power supply closer and 14:05
14 having a unique power supply for each DIMM rather 14:05
15 than a shared power supply for all the DIMMs, he can 14:05
16 reduce the requirement for bypass capacitors. I 14:05
17 believe holdup capacitors are essentially the same 14:05
18 thing. 14:05

19 Q. When you say bypass capacitors are 14:05
20 capacitors that are placed very close to in this 14:05
21 case a chip, which chip are you referring to? 14:05

22 A. Probably every chip on the DIMM, but most 14:05
23 importantly the DRAMs. 14:05

24 Q. Okay. So you are referring to the chips on 14:05
25 the DRAM, not to the, for example, the processes on 14:05

1 the motherboard? 14:05

2 A. They would also have bypass capacitors, but 14:05

3 their requirements would not change. It's only the 14:05

4 ones that are being supplied local power in Harris' 14:05

5 solution that would have a reduced need for bypass 14:06

6 capacitors. 14:06

7 Q. So on page 9 of Exhibit 1028, there is 14:06

8 listed a number of supply voltages. 14:07

9 Do you see that? 14:07

10 A. I do. Four supply voltages. 14:07

11 Q. And for standard FB-DIMMs, these are the 14:07

12 voltages that are provided to the DIMM by the host; 14:07

13 is that right? 14:07

14 A. For FB-DIMMs compliant with JEDEC standard 14:07

15 205, the voltages on page 9 are supplied from the 14:07

16 host to the DIMM. 14:07

17 Q. Okay. And in your combination of Harris and 14:07

18 FB-DIMM, is the combined system compliant with the 14:07

19 JEDEC standard? 14:07

20 MR. CHANDLER: Object to form. 14:07

21 THE WITNESS: No, probably not. 14:08

22 BY MS. ZHONG: 14:08

23 Q. So why would they be looking to the FB-DIMM 14:08

24 standard if they are not going to create a 14:08

25 JEDEC-compliant memory module? 14:08

1 MR. CHANDLER: Object to form. 14:08

2 THE WITNESS: One, Harris specifically tells 14:08

3 the reader that he can use a modification of the FBD 14:08

4 standard as part of his invention. 14:08

5 But further than that, the FBD standard 14:08

6 teaches how to use a buffer, it teaches details 14:08

7 about what kinds of power supplies one might need 14:08

8 for DRAM chips or for buffer chips or for 14:08

9 termination, so there -- that Harris points to that 14:08

10 standard. Harris mentions it as suitable, and then 14:09

11 there's lots of useful information there to inform a 14:09

12 person of ordinary skill who wants to design a DIMM. 14:09

13 BY MS. ZHONG: 14:09

14 Q. Would the design rules change if you changed 14:09

15 the supply voltage for the FB-DIMM? 14:09

16 A. By "design rules," you mean the thicknesses 14:09

17 and spacing of conductors? 14:09

18 Q. Among other things, yes. 14:09

19 A. I'm not sure what "other things" you mean. 14:09

20 You would have to tell me. 14:09

21 Q. The trace placement, trace routing. 14:09

22 A. Yeah, all of those things could change in 14:10

23 ordinary ways. Every time you would make changes to 14:10

24 a DIMM, there is a possibility that some of those 14:10

25 things could change and those are ordinary 14:10

1 engineering tasks to re-implement them. 14:10

2 Q. Okay. So what are they looking for exactly? 14:10

3 You said there are a lot of information in the 14:10

4 FB-DIMM standard that we'd be looking to. What 14:10

5 specifically are they looking for if all those 14:10

6 things are going to change and it's within their 14:10

7 skill set to know how to change them? 14:10

8 A. Again, I cite a number of things throughout 14:10

9 my report, throughout my declaration, so all of 14:10

10 those things are relevant. But in particular, the 14:10

11 specific voltages that one might want to use for a 14:10

12 memory. 14:10

13 Q. Uh-huh.

14 A. And also the specific characteristics of an 14:10

15 exemplary memory buffer. And the exemplary 14:11

16 characteristics of specific exemplary DRAM chips. 14:11

17 So those would be some of the things that 14:11

18 would be most important that one might learn from 14:11

19 the FB-DIMM standard, including the number of 14:11

20 voltages that are useful to use in a DIMM. 14:11

21 Q. What do you mean by "the number of 14:11

22 voltages"? 14:11

23 A. Well, we looked, for example, at the 14:11

24 specification that showed that there were four 14:11

25 important voltages on an FB-DIMM. So that would 14:11

1 inform one that if one were to generate voltages 14:12
2 from a 12-volt supply as suggested by Harris, that 14:12
3 one would want to generate perhaps 4 voltages. 14:12
4 Q. Have you ever seen a host memory controller 14:12
5 that is configured to provide 12 volts to a DIMM? 14:13
6 A. No. It would be unusual for a host memory 14:13
7 controller to supply the power to a DIMM. The power 14:13
8 supply generally does that. 14:14
9 Q. And have you ever seen a power supply that 14:14
10 is configured to provide 12 volts to a DIMM at the 14:14
11 time of the invention? 14:14
12 A. Outside of Harris? 14:14
13 Q. Correct. 14:14
14 A. I don't recall seeing that outside of 14:15
15 Harris. It doesn't mean that nobody did, but I 14:15
16 don't recall seeing it. 14:15
17 Q. And at the time of the invention, were you 14:15
18 aware that -- aware of any computer power supply 14:15
19 systems that is configured to provide 12 volts to a 14:15
20 DIMM? 14:15
21 A. I don't recall being aware of that, again, 14:15
22 other than from the Harris reference. 14:15
23 Q. So you were -- back in 2007, you were aware 14:15
24 of Harris? 14:15
25 A. No. No. 14:15

1 Q. Back in 2007, were you aware of any 14:15
2 references similar to Harris -- or systems? 14:15
3 A. There were definitely graphic cards at the 14:16
4 time that used 12-volt power from the host to supply 14:16
5 their on-board memory, their DRAM. But that -- 14:16
6 those were not main memory DIMMs. 14:16
7 Q. Okay. Would you call those graphic cards 14:16
8 memory modules? 14:16
9 A. They included memory modules, so they 14:16
10 included both a graphics processor and a graphics 14:16
11 memory. That graphics memory was accessible by the 14:16
12 host computer, and it was powered by a separate 14:16
13 12-volt power supply with a regulator on the board. 14:16
14 Q. I asked you, do you consider those graphic 14:16
15 cards memory modules? 14:16
16 A. They were modules that contained memory. 14:16
17 But when we use the term "memory modules," we 14:17
18 typically were referring to main memory modules. It 14:17
19 depends on the context. 14:17
20 Q. When you say "main memory modules," what do 14:17
21 you mean? 14:17
22 A. Memory modules that are designed to connect 14:17
23 to the primary memory controller for the purpose of 14:17
24 holding general purpose code and data in a computer 14:17
25 system. 14:17

1 Q. So, basically, memory modules would refer to 14:17
2 the RAM modules; correct? 14:17

3 A. Again, it depends on context. But I think, 14:17
4 most commonly, they would refer to -- or, you know, 14:17
5 in that time frame, they would refer typically to 14:17
6 ordinary memory DIMMs. You know, what's on the 14:17
7 graphics card is a RAM module. 14:18

8 Q. What is a "module" versus a "DRAM package"? 14:18

9 A. A module is usually a collection of 14:18
10 components. 14:18

11 MR. CHANDLER: Objection to form. 14:18

12 BY MS. ZHONG: 14:18

13 Q. So a module usually refers to more than one 14:18
14 DRAM package? 14:18

15 MR. CHANDLER: Objection. Form. 14:18

16 THE WITNESS: Again, so it's an ordinary 14:18
17 word that depends on context. But usually in the 14:18
18 electronics field, a module is a subassembly of 14:18
19 components. 14:18

20 BY MS. ZHONG: 14:18

21 Q. What do you mean by "components"? 14:18

22 MR. CHANDLER: Objection to form. 14:18

23 THE WITNESS: Again, it depends on context. 14:18
24 But a component in the most common usage probably in 14:19
25 electronics is -- again, it does depend on context, 14:19

1 but when we are talking about circuit boards, a 14:19
2 component would be a single physical package that 14:19
3 got mounted on the circuit board. 14:19
4 BY MS. ZHONG: 14:19
5 Q. Okay. So, basically, a module is usually an 14:19
6 assembly of multiple components. 14:19
7 MR. CHANDLER: Objection. Form. 14:19
8 THE WITNESS: In an electronic circuit board 14:19
9 context, that is the most common way that term is 14:19
10 used. 14:19
11 BY MS. ZHONG: 14:19
12 Q. Okay. And you said that at the time of the 14:19
13 invention, memory modules are generally understood 14:20
14 to be ones designed to connect to the primary memory 14:20
15 controller for the purpose of the holding general 14:20
16 purpose code and data in a computer system. 14:20
17 A. If we were talking about them in a general 14:20
18 purpose computer context, I think that that would be 14:20
19 the most common understanding. 14:20
20 Q. Okay. What about in the context of '918? 14:20
21 What is that understanding? 14:20
22 MR. CHANDLER: Objection. Form. 14:20
23 THE WITNESS: I think the '918 is a little 14:21
24 bit broader, that it talks about a memory module as 14:21
25 kind of being a circuit board that connects to a 14:21

1 host computer that includes memory. 14:21

2 BY MS. ZHONG: 14:21

3 Q. Where does it say that? 14:21

4 A. In the abstract. Let me see if it says it 14:21

5 anywhere else. 14:21

6 Q. Where in the abstract does it indicate the 14:22

7 use of memory module deviates from the common 14:22

8 understanding? 14:22

9 MR. CHANDLER: Objection. Form. 14:22

10 THE WITNESS: Well, it doesn't make any 14:22

11 reference there to being a main memory, so it 14:22

12 does -- at least in that description, appears to be 14:22

13 a little bit broader. Also -- 14:22

14 BY MS. ZHONG:

15 Q. Well, does it say -- okay, go ahead. 14:22

16 A. There's also -- there are also claims on a 14:22

17 memory module that, again, don't talk about its 14:22

18 functionality or what it needs to connect to. 14:22

19 Q. But doesn't that indicate it's just adopting 14:22

20 the common understanding of what a memory module is 14:22

21 so you don't need to add additional description to 14:22

22 limit it? 14:22

23 A. Well, as I said, that might be the most 14:22

24 common, but not the only understanding of a memory 14:22

25 module. Now, there is Figure 12, which shows that 14:23

1 it plugs into a standard DIMM interface, which would 14:23
2 indicate that at least that embodiment is intended 14:23
3 to be DIMM compatible. 14:23
4 Q. Okay. 14:23
5 A. Although it does also say in column 13 that 14:23
6 the DIMM form factor is only illustrative. 14:23
7 Q. Okay. So that could just mean that the 14:23
8 specific DIMM form factors are illustrated; right? 14:23
9 Just like in Harris, it had a different DIMM form 14:23
10 factor? 14:23
11 A. Yeah. It doesn't refer to a different DIMM 14:23
12 structure. It just says memory systems using other 14:23
13 form factors are contemplated as well. 14:23
14 Q. Okay. And do the claims say -- to the 14:23
15 extent you are correct that they include non-memory 14:24
16 module embodiments, do the claims say that they are 14:24
17 directed to those non-memory module embodiments? 14:24
18 MR. CHANDLER: Objection. Form. 14:24
19 THE WITNESS: I don't think I ever said that 14:24
20 there -- includes non-memory module embodiments. I 14:24
21 think what I said -- 14:24
22 BY MS. ZHONG:
23 Q. Okay.
24 A. -- is I don't think the claims are limited 14:24
25 to main memory. 14:24

1 Q. Is a SIMM a memory module? 14:25

2 A. I would generally consider a SIMM to be a 14:25

3 memory module. 14:26

4 Q. And SIMM does not adopt the non-DIMM form 14:26

5 factor; right?

6 MR. CHANDLER: Objection to form. 14:26

7 MS. ZHONG: Let me just withdraw. 14:26

8 BY MS. ZHONG: 14:26

9 Q. So SIMM, S-I-M-M, does not have the DIMM 14:26

10 form factor; correct? 14:26

11 A. I think that's correct. 14:26

12 MS. ZHONG: For Janis, S-I-M needs to have 14:26

13 two Ms, not a single M. 14:26

14 DEPOSITION REPORTER: Thank you. It was in

15 my dictionary from some other case. 14:27

16 BY MS. ZHONG: 14:27

17 Q. Can you take a look at Figure 4 of Harris. 14:27

18 A. Okay. 14:27

19 Q. Does Figure 4 show the power path or voltage 14:27

20 path? 14:27

21 A. No. I think Figure 4 is a higher level 14:27

22 block diagram. 14:27

23 Q. What is a "link 411"? 14:27

24 A. Sorry. One more time. 14:28

25 Q. What is "link 411"? 14:28

1	A. It's a memory link.	14:28
2	Q. And what is your understanding of what a	14:28
3	memory link is?	14:28
4	A. I think it's whatever connection is used	14:28
5	between the memory controller and the memory	14:28
6	modules. Harris contemplates FB-DIMMs, but he also	14:28
7	contemplates RDIMMs and UDIMMs and other kinds of	14:28
8	things.	14:28
9	Q. You don't contend that power is provided to	14:28
10	the memory modules via the memory link, do you?	14:28
11	MR. CHANDLER: Objection to form.	14:29
12	THE WITNESS: No, it is provided alongside	14:29
13	the memory link.	14:29
14	BY MS. ZHONG:	14:29
15	Q. What do you mean by "alongside"? Is it	14:29
16	shown anywhere in Figure 4?	14:29
17	A. No. It's shown in Figure 1.	14:29
18	Q. Okay. Figure 1 doesn't really show where	14:29
19	the DIMM connectors are; right?	14:29
20	MR. CHANDLER: Objection. Form.	14:29
21	THE WITNESS: Correct. It simply refers us	14:29
22	to the variety of known standards.	14:29
23	BY MS. ZHONG:	14:29
24	Q. Okay. So in Figure 1, there is no expressed	14:29
25	disclosure that the external voltage is supplied	14:30

1 through the DIMM connectors; right? 14:30

2 MR. CHANDLER: Objection. Form. 14:30

3 THE WITNESS: Well, we already talked about 14:30

4 the text that relates to Figure 1 and how it 14:30

5 describes substituting the old power pins with new 14:30

6 power pins and how a person of ordinary skill would 14:30

7 understand that those power pins would be on the 14:30

8 same connector. So that's where that disclosure 14:30

9 comes from in paragraph 12. 14:30

10 BY MS. ZHONG: 14:30

11 Q. But Figure 1 itself does not show that the 14:30

12 voltage had to be supplied through the DIMM 14:30

13 connectors; right? 14:31

14 MR. CHANDLER: Objection. Form. 14:31

15 THE WITNESS: If you read it in the context 14:31

16 of paragraph 12, which refers twice to Figure 1A, 14:31

17 then that's clear that that's what happens. 14:31

18 BY MS. ZHONG: 14:31

19 Q. And Figure 3 does not show where the power 14:31

20 supply comes from; correct? 14:31

21 MR. CHANDLER: Objection to form. 14:31

22 THE WITNESS: Figure 3 is a block diagram 14:31

23 and it does not show the power supplies. 14:31

24 BY MS. ZHONG: 14:31

25 Q. Okay. And memory controllers are usually 14:31

1 understood as not a voltage source for DIMMs; right? 14:32

2 A. Correct. Usually the memory controller does 14:32

3 not supply the voltage for DIMM. The motherboard 14:32

4 supplies the voltage for DIMM alongside the memory 14:32

5 controller signals. 14:32

6 Q. Are you aware of any memory controllers that 14:32

7 actually supply voltages to memory modules? 14:32

8 A. You mean supplied power supply voltages? 14:32

9 Q. Correct. 14:32

10 A. No, I'm not. 14:32

11 MS. ZHONG: Why don't we take a 10-minute 14:33

12 break. 14:33

13 MR. CHANDLER: Okay. 14:33

14 DEPOSITION REPORTER: We're off the record. 14:33

15 (Off the record.) 14:49

16 BY MS. ZHONG: 14:49

17 Q. For DDR2, is VDD, VDDL and VDDQ at the same 14:49

18 voltage level? 14:49

19 A. Sorry. Was the question are they at the 14:50

20 same voltage level? 14:50

21 Q. Correct. 14:50

22 A. Nominally, yes. 14:50

23 Q. What is VDDL supplied for? 14:50

24 A. It's the power voltage for the delay watt 14:50

25 loop. 14:50

1 Q. Does a separate regulator have to be 14:50
2 provided for VDD, VDDL and VDDQ? 14:51
3 A. Section 2.31 of the specification gives you 14:51
4 the option of either running them from a single 14:51
5 power output or sequencing them from multiple power 14:51
6 outputs. 14:51
7 Q. So how can this be achieved in standard 14:51
8 FB-DIMM? 14:51
9 A. How can what be achieved? 14:51
10 Q. Let me put it this way. You said it gives 14:51
11 you the option of providing from a single power or 14:51
12 separate power. 14:51
13 How can this be achieved in the standard 14:51
14 FB-DIMM? 14:51
15 A. In a standard FB-DIMM? You could have a 14:51
16 circuit that would sequence and separate the power, 14:51
17 but you don't need one in a standard FB-DIMM, but 14:51
18 you can have one. 14:52
19 Q. How do you sequence the power if it's all 14:52
20 coming from the same power supply? 14:52
21 A. You would need a circuit that connects the 14:52
22 power supply to these three different destinations 14:52
23 through switches. 14:52
24 Q. Does FB-DIMM describe such a circuit? 14:52
25 A. I don't think it -- it's silent on it. I 14:52

1 mean, it certainly refers you to the DDR2 14:52
2 specification where you would understand that that 14:52
3 was one of two options, but that's -- that's up to 14:52
4 the DIMM designer. 14:52
5 Q. As far as you know for the FB-DIMM designs, 14:52
6 which option did the designers choose? 14:52
7 A. The unmodified FB-DIMMs that I'm aware of 14:52
8 connect VDD, VDDL and VDDQ to a single power 14:53
9 converter output. 14:53
10 Q. Okay. So you're not aware of any FB-DIMMs 14:53
11 available at the time of the invention that actually 14:53
12 tie VDD, VDDL and VDDQ to three different power 14:53
13 rails; is that right? 14:53
14 MR. CHANDLER: Object to form. 14:53
15 THE WITNESS: I'm not aware of any on the 14:53
16 market. Obviously, the teaching is right here in 14:53
17 the JEDEC specification. 14:53
18 BY MS. ZHONG: 14:53
19 Q. And those designers who design the 14:53
20 commercially available FB-DIMM, they're POSITAs; 14:53
21 right? 14:53
22 MR. CHANDLER: Objection. Form. I didn't 14:53
23 hear the end of the question. 14:53
24 MS. ZHONG: Let me see what it is in the 14:54
25 transcript. 14:54

1 BY MS. ZHONG: 14:54

2 Q. And those designers who designed the 14:54

3 commercially available FB-DIMM at the time, they 14:54

4 would be POSITAs; correct? 14:54

5 A. Presumably, they would have at least 14:54

6 ordinary skill in the art at the time. 14:54

7 Q. But as far as you know, the products 14:54

8 designed by them all tied VDD, VDDL and a VDDQ to a 14:54

9 single voltage supply rail; correct? 14:54

10 MR. CHANDLER: Objection. Form. 14:54

11 THE WITNESS: No. I think it would be a 14:54

12 stretch to say that's true of all the products 14:54

13 they've designed. It is true of JESD 205-compliant 14:54

14 FB-DIMMs that I'm aware of on the market. 14:54

15 BY MS. ZHONG: 14:55

16 Q. Okay. Are you aware of any JESD 205 14:55

17 non-compliant FB-DIMMs? 14:55

18 A. I'm not even sure what that would mean. But 14:55

19 I'm certainly aware of DDR2 DIMMs that are not 14:55

20 compliant with the JESD 205 standard. Okay. 14:55

21 Q. Well, so in the DIMMs you have designed or 14:55

22 you are aware of -- let me withdraw. 14:55

23 In the DDR2 DIMMs that you're aware of, were 14:55

24 there any that [audio distortion] -- 14:55

25 (Clarification requested by Reporter.) 14:56

1 BY MS. ZHONG: 14:56

2 Q. In the DDR2 DIMMs that you are aware of at 14:56

3 the time of the invention, were there any that 14:56

4 applied a single power supply -- let me withdraw 14:56

5 that and ask. 14:56

6 In the DDR2 DIMMs that you are aware of at 14:56

7 the time of the invention, were there any that 14:56

8 applied separate power supply rails to VDD, VDDL and 14:56

9 VDDQ? 14:56

10 MR. CHANDLER: Objection. Form. 14:56

11 THE WITNESS: Of the commercial DIMMs that 14:56

12 I'm aware of at the time, I don't recall. 14:56

13 BY MS. ZHONG: 14:56

14 Q. Okay. So for the commercially available 14:56

15 FB-DIMMs you are aware of at the time of the 14:57

16 invention, did they apply separate voltage rails for 14:57

17 VCC and the VCC FBD? 14:57

18 A. I must have misunderstood the question. Can 14:57

19 I hear it again? 14:57

20 Q. So for the commercially available FB-DIMMs, 14:57

21 were you aware of any that applied separate voltage 14:57

22 supply rails for VCC and a VCC FBD? 14:57

23 A. I'm not aware one way or the other. 14:58

24 Q. Did you investigate that at all? 14:59

25 MR. CHANDLER: Objection. Form. 14:59

1 THE WITNESS: As to whether or not actual 14:59
2 modules at the time did it? No. 14:59
3 BY MS. ZHONG: 14:59
4 Q. But there are registered DIMMs; correct, at 14:59
5 the time? 14:59
6 A. Yes. Yes. 14:59
7 Q. Do registered DIMMs have -- let me withdraw. 14:59
8 So the registered DIMMs will have a buffer 14:59
9 called RCD that buffers the control and command 14:59
10 signals; correct many? 14:59
11 A. Some do. There were -- 14:59
12 MR. CHANDLER: Object to form. 14:59
13 THE WITNESS: -- there were a variety of 14:59
14 registered DIMM specifications. 14:59
15 BY MS. ZHONG: 15:00
16 Q. So for the registered -- let me withdraw and 15:00
17 ask. 15:00
18 Do all the registered DIMMs you are aware of 15:00
19 have buffers? 15:00
20 A. Yes. 15:00
21 Q. And at the time of the invention, what -- do 15:00
22 those buffers have both VCC and the VCC DIMMs as 15:00
23 well? 15:00
24 MR. CHANDLER: Objection. 15:00
25 MS. ZHONG: So let me just withdraw and ask 15:00

1 this question. 15:00

2 BY MS. ZHONG: 15:00

3 Q. VCC is the voltage supply for the core of 15:00

4 the buffer; correct? 15:00

5 A. It depends what your context is and what 15:00

6 documents you are looking at. In the context of the 15:01

7 JEDEC standard 82-20, VCC is the buffer core. But 15:01

8 VCC is used many other places in many other 15:01

9 documents to mean many other different things. 15:01

10 Q. Okay. So for a buffer on a register DIMM, 15:01

11 does it need both a supply voltage for the core as 15:01

12 well as a supply voltage for the I/O interface with 15:01

13 a memory module? 15:01

14 A. I don't recall in general. There are 15:01

15 various different designs and we'd have to look at a 15:01

16 particular specification. 15:01

17 Q. And for those with -- for those buffers that 15:01

18 have the same voltage level for the I/O interface 15:02

19 and the core, are you aware of any DIMMs that use 15:02

20 the different voltage regulators to generate those 15:02

21 voltage supplies? 15:02

22 A. I don't know one way or the other. 15:02

23 DEPOSITION REPORTER: Excuse me. What did 15:02

24 you say, Mr. Chandler? 15:02

25 MR. CHANDLER: I coughed. I coughed, 15:03

1	therefore, I am.	15:03
2	BY MS. ZHONG:	15:03
3	Q. There is only a single pin for VDDSPD on the	15:03
4	FB-DIMMs; correct?	15:03
5	A. On a JEDEC standard 205-compliant FB-DIMM,	15:03
6	that is true.	15:03
7	Q. Does that usually indicate that the	15:03
8	requirement for the component connected to VDDSPD	15:03
9	doesn't really have a very high power demand?	15:03
10	MR. CHANDLER: Objection. Form.	15:03
11	THE WITNESS: It would indicate a moderate	15:03
12	power demand in both.	15:03
13	BY MS. ZHONG:	15:03
14	Q. Okay. And you said though you don't know	15:03
15	what kind of regulator is usually used to provide	15:03
16	VDDSPD; correct?	15:03
17	A. I think it varies from system to system.	15:03
18	And, certainly, on many standard-compliant systems,	15:04
19	it would be the main power supply of the system,	15:04
20	which would be a switching supply based on a buck	15:04
21	converter.	15:04
22	Q. Have you ever designed a voltage regulator	15:04
23	for VDDSPD for memory systems?	15:04
24	A. I have never designed one, but I have seen	15:04
25	the schematics of computers that have them.	15:04

1 Q. And where is that cited in your declaration? 15:04

2 A. It's not because I don't think any of the 15:05

3 theories in my declaration are based on an 15:05

4 unmodified FB-DIMM design. 15:05

5 Q. Okay. So you say you don't think that the 15:05

6 type of voltage regulators used for the standard 15:05

7 FB-DIMM design are relevant to your analysis? 15:05

8 MR. CHANDLER: Objection. Form. 15:05

9 THE WITNESS: No, I didn't say that. But 15:05

10 what I did say is that a person of ordinary skill 15:05

11 would choose the regulator for SPD power based on 15:05

12 the same criteria one always uses to choose a 15:05

13 regulator, the amount of voltage, the amount of 15:05

14 current, size, cost, heat generation and other 15:05

15 similar factors. 15:05

16 BY MS. ZHONG: 15:05

17 Q. Okay. And you did not specify the amount of 15:05

18 current for the SPD in the FB-DIMM; correct? 15:06

19 A. That's correct. It would be the ordinary 15:06

20 amount of current. It would vary somewhat from 15:06

21 system to system. 15:06

22 Q. Okay. And you said you don't even know what 15:06

23 is the range for that ordinary amount of current; 15:06

24 correct? 15:06

25 A. Not precisely. 15:06

1 Q. Okay. Do you know what the range would be? 15:06
2 A. If by "range," you mean an upper bound and a 15:06
3 lower bound, I cannot give you those. 15:06
4 Q. And your declaration did not provide any 15:06
5 specific size for the SPD; correct? 15:06
6 MR. CHANDLER: Objection. Form. 15:06
7 THE WITNESS: The size of the SPD itself? 15:06
8 No. It would be a standard size. 15:06
9 BY MS. ZHONG: 15:07
10 Q. And your declaration did not provide the 15:07
11 cost of SPD; correct? 15:07
12 A. Correct. SPDs' cost's going to change from 15:07
13 year to year, and it is whatever it is. It's 15:07
14 present on all the DIMMs that have been discussed. 15:07
15 Q. And you did not provide any analysis on the 15:07
16 cost of buck converters versus LDOs that can be used 15:07
17 to generate the needed voltage rail; correct? 15:07
18 MR. CHANDLER: Object to form. 15:07
19 THE WITNESS: Not a specific comparison, 15:07
20 other than to say that both are available at very 15:07
21 low cost today and both would be feasible to provide 15:07
22 SPD power, and that the trend over the years has 15:07
23 been to move all computer power supplies to buck 15:07
24 converters. 15:08
25 / / / 15:08

1 BY MS. ZHONG: 15:08

2 Q. Okay. And you did not provide any analysis 15:08

3 as to the amount of heat that's going to be 15:08

4 generated for the operation of the SPD and the I2C 15:08

5 interface of the AMB buffer; correct? 15:08

6 MR. CHANDLER: Objection to form. 15:08

7 THE WITNESS: I did not quantify that. 15:08

8 BY MS. ZHONG: 15:08

9 Q. Okay. And you did not look at what a POSITA 15:08

10 actually did at the time of invention for the type 15:08

11 of regulators they actually used in connection with 15:08

12 FB-DIMM of FBDSPD power supply rail; correct? 15:08

13 A. That was not a primary factor in my 15:08

14 analysis. I looked at what was known and what was 15:08

15 obvious. 15:08

16 Q. Okay. You are familiar with PCI cards; 15:08

17 correct? 15:10

18 A. In general, yes. Not every card, but yes. 15:10

19 Q. Okay. There are no VTT pins for PCI cards; 15:10

20 correct? 15:10

21 A. There's no pin with that name, that's 15:10

22 correct. 15:10

23 Q. Is there a pin that would supply -- that 15:10

24 would function the same? 15:10

25 A. There are power pins that can be used to 15:10

1 terminate signals, but there's no dedicated VTT pin, 15:10
2 no. 15:11
3 Q. Can you tell me which pins can be used to 15:11
4 terminate the signals? 15:11
5 A. Any of the power supply pins, the 5 volt or 15:11
6 3.3 volt can be used to terminate a signal together 15:11
7 with ground. 15:11
8 Q. Would a PCI card work if you terminated 15:11
9 signals? 15:11
10 MR. CHANDLER: Objection. Form. 15:11
11 THE WITNESS: It depends which signals. 15:11
12 BY MS. ZHONG: 15:11
13 Q. Data address command signals? 15:11
14 MR. CHANDLER: Objection. Form. 15:11
15 THE WITNESS: It depends on whether those 15:12
16 data address and command signals are the ones that 15:12
17 travel over the PCI bus or whether or not they're 15:12
18 ones that operate on the card itself. 15:12
19 BY MS. ZHONG: 15:12
20 Q. So do PCI cards receive address signals? 15:12
21 A. PCI cards receive address information, but 15:12
22 there are no separate address signals. 15:12
23 Q. Okay. So do PCI cards receive control 15:12
24 information? 15:12
25 A. They do. 15:12

1 Q. Do PCI receive data signals? 15:12

2 A. They do. They share pins with address 15:12

3 signals, but they do. 15:12

4 Q. Okay. And so for those signals that's 15:12

5 received from the PCI connector pins, do they need 15:12

6 to be terminated? 15:13

7 A. Again, there are a lot of varieties of PCI, 15:13

8 but my recollection is that PCI version 2.2 bus pins 15:13

9 do not need to be terminated, at least not on the 15:13

10 card. 15:13

11 Q. Is it the case the PCI bus signaling 15:13

12 protocol requirements depends on initial signal 15:13

13 reflection? 15:14

14 A. I don't recall. 15:14

15 Q. Can you take a look at page 139 of 15:14

16 Exhibit 1031, the last paragraph on the page. 15:15

17 A. Okay. 15:15

18 Q. Does this paragraph indicate to you one way 15:15

19 or the other whether a VTT would be desirable on the 15:15

20 PCI component? 15:15

21 A. No. Because VTT need not be used in PCI 15:15

22 signaling. It may be used elsewhere on the card. 15:15

23 Q. And where else on the card would it be used? 15:15

24 A. It might be used, for example, to 15:15

25 communicate to a memory chip on the card. But 15:15

1	that's not directly connected to the PCI bus.	15:16
2	Q. Okay. So, for example, in Spiers' PCI card,	15:16
3	are you saying that a VTT would be desirable between	15:16
4	the processor and the DRAM?	15:16
5	A. In certain embodiments, it would.	15:16
6	Q. In which embodiments would it be desirable?	15:16
7	A. Ones that use DDR2 or DDR3 memory.	15:16
8	Q. Regardless of the distance between the	15:16
9	processor and the DRAMs?	15:16
10	A. Yes. I believe that those particular	15:16
11	protocols expect termination for at least some pins.	15:16
12	Q. Okay. Do VTT need it for the flash?	15:17
13	MR. CHANDLER: Objection to form.	15:17
14	THE WITNESS: I don't know. There are	15:17
15	various flash protocols, and I think it would be	15:17
16	specific to the protocol.	15:17
17	BY MS. ZHONG:	15:17
18	Q. Your declaration does not rely on a VTT for	15:17
19	terminating the signals between the processor and	15:17
20	the flash. Is that fair?	15:17
21	A. That's fair.	15:17
22	Q. Okay. If Spiers does not use DDR2 or DDR3,	15:17
23	would a POSITA still use VTT?	15:17
24	MR. CHANDLER: Objection. Form.	15:17
25	THE WITNESS: Not necessarily.	15:17

1 BY MS. ZHONG: 15:17

2 Q. What do you mean by "not necessarily"? 15:17

3 A. It would depend on what they use instead. 15:18

4 Q. Okay.

5 A. The four embodiments that I relied on all 15:18

6 use either DDR2 or DDR3. 15:18

7 Q. Okay. So if they used SDR DRAM, then I 15:18

8 understand you said that you are not aware of VTT 15:18

9 being used in connection with SDR SDRAM; correct? 15:18

10 A. Correct. I'm not aware of a separate FTT 15:18

11 voltage supply being used with single data rate 15:18

12 DRAM. 15:18

13 Q. What about if they used DDR1 DRAM, would a 15:18

14 VTT be used in that situation? 15:18

15 A. I believe so. 15:19

16 Q. Is it because JEDEC standard for the DDR1 15:19

17 required the usage of VTT? 15:19

18 A. It does in the system. I don't recall off 15:19

19 the top of my head whether or not it has to go on 15:19

20 both ends. Yes, I believe so. I believe that there 15:19

21 is a VTT that is supplied to the system. 15:20

22 Q. What would be the termination voltage for 15:20

23 the VTT -- let me withdraw and ask. 15:20

24 In Spiers, there are two voltages mentioned 15:20

25 specifically; correct? 15:20

1 MR. CHANDLER: Objection. Form. 15:20

2 THE WITNESS: In the Spiers reference? 15:20

3 BY MS. ZHONG: 15:20

4 Q. Correct. 15:20

5 A. There are more than two voltages that are 15:20

6 discussed. 15:21

7 Q. Can you point me to those voltages? 15:21

8 A. For example, in Figure 5, there's a 15:21

9 discussion -- 15:21

10 Q. Sorry. Can you just give me a second? 15:21

11 Sorry for that. 15:21

12 A. For example, in Figure 5, there's mention of 15:21

13 5 volts, 3.3 volts and 1.8 volts. 15:22

14 Q. Okay. But the 5 volts and the 3.3 volts can 15:22

15 both be supplied from the PCI connectors; correct? 15:22

16 A. Maybe they can, but there's also a regulator 15:22

17 that supplies the 3.3 volts onboard. 15:22

18 Q. And that regulator is used when the PCI 15:22

19 supply voltage is not available from the power rail; 15:22

20 correct? 15:22

21 MR. CHANDLER: Object to form. 15:22

22 THE WITNESS: Yes, I think that's where it's 15:22

23 intended to be used, or at least that's where it's 15:23

24 clearly disclosed as being used. It doesn't say 15:23

25 that that's the only time it's used, but that's 15:23

1 where it's clearly disclosed as being used. 15:23

2 BY MS. ZHONG: 15:23

3 Q. Okay. And when the voltage is not available 15:23

4 from the connectors -- let me withdraw and ask. 15:24

5 So, for example, if the 5V supply voltage is 15:24

6 not available from the PCI connector, that supply 15:24

7 voltage is not coupled to the 5V to 3.3V regulator; 15:24

8 is that right? 15:24

9 MR. CHANDLER: Objection. Form. 15:24

10 THE WITNESS: I don't recall saying that 15:24

11 it's not. 15:24

12 BY MS. ZHONG: 15:24

13 Q. So if the 5V input voltage from the 15:24

14 connector is not available, that voltage is still 15:24

15 coupled to the regulator 184? 15:24

16 A. No, if it's not available, then it's not -- 15:24

17 well, what do you mean by "coupled"? No, if it's 15:24

18 not available, it's not being used by regulator 184. 15:25

19 During a power-down situation, regulator 184 is 15:25

20 powered by the battery -- by the super caps. 15:25

21 (Clarification requested by Reporter.)

22 THE WITNESS: That is super caps, like 15:25

23 superman, but "caps." 15:25

24 MR. CHANDLER: But to be clear, you mean 15:25

25 capacitors, is that -- 15:25

1 THE WITNESS: They are capacitors. They are 15:25
2 labeled "super cap," but they are capacitors. 15:25
3 BY MS. ZHONG: 15:25
4 Q. So the regulator 184 draws its power from 15:25
5 the super capacitors 176; is that right? 15:25
6 A. We're explicitly told that is true in a 15:25
7 backup situation. 15:26
8 Q. Does it show that the regulator is connected 15:26
9 directly to the 5V or 3.3V power supply from the 15:26
10 connectors? 15:26
11 MR. CHANDLER: Objection. Form. 15:26
12 THE WITNESS: It's not part of the 15:26
13 illustration, no. 15:26
14 BY MS. ZHONG: 15:26
15 Q. Okay. So if you're a designer and the 3.3V 15:26
16 supply is available from the connector, would you 15:26
17 still be using the regulator 184 during normal 15:26
18 operation? That is when the supply voltage through 15:26
19 the connector is available? 15:27
20 A. I think it's a design choice. You have to 15:27
21 put a voltage switch in somewhere, and it would be 15:27
22 perfectly reasonable to put it either on the 5 volt 15:27
23 line or on the 3.3 volt line. 15:27
24 Q. Based on Spiers' description, where would 15:27
25 you put it as a designer? 15:27

1 A. I don't think he gives us a preference one 15:27
2 way or the other. He's not very concerned about 15:27
3 where you get normal power because it's normal. 15:27
4 He's much more concerned about how you get backup 15:27
5 power. 15:27
6 Q. And he certainly does not say that you draw 15:27
7 the power from the 184 regulator during normal 15:27
8 operation; right? There is no reference to that at 15:28
9 all? 15:28
10 A. That's not -- that's not explicit. 15:28
11 Q. And as a designer, when would you use 15:28
12 the 3.3 volt supply voltage that's provided 15:28
13 directly from the connector, and when would you 15:28
14 use a 3.3 volt coming from the regulator 184? 15:28
15 A. Again, you don't need to use the 3.3 volt 15:28
16 from the bus ever. You can use the 5 volt from the 15:28
17 bus and regulate that down to 3.3 in there, but you 15:28
18 also could use the 3.3 volt from the PCI bus when 15:28
19 the power supply is good, and use the 3.3 volts from 15:28
20 184 when the power supply fails. 15:29
21 The indication here is that you're always 15:29
22 using 184 because what's being monitored is the 15:29
23 5 volt supply, not the 3.3 volt supply, and the 15:29
24 5 volt supply feeds into 184. It would not be a 15:29
25 great idea to rely on the 3.3 volts from the bus and 15:29

1 not monitor it. 15:29

2 Q. Now, aside from the 1.8 volt at PGA core and 15:29

3 the 3.3-volt output from the regulator, does it 15:29

4 mention any other voltage supply for the components 15:29

5 on the PCI board? 15:30

6 MR. CHANDLER: Objection. Form. 15:30

7 THE WITNESS: Spiers alone doesn't, but it 15:30

8 does tell you that it uses industry standard RAM and 15:30

9 industry standard flash, so a person of ordinary 15:30

10 skill would look to what industry standard RAM and 15:30

11 industry standard flash required in terms of 15:30

12 voltages. 15:30

13 BY MS. ZHONG: 15:30

14 Q. Okay. So for example, if the industry 15:30

15 standard SDRAM is the SDR SDRAM, then you only 15:30

16 needed the 3.3 volt to power it; correct? 15:30

17 A. Yes. But, of course, by the time of the 15:30

18 invention, SDRAM was quite old and pretty 15:30

19 deprecated. 15:30

20 Q. Why would you use faster DDR2 DRAMs on 15:30

21 Spiers PCI card? 15:31

22 A. There are a number of reasons. One is that 15:31

23 by the time of the invention, PCI, especially in the 15:31

24 64-bit version that is described in Spiers, had been 15:31

25 extended up to 1,066 megahertz, so you may need it 15:31

1 just for the speed. 15:31

2 But, more importantly, DDR2 was available at 15:31

3 higher densities. Over time, it had a lower cost 15:31

4 per bit than older memories. It used less power per 15:31

5 transaction than older memories, and because by 15:31

6 2007, DDR2 and DDR3 were the mainstream memories, 15:31

7 they were much easier to obtain from multiple 15:31

8 suppliers and across the supply chain, including 15:31

9 spot markets because they had become the norm. 15:32

10 So all those reasons, including the improved 15:32

11 density, the fact that you could get much more 15:32

12 storage in a DDR2 or DDR3 than you could in an SDR 15:32

13 would all motivate you to use the newer memory. And 15:32

14 in fact, if we look across the industry, newer DRAM 15:32

15 designs are almost ubiquitously used for new 15:32

16 products. 15:32

17 Q. Okay. The PCI standard that you are relying 15:32

18 on is 33 megahertz or 66 megahertz; correct? 15:32

19 MR. CHANDLER: Object to form. 15:32

20 THE WITNESS: The exemplary one. But 15:32

21 certainly at the time, that was not the only PCI 15:32

22 standard that was out there. 15:32

23 BY MS. ZHONG: 15:32

24 Q. And you did not analyze whether the 15:32

25 limitations were met for those later PCI standards; 15:32

1 correct? 15:32

2 A. Well, the difference is speed. Speed wasn't 15:32

3 a part of the analysis, so there are many reasons to 15:33

4 update your DRAM technology independently of speed. 15:33

5 Q. Do you know whether those later PCI cards 15:33

6 even have the 5 volt supply rail? 15:33

7 A. I don't recall for certain. 15:33

8 Q. Okay. When did DDR2 become popular or 15:33

9 widely available? 15:34

10 A. Those are pretty subjective terms, but my 15:34

11 recollection is starting somewhere around 2006. 15:34

12 Q. Okay. And the Spiers was filed in 2004; 15:34

13 right? 15:34

14 A. It was. But I evaluated it from the 15:34

15 perspective of a person of ordinary skill at the 15:34

16 time of the invention of the '918 and '054 patent. 15:34

17 Q. But even the standard for the DDR2 was not 15:34

18 adopted until 2005; correct? 15:34

19 MR. CHANDLER: Objection to form. 15:34

20 THE WITNESS: Is that true? Let me... 15:34

21 BY MS. ZHONG: 15:35

22 Q. Why don't you take a look at Exhibit 1026. 15:35

23 A. It's true for 2B. I'm trying to remember 15:35

24 what 2A was. I believe 2A was also a DDR2 15:35

25 specification. It was. It was adopted in -- it was 15:35

1 published in January 2004. 15:35

2 Q. Isn't 2A DDR? 15:35

3 A. It might be. Let me see. No, I think 15:35

4 JESD 79 is -- yeah, JESD 79 is DDR. I believe 2A 15:35

5 was an earlier draft of DDR2. I don't have it in 15:35

6 front of me. 15:35

7 Q. What's the difference between 2A and 2B? 15:36

8 A. If you look at Exhibit 1026, starting at 15:36

9 page 102, all the differences are documented. They 15:36

10 are quite minor. I'm sorry. That's the middle of 15:36

11 it. It starts on page 92. 15:36

12 Q. Spiers does not describe additional 15:38

13 regulators to generate additional power rails; 15:38

14 correct? 15:38

15 A. I'm not sure what you mean by that. It does 15:38

16 generate -- it describes a 3.3 volt regulator and a 15:38

17 1.8 volt regulator to generate two different power 15:38

18 rails. 15:38

19 Q. Okay. And the 1.8 volt regulator is for the 15:38

20 FPGA core; right? 15:39

21 A. In a particular embodiment it is. 15:39

22 Q. Okay. And a POSITA would also use the 1.8 15:39

23 volts to supply the VDD, VDDQ and VDDL required for 15:39

24 DDR2 as well; right? 15:39

25 MR. CHANDLER: Objection. Form. 15:39

1 THE WITNESS: They could. I mean, again, we 15:39
2 talked about this before. It's really a simple 15:39
3 design decision as to whether or not one uses one 15:39
4 regulator or two regulators when one has two 15:39
5 different systems that require the same voltage. 15:39
6 BY MS. ZHONG: 15:39
7 Q. And so it certainly doesn't suggest having a 15:39
8 different regulator to -- let me put it this way. 15:40
9 Spiers certainly did not suggest using a 15:40
10 separate regulator for generating a voltage of the 15:40
11 same level; is that correct? 15:40
12 MR. CHANDLER: Objection. Form. 15:40
13 THE WITNESS: I don't think it explicitly 15:40
14 does. But, again, that would be an ordinary 15:40
15 engineering design decision, as I mentioned before. 15:40
16 Spiers generates the voltages that it needs 15:40
17 for the particular memory technology that the 15:40
18 designer uses, so it would be obvious to generate as 15:40
19 many voltages as your particular memory and 15:40
20 controller chips need. 15:40
21 BY MS. ZHONG: 15:40
22 Q. Okay. Spiers includes a diode before the 15:40
23 5 volt to 3.3 volt regulator; correct? 15:40
24 A. In one embodiment, yes. 15:40
25 Q. And in the Figure 5 embodiment, it relied 15:40

1 on; correct? 15:41

2 A. That is in the Figure 5 embodiment. 15:41

3 Q. Okay. What is the diode used for? 15:41

4 A. To switch the source of voltage. Again, 15:41

5 that's consistent with the idea that 184 receives 15:41

6 the 5 volts all the time, and if the super cap 15:41

7 voltage were to be higher than the 5 volt system 15:41

8 voltage, then that diode would switch on and current 15:41

9 would flow out of the super cap into regulator 184. 15:41

10 Q. Wouldn't that also be consistent of only 15:41

11 supplying the voltage from the super cap when the 15:41

12 5 volt is not available? 15:41

13 A. How would you tell the diode when to switch 15:41

14 on if it didn't have another 5 volt supply to 15:42

15 compare to? Diodes switch on when one side of the 15:42

16 voltage is higher than the other. So if there were 15:42

17 not an alternative supply of 5 volts to run 184, 15:42

18 it's not clear how you would turn the diode on. 15:42

19 Q. So are you saying that it was -- the 15:42

20 inclusion of a diode, it necessarily means that the 15:43

21 5 volt regulator -- the 5 volts to 3.3 volt 15:43

22 regulator is connected to the 5V PCI connectors 15:43

23 directly? 15:43

24 MR. CHANDLER: Object to form. 15:43

25 THE WITNESS: I don't know that it's 15:43

1 necessarily true, but it's certainly a configuration 15:43
2 that I'm familiar with and that's commonly used. 15:43
3 BY MS. ZHONG: 15:43
4 Q. So how in that case would the diode operate? 15:43
5 A. The line that you see between 180 and 184 15:43
6 would be connected to the PCI 5 volts. Depending on 15:43
7 the chemical composition of the diode, there is a 15:43
8 threshold below which 5 volts could drop, at which 15:43
9 point the diode would turn on. That threshold would 15:43
10 be somewhere between .2 and .7 volts, depending on 15:43
11 the chemical composition of the diode. 15:44
12 So typically, if the PCI 5 volts dropped 15:44
13 maybe to 4.3 or 4.4 volts, at that point, the diode 15:44
14 would allow current to flow from the super cap and 15:44
15 continue to power the 3.3 volt regulator. 15:44
16 Q. I'm asking you, say, if the regulator is not 15:44
17 connected to the 5 volt PCI connector, how would it 15:44
18 operate? 15:44
19 A. There would have to be some other switch 15:44
20 somewhere and some other bias voltage provided to 15:45
21 regulator 184, or perhaps an enabled signal on the 15:45
22 regulator. 15:45
23 Q. Why is 184 dropped from 5 volts to 3.3 volts 15:45
24 in particular? 15:45
25 A. I believe it's because 5 volts is supplied 15:45

1 on the PCI bus, which is used to power 184 and also 15:46
2 to charge the super caps. Often super caps have a 15:46
3 5.5 volt limit so that would be a good voltage to 15:46
4 use to charge the super cap, and that's why the 5 15:46
5 volts is there and the 3.3 volts is there because 15:46
6 other chips on that board require 3.3 volts. It's 15:46
7 arbitrary on the selection of chips that are in a 15:46
8 particular embodiment. 15:46
9 Q. Why isn't there any reference of a 5 volt to 15:46
10 1.8 volt regulator? 15:46
11 MR. CHANDLER: Object to form. 15:46
12 THE WITNESS: Well, there is a 1.8 volt 15:46
13 regulator. I don't think it's really important as 15:46
14 to whether or not it starts with 5 volts or 3.3, so 15:46
15 maybe that's why it's just not discussed. 15:46
16 What's the -- let me look at the part number 15:47
17 there. 15:47
18 BY MS. ZHONG: 15:47
19 Q. What do you mean? What is a particular part 15:47
20 number there? 15:47
21 A. I meant 206. It just says that it's the 15:47
22 regulator that is used to provide power to the FPGA 15:47
23 core. Again, it's ordinary. 15:47
24 Q. Do you need additional regulators if you are 15:47
25 using SDRAMs -- SDR SDRAMs? 15:47

1 MR. CHANDLER: Objection. Form. 15:48

2 THE WITNESS: If you were using SDR SDRAMs, 15:48

3 then you could power them from 3.3 volts. You would 15:48

4 have to look at all the other chips on the board. 15:48

5 Again, just like any design, the person of ordinary 15:48

6 skill would know that they have to provide whatever 15:48

7 voltages the chips require. 15:48

8 BY MS. ZHONG: 15:48

9 Q. Okay. So if you are using SDR SDRAMs, then 15:48

10 1.8 volts and 3.3 volts should be sufficient to 15:48

11 power the NAND, the SDRAM and the processor; right? 15:48

12 A. It depends on your choice of NAND and your 15:48

13 choice of ADC and your choice of EEPROM. You know, 15:48

14 it is just a standard design problem. You just look 15:48

15 at all the chips on your board and you figure out 15:48

16 what voltages they need, and you provide the power 15:48

17 supplies for those voltages. 15:48

18 Q. What is the voltage supply for the NAND that 15:48

19 you relied on in your declaration? 15:49

20 A. I did not rely on it because I relied on 15:49

21 DDR2 and DDR3 embodiments. Oh, no, I'm sorry, in 15:49

22 some -- in one of my mappings, I used 3.3 volts for 15:49

23 the nonvolatile memory. 15:49

24 Q. Okay. Why don't you look at page 300, the 15:49

25 declaration for Spiers. 15:50

1 MR. CHANDLER: I'm sorry. What exhibit? 15:50
2 MS. ZHONG: Exhibit 1003. 15:50
3 MR. CHANDLER: For the '918. 15:50
4 BY MS. ZHONG: 15:50
5 Q. Isn't it the case that for each of your 15:50
6 mapping, you relied on a 3.3 volt supply voltage to 15:50
7 the NV memory? 15:50
8 A. Yes, but for two of the mappings, it's 15:50
9 redundant because it's also required for the FPGA 15:50
10 I/O. 15:51
11 Q. And isn't the reason that it is required 15:51
12 for the FPGA I/O is because the voltage for the NV 15:51
13 memory is 3.3 volts? 15:51
14 A. No. It's also so that they can talk on the 15:51
15 PCI bus. 15:51
16 Q. So if you used DDR2 or DDR3, you would need 15:51
17 more than two voltages for this PCI board; correct? 15:51
18 A. You would need more than two power supplies. 15:52
19 In voltage mappings, there is only two different 15:52
20 voltages, but [audio distortion] --
21 DEPOSITION REPORTER: Excuse me. I need
22 that answer. There was a feedback. 15:52
23 (Clarification requested by Reporter.) 15:52
24 THE WITNESS: You would need more than two 15:52
25 power supplies for my first and second mapping, but 15:52

1 for the third mapping, you would only need two 15:52
2 different voltages, but it would be obvious to use 15:52
3 four power supplies. 15:52
4 BY MS. ZHONG: 15:52
5 Q. Okay. What I'm saying is that if you use 15:52
6 SDR SDRAM, all you need are two voltage levels; 15:52
7 correct? 15:52
8 MR. CHANDLER: Objection. Form. 15:52
9 THE WITNESS: That would depend on the other 15:52
10 chips you select for the board. 15:52
11 BY MS. ZHONG: 15:52
12 Q. Based on your assumption, using the same 15:53
13 assumption you applied here. 15:53
14 MR. CHANDLER: Objection. Form. 15:53
15 THE WITNESS: Yeah. I haven't made any 15:53
16 assumptions about SDR, but hypothetically, one could 15:53
17 have an SDR-based design that only required two 15:53
18 different voltage levels. 15:53
19 BY MS. ZHONG: 15:53
20 Q. The SDR supplied 3.3 volts and the NV memory 15:53
21 is also 3.3 volts; correct? 15:53
22 A. That kind of embodiment could exist. 15:53
23 Q. Okay. And that's your -- actually, your 15:53
24 assumption is the NV memory would be operating on 15:53
25 3.3 volts, the FPGA I/O would be operating on 3.3 15:53

1 volts, the FPGA core would be operating at 1.8 15:53
2 volts; correct? 15:53
3 A. In the particular embodiments that I 15:53
4 discussed in my declaration, that's true. There 15:54
5 would be other embodiments where some of those 15:54
6 components could use different voltages. 15:54
7 Q. Okay. And for SDR DRAMs, you also don't 15:54
8 need a VTT; right? 15:54
9 A. You do not need a VTT for an SDR DRAM. 15:54
10 Q. Okay. So the usage of SDR DRAM would be 15:54
11 consistent with what is shown in Figure 5; correct? 15:54
12 A. You could have an embodiment that used SDR 15:54
13 DRAM that was consistent with Figure 5, but that's 15:54
14 not the only embodiment that a person of ordinary 15:54
15 skill would understand from reading the Spiers 15:54
16 reference. 15:54
17 Q. Okay. The only embodiment -- let me 15:54
18 withdraw and ask this question. 15:55
19 If you used DDR2 and DDR3, you will 15:55
20 definitely need a voltage supply other than 1.8 15:55
21 volts and 3.3 volts, fair, according to you? 15:55
22 A. No. It's actually possible to do DDR2 with 15:55
23 1.8 volts and 3.3 volts, but you would preferably 15:55
24 have multiple supplies. 15:55
25 Q. So if you used DDR2, you don't need a VTT; 15:55

1 right? 15:55

2 A. Well, actually, I do believe -- I think you 15:55

3 need VTT. 15:55

4 Q. Okay. So you need at least three voltage 15:55

5 levels for DDR2? 15:55

6 A. For a complete system, yes. I haven't 15:55

7 looked at them all in my analysis, but you would 15:56

8 need a VTT voltage. 15:56

9 Q. Okay. That is what I'm saying. If you use 15:56

10 DDR2, then you would need more than a 1.8-volt and a 15:56

11 3.3 volt that is illustrated expressly in Figure 5; 15:56

12 correct? 15:56

13 A. Correct. 15:56

14 Q. The same with DDR3; correct? 15:56

15 A. For DDR3, you would need 1.5 and also 0.75. 15:56

16 Q. Okay. And Spiers only expressly mentioned 15:56

17 3.3 volt and a 1.8-volt as the output of the 15:56

18 regulators; right? 15:56

19 MR. CHANDLER: Objection. Form. 15:56

20 THE WITNESS: In an exemplary embodiment, 15:57

21 those are the numbers that he uses. 15:57

22 BY MS. ZHONG: 15:57

23 Q. Okay. And that's the only exemplary 15:57

24 embodiment that's provided in Spiers; right? 15:57

25 Figure 5? 15:57

1	MR. CHANDLER: Objection. Form.	15:57
2	THE WITNESS: Those are the only exemplary	15:57
3	voltages. But, again, a person of ordinary skill	15:57
4	would understand that there is nothing in Spiers	15:57
5	that limits anyone in any way to those particular	15:57
6	voltages and would be motivated to use a	15:57
7	contemporaneous SDRAM technology.	15:57
8	BY MS. ZHONG:	15:57
9	Q. Have you ever designed write-back caches?	15:58
10	A. Yes.	15:58
11	Q. What are write-back caches?	15:58
12	A. Where are they?	15:58
13	Q. What are they?	15:58
14	A. Oh, what are they?	15:58
15	Q. Uh-huh.	15:58
16	A. A cache is a memory that's used for	15:58
17	temporary storage. A write-back cache is a cache	15:58
18	that when data is written to it, it doesn't	15:58
19	immediately write it back to the main memory, but	15:58
20	can defer the write-back of data to main memory	15:58
21	until the space in the cache is needed for something	15:58
22	else.	15:58
23	Write-back caches are used in	15:58
24	microprocessors, but they are also used in	15:59
25	other portions of a computer system as well.	15:59

1 Q. How does Spiers' write-back cache operate? 15:59

2 A. Spiers uses his volatile memory as a type of 15:59

3 a write-back cache, not what we would normally call 15:59

4 a write-back cache, but something quite similar. 15:59

5 What Spiers does is he writes data to the 15:59

6 volatile memory and keeps it there until the space 16:00

7 in the write-back memory is needed for different 16:00

8 data, at which point he may write it to the 16:00

9 nonvolatile memory, but that's not the primary 16:00

10 discussion in Spiers. 16:00

11 The primary discussion in Spiers is that he 16:00

12 keeps data in the volatile memory until the power 16:00

13 becomes unreliable, at which point he writes it more 16:00

14 permanently into the nonvolatile memory. 16:00

15 Q. What is the data transfer rate for the PCI 16:00

16 interface that you rely on? 16:01

17 A. Well, I only give an example. But the 16:01

18 exemplary PCI data rate -- let me check. Is up 16:01

19 to -- let me do a little bit of math. Up to 528 16:01

20 megabytes per second, I believe. 16:02

21 Q. And that's 66 times 8? 16:02

22 A. Yes. 66 million times 8. 16:02

23 Q. Okay. And what is the data transfer rate 16:02

24 for SDR DRAM? 16:02

25 A. I guess it depends which one and how wide. 16:02

1 You can also find that 528 number on page 4 of 16:02
2 Exhibit 1031. 16:02
3 Q. Okay. So for SDR DRAM, what are the data 16:02
4 transfer rates at the time? 16:02
5 A. I don't have the specification. I remember 16:02
6 up until like 133 megahertz, but I don't remember if 16:02
7 it got faster than that, and again, it depends on 16:02
8 how wide. 16:02
9 Q. And what is the data transfer rate for NAND 16:02
10 flash? 16:03
11 A. It varies from component to component. 16:03
12 Q. At the time, is it much slower than the 16:03
13 SDRAMs? 16:03
14 A. It would depend on what component you 16:03
15 selected. The throughput is lower, but the peak 16:03
16 rate may have been similar. Again, it depends on 16:03
17 how wide you make it. 16:03
18 Q. You cited NAND data sheets in your 16:03
19 declaration; right? 16:03
20 A. I did. 16:03
21 Q. And what is the data transfer rate for that 16:03
22 one? 16:03
23 A. I think a single chip is about 80 megabytes 16:03
24 per second, but again, you can have multiple chips 16:04
25 being used which would just multiply that out. 16:04

1 Q. Okay. And you mentioned that the SDR DRAM 16:05
2 at the time can be up to 133 megahertz. Is that the 16:05
3 number of transfers? So like when you computed the 16:05
4 data transfer rate, you need to time -- multiply 16:05
5 that number by 8? 16:05
6 A. It depends on how you configure it. It 16:05
7 could be less than 8, it could be more than 8, it 16:05
8 could be 8. It's a design choice. 16:05
9 Q. So in the PCI example, when it's used for 16:05
10 the write-back cache similar to the Spiers 16:05
11 application? 16:05
12 A. I don't think Spiers is specific to exactly 16:05
13 how many chips of what type one would use. 16:05
14 Q. I'm just talking about a single SDR DRAM. 16:05
15 A. Again, there are various kinds. There were, 16:06
16 if I recall correctly, 8-, 16- and 32-bit versions, 16:06
17 but there's nothing that suggests that one would 16:06
18 only use a single SDRAM chip in Spiers. 16:06
19 Q. Okay. So if it's a 133 megahertz one with, 16:06
20 you said, 8 bits or 16 bits -- 16:06
21 A. Uh-huh. 16:06
22 Q. -- okay so that would be 133 times 8 or 133 16:06
23 times 16 a chip; right? 16:06
24 A. No, that's bits. I have been measuring 16:06
25 everything else in bytes. If it were an 8-bit-wide 16:06

1 chip, it would peak out at 133 megabytes. If it 16:06
2 were a 4-bit chip, it would be half that. 16:07
3 Q. So for the PCI interface, when you said 512, 16:07
4 is that a megabits or megabytes? 16:07
5 A. 528 megabytes per second, if I got that 16:07
6 correct. Yes, that's correct. Peak. 16:07
7 Some of the SDR chips were as little as 16:08
8 66 megabytes per second peak per chip. Some of them 16:08
9 even slower than that; some of them half that. 16:09
10 So in a four-chip configuration such as 16:09
11 Spiers, there would definitely be a bandwidth 16:09
12 motivation to use a faster memory. 16:09
13 Q. So why don't you take a look at Exhibit 2012 16:10
14 [verbatim], and PDF page No. 2. 16:10
15 A. Okay. 16:10
16 Q. Do you disagree with the maximum transfer 16:10
17 rate that's listed in Table 1 there? 16:10
18 A. That's based on some assumption as to how 16:10
19 many bytes wide the system is. That assumption is 16:11
20 not necessarily present in Spiers. That's not true 16:11
21 for a single chip. 16:11
22 Q. Where does it indicate that it's not for 16:11
23 single chip? 16:11
24 A. You can just do the math. So some PC100 16:11
25 SDRAM chips, for example, use a 4-bit-wide 16:11

1 configuration. That means that 100 million times 16:11
2 per second, they can send half a byte. In that 16:12
3 case, they can only manage 50 megabytes per second. 16:12
4 So it would take 16 of those chips lined up to get 16:12
5 to 800 megabytes per second. Of course, you can 16:12
6 line up more or less and get to whatever number you 16:12
7 want. 16:12

8 Q. You are saying that the Table 1 transfer 16:12
9 rate is assuming there is a certain number of DRAMs? 16:12

10 A. Operating simultaneously, correct. And 16:13
11 again, in the case of PC100 or PC133, that may be as 16:13
12 many as 16 simultaneously operating DRAM chips. 16:13

13 Q. Why is it uniformly basically the number in 16:13
14 the real clock and the maximum transfer rate, it's 16:13
15 all times 8? Do you see that? 16:13

16 A. They've made some assumptions. Those 16:13
17 assumptions don't seem to be -- let's see. They've 16:13
18 made the assumption that they've physically built a 16:13
19 memory system that is 8-bytes wide. That's an 16:13
20 assumption for this document, but it's certainly not 16:13
21 an assumption that's true for every memory system 16:13
22 design. 16:14

23 Q. Where does it say the assumption is an 16:14
24 8-byte-wide memory system? 16:14

25 A. Well, again, we can derive that just from 16:14

1 the numbers. But it also, when it talks about types 16:14
2 of DDR memory, it keeps mentioning 8 bytes. 16:14
3 Q. Where? 16:14
4 A. Under subsection 1 and under subsection 2. 16:14
5 Q. When you say subsection 1, where is it? 16:14
6 Which section are you referring to? 16:14
7 A. On page 71. 16:14
8 Q. Page 71. Okay. 16:14
9 A. Types of DDR memories. There are presently 16:14
10 three generations of DDR memories; DDR1 memory with 16:14
11 a maximum rated clock of 400 megahertz and a 64-bit 16:15
12 8-bytes data bus is now becoming obsolete, which I 16:15
13 don't know what the date is on this document, but 16:15
14 even by here, you can see it's already become 16:15
15 obsolete. 16:15
16 But, again, you can make those numbers 16:15
17 whatever you want. If you assume, it is 100 bytes 16:15
18 wide, it will be 100 times the rated clock. And if 16:15
19 you assume it is a half-a-byte wide, like many 16:16
20 common PC133 chips, then it's half the rated clock. 16:16
21 Q. For the Spiers operating -- let me withdraw 16:16
22 and ask. 16:16
23 So for the Spiers application, does that 16:16
24 involve an operating environment that has a high 16:16
25 write-to-read ratio? 16:16

1 A. It might. Spiers isn't specific to any 16:16
2 write-to-read ratio. 16:16
3 Q. And I'm just saying for Spiers' specific 16:16
4 application, the write cache -- write-back cache 16:17
5 application, does that involve a high write-to-read 16:17
6 ratio? 16:17
7 MR. CHANDLER: Objection. Form. 16:17
8 THE WITNESS: It just depends how you choose 16:17
9 to use it. It's memory -- you can write to it or 16:17
10 you can read from it. 16:17
11 BY MS. ZHONG: 16:17
12 Q. How does Spiers, according to Spiers, 16:17
13 disclose embodiments when is a write operation done 16:17
14 to the DRAM and when is read operation done? 16:17
15 A. I believe that a write -- I mean, there are 16:17
16 multiple cases. But a write operation is done when 16:17
17 the host writes data, and a read operation is done 16:17
18 when the host reads data. And then there are other 16:17
19 times as well, but those would be certainly 16:17
20 dominant. 16:17
21 Q. When does a host read data from Spiers' 16:18
22 DRAM? 16:18
23 A. When it wants to know the data that it's 16:18
24 previously written. 16:18
25 Q. Isn't it the case that a data stored in the 16:18

1	SDRAM is written to the disk?	16:18
2	A. Eventually. But since it's a write-back	16:18
3	cache, that write-back to the -- you know, I	16:18
4	wouldn't call it the disk -- the nonvolatile	16:18
5	storage, is deferred as long as possible.	16:18
6	Q. According to Spiers, when are the SDRAM's	16:19
7	data being read?	16:21
8	A. There are lots of different times when the	16:21
9	SD data can be read. It's a cache, so whenever it	16:21
10	contains the data that the host wants, it should be	16:21
11	read. There are other times as well.	16:21
12	Q. Isn't the case in Spiers the data is written	16:21
13	to the DRAM just to speed up the disk-write timing?	16:21
14	A. That's one reason, but it's described as a	16:21
15	write-back cache. So reading from the disk drive	16:21
16	also takes a long time. Normally in a write-back	16:21
17	cache, if the data is in the cache, you would read	16:22
18	from the cache.	16:22
19	Q. So what would be the read-to-write ratio in	16:22
20	Spiers' operation then?	16:23
21	A. I think it depends on the particular	16:23
22	software that you run on the host. I think it would	16:23
23	vary.	16:23
24	Q. Do you know the range?	16:23
25	A. No. I'm not sure that it's even bound.	16:23

1 DEPOSITION REPORTER: Miss Zhong, is this a 16:24
2 good time to take another break, a few minutes? 16:24
3 MS. ZHONG: Sure, we can take our break. 16:24
4 (Off the record.) 16:24
5 BY MS. ZHONG: 16:40
6 Q. For Spiers -- can you pull up Spiers 16:40
7 paragraph 37. 16:40
8 A. Okay. 16:40
9 Q. Do you see it references SDRAM modules 190? 16:40
10 A. Yes. 16:40
11 Q. So do those refer to individual DRAM 16:40
12 packages, or they're referring to a memory module 16:40
13 with multiple SDRAMs on them? 16:40
14 MR. CHANDLER: Objection. Form. 16:40
15 THE WITNESS: In that embodiment, they could 16:40
16 be memory -- they could be multiple SDRAMs on board. 16:40
17 BY MS. ZHONG: 16:41
18 Q. And to you, when they say "SDRAM modules," 16:41
19 what does it usually mean to a POSITA? 16:41
20 A. It probably at that time means a DIMM or 16:41
21 something like it. 16:41
22 Q. Okay. So it means there are four DIMMs on 16:41
23 the PCI? 16:41
24 A. Not on the PCI. Connected to the 16:41
25 controller. 16:41

1 Q. Well, it says, "SDRAM modules 190" and 16:41
2 that's in Figure 5, and that's on the PCI card. 16:41
3 A. It's on the PCI card, but it's not on the 16:41
4 PCI bus. It's connected to the processor 198. 16:41
5 Q. Okay. 16:42
6 A. The processor 198 has internal local memory. 16:42
7 We're taught that. It reads data and then 16:42
8 separately writes it. So there are two transfers 16:42
9 that happen. It gets transferred into processor 16:42
10 198, and then to the SDRAM, or from the SDRAM to 16:42
11 processor 198 and then to the PCI bus. 16:42
12 Q. That I understand, but you said the 190 are 16:42
13 DIMMs? 16:42
14 A. It could be, or SO-DIMMs or any other kind 16:42
15 of a memory module. 16:42
16 Q. But don't DIMMs require there to be memory 16:42
17 slots in order for them to fit in? 16:42
18 A. There could be slots on the board. 16:42
19 Q. Okay. So you're saying that it's possible 16:42
20 on the PCI card itself, there are memory slots for 16:42
21 you to insert the SDRAM memory modules? 16:42
22 A. That's certainly possible. 16:42
23 Q. And at the time, usually how many DRAMs are 16:43
24 there on the DIMM module? 16:43
25 MR. CHANDLER: Objection to form. 16:43

1 THE WITNESS: Well, it varies a lot. 16:43
2 Probably anywhere from 2 to 16 -- 16:43
3 BY MS. ZHONG:
4 Q. 2 to 16?
5 A. -- on a traditional module. But there are 16:43
6 all kinds of specialty modules as well. 16:43
7 Q. Are you aware of any SDR that's by 4? 16:43
8 A. That's my recollection. 16:43
9 DEPOSITION REPORTER: What was the last 16:43
10 word?
11 MS. ZHONG: That's by 4. You can just say 16:43
12 X4. 16:43
13 DEPOSITION REPORTER: What was your answer?
14 I apologize. 16:43
15 THE WITNESS: My recollection is that SDR 16:43
16 came in X4, X8 and X16. 16:43
17 BY MS. ZHONG: 16:44
18 Q. And if you can take a look at Exhibit 2013. 16:44
19 Does that describe a 64-bit-wide SO-DIMM 16:44
20 comprised of FDRs? 16:44
21 A. Yes. 16:45
22 Q. Okay. So for that one, the calculation that 16:45
23 we saw before regarding the data transfer rate is 16:45
24 correct; right? 16:45
25 MR. CHANDLER: Objection. Form. 16:45

1 THE WITNESS: Correct. For these -- for 16:45
2 this particular module, if this particular module 16:45
3 had been used, a person of ordinary skill in the art 16:45
4 would certainly know how to change the width of a 16:45
5 memory system. 16:45
6 BY MS. ZHONG: 16:45
7 Q. Okay. So if the PCI memory width is 64, 16:45
8 does that indicate the SDRAM DIMMs would also be 64? 16:45
9 MR. CHANDLER: Object to form. 16:46
10 THE WITNESS: Not necessarily because there 16:46
11 is a controller in between. It could change the 16:46
12 width to make it wider or narrower. It could -- if 16:46
13 it had enough bandwidth, it could use a X8, which 16:46
14 would save a lot of money for the DRAM connection. 16:46
15 BY MS. ZHONG: 16:46
16 Q. Do you see that between the processor and 16:46
17 the SDRAM it says "64"? 16:46
18 A. In Figure 5, yes, that's the example that's 16:46
19 given. 16:46
20 Q. So that means it's 64 bits is transferred 16:46
21 from the SDRAM to the processor? 16:46
22 A. In this particular embodiment in Figure 5, 16:46
23 that's correct. 16:46
24 Q. Okay. So for that one, it's the -- each of 16:46
25 the SDRAM module would be 64-bit wide; is that 16:46

1 right? 16:46

2 A. Not necessarily. It could be four 16:46

3 16-bit-wide modules. They don't tell us. It 16:46

4 doesn't matter. A person of ordinary skill would 16:46

5 know how to implement any combination of DRAM 16:47

6 widths. 16:47

7 I should mention there is also DRAM 218 that 16:47

8 has some additional bits. It's not actually a 16:47

9 64-bit transfer. There are some additional error 16:47

10 correction bits as well. 16:47

11 Q. Okay. But the transfer between the 16:47

12 processor and the SDRAM 190, that's 64 bit; right? 16:47

13 MR. CHANDLER: Objection. Form. 16:47

14 THE WITNESS: In this embodiment, yes. 16:47

15 BY MS. ZHONG: 16:47

16 Q. Do you regard a PCI card with memory modules 16:47

17 on them a memory module? 16:48

18 A. It would depend on context. Certainly, 16:48

19 there were times in the history of PCs where an I/O 16:48

20 card with memory chips on it was called a memory 16:48

21 module. 16:48

22 By the beginning of 2007, I think absent any 16:48

23 other context, memory module probably refers to 16:48

24 something that's designed to fit into a 16:48

25 memory-specific slot. 16:48

1 Q. Okay. So, for example, in Figure 5, you 16:48
2 would probably refer to the SDRAM modules as memory 16:48
3 modules but not necessarily the entire PCI card; is 16:48
4 that right? 16:48
5 MR. CHANDLER: Objection. Form. 16:48
6 THE WITNESS: Again, it would depend on 16:48
7 context. So I've heard people refer to a PCI memory 16:49
8 card as a memory module, but in some contexts, you 16:49
9 would not assume that if someone said memory module 16:49
10 that that was a PCI card. 16:49
11 BY MS. ZHONG: 16:49
12 Q. Okay. So in the context of Spiers, would 16:49
13 you regard the PCI card with memory modules a memory 16:49
14 module? 16:49
15 A. Under the general understanding of a memory 16:49
16 module, I think probably, right, because it's a card 16:49
17 that contains memory. 16:49
18 Q. But it's not used with memory-specific slot; 16:49
19 right? 16:49
20 MR. CHANDLER: Objection to form. 16:49
21 THE WITNESS: It's not used with memory 16:49
22 specific -- it doesn't fit into a memory specific 16:49
23 slot, that's true. 16:50
24 BY MS. ZHONG: 16:50
25 Q. Okay. So by 2007 or so, a PCI card probably 16:50

1 would not be regarded in general as a memory module; 16:50
2 correct? 16:50
3 MR. CHANDLER: Objection. Form. 16:50
4 THE WITNESS: No. Like I said, it's 16:50
5 depending on context. If it's a PCI card that's 16:50
6 used to host memory, it would be reasonable to call 16:50
7 it a memory module. It's just not the most common 16:50
8 kind of memory module. 16:50
9 BY MS. ZHONG: 16:50
10 Q. Sure. Is a PCI card designed to fit into a 16:50
11 memory specific slot? 16:51
12 MR. CHANDLER: Object to form. 16:51
13 THE WITNESS: No. A PCI slot is useful for 16:51
14 input, output or memory. This particular card would 16:51
15 be memory. 16:51
16 BY MS. ZHONG: 16:51
17 Q. Why? 16:51
18 A. Why would this card be memory? Because its 16:52
19 purpose is to hold memories. If you look at the 16:52
20 intended use of the PCI bus in the spec, it says 16:52
21 it's used for peripheral controllers, add-in boards 16:52
22 and processor memory systems. 16:52
23 Q. Where are you reading from? 16:52
24 A. Page 1 of Exhibit 1031. 16:52
25 Q. So according to you then, the PCI card would 16:52

1 always be a memory card, wouldn't it? 16:54

2 A. No. PCI cards that are intended to provide 16:54

3 memory are memory modules, and PCI cards that are 16:54

4 intended to provide peripheral input/output are I/O 16:54

5 modules. 16:54

6 Q. So you're saying the PCI card in Spiers is a 16:54

7 memory module having memory modules on them? 16:55

8 A. Yes. And, again, a module is just a 16:55

9 collection of components. 16:55

10 Q. So would the FPGA on the PCI card operating 16:55

11 as a processor in the same manner as that for a 16:56

12 memory controller? 16:56

13 MR. CHANDLER: Objection. Form. 16:56

14 THE WITNESS: Processor 198 in Figure 5 16:56

15 would incorporate a memory controller as well as 16:56

16 other things. 16:56

17 BY MS. ZHONG: 16:57

18 Q. Then if the DDR2 are on the DIMM modules, 16:57

19 then the VTT is not supplied on the PCI card, is it? 16:57

20 MR. CHANDLER: Objection to form. 16:58

21 THE WITNESS: I'm not sure I understand the 16:58

22 question. The DDR2 does not have to be in an 16:58

23 industry standard module, so the VTT could certainly 16:58

24 come from the PCI card. And in the embodiments I 16:58

25 described, it would come from a buck regulator on 16:58

1 the PCI card. 16:58

2 There's also an example in Figure 5 uses 16:58

3 SDRAM modules, there's -- certainly a person of 16:58

4 ordinary skill would understand that they could also 16:58

5 build Spiers' invention by putting SDRAM chips 16:58

6 directly on the PCI board. 16:58

7 BY MS. ZHONG:

8 Q. Yeah. But you don't have 64-bit wide 16:58

9 SD DDR2 SDRAMs, do you? 16:58

10 A. Well, one, you could combine them just like 16:58

11 is done in any memory system. You have 32-bit-wide 16:59

12 DDR2, I believe. But, secondly, there is nothing 16:59

13 that says you need to use 64. That is just an 16:59

14 arbitrary number that is chosen for one embodiment. 16:59

15 That would be another motivation to move to 16:59

16 DDR2 or DDR3 because you might be able to get the 16:59

17 same performance out of 32 or 16 or even 8 bits 16:59

18 wide. So you would be able to build this card much 16:59

19 cheaper, avoid a bunch of connectors and be much 16:59

20 more efficient. 16:59

21 Q. Why is that? 16:59

22 A. Because all the SDRAMs use block transfers. 17:00

23 So if you can transfer data twice as fast, or in the 17:00

24 case of DDR3 perhaps eight times as fast per pin, 17:00

25 then you can achieve approximately the same 17:00

1 performance with one-eighth as many pins. 17:00

2 So it's just an ordinary design tradeoff to 17:00

3 either increase the performance when moving to the 17:00

4 next DRAM generation or to reduce the bus width and 17:00

5 maintain the performance. 17:00

6 DDR2 and DDR3 chips also can contain four to 17:01

7 eight times as many bits per chip, so that would be 17:01

8 another motivation to reduce the number of chips and 17:01

9 move to the new memory technology. 17:01

10 Q. But the bus width is always 32 or 64 bit 17:01

11 depending on what the PCI bus width it is; right? 17:01

12 A. No. There is a processor in between. That 17:01

13 processor has buffers. It can change the bus width 17:01

14 to whatever it wants. 17:01

15 Q. Yeah, but when you go to the PCI one, it's 17:01

16 always going to be 64 bits anyways. 17:01

17 A. Correct. But that 64 bits can be eight 17:01

18 8-bit transfers onto the SDRAM. That is done all 17:01

19 the time. That's why there's a processor in between 17:01

20 and a separate memory controller, to be able to act 17:01

21 as an interface between the PCI protocol and the 17:01

22 SDRAM protocol. 17:02

23 Q. But you can make the transfer between the 17:02

24 SDRAM and the processor more efficient, but if the 17:02

25 bottleneck is at the PCI interconnectors, how would 17:02

1	what are those motivations?	17:04
2	A. I will see if I can find them. Partly, it's	17:04
3	the combination with Amidi, which discloses the use	17:04
4	of DDR and DDR2 devices, and then -- let's see.	17:05
5	I mention the fact that those newer devices	17:05
6	had already been standardized in paragraph 198.	17:05
7	Those are the ones that I see at the moment,	17:05
8	but there may be other explanations as well in	17:06
9	this -- in the declaration.	17:06
10	Q. Is it fair to say the reasons you mentioned	17:06
11	five to ten minutes ago, those are not in your	17:06
12	declaration; right?	17:06
13	MR. CHANDLER: Objection. Form.	17:06
14	THE WITNESS: I don't recall.	17:06
15	BY MS. ZHONG:	17:06
16	Q. Okay. Is it fair to say that in your	17:06
17	declaration, in your analysis, you kind of assumed	17:07
18	that the SDRAM refers to DDR2 or DDR3?	17:07
19	MR. CHANDLER: Objection. You drifted out	17:07
20	at the end. It was a little hard to hear.	17:07
21	DEPOSITION REPORTER: I'm sorry. I don't	17:07
22	think I got the full question.	17:07
23	BY MS. ZHONG:	17:07
24	Q. So is it fair to say that in your	17:07
25	declaration, your analysis assumed that the SDRAM	17:07

1 disclosed for Spiers are DDR2 or DDR3? 17:07

2 MR. CHANDLER: Objection to form. 17:08

3 THE WITNESS: No, I assumed that Spiers did 17:08

4 not describe a specific type of SDRAM, and that a 17:08

5 person of ordinary skill in the art, in view of 17:08

6 Amidi, would have chosen, or at least it would have 17:08

7 been obvious to choose, the most popular SDRAMs at 17:08

8 the time of the invention, which would have been 17:08

9 DDR2 and DDR3. 17:08

10 BY MS. ZHONG: 17:08

11 Q. So how does Amidi fit into your analysis 17:08

12 with Spiers? 17:08

13 A. It's analogous art. They're both describing 17:08

14 ways to provide backup power for a backup memory 17:08

15 system in light of a power failure. 17:09

16 Amidi uses a battery instead of a capacitor, 17:09

17 which would have been an obvious substitution. And 17:09

18 Amidi uses DDR and DDR2 DRAM. And Amidi also 17:09

19 discloses a specific structure, a power switch 17:09

20 multiplexer, that is relevant to some portions of 17:09

21 the analysis. 17:09

22 So I think that a person of ordinary skill 17:09

23 would have combined them because they are directed 17:09

24 to solving the same problem in very similar ways, 17:09

25 and that that combination would have further 17:09

1 motivated a person of ordinary skill to use DDR2 or 17:10
2 DDR3 memory since it's very clear that Amidi intends 17:10
3 to support the newest memory technologies. 17:10
4 Q. And you said "Amidi also discloses a 17:10
5 specific structure, a power switch multiplexer, that
6 is relevant to some portions of the analysis." 17:10
7 Which portions are you referring to in 17:10
8 specific? 17:10
9 A. In particular, I think I relied on as part 17:11
10 of claim 6 -- 17:11
11 Q. Okay. 17:11
12 A. -- because although claim 6 is supported by 17:11
13 Spiers, it's clear that Amidi has a trigger and also 17:11
14 Amidi mentions specific tolerances for that trigger. 17:12
15 So that supports some of those dependent claims, in 17:12
16 addition to the factors that I've mentioned before. 17:12
17 Q. So what is in Amidi that is absent from 17:12
18 Spiers? 17:12
19 DEPOSITION REPORTER: Was that for the 17:12
20 record, Counsel? 17:12
21 MR. CHANDLER: No. Just a cough. 17:12
22 THE WITNESS: The specific reference to DDR2 17:12
23 DRAMs is one. 17:12
24 BY MS. ZHONG: 17:13
25 Q. What else? 17:13

1 THE WITNESS: Not unless it was necessary. 17:17
2 You could do that. A person of ordinary skill would 17:17
3 know how to do that, but typically, if you have a 17:17
4 .2-volt drop in a modern buck converter, you can 17:17
5 support that. 17:17
6 So I would -- depending on the situation, I 17:17
7 would certainly -- as a person of ordinary skill, 17:17
8 would know how to generate 1.5 volts, 1.8 volts, 3.3 17:17
9 volts, 2.5 volts from a 3.6-volt lithium ion 17:17
10 battery. In fact, every phone in existence does it. 17:17
11 BY MS. ZHONG: 17:17
12 Q. I'm asking a slightly different question. 17:17
13 Would a POSITA step up the 3.6-volt power 17:18
14 supply to 12 volts, and then somehow step it back 17:18
15 down to 1.8 volts? 17:18
16 MR. CHANDLER: Objection. Form. 17:18
17 THE WITNESS: They might. That would be 17:18
18 certainly something they would know how to do, and 17:18
19 it would be something that they might rationally 17:18
20 choose to do if they wanted to handle a higher 17:18
21 degree of battery droop at the expense of lower 17:18
22 efficiency. 17:18
23 But I think the most straightforward thing 17:18
24 to do would be to generate all the voltages from 3.3 17:18
25 volts down directly from the 3.6-volt value. And a 17:18

1 buck converter -- 17:18

2 BY MS. ZHONG:

3 Q. How would stepping down --

4 A. -- a buck converter could substitute in 3.6 17:18

5 volts for 12 and still operate. 17:18

6 Q. So how would stepping this 3.6 volts first 17:18

7 to 12 volts and then convert it down to 1.8 volts 17:19

8 solve the droop problem, when in Amidi a straight 17:19

9 conversion from 3.6 to 1.8 doesn't have that 17:19

10 problem? 17:19

11 MR. CHANDLER: Objection. Form. 17:19

12 THE WITNESS: That would solve the problem 17:19

13 if, for example, your lithium ion battery got down 17:19

14 to 3.3 volts as it got old. But as I said, most 17:19

15 people would not take that approach. Most people 17:19

16 would simply directly convert the 3.6 volts to the 17:19

17 lower voltages. 17:19

18 BY MS. ZHONG: 17:19

19 Q. So if it gets down to 3.3 volts, wouldn't 17:19

20 that still work if the memory operates at a 1.8 17:19

21 volts? 17:19

22 A. Yes, but you could not use a buck converter 17:19

23 to get 3.3 volts out from 3.3 volts in. You would 17:20

24 need something a tiny bit higher. So you would 17:20

25 just --

1 Q. No, no, no --

2 A. -- need a different set of choices with 17:20

3 respect to what voltages you output. 17:20

4 Again, getting an output voltage from a 17:20

5 higher voltage with a buck converter is ordinary 17:20

6 engineering, and any person of ordinary skill would 17:20

7 know how to do that based on the specifics of a 17:20

8 particular design. 17:20

9 Q. I don't know where you got the 3.3 volt 17:20

10 from. I am saying the output I desire is 1.8 volts. 17:20

11 So even if the battery dropped to 3.3 volts, why 17:20

12 would there be a problem for you to use a buck 17:20

13 converter directly to convert the 3.3 volt to 17:20

14 1.8 volt? 17:20

15 A. There would not. If, hypothetically, I 17:20

16 would want to choose to only get 1.8 volts out of 17:21

17 the buck converter and supply 3.6 volts in, that 17:21

18 would work just fine. 17:21

19 Q. So in Amidi's situation where the battery 17:21

20 output is 3.6 volts and the ultimate desired voltage 17:21

21 is 1.8 volts, a POSITA generally would not step that 17:21

22 3.6 volts to 12 volts first and then step it down to 17:21

23 1.8 volts. 17:21

24 MR. CHANDLER: Objection. Form. And 17:21

25 incomplete. 17:21

1 THE WITNESS: No, they might. There are 17:21
2 reasons why one might do that, but there are also 17:21
3 reasons why one might not do that. A person of 17:21
4 ordinary skill would be able to implement either 17:21
5 approach with these. 17:21
6 BY MS. ZHONG:
7 Q. What would be the reason to step it up to 12 17:21
8 volts and where is that discussed in your 17:21
9 declaration? 17:21
10 A. None of this is discussed in my declaration. 17:21
11 This isn't what I proposed. What I proposed is 17:22
12 taking the teachings of Amidi and using them in 17:22
13 combination with Spiers. 17:22
14 Q. You never proposed to step up the 3.6 volts 17:22
15 to 12 volts first? 17:22
16 A. No. Like I said, a person could do that. A 17:22
17 person -- that would be a perfectly reasonable thing 17:22
18 to do. 17:22
19 Q. And why would you do that? 17:22
20 A. You might do that because if you want to 17:22
21 also generate 3.3 volts from the same power, it 17:22
22 would be easier to do so; or to give you other 17:22
23 flexibility in terms of the range of voltages that 17:22
24 you output. 17:22
25 Q. But Amidi already has a DC-DC boost buck 690 17:22

1 to generate the 3.3 volt rail; right? 17:23

2 A. Yes, and a boost buck is simply a boost 17:23

3 converter followed by a buck converter, which is 17:23

4 exactly what I suggested. 17:23

5 Q. Okay. And Amidi doesn't really say that you 17:23

6 do that by converting to 12 volts first. 17:23

7 MR. CHANDLER: Objection. Form. 17:23

8 THE WITNESS: No. A person of ordinary 17:23

9 skill would be able to analyze a power supply and 17:23

10 determine what the appropriate intermediate voltage 17:23

11 should be. 17:23

12 BY MS. ZHONG: 17:23

13 Q. I know a POSITA can do that, but what is the 17:23

14 reason for stepping up to 12 volts first and then 17:23

15 down to 1.8 volts? 17:23

16 A. In order to use the same supply for 17:23

17 3.3 volts or to be able to use the battery as it 17:23

18 becomes depleted. That would be a motivation to 17:24

19 do that. 17:24

20 MS. ZHONG: I want to take a five-minute 17:28

21 break. 17:28

22 MR. CHANDLER: Sure. 17:28

23 DEPOSITION REPORTER: We're off the record. 17:28

24 (Off the record.) 17:28

25 / / / 17:34

1 BY MS. ZHONG: 17:34

2 Q. As far as power efficiency is concerned, 17:34

3 would it be better for you to step the 3.6-volt 17:34

4 output from the lithium ion battery to 12 volts 17:34

5 first, and then generate the 1.8 volts or 1.5 volts

6 or would it be better for you to --

7 (Clarification requested by Reporter.)

8 BY MS. ZHONG:

9 Q. As far as power efficiency is concerned, 17:35

10 would it be better for a designer to step the 3.6 17:35

11 volt from the lithium ion battery charger 410 17:35

12 directly to 1.8 volts or 1.5 volts; or would it be 17:35

13 better for you to step the lithium ion battery 17:35

14 charge's output to 12 volts first and then down 17:35

15 convert that 12 volts to 1.8 volts and then 1.5 17:35

16 volts? 17:35

17 MR. CHANDLER: Objection. Form. Also 17:35

18 incomplete. 17:35

19 THE WITNESS: Yeah, I haven't suggested 17:36

20 either of those because the proposals that I put 17:36

21 forth all include 3.3 volts, as well, and that's 17:36

22 what would motivate you to convert to 12 volts. 17:36

23 The analysis is actually more complicated. 17:36

24 There is no simple answer. And the reason is that, 17:36

25 one, it may be difficult to get 3.3 volts from 3.6 17:36

1 volts depending on the circumstances, so you may 17:36
2 need to step it up anyway. 17:36
3 But also by allowing you to step up once and 17:36
4 then use that to supply all of your lower voltages, 17:36
5 you may be closer to the high efficiency operating 17:36
6 point for that conversion because you've combined 17:37
7 all of your outputs into a single up-conversion as 17:37
8 composed -- as opposed to something like the buck -- 17:37
9 the boost buck converter for one, and separate buck 17:37
10 converters for the others. 17:37
11 So you would have to do the specific 17:37
12 analysis to know which one is actually more 17:37
13 efficient, and it would vary based on current 17:37
14 requirements and specific combinations of voltages 17:37
15 that were selected. But, again, either one of them 17:37
16 would be obvious to a person of ordinary skill. 17:37
17 BY MS. ZHONG: 17:37
18 Q. Did you perform that analysis anywhere? 17:37
19 MR. CHANDLER: Objection. Form. 17:37
20 THE WITNESS: No. I simply explained one 17:37
21 set of obviousness implementations. 17:37
22 BY MS. ZHONG: 17:37
23 Q. Did you analyze how that would work out in 17:37
24 Harris' system? 17:38
25 A. I did. I show how it would work. Again, 17:38

1 there is no obligation in an obviousness analysis to 17:38
2 show that it's the best solution, only that it's an 17:38
3 obvious solution, and I believe I did that. 17:38

4 Q. And you did not show how the operation would 17:38
5 perform compared to what is shown here in Amidi 17:38
6 itself; right? 17:38

7 MR. CHANDLER: Objection. Form. 17:38

8 THE WITNESS: Well, it's a different design. 17:38
9 Amidi is not the combination of Harris and Amidi. 17:38
10 So no, I did not wholesale adopt Amidi's power 17:38
11 system into the combination with Harris. I took the 17:38
12 teachings from Amidi and used them to modify Harris. 17:38

13 BY MS. ZHONG: 17:39

14 Q. Okay. And in Amidi, there is a buck boost 17:39
15 690 that can generate 3.3 volts; right? 17:39

16 A. A boost buck 690, right. And as I 17:39
17 explained, one would have to do an analysis of a 17:39
18 particular system with particular currents and 17:39
19 particular converters to compare the efficiency. 17:39
20 But they would both be adequately efficient. 17:39
21 Whether or not one is better than the other is not 17:39
22 something I had to take into consideration. 17:39

23 Q. Okay. And so you did not perform any 17:39
24 analysis to show that for Harris FB-DIMM system 17:39
25 the -- your proposed operation would yield a better 17:39

1 performance in any circumstance; right? You just 17:40
2 think that there could be, but you did not perform 17:40
3 any analysis that that is the case; correct? 17:40
4 MR. CHANDLER: Objection. Form. 17:40
5 THE WITNESS: I did not perform an analysis 17:40
6 to show that the obvious solution that I explained 17:40
7 in my declaration would be better than some 17:40
8 alternative solution, no. 17:40
9 BY MS. ZHONG: 17:40
10 Q. I'm not talking about the alternative 17:40
11 solution. I'm talking about the solution that 17:40
12 Amidi -- how Amidi uses the output from its lithium 17:40
13 battery charger. 17:40
14 You did not compare it to how Amidi's 17:40
15 solution would be; right? 17:40
16 MR. CHANDLER: Objection. Form. 17:40
17 THE WITNESS: Amidi alone? No, I did not 17:41
18 compare the combination of Harris and Amidi to Amidi 17:41
19 alone. 17:41
20 BY MS. ZHONG: 17:41
21 Q. Okay. Have you designed VTT regulators for 17:41
22 DDR2 and DDR3 memory modules? 17:42
23 MR. CHANDLER: Objection. Form. 17:42
24 THE WITNESS: No. I have not designed 17:42
25 voltage regulators. They are readily available for 17:42

1 purchase. 17:42

2 BY MS. ZHONG: 17:42

3 Q. Okay. Do you provide any evidence as to the 17:42

4 type of VTT regulators -- let me put it this way. 17:42

5 What is the evidence in your declaration 17:42

6 regarding the type of regulators used to generate 17:42

7 VTT for DDR2 and DDR3 memory modules? 17:42

8 A. I think I provided evidence, for example, of 17:43

9 three different off-the-shelf regulators that can 17:43

10 provide voltages in the appropriate VTT range. 17:43

11 That's how, as I have explained, a person of 17:43

12 ordinary skill selects a voltage regulator. 17:43

13 Q. Okay. And which are those three voltage 17:43

14 regulators? 17:43

15 A. I believe they are Exhibit 1040, 1041, and 17:43

16 1048. But the references themselves also refer to 17:43

17 ordinary voltage regulators that a person of 17:43

18 ordinary skill would know how to implement at a 17:43

19 variety of different voltage levels. And I believe 17:43

20 Harris specifically mentions a range of voltage 17:43

21 levels that can be produced. 17:43

22 Q. Exhibit 1040 when it says "DDR selectable," 17:44

23 is it referring to the DDR1 or DDR2? 17:44

24 MR. CHANDLER: Objection. Form. 17:44

25 THE WITNESS: What page are you looking at? 17:44

1 BY MS. ZHONG: 17:44
2 Q. I'm just looking at the title. 17:44
3 A. It says right on the page that it's useful, 17:45
4 for example, for DDR1 or DDR2 termination. 17:45
5 Q. On which page? 17:45
6 A. On page 1 of Exhibit 1040 under 17:45
7 "Applications." 17:45
8 MR. CHANDLER: Annita, I think the seven 17:46
9 hours is up for today, so should we resume 9:00 a.m. 17:46
10 in the morning? 17:46
11 MS. ZHONG: Okay. That's fine. 17:46
12 DEPOSITION REPORTER: We're off the record. 17:46
13 (Ending time: 5:47 p.m.) 17:47
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I, ANDREW WOLFE, Ph.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this ____ day of _____,
2023, at _____, - _____.
(City) (State)

ANDREW WOLFE, Ph.D.

1 I, JANIS JENNINGS, CSR No. 3942, Certified
2 Shorthand Reporter, certify:

3 That the foregoing proceedings were taken
4 before me at the time and place therein set forth, at
5 which time the witness was duly sworn by me;

6 That the testimony of the witness, the
7 questions propounded, and all objections and statements
8 made at the time of the examination were recorded
9 stenographically by me and were thereafter transcribed;

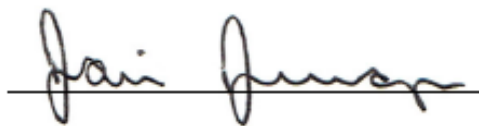
10 That the foregoing pages contain a full, true
11 and accurate record of all proceedings and testimony.

12 Pursuant to F.R.C.P. 30(e)(2) before
13 completion of the proceedings, review of the transcript
14 [X] was [] was not requested.

15 I further certify that I am not a relative or
16 employee of any attorney of the parties, nor financially
17 interested in the action.

18 I declare under penalty of perjury under the
19 laws of California that the foregoing is true and
20 correct.

21 Dated this 21st day of March 2023.

22
23 

24 JANIS JENNINGS, CSR NO. 3942

25 CLR, CCRR

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UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD

Samsung Electronics Co. Ltd.	Case No. IPR2022-00996
Petitioner,	Patent No. 11,016,918
vs.	
Netlist, Inc.,	Case No. IPR2022-00999
Patent Owner.	Patent No. 11,232,054

-----/

VIDEOCONFERENCE DEPOSITION OF ANDREW WOLFE, Ph.D.

Friday, March 17, 2023

Volume II (Pages 200 - 296)

Reported Remotely and Stenographically by:
JANIS JENNINGS, CSR No. 3942, CLR, CCRR
Job No. 5773633

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DEPOSITION OF ANDREW WOLFE, Ph.D., appearing remotely,
located in Santa Clara, California, taken on behalf of
the Petitioner, beginning at 9:01 a.m., on Friday,
March 17, 2023, sworn remotely by Janis Jennings,
Certified Shorthand Reporter No. 3942, CCRR, located in
the City of Walnut Creek, County of Contra Costa, State
of California.

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I N D E X

WITNESS	PAGE
ANDREW WOLFE, Ph.D.	
VOLUME II (Pages 200 - 296)	
EXAMINATION BY MS. ZHONG (Resumed)	204

E X H I B I T S

EXHIBIT	PAGE
Exhibit 2102 Design Notes PCI Express Power and Mini Card Solutions - Design Notes	219
346	

1 Friday, March 17, 2023; 9:01 a.m.

2

3 ANDY WOLFE,

4 the witness herein, was sworn

5 and testified as follows:

6

7 EXAMINATION (Resumed) 09:00

8 BY MS. ZHONG: 09:00

9 Q. Dr. Wolfe, can you please pull up 09:01
10 Exhibit 1025, Spiers. 09:01

11 A. Okay. 09:01

12 Q. Can you please go to Figure 3? 09:01

13 A. Yes. 09:01

14 Q. Do you see that in Figure 3, there is a 09:01
15 write-back cache 148 within the storage device 140? 09:01

16 A. I do. I think it's important to understand 09:02
17 that that's a different embodiment than the one that 09:02
18 I identified in my declaration. 09:02

19 Q. Okay. And there's a separate backup device 09:02
20 144, separate from the storage device 140. 09:02

21 Do you see that? 09:02

22 A. I do. Again, that's not the embodiment that 09:02
23 I identified in my declaration. 09:02

24 Q. Okay. And the write-back cache and backup 09:02
25 device are two different things; correct? 09:02

Page 204

1 MR. CHANDLER: Objection. Form. 09:02

2 THE WITNESS: In the Figure 3 embodiment, 09:02

3 they are. 09:02

4 BY MS. ZHONG: 09:02

5 Q. Okay. And in Figure 4, Figure 4 is an 09:02

6 illustration of a backup device 144; correct? 09:02

7 A. Correct. 09:02

8 Q. And the Figure 5 is an illustration of the 09:02

9 backup device 144; correct? 09:03

10 A. Of an embodiment of a backup device, 144. 09:03

11 Q. Okay. And if we go back to Figure 3, when 09:03

12 the storage controller on host system wants to 09:03

13 access data, does it access data from the backup 09:03

14 device or from the write-back cache 148? 09:03

15 A. I'm sorry. Did I reference Figure 3 at all 09:03

16 in my declaration? I don't believe I provided any 09:03

17 opinions on Figure 3. It's -- 09:03

18 Q. I'm asking a question. 09:03

19 A. -- of the patent.

20 Q. I'm asking the question. Can you answer the 09:03

21 question? 09:03

22 A. Ask the question again. Again, I have not 09:03

23 provided any opinions, I don't believe, about 09:03

24 Figure 3, unless you can point me to one in my 09:03

25 declaration. 09:04

1 Q. So when the storage system wants to access 09:04
2 data, does it access data from the write-back cache 09:04
3 or from the backup device? 09:04
4 A. In the Figure 3 device, which is completely 09:04
5 different than the Figure 5 device, I don't recall. 09:04
6 Q. Figure 5 is an illustration -- is an 09:04
7 embodiment of the backup device 144 in Figure 3; 09:04
8 correct? 09:04
9 A. It could be. Again, these are different 09:04
10 embodiments. Figure 5's embodiment is described 09:06
11 independently in the patent. 09:06
12 Q. So when the storage system wants to access 09:06
13 data, does it access data from the write-back cache 09:06
14 or from the backup device in Figure 3? 09:06
15 A. The patent clearly describes that it can 09:06
16 access data from the backup device; whether or not 09:06
17 it also can access data from the write-back cache, 09:06
18 perhaps. 09:06
19 But the backup device is clearly described 09:06
20 as having independent ability to read and write, and 09:06
21 that can be seen in Figure 10 and Figure 11, for 09:06
22 example. 09:06
23 Q. So when it needs to access data, does the 09:06
24 write-back cache act as a main memory or does the 09:07
25 host goes to backup device first? 09:07

1	MR. CHANDLER: Objection. Form.	09:07
2	THE WITNESS: As I said, the host has	09:07
3	the ability to directly and independently access	09:07
4	the backup device as described in Figures 10 and	09:07
5	Figures 11.	09:07
6	BY MS. ZHONG:	09:07
7	Q. Understood. Go ahead.	09:07
8	A. You have got to let me finish my answers.	09:07
9	The particular software on the host can	09:07
10	decide how it uses that capability, but certainly,	09:07
11	there is a disclosure of the ability to directly	09:07
12	access the backup device for either read or write	09:07
13	operations.	09:07
14	Q. Uh-huh. What I want to understand is which	09:07
15	one acts as the main memory storage?	09:07
16	A. Neither.	09:07
17	Q. For -- let's say the storage device operates	09:07
18	normally. Does the host go to the write-back cache	09:08
19	first to get the data, or does it go to the backup	09:08
20	device first?	09:08
21	MR. CHANDLER: Objection. Form.	09:08
22	THE WITNESS: It has the capability to do	09:08
23	either, depending on what the software on the host	09:08
24	chooses to do.	09:08
25	/ / /	09:08

1 BY MS. ZHONG: 09:08

2 Q. Based on Spiers' description, which one does 09:08

3 it access first? 09:08

4 MR. CHANDLER: Objection. Form. 09:08

5 THE WITNESS: The software has the 09:08

6 capability to access either one independently. 09:08

7 There's no need to access one before the other in 09:08

8 general. Both devices are on the bus, and as I've 09:08

9 said several times, Figure 10 and Figure 11 show 09:08

10 that the backup device can be directly accessed 09:08

11 independently of whether or not the write-back cache 09:08

12 is accessed. 09:09

13 BY MS. ZHONG: 09:09

14 Q. So if the data in the storage device is not 09:09

15 lost, does the host access the storage device data 09:09

16 first or access data from the backup device first? 09:09

17 MR. CHANDLER: Objection. Form. 09:09

18 THE WITNESS: It has the capability to do 09:09

19 either. 09:09

20 BY MS. ZHONG: 09:09

21 Q. I'm not asking about the capability. I'm 09:09

22 asking you how Spiers is programmed to do. 09:09

23 A. Spiers -- 09:09

24 MR. CHANDLER: Same objections to form. 09:09

25 THE WITNESS: Spiers discloses both 09:09

1 capabilities. It does not in any way tell us that 09:09
2 only one of them can be used. 09:09
3 BY MS. ZHONG: 09:09
4 Q. I'm not saying only one is used. I'm asking 09:09
5 in the normal operation, which one is accessed 09:09
6 first? 09:09
7 A. I don't know what you mean by "normal 09:10
8 operation." It's a computer. It has software. It 09:10
9 has the capability to independently access either 09:10
10 memory system. 09:10
11 Q. For "normal operation," that means the 09:10
12 storage device operates normally, there is no fault. 09:10
13 A. It has the capability to read either memory, 09:10
14 depending on what the software that's running on the 09:10
15 main processor chooses to do. 09:10
16 Q. So you did not consider how actually Spiers 09:10
17 operates, which device it accesses first when both 09:10
18 the storage device and the backup device are 09:10
19 available? 09:10
20 MR. CHANDLER: Objection. Form. 09:10
21 THE WITNESS: I'm not sure what you're 09:10
22 referring to, but in any case, that would be a 09:10
23 single circumstance. I took the entirety of the 09:10
24 disclosure of Spiers, including the capabilities 09:10
25 that were taught with respect to the backup device 09:10

1 in Figure 10 and Figure 11. 09:11

2 BY MS. ZHONG: 09:11

3 Q. Okay. And the fact is you did not consider 09:11

4 Figure 3; correct? You considered that to be a 09:11

5 different embodiment from Figure 5; is that correct? 09:11

6 MR. CHANDLER: Object to form. 09:11

7 THE WITNESS: Figure 3 encompasses many 09:11

8 embodiments. It's a general diagram. Figure 5 09:11

9 embodiment is specific to the capabilities that are 09:11

10 shown in Figures 10 and Figures 11. Those need not 09:11

11 be present for other embodiments that may be 09:11

12 encompassed by Figure 3. 09:11

13 BY MS. ZHONG: 09:11

14 Q. Okay. So is Figure 5 a specific example of 09:11

15 the backup device in Exhibit 3? 09:11

16 A. It's a backup device of one embodiment of 09:11

17 the invention. 09:12

18 Q. Did you consider Figure 3? 09:12

19 MR. CHANDLER: Objection. Form. 09:12

20 THE WITNESS: I considered the entirety of 09:12

21 the patent, but Figure 3 is not really critical to 09:12

22 my opinion because my opinion is about backup device 09:12

23 144, which is only shown as a single block in 09:12

24 Figure 3. 09:12

25 / / / 09:12

1 BY MS. ZHONG: 09:12

2 Q. Okay. And so you did not consider how 144 09:12

3 operates in the entire system; correct? Because 09:12

4 it's not important to your analysis? 09:12

5 MR. CHANDLER: Object to form. 09:12

6 THE WITNESS: No, that's wrong. I 09:12

7 considered how it operates in the entire system, 09:13

8 including the disclosures of Figures 10 and 11 and 09:13

9 how they worked together with the disclosures of 09:13

10 Figure 4 and Figure 5. 09:13

11 BY MS. ZHONG: 09:13

12 Q. And did you consider how 144 works with 148 09:13

13 and 140? 09:13

14 A. No, not really, because there's an 09:13

15 independent description of the capabilities of the 09:13

16 storage controller's interactions with backup device 09:13

17 144, and that's sufficient to meet the elements that 09:13

18 I needed for the claim. Whether or not it also has 09:13

19 the capability of interacting with other devices 09:13

20 wasn't necessary for me to form my opinion. 09:13

21 Q. What is the typical size of the write-back 09:13

22 cache?

23 A. There's no -- 09:14

24 MR. CHANDLER: Objection. Form. 09:14

25 THE WITNESS: There is no typical size. The 09:14

1 size is selected based on the requirements of a 09:14
2 particular system. 09:14
3 BY MS. ZHONG: 09:14
4 Q. So for Spiers' system, any idea what the 09:14
5 range of the size for the write-back cache 148? 09:14
6 A. I don't recall Spiers limiting it in any 09:14
7 way. 09:14
8 Q. So at the time of the invention, what is a 09:14
9 typical write-back cache for a disk drive? 09:14
10 A. I don't recall. And, again, it wouldn't 09:15
11 have impacted my opinion. 09:15
12 Q. And is a disk drive controller a memory 09:15
13 controller? 09:15
14 MR. CHANDLER: Objection. Form. 09:15
15 THE WITNESS: A disk -- what do you mean by 09:15
16 a "disk drive controller"? 09:15
17 BY MS. ZHONG: 09:15
18 Q. For example, a hard drive disk controller. 09:15
19 A. That's not helpful for me. There are 09:15
20 different kinds of devices that one might refer to 09:15
21 with those words. 09:15
22 Q. What is your understanding of a "disk drive 09:16
23 controller"? 09:16
24 A. Most commonly, I would understand that to be 09:16
25 the microprocessor that is embedded in a disk drive. 09:16

1 Q. And what is the storage controller in 09:16
2 Figure 3 of Spiers? 09:16
3 A. I think the most likely understanding of a 09:16
4 person of ordinary skill is that it's an ordinary 09:17
5 microprocessor. 09:17
6 Q. Is that a memory controller? 09:17
7 A. It would incorporate a memory controller to 09:17
8 access memory. 09:17
9 Q. And do you consider the processor on the PCI 09:17
10 card a memory controller as well? 09:17
11 A. I think we went over this yesterday. No, 09:17
12 but it would incorporate one or more memory 09:17
13 controllers. 09:17
14 Q. And is the storage controller 132 a memory 09:17
15 controller then, or it just includes -- may include 09:17
16 a memory controller? 09:17
17 MR. CHANDLER: Objection. Form. 09:17
18 THE WITNESS: The storage controller would 09:17
19 be a microprocessor system. It would include a 09:17
20 memory controller, but it would also include things 09:17
21 that are not a memory controller. And at that time, 09:17
22 it could be one chip or it could be multiple chips. 09:18
23 BY MS. ZHONG: 09:18
24 Q. What is a memory controller? 09:18
25 MR. CHANDLER: Objection. Form. 09:18

1 THE WITNESS: Again, it depends on context, 09:18
2 but in the context of an ordinary microprocessor, 09:18
3 it's the interface that provides the timing and 09:18
4 control signals to memory. 09:18
5 BY MS. ZHONG: 09:18
6 Q. So for the DRAMs on the PCI card, what is 09:18
7 the device that provides the timing and control 09:18
8 signals to the memory? 09:18
9 MR. CHANDLER: Objection. Form. 09:18
10 THE WITNESS: A portion of processor 198. 09:18
11 BY MS. ZHONG: 09:18
12 Q. Does the storage controller provide the 09:19
13 timing and control signals? 09:19
14 MR. CHANDLER: Objection. Form. 09:19
15 THE WITNESS: To something, yes. 09:19
16 BY MS. ZHONG: 09:19
17 Q. Does the storage controller provide timing 09:19
18 and the control signals to the SDRAMs on the PCI 09:19
19 card? 09:19
20 MR. CHANDLER: Objection. Form. 09:19
21 THE WITNESS: No. 09:19
22 BY MS. ZHONG: 09:19
23 Q. Does the storage controller 132 provide 09:19
24 timing and control signals to the NAND flash on the 09:19
25 PCI card? 09:19

1	MR. CHANDLER: Objection. Form.	09:19
2	THE WITNESS: No.	09:19
3	BY MS. ZHONG:	09:19
4	Q. Does the memory controller in 132 -- let me	09:19
5	withdraw and ask.	09:19
6	So your answer just now includes the memory	09:19
7	controller that's included within the storage	09:19
8	controller; is that correct?	09:20
9	A. I don't understand the question.	09:20
10	Q. Okay. You said that the storage controller	09:20
11	132 includes a memory controller -- in-memory	09:20
12	controller; correct?	09:20
13	A. Yes.	09:20
14	Q. Okay. So does the memory controller within	09:20
15	the storage controller 132 provide the timing and	09:20
16	control signals to the NAND flash on the PCI card?	09:20
17	MR. CHANDLER: Objection. Form.	09:20
18	THE WITNESS: No.	09:20
19	BY MS. ZHONG:	09:20
20	Q. Does the memory controller within the	09:20
21	storage controller 132 provide the timing and	09:20
22	control signals to the SDRAM on the PCI card?	09:20
23	MR. CHANDLER: Objection. Form.	09:20
24	THE WITNESS: No.	09:20
25	/ / /	09:20

1 BY MS. ZHONG: 09:20

2 Q. And so the only memory controller that 09:20

3 provides the timing and control signals to the SDRAM 09:20

4 and the NAND flash on the PCI card is the memory 09:20

5 controller within processor 198 on the PCI card; is 09:21

6 that correct? 09:21

7 MR. CHANDLER: Objection. Form. 09:21

8 THE WITNESS: There would likely be multiple 09:21

9 memory controllers within 198, one for the NAND 09:21

10 flash and one for the SDRAM. 09:21

11 BY MS. ZHONG: 09:21

12 Q. Okay. So the memory controllers that 09:21

13 provide the timing and the control signals to the 09:21

14 memories on the PCI card, are those residing within 09:21

15 processor 198? Is that fair? 09:21

16 MR. CHANDLER: Objection. Form. 09:21

17 THE WITNESS: Yes. 09:21

18 BY MS. ZHONG: 09:21

19 Q. In your analysis of Spiers, did you rely on 09:21

20 any interface other than the PCI interface? 09:22

21 A. Yes. 09:22

22 Q. Which interface? 09:22

23 A. I rely on the memory interfaces as well and 09:22

24 on the PCI detector. We'd have to go through the 09:22

25 entirety of my analysis, but certainly there are 09:22

1 interfaces in numerous places between chips. 09:22

2 Q. When you say "the PCI detection interface," 09:22

3 that's still for the PCI, isn't that? 09:22

4 A. It's really for the power supply. I guess 09:22

5 it comes over the PCI connector, but not normally 09:22

6 what we would think of as part of the PCI bus. 09:22

7 Q. Okay. So maybe it's poorly phrased. 09:22

8 When I'm saying like a "PCI interface," are 09:23

9 you relying on any -- so, for example, for the 09:23

10 limitation of plurality of edge connection, you are 09:23

11 only relying on the PCI-X connections for that 09:23

12 limitation; is that correct? 09:23

13 A. What claim is that? 09:23

14 Q. Claim 1, for example. 09:23

15 A. Correct. But I will note that that's 09:23

16 different language; that that is power, data, 09:23

17 address and control signals between the memory 09:24

18 module and the host system. It's not provided to 09:24

19 the memory devices. 09:24

20 Q. Okay. So for the interface between the host 09:24

21 system and the -- whatever you call the module, the 09:24

22 PCI interface is the only one that you relied on; is 09:24

23 that correct? 09:24

24 A. Correct. The module is the PCI card, and 09:24

25 the PCI connector is the interface that enclosed a 09:24

1 plurality of edge connections. 09:24

2 Q. And so you're not relying on any other types 09:24

3 of module powers? 09:24

4 A. Not for Spiers, no. 09:24

5 Q. Okay. And the only PCI standard that you 09:24

6 relied on in your declaration is Exhibit 1031; is 09:25

7 that correct? 09:25

8 A. That's the exemplary one that I gave, but -- 09:25

9 Q. Did you rely on any other PCI specification 09:25

10 for your analysis? 09:25

11 A. Well, Spiers discloses PCI in general, so a 09:25

12 skilled artisan would have been aware of all the PCI 09:25

13 specifications that were known at the time, but I 09:25

14 did use the PCI 2.2 specification as an example. 09:25

15 Q. Okay. And I think yesterday I asked you 09:25

16 whether you were aware of the fact that PCI Express 09:25

17 did not have a 5 volt supply voltage rail, and you 09:26

18 said you don't know one way or the other. 09:26

19 Remember that exchange? 09:26

20 A. Yeah. I believe that's incorrect as I think 09:26

21 about it more. I don't think it uses any 5 volt 09:26

22 signaling, but my recollection is that the PCI-X did 09:26

23 have a 5 volt supply rail. 09:26

24 Q. Did you look up the PCI Express standard or 09:26

25 the PCI Express data sheets? 09:27

1	A.	Not recently, no.	09:27
2	Q.	Okay.	09:27
3	A.	But I do -- I thought I had seen it in one	09:27
4		of the exhibits. I believe it's referenced in	09:27
5		Exhibit 2016.	09:27
6	Q.	Okay. Where in Exhibit 2016?	09:27
7	A.	Page 8, there's a section called "Powering	09:28
8		Voltage" where it says:	09:28
9		"All PCI system slots are required	09:28
10		to deliver +5 and +3.3 volt power	09:28
11		independently of their 5 volt or	09:28
12		3.3 volt signaling system."	09:28
13	Q.	Yeah. Those are PCI, which is up to 3.0.	09:28
14		It doesn't include PCI Express.	09:28
15	A.	It says "all PCI" and certainly most of this	09:28
16		document is discussing PCI-X.	09:29
17	MS. ZHONG:	PCI -- I don't believe so.	09:29
18		Let's take a look at it.	09:29
19		Can you please open up Exhibit 2102 in	09:30
20		Exhibit Share.	09:30
21		(Exhibit 2102 marked for identification.)	09:30
22	MR. CHANDLER:	I don't see it.	09:30
23	THE WITNESS:	I don't either. Did it get	09:30
24		put into a different directory?	09:30
25	MS. ZHONG:	Yeah. There is a March 13	09:30

1 directory. 09:30

2 MR. CHANDLER: I'm downloading it. Just one 09:30

3 moment, please. 09:30

4 THE WITNESS: Yes. What's the question? 09:30

5 MR. CHANDLER: One moment, please. 09:30

6 BY MS. ZHONG: 09:31

7 Q. Do you see that in Exhibit 2102, there 09:31

8 are only two power rails, 12 volts and 3.3 volts, 09:31

9 but not a 5 volt one? 09:31

10 MR. CHANDLER: One moment, please. 09:31

11 Okay. I have it. Go ahead. 09:31

12 THE WITNESS: Yes. But this is about PCI 09:31

13 Express. PCI Express is a completely different 09:31

14 standard than PCI-X. 09:31

15 BY MS. ZHONG: 09:31

16 Q. I thought you said yesterday we were talking 09:31

17 about PCI Express. 09:31

18 A. No. PCI-X. 09:31

19 Q. Okay. Is PCI-X the same as PCI? 09:31

20 A. No. It's a higher bandwidth solution that's 09:31

21 available -- I mean, it's a flavor of PCI. It's one 09:32

22 of the variations of PCI, as one can see in 09:32

23 Exhibit 2016, but it was designed for servers. 09:32

24 Q. Okay. And is PCI Express considered a 09:32

25 flavor of PCI, or that's also totally different than 09:32

1	PCI?	09:32
2	A. PCI Express was considered a replacement	09:32
3	rather than an evolution. It used a completely	09:32
4	different theory of operation. There was zero	09:32
5	compatibility.	09:32
6	In fact, if we look at Exhibit 2016, it	09:32
7	describes PCI-X as a high performance evolution of	09:33
8	conventional PCI, and PCI Express as a replacement.	09:33
9	Q. Okay. But as you say, PCI-X and PCI are two	09:33
10	different species; correct?	09:33
11	A. Two different what?	09:33
12	Q. Species.	09:33
13	MR. CHANDLER: Species?	09:33
14	BY MS. ZHONG:	09:33
15	Q. Correct.	09:33
16	A. They are variations on the PCI standard.	09:33
17	Q. You did not -- your analysis relies on	09:33
18	Exhibit 1031; correct?	09:33
19	A. I gave Exhibit 1031 as an example of a PCI	09:33
20	specification that would be suitable for use with	09:33
21	Spiers.	09:33
22	Q. Okay. And you did not cite PCI-X anywhere	09:33
23	in your declaration; correct?	09:33
24	A. I don't think I did, no.	09:34
25	Q. Okay. What is an "add-in card"?	09:34

1 MR. CHANDLER: I didn't hear the word. 09:34
2 MS. ZHONG: Add-in card. 09:34
3 THE WITNESS: I would need context again, 09:34
4 but that term is often used with computers to refer 09:34
5 to a removable circuit board or an optional circuit 09:35
6 board. 09:35
7 BY MS. ZHONG: 09:35
8 Q. So in the context of Exhibit 1031, 09:35
9 section 1.1. 09:35
10 A. Let me look. Are you talking about the 09:35
11 phrase "peripheral add-in boards"? 09:35
12 Q. Correct. 09:35
13 A. A peripheral is usually some type of an 09:35
14 input/output device that would be connected to a 09:36
15 computer. So a peripheral add-in board would 09:36
16 presumably be a board that includes a peripheral or 09:36
17 a board that acts as an interface to a peripheral. 09:36
18 Q. It's not referring to what we usually call a 09:36
19 PCI card, is it? 09:36
20 A. Oh, yes. All three of these are three 09:36
21 different kinds of PCI cards; a peripheral 09:36
22 controller, a peripheral board or a processor memory 09:36
23 system. 09:36
24 I'm sorry. Let me correct that. The 09:36
25 complete phrase "highly integrated peripheral 09:37

1 controller components" I think is designed for PCI 09:37
2 components that are not on a card. Peripheral 09:37
3 add-in boards and memory cards would be on cards. 09:37
4 Q. Peripheral add-in boards, those are the 09:37
5 removable PCI cards? 09:37
6 A. That is one kind of removable PCI card. You 09:37
7 can also have a memory card or a processor card. 09:37
8 Q. Can you pull up Exhibit -- let me see which 09:37
9 one is Hajeck. Exhibit 1033. 09:38
10 A. Hajeck is 1038. 09:38
11 Q. Sorry. My handwriting is really bad. 09:38
12 Exhibit 1038. 09:38
13 A. Okay. 09:38
14 Q. In Exhibit 1038, when the voltage detection 09:38
15 circuit detects an anomaly, it sends the ready and 09:38
16 busy signal back to the host system; correct? 09:38
17 MR. CHANDLER: Objection. Form. 09:38
18 THE WITNESS: Yes, it does. 09:38
19 BY MS. ZHONG: 09:39
20 Q. Okay. So the busy signal is never sent to, 09:39
21 for example, the controller 40. 09:39
22 A. Not directly. 09:40
23 Q. So the busy signal -- Hajeck doesn't really 09:40
24 disclose sending the busy signal to controller 40; 09:40
25 correct? 09:40

1	A. Not directly.	09:40
2	Q. The busy signal is not sent to controller	09:40
3	40; correct?	09:40
4	MR. CHANDLER: Objection. Form.	09:40
5	THE WITNESS: Not directly.	09:40
6	BY MS. ZHONG:	09:40
7	Q. Does controller 40 receive the busy signal	09:41
8	sent from the voltage detection circuit?	09:41
9	MR. CHANDLER: Objection. Form.	09:41
10	THE WITNESS: Not directly, but eventually	09:41
11	it would be informed by the host that it should	09:41
12	complete its operation in response to the ready-busy	09:41
13	signal.	09:41
14	BY MS. ZHONG:	09:41
15	Q. Okay. But it's not the busy signal that is	09:41
16	sent from the voltage detection circuit, it's from	09:41
17	other command; is that right?	09:41
18	MR. CHANDLER: Objection. Form.	09:41
19	THE WITNESS: It's not the physical direct	09:41
20	signal 38, but it would be in response to 38.	09:41
21	BY MS. ZHONG:	09:41
22	Q. And what is a "charge pump"?	09:41
23	A. A charge pump is a type of switching power	09:41
24	inverter, usually for switching from a low voltage	09:41
25	to a higher voltage.	09:41

1 Q. So it's more -- 09:42

2 A. I'm sorry. But a charge pump can also be 09:42

3 used to switch the plurality of a voltage as well 09:42

4 from positive to negative or negative to positive. 09:42

5 Q. So it's a bit like a heat pump? 09:42

6 A. In a very abstract way. It does -- it pumps 09:42

7 charge in and out of a capacitor and in doing so, 09:42

8 can alter the voltage current characteristics of the 09:42

9 power system. It's not pumping from in to out. It 09:42

10 pumps internally. 09:42

11 Q. Is a charge pump a buck boost converter? 09:42

12 A. It's similar, but I don't think it's -- 09:42

13 meets the textbook definition of a buck boost 09:43

14 converter. 09:43

15 Q. What is your textbook definition of a buck 09:43

16 boost converter? 09:43

17 A. A textbook buck boost converter would depend 09:43

18 on an inductor. A charge pump can't operate with 09:43

19 capacitors alone. 09:43

20 Q. So is a charge pump a switched capacitor 09:43

21 converter then? 09:43

22 A. Yes. I would consider it to be a type of a 09:43

23 switched capacitor converter. But it is defined 09:43

24 rather broadly within the Hajeck reference as a DC 09:44

25 step up/step down converter. 09:44

1 Q. Uh-huh. But to a POSITA when they see the 09:44
2 word "charge pump," they don't really consider that 09:44
3 to be a buck boost converter? 09:44
4 MR. CHANDLER: Objection. Form. 09:44
5 THE WITNESS: Independently of any 09:44
6 additional teaching, that probably is true. But I 09:44
7 think in the context of Hajeck where he broadly says 09:44
8 that it comprises a DC step up/step down converter, 09:44
9 DC-to-DC step up/step down converter, a POSITA would 09:45
10 read it as being any type of step up/step down 09:45
11 converter. 09:45
12 BY MS. ZHONG: 09:45
13 Q. Is a switched capacitor converter a step 09:45
14 up/step down converter? 09:45
15 A. It can be. 09:45
16 Q. So in Hajeck, how does the operating mode of 09:45
17 the memory subsystem change in response to the 09:45
18 detection by the voltage detection circuit? 09:46
19 A. It completes any write operations in 09:46
20 progress, it backs up any configuration data stored 09:46
21 in volatile memory, and it can complete a shutdown 09:46
22 sequence. 09:46
23 Q. And does it switch -- let me ask it this 09:46
24 way. 09:46
25 If there is no voltage anomaly detected, the 09:46

1 charge pump provides the power supply voltage; is 09:46
2 that correct? 09:47

3 A. The controller and possibly two other 09:47
4 elements would suggest that there may be other 09:47
5 elements that are supplied in a different way as 09:47
6 well. 09:47

7 Q. Okay. So at least as far as the elements 09:47
8 that's shown in figures -- like for the 09:47
9 controller that's shown in -- let me withdraw and 09:47
10 ask it this way. 09:47

11 So at least with respect to the components 09:47
12 shown in the non-volatile memory subsystem 30 in 09:47
13 Figure 1, the charge pump supplies the power supply 09:47
14 voltage when the voltage detection circuit doesn't 09:48
15 detect any anomaly; is that right? 09:48

16 A. I don't think that's what it says. It says 09:48
17 that it supplies the power to disk drive controller 09:48
18 40 and possibly other active components. 09:48

19 Q. Such as volatile memory used as a buffer? 09:48

20 A. Right. Which at least in Figure 1 is not 09:48
21 shown. 09:48

22 Q. And after the detection of a voltage 09:48
23 anomaly, the charge pump continues to supply the 09:49
24 power; is that correct? 09:49

25 A. For at least a minimum time period. 09:49

1 Q. And according to Hajeck, as long as the V-in 09:49
2 exceeds 0.7 volts -- 09:50
3 (Clarification requested by Reporter.) 09:50
4 BY MS. ZHONG: 09:50
5 Q. So according to Hajeck, as long as the V-in 09:50
6 exceeds 0.7 volts, the charge pump is capable of 09:50
7 maintaining the VREF at 5.4 volts indefinitely; 09:50
8 Correct? 09:50
9 MR. CHANDLER: Are you reading from 09:50
10 something? I mean, are you reading the document? 09:50
11 MS. ZHONG: Yes. It's Exhibit 1038 columns 09:50
12 3, lines 6 to 10. 09:50
13 DEPOSITION REPORTER: Thank you. That's 09:51
14 very helpful. I appreciate that. 09:51
15 THE WITNESS: Can I answer? 09:51
16 BY MS. ZHONG: 09:51
17 Q. Sure.
18 A. That is true in one embodiment that's 09:51
19 described in column 3. 09:51
20 Q. Okay. So at least Hajeck's teaches a way 09:51
21 where the charge pump can maintain the required 09:51
22 voltage regulation indefinitely as long as the in 09:51
23 exceeds a 0.7 volt threshold; is that right? 09:51
24 A. Hajeck does teach one embodiment that does 09:51
25 that. 09:51

1 Q. How does the charge pump serve to protect 09:51
2 the controller 40 and other circuit from damage 09:52
3 caused by voltage surges and spikes? 09:52
4 A. Let me think of a reasonably simple way to 09:52
5 do this. The charge pump does not pass V-in to the 09:52
6 disk drive controller. Instead, it accumulates the 09:52
7 energy from V-in into a capacitor and then switches 09:52
8 that energy out, and, therefore, there's an energy 09:52
9 reservoir. So something like a spike would be 09:52
10 diluted in that reservoir and would not be passed 09:52
11 through. 09:52
12 Q. So as far as the charge pump itself is 09:52
13 concerned, it can operate normally even if there is 09:53
14 a voltage surge or spike; is that right? 09:53
15 A. Depending on the characteristics of the 09:53
16 surge or the spike. If it's large enough, it would 09:53
17 damage the charge pump. But if it's small enough, 09:53
18 then the charge pump potentially could stay within 09:53
19 its normal operating parameters. 09:53
20 Q. So if the surge or spike is large enough and 09:53
21 it damages the charge pump, the charge pump won't be 09:53
22 able to serve the purpose of protecting the 09:53
23 controller 40 and other circuit from damages caused 09:53
24 by voltage surges and spikes; correct? 09:53
25 A. Yes. I think that's true of all circuits. 09:53

1 If this gets hit by lightning, it's going to be 09:53
2 damaged. 09:53
3 Q. Okay. So if the charge pump serves its 09:53
4 purpose of protecting controller 40 and other 09:53
5 circuits from damage caused by voltage surges and 09:54
6 spikes, that is an indication that the voltage surge 09:54
7 and spike is really not a problem as far as the 09:54
8 charge pump is concerned, it can absorb the excess 09:54
9 charges? 09:54
10 MR. CHANDLER: Objection. Form. 09:54
11 THE WITNESS: There will be some set of 09:54
12 spikes and surges that can be absorbed by the charge 09:54
13 pump. That doesn't mean there is not a problem. 09:54
14 Sometimes those can be indicative of upcoming 09:54
15 problems. 09:54
16 BY MS. ZHONG: 09:54
17 Q. So in Hajeck's case, before and after the 09:55
18 detection of an input undervoltage or overvoltage, 09:55
19 there is no switching of the power supplies; is that 09:55
20 right? 09:56
21 A. Did you say before or after? 09:56
22 Q. Before and after, yes. 09:56
23 A. Well, after there is an indication that 09:56
24 there's a shutdown, so that would certainly indicate 09:56
25 to me that everything is being shut down, the entire 09:56

1 computer. 09:56

2 Also, Hajeck contemplates that some of the 09:56

3 anomalies may be a loss of power, in which case the 09:56

4 power supplies are maintained for a minimum period, 09:56

5 but then they're shut down. 09:56

6 Q. Okay. But during that period it's -- the 09:56

7 power is supplied by the charge pump as before 09:56

8 detection of the anomaly; is that right? 09:56

9 A. Well, there are two embodiments. There is 09:57

10 one where it is supplied by the charge pump and 09:57

11 there is another one in which a battery takes over 09:57

12 to provide additional time for shutdown. 09:57

13 Q. But even during that second embodiment, the 09:57

14 charge pump still supplies the -- still continues to 09:57

15 supply the voltage; correct? 09:57

16 MR. CHANDLER: Object to form. 09:57

17 THE WITNESS: Long enough to complete 09:57

18 outstanding operations, but subsequent things such 09:57

19 as the shutdown sequence may need to happen on a 09:57

20 battery. 09:57

21 BY MS. ZHONG: 09:57

22 Q. The battery and the capacitive array is just 09:57

23 used to extend the operating time -- it's just to 09:58

24 extend the time duration for which backup power is 09:58

25 provided; is that right? 09:58

1 MR. CHANDLER: Objection to form. 10:01

2 THE WITNESS: I don't see what the 10:01

3 relationship is. But one would presumably choose a 10:01

4 super cap of appropriate size to provide back -- the 10:01

5 necessary amount of backup power, whether it's 10:01

6 regulated or not. 10:01

7 In this case, it is going to be regulated 10:01

8 down to 3.3 volts, which means that it would likely 10:01

9 continue to provide power until the super cap 10:01

10 voltage got close to 3.3 volts. 10:01

11 BY MS. ZHONG: 10:01

12 Q. What I'm saying that if they choose a 10:01

13 regulator that is 5 volts to 3.3 volts, is that an 10:02

14 indication that the designer believes that the super 10:02

15 cap will be sufficiently charge -- will have enough 10:02

16 capacity to maintain the input voltage of 5 volts 10:02

17 for the duration needed for the backup operation? 10:02

18 MR. CHANDLER: Objection. Form. 10:02

19 THE WITNESS: Well, let me say two things. 10:02

20 One is I think the marking 5 volts to 3.3 volts is 10:02

21 nominal. That is the inversion while it is 10:02

22 operating off of post power, but I believe that if 10:02

23 the regulator is a normal common regulator, it's 10:02

24 going to be able to output 3.3 volts over some range 10:02

25 of inputs, probably higher than 5 volts and probably 10:02

1 down to something close to 3.3 volts. 10:03

2 So I wouldn't -- as a person of ordinary 10:03

3 skill wouldn't read that to indicate that that 10:03

4 regulator always needs exactly a 5 volt input. 10:03

5 But, as I mentioned before, the person would 10:03

6 perform an energy analysis to determine the 10:03

7 appropriate super cap size, and provide a super cap 10:03

8 that provides the appropriate amount of energy or 10:03

9 more. I don't think the regulator is a significant 10:03

10 impact to that analysis. You would use the 10:03

11 regulator's shutoff minimum voltage, which again 10:03

12 here is probably 3.5 or 3.6 as a factor in that 10:03

13 calculation. 10:03

14 BY MS. ZHONG: 10:03

15 Q. If you have a linear regulator, can you 10:03

16 convert 3.6 to 3.3 volts with high efficiency or you 10:04

17 can't do that? 10:04

18 MR. CHANDLER: Objection. Form. 10:04

19 You said "linear"? Is that what you said? 10:04

20 BY MS. ZHONG: 10:04

21 Q. Yes. 10:04

22 A. It would depend which linear regulator. 10:04

23 There are linear regulators that could, I believe, 10:04

24 convert 3.6 volts to 3.3 volts. 10:04

25 It depends what you mean by "high 10:04

1 efficiency." Would it be higher than a switching 10:04
2 regulator? It would depend on the actual currents 10:04
3 involved and the design of the particular 10:04
4 regulators. It would be -- converting 3.6 volts to 10:04
5 3.3 volts with a linear regulator is more efficient 10:04
6 than converting 20 volts to 3.3 volts with a linear 10:04
7 regulator, but again, these are mathematical 10:04
8 analyses that have to do with the specifications of 10:05
9 the exact part that an engineer would ordinarily do 10:05
10 in choosing a regulator. 10:05

11 Q. I thought you mentioned yesterday that 10:05
12 converting 3.6 volts to 3.3 volts using a buck 10:05
13 converter, there could be some difficulties; is that 10:05
14 correct? 10:05

15 A. Converting 3.3 volts to 3 -- I'm sorry, 10:05
16 converting 3.6 volts to 3.3 volts using either a 10:05
17 buck converter or a linear regulator, there could be 10:05
18 some difficulties. You would have to choose one 10:05
19 that has the appropriate low voltage drop 10:05
20 properties. Those are known, but you would have to 10:05
21 go to the extra effort of choosing one that was 10:05
22 suited for that particular situation. 10:06

23 What I mentioned yesterday was that if the 10:06
24 input voltage dropped below 3.6 to 3.3, that that 10:06
25 would be difficult to do with a buck converter, but 10:06

1 it would also be impossible to do with a linear 10:06
2 regulator. 10:06

3 Q. At the time of the invention, when you hear 10:06
4 the word "LDO," that usually refers to a linear 10:06
5 regulator; is that right? 10:06

6 A. If by "usually" you mean more often than 10:06
7 not, then that's probably true. But I believe that 10:07
8 there were data sheets at the time for switching 10:07
9 regulators that called them LDO and also for linear 10:07
10 regulators that called them LDO. 10:07

11 MS. ZHONG: Janis, my question is at the 10:07
12 time of the invention, not in the part of the 10:07
13 invention. 10:07

14 DEPOSITION REPORTER: Thank you. 10:07

15 BY MS. ZHONG: 10:07

16 Q. What is the amount of current that goes 10:08
17 through termination resistors for DDR2? 10:08

18 A. DDR2. Let me see if that's in the spec. 10:08
19 I don't recall the exact termination 10:09
20 resistor value off the top of my head for DDR2, but 10:09
21 in any case, the current would depend on the 10:09
22 incoming signals and the number of incoming signals 10:09
23 and their values. It would vary over time. 10:09

24 Q. How did it depend on the incoming signals? 10:09
25 A. They're very complicated. But the 10:09

1 termination resistance is part of a circuit and one 10:10
2 side of that circuit is the incoming signal. For 10:10
3 the terminations that are powered by VTT, those are 10:10
4 address and control signals, and depending on 10:10
5 whether a particular line is at a zero voltage or at 10:10
6 a 1.5 voltage or 1.8 voltage, the current would be 10:10
7 different. 10:10

8 But because they are changing so rapidly, 10:10
9 you can't really just analyze them in a steady 10:10
10 state. You have to analyze them by -- through an 10:10
11 integral, so you would need a particular sequence of 10:11
12 patterns on each signal and you would need to 10:11
13 perform a simulation with a circuit simulator that 10:11
14 has an accurate model of the transmission line 10:11
15 properties of the wiring. 10:11

16 Q. But on average, it is expected that half the 10:11
17 time, the VDD will be -- half the time the voltage 10:11
18 on the transmitter side will be at VDD and the other 10:11
19 half of the time, it will be at zero. So -- 10:11

20 A. Okay. Finish your question, please. 10:11

21 Q. Go ahead. 10:11

22 A. No. That's not true for address and 10:11
23 command, in particular. Right? So it may be 10:11
24 that -- that would require that you are using all of 10:12
25 the commands in equal proportion, which would be 10:12

1 unlikely, and it would require that you use every 10:12
2 location in memory with equal likelihood, which is 10:12
3 also unlikely. 10:12

4 Q. Okay. Do you have any idea what is the 10:12
5 range of the current for the signal line for address 10:12
6 command and card signal line? 10:12

7 MR. CHANDLER: Objection. Form.

8 THE WITNESS: No. It depends on how many 10:12
9 pins are being used in a particular embodiment, how 10:12
10 much memory there is, how much memory traffic there 10:12
11 is, the speed at which the memory is operating, the 10:12
12 particular selection of termination resistor. I 10:12
13 believe there was a choice of selections for DDR2. 10:12

14 So it's a very complicated analysis and 10:12
15 depends on lots of design decisions, and it's 10:13
16 typically something that nobody would try to compute 10:13
17 by hand. You would -- you would build a model and 10:13
18 feed it through simulation tools. 10:13

19 BY MS. ZHONG: 10:13

20 Q. Do you have any idea what its range might 10:13
21 be? 10:13

22 MR. CHANDLER: Objection. Form. 10:13

23 THE WITNESS: No, because you can build all 10:13
24 kinds of different systems, right? You can build 10:13
25 systems that range at very different speeds, that 10:13

1 have very different utilization; so, no, I don't. 10:13

2 BY MS. ZHONG: 10:13

3 Q. What about for Harris FB-DIMM? 10:13

4 A. Again, there's a great range of 10:13

5 implementations, and it would depend on a large 10:13

6 number of design decisions as to what the actual 10:13

7 value is or what the actual value range is. 10:13

8 Q. And in your proposal, the VTT is for 10:14

9 terminating the transmission lines between the AMB 10:14

10 and the DDR2 devices in Harris; is that right? 10:14

11 MR. CHANDLER: Objection. Form. 10:14

12 THE WITNESS: I may have missed part of the 10:14

13 question. It's used to terminate the address 10:14

14 command lines just as it is in the DDR2 and DDR3 10:14

15 standards, or DDR2 standard with respect to Harris. 10:14

16 BY MS. ZHONG: 10:14

17 Q. And the termination point is for the address 10:14

18 and the control signals sent by the AMB to the DDR2; 10:14

19 is that correct? 10:14

20 A. Correct. And the other -- yes. 10:14

21 Q. And you're not proposing to use 10:15

22 the on-module VTT regulator for the termination of 10:15

23 the signal --

24 (Clarification requested by Reporter.)

25 / / /

1 BY MS. ZHONG:

2 Q. And you are not proposing to use an 10:15
3 on-module voltage regulator to provide the 10:15
4 termination voltage for the information exchanged 10:15
5 between the memory controller on the host system and 10:15
6 the FB-DIMM; is that right? 10:15

7 MR. CHANDLER: Objection. Form. 10:15

8 THE WITNESS: To the extent that those are 10:15
9 on-die terminators in the buffer, they would be 10:15
10 powered by the VDDQ signal, I believe. 10:16

11 BY MS. ZHONG: 10:16

12 Q. And for the Spiers grant, the VTT is for 10:16
13 terminating the address command and the clock 10:16
14 information from the processor 198 to the DDR2 or 10:16
15 DDR3; is that right? 10:16

16 A. Yes. 10:16

17 Q. And it's for terminating from the processor 10:16
18 to the module -- 10:16

19 MR. CHANDLER: Objection. Form.

20 BY MS. ZHONG:

21 Q. -- is that right? 10:16

22 MR. CHANDLER: Objection. Form. 10:16

23 THE WITNESS: It's from the processor to the 10:17
24 DRAMs on the board, on the memory module. Whether 10:17
25 those DRAMs are directly on the PCI board or whether 10:17

1	they're on daughter boards.	10:17
2	BY MS. ZHONG:	10:17
3	Q. So if the DRAMs are on the daughter DIMM	10:17
4	boards, where will the terminating resistors be?	10:17
5	A. Where will the terminating resistors -- if	10:17
6	the SDRAMs are on daughter boards, then the	10:17
7	terminating resistors -- it would depend how you	10:17
8	hook up the SDRAM. They could be on the main board	10:17
9	or -- I mean, they could be on the PCI card or they	10:18
10	could be on the daughter boards, depending on what	10:18
11	kind of SDRAM you chose.	10:18
12	Q. I said DDR2.	10:18
13	A. I'll look at the DDR2 spec. You would have	10:18
14	to model the wiring stubs in the interconnect and	10:18
15	see which are the best solutions, but certainly, you	10:18
16	could put them directly next to the DRAM chips. I	10:18
17	think in certain circumstances, you could put them	10:19
18	on the board as well.	10:19
19	Q. I guess a more germane question is where	10:19
20	will the regulators be placed? Will the regulators	10:19
21	be placed on the motherboard or on the daughter	10:19
22	board?	10:19
23	A. They will be placed --	10:19
24	MR. CHANDLER: Object to form.	10:19
25	THE WITNESS: -- on -- they will be placed	10:19

1 on card 144. Because the daughter boards are 10:19
2 optional. They're not required. 10:19
3 BY MS. ZHONG: 10:19
4 Q. So if 190 is a memory module, which it is 10:19
5 there, where will the regulators be placed? 10:19
6 A. They'll be placed on 144 because 144 is 10:19
7 still a memory module, even if the memory -- whether 10:19
8 the memories are directly mounted on it or whether 10:20
9 the memories are mounted on daughter boards. 10:20
10 Q. Even if the termination resistors are placed 10:20
11 on the daughter board? 10:20
12 A. Yes. It would still be a memory module. 10:20
13 Q. What does that have anything to do with 10:20
14 whether the PCI is a memory module or not? 10:20
15 MR. CHANDLER: Objection to form. 10:20
16 THE WITNESS: Because this patent is about 10:20
17 memory modules that have voltage converters on it 10:20
18 and Spiers discloses one. 10:20
19 BY MS. ZHONG: 10:20
20 Q. Setting aside the fact that you are trying 10:20
21 to do an invalidity analysis of the '918, I'm just 10:21
22 talking about Spiers itself, how you would be doing 10:21
23 the design for Spiers. 10:21
24 So in the context of Spiers' PCI and with 10:21
25 DRAMs mounted on the module 190, and if the 10:21

1 termination resistors are on the daughter board, 10:21
2 what would be the advantage of having VTT be 10:21
3 supplied from the motherboard instead -- from the 10:21
4 PCI board instead? 10:21
5 MR. CHANDLER: Objection. Form. 10:21
6 THE WITNESS: There wouldn't necessarily be 10:22
7 an advantage, but it is what's taught by Spiers. 10:22
8 BY MS. ZHONG: 10:22
9 Q. Where does Spiers talk about supplying VTT 10:22
10 on the PCI board? 10:22
11 A. Spiers talks about having all of its 10:22
12 regulators on the PCI board. And a person of 10:22
13 ordinary skill would understand that if you needed 10:22
14 more voltages, you would have more regulators and 10:22
15 you would operate them in the same manner. 10:22
16 Q. Spiers did not discourage of having 10:22
17 regulators on the DRAM board -- on the DIMM board; 10:22
18 correct? 10:22
19 MR. CHANDLER: Objection. Form. 10:22
20 THE WITNESS: Spiers does not discourage 10:22
21 that, no. But it also doesn't teach it. 10:22
22 BY MS. ZHONG: 10:22
23 Q. Okay. And would a POSITA know that you can 10:22
24 place regulators on the DIMM board? 10:22
25 MR. CHANDLER: Objection. Form. 10:23

1 THE WITNESS: If they were nonstandard DIMM 10:23
2 boards -- if they were standard unbuffered DDR2 or 10:23
3 DDR3 DIMM boards, then they would not have 10:23
4 regulators. But certainly, a person of ordinary 10:23
5 skill would know that one could have a memory DIMM 10:23
6 with on-board regulators at that time. A person of 10:23
7 ordinary skill would also know from Spiers that one 10:23
8 could put regulators on a PCI card. 10:23
9 BY MS. ZHONG: 10:23
10 Q. Okay. And so they know that there were two 10:23
11 options. So what would be the advantage of having 10:23
12 the VTT voltage be generated on the PCI card versus 10:23
13 be generated on the DIMM? 10:23
14 MR. CHANDLER: Object to form. 10:24
15 THE WITNESS: Well, presumably by the time 10:24
16 of the invention, a person of ordinary skill would 10:24
17 have known that the cheapest option would have 10:24
18 simply been to put SDRAM chips on the PCI card and 10:24
19 not to have a DIMM. 10:24
20 The motivation at that time in this 10:24
21 particular design to use a DIMM module for 190 would 10:24
22 probably be if it was a commodity existing module. 10:24
23 Since you're already designing board 144 for your 10:24
24 own purposes, that would be the logical place to 10:24
25 deviate from the standards and apply the teaching of 10:24

Page 244

1 Spiers because you're selecting all the components 10:24
2 anyway. 10:24
3 BY MS. ZHONG: 10:25
4 Q. If you have the DRAMs directly on the PCI 10:25
5 board, how do you have the 64-bit wide bus? 10:25
6 A. Well, a person of ordinary skill would 10:26
7 understand the 64-bit-wide bus is exemplary and 10:26
8 certainly not a requirement. 10:26
9 But if you chose to have a 64-bit-wide bus, 10:26
10 you would simply, for example, choose four 10:26
11 16-bit-wide SDRAM chips and operate them in 10:26
12 parallel, or two 32-bit-wide SDRAM chips and operate 10:26
13 them in parallel. 10:26
14 Q. Would it have the same capacity as if you 10:26
15 used modules instead? 10:26
16 A. You could certainly have a very small number 10:26
17 of DDR3 chips that would have the same capacity as 10:26
18 an SDR module or even four SDR modules. 10:27
19 Q. So you are assuming 190 is an SDR DRAM 10:27
20 module? 10:27
21 MR. CHANDLER: Objection. Form. 10:27
22 THE WITNESS: No. But if you want to talk 10:27
23 about the same capacity, you have to compare two 10:27
24 different things so that is just an example. 10:27
25 You could have DDR3 chips on a board that 10:27

1 have the same capacity as a DDR2 module -- a 10:27
2 collection of two DDR2 daughter board modules. It's 10:27
3 really just a matter of engineering convenience at 10:27
4 that point as to where you put the chips, whether 10:27
5 you put them on a separate board or whether you put 10:27
6 them on the PCI card. And it was very common to put 10:27
7 memory chips on a PCI card. Graphics cards did it 10:27
8 all the time. 10:27
9 BY MS. ZHONG: 10:27
10 Q. I'm just kind of confused. 10:27
11 Why do you have to compare the single DDR3 10:27
12 chip with a different generation of a DDR module? 10:28
13 A. Oh, it could be the same. So, yes, it's 10:28
14 certainly possible that you could have DDR modules 10:28
15 that have the same capacity as individual DDR chips, 10:28
16 or DDR3 modules that have the same capacity as 10:28
17 individual DDR chips. But at some point, you only 10:28
18 need sufficient capacity. You don't need the most 10:28
19 capacity that one could possibly have. 10:28
20 And once you've selected your NAND flash 10:28
21 capacity, in this particular design, it doesn't make 10:28
22 much sense to have more SDRAM capacity than NAND 10:28
23 flash capacity. So there's only two NAND flash 10:28
24 chips, so you don't need an unlimited amount of 10:28
25 SDRAM. You only need enough to supply the same 10:28

1 capacity as two NAND flash chips. 10:28

2 Q. Okay. So at the time of the invention, what 10:28

3 is the maximum NAND flash capacity? 10:28

4 A. I don't know. I would have to go back and 10:29

5 look it up. It changed from month to month at that 10:29

6 time. 10:29

7 Q. Do you know the range? 10:29

8 A. Not for that particular month, and it was 10:29

9 rapidly changing at the time. 10:29

10 Q. Just generally in 2007 and 2008, do you know 10:29

11 the range? 10:29

12 A. The changes over time were by factors of 10:29

13 two. So I would need to go look. I would not want 10:29

14 to try to recall 15 years ago what the maximum 10:29

15 capacity of a NAND chip was. And, again, you don't 10:29

16 need to use the maximum capacity in an embodiment of 10:29

17 Spiers. 10:29

18 Q. What would be an appropriate capacity for 10:29

19 Spiers then? 10:29

20 A. It depends how much information you need to 10:29

21 back up. It could be -- 10:29

22 Q. Okay. 10:29

23 A. -- it could be a couple megabytes. 10:29

24 Q. Is that pretty typical for, say, a 10:30

25 write-back cache size? 10:30

1 MR. CHANDLER: Objection. Form. 10:30
2 THE WITNESS: Well, again, the write-back 10:30
3 cache is separate. This is the backup device -- 10:30
4 BY MS. ZHONG:
5 Q. Okay. 10:30
6 A. Certainly -- again, it varied from year to 10:30
7 year, but certainly, there are places where one can 10:30
8 find a write-back cache of 2 to 4 megabytes that's 10:30
9 useful. 10:30
10 Q. 2 to 4 megabytes? 10:30
11 A. Yes. But also larger ones and smaller ones. 10:30
12 Q. Okay. What's the biggest that you're aware 10:30
13 of? 10:30
14 MR. CHANDLER: Objection. Form. 10:30
15 THE WITNESS: In 2007? 10:30
16 BY MS. ZHONG: 10:30
17 Q. Or around 2008, around that time period. 10:30
18 A. I don't recall. 10:31
19 Q. Is it order of magnitude higher -- 10:31
20 (Clarification requested by Reporter.) 10:31
21 BY MS. ZHONG: 10:31
22 Q. Is it orders of magnitude higher than 2 to 4 10:31
23 megabytes? 10:31
24 MR. CHANDLER: Objection. Form. 10:31
25 THE WITNESS: Yes. I'm sure there were 10:31

1 systems in existence that had write-back caches that 10:31
2 were orders of magnitude larger than 2 to 4 10:31
3 megabytes. 10:31
4 BY MS. ZHONG: 10:31
5 Q. And for which applications are those? 10:31
6 MR. CHANDLER: Objection. Form. 10:32
7 THE WITNESS: They could have been for super 10:32
8 computing systems. They could have been for 10:32
9 enterprise level storage systems. 10:32
10 BY MS. ZHONG: 10:32
11 Q. What is a suitable backup device size? 10:33
12 A. It depends on the application. There are 10:33
13 certainly systems where one has a very small amount 10:33
14 of critical data that one needs to back up in case 10:33
15 of a failure, and there are other systems that have 10:33
16 very large amounts of backup -- of critical data 10:33
17 that needs to be backed up. 10:33
18 Q. For Spiers' storage application. 10:33
19 A. It would vary from embodiment to embodiment. 10:33
20 There is nothing about Spiers that ties it to any 10:33
21 particular size. It's applicable across a wide 10:33
22 range of sizes. 10:33
23 Q. And what would be the size range be? 10:33
24 MR. CHANDLER: Objection. Form. 10:34
25 THE WITNESS: I mean, Spiers is a perfectly 10:34

1 rational solution if you have 1 kilobyte of critical 10:34
2 data and it's a perfectly rational solution if you 10:34
3 have 1 gigabyte of critical data, and over time, 10:34
4 perhaps more. 10:34
5 MS. ZHONG: Let's take a break. 10:34
6 MR. CHANDLER: Okay. Actually, hold on, 10:34
7 before we take a break, I did have a chance to look 10:34
8 at Exhibit 2102. And so I will just lodge my 10:34
9 objections, which are lack of relevance, lack of 10:35
10 authenticity and hearsay. 10:35
11 And with that, we can take a break. 10:35
12 DEPOSITION REPORTER: Off the record, 10:35
13 Miss Zhong. 10:35
14 (Off the record.) 10:35
15 BY MS. ZHONG: 10:54
16 Q. Dr. Wolfe, can you pull up Exhibit 1038 10:54
17 again. 10:54
18 A. Okay. 10:54
19 Q. So for Exhibit 1038, is any signal sent from 10:54
20 the voltage detection circuit to the charge pump? 10:54
21 MR. CHANDLER: Object to form. 10:54
22 THE WITNESS: Not directly. 10:55
23 BY MS. ZHONG: 10:55
24 Q. So the busy signal is not sent to the charge 10:55
25 pump from the voltage detection circuit; correct? 10:55

1 MR. CHANDLER: Objection to form. 10:55

2 THE WITNESS: Not directly. The busy signal 10:55

3 goes to the host system, the host system then sends 10:55

4 signals out to the various components on element 30. 10:55

5 BY MS. ZHONG: 10:55

6 Q. How does the charge pump operate differently 10:55

7 in response to the busy signal? 10:56

8 A. The charge pump only operates differently to 10:56

9 the extent that the host system cuts the power. 10:56

10 Q. So in the overvoltage situation, how does 10:56

11 the charge pump operate differently? 10:56

12 A. The charge pump gets the power signal from 10:56

13 the host, so if the power signal from the host is 10:56

14 cut off because an anomaly was detected and reported 10:56

15 to the host through ready-busy, then the charge pump 10:56

16 begins to shut down. 10:56

17 Q. So you're saying that if a busy signal is 10:56

18 sent to the host, the V gain might be cut off and 10:56

19 that's how the operation of the charge pump might be 10:57

20 affected? 10:57

21 A. Yes. That appears to be part of what's 10:57

22 claimed in Claim 1. It is described as a signal 10:57

23 that's provided to the controller. 10:57

24 Q. Which Claim 1 are you referring to? 10:57

25 A. Claim 1 of Hajeck. 10:57

1 Q. Uh-huh. 10:57

2 A. The charge pump limitation. 10:57

3 Q. So you're referring to the power signal? 10:57

4 A. Yes. 10:57

5 Q. And where in Exhibit 1038 is it indicated 10:57

6 that in response to the busy signal, the host would 10:58

7 remove the V-in signal? 10:58

8 A. I think you have to kind of put the whole 10:58

9 spec together. It says that the ready-busy signal 10:58

10 is what indicates that a power anomaly has been 10:58

11 detected, and it says that the power signal is what 10:58

12 causes a shutdown of the disk drive 10:58

13 controller and -- 10:58

14 Q. Sorry. Can you tell me like the line number 10:58

15 or the column and line number that you're reading 10:58

16 from?

17 A. Well, I can start to look and put things 10:58

18 together. But like I said, this is an understanding 10:59

19 of the entirety of the description specification. 10:59

20 Q. Okay. Because if you look at column 3, line 10:59

21 62, starting from line 62 and 63, it says: 10:59

22 "Upon detecting the anomaly, the 10:59

23 voltage detection circuit 48 10:59

24 generates a busy signal on line 36, 10:59

25 causing the host to refrain from 10:59

1 writing or reading data to/from the 10:59
2 memory subsystem." 10:59
3 It doesn't really say what the host does 10:59
4 with the power input signal. 10:59
5 A. Well, that's why I wouldn't try to 11:00
6 understand it by reading individual sentences 11:00
7 independent of each other. 11:00
8 If you read the entirety of the description, 11:00
9 what it says is that there's a power detection 11:00
10 circuit, that power detections are reported to the 11:00
11 host. It also says there is a power signal, that 11:00
12 that power signal goes to the charge pump from the 11:00
13 host and can initiate a backup and shutdown process, 11:00
14 and it also explains that backups and shutdowns 11:00
15 happen in response to anomalies. 11:00
16 So if you put those three sets of 11:00
17 descriptions together, it's the least obvious, and 11:00
18 really only makes sense, that those three things are 11:00
19 working together, and that it's the ready-busy 11:00
20 signal that reports to the host, the host will 11:00
21 realize that there's a power anomaly, it will stop 11:00
22 writing new data, and it will cut the power to 11:00
23 initiate the power-down sequence. 11:00
24 Otherwise, how would this system know that a 11:01
25 power-down sequence should happen? We're given one 11:01

1 mechanism that goes through the charge pump that's 11:01
2 described as having that functionality. 11:01
3 Q. Well, there's address data control 11:01
4 information exchanged between the host system disk 11:02
5 drive controller directly; right? So it doesn't 11:02
6 have to go through the charge pump. 11:02
7 A. That's true. Not all of the information has 11:02
8 to go through the charge pump, but we are told that 11:02
9 the -- that the charge pump is provided with a 11:02
10 signal so that the charge pump acts as the backup 11:02
11 power supply when power from the host is 11:02
12 interrupted. So it is signaled. 11:02
13 Q. But what I am saying is that the shutdown 11:02
14 sequence doesn't have to have anything to do with a 11:03
15 power signal. It could just be directly under the 11:03
16 control of the host system. 11:03
17 A. It is possible that in some embodiments the 11:03
18 host tells the disk drive controller to perform the 11:03
19 shutdown sequence in response to the ready-busy 11:03
20 signal. 11:03
21 Q. Does Harris detect overvoltage? 11:03
22 A. I'm sorry. I didn't understand the 11:05
23 question. 11:05
24 Q. Does Harris detect overvoltage at the power 11:05
25 input side? 11:05

1 A. I don't think Harris alone teaches it, but 11:05
2 Harris in combination with Amidi teaches it. 11:06
3 Q. Does Amidi teach overvoltage detection for 11:06
4 input voltage? 11:07
5 A. Yes. It uses the system supply as an input 11:07
6 to the voltage supervisory block 665 and that can 11:08
7 detect an overvoltage. 11:08
8 Q. It can, but does it actually detect it? It 11:08
9 only talks about undervoltage detection; correct? 11:08
10 MR. CHANDLER: Objection to form. 11:08
11 THE WITNESS: Let me take a quick look. 11:08
12 BY MS. ZHONG: 11:08
13 Q. Look at Figure 14, for example. 11:08
14 A. It certainly teaches a circuit that 11:10
15 determines whether or not a power input voltage 11:10
16 is -- has an amplitude that is greater than a first 11:10
17 threshold. 11:10
18 Q. In Figure 14, it is only examining whether 11:10
19 the input voltage is below the 3.0-volt threshold; 11:11
20 right? 11:11
21 A. No. It's only acting in a particular way if 11:11
22 it's below a 3.0-volt threshold. It has got two 11:11
23 paths, a yes and a no. One is if it's greater than 11:11
24 or equal to 3.0 volts, and one is if it's less than 11:11
25 3.0 volts. 11:11

1 Q. And the 3.0 volt is below 3.3 volt; right? 11:11

2 A. Yeah. Are we talking about the claims? 11:11

3 Because I don't see the claims saying that the first 11:11

4 threshold has to be greater than or less than some 11:11

5 particular value. 11:11

6 What it says is it has to determine whether 11:11

7 it's greater than or less than, depending on which 11:11

8 claim, a threshold voltage. And this particular 11:12

9 circuit distinguishes the two. It determines 11:12

10 whether it is greater than a threshold voltage or if 11:12

11 it's less than a threshold voltage. 11:12

12 Q. Does it determine -- well, if it's less than 11:12

13 3.0 volt -- if the answer is no, it could be because 11:12

14 it's equal to 3.0 volt; correct? 11:12

15 A. Not really. There's no -- there's no such 11:12

16 thing in the real world as two things being 11:12

17 exactly -- two voltages being exactly equal. So in 11:12

18 the real world, it's either going to be greater than 11:12

19 or less than. 11:12

20 Q. But in this particular one, it is examining 11:12

21 whether the voltage is below a threshold that's 11:13

22 below the nominal value for the power supply; is 11:13

23 that correct? 11:13

24 MR. CHANDLER: Objection to form. 11:13

25 THE WITNESS: Yes. But it's also 11:13

1 determining if it is greater than the threshold so 11:13
2 that it can maintain operation. 11:13
3 BY MS. ZHONG: 11:13
4 Q. And when it detects that it's not below 3.0 11:13
5 volt, does -- Amidi proceeds as before; right? 11:13
6 There is no change in the operating state; correct? 11:13
7 A. In Amidi, as literally expressed, that is 11:13
8 true. Although, clearly, it's a trivial 11:13
9 modification and well within the knowledge of a 11:14
10 person of ordinary skill in the art to respond when 11:14
11 the voltage is too high as it is to respond when the 11:14
12 voltage is too low. 11:14
13 Q. Okay. And in the way you are reading the 11:14
14 claim, when it's detected that the voltage is not 11:14
15 below 3.0 volt, Amidi does not switch to backup 11:14
16 power; is that correct? 11:14
17 A. Are we talking about Claim 5? 11:14
18 Q. I'm just ask -- I'm asking you questions 11:14
19 regarding Amidi. I want to know the facts. I know 11:14
20 that we cannot agree on the ultimate conclusion, so 11:14
21 let's get the facts right. 11:14
22 A. I'm sorry, you asked me a question about the 11:14
23 claim, and I'm asking you which claim. 11:14
24 Q. I'm not asking about the claim. I'm asking 11:14
25 you how Amidi operates. 11:14

1 A. Well, I'm sorry, I must have misheard the 11:15
2 question because I thought you said "the claim." 11:15
3 MR. CHANDLER: I object to the form of 11:15
4 the question. I'm a little unclear what the 11:15
5 question is now. 11:15
6 BY MS. ZHONG: 11:15
7 Q. Now, when Amidi detects that its supply 11:15
8 voltage is not below 3.0 volt, Amidi does not switch 11:15
9 to backup power; is that correct? 11:15
10 A. That is correct with respect to one 11:16
11 embodiment. 11:16
12 Q. Now, does Amidi disclose anywhere that if 11:16
13 its supply voltage is suffering from input voltage 11:16
14 overvoltage, that it will switch to the backup 11:16
15 power? 11:16
16 A. I don't believe so, not in Amidi alone, 11:16
17 although it does give a general disclosure that it 11:17
18 checks for proper power levels. 11:17
19 Q. Is power level the same as voltage level? 11:17
20 A. In this context, I believe so. 11:17
21 Q. Isn't the power depends on both current and 11:17
22 voltage? 11:17
23 A. From a physics perspective, but I don't 11:17
24 think that's how the language is being used in that 11:17
25 particular part of Amidi. 11:17

1 Q. Okay. And when -- in a PCI card -- let me 11:17
2 withdraw and ask. 11:17
3 In Spiers, does Spiers detect when a voltage 11:17
4 is above the 5 volt threshold? 11:18
5 A. It simply tells us that there's a 5 volt PCI 11:18
6 detector, and then it says that that responds to 11:18
7 power failures, but it doesn't define specifically 11:18
8 what it means by a power failure. 11:19
9 Q. And what is a POSITA's understanding of the 11:19
10 term "power failure"? 11:19
11 A. It could be -- I mean, the actual language 11:19
12 here is "power failure, power interruption or other 11:19
13 failure." 11:19
14 So I think in that context, you would read 11:19
15 it to be broader than a power interruption. So it 11:19
16 would presumably mean any failure to maintain the 11:19
17 proper voltage levels or the proper current levels. 11:19
18 Q. What is a "power interruption"? 11:19
19 A. That's when the power supply goes away. 11:19
20 Q. How does the PCI specification specify that 11:19
21 the input voltage be provided within a specified 11:20
22 range? 11:20
23 A. The input voltage to what? 11:20
24 Q. To the PCI bus. To the interface. 11:20
25 MR. CHANDLER: Objection to form. 11:20

1 THE WITNESS: I'm not sure what you are 11:20
2 asking about. 11:20
3 BY MS. ZHONG: 11:20
4 Q. Does the PCI local bus specification in 11:20
5 Exhibit 2031 keep detecting input voltage, 11:21
6 overvoltage or undervoltage? 11:21
7 A. That's specified in a different document, 11:21
8 which I don't happen to have in front me, the PCI 11:21
9 bus power management interface. 11:21
10 Q. You did not cite that in your declaration; 11:22
11 correct? 11:22
12 A. Correct. 11:22
13 Q. And according to your understanding of that 11:22
14 uncited document, is there voltage detection on the 11:22
15 PCI card? 11:22
16 A. I don't recall whether that particular 11:22
17 document teaches it or not, but the references that 11:22
18 I cited, in combination, teach it. 11:22
19 Q. Now, can you go to page 121 of Exhibit 1031. 11:22
20 A. Yes. 11:23
21 Q. What is shown here in Figure 4-3? 11:23
22 A. These are the AC properties of non-power 11:23
23 signals on PCI bus in particular with respect to 11:23
24 5 volt signaling. 11:23
25 Q. So those are not for the power supplies, 11:23

Page 260

1	they're for the signaling rail?	11:23
2	A. Correct.	11:23
3	Q. So they have nothing to do with detecting	11:23
4	overvoltage or detecting undervoltage on the power	11:23
5	rail.	11:23
6	MR. CHANDLER: Objection. Form.	11:24
7	THE WITNESS: Not directly.	11:24
8	BY MS. ZHONG:	11:24
9	Q. And how indirectly?	11:24
10	A. Somebody might be able to build a detector	11:24
11	that infers that if there is an overvoltage on the	11:24
12	signals, there is an overvoltage on the power, but	11:24
13	it would make more sense to simply directly measure	11:24
14	the power.	11:24
15	Q. Okay. So Figure 4-3 does not indicate	11:24
16	measuring the overvoltage and undervoltage on the	11:24
17	power rail?	11:24
18	A. Correct.	11:24
19	Q. And go to 122, note 1, the first sentence.	11:25
20	What does it mean, "This specification	11:25
21	should be guaranteed by design"?	11:25
22	A. I believe it simply means that you should	11:25
23	design your circuits to always support this portion	11:25
24	of the specification.	11:25
25	Q. Is that also true for the power supply for	11:25

Page 261

1 any -- for the PCI card, the designers should, 11:25
2 through design, guarantee that the 5 volt and 11:26
3 3.3 volt power rails be within the specified voltage 11:26
4 range? 11:26
5 A. This note is specific to the IPU. It 11:26
6 doesn't say anything about those other systems. I 11:26
7 mean, there are hundreds of pages of specifications 11:26
8 here. If the -- the power doesn't necessarily -- 11:26
9 the power is supplied by the host computer, and it 11:26
10 doesn't necessarily have to be always within range 11:26
11 as long as the proper communications take place with 11:26
12 the PCI card. 11:26
13 Q. So a POSITA would know that the voltage can 11:27
14 be outside the specification and proper 11:27
15 communication can still take place between the PCI 11:27
16 card and the host system. 11:27
17 MR. CHANDLER: Object to form. 11:27
18 THE WITNESS: Not necessarily. Systems can 11:27
19 fail in various ways. In a system that has got a 11:27
20 power error, lots of different things can happen, 11:27
21 and it's up to the PCI card designer to decide which 11:27
22 of those they want to respond to and in which ways. 11:27
23 BY MS. ZHONG: 11:27
24 Q. Can you pull up Exhibit 1063. 11:28
25 A. Yes. 11:29

1 Q. What is this? 11:29

2 A. This is an exemplary PCI power volt 11:29

3 detection chip that was known at the time of the 11:30

4 invention. 11:30

5 Q. So is it used on the host system or on the 11:30

6 PCI card? 11:30

7 A. It can be used on either. 11:30

8 Q. What does it mean by "all boldface limits 11:30

9 are guaranteed for certain operating conditions"? 11:30

10 MR. CHANDLER: I didn't hear you. Are you 11:30

11 reading from a document? 11:30

12 MS. ZHONG: Yes. On page 2 under DC 11:30

13 electrical characteristics and AC electrical 11:31

14 characteristics. 11:31

15 THE WITNESS: It means that all the numbers 11:31

16 on this page that are shown in boldface are 11:31

17 specifications that have been characterized at a 11:31

18 junction temperature between zero and 70c, at a 11:31

19 nominal power of 5 volts, with a pull-up resistor of 11:31

20 4.7 kilohms and an external capacitor of .0.1 11:31

21 microfarads. 11:31

22 BY MS. ZHONG: 11:31

23 Q. So basically it's a suggestion that if you 11:31

24 want to design a board, you should use similar 11:31

25 operating conditions and similar passive components? 11:31

1 MR. CHANDLER: Objection. Form. 11:32

2 THE WITNESS: Not necessarily. It means if 11:32

3 you want to rely on these particular specifications, 11:32

4 then you should design for a typical temperature 11:32

5 range -- for the same temperature range and using 11:32

6 the same range of components, otherwise, you may 11:32

7 need to do some additional research to determine 11:32

8 what specifications would be met. 11:32

9 But those are very ordinary specifications. 11:32

10 That's the normal commercial temperature range and a 11:32

11 normal power supply range for this chip. 11:32

12 BY MS. ZHONG: 11:32

13 Q. So if for a given condition, you know a 11:32

14 priority what the minimum and maximum of the supply 11:32

15 voltage would be -- never mind. Let me withdraw and 11:32

16 ask a different question. 11:33

17 What does the timing diagram shown on page 3 11:33

18 demonstrate? 11:33

19 A. It shows how certain characteristics that 11:33

20 are described on page 2 were measured and shows an 11:33

21 exemplary response time to overvoltage and 11:33

22 undervoltage conditions on the PCI power supply. 11:34

23 Q. And can you be able to state -- let's just 11:34

24 start with the 5 volt signal, the top one. 11:34

25 What characteristics are measured in the top 11:34

1 diagram? 11:34

2 A. These diagrams all work together. 11:35

3 Q. Okay. 11:35

4 A. They're not -- I don't think they can be 11:35

5 interpreted individually. But there are exemplary 11:35

6 overvoltage and undervoltage conditions shown in the 11:35

7 top graph. And then in the bottom graph, there are 11:35

8 the responses on the reset signal in that particular 11:35

9 case and the timing of those responses. 11:35

10 Q. Okay. So the top one is just showing the 11:35

11 time variants of different voltages on the 5 volt 11:35

12 signal rail; is that right? 11:35

13 A. In an exemplary situation, yes. 11:35

14 Q. And the second one is showing time variants 11:35

15 on the 3.3 volt signaling rail. 11:36

16 A. Again, for illustrative purposes only. 11:36

17 Q. Okay. And then the third one is with 11:36

18 respect to a parameter called MR. 11:36

19 And then the last one is showing how the 11:36

20 combination of the different conditions is going to 11:36

21 affect the reset value, whether it's going to be 11:36

22 reset or whether it's not going to be reset. 11:36

23 Is that right? 11:36

24 A. Yes. That signal is named "reset," but the 11:36

25 PCI card can use it for whatever it wants. It's 11:36

1 simply a detection. The MR is an indication of 11:36
2 perhaps resetting the entire computer, where the 11:36
3 reset pound signal is an indication of an over- or 11:36
4 undervoltage condition to a device on the PCI card, 11:37
5 which could be used for reset, or it could be used 11:37
6 for a power failure response of some other type. 11:37
7 Q. So is it detecting the 5 volt signaling rail 11:37
8 or is it detecting the 5 volt power rail? 11:37
9 A. In the exemplary applications on page 1, one 11:37
10 for the host system and one for the add-in card, 11:37
11 those are connected together. 11:37
12 Q. So they're sort of together and they are 11:37
13 measuring the same thing? 11:37
14 A. In the examples. They could be separated if 11:37
15 one chose to do so. 11:37
16 Q. What happens when the reset signal is sent 11:37
17 due to a fault -- detected fault condition? 11:38
18 A. It depends on how the person uses his chip 11:38
19 on the board. It could be used to reset a PCI card, 11:38
20 or it could be used to instruct to signal something 11:38
21 on the PCI card that a power failure has happened 11:38
22 and the device that has become aware of the -- of 11:38
23 the power anomaly can respond in whatever way is 11:38
24 appropriate for that particular device. 11:38
25 Q. Okay. So does the reset signal guarantee 11:39

1 compliance with the specification for the -- let me 11:39
2 withdraw and ask. 11:39
3 So does the reset signal guarantee 11:39
4 compliance with the PCI specification? 11:39
5 MR. CHANDLER: Objection. Form. 11:39
6 THE WITNESS: No. An engineer would have to 11:39
7 understand how to use this chip properly to 11:39
8 guarantee compliance. 11:39
9 BY MS. ZHONG: 11:39
10 Q. And what is shown on page 7? 11:39
11 A. There's a block diagram of the chip. 11:39
12 There's a truth table that essentially shows that 11:39
13 the reset is asserted when any type of power failure 11:40
14 or power anomaly is detected, and then there are 11:40
15 descriptions of the pins. 11:40
16 Q. So is the top comparator comparing the 11:40
17 5 volt signal or power rail against an overvoltage 11:40
18 threshold? 11:40
19 A. Yes. 11:40
20 Q. And the second one is comparing that 5 volt 11:40
21 rail against an undervoltage threshold? 11:40
22 A. Correct. 11:40
23 Q. Okay. If either -- if there is an 11:40
24 undervoltage or -- if there is an overvoltage or 11:40
25 undervoltage condition, then that will trigger the 11:40

Page 267

1 reset bar signal; is that right? 11:40

2 A. On this particular chip, that's correct. 11:40

3 Q. And the reset -- what will happen with the 11:40

4 reset, that's up to the engineer? 11:41

5 A. Correct. But there is a suggestion on 11:41

6 page 1 that it be connected to a device on board the 11:41

7 PCI card. 11:41

8 Q. What do you mean by "there is a suggestion 11:41

9 on page 1 that it be connected to a device on board 11:41

10 the PCI card"? 11:41

11 What device are you referring to? 11:41

12 A. It is simply referred to as a device on 11:41

13 board. It could be any device on the PCI card. 11:42

14 That's the choice of the engineer. 11:42

15 Q. So you mean like the signal can be sent to 11:42

16 any device on the PCI card? 11:42

17 A. Correct. Any or all. 11:42

18 Q. What does "pre-regulated" mean in Claim 16 11:42

19 of the '918 patent? 11:42

20 A. I think it simply means that the voltage 11:42

21 that is supplied as an input to the first, second, 11:43

22 third and fourth converters has already passed 11:43

23 through some type of a regulator and is being 11:43

24 controlled within some range. 11:43

25 Q. Okay. So all it means, it means that the 11:43

1 input to the buck converters and the conversion 11:43
2 circuit is a regulated voltage; correct? 11:43
3 A. Yes. 11:44
4 MR. CHANDLER: Objection. Form. 11:44
5 THE WITNESS: I mean, if you read it in 11:44
6 context, it has to be regulated on the memory 11:44
7 module. 11:44
8 BY MS. ZHONG: 11:44
9 Q. And where did you get that from, from the 11:44
10 claim language itself? 11:44
11 MR. CHANDLER: Object to form. 11:44
12 THE WITNESS: I think because it's part of 11:44
13 the memory module and because it's distinguished 11:45
14 from the power that comes into the memory module, so 11:45
15 this appears to be something different. 11:45
16 BY MS. ZHONG: 11:45
17 Q. Okay. So you are applying an understanding 11:45
18 that the preregulated voltage needs to be a voltage 11:45
19 that's generated on the motherboard -- on the memory 11:45
20 module; is that correct? 11:45
21 MR. CHANDLER: Objection. Form. 11:45
22 THE WITNESS: I looked at both situations. 11:45
23 I didn't -- I didn't make that a part of my -- I 11:45
24 didn't limit my analysis to that case. I looked at 11:45
25 whether it does or does not because it is a claim 11:46

1 construction issue, and that's a matter of law. 11:46

2 So I found it to be obvious whether it does 11:46

3 have to be regulated on the module or whether or not 11:46

4 it's broad enough to allow for regulation off the 11:46

5 module. 11:46

6 BY MS. ZHONG: 11:46

7 Q. Okay. So in the case of Harris, the 12-volt 11:46

8 power source is off the module; correct? 11:46

9 MR. CHANDLER: Objection. Form. 11:46

10 THE WITNESS: In the simplest 11:47

11 implementation, it is. And then what I explain 11:47

12 later in paragraph 489 and 490 is that it would also 11:47

13 be obvious to regulate it on the module in a way 11:47

14 that Amidi does. 11:47

15 BY MS. ZHONG: 11:47

16 Q. So Amidi's battery is only used in the 11:48

17 backup power when the normal voltage is not 11:48

18 available; is that right? 11:48

19 MR. CHANDLER: Objection. Form. 11:48

20 THE WITNESS: That's the only time that the 11:48

21 battery is used, but the regulation circuitry is used 11:49

22 whether or not the battery is being used. 11:49

23 BY MS. ZHONG: 11:49

24 Q. Why would Amidi be using the regulation 11:49

25 circuitry when the lithium ion battery is not used? 11:49

1 The system provides a 1.8-volt input already 11:49
2 in Amidi; right? 11:50
3 A. It does. But it also teaches that 11:50
4 preregulated voltages are provided to buck 11:50
5 converters. 11:50
6 BY MS. ZHONG: 11:51
7 Q. Is the output from a battery a regulated 11:51
8 voltage or an unregulated voltage? 11:51
9 A. It could be either. The direct output is an 11:51
10 unregulated voltage. But, for example, the 11:51
11 regulated one -- the regulated voltage from the 11:51
12 battery charger is provided to the DC-to-DC boost 11:51
13 regulator and the DC-to-DC buck boost regulator and 11:51
14 the DC-to-DC buck regulator. 11:51
15 Q. And is the output from a super cap a 11:51
16 regulated or unregulated voltage? 11:51
17 A. It's directly unregulated, but then it 11:52
18 gets -- could be passed through a regulator. 11:52
19 Q. Okay. Why would you convert a 12-volt 11:52
20 unregulated voltage to a 12-volt regulated voltage 11:52
21 in the case of Harris? 11:52
22 A. So that you could have tighter regulation 11:52
23 locally. If, for example, you wanted plus or minus 11:52
24 5 percent instead of plus or minus 15 percent, that 11:52
25 would be a reason. 11:52

1 Q. In the case of Harris, is there a reason to 11:52
2 have a tighter input voltage range? 11:53
3 A. Yeah. Because Harris tells us, I believe, 11:53
4 if I recall correctly -- let me go back and look. 11:53
5 Yeah, Harris tells us in some embodiments 11:53
6 the incoming voltage is unregulated, so that's why 11:53
7 you would want to regulate it on board. 11:53
8 Q. That is what I'm asking you. Why does it 11:53
9 matter? The buck converters has a huge input 11:53
10 voltage operating range, so a tighter control 11:53
11 doesn't really matter for it one way or the other. 11:53
12 MR. CHANDLER: Objection to form. 11:54
13 THE WITNESS: For the same reasons that 11:54
14 we've seen in some of the other references. If you 11:54
15 want to predetect a failure, detect a failure early, 11:54
16 you would look at a variance in a regulated voltage. 11:54
17 And you don't want to do that at the last stage 11:54
18 where it is supplying the voltage to your critical 11:54
19 components. You want to look at it at an earlier 11:54
20 stage. 11:54
21 BY MS. ZHONG: 11:54
22 Q. But you can do that equally well with a 15 11:54
23 percent unregulated 12 volts; right? Once it starts 11:54
24 to draw like 15 percent below 12 volts or 15 percent 11:54
25 above 12 volts, that should give you sufficient time 11:54

1 to react, isn't it? 11:54

2 A. Not necessarily. But in any case, Harris 11:55

3 teaches us that some of his embodiments have an 11:55

4 unregulated 12-volt supply, not the plus/minus 15. 11:55

5 So you would want to be able to work with those 11:55

6 embodiments as well. 11:55

7 Q. So the plus/minus 15 percent, that is not 11:55

8 the power tolerance range for the unregulated 11:55

9 voltage? 11:55

10 A. No. I believe that that's a tolerance range 11:55

11 for a regulated voltage with a wide tolerance. I 11:55

12 believe that's how it's described in Harris. 11:55

13 Q. So are you saying an unregulated voltage is 11:56

14 a voltage without any tolerance range? 11:56

15 A. No. An unregulated voltage is a voltage 11:56

16 that hasn't gone through a regulator. The tolerance 11:56

17 at that point is up to the user. That's why you 11:56

18 would want to have some kind of detection circuitry 11:56

19 or have an additional regulator on board. 11:56

20 Q. Can you look at paragraph 16 of Harris. 11:57

21 A. Okay. 11:58

22 Q. The second sentence it says: 11:58

23 "As set forth at block 202, voltage 11:58

24 is supplied to a memory board assembly 11:58

25 from an external source, e.g., an 11:58

1 unregulated source generating fairly 11:58
2 high voltages with a wide tolerance." 11:58
3 Do you see that sentence? 11:58
4 A. Yes. 11:58
5 Q. So what is the tolerance range for a 12 volt 11:58
6 unregulated source? 11:58
7 A. It would be system specific. 11:58
8 Q. And one wide tolerance is plus/minus 15 11:58
9 percent for example; right? 11:58
10 MR. CHANDLER: I didn't hear the beginning 11:59
11 of that. 11:59
12 BY MS. ZHONG: 11:59
13 Q. And one example of a tolerance is plus or 11:59
14 minus 15 percent; correct? 11:59
15 A. Plus or minus 15 percent is an example of a 11:59
16 tolerance, yes. 11:59
17 Q. Okay. So one example in Harris for the 11:59
18 tolerance for the unregulated voltage is 12 volts 11:59
19 with plus/minus 15 percent; is that correct? 11:59
20 A. No, I don't think it says that. He doesn't 11:59
21 give a tolerance for his exemplary unregulated 11:59
22 voltage. He does separately give a plus/minus 15 11:59
23 percent tolerance for a 12-volt power supply, but he 11:59
24 doesn't say that that one is unregulated. 11:59
25 Q. Okay.

1 A. It does teaches that his design is suitable 11:59
2 for a wide range of input power supplies, including 11:59
3 both regulated and unregulated. 11:59
4 Q. He does give an example for the term "wide 12:00
5 tolerance" as around plus/minus 15 percent; correct? 12:00
6 A. He does give that as an example for one 12:00
7 power supply, yes. 12:00
8 Q. And that power supply is also at 12 volts; 12:00
9 correct? 12:00
10 A. It is nominally. 12:00
11 Q. Can you take a look at '918, claim number 1. 12:00
12 A. Okay. 12:02
13 Q. Can you take a look at the last two 12:02
14 elements. 12:02
15 A. Okay. 12:02
16 Q. Do these two elements need to be satisfied 12:03
17 simultaneously? 12:03
18 A. Let's make sure we are on the same page 12:03
19 about what are the two elements. 12:03
20 Q. A plurality of SDRAM devices coupled to 12:03
21 the first regulated voltage and the really long 12:03
22 implementation afterwards. 12:03
23 A. I believe they do. 12:03
24 Q. And a device is not coupled to a particular 12:03
25 voltage if that voltage is set to zero; is that 12:03

1 correct? 12:03

2 MR. CHANDLER: Objection. Form. 12:03

3 THE WITNESS: Well, it would depend on the 12:03

4 circumstances, but I think it is still coupled. I 12:03

5 mean, this seems to me to be a structural 12:04

6 limitation, not one that -- not one that is the 12:04

7 result of a particular set of steps or operations. 12:04

8 BY MS. ZHONG: 12:04

9 Q. What is your understanding of the word 12:04

10 "coupled to"? Go ahead. 12:04

11 A. Coupled to can be interpreted differently by 12:04

12 lots of different courts and my experience based on 12:04

13 the totality of the context, but here to be coupled 12:04

14 to the first regulated voltage, I think means 12:05

15 directly or indirectly connected to the first 12:05

16 regulated voltage. 12:05

17 Q. And when you say -- 12:05

18 A. And the first regulated voltage is the 12:05

19 output of the first buck converter in this 12:05

20 particular claim. 12:05

21 Q. Okay. If the -- if there's a line to the 12:05

22 output of the first buck converter but, for example, 12:05

23 because the input to the buck converter is somehow 12:05

24 unavailable so there is no first regulated voltage 12:05

25 generated, is the SDRAM still coupled to that first 12:05

1 regulated voltage? 12:05

2 MR. CHANDLER: Objection. Form. 12:06

3 Incomplete. 12:06

4 THE WITNESS: My understanding is this is an 12:06

5 apparatus claim and that one can determine whether 12:06

6 or not this claim is being practiced by looking at a 12:06

7 memory module. So I mean, if that were the case, 12:06

8 then a memory module sitting on a table could never 12:06

9 infringe this claim. 12:06

10 I don't think that's what the patentee 12:06

11 intended, but again, that is a claim construction 12:06

12 issue that I'll leave to the courts. 12:06

13 BY MS. ZHONG: 12:06

14 Q. So if the SDRAM is coupled to the first 12:06

15 regulated voltage in one operating mode and the one 12:07

16 circuit is coupled to the second and the fourth 12:07

17 regulated voltage only in a second operating mode, 12:07

18 is this limitation still met? 12:07

19 MR. CHANDLER: Objection. Form. 12:07

20 Incomplete. 12:07

21 THE WITNESS: I don't know. I didn't have 12:07

22 to consider that as part of my analysis. 12:07

23 BY MS. ZHONG: 12:07

24 Q. So, for example, if in Spiers, if the 5 12:07

25 volts to 3.3 volt regulator is only operating in the 12:07

1 backup mode but not in the -- but not in the 12:07
2 normal -- like when there is normal PCI power supply 12:08
3 voltage, and if the 1.8 volt regulator is only 12:08
4 operating during the -- so let me withdraw and ask. 12:08
5 If in Spiers the 5 volt to 3.3 volt 12:08
6 regulator, if that one is only generating the 12:08
7 3.3 volt output in the backup mode, does that fact 12:08
8 affect our analysis as to whether Spiers rendered 12:09
9 obvious the claims? 12:09
10 MR. CHANDLER: Objection. Form and 12:09
11 incomplete. 12:09
12 THE WITNESS: No. One, that is not 12:09
13 consistent with my understanding of Spiers. But 12:09
14 even if it was, it would still be obvious to have 12:09
15 the regulator operate all the time. 12:09
16 BY MS. ZHONG: 12:09
17 Q. Okay. So let's say if the board decides 12:09
18 that there is no evidence to say that the 5 volt or 12:09
19 3.3 volt should be operating all the time, would 12:09
20 that -- the fact that the 5 volt to 3.3 volt is only 12:09
21 operating during the backup mode affect your 12:09
22 analysis? 12:09
23 MR. CHANDLER: Objection. Form. 12:09
24 THE WITNESS: In my opinion under my 12:10
25 analysis, it would be obvious to have a single 12:10

1 regulator provide the 3.3 volts all the time 12:10
2 whether -- so -- 12:10
3 BY MS. ZHONG: 12:10
4 Q. If that's -- 12:10
5 A. -- that's not a portion of my analysis. 12:10
6 If it's not, I think it's still coupled 12:10
7 because there would be two converters that would be 12:10
8 connected to the same wire. I don't see any 12:10
9 disclosure of a -- yeah, they would still be 12:10
10 coupled. They would still be directly or indirectly 12:10
11 connected. 12:10
12 Q. So "coupled" just means that as long as the 12:10
13 wiring is in existence between the voltage rail and 12:10
14 the component? 12:11
15 MR. CHANDLER: Objection. Form. 12:11
16 THE WITNESS: Again, that's a complex issue 12:11
17 that the courts struggle with and this court would 12:11
18 have to decide, but I think that that's the 12:11
19 approach -- that's one of the approaches that I 12:11
20 would use. 12:11
21 As I said, my actual opinion is that it 12:11
22 would be obvious to use the same 3.3 regulator all 12:11
23 the time, in which case it would clearly be coupled 12:11
24 under I think any construction that's reasonable. 12:11
25 / / / 12:11

1 BY MS. ZHONG: 12:11

2 Q. Why would it be obvious to use the 5 volt to 12:11

3 3.3 volt regulator all the time instead of using the 12:12

4 3.3 volt power supply? 12:12

5 A. Because it is difficult to enact multiple 12:12

6 regulator outputs together without some type of a 12:12

7 switch. There's no switch that's illustrated here 12:12

8 because there is ample 5 volt power being provided. 12:12

9 And because, as we discussed before, it is 12:12

10 the 5 volt supply that's being monitored so, 12:12

11 therefore, if I'm going to monitor the 5 volt 12:12

12 supply, I would want to monitor the supply that is 12:12

13 supplying power to my system. That's a much more 12:12

14 sensible approach than monitoring a different supply 12:12

15 than is supplying power to my system. 12:12

16 So if I'm going to monitor 5 volts with a 12:12

17 5 volt PCI detector, I would want to power my system 12:12

18 from the 5 volts from the PCI so that I am 12:13

19 monitoring the thing that I'm using. 12:13

20 Q. But wouldn't it also make sense you detect 12:13

21 the 5 volts because if the 5 volts is dropping, the 12:13

22 3.3 is probably not operating correctly either? 12:13

23 MR. CHANDLER: Objection. Form. 12:13

24 BY MS. ZHONG: 12:13

25 Q. Since it is all coming from the host system. 12:13

1 A. That's true. But if the failure is in the 12:13
2 5.5-volt power system if, for example, something is 12:13
3 shorting 5 volts or something like that, I would 12:13
4 want to detect that. 12:13

5 So rather than monitoring something that 12:13
6 might be correlated, I would rather monitor the 12:13
7 thing that I'm actually using. 12:13

8 And, again, all the indications in Spiers 12:13
9 are that that 3.3 volts comes from the 5 volt to 3.3 12:13
10 regulator. There is nothing to dissuade me from 12:13
11 that. 12:14

12 Q. Aside from like he does not say that; right? 12:14

13 A. Well, but he certainly suggests it. Again, 12:14
14 it's also not clear how the diode would work as a -- 12:14
15 as a carryover switching device unless that were the 12:14
16 case. Everything that he says is consistent with 12:14
17 that and would lead one to that conclusion. 12:14

18 Q. But for the diode to switch, all you need is 12:14
19 a 5 volt not necessarily power rail, but some kind 12:14
20 of signaling indicating what the voltage level is; 12:14
21 right? 12:14

22 A. Signaling to what? 12:14

23 Q. What do you mean by "signaling to what"? 12:14

24 A. Well, you said all you need is some kind of 12:14
25 signaling. Obviously, you need a specific kind of 12:14

1 signaling and I don't see it here, and I -- you 12:14
2 can't provide the signal to a diode to tell it to 12:15
3 switch because the diode doesn't work that way. 12:15
4 Q. A voltage signal? 12:15
5 A. How would the voltage signal cause the diode 12:15
6 to begin to conduct? 12:15
7 Q. But isn't the diode responding to a 12:15
8 particular voltage level? 12:15
9 A. Yes, it's responding to the voltage level at 12:15
10 the input to the 5 volt regulator and at the output 12:15
11 to the super cap. And that's why the input to the 12:15
12 5 volt regulator needs to be the 5 volt system power 12:15
13 so that it can respond to the differential between 12:15
14 those two things. 12:15
15 MR. CHANDLER: Should we think about lunch? 12:16
16 MS. ZHONG: We can go off the record. 12:16
17 (Lunch recess.) 12:16
18 BY MS. ZHONG: 13:00
19 Q. Dr. Wolfe, what is an "S3 state"? 13:00
20 A. I'm sorry. I didn't hear the whole 13:00
21 question. 13:00
22 Q. What is an "S3 state"? 13:00
23 A. In a traditional personal computer or an 13:01
24 Intel-based server, an S3 state is defined by a 13:01
25 standard, I think it's called ACPI, and the S3 is 13:01

1 what we commonly call a "sleep state," where the 13:01
2 main memory DRAM is placed into a self-refresh mode 13:01
3 and most of the rest of the computer system is 13:01
4 powered off so that you can go into a very low power 13:01
5 mode for maybe a couple of days or more, but then 13:01
6 very quickly recover back to a full operating state. 13:01
7 Q. Okay. So it's the host that determines 13:02
8 whether the memory module should be placed into -- 13:02
9 the DRAM on the memory module should be placed into 13:02
10 the self-refresh mode or not; is that correct? 13:02
11 MR. CHANDLER: Objection. Form. 13:02
12 THE WITNESS: In the simplest systems where 13:02
13 you would have a JEDEC-compliant memory module 13:02
14 connected to a host, that would be true, but that 13:02
15 doesn't always have to be true for every memory 13:02
16 module in the system. 13:02
17 BY MS. ZHONG: 13:02
18 Q. So for a standard-compliant FB-DIMM, the S3 13:02
19 state is entered into -- determined by the host, not 13:02
20 by the memory module itself. Fair? 13:02
21 MR. CHANDLER: Objection to form. 13:02
22 THE WITNESS: It's always determined by 13:03
23 something other than the memory module. If its 13:03
24 memory module is connected to some other memory 13:03
25 controller other than the host, then that can make 13:03

1 the decision. If the memory module is connected 13:03
2 directly to the host, then it would normally be the 13:03
3 host that indicates S3 mode. 13:03
4 BY MS. ZHONG: 13:03
5 Q. Okay. So whether the S3 mode is -- whether 13:03
6 the S3 mode affects a particular DRAM is really 13:03
7 determined by the memory module that controls that 13:03
8 particular DRAM; is that right? 13:03
9 MR. CHANDLER: Objection to form. 13:03
10 THE WITNESS: No. It's controlled by a 13:03
11 processor somewhere. It may initially be indicated 13:03
12 by a person or something else. So there's a 13:03
13 sequence of events. 13:03
14 So, for example, it could be a low battery 13:03
15 that indicates to a host that it's time to enter S3 13:04
16 mode. Then the host would then communicate that to 13:04
17 the various devices in the computer, including the 13:04
18 host-based memory, or it could be that the user 13:04
19 selects it. 13:04
20 There's always some control device that's 13:04
21 involved in communicating that information, but it 13:04
22 can use various criteria to decide when to do it. 13:04
23 The memory itself would not put itself into a 13:04
24 self-refresh mode. It would be told to put itself 13:04
25 into self-refresh mode. 13:04

1	/ / /	13:04
2	BY MS. ZHONG:	13:04
3	Q. And in FB-DIMM, according to the JEDEC	13:04
4	standard, there are certain S3 recovery	13:04
5	configuration registers; is that correct?	13:05
6	A. I'm not familiar with that off the top of my	13:05
7	head. If you can point me to something, I would be	13:05
8	happy to look at it.	13:05
9	Q. Exhibit 1027, page 25.	13:05
10	MR. CHANDLER: Give me a minute.	13:05
11	THE WITNESS: Yes. I see those.	13:05
12	BY MS. ZHONG:	13:05
13	Q. Are they -- where are they located?	13:05
14	A. I'd have to track each one down to be sure,	13:05
15	but generally those are CSRs, and CSRs on an	13:06
16	FB-DIMM, I believe, are primarily in the AMB.	13:06
17	Q. Okay. What are "CSRs"?	13:06
18	A. What does that stand for? I don't recall	13:06
19	the acronym right now. I think they are like	13:06
20	command and status registers or something like that.	13:07
21	Let's see if it's in the table here. I don't see a	13:07
22	definition in this document.	13:07
23	Q. And it says "the following CSR should be	13:07
24	stored in non-volatile memory."	13:07
25	And where is that non-volatile memory	13:07

1 located? 13:07

2 A. It doesn't matter from the perspective of 13:07

3 the standard, as long as you preserve those values 13:07

4 and can restore them when S3 mode is exited. 13:07

5 Q. And so they don't have to be on the AMB? 13:07

6 They could be on some other non-volatile memories on 13:07

7 the DIMM? 13:07

8 A. I believe so. It would still be standard 13:07

9 compliant, yes, or even off the DIMM, as long as you 13:08

10 can save them and restore them. 13:08

11 Q. Okay. So in 3.7.3, when it says, "The 13:08

12 following CSRs should be stored in non-volatile 13:08

13 memory," that non-volatile memory doesn't refer to a 13:08

14 memory space in the AMB. 13:08

15 MR. CHANDLER: Objection. Form. 13:08

16 THE WITNESS: It could, but I don't think 13:08

17 that the standard requires that it be in the AMB. 13:08

18 BY MS. ZHONG: 13:08

19 Q. And are control status register values

20 considered to be configuration information? 13:09

21 MR. CHANDLER: Objection to form. 13:09

22 THE WITNESS: It would depend on the 13:09

23 particular register. A status register might not be 13:09

24 configuration information. It would depend on each 13:09

25 individual register. We would have to look at the 13:09

1 definitions. 13:09

2 BY MS. ZHONG: 13:09

3 Q. What about the six recorded here? 13:09

4 A. I can't tell you based on those acronyms 13:09

5 alone. I would have to go look at the documentation 13:09

6 for each one. 13:09

7 Q. So you haven't done that analysis? 13:09

8 MR. CHANDLER: Objection. Form. 13:09

9 THE WITNESS: Not for the -- not 13:09

10 individually for each of those, no. 13:09

11 BY MS. ZHONG: 13:09

12 Q. But do you know which one could be a 13:09

13 configuration information? 13:09

14 A. Yes. The personality bytes certainly could 13:09

15 be configuration information. 13:10

16 Q. And what information is in the SPD part, the 13:10

17 personality bytes? 13:10

18 A. It's just general configuration information 13:10

19 about a particular module. 13:10

20 Q. And is it stored in the SPD? 13:10

21 A. That's up to the AMB implementer. So the 13:10

22 actual value is not stored there, but the backup 13:10

23 could be stored there. VRC is the DRAM controller 13:10

24 mode register. That would be configuration 13:10

25 information. 13:10

1 Q. Uh-huh. And the SPD personality bytes, it's 13:11
2 regarding the configuration information for the SPD? 13:11
3 MR. CHANDLER: Objection. Form. 13:11
4 THE WITNESS: Yes. That's typically -- I 13:11
5 believe that that's vendor-specific information. 13:11
6 BY MS. ZHONG: 13:11
7 Q. Vendor-specific information for SPD? 13:11
8 A. Defining what -- yes. About things that 13:11
9 could be stored in the SPD, yes. 13:11
10 Q. What I want to know is what kind of 13:11
11 information are those bits? Are they generally 13:11
12 information related to the FB-DIMMs, or are they 13:11
13 information related to SPD? 13:12
14 MR. CHANDLER: Objection. Form. 13:12
15 THE WITNESS: Well, the SPD would be part of 13:12
16 the FB-DIMMs, but we would have to look in the ACPI 13:12
17 specification version 2.0C to see the actual 13:12
18 definitions of those things. 13:12
19 BY MS. ZHONG: 13:12
20 Q. Okay. You did not -- 13:12
21 (Clarification requested by Reporter.) 13:12
22 BY MS. ZHONG: 13:12
23 Q. And you did not cite ACPI version 2.0C; is 13:12
24 that right? 13:12
25 A. Correct. The DRC is sufficient to establish 13:12

1 that there is configuration information in those 13:12
2 registers. 13:12

3 Q. And what information is usually stored in 13:13
4 the SPD? 13:13

5 A. There is a big table that describes it all, 13:13
6 but it varies from DIMM to DIMM. Typically, 13:13
7 information about timing, information about 13:13
8 capacity, but we would have to look at the SPD spec. 13:13
9 There can be dozens of things in there. 13:13

10 Q. Does the host need to read what's stored in 13:13
11 the SPD first before it can control the DIMMs 13:13
12 properly? 13:13

13 A. That depends on the host. That depends on 13:13
14 the host and the system. There are lots of systems 13:13
15 that will use a default configuration to talk to 13:13
16 the -- to memory DIMMs and then consult the SPD, 13:13
17 perhaps define other possible configurations. That 13:14
18 would not be unusual. 13:14

19 But it really just depends on how the 13:14
20 particular host is configured. The SPD provides 13:14
21 information, but the host is not compelled to use 13:14
22 that information. 13:14

23 Q. Okay. An SPD communicates with the host 13:14
24 through the so-called I2C bus; is that correct? 13:14

25 A. Correct. 13:14

1 Q. And does it communicate with the AMB through 13:14
2 the I2C bus as well? 13:14

3 A. I don't see -- let me look. The AMB is on 13:14
4 the SM bus, but I don't know whether or not they 13:15
5 directly communicate or not. 13:15

6 Q. And "SM bus" is another word for I2C? 13:15

7 A. No. But SM bus is the bus that uses I2C 13:15
8 that would be used to communicate with the SPD. 13:15

9 Q. Why don't you take a look at Exhibit 1028, 13:16
10 page 29 to 30, in particular the top of page 30. 13:16

11 A. I see that. 13:17

12 Q. So does that indicate to you whether AMB 13:17
13 communicates with the SPD via the I2C bus? 13:17

14 A. No. The host can communicate with the AMB, 13:17
15 and that may be the bus that's being used. So I 13:17
16 don't recall whether the host communicates with them 13:17
17 each separately or whether or not they can 13:17
18 communicate with each other. 13:17

19 Q. So the SPD bus interface signal doesn't mean 13:17
20 that it is the interface between the SPD and the 13:17
21 AMB? 13:17

22 A. Not necessarily. It may be the interface 13:17
23 between the SPD and the host and also be used to 13:17
24 communicate with the AMB. I don't see two 13:17
25 connections. 13:18

1 Q. It says Advanced Memory Buffer Pin 13:18
2 Description, though. 13:18
3 A. Right. In other words, I don't see two 13:18
4 different connections, and there is a host 13:18
5 connection that's described in JESD 82-20, and I 13:18
6 believe that that's the same one. 13:18
7 Q. And the description you just referred to, 13:18
8 where are they in Exhibit 1027? 13:18
9 A. On page 3, you can see it in the diagram on 13:18
10 the lower left. And where else? So if we look at 13:18
11 page 4 of the document -- let me see. I'm sorry, 13:19
12 it's page 5. It's wrong in the -- in the table of 13:19
13 contents. It's described as an "SM bus slave 13:19
14 interface" and usually to talk to an SPD chip, you 13:19
15 need a master interface. 13:19
16 Q. And in the section 1.4.3, "SMBus Slave 13:19
17 Interface" in Exhibit 1027, it says: 13:19
18 "The Advanced Memory Buffer supports 13:20
19 an SMBus interface to allow system 13:20
20 access to configuration registers 13:20
21 independent of the FBD link." 13:20
22 Do you see that sentence? 13:20
23 A. Yes. 13:20
24 Q. What is the FBD link? 13:20
25 A. The FBD link are the northbound and 13:20

1 southbound links. 13:20

2 Q. Okay. 13:20

3 A. I think it just stands for fully-buffered 13:20

4 DIMM link. And you can see that on page 6. 13:20

5 Q. And where on page 6? 13:20

6 A. It's called the SFBD Channel instead of the 13:20

7 FBD link here, but it's the same thing. 13:21

8 Q. Okay. 13:21

9 A. It says it's a combination of links. 13:21

10 Q. Okay. Do you know whether AMB includes 13:21

11 non-volatile memories? 13:21

12 MR. CHANDLER: Objection. Form. 13:21

13 THE WITNESS: I don't see any disclosure of 13:21

14 a requirement for that in 82-20. 13:21

15 BY MS. ZHONG: 13:21

16 Q. Are you aware of any AMB that includes 13:21

17 non-volatile memories? 13:21

18 A. I don't know one way or the other. Most 13:22

19 DIMMs would have non-volatile memory in an SPD 13:22

20 device, such as is shown in JEDEC standard 205. 13:22

21 Q. But SPD is not AMB; is that right? Those 13:22

22 are two separate components? 13:22

23 A. Those are two separate components -- 13:22

24 Q. Okay. 13:22

25 A. -- on the same DIMM. 13:22

1 Q. I'm asking you specifically whether you know 13:22
2 whether there is any non-volatile memory in the 13:22
3 advanced memory buffer. 13:22
4 MR. CHANDLER: Objection. Form. 13:22
5 THE WITNESS: I don't know whether or not 13:22
6 there is any inside, no. 13:22
7 BY MS. ZHONG: 13:22
8 Q. Are the registers volatile memory or 13:22
9 non-volatile memory? 13:23
10 A. What registers? 13:23
11 MR. CHANDLER: Objection. Form. 13:23
12 BY MS. ZHONG: 13:23
13 Q. Any registers in the AMB. 13:23
14 MR. CHANDLER: Objection. Form. 13:23
15 THE WITNESS: Ordinarily, they would be 13:23
16 volatile memory. 13:23
17 BY MS. ZHONG: 13:23
18 Q. What about the six that's specifically 13:23
19 called out in that section we were just at? 13:23
20 Page 29-ish? Is that... 25 actually. Yeah, on 13:23
21 page 25, there were six CSRs. 13:23
22 A. Those would almost certainly be volatile 13:23
23 memory. That's why you get the instruction to store 13:23
24 them in non-volatile memory or their values before 13:23
25 entering S3 mode and restoring them. There would be 13:23

Page 293

1 no need to store them and restore them if they were 13:24
2 not in volatile memory. 13:24
3 MS. ZHONG: Can we go off the record? 13:25
4 MR. CHANDLER: Sure. 13:25
5 DEPOSITION REPORTER: Off the record. 13:25
6 (Off the record.) 13:25
7 MS. ZHONG: I will pass the witness. 13:38
8 MR. CHANDLER: Okay. Let's go off the 13:39
9 record. I'll check my notes. 13:39
10 MS. ZHONG: Okay. 13:39
11 (Off the record.) 13:39
12 MR. CHANDLER: No questions, but I did want 14:00
13 to note that we would like an opportunity to review 14:00
14 the transcript, make any corrections if needed. So 14:00
15 to that end, if we could get the final transcript on 14:00
16 Tuesday from yesterday, and then the final 14:00
17 transcript from today, I think we said Wednesday, 14:00
18 the 22nd. 14:00
19 And with that, the deposition is concluded. 14:00
20 MS. ZHONG: Okay. Thank you, Dr. Wolfe. 14:00
21 THE WITNESS: Thank you. 14:00
22 (Ending time: 2:00 p.m.)
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I, ANDREW WOLFE, Ph.D., do hereby declare under penalty of perjury that I have read the foregoing transcript; that I have made corrections as appear noted, in ink, initialed by me, or attached hereto; that my testimony as contained herein, as corrected, is true and correct.

EXECUTED this ____ day of _____,
2023, at _____, - _____.
(City) (State)

ANDREW WOLFE, Ph.D.

1 I, JANIS JENNINGS, CSR No. 3942, Certified
2 Shorthand Reporter, certify:

3 That the foregoing proceedings were taken
4 before me at the time and place therein set forth, at
5 which time the witness was duly sworn by me;

6 That the testimony of the witness, the
7 questions propounded, and all objections and statements
8 made at the time of the examination were recorded
9 stenographically by me and were thereafter transcribed;

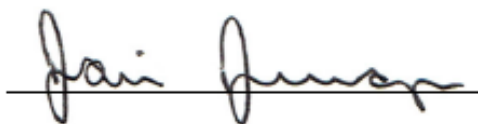
10 That the foregoing pages contain a full, true
11 and accurate record of all proceedings and testimony.

12 Pursuant to F.R.C.P. 30(e)(2) before
13 completion of the proceedings, review of the transcript
14 [X] was [] was not requested.

15 I further certify that I am not a relative or
16 employee of any attorney of the parties, nor financially
17 interested in the action.

18 I declare under penalty of perjury under the
19 laws of California that the foregoing is true and
20 correct.

21 Dated this 21st day of March 2023.

22 
23

24 JANIS JENNINGS, CSR NO. 3942

25 CLR, CCRR

1 THEODORE W. CHANDLER, ESQ.

2 ted.chandler@bakerbotts.com

3 March 21, 2023

4 RE: Samsung Electronics Co. Ltd. vs. Netlist, Inc.

5 March 17, 2023-ANDREW WOLFE, Ph.D.-5773633

6 The above-referenced transcript has been
7 completed by Veritext Legal Solutions and
8 review of the transcript is being handled as follows:

9 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Contact Veritext
10 to schedule a time to review the original transcript at
11 a Veritext office.

12 ___ Per CA State Code (CCP 2025.520 (a)-(e)) - Locked .PDF
13 Transcript - The witness should review the transcript and
14 make any necessary corrections on the errata pages included
15 below, notating the page and line number of the corrections.
16 The witness should then sign and date the errata and penalty
17 of perjury pages and return the completed pages to all
18 appearing counsel within the period of time determined at
19 the deposition or provided by the Code of Civil Procedure.

20 ___ Waiving the CA Code of Civil Procedure per Stipulation of
21 Counsel - Original transcript to be released for signature
22 as determined at the deposition.

23 ___ Signature Waived - Reading & Signature was waived at the
24 time of the deposition.

25

Page 297

1 _X_ Federal R&S Requested (FRCP 30(e)(1)(B)) - Locked .PDF
2 Transcript - The witness should review the transcript and
3 make any necessary corrections on the errata pages included
4 below, notating the page and line number of the corrections.
5 The witness should then sign and date the errata and penalty
6 of perjury pages and return the completed pages to all
7 appearing counsel within the period of time determined at
8 the deposition or provided by the Federal Rules.
9 ___ Federal R&S Not Requested - Reading & Signature was not
10 requested before the completion of the deposition.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2022-00996

Patent 11,016,918

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (MARCH 16–17, 2023)**

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner.

Case IPR2022-00999

Patent 11,232,054

**ERRATA TO THE DEPOSITION OF
ANDREW WOLFE (MARCH 16–17, 2023)**

I, ANDREW WOLFE, have read the transcript of my deposition taken on March 16–17, 2023. Listed below are changes to the transcript that I wish to make and the reasons for making them:

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
7:2–:15	<p>Q. . . . the AMB will receive information from the memory controller of the host system; is that correct?</p> <p>A. It needs a little bit more than that. . . .</p> <p>Q. Okay. So assume that if the FB-DIMM is inserted into a memory slot, a properly configured computer system that is operating and that is programmed to interact with the particular memory module, <u>the MB</u> receives information from the memory controller of that host system; is that correct?</p> <p>A. That would normally be true.</p>	<p>Q. . . . the AMB will receive information from the memory controller of the host system; is that correct?</p> <p>A. It needs a little bit more than that. . . .</p> <p>Q. Okay. So assume that if the FB-DIMM is inserted into a memory slot, a properly configured computer system that is operating and that is programmed to interact with the particular memory module, <u>the AMB</u> receives information from the memory controller of that host system; is that correct?</p> <p>A. That would normally be true.</p>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
16:2–:4	So how can the <u>FTT</u> be used to selectively terminate the address and command information signals but not the data signals?	So how can the <u>VTT</u> be used to selectively terminate the address and command information signals but not the data signals?	Misstatement. See 16:8.
16:16–:19	So where <u>on</u> the termination resistors placed between the <u>FTT</u> pins and the address command clock signals to the DRAM, or <u>they are</u> terminated on the motherboard?	So where <u>are</u> the termination resistors placed between the <u>VTT</u> pins and the address command clock signals to the DRAM, or <u>are they</u> terminated on the motherboard?	Typographical errors and misstatement.
27:11 46:17 46:25 47:8 47:12 47:16 47:19 48:8 48:19 49:2 49:13 135:17 135:22	<u>VCC FBD</u>	<u>VCCFBD</u>	Typographical errors
29:13–:15	Table 16, note 4, it says: "VTT of transmitting device must track <u>VRAM</u> of receiving device."	Table 16, note 4, it says: "VTT of transmitting device must track <u>VREF</u> of receiving device."	Typographical error
32:20	unknown DDR <u>time</u>	unknown DDR <u>type</u>	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
39:21–:22	Not between the three different <u>FDD</u> -derived power lines	Not between the three different <u>VDD</u> -derived power lines	Typographical error
40:21–:22	And did Harris expressly suggest or disclose <u>pinning</u> VDD, VDDQ and VDDL independently?	And did Harris expressly suggest or disclose <u>sequencing</u> VDD, VDDQ and VDDL independently?	Typographical error
47:4–:5	<u>very skilled</u> in the art	<u>of ordinary skill</u> in the art	Typographical error
48:15	had given	had <u>been</u> given	Typographical error
56:7–:10	one would understand a pulse-width modulated voltage converter that <u>inverts</u> between those particular voltages in this particular kind of a system to be a buck converter	one would understand a pulse-width modulated voltage converter that <u>converts</u> between those particular voltages in this particular kind of a system to be a buck converter	Typographical error
61:25	When the <u>words</u> converter's used	When the <u>word</u> converter's used	Typographical error
62:2–:3	I'm not really familiar with linear regulators being called <u>inverters</u> very often	I'm not really familiar with linear regulators being called <u>converters</u> very often	Typographical error
75:4–:5	So as far as you recall, <u>FDRs</u> don't need a VTT?	So as far as you recall, <u>SDRs</u> don't need a VTT?	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
83:5–:7	I looked for buck converters that could produce 3.3 volts at sufficient currents to support a -- a <u>SP-DIMM</u> .	I looked for buck converters that could produce 3.3 volts at sufficient currents to support a -- a <u>FB-DIMM</u> .	Typographical error
83:16–:20	The words show up later when I talk about the <u>VSPD</u> and refer back to those paragraphs because those paragraphs explain how a buck converter can be used to generate a step-down voltage from 12 volts, such as a 3.3V voltage.	The words show up later when I talk about the <u>VDDSPD</u> and refer back to those paragraphs because those paragraphs explain how a buck converter can be used to generate a step-down voltage from 12 volts, such as a 3.3V voltage.	Typographical error or misstatement
84:7–:10	I explain how those paragraphs are used to explain the reasons why one would supply <u>VSPD</u> using a buck converter.	I explain how those paragraphs are used to explain the reasons why one would supply <u>VDDSPD</u> using a buck converter.	Typographical error or misstatement
88:4–:7	As a designer, if the load at the peak is 20 to 30 milliamp, would you use the buck converter showing in Exhibit 1040, or would you just use a <u>new</u> regulator in that case?	As a designer, if the load at the peak is 20 to 30 milliamp, would you use the buck converter showing in Exhibit 1040, or would you just use a <u>linear</u> regulator in that case?	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
96:14–:15	the DIMMs are <u>powered supply</u> rails from the host system	the DIMMs are <u>powered by supply</u> rails from the host system	Typographical error
100:2–:3	And if you use a single <u>conductor</u> multiple output buck converter	And if you use a single <u>inductor</u> multiple output buck converter	Typographical error
108:23	the <u>un-DIMM</u> AMB buffer	the <u>on-DIMM</u> AMB buffer	Typographical error
109:5–:8	And for the potential <u>wide</u> length between the transmitting device AMB and the receiving device FB-DIMM, would that <u>wide</u> length be sufficiently long that a VTT would be required?	And for the potential <u>wire</u> length between the transmitting device AMB and the receiving device FB-DIMM, would that <u>wire</u> length be sufficiently long that a VTT would be required?	Typographical errors
109:24–:25	Where does Harris say <u>if</u> FB-DIMM is JEDEC compliant?	Where does Harris say <u>his</u> FB-DIMM is JEDEC compliant?	Typographical error
117:16–:17	a standard <u>FB-DIMM</u> <u>doesn't</u> supply 12 volts and does supply other voltages	a standard <u>FB-DIMM socket</u> <u>doesn't</u> supply 12 volts and does supply other voltages	Typographical error or misstatement

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
118:19– 119:1	<p>Q. When you say bypass capacitors are capacitors that are placed very close to in this case a chip, which chip are you referring to?</p> <p>A. Probably every chip on the DIMM, but most importantly the DRAMs.</p> <p>Q. So you are referring to the chips on the <u>DRAM</u>, not to the, for example, the <u>processes</u> on the motherboard?</p>	<p>Q. When you say bypass capacitors are capacitors that are placed very close to in this case a chip, which chip are you referring to?</p> <p>A. Probably every chip on the DIMM, but most importantly the DRAMs.</p> <p>Q. So you are referring to the chips on the <u>DIMM</u>, not to the, for example, the <u>processor</u> on the motherboard?</p>	Typographical errors
131:24–:25	It's the power voltage for the <u>delay watt</u> loop.	It's the power voltage for the <u>delay-locked</u> loop.	Typographical error
137:10	buffer on a <u>register</u> DIMM	buffer on a <u>registered</u> DIMM	Typographical error
145:10–:12	I'm not aware of a separate <u>FTT</u> voltage supply being used with single data rate DRAM.	I'm not aware of a separate <u>VTT</u> voltage supply being used with single data rate DRAM.	Typographical error or mistatement
150:2	Now, aside from the 1.8 volt <u>at PGA</u> core	Now, aside from the 1.8 volt <u>FPGA</u> core	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
150:14–:19	Q. Okay. So for example, if the industry standard SDRAM is the SDR SDRAM, then you only needed the 3.3 volt to power it; correct? A. Yes. But, of course, by the time of the invention, SDRAM was quite old and pretty deprecated.	Q. Okay. So for example, if the industry standard SDRAM is the SDR SDRAM, then you only needed the 3.3 volt to power it; correct? A. Yes. But, of course, by the time of the invention, <u>SDR SDRAM</u> was quite old and pretty deprecated.	Clarification
154:25– 155:1	And in the Figure 5 <u>embodiment</u> , it relied on	And in the Figure 5 <u>embodiment you</u> relied on	Typographical error
171:6–:9	Q. According to Spiers, when are the SDRAM's data being read? A. There are lots of different times when the <u>SD</u> data can be read.	Q. According to Spiers, when are the SDRAM's data being read? A. There are lots of different times when the <u>SDRAM</u> data can be read.	Typographical error
171:25	I'm not sure that it's even <u>bound</u> .	I'm not sure that it's even <u>bounded</u> .	Typographical error
174:18–:20	And if you can take a look at Exhibit 2013. Does that describe a 64-bit-wide SO-DIMM comprised of <u>FDRs</u> ?	And if you can take a look at Exhibit 2013. Does that describe a 64-bit-wide SO-DIMM comprised of <u>SDRs</u> ?	Typographical error
180:8–:9	But you don't have 64-bit wide <u>SD</u> <u>DDR2</u> SDRAMs, do you?	But you don't have 64-bit wide <u>SD --</u> <u>DDR2</u> SDRAMs, do you?	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
193:20–:21	I simply explained one set of <u>obviousness</u> implementations.	I simply explained one set of <u>obvious</u> implementations.	Typographical error
204:3	<u>ANDY WOLFE</u>	<u>ANDREW WOLFE, Ph.D.</u>	Typographical error
217:24– 218:3	A. . . . The module is the PCI card, and the PCI connector is the interface that <u>enclosed</u> a plurality of edge connections. Q. And so you're not relying on any other types of module <u>powers</u> ?	A. . . . The module is the PCI card, and the PCI connector is the interface that <u>disclosed</u> a plurality of edge connections. Q. And so you're not relying on any other types of module <u>interfaces</u> ?	Typographical errors
224:23–:25	A charge pump is a type of switching power <u>inverter</u> , usually for switching from a low voltage to a higher voltage.	A charge pump is a type of switching power <u>converter</u> , usually for switching from a low voltage to a higher voltage.	Typographical error
225:2–:4	But a charge pump can also be used to switch the <u>plurality</u> of a voltage as well from positive to negative or negative to positive.	But a charge pump can also be used to switch the <u>polarity</u> of a voltage as well from positive to negative or negative to positive.	Typographical error
225:18–:19	A textbook buck boost converter would depend on an inductor. A charge pump <u>can't</u> operate with capacitors alone.	A textbook buck boost converter would depend on an inductor. A charge pump <u>can</u> operate with capacitors alone.	Typographical error

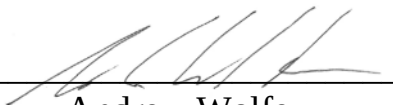
<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
233:20–:22	I think the marking 5 volts to 3.3 volts is nominal. That is the <u>inversion</u> while it is operating off of <u>post</u> power	I think the marking 5 volts to 3.3 volts is nominal. That is the <u>conversion</u> while it is operating off of <u>host</u> power	Typographical errors
240:12–:15	And for the Spiers <u>grant</u> , the VTT is for terminating the address command and the clock information from the processor 198 to the DDR2 or DDR3; is that right?	And for the Spiers <u>Ground</u> , the VTT is for terminating the address command and the clock information from the processor 198 to the DDR2 or DDR3; is that right?	Typographical error
246:13–:17	So, yes, it's certainly possible that you could have DDR modules that have the same capacity as individual DDR chips, or DDR3 modules that have the same capacity as individual <u>DDR</u> chips.	So, yes, it's certainly possible that you could have DDR modules that have the same capacity as individual DDR chips, or DDR3 modules that have the same capacity as individual <u>DDR3</u> chips.	Clarification
253:17	it's <u>the</u> least obvious	it's <u>at</u> least obvious	Typographical error
262:5	This note is specific to <u>the IPU</u> .	This note is specific to <u>V_{ipu}</u> .	Typographical error
263:2–:4	This is an exemplary PCI power <u>volt</u> detection chip that was known at the time of the invention.	This is an exemplary PCI power <u>voltage</u> detection chip that was known at the time of the invention.	Typographical error

<u>Page:Line</u>	<u>Now Reads</u>	<u>Should Read</u>	<u>Reason for Change</u>
266:18–:19	It depends on how the person uses <u>his</u> chip on the board.	It depends on how the person uses <u>this</u> chip on the board.	Typographical error
275:1	It does <u>teaches</u> that his design is suitable	It does <u>teach</u> that his design is suitable	Typographical error
276:11–:13	Coupled to can be interpreted differently by lots of different courts <u>and</u> my experience based on the totality of the context	Coupled to can be interpreted differently by lots of different courts <u>in</u> my experience based on the totality of the context	Typographical error
278:17	let’s say if the <u>board</u> decides	let’s say if the <u>Board</u> decides	Typographical error
280:5–:7	it is difficult to <u>enact</u> multiple regulator outputs together without some type of a switch	it is difficult to <u>connect</u> multiple regulator outputs together without some type of a switch	Typographical error
281:1–:4	But if the failure is in the <u>5.5-volt</u> power system if, for example, something is shorting 5 volts or something like that, I would want to detect that.	But if the failure is in the <u>5-volt</u> power system if, for example, something is shorting 5 volts or something like that, I would want to detect that.	Typographical error
287:23–:24	<u>VRC</u> is the DRAM controller mode register.	<u>DRC</u> is the DRAM controller mode register.	Typographical error
292:6	It’s called the <u>SFBD</u> Channel	It’s called the <u>FBD</u> Channel	Typographical error

I hereby certify that the transcript of my deposition on March 16–17, 2023, as corrected above, is a true and accurate transcription of my testimony.

I, Andrew Wolfe, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: March 26, 2023



Andrew Wolfe