

Fully Buffered DIMM (FB-DIMM) Design Considerations

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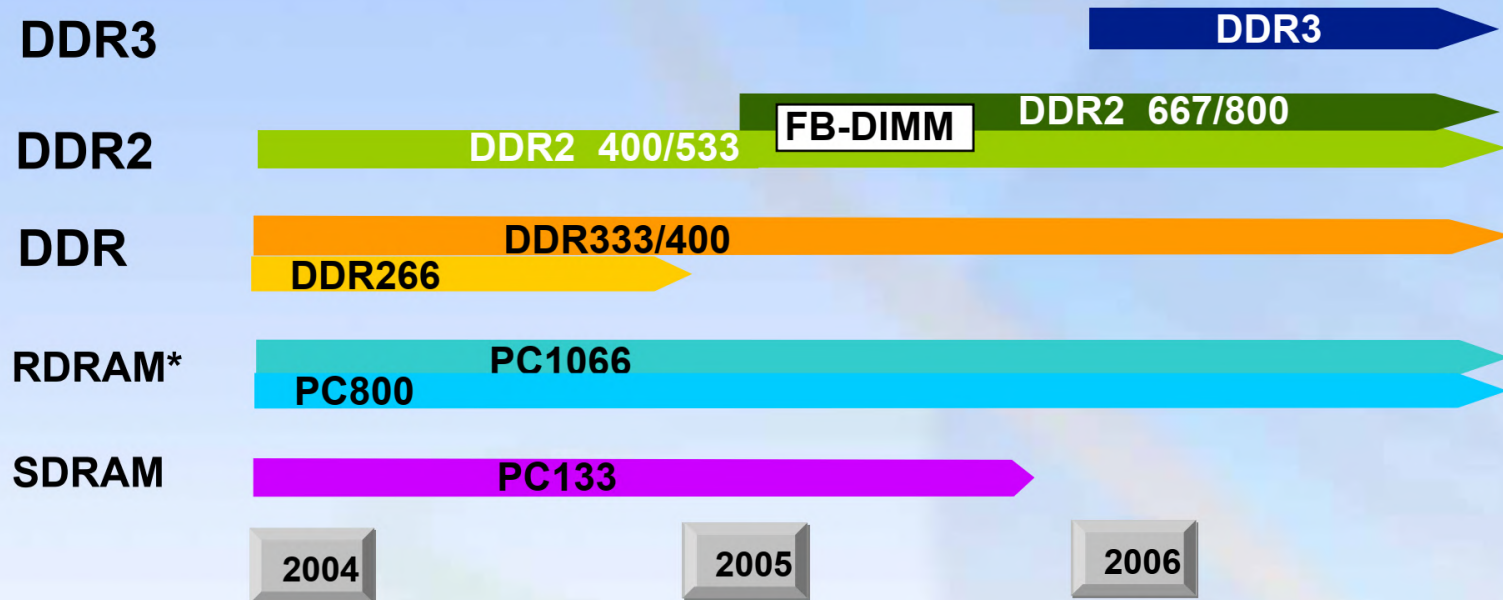
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Agenda

- **FB-DIMM Architecture**
- **FB-DIMM Channel Electrical Characteristics**
- **FB-DIMM Physical Design**
- **FB-DIMM System Design Considerations**



Intel Platform Memory Technology Roadmap



- DDR2 400/533 support in all main IA segments in 2004
 - with DDR flexibility
- FB-DIMM new server interconnect in 2005
- Low Power SDRAM moving to low power DDR
- RDRAM still used in specific applications

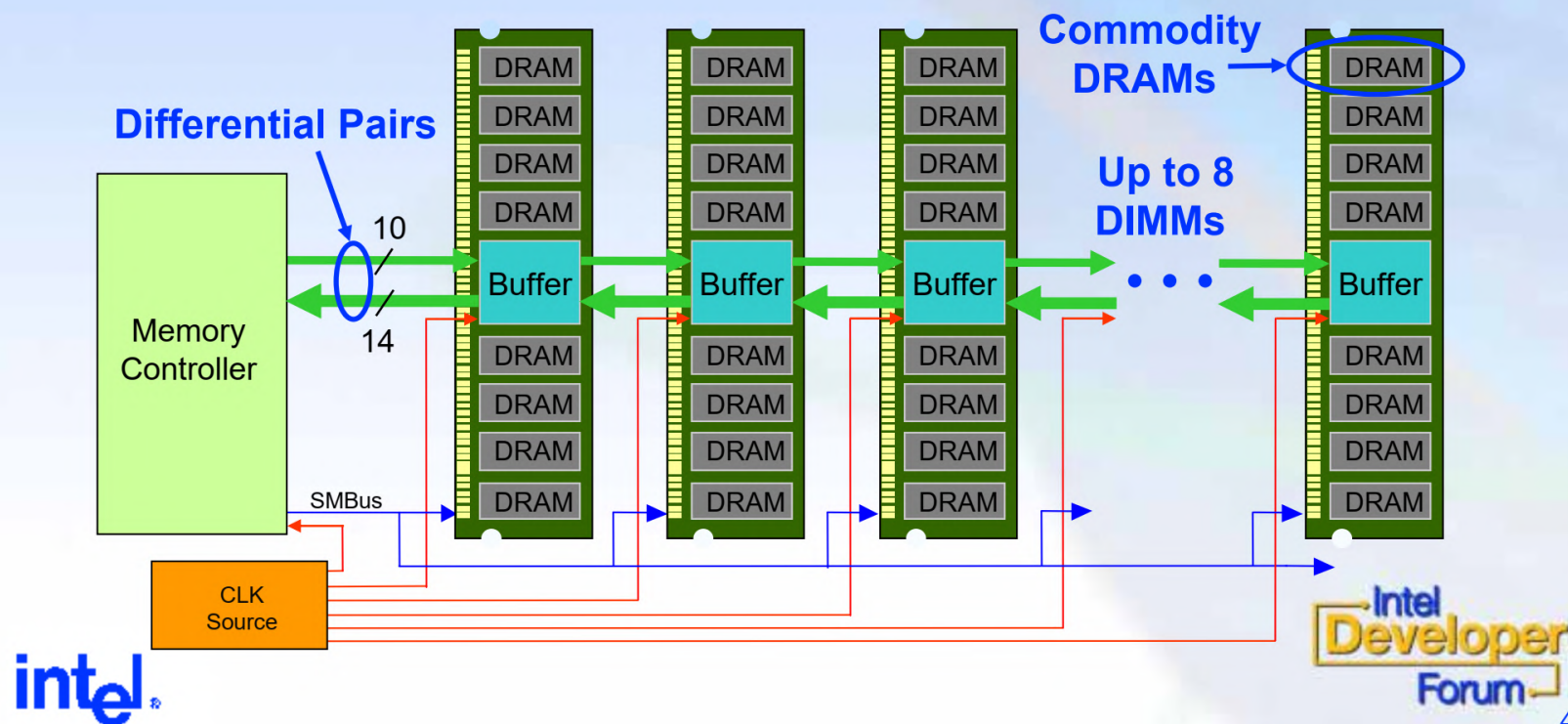


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FB-DIMM Block Diagram

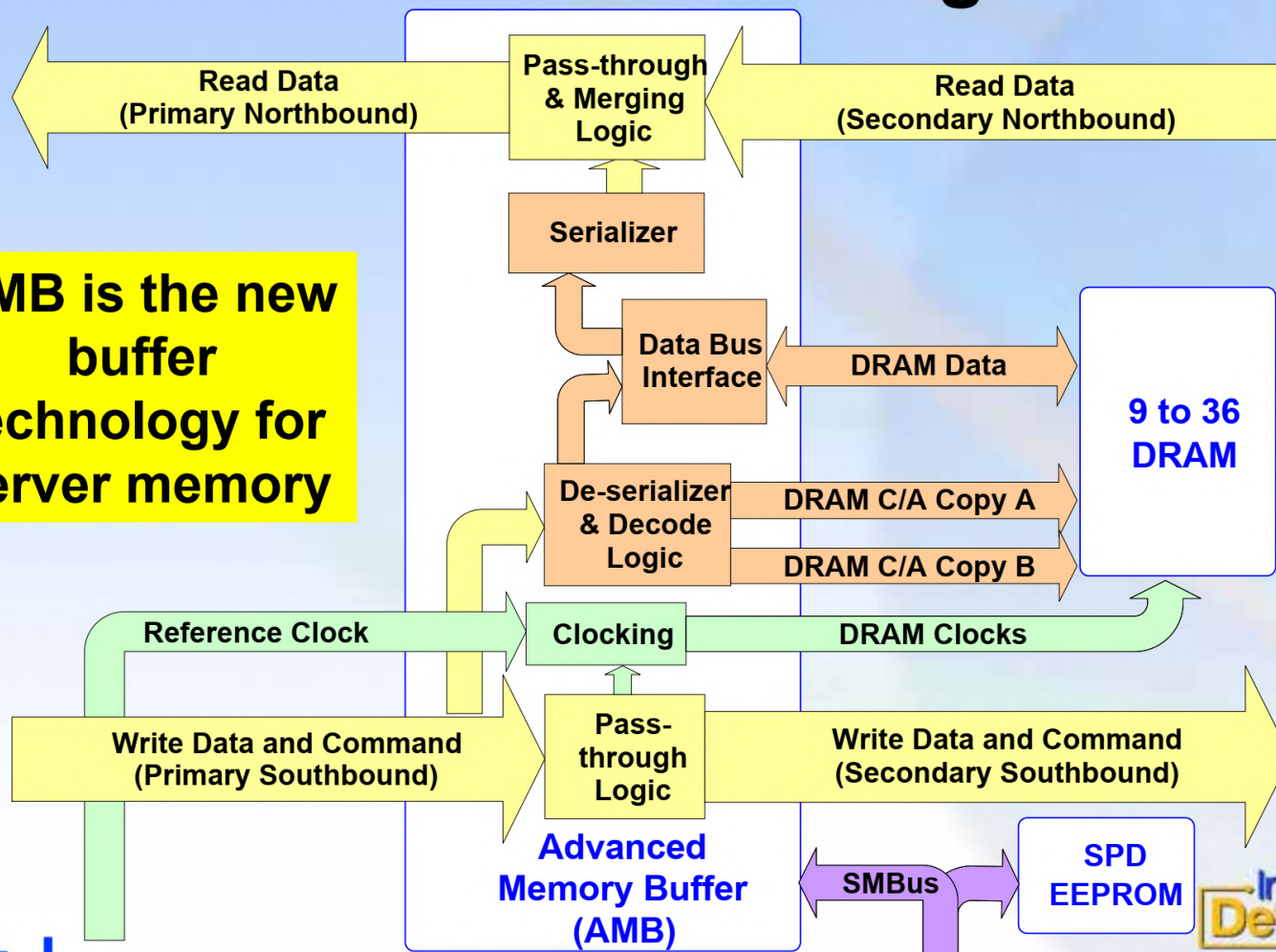
- DRAM interface is entirely behind the buffer
 - DDR2 DRAM scales from 533 to 800 MT/s, with up to 8 DIMMs (288 devices) per channel



FB-DIMM Architecture

FB-DIMM Module Block Diagram

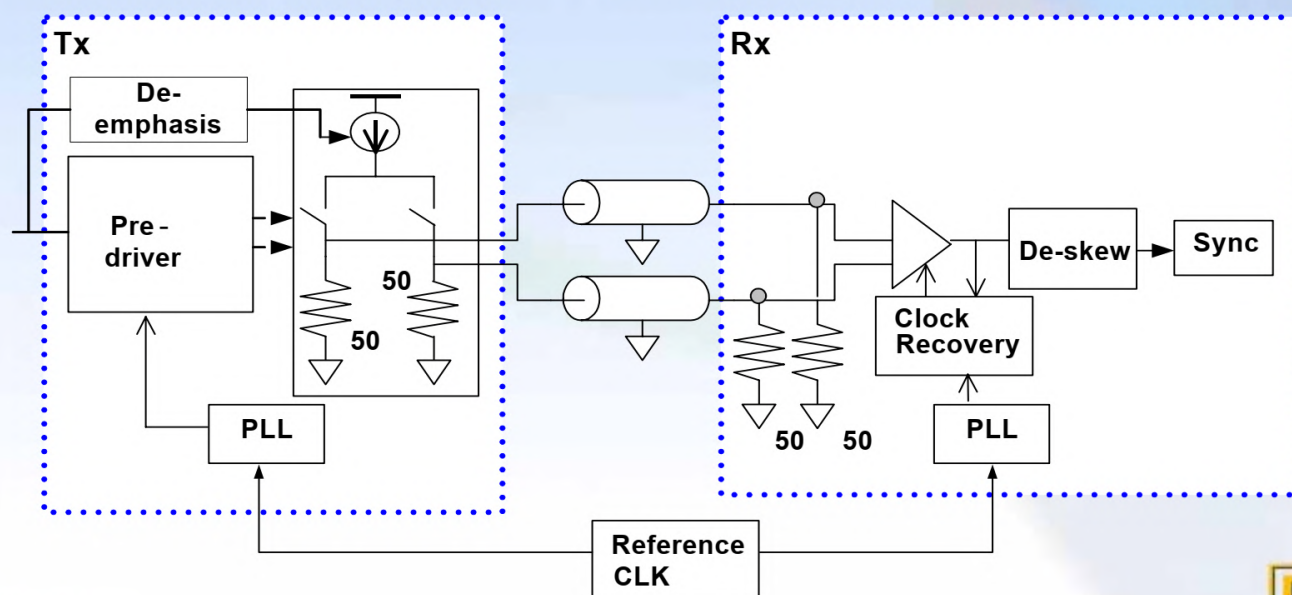
**AMB is the new
buffer
technology for
server memory**



FB-DIMM Channel Electrical Characteristics

Signaling Characteristics

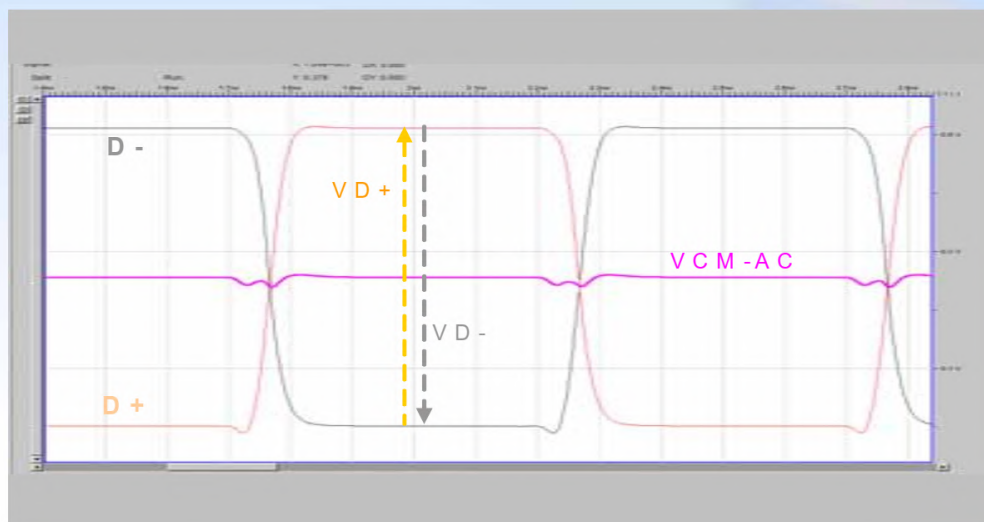
- Differential point-to-point, 50 Ω termination
- DC coupled, current mode driver
- Derived clocking (mesochronous clocking)
- Transmitter de-emphasis to reduce ISI
- 3.2 Gb/s, 4.0 Gb/s, and 4.8 Gb/s data rates



FB-DIMM Channel Electrical Characteristics

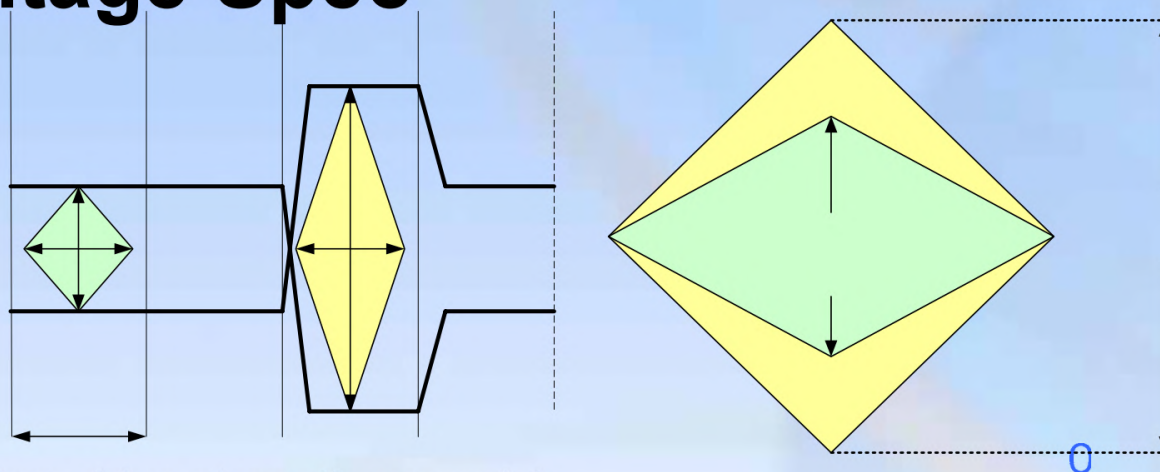
Differential Signaling

Parameter	Description	Equation
VDIFFp-p	Differential Peak to Peak Voltage	$2 \cdot \max[VD+ - VD-]$
VCM-AC	AC Common Mode Voltage	$(VD+ + VD-)/2$
VCM-DC	DC Common Mode Voltage	$AVG[(VD+ + VD-)/2]$



FB-DIMM Channel Electrical Characteristics

Tx Voltage Spec



(Medium drive strength example)

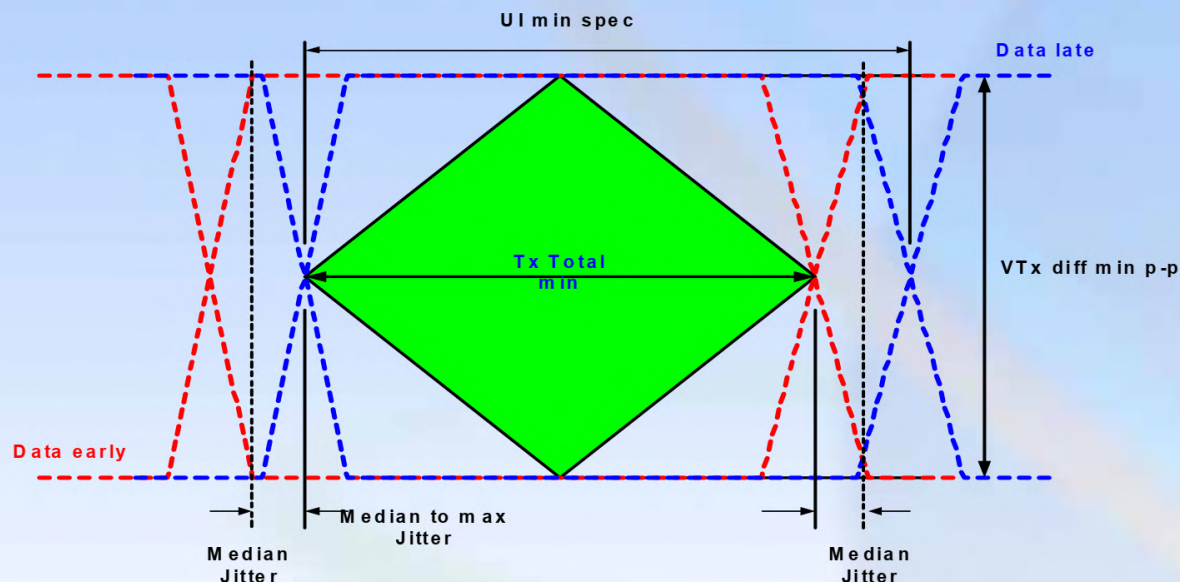
Parameter	Description	Min	Max
VTX-DIFF _{p-p} -Min D+, D-	Differential Swing, De-emphasis off	800 mv 1	
VTX-DIFF _{p-p} -Min, -3.5 Db	Differential swing, De-emphasis on	505 mv	566 mv
VTX-DIFF _{p-p} -Min, -6.0 Db D-, D+	Differential swing, De-emphasis on	357 mv 0	450 mv
VTX-DIFF _{p-p} -Min, -9.0 Db	Differential swing, De-emphasis on	239 mv	301 mv
VTX-SE	Single Ended Swing		700 mv

Unit



FB-DIMM Channel Electrical Characteristics

Tx Timing Spec



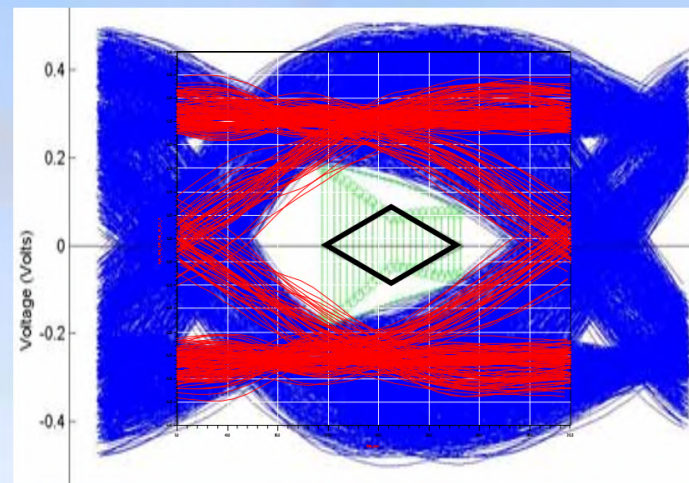
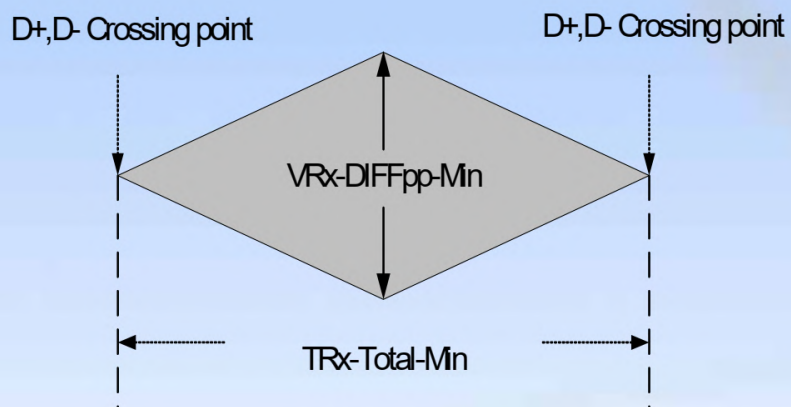
$$UI_{min} - Tx_{min} - 2Tx_{median\ to\ max\ jitter} = 0$$

Transfer Rate (Gb/s)	UI Nom (ps)	TTx-Total-min (ps)	TTX-Eye-Median-Max-Jitter (ps)
3.2	312.0	248.5	32.0
4.0	250.0	191.0	29.5
4.8	208.0	157.0	25.68



FB-DIMM Channel Electrical Characteristics

Rx Spec



•Measured
•Simulated

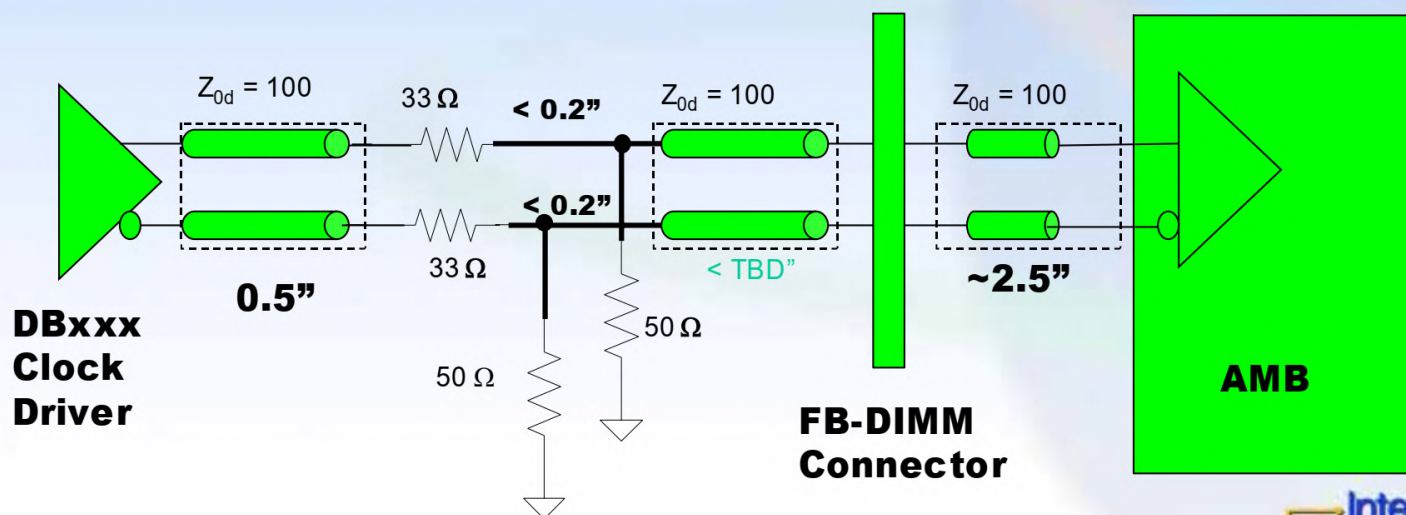
Data Rate (Gb/s)	UI, Nom (ps)	TRX-Total-Min (ps)	TRX-EYE-Median-Max Jitter (ps)	$V_{RX-DIFFp-p-MIN}$ (mV)
3.2	312.0	115	98.67	170
4.0	250.0	90	80.0	170
4.8	208.0	75	66.68	170



FB-DIMM Channel Electrical Characteristics

Clock Spec

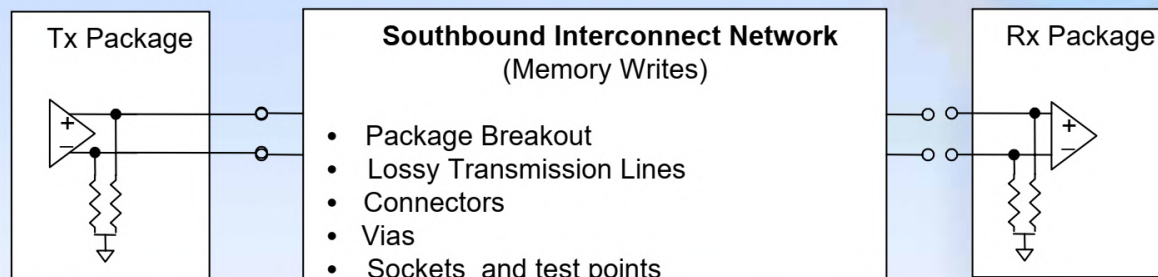
- HCSL (High-Speed Current Steering Logic) clock
- 0.7 v swing
- 1/4th of the DDR2 DRAM frequency (133, 166, and 200 MHz)
- Spread Spectrum Clock (SSC) with up to -0.5% down spread
- Reference clock jitter specified to allow standard clock buffers.



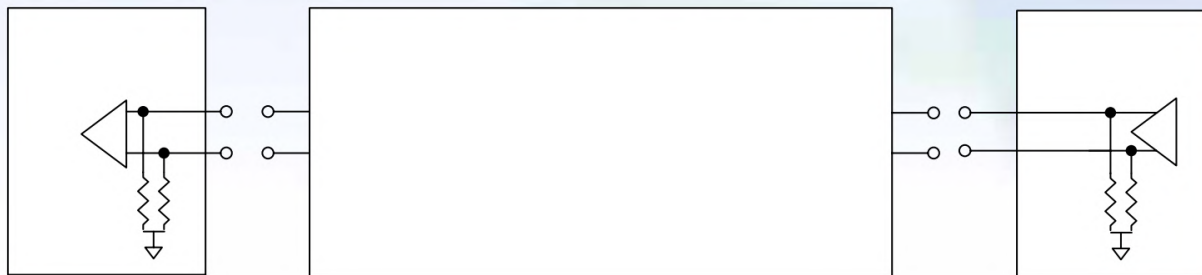
FB-DIMM Channel Electrical Characteristics

Interconnect Modeling

- Three (3) Topologies supported
- Accurately models connection from Tx pin to Rx pin
- Non-Interleaved routing with no bit to bit length matching required
- Differential signaling design rules



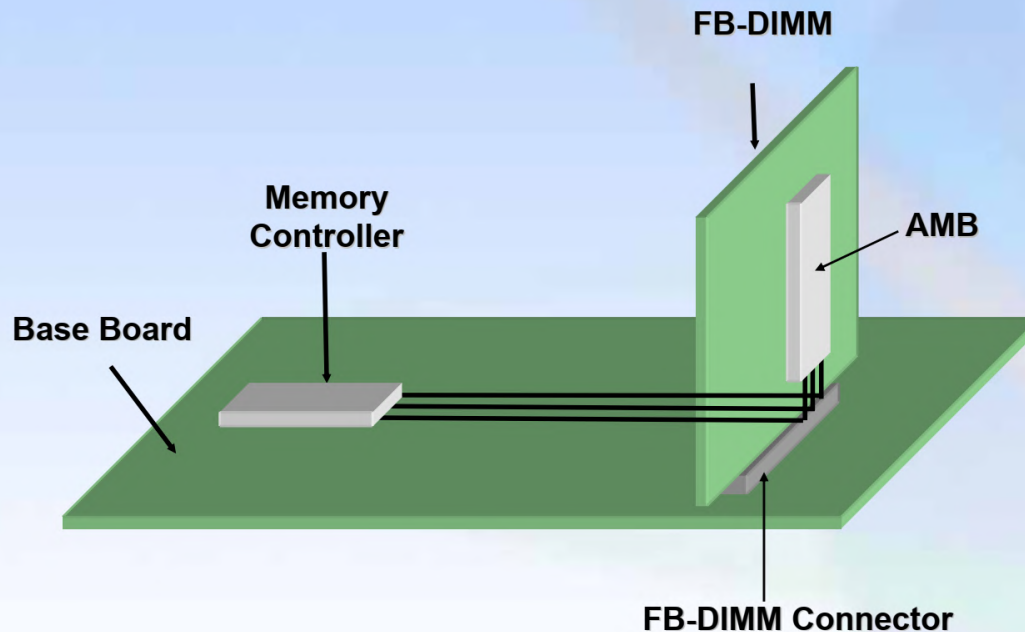
Not Equivalent due to DIMM Routing and connector location



FB-DIMM Channel Electrical Characteristics

FB-DIMM Topologies

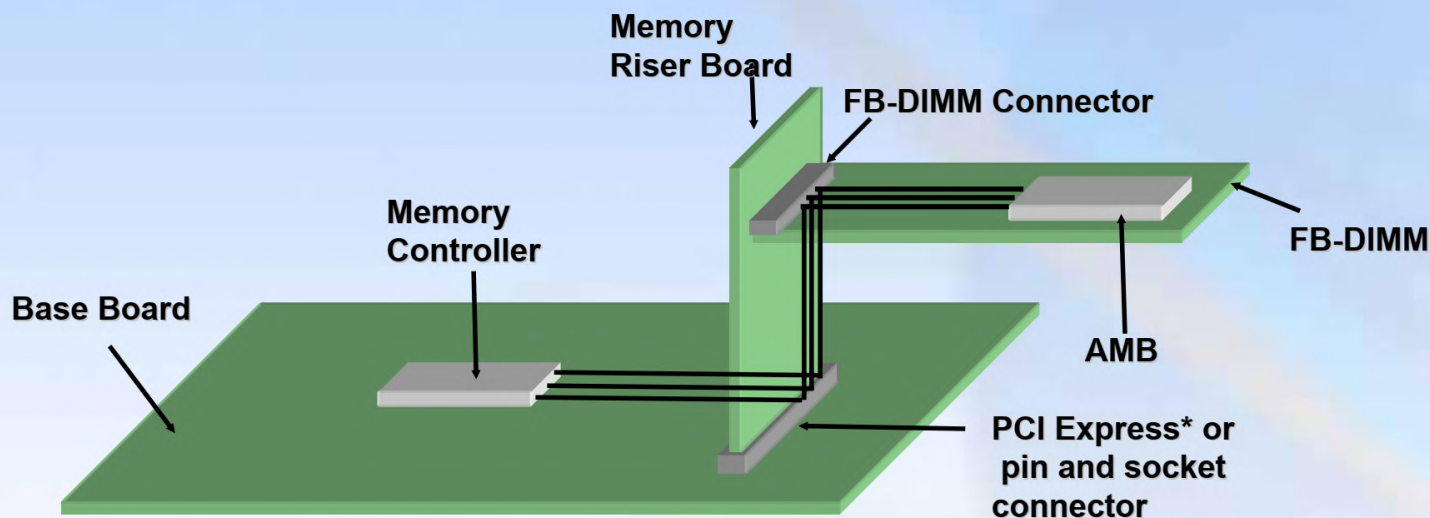
DIMMs on Motherboard



FB-DIMM Channel Electrical Characteristics

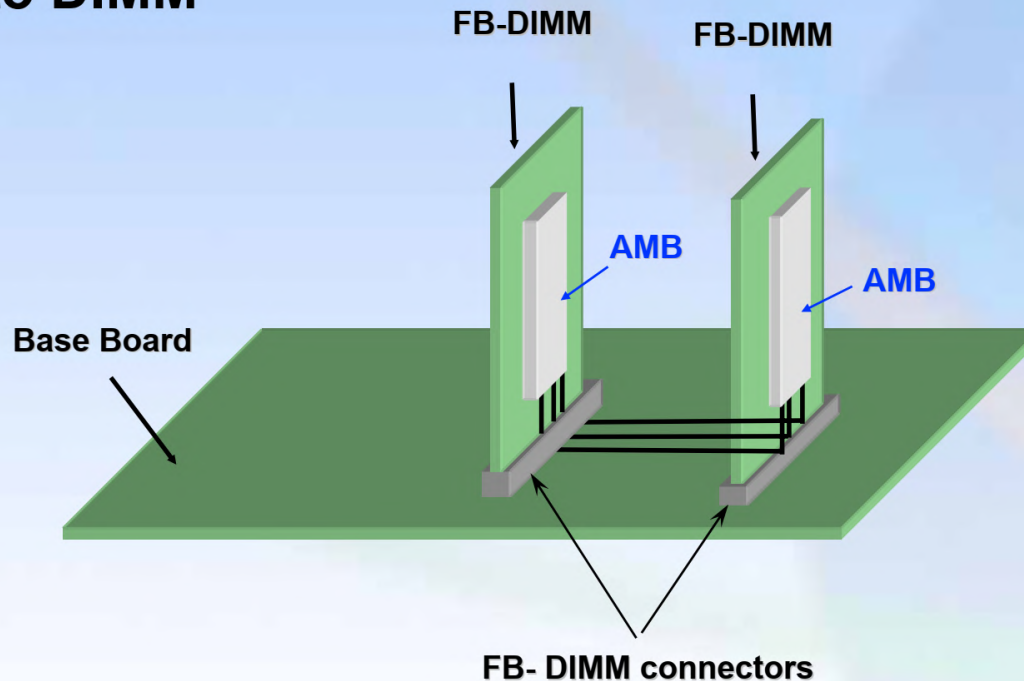
FB-DIMM Topologies

DIMMs on a Riser Card



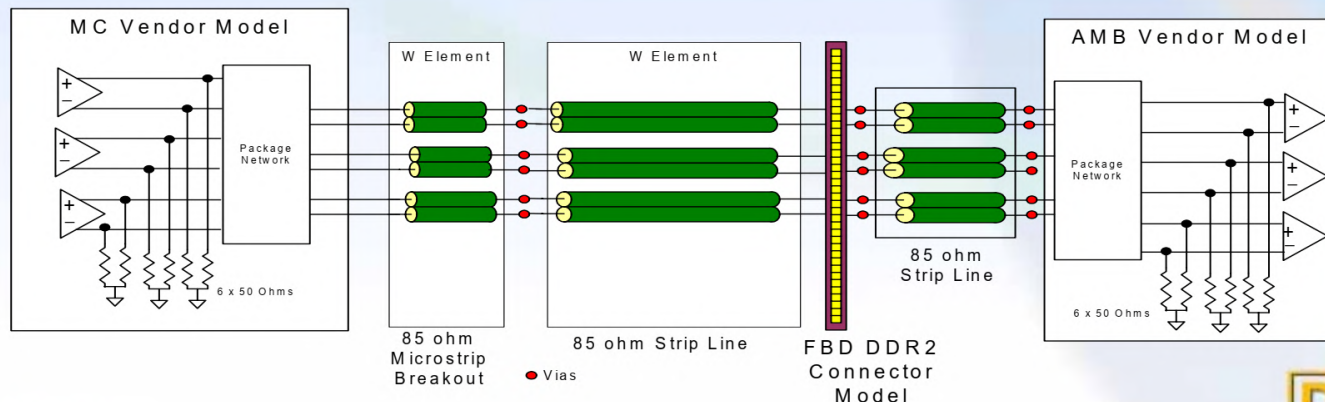
FB-DIMM Topologies

DIMM to DIMM



Interconnect Components

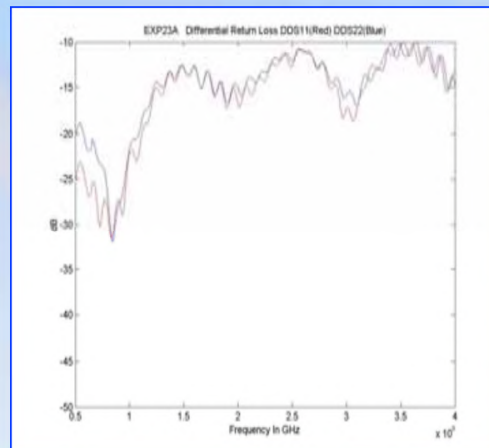
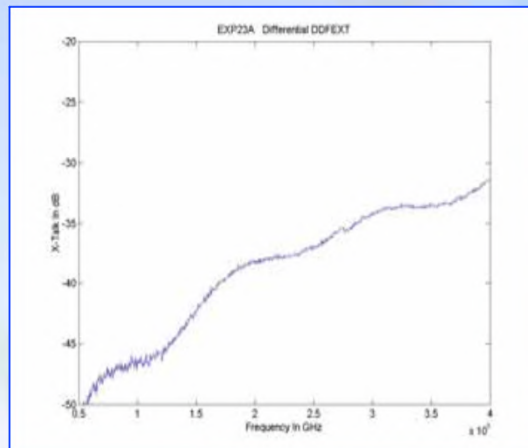
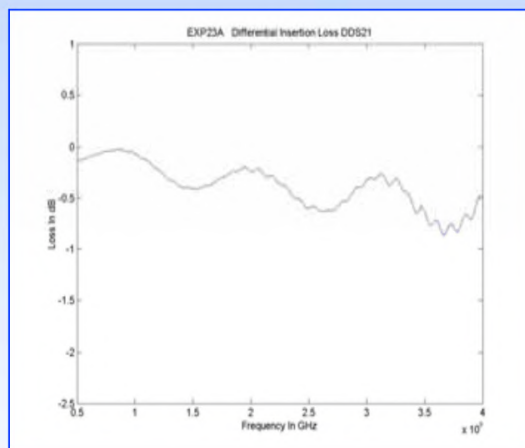
- **Package Models**
 - Return Loss (<-10 Db)
- **PCB Model**
 - Impedance, delay, and loss characteristics of traces
 - 3 pair, non-interleaved, cross talk model
 - VIA Models
- **Connector(s)**
 - 3D Models validated using Measurements



FB-DIMM Channel Electrical Characteristics

FB-DIMM Connector

- Standard DDR2 Connector w/ FB-DIMM connector spec
- Characterized up to 8 GHz
- Q3D Spice Model based on FOXCONN* Connector Data



- Less than 1 Db insertion loss.
- Less than 3.2% Far end Cross talk
- Less than 10 Db insertion loss

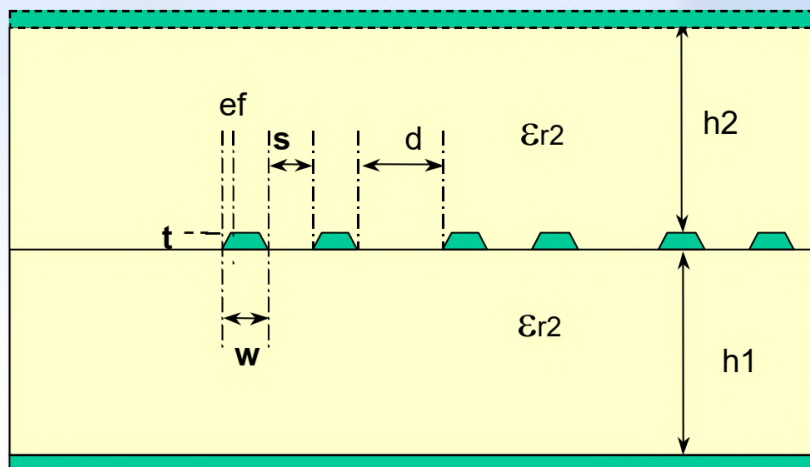


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Channel Design Rules

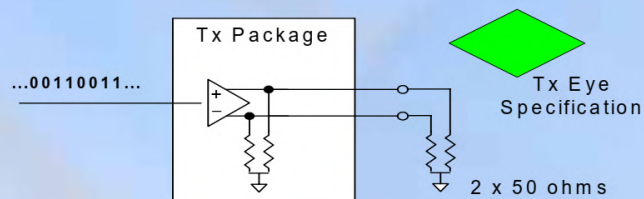
- Channel impedance: 85 ohms , normal distribution
- Microstrip trace geometry
 - $w=6\text{m}$, $s=4x\ h$, tolerance = $\pm 20\%$, etc.
- Strip line trace geometry
 - $w=5\text{ mil}$, $s=3x\ h$, tolerance = $\pm 15\%$, etc
- Asymmetric strip line geometry
 - $w=5\text{ mil}$, $s=4x\ h$, tolerance = $\pm 15\%$, etc, etc
- Loss tangent 0.017 to 0.025, $\epsilon \sim 3.4$ (FR4 materials)



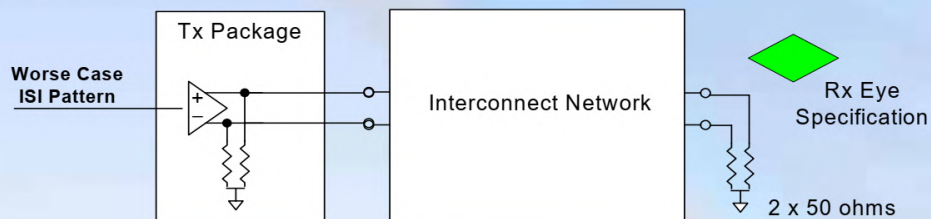
FB-DIMM Channel Electrical Characteristics

Channel Validation

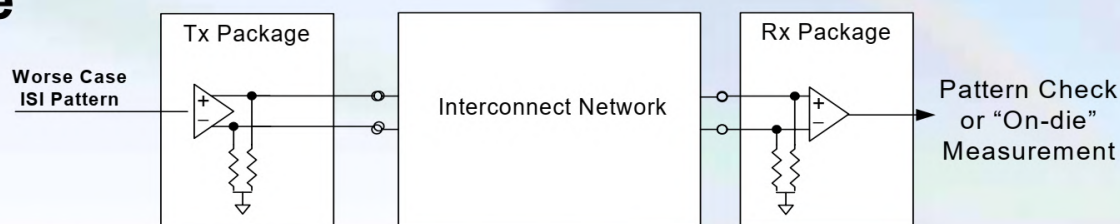
1. Tx Stand alone Test



2. Interconnect meets Rx Eye Spec



3. Rx Meets BER with Minimum Eye



FB-DIMM channel requires new memory design techniques



FB-DIMM Physical Design

Mechanical Prototype



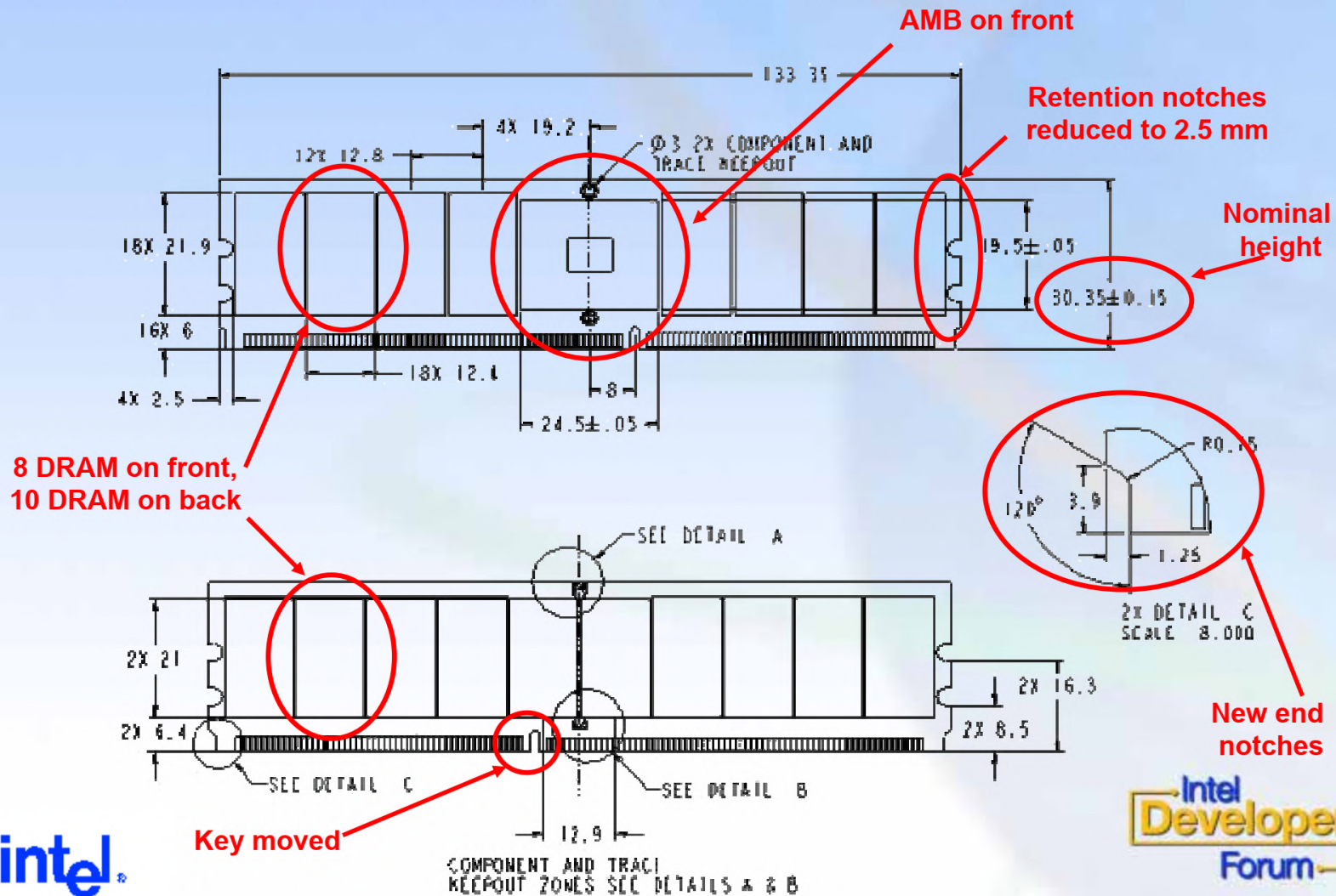
Physically Compatible Approach

- FB-DIMM fits into existing system infrastructure

	Registered DIMM	FB-DIMM
Max Dimension	133.5 x 30.5 mm	133.5 x 30.5 mm
Gold fingers	240	240
Key position	4 mm right of center	8 mm right of center
# of DRAM	9, 18 or 36	9, 18 or 36
DRAM Outline	12.3 x 21.9 mm	12.3 x 21.9 mm
Silicon Support Components	1,2 or 4 registers 1 PLL clock buffer 1 SPD EEPROM	1 Advanced Memory Buffer (AMB) 1 SPD EEPROM

FB-DIMM Physical Design

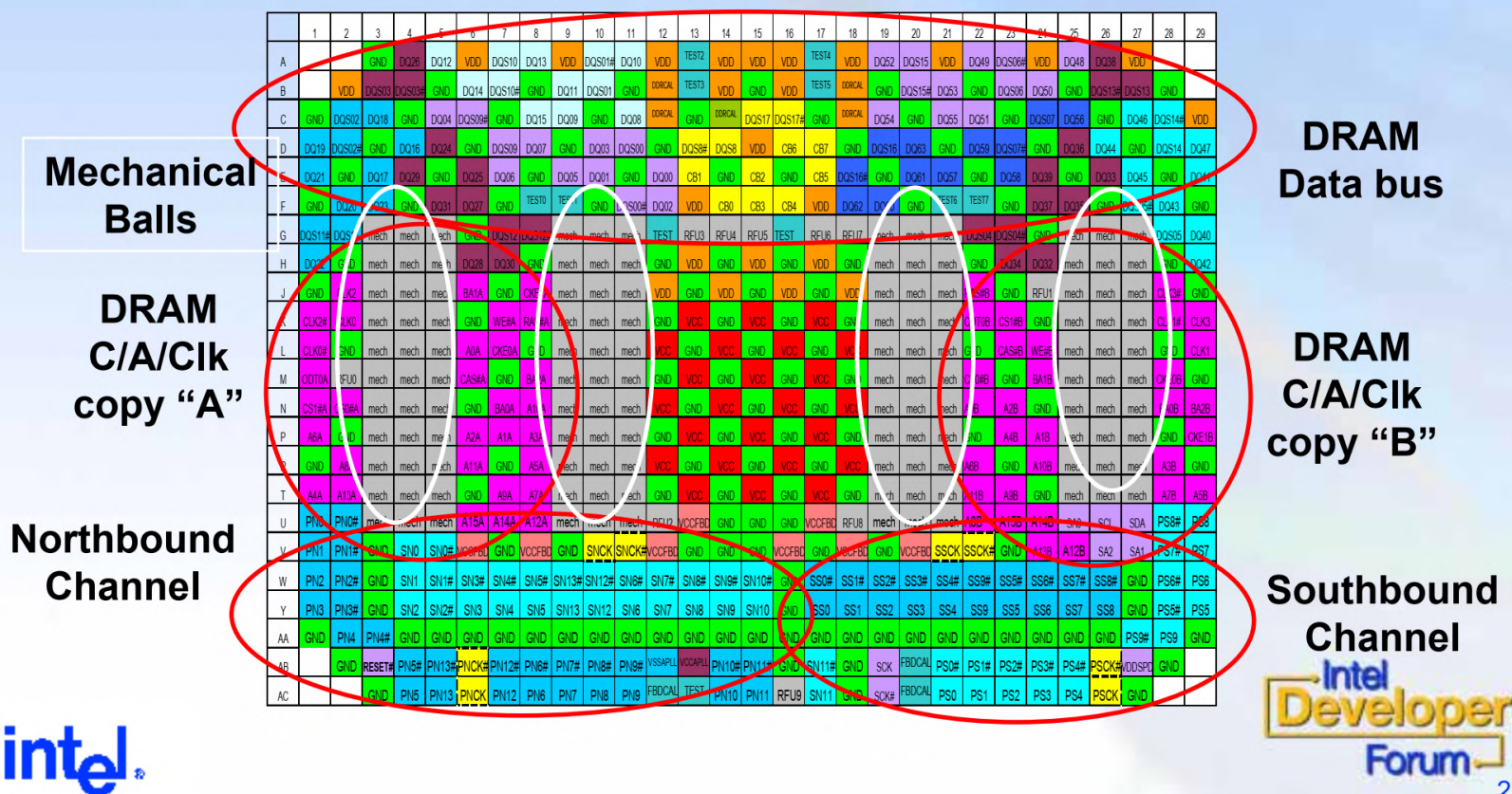
DIMM Mechanical Outline



FB-DIMM Physical Design

Advanced Memory Buffer (AMB)

- New 0.8 mm ball pitch package
 - 24.5 mm x 19.5 mm x 2.15 mm
 - (29 columns x 23 rows) – 12 corner balls = 655 balls



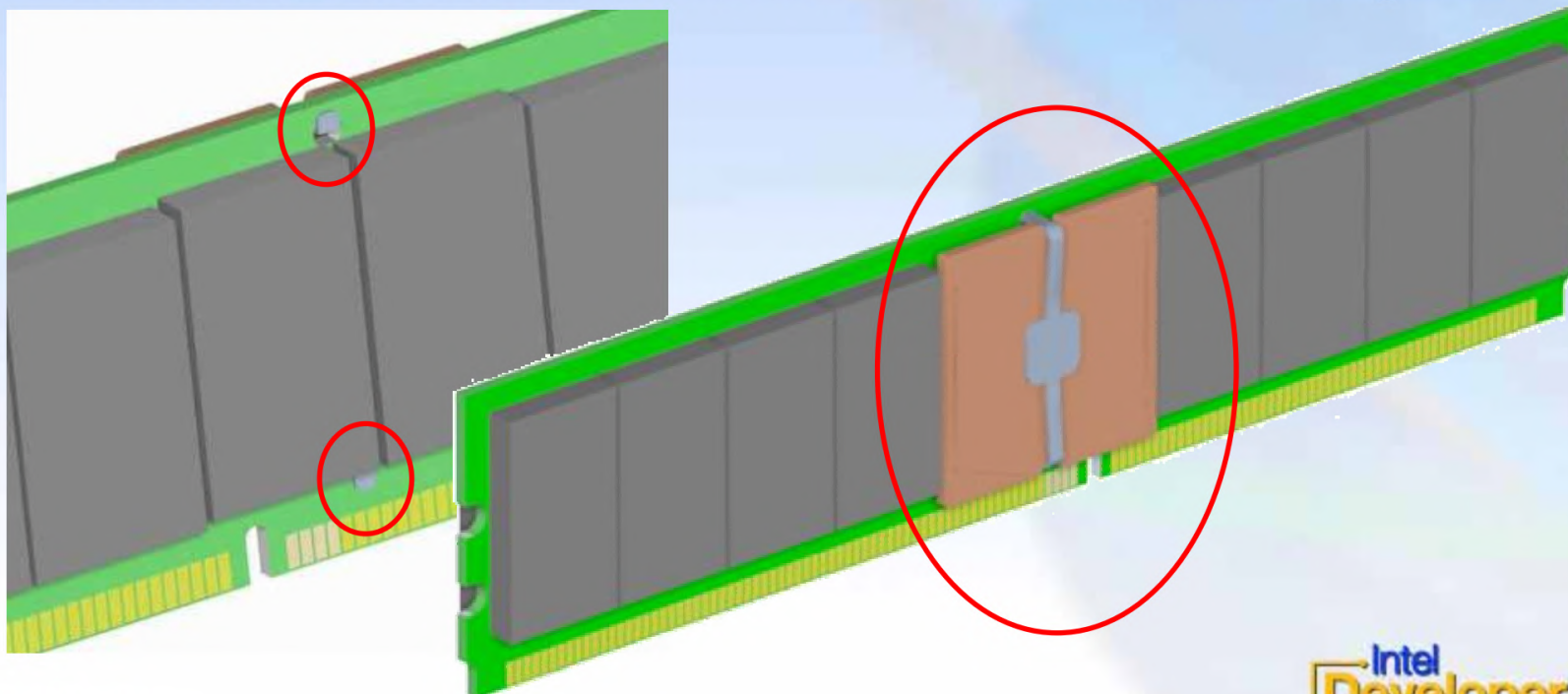
FB-DIMM Bus Topologies

- Bus topologies scale to higher frequencies than the registered DIMMs
 - DRAM farthest from AMB gets latest clock, C/A and data

	Registered DIMM	FB-DIMM
Data bus	Stub Topology up to 667, one DIMM per channel at 800 & higher	One or two DRAM at the end of a 15-75 mm trace
C/A bus	One unterminated tree at 400/533, ? at 667 & higher	Two terminated daisy chains
Clock bus	P-to-P to 1, 2 or 4 DRAM	Two or four terminated daisy chains

Thermal Solution for x8 based DIMMs

- x8 DIMMs will have an AMB-only heat spreader
 - Attached using a spring clip, inserted into two holes
- Stacked BGA and dual die x4 DIMMs under investigation



Raw Cards under Design

- The JEDEC DIMM and Socket Task Group is standardizing these DIMMs: (R/C=Raw Card)

– R/C A	SR x8	9 DRAM
– R/C B	DR x8	18 DRAM
– R/C C	SR x4	18 DRAM
– R/C D	DR x4	36 DRAM (Stacked)
- All DIMMs will fit standard MO & are designed to meet signal integrity, timing and power delivery
- FB-DIMM channels will be routed to same rules

DRAM interface is self-contained on industry standard DIMMs



System Design Overview

- **FB-DIMM uses standard baseboard technology**
 - With 6 layers, can route 4 FB-DIMM channels
 - Compared to 2 “stub bus” DDR2 channels
- **Will support standard pitch of 0.4”**
 - Evaluating wider pitch for stacked BGA x4 DIMMs
- **Three voltage regulators for DRAM and buffer**
 - 1.8V for DDR2 DRAM
 - 0.9V to terminate DRAM C/A
 - 1.5V for AMB



Cooling

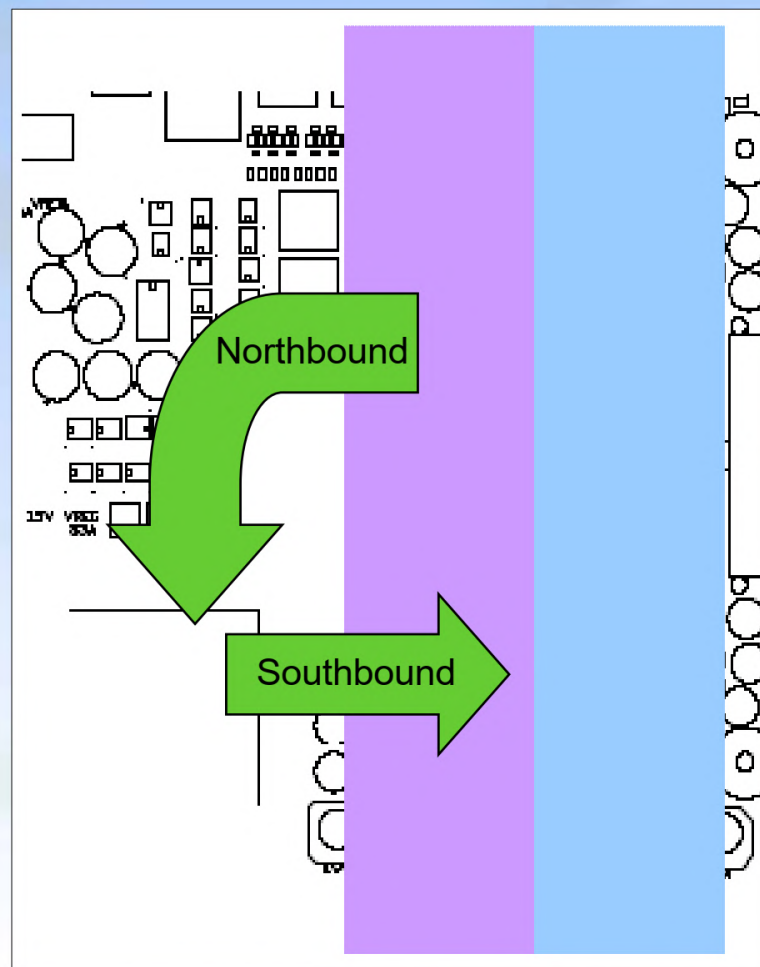
- **Need to meet component requirements:**
 - Normal refresh: DRAM Tcase $\leq 85^{\circ}\text{C}$ (tREFI=7.8us)
 - 2X refresh: DRAM Tcase $\leq 95^{\circ}\text{C}$ (tREFI=3.9us)
 - AMB Tcase $\leq 105^{\circ}\text{C}$
- **Recommend ducted air flow at 1.5-3.0 m/s inlet air speed**
 - A function of inlet air temperature and application
- **1st DIMM on channel is highest AMB power – typ. 3.4W**
- **Last DIMM on channel is lowest AMB power – typ. 2.4W**
 - Secondary channel disabled
- **Memory Controller will throttle activity to meet Tcase**
 - Algorithm enhanced by AMB thermal sensor



FB-DIMM System Design Considerations

8 DIMM Layout

- **Non-interleaved DIMM layout**
 - Better for thermals
- **0.4" DIMM-to-DIMM**
- **Length matching not required**
- **Shortest lead-in 1.2"**
 - Southbound channel 0
- **Longest lead-in 7.3"**
 - Northbound channel 3



Intel will present detailed design guidelines at Fall'04 IDF



Summary

- **AMB is the new buffer technology for server memory**
- **FB-DIMM channel requires new memory design techniques**
- **DRAM interface is self-contained on industry standard DIMMs**
- **Intel will present detailed design guidelines at Fall'04 IDF**

FB-DIMM is the next server memory technology



**Please fill out the Session
Evaluation Form.**

Thank You!



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Acronyms

- **AMB** **Advanced Memory Buffer**
- **ISI** **Inter-Symbol Interference**
- **Tx** **Transmitter**
- **Rx** **Receiver**
- **P-to-P** **Point-to-point**
- **BER** **Bit Error Rate**
- **PCB** **Printed Circuit Board**
- **MCH** **Memory Controller Hub**
- **MO** **Mechanical Outline**
- **R/C** **Raw Card**
- **JEDEC** **JEDEC Solid State Technology Association**
- **C/A** **Command/Address**



Birds-of-a-Feather Lunch Discussions

Where: Level 3 Foyer (Not in the main lunch area)
Arrive early – seating is limited

- When:**

Wednesday 12PM – 1:30PM	
802.11*	Extensible Firmware Interface (EFI)
802.16*/ WiMax*	Latin America Mobile/Data Services
Server Manageability	Advanced TCA*
Client Manageability	Advanced Switching based on PCI Express* Architecture
DMTF* Server Manageability Working Group	Connecting consumers in the digital home
IPMI (Intelligent Platform Management Interface)	
Thursday 12PM – 1:30PM	
Enthusiast PC	Ethernet in the Datacenter
Trusted Computing Group for More Secure Computing	Advanced Switching based on PCI Express* Architecture
Extended Battery Life	



Round Tables for Innovation

***Where: Level 2 – Alcoves across from Rooms 2018-2024
Immediately following Solution Keynotes***

What: This is your chance to focus on relevant issues, compare notes with colleagues, and gain insight from professionals who face similar challenges.

When: Tuesday 17th from 4:15 to 6:00pm

Topics:

- Emerging worker models for the highly connected employee
- Improving PC usability
- IT Benchmarking Programs
- Technology and Work/Life Balance
- Internal IT Consulting Model
- Managing wireless networks
- Productivity/collaboration/eWorkforce
- Capturing IT Business Value and ROI
- Mobilized Software: Addressing Technology and Business Challenges Consistently
- Creating Mobility Business Value in the Enterprise
- Reducing Costs and Increasing Revenue with Secure WLAN Solutions
- Achieving Competitive Advantages with Real-time Mobile Business Solutions
- Collaborating with Mobility
- Mobile Point of Care Solutions for Healthcare
- RFID technologies transforming the Retail environment



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