IN THE UNITED STATES DISTRICT COURT
FOR THE EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC. Plaintiff, v. **SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG SEMICONDUCTOR, INC., AVNET, INC.** Defendants.	)	Civil Action No. 2:25-cv-748 JURY TRIAL DEMANDED

COMPLAINT

1. Plaintiff Netlist, Inc. ("Netlist"), by its undersigned counsel, brings this action against Defendants Samsung Electronics Co., Ltd. ("SEC"), Samsung Electronics America, Inc. ("SEA"), Samsung Semiconductor, Inc. ("SSI" and, together with SEC and SEA, "Samsung"), and Avnet, Inc. ("Avnet" and, together with Samsung, "Defendants") for Defendants' infringement of U.S. Patent No. 12,373,366 (the "'366 Patent").

I. THE PARTIES

2. Plaintiff Netlist is a corporation organized and existing under the laws of the State of Delaware, having a principal place of business at 111 Academy Way, Suite 100, Irvine, CA 92617.

3. On information and belief, SEC is a corporation organized and existing under the laws of the Republic of Korea, with its principal place of business at 129 Samsung-ro, Yeongtong-gu, Suwon, Gyeonggi-Do, 443-742, Republic of Korea. On information and belief, SEC is the

worldwide parent corporation for SEA and SSI, and is responsible for the infringing activities identified in this Complaint. On information and belief, SEC's Device Solutions division is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, SEC is also involved in the design, manufacture, and provision of products sold by SEA.

4. On information and belief, SEA is a corporation organized and existing under the laws of the State of New York. On information and belief, SEA, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. Defendant SEA maintains facilities at 6625 Excellence Way, Plano, Texas 75023. SEA may be served with process through its registered agent for service in Texas: CT Corporation System, 1999 Bryan Street, Suite 900, Dallas, Texas 75201-3136. SEA is a wholly owned subsidiary of SEC.

5. On information and belief, SSI is a corporation organized and existing under the laws of the State of California. On information and belief, SSI, collectively with SEC, operates the Device Solutions division, which is involved in the design, manufacture, use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below. On information and belief, Defendant SSI maintains facilities at 6625 Excellence Way, Plano, Texas 75023. Defendant SSI may be served with process through its registered agent National Registered Agents, Inc., 1999 Bryan St., Ste. 900, Dallas, TX 75201. On information and belief, SSI is a wholly owned subsidiary of SEA.

6. On information and belief, Avnet is a corporation organized and existing under the laws of the State of New York. On information and belief, Avnet is involved in the use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as

defined below. On information and belief, Avnet has a regular and established place of business at 3101 E. President George Bush Highway, Suite 250, Richardson, TX 75082. On information and belief, Avnet is registered with the Texas Secretary of State to do business in Texas. On information and belief, Avnet can be served through its registered agent, The Corporation Service Company, 211 E. 7th Street, Suite 620, Austin, Texas, 78701-3218.

7. On information and belief, Defendants have used, sold, or offered to sell products and services, including the Accused Instrumentalities, in this judicial district.

II. JURISDICTION AND VENUE

8. Subject matter jurisdiction is based on 28 U.S.C. § 1338, in that this action arises under Federal statute, the patent laws of the United States (35 U.S.C. §§ 1, *et seq.*).

9. Each Defendant is subject to this Court's personal jurisdiction consistent with the principles of due process and/or the Texas Long Arm Statute.

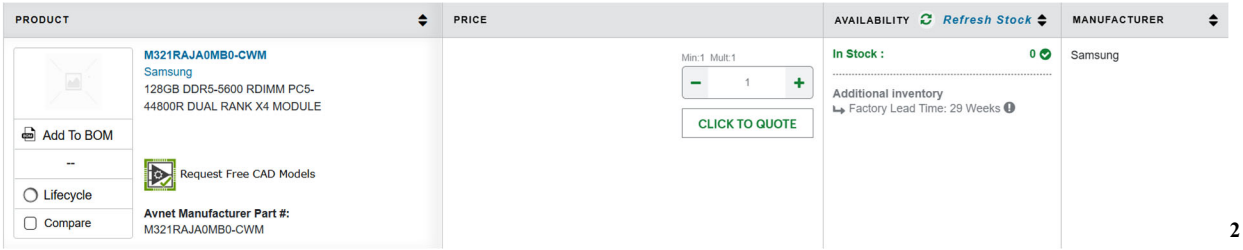
10. Personal jurisdiction exists generally over the Defendants because each Defendant has sufficient minimum contacts and/or has engaged in continuous and systematic activities in the forum as a result of business conducted within the State of Texas and the Eastern District of Texas. Personal jurisdiction also exists over each Defendant because each, directly or through subsidiaries, makes, uses, sells, offers for sale, imports, ships, distributes, advertises, makes available, and/or markets products within the State of Texas and the Eastern District of Texas that infringe one or more claims of the '366 Patent. Further, on information and belief, Defendants have placed or contributed to placing infringing products into the stream of commerce, both directly and through intermediaries (including distributors, retailers, authorized dealers, sales agents, and other individuals or entities), knowing or understanding that such products would be sold and used in the United States, including in this District.

11. Venue is proper in this Court pursuant to 28 U.S.C. §§ 1391(b) and (c) and/or 1400(b). For example, SEC maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. As another example, SEA maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district. Venue is also proper for SSI because it maintains a regular and established place of business in this judicial district at 6625 Excellence Way, Plano, Texas 75023 and has committed acts of infringement in this judicial district.

12. Samsung has not contested venue in this District. *See, e.g.*, Answer ¶ 10, *Arbor Glob. Strategies LLC v. Samsung Elecs. Co.*, No. 2:19-cv-333, Dkt. 43 (E.D. Tex. Apr. 27, 2020); Answer ¶ 29, *Acorn Semi, LLC v. Samsung Elecs. Co.*, No. 2:19-cv-347, Dkt. 14 (E.D. Tex. Feb. 12, 2020). Nor have Defendants contested venue in any of the prior actions between the Parties in this district. *See Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:21-cv-463 (E.D. Tex.) ("*Samsung I*"), *Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:21-cv-293 (E.D. Tex.) ("*Samsung II*").

13. Venue is also proper for Avnet because it maintains a regular and established place of business in this judicial district at 3101 E. President George Bush Highway, Suite 250, Richardson, TX 75082 and has committed acts of infringement in this judicial district. Specifically, Avnet offers for sale and distributes its products, including the Accused Instrumentalities supplied by Samsung, all throughout the United States, including the State of Texas and the Eastern District of Texas. Avnet's website, https://www.avnet.com/americas/, has an (800) contact number that prospective customers can call to obtain more information or a quote for the Accused Instrumentalities (and other products). Avnet's website also specifically targets customers in Texas, including those in the Eastern District of Texas, by providing region-specific

email contact, including dallas@avnet.com.[1] Furthermore, Avnet's website advertises products for sale and lead times, including certain Accused Instrumentalities manufactured by Samsung, as shown below:



[2]

14. Therefore, Samsung, together with Avnet as the distributor of the Accused Instrumentalities, have offered to sell, have sold, and have intentionally and voluntarily placed infringing products into the stream of commerce with the expectation and understanding that those products will be sold, purchased, and/or used by its customers in the State of Texas, including the Eastern District of Texas.

III. FACTUAL ALLEGATIONS

A. Background

15. Since its founding in 2000, Netlist has been a leading innovator in high-performance memory module technologies. Netlist designs and manufactures a wide variety of high-performance products for the cloud computing, virtualization and high-performance computing markets. Netlist's technology enables users to derive useful information from vast amounts of data in a shorter period of time. These capabilities will become increasingly valuable as the volume of data continues to dramatically increase. Netlist has secured multiple jury verdicts

[1] *Locations: Avnet Americas*, Avnet (last visited July 28, 2025), https://www.avnet.com/americas/about-avnet/locations/.

[2] *Products*, Avnet (last visited July 28, 2025), https://www.avnet.com/americas/products/c/search?search=Samsung%20DDR5&page=1&limit=20&orderby=&orderbydirection=asc&__c_HomeTabList=PLT.

confirming the commercial success of its inventions. For example, in 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist $303.15 million in damages. *See* Verdict at 7, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:21-cv-463, Dkt. 479 (E.D. Tex. Apr. 21, 2023). As another example, in May 2024, a jury in the Eastern District of Texas awarded Netlist $445 million in damages against Micron, another dominant memory module manufacturer. *See* Verdict at 5, *Netlist, Inc. v. Micron Tech., Inc.*, No. 2:22-cv-294, Dkt. 135 (E.D. Tex. May 23, 2024). And in November 2024, a jury found that Samsung willfully infringed three Netlist patents and awarded Netlist $118 million in damages. *See* Verdict at 7, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:22-cv-293, Dkt. 847 (E.D. Tex. Nov. 22, 2024).

16. Netlist has a long history of being the first to market with disruptive new products such as the first load-reduced dual in-line memory module ("LRDIMM"), HyperCloud®, based on Netlist's distributed buffer architecture later adopted by the industry for DDR4 LRDIMM. Netlist was also the first to bring NAND flash to the memory channel with its NVvault® NVDIMM. Netlist's pioneering NVDIMM products utilized the same on-module power management technology found on newer-generation DDR5 DIMMs. These innovative products built on Netlist's early pioneering work in areas such as embedding passives into printed circuit boards to free up board real estate, doubling densities via quad-rank double data rate (DDR) technology, and other off-chip technology advances that result in improved performance and lower costs compared to conventional memory.

17. In many commercial products, a memory module is a printed circuit board that contains, among other components, a plurality of individual memory devices (such as DRAMs). The memory devices are typically arranged in "ranks," which are accessible by a processor or memory controller of the host system. A memory module is typically installed into a memory slot on a computer motherboard.

18. Memory modules are designed for, among other things, use in servers such as those supporting cloud-based computing, artificial intelligence, and other data-intensive applications, as well as in consumer applications such as PCs and laptops. Memory modules are typically characterized by, among other things, the generation of DRAM on the module (*e.g.*, DDR5, DDR4, DDR3) and the type of module (*e.g.*, UDIMM, SODIMM, RDIMM).

B. U.S. Patent No. 12,373,366

19. The ’366 Patent is entitled “Memory with On-Module Power Management.”

20. Netlist owns by assignment the entire right, title, and interest in and to the ’366 Patent. The ’366 Patent was filed as Application No. 17/582,797 on January 24, 2022, issued as a patent on July 29, 2025 and claims priority to, among others, U.S. Application No. 13/559,476 filed on July 26, 2012; U.S. Application No. 12/240,916 filed on September 29, 2008; U.S. Application No. 12/131,873 filed on June 2, 2008; as well as to two provisional applications, filed on June 1, 2007 (No. 60/941,586) and July 28, 2011 (No. 61/512,871).

21. Samsung had pre-suit knowledge of the ’366 Patent no later than May 17, 2022. *See Samsung Elecs. Co. Ltd. v. Netlist, Inc.*, IPR2022-00996, Paper 1. Samsung also gained knowledge of the ’366 Patent via this Complaint.

22. Claim 1 of the ’366 Patent provides:

> [**1pre**] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:
>
> [**1a**] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:
>
> > a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the

power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

[**1b**] a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

(i) monitor an input voltage supplied via the input voltage supply line;

(ii) generate a trigger signal upon detecting a trigger condition; and

(iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

[**1c**] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

[**1d**] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,

[**1e**] wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

- the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

- the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data

lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

C. Defendants' Infringing Activities

23. Samsung is a global technology company and one of the largest manufacturers of semiconductor memory products such as DRAM, NAND Flash, and MCP (Multi-Chip Package). Samsung develops, manufactures, sells, offers to sell, and imports into the United States memory components and memory modules designed for, among other things, use in servers such as those supporting cloud-based computing, artificial intelligence, and other data-intensive applications as well as use in consumer applications such as in PCs, laptops, and gaming.

24. Samsung and Netlist were initially partners under a 2015 Joint Development and License Agreement ("JDLA"). Samsung used Netlist's technologies to develop products both in mature markets such as those for DDR4 memory modules and emerging markets for new generations of DRAM technologies, including DDR5. Under the JDLA, Samsung was obligated to supply Netlist certain memory products at competitive prices. Samsung, however, did not honor its promises and repeatedly failed to fulfill Netlist's product orders. As a result, Netlist terminated the JDLA on July 15, 2020, which termination was found effective by a federal district court in the Central District of California in 2021. *See* Order at 22, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 8:20-cv-993, Dkt. 186 (C.D. Cal. Oct. 14, 2021).

25. Samsung appealed that decision, and the Ninth Circuit partially reversed the district court's summary judgment ruling. Following remand, the contract action in the Central District of California proceeded to a jury trial. On May 17, 2024, the jury returned a verdict finding that Netlist's interpretation of the JDLA's supply provision was correct, and Samsung's breach of that provision was material. *See* Verdict, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 8:20-cv-993, Dkt. 556 (C.D. Cal. May 17, 2024).

26. Upon Samsung's motion, the district court vacated the jury's verdict and ordered a new trial. That trial took place in March 2025. Again, the jury returned a verdict finding that Netlist's interpretation of the JDLA's supply provision was correct. *See* Verdict, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 8:20-cv-993, Dkt. 769 (C.D. Cal. Mar. 24, 2025). Samsung's latest motion for a new trial is currently pending. *See* Order, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 8:20-cv-993, Dkt. 810 (C.D. Cal. July 17, 2025) (scheduling evidentiary hearing regarding Samsung's motion for a new trial for July 30, 2025).

27. In April 2023, a jury in the Eastern District of Texas found that Samsung willfully infringed five Netlist patents and awarded Netlist $303.15 million in damages, including $147,225,000 for U.S. Pat. Nos. 11,016,918 and 11,232,054—asserted against Samsung's DDR5 memory modules. *See* Verdict at 7, *Netlist, Inc. v. Samsung Elecs. Co.*, No. 2:21-cv-463, Dkt. 479 (E.D. Tex. Apr. 21, 2023).

28. Avnet "is one of the largest distributors of electronic components, computer products and embedded technology."[3] As an authorized distributor of Samsung memory products,[4] Avnet "accelerates its partners' success by connecting the world's leading technology suppliers with a broad base of customers by providing cost-effective, value-added services and solutions."[5] Avnet is involved in the use, offering for sale and/or sales of certain semiconductor products, including the Accused Instrumentalities as defined below.

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[3] *Avnet, Inc. Names Rodney C. Adkins to Its Board of Directors*, SEC (June 15, 2015), https://www.sec.gov/Archives/edgar/data/8858/000129993315000942/exhibit1.htm.

[4] *Samsung*, Avnet (last visited July 28, 2025), https://www.avnet.com/americas/manufacturers/m/samsung/.

[5] *Avnet, Inc. Names Rodney C. Adkins to Its Board of Directors*, *supra*.

D. DDR5 Memory Modules

29. The Accused DDR5 Products include, without limitation, any Samsung DDR5 products made, sold, offered for sale, used and/or imported into the United States by Defendants. By way of non-limiting example, the accused DDR5 memory modules include Samsung's DDR5 RDIMMs and other products with similar structures and features. As further example, the Accused Instrumentalities include, without limitation, any DDR5 products made, sold, offered for sale, used and/or imported into the United States by Samsung, including those modules utilizing Samsung's own power management IC, including at least PMIC components having the following part numbers: S2FPC01, S2FPD01, and S2FPD02.[6] The Accused DDR5 Products also include any DDR5 products sold, offered for sale, used and/or imported into the United States by Samsung that include PMICs supplied by third parties.

30. Each of the DDR5 memory modules includes a plurality of connections at the edge through which command/address signals are received from a memory controller of the host computer system and data is exchanged with the memory controller.

31. DDR5 memory modules introduced important upgrades over DDR4 modules. For example, it introduced the feature of two 40-bit (32 data bits plus 8 ECC bits) channels that can operate independently. This feature, combined with a new default burst length of 16 in the DDR5 component allows a single burst to access 64B of data in a typical CPU cache line using only one of the independent channels which in turn permits interleaving accesses from the two independent channels. This leads to significant improvement in concurrency, bandwidths and performance.

32. To accommodate increased data rates, DDR5 memory modules also moved the power management from the motherboard onto the module itself, leading to more precise voltage

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[6] *See, e.g.*, *Product Brief: S2FPD01 Power IC*, Samsung (2022), https://download.semiconductor.samsung.com/resources/brochure/S2FPD01%20Power%20IC.pdf.

control needed for high data rates as well as a reduction in power loss. Samsung notes on its website that its DDR5 modules include an "on-DIMM PMIC" that "further boosts power management efficiency and power supply stability."[7] Furthermore, "[o]ne major design improvement to the newest generation DRAM solution involves integrating the PMIC into the memory module—previous generations placed the PMIC on the motherboard—offering increased compatibility and signal integrity, and providing a more reliable and sustained performance."[8]

IV. FIRST CLAIM FOR RELIEF – '366 Patent

33. Netlist re-alleges and incorporates by reference the allegations of the preceding paragraphs of this Complaint as if fully set forth herein.

34. Upon information and belief, Defendants directly infringed and are currently infringing at least one claim of the '366 Patent by, among other things, making, using, selling, offering to sell, and/or importing within this District and elsewhere in the United States, without authority, the Accused DDR5 DIMMs, and other products with materially the same structure in relevant part. For example, and as shown below, the accused DDR5 RDIMMs and other products with materially the same structures in relevant parts infringe at least one claim of the '366 Patent.

35. The allegations below are based upon Netlist's current information and belief. Internal documentation from Defendants, including confidential Samsung product specifications and source code, will show infringement. The examples provided below are not intended to be, and should not be understood as, limiting in any way.

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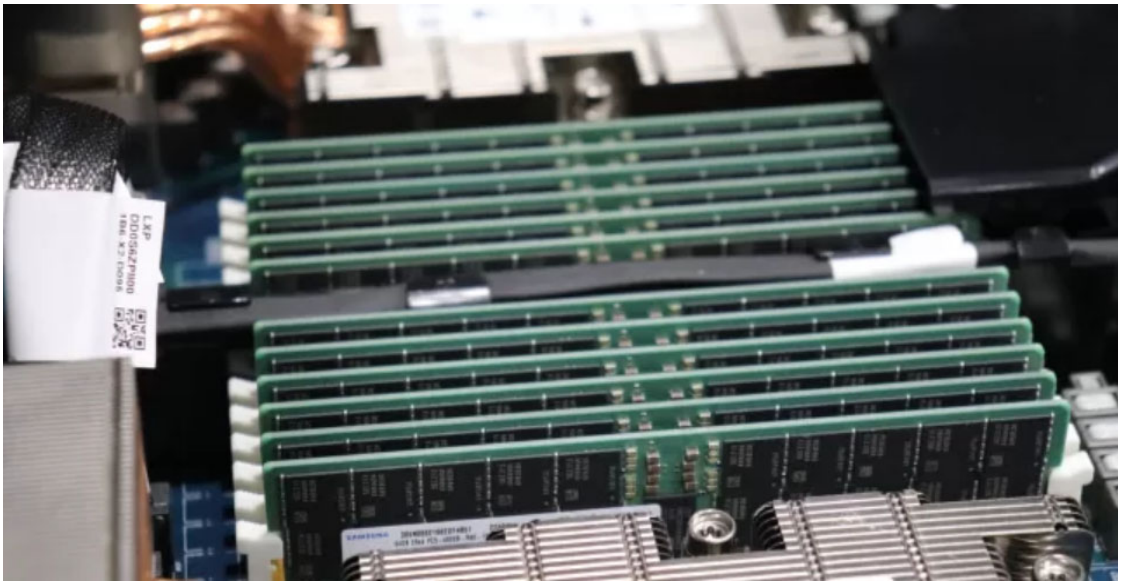
[7] *DDR5 Ushers in Data-Centric Innovation*, Samsung (last visited July 28, 2025), https://semiconductor.samsung.com/dram/ddr/ddr5/.

[8] *Samsung Unveils New Power Management Solutions for DDR5 Modules*, Samsung (May 18, 2021), https://news.samsung.com/global/samsung-unveils-new-power-management-solutions-for-ddr5-modules.

36. To the extent the preamble is limiting, the Accused DDR5 Products are DIMMs "configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits."

37. For example, a Samsung DDR5 RDIMM module fits into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits [*e.g.*, Vin_Bulk, Vin_Mgmt, and VSS], a set of data conduits [*e.g.*, DIMM's memory channels (A and B)], and a set of address and control conduits [*e.g.*, Command and Address (CA) Bus], wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits.

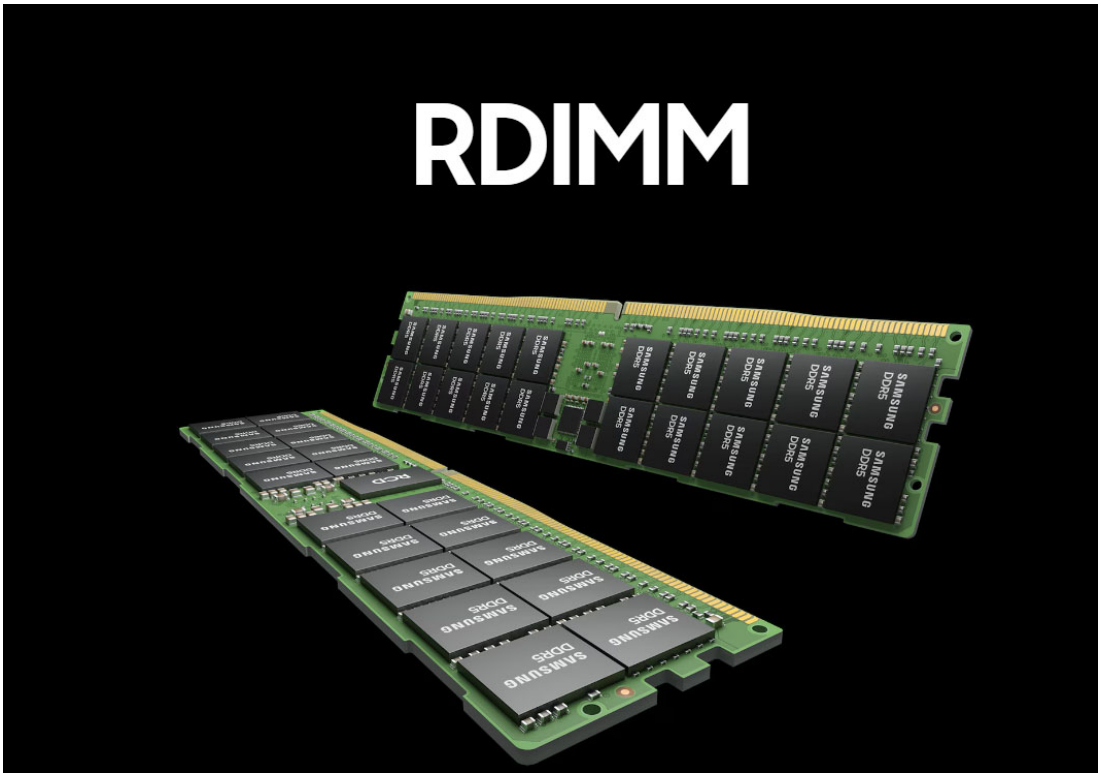


[9]

[9] Michael Larabel, *DDR5 Memory Channel Scaling Performance with AMD EPYC 9004 Series*, Phoronix (Jan. 6, 2023), https://www.phoronix.com/review/ddr5-epyc-9004-genoa (describing "performance across varying numbers of populated DDR5 memory channels" and

38. The Accused DDR5 Products are DIMMs comprising "a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board."

39. For example, a Samsung DDR5 RDIMM comprises a PCB that includes edge connections, *i.e.*, "gold fingers," that fit into the memory slot connector of the system board, as shown below:



[10]

40. The Accused DDR5 Products contain a PCB that includes "a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,

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noting that "[a]ll of the memory was 64 GP DDR5-4800MT/S Samsung . . . memory modules[.]").

[10] *RDIMM*, Samsung (last visited July 28, 2025), https://semiconductor.samsung.com/dram/module/rdimm/.

wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM."

41. For example, as shown below,[11] a Samsung DDR5 RDIMM's PCB includes a first set of edge connections (*e.g.*, at pins specifically configured for receiving power and ground supplies) configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits. The DIMM power supply is delivered from the system to the PMIC.

Need to support 12V power line inside motherboard

Voltage converter for memory was located in the system and converts 12V to 1.2V and delivers power to DIMM socket directly. But 12V power line is directly connected to DIMM socket from DDR5 and built in VR converts to 1.1V, which delivers power to DRAM. As VR disappears from system, the system design has the advantage of being simplified, but on the contrary, the memory module need a lot of components. As such, the number of various components such as PMIC, Power Inductor, and MLCC will increase. From a server and network system designer's point of view, power line voltage from PSU to DIMM socket will be increased from 1.2V to 12V, so the system needs new 25V MLCC which need to be located as close to the DIMM socket as possible.

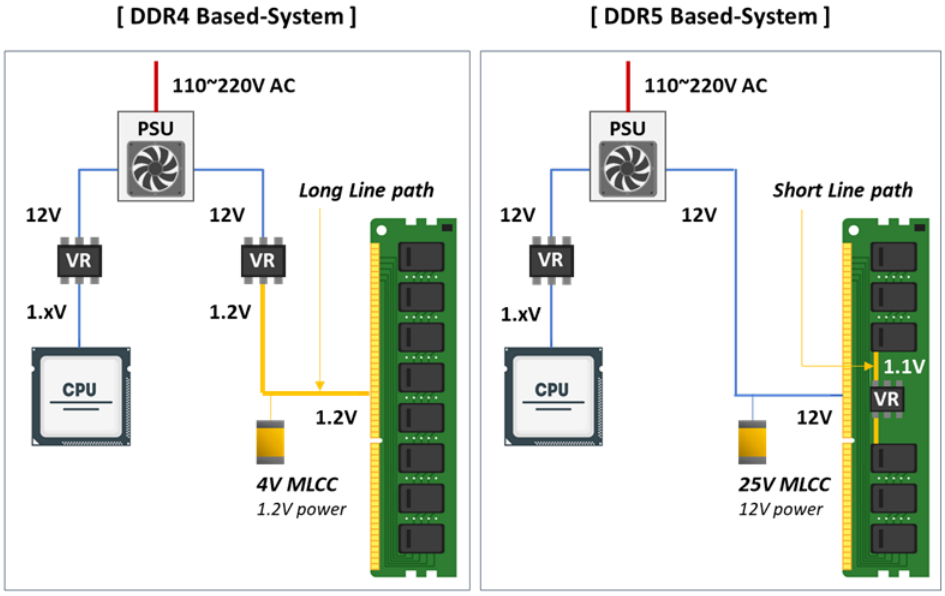


Figure2. DDR4 Based-system vs DDR5 Based-system

42. The Accused DDR5 Products contain a PCB that includes "a second set of edge connections configured to be electrically connected to the set of data conduits" (*e.g.*, pins for DQ

[11] *Memory VR Changes in the System by DDR5 Adoption*, Samsung Electro-Mechanics (Mar. 29, 2022), https://www.samsungsem.com/global/newsroom/news/view.do?id=5026.

and ECC signals) and "a third set of edge connections configured to be electrically connected to the set of address and control conduits" (*e.g.*, edge connections for address and control signals).

43. The Accused DDR5 Products also contain a PCB that includes "a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM," such as a set of voltage supply lines that are electrically connected to the first set of edge connections (power and ground pins) and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board when the DIMM is fitted into the memory slot connector.

44. The Accused DDR5 Products contain a PCB that includes "a set of data lines [*e.g.*, DQ and error check bit lines] electrically connected to the second set of edge connections [*e.g.*, pins for data (DQ) and error check bits]."

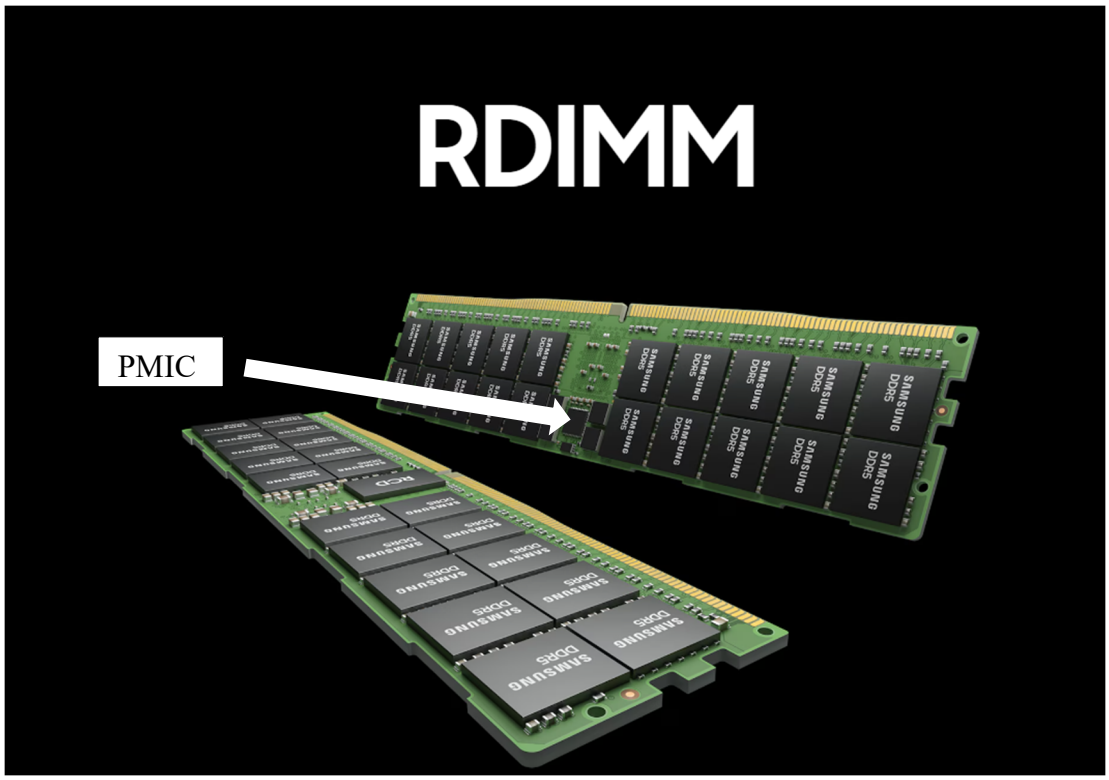
45. For example, a Samsung DDR5 RDIMM's PCB includes data lines that are electrically connected to the second set of edge connections. That is, each DQ edge connection is electrically connected respectively to a DQ pin of the memory slot connector when the DIMM is fitted into the memory slot connector.

46. The Accused DDR5 Products contain a PCB that includes "a set of address and control lines electrically connected to the third set of edge connections."

47. For example, a Samsung DDR5 RDIMM's PCB includes a set of address and control lines, each of which is a line that is electrically connected to one designated edge connection.

48. The Accused DDR5 Products are DIMMs comprising "a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines."

49. For example, a Samsung DDR5 RDIMM module comprises a controller (*e.g.*, PMIC) that includes a voltage monitor circuit and nonvolatile memory. The PMIC, which includes a voltage monitor and nonvolatile memory, is coupled to the PCB, as shown in the annotated figure below:



[12]

50. The Accused DDR5 Products contain a voltage monitor circuit configured to "monitor an input voltage supplied via the input voltage supply line."

[12] *RDIMM*, Samsung (last visited July 28, 2025), https://semiconductor.samsung.com/dram/module/rdimm/.

51. For example, a Samsung DDR5 RDIMM's PMIC is connected to an input voltage supply line (*e.g.*, Vin_Bulk) and includes a voltage monitor circuit to actively monitor the input voltage supply line.

52. The Accused DDR5 Products contain a voltage monitor circuit configured to "generate a trigger signal upon detecting a trigger condition."

53. For example, a Samsung DDR5 RDIMM's PMIC's voltage monitor circuit is configured to generate a trigger signal indicating when a Vin_Bulk overvoltage condition has occurred.

54. The Accused DDR5 Products contain a voltage monitor circuit configured to "transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage."

55. For example, a Samsung DDR5 RDIMM's PMIC's voltage monitor circuit is configured to transmit the generated trigger signal to circuitry within the PMIC, that is, the command (trigger condition) is transmitted internally to at least one other portion of the controller, which could be (1) circuitry configured to execute a power down sequence in response to the generated command, and/or (2) the generated trigger signal is captured by writing binary code into real time status registers indicating the Vin_Bulk overvoltage has occurred. The event triggers would lead to actions that include updating memory spaces in the non-volatile memory through a write operation.

56. The Accused DDR5 Products comprise "a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to

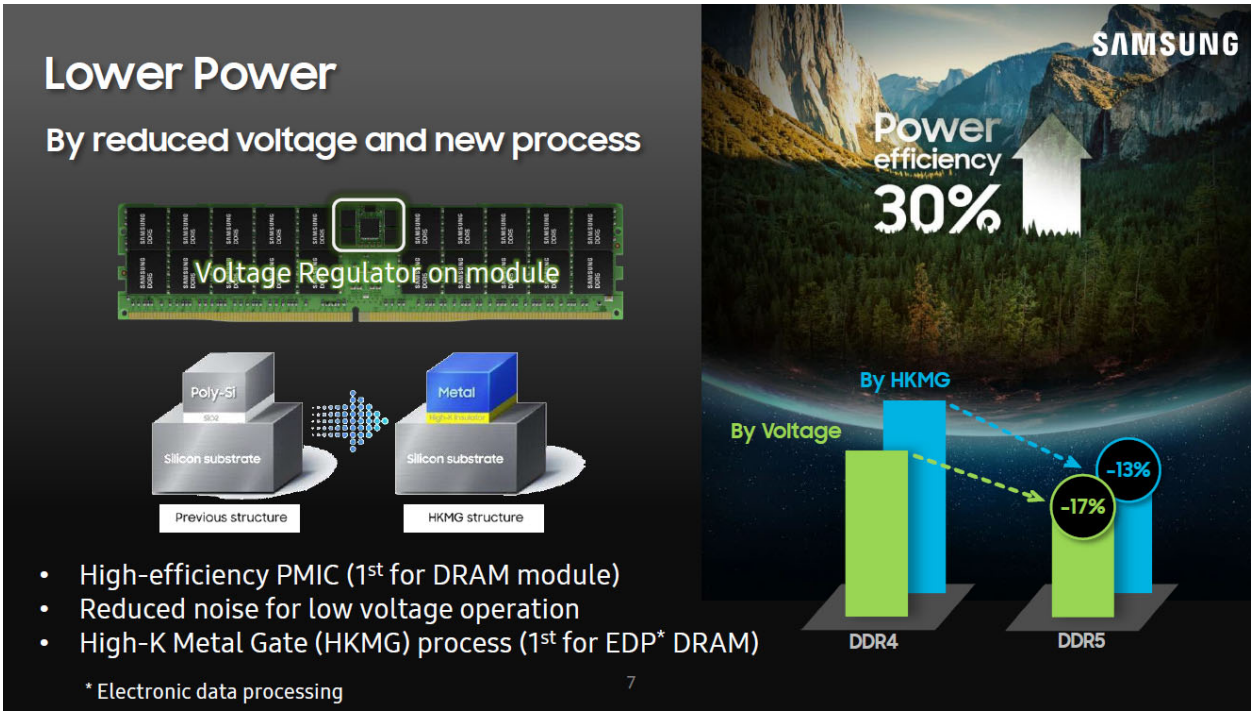
the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines."

57. For example, a Samsung DDR5 RDIMM further comprises a set of components coupled to the PCB. These include DDR5 SDRAM memory devices, a register clock driver (RCD), PMIC, and temperature sensors. The DDR5 SDRAM devices are coupled to (1) the set of address and control lines via the RCD, and (2) to the set of data lines for data signals. The DDR5 SDRAM devices are configured to receive or output data signals via the set of data lines based on address and control signals received from the output of the RCD based on the set of address and control signals received by the RCD. Each of the DDR5 SDRAM devices include data pins connected to specific data lines of the set of data lines, and the address and control pins connected to the RCD's address and control output pins.

58. On information and belief, the Accused DDR5 products comprise "first, second, third, a fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines."

59. For example, as shown below,[13] a Samsung DDR5 RDIMM's PMIC comprises circuitry that makes up four converter circuits, each of which is configured to receive power from the input voltage supply line (*e.g.*, Vin_Bulk and/or Vin_MGMT), as described above, and to deliver regulated power via first, second, third, and fourth regulated voltage lines.

[13] Sung Joo Park et al., *Industry's First 7.2 Gbps 512GB DDR5 Module*, Hot Chips (last visited July 28, 2025), https://hc33.hotchips.org/assets/program/posters/HC2021.Samsung.SungJooPark.v03.pdf.



Need to support 12V power line inside motherboard

Voltage converter for memory was located in the system and converts 12V to 1.2V and delivers power to DIMM socket directly. But 12V power line is directly connected to DIMM socket from DDR5 and built in VR converts to 1.1V, which delivers power to DRAM. As VR disappears from system, the system design has the advantage of being simplified, but on the contrary, the memory module need a lot of components. As such, the number of various components such as PMIC, Power Inductor, and MLCC will increase. From a server and network system designer's point of view, power line voltage from PSU to DIMM socket will be increased from 1.2V to 12V, so the system needs new 25V MLCC which need to be located as close to the DIMM socket as possible.

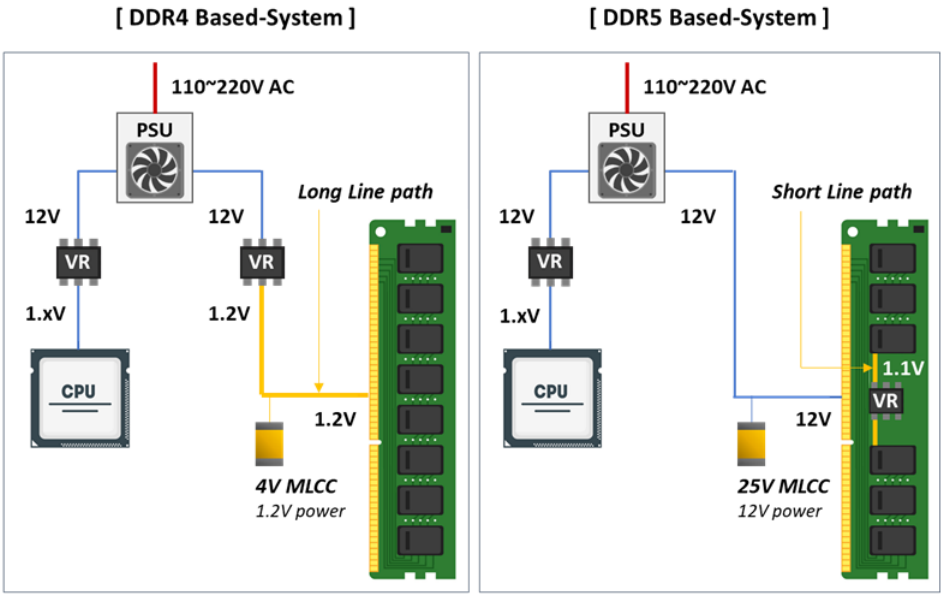


Figure2. DDR4 Based-system vs DDR5 Based-system

60. The Accused DDR5 Products comprise a set of components that includes "a first component configured to receive power via at least the first regulated voltage line."

61. For example, a Samsung DDR5 RDIMM includes components such as DDR5 SDRAM devices, RCD, Hub and temperature sensors that are specified to receive one or more of the first, second, third, and fourth regulated voltages which are generated by the first, second, third, and fourth converter circuits configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines. A first component may be the SPD_Hub component, which receives power via at least a first regulated voltage. Alternatively, the first component may be an SDRAM D01 component that receives power via an alternate first regulated voltage.

62. The Accused DDR5 Products comprise a set of components that includes "a second component configured to receive power via at least the second regulated voltage line."

63. For example, a Samsung DDR5 RDIMM includes a second component, which may be the RCD component that receives power at least via VDDIO (also referred to as VIO). The RCD component receives two regulated voltages, VDDIO and VDD.

64. The Accused DDR5 Products comprise a set of components that includes "a third component configured to receive power via at least the third regulated voltage line."

65. For example, a Samsung DDR5 RDIMM includes a third component, which may be the SDRAM D02 component that receives power via at least VDD.

66. The Accused DDR5 Products comprise a set of components that includes "a fourth component configured to receive power via at least the fourth regulated voltage line."

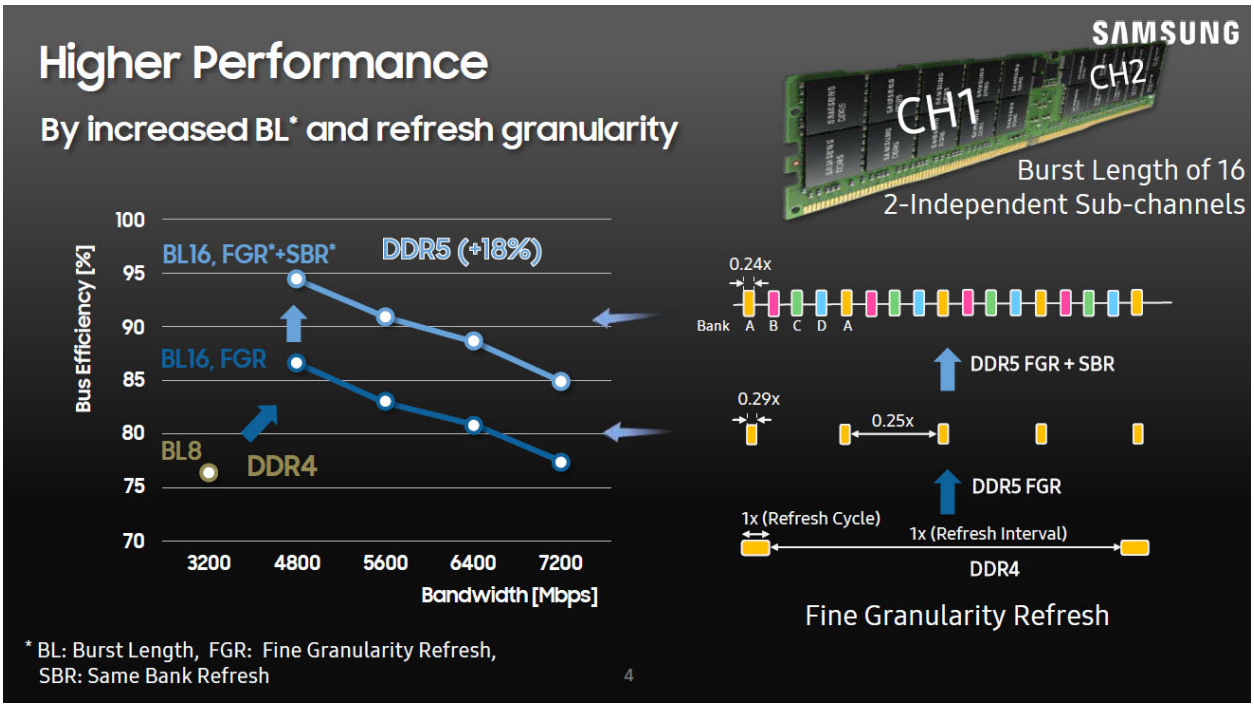
67. For example, a Samsung DDR5 RDIMM includes a fourth component, which may be the SDRAM D03 component that receives power at least via VPP.

68. The Accused DDR5 Products comprise a set of components as described above, wherein each component of the set of components "is electrically connected to one or more of the

first, second, third, and fourth regulated voltage lines" and "receives power only via the one or more of the first, second, third, and fourth regulated voltage lines."

69. The Accused DDR5 Products comprise a plurality of DDR SDRAM devices that includes "a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal."

70. For example, as shown below,[14] a Samsung DDR5 RDIMM module includes a first chip select line connected to each of a first group of at least 5 SDRAM devices (Channel A) and a second chip select line connected to each of a second group of at least 5 SDRAM devices (Channel B). In the case of 80-bit DDR5 RDIMM, each of Channel A and Channel B are designed to receive or output 40-bit DDR data signals independently of each other by using separate chip select signal groups for Channel A and Channel B. The SDRAMs are x4 or x8 for DDR5 RDIMMs, such that each channel includes five SDRAMs for x8 and 10 SDRAMs for x4.



[14] Sung Joo Park et al., *supra*.

71. The Accused DDR5 Products comprise a plurality of DDR SDRAM devices that include "a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal."

72. For example, as explained above, a Samsung DDR5 RDIMM includes a second chip select line connected to each of a second group of at least 5 SDRAM devices.

73. In the Accused DDR5 Products, when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode, "the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines."

74. For example, a Samsung DDR5 RDIMM includes an RCD that receives a first chip select signal for Channel A and outputs a corresponding signal to the first group of SDRAM, and receives a second chip select signal for Channel B and outputs a corresponding signal to the second group of SDRAM. When Vin_Bulk, Vin_Mgmt and ground rails are provided to the DDR5 RDIMM and received by the PMIC, the system generates the four regulated voltages that are used to power the set of components on the DIMM, including the first and second groups of DDR SDRAM. After the initialization process, when the DDR5 RDIMM receives independent read or write commands for either Channel A or Channel B, the RCD output corresponding commands to the first or second groups of DDR SDRAM. The output commands in turn enable Channel A or Channel B to receive or output data via data lines in accordance with executing the read or write

operation. The self-refresh state is a deep power saving state where no access to the SDRAM is possible.

75. In the Accused DDR5 Products, when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode, "the at least 40 1-bit DDR data signals [that are received or output in response the received C/A signals] include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals."

76. For example, in a Samsung DDR5 RDIMM, the number of data lines per channel (A and B) is 40, including 32 bits of data and 8 bits of error correction data (also called error check bits).

77. In the Accused DDR5 Products, "the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits."

78. For example, in a Samsung DDR5 RDIMM, each of Channel A and Channel B is designed to receive or output 40 bits of DDR data signals independently of one another by using separate chip select signals. The sum of the data lines of Channel A and Channel B is 80 data lines, which equals a total number of data conduits of 80 data conduits, which is greater than at least 72 data conduits.

79. On information and belief, Defendants also indirectly infringe the '366 Patent, as provided in 35 U.S.C. § 271(b), by inducing infringement by others, such as Defendants' customers and end users, in this District and elsewhere in the United States. For example, on information and belief, Defendants have induced, and currently induce, infringement of the '366 Patent through their affirmative acts of selling, offering to sell, distributing, and/or otherwise making available the Accused DDR5 Products and other materially similar products that

infringement the ’366 Patent. On information and belief, Defendants provide specifications, datasheets, instruction manuals, and/or other materials that encourage and facilitate infringing uses of the Accused Instrumentalities and other materially similar products by users in a manner that they know or should have known would result in infringement and with the intent of inducing infringement. On information and belief, Samsung is encouraging and facilitating infringement of the ’366 Patent by others. For example, on information and belief, Samsung sells or otherwise provides the Accused Instrumentalities to distributors or U.S.-based sales entities, including but not limited to Avnet, knowing that these entities intend to make, use, offer for sale, and/or sell the Accused Instrumentalities within the United States and/or import the Accused Instrumentalities into the United States in an infringing manner.

80. On information and belief, Defendants also indirectly infringe the ’366 Patent, as provided in 35 U.S.C. § 271(c), contributing to direct infringement committed by others, such as customers and end users, in the Eastern District of Texas and elsewhere in the United States. For example, on information and belief, Defendants have contributed to, and currently contribute to, Defendants’ customers’ and end-users’ infringement of the ’366 Patent through their affirmative acts of selling and offering to sell, either directly or through distributors, in this District and elsewhere in the United States, the Accused DDR5 Products and other materially similar products that infringe the ’366 Patent. On information and belief, the Accused Instrumentalities and other materially similar products have no substantial noninfringing uses, and constitute a material part of the patented invention. On information and belief, Defendants are aware that the product or process that includes the Accused DDR5 Products and other materially similar products may be covered by one or more claims of the ’366 Patent. On information and belief, the use of the product or process that includes the Accused DDR5 Products and other materially similar products infringes at least one claim of the ’366 Patent.

81. Samsung's infringement of the '366 Patent has damaged and will continue to damage Netlist. Samsung has had actual notice of the '366 Patent since at least the filing of this Complaint. Samsung's infringement of the '366 Patent is willful. Samsung continues to commit acts of infringement despite a high likelihood that its actions constitute infringement, and Samsung knew or should have known that its action constituted an unjustifiably high risk of infringement.

82. Avnet's infringement of the '366 Patent has damaged and will continue to damage Netlist. Avnet has had actual notice of the '366 Patent since at least the filing of this Complaint. Avnet's infringement of the '366 Patent is willful. Avnet continues to commit acts of infringement, including advertising, marketing, offering to sell and/or selling the Accused Instrumentalities, despite a high likelihood that its actions constitute infringement, and Avnet knew or should have known that its actions constituted an unjustifiably high risk of infringement.

V. DEMAND FOR JURY TRIAL

83. Pursuant to Federal Rule of Civil Procedure 38(b) and Local Rule CV-38, Netlist demands a trial by jury on all issues triable to a jury.

VI. PRAYER FOR RELIEF

WHEREFORE, Netlist respectfully requests that this Court enter judgment in its favor ordering, finding, declaring, and/or awarding Netlist relief as follows:

A. that Defendants infringe the '366 Patent;

B. all equitable relief the Court deems just and proper as a result of Defendants' infringement;

C. an award of damages resulting from Defendants' acts of infringement in accordance with 35 U.S.C. § 284;

D. that Samsung's infringement of the '366 Patent is willful;

E. that Avnet's infringement of the '366 Patent is willful;

F. enhanced damages pursuant to 35 U.S.C. § 284;

G. that this is an exceptional case and awarding Netlist its reasonable attorneys' fees and costs pursuant to 35 U.S.C. § 285;

H. an accounting for acts of infringement and supplemental damages, without limitation, prejudgment and post-judgment interest; and

I. in the alternative to an award of damages under 35 U.S.C. § 284, an order pursuant to 35 U.S.C. § 283 permanently enjoining Defendants, their distributors, officers, agents, servants, employees, attorneys, instrumentalities, and those persons in privity, active concert, or participation with them, from further acts of direct and/or indirect infringement of the '366 Patent, including the manufacture, sale, offer for sale, importation, and/or use of the Accused Instrumentalities.

J. such other equitable relief which may be requested and to which Netlist is entitled.

Dated: July 28, 2025

Respectfully submitted,

/s/ Jennifer Truelove

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