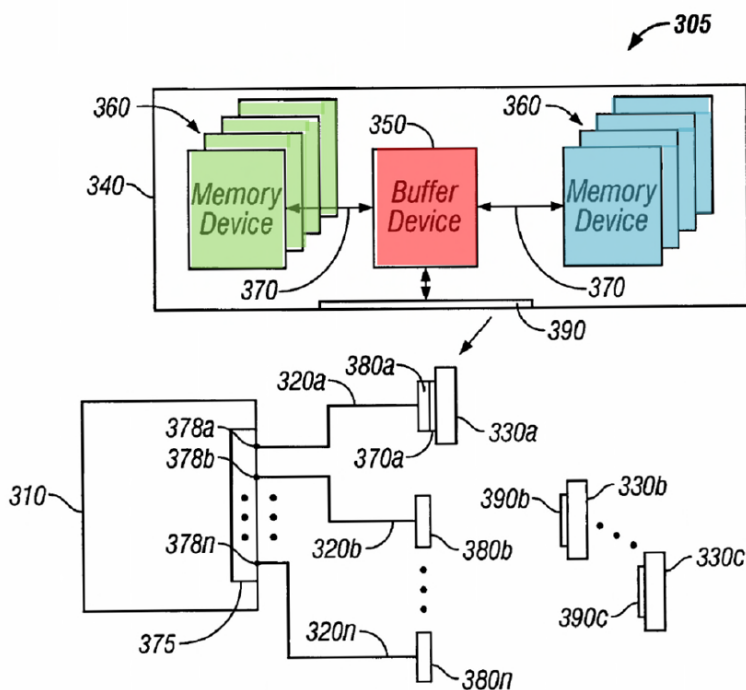


**EX1113: Invalidity Claim Chart for
Ground 2 (Perego + Harris + Amidi)**

Claim 1 (independent)

[1.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,

Perego discloses a “dual in-line memory module (DIMM) [330, 340, 395] configured to fit into a memory slot connector [380] of a system board [(“common substrate”)] of a computer system [including memory system 305].” EX1035 (Perego) at Fig. 3B (below, annotated).



Perego explains that “each of memory subsystems 330a–330c is a buffered memory module” which include “connectors 390a–390c,” e.g., “edge connectors,” that fit into “mating connectors 380a–380n” which can be “socket connectors” “attached to a common substrate shared with point-to-point links 320a–320n and controller 310.” *Id.* at 5:56–6:11 and 6:57–62. Perego also discloses that its “memory subsystems” are included in “an overall system, for example, a computer system.” *Id.* 4:13–17.

Perego discloses further details of the connector 390a with reference to its Fig. 3C. EX1035 (Perego) at Fig. 3C (below, annotated).

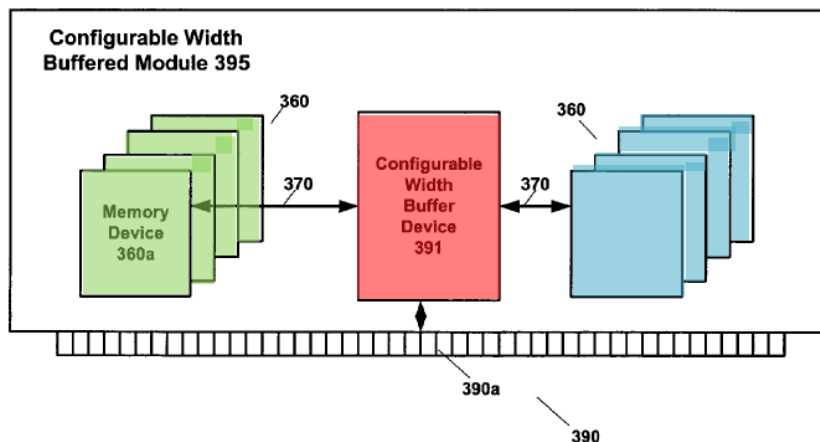
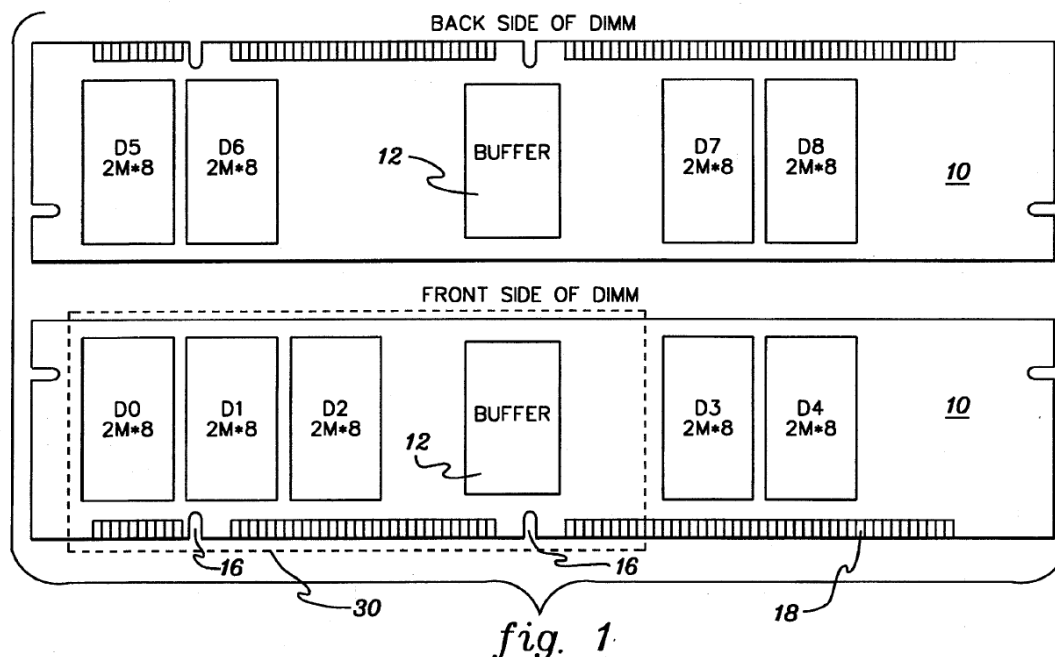


Fig. 3C

Fig. 3C shows one side of buffered module 395, and a Skilled Artisan would have understood that separate memories and edge connectors can be on both sides of the module PCB, which was known as a “*dual in-line memory module (DIMM)*” for more than a decade at the time. Perego also discloses socket and connector interfaces for DIMMs. *Id.* at 1:58-2:6 (describing DIMMs and referencing U.S. Pat. No. 5,513,135 to Dell et al., “Dell”), 6:25-33 (“the conventional DIMM module”); EX1108 (Dell) at Fig. 1 (edge connectors on both sides of a DIMM) and 1:65-2:20 (“Single in-line memory modules (SIMMs) are compact circuit boards designed to accommodate surface mounted memory chips, such as DRAMs. ... A DIMM essentially comprises a SIMM wherein memory chips are surface mounted to opposite sides of the circuit board, and the connector tabs are unique on each side. ... A significant portion of the connectors, motherboards, etc., presently marketed for DIMM packages are configured to accommodate this ... configuration for main memory.”).



See also EX1051 (Doblar) at [0043-47], Figs. 1-5 (DIMMs with edge connector pins and mating connector sockets).

Harris also discloses that memory modules “may be implemented as a Dual In-Line Memory Module (DIMM),” rendering obvious the Perego-Harris combination using a DIMM format for its memory module. EX1023 (Harris) at [0009]. Harris further discloses that DIMMs “are powered from system board or main board voltage sources,” and its invention allows “reduction in the pin count on DIMM connector to system board,” rendering obvious that the DIMM of the Perego-Harris combination is “*configured to fit into a memory slot connector of a system board*” through which it also receives power. *Id.* [0002], [0019]; EX1003, ¶¶153-170.

Similarly, Amidi discloses to a Skilled Artisan implementing its module in a DIMM format, including a card interface 360 with edge connector pins on both sides of a PCB memory card. EX1024 (Amidi) at Figs. 3 and 4, 3:49-63.

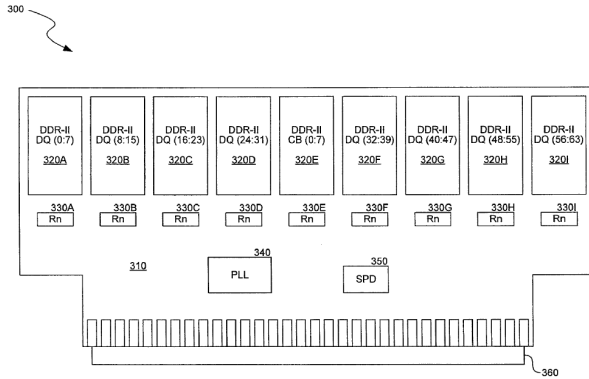


FIG. 3

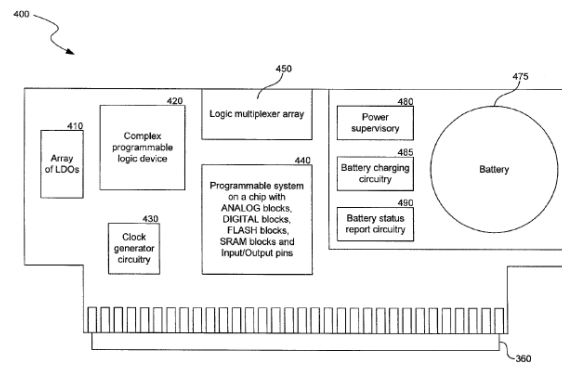


FIG. 4

Accordingly, Ground 2 discloses a “*dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system.*”

[1.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,

Perego expressly discloses “*the memory slot connector [380] including ... a set of data conduits [interfacing DQ data signals], and a set of address and control conduits [interfacing RQ address and control signals].*” EX1035 (Perego) at Fig. 4B (below, annotated).

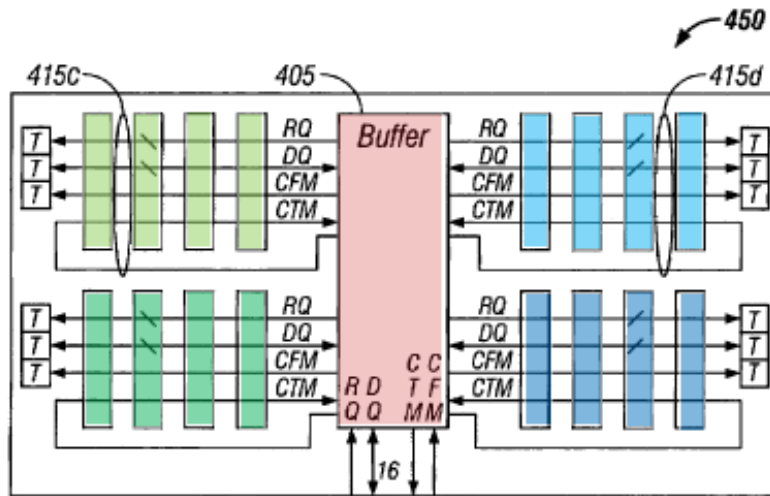


FIG. 4B

As shown in its Fig. 4B, Perego discloses that channels (415) “include control lines (RQ), [and] data lines (DQ)” which may equally apply to links 320 connecting the buffer to the controller. *Id.* 9:43-49 (“Signal lines of channels 415a and 415b

include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM). The varieties of interconnect topologies, interconnect types, clocking methods, signaling references, signaling methods, and signaling apparatus described above in reference to point-to-point links 320a–320n may equally apply to channels 415a and 415b.”). For example, “control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines.” *Id.* at 9:58-60. As shown by the well-known JEDEC standards, “row address strobe” and “column address strobe” lines were standard JEDEC control lines abbreviated as “RAS” and “CAS,” respectively. EX1026 (JESD79-2B), p.6 (“Command Inputs: RAS, CAS and WE (along with CS) define the command entered.”); EX1107 (Jacob paper), p.4 (“DRAM’s RAS pin (*row address strobe*) ... DRAM’s CAS pin (*column address strobe*)”); EX1090, 24-32 (finding Perego compatible with JEDEC standards); EX1091, 28-37 (same).

Perego’s memory module receives the DQ data signals and RQ address/control signals from the system controller via “edge connectors” 390 which fit into corresponding memory slot connectors 380. EX1035 (Perego), Fig.3C (below) Fig.4 (above showing the buffer 405 having “RQ” and “DQ” ports leading to the edge of the module), 13:13-17 (“to provide electrical connections between interface 596 [in the buffer 391, 405] and connector 390 (FIG. 3C)).”

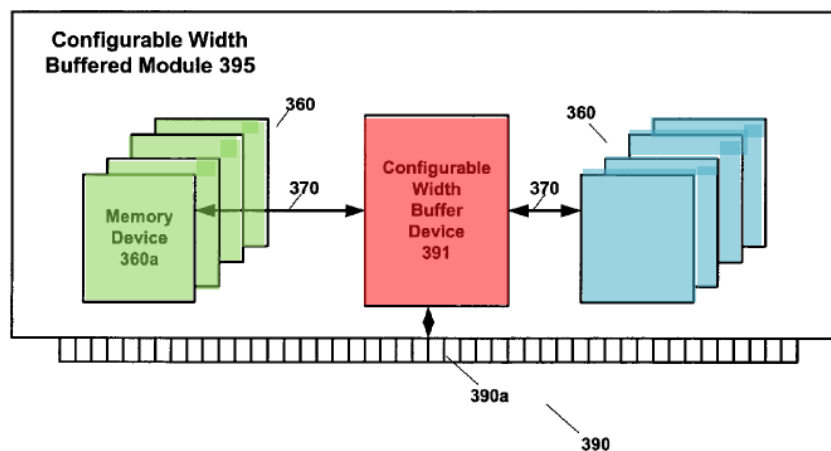


Fig. 3C

Similarly, Harris and Amidi disclose edge connectors by which the memory module communicates data and address/control signals with the system controller, as was common at the time for DIMMs. EX1023 (Harris), ¶¶[0013] (“compatible with...(JEDEC) standards”), [0009] (“buffer/logic component 112... buffering command/address (C/A)...as well as data”), Fig.3 (showing the buffer 112

receiving data and address/control signals via edge connectors); EX1024 (Amidi), Figs. 3, 4, 3:58-62 (“a set of printed conductors on an edge”), 4:1-2 (“Card interface 360 is present on this side as well, providing connectivity.”); EX1108 (Dell), Figs.1-4. Edge connector pins for data signals and those for address/control signals were commonly separate from one another, consistent with the JEDEC standards at the time. See, e.g., EX1108 (Dell), Fig.3 (showing “168 PIN SDRAM DIMM” including separate data (DQ0-DQ79) and control/address (A0-A13, Write Enable, Column Address Strobe (CAS), Row Address Strobe (RAS), CS0-CS4, etc.) pins).

As discussed above, the DQ data lines and RQ control lines on the memory module—which deliver data signals and control/address signals received from the edge connectors 390—“may equally apply” to links 320 between the memory module and the system controller. EX1035 (Perego), 9:45-49. Perego further discloses that “mating connectors 380a-380n interface with [edge] connectors 390” for the module to communicate with the system controller. *Id.*, 6:1-11; see also EX1024, 3:58-62 (“a set of printed conductors on an edge...mat[ing] with a slot or socket...to which memory module 300 is connected”). A Skilled Artisan would have understood from these disclosures that “mating connectors 380a-380n” (“*memory slot connector*”) include “*a set of data conduits*” electrically coupled with the data edge connector pins to interface data and “*a set of address and control conduits*” electrically coupled with the address/control edge connector pins to interface address/control signals.

Thus, the proposed combination discloses “*the memory slot connector including ... a set of data conduits* [interfacing (DQ) data signals], *and a set of address and control conduits* [interfacing (RQ) address and control signals].”

The proposed combination also discloses to a Skilled Artisan that the connector further includes “*a set of power conduits*” to interface with power supplies from the system. For example, Perego’s memory module has a memory slot connector 390 which connects the memory module to the rest of the system through a corresponding memory slot connector 380, thus connector 390 includes power connectors that are configured to receive power through a corresponding “*set of power conduits*” in the memory slot 380 for the module’s operation. EX1035 (Perego), e.g., at FIG. 3B (below, annotated), 6:3-6 (“Each of mating connectors 380a–380n interface with connectors 390a–390c to allow removal/inclusion of memory subsystems 330a–330c in memory system 305.”).

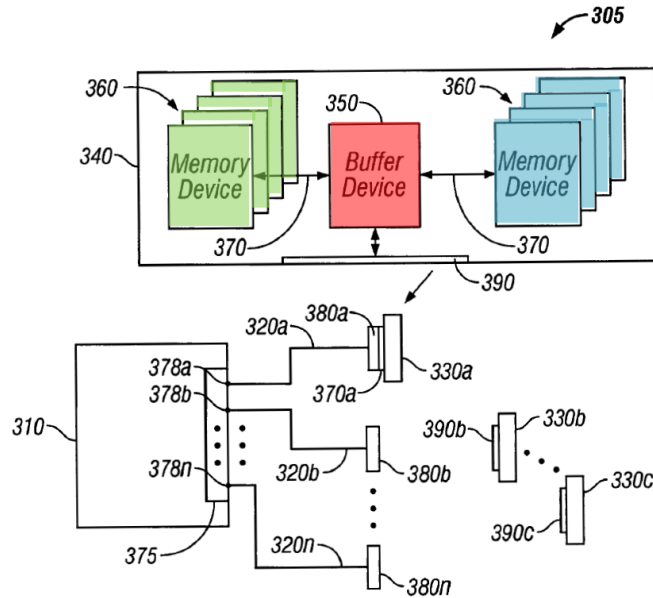


FIG. 3B

Indeed, it was well known at the time that DIMMs receive power through their edge connectors. See, e.g., EX1108 (Dell, cited by Perego (EX1023) at 2:4-6) at 1:65-2:20 (“A SIMM generally is easily inserted into a connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom. ... A DIMM essentially comprises a SIMM ...”), Fig.3 (DIMM having Power Supply and Ground pins); EX1051 (Doblar) at [0043-47] and Figs. 1-5 (DIMMs with edge connector pins and mating connector sockets including pins for power); EX1104 (JESD21-C) at 4.20.4-1 (“DDR SDRAM Registered DIMM Design Specification”) and 4.20.4-6 (“Pin Description [...] V_{DD} SDRAM positive power supply [] V_{DDQ} SDRAM I/O Driver positive power supply [] V_{REF} SDRAM I/O reference supply [] V_{DDSPD} Serial EEPROM positive power supply ”); EX1028 (JESD205) at p.1 (“DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification”) and p.11 (“DIMM Connector Pin Description [...] V_{CC} AMB Core Power and AMB Channel Interface Power (1.5 Volt) [...] V_{DD} DRAM Power and AMB DRAM I/O Power (1.8 Volt) [...] V_{TT} DRAM Address/Command/Clock Termination Power ($V_{DD}/2$) [...] V_{DDSPD} SPD Power ...”).

Harris further discloses that standard DIMMs have “a relatively large number of pins” coupled to “power supply rails ... powered from system board or main board voltage sources, and are specific to the memory technology.” EX1023 (Harris) at [0002]; see also *id.* at [0012] (“a standard FBD module requires 28 V_{dd} pins (for DRAM devices) and 8 V_{cc} pins (for buffer and logic) and associated Ground returns, resulting in a total of 72 pins that provide a power supply interface”) and

EX1108 (Dell) at Fig. 3 (168 Pin SDRAM DIMM having 17+2 Power Supply pins and 18 Ground pins). Harris's "technology-independent voltage distribution scheme" is "replacing these power supply interface pins [for receiving voltages specific to the memory technology on the module] with as few as six +12V pins." EX1023 (Harris) at [0002], [0012], [0019].

As discussed above (see motivations to combine, EX1003 at ¶¶153-170), a Skilled Artisan would have understood that 12V power rails were readily available on motherboards at the time to provide 12V power supply for a memory module under Harris's voltage distribution scheme. See, e.g., EX1023 (Harris) at [0014] ("It should be readily recognized that the external voltage sources may comprise any combination of known or heretofore unknown voltage supplies, either regulated or unregulated, and even including variable voltages."), [0020] ("Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated."). Harris also explains that, in its Fig. 3, "each memory board ... receives a supply voltage that ... may be sourced from the memory controller 302." *Id.* at Fig. 3 (below) and [0017] ("Although not explicitly shown in this FIGURE, each memory board also receives a supply voltage that is locally converted by an on-board VRM for powering the DRAM and buffer components therein. In one arrangement, the supply voltage may be sourced from the memory controller 302 or from a separate voltage source."). A Skilled Artisan would have understood from Harris's disclosure that the module receives its supply voltage through the expressly shown edge connectors which have power pins to interface with "*a set of power conduits*" in the memory slot 380. *Id.*

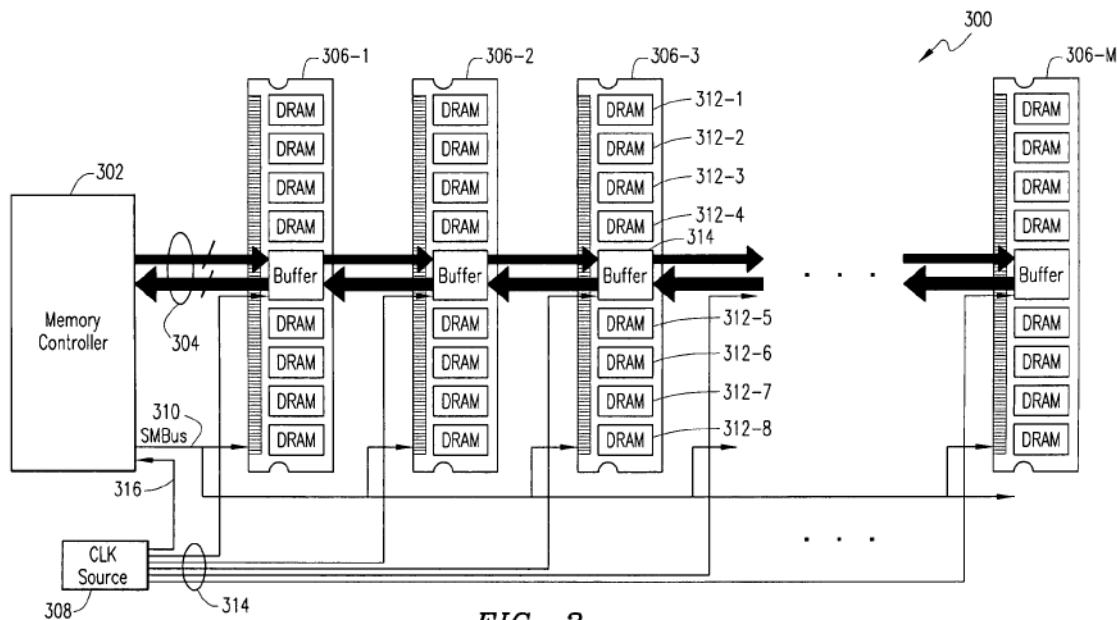


FIG. 3

Accordingly, it would have been obvious to a Skilled Artisan to implement Harris's "technology-independent voltage distribution scheme" in the memory system of Perego and to include power connectors in the module's edge connectors to receive power supply from "a set of power conduits" in the memory slot as taught by Harris and Perego, and as it was common at the time, and shown below in a schematic illustration of the Perego-Harris combination. EX1003 at ¶¶153-170

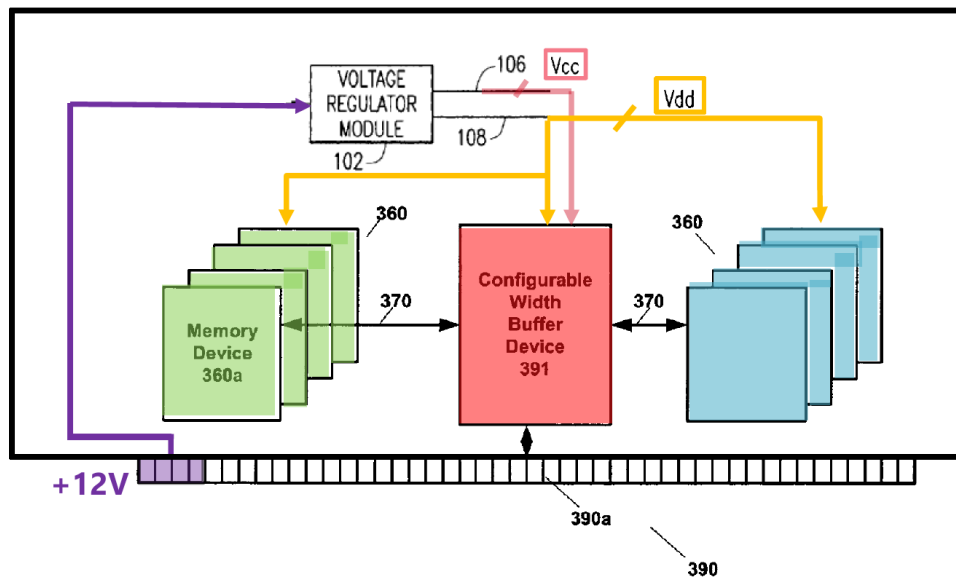


Fig. 3C

In prior IPRs, Netlist argued that Harris does not disclose that the module's edge connections are "configured to couple power ... between the memory module and the host system," but the Board already considered and rejected those arguments. EX1070 (IPR2022-00996, FWD) at 42-50; EX1071 (IPR2022-00999, FWD) at 37-39. For example, the Board found that Harris discloses that DRAM devices may be "powered from system board or main board voltage sources," and this was known to a Skilled Artisan. EX1070 at 49. The Board further found that Harris's teaching of "replacing ... power supply interface pins with as few as six +12V pins" means that those six pins take the place of the power pins in the prior art interface, "implying that power still comes from the interface with the host system." *Id.* (citing EX1023, [0012] and [0017]). The Board also found that Harris's teaching that "external voltage sources may comprise any combination of known or heretofore unknown voltage supplies" means that the voltage supply "may be the host system," which was known to provide 12V supply. *Id.* at 50 (citing EX1023, [0014]). The Board credited expert testimony explaining that Harris's statement that "system board power supply and associated voltage plane(s) are eliminated" means that "supplies such as the memory V_{DD} and memory V_{CC} that are specific to a particular generation of memory chips ... can be supplied on the DIMM rather than being supplied from the motherboard." *Id.* (citing EX1076 (Dr. Wolfe) at 116:25-117:6). The Board also relied on the undisputed fact and supporting evidence that commercially available DIMMs derive their power from the host. *Id.* (citing EX1076 (Dr. Wolfe) at 92:9-95:8

(“Lots of computer systems had 12-volt power rails”); EX1075 (Dr. Mangione-Smith) at 180:14-183:3 (“Q. ... this document indicates that the power supply on the [ATX] is 12 volts; correct? A. It indicates that ... there has to be a 12-volt output, that has to be provided by the power supply, yeh.”)).

The combination with Amidi has the same power edge connectors to receive Harris’s +12V power supply from “a set of power conduits” in the memory slot. EX1003 at ¶¶153-170.

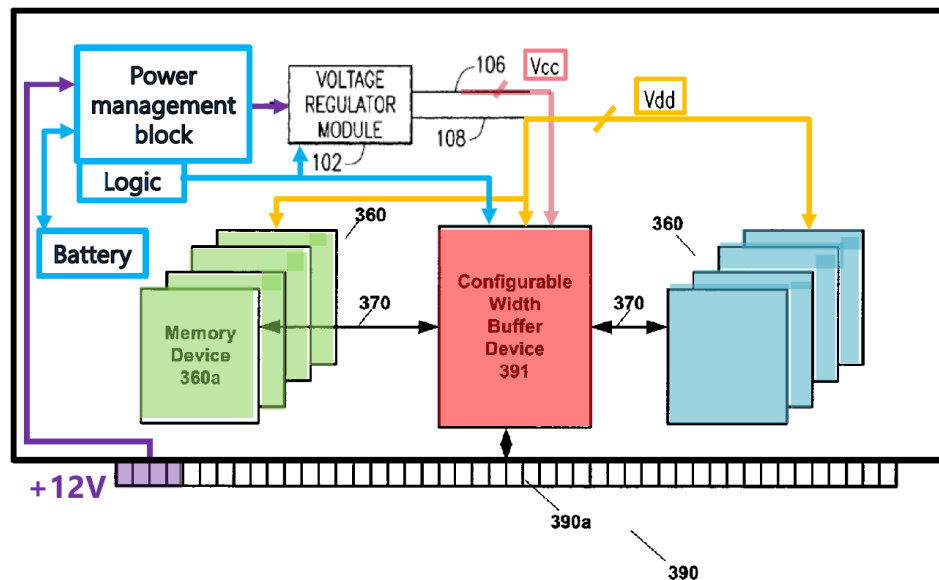


Fig. 3C

Accordingly, the proposed combination under Ground 2 discloses that the memory module includes edge connectors not only to communicate data and address/control signals as explained above, but also to receive a power supply from the system. Thus, in the combination, “mating connectors 380a-380n” further include “a set of power conduits” electrically coupled to the power supply edge connectors to deliver the system power to the module.

Thus, the Perego-Harris combination alone and in view of Amidi disclose that the module’s “memory slot connector includ[es] a set of power conduits” to interface with Harris’s +12V power supply.

[1.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and

Perego discloses that “data signals [DQ] are transferred between the system board and the DIMM via the set of data conduits” in the DIMM’s connector for the reasons discussed above with reference to claim element **[1.a.2]**. *Supra* at 4-11; see, e.g., EX1035 (Perego) at Fig. 4B (below, annotated).

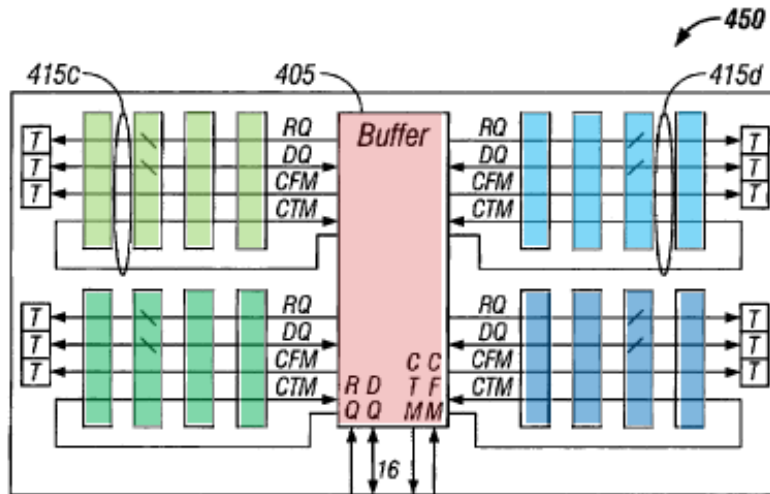


FIG. 4B

[1.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

Perego discloses that “address and control signals [RQ] are delivered from the system board to the DIMM via the set of address and control conduits” in the DIMM’s connector for the reasons discussed above with reference to claim element **[1.a.2]**. *Supra* at 4-11; see, e.g., EX1035 (Perego) at Fig. 4B (below, annotated).

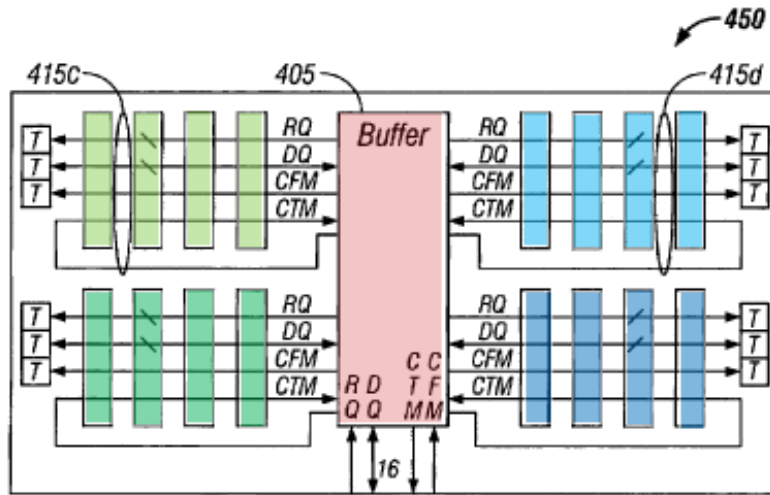
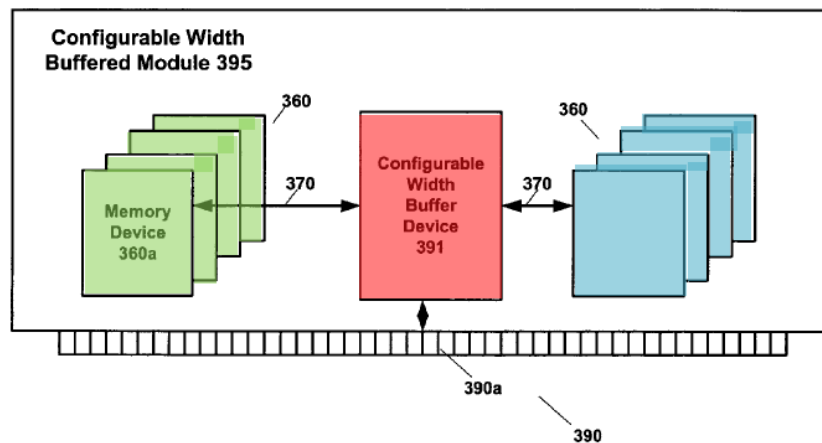
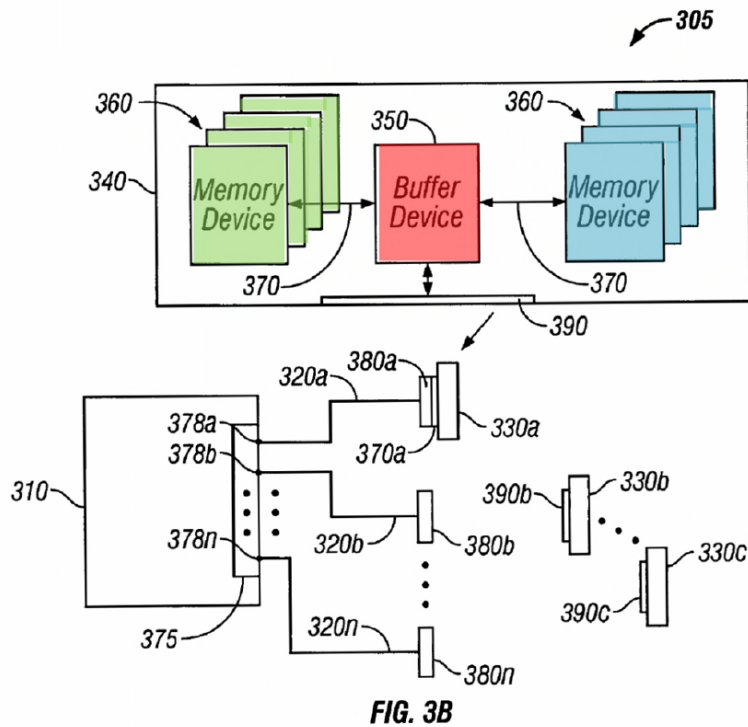


FIG. 4B

[1.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

Perego discloses that the DIMM includes “a printed circuit board (PCB) having edge connections [390] configured to fit into the memory slot connector [380] of the system board” for the reasons discussed above with reference to claim element **[1.a.1]**. *Supra* at 1-4; see, e.g., EX1035 (Perego) at 5:56-6:11 (“memory subsystems [330] are incorporated onto individual substrates (e.g., PCBs) ...that include connectors 390a-390c ... Each of mating connectors 380a-380n interface with connectors 390a-390c to allow removal/inclusion of memory subsystems 330a-330c in memory system 305. In one embodiment, mating connectors 380a-380n are sockets and connectors 390a-390c are edge connectors disposed on an edge of each memory subsystems 330a-330c. Mating connectors 380a-380n, are attached to a common substrate shared with point-to-point links 320a-320n and controller 310.”), Figs. 3B and 3C (below, annotated).



For the reasons discussed above with reference to **claim element [1.a.1]**, Harris and Amidi also disclose that their DIMM includes “*a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board.*” *Supra* pp.1-4; EX1023 (Harris) at [0013] (“It is contemplated that local supply voltage conversion for double-rank DIMMs can be accommodated with a form factor design of approximately about one square inch (both sides of the printed circuit board), and at a component height compatible

with applicable Joint Electron Device Engineering Council (JEDEC) standards.”); EX1024 (Amidi) at 3:49-53 (“In one embodiment, memory module 300 includes a memory card (e.g. a printed circuit board), memory chips, series termination resistors, PLL (Phase-Lock-Loop) and SPD (Serial Presence Detect) components, and a card interface. ”).

Thus, the Perego-Harris combination alone and in view of Amidi disclose that the DIMM includes “a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board.”

[1.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,

The combination of Perego and Harris alone and in view of Amidi disclose “a first set of edge connections [purple in edge connector 390] configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from [12V] power rails of the system board via the set of power conduits” for the reasons discussed above with reference to claim element **[1.a.2]**. *Supra* at 4-11; see, e.g., annotated Fig. 3C of Perego (below). EX1003 at ¶¶153-170.

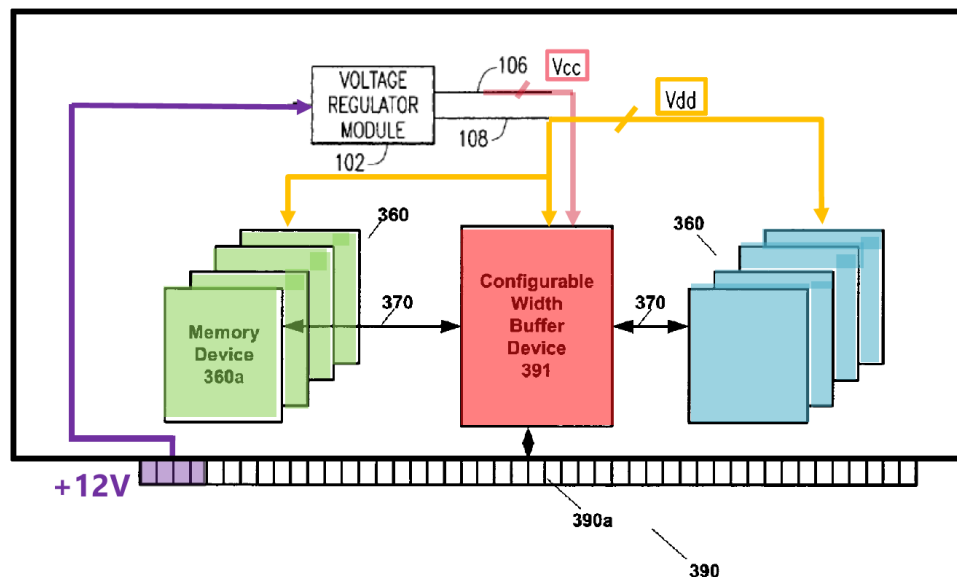


Fig. 3C

For example, Harris teaches to use only a “few” pins to provide a technology-independent (e.g. 12V) power to the memory module from power supply rails of the system board through the edge connector and locally convert the received power on board to voltage levels as required by the specific memory and buffer technology on the module. See, e.g., EX1023 (Harris) at [0012] (“A voltage-independent ... design incorporating the embodiment of FIG. 1A is capable of replacing these [V_{dd} and V_{cc}] power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added.”), [0020] (“Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.”).

The combination with Amidi uses the same “*first set of edge connections*” as illustrated in annotated Fig. 3C of Perego (below). EX1003 at ¶¶153-170.

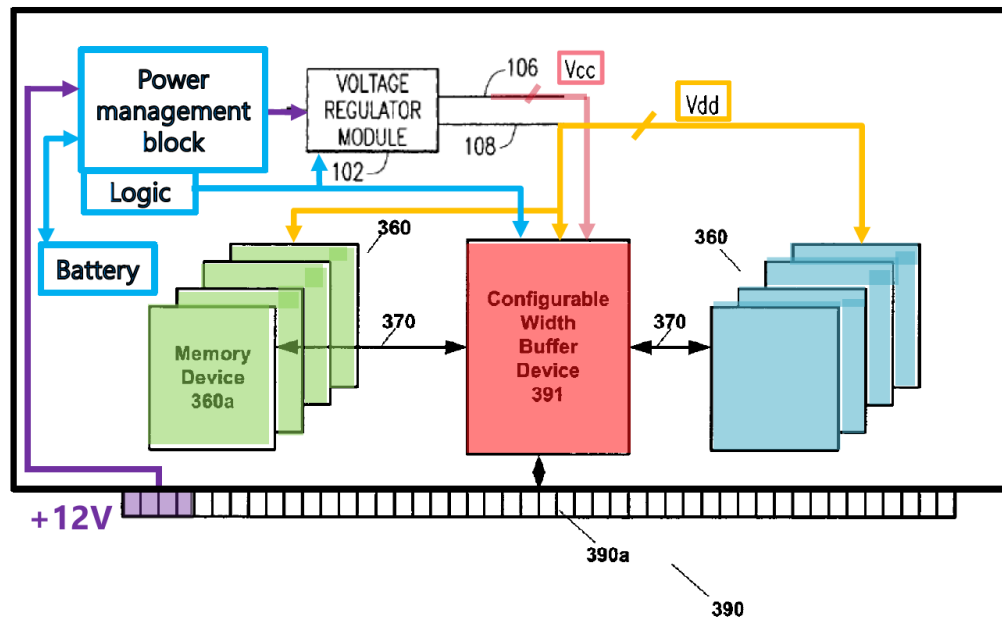


Fig. 3C

[1.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

The combination of Perego, Harris, and Amidi discloses that “*the power delivered to the DIMM from the [12V] power rails of the system board is the only power received by the DIMM*” for the reasons discussed above for claim elements [1.a.2] and [1.b.2]. *Supra* at 4-11, 15-16; EX1003 at ¶¶153-170.

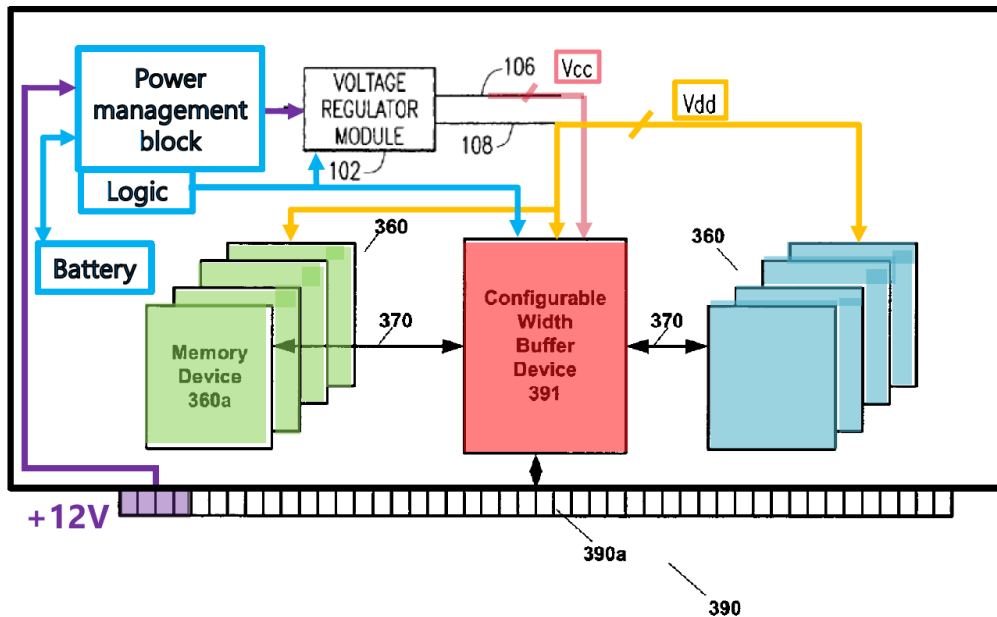


Fig. 3C

As shown in the annotated Fig. 3C of Perego, the combination discloses that “the power delivered to the DIMM from the [12V] power rails of the system board is the only power received by the DIMM.” EX1003 at ¶¶153-170. For example, it was common practice at the time to have “the power delivered to the DIMM from the power rails of the system board.” *Id.* Harris, for example, discloses that “Dual In-line Memory Modules (DIMMS) populated with dynamic random access memory (DRAM) devices, are provided with power supply rails ... that are powered from system board or main board voltage sources” and specifically teaches that its “embodiments are amenable to dual +12V power supply rail implementations.” EX1023 (Harris) at [0002] and [0020]. Harris does not disclose any power source for delivering power to the DIMM other than the power supply rails of the system board.

Furthermore, “deriving all necessary power” from the DIMM’s connector was common practice at the time. EX1108 (Dell, cited by Perego (EX1035) at 2:4-6) at 1:65-2:20 (“A SIMM generally is easily inserted into a connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom. ... A DIMM essentially comprises a SIMM ...”). Thus, the combination of Perego and Harris discloses to a Skilled Artisan that “the power delivered to the DIMM from the [12V] power rails of the system board is the only power received by the DIMM.”

Amidi also teaches delivering power to the DIMM from the power rails of the system board only. For example, Amidi teaches that its module includes an on-board battery charger (620) that uses the same system supply (605) to charge the battery (630) as what provides power to the rest of the module. EX1024 (Amidi) at Fig. 6 (below), 4:23-43 (“System supply 605 provides a system power supply to a boost power converter 610 ... Boost converter 610 provides a power output 615 which powers battery charger 620—which in turn supplies battery 630.”).

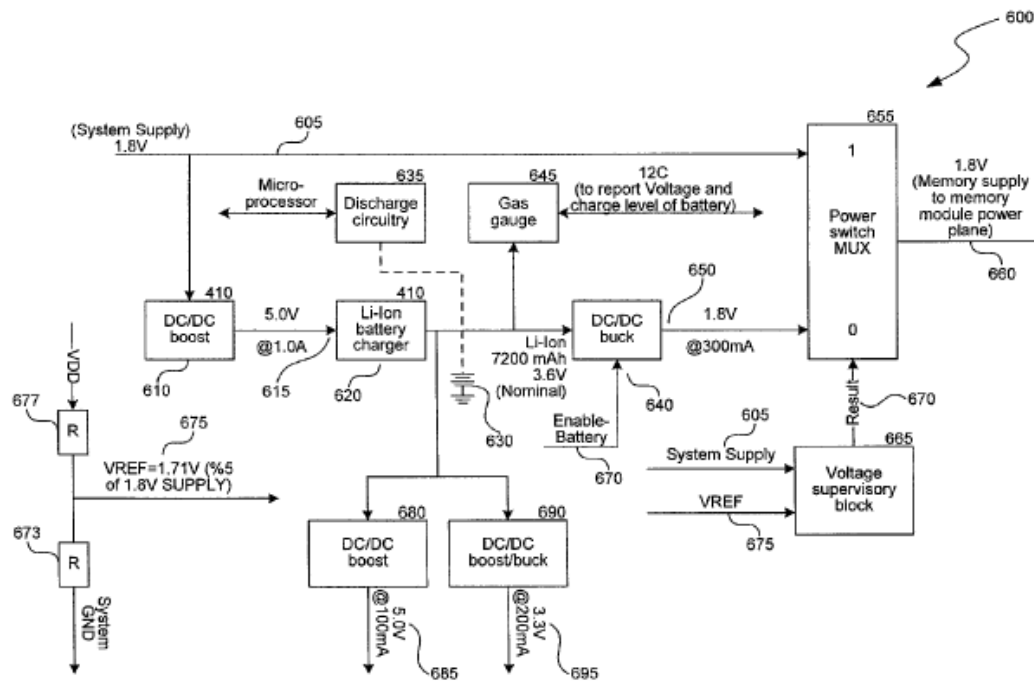


FIG. 6

As illustrated in Fig. 4 of Amidi, the battery charger (485) and the battery (475) are part of Amidi’s memory module. EX1024 (Amidi) at Fig. 4, 3:64-4:13.

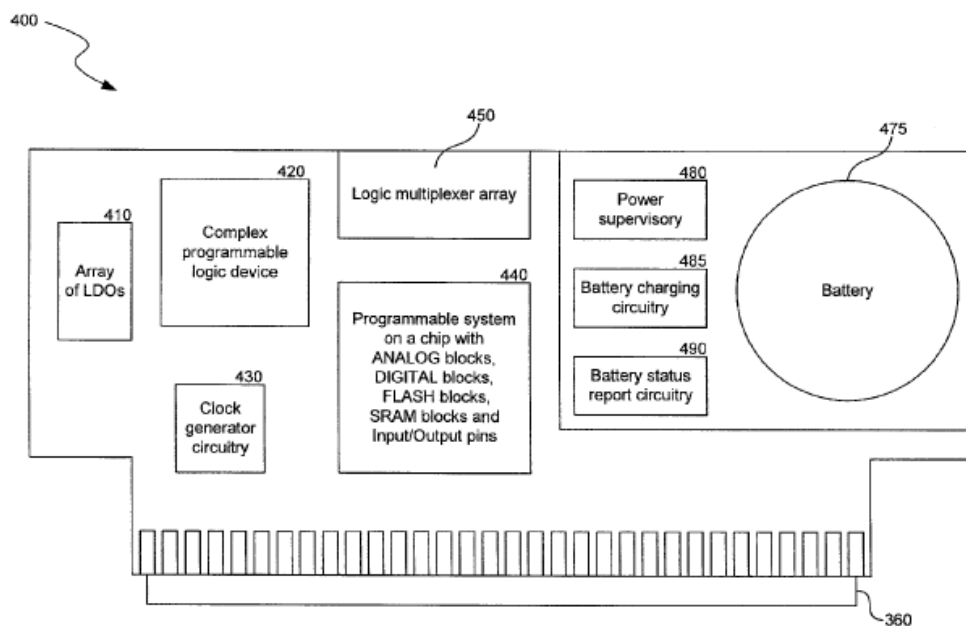


FIG. 4

Thus, Amidi also teaches “deriving all necessary power,” including the power required to charge the battery, from the memory PCB connector, as was common practice at the time. EX1108 (Dell, cited by Perego (EX1035) at 2:4-6) at 1:65-2:20 (“A SIMM generally is easily inserted into a connector within the computer system, the SIMM thereby deriving all necessary power, ground, and logic signals therefrom...”).

Amidi’s chargeable battery operates substantially the same way as the secondary power source of the ’366 Patent, including the use of power from the system board to charge the secondary power source. EX1001, 20:63-67 (“For example, when no power failure is detected, the power module may provide power to certain components, such as the volatile memory, from system power while charging a secondary power source (e.g., a capacitor array).”). The ’366 specification suggests that capacitors may be better than batteries for the second (backup) power supply, but these concerns are limited to batteries that “need to be replaced” and, in any event, do not support excluding batteries in general. EX1001, 26:19-35. Rather, the ’366 Patent discusses some known advantages of using capacitors (which are like rechargeable batteries) over non-rechargeable batteries. EX1003, ¶184. Indeed, the ’366 patent expressly teaches that, “in certain embodiments, the second power supply ... may comprise a battery.” EX1001, 26:35-39. Using either a capacitor or a battery as a secondary power source on a memory module were well-known, and obvious, alternatives at the

time. EX1025 (Spiers), [0009] (“The secondary power source may comprise a capacitor, a battery, or any other suitable power source.”).

Accordingly, a Skilled Artisan would have understood that power was readily available to the DIMM from the power rails of the system board and thus been motivated to implement the combination of Perego, Harris, and Amidi such that “the power delivered to the DIMM from the [12V] power rails of the system board is the only power received by the DIMM.” EX1003 at ¶¶153-170.

[1.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits, and

The combination of Perego, Harris, and Amidi discloses “a second set of edge connections [in connector 390] configured to be electrically connected to the set of data conduits” for interfacing DQ signals to and from the memory controller for the reasons discussed above with reference to claim element [1.a.2]. *Supra* at 4-11; EX1035 (Perego) at Figs. 3C and 4B (below, annotated).

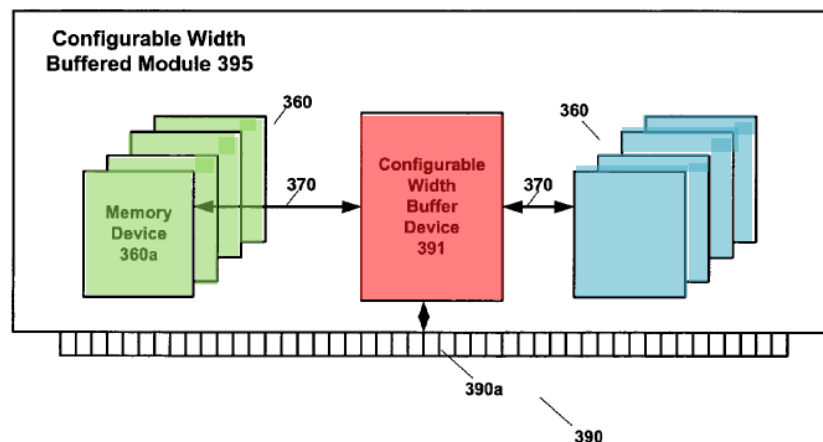


Fig. 3C

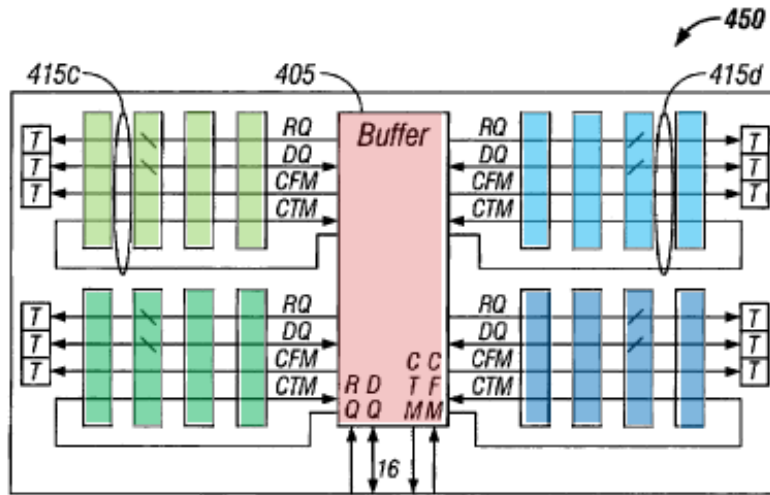


FIG. 4B

[1.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,

The combination of Perego, Harris, and Amidi discloses “a third set of edge connections [in connector 390] configured to be electrically connected to the set of address and control conduits” for interfacing address and control (RQ) signals from the memory controller for the reasons discussed above with reference to claim elements **[1.a.2]**. *Supra* at 4-11; EX1035 (Perego) at Figs. 3C and 4B (below, annotated).

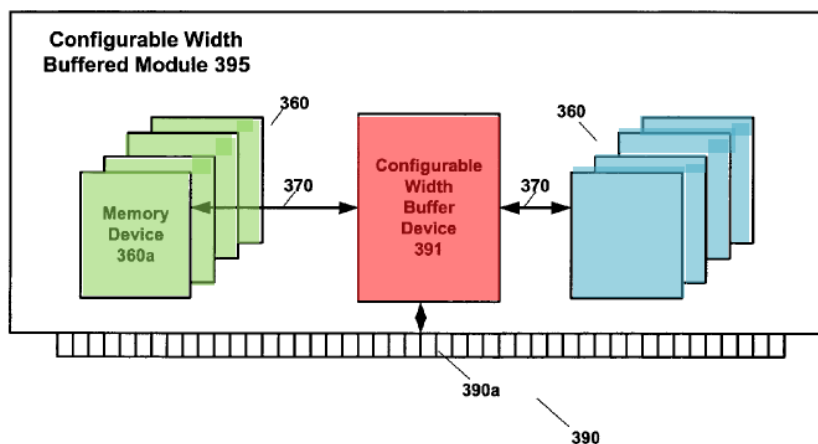


Fig. 3C

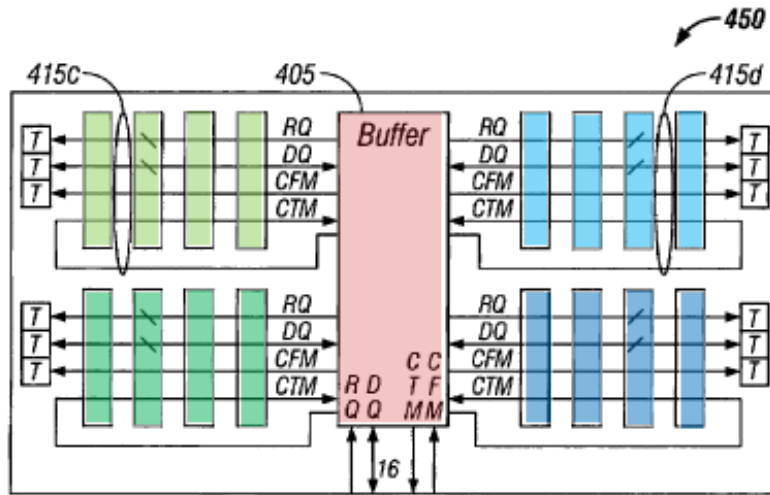


FIG. 4B

[1.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

The combination of Perego, Harris, and Amidi discloses “a set of voltage supply lines electrically connected to the first set of edge connections [e.g., ‘as few as six +12V pins’] and configured to receive the power delivered to the DIMM from the [+12V] power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM” for the reasons discussed above with reference to claim elements [1.a.2], [1.b.2], and [1.b.3]. *Supra* at 4-11, 15-16, 16-20.

It would have been obvious to a Skilled Artisan to implement Harris’s power distribution functionality in a system using Perego’s memory modules. EX1003, ¶¶153-170. For example, Harris discloses that “the embodiment of FIG. 1A is capable of replacing these [standard] power supply interface pins with as few as six +12V pins (from an external voltage source), with local conversion to V_{dd} (to DRAM) and V_{cc} (to buffer/logic) being added.” EX1023 at [0012]. “Alternatively, using additional power supply pins would provide the capability to support even more devices. For instance, with 12 supply pins (at +12V), the embodiment of FIG. 1A can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.” *Id.*, see also *id.* at [0020] (“Further, the embodiments are amenable to dual

+12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.”).

A Skilled Artisan would have understood that, in the combination with Amidi, there are “a set of voltage supply lines [purple] electrically connected to the first set of edge connections [of ‘+12V pins’]” and to Amidi’s Power management block. See, e.g., annotated Fig. 3C of Perego (below); EX1003 at ¶¶153-170. Those “voltage supply lines” are “configured to receive the power delivered to the DIMM from the [+12V] power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM.” *Id.*

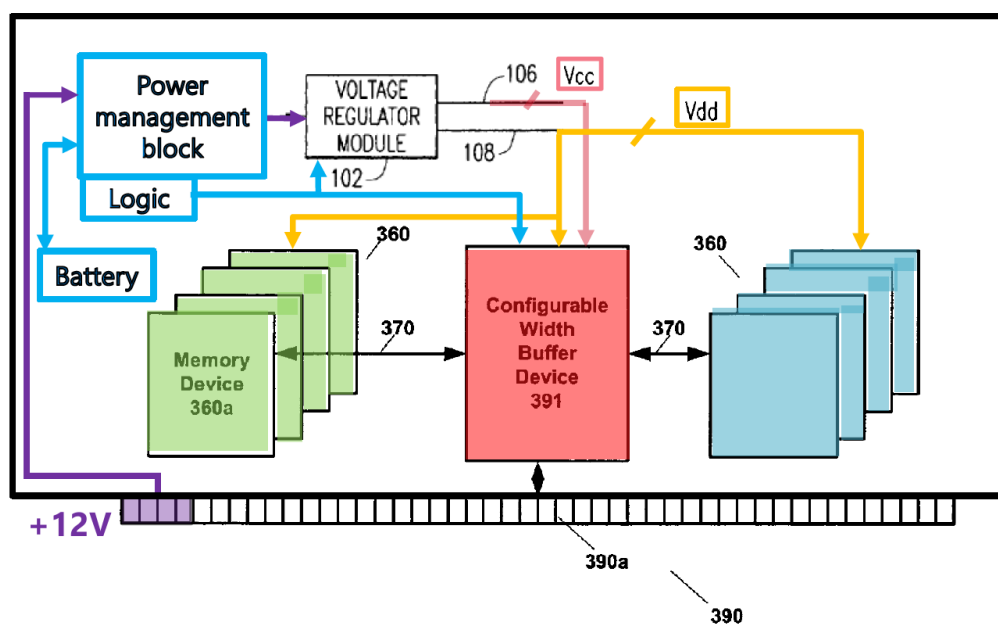


Fig. 3C

[1.b.7] a set of data lines electrically connected to the second set of edge connections, and

The combination of Perego, Harris, and Amidi discloses “a set of data lines [DQ] electrically connected to the second set of edge connections [in connector 390]” and to Perego’s buffer device (red) for the reasons discussed above with reference to claim elements [1.a.2], [1.a.3] and [1.b.4]. See, e.g., *supra* at 4-11, 12-12, 20-21, and EX1035 (Perego) at Figs. 3C and 4B (below, annotated).

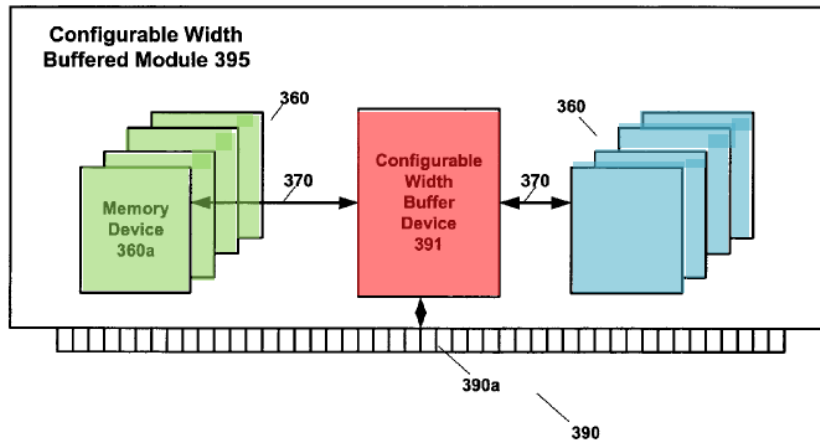


Fig. 3C

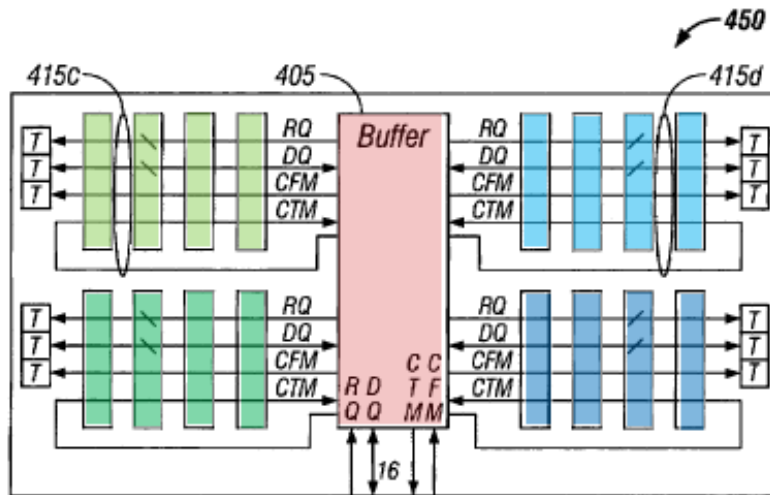


FIG. 4B

[1.b.8] a set of address and control lines electrically connected to the third set of edge connections;

The combination of Perego, Harris, and Amidi discloses “a set of address and control lines [RQ] electrically connected to the third set of edge connections [in connector 390]” and to Perego’s buffer device (red) for the reasons discussed above with reference to claim elements [1.a.2], [1.a.4] and [1.b.5]. See, e.g., *supra* at 4-11, 12-13, 21-22, and EX1035 (Perego) at Figs. 3C and 4B (below, annotated).

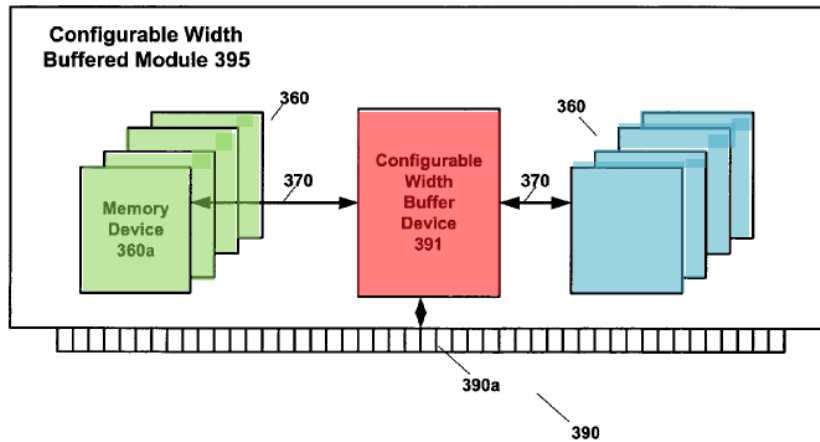


Fig. 3C

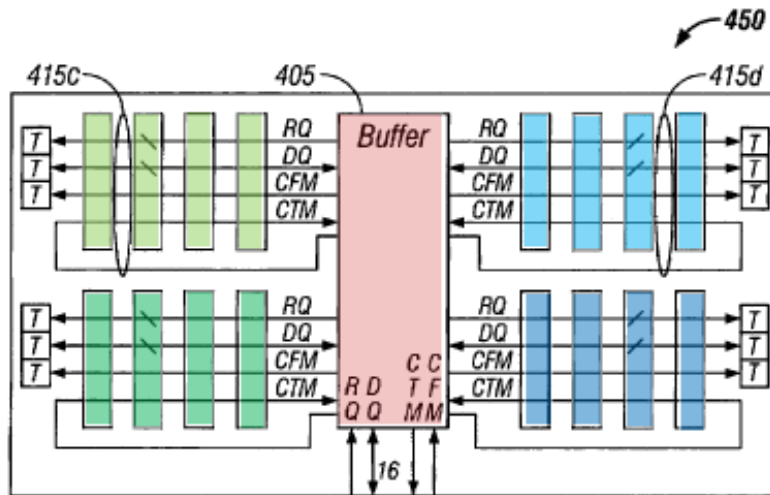


FIG. 4B

[1.c.1] a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

The combination of Perego, Harris, and Amidi discloses “a controller [including control circuitry in Perego’s buffer device and circuitry implementing control functionality of Amidi’s logic and Power management block] including a voltage monitor circuit [in Amidi’s Power management block] and nonvolatile

memory [e.g., in operations circuit 572 in Perego's buffer device or in an SPD device], the controller coupled to the PCB and to an input [+12V] voltage supply line of the set of voltage supply lines.” See, e.g., annotated Fig. 3C of Perego (below); EX1003 at ¶¶153-170.

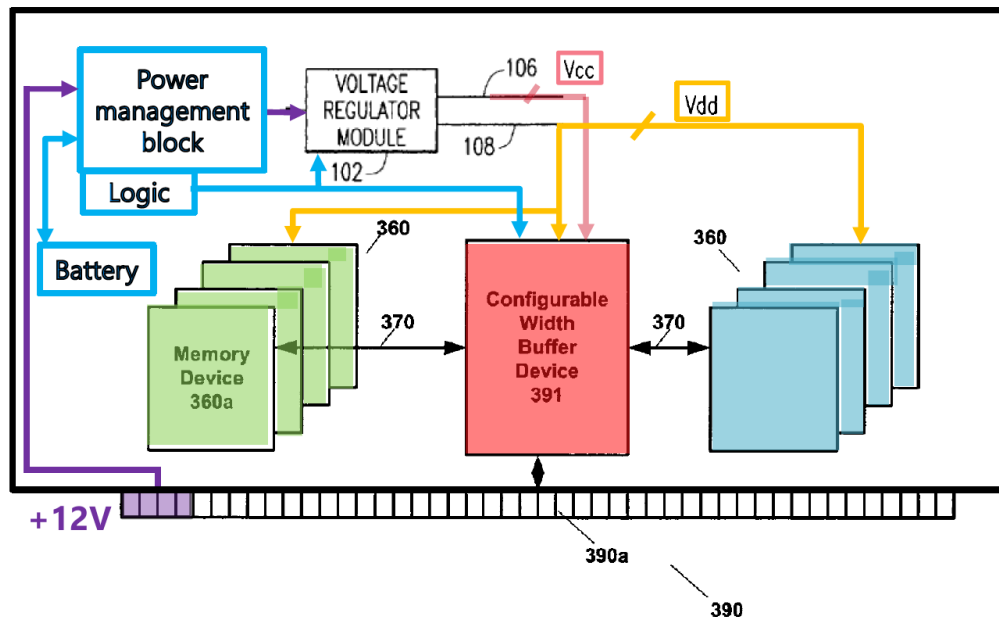
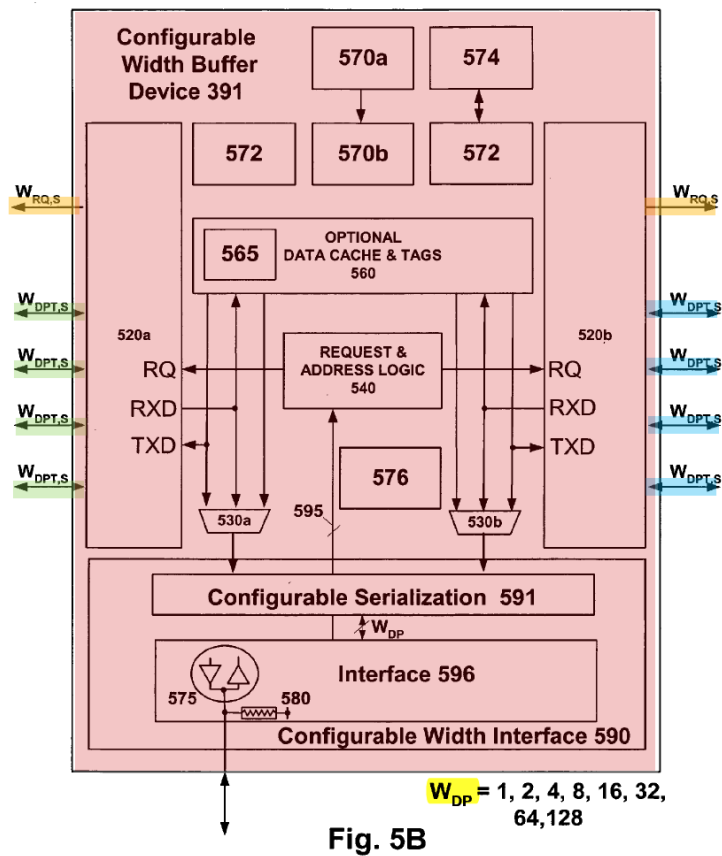


Fig. 3C

Perego discloses circuitry of a “controller” in buffer device (red, e.g., 391) which is “coupled to the PCB.” See, e.g., annotated Fig. 3C of Perego (above); EX1003 at ¶¶153-170. Perego also discloses the “controller including ... nonvolatile memory,” e.g., in operations circuit 572 or in “an SPD device for example, an EEPROM device.” See, e.g., EX1035 (Perego), Fig. 5B (below, annotated).

Perego explains that “[o]perations circuit 572 includes storage circuit to store information used by the system in which the configurable width buffer device 391 is situated in, for example, to perform configuration operations. ... The functionality of operations circuit 572 may be included on an SPD device for example, an EEPROM device, that is readable by the system, such as a controller, to determine the capabilities of a configurable width buffer device 391 and/or configurable width buffered module 395.” *Id.* 15:46-16:12.



Amidi, in combination with Perego and Harris, also discloses “a controller including a voltage monitor circuit [Amidi’s Voltage supervisor (665, red) in its Power management block].” EX1024 (Amidi) at Fig. 6 (below, annotated).

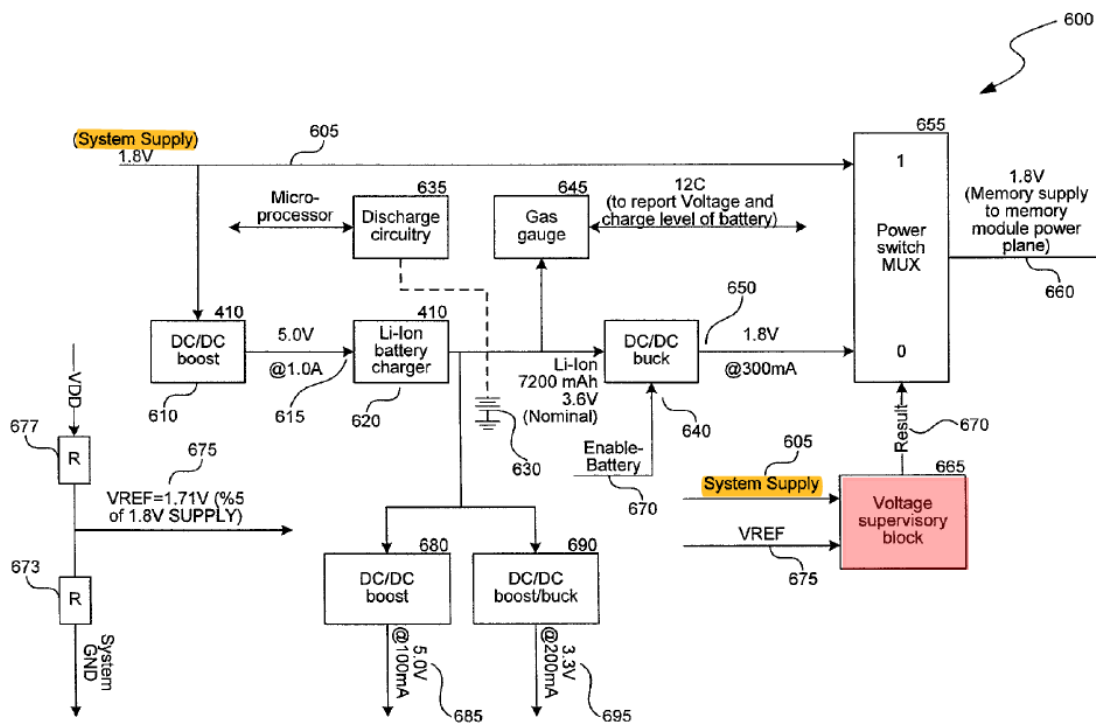


FIG. 6

Amidi explains that its “voltage supervisory block 665 [(including a “voltage monitor circuit”)]... receives system supply 605” which is “an input voltage supply line of the set of voltage supply lines” and which has a +12V input voltage in the combination with Harris. EX1003 at ¶¶153-170. As discussed above, a Skilled Artisan would have understood how, and been motivated, to implement the functionality of Amidi’s Power management block, including its voltage supervisor for a +12V input voltage, according to the Harris power management technique. EX1003, ¶¶153-170. For example, Amidi discloses that “voltage supervisory block 665... receives system supply 605 and a reference voltage 675, and compares the two,” and a Skilled Artisan understood how to compare voltages. EX1024 (Amidi), 4:44-46, Fig. 8. Thus, the proposed combination discloses “a voltage monitor circuit ... coupled ... to an input [+12V] voltage supply line of the set of voltage supply lines.”

Amidi also discloses that its “voltage monitor circuit [(in power supervisory block, red) is] ... coupled to the PCB.” See, e.g., EX1024 (Amidi), Fig. 4 (below, annotated). Amidi’s other control circuitry is also “coupled to the PCB.” *Id.*

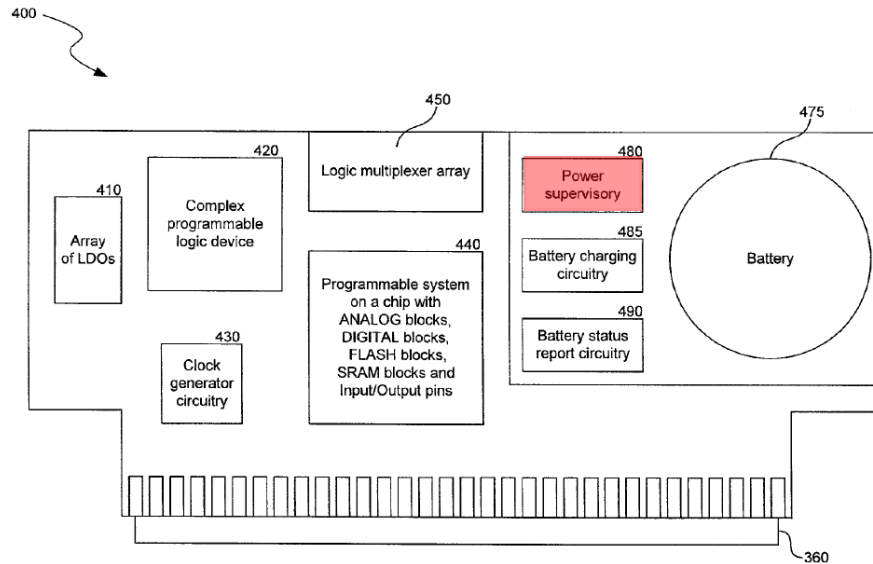


FIG. 4

Furthermore, the Board already found that “Harris discloses that its +12V power supply has a tolerance of ‘+/-15%’ which indicates it would be a concern if the power supply was greater than 15% ...[and] Amidi indicates concern with ‘power fault[s].’” EX1070 (918 FWD), 79; EX1071 (054 FWD), 65. The Board also agreed that “a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal in response to the detection.” EX1070, 79. The Board also found that “[t]here is no dispute on this record that [Harris’s] SPD is non-volatile memory.” *Id.* 68.

Accordingly, the combination of Perego, Harris, and Amidi discloses “a controller including a voltage monitor circuit [in Amidi’s Power management block] and nonvolatile memory [in Perego’s buffer device], the controller coupled to the PCB and to an input [+12V] voltage supply line of the set of voltage supply lines.”

[1.c.2] (i) monitor an input voltage supplied via the input voltage supply line;

The combination of Perego, Harris, and Amidi discloses that “the voltage monitor circuit [in Amidi’s Power management block is] configured to: (i) monitor an input [+12V] voltage supplied via the input voltage supply line [as taught by Harris]” as discussed above with reference to **claim element [1.c.1]**. *Supra* at 25-29. Indeed, Harris teaches to use a +12V input voltage, and Amidi expressly teaches to “monitor an input voltage supplied via the input voltage supply line.”

See, e.g., EX1023 (Harris) [0012] (“For instance, with 12 supply pins (at +12V), the embodiment of FIG. 1A can provide enough power to supply 4 ranks (i.e., 72 devices). Likewise, a memory assembly of 8 ranks (144 devices) may be powered with 24 pins at +12V.”); EX1024 (Amidi), 4:44-46 (“Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two.”), Fig. 6 (below).

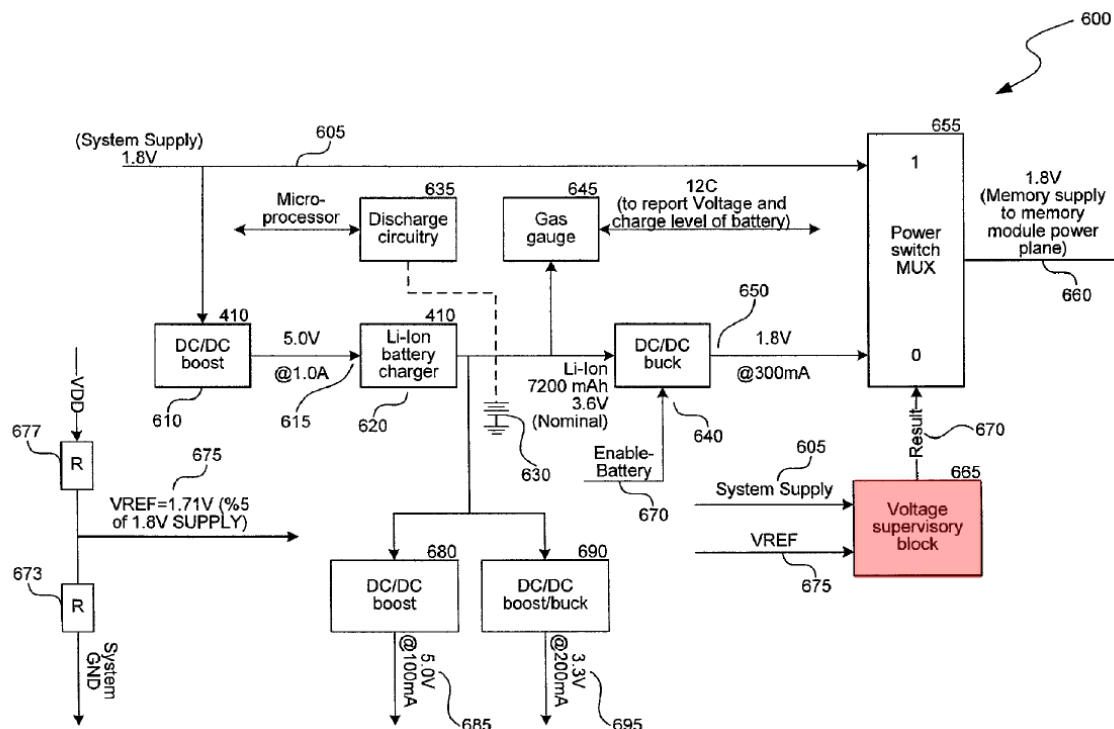


FIG. 6

Furthermore, the Board already found that “Harris discloses that its +12V power supply has a tolerance of ‘+/-15%’ which indicates it would be a concern if the power supply was greater than 15% ...[and] Amidi indicates concern with ‘power fault[s]’ ... [thus] a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal in response to the detection.” EX1070 (918 FWD), 79; EX1071 (054 FWD), 65 (similar).

[1.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and

The combination of Perego, Harris, and Amidi discloses that “the voltage monitor circuit [in Amidi’s Power management block is] configured to: ... (ii)

generate a trigger signal [similar to signal 670 in *Amidi* which indicates the need to switch to backup power] upon detecting a trigger condition [such as an input voltage outside of the tolerance of +/-15% around +12V]” as discussed above with reference to **claim elements [1.c.1] and [1.c.2]**. *Supra* at 25-29, 29-30. See, e.g., EX1024 (*Amidi*), 4:44-46 (“Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660. If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 for memory supply 660.”).

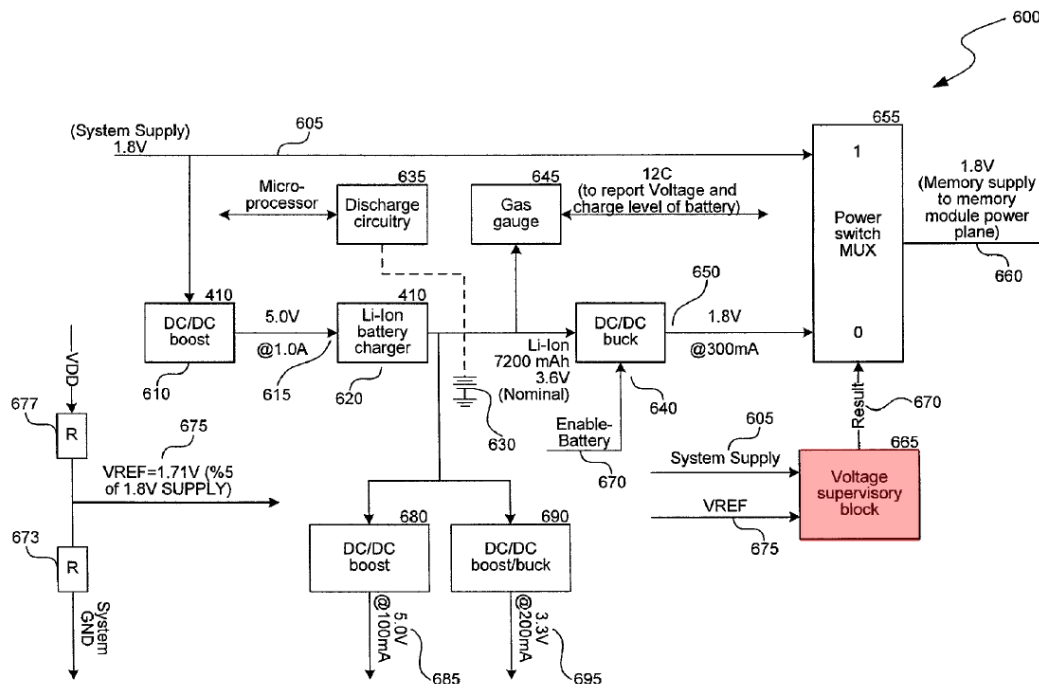


FIG. 6

The Board agreed. EX1070 (918 FWD), 79 (“Harris discloses that its +12V power supply has a tolerance of ‘+/-15%’ which indicates it would be a concern if the power supply was greater than 15% ...[and] *Amidi* indicates concern with ‘power fault[s]’ ... [thus] a person of ordinary skill in the art considering these teachings would have considered it obvious to detect overvoltage and generate a trigger signal in response to the detection.”); EX1071 (054 FWD), 65 (similar).

[1.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,

The combination of Perego, Harris, and Amidi discloses that “*the voltage monitor circuit [in Amidi’s Power management block is] configured to: ... (iii) transmit the trigger signal [e.g., “signal 670” in Amidi which indicates the need to switch to backup power] to at least one other portion of the controller [e.g., to “power switch multiplexer 655” to “cause [it] to choose battery power 650”],*” EX1024, 4:44-55, as discussed above with reference to **claim elements [1.c.1], [1.c.2], and [1.c.3]**. *Supra* at 25-29, 29-30, 30-31.

[1.c.5] wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and

The combination of Perego, Harris, and Amidi discloses that “*the controller is configured to perform, in response to the trigger signal [indicating a power fault], a write operation to write data [such as configuration and/or state information which can be used for restoring normal operation, e.g., from Perego’s state storage 576, or information related to the power fault which can be used for failure analysis as taught by Amidi] into the nonvolatile memory [such as Perego’s operations circuit 572 or SPD].*”

In particular, Amidi teaches that “one may expect that SDRAM will be properly refreshed when system power is present and a system operates normally, but if SDRAM is to retain memory in a power fail situation, refresh operations must be implemented without benefit of other parts of a system, requiring that the memory module trigger SDRAM refresh operations itself.” EX1024 (Amidi), 6:40-52. Thus, as part of its power fault detection and switching to backup power, Amidi “provide[s] a process which operates to detect voltage ... signals, initiate backup operations, maintain memory (through refresh, for example), and detect a recovery status.” EX1024 (Amidi), 2:11-26. For maintaining memory, Amidi teaches putting the memories into a “self refresh state.” *Id.*, 6:53-7:8, Fig. 11 (finite state machine including commands to self-refresh memory), Fig. 14 (below, showing memory in self-refresh state 1450 after power fault detection 1440).

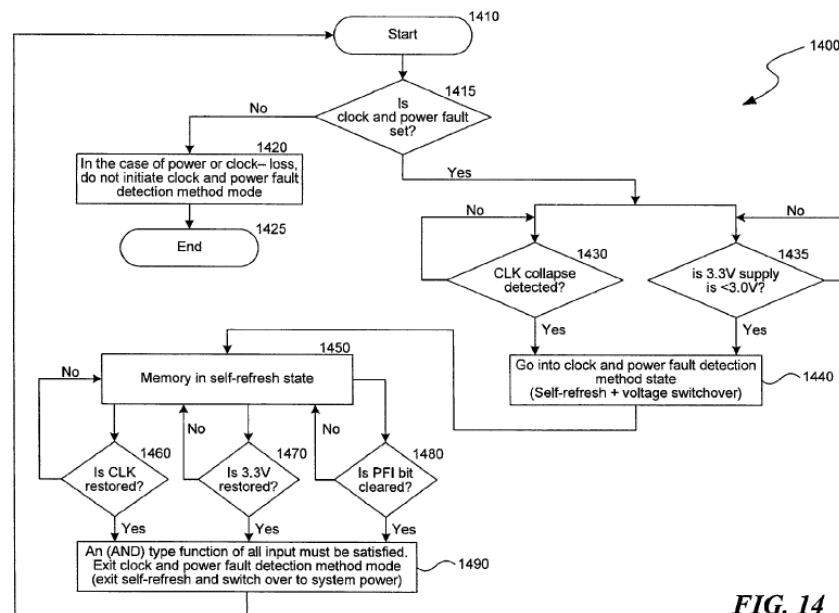


FIG. 14

Putting memory into a self-refresh state while using lower power as taught by Amidi was also known from a so-called “S3 sleeping state.” EX1109 (ACPI), p.229 (“The S3 state is defined as a low wake-latency sleep state ... [in which] some devices may be in a lower power state...”). For example, an S3 sleeping state transition can include “[p]lacing the memory into a low-power auto-refresh or self-refresh state” and “[d]evices that are maintaining memory isolating themselves from other devices in the system” such that “only devices supporting memory are powered (possibly partially powered).” *Id.* The S3 sleeping state was also used in “a standard FBD module,” i.e., a standard fully buffered DIMM, which Harris expressly references. EX1023 (Harris), [0012]. For example, one of the FBD standards explains that “S3 is an ACPI mode in which the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode.” EX1027 (JESD82-20), p.39.

Amidi also discloses that its memory module returns to normal operation after the power is restored and the system is ready for controlling the normal operation. EX1024 (Amidi), Fig. 15 (below), 8:62-9:2 (“Process 1500 includes initiating monitoring, detecting a fault, initiating a backup system, maintaining memory, detecting potential restoration, checking whether a system is ready, and restoring control to the system.”). Amidi explains that “some data may be useful for restarting a system after a failure.” *Id.* 1:23-25. For example, in order to wake up from the S3 sleeping state properly, “the BIOS needs to store the pre-sleeping state or initial boot state configuration in a non-volatile memory area ... to enable it to restore the values during the waking process.” EX1109 (ACPI), p.229.

Similarly, Amidi's teaching of "restoring control to the system" would also require "to store the pre-sleeping state ... in a non-volatile memory area ... to enable it to restore the values during the waking process." *Id.*

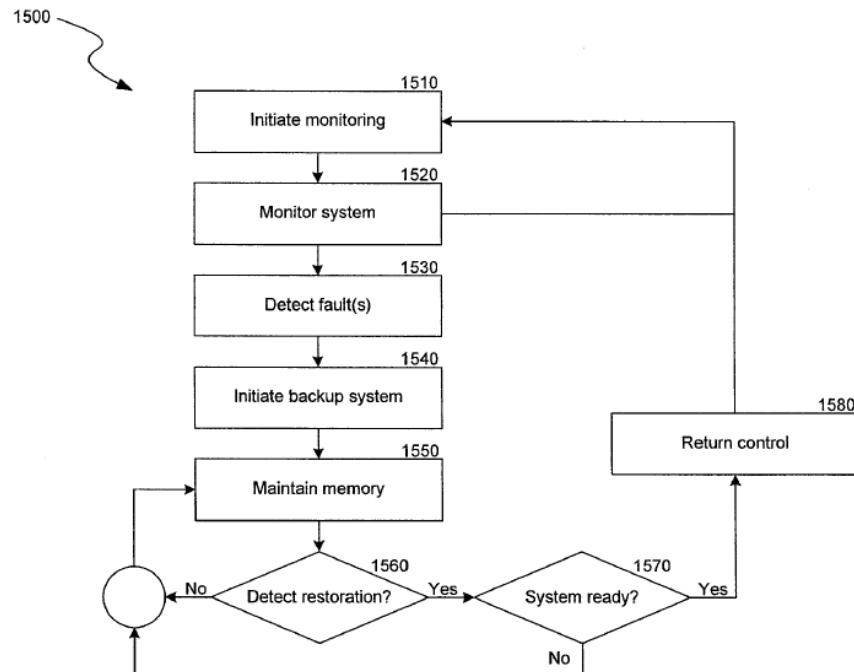


FIG. 15

The standard FBD referenced by Harris also requires that S3 recovery configuration registers "should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin." EX1027 (JESD82-20), p.25. For example, "S3RESTORE ... registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs ... [such as] calibration information for DDR IO drivers. BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up." *Id.* p.141. Perego also discloses parameters needed to restore system control, including Perego's state storage 576 which "may store ... the desired width of configurable width interface 590, and ... the desired width of one or more of interfaces 520a and 520b" which can be used "to establish the desired configuration" of these interfaces. EX1035 (Perego), 16:13-21.

Thus, restoring system control after a power failure as taught by Amidi includes or at least renders obvious using the known techniques for restoring memory operations after an S3 sleeping state, including writing configuration/state information before the sleeping state into non-volatile memory, such as operations

circuit 572 or an SPD device of Perego, and using the stored configuration/state information for restoring normal operation. *See, e.g.*, EX1024 (Amidi) 1:23-25 (“some data may be useful for restarting a system after a failure”). The Board also agreed that a Skilled Artisan would use the S3 sleep mode to conserve power during Amidi’s battery backup mode and that the S3 sleep mode requires writing S3 configuration information into the non-volatile memory in the SPD before going to sleep. EX1070 (918 FWD), pp.80-81 (considering the limitations of “in response to the trigger signal, the logic element writes information into the non-volatile memory,” the Board agreed that “the features of these claims are taught or at least suggested by the combination of Harris, the FBDIMM Standards, and Amidi”); EX1071 (054 FWD), pp.61-63 (similar).

In addition, Amidi further discloses that “failure analysis can be much simpler if information about the state of a system is available after a failure occurs.” EX1024 (Amidi) 1:21-22. The “information about the state of a system is available after a failure occurs” if such failure information (along with the configuration information for recovery) is written into the non-volatile memory, such as Perego’s operations circuit 572 or an SPD device in the proposed combination. EX1003 at ¶¶153-170. Indeed, storing failure-related information into nonvolatile memory was a well-known technique at the time. *See, e.g.*, EX1025 (Spiers) [0038] (“An EEPROM 210 is connected to the FPGA processor 198, and is utilized to store various status indicators and counters, which may be utilized during operations.”), [0042] (“the backup device includes an EEPROM that contains various status indicators as well as other statistics”).

[1.c.6] wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

The combination of Perego, Harris, and Amidi discloses that “*the trigger condition* [e.g., overvoltage] *occurs when the input voltage exceeds a first threshold voltage* [e.g., above the tolerance of +/-15% around +12V (therefore 15% above +12V)]” as discussed above with reference to **claim elements [1.c.1-1.c.5]**. *Supra* at 25-35, *see, e.g.*, EX1023 (Harris), [0013] (“since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/-15%) can be accommodated”). The Board already found that “Amidi provides the teaching of generating the trigger signal **onboard the memory module** in response to detecting a ‘power fault’ or ‘disruption’.” EX1070 (918 FWD), p.83 (emphasis by the Board). The Board also found that “Harris discloses that its +12V power supply has a tolerance of ‘+/-15%’ which indicates it would be a concern if the power

supply was greater than 15% ...[and Amidi's] 'power fault' is broad enough to encompass overvoltage as well." *Id.*, p.79; EX1071 (054 FWD), 65 (similar).

[1.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,

The combination of Perego, Harris, and Amidi discloses "*a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices [e.g., memory devices 360 in Figs. 3A-3C and 410 in Figs. 4A-4C of Perego] coupled to the set of address and control lines [RQ] and to the set of data lines [DQ].*" Perego discloses the PCB, the address and control lines RQ, and data lines DQ for the reasons discussed above with reference to **claim elements [1.a.2], [1.b.1], [1.b.4]-[1.b.5], and [1.b.7]-[1.b.8]**. *Supra* at 4-11, 13-15, 20-22, 23-25.

Perego also discloses memory devices coupled to the PCB. EX1035 (Perego), Figs. 3C, 4A and 4B (below), 7:30-34 ("Configurable width buffered module 395 includes memory devices 360, channels 370, configurable width buffer device 391 and connector 390."), 9:26-32 ("With reference to FIGS. 4A, 4B and 4C, buffered memory modules ... include buffer device 405 and a plurality of memory devices 410a-410h."). Perego further teaches that the memory devices are coupled to the address and control lines RQ and to data lines DQ. *Id.*, *see also* 9:43-49 ("Signal lines of channels 415a and 415b include control lines (RQ), data lines (DQ) and clock lines (CFM, CTM). The varieties of interconnect topologies, interconnect types, clocking methods, signaling references, signaling methods, and signaling apparatus described above in reference to point-to-point links 320a-320n may equally apply to channels 415a and 415b."), 9:58-60 ("control lines (RQ) may comprise individual control lines, for example, row address strobe, column address strobe, etc., and address lines").

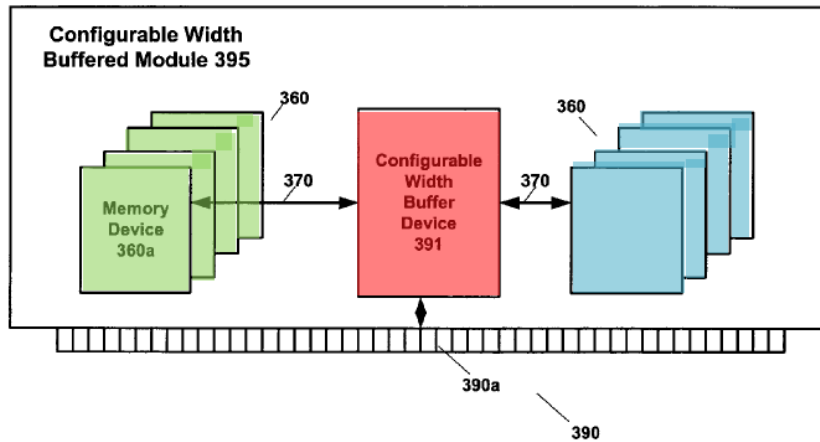


Fig. 3C

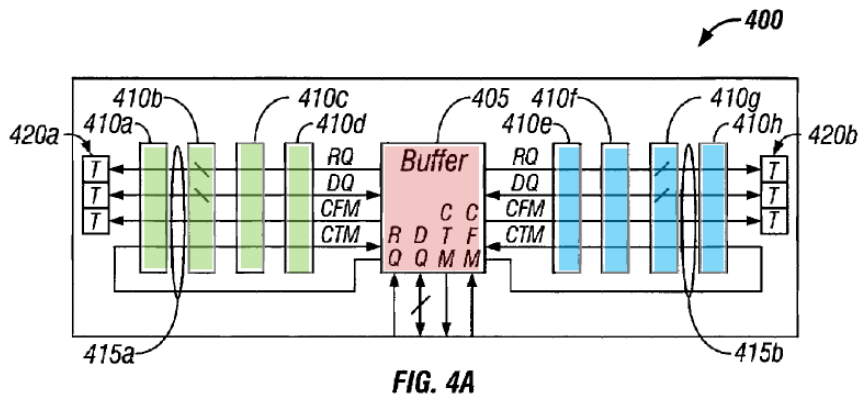


FIG. 4A

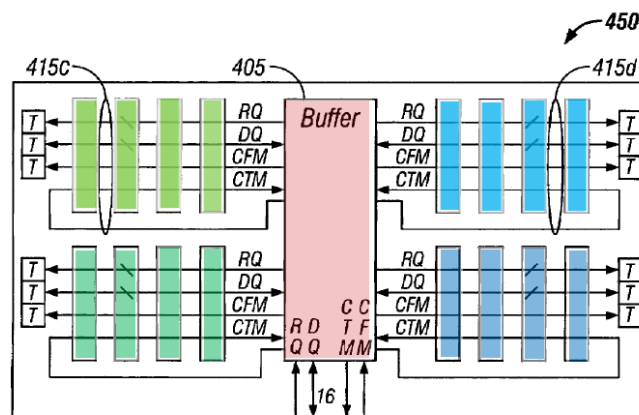


FIG. 4B

Perego further discloses “double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices.” EX1035 (Perego), 8:1-4 (“memory

devices 360 are discretely packaged Synchronous type DRAM integrated circuits (ICs), for example, DDR memory devices”), 10:54-59 (“memory devices may be ... Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.”). Harris and Amidi also disclose memory modules with DDR SDRAMs. EX1023 (Harris), [0009] (“the memory module 100A may be implemented as a Dual In-line Memory Module (DIMM) wherein each of the memory devices 110-1 through 110-N comprises a Double Data Rate (DDR) dynamic random access memory (DRAM) device Also, the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like.”). EX1024 (Amidi) Claim 4 (“the volatile memory is DDR2 SDRAM”); *see also* EX1045, p.Cover (“(DDR) SDRAM”); EX1026, p.Cover-1 (“DDR2 SDRAM”).

[1.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

The combination of Perego, Harris, and Amidi discloses “*the DDR SDRAM devices being operable to receive [during normal write operations] or output [during normal read operations] data signals via the set of data lines [DQ] based on address and control signals [for write and read operations, respectively] received from the system board via the set of address and control lines [RQ],*” as was typical for DDR SDRAM memory devices. *See, e.g.*, EX1035 (Perego), 3:64-4:12 (“A memory device stores data (which may be retrieved) associated with a particular address provided, for example, as part of a write or read command. Examples of types of memory devices include dynamic random access memory (DRAM), static random access memory (SRAM), and double data rate SDRAM (DDR). A memory device typically includes request decode and array access logic that, among other functions, decodes request and address information, and controls memory transfers between a memory array and routing path. A memory device includes a transceiver for transmitting and receiving data in an embodiment of the present invention.”); *see also* EX1026, pp.20-30 (Bank Activate followed by Read and write access modes), Figure 20 (p.21, reproduced below, Bank activate with row address followed by Read command with column address), and Figure 21 (p.22, reproduced below, showing data transfer for read and write commands).

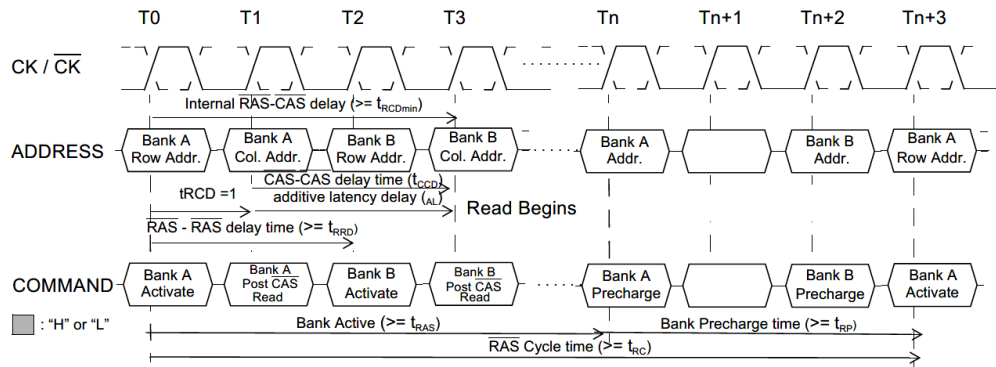


Figure 20 — Bank activate command cycle: $t_{RCD} = 3$, $AL = 2$, $t_{RP} = 3$, $t_{RRD} = 2$, $t_{CCD} = 2$

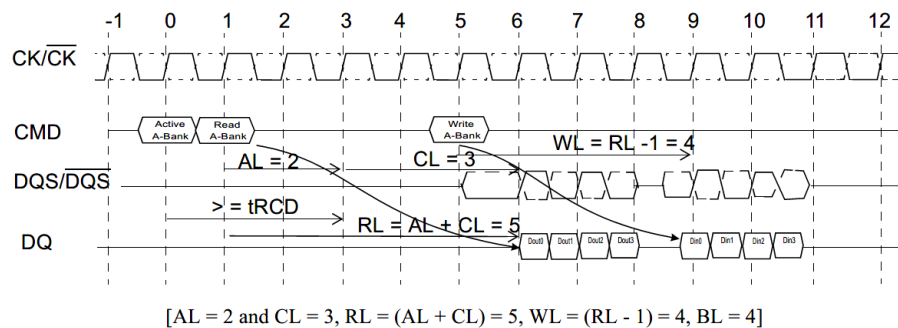


Figure 21 — Example 1: Read followed by a write to the same bank, where $AL = 2$ and $CL = 3$, $RL = (AL + CL) = 5$, $WL = (RL - 1) = 4$, $BL = 4$

Perego also discloses that the address and control signals for memory operations like read and write are received from the system board. EX1035 (Perego), Fig. 3B (below), 6:12-27 (“In a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits corresponding signals to one or more, or all of memory devices 360 via channels 370. One or more of memory devices 360 may respond by transmitting data to Buffer device 350 which receives the data via one or more of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320a. Controller 310 receives the signals corresponding to the data at corresponding ports 378a–378n.”).

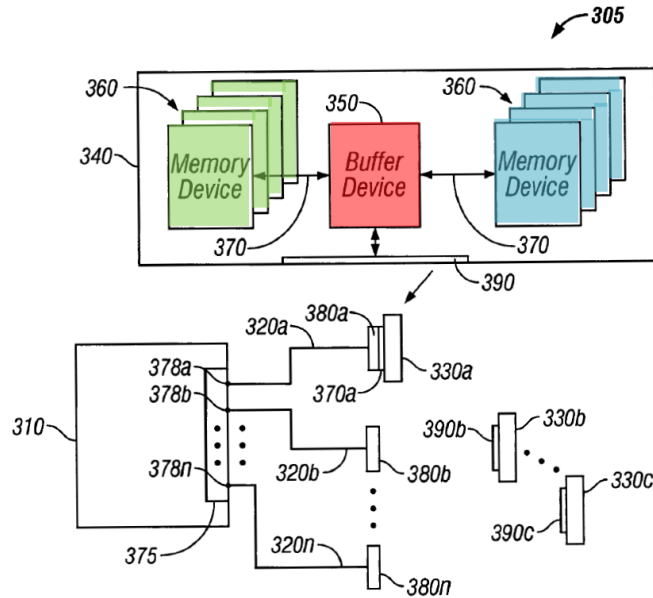


FIG. 3B

[1.e] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

The combination of Perego, Harris, and Amidi discloses “*first, second, third, and fourth converter circuits [e.g., in Voltage Regulator module as taught by Harris] coupled to the PCB and to the [+12V] input voltage supply line, and configured to receive power from the [+12V] input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines [for delivering, respectively, (i) Vdd to the memory devices and to the buffer device and (ii) Vcc to the buffer device taught by Harris, (iii) Vtt for terminating on-board control lines and (iv) VddSPD for the non-volatile memory or SPD device taught by Perego].*” See, e.g., annotated Fig. 3C of Perego (below); EX1003 at ¶¶153-170.

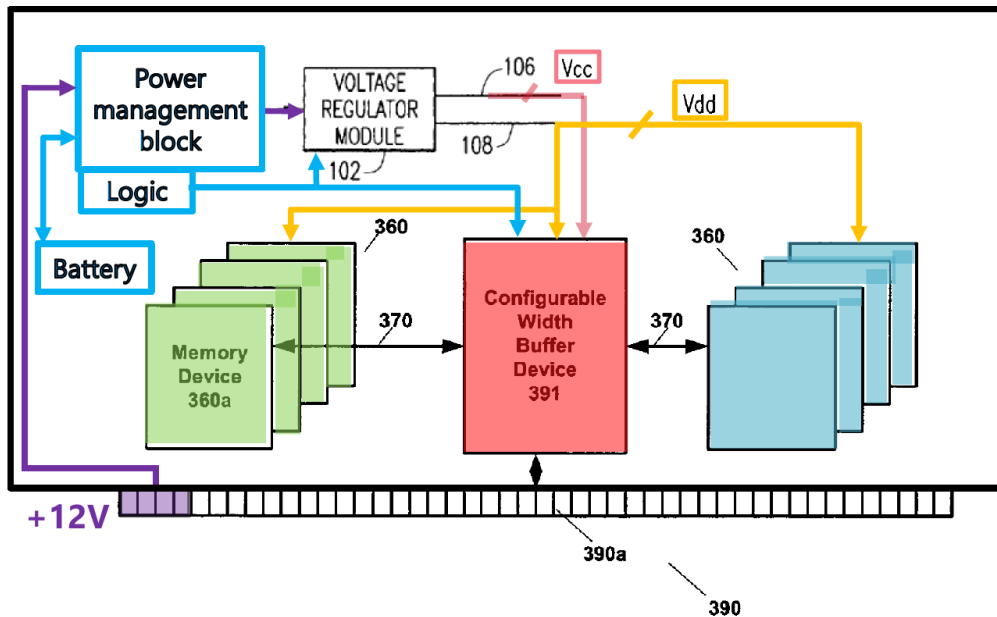


Fig. 3C

Harris teaches that its on-board Voltage Regulator Module (VRM 102) includes “*converter circuits coupled to the PCB*” which provide regulated voltages with “*tightly controlled voltage levels*” for the components of the module. EX1023 (Harris), [0010] (“In accordance with the teachings of the present patent disclosure, at least one on-board voltage regulator module (VRM) is provided as part of the memory board assembly module 100A for converting an externally supplied voltage level available on external source path 104 into appropriate local voltage levels that power the first and second voltage paths, i.e., the V_{dd} and V_{cc} paths 108, 106, respectively. Preferably, a high-frequency switching voltage converter capable of generating tightly-controlled voltage levels may be implemented as the on-board VRM 102 for purposes of the present patent disclosure.”).

Harris also teaches “a first voltage path 108, typically referred to as a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to 3.5V or more.” EX1023 (Harris), [0009]. Perego discloses using DDR2 SDRAM memory devices, EX1035 (Perego), 10:56-59, and Harris teaches that “the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like,” EX1023 (Harris), [0009]. Thus, in a DDR2 implementation, the V_{dd} path would include “*first ... regulated voltage lines*” and the Voltage regulator module would include a “*first ...*”

converter circuit” to convert the +12V input voltage to 1.8V regulated voltage to power DDR2 memories. Perego’s buffer would also receive the regulated V_{dd} voltage (1.8V for DDR2 technology) in order to communicate with those memory devices (e.g., DDR2 memories). *Id.*, [0002] (“As the performance of the DRAM technology goes up, and timing margins shrink, it is becoming increasingly more difficult for the system board sources to provide tightly regulated power for the DRAM cores as well as input/output (I/O) interface buffers.”).

Harris also discloses that “bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a V_{cc} path, are provided with respect to the buffer component 112, wherein the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.” EX1023 (Harris), [0009]. Similar to Harris, Perego also discloses that its DIMM uses a buffer device interfacing with memories on one side and with the memory controller on the other side. *See, e.g.*, EX1035 (Perego), 10:54-67 (“Utilizing buffer device 405 between the memory devices and controller in accordance with the present invention (e.g., see FIG. 3) may feasibly render the type of memory device transparent to the system. Different types of memory devices may be included on different modules within a memory system, by employing buffer device 405 to translate protocols employed by controller 310 to the protocol utilized in a particular memory device implementation.”). Thus, in the combination with Perego, Harris’s V_{cc} path would include “*second ... regulated voltage lines*” and the Voltage regulator module would include a “*second ... converter circuit*” to convert the +12V input voltage to a regulated voltage level as required to power the specific implementation of the buffer device and the DIMM’s memory controller interface of Perego.

Perego also discloses that signals to the memory devices are terminated by termination elements (420). EX1035 (Perego), Fig. 4A (below, annotated), 9:34-38 (“The plurality of signal lines may be controlled impedance transmission lines that are terminated using respective termination elements 420*a* and 420*b*.”).

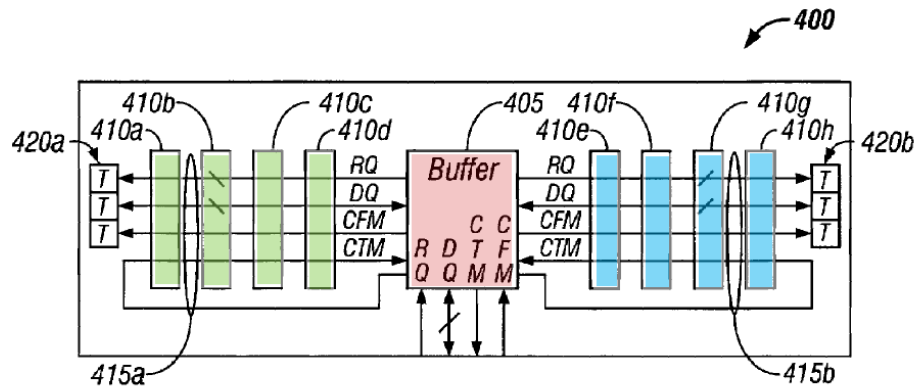


FIG. 4A

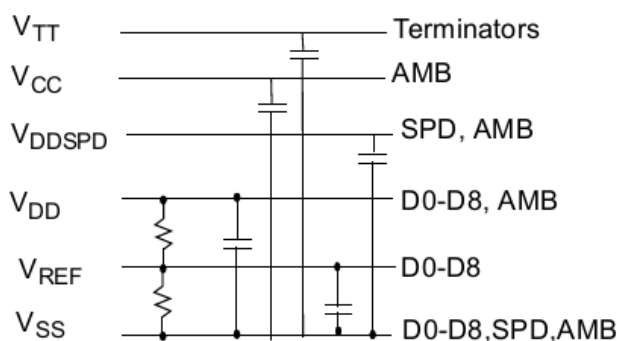
Perego further explains that such “terminator(s) connect to a termination voltage, such as ground or a reference voltage.” *Id.*, 9:1-12. Thus, in the combination with Harris, the Voltage Regulator Module also includes a converter circuit to provide the proper “termination voltage” V_{tt} to terminate signal lines to the memory devices. The Board has already found that it would be obvious in light of Harris to generate V_{tt} on the module using a buck converter. EX1070 (918 FWD), pp.34-38; EX1071 (054 FWD), pp.30-34. In the case of DDR2 memory devices, the address and command lines are terminated by a V_{tt} voltage which is half (i.e., 0.9V) of the memories’ operating voltage V_{dd} (1.8V). EX1026 (JESD79-2B), p.9 (Power-up and initialization sequence includes applying VTT), p.49 (operating condition require VTT to track the reference voltage V_{REF} of $0.5 \times 1.8V$). Thus, in a DDR2 implementation, the paths would include “*third ... regulated voltage lines*” and the Voltage regulator module would include a “*third ... converter circuit*” to convert the +12V input voltage to 0.9V regulated voltage to properly terminate address and command lines to the DDR2 memories.

As discussed above with reference to **claim element [1.c.1]**, Perego also discloses that operations circuit 572 in its buffer device or a separate SPD device includes non-volatile memory. *Supra* at 25-29. Such a non-volatile memory also requires power with a proper voltage for its operation, including power to write information into its non-volatile storage, as discussed above with reference to **claim element [1.c.5]**. *Supra* at 32-35. For example, SPD devices at the time used a voltage of 3.3V. EX1027 (JESD82-20), p.32 (V_{DDSPD} typical value of 3.3V). Thus, in the combination with Perego, Harris’s V_{cc} path would also include “*fourth ... regulated voltage lines*” and the Voltage regulator module would include a “*fourth ... converter circuit*” to convert the +12V input voltage to a

regulated voltage level as required to power the non-volatile memory in the operations circuit 572 in Perego's buffer device or a separate SPD device.

As Harris explained, the specific values of the voltages that are provided by the voltage regulator module depend on the type of the memory module and the technologies used. *See, e.g.,* EX1023 (Harris), [0009] ("Further, the DIMM configuration of an exemplary memory module may include unbuffered DIMMs, registered DIMMs (RDIMMs), or fully buffered DIMMs (FBDs), and may be configured as having one or more ranks (e.g., 2, 4, 8, or more)."). Taking the example of the FBDs, the corresponding JEDEC standards specify the required voltage levels. *See, e.g.,* EX1027 (JESD82-20) p.32 (Advanced Memory Buffer requiring a V_{CC} voltage of 1.5V for its link and core functions, a V_{DD} voltage of 1.8V for interfacing with the DDR2 memories, a V_{DDSPD} voltage of 3.3V for operating the SPD, and "[t]here will also be a V_{TT} termination supply at $V_{DD}/2$ available on the DIMM"); and EX1028 (JESD205) p.9 (listing supply voltages, below), p.13 (reproduced below in part, showing power line connections).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ} , AMB V_{DDQ})
	1.455 ¹	1.5	1.575 ¹	(AMB V_{CC}/V_{CCFBD})
	$0.453 \cdot V_{DD}$	$0.5 \cdot V_{DD}$	$0.547 \cdot V_{DD}$	(DRAM Interface V_{TT}) This supply should track as $0.5 \cdot 1.8$ volt supply
	3.0	3.3	3.6	(V_{DDSPD})



Perego's memory module can use DDR2 memories and a buffer device which interfaces with those memories on one hand and with the system's memory controller on the other, similar to the fully buffered DIMM (FBD) discussed by Harris. *Compare, e.g.,* EX1023 (Harris) at Fig. 1A, *with* EX1035 (Perego) at Fig. 3C.

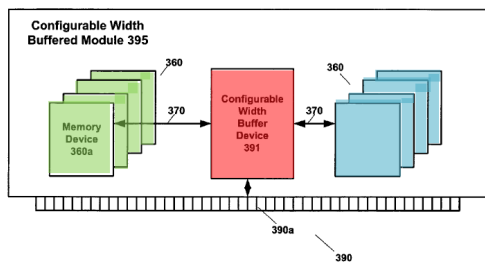


Fig. 3C

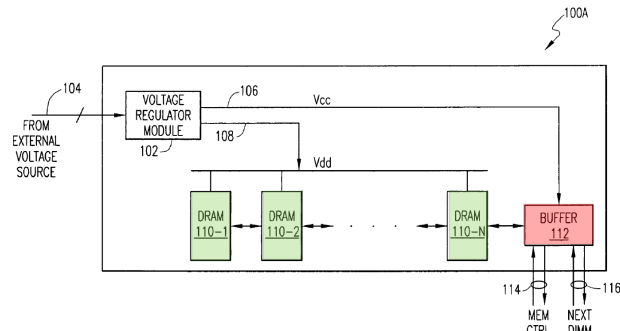


FIG. 1A

Thus, like Harris's FBD, Perego's module in combination with Harris requires the Voltage Regulator Module to include at least four converter circuits to provide at least four voltages: V_{DD} for the memories, V_{CC} for the buffer, V_{TT} to terminate the address and control lines from the buffer to the memories, and V_{DDSPD} for the non-volatile memory, like SPD.

The Board has already considered the issues related to the converter circuits in Harris and rejected Netlist's counter arguments, finding that Harris, in light of the Skilled Artisan's knowledge of the JEDEC standards, renders obvious a memory module having at least four converters, EX1070 (918 FWD) at pp.24-29, including separate buck converters to generate $V_{DD}/V_{DDQ}/V_{DDL}$ or V_{CC}/V_{CCFBD} , *id.* at pp.30-34, a buck converter for the termination voltage V_{TT} , *id.* at pp. 34-38, and a buck converter to provide V_{DDSPD} for the non-volatile memory, *id.* at pp.38-41. The Board also found that the four buck converters provide four respective regulated voltages. *Id.* at pp.56-59. Since Perego's module requires the same or similar voltages as Harris's FBD implementation, the Board's reasons equally apply to the combination of Harris and Perego.

For the reasons discussed above, the combination of Harris, Perego, and Amidi render obvious "*first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines.*" EX1003 at ¶¶153-170.

[1.f.1] wherein the set of components includes:

The combination of Perego, Harris, and Amidi discloses "*the set of components*" of the memory module. *See, e.g.,* Perego at Figs. 4A and 5B (reproduced below).

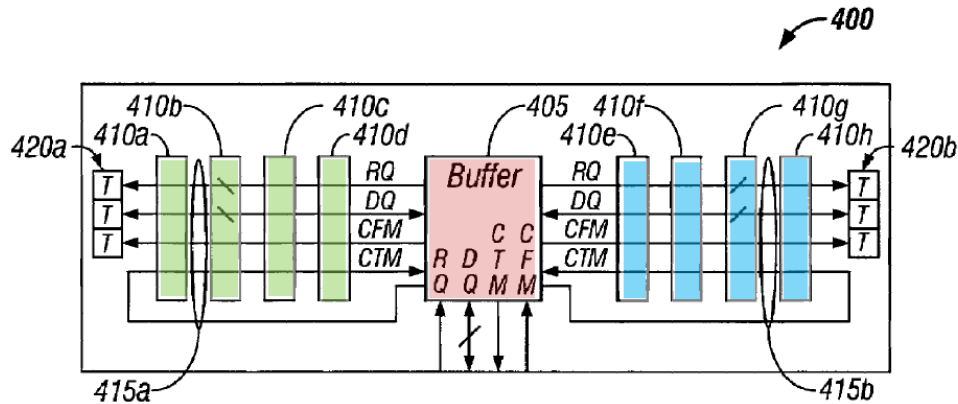


FIG. 4A

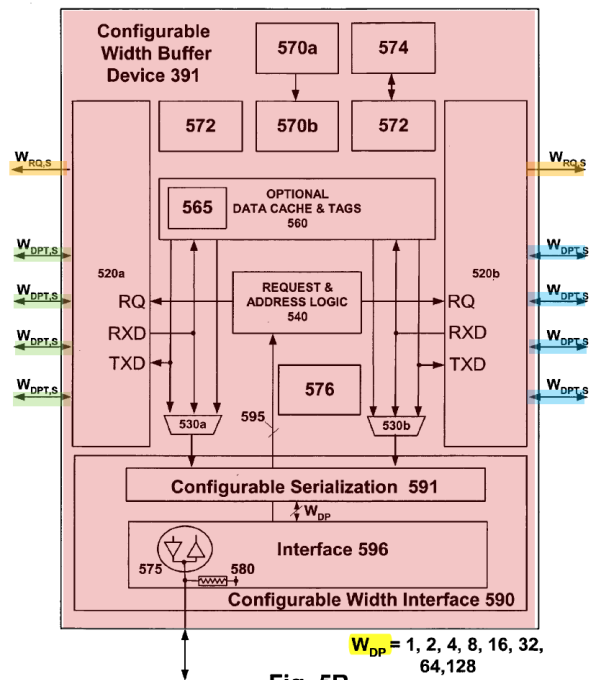


Fig. 5B

[1.f.2] a first component configured to receive power via at least the first regulated voltage line;

The combination of Perego, Harris, and Amidi discloses “a first component [e.g., Perego’s DDR2 memory devices] configured to receive power [Vdd] via at least the first regulated voltage line” for the reasons discussed above with reference to **claim element [1.e]**. *Supra* at 40-45; see, e.g., EX1035 (Perego) 10:54-67 (“Other memory devices may be implemented on module 400, for example, Double Data Rate 2 (DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices.”); EX1023 (Harris), [0009] (“One or more memory devices

110-1 through 110-N are provided as part of the memory module 100A, each receiving a first voltage path 108, typically referred to as a V_{dd} path, that may be energized to appropriate voltage levels depending on the type, functionality, and design of the memory devices, e.g., from about 0.5V to 3.5V or more. ... Also, the memory devices can be of any known or heretofore unknown DDR type, e.g., DDR2 (operable with 1.8 V), DDR3 (operable with 1.35V to 1.5V), and the like.”). See also annotated Fig. 3C of Perego (below). EX1003 at ¶¶153-170.

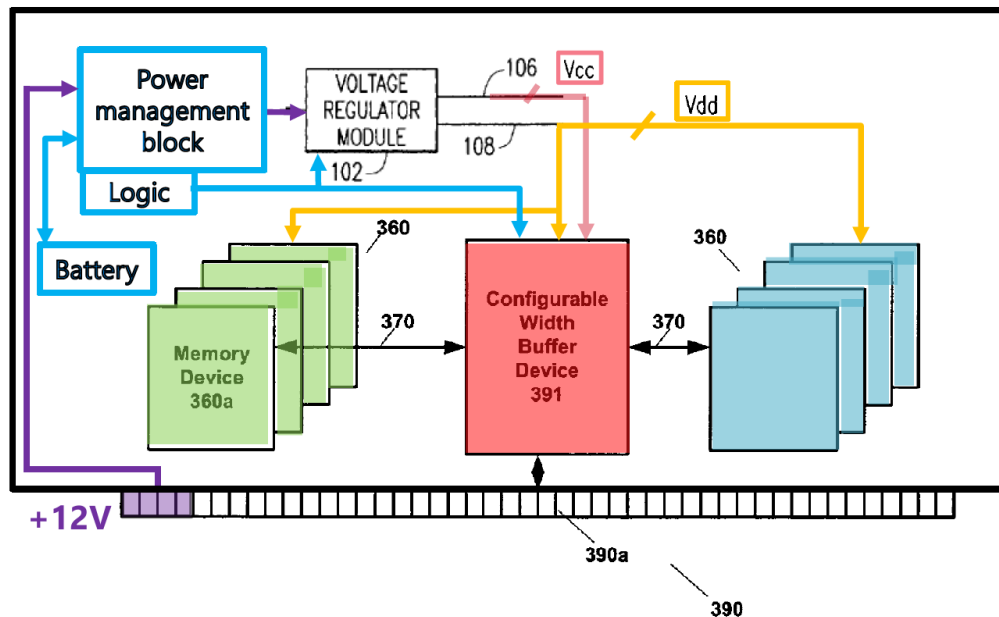
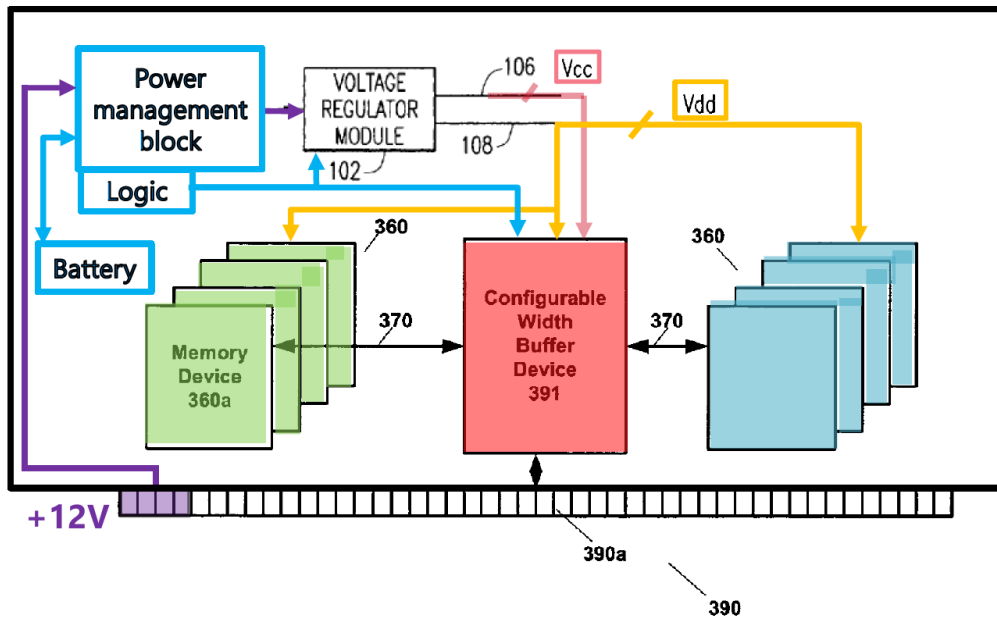


Fig. 3C

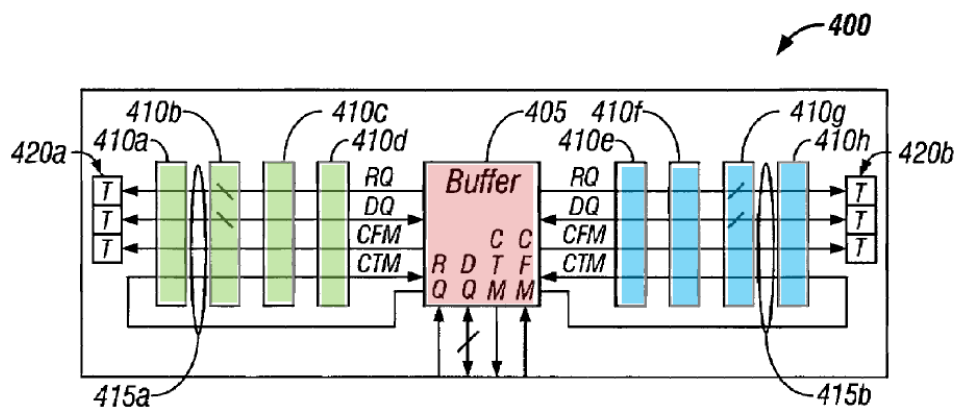
[1.f.3] a second component configured to receive power via at least the second regulated voltage line;

The combination of Perego, Harris, and Amidi discloses “a second component [e.g., Perego’s Buffer device] configured to receive power [V_{cc}] via at least the second regulated voltage line” for the reasons discussed above with reference to **claim element [1.e]**. *Supra* at 40-45; see, e.g., EX1023 (Harris), [0009] (“A bidirectional memory controller interface path 114 as well as a second voltage path 106, typically referred to as a V_{cc} path, are provided with respect to the buffer component 112, wherein the V_{cc} path may be energized to appropriate voltage levels depending on the buffer and DIMM technology, e.g., from about 0.5V to 3.5V or more.”). See also annotated Fig. 3C of Perego (below). EX1003 at ¶¶153-170.



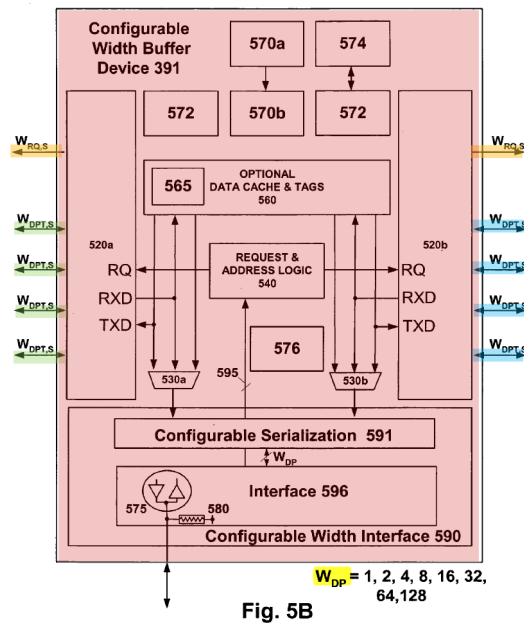
[1.f.4] a third component configured to receive power via at least the third regulated voltage line; and

The combination of Perego, Harris, and Amidi discloses “a third component [e.g., Perego’s termination elements, like 420] *configured to receive power [V_{tt}] via at least the third regulated voltage line*” for the reasons discussed above with reference to **claim element [1.e]**. *Supra* at 40-45; see, e.g., EX1035 (Perego), 9:3-12 (“The terminator(s) connect to a termination voltage, such as ground or a reference voltage.”), Fig. 4A (below).



[1.f.5] a fourth component configured to receive power via at least the fourth regulated voltage line;

The combination of Perego, Harris, and Amidi discloses “a fourth component [e.g., Perego’s operation circuit 572 or SPD] configured to receive power [V_{DDSPD}] via at least the fourth regulated voltage line” for the reasons discussed above with reference to **claim element [1.e]**. *Supra* at 40-45; see, e.g., EX1035 (Perego), Fig. 5B.



[1.g.1] wherein each component of the set of components:

The combination of Perego, Harris, and Amidi discloses “each component of the set of components” for the reasons discussed above with reference to **claim elements [1.f.1]-[1.f.5]**. *Supra* at 45-49.

[1.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

The combination of Perego, Harris, and Amidi discloses that “each component of the set of components ... is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines” for the reasons discussed above with reference to **claim elements [1.f.1]-[1.f.5]**. *Supra* at 45-49.

[1.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,

The combination of Perego, Harris, and Amidi discloses that “each component of the set of components ... receives power only via the one or more of the first, second, third, and fourth regulated voltage lines” for the reasons discussed above with reference to **claim elements [1.f.]-[1.f.5]**. *Supra* at 45-49. For example, the memory module according to the combination uses only the technology-independent voltage distribution by the +12V input voltage to power “each component of the set of components.” See, e.g., annotated Fig. 3C of Perego (below); EX1023 (Harris), [0011] (“Since the V_{dd} and V_{cc} power supply rails are rendered independent from external voltage sources, the overall power supply interface to the memory module 100A is improved to better support large memory capacity scaling, hot-pluggability, DRAM technology independence (e.g., DDR2, DDR3, DDR4, and other DRAM types), high DRAM device count (i.e., amenable to multi-ranking), as well as provide improved system-level cost sharing”), [0020] (“the embodiments are amenable to dual +12V power supply rail implementations”); EX1003 at ¶¶153-170.

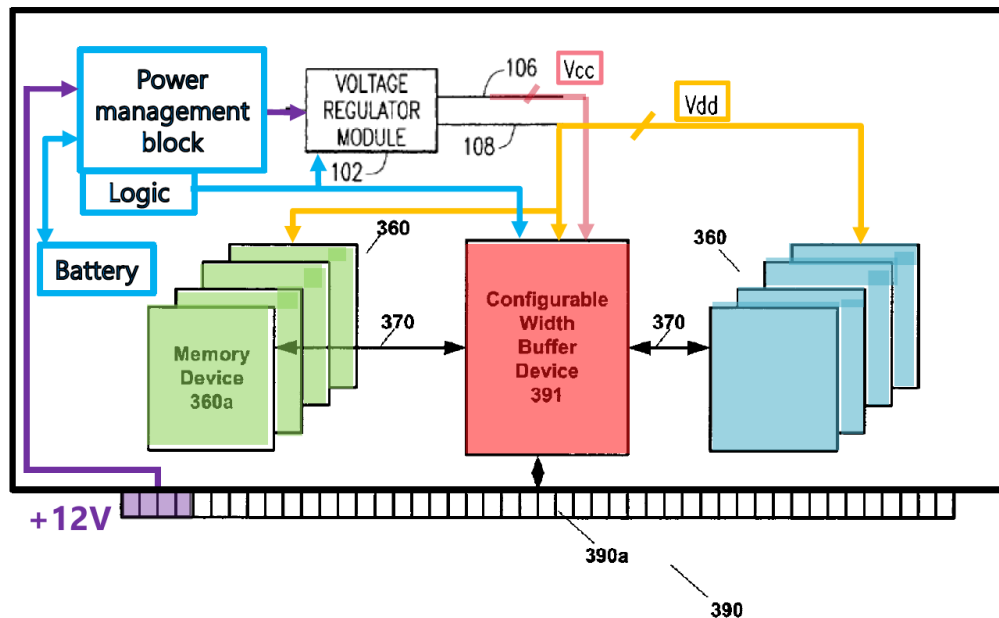


Fig. 3C

In the combination, “the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly,” as taught by Harris, EX1023 (Harris), [0013], thus “each component in the set of components” receives

power only from the corresponding converter circuit “via the one or more of the first, second, third, and fourth regulated voltage lines.”

[1.h.1] wherein the plurality of DDR SDRAM devices includes:

The combination of Perego, Harris, and Amidi discloses “the plurality of DDR SDRAM devices” for the reasons discussed above with reference to **claim element [1.d.1]**. *Supra* at 36-38.

[1.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

The combination of Perego, Harris, and Amidi discloses “a first group of at least five DDR SDRAM devices [5 memory devices in channel 415b or in channel 415d as shown in Perego’s Fig. 4C] that are each connected to a first chip select line configured to electrically conduct a first chip select signal [which selects the memory devices in that channel to transmit or receive data for a read or write operation].” See, e.g., EX1035 (Perego), 21:16-20 (“Any number of channels 415a–415d, for example...two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.”), Fig. 4C (below).

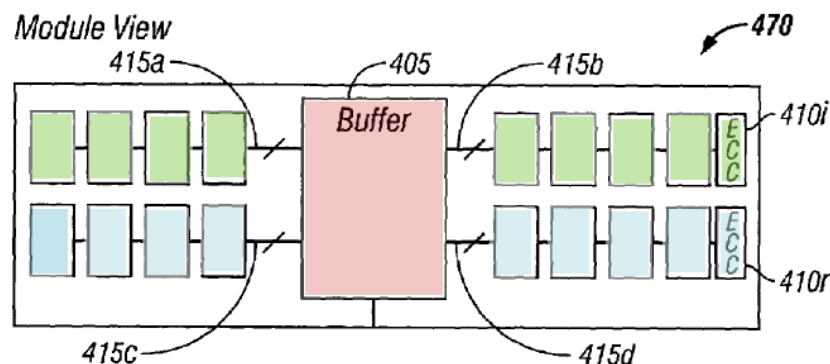


FIG. 4C

Perego explains that, “[i]n a normal memory read operation, buffer device 350 receives control, and address information from controller 310 via point-to-point link 320a and in response, transmits *corresponding signals* to one or more, or all of memory devices 360 via channels 370.” EX1035 (Perego), 6:15-24. As discussed above with reference to **claim element [1.d.1]**, Perego discloses using DDR2 memory devices. *Supra* at 36-38. For a “normal memory read operation” from

such DDR2 memory devices, the signals “corresponding” to “control, and address information” include a “*chip select signal*” which selects the memory devices to perform the operation, as taught by Amidi. EX1024, 7:55-56 (“Truth table 1300 represents the values of signals to memory components of a DDR2 SDRAM”), Fig.13 & n.4 (“Write” and “Read” commands require “CS” chip-select signal asserted Low); EX1026 (JESD79-2B), p.6 (“Chip Select: All commands are masked when CS is registered HIGH. CS provides for external Rank selection on systems with multiple Ranks. CS is considered part of the command code.”), pp.46-47 & n.1 (Command truth table including chip select (CS) signal asserted low for read and write operations); EX1107 (Jacob paper) at 2-3 (“chip-select...is essential”). The chip select signal is required for other memory operations, including write operations, as well. *Id.*

Perego further discloses that “[o]ne or more of memory devices 360 may respond [to the read command] by transmitting data to Buffer device 350 which receives the data via *one or more of channels 370*,” making clear that memory devices in one channel can carry out the read operation. EX1035 (Perego), 6:15-24. Since receiving a chip select signal is needed for the DDR SDRAMs to carry out the read operation and transmit data to the buffer, as discussed directly above, Perego discloses that the “*at least five DDR SDRAM devices [in channel 415b or in channel 415d] ... are each connected to a first chip select line configured to electrically conduct a first chip select signal.*”

[1.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

The combination of Perego, Harris, and Amidi discloses “*a second group of at least four DDR SDRAM devices [4 memory devices in channel 415a or in channel 415c as shown in Perego’s Fig. 4C] that are each connected to a second chip select line configured to electrically conduct a second chip select signal [which selects the memory devices in that channel to transmit or receive data for a read or write operation]*” for the reasons discussed above with reference to **claim element [1.h.2]** and further discussed below. *Supra* at 51-52; see, e.g., EX1035 (Perego), Fig. 4C (below).

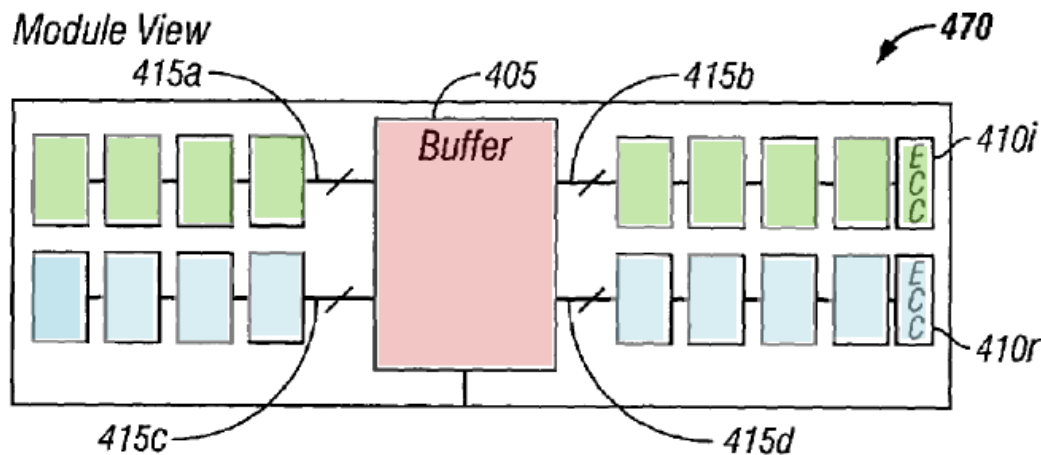


FIG. 4C

For example, Perego discloses that “[a]ny number of channels 415a–415d, for example...two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.” *Id.* 21:16-20. Perego also expressly discloses that the memory devices in a single channel can be selected for a read or write operation. *Id.* 6:15-24 (“Buffer device 350 which receives the data via one or more of channels 370”). Since DDR SDRAMs are selected by chip select signals, and the memory devices in any one of Perego’s channel can be selected for a read or write operation, each channel has its respective chip select signal to carry out the selection, for the reasons discussed above with reference to **claim element [1.h.2]**. *Supra* at 51-52.

Thus, Perego discloses that the “second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal” which selects those four DDR SDRAM devices to perform a read or write operation.

[1.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

The combination of Perego, Harris, and Amidi discloses “when power from the power rails of the system board is provided to the DIMM [in normal mode when power from the system is available] and each group of the first and second groups of DDR SDRAM devices is [being normally accessed or in a ready or standby state thus] not in self-refresh mode [which Amidi discloses being used other times, such as when power from the system is not available].”

For example, Amidi discloses that “[d]uring normal operation of the system with proper power and/or clock operation the system control and command bus input ... will be chosen,” and the memory module operates according to that “system control and command bus input.” EX1024 (Amidi) 7:35-38. Amidi teaches putting the DDR SDRAM devices into self-refresh mode only when the power (or the system clock) fails, as discussed above with reference to **claim element [1.c.5]**, *supra* at 32-35, and shown by Figure 14 of Amidi (below).

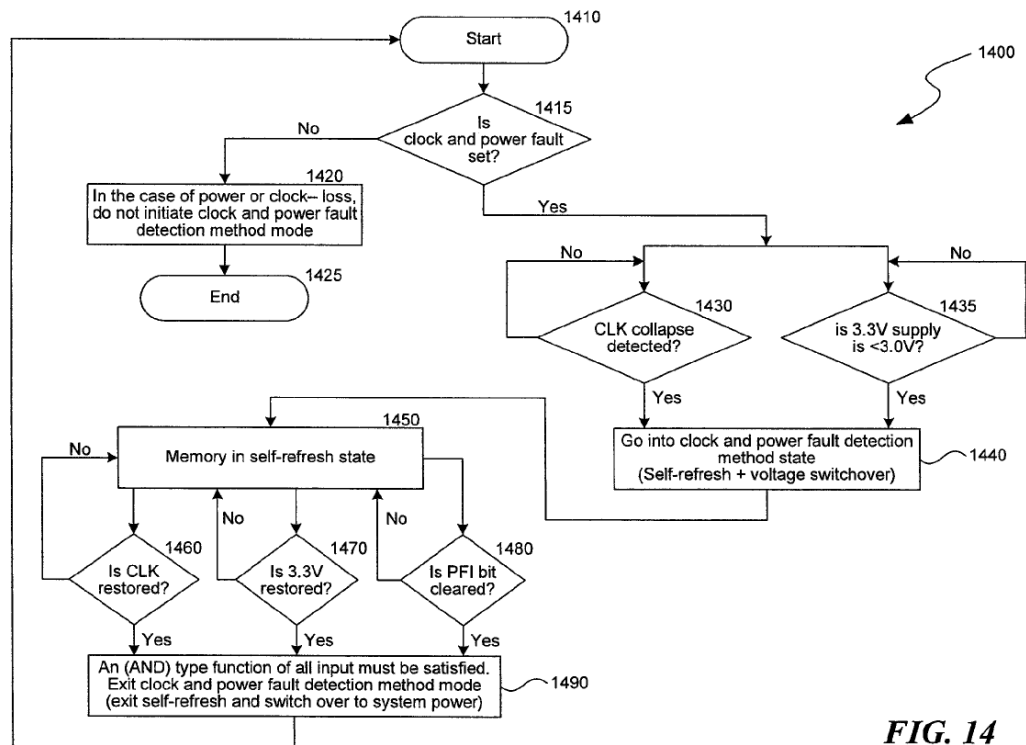


FIG. 14

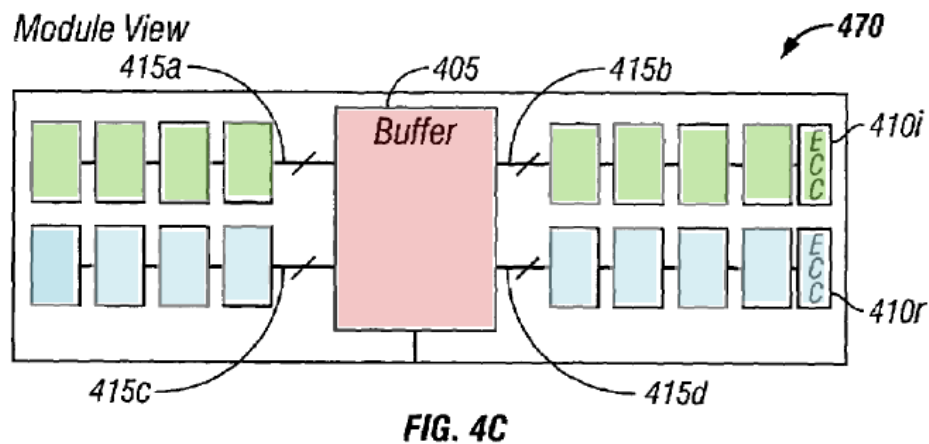
Perego also discloses that, during normal operations, the memories are accessed or they are in a ready or standby state. EX1035 (Perego), 21:16-20 (“Any number of channels 415a–415d, for example[] two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.”). A Skilled Artisan would have understood that, for DDR SDRAMs, the “ready or standby state” is different from the self-refresh mode, because the self-refresh mode disables all but CKE inputs (thus preventing normal read/write commands), turns off ODT, and requires a sequence of commands to exit from, followed by a preset time (e.g., tXSRD) after which other memory operations (e.g., read) can be performed. EX1026 (JESD79-2B), 6 (“Input buffers, excluding CKE, are disabled during self-refresh”), 16 (“ODT is

turned off and not supported in SELF REFRESH mode.”), 39 (“When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are ‘don’t care’. ... The procedure for exiting Self Refresh requires a sequence of commands.”), p.68 (Exit self refresh to a read command time tXSRD has a minimum of 200 clock cycle tCK). Thus, self-refresh mode is not a “ready or standby state,” because the memory in self-refresh mode is not ready to receive and execute memory commands like a read or write command.

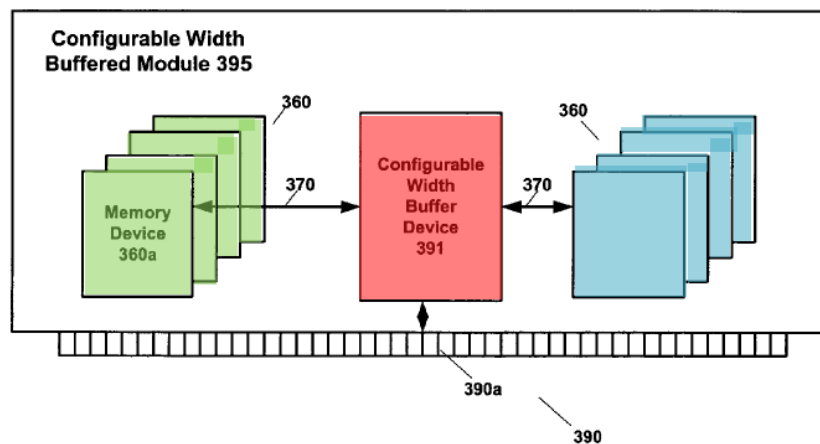
Thus, the combination of Perego, Harris, and Amidi discloses a normal mode “*when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode.*”

[1.i.2] the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

The combination of Perego, Harris, and Amidi discloses that, during normal operation, “*the first group of DDR SDRAM devices [including 5 memory devices in channel 415b or in channel 415d as shown in Perego’s Fig. 4C] is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines [when each of the 5 memory devices in one channel is 8-bit wide, including four x8 memories for data and one x8 memory for ECC] independently of whether the second group of DDR SDRAM devices [including 4 memory devices in channel 415a or in channel 415c as shown in Perego’s Fig. 4C] is enabled, in response to the second chip select signal, to receive or output an integer number of [32=4x8] 1-bit DDR data signals in parallel via an integer number of [32=4x8] data lines of the set of data lines [when each of the 4 memory devices in one channel is 8-bits wide]” for the reasons discussed above with reference to **claim elements [1.h.2]-[1.h.3]** and further discussed below. *Supra* at 51-53; see, e.g., EX1035 (Perego), Fig. 4C (below), and 10:48-53 (“Other features may also be incorporated to enhance module 400 in high capacity memory systems, for example, additional memory devices and interface signals for error correction code storage and transport (ECC). Referring to FIG. 4C, memory devices 410i and 410r intended for ECC are disposed on module 470.”).*



Perego discloses that “[a]ny number of channels 415a–415d, for example...two channels 415c and 415d may transfer information simultaneously and the memory devices on the other two channels 415a and 415b remain in a ready or standby state until called upon to perform memory access operations.” EX1035 (Perego), 21:16-20. As another example, “Buffer device 350 ... receives the data via one ... of channels 370 and in response, transmits corresponding signals to controller 310 via point-to-point link 320 a.” *Id.* 6:15-24, Fig. 3C (below).



Thus, Perego teaches that the memory devices in each of the channels are enabled to output data in response to read commands independent of whether the memory devices in another channel are enabled or not. As discussed above with reference to **claim elements [1.h.2]-[1.h.3]**, the memory devices are enabled for read and write operations by chip select signals. *Supra* at 51-53. Therefore,

Perego discloses that “the first group of [five] DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output ... DDR data signals ... independently of whether the second group of [four] DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output ... DDR data signals.”

Perego further discloses that each of the memory devices can be 8-bits wide (“x8”). EX1035 (Perego), 14:10-15 (“For example, interfaces 520a and 520b may be programmed to connect to 16‘x4’ width memory devices, 8‘x8’ width memory devices or 4‘x16’ width memory devices.”). In fact, 8-bit wide DDR SDRAM memory devices were standardized. See, e.g., EX1026 (JESD79-2B) p.2 (DDR2 SDRAM x8 ballout), pp.7-8 (DDR2 SDRAM addressing for x4, x8 and x16 devices). Accordingly, when the five 8-bit wide memory devices in one channel, for example in channel 415d (FIG. 4C above), are enabled to output data by the “first chip select signal,” they provide a total of $5 \times 8 = 40$ “1-bit DDR data signals in parallel.” EX1035 (Perego), FIG. 4C (above). Similarly, when the four 8-bit wide memory devices in another channel, for example in channel 415c, are enabled by “the second chip select signal,” they provide $4 \times 8 = 32$ “1-bit DDR data signals in parallel.” *Id.*

In the implementation where “two channels 415c and 415d ... transfer information simultaneously,” the total number of data bits received by the buffer device is 72 bits (= 40 bits + 32 bits). EX1035 (Perego), 21:16-20. Perego also discloses that the “Memory Device Access Width” (W_A) can be the same as the Buffer device interface width (W_{DP}), which corresponds to a serialization ratio of one-to-one ($R_S = W_A : W_{DP}$). *Id.*, 14:32-51, 17:26-28 (“For the embodiment illustrated by FIG. 5C, the serialization ratio is 1:1.”). For example, when channels 415c and 415d are accessed simultaneously and channel 415c has four x8 memories and channel 415d has five x8 memories, the 40 bits of data from channel 415d are output to the controller “via at least 40 data lines of the set of data lines,” and the 32 bits of data from channel 415c are output to the controller “via an integer number of [32] data lines of the set of data lines”—a total of 72 data lines. *Id.* Fig. 4C (above). Such 72-bit wide memory modules with 8-bit wide DDR2 SDRAMs were standard at the time. See, e.g., EX1106 (JESD21-C), p.10; EX1090, 24-32 (finding Perego compatible with JEDEC standards); EX1091, 28-37 (same).

Thus, the combination of Perego, Harris, and Amidi discloses that, during normal operation, “the first group of [five 8-bit wide] DDR SDRAM devices [e.g., in channel 415d] is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at

least 40 data lines of the set of data lines independently of whether the second group of [four] DDR SDRAM devices [e.g., in channel 415c] is enabled, in response to the second chip select signal, to receive or output an integer number of [32] 1-bit DDR data signals in parallel via an integer number of [32] data lines of the set of data lines” to the system memory controller.

[1.i.3] the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

The combination of Perego, Harris, and Amidi discloses that “the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals [from 4 of the non-ECC DDR memory devices in channel 415b or in channel 415d] and at least eight 1-bit DDR error-correcting code (ECC) data signals [from the ECC memory device 410i in channel 415b or the ECC memory device 410r in channel 415d]” for the reasons discussed above with reference to **claim element [1.i.2]**. *Supra* at 55-58; see, e.g., EX1035 (Perego), Fig. 4C (below), and 10:48-53 (“Other features may also be incorporated to enhance module 400 in high capacity memory systems, for example, additional memory devices and interface signals for error correction code storage and transport (ECC). Referring to FIG. 4C, memory devices 410i and 410r intended for ECC are disposed on module 470.”).

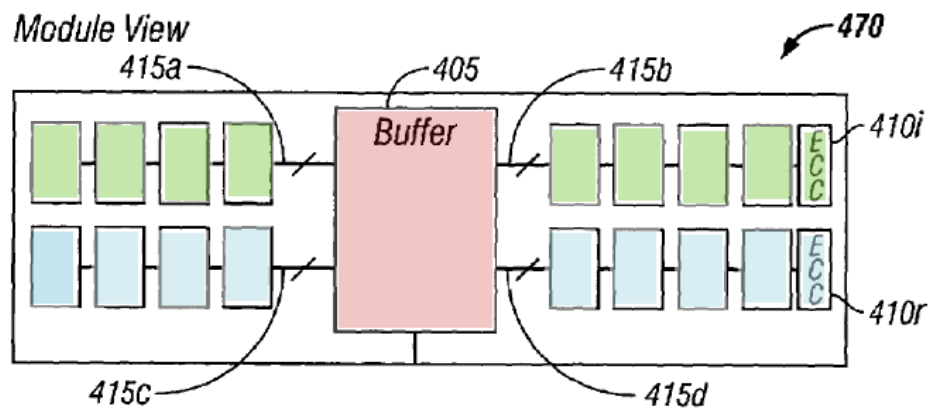


FIG. 4C

[1.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and

The combination of Perego, Harris, and Amidi discloses that “*the sum of the at least 40 data lines [in channel 415b or in channel 415d] and the integer number of [32] data lines [in channel 415a or in channel 415c] equals a total number of [72] data conduits of the set of data conduits of the memory slot connector*” for the reasons discussed above with reference to **claim element [1.i.2]**. *Supra* at 55-58; see, e.g., EX1035 (Perego), 21:16-20 (“Any number of channels 415a–415d, for example...two channels 415 c and 415 d may transfer information simultaneously”), 14:32-51 (serialization ratio $R_S = W_A : W_{DP}$ is the ratio of “Memory Device Access Width” (W_A) and the Buffer device interface width (W_{DP})), 17:26-28 (“... the serialization ratio is 1:1.”).

[1.j.2] the total number of data conduits is at least 72 data conduits.

The combination of Perego, Harris, and Amidi discloses that “*the total number of data conduits is at least 72 data conduits*” for the reasons discussed above with reference to **claim elements [1.i.2] and [1.j1]**. *Supra* at 55-58, 59-59; see, e.g., EX1035 (Perego), Fig. 4C (above), 14:10-15 (“For example, interfaces 520a and 520b may be programmed to connect to 16‘x4’ width memory devices, 8‘x8’ width memory devices or 4“x16” width memory devices.”), and 10:48-53 (“Other features may also be incorporated to enhance module 400 in high capacity memory systems, for example, additional memory devices and interface signals for error correction code storage and transport (ECC). Referring to FIG. 4C, memory devices 410i and 410r intended for ECC are disposed on module 470.”).

Claim 2

[2.a.1] The DIMM of claim 1, wherein the controller further includes:

The combination of Perego, Harris, and Amidi discloses “*the controller*” of claim 1 for the reasons discussed above with reference to **claim elements [1.c.1]-[1.c.6]**. *Supra* at 25-36.

[2.a.2] a data storage element configured to store a plurality of data bits and

The combination of Perego, Harris, and Amidi also discloses that “*the controller further includes ... a data storage element [e.g., a FIFO or a similar*

buffer for writing data to nonvolatile memory] *configured to store a plurality of data bits* [corresponding to one or more pages to be written to nonvolatile memory].” As discussed above with reference to **claim element [1.c.5]**, the proposed combination discloses that “*the controller is configured to perform, in response to the trigger signal, a write operation to write [configuration/status] data into the nonvolatile memory.*” *Supra* at 32-35. To perform such “*a write operation to write [configuration/status] data into the nonvolatile memory*” in an efficient way, a Skilled Artisan would have been motivated to use a temporary “*data storage element*” such as a FIFO or similar buffer to organize the configuration/status data into blocks or pages which the nonvolatile memory was typically organized into, and write those blocks or pages as units from that FIFO or similar buffer into the nonvolatile memory. Using such page write operations reduces the number of write operations into the nonvolatile memory thereby increasing speed and efficiency of the backup operations as discussed below in detail.

A feature of “nonvolatile memory” is that it “may be erased and reprogrammed in units of memory referred to as blocks or pages.” *See, e.g.,* EX1025 (Spiers), [0036]; *see also* EX1110 (EEPROM datasheet), p.1 (“64 byte page”), p.6 (“Up to 64 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Note: Page write operations are limited to writing bytes within a single physical page.”). “When writing a page of data, having a page address, the page is first erased and then data is written to the page.” EX1025 (Spiers), [0049]. Thus, a page write operation writes “*a plurality of data bits*” as a unit corresponding to the size of the page into the nonvolatile memory. *Id.* A Skilled Artisan would have understood that such page write operations can be advantageously used in the proposed combination to write data blocks into nonvolatile memory in case of a power failure. Indeed, the data to be stored in nonvolatile memory is about the status and configuration of the memory module and is meant for recovery and/or failure analysis. Thus, there is no need to store or access each byte of data separately—the status/configuration data can be stored and accessed in blocks for recovery and/or failure analysis. A Skilled Artisan would have also understood that organizing configuration/status data into pages requires temporary storage, such as a FIFO or similar buffer, before the pages are written as units into the nonvolatile memory. For example, Spiers teaches that, in case of a power failure, a “backup device processor writes the data to the FIFO,” which is a “*data storage element*” organized as a first-in-first out buffer having a size corresponding to the size of the page of the nonvolatile memory. *Id.*, [0036], [0050]. After collecting the configuration/status data into the FIFO, “the backup device processor reads the

data from the FIFO” and writes the one or more pages of data into the non-volatile memory. *Id.*

A Skilled Artisan at the time would have been particularly motivated to write data into non-volatile memory in units of pages and to organize the data into such pages before the write operation, because page write operation was a known, reliable technique to efficiently write a block of data into nonvolatile memory. *See, e.g.,* EX1025 (Spiers), [0049-50]; EX1110 (EEPROM datasheet), p.6. A Skilled Artisan would have also been motivated to use a FIFO or similar buffer to collect configuration/status data that needs to be stored in nonvolatile storage in case of a power failure and use one or more page write operations to move entire pages of the collected data into nonvolatile storage instead of writing the data byte-by-byte individually into the nonvolatile storage which would require more write operations, thus more time, and would use more power. EX1025 (Spiers), [0054-55] (“Referring now to FIG. 14, the operational steps performed by the backup device upon detection of a power failure are now described. ... At block 788, the data is written to the data FIFO, and CRC values are generated during the write to the FIFO. At block 792, the page burst length is set to 512, indicating that 512 bytes of data are included in each page when writing to the NVRAM. At block 796, the backup device processor sends a flash page write command. The data is then read from the FIFO, and written to the flash page RAM, as noted by block 800.”).

Thus, the combination of Perego, Harris, and Amidi discloses writing configuration and status data into nonvolatile memory in case of a power failure for the reasons discussed above with reference to **claim element [1.c.5]**, *supra* at 32-35, and a Skilled Artisan would have been motivated to write such data into the nonvolatile memory by the well-known and efficient page write operations, which includes collecting the configuration/status data into “*a data storage element*,” such as a FIFO or similar buffer, and writing one page of data at a time from the FIFO to the nonvolatile memory.

[2.a.3] a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and

The combination of Perego, Harris, and Amidi discloses “*a logic element* [which controls the collection of the configuration/status data into a FIFO or similar buffer device and the write operation from that FIFO or buffer into the nonvolatile memory] *coupled to the nonvolatile memory* [since the logic controls the write operation into the nonvolatile memory] *and the data storage element*

[such as a FIFO or similar buffer device] *and configured to electrically communicate with the nonvolatile memory and the data storage element* [in order to move the configuration/status data from the FIFO or similar buffer into the nonvolatile memory]” for the reasons discussed above with reference to **claim elements [1.c.5] and [2.a.2]**. *Supra* at 32-35, 59-61.

[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes:

The combination of Perego, Harris, and Amidi discloses “*the write operation conducted by the controller in response to the trigger signal*” for the reasons discussed above with reference to **claim element [1.c.5]**. *Supra* at 32-35.

[2.a.5] a first write operation to write a first set of data bits into a first portion of the data storage element;

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan “*a first write operation to write a first set of data bits* [e.g., a first set of configuration or status information for recovery or fault analysis, such as a value that represents the desired width of Perego’s configurable width interface to the memory controller] *into a first portion of the data storage element* [e.g., a first portion of a FIFO or similar buffer of the size corresponding to the page in the nonvolatile memory]” for the reasons discussed above with reference to **claim elements [1.c.5] and [2.a.2]**. *Supra* at 32-35, 59-61; *see, e.g.*, EX1035 (Perego), 16:13-21 (“In addition, state storage may store a plurality of values, for example, a first value that represents the desired width of configurable width interface 590, and a second value that represents the desired width of one or more of interfaces 520a and 520b.”).

[2.a.6] a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

The combination of Perego, Harris, and Amidi also discloses to a Skilled Artisan “*a second write operation to write a second set of data bits* [e.g., a second set of configuration or status information for recovery or fault analysis, such as values for desired widths and/or driver settings for the interfaces to the memory devices] *into a second portion of the data storage element* [e.g., a second portion of a FIFO or similar buffer of the size of the page in the nonvolatile memory]” in order to collect the configuration/status data and organize that data into one or more pages to be stored in the nonvolatile memory for the reasons discussed above with reference to **claim elements [1.c.5] and [2.a.2]**. *Supra* at 32-35, 59-61; *see*,

e.g., EX1035 (Perego), 16:13-21 (“In addition, state storage may store a plurality of values, for example, a first value that represents the desired width of configurable width interface 590, and a second value that represents the desired width of one or more of interfaces 520a and 520b.”); EX1027 (JESD82-20), p.141 (“S3RESTORE ... registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs ... [such as] calibration information for DDR IO drivers. BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up.”).

[2.a.7] a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,

The combination of Perego, Harris, and Amidi also discloses to a Skilled Artisan “a third write operation to write a third set of data bits [a full page of data corresponding to the page size in the nonvolatile memory which includes the collected configuration/status data from [2.a.5] and [2.a.6]] *from the data storage element* [such as a FIFO or similar buffer of the size of the page in the nonvolatile memory] *into the nonvolatile memory* [e.g., in operations circuit 572 or an SPD device]” so that the configuration/status data would be available for recovery and/or failure analysis for the reasons discussed above with reference to **claim elements [1.c.5], [2.a.2], and [2.a.5]-[2.a.6]**. *Supra* at 32-35, 59-61, 62-63.

[2.a.8] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that “the third set of data bits [a page of data written from the FIFO or similar buffer to the nonvolatile memory] *includes the first and second sets of data bits* [including the configuration/status data from [2.a.5] and [2.a.6] collected into the FIFO or similar buffer] *written during the first and second write operations*” so that the configuration/status data would be available for recovery and/or failure analysis for the reasons discussed above with reference to **claim elements [1.c.5], [2.a.2], and [2.a.5]-[2.a.6]**. *Supra* at 32-35, 59-61, 62-63.

Claim 3

[3] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that, “*prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to generate the third set of data bits [in [2.a.8], e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] based on a combination of the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] written during the first and second write operations [e.g., into the FIFO or similar buffer]*” so that the configuration/status data would be available for recovery and/or failure analysis for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63.

Claim 4

[4] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that, “*prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to generate the third set of data bits [in [2.a.8], e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] based on groups of data bits stored in the data storage element including the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] written during the first and second write operations [e.g., into the FIFO or similar buffer]*” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63.

Claim 5

[5] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that, “prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to perform, in response to the detected trigger signal [from [1.c.5]], a plurality of read operations [e.g., from the FIFO or similar buffer] to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data collected in the FIFO or similar buffer] and to generate the third set of data bits [e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages to be written to the nonvolatile memory] based on the read first and second sets of data bits” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63; see also EX1025 (Spiers), [0050] (“... the backup device processor reads the data from the FIFO and writes the data to the NVRAM page RAM. As is also understood, when writing data to a flash memory, the data is written to a page RAM within the flash memory, and the data is then moved from the page RAM to the designated flash page memory. Moving data to NVRAM page RAM is referred to as a page burst, and moving data from the NVRAM page RAM to the NVRAM page is referred to as a NVRAM write.”).

Claim 6

[6] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that, “prior to performing the third write operation [in [2.a.7], e.g., from the FIFO

or similar buffer to the nonvolatile memory], *the logic element is configured to perform, in response to the detected trigger signal* [from [1.c.5]], *a read operation* [e.g., from the FIFO or similar buffer] *to read the first and second sets of data bits from the first and second portions of the data storage element, respectively,* [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data collected in the FIFO or similar buffer] *and to generate the third set of data bits* [e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] *based on the read first and second sets of data bits*” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63; *see also* EX1025 (Spiers), [0050] (“the backup device processor reads the data from the FIFO and writes the data to the NVRAM page RAM. As is also understood, when writing data to a flash memory, the data is written to a page RAM within the flash memory, and the data is then moved from the page RAM to the designated flash page memory. Moving data to NVRAM page RAM is referred to as a page burst, and moving data from the NVRAM page RAM to the NVRAM page is referred to as a NVRAM write.”).

Claim 7

[7] The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that, “*prior to performing the first and second write operations* [from [2.a.5] and [2.a.6], e.g., into the FIFO or similar buffer to collect the configuration/status data for recovery or fault analysis], *the logic element is configured to perform, in response to the detected trigger signal* [from [1.c.5]], *one or more read operations* [e.g., to read the first and second set of configuration/status data from Perego’s “state storage 576,” EX1035, 16:13-21, or DDR SDRAM devices discussed below in claim 8, before moving them into the FIFO or similar buffer]” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63; *see also* EX1035 (Perego) 16:13-21 (“In addition, state storage may store a plurality of values, for example, a first value that represents the desired width of configurable width interface 590, and a second value that represents the desired width of one or more of interfaces 520 *a* and 520 *b*.”); EX1027 (JESD82-20), p.141 (“S3RESTORE ... registers contain implementation dependent state needed to recover connections to DRAMs left in self refresh without destroying data in the DRAMs ... [such as] calibration information for DDR IO drivers.

BIOS will copy these registers into some form of stable storage prior to system standby then restore these registers after system wakes up.”).

Claim 8

[8] The DIMM of claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that “a first read operation of the one or more read operations [of claim 7] by reading the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] from the first and second groups of DDR SDRAM devices” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**, *supra* at 32-35, 59-63, and because it would have been obvious to store configuration and status information in “the first and second groups of DDR SDRAM devices” of Perego before and in preparation for potential backup operations, and to read that configuration and status information from the DDR SDRAM devices and write them into nonvolatile memory in case of a backup operation as discussed below in detail.

For example, Amidi explains that, “as systems become more mission critical, the possibility of irreplaceable data being stored in volatile memory increases. Similarly, failure analysis can be much simpler if information about the state of a system is available after a failure occurs. Moreover, some data may be useful for restarting a system after a failure, even though that information is not otherwise vital for external purposes. Also, some data may simply be desirable for retention purposes, but may also be most useful in volatile memory.” EX1024 (Amidi), 1:19-27. Thus, Amidi teaches to a Skilled Artisan that, at least some data about the configuration and state of a system for recovery and failure analysis may be stored in volatile memory, which a Skilled Artisan understood includes “the first and second groups of DDR SDRAM devices” of Perego in the proposed combination. A Skilled Artisan would have been motivated to store such configuration and state information in Perego’s DDR SDRAM devices, because DDR SDRAMs provided a large capacity and fast storage to collect and store efficiently even larger amount of configuration and status data for recovery and failure analysis at a single location which can be readily accessed in the proposed combination in case of power failure. It would have been obvious to move such configuration and state data from the DDR SDRAM devices into nonvolatile memory, such as those in Perego’s operations circuit (572) or SPD memory, in case of a power failure for the

reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63.

Furthermore, it would have been obvious to store “*the first and second sets of data bits ...[in] the first and second groups of DDR SDRAM devices, respectively,*” because the specific storing locations of different pieces of configuration and status information was a simple design choice.

Claim 9

[9.a.1] The DIMM of claim 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that “*the third write operation [from [2.a.7], e.g., into the nonvolatile memory] comprises a transfer of the third set of data bits [e.g., the full set of the configuration/status data corresponding to one or more pages of the nonvolatile memory] from the data storage element [e.g., the FIFO or similar buffer] to the nonvolatile memory via a first connection [e.g., the connection between the FIFO or similar buffer and the nonvolatile memory]*” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63.

[9.a.2] wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that “*the first and second write operations [from [2.a.5] and [2.a.6], e.g., into the FIFO or similar buffer] comprise a transfer of the first and second sets of data bits into the data storage element [e.g., the FIFO or similar buffer] via a second connection [e.g., between the local storage, such as Perego’s “state storage 576,” which stores the first and second set of configuration/status data, and the FIFO or similar buffer]*” for the reasons discussed above with reference to **claim element [1.c.5]** and **claims 2** and **7**. *Supra* at 32-35, 59-63, 66-67.

Claim 10

[10] The DIMM of claim 2, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.

The combination of Perego, Harris, and Amidi discloses to a Skilled Artisan that “*the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits*” for the reasons discussed above with reference to **claim element [1.c.5]** and **claim 2**. *Supra* at 32-35, 59-63; see, e.g., EX1025 (Spiers), [0048] (“... the backup device processor writes the data to a FIFO and generates a CRC value for the data. The FIFO stores the data for transmission over the bus.”).

Claim 11

[11] The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.

The combination of Perego, Harris, and Amidi discloses that, “*when [+12V] power is provided to the DIMM from the [+12V] power [supply] rails of the system board [see **claim element [1.b.3]**, *supra* at 16-20] the voltage monitor circuit compares the input voltage to a plurality of threshold voltages [as taught by Amidi] including the first threshold voltage [from [1.c.6], e.g., 15% above +12V] and a second threshold voltage [e.g., 15% below +12V]*” for the reasons discussed above with reference to **claim elements [1.c.3] and [1.c.6]**. *Supra* at 30-31, 35-36; see, e.g., EX1023 (Harris), at [0013] (“Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/-15%) can be accommodated”), [0020] (“Further, the embodiments are amenable to dual +12V power supply rail implementations so that industry-standard form factors can be advantageously accommodated.”), EX1024 (Amidi), 9:8-10 (“the system is monitored, with power ... signals checked for proper levels”). The Board has already found that “Amidi discloses detection of undervoltage (EX1024, Fig. 14), [and Amidi’s] ‘power fault’ is broad enough to encompass overvoltage as well.” EX1070, p.79; EX1071, p.65.

Claim 12

[12] The DIMM of claim 1, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.

The combination of Perego, Harris, and Amidi discloses that “the second component [e.g., Perego’s Buffer device, red below] is further connected to the first regulated voltage line [Vdd] and is powered by the first [(Vdd)] and second [(Vcc)] regulated voltages when power from the [+12V] power rails of the system board is provided to the DIMM” for the reasons discussed above with reference to **claim elements [1.e] and [1.f.1]-[1.f.3]**, and illustrated in annotated Fig. 3C of Perego. EX1003 at ¶¶153-170; *supra* at 40-45, 45-48; EX1035 (Perego), Fig. 3C (below, annotated). For example, Perego discloses that its Buffer device (red) communicates with the memory devices (blue and green) powered by a Vdd voltage, thus the Buffer device also uses a Vdd voltage for this communication, similar to the AMB of the standard fully buffered DIMM. See, e.g., EX1028 (JESD205) pp.13-16 (V_{DD} coupled to AMB); EX1027 (JESD82-20), p.32 (Advanced Memory Buffer in normal mode receiving V_{DD}); EX1026 (JESD79-2B), p.49 (DDR2 supply voltage VDDQ is “Supply Voltage for Output”).

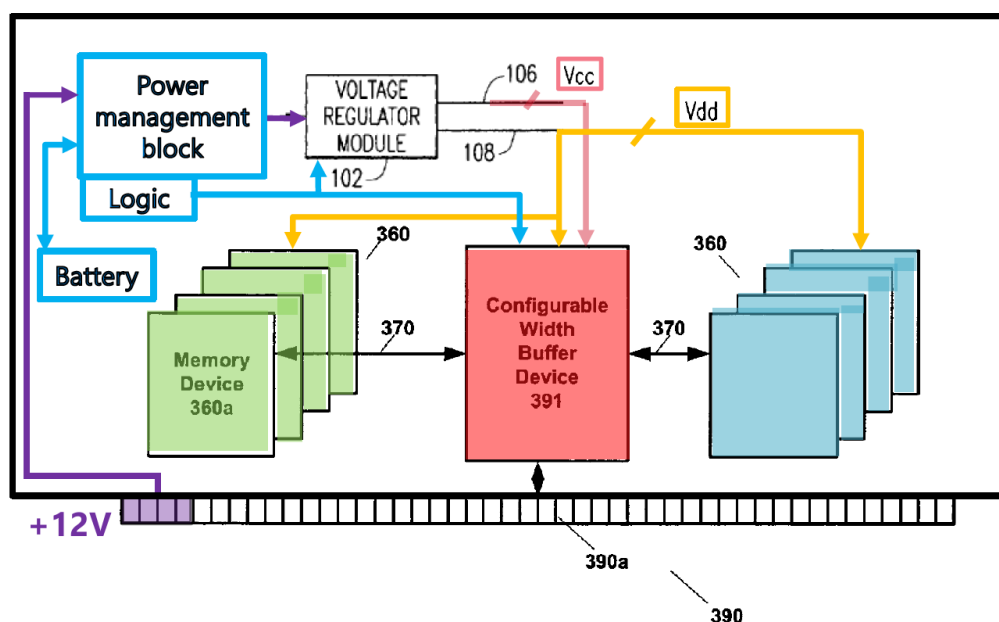


Fig. 3C

Claim 13

[13.a.1] The DIMM of claim 12, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

As an initial matter, the term “*the second threshold*” lacks a proper antecedent basis in claim 12 or claim 1 which claim 13 depends from. The lack of antecedent basis was introduced by Netlist’s amendment during prosecution. EX1002, pp.1401, 1406, 1408 (Amendment dated March 24, 2025, at p.4 (deleting “a second threshold voltage” from pending claim 2), p. 9 (amending pending claim 31 to depend from claim 2 without reciting “second threshold”), p.11 (amending pending claim 43 to depend from claim 31 without amending the term “the second threshold”)).

There are three possible ways to interpret claim 13, discussed below, but the claim is invalid under each interpretation.

First Interpretation: To the extent claim 13 is interpreted to require that “*the first threshold*” is the upper threshold corresponding to an overvoltage “*trigger condition*” in response to which data is written into non-volatile memory as required by base claim 1, and “*the second threshold*” is an even higher threshold voltage, then the ’366 patent lacks any disclosure of such “*second threshold*” or any “*additional trigger condition [which] occurs when the input voltage is above the first threshold and below the second threshold.*” Indeed, Netlist asserted during prosecution that the limitations of issued claim 13 (pending as claim 43) are supported by the following disclosure:

In certain embodiments, the trigger condition occurs when the memory system 1010 **detects** that the **system voltage** is below **a certain threshold voltage**. For example, in one embodiment, the threshold voltage is 10 percent below **a specified operating voltage**. In certain embodiments, **a trigger condition** occurs when the voltage goes above **a certain threshold value**, such as, for example, 10 percent above **a specified operating voltage**. **In some embodiments, a trigger condition occurs when the voltage goes below a threshold or above another threshold.**

EX1002, pp.1449-50 (emphasis by Netlist) (Amendment dated March 24, 2025, Appendix A at pp.17-18); EX1001, 24:34-45. This disclosure, however, lacks any written description of a first threshold above which there is a trigger condition corresponding to an overvoltage, and an even higher second threshold below which there is “*an additional trigger condition.*” *Id.*; EX1003, ¶134.

Second Interpretation: Netlist argued during prosecution that, “[i]f the input voltage[] goes above the second, upper threshold, then by definition it also goes above the first lower threshold.” EX1002, pp.1428-29 (Amendment dated March 24, 2025, at pp.31-32). Under such an interpretation of claim 13, when combined with claims 1 and 12 it depends from, “*the first threshold*” is lower than “*the second threshold*,” and the combination of Perego, Harris, and Amidi discloses that, “*when [+12V] power from the [+12V] power[supply] rails of the system board is provided to the DIMM, an additional trigger condition [indicating to return to normal operation] occurs when the input voltage is [in the normal operating range, that is] above the first threshold [corresponding to the lower edge of the normal operating range, e.g., 15% below +12V] and below the second threshold [corresponding to the upper edge of the normal operating range, e.g., 15% above +12V]*” for the reasons discussed above with reference to **claim 11**, and **claim elements [1.c.3] and [1.c.6]**. *Supra* at 69-69, 30-31, 35-36; see, e.g., EX1023 (Harris), at [0013] (“Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around +/-15%) can be accommodated”; EX1024 (Amidi), 9:8-10 (“the system is monitored, with power ... signals checked for proper levels”), 4:44-55 (“If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660.”).

Third Interpretation: To the extent the claim term “*an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold*” is interpreted as a “trigger condition [which] occurs when the voltage goes below a threshold or above another threshold” as described in the specification, EX1001, 24:34-45 (reproduced immediately above), then the “*second threshold*” can be lower than the “*first threshold.*” In this case, the combination of Perego, Harris, and Amidi discloses that, “*when [+12V] power from the [+12V] power[supply] rails of the system board is provided to the DIMM, an additional trigger condition [indicating out of the normal operating range] occurs when the input voltage is [outside of the normal operating range, that is] above the first threshold [corresponding to the upper edge of the normal operating range, e.g., 15% above +12V] and [or] below the second threshold [corresponding*

to the lower edge of the normal operating range, e.g., 15% below +12V]” for the reasons discussed above with reference to **claim 11**, and **claim elements [1.c.3] and [1.c.6]**. *Supra* at 69-69, 30-31, 35-36; *see, e.g.*, EX1023 (Harris), at [0013] (“Further, since the +12V power supply is not used directly by DRAM devices or buffer/logic components of the memory assembly, a wide tolerance (e.g., around $\pm 15\%$) can be accommodated”; EX1024 (Amidi), 9:8-10 (“the system is monitored, with power ... signals checked for proper levels”), 4:44-55 (“If system supply 605 has a magnitude lower than reference voltage 675, then signal 670 causes power switch multiplexer 655 to choose battery power 650 as a source for memory supply 660.”).

[13.a.2] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

For the reasons discussed above with reference to **claim element [13.a.1]**, to the extent one might interpret claim 13 to require that “*the first threshold*” is the upper threshold corresponding to an overvoltage “*trigger condition*” in response to which data is written into non-volatile memory as required by base claim 1, **and** “*the second threshold*” is an even higher threshold voltage, then the ’366 patent lacks any disclosure of “*the additional trigger condition*” and that, “*in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.*”

In case “*the second threshold*” is lower than “*the first threshold*” and **claim element [13.a.1]** corresponds to a “trigger condition [which] occurs when the voltage goes below a threshold **or** above another threshold” as described in the specification, EX1001, 24:34-45, the combination of Perego, Harris, and Amidi discloses that, “*in response to the additional trigger condition* [corresponding to being out of normal operating range], *the voltage monitor circuit is further configured to generate and transmit a second trigger signal* [similar to a signal value 670 which indicates backup operation, including choosing the power from the battery to power the memory module]” for the reasons discussed above with reference to **claim 11**, and **claim elements [1.c.3] and [1.c.5]-[1.c.6]**. *Supra* at 69-69, 30-31, 32-36.

Under the interpretation that, for the purposes of claim 13, “*the first threshold*” is lower than “*the second threshold*” and the input voltage is above the “*first threshold*” by definition if it is over the “*second threshold*” as argued by Netlist during prosecution and discussed above with reference to **claim element [13.a.1]**, the combination of Perego, Harris, and Amidi discloses that, “*in response to the*

additional trigger condition [corresponding to returning to normal operation], *the voltage monitor circuit is further configured to generate and transmit a second trigger signal* [similar to a signal value 670 which indicates to restore normal operation, including choosing the power from the power rails of the system board to power the memory module]” for the reasons discussed above with reference to **claim element [1.c.5]**. *Supra* at 32-35. For example, Amidi teaches that the memory module restarts normal operations once the power is restored. EX1024, 1:23-25 (“some data may be useful for restarting a system after a failure.”), Fig.15 (below), 4:44-55 (“Signal 670 is controlled by voltage supervisory block 665, which receives system supply 605 and a reference voltage 675, and compares the two. If system supply 605 has a greater magnitude than reference voltage 675, signal 670 causes power switch multiplexer 655 to choose system supply 605 as a source for memory supply 660.”), 8:62-9:2 (“Process 1500 includes...detecting potential restoration, checking whether a system is ready, and restoring control to the system.”).

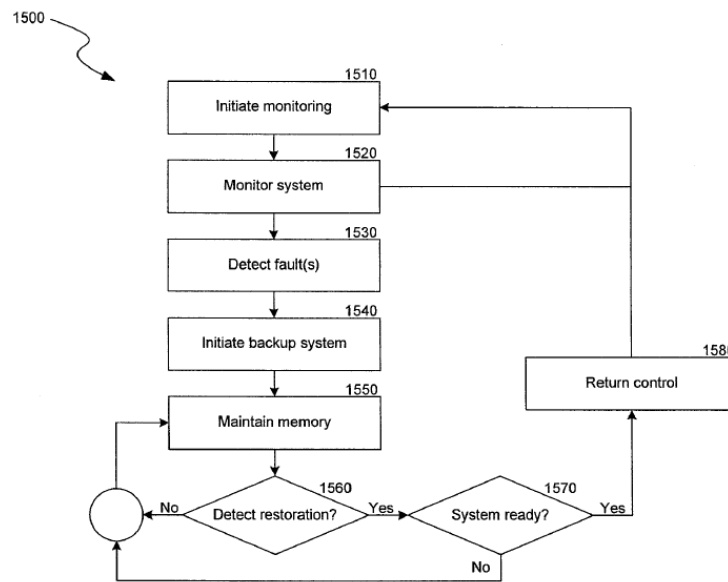


FIG. 15

In the proposed combination, detecting “potential restoration” happens after the voltage monitor circuit detects the return to normal voltage levels and generates a “*second trigger signal*” to indicate to the rest of the module that control can be returned to the system. *Id.*

Claim 14

[14] The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.

The combination of Perego, Harris, and Amidi discloses that, “*when [+12V] power from the [+12V] power rails of the system board is provided to the DIMM, the nonvolatile memory is [powered by the fourth regulated voltage VddSPD, e.g., 3.3V, and is] not powered using the first regulated voltage [Vdd, e.g., 1.8V which is used to power DDR2 memory devices]*” for the reasons discussed above with reference to **claim element [1.e]**. *Supra* at 40-45.

Claim 15

[15] The DIMM of claim 1, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.

The combination of Perego, Harris, and Amidi discloses that “*each of the first, second, and third converter circuits is a buck converter [which efficiently converts the input +12V into lower first, second, and third regulated voltages, respectively], and the fourth converter circuit is a voltage reducing circuit [e.g., another buck converter which efficiently converts the input +12V into the lower fourth regulated voltage]*” for the reasons discussed above with reference to **claim element [1.e]** and in the analysis of the background technology and the motivation to combine. *Supra* at 40-45; EX1003, ¶¶66-70, 161-167. For example, a Skilled Artisan would have understood and been motivated to use well-known (and commercially available) and highly efficient buck converters to convert Harris’s +12V power supply to each of the lower voltage levels that are used on the module of the proposed combination, including the four specific voltages (Vdd, Vcc, Vtt, and VddSPD) discussed above with reference to claim element [1.e]. *Id.*; EX1023, ¶¶[0009]-[0010], [0012] (“high-frequency switching voltage converter” to convert from 12V input to “0.5V to 3.5V”). Indeed, Amidi also discloses using a buck converter to efficiently reduce a higher voltage (3.6V) into a lower regulated voltage (1.8V). EX1024 (Amidi), Fig. 6 (below, annotated).

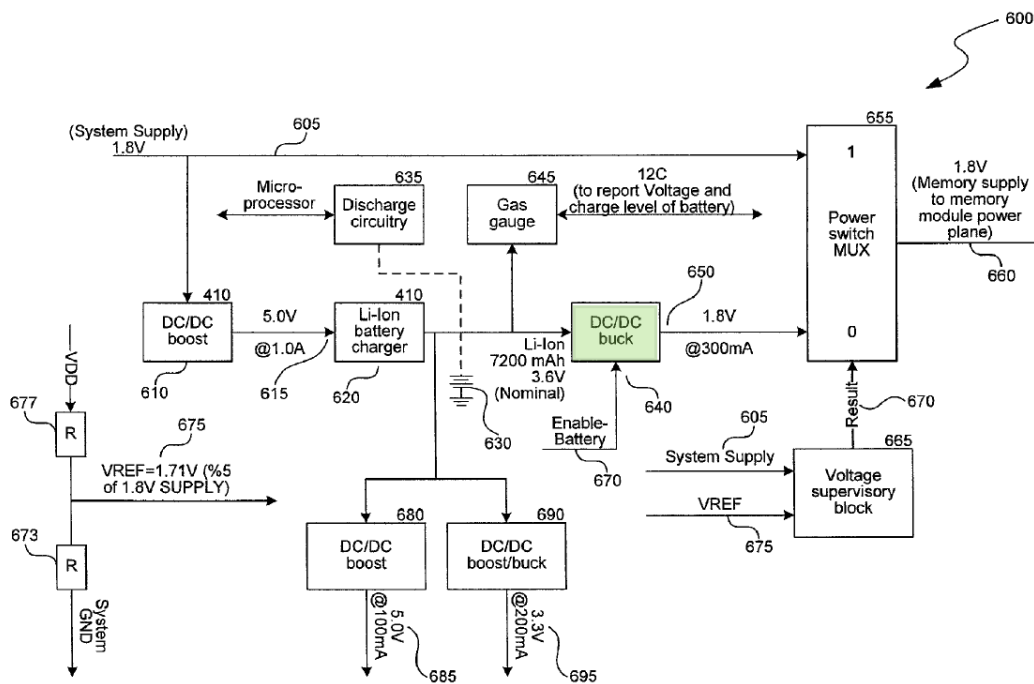


FIG. 6

The use of buck converters to convert a +12V input voltage into different lower voltages was well within the level of skill as evidenced by textbooks and commercially available buck converters. EX1003, ¶¶161-167.

Claim 16 (independent)

[16.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,

Claim limitation **[16.a.1]** is substantially similar to **[1.a.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.1-4.

Claim 1	Claim 16
[1.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,	[16.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,

[16.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,

Claim limitation **[16.a.2]** is substantially similar to **[1.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.4-11.

Claim 1	Claim 16
[1.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,	[16.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,

[16.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and

Claim limitation **[16.a.3]** is substantially similar to **[1.a.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.12-12.

Claim 1	Claim 16
[1.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and	[16.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and

[16.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

Claim limitation **[16.a.4]** is substantially similar to **[1.a.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.12-13.

Claim 1	Claim 16
[1.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:	[16.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

[16.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

Claim limitation **[16.b.1]** is substantially similar to **[1.b.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp. 13-15.

Claim 1	Claim 16
[1.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:	[16.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

[16.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits,

Claim limitation **[16.b.2]** is substantially similar to **[1.b.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.15-16.

Claim 1	Claim 16
[1.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,	[16.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits,

[16.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

Claim limitation **[16.b.3]** is substantially similar to **[1.b.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.16-20.

Claim 1	Claim 16
[1.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;	[16.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

[16.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits,

Claim limitation **[16.b.4]** is substantially similar to **[1.b.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.20-21.

Claim 1	Claim 16
[1.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits, and	[16.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits,

[16.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,

Claim limitation **[16.b.5]** is substantially similar to **[1.b.5]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.21-22.

Claim 1	Claim 16
[1.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,	[16.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,

[16.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

Claim limitation **[16.b.6]** is substantially similar to **[1.b.6]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.22-23.

Claim 1	Claim 16
[1.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,	[16.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

[16.b.7] a set of data lines electrically connected to the second set of edge connections, and

Claim limitation **[16.b.7]** is substantially similar to **[1.b.7]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.23-24.

Claim 1	Claim 16
[1.b.7] a set of data lines electrically connected to the second set of edge connections, and	[16.b.7] a set of data lines electrically connected to the second set of edge connections, and

[16.b.8] a set of address and control lines electrically connected to the third set of edge connections;

Claim limitation **[16.b.8]** is substantially similar to **[1.b.8]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.24-25.

Claim 1	Claim 16
[1.b.8] a set of address and control lines electrically connected to the third set of edge connections;	[16.b.8] a set of address and control lines electrically connected to the third set of edge connections;

[16.c.1] a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

Claim limitation **[16.c.1]** is substantially similar to **[1.c.1]**, **[2.a.1]**, and **[2.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.25-29, 59-61.

Claim 1	Claim 16
[1.c.1] a controller including a voltage monitor circuit ... the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: [2.a.1] The DIMM of claim 1, wherein the controller further includes: [2.a.2] a data storage element configured to store a plurality of data bits and	[16.c.1] a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

[16.c.2] (i) monitor an input voltage supplied via the input voltage supply line;

Claim limitation **[16.c.2]** is substantially similar to **[1.c.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.29-30.

Claim 1	Claim 16
[1.c.2] (i) monitor an input voltage supplied via the input voltage supply line;	[16.c.2] (i) monitor an input voltage supplied via the input voltage supply line;

[16.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and

Claim limitation **[16.c.3]** is substantially similar to **[1.c.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.30-31.

Claim 1	Claim 16
[1.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and	[16.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and

[16.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,

Claim limitation **[16.c.4]** is substantially similar to **[1.c.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.32-32.

Claim 1	Claim 16
[1.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,	[16.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,

[16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

Claim limitation **[16.c.5]** is substantially similar to **[1.c.5]**, **[2.a.4]**, and **[2.a.5]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.32-35, 62-62.

Claims 1, 2	Claim 16
[1.c.5] wherein the controller is configured to perform, in response to the trigger signal, a write operation ..., and [2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.5] a first write operation to write a first set of data bits into a first portion of the data storage element;	[16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

Furthermore, the combination of Perego, Harris, and Amidi discloses to a Skilled Artisan to use a FIFO or similar buffer of the size of one page in the nonvolatile memory, and have the “*controller [...] configured to periodically perform, at regular intervals of time* [corresponding to a time interval required to write one page of data before writing a next page into the nonvolatile memory from the FIFO or similar buffer], *a plurality of write operations* [including write operations to collect one page of configuration/status data into the FIFO or similar buffer and the page write operation of writing the collected one page of data into the nonvolatile memory].”

As discussed above with reference to **claim 2**, Ground 2 discloses to a Skilled Artisan using a temporary “*data storage element*” such as a FIFO or similar buffer to organize the configuration/status data into blocks or pages which the nonvolatile memory was organized into, and write those blocks or pages as units from that FIFO or similar buffer into the nonvolatile memory. *Supra* pp.59-63. Furthermore, it would have been obvious to a Skilled Artisan to have the size of the FIFO or similar buffer to correspond to one page of the nonvolatile memory, and write one page at a time from the FIFO to the non-volatile memory, because it allowed using the efficient page writing feature of the nonvolatile memory without a large sized FIFO or similar buffer. *Id.*

A page write operation into the nonvolatile memory takes a predefined time interval before a subsequent write operation can be started. *See, e.g.*, EX1049 (Flash datasheet), p.1 (“Write performance: Page program: 300µs (TYP)”), p.41 (“Page program time t_{PROG} 300 [Typ] 700 [Max] µs”); EX1110 (EEPROM datasheet), p.1 (“Self-timed ERASE and WRITE cycles (5ms max.)”), p.4 (“TWC Internal Write Cycle Time – 5 ms [Max]”). Therefore, when writing multiple pages of configuration/status data into the nonvolatile memory, Ground 2 renders obvious writing one page at a time into the nonvolatile memory periodically at a regular interval of time which corresponds to the internal write cycle of the nonvolatile memory, and refilling the FIFO or similar buffer with the next page of configuration/status data during that time interval. Accordingly, the proposed combination renders obvious that “*the controller is configured to periodically perform* [for each page], *at regular intervals of time* [corresponding to an Internal Write Cycle Time of the non-volatile memory], *a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element* [such as a FIFO or similar buffer]” as discussed above with reference to **claim elements [1.c.5], [2.a.4], and [2.a.5]**. *Supra* pp.32-35, 62-62.

[16.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,

Claim limitation **[16.d.1]** is substantially similar to **[1.d.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.36-38.

Claim 1	Claim 16
[1.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,	[16.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,

[16.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

Claim limitation **[16.d.2]** is substantially similar to **[1.d.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.38-39.

Claim 1	Claim 16
[1.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and	[16.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

[16.e] first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

Claim limitation **[16.e]** is substantially similar to **[1.e]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.40-45.

Claim 1	Claim 16
[1.e] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,	[16.e] first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

[16.f.1] wherein the set of components includes:

Claim limitation **[16.f.1]** is substantially similar to **[1.f.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.45-46.

Claim 1	Claim 16
[1.f.1] wherein the set of components includes:	[16.f.1] wherein the set of components includes:

[16.f.2] a first component configured to receive power via the first regulated voltage line;

Claim limitation **[16.f.2]** is substantially similar to **[1.f.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.46-47.

Claim 1	Claim 16
[1.f.2] a first component configured to receive power via at least the first regulated voltage line;	[16.f.2] a first component configured to receive power via the first regulated voltage line;

[16.f.3] a second component configured to receive power via the second regulated voltage line;

Claim limitation **[16.f.3]** is substantially similar to **[1.f.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.47-48.

Claim 1	Claim 16
[1.f.3] a second component configured to receive power via at least the second regulated voltage line;	[16.f.3] a second component configured to receive power via the second regulated voltage line;

[16.f.4] a third component configured to receive power via the third regulated voltage line; and

Claim limitation **[16.f.4]** is substantially similar to **[1.f.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.48-48.

Claim 1	Claim 16
[1.f.4] a third component configured to receive power via at least the third regulated voltage line; and	[16.f.4] a third component configured to receive power via the third regulated voltage line; and

[16.f.5] a fourth component configured to receive power via the fourth regulated voltage line;

Claim limitation **[16.f.5]** is substantially similar to **[1.f.5]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 16
[1.f.5] a fourth component configured to receive power via at least the fourth regulated voltage line;	[16.f.5] a fourth component configured to receive power via the fourth regulated voltage line;

[16.g.1] wherein each component of the set of components:

Claim limitation **[16.g.1]** is substantially similar to **[1.g.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 16
[1.g.1] wherein each component of the set of components:	[16.g.1] wherein each component of the set of components:

[16.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;

Claim limitation **[16.g.2]** is substantially similar to **[1.g.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 16
[1.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and	[16.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;

[16.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

Claim limitation **[16.g.3]** is substantially similar to **[1.g.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.50-51.

Claim 1	Claim 16
[1.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,	[16.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and

[16.h.1] wherein the plurality of DDR SDRAM devices includes:

Claim limitation **[16.h.1]** is substantially similar to **[1.h.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.51-51.

Claim 1	Claim 16
[1.h.1] wherein the plurality of DDR SDRAM devices includes:	[16.h.1] wherein the plurality of DDR SDRAM devices includes:

[16.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

Claim limitation **[16.h.2]** is substantially similar to **[1.h.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.51-52.

Claim 1	Claim 16
[1.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;	[16.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

[16.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

Claim limitation **[16.h.3]** is substantially similar to **[1.h.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.52-53.

Claim 1	Claim 16
[1.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;	[16.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

[16.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

Claim limitation **[16.i.1]** is substantially similar to **[1.i.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.53-55.

Claim 1	Claim 16
[1.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:	[16.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

[16.i.2] the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

Claim limitation **[16.i.2]** is substantially similar to **[1.i.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.55-58.

Claim 1	Claim 16
[1.i.2] the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;	[16.i.2] the first group of DDR SDRAM packages ^[1] is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages ^[2] is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

[16.i.3] the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

Claim limitation **[16.i.3]** is substantially similar to **[1.i.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.58-58.

¹ “[T]he first group of **DDR SDRAM packages**” has no antecedent basis. This term should have been “the first group of **at least five DDR SDRAM devices**” as recited in [16.h.2].

² “[T]he second group of **DDR SDRAM packages**” has no antecedent basis. This term should have been “the second group of **at least four DDR SDRAM devices**” as recited in [16.h.3].

Claim 1	Claim 16
[1.i.3] the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and	[16.i.3] the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

[16.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and

Claim limitation **[16.j.1]** is substantially similar to **[1.j.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.59-59.

Claim 1	Claim 16
[1.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and	[16.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and

[16.j.2] the total number of data conduits is at least 72 data conduits.

Claim limitation **[16.j.2]** is substantially similar to **[1.j.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.59-59.

Claim 1	Claim 16
[1.j.2] the total number of data conduits is at least 72 data conduits.	[16.j.2] the total number of data conduits is at least 72 data conduits.

Claim 17

[17] The DIMM of claim 16, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

Claim limitation [17] is substantially similar to [1.c.1] and [2.a.1]-[2.a.3] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.25-29, 59-62.

Claim 2	Claim 17
[1.c.1] a controller including a ... nonvolatile memory ... [2.a.1] The DIMM of claim 1, wherein the controller further includes: [2.a.2] a data storage element configured to store a plurality of data bits and [2.a.3] a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and	[17] The DIMM of claim 16, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.

Claim 18

[18] The DIMM of claim 17, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

Claim limitation [18] is substantially similar to [2.a.4] and [2.a.6] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.62-62, 62-63.

Claim 2	Claim 18
[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.6] a second write operation to write a second set of data bits into a second portion of the data storage element ...	[18] The DIMM of claim 17, wherein the logic element [included in the controller of claim 17] is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.

Claim 19

[19.a.1] The DIMM of claim 18, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory,

Claim limitation [19.a.1] is substantially similar to [2.a.4], [2.a.6], and [2.a.7] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.62-62, 62-63.

Claim 2	Claim 19
[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.6] ... and subsequently [2.a.7] a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,	[19.a.1] The DIMM of claim 18, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory,

[19.a.2] wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and

Claim limitation **[19.a.2]** is substantially similar to **[2.a.8]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.63-63.

Claim 2	Claim 19
[2.a.8] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.	[19.a.2] wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and

[19.a.3] wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

Claim limitation **[19.a.3]** is substantially similar to claim elements **[16.c.5]**, **[2.a.6]**, and **[2.a.7]**, and as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.83-84, 62-63.

Claims 2 and 16	Claim 19
[16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element; [2.a.6] a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently [2.a.7] a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,	[19.a.3] wherein, in response to the detected trigger condition, the logic element [included in the controller of claim 17] is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

Furthermore, as discussed above with reference to **claim element [16.c.5]** and **claim 2**, Ground 2 renders obvious “*to periodically perform, at regular intervals of time, a plurality of write operations*” in order to write multiple pages of configuration/status data into the nonvolatile memory one page at a time, each page of data being collected into a FIFO or similar buffer having a size of one-page. Thus, each page write cycle includes “*the first and second write operations [of configuration/status data pieces into the FIFO or similar buffer] followed by the third write operation [of the entire page from the FIFO or similar buffer into the nonvolatile memory]*.” As also discussed above with reference to **claim element [16.c.5]**, the “*regular intervals of time*” corresponds to the page write cycle of the nonvolatile memory, which is on the order of one millisecond depending on the specific implementation (e.g., between 300 μ s and 5 ms). *Supra* pp.83-84; *see, e.g.*, EX1049 (Flash datasheet), p.1 (“Write performance: Page program: 300 μ s (TYP)”), p.41 (“Page program time t_{PROG} 300 [Typ] 700 [Max] μ s”); EX1110 (EEPROM datasheet), p.1 (“Self-timed ERASE and WRITE cycles (5ms max.)”), p.4 (“TWC Internal Write Cycle Time – 5 ms [Max]”). It would have been a simple design choice, thus obvious, to a Skilled Artisan to choose a specific nonvolatile

memory and a corresponding write cycle time that allows “*to periodically perform every millisecond*” a page write operation into the nonvolatile memory, because nonvolatile memories with page write cycle around one millisecond were available. For example, a Skilled Artisan would have understood that a page write operation can be safely performed “every millisecond” into a nonvolatile memory with a write cycle time somewhat less than 1 ms in order to allow for potential timing issues, such as delays and skews.

Claim 20

[20] The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

Claim limitation [20] is substantially similar to **claim 5** and **claim element [16.c.5]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.65-65, 83-84.

Claim 5	Claim 20
[5] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits. [16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;	[20] The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.

Claim 21

[21.a.1] The DIMM of claim 19, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and

Claim limitation **[21.a.1]** is substantially similar to **[2.a.4]** and **[2.a.7]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.62-62, 63-63.

Claim 2	Claim 21
[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.7] a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,	[21.a.1] The DIMM of claim 19, wherein the logic element [included in the controller of claim 17] is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and

[21.a.2] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

Claim limitation **[21.a.2]** is substantially similar to **[2.a.8]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.63-63.

Claim 2	Claim 21
[2.a.8] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.	[21.a.2] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.

Claim 22

[22] The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

Claim limitation **[22]** is substantially similar to **[4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.64-64.

Claim 4	Claim 22
[4] The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element ...	[22] The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.

Claim 23

[23.a.1] The DIMM of claim 19, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and

Claim limitation **[23.a.1]** is substantially similar to **[2.a.8]** and **[9.a.1]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.63-63, 68-68.

Claims 2, 9	Claim 23
[2.a.8] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations. [9.a.1] The DIMM of claim 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and	[23.a.1] The DIMM of claim 19, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and

[23.a.2] wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

Claim limitation **[23.a.2]** is substantially similar to **[9.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.68-68.

Claim 9	Claim 23
[9.a.2] wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.	[23.a.2] wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.

Claim 24

[24] The DIMM of claim 18, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

Claim limitation **[24]** is substantially similar to **claims 7 and 8** and **claim element [16.c.5]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.66-68, 83-84.

Claims 7, 8	Claim 24
[7] The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations. [8] The DIMM of claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively. [16.c.5] wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;	[24] The DIMM of claim 18, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

Claim 25

[25] The DIMM of claim 16, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

Claim limitation **[25]** is substantially similar to **[14]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.75-75.

Claim 14	Claim 25
[14] The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.	[25] The DIMM of claim 16, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

Claim 26

[26] The DIMM of claim 16, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

Claim limitation **[26]** is substantially similar to **[11]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.69-69.

Claim 11	Claim 26
[11] The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.	[26] The DIMM of claim 16, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

Claim 27

[27] The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

Claim limitation [27] is substantially similar to [1.c.6] and [11] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.35-36, 69-69.

Claims 1, 11	Claim 27
[1.c.6] wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage; [11] The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage ...	[27] The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

Claim 28

[28.a] The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

Claim limitation [28.a] is substantially similar to [13.a.1] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.71-73.

Claim 13	Claim 28
[13.a.1] The DIMM of claim 12, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and	[28.a] The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

[28.b] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

Claim limitation **[28.b]** is substantially similar to **[13.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.73-74.

Claim 13	Claim 28
[13.a.2] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.	[28.b] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

Claim 29 (independent)

[29.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,

Claim limitation **[29.a.1]** is substantially similar to **[1.a.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.1-4.

Claim 1	Claim 29
[1.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,	[29.a.1] A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,

[29.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,

Claim limitation **[29.a.2]** is substantially similar to **[1.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.4-11.

Claim 1	Claim 29
[1.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,	[29.a.2] the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,

[29.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and

Claim limitation **[29.a.3]** is substantially similar to **[1.a.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.12-12.

Claim 1	Claim 29
[1.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and	[29.a.3] wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and

[29.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

Claim limitation **[29.a.4]** is substantially similar to **[1.a.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.12-13.

Claim 1	Claim 29
[1.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:	[29.a.4] address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

[29.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:

Claim limitation **[29.b.1]** is substantially similar to **[1.b.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.13-15.

Claim 1	Claim 29
[1.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:	[29.b.1] a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:

[29.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits,

Claim limitation **[29.b.2]** is substantially similar to **[1.b.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.15-16.

Claim 1	Claim 29
[1.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,	[29.b.2] a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits,

[29.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

Claim limitation **[29.b.3]** is substantially similar to **[1.b.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.16-20.

Claim 1	Claim 29
[1.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;	[29.b.3] wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,

[29.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits,

Claim limitation **[29.b.4]** is substantially similar to **[1.b.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.20-21.

Claim 1	Claim 29
[1.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits, and	[29.b.4] a second set of edge connections configured to be electrically connected to the set of data conduits,

[29.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,

Claim limitation [29.b.5] is substantially similar to [1.b.5] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.21-22.

Claim 1	Claim 29
[1.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,	[29.b.5] a third set of edge connections configured to be electrically connected to the set of address and control conduits,

[29.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

Claim limitation [29.b.6] is substantially similar to [1.b.6] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.22-23.

Claim 1	Claim 29
[1.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,	[29.b.6] a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

[29.b.7] a set of data lines electrically connected to the second set of edge connections, and

Claim limitation [29.b.7] is substantially similar to [1.b.7] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.23-24.

Claim 1	Claim 29
[1.b.7] a set of data lines electrically connected to the second set of edge connections, and	[29.b.7] a set of data lines electrically connected to the second set of edge connections, and

[29.b.8] a set of address and control lines electrically connected to the third set of edge connections,

Claim limitation [29.b.8] is substantially similar to [1.b.8] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.24-25.

Claim 1	Claim 29
[1.b.8] a set of address and control lines electrically connected to the third set of edge connections;	[29.b.8] a set of address and control lines electrically connected to the third set of edge connections,

[29.b.9] wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection,

Claim limitation [29.b.9] is substantially similar to [1.b.7] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.23-24.

Claim 1	Claim 29
[1.b.7] a set of data lines electrically connected to the second set of edge connections, and	[29.b.9] wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection,

[29.b.10] wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;

Claim limitation [29.b.10] is substantially similar to [1.i.2] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.55-58.

Claim 1	Claim 29
[1.i.2] the first group of DDR SDRAM devices to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines ...	[29.b.10] wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;

DRAM devices communicating “40 1-bit DDR data signals in parallel via ... 40 data lines of the set of data lines” in [1.i.2] means “each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal” in [29.b.10].

[29.c.1] a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

Claim limitation [29.c.1] is substantially similar to [1.c.1], [2.a.1], and [2.a.2] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.25-29, 59-61.

Claim 1	Claim 29
[1.c.1] a controller including a voltage monitor circuit ... the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: [2.a.1] The DIMM of claim 1, wherein the controller further includes: [2.a.2] a data storage element configured to store a plurality of data bits and	[29.c.1] a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:

[29.c.2] (i) monitor an input voltage supplied via the input voltage supply line;

Claim limitation **[29.c.2]** is substantially similar to **[1.c.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.29-30.

Claim 1	Claim 29
[1.c.2] (i) monitor an input voltage supplied via the input voltage supply line;	[29.c.2] (i) monitor an input voltage supplied via the input voltage supply line;

[29.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and

Claim limitation **[29.c.3]** is substantially similar to **[1.c.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.30-31.

Claim 1	Claim 29
[1.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and	[29.c.3] (ii) generate a trigger signal upon detecting a trigger condition; and

[29.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,

Claim limitation **[29.c.4]** is substantially similar to **[1.c.4]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.32-32.

Claim 1	Claim 29
[1.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,	[29.c.4] (iii) transmit the trigger signal to at least one other portion of the controller,

[29.c.5] wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

Claim limitation **[29.c.5]** is substantially similar to **[1.c.5]**, **[2.a.4]**, and **[2.a.5]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.32-35, 62-62.

Claims 1, 2	Claim 29
[1.c.5] wherein the controller is configured to perform, in response to the trigger signal, a write operation ..., and [2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.5] a first write operation to write a first set of data bits into a first portion of the data storage element;	[29.c.5] wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;

[29.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,

Claim limitation **[29.d.1]** is substantially similar to **[1.d.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.36-38.

Claim 1	Claim 29
[1.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,	[29.d.1] a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,

[29.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

Claim limitation **[29.d.2]** is substantially similar to **[1.d.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.38-39.

Claim 1	Claim 29
[1.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and	[29.d.2] the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

[29.e] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

Claim limitation **[29.e]** is substantially similar to **[1.e]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.40-45.

Claim 1	Claim 29
[1.e] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,	[29.e] first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

[29.f.1] wherein the set of components includes:

Claim limitation **[29.f.1]** is substantially similar to **[1.f.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.45-46.

Claim 1	Claim 29
[1.f.1] wherein the set of components includes:	[29.f.1] wherein the set of components includes:

[29.f.2] a first component configured to receive power via the first regulated voltage line;

Claim limitation **[29.f.2]** is substantially similar to **[1.f.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.46-47.

Claim 1	Claim 29
[1.f.2] a first component configured to receive power via at least the first regulated voltage line;	[29.f.2] a first component configured to receive power via the first regulated voltage line;

[29.f.3] a second component configured to receive power via the second regulated voltage line;

Claim limitation **[29.f.3]** is substantially similar to **[1.f.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.47-48.

Claim 1	Claim 29
[1.f.3] a second component configured to receive power via at least the second regulated voltage line;	[29.f.3] a second component configured to receive power via the second regulated voltage line;

[29.f.4] a third component configured to receive power via the third regulated voltage line; and

Claim limitation [29.f.4] is substantially similar to [1.f.4] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.48-48.

Claim 1	Claim 29
[1.f.4] a third component configured to receive power via at least the third regulated voltage line; and	[29.f.4] a third component configured to receive power via the third regulated voltage line; and

[29.f.5] a fourth component configured to receive power via the fourth regulated voltage line;

Claim limitation [29.f.5] is substantially similar to [1.f.5] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 29
[1.f.5] a fourth component configured to receive power via at least the fourth regulated voltage line;	[29.f.5] a fourth component configured to receive power via the fourth regulated voltage line;

[29.g.1] wherein each component of the set of components:

Claim limitation [29.g.1] is substantially similar to [1.g.1] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 29
[1.g.1] wherein each component of the set of components:	[29.g.1] wherein each component of the set of components:

[29.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

Claim limitation **[29.g.2]** is substantially similar to **[1.g.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.49-49.

Claim 1	Claim 29
[1.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and	[29.g.2] (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

[29.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

Claim limitation **[29.g.3]** is substantially similar to **[1.g.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.50-51.

Claim 1	Claim 29
[1.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,	[29.g.3] (ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;

[29.h.1] wherein the plurality of DDR SDRAM devices includes:

Claim limitation **[29.h.1]** is substantially similar to **[1.h.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.51-51.

Claim 1	Claim 29
[1.h.1] wherein the plurality of DDR SDRAM devices includes:	[29.h.1] wherein the plurality of DDR SDRAM devices includes:

[29.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and

Claim limitation **[29.h.2]** is substantially similar to **[1.h.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.51-52.

Claim 1	Claim 29
[1.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;	[29.h.2] a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and

[29.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal, and

Claim limitation **[29.h.3]** is substantially similar to **[1.h.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.52-53.

Claim 1	Claim 29
[1.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;	[29.h.3] a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal, and

[29.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

Claim limitation **[29.i.1]** is substantially similar to **[1.i.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.53-55.

Claim 1	Claim 29
[1.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:	[29.i.1] wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

[29.i.2] the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

Claim limitation **[29.i.2]** is substantially similar to **[1.i.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.55-58.

Claim 1	Claim 29
[1.i.2] the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;	[29.i.2] the first group of DDR SDRAM devices ^[3] is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices ^[4] is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and

[29.i.3] the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

Claim limitation **[29.i.3]** is substantially similar to **[1.i.3]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.58-58.

³ “[T]he first group of **DDR SDRAM devices**” has no antecedent basis. This term should have been “the first group of **at least five DDR SDRAM devices**” as recited in [29.h.2].

⁴ “[T]he second group of **DDR SDRAM devices**” has no antecedent basis. This term should have been “the second group of **at least four DDR SDRAM devices**” as recited in [29.h.3].

Claim 1	Claim 29
[1.i.3] the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and	[29.i.3] the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and

[29.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and

Claim limitation **[29.j.1]** is substantially similar to **[1.j.1]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.59-59.

Claim 1	Claim 29
[1.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and	[29.j.1] wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and

[29.j.2] the total number of data conduits is at least 72 data conduits.

Claim limitation **[29.j.2]** is substantially similar to **[1.j.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.59-59.

Claim 1	Claim 29
[1.j.2] the total number of data conduits is at least 72 data conduits.	[29.j.2] the total number of data conduits is at least 72 data conduits.

Claim 30

[30] The DIMM of claim 29, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

Claim limitation [30] is substantially similar to [14] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.75-75.

Claim 14	Claim 30
[14] The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.	[30] The DIMM of claim 29, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory ^[5] is not powered using the first regulated voltage.

Claim 31

[31] The DIMM of claim 29, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.

Claim limitation [31] is substantially similar to [14] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.75-75.

⁵ “[T]he nonvolatile memory” lacks antecedent basis.

Claim 14	Claim 31
[14] The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.	[31] The DIMM of claim 29, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory ^[6] is not powered using the first regulated voltage.

Claim 32

[32] The DIMM of claim 29, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

Claim limitation [32] is substantially similar to [11] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.69-69.

Claim 11	Claim 32
[11] The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.	[32] The DIMM of claim 29, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

⁶ “[T]he nonvolatile memory” lacks antecedent basis.

Claim 33

[33] The DIMM of claim 32, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

Claim limitation [33] is substantially similar to [1.c.6] and [11] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.35-36, 69-69.

Claims 1, 11	Claim 33
[1.c.6] wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage; [11] The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage ...	[33] The DIMM of claim 32, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.

Claim 34

[34.a] The DIMM of claim 32, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

Claim limitation [34.a] is substantially similar to [13.a.1] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.71-73.

Claim 13	Claim 34
[13.a.1] The DIMM of claim 12, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and	[34.a] The DIMM of claim 32, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and

[34.b] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

Claim limitation **[34.b]** is substantially similar to **[13.a.2]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.73-74.

Claim 13	Claim 34
[13.a.2] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.	[34.b] wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.

Claim 35

[35.a.1] The DIMM of claim 29, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and

Claim limitation **[35.a.1]** is substantially similar to **[1.c.1]** and **[2.a.1]-[2.a.3]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.25-29, 59-62.

Claim 2	Claim 35
[1.c.1] a controller including a ... nonvolatile memory ... [2.a.1] The DIMM of claim 1, wherein the controller further includes: [2.a.2] a data storage element configured to store a plurality of data bits and [2.a.3] a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and	[35.a.1] The DIMM of claim 29, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and

[35.a.2] the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.

Claim limitation **[35.a.2]** is substantially similar to **[2.a.4]**, **[2.a.5]**, and **[2.a.6]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.62-63.

Claim 2	Claim 35
[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.5] a first write operation to write a first set of data bits into a first portion of the data storage element; [2.a.6] a second write operation to write a second set of data bits into a second portion of the data storage element ...	[35.a.2] the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to write a second set of data bits into a second portion of the data storage element.

Claim 36

[36.a.1] The DIMM of claim 35, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and

Claim limitation **[36.a.1]** is substantially similar to **[2.a.4]**, **[2.a.6]**, and **[2.a.7]** as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.62-62, 62-63.

Claim 2	Claim 36
[2.a.4] wherein the write operation conducted by the controller in response to the trigger signal includes: [2.a.6] ... and subsequently [2.a.7] a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,	[36.a.1] The DIMM of claim 35, wherein the logic element [included in the controller of claim 35] is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and

[36.a.2] wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

Claim limitation **[36.a.2]** is substantially similar to **[2.a.8]** as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.63-63.

Claim 2	Claim 36
[2.a.8] wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.	[36.a.2] wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

Claim 37

[37] The DIMM of claim 35, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

Claim limitation [37] is substantially similar to [7] and [8] as shown by the comparison below, and thus obvious for the reasons already given for those limitations. *Supra*, pp.66-68.

Claims 7, 8	Claim 37
[7] The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations. [8] The DIMM of claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.	[37] The DIMM of claim 35, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.

Claim 38

[38] The DIMM of claim 29, wherein each of the first, second, and third converter circuits is a buck converter.

Claim limitation [38] is substantially similar to [15] as shown by the comparison below, and thus obvious for the reasons already given for the limitation. *Supra*, pp.75-76.

Claims 15	Claim 38
[15] The DIMM of claim 1, wherein each of the first, second, and third converter circuits is a buck converter, ...	[38] The DIMM of claim 29, wherein each of the first, second, and third converter circuits is a buck converter.