

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Case IPR2026-00018

Patent 12,373,366

**PETITION FOR INTER PARTES REVIEW OF
U.S. PATENT NO. 12,373,366**

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1002	File History of U.S. Patent No. 12,373,366 (Application No. 17/582,797), <i>available at</i> < https://patentcenter.uspto.gov/applications/17582797/ifw/docs?application= >
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
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1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	File History of U.S. Patent Application No. 17/138,766
1014	<i>SanDisk Corp. v. Netlist, Inc.</i> , IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
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1016	<i>Smart Modular Techs. Inc. v. Netlist, Inc.</i> , IPR2014-01370, Paper No. 8 (PTAB September 22, 2014) (833 Patent IPR Corrected Petition)

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1018	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00649, Paper No. 1 (PTAB January 13, 2017) (833 Patent IPR Petition)
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1023	U.S. Patent Application Publication No. 2006/0174140 to Harris <i>et al.</i>
1024	U.S. Patent No. 7,724,604 to Amidi <i>et al.</i>
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers <i>et al.</i>
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) (“JESD79-2B”)
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (“JESD82-20”)
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1029	Declaration of Julie Carlson for JESD82-20 and JESD205
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1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d Ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete <i>et al.</i>
1034	U.S. Patent No. 6,798,709 to Sim <i>et al.</i>
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1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
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1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi <i>et al.</i>
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
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1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	U.S. Patent Application Publication No. 2003/0090879 to Doblar <i>et al.</i>
1052	File History of U.S. Patent No. 11,232,054 (EX1002 in IPR2022-00999)
1053	U.S. Patent No. 11,232,054 (EX1001 in IPR2022-00999)
1054	U.S. Patent No. 11,016,918
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
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1066	U.S. Patent No. 10,672,458 to Shaeffer <i>et al.</i>
1067	LatticeXP Family Data Sheet (March 2006)
1068	Declaration of Dr. Andrew Wolfe in IPR2022-00996 (EX1003 in IPR2022-00996)
1069	Declaration of Dr. Andrew Wolfe in IPR2022-00999 (EX1003 in IPR2022-00999)
1070	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00996, Paper 49 (PTAB Dec. 6, 2023) (U.S. Patent No. 11,016,918)
1071	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2022-00999, Paper 51 (PTAB Dec. 5, 2023) (U.S. Patent No. 11,232,054)
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1073	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-1859 (Fed. Cir. May 23, 2024) (appeal from IPR2022-00996 of U.S. Patent No. 11,016,918)
1074	Notice of Docketing, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd.</i> , No. 2024-1863 (Fed. Cir. May 23, 2024) (appeal from IPR2022-00999 of U.S. Patent No. 11,232,054)
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1080	Romo, Joaquin, <i>DDR Memories: Comparison and overview</i>, NXP technical note, downloaded from https://www.nxp.com/docs/en/supporting-information/BeyondBits2article17.pdf (last access 09/08/2022). As downloaded the file shows the following meta data: Created: 6/8/2007 9:56:44 AM Modified: 8/2/2007 2:56:29 PM (EX2012 in IPR2022-00996 and IPR2022-00999)
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1084	Netlist Presentation (excerpt) (EX2035 in IPR2022-00996 and IPR2022-00999)
1085	Intel, ATX12V, Power Supply Design Guide, Version 2.2 (March 2005), downloaded from https://web.archive.org/web/20070403181612/http://www.formfactors.org/developer/specs/ATX12V_PSDG_2_2_public_br2.pdf (EX2038 in IPR2022-00996 and IPR2022-00999)

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1087	Wolfe Deposition exhibit, FB-DIMM Design Considerations (Feb. 18, 2004) (EX2101 in IPR2022-00996 and IPR2022-00999)
1088	Final Written Decision, <i>Micron Technology, Inc. et al. v. Netlist, Inc.</i> , IPR2022-00418, Paper 30 (PTAB Aug. 28, 2023) (U.S. Patent No. 8,301,833)
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1091	Final Written Decision, <i>Samsung Electronics Co., Ltd. v. Netlist, Inc.</i> , IPR2023-00455, Paper 45 (PTAB July 30, 2024) (U.S. Patent No. 9,858,215)
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1096	Netlist's Responsive Brief, <i>Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.</i> , No. 2024-2203 (Fed. Cir. Mar. 28, 2025)

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1106	JEDEC JESD21-C design specification for DDR2 SDRAM Registered DIMM, Rev. 3.2 (Oct. 4, 2005), <i>available at</i> http://web.archive.org/web/20060912004633/http://www.jedec.org:80/Catalog/display.cfm , http://web.archive.org/web/20061002003035/http://www.jedec.org/download/search/4_20_10R15.pdf , http://web.archive.org/web/20061002003035if_/http://www.jedec.org/download/search/4_20_10R15.pdf
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1110	Microchip 25LC256 EEPROM datasheet (2003), <i>available at</i> https://web.archive.org/web/20041130175640/http://www.microchip.com/stellent/idcplg?IdcService=SS_GET_PAGE&nodeId=1335&dDocName=en010846 >, https://web.archive.org/web/20040805021246/http://ww1.microchip.com/downloads/en/DeviceDoc/21822c.pdf >, https://web.archive.org/web/20040805021246if_/http://ww1.microchip.com:80/downloads/en/DeviceDoc/21822c.pdf >
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1112	Complaint, <i>In the Matter of Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof</i> , Inv. No. 337-TA-3854 (USITC filed Sept. 30, 2025) (U.S. Patent No. 12,373,366)
1113	Invalidity claim chart by Dr. Andrew Wolfe

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
1.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
1.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
1.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:
1.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:
1.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits,
1.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;
1.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits, and
1.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
1.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,
1.b.7	a set of data lines electrically connected to the second set of edge connections, and
1.b.8	a set of address and control lines electrically connected to the third set of edge connections;
1.c.1	a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
1.c.2	(i) monitor an input voltage supplied via the input voltage supply line;

Ref. #	Listing of Challenged Claims
1.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
1.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
1.c.5	wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and
1.c.6	wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;
1.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
1.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
1.e	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
1.f.1	wherein the set of components includes:
1.f.2	a first component configured to receive power via at least the first regulated voltage line;
1.f.3	a second component configured to receive power via at least the second regulated voltage line;
1.f.4	a third component configured to receive power via at least the third regulated voltage line; and
1.f.5	a fourth component configured to receive power via at least the fourth regulated voltage line;
1.g.1	wherein each component of the set of components:
1.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
1.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,
1.h.1	wherein the plurality of DDR SDRAM devices includes:

Ref. #	Listing of Challenged Claims
1.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
1.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;
1.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
1.i.2	the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;
1.i.3	the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and
1.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and
1.j.2	the total number of data conduits is at least 72 data conduits.
2.a.1	The DIMM of claim 1, wherein the controller further includes:
2.a.2	a data storage element configured to store a plurality of data bits and
2.a.3	a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and
2.a.4	wherein the write operation conducted by the controller in response to the trigger signal includes:
2.a.5	a first write operation to write a first set of data bits into a first portion of the data storage element;
2.a.6	a second write operation to write a second set of data bits into a second portion of the data storage element; and subsequently

Ref. #	Listing of Challenged Claims
2.a.7	a third write operation to write a third set of data bits from the data storage element into the nonvolatile memory,
2.a.8	wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.
3	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on a combination of the first and second sets of data bits written during the first and second write operations.
4	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on groups of data bits stored in the data storage element including the first and second sets of data bits written during the first and second write operations.
5	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a plurality of read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
6	The DIMM of claim 2, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger signal, a read operation to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
7	The DIMM of claim 2, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger signal, one or more read operations.
8	The DIMM of claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
9.a.1	The DIMM of claim 2, wherein the third write operation comprises a transfer of the third set of data bits from the data storage element to the nonvolatile memory via a first connection, and

Ref. #	Listing of Challenged Claims
9.a.2	wherein the first and second write operations comprise a transfer of the first and second sets of data bits into the data storage element via a second connection.
10	The DIMM of claim 2, wherein the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits.
11	The DIMM of claim 1, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including the first threshold voltage and a second threshold voltage.
12	The DIMM of claim 1, wherein the second component is further connected to the first regulated voltage line and is powered by the first and second regulated voltages when power from the power rails of the system board is provided to the DIMM.
13.a.1	The DIMM of claim 12, wherein, when power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
13.a.2	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
14	The DIMM of claim 1, wherein, when power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is not powered using the first regulated voltage.
15	The DIMM of claim 1, wherein each of the first, second, and third converter circuits is a buck converter, and the fourth converter circuit is a voltage reducing circuit.
16.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
16.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
16.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
16.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

Ref. #	Listing of Challenged Claims
16.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:
16.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver the DIMM power from the power rails of the system board via the set of power conduits,
16.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,
16.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits,
16.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
16.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,
16.b.7	a set of data lines electrically connected to the second set of edge connections, and
16.b.8	a set of address and control lines electrically connected to the third set of edge connections;
16.c.1	a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
16.c.2	(i) monitor an input voltage supplied via the input voltage supply line;
16.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
16.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
16.c.5	wherein, in response to the detected trigger condition, the controller is configured to periodically perform, at regular intervals of time, a plurality of write operations, including a first write operation to write a first set of data bits into a first portion of the data storage element;

Ref. #	Listing of Challenged Claims
16.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
16.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
16.e	first, second, third, and fourth converters coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
16.f.1	wherein the set of components includes:
16.f.2	a first component configured to receive power via the first regulated voltage line;
16.f.3	a second component configured to receive power via the second regulated voltage line;
16.f.4	a third component configured to receive power via the third regulated voltage line; and
16.f.5	a fourth component configured to receive power via the fourth regulated voltage line;
16.g.1	wherein each component of the set of components:
16.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines;
16.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines, and
16.h.1	wherein the plurality of DDR SDRAM devices includes:
16.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;
16.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

Ref. #	Listing of Challenged Claims
16.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
16.i.2	the first group of DDR SDRAM packages is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM packages is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and
16.i.3	the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and
16.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and
16.j.2	the total number of data conduits is at least 72 data conduits.
17	The DIMM of claim 16, wherein the controller further includes a nonvolatile memory and a logic element, the logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element.
18	The DIMM of claim 17, wherein the logic element is configured to perform a second write operation to write a second set of data bits into a second portion of the data storage element.
19.a.1	The DIMM of claim 18, wherein the plurality of write operations further includes a third write operation subsequent to the first and second write operations to write a third set of data bits from the data storage element into the nonvolatile memory,
19.a.2	wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations, and
19.a.3	wherein, in response to the detected trigger condition, the logic element is configured to periodically perform every millisecond all of the first and second write operations followed by the third write operation.

Ref. #	Listing of Challenged Claims
20	The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, and to generate the third set of data bits based on the read first and second sets of data bits.
21.a.1	The DIMM of claim 19, wherein the logic element is configured to perform the third write operation by writing the third set of data bits from the data storage element into the nonvolatile memory, and
21.a.2	wherein the third set of data bits includes the first and second sets of data bits written during the first and second write operations.
22	The DIMM of claim 19, wherein, prior to performing the third write operation, the logic element is configured to generate the third set of data bits based on the groups of data bits stored in the data storage element.
23.a.1	The DIMM of claim 19, wherein the third write operation comprises a transfer of the first and second set of data bits from the data storage element to the nonvolatile memory via a first connection, and
23.a.2	wherein the first and second write operations comprise a transfer of the first and second set of data bits into the data storage element via a second connection.
24	The DIMM of claim 18, wherein, prior to performing the first and second write operations, the logic element is configured to perform, in response to the detected trigger condition, periodically at regular intervals of time one or more read operations to read the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
25	The DIMM of claim 16, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
26	The DIMM of claim 16, wherein when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.

Ref. #	Listing of Challenged Claims
27	The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.
28.a	The DIMM of claim 26, wherein when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
28.b	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
29.a.1	A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system,
29.a.2	the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits,
29.a.3	wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and
29.a.4	address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:
29.b.1	a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector, the PCB including:
29.b.2	a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from the power rails of the system board via the set of power conduits,
29.b.3	wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM,
29.b.4	a second set of edge connections configured to be electrically connected to the set of data conduits,
29.b.5	a third set of edge connections configured to be electrically connected to the set of address and control conduits,
29.b.6	a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

Ref. #	Listing of Challenged Claims
29.b.7	a set of data lines electrically connected to the second set of edge connections, and
29.b.8	a set of address and control lines electrically connected to the third set of edge connections,
29.b.9	wherein the set of data lines are electrically coupled to respective edge connections of the second set of edge connection,
29.b.10	wherein each data line of the set of data lines is configured to electrically conduct a 1-bit DDR data signal;
29.c.1	a controller including a voltage monitor circuit and a data storage element configured to store a plurality of data bits, the controller coupled to the PCB and an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to:
29.c.2	(i) monitor an input voltage supplied via the input voltage supply line;
29.c.3	(ii) generate a trigger signal upon detecting a trigger condition; and
29.c.4	(iii) transmit the trigger signal to at least one other portion of the controller,
29.c.5	wherein the controller is configured to perform, in response to the trigger signal, one or more write operations to write data into the data storage element;
29.d.1	a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines,
29.d.2	the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and
29.e	first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,
29.f.1	wherein the set of components includes:
29.f.2	a first component configured to receive power via the first regulated voltage line;
29.f.3	a second component configured to receive power via the second regulated voltage line;

Ref. #	Listing of Challenged Claims
29.f.4	a third component configured to receive power via the third regulated voltage line; and
29.f.5	a fourth component configured to receive power via the fourth regulated voltage line;
29.g.1	wherein each component of the set of components:
29.g.2	(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and
29.g.3	(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines;
29.h.1	wherein the plurality of DDR SDRAM devices includes:
29.h.2	a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal; and
29.h.3	a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal, and
29.i.1	wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:
29.i.2	the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines; and
29.i.3	the at least 40 1-bit DDR data signals include 32 1-bit DDR data signals and eight 1-bit DDR error-correcting code (ECC) data signals; and
29.j.1	wherein the sum of the at least 40 data lines and the integer number of data lines matches a total number of data conduits of the set of data conduits of the memory slot connector, and
29.j.2	the total number of data conduits is at least 72 data conduits.

Ref. #	Listing of Challenged Claims
30	The DIMM of claim 29, wherein, when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
31	The DIMM of claim 29, wherein when power is provided to the DIMM from the power rails of the system board, the nonvolatile memory is not powered using the first regulated voltage.
32	The DIMM of claim 29, when power is provided to the DIMM from the power rails of the system board the voltage monitor circuit compares the input voltage to a plurality of threshold voltages including a first threshold voltage and a second threshold voltage.
33	The DIMM of claim 32, wherein when power is provided to the DIMM from the power rails of the system board the trigger condition occurs when the input voltage goes above a specified operating voltage.
34.a	The DIMM of claim 32, wherein, when power is provided to the DIMM from the power rails of the system board, an additional trigger condition occurs when the input voltage is above the first threshold and below the second threshold; and
34.b	wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal.
35.a.1	The DIMM of claim 29, wherein the controller further includes a logic element coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element, and
35.a.2	the one or more write operations include a first write operation to write a first set of data bits into a first portion of the data storage element and a second write operation to wire a second set of data bits into a second portion of the data storage element.
36.a.1	The DIMM of claim 35, wherein the logic element is configured to perform a third write operation subsequent to the first and second write operations by writing a third set of data bits from the data storage element into the nonvolatile memory, and
36.a.2	wherein the third set of data bits includes the first and second set of data bits written during the first and second write operations.

Ref. #	Listing of Challenged Claims
37	The DIMM of claim 35, wherein the logic element is configured to perform, prior to the first and second write operations, first and second read operations by reading the first and second sets of data bits from the first and second groups of DDR SDRAM devices, respectively.
38	The DIMM of claim 29, wherein each of the first, second, and third converter circuits is a buck converter.

I. PETITIONER’S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 12,373,366.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, PGR2026-00001 (U.S. Patent No. 12,373,366)
- *In the Matter of Certain Dynamic Random Access Memory (DRAM) Devices, Products Containing the Same, and Components Thereof*, Inv. No. 337-TA-3854 (USITC filed Sept. 30, 2025) (U.S. Patent No. 12,373,366)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00996, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-00406, *appeal docketed*, No. 2024-1859 (Fed. Cir. May 23, 2024) (U.S. Patent No. 11,016,918)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00999, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-00405, *appeal*

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docketed, No. 2024-1863 (Fed. Cir. May 23, 2024) (U.S. Patent No. 11,232,054)

- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex.), *appeal docketed*, No. 2024-2203 (Fed. Cir. Aug. 13, 2024) (U.S. Patent Nos. 11,016,918 and 11,232,054)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:22-cv-00203 (E.D. Tex. filed June 10, 2022) (U.S. Patent Nos. 11,016,918 and 11,232,054)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00454, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-01141, *appeal docketed*, No. 2025-1296 (Fed. Cir. Dec. 17, 2024) (U.S. Patent No. 11,093,417)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2023-00455, and *Micron Tech., Inc. et al. v Netlist, Inc.*, IPR2023-01142, *appeal docketed*, No. 2025-1286 (Fed. Cir. Dec. 16, 2024) (U.S. Patent No. 9,858,215)
- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:25-cv-00626 (D. Del. filed May 20, 2025) (U.S. Patent No. 12,373,366)
- *Micron Technology, Inc. et al. v. Netlist, Inc.*, No. 1:25-cv-00942 (D. Del. Filed July 29, 2025) (U.S. Patent No. 12,373,366)

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- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:25-cv-00748 (E.D. Tex. July 28, 2025) (U.S. Patent No. 12,373,366)
- *Netlist, Inc. v. Micron Technology, Inc. et al.*, No. 2:25-cv-00749 (E.D. Tex. July 28, 2025) (U.S. Patent No. 12,373,366)
- Application No. 19/261,245

The following proceedings are no longer pending:

- *Micron Technology, Inc. et al. v. Netlist, Inc.*, IPR2022-00418 (U.S. Patent No. 8,301,833)
- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00692 (U.S. Patent No. 8,874,831)

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is: Eliot D. Williams (Reg. No. 50,822),

DLSamsungNetlistIPRs@BakerBotts.com, (202) 639-1334, Baker Botts L.L.P.,
700 K Street, N.W., Washington, D.C. 20001.

Back-up Counsel are:

- Theodore W. Chandler (Reg. No. 50,319),
DLSamsungNetlistIPRs@BakerBotts.com, (213) 202-5702
- Ferenc Pazmandi (Reg. No. 66,216),
DLSamsungNetlistIPRs@BakerBotts.com, (415) 291-6255

- Mark A. Speegle (Reg. No. 77,512),

DLSamsungNetlistIPRs@BakerBotts.com, (512) 322-2536

The fax number for lead and backup counsel is (202) 639-7890.

D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above.

Petitioner consents to service of all documents via electronic mail to

DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-38 of U.S. Patent No. 12,373,366 (“’366 Patent”) (EX1001).

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

If PGR2025-00001 is not instituted, then the ’366 Patent is available for IPR and Petitioner is not barred or estopped from requesting IPR on the below-identified grounds.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-38 of the ’366 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	Omitted in this IPR. See Paper No. 3 (ranking petitions).		
2	1-38	103(a)	<u>Perego</u> + <u>Harris</u> + <u>Amidi</u>

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above starting on page vii, and includes an expert declaration by Andrew Wolfe, Ph.D., EX1003.

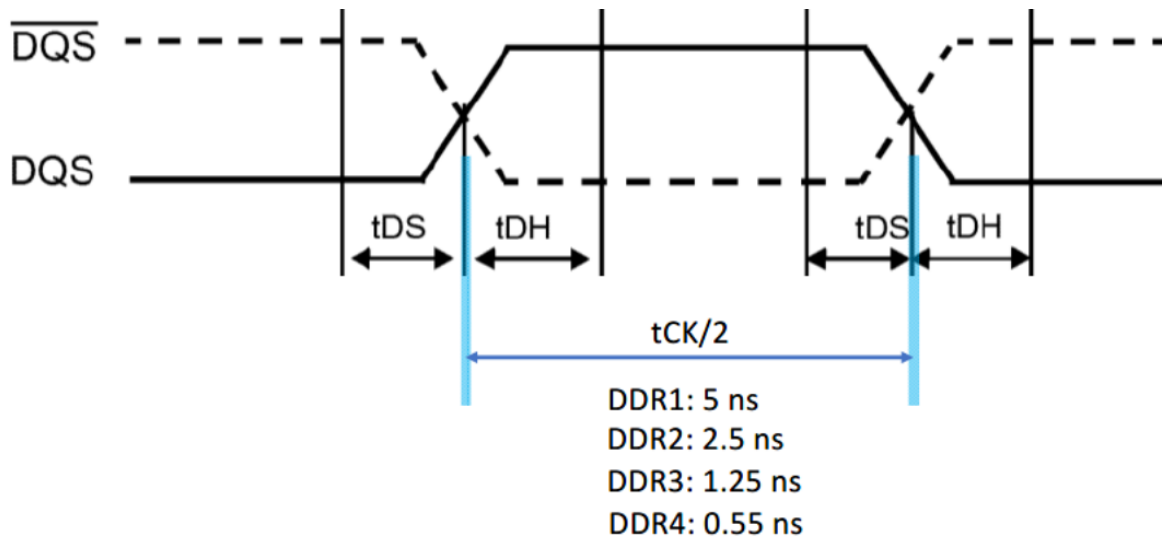
IV. BACKGROUND ON THE '366 PATENT

A. Background Technology

1. JEDEC standards

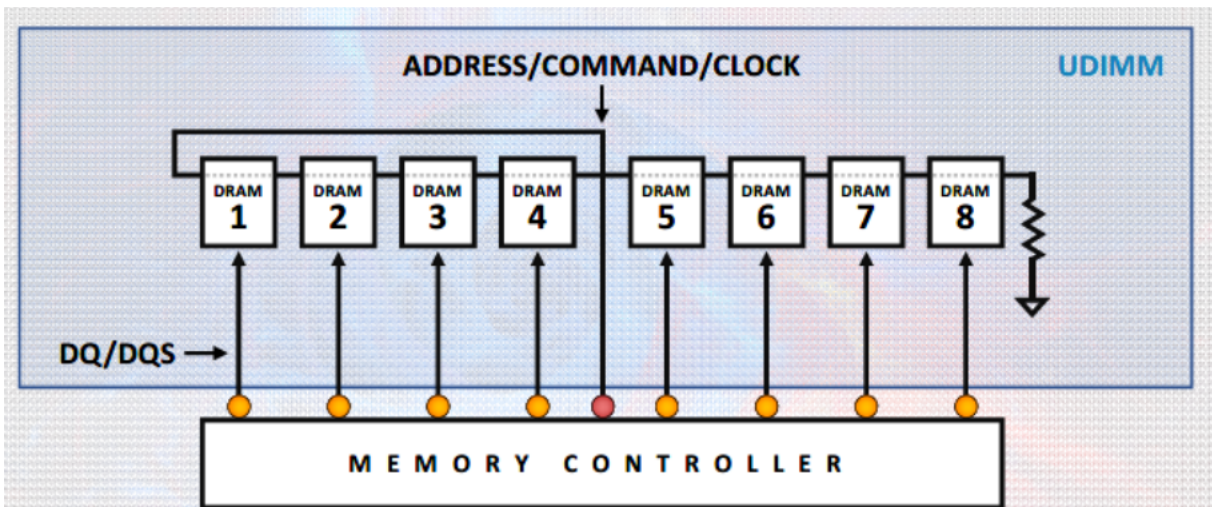
The '366 Patent relates generally to memory devices on a memory module. EX1001, 2:6-9. An industry organization called JEDEC had already standardized various relevant technologies, including the various generations of double data rate (DDR) DRAM memory devices and the different types of memory modules used in servers and workstations. EX1077, 3; EX1105, ¶¶4-5; EX1003, ¶¶55-65. As discussed below (pp.19-20), a POSITA would have been familiar with the JEDEC standards.

The JEDEC standards defined the progression of DRAM memory technology from SDRAM through DDR, DDR2, DDR3, and beyond, with each generation essentially doubling the data transfer rate of its predecessor:

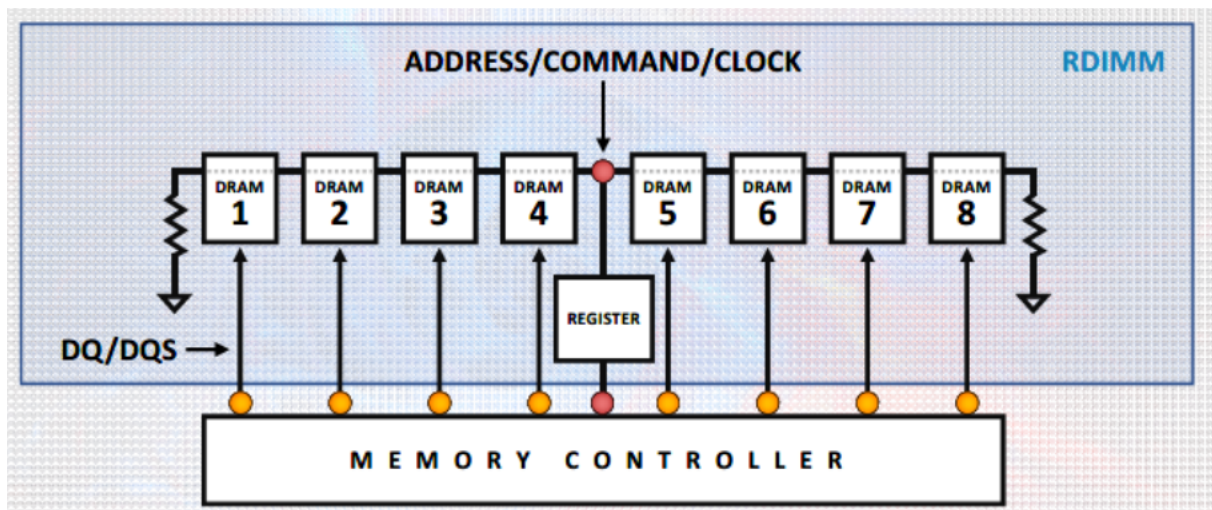


EX1077, 3-6 (showing decrease in nominal clock cycle speed over consecutive DRAM generations); EX1045, 58 (DDR1); EX1026, 66 (DDR2); EX1046, 144-48 (DDR3).

JEDEC also standardized various types of Dual In-Line Memory Modules (DIMMs), including unbuffered DIMMs (UDIMMs), registered DIMMs (RDIMMs), and fully-buffered DIMMs (FBDs or FBDIMMs), illustrated below. EX1077, 2, 7-11; EX1023, ¶[0009]; EX1003, ¶¶55-58. UDIMMs—as pictured below—connect DRAM devices directly to the memory controller (at the bottom).

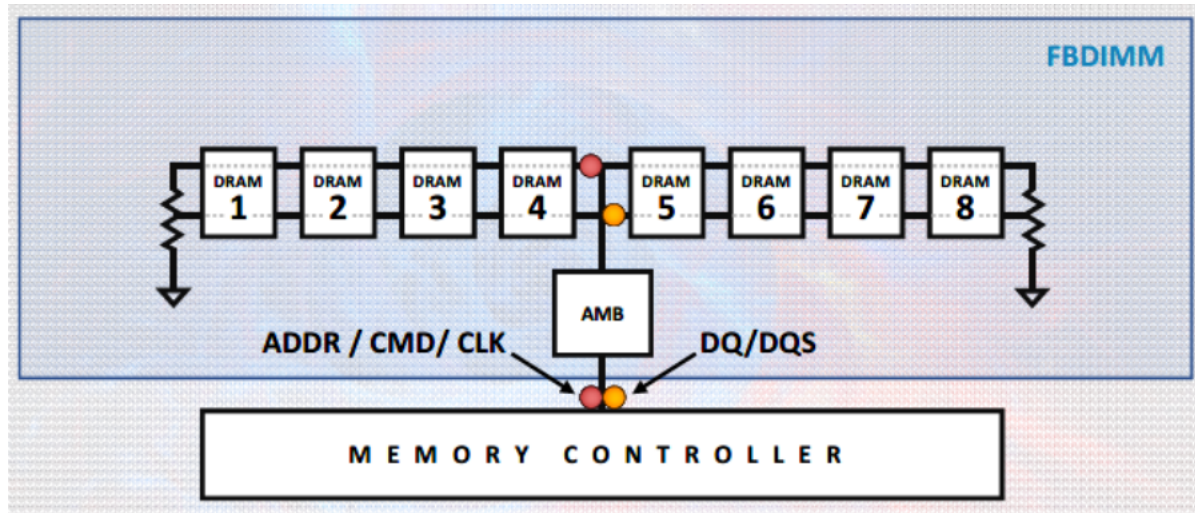


Id. This gives low latency but means the memory controller must drive the full electrical load of all DRAM chips, limiting the number of modules per channel at high speeds. *Id.* RDIMMs (as below) insert a *register* between the DRAM chips and the memory controller for address and control lines (red).



Id. This register buffers these signals, reducing the electrical load on the memory controller and allowing more DIMMs per channel. *Id.* FBDIMMs (below) go

further by replacing the parallel DQ/DQS data lines to the memory module with a high-speed link through an Advanced Memory Buffer (AMB) on each module.



Id. The AMB handles address/control and also re-drives and buffers data signals, completely isolating DRAM loading from the memory controller. This enables very large memory capacities. *Id.*

The JEDEC standards also specified the voltages required for each generation of DDR memory devices, with lower voltages for newer generations:

DDR (JESD79) (EX1045): The original DDR standard in 2000 (now sometimes referred to as DDR1) specified multiple voltages for operating DDR memory devices, including supply voltage “VDD,” I/O supply voltage “VDDQ,” reference voltage “VREF,” and I/O termination voltage “VTT,” as shown below:

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage (for devices with a nominal VDD of 3.3 V)	VDD	3	3.6	V	
Supply Voltage (for devices with a nominal VDD of 2.5 V)	VDD	2.3	2.7	V	
I/O Supply Voltage	VDDQ	2.3	2.7	V	
I/O Reference Voltage	VREF	0.49*VDDQ	0.51*VDDQ	V	6
I/O Termination Voltage (system)	VTT	VREF-0.04	VREF+0.04	V	7

EX1045, 54; EX1003, ¶59.

DDR2 (JESD79-2B) (EX1026): The DDR2 standard in 2005 specified multiple voltages, lower than for DDR1 above, including supply voltage “VDD,” supply voltage “VDDL” for DLL, supply voltage “VDDQ” for output, input reference voltage “VREF,” and termination voltage “VTT,” as shown below:

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.7	1.8	1.9	V	1
VDDL	Supply Voltage for DLL	1.7	1.8	1.9	V	5
VDDQ	Supply Voltage for Output	1.7	1.8	1.9	V	1, 5
VREF	Input Reference Voltage	0.49*VDDQ	0.50*VDDQ	0.51*VDDQ	mV	2, 3
VTT	Termination Voltage	VREF-0.04	VREF	VREF+0.04	V	4

NOTE 1 There is no specific device VDD supply voltage requirement for SSTL-1.8 compliance. However under all conditions VDDQ must be less than or equal to VDD.

NOTE 2 The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 x VDDQ of the transmitting device and VREF is expected to track variations in VDDQ.

NOTE 3 Peak to peak ac noise on VREF may not exceed +/-2% VREF (dc).

NOTE 4 VTT of transmitting device must track VREF of receiving device.

NOTE 5 VDDQ tracks with VDD, VDDL tracks with VDD. AC parameters are measured with VDD, VDDQ and VDDL tied together

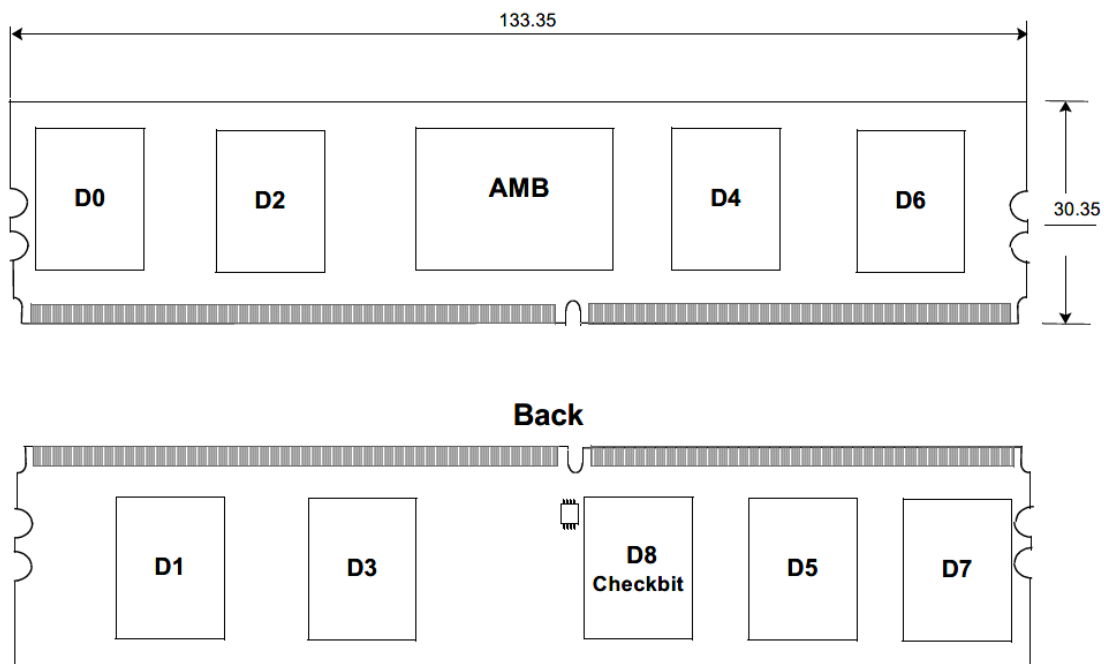
EX1026, 49; EX1003, ¶60.

DDR3 (JESD79-3A) (EX1046): The DDR3 standard in 2007 specified multiple voltages, lower than for DDR2 above, including supply voltages “VDDQ” and “VDD” and reference voltages “VREFDQ” and “VREFCA,” as shown in the table below, as well as termination voltage “VTT”:

V _{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V _{SSQ}	Supply	DQ Ground
V _{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V _{SS}	Supply	Ground
V _{REFDQ}	Supply	Reference voltage for DQ
V _{REFCA}	Supply	Reference voltage

EX1046, 10, 15 (“VTT”); EX1003, ¶¶61.

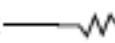
DIMM Standards: JEDEC also standardized many types of memory modules, including RDIMMs with DDR/DDR2 SDRAMs, *see* EX1104; EX1106, and FBDIMMs with DDR2 SDRAMs, *see* EX1027 (JESD82-20); EX1028 (JESD205). EX1003, ¶¶62-63. FBDIMMs include an advanced memory buffer (AMB) on the module to interface with DDR2 memory devices, as discussed above (p.8) and shown below:



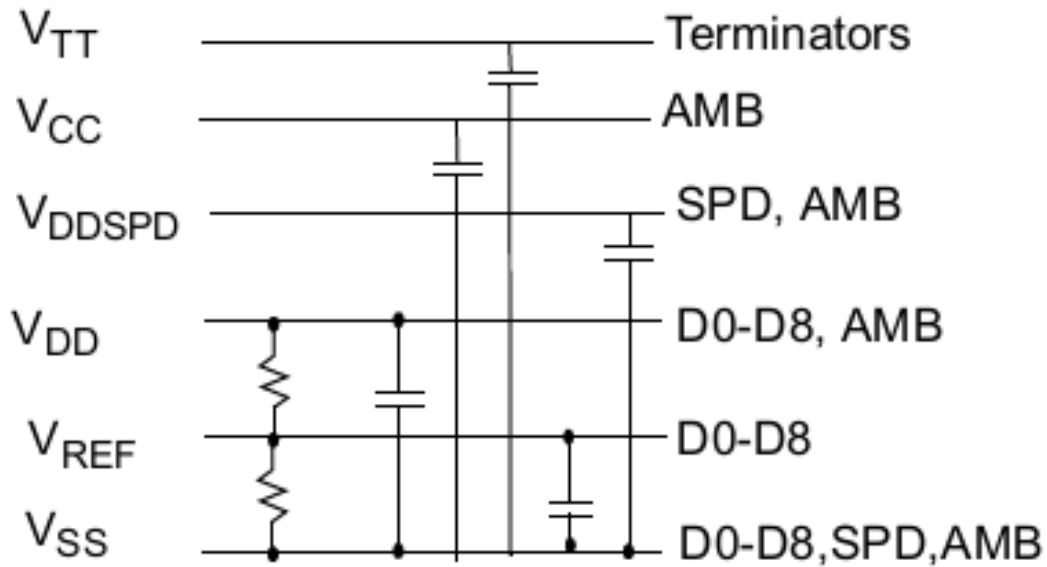
EX1028, 37 (above); *see also id.* 9, 13-16, 38-40; EX1027; EX1003, ¶¶63.

The JEDEC standards for memory modules also specified voltages. For example, an FBDIMM requires supply voltages for the DRAM devices (V_{DD}/V_{DDQ}), the AMB (V_{CC}/V_{CCFBD}), the DRAM interface termination (V_{TT}), and an SPD device (V_{DDSPD}):

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ} , AMB V_{DDQ})
	1.455 ¹	1.5	1.575 ¹	(AMB V_{CC}/V_{CCFBD})
	$0.453 \cdot V_{DD}$	$0.5 \cdot V_{DD}$	$0.547 \cdot V_{DD}$	(DRAM Interface V_{TT}) This supply should track as $0.5 \cdot 1.8$ volt supply
	3.0	3.3	3.6	(V_{DDSPD})

All address/command/control/clock  V_{TT}

EX1028, 9 (table above), 105 (“SPD”), 13 (above in part, showing address/command/clock signal lines of the DRAM interface are terminated at V_{TT} on the FBDIMM); EX1003, ¶64. Furthermore, as shown below, JEDEC specified that the AMB on the FBDIMM uses V_{CC} (for its core), V_{DD} (to interface with the memory devices), and V_{DDSPD} (to interface with the SPD):



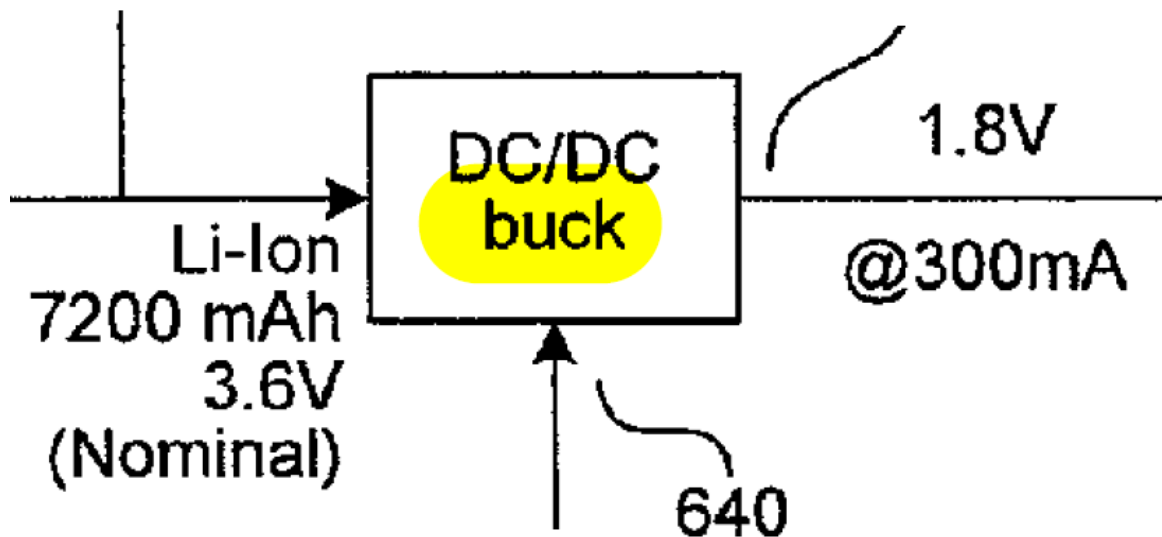
EX1028, 13 (above); EX1003, ¶64.

When a host computer system provides the operating voltages discussed above to a DIMM memory module, the DRAM memory devices on the module can perform normal read/write operations in response to address/command signals received from the host system. *See* EX1077, 5, 7-9; EX1003 ¶65. To increase bandwidth for the normal read/write operations, DIMMs provide a rank operation, where a group of DRAM devices (“rank”) are enabled together by the same chip select (“CS”) signal from the host system to concurrently communicate data signals. *Id.*; EX1026 at 6 (“CS”); EX1106, 9 (“CS”). For example, one rank on a standard DDR2 memory module includes nine x8 memory devices, which are enabled together to concurrently communicate 72 bits (9x8) of data/ECC signals for normal read/write operations. *See, e.g.,* EX1106, 4 (“x72 ECC”), 6 (“S[3:0]”

for “Chip Selects”), 7 (similar), 9 (“x72 DIMM, populated as one physical rank of x8 DDR2 SDRAMs”); EX1003 ¶65.

2. Buck Converters (EX1032, EX1058)

As discussed below (pp.19-20), a POSITA also would have been familiar with “buck converters” — one of “the most basic building blocks in power electronics” — to step down a higher input voltage to a lower output voltage. EX1050, 1:21-23; EX1058, 3 (“buck...also known as a *step-down* converter”), 5, 12-15; EX1032, 161 (“basic converter topologies”), 164; EX1003, ¶¶66-67. An example of a buck converter on a memory module to step down an input voltage is shown below:



EX1024 (Amidi), Fig.6;¹ EX1003, ¶68.

Further, buck converters to generate V_{DDQ} and V_{TT} voltages for DDR memory devices were commercially available at the time. EX1040, 1; EX1041, 1; EX1003, ¶69. Buck converters were more efficient to provide a step-down voltage than non-switching, linear regulators, such as low-dropout regulators (LDO). EX1058, 5; EX1059, 5:23-30 (“buck converters...more efficient than...(LDO)”); EX1075, 112:12-114:8; EX1003, ¶70.

B. The '366 Patent

1. Technical Overview

The '366 Patent claims priority, at least in part, back to applications filed in 2007 and 2008. EX1001; EX1005; EX1006. As shown below, the '366 Patent describes a memory system 1010 that “can be coupled to a host computer system and can include a volatile memory subsystem 1030 [yellow], a non-volatile memory subsystem 1040 [green], and a controller 1062 [red] operatively coupled to the non-volatile memory subsystem 1040,” as well as a “second power supply 1080” (blue) comprising either “capacitors” or a “battery” to supply power during a power failure. EX1001, 21:30-34, 26:22-57, Fig.12 (below).

¹ Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.

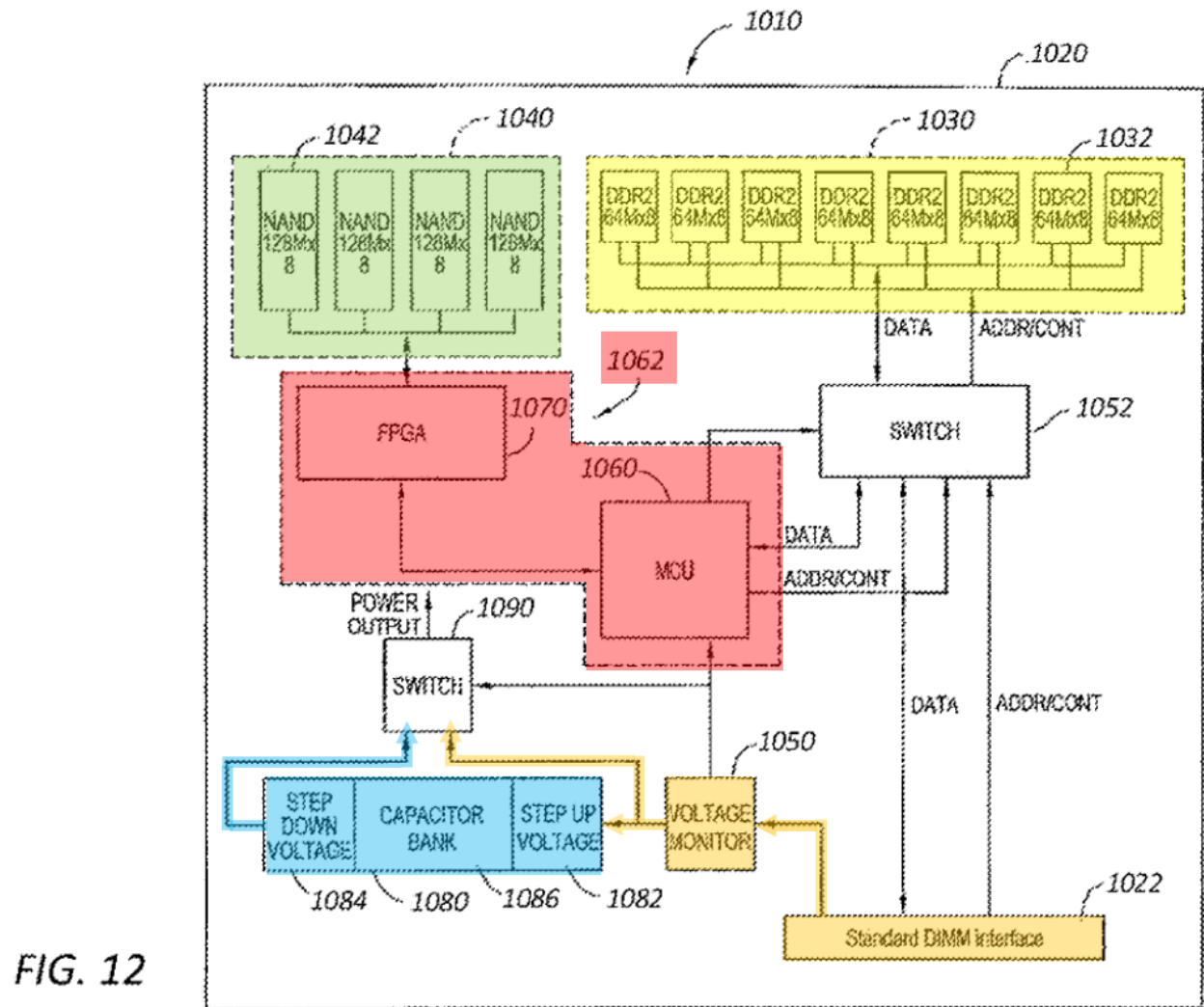


FIG. 12

In the event of a power failure detected by voltage monitor 1050 (orange above), “[t]he controller [red] backs up the volatile memory [yellow] using the non-volatile memory [green].” EX1001, 20:34-37, 25:23-41, 35:38-36:58, Fig.21.

Figure 16 (below) illustrates a power module 1100, which “provides power [e.g., 1102 below, orange] to the various components of the memory system 1010 [e.g., ‘Drams,’ ‘Flash,’ and ‘FPGA’] using different elements based on” the system power (1106) condition. EX1001, 28:6-30:13. For example, when the system

power is available, “the first voltage 1102 [orange] is provided to the memory system 1010 from the [system] input 1106,” and when “power failure has occurred,” “the first voltage 1102 is provided to the memory system 1010 from the conversion element 1120 [blue]” on the power module 1100. *Id.*, 28:40-61.

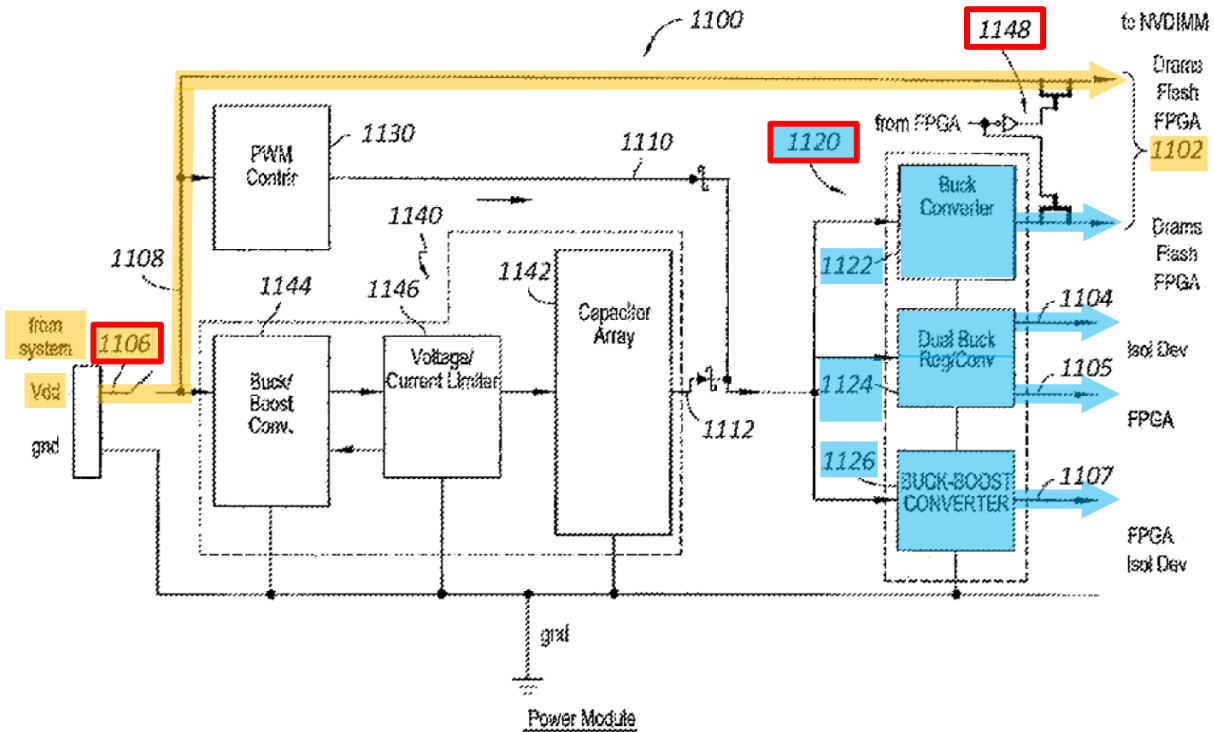


FIG. 16

2. Prosecution History

Before the application for the '366 Patent was filed, the Board invalidated claims in the related '831 and '833 Patents. EX1021; EX1088; EX1089.

During prosecution of the '366 Patent, the Examiner allowed all the claims shortly before the Board invalidated all claims of the '054 and '918 Patents — the parent and grandparent of the '366 Patent — in response to IPRs filed by Petitioner

Petition for *Inter Partes* Review of U.S. Patent No. 12,373,366

supported by the opinions of Dr. Wolfe, the same expert in this proceeding.

EX1002, 479-86; EX1071 (EX1053); EX1070 (EX1054); EX1072; EX1003, ¶¶86-87.

Next, Netlist made various amendments and arguments trying to distinguish the Board's Final Written Decision for the '918 Patent and some of the references cited by the Board (Harris, Amidi, and the FBDIMM Standards). EX1002, 491-503, 510-11, 507, 523, 528-35, 565-71, 645-62, 663-83, 1122-66, 1169-1236.

On January 24, 2025, the Examiner issued a Final Rejection of all pending claims based on lack of written description, and the Examiner also found "not...persuasive" Netlist's attempts to distinguish the references cited by the Board's Final Written Decision for the '918 Patent (Harris, Amidi, and the FBDIMM Standards). *Id.* 1261-74.

In response, Netlist filed another RCE and made more amendments with a chart that purported to show written description support, and then Netlist filed a "Petition to Make Special" based on the age of one of the inventors to rush the application through the examination process. EX1002, 1275-1390, 1393-94, 1398-1496, 1500, 1497, 1503-21. A few weeks later, the Examiner allowed the claims, *id.* 1531-40, but then Netlist made further amendments, *id.* 1544-66, 1570-85, 1589-1606.

On June 18, 2025, the Examiner issued a Notice of Allowance. *Id.* 1606, 1609, 1617-25. The Examiner did not explain why the claims had written description support and did not specifically address prior-art references such as Harris or Amidi. Instead the Examiner reprinted some claim language that purported to make the claims “patentably distinct from the prior art of record.” *Id.* 1623-24. But the language quoted by the Examiner does not actually match the language in the issued claims, and concerns features found in the DDR5 standard dated approximately 10 years *after* the effective filing date of the ’366 Patent. EX1003, ¶¶106, 109.

C. Estoppel from IPRs against related patents

As a result of the Final Written Decisions invalidating claims of the related ’054, ’918, ’831, and ’833 Patents, EX1070-72; EX1021; EX1088, Netlist is “precluded from taking action inconsistent with [those] adverse judgment[s],” 37 C.F.R. §42.73(d)(3), including, but not limited to, “obtaining . . . [a] claim that is not patentably distinct from a finally refused or canceled claim,” *id.* §42.73(d)(3)(i); *SoftView LLC v. Apple Inc.*, 108 F.4th 1366, 1373 (Fed. Cir. 2024) (“[S]ection 42.73(d)(3) . . . ensur[es] the integrity of the proceedings before the PTO by preventing actions that would undermine the outcomes of those proceedings.”). Netlist is also “bound...by any subsidiary factual determinations that were actually litigated and essential to the judgment[s]” in those prior

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proceedings. *Mobile Tech, Inc. v. InVue Security Prods. Inc.*, IPR2018-00481, Paper 29, at 18 (PTAB July 16, 2019); *see also B & B Hardware, Inc. v. Hargis Indus., Inc.*, 575 U.S. 138, 148 (2015) (following the Restatement); Restatement (Second) of Judgments §§13, 27.

D. Person of Ordinary Skill in the Art (“POSITA”)

Petitioner proposes the following definition of a POSITA, which is consistent with the definition adopted by the Board for the related ’054 and ’918 Patents, “with the exception of the open-ended language ‘at least.’” EX1071, 11-12; EX1070, 11-13; EX1003, ¶72. Petitioner does not object to omitting “at least” from the following definition.

A POSITA in the field of the ’366 Patent in 2007 and 2008 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory systems, or a bachelor’s degree in such engineering disciplines and at least three years working in the field. EX1003, ¶71. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses

and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry. *Id.*

V. CLAIM CONSTRUCTION

Petitioner contends that no express claim constructions are needed for this proceeding because the claims are invalid regardless of their precise construction. *See* 37 C.F.R. §42.100(b); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); EX1003, ¶¶112-114. Petitioner's Grounds below are consistent with the construction for “*memory module*” in the preamble of the related '918 and '054 Patents adopted by the district court, *see* EX1083, 35 (“Limiting”), and by the Board, *see* EX1070, 17 (“‘memory module’ is not limited to ‘*main* memory modules...designed to connect to the *primary* memory controller’....[and] includes structure to connect with a ‘host system’ including its memory controller”), EX1071, 16-17 (similar). *See* EX1003, ¶¶113-114. For other terms in the '918 and '054 Patents, they were either construed to

have their “[p]lain and ordinary meaning,” or are terms that do not appear in the claims of the ’366 Patent, and thus Petitioner’s Grounds below are consistent with those constructions. *See id.* (citing EX1083, 34-35; EX1070, 18).

VI. ARGUMENT

A. Ground 2 (all claims are obvious)

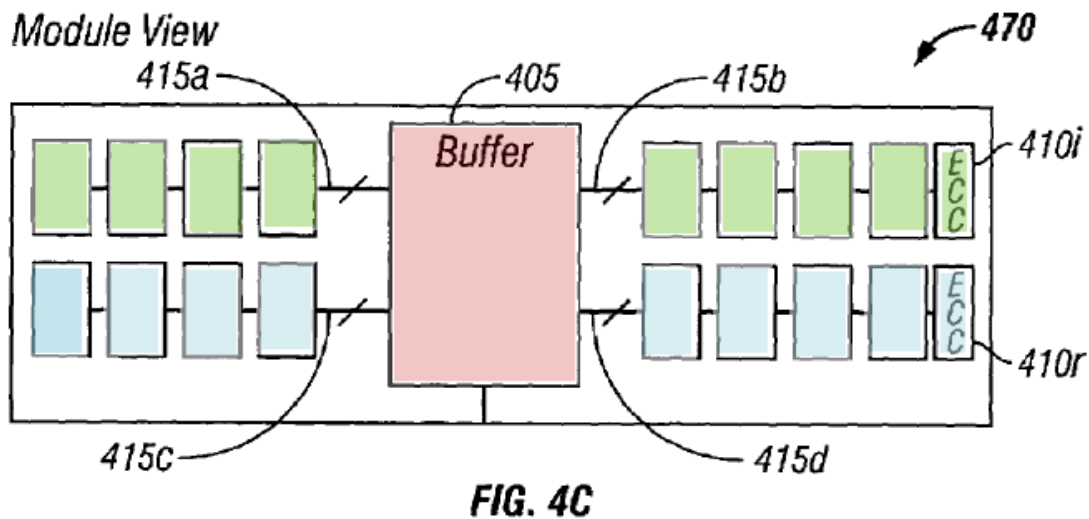
All claims are also obvious in light of Ground 2, as explained below.

1. Ground 2 references

a) Perego (EX1035)

“Perego” (EX1035) is a patent that is prior art under §102(a), (b), and (e) (pre-AIA) because it was filed and published more than one year before the earliest claimed priority date of the ’366 Patent (June 1, 2007), and alternatively is prior art under §102(a)(1) and (a)(2) (post-AIA). Perego was not cited or discussed during prosecution of the ’366 Patent, *see* EX1002, and as explained in the limitation-by-limitation analysis below, Perego discloses features similar to those found in the DDR5 standard that the Examiner erroneously believed distinguished the claims of the ’366 Patent from the prior art, as discussed above (pp.16-18).

Similar to the DDR5 standard discussed above (p.18), Perego discloses a memory module (below) where “two channels 415c and 415d” may “transfer information simultaneously,” such as 32 bits from the 4 memory devices in channel 415c, and 40 bits from the 5 memory devices (including ECC) in channel 415d:



EX1035, 21:16-20, Fig.4C; *see also id.* 10:54-59 (disclosing DDR memory devices, which can be 8-bits wide, *see* EX1026, 2 (“x8”)); EX1090, 28-32 (finding Perego compatible with JEDEC standards); EX1091, 32-37 (same).

The buffer device (red above and below) “provides a high degree of system flexibility,” EX1035, 6:34-43, by incorporating programmable interfaces 520a and 520b that accommodate different number and types of memory devices, *id.*, Fig.5B (below, annotated), 13:60-14:15. Perego’s buffer “translate[s] protocols” of a memory controller to those of memory devices on the module, “render[ing] the type of memory device transparent to the system.” EX1035, 10:54-67.

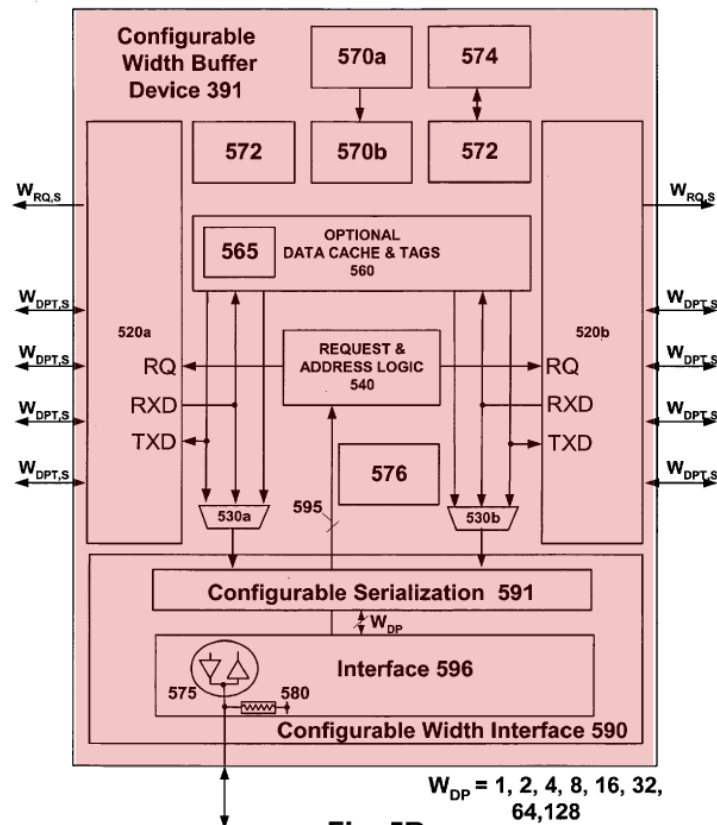


Fig. 5B

b) Harris (EX1023)

“Harris” (EX1023) is prior art under at least §102(a) and (e) (pre-AIA) because it was filed and published before the earliest claimed priority date of the ’366 Patent (June 1, 2007), and alternatively is prior art under §102(a)(1) and (2) (post-AIA). The Board relied on Harris (in combination with other references) to invalidate the related ’918 and ’054 Patents, as discussed above (pp.16-18). EX1070, 90; EX1071, 79.

To resolve the “difficult[y] to mix memory technologies...or provide upgrades to next generation DRAM technology,” EX1023, ¶[0002], Harris

discloses a memory module 100A that includes an on-board voltage regulator module 102 to convert an externally supplied voltage 104 to “appropriate local voltage levels” for DRAM devices on the module, *id.*, Fig.1A (below), ¶¶[0003], [0009-11].

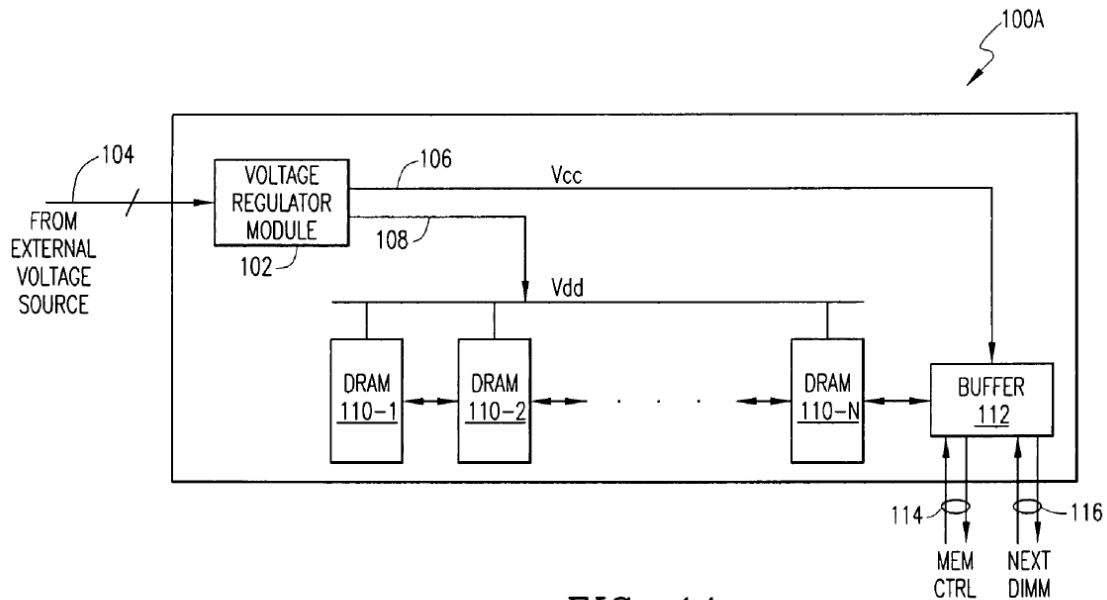


FIG. 1A

c) **Amidi** (EX1024)

“Amidi” (EX1024) is a patent that is prior art under at least §102(e) (pre-AIA) because it was filed before the earliest claimed priority date of the ’366 Patent (June 1, 2007), and alternatively is prior art under §102(a)(2) (post-AIA). The Board relied on Amidi (in combination with other references) to invalidate the related ’918 and ’054 Patents, as discussed above (pp.16-18). EX1070, 90; EX1071, 79.

To avoid loss of “irreplaceable” and “useful” data during power failures, EX1024, 1:19-35, Amidi discloses a memory module that includes a power management block 510 to monitor the system supply voltage 520 and to switch to a battery supply 530 when the system supply fails, *id.*, Figs.5 (below), 6, 4:14-55, Fig.14, 8:23-36.

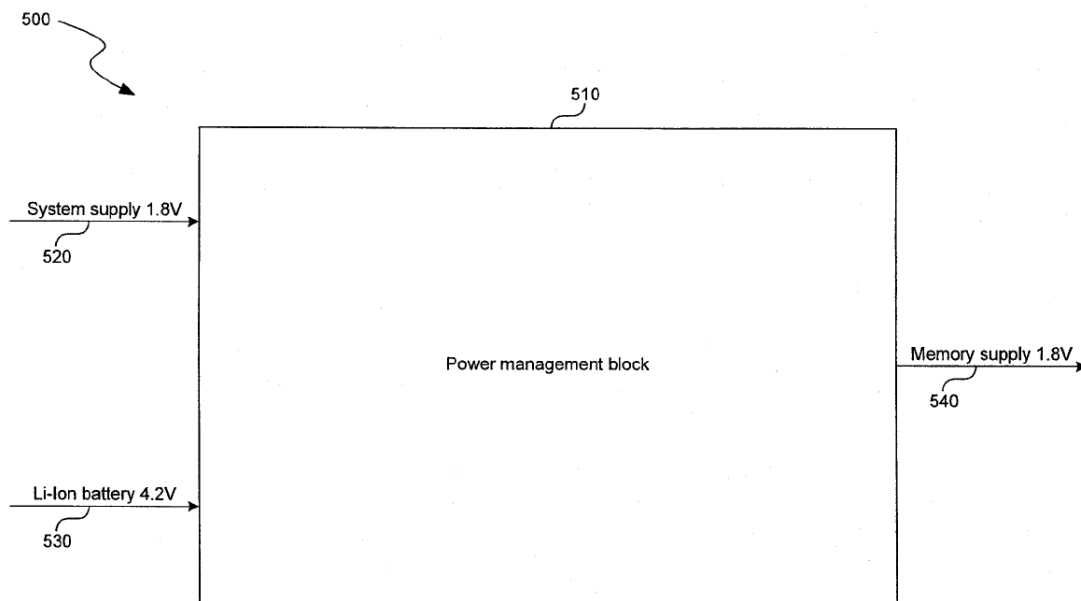


FIG. 5

2. Ground 2 combination: Perego (EX1035) and Harris (EX1023) further in view of Amidi (EX1024)

A POSITA would have been motivated to combine the teachings of Perego and Harris with a reasonable expectation of success. EX1003, ¶153. In the combination, Harris’s power distribution techniques power the components in Perego’s memory module, including the memory devices 360 (green) and the buffer 391 (red), as illustrated below:

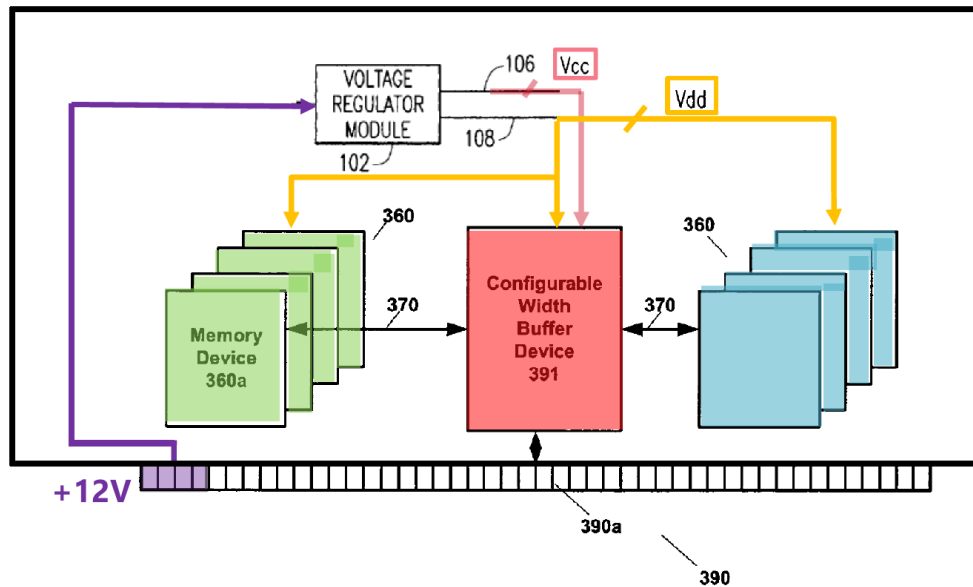


Fig. 3C

EX1035, Fig.3C (modified to illustrate proposed combination); EX1003, ¶153. In the combination, Perego’s memory module includes Harris’s voltage regulator module 102 receiving a 12V power supply (purple) from which it provides the required voltages Vdd (orange) to the memory devices 360 and voltages Vcc (pink) to the buffer device 391. *Id.*

Perego and Harris are analogous art to the ’366 Patent, each being directed to memory modules/systems, and pertinent to solving problems associated with using different types of memory devices in a memory system, including techniques to power these devices. EX1001, 2:6-9 (“employ[ing] different types of memory devices”), 20:56-60 (“provid[ing] power to the various components of the memory system from different sources”); EX1035, 1:12-17 (“memory systems” and

“memory modules...having memory devices”), 10:54-67 (“different types of memory devices...on different modules”), 20:41-47 (“subsets of available memory devices...powered-on during various modes of operation...to achieve power savings”); EX1023, ¶¶[0003] (“a voltage distribution system for a memory board assembly”), [0020] (“provid[ing] upgradeability and extensibility without changing system board,” enabling “cost-effective” “transitioning to newer DRAM technologies”); EX1003, ¶154.

Perego teaches a memory module including a “buffer device...for flexible system configurations, and several performance benefits.” EX1035, 3:23-25. For example, Perego’s buffer (red above) “translate[s] protocols [of the system controller] to the protocol utilized in a particular memory device,” thereby “render[ing] the type of memory device transparent to the system.” *Id.*, 10:59-67, 4:38-42 (“isolating data, control, and address signals of the memory devices”), 6:12-15. This way, “[d]ifferent types of memory devices may be included on different modules within a memory system.” *Id.*, 10:63-64. Perego also teaches that its techniques apply to “DDR2” and “SDRAM,” *id.*, 10:56-59, as well as “[n]ew generations of memory devices,” *id.*, 6:34-43. A POSITA would have understood that using different types of memory devices on Perego’s memory module requires “different power suppl[ies],” “making it difficult to mix memory technologies...or provide upgrades to next generation DRAM technology in a cost-

effective manner.” EX1023, ¶[0002]; EX1003, ¶¶155-156. Harris solves this problem with a “voltage distribution system,” which is “locally converting the voltage by an on-board voltage regulator module to generate appropriate local voltage levels for...memory devices” on the module. EX1023, ¶[0003].

Therefore, a POSITA would have been motivated to implement Harris’s “voltage distribution” functionality in Perego’s memory module to provide a simple, cost effective, and advantageous power supply. EX1003, ¶156. Indeed, Harris teaches its “voltage-independent,” on-board voltage converting technique “provide[s] upgradeability and extensibility without changing system board power distribution,” allowing “transitioning to newer DRAM technologies” in a “more cost-effective” and “simpler” way. EX1023, ¶[0020]. Harris further teaches many other technical benefits gained by its technique. *Id.*, ¶¶[0011] (“support[ing] large memory capacity scaling, hot-pluggability, DRAM technology independence..., high DRAM device count (i.e., amenable to multi-ranking), as well as provid[ing] improved system level cost sharing...[and] tighter voltage regulation”); [0019] (reducing “power supply design’s complexity” and “cost,” “provision of tighter, lower inductance regulation,” “reduction in the pin count,” and “improved signal integrity”). Realizing any one or more of the benefits taught by Harris would have further motivated a POSITA to implement Harris’s power distribution teachings in Perego’s memory system. EX1003, ¶¶157-159.

Such a combination would have been well within the level of skill, as taught by Perego, Harris, and the knowledge of a POSITA. EX1003, ¶160. For example, Harris teaches “Dual In-line Memory Modules (DIMMS)” powered by the system board, EX1023, ¶[0002], via a “+12V power supply rail,” *id.*, ¶[0020]. A POSITA would have understood that such a “+12V power supply rail” was provided on commercially available motherboards. EX1085, 8 (“+12 VDC currents”), 13 (Table 2, including two 12V outputs); EX1003, ¶160. Converting the 12V power supply locally on a memory module was also well known, as evidenced by commercially available buck converters converting a 12V power supply to a lower voltage to operate module components, such as DRAM devices (e.g., V_{DDQ} and V_{TT}). *See, e.g.*, EX1041, 1; EX1023, ¶[0009]; EX1062, 15; EX1078, 1; EX1048, 1; EX1003, ¶161. Thus, a POSITA would have successfully implemented the combination, where Perego’s memory module receives a well-known 12V power supply from the motherboard, and Harris’s on-board voltage regulator module uses known buck converters to provide the appropriate voltage levels for various components on the module. EX1003, ¶161.

A POSITA would have been further motivated to use Amidi’s power monitoring and backup techniques in the Perego-Harris memory module to prevent data loss during power failures, as illustrated by the further combination below:

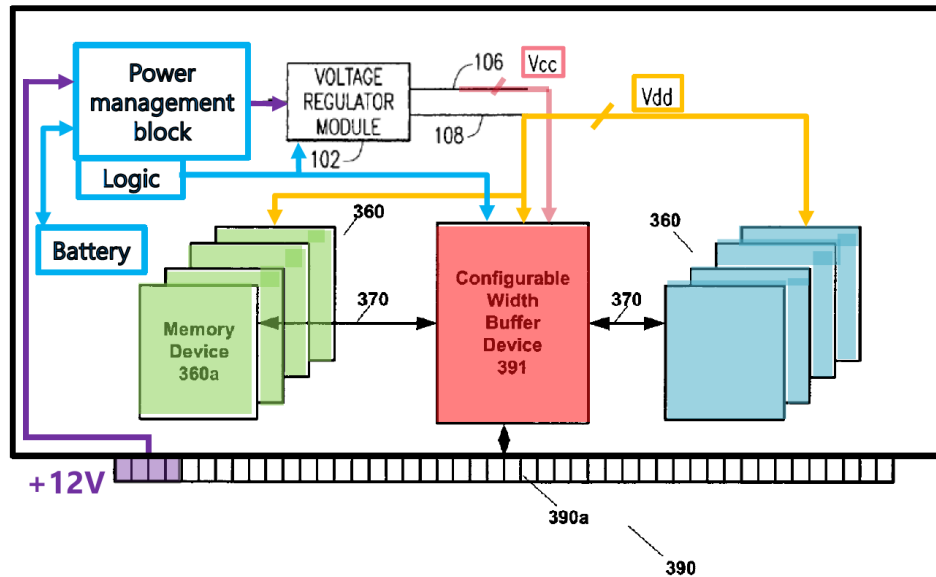


Fig. 3C

EX1003, ¶162. In the combination, Amidi's Logic and Power management functionalities (light blue) detect faults in Harris's +12V system power (purple), switch to on-board battery power, and put the memory devices 360 into self-refresh mode to save power while preserving data. EX1003, ¶162. The Board has already found that a POSITA would have been motivated to combine Amidi and Harris with a reasonable expectation of success. EX1070, 72-75; EX1071, 56-60 EX1003, ¶163.

Amidi, like Perego and Harris, is analogous art to the '366 Patent, each being directed to memory modules/systems, solving problems of using different types of memory devices, and powering these devices. *Supra* pp.26-27; EX1024, Abstract ("power fault detection for a memory module"), 2:11-26 (providing "[c]lock and power fault detection" "within a memory module" is "very helpful"

because it removes “the overhead to deal with many different types of memory modules”); EX1003, ¶164.

A POSITA would have been motivated to implement Amidi’s power monitoring and backup techniques in the Perego-Harris module with a reasonable expectation of success. EX1003, ¶165. For example, Amidi teaches the need for “keeping data in volatile memory [like DRAMs]” during power failures. EX1024, 1:28-30; 1:19-27 (“irreplaceable” and “useful” volatile data). Harris also recognizes the importance of reliable power and proposes a “redundant” power source. EX1023, ¶¶[0012-14], [0016], Figs.1B, 2. Amidi teaches that power fault detection and supplying backup power “within a memory module can be very helpful” because it removes the need for external system circuitry or the overhead associated with “different types of memory modules.” EX1024, 2:11-26. Thus, a POSITA would have been motivated to implement Amidi’s power-fault detection technique “within a memory module” itself for maintaining data during power failures. *Id.*, Abstract, 1:28-35, 2:6-26, 4:14-60, Figs.4-6; EX1003, ¶165.

Such a combination would have been well within the level of skill as taught by Amidi, Harris, and the knowledge of a POSITA. EX1003, ¶166. For example, Amidi’s “power management block” could be modified easily to work with the Perego-Harris combination, as shown in the annotated Fig.5 of Amidi below:

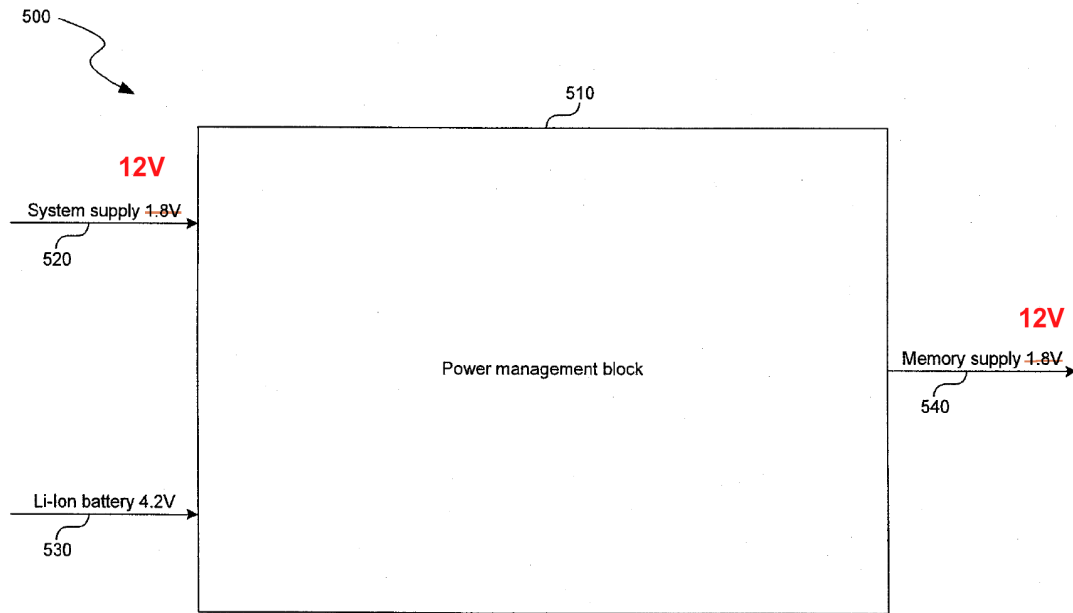


FIG. 5

EX1024, Fig.5 (annotated); EX1003, ¶166. Harris teaches a 12V supply voltage, EX1023, ¶[0012], thus it would have been obvious to a POSITA that, in a combination with Harris, Amidi's "power management block" also uses the 12V as the system supply (520, above left). EX1003, ¶166. A POSITA would have also understood that Harris's 12V supply can be stepped-down and stepped-up within Amidi's "power management block" as needed to charge an on-board battery 620, below, and to provide a supply voltage to Harris's memory module (via 660 below and 540 above). EX1024, Fig.6 (below), 4:25-27 ("FIG. 6 illustrates an embodiment of the internals of a power management block."); EX1003, ¶¶166-167.

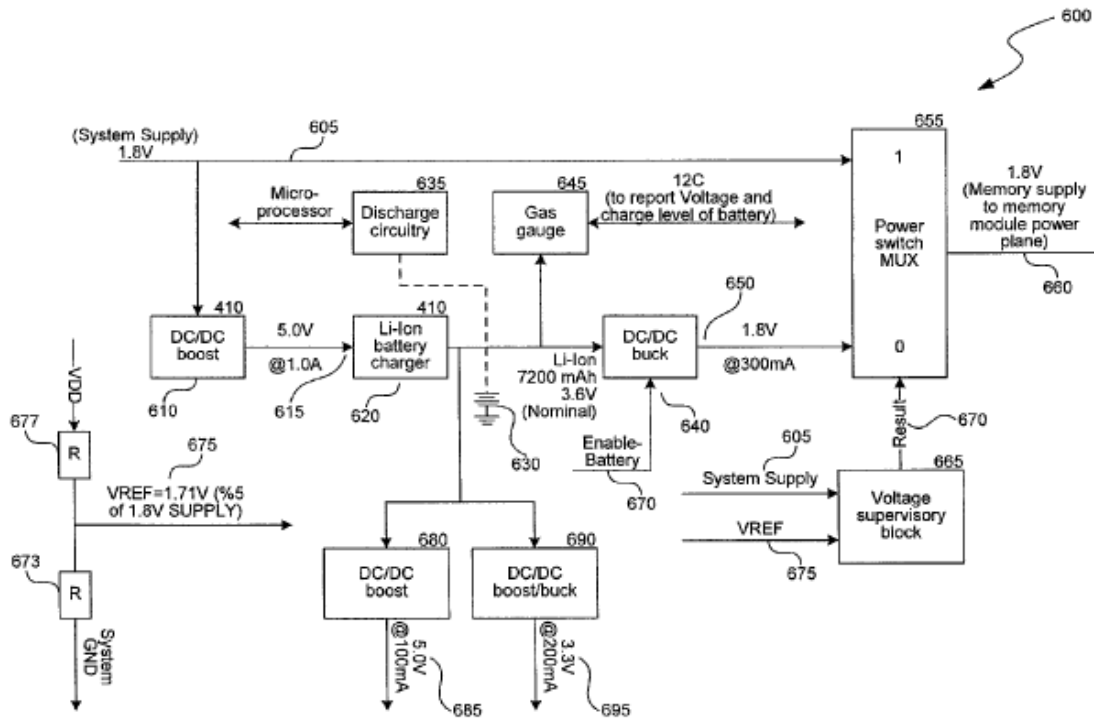


FIG. 6

Indeed, Amidi expressly discloses that its “power management block” uses “buck” converters to step-down voltages as needed, *see, e.g.*, EX1024, 4:38-40 & Fig.6 (640 “buck”), and “boost” converters to step-up voltages as needed, *id.*, 4:27-32 & Fig.6 (610 “boost”). Boost and buck converters were well-known, widely used at the time, and had long been taught in textbooks, as discussed above (pp.13-14). EX1003, ¶167.

Amidi also teaches that data in the volatile memory devices in the combination can be preserved while saving power by performing self-refresh operations, EX1024, 2:16-19 (“maintain memory (through refresh)”), 6:40-52 (“refresh SDRAM of a memory module”), Figs.11, 13 (control of self-refresh

operations), which were available on standard memory devices at the time, *see*, *e.g.*, EX1026, 39-40 (“Self Refresh...to retain data in the DDR2 SDRAM”); EX1046, 70-71 (similar for DDR3); EX1003, ¶168. Furthermore, Amidi’s battery backup mode is similar to the well-known S3 power-saving mode, where a memory module, like FBDIMM, is “put into a very lower power state, with the DRAMs in self refresh mode.” EX1027, 39; EX1003 ¶169. Amidi, like the S3 mode, puts the DRAMs in a self-refresh state to save battery power and extend data retention time, when the system power fails, and thus the battery powers the module. EX1024, 6:40-52. Accordingly, a POSITA would have been motivated to follow relevant, known S3 power saving techniques when implementing Amidi’s techniques in the Perego-Harris module. EX1027, 21 (During “S3 power mode,” only VDD is “on” to put “DRAMs...in self refresh,” while CKE and all other power supplies, VCC/VCCFBD, VTT, and VDDSPD, are disabled.); EX1028, 9 (“[s]upply voltages” including VDD, VCC/VCCFBD, VTT, and VDDSPD); EX1003 ¶169.

Thus, a POSITA would have been motivated to implement the Perego-Harris module with the functionality of Amidi’s power management and logic for detecting power faults and switching over to battery backup when needed. EX1003, ¶170. This straightforward combination simply uses a known technique (*e.g.*, Amidi’s battery backup techniques) to improve a similar device (*e.g.*, the

Perego-Harris module) in the same way (e.g., to provide a backup power supply using a battery), while providing predictable results (e.g., preserving data with the redundant power during system supply/clock failures). *Id.*

3. Independent Claim 1

a) [1.a.1] DIMM

Ground 2 discloses “[a] *dual in-line memory module (DIMM)* [e.g., “memory subsystems 330a-330c” or 340] *configured to fit into a memory slot connector* [e.g., “mating connectors 380a-380n”] *of a system board* [e.g., “a common substrate”] *of a computer system* [e.g., “incorporat[ing]” “point-to-point links 320a-320n, memory subsystems 330a-330c (including mating connectors 380a-n), and controller 310” in “memory system 305”].” EX1035, 5:56-6:11, 6:57-62 (“a buffered memory module”), Fig.3B (below, annotated).

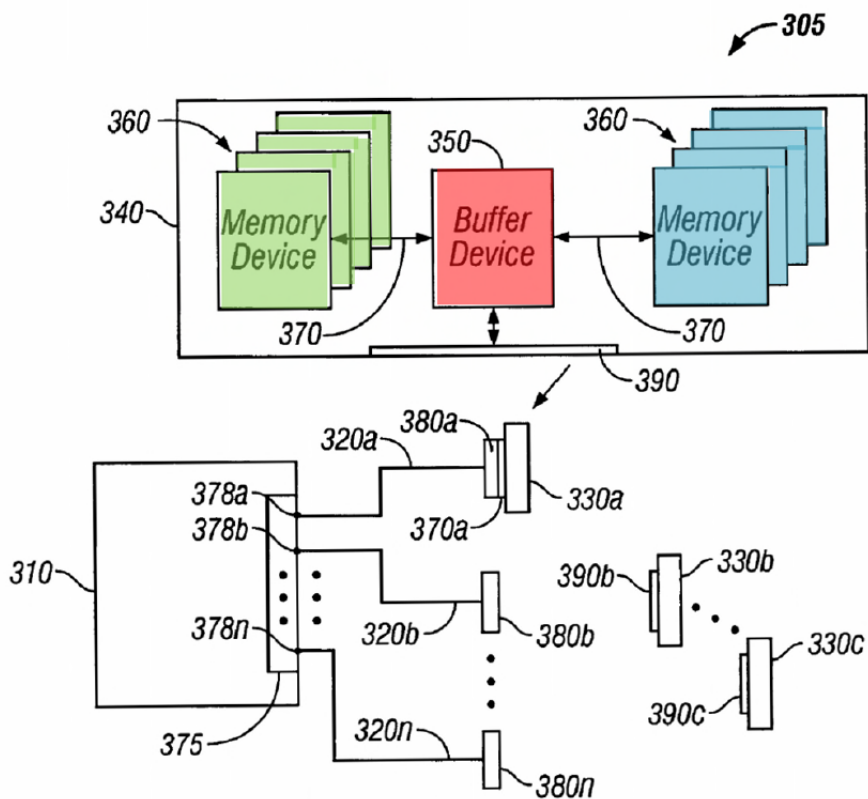


FIG. 3B

Also, Perego discloses his memory module may a “conventional DIMM module.” EX1035, Fig.3C (below), 6:25-33, 1:58-2:6 (“dual inline memory module (DIMM)” citing EX1108 (Dell), Fig.1 (below, edge connectors on both sides of a DIMM), 1:65-2:20); *see also* EX1051 (Doblar), ¶¶[0043-47], Figs.1-5 (similar).

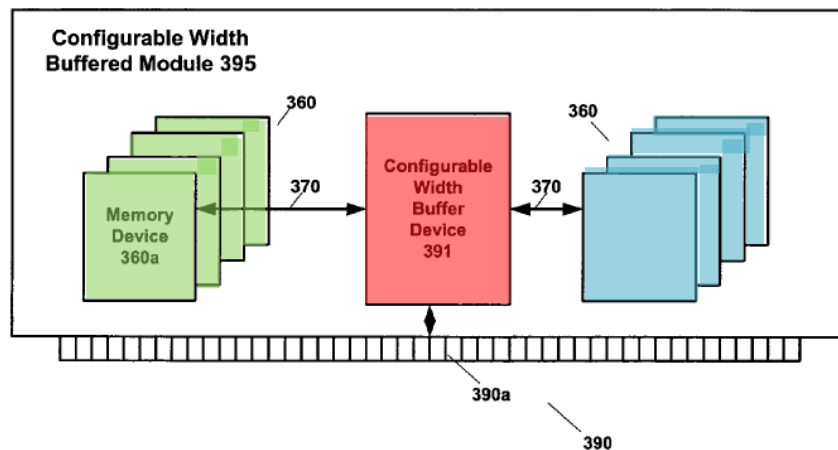
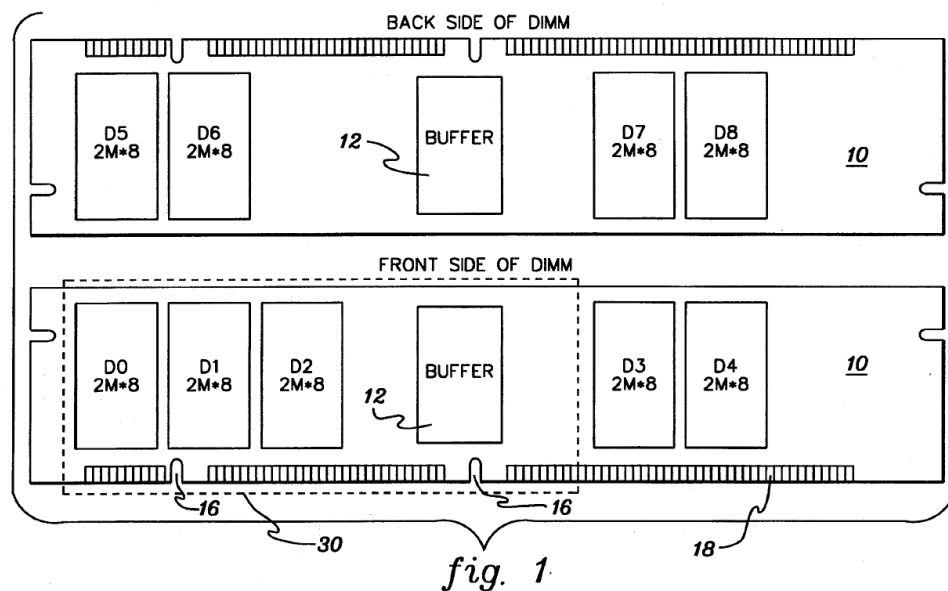


Fig. 3C



Similarly, Harris and Amidi disclose their memory modules can be “implemented as a...DIMM,” coupled to the system board via slot connectors. EX1023, ¶¶[0009], [0002], [0019] (“DIMM connector to system board”); EX1024, Figs.3, 4 (below), 3:49-63 (“edge connector pins”).

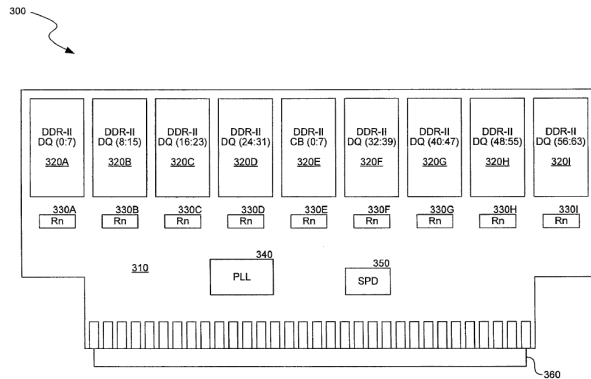


FIG. 3

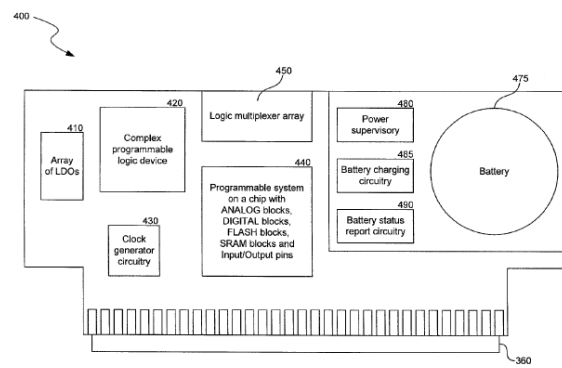


FIG. 4

b) [1.a.2] Conduits

Ground 2 discloses “*the memory slot connector [e.g., “mating connectors 380a-380n”] including a set of power conduits [e.g., receiving power supplies from the system], a set of data conduits [e.g., interfacing “DQ” data signals], and a set of address and control conduits [e.g., interfacing “RQ” address/control signals].*” EX1035, Fig.4B (below, annotated); EX1003, ¶172.

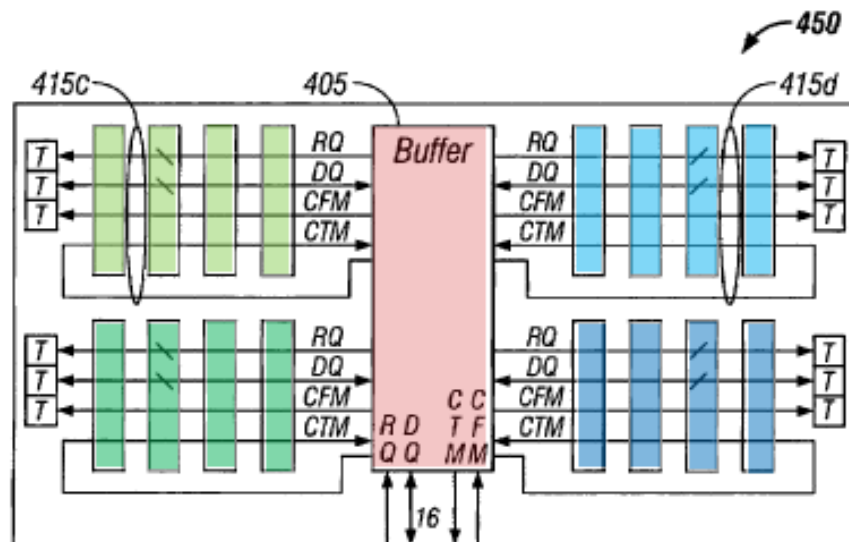


FIG. 4B

Perego teaches channels 415 “include control lines (RQ) [and] data lines (DQ),” which transfer address/control and data signals the module receives from “edge connectors” 390. EX1035, 9:43-45, 9:58-60 (the RQ control lines including “row address strobe, column address strobe, etc., and address lines.”), Figs.3C (below), 4B (above), 13:13-17 (“to provide electrical connections between [the buffer 391] and connector 390”); *see also* EX1026, 6 (“Command Inputs: RAS, CAS and WE (along with CS) define the command entered.”); EX1107, 4 (“DRAM’s RAS pin (*row address strobe*)...DRAM’s CAS pin (*column address strobe*)”) (emphasis in original); EX1090, 24-32 (finding Perego compatible with JEDEC standards); EX1091, 28-37 (same). EX1003, ¶173.

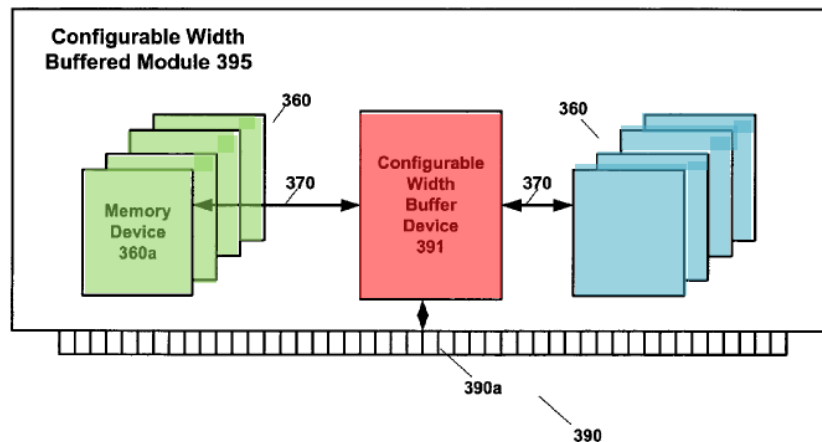


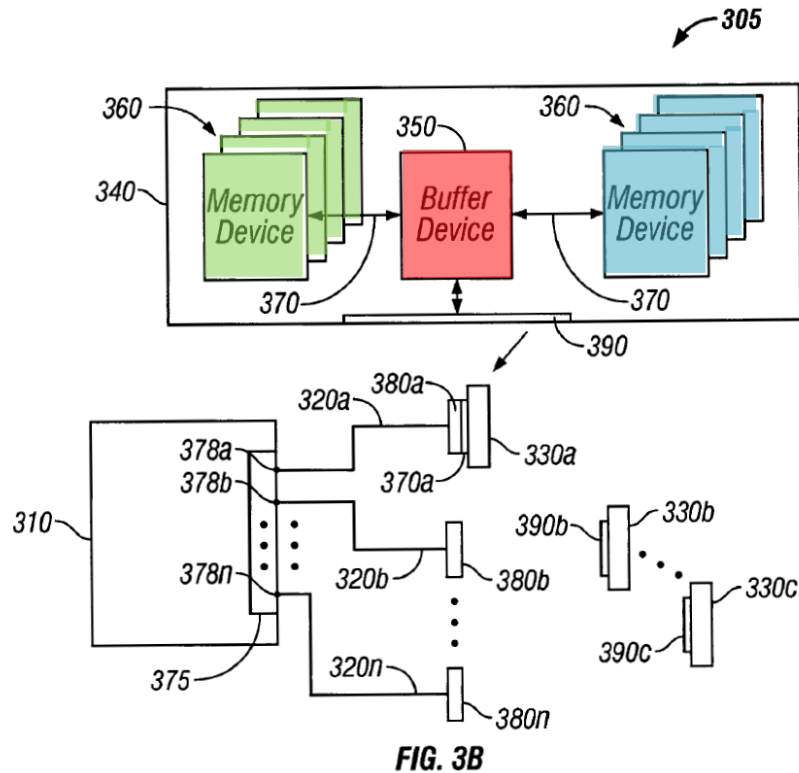
Fig. 3C

Similarly, Harris and Amidi disclose edge connectors by which the memory module communicates data and address/control signals with the memory controller, as was common at the time for DIMMs. EX1023, ¶¶[0013]

(“compatible with...(JEDEC) standards”), [0009] (“buffer/logic component 112...buffering command/address (C/A)...as well as data”), Fig.3 (showing buffer 112 receiving data and address/control signals via edge connectors); EX1024, Figs.3, 4, 3:58-62 (“set of printed conductors on an edge”), 4:1-2; EX1108 (Dell), Figs.1-4; EX1003, ¶174. The edge connectors for data signals may be separate from those for address/control signals. *See, e.g.*, EX1108 (Dell), Fig.3 (showing “168 PIN SDRAM DIMM” including separate data (DQ0-DQ79) and control/address (A0-A13, CS0-CS4, etc.) pins); EX1003, ¶174.

Perego also discloses that RQ control and DQ data lines “may equally apply” to links 320 between the memory module and the system controller, EX1035, 9:43-49, and that “mating connectors 380a-380n interface with [edge] connectors 390” for the module to communicate with the system controller, *id.*, 6:1-11. *See also* EX1024, 3:58-62 (“set of printed conductors on an edge...mat[ing] with a slot or socket...to which memory module 300 is connected”). Thus, the “mating connectors 380a-380n” include “*a set of data conduits*” electrically coupled with the data edge connectors to interface data and also include “*a set of address and control conduits*” electrically coupled with the address/control edge connectors to interface address/control signals. EX1003, ¶175.

The “mating connectors 380a-380n” further include “*a set of power conduits*” to receive power supplies from the system. EX1003, ¶176. For example, Perego discloses the DIMM’s edge connectors 390 include power supply connectors to receive system power through the “mating connectors 380a-380n,” as was common at the time. EX1035, FIG.3B (below, annotated); EX1108 (Dell), 1:65-2:20 (“connector tabs” for “deriving all necessary power, ground, and logic signals”), Fig.3 (DIMM having Power Supply and Ground pins); EX1051 (Doblar), ¶¶[0043-47], Figs.1-5 (DIMMs with edge connector pins and mating connector sockets including pins for power); EX1104, 4.20.4-1 (“Registered DIMM Design Specification”), 4.20.4-6 (various power supply pins, including V_{DD} , V_{DDQ} , V_{REF} , and V_{DDSPD}); EX1028, 1 (“(FBDIMM) Design Specification”), 11 (various power supply pins); EX1003, ¶176.



Harris similarly discloses edge connectors on the module receiving power supply from the system. EX1003, ¶177. For example, Harris discloses that standard DIMMs have “pins” for “power supply” and that his memory module uses “as few as six +12V pins” to receive power supplies from the system. EX1023, ¶¶[0012], [0002] (“(DIMMS)” with “a relatively large number of pins[] that are powered from system board”), [0019]. As discussed above, *supra* pp.25-29, providing 12V power supplies from a motherboard to Harris’s module was readily available. EX1023, ¶¶[0014] (“any combination of known or heretofore unknown voltage supplies”), [0020] (“industry-standard form factors,” including “dual +12V power supply rail implementations”), [0017] (“the supply

voltage...sourced from the memory controller 302”), Fig.3 (below); EX1003, ¶177. The Board also previously found that Harris’s memory module includes edge connectors to receive power “from...the host system.” EX1070, 42-50; EX1071, 37-39; EX1003, ¶178.

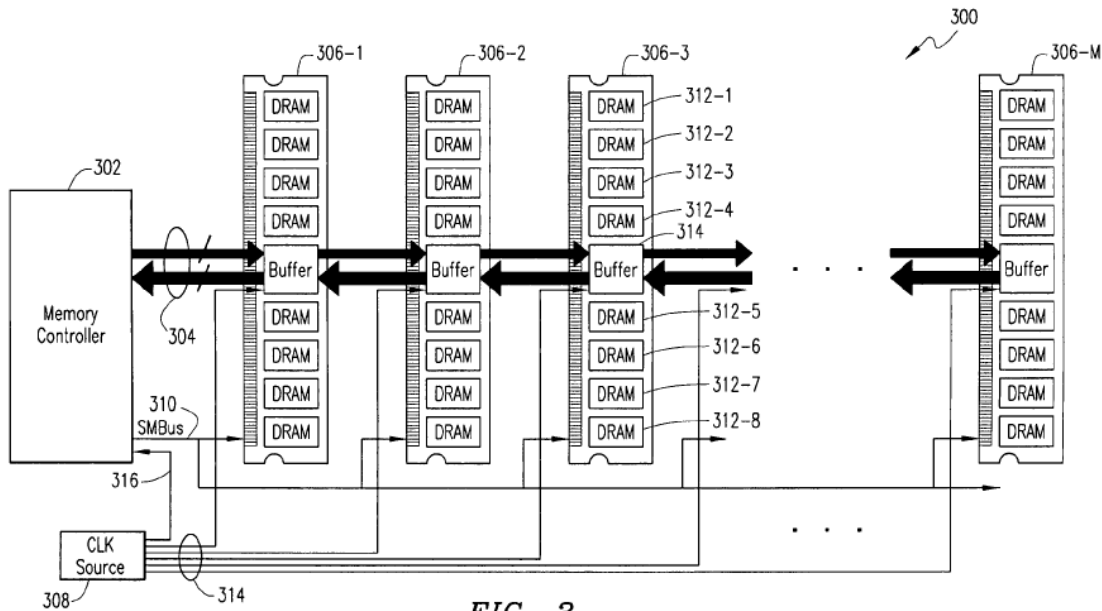


FIG. 3

Accordingly, the memory module of Ground 2 includes edge connectors not only to communicate data and address/control signals as explained above, but also to receive a +12V power supply (purple, below) as taught by the references and common at the time. *Supra* pp.25-35; EX1035, Fig.3C (below, annotated); EX1003, ¶179. Thus, the “mating connectors 380a-380n” further include “a set of *power conduits*” electrically coupled to the power supply edge connectors to deliver the system power to the module. EX1035, 6:1-11; EX1003, ¶179.

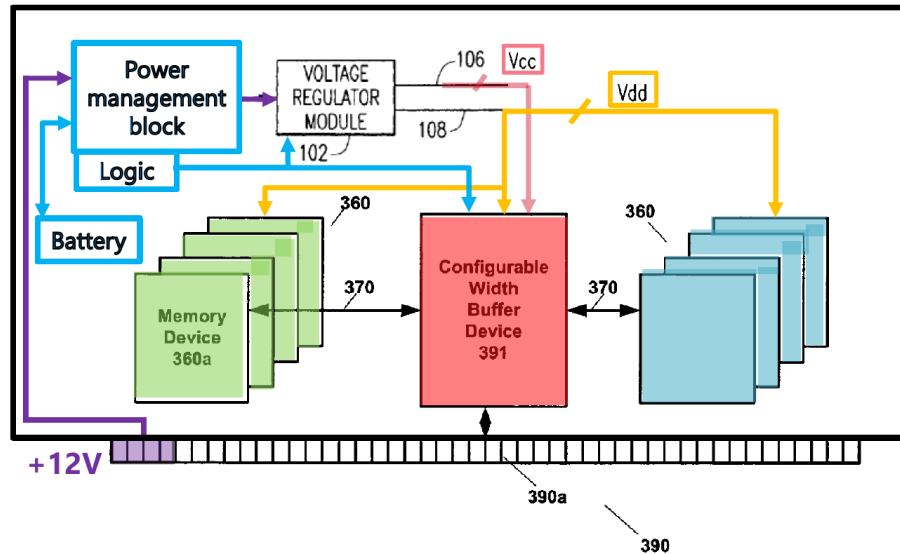


Fig. 3C

c) [1.a.3] Data Conduits

Ground 2 discloses “*data signals [e.g., “DQ” signals] are transferred between the system board and the DIMM via the set of data conduits*” for the reasons discussed above for [1.a.2] (pp.38-44); *see also* EX1035, Figs.3B, 4B (below, annotated), 9:43-49 (“data lines (DQ)”), 6:1-11.

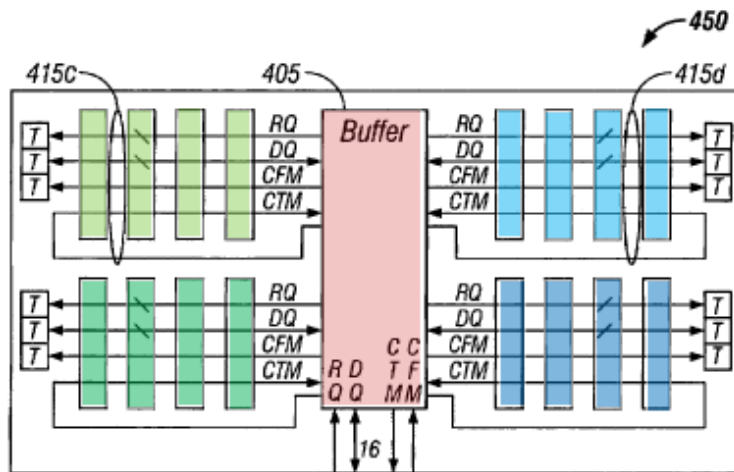


FIG. 4B

d) [1.a.4] Address/Control Conduits

Ground 2 discloses “address and control signals [e.g., “RQ” signals] are delivered from the system board to the DIMM via the set of address and control conduits” for the reasons discussed above for [1.a.2] (pp.38-44); see also EX1035, Figs.3B, 4B (below, annotated), 9:43-49 (“control lines (RQ)”), 9:58-60 (“row address strobe, column address strobe, etc., and address lines”), 6:1-11.

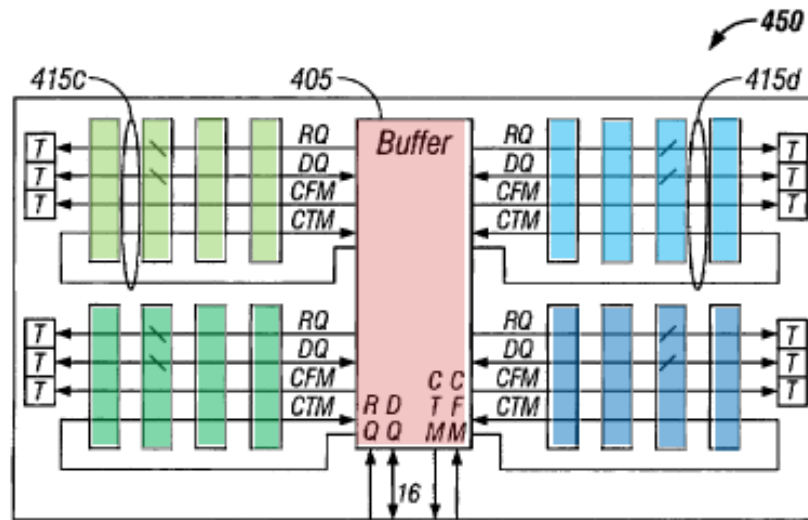


FIG. 4B

e) [1.b.1] PCB

Ground 2 discloses “a printed circuit board (PCB) having edge connections [e.g., “edge connectors” 390] configured to fit into the memory slot connector [e.g., “mating connectors 380a-380n”] of the system board.” EX1035, 6:1-11, Figs.3B, 3C (below, annotated).

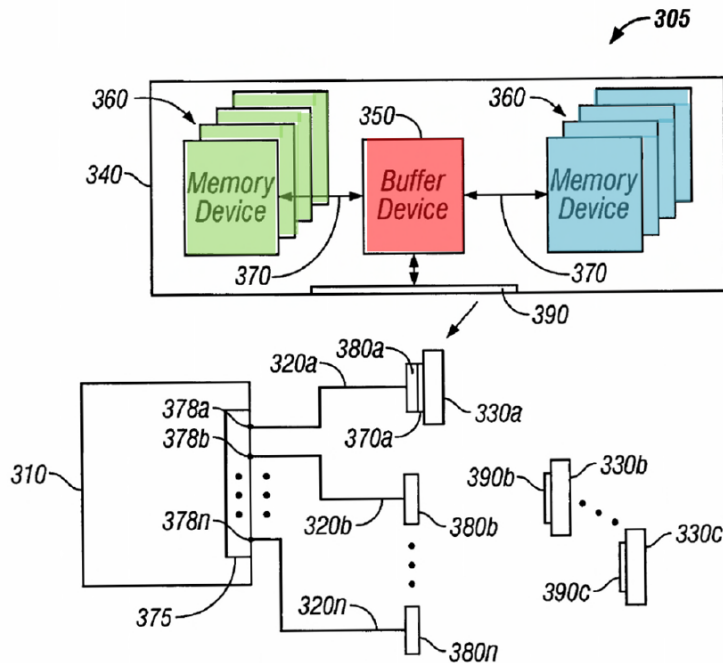


FIG. 3B

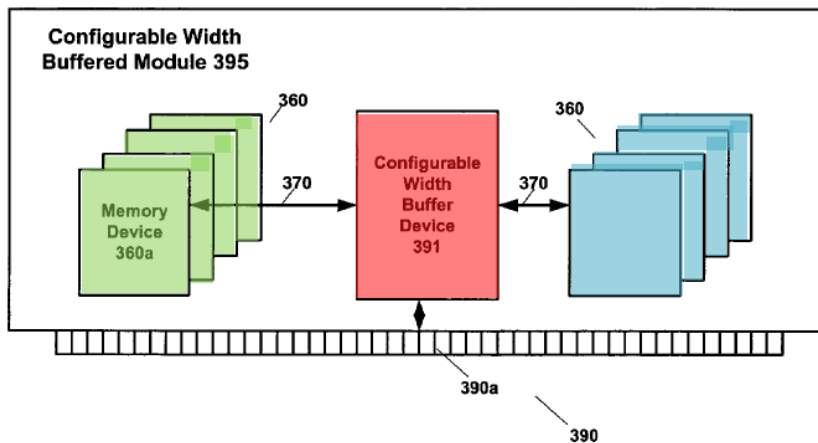


Fig. 3C

Perego teaches the DIMMs are “incorporated onto...PCBs” with “[edge] connectors 390a-390c,” which “interface with mating connectors 380a-380n to allow removal/inclusion of [the DIMM] in memory system 305” as discussed above for [1.a.1] (pp.35-38). EX1035, 5:56-6:6. Thus, the edge connectors 390

are “*configured to fit into*” the “mating connectors 380a-380n.” EX1035, 6:6-11 (“mating connectors 380a-380n are **sockets** and connectors 390a-390c are **edge connectors** disposed on” the DIMM) (emphasis added), Figs.3B, 3C. Similarly, Harris and Amidi disclose this limitation as discussed above for [1.a.1] (pp.35-38). EX1023, ¶[0013] (“printed circuit board...compatible with...(JEDEC) standards”); EX1024, 3:49-53 (“printed circuit board”), 3:58-62 (“a set of printed conductors on an edge...mat[ing] with a slot or socket”), Figs.3, 4 (showing edge connectors).

f) [1.b.2] First Set of Edge Connections

Ground 2 discloses “*a first set of edge connections [e.g., purple in edge connectors 390 below] configured to be electrically connected to the set of power conduits [e.g., in “mating connectors 380a-380n”] and operable to deliver to the DIMM power [e.g., +12V] from power rails of the system board via the set of power conduits*” for the reasons discussed above for [1.a.2] (pp.38-44). EX1035, Fig.3C (below, annotated); EX1023, ¶¶[0012] (“as few as six +12V pins”), [0020] (“dual +12V power supply rail”).

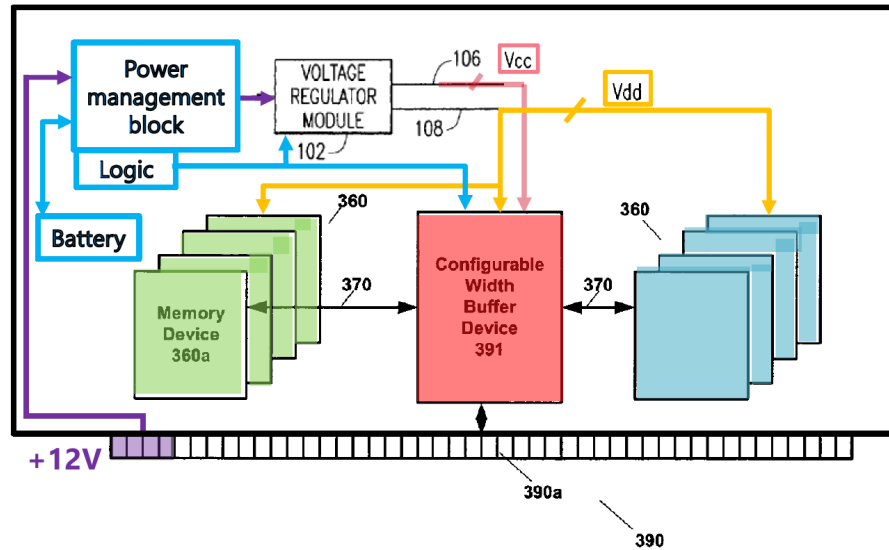


Fig. 3C

g) [1.b.3] Power Delivered to the DIMM

Ground 2 discloses “the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM” as explained above for [1.a.2] (pp.38-44) and [1.b.2] (pp.47-48) and as shown in the annotated Fig.3C below. EX1035, Fig.3C (below); EX1003, ¶180.

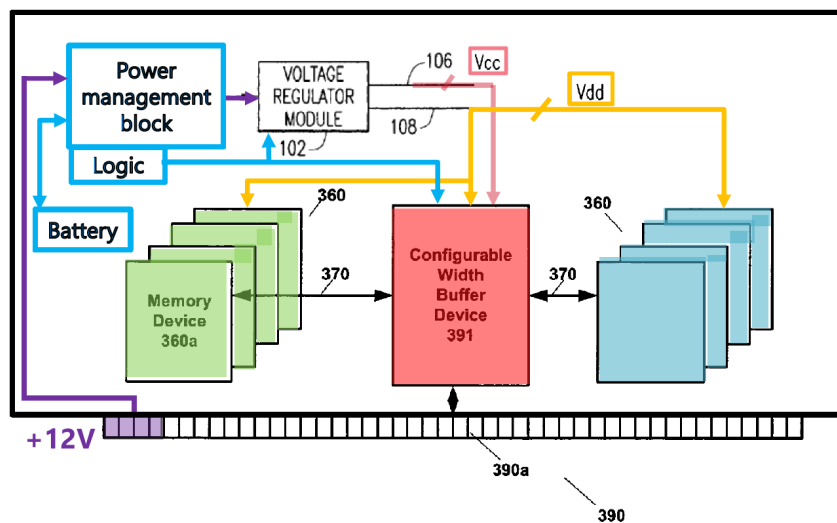


Fig. 3C

For example, Harris teaches “power supply rails...from system board” as the only power source to the DIMM, as was common at the time. EX1023, ¶¶[0002], [0020]; EX1003, ¶181. Also common was “deriving all necessary power” from the DIMM’s connectors coupled to the system board. EX1108 (Dell, cited by Perego (EX1035) at 2:4-6), 1:65-2:20; EX1003, ¶182. Similarly, Amidi teaches the “system supply” is the only power source for the memory module’s operations, including charging an on-board battery 475 or 630. EX1024, Figs.4, 6 (below), 3:64-4:13, 4:23-43; EX1003, ¶183. Amidi’s disclosure is similar to that of the ’366 Patent. EX1001, 20:63-67, 26:19-39; EX1003, ¶184.

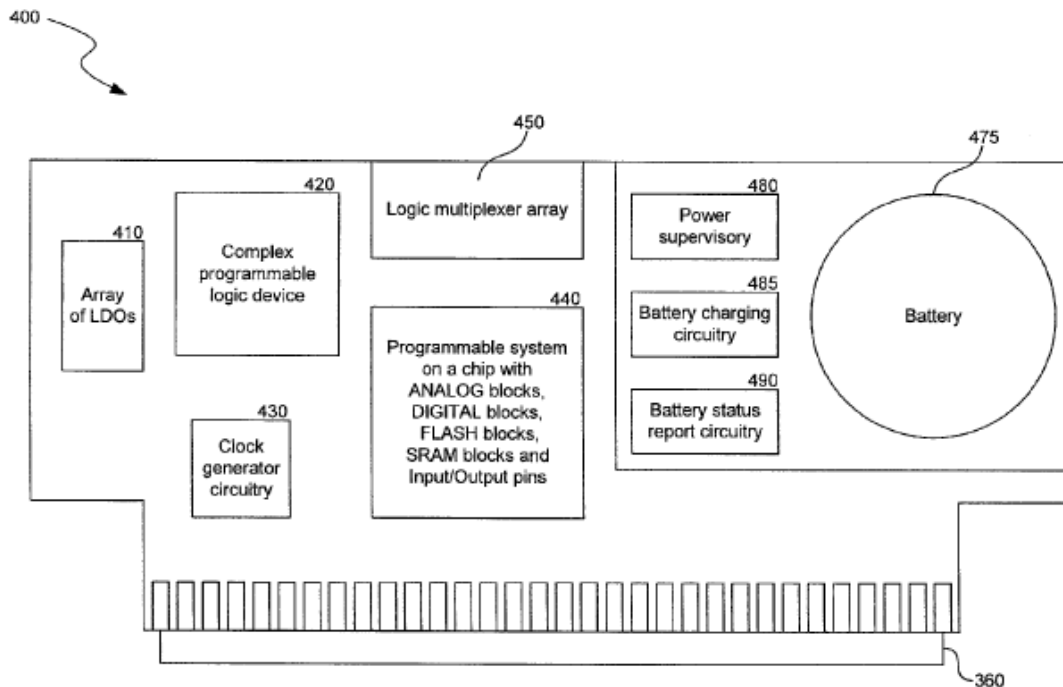


FIG. 4

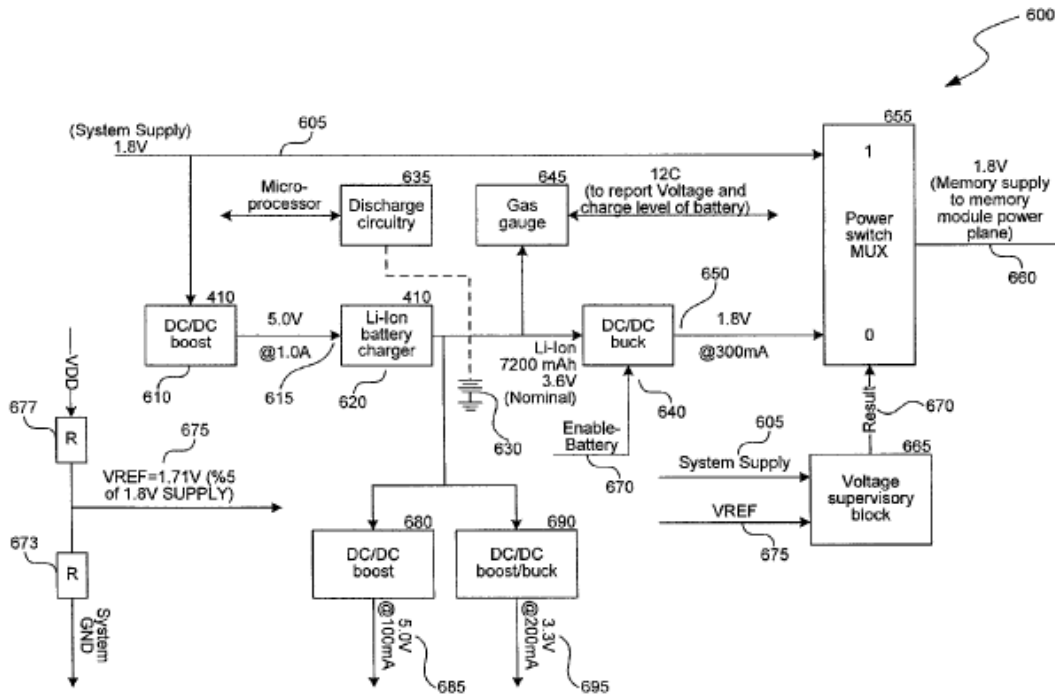


FIG. 6

h) [1.b.4] Second Set of Edge Connections

Ground 2 discloses “a second set of edge connections [e.g., in edge connectors 390 below] configured to be electrically connected to the set of data conduits [e.g., in “mating connectors 380a-380n” for interfacing DQ signals between the DIMM and the system controller]” for the reasons discussed above for [1.a.2] (pp.38-44). EX1035, Fig.3C, 4B (below, annotated).

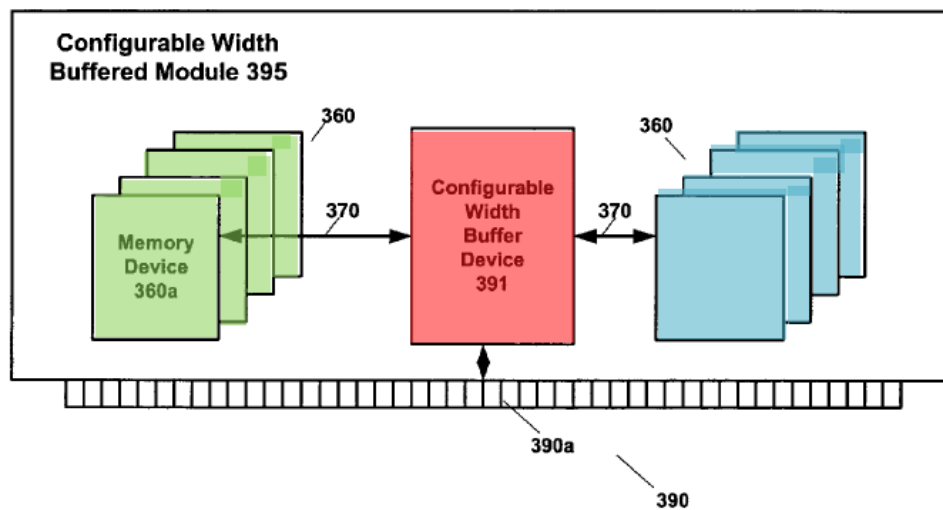


Fig. 3C

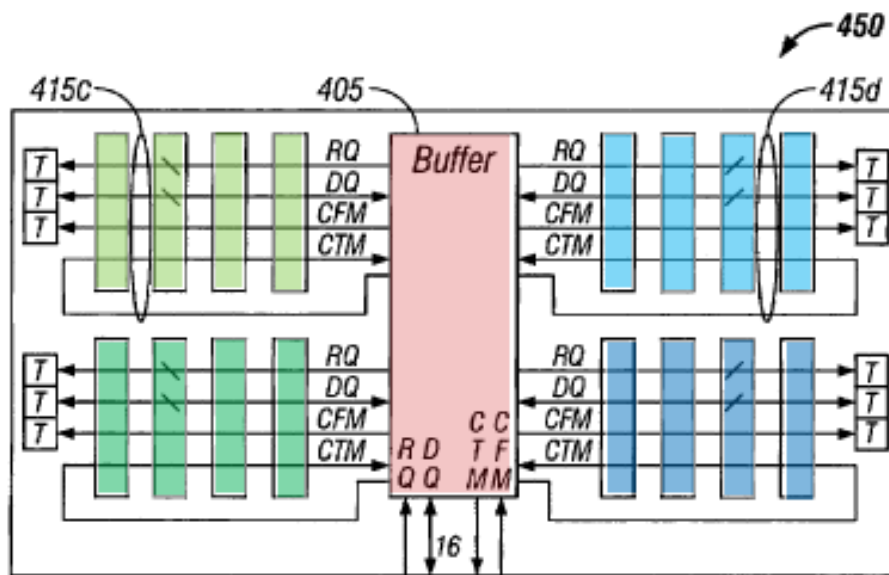


FIG. 4B

i) [1.b.5] Third Set of Edge Connections

Ground 2 discloses “a third set of edge connections [e.g., in edge connectors 390 below] configured to be electrically connected to the set of address and

control conduits [e.g., in “mating connectors 380a-380n” for interfacing RQ signals between the DIMM and the system controller]” for the reasons discussed above for [1.a.2] (pp.38-44). EX1035, Fig.3C, 4B (below, annotated).

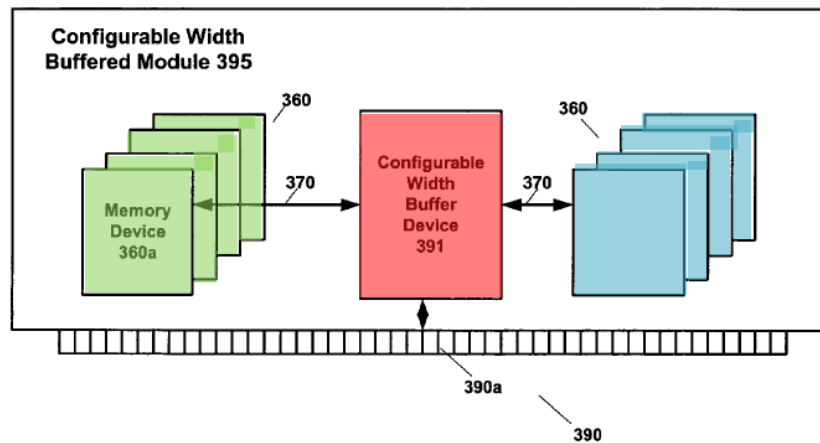


Fig. 3C

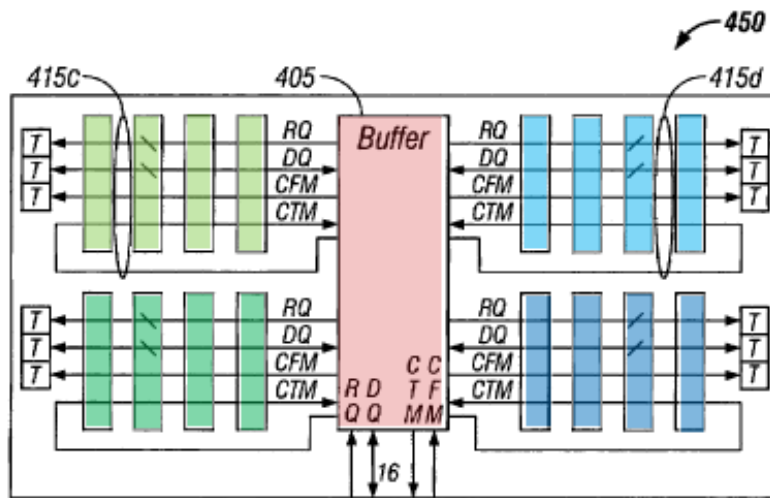


FIG. 4B

j) [1.b.6] Voltage Supply Lines

Ground 2 discloses “a set of voltage supply lines [e.g., purple arrow below providing power to the module components] *electrically connected to the first set of edge connections* [e.g., purple in edge connectors 390] *and configured to receive the power delivered to the DIMM* [e.g., receiving a +12V supply] *from the power rails of the system board by way of the memory slot connector of the system board* [e.g., “mating connectors 380a-380n,” coupled to the system controller] *and the first set of edge connections of the DIMM*” for the reasons discussed above for [1.a.2], [1.b.2], and [1.b.3] (pp.38-44, 47-50). EX1035, Fig.3C (below, annotated); see also EX1023, ¶¶[0012] (“+12V pins” providing “power” to the memory devices), [0020] (“dual +12V power supply rail implementations”).

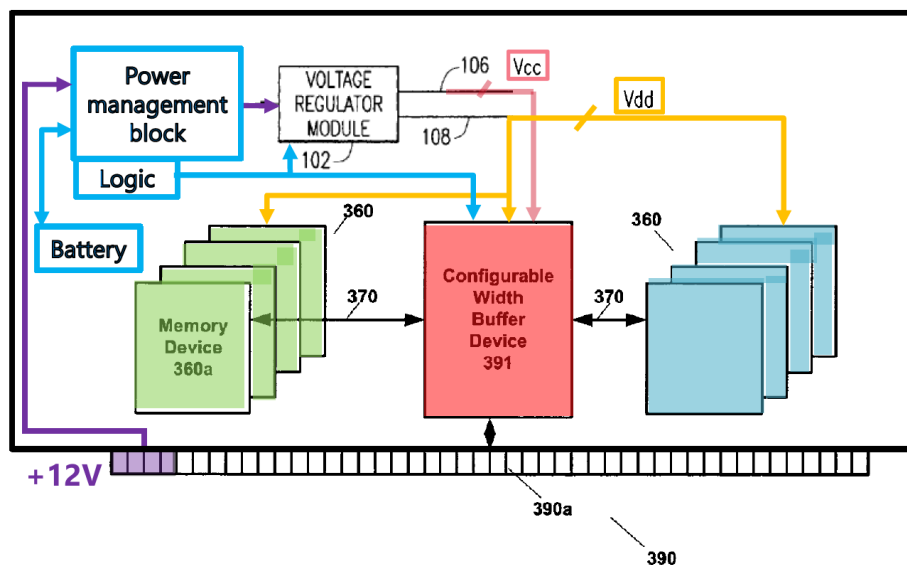


Fig. 3C

k) [1.b.7] Data Lines

Ground 2 discloses “a set of data lines [e.g., DQ data lines in channel 370 or 415 leading to edge connectors 390 via buffer device (red) below] *electrically connected to the second set of edge connections* [e.g., in edge connectors 390]” for the reasons discussed above for [1.a.2], [1.a.3] and [1.b.4] (pp.38-44, 50-51).

EX1035, Fig.3C, 4B (below, annotated).

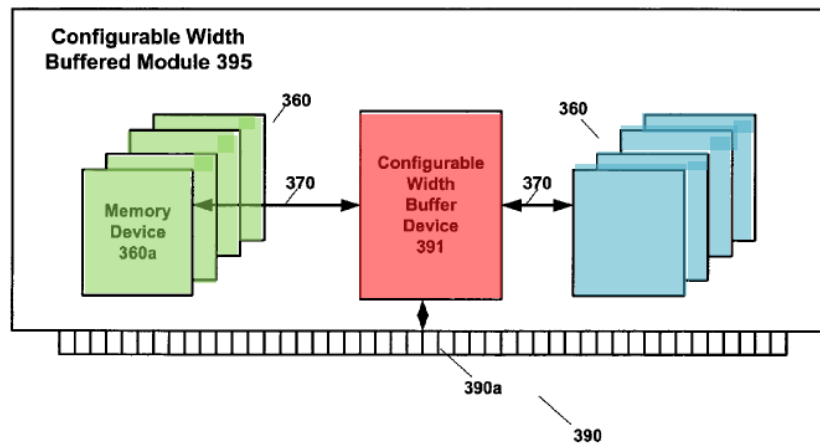


Fig. 3C

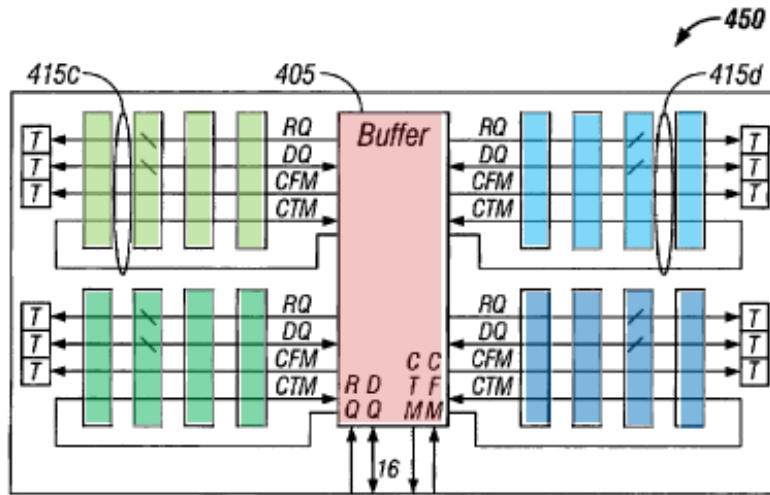


FIG. 4B

l) [1.b.8] Address/Control Lines

Ground 2 discloses “a set of address and control lines [e.g., RQ address/control lines in channel 370 or 415 leading to edge connectors 390 via buffer device (red) below] *electrically connected to the third set of edge connections* [e.g., in edge connectors 390]” for the reasons discussed above for [1.a.2], [1.a.4] and [1.b.5] (pp.38-44, 45-45, 51-52). EX1035, Fig.3C, 4B (below, annotated).

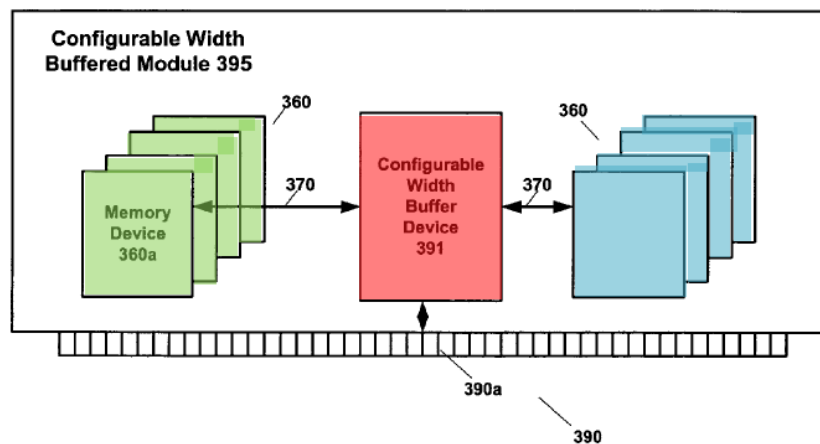


Fig. 3C

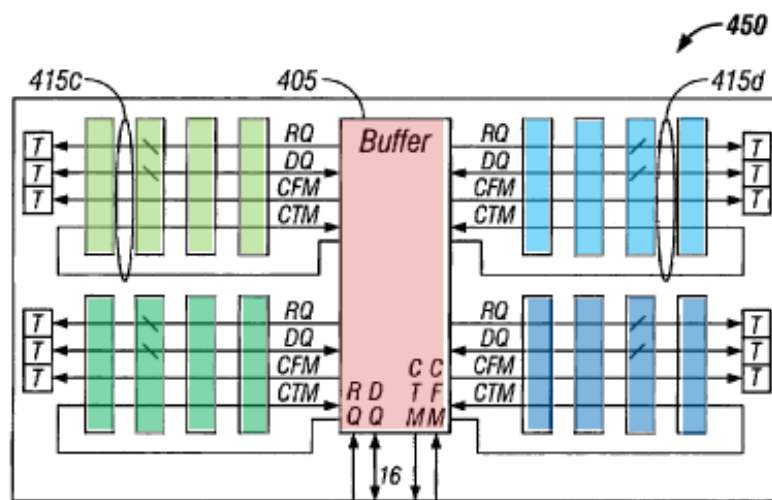


FIG. 4B

m) [1.c.1] Controller

Ground 2 discloses “a controller [e.g., including control circuitry in Perego’s buffer device 391 and Amidi’s logic and power management block below in Fig.3C] including a voltage monitor circuit [e.g., Amidi’s “voltage supervisory block 665” below in Fig.6] and nonvolatile memory [e.g., in “operations circuit

572” or an “SPD device” in Perego’s buffer device in Fig.5B], *the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to...*” EX1035, Fig.3C, 5B (below, annotated); EX1024, Fig.6 (below, annotated).

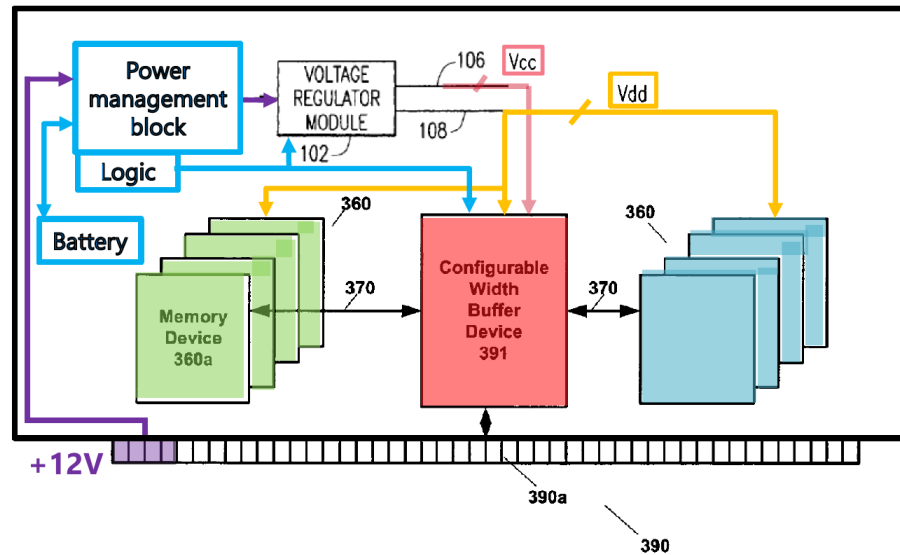
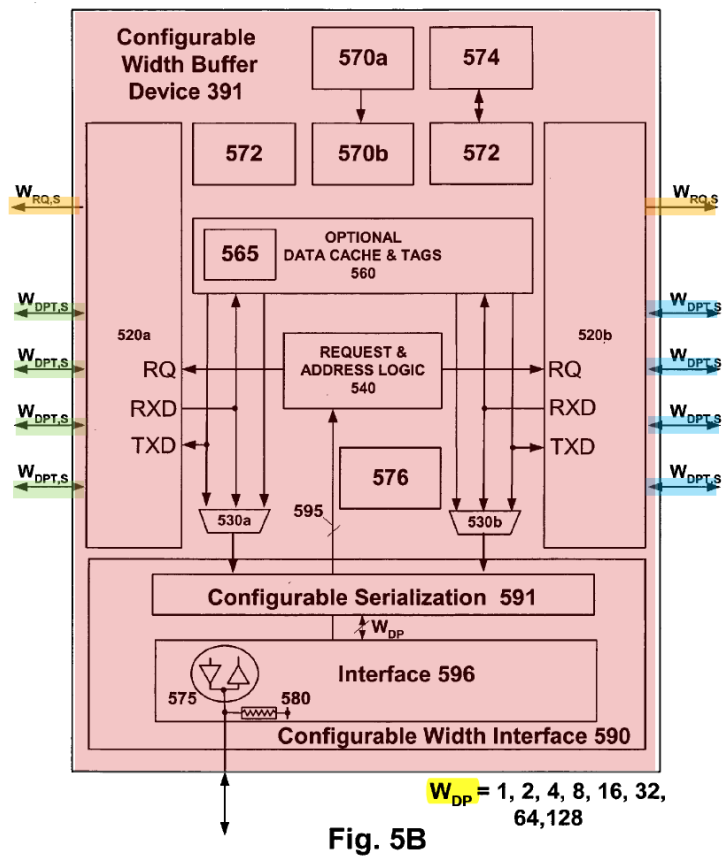


Fig. 3C



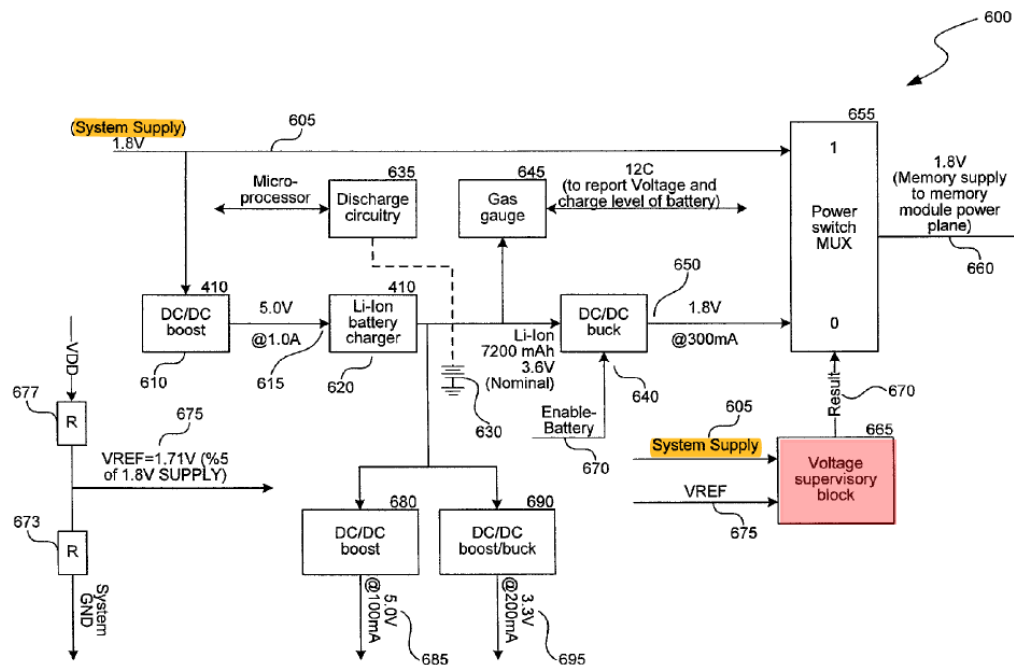


FIG. 6

For example, Perego's buffer device 391 includes “*nonvolatile memory*” in “[o]perations circuit 572...to store information used by” the buffer device “to perform configuration operations” or in “an SPD device for example, an EEPROM device.” EX1035, 15:46-16:12, Fig.5B; EX1024, 3:49-52 (“memory module 300 includ[ing]...SPD”). Further, Amidi's “voltage supervisory block 665 [in the power management block]...receives system supply 605 [+12V] and a reference voltage 675, and compares the two” to monitor the system supply voltage. EX1024, 4:44-52, Figs.6 (above), 8. The “*controller*” in the combination, included in Perego's buffer device 391 and Amidi's logic and power management block, is “*coupled to the PCB*” of the memory module and “*an input voltage supply line of*

the set of voltage supply lines” to receive and monitor a +12V of the system supply, as shown in the purple arrow in the annotated Fig.3C above. *See also* EX1024, Fig.4 (below, annotated). The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations. EX1070, 68 (“SPD is non-volatile memory”), 79 (combination discloses “detect[ing] overvoltage and generat[ing] a trigger signal in response”), 83; EX1071, 65 (similar).

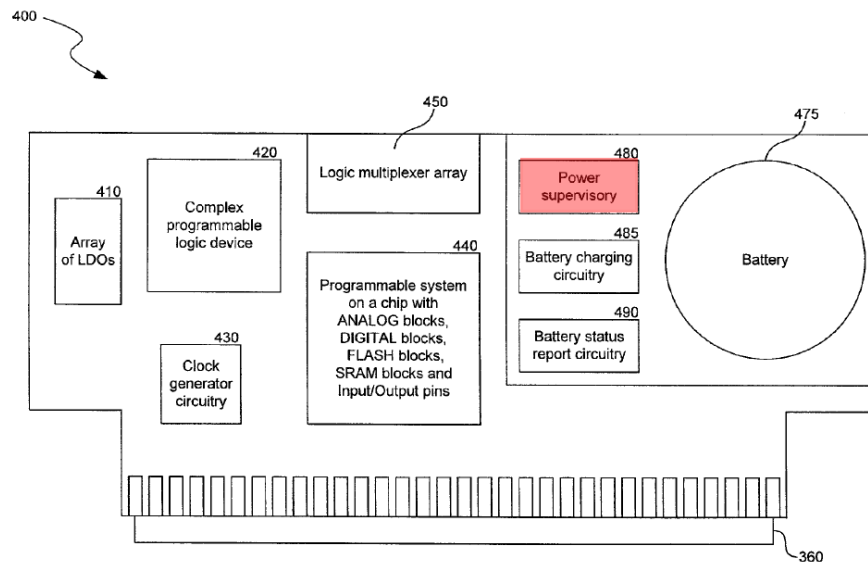


FIG. 4

n) [1.c.2] Voltage Monitor Circuit

Ground 2 discloses “*the voltage monitor circuit* [e.g., Amidi’s “voltage supervisory block 665”] *configured to: (i) monitor an input voltage* [e.g., +12V] *supplied via the input voltage supply line*” as discussed above for [1.c.1] (pp.56-60). EX1023, ¶[0012] (“12 supply pins (at +12V)”; EX1024, 4:44-46 (“voltage supervisory block 665” monitoring a system supply), Fig.6 (below, annotated).

The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations. EX1070, 79, 83; EX1071, 65.

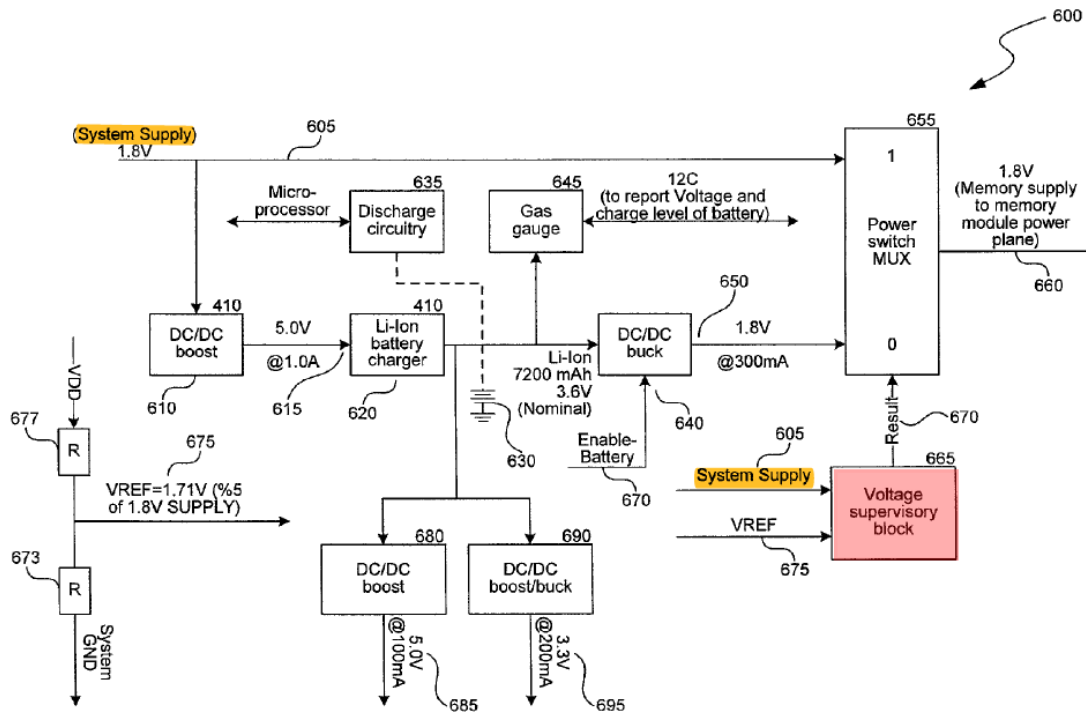


FIG. 6

o) [1.c.3] Trigger Signal

Ground 2 discloses “the voltage monitor circuit [e.g., Amidi’s “voltage supervisory block 665”] configured to:...(ii) generate a trigger signal [e.g., “signal 670 caus[ing] power switch multiplexer 655 to choose battery power 650”] upon detecting a trigger condition [e.g., “[i]f system supply 605 has a magnitude lower than reference voltage 675”]” as discussed above for [1.c.1]-[1.c.2] (pp.56-61). EX1024, 4:44-55, Fig.6 (below, annotated); EX1003, ¶186. In the combination, the voltage monitor circuit may also detect both over- and under-voltage as “a

trigger condition,” such as when the system voltage is outside “a wide tolerance” of “around +/-15%” of +12V. EX1023, ¶[0013]; EX1003, ¶187. The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations, specifically finding that the combination teaches “detect[ing] [both] overvoltage” and “undervoltage.” EX1070, 79, 83; EX1071, 65 (similar).

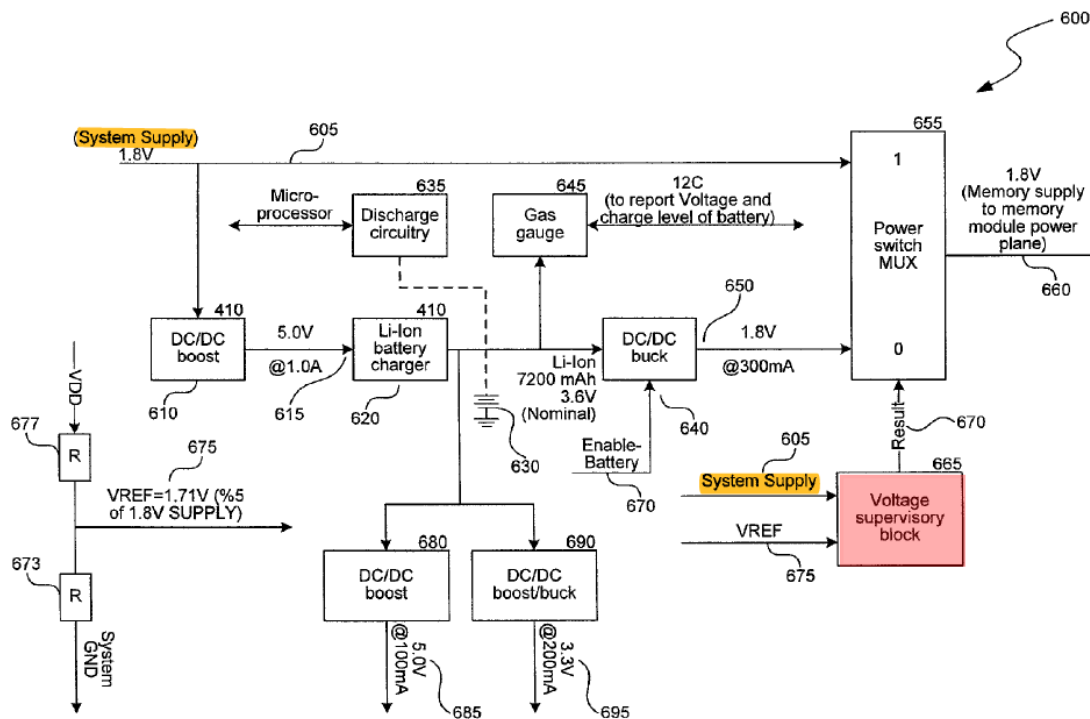


FIG. 6

p) [1.c.4] Transmitting Trigger Signal

Ground 2 discloses “the voltage monitor circuit [e.g., Amidi’s “voltage supervisory block 665”] configured to:...(iii) transmit the trigger signal [e.g., “signal 670”] to at least one other portion of the controller [e.g., to “power switch

multiplexer 655” to “cause [it] to choose battery power 650”), EX1024, 4:44-55, Fig.6 (below, annotated), as discussed above for [1.c.1]-[1.c.3] (pp.56-62).

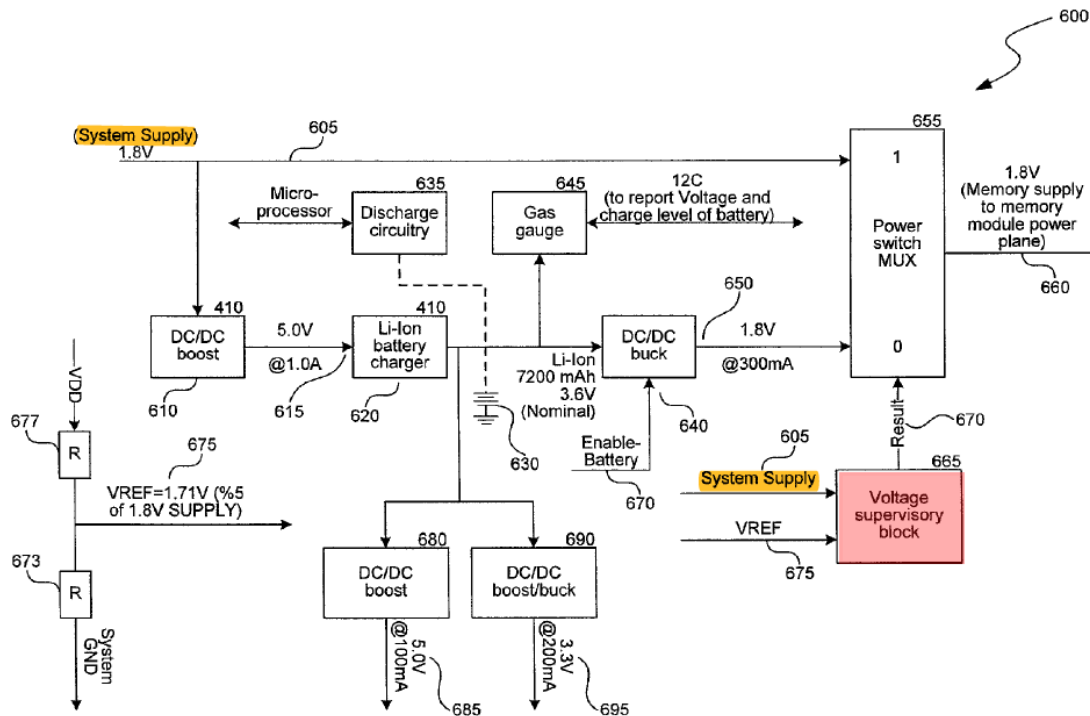


FIG. 6

q) [1.c.5] Write Operation

Ground 2 discloses “the controller is configured to perform, in response to the trigger signal [e.g., Amidi’s “signal 670” indicating a power failure], a write operation to write data [e.g., configuration/status information used for restoration, EX1024, 1:23-25, 8:62-9:2, or information about the power failure to be used for failure analysis, EX1024, 1:21-22] into the nonvolatile memory [e.g., in Perego’s “operations circuit 572” or “SPD device,” *supra* pp.56-60].” EX1003, ¶188.

Amidi teaches that, when a power failure is detected and the “*trigger signal*,” such as “signal 670,” is generated, memories on the module are put into a “self refresh state.” EX1024, 6:53-7:8, Fig.11 (finite state machine for self-refresh), Fig.14 (below, “[m]emory in self-refresh state” at 1450 after “power fault detection” at 1440), 6:40-52 (“memory module trigger[ing] SDRAM refresh operations itself”), 2:11-26 (“maintain[ing] memory (through refresh, for example)”); EX1003, ¶189.

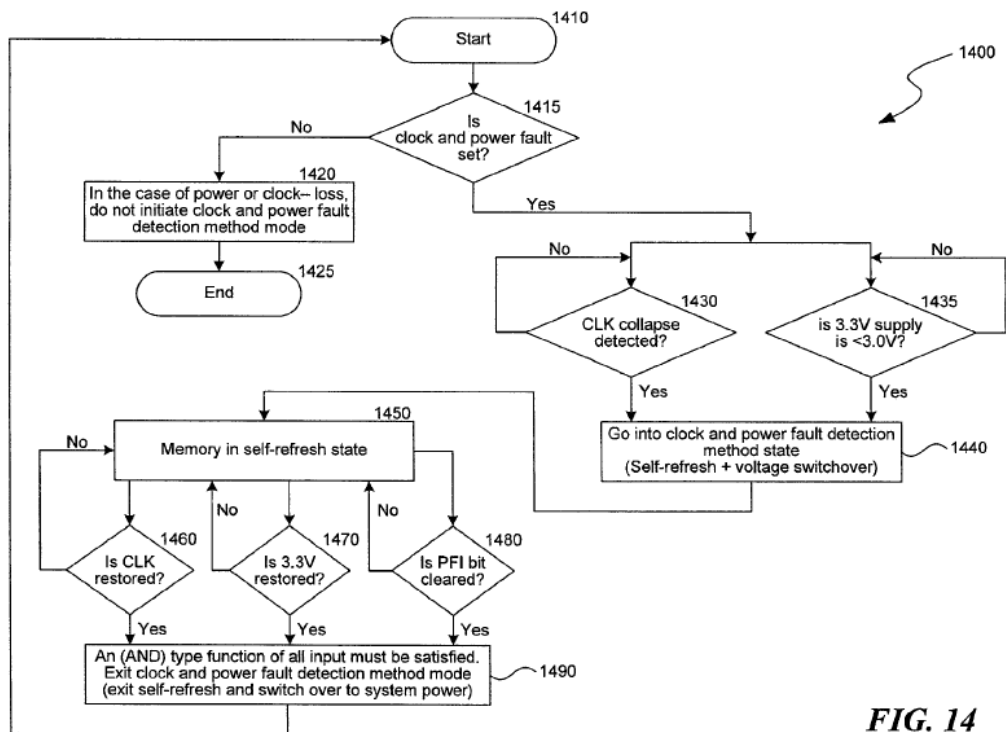


FIG. 14

Amidi’s self-refresh mode is also known as the “S3 sleeping state” used in Harris’s “standard FBD [Fully Buffered DIMM] module.” EX1023, ¶[0012]; EX1027, 39 (“S3 is an ACPI mode in which...DRAMs [are] in self refresh

mode”); EX1109 (ACPI), 229 (S3 “[p]lacing the memory into a low-power...self-refresh state”); EX1003, ¶190. Amidi further teaches the memory module restarts normal operations once the power is restored and storing “some data may be useful for restarting a system after a failure.” EX1024, 1:23-25, Fig.15 (below), 8:62-9:2 (“Process 1500 includes...detecting potential restoration, checking whether a system is ready, and restoring control to the system.”); EX1109 (ACPI), 229 (“the pre-sleeping state or initial boot state configuration in a non-volatile memory area...to enable it to restore the values during the waking process”); EX1003, ¶191.

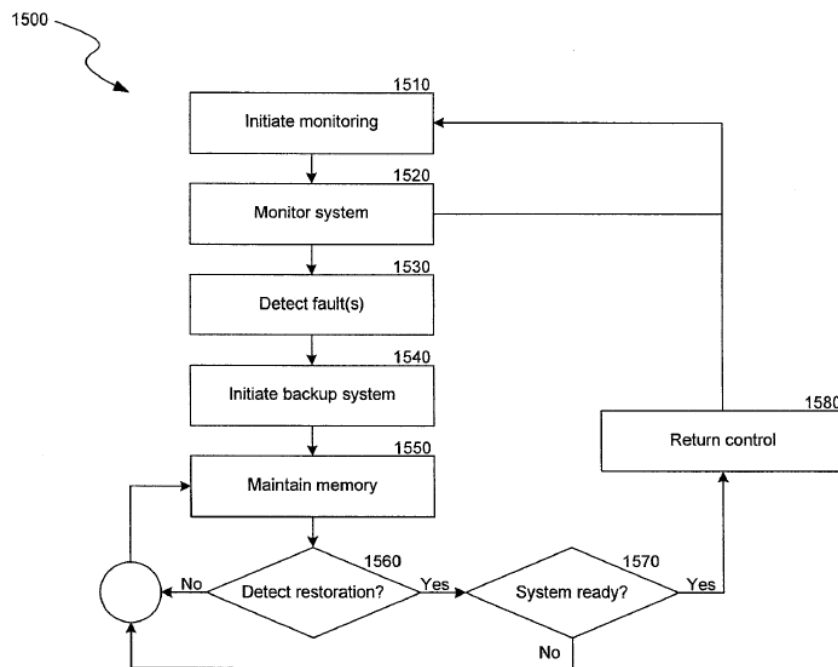


FIG. 15

Harris’s standard FBDIMM also requires that S3 recovery information “should be stored in non-volatile memory before entering S3 mode and restored before normal

DRAM transactions begin.” EX1027, 25, 141 (“copy[ing] these registers into some form of stable storage prior to system standby”); EX1003, ¶192. Further, Perego discloses parameters required to restore system control, such as “the desired width of configurable width interface 590, and...one or more of interfaces 520a and 520b.” EX1035, 16:13-21; EX1003, ¶192. Thus, Ground 2 teaches that Amidi’s data retention and restoration operation “*in response to the trigger signal*” is generated as a result of a power failure, and includes “*a write operation to write*” configuration information “*into the nonvolatile memory,*” e.g., Perego’s “operations circuit 572” or “SPD device,” *supra* pp.56-60, so that the information is used to restore the normal operation after the power failure. EX1003, ¶193. Ground 2 further teaches that “information about the state of a system” can also be written into a nonvolatile memory “after a failure occurs” to make “failure analysis...much simpler,” EX1024, 1:21-22, as was common at the time. *See, e.g.,* EX1025, ¶¶[0038] (“[a]n EEPROM 210...to store various status indicators and counters, which may be utilized during operations”), [0042] (“an EEPROM that contains various status indicators”); EX1003, ¶193. The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations. EX1070, 80-81 (finding the combination discloses the “logic element writes information into the non-volatile memory in response to the trigger signal”); EX1071, 61-63 (similar); EX1003, ¶194.

r) [1.c.6] Trigger Condition

Ground 2 discloses “*the trigger condition occurs when the input voltage exceeds a first threshold voltage [e.g., +15% above 12V]*” as discussed above for [1.c.1]-[1.c.5] (pp.56-66); *see also, e.g.,* EX1023, ¶[0013] (“a wide tolerance (e.g., around $\pm 15\%$)” of the system supply 12V). The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations. EX1070, 79 (Harris’s disclosure of “+12V power supply [with] a tolerance of ‘ $\pm 15\%$ ’” and Amidi’s concern with “‘power fault[s]’” teach “detect[ing] overvoltage and generate a trigger signal in response to the detection”), 83; EX1071, 65 (similar).

s) [1.d.1] DDR SDRAM

Ground 2 discloses “*a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices [e.g., Perego’s memory devices 360 in Figs. 3A-3C and 410 in Figs. 4A-4C] coupled to the set of address and control lines [e.g., RQ address/control lines, *supra* pp.55-56] and to the set of data lines [e.g., DQ data lines, *supra* pp.54-55].*”

Perego discloses memory devices 360 “*coupled to the PCB*” of the memory module. EX1035, Figs.3C, 4A-4B (below), 7:30-34 (“memory devices 360”), 9:26-32 (“buffered memory modules...includ[ing]...a plurality of memory devices

410a-410h.”); *supra* pp.45-47. The memory devices are also coupled to the RQ address/control lines and to the DQ data lines. *Id.*; *see also id.*, 9:43-49 (“Channels 415a and 415b...coupled to...memory devices” “include control lines (RQ), [and] data lines (DQ).”), 9:58-60 (“[C]ontrol lines (RQ) may comprise...row address strobe, column address strobe, etc., and address lines.”).

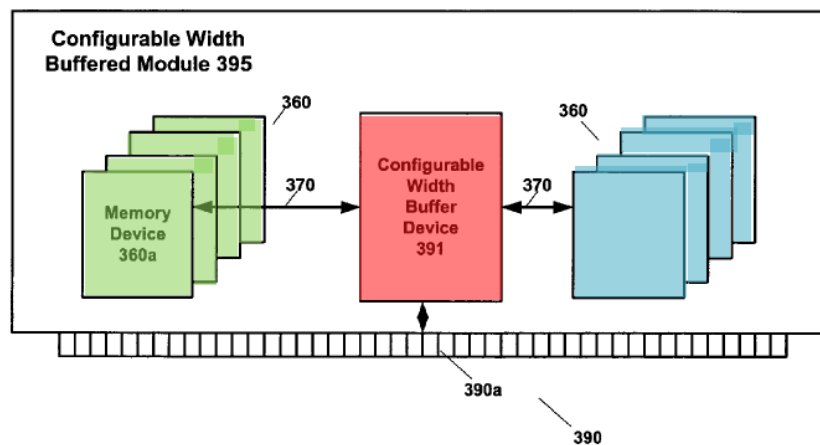


Fig. 3C

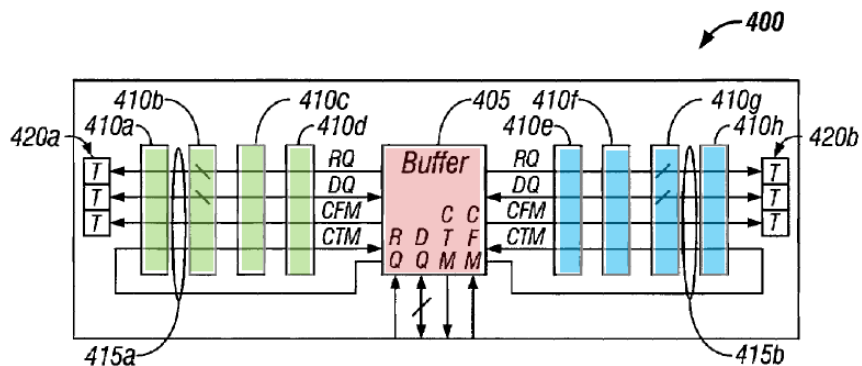


FIG. 4A

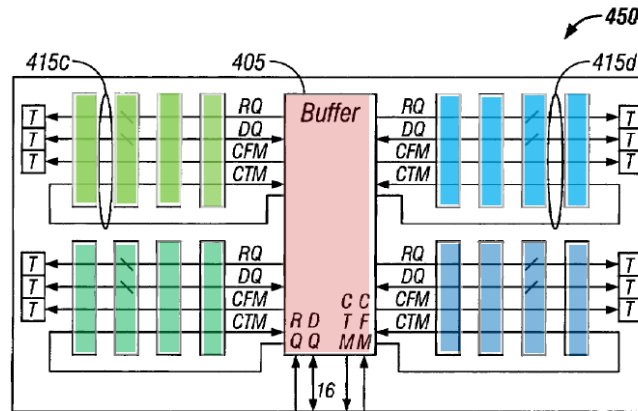


FIG. 4B

Perego, Harris, and Amidi further disclose “double data rate (DDR) [SDRAM]” memory devices. EX1035, 4:2-3, 8:1-4 (“DDR memory devices”), 10:54-59 (“(DDR2) DRAM devices and Synchronous DRAM (SDRAM) devices”); EX1023, ¶[0009] (“Double Data Rate (DDR)...(DRAM) device”); EX1024, Claim 4 (“DDR2 SDRAM”); *see also* EX1045, Cover (“(DDR) SDRAM”); EX1026, Cover-1 (“DDR2 SDRAM”).

t) [1.d.2] Receiving or Outputting Data

Ground 2 discloses “the DDR SDRAM devices being operable to receive or output data signals [e.g., “stor[ing]” and “retriev[ing]” data, EX1035, 3:64-65] via the set of data lines [e.g., DQ data lines, *supra* pp.54-55] based on address and control signals [e.g., “associated with a particular address provided...as part of a write or read command,” EX1035, 3:65-66] received from the system board via the set of address and control lines [e.g., RQ address/control lines, *supra* pp.55-56].”

See also EX1035, 3:66-4:12 (“SDRAM (DDR)...decodes request and address information [for]...transmitting and receiving data.”). EX1003, ¶195.

As Perego teaches, receiving and outputting data based on address/command signals were typical write and read operations of DDR DRAMs at the time.

EX1026, 20-30 (DDR2 SDRAM receiving/outputting data based on write/read command/address), Fig.20 (below, Bank activate with row address followed by Read command with column address), Fig.21 (below, data being transferred for read/write commands); EX1003, ¶195.

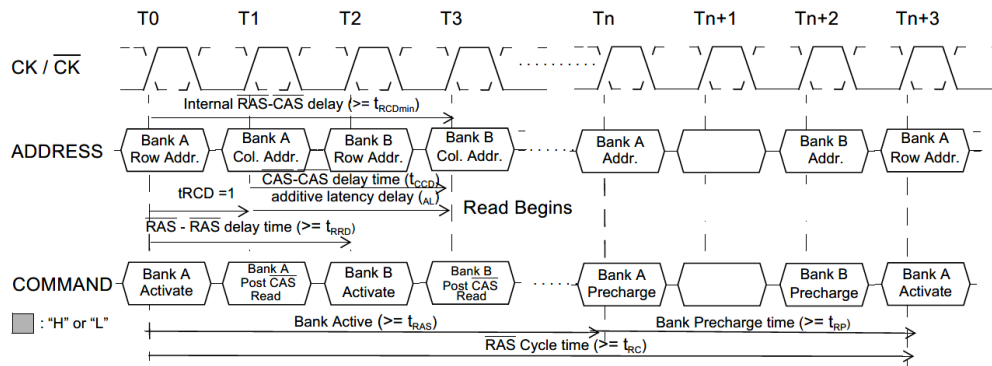
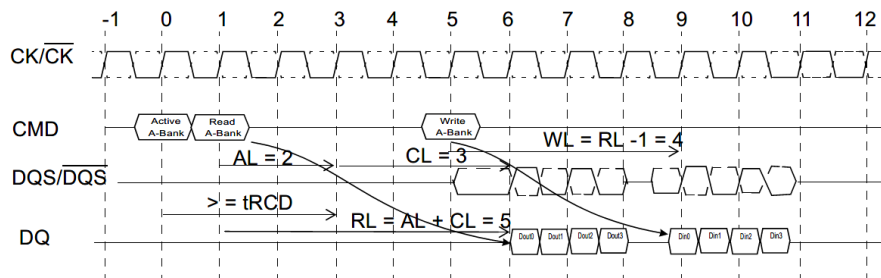


Figure 20 — Bank activate command cycle: $t_{RCD} = 3$, $AL = 2$, $t_{RP} = 3$, $t_{RRD} = 2$, $t_{CCD} = 2$



$$[AL = 2 \text{ and } CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]$$

Figure 21 — Example 1: Read followed by a write to the same bank, where $AL = 2$ and $CL = 3$, $RL = (AL + CL) = 5$, $WL = (RL - 1) = 4$, $BL = 4$

Perego also discloses the DDR SDRAMs “receive[] control, and address information from [the system] controller 310” for read/write operations “via [RQ address/control lines in] channels 370” and communicate “data” accordingly “via [DQ data lines in] channels 370.” EX1035, 6:12-27, Fig.3B (below); EX1003, ¶196.

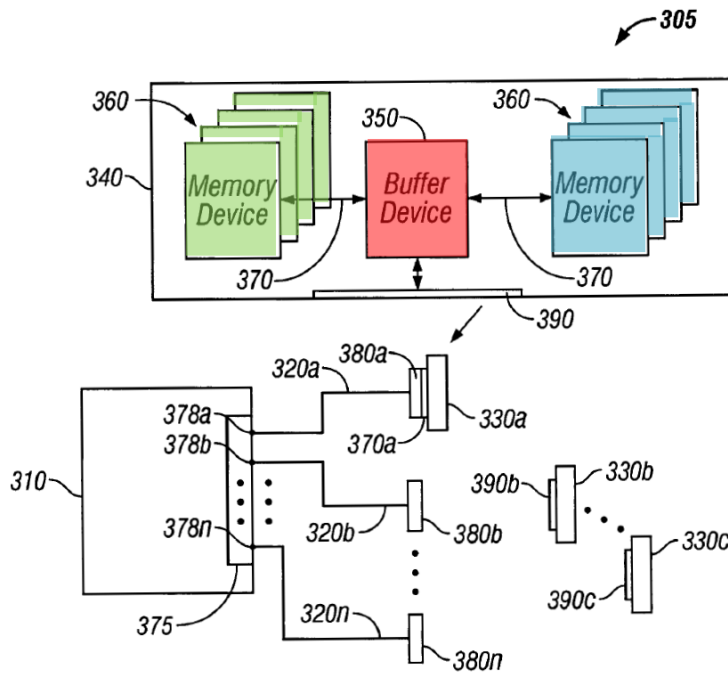


FIG. 3B

u) [1.e] Converter Circuits

Ground 2 discloses “first, second, third, and fourth converter circuits [e.g., in Harris’s Voltage Regulator Module 102 in Fig.3C below] coupled to the PCB and to the input voltage supply line [e.g., purple line in Fig.3C providing +12V input supply], and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines

[e.g., for delivering, respectively, (i) V_{dd} to the memory devices 360 and to the buffer device 391 in Fig.3C, (ii) V_{cc} to the buffer device 391 in Fig.3C, (iii) V_{tt} to on-board “termination elements 420” in Fig.4A below, and (iv) V_{DDSPD} to the non-volatile memory in “operations circuit 572” or SPD in the buffer device 391 as shown in Fig.5B].” EX1035, Figs.3C, 5B, 4A (below, annotated); *supra* pp.25-35; EX1003, ¶197.

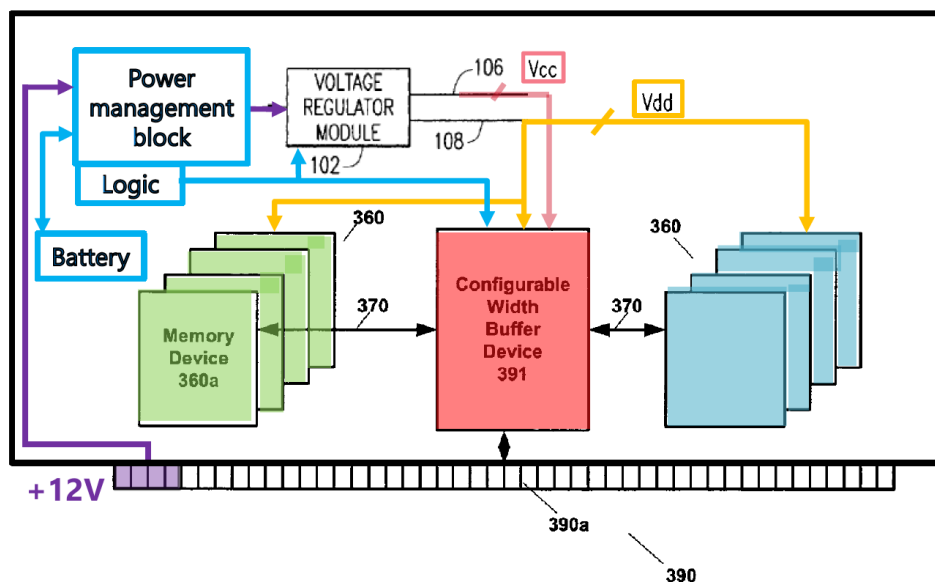
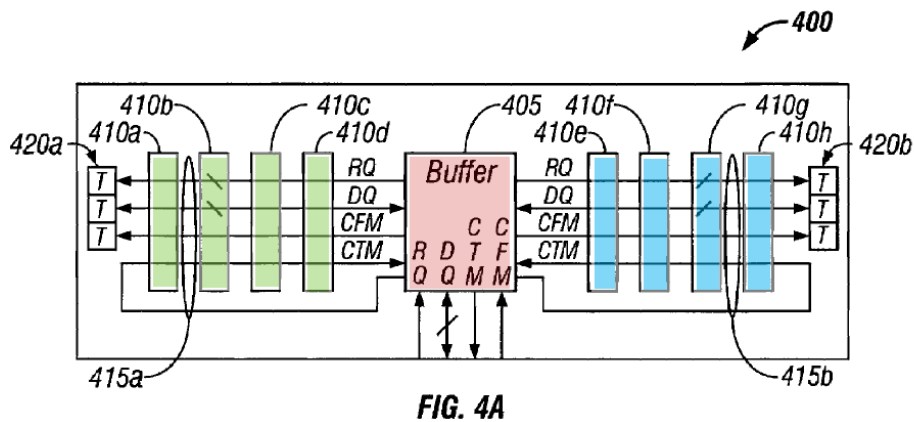
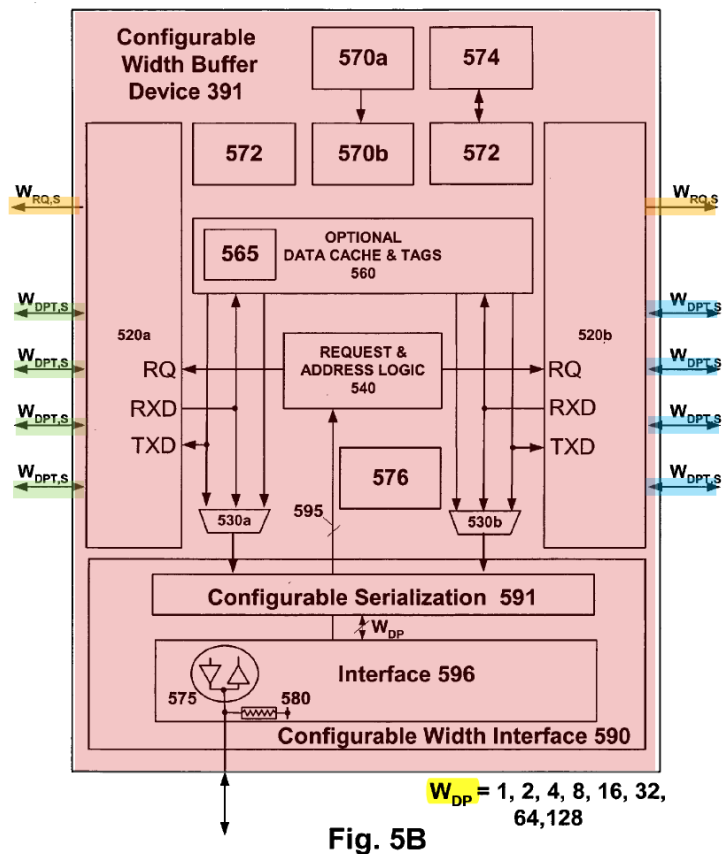


Fig. 3C



Harris teaches “at least one on-board voltage regulator module” (“VRM 102”), including “*converter circuits coupled to the PCB,*” which receive and “convert[] an externally supplied voltage level,” such as +12V, “into appropriate

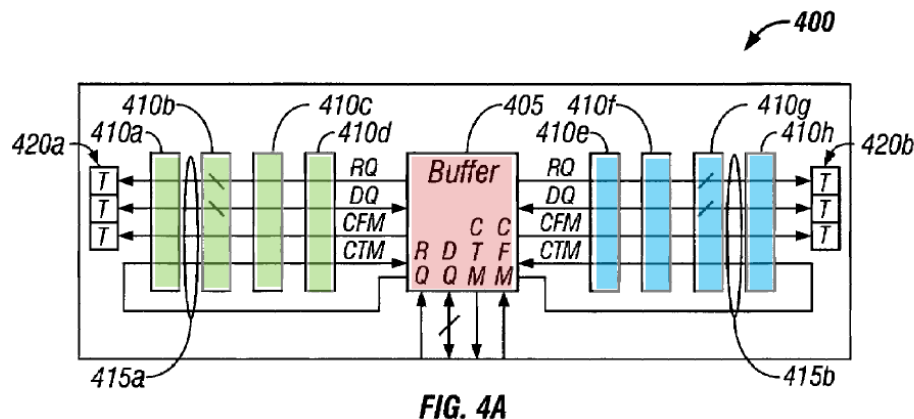
local voltage levels” for various components on the module. EX1023, ¶[0010]; EX1003, ¶198.

First, the VRM provides “appropriate voltage levels” to the memory devices, like “DDR2” SDRAM “operable with 1.8 V,” via “a first voltage path 108, typically referred to as a V_{dd} path.” EX1023, ¶[0009]; EX1035, 10:56-59 (“DDR2” “(SDRAM) devices”). Thus, in Ground 2, the “ V_{dd} path” would include “*first...regulated voltage lines*,” and the VRM would include a “*first...converter circuit*” converting the +12V input voltage to a regulated voltage V_{dd} (1.8V for DDR2) to power memory devices. EX1003 ¶198. Perego’s buffer would also receive the on-board regulated V_{dd} to communicate with the memory devices. See EX1023, ¶[0002] (explaining the need to power buffer devices using an on-board supply voltage); EX1003, ¶198.

Second, the VRM also provides “appropriate voltage levels” to “the buffer component 112” via “a second voltage path 106, typically referred to as a V_{cc} path.” EX1023, ¶[0009]. Perego also discloses a “buffer device 405,” similar to Harris’s, which interfaces between memory devices on the module and the system controller. See, e.g., EX1035, 10:54-67; EX1003, ¶199. Thus, in Ground 2, Harris’s “ V_{cc} path” would include “*second...regulated voltage lines*,” and the VRM would include a “*second...converter circuit*” converting the +12V input

voltage to a regulated voltage V_{cc} as required to power the specific implementation of Perego's buffer device and memory controller interface. *Id.*

Third, Perego also discloses "termination elements 420a and 420b," EX1035, Fig.4A (below), 9:34-38, "connect[ed] to a termination voltage, such as...a reference voltage," *id.*, 9:1-12. Thus, in Ground 2, Harris's VRM further includes a "*third...converter circuit*" to provide the proper "termination voltage" (e.g., V_{tt}) for Perego's termination elements via "*third...regulated voltage lines*," consistent with the Board's previous findings. EX1070, 34-38; EX1071, 30-34; EX1026, 9 (applying V_{tt} during power-up), 49 (V_{tt} set to 0.9V, a half of DDR2 operating voltage, 1.8V); EX1003, ¶200.

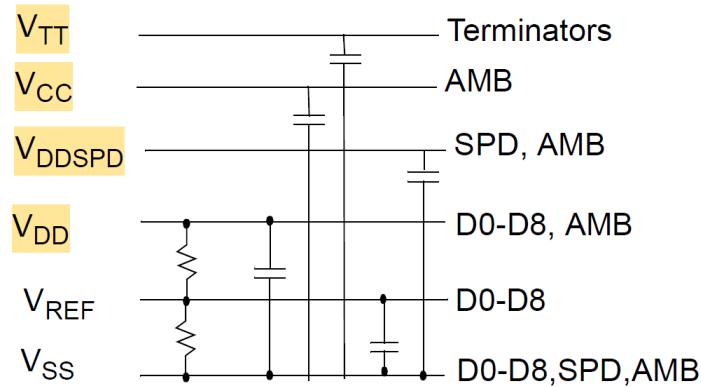


Fourth, as discussed above for [1.c.1] (pp.56-60), Perego's buffer device includes non-volatile memory in the "operations circuit 572" or "SPD device." EX1035, 15:46-16:12. Such non-volatile memory in SPD also requires a proper supply voltage (e.g., V_{DDSPD}) for its operations, such as writing configuration

information, as discussed above for [1.c.5] (pp.63-66). EX1027, 32 (V_{DDSPD} of 3.3V powering SPD devices); EX1003, ¶201. Thus, in the memory module under Ground 2, Harris's VRM further includes a “*fourth...converter circuit*” to power the non-volatile memory in Perego's buffer device via “*fourth...regulated voltage lines*.” *Id.*

In sum, the memory module under Ground 2 requires at least four separate regulated voltages V_{dd} , V_{cc} , V_{tt} , and V_{DDSPD} to power four separate components—the memory devices, buffer device, termination elements, and nonvolatile memory—respectively, similar to the supply voltage requirements of FBDIMM disclosed by Harris which is similar to Perego's buffered memory module. EX1023, ¶[0009] (“fully buffered DIMMs (FBDs)”); EX1027, 32 (FBDIMM requiring V_{dd} , V_{cc} , V_{tt} , and V_{DDSPD}); EX1028, 9 (below annotated, listing required voltages for FBDIMM), 13 (below annotated, showing power line connections); EX1003, ¶202.

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD} / V_{DDQ} , AMB V_{DDQ})
	1.455 ¹	1.5	1.575 ¹	(AMB V_{CC} / V_{CCFBD})
	$0.453 \cdot V_{DD}$	$0.5 \cdot V_{DD}$	$0.547 \cdot V_{DD}$	(DRAM Interface V_{TT}) This supply should track as $0.5 \cdot 1.8$ volt supply
	3.0	3.3	3.6	(V_{DDSPD})



Accordingly, Harris's VRM implemented on the memory module includes at least four “*converter circuits to receive power from the input voltage supply line [e.g., +12V] and to deliver*” “appropriate voltage levels” (V_{dd} , V_{cc} , V_{tt} , and V_{DDSPD}) to those four components via four separate “*regulated voltage lines.*” EX1003, ¶202. The Board has also found that Harris's VRM implemented on an FBDIMM (similar to Perego's buffered module) includes at least four converter circuits to provide the four respective regulated voltages, and the Board's reasons apply equally to the combination of Harris and Perego. EX1070, 24-41, 56-59; EX1003, ¶203.

v) [1.f.1]-[1.f.2] First Component

Ground 2 discloses “*wherein the set of components includes: a first component [e.g., Perego's or Harris's DDR2 memories] configured to receive power [e.g., V_{dd}] via at least the first regulated voltage line*” for the reasons discussed above for [1.e] (pp.71-77). EX1035, Fig.3C (below, annotated), 10:54-

67 (“DDR2”); EX1023, ¶[0009] (“a first voltage path 108, typically referred to as a V_{dd} path”).

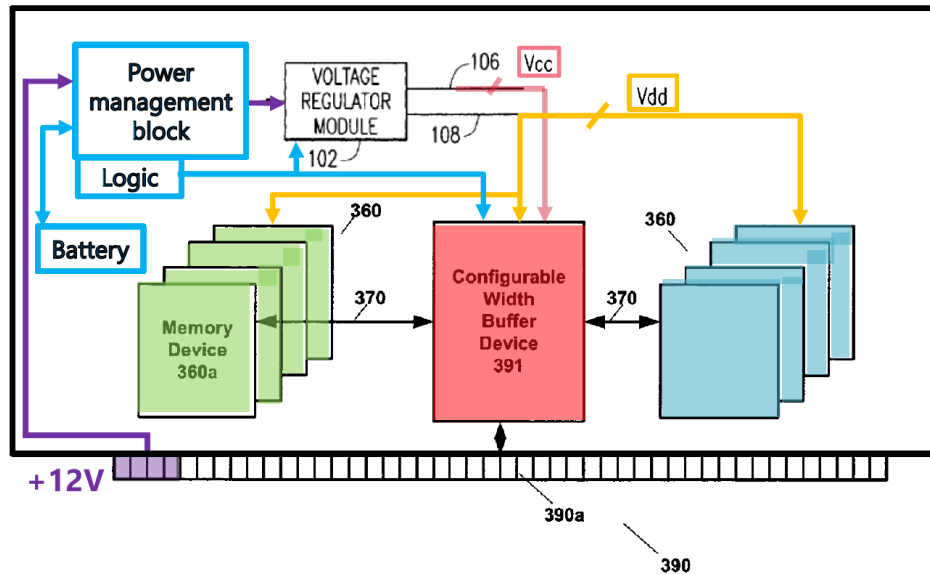


Fig. 3C

w) [1.f.3] Second Component

Ground 2 discloses “a second component [e.g., Perego’s buffer device] configured to receive power [e.g., V_{cc}] via at least the second regulated voltage line” for the reasons discussed above for [1.e] (pp.71-77). EX1035, Fig.3C (below, annotated); EX1023, ¶[0009] (“a second voltage path 106, typically referred to as a V_{cc} path”).

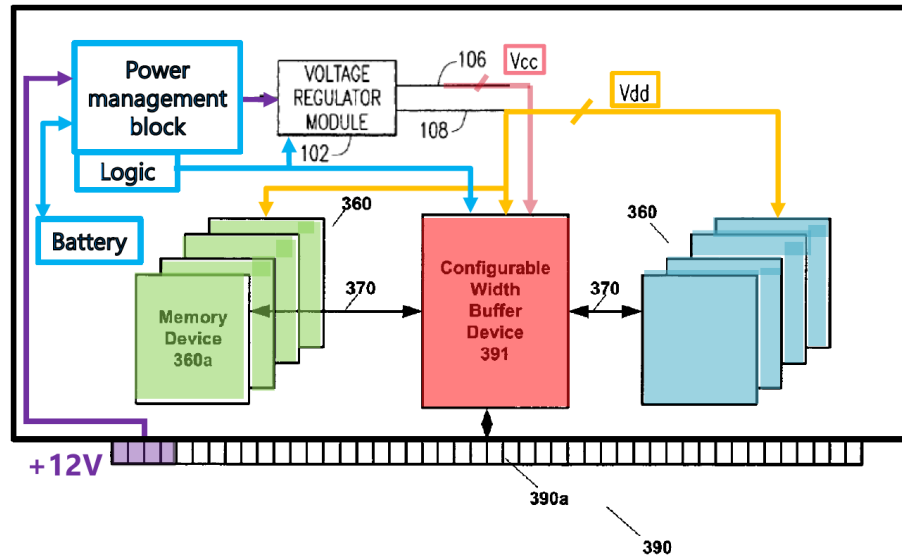


Fig. 3C

x) [1.f.4] Third Component

Ground 2 discloses “a third component [e.g., Perego’s “termination elements” 420a-b] configured to receive power [e.g., V_{tt}] via at least the third regulated voltage line” for the reasons discussed above for [1.e] (pp.71-77).

EX1035, Fig.4A (below, annotated), 9:3-12 (“terminator(s) connect to a termination voltage...such as a reference voltage”).

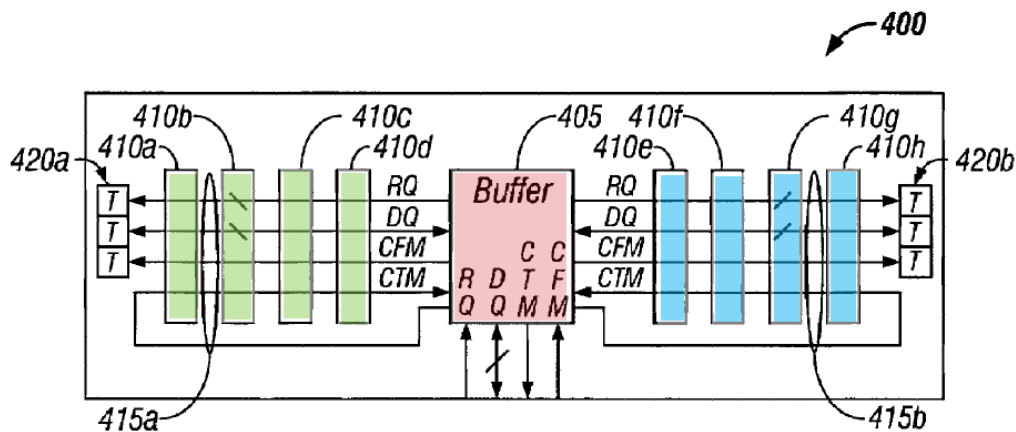


FIG. 4A

y) [1.f.5] Fourth Component

Ground 2 discloses “a fourth component [e.g., Perego’s “operations circuit 572” or “SPD device”] configured to receive power [e.g., V_{DDSPD}] via at least the fourth regulated voltage line” for the reasons discussed above for [1.e] (pp.71-77). EX1035, Fig.5B (below).

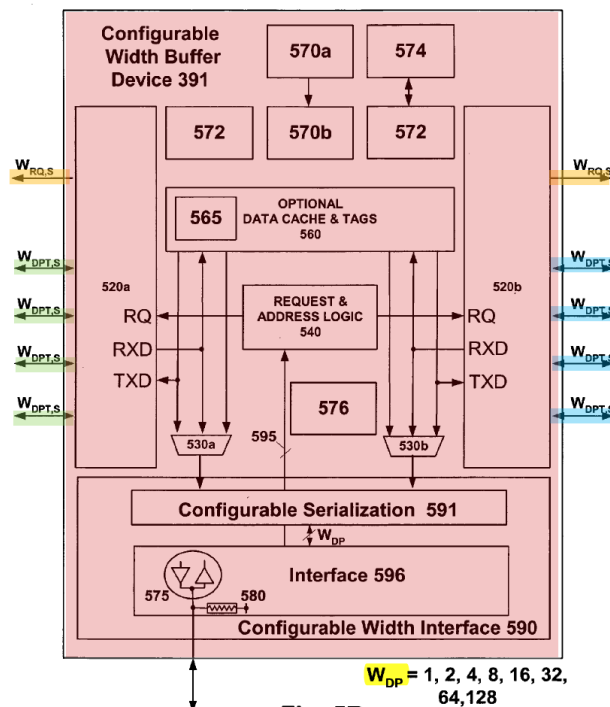


Fig. 5B

z) [1.g.1]-[1.g.2] Electrical Connection

Ground 2 discloses “wherein each component of the set of components: (i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines [e.g., to receive power]” for the reasons discussed above for [1.e], [1.f.1]-[1.f.5] (pp.71-80).

aa) [1.g.3] Receiving Power

Ground 2 discloses “each component of the set of components...(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines” for the reasons discussed above for [1.e], [1.f.1]-[1.f.5] (pp.71-80). For example, in Ground 2, Harris’s VRM is the only power source for “each component of the set of components” via the respective “regulated voltage lines.” *Supra* pp.25-35; EX1035, Fig.3C (below); EX1023, ¶¶[0011] (“V_{dd} and V_{cc} power supply rails...independent from external voltage sources”), [0013] (“+12V power supply...not used directly by DRAM devices or buffer/logic components”), [0020].

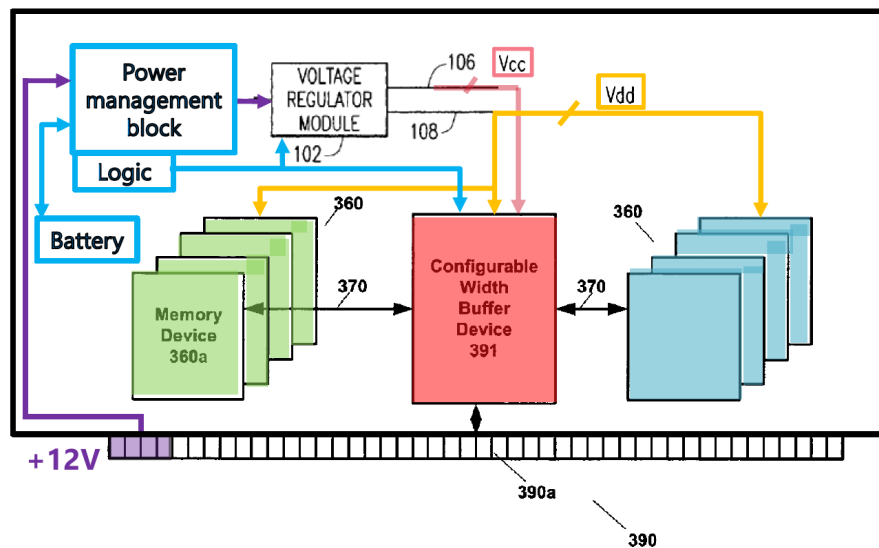
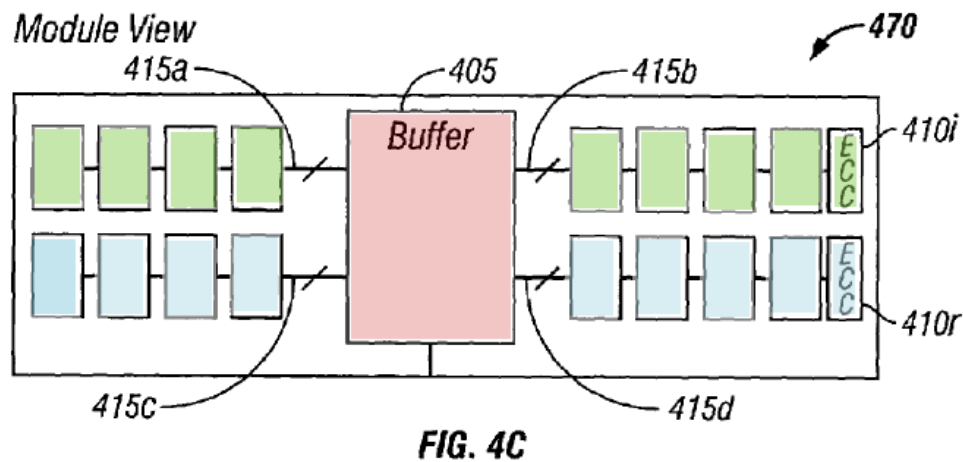


Fig. 3C

bb) [1.h.1]-[1.h.2] First Group of DDR SDRAM

Ground 2 discloses “wherein the plurality of DDR SDRAM devices includes: a first group of at least five DDR SDRAM devices [e.g., five memory devices in

channel 415b or 415d below in Fig.4C] *that are each connected to a first chip select line configured to electrically conduct a first chip select signal* [e.g., to select memory devices in the channel for read/write operations].” EX1035, Fig.4C (below), 21:16-20 (“Any number of channels 415a-415d [can be selected and]...may transfer information simultaneously.”); EX1003, ¶204.



Perego explains “[i]n a normal memory read operation,” the DDR2 memory devices receive signals corresponding to “control, and address information” from the system controller “via channels” 415. EX1035, 6:15-19; 10:54-59. For DDR2, the “corresponding signals” include a “*chip select signal*” to select memory devices to perform read/write operations, as taught by Amidi. EX1024, 7:55-56 (“DDR2”), Fig.13 & n.4 (“Write” and “Read” commands require “CS” chip-select signal asserted Low); EX1026, 6 (“CS [Chip Select]...considered part of the command code”), 46-47 & n.1 (Command truth table including chip select (CS) signal for read/write operations); EX1107, 2-3 (“chip-select...is essential”);

EX1003, ¶205. “One or more of memory devices 360 [selected by the CS signal in a given channel] may respond [to the read/write command] by transmitting [receiving] data.” EX1035, 6:19-24. Given Perego’s channel 415b or 415d includes at least five memory devices (as shown in Fig.4C above) selected together by a chip select signal, Ground 2 discloses this limitation. EX1003, ¶206.

cc) [1.h.3] Second Group of DDR SDRAM

Ground 2 discloses “a second group of at least four DDR SDRAM devices [e.g., four memory devices in channel 415a or 415c below in Fig.4C] that are each connected to a second chip select line configured to electrically conduct a second chip select signal [e.g., to select memory devices in the channel for read/write operations]” for the reasons discussed above for [1.h.1]-[1.h.2] (pp.81-83). EX1035, Fig.4C (below), 6:15-24, 21:16-20.

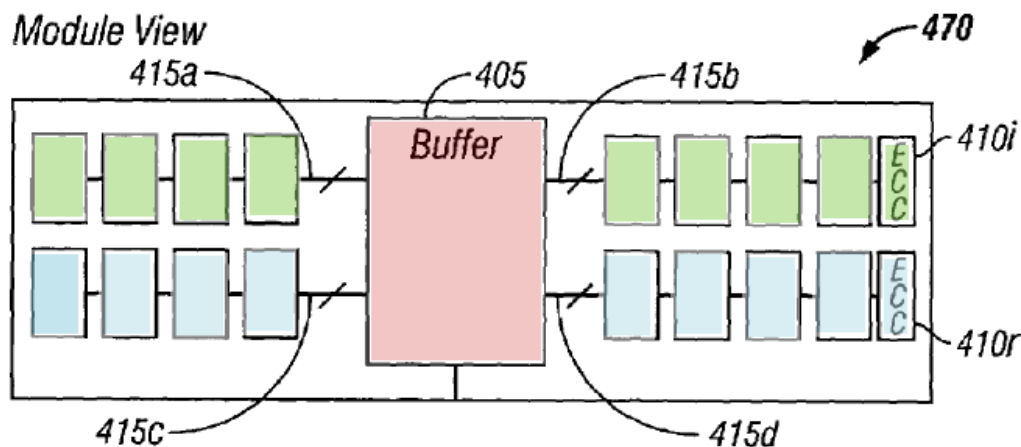


FIG. 4C

dd) [1.i.1] Not in Self-Refresh Mode

Ground 2 discloses “*when [+12V] power from the power rails of the system board is provided to the DIMM [in normal mode when the system power is available] and each group of the first and second groups of DDR SDRAM devices is [being normally accessed or in “a ready or standby state,” EX1035, 21:16-20, and thus] not in self-refresh mode [which is used when the system power is not available, EX1024, Fig.14, as explained above for [1.c.5] (pp.63-66)].*” EX1003, ¶207.

For example, Amidi discloses that “[d]uring normal operation...with proper power” provided, the DIMM operates according to the “system control and command bus input.” EX1024, 7:35-38; EX1003, ¶208. Amidi teaches putting memory devices into self-refresh mode only when the power or clock fails, as discussed above for [1.c.5] (pp.63-66). EX1024, Fig.14 (below right at 1435); EX1003, ¶208.

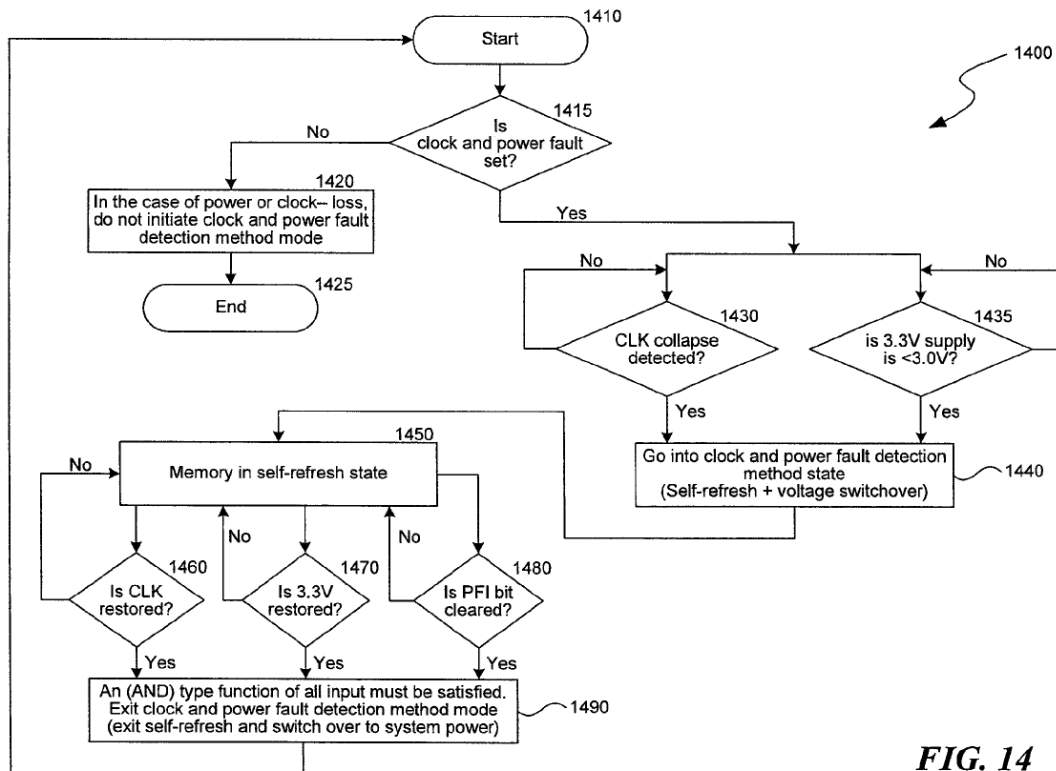
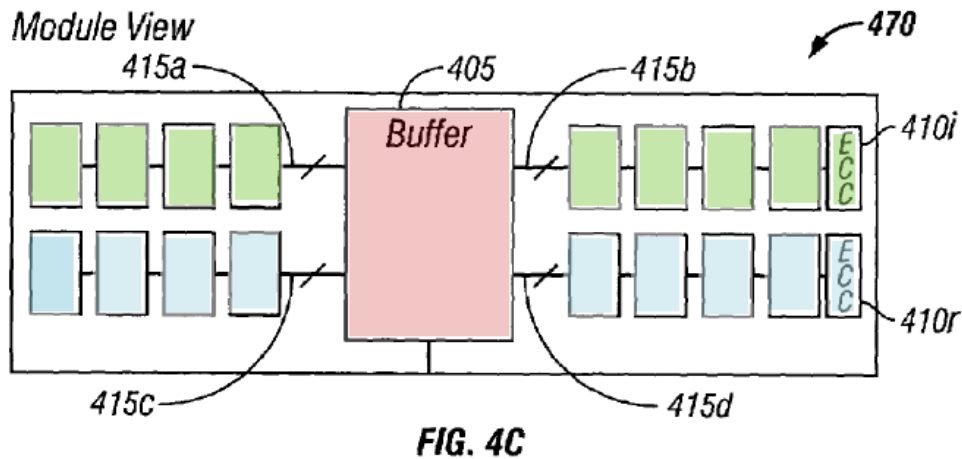


FIG. 14

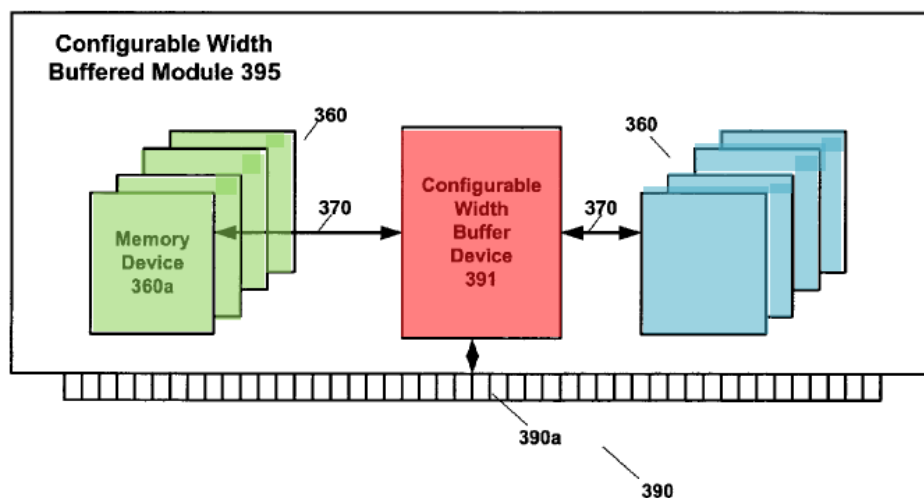
Perego also discloses that, during normal operations where the DIMM receives the system power, selected memories operate based on control/address signals, and unselected ones “remain in a ready or standby state.” EX1035, 21:16-20. The “ready or standby state” is different from the self-refresh mode, which disables all but the CKE input (thus preventing normal read/write commands) and requires a sequence of commands to exit from. EX1026, 6, 16, 39, 68; EX1003, ¶209. Thus, Ground 2 teaches that, during normal operations, the DIMM receives “power from the power rails of the system board” and “DDR SDRAM devices” are “not in self-refresh mode.” *Id.*

ee) [1.i.2] First Group of DDR SDRAM Enabled

Ground 2 discloses, during normal operations, “*the first group of DDR SDRAM devices [e.g., including 5 memory devices in channel 415b or 415d in Fig.4C below] is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines [e.g., when each of the 5 memory devices in one channel is 8-bits wide, including four x8 memories for data and one x8 memory for ECC] independently of whether the second group of DDR SDRAM devices [e.g., including 4 memory devices in channel 415a or 415c in Fig.4C] is enabled, in response to the second chip select signal, to receive or output an integer number of [e.g., 32 = 4 memories each 8-bits wide] 1-bit DDR data signals in parallel via an integer number of [e.g., 32=4x8] data lines of the set of data lines [e.g., when each of the 4 memory devices in one channel is 8-bits wide]” for the reasons discussed for [1.h.1]-[1.h.3] (pp.81-83), and further discussed below. EX1035, Fig.4C (below), 10:48-53 (“memory devices 410i and 410r intended for ECC”); EX1003, ¶210.*



Perego discloses that “[a]ny number of channels 415a-415d, for example...two channels 415c and 415d may transfer information simultaneously and...the other two channels 415a and 415b remain in a ready or standby state.” EX1035, 21:16-20; *see also id.*, 6:15-24 (buffer device 391 receiving “data via one...of channels 370 and in response, transmit[ing] corresponding signals to [the memory] controller”), Fig.3C (below).



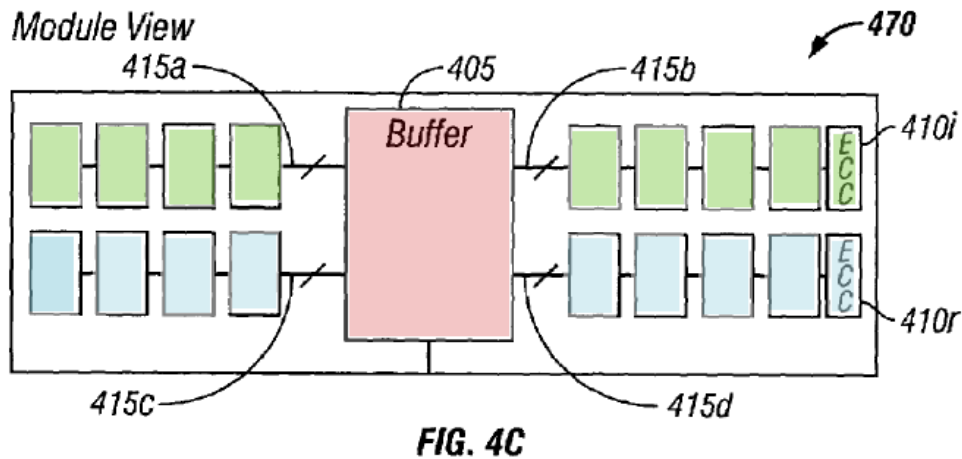
Thus, Perego teaches that the memory devices in each of the channels are enabled to output/receive data in response to read/write commands independent of whether the memory devices in another channel are enabled or not. EX1003, ¶¶211-212. Also, as discussed above for [1.h.1]-[1.h.3] (pp.81-83), the memory devices are enabled in response to chip-select signals for read/write operations.

Perego further discloses that each of the memory devices can be 8-bits wide (“x8”), EX1035, 14:10-15, as standardized, EX1026, 2 (x8 DDR2 SDRAM), 7-8. EX1003, ¶213. Accordingly, when the **five 8-bit wide** memory devices in *e.g.*, channel 415b or 415d (in FIG.4C above), are enabled to output data by the “*first chip select signal*,” they provide a total of “40 [=5x8] 1-bit DDR data signals in parallel.” *Id.* Similarly, when the **four 8-bit wide** memory devices in channel 415a or 415c (in FIG.4C), are enabled to output data by the “*the second chip select signal*,” they provide “an integer number [32=4x8] of 1-bit DDR data signals in parallel.” *Id.* In the implementation where “two channels 415c and 415d...transfer information simultaneously,” the total number of data bits received by the buffer device is 72 (=40+32). EX1035, 21:16-20; EX1003, ¶214. Perego also discloses that “Memory Device Access Width” (W_A) can be the same as “Buffer Device Interface Width (W_{DP}), which corresponds to one-to-one serialization ratio ($R_S=W_A:W_{DP}$). EX1035, 14:32-51, 17:26-28 (“[T]he serialization ratio is 1:1.”); EX1003, ¶214. For example, when channels 415c

(with four x8 memories) and 415d (with five x8 memories) are accessed simultaneously, the 40 bits of data from channel 415d are output to the controller “*via at least 40 data lines of the set of data lines,*” and the 32 bits of data from channel 415c are output to the controller “*via an integer number [32] of data lines of the set of data lines*”—a total of 72 data lines. EX1003, ¶214; EX1035, Fig.4C (above). Such 72-bit wide memory modules with 8-bit wide DDR2 SDRAMs were standard at the time. *See, e.g.,* EX1106, 10; EX1090, 24-32 (finding Perego compatible with JEDEC standards); EX1091, 28-37 (same); EX1003, ¶214.

ff) [1.i.3] 40 1-bit DDR Data Signals

Ground 2 discloses “*the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals [e.g., from 4 of the non-ECC DDR memory devices in channel 415b or 415d] and at least eight 1-bit DDR error-correcting code (ECC) data signals [e.g., from the ECC memory device 410i in channel 415b, or 410r in channel 415d]*” for the reasons discussed above for [1.i.2] (pp.86-89). EX1035, Fig.4C (below), 10:48-53 (“ECC”).



gg) [1.j.1]-[1.j.2] 72 Data Conduits

Ground 2 discloses “the sum of the at least 40 data lines [e.g., in channel 415b or 415d] and the integer number of [e.g., 32=4x8] data lines [e.g., in channel 415a or 415c] equals a total number of data conduits [e.g., 72=40+32] of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits” for the reasons discussed above for [1.i.2] (pp.86-89). EX1035, 21:16-20 (“[T]wo channels 415c [with 32 data lines] and 415d [with 40 data lines] may transfer information simultaneously.”), Fig.5B, 14:10-15 (flexible data width of “interfaces 520a and 520b”), 14:32-51 (“Serialization Ratio” (R_S)=“Memory Device Access Width” (W_A):“Buffer Device Interface Width” (W_{DP})), 17:26-28 (“serialization ratio is 1:1”), Fig.4C, 10:48-53 (“ECC”).

4. Claim 2

a) [2.a.1]-[2.a.2] Data Storage Element

Ground 2 discloses “*the controller further includes: a data storage element [e.g., a FIFO or similar buffer for writing data to the nonvolatile memory] configured to store a plurality of data bits [e.g., corresponding to one or more pages to be written to the nonvolatile memory].*” EX1003, ¶215. As discussed above for [1.c.5] (pp.63-66), the controller in Ground 2 “*write[s] [configuration/status] data into the nonvolatile memory,*” such as Perego’s “operations circuit 572” or “SPD device,” in case of power failures.

To perform such a write operation efficiently, a POSITA would have been motivated to use a temporary “*data storage element,*” such as a FIFO or similar buffer, that organizes the configuration/status data into one or more pages before writing them “*into the nonvolatile memory.*” EX1025, ¶[0050] (“backup device processor writes the data to the FIFO,...reads the data from the FIFO and writes the data to NVRAM [nonvolatile memory]”); EX1003, ¶¶216-217. Nonvolatile memory writes data in “units...referred to as blocks or pages,” which comprise tens or hundreds of bytes. EX1025, ¶¶[0036], [0049] (“writing a page of data”); EX1110, 1 (“64 bytes page”), 6; EX1003, ¶217. Also, the data to be stored in Ground 2 need not be stored and accessed on a per-byte basis because the data as a whole contain configuration/status information used for recovery or failure

analysis. *Id.* Thus, in Ground 2, a POSITA would have been motivated to organize the configuration/status data into one or pages using a temporary “*data storage element*” and then to write the page(s) to the nonvolatile memory, as was common at the time. EX1025, ¶¶[0049]-[50]; EX1110, 6; EX1003, ¶¶217-218.

Writing the configuration/status data into the nonvolatile memory in a large unit of pages (instead of small bytes) improves speed, efficiency, and power because it reduces the number of write cycles required to store the entire configuration/status data. EX1025, ¶¶[0054]-[55] (“512 bytes of data...included in each page when writing to the NVRAM [nonvolatile memory]”); EX1003, ¶218.

b) [2.a.3] Logic Element

Ground 2 discloses “*a logic element [e.g., which controls the collection of the configuration/status data into the FIFO or similar buffer, organization of the data into one or more pages, and the page write operation into the nonvolatile memory] coupled to the nonvolatile memory and the data storage element and configured to electrically communicate with the nonvolatile memory and the data storage element [e.g., to read the configuration/status data from the FIFO or similar buffer and write into the nonvolatile memory]*” for the reasons discussed above for [1.c.5] and [2.a.2] (pp.63-66, 91-92).

c) [2.a.4] Write Operation

Ground 2 discloses “*the write operation conducted by the controller in response to the trigger signal*” for the reasons discussed above for [1.c.5] (pp.63-66).

d) [2.a.5] First Write Operation

Ground 2 discloses “*a first write operation to write a first set of data bits [e.g., a first set of configuration/status information for recovery or fault analysis, such as “a first value that represents the desired width of [Perego’s] configurable width interface 590 [coupled to the system memory controller],” EX1035, 16:13-21] into a first portion of the data storage element [e.g., a first portion of the FIFO or similar buffer]*” for the reasons discussed above for [1.c.5] and [2.a.2] (pp.63-66, 91-92).

e) [2.a.6] Second Write Operation

Ground 2 discloses “*a second write operation to write a second set of data bits [e.g., a second set of configuration/status information for recovery or fault analysis, such as “a second value that represents the desired width of [Perego’s] interfaces 520a and 520b [coupled to the memory devices],” EX1035, 16:13-21, or driver settings for these interfaces, EX1027, 141] into a second portion of the data storage element [e.g., a second portion of the FIFO or similar buffer]; and subsequently*” in order to collect the first and second set of configuration/status

data and organize them into one or more pages to be stored in the nonvolatile memory for the reasons discussed above for [1.c.5] and [2.a.2] (pp.63-66, 91-92).

f) [2.a.7] Third Write Operation

Ground 2 discloses “*a third write operation to write a third set of data bits* [e.g., a full set of data corresponding to one or more pages to be written into the nonvolatile memory, which includes the collected first and second set of configuration/status data from [2.a.5] and [2.a.6]] *from the data storage element* [e.g., the FIFO or similar buffer of the size corresponding to one or more pages of the nonvolatile memory] *into the nonvolatile memory* [e.g., Perego’s “operations circuit 572” or “SPD device”],” so that the configuration/status data would be available for recovery or failure analysis for the reasons discussed above for [1.c.5], [2.a.2], and [2.a.5]-[2.a.6] (pp.63-66, 91-92, 93-94).

g) [2.a.8] Third Set of Data Bits

Ground 2 discloses “*the third set of data bits* [e.g., the full set of the configuration/status data corresponding to one or more pages of the nonvolatile memory] *includes the first and second sets of data bits* [e.g., the first and second set of configuration/status data from [2.a.5] and [2.a.6]] *written during the first and second write operations* [e.g., into the FIFO or similar buffer]” for the reasons discussed above for [1.c.5], [2.a.2], and [2.a.5]-[2.a.6] (pp.63-66, 91-92, 93-94).

5. Claim 3

Ground 2 discloses “*claim 2, wherein, prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to generate the third set of data bits [in [2.a.8], e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] based on a combination of the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] written during the first and second write operations [e.g., into the FIFO or similar buffer]*” for the reasons discussed above with reference to claim element [1.c.5] and claim 2 (pp.63-66, 91-94).

6. Claim 4

Ground 2 discloses “*claim 2, wherein, prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to generate the third set of data bits [in [2.a.8], e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] based on groups of data bits stored in the data storage element including the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] written during the first and second write operations [e.g.,*

into the FIFO or similar buffer]” for the reasons discussed above with reference to claim element [1.c.5] and claim 2 (pp.63-66, 91-94).

7. Claim 5

Ground 2 discloses “*claim 2, wherein, prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile memory], the logic element is configured to perform, in response to the detected trigger signal [from [1.c.5]], a plurality of read operations [e.g., from the FIFO or similar buffer] to read the first and second sets of data bits from the first and second portions of the data storage element, respectively, [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data collected in the FIFO or similar buffer] and to generate the third set of data bits [e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages to be written to the nonvolatile memory] based on the read first and second sets of data bits*” for the reasons discussed above with reference to claim element [1.c.5] and claim 2 (pp.63-66, 91-94). EX1025, ¶[0050] (“[T]he backup device processor reads the data from the FIFO and writes the data to the NVRAM” in “a page burst.”).

8. Claim 6

Ground 2 discloses “*claim 2, wherein, prior to performing the third write operation [in [2.a.7], e.g., from the FIFO or similar buffer to the nonvolatile*

memory], *the logic element is configured to perform, in response to the detected trigger signal* [from [1.c.5]], *a read operation* [e.g., from the FIFO or similar buffer] *to read the first and second sets of data bits from the first and second portions of the data storage element, respectively*, [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data collected in the FIFO or similar buffer] *and to generate the third set of data bits* [e.g., to organize the collected configuration/status data into a full set corresponding to one or more pages of the nonvolatile memory] *based on the read first and second sets of data bits*” for the reasons discussed above with reference to claim element [1.c.5] and claim 2 (pp.63-66, 91-94). EX1025, ¶[0050] (“[T]he backup device processor reads the data from the FIFO and writes the data to the NVRAM” in “a page burst.”).

9. Claim 7

Ground 2 discloses “*claim 2, wherein, prior to performing the first and second write operations* [from [2.a.5] and [2.a.6], e.g., into the FIFO or similar buffer to collect the configuration/status data for recovery or fault analysis], *the logic element is configured to perform, in response to the detected trigger signal* [from [1.c.5]], *one or more read operations* [e.g., to read the first and second set of configuration/status data from Perego’s “state storage 576,” EX1035, 16:13-21, or DDR SDRAM devices discussed below in claim 8 (pp.98-99), before moving them

into the FIFO or similar buffer]” for the reasons discussed above for [1.c.5] and claim 2 (pp.63-66, 91-94).

10. Claim 8

Ground 2 discloses “*claim 7, wherein the logic element is configured to perform a first read operation of the one or more read operations [of claim 7] by reading the first and second sets of data bits [from [2.a.5] and [2.a.6], e.g., the first and second set of configuration/status data] from the first and second groups of DDR SDRAM devices, respectively*” for the reasons discussed above for [1.c.5] and claim 2 (pp.63-66, 91-94), and further explained below. EX1003, ¶220.

In Ground 2, the first and second set of configuration/status data can be initially stored in “*the first and second groups of DDR SDRAM devices.*” *Id.* For example, Amidi explains that, “as systems become more mission critical, the possibility of irreplaceable data being stored in volatile memory [such as DRAM devices] increases,” and such data include those “useful for restarting a system after a failure” or “failure analysis.” EX1024, 1:19-27. Thus, at least some configuration/status data for recovery or failure analysis may be initially stored in “*the first and second groups of DDR SDRAM devices,*” which are volatile memories. EX1003, ¶¶221-222. DDR SDRAMs provide a large capacity and fast operation, allowing swift access to a large amount of configuration/status data so

that they are promptly moved to the nonvolatile memory during power failures and used for recovery or failure analysis. *Id.*

11. Claim 9

a) [9.a.1] Transfer of Third Set of Data Bits

Ground 2 discloses “*claim 2, wherein the third write operation [from [2.a.7], e.g., into the nonvolatile memory] comprises a transfer of the third set of data bits [e.g., the full set of the configuration/status data corresponding to one or more pages of the nonvolatile memory] from the data storage element [e.g., the FIFO or similar buffer] to the nonvolatile memory via a first connection [e.g., the connection between the FIFO or similar buffer and the nonvolatile memory]*” for the reasons discussed above for [1.c.5] and claim 2 (pp.63-66, 91-94).

b) [9.a.2] Transfer of First/Second Sets of Data Bits

Ground 2 discloses “*the first and second write operations [from [2.a.5] and [2.a.6], e.g., into the FIFO or similar buffer] comprise a transfer of the first and second sets of data bits into the data storage element [e.g., the FIFO or similar buffer] via a second connection [e.g., between the local storage, such as Perego’s “state storage 576,” which stores the first and second set of configuration/status data, and the FIFO or similar buffer]*” for the reasons discussed above for [1.c.5] and claims 2 and 7 (pp.63-66, 91-94, 97-98).

12. Claim 10

Ground 2 discloses “*claim 2, wherein, the data storage element is a buffer configured to store a plurality of data bits or a First-In First-Out (FIFO) buffer configured to store the plurality of data bits*” for the reasons discussed above for [1.c.5] and claim 2 (pp.63-66, 91-94). EX1025, ¶[0048] (“The FIFO stores the data for transmission.”).

13. Claim 11

Ground 2 discloses “*claim 1, wherein when [+12V] power is provided to the DIMM from the [+12V] power [supply] rails of the system board [see [1.b.3] (pp.48-50)] the voltage monitor circuit compares the input voltage to a plurality of threshold voltages [as taught by Amidi] including the first threshold voltage [from [1.c.6], e.g., 15% above +12V] and a second threshold voltage [e.g., 15% below +12V]*” for the reasons discussed above for [1.c.3] and [1.c.6] (pp.61-62, 67-67). EX1023, ¶[0013] (“+/-15%”), [0020] (“dual +12V power supply rail”), EX1024, 9:8-10 (“power...signals checked for proper levels”). The Board has also found that the combination of Harris and Amidi discloses substantially similar limitations. EX1070, 79; EX1071, 65.

14. Claim 12

Ground 2 discloses “*claim 1, wherein the second component [e.g., Perego’s buffer device (red) below] is further connected to the first regulated voltage line [e.g., for V_{dd} (orange)] and is powered by the first [e.g., V_{dd}] and second [e.g., V_{cc}]*

(pink)] regulated voltages when power from the [+12V] power rails of the system board is provided to the DIMM” for the reasons discussed above for [1.e] and [1.f.1]-[1.f.3] (pp.71-79). EX1035, Fig.3C (below).

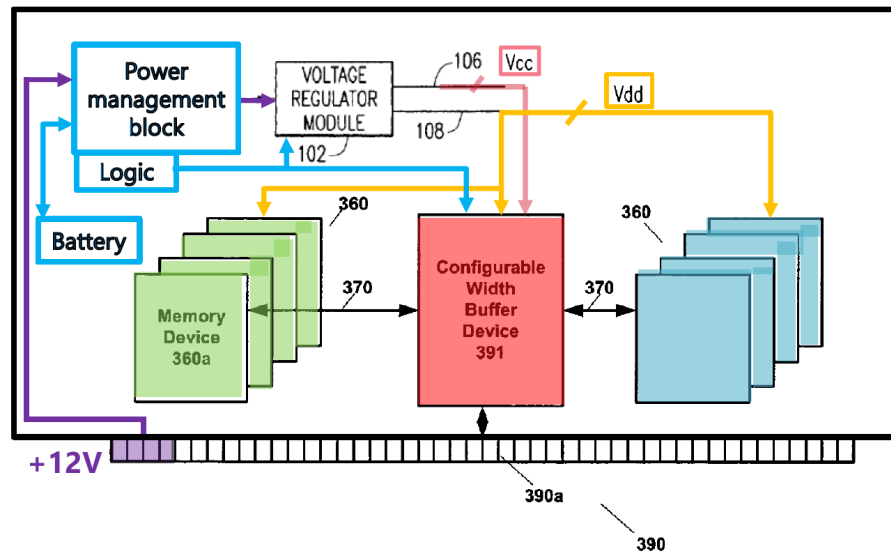


Fig. 3C

As explained above for [1.e] (pp.71-77), the buffer device in Ground 2 requires both V_{cc} (for its own operation) and V_{dd} (for communication with the memory devices (blue and green), which also use V_{dd}), as was common, see EX1028, 13-16 (V_{dd} coupled to buffer); EX1027, 32 (similar); EX1026, 49 (V_{ddq} for DDR memory device I/O supply).

15. Claim 13

Ground 2 discloses “claim 12, wherein, when [+12V] power from the power rails of the system board is provided to the DIMM, an additional trigger condition occurs when the input voltage is above the first threshold and below the second

threshold [e.g., under the **Second Interpretation** below, when the input voltage is **within** a normal operating range, e.g., $\pm 15\%$ of the +12V; or, under the **Third Interpretation** below, when the input voltage is **outside** a normal operating range]; and wherein, in response to the additional trigger condition, the voltage monitor circuit is further configured to generate and transmit a second trigger signal [e.g., a signal similar to Amidi's "signal 670" causing to select "system supply 605" under the **Second Interpretation**, EX1024, 4:44-55, or to select "battery power 650" under the **Third Interpretation**, see *id.*]." EX1003, ¶223.

There are three possible interpretations of the claim language. The **First Interpretation** is that the "second threshold" is even higher than the "first threshold," which is not disclosed by the patent and would not make much sense. EX1003, ¶134.

Under the **Second Interpretation**, the "first" and "second threshold" may represent the lower and upper limit of a normal operating range, respectively, see EX1002, 1428-29, in which case "*an additional trigger condition*" occurs when the input voltage is **within** the normal range. Under this interpretation, Ground 2 discloses this limitation for the reasons discussed above for claim 11, [1.c.3], [1.c.5], and [1.c.6] (pp.100-100, 61-62, 63-67); EX1003, ¶224. For example, a normal operating range for the purpose of detecting a power failure may be " $\pm 15\%$ " of the 12V input supply. EX1023, ¶[0013]; *supra* pp.61-62. And

Amidi teaches “detecting...whether a system is ready [i.e., whether the input supply voltage is within the normal operating range], and restoring control to the system,” which involves the controller issuing “*a second trigger signal*” to switch back to the input supply voltage. EX1024, 8:62-9:2, Fig.15 (below), 1:23-25, 9:8-10, 4:44-55 (“signal 670 caus[ing] power switch multiplexer 655 to choose system supply 605” when no power failure is detected), Fig.6; EX1023, ¶[0013]; EX1003, ¶224.

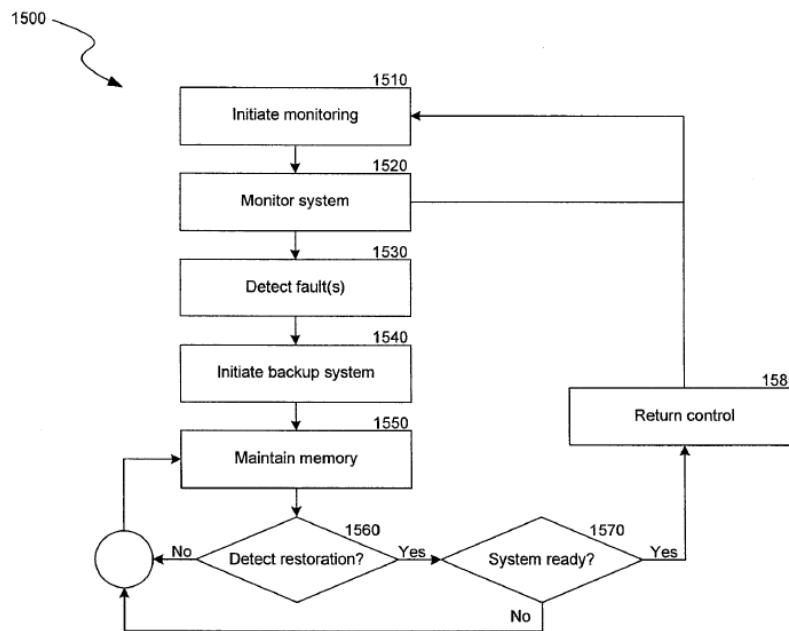


FIG. 15

Under the ***Third Interpretation*** — consistent with the specification, where “*an additional trigger condition*” occurs when the input voltage is ***outside*** a normal operating range — Ground 2 discloses this limitation for the reasons discussed above for claim 11, [1.c.3], [1.c.5], and [1.c.6] (pp.100-100, 61-62, 63-

67); EX1023, ¶[0013] (“+/-15%”); EX1024, 9:8-10 (“power...signals checked for proper levels”); 4:44-55 (“signal 670 caus[ing] power switch multiplexer 655 to choose battery power 650” upon detecting power failure), Fig.6; EX1003, ¶225.

16. Claim 14

Ground 2 discloses “*claim 1, wherein, when [+12V] power from the power rails of the system board is provided to the DIMM, the nonvolatile memory is [e.g., powered by the fourth regulated voltage V_{DDSPD} , e.g., 3.3V, and is] not powered using the first regulated voltage [e.g., V_{dd} , e.g., 1.8V, which is used to power DDR2 memory devices]*” for the reasons discussed above for [1.e] (pp.71-77).

17. Claim 15

Ground 2 discloses “*claim 1, wherein each of the first, second, and third converter circuits is a buck converter [discussed above (pp.13-14, 25-35), which efficiently converts the input +12V into lower first, second, and third regulated voltages], and the fourth converter circuit is a voltage reducing circuit [e.g., another buck converter, which efficiently converts the input +12V into the lower fourth regulated voltage]*” for the reasons discussed above for [1.e] (pp.71-77).

Both Amidi and Harris disclose using a buck converter to efficiently reduce a higher voltage into a lower regulated voltage. EX1024, Fig.6 (640, below); EX1023, ¶¶[0009]-[0010], [0012] (“high-frequency switching voltage converter” to convert 12V input down to “0.5V to 3.5V”); EX1003, ¶¶66-70, 161-167.

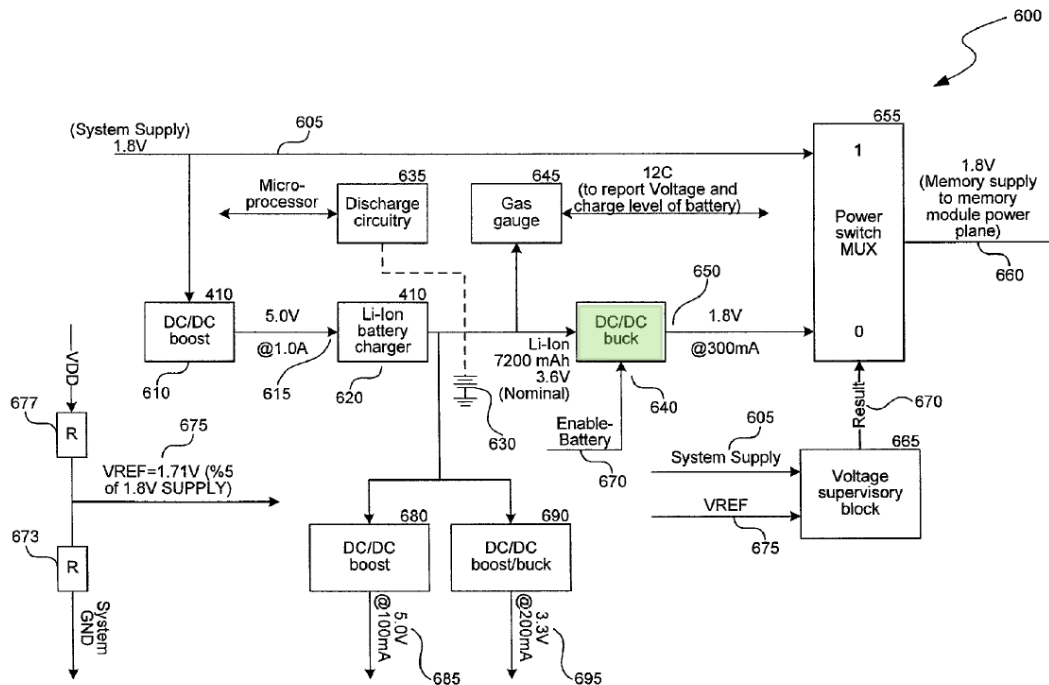


FIG. 6

18. Claims 16-28

The limitations of claims 16-28 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 2 for at least the same reasons discussed above:

This limitation in claims 16-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[16.a.1]	[1.a.1]
[16.a.2]	[1.a.2]
[16.a.3]	[1.a.3]
[16.a.4]	[1.a.4]
[16.b.1]	[1.b.1]

This limitation in claims 16-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[16.b.2]	[1.b.2]
[16.b.3]	[1.b.3]
[16.b.4]	[1.b.4]
[16.b.5]	[1.b.5]
[16.b.6]	[1.b.6]
[16.b.7]	[1.b.7]
[16.b.8]	[1.b.8]
[16.c.1]	[1.c.1], [2.a.1]-[2.a.2]
[16.c.2]	[1.c.2]
[16.c.3]	[1.c.3]
[16.c.4]	[1.c.4]
[16.c.5]	[1.c.5], [2.a.4]-[2.a.5], <i>see</i> below the table
[16.d.1]	[1.d.1]
[16.d.2]	[1.d.2]
[16.e]	[1.e]
[16.f.1]	[1.f.1]
[16.f.2]	[1.f.2]
[16.f.3]	[1.f.3]
[16.f.4]	[1.f.4]
[16.f.5]	[1.f.5]
[16.g.1]	[1.g.1]

This limitation in claims 16-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[16.g.2]	[1.g.2]
[16.g.3]	[1.g.3]
[16.h.1]	[1.h.1]
[16.h.2]	[1.h.2]
[16.h.3]	[1.h.3]
[16.i.1]	[1.i.1]
[16.i.2] ²	[1.i.2]
[16.i.3]	[1.i.3]
[16.j.1]	[1.j.1]
[16.j.2]	[1.j.2]
[17]	[1.c.1], [2.a.1]-[2.a.3]
[18] ³	[2.a.4], [2.a.6]
[19.a.1]	[2.a.4], [2.a.6]-[2.a.7]
[19.a.2]	[2.a.8]
[19.a.3] ⁴	[16.c.5], [2.a.6]-[2.a.7], <i>see below the table</i>
[20]	[16.c.5], [5], <i>see below the table</i>

² The antecedents in [16.h.2]-[16.h.3] are “*devices*” not “*packages*.”

³ The “*logic element*” is included in the “*controller*” of claim 17.

⁴ *See* p.107 n.3.

This limitation in claims 16-28...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[21.a.1] ⁵	[2.a.4], [2.a.7]
[21.a.2]	[2.a.8]
[22]	[4]
[23.a.1]	[2.a.8], [9.a.1]
[23.a.2]	[9.a.2]
[24]	[16.c.5], [7]-[8], <i>see below the table</i>
[25]	[14]
[26]	[11]
[27]	[1.c.6], [11]
[28.a]	[13.a.1]
[28.b]	[13.a.2]

Claim limitation [16.c.5] and claim 20 additionally recite “*periodically perform[ing]*” write/read operations into/from the “*data storage element,*” such as a FIFO or similar buffer, *supra* pp.91-92, “*at regular intervals of time.*” Similarly, claim 24 requires “*periodically at regular intervals of time*” reading data from “*DDR SDRAM devices.*” As discussed above for claims 2, 5, and 7-8, the process of organizing configuration/status data into pages using a FIFO circuit or similar

⁵ See p.107 n.3.

buffer before page write operations to the nonvolatile memory in Ground 2 discloses all these write/read operations involving the “*data storage element*,” *supra* pp.91-94, 96-96, and “*DDR SDRAM devices*,” *supra* pp.97-99. Ground 2 further teaches the “*periodically at regular intervals of time*” limitation. For such page write operations, the size of the FIFO or similar buffer would correspond to one page of the nonvolatile memory. EX1003, ¶229. This way, one page at a time is written from the FIFO to the non-volatile memory, avoiding the need for a larger FIFO or buffer. *Id.* Also, in this case, each page write operation is performed at a predefined time interval corresponding to the internal write cycle of the nonvolatile memory. *See, e.g.*, EX1049, pp.1 (“Page program: 300µs (TYP)”), 41 (“Page program time tPROG 300 [Typ] 700 [Max] µs”); EX1110, pp.1 (“Self-timed ERASE and WRITE cycles (5ms max.)”), 4 (“TWC Internal Write Cycle Time – 5 ms [Max]”); EX1003, ¶230. Thus, all the pre-process of organizing the configuration/status data into pages before the page write operations — including writing/reading the data into/from the FIFO circuit (claims 16 and 20), *supra* pp.93-94, 96-96, and reading the data from DDR DRAMs (which originally store the data) to refill the FIFO (claim 24), *supra* pp.97-99 — are also performed “*periodically at regular intervals of time*,” corresponding to the internal write cycle of the nonvolatile memory, such as “TWC.” *Id.*

Claim limitation [19.a.3] is similar to [16.c.5], but adds that the periodic write operations are “*perform[ed] every millisecond.*” As discussed above, the write cycle of the nonvolatile memory is on the order of one millisecond depending on the specific implementation. EX1049, pp.1, 41; EX1110, pp.1, 4; EX1003, EX1003, ¶234. Thus, given the known range of times required to write to nonvolatile memory, it was obvious to use a nonvolatile memory with a page write cycle around (or somewhat less than) 1ms, allowing periodic writes “*every millisecond.*” *Id.*; *Gen. Hosp. Corp. v. Sienna Biopharms., Inc.*, 888 F.3d 1368, 1373 (Fed. Cir. 2018); *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004).

19. Claims 29-38

The limitations of claims 29-38 are substantially identical to earlier limitations, as shown in the following table, and thus they are obvious in light of Ground 2 for at least the same reasons discussed above:

This limitation in claims 29-38...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[29.a.1]	[1.a.1]
[29.a.2]	[1.a.2]
[29.a.3]	[1.a.3]
[29.a.4]	[1.a.4]
[29.b.1]	[1.b.1]

This limitation in claims 29-38...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[29.b.2]	[1.b.2]
[29.b.3]	[1.b.3]
[29.b.4]	[1.b.4]
[29.b.5]	[1.b.5]
[29.b.6]	[1.b.6]
[29.b.7]	[1.b.7]
[29.b.8]	[1.b.8]
[29.b.9]	[1.b.7]
[29.b.10]	[1.i.2] ⁶
[29.c.1]	[1.c.1], [2.a.1]-[2.a.2]
[29.c.2]	[1.c.2]
[29.c.3]	[1.c.3]
[29.c.4]	[1.c.4]
[29.c.5]	[1.c.5], [2.a.4]-[2.a.5]
[29.d.1]	[1.d.1]
[29.d.2]	[1.d.2]

⁶ DRAM devices communicating “**40 1-bit DDR data signals in parallel** via...**40 data lines**” in [1.i.2] means “**each data line...conduct[s] a 1-bit DDR data signal**” in [29.b.10].

This limitation in claims 29-38...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[29.e]	[1.e]
[29.f.1]	[1.f.1]
[29.f.2]	[1.f.2]
[29.f.3]	[1.f.3]
[29.f.4]	[1.f.4]
[29.f.5]	[1.f.5]
[29.g.1]	[1.g.1]
[29.g.2]	[1.g.2]
[29.g.3]	[1.g.3]
[29.h.1]	[1.h.1]
[29.h.2]	[1.h.2]
[29.h.3]	[1.h.3]
[29.i.1]	[1.i.1]
[29.i.2] ⁷	[1.i.2]
[29.i.3]	[1.i.3]
[29.j.1]	[1.j.1]
[29.j.2]	[1.j.2]
[30]	[14]

⁷ The antecedents in [29.h.2]-[29.h.3] are “[*first/second*] group of ***at least [five/four]*** DDR SDRAM devices.”

This limitation in claims 29-38...	...is substantially similar to this limitation and thus obvious for at least the same reasons above
[31]	[14]
[32]	[11]
[33]	[1.c.6], [11]
[34.a]	[13.a.1]
[34.b]	[13.a.2]
[35.a.1]	[1.c.1], [2.a.1]-[2.a.3]
[35.a.2]	[2.a.4]-[2.a.6]
[36.a.1] ⁸	[2.a.4], [2.a.6]-[2.a.7]
[36.a.2]	[2.a.8]
[37]	[7]-[8]
[38]	[15]

VII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-38 be canceled as unpatentable.

Dated: November 7, 2025

/Eliot D. Williams/
 Eliot D. Williams
 Reg. No. 50,822
BAKER BOTTS L.L.P.
 700 K Street, N.W.

⁸ The “*logic element*” is included in the “*controller*” of claim 35.

Petition for *Inter Partes* Review of U.S. Patent No. 12,373,366

Washington, D.C. 20001
T: (202) 639-1334
F: (202) 639-1167

Theodore W. Chandler
Reg. No. 50,319
BAKER BOTTS L.L.P.
1801 Century Park East
Suite 2400
Los Angeles, CA 90067
T: (213) 202-5702
F: (213) 202-5732

Ferenc Pazmandi
Reg. No. 66,216
BAKER BOTTS L.L.P.
101 California Street
Suite 3200
San Francisco, CA 94111
T: (415) 291-6255
F: (415) 291-6355

Mark A. Speegle
Reg. No. 77,512
BAKER BOTTS L.L.P.
401 South First Street, Suite 1300
Austin, Texas 78704
T: (512) 322-2536
F: (512) 322-3636

Counsel for Petitioner
Samsung Electronics Co., Ltd.

CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24(a)(1)(i) (“14,000 words”) because it contains 13,998 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24(a)(1).

Dated: November 7, 2025

/Eliot D. Williams/

Eliot D. Williams

Reg. No. 50,822

BAKER BOTTS L.L.P.

700 K Street, N.W.

Washington, D.C. 20001

T: (202) 639-1334

F: (202) 639-1167

Counsel for Petitioner

Samsung Electronics Co., Ltd.

CERTIFICATE OF SERVICE

I hereby certify that on this 7th day of November, 2025, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

Khaled Shami
Netlist Inc.
1909 K Street, NW
9th Floor
Washington DC 20006-1152
(202) 467-8800

Dated: November 7, 2025

/Eliot D. Williams/
Eliot D. Williams
Reg. No. 50,822
BAKER BOTTS L.L.P.
700 K Street, N.W.
Washington, D.C. 20001
T: (202) 639-1334
F: (202) 639-1167

Counsel for Petitioner
Samsung Electronics Co., Ltd.