Claim 1 of U.S. Patent No. 11,232,054 vs. Claim 1 of U.S. Patent No. 12,373,366

1. ~~A memory module comprising:~~ A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having ~~an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of~~ edge connections configured to ~~couple power, data, address and control signals between~~fit into the memory ~~module and~~slot connector of the ~~host~~ system~~;~~ board, the PCB including:

~~a~~ a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage ~~conversion~~supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and ~~configured to provide at least three~~to an input

voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated ~~voltages,~~ voltage lines,

wherein the ~~voltage conversion circuit~~set of components includes:

a first component configured to receive power via at least ~~three buck converters each of which is configured to produce a~~ the first regulated voltage ~~of the~~ line;

a second component configured to receive power via at least ~~three~~the second regulated ~~voltages~~voltage line;

a ~~plurality of components coupled~~third component configured to receive power via at least the ~~PCB,~~third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the ~~plurality~~set of components ~~coupled~~:

(i) is electrically connected to ~~at least~~ one ~~regulated voltage of the at least three regulated voltages,~~ or more of the ~~plurality~~first, second, third, and fourth regulated voltage lines; and

(ii) receives power only via the one or more of ~~components including a~~the first, second, third, and fourth regulated voltage lines,

wherein the plurality of ~~synchronous dynamic random access memory (~~DDR SDRAM~~)~~ devices ~~and~~ includes:

a first ~~circuit that is coupled to the plurality of~~ group of at least five DDR SDRAM devices ~~and~~ that are each connected to a first ~~set of edge connections of the plurality of edge connections, wherein the first circuit is coupled~~chip select line configured to electrically conduct a first ~~and~~chip select signal;

a second ~~regulated voltages~~group of ~~the~~ at least ~~three regulated voltages, and wherein the plurality of~~four DDR SDRAM devices ~~are coupled~~that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the ~~first regulated voltage~~DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least ~~three regulated voltages~~40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

Claim 1 of U.S. Patent No. 11,016,918 vs. Claim 1 of U.S. Patent No. 12,373,366

1. A dual in-line memory module ~~comprising:~~

~~a printed circuit board (PCB) having an interface~~(DIMM) configured to fit into a ~~corresponding~~ memory slot connector of a ~~host~~system board of a computer system, the ~~interface~~memory slot connector including a ~~plurality of edge connections configured to couple~~ set of power~~,~~ conduits, a set of data~~,~~ conduits, and a set of address and control conduits, wherein data signals are transferred between the ~~memory module~~system board and the ~~host system;~~ DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

~~a first buck converter~~a printed circuit board (PCB) having edge connections configured to ~~provide a first regulated~~fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage ~~having a~~supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage ~~amplitude~~monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

~~a second buck converter configured to provide a second regulated voltage having a second voltage amplitude;~~

~~a third buck converter configured to provide a third regulated voltage having a third voltage amplitude;~~

~~a converter circuit configured to provide a fourth regulated voltage having a fourth voltage amplitude; and~~

~~a plurality of~~ a set of components coupled to the PCB, ~~each component of~~ the ~~plurality~~set of components ~~coupled to one or more regulated voltages of the first, second, third and fourth regulated voltages, the plurality of components comprising:~~

including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the ~~first regulated voltage,~~set of address and

~~at least one circuit coupled between a first portion of~~ control lines and to the ~~plurality~~set of ~~edge connections and~~ data lines, the ~~plurality of~~DDR SDRAM devices~~, the at least one circuit operable to (i) receive a first plurality of address and control signals via the first portion of the plurality of edge connections, and (ii)~~ being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage

supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second ~~plurality of address and control signals to the plurality of SDRAM devices, the~~ component configured to receive power via at least ~~one circuit coupled to both~~ the second regulated voltage ~~and~~ line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage~~,~~ line;

wherein ~~a~~each component of the set of components:

(i) is electrically connected to one or more of the first ~~one of the~~, second, third, and fourth regulated voltage ~~amplitudes is less than a~~lines; and

(ii) receives power only via the one or more of the first, second ~~one of the second~~, third, and fourth regulated voltage ~~amplitudes~~lines,

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices

is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

Claim 1 of U.S. Patent No. 8,874,831 vs. Claim 1 of U.S. Patent No. 12,373,366

1. ~~A memory module couplable to a memory controller of a host system, comprising:~~

~~a non-volatile memory subsystem;~~

~~a data manager coupled to the non-volatile memory subsystem;~~

~~a volatile memory subsystem coupled to the data manager and operable to exchange data with the non-volatile memory subsystem by way of the data manager; and~~

~~a controller operable to receive commands from the memory controller and to direct (i) operation of the non-volatile memory subsystem, (ii) operation of the volatile memory subsystem, and (iii) transfer of data between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on at least one received command from the memory controller, wherein:~~

~~at least one of the volatile and non-volatile memory subsystems comprises one or more memory segments, each memory segment comprising at least one memory circuit, memory device, or memory die, and~~

~~the data manager is configured as a bi-directional data transfer fabric having two or more sets of data ports, a first set of data ports of the two or more sets of data ports is coupled to the volatile memory subsystem, a second set of data ports of the two or more sets of data ports is coupled to the non-volatile memory subsystem, the two or more sets of data ports being operable by the data manager to transfer data to or from one or more memory segments of the volatile or non-volatile memory subsystems, the data manager further including a data buffer for buffering data delivered to or from the non-volatile memory subsystem, and a data format module configured to format data to be transferred between any two or more of the memory controller, the volatile memory subsystem, and the non-volatile memory subsystem based on control information received from the controller.~~

A dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system board of a computer system, the memory slot connector including a set of power conduits, a set of data conduits, and a set of address and control conduits, wherein data signals

are transferred between the system board and the DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the PCB including:

a first set of edge connections configured to be electrically connected to the set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is the only power received by the DIMM;

a second set of edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.

Claim 1 of U.S. Patent No. 8,301,833 vs. Claim 1 of U.S. Patent No. 12,373,366

1. A ~~method for controlling~~dual in-line memory module (DIMM) configured to fit into a memory slot connector of a system ~~operatively coupled to a host~~board of a computer system, the memory ~~system~~ slot connector including a ~~volatile memory subsystem~~set of power conduits, a set of data conduits, and a ~~non-volatile memory subsystem, the method comprising:~~

~~operating the volatile memory subsystem at a first clock frequency when the memory system is in a first mode of operation in which data is communicated~~set of address and control conduits, wherein data signals are transferred between the ~~volatile memory subsystem and the host system;~~

~~operating the non-volatile memory subsystem at a second clock frequency when the memory system is in a second mode of operation in which data is communicated between the volatile memory subsystem~~system board and the ~~non-volatile memory subsystem;~~DIMM via the set of data conduits, and address and control signals are delivered from the system board to the DIMM via the set of address and control conduits, the DIMM comprising:

~~operating~~a printed circuit board (PCB) having edge connections configured to fit into the memory slot connector of the system board, the ~~volatile memory subsystem at a third clock frequency when~~PCB including:

a first set of edge connections configured to be electrically connected to the ~~memory~~set of power conduits and operable to deliver to the DIMM power from power rails of the system board via the set of power conduits, wherein the power delivered to the DIMM from the power rails of the system board is ~~in~~ the only power received by the DIMM;

a second ~~mode~~set of ~~operation,~~edge connections configured to be electrically connected to the set of data conduits, and

a third set of edge connections configured to be electrically connected to the set of address and control conduits,

a set of voltage supply lines electrically connected to the first set of edge connections and configured to receive the power delivered to the DIMM from the power rails of the system board by way of the memory slot connector of the system board and the first set of edge connections of the DIMM,

a set of data lines electrically connected to the second set of edge connections, and

a set of address and control lines electrically connected to the third ~~clock frequency~~set of edge connections;

a controller including a voltage monitor circuit and nonvolatile memory, the controller coupled to the PCB and to an input voltage supply line of the set of voltage supply lines, the voltage monitor circuit configured to: (i) monitor an input voltage supplied via the input voltage supply line; (ii) generate a trigger signal upon detecting a trigger condition; and (iii) transmit the trigger signal to at least one other portion of the controller, wherein the controller is configured to perform, in response to the trigger signal, a write operation to write data into the nonvolatile memory, and wherein the trigger condition occurs when the input voltage exceeds a first threshold voltage;

a set of components coupled to the PCB, the set of components including a plurality of double data rate (DDR) synchronous dynamic random access memory (SDRAM) devices coupled to the set of address and control lines and to the set of data lines, the DDR SDRAM devices being ~~less than the first clock frequency~~operable to receive or output data signals via the set of data lines based on address and control signals received from the system board via the set of address and control lines; and

first, second, third, and fourth converter circuits coupled to the PCB and to the input voltage supply line, and configured to receive power from the input voltage supply line and to deliver power via first, second, third, and fourth regulated voltage lines,

wherein the set of components includes:

a first component configured to receive power via at least the first regulated voltage line;

a second component configured to receive power via at least the second regulated voltage line;

a third component configured to receive power via at least the third regulated voltage line; and

a fourth component configured to receive power via at least the fourth regulated voltage line;

wherein each component of the set of components:

(i) is electrically connected to one or more of the first, second, third, and fourth regulated voltage lines; and

(ii) receives power only via the one or more of the first, second, third, and fourth regulated voltage lines,

wherein the plurality of DDR SDRAM devices includes:

a first group of at least five DDR SDRAM devices that are each connected to a first chip select line configured to electrically conduct a first chip select signal;

a second group of at least four DDR SDRAM devices that are each connected to a second chip select line configured to electrically conduct a second chip select signal;

wherein when power from the power rails of the system board is provided to the DIMM and each group of the first and second groups of DDR SDRAM devices is not in self-refresh mode:

the first group of DDR SDRAM devices is configured to be enabled, in response to the first chip select signal, to receive or output at least 40 1-bit DDR data signals in parallel via at least 40 data lines of the set of data lines independently of whether the second group of DDR SDRAM devices is enabled, in response to the second chip select signal, to receive or output an integer number of 1-bit DDR data signals in parallel via an integer number of data lines of the set of data lines;

the at least 40 1-bit DDR data signals include at least 32 1-bit wide DDR data signals and at least eight 1-bit DDR error-correcting code (ECC) data signals; and

wherein the sum of the at least 40 data lines and the integer number of data lines equals a total number of data conduits of the set of data conduits of the memory slot connector, and the total number of data conduits is at least 72 data conduits.