Paper No. 1

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD.,

Petitioner,

v.

NETLIST, INC.,

Patent Owner

Patent No. 11,232,054

Issued: January 25, 2022

Filed: May 24, 2021

Inventors: Chi-She Chen, Jeffrey C. Solomon, Scott H. Milton, and Jayesh Bhakta

Title: Flash-DRAM Hybrid Memory Module

Inter Partes Review No. IPR2022-00999

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 11,232,054

Netlist EX2056
Samsung v. Netlist
IPR2026-00018

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EXHIBIT LIST

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1001	U.S. Patent No. 11,232,054
1002	File History of U.S. Patent No. 11,232,054
1003	Declaration of Dr. Andrew Wolfe
1004	Curriculum Vitae of Dr. Andrew Wolfe
1005	File History of U.S. Provisional Application No. 60/941,586
1006	File History of U.S. Patent Application No. 12/131,873
1007	File History of U.S. Patent Application No. 12/240,916
1008	File History of U.S. Provisional Application No. 61/512,871
1009	File History of U.S. Patent Application No. 13/559,476
1010	File History of U.S. Patent Application No. 14/489,269
1011	File History of U.S. Patent Application No. 14/840,865
1012	File History of U.S. Patent Application No. 15/934,416
1013	File History of U.S. Patent Application No. 17/138,766
1014	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 1 (PTAB June 20, 2014) (833 Patent IPR Petition)
1015	*SanDisk Corp. v. Netlist, Inc.*, IPR2014-00994, Paper No. 8 (PTAB December 16, 2014) (833 Patent Institution Decision)
1016	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 8 (PTAB September 22, 2014) (833 Patent IPR Corrected Petition)
1017	*Smart Modular Techs. Inc. v. Netlist, Inc.*, IPR2014-01370, Paper No. 13 (PTAB March 13, 2015) (833 Patent Institution Decision)

Exhibit #	Description
1018	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 1 (PTAB January 13, 2017) (833 Patent IPR Petition)
1019	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00649, Paper No. 7 (PTAB July 24, 2017) (833 Patent Institution Decision)
1020	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 1 (PTAB January 17, 2017) (831 Patent IPR Petition)
1021	*SK hynix Inc. et al. v. Netlist, Inc*., IPR2017-00692, Paper No. 25 (PTAB July 5, 2018) (831 Patent Final Written Decision)
1022	*Micron Tech., Inc. et al. v. Netlist, Inc.*, IPR2022-00418, Paper No. 2 (PTAB January 14, 2022) (831 Patent IPR Petition)
1023	U.S. Patent Application Publication No. 2006/0174140 to Harris *et al.*
1024	U.S. Patent No. 7,724,604 to Amidi *et al.*
1025	U.S. Patent Application Publication No. 2006/0080515 to Spiers *et al.*
1026	JEDEC Standard, DDR2 SDRAM Specification, JESD79-2B (January 2005) (“JESD79-2B”)
1027	JEDEC Standard, FBDIMM: Advanced Memory Buffer (AMB), JESD82-20 (March 2007) (“JESD82-20”)
1028	JEDEC Standard, FBDIMM Specification: DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification, JESD205 (March 2007) (“JESD205”)
1029	Declaration of Julie Carlson for JESD82-20 and JESD205
1030	U.S. Patent No. 7,719,866 to Boldo
1031	PCI Local Bus Specification Revision 2.2 (1998)

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1032	Mohan et al., Power Electronics: Converters, Applications, and Design (2d Ed. 1995)
1033	U.S. Patent No. 7,721,130 to Prete *et al.*
1034	U.S. Patent No. 6,798,709 to Sim *et al.*
1035	[Intentionally Omitted]
1036	[Intentionally Omitted]
1037	U.S. Patent Application Publication No. 2008/0238536 to Hayashi *et al.*
1038	U.S. Patent No. 6,856,556 to Hajeck
1039	U.S. Patent Application Publication No. 2010/0257304 to Rajan *et al.*
1040	Texas Instruments, TPS51020 Datasheet (December 2003)
1041	Fairchild Semiconductor, FAN5026 Datasheet (October 2005)
1042	Murata Power Supply Reference Guide for Xilinx FPGAs (September 2006)
1043	Murata Power Supply Reference Guide for Altera FPGAs (February 2008)
1044	U.S. Patent Application Publication No. 2010/0205470 to Moshayedi *et al.*
1045	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) ("JESD79")
1046	JEDEC Standard, DDR3 SDRAM, JESD79-3C (September 2007) ("JESD79-3A")
1047	U.S. Patent No. 7,023,187 to Shearon *et al.*

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1048	Murata, DC-DC Converter Specification (DRAFT), MPD4S014S Datasheet (January 21, 2008)
1049	Micron, NAND Flash Memory Datasheet (January 2006)
1050	U.S. Patent No. 7,692,938 to Petter
1051	[Intentionally Omitted]
1052	[Intentionally Omitted]
1053	[Intentionally Omitted]
1054	U.S. Patent No. 11,016,918
1055	U.S. Patent Application Publication No. 2008/0101147 to Amidi
1056	U.S. Patent No. 5,563,839 to Herdt *et al.*
1057	U.S. Patent No. 6,693,840 to Shimada *et al.*
1058	Lenk, John D., *Simplified Design of Switching Power Supplies* (1995)
1059	U.S. Patent No. 7,061,214 to Mayega *et al.*
1060	U.S. Patent No. 5,630,096 to Zuravleff *et al.*
1061	Analog Devices, ADM1066 Datasheet (2006)
1062	Alan Moloney, *Power-Supply Management—Principles, Problems, and Parts*, Analog Dialogue (May 2006)
1063	National Semiconductor, LMC6953 PCI Local Bus Power Supervisor Datasheet (October 1996)
1064	U.S. Patent Application Publication No. 2007/0136523 to Bonella *et al.*
1065	U.S. Patent Application Publication No. 2009/0034354 to Resnick

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1066	U.S. Patent No. 10,672,458 to Shaeffer *et al.*
1067	LatticeXP Family Data Sheet (March 2006)
1068	Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
1069	First Amended Complaint for Declaratory Judgment of Non-Infringement and Unenforceability; Breach of Contract, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Jan. 18, 2022)
1070	Netlist's motion to dismiss the First Amended Complaint, *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Feb. 16, 2022)
1071	Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
1072	Answer in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Apr. 12, 2022)
1073	Amended Complaint in *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed May 3, 2022)

CLAIM LISTING

Ref. #	Listing of Challenged Claims
1.a	1. A memory module comprising:
1.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections configured to couple power, data, address and control signals between the memory module and the host system;
1.c	a voltage conversion circuit coupled to the PCB and configured to provide at least three regulated voltages, wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages;
1.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices and [3] a first circuit that is coupled to the plurality of SDRAM devices and to a first set of edge connections of the plurality of edge connections, [4] wherein the first circuit is coupled to first and second regulated voltages of the at least three regulated voltages, and [5] wherein the plurality of SDRAM devices are coupled to the first regulated voltage of the at least three regulated voltages.
2.a	2. The memory module of claim 1, wherein the first regulated voltage has a first voltage amplitude, and the second regulated voltage has a second voltage amplitude; and
2.b	wherein a first one of the first and second voltage amplitudes is less than a second one of the first and second voltage amplitudes.
3	3. The memory module of claim 1, wherein a third regulated voltage of the at least three regulated voltages has a voltage amplitude of 1.8 volts.
4.a	4. The memory module of claim 1, further comprising:

Ref. #	Listing of Challenged Claims
4.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude below a predetermined threshold voltage,
4.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
5.a	5. The memory module of claim 4, further comprising:
5.b	a controller coupled to the voltage monitor circuit;
5.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
6.a	6. The memory module of claim 1, further comprising:
6.b	a voltage monitor circuit coupled to the PCB and to a second set of edge connections of the plurality of edge connections, the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections, the voltage monitor circuit configured to produce a trigger signal in response to the input voltage having a voltage amplitude above a predetermined threshold voltage,
6.c	wherein the memory module transitions from a first operable state to a second operable state in response to the trigger signal.
7.a	7. The memory module of claim 6, further comprising:
7.b	a controller coupled to the voltage monitor circuit;
7.c	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
8.a	8. The memory module of claim 1, further comprising:
8.b	a controller coupled to the PCB, the controller including a voltage monitor circuit configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections,
8.c	wherein, in response to the voltage monitor circuit detecting a power threshold condition, the voltage monitor circuit transmits a signal to one or more portions of the controller.

Ref. #	Listing of Challenged Claims
9.a	9. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being above a first predetermined threshold voltage, and
9.b	wherein the first predetermined threshold voltage is above a specified operating voltage.
10	10. The memory module of claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage.
11.a	11. The memory module of claim 9, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting an amplitude of the input voltage being below a second predetermined threshold voltage, and
11.b	wherein the second predetermined threshold voltage is below the specified operating voltage, and
11.c	wherein the memory module transitions from a first operable state to a second operable state in response to the signal.
12	12. The memory module of claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage.
13	13. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a power reduction condition or a low voltage condition of the input voltage.
14	14. The memory module of claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system.
15	15. The memory module of claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.
16.a	16. A memory module comprising:
16.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
16.c	a voltage conversion circuit coupled to the PCB and configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

Ref. #	Listing of Challenged Claims
16.d	[1] a plurality of components coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] the plurality of SDRAM devices coupled to a first regulated voltage of the plurality of regulated voltages; and
16.e	[1] a controller coupled to the PCB, the controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface, the voltage monitor circuit configured to detect an amplitude change in the input voltage, [2] wherein, in response to the voltage monitor detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
17	17. The memory module of claim 16, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage and to detect the input voltage being below a second predetermined threshold voltage.
18.a	18. The memory module of claim 16, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
18.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
19.a	19. The memory module of claim 18, wherein, in the first operable state, the first pre-regulated voltage is supplied to the voltage conversion circuit via a circuit, and
19.b	wherein, in the second operable state, the second pre-regulated voltage is supplied to the voltage conversion circuit via the circuit.
20.a	20. The memory module of claim 19, wherein the circuit includes a first diode having a first input and a first output, the first input is coupled to the first pre-regulated voltage and the first output is coupled to the voltage conversion circuit, and

Ref. #	Listing of Challenged Claims
20.b	wherein the circuit includes a second diode having a second input and a second output, the second input is coupled to the second pre-regulated voltage and the second output is coupled to the first output and to the voltage conversion circuit.
21.a	21. The memory module of claim 16, further comprising:
21.b	a first circuit having a first input, a second input and an output, the first input coupled to a first pre-regulated voltage, the second input coupled to a second pre-regulated voltage, the output coupled to the voltage conversion circuit,
21.c	wherein the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a supply voltage,
21.d	wherein, in the first operable state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the first pre-regulated voltage, and
21.e	wherein, in the second state, the first circuit provides the supply voltage to the voltage conversion circuit via the output using the second pre-regulated voltage.
22	22. The memory module of claim 21, wherein the first circuit includes a first diode coupled between the first input and the output and a second diode coupled between the second input and the output.
23.a	23. The memory module of claim 16, wherein the voltage monitor circuit is configured to produce a trigger signal in response to detecting an amplitude change in the input voltage; and
23.b	wherein, in response to the trigger signal, the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory.
24.a	24. A memory module comprising:
24.b	a printed circuit board (PCB) having an interface configured to fit into a corresponding slot connector of a host system;
24.c	a voltage conversion circuit configured to provide a plurality of regulated voltages, wherein the voltage conversion circuit includes three buck converters each of which is configured to produce a regulated voltage of the plurality of regulated voltages;

Ref. #	Listing of Challenged Claims
24.d	[1] a plurality of components each coupled to at least one regulated voltage of the plurality of regulated voltages, [2] the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices, [3] wherein the plurality of SDRAM devices are coupled to a first regulated voltage of the plurality of regulated voltages; and
24.e	[1] a controller including a voltage monitor circuit coupled to an input voltage received from the host system via the interface of the PCB, the voltage monitor circuit configured to monitor the input voltage, [2] wherein the controller is configured to perform one or more operations in response to the voltage monitor circuit detecting an amplitude change in the input voltage, and [3] wherein the one or more operations include a write operation to transfer data into non-volatile memory.
25	25. The memory module of claim 24, wherein, in response to the voltage monitor circuit detecting an amplitude change in the input voltage, the memory module transitions from a first operable state to a second operable state.
26.a	26. The memory module of claim 25, wherein, in the first operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a first pre-regulated voltage, and
26.b	wherein, in the second operable state, the voltage conversion circuit provides the first regulated voltage to the plurality of SDRAM devices using a second pre-regulated voltage.
27	27. The memory module of claim 26, wherein the first pre-regulated voltage is coupled to the voltage conversion circuit via a first diode.
28	28. The memory module of claim 27, wherein the second pre-regulated voltage is coupled to the voltage conversion circuit via a second diode.
29	29. The memory module of claim 24, wherein the voltage monitor circuit is configured to detect the input voltage being above a first predetermined threshold voltage or below a second predetermined threshold voltage.

Ref. #	Listing of Challenged Claims
30	30. The memory module of claim 29, wherein the first predetermined threshold voltage is above a specified operating voltage, and the second predetermined threshold voltage is below the specified operating voltage.

I. PETITIONER'S MANDATORY NOTICES

A. Real Parties-in-Interest (37 C.F.R. § 42.8(b)(1))

The real parties in interest are the Petitioner, Samsung Electronics Co., Ltd.; and Samsung Semiconductor, Inc.

B. Related Matters (37 C.F.R. § 42.8(b)(2))

The following judicial or administrative matters would affect, or be affected by, a decision in this proceeding concerning U.S. Patent No. 11,232,054.

The following proceedings are currently pending:

- *Samsung Electronics Co., Ltd. et al. v. Netlist, Inc.*, No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- *Samsung Electronics Co., Ltd. v. Netlist, Inc.*, IPR2022-00996 (U.S. Patent No. 11,016,918)
- Application No. 17/582,797

The following proceeding is no longer pending:

- *SK hynix Inc. et al. v. Netlist, Inc.*, IPR2017-00692 (U.S. Patent No. 8,874,831)

C. Lead and Back-up Counsel (37 C.F.R. § 42.8(b)(3))

Lead Counsel is Eliot D. Williams (Reg. No. 50,822), DLSamsungNetlistIPRs@BakerBotts.com, (650) 739-7511, Baker Botts L.L.P., 1001 Page Mill Road, Building One, Suite 200, Palo Alto, CA 94304.

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D. Service Information (37 C.F.R. § 42.8(b)(4))

Service information is provided in the designation of counsel above. Petitioner consents to service of all documents via electronic mail to DLSamsungNetlistIPRs@BakerBotts.com.

II. INTRODUCTION

Petitioner respectfully requests trial on claims 1-30 of U.S. Patent 11,232,054 ("054 Patent") (EX1001) based on grounds not considered during prosecution.

III. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW

A. Standing (§42.104(a))

Petitioner certifies that the 054 Patent is available for IPR and that Petitioner is not barred or estopped from requesting an IPR challenging the 054 Patent claims on the grounds identified below.

B. Identification of Challenge (§42.104(b))

Petitioner challenges claims 1-30 of the 054 Patent as follows:

Ground	Claims Challenged	35 U.S.C. §	References
1	1-3, 15	103(a)	Harris + FBDIMM Standards
2	1-30	103(a)	Ground 1 + Amidi
3	1-30	103(a)	Ground 2 + Hajeck
4	1-30	103(a)	Spiers+Amidi
5	1-30	103(a)	Ground 4 + Hajeck

Petitioner's proposed claim constructions and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon is listed above on page vii.

IV. RELEVANT INFORMATION CONCERNING THE CONTESTED PATENT

A. Effective Filing Date of the 054 Patent

All the prior art in the Grounds above predate June 1, 2007, when the earliest provisional application for the 054 Patent was filed, but to the extent it matters, the claims of the 054 Patent do not appear to have support in any application filed before ***June 2, 2008***. EX1003, ¶¶47-60. For example, the claimed "voltage conversion circuit" with "three buck converters" lacks support in the earliest provisional, which just discloses a "step-down transformer 84." EX1005, ¶[0017]; EX1003, ¶¶51-54. Furthermore, there is no disclosure of a "dual buck converter" or a first or second "diode" in the earliest provisional as required by multiple claims. EX1003, ¶¶55-60.

B. The 054 Patent

1. Technical Overview

The 054 Patent describes a memory system 1010 that "can be coupled to a host computer system and can include a volatile memory subsystem 1030 [yellow], a non-volatile memory subsystem 1040 [green], and a controller 1062 [red] operatively coupled to the non-volatile memory subsystem 1040," as well as a "second power supply 1080" (blue) comprising either "capacitors" or a "battery" to

supply power during a power failure, as shown in Figure 12 (below).[1] EX1001, 21:16-20, 26:8-43; EX1003, ¶¶62-75.

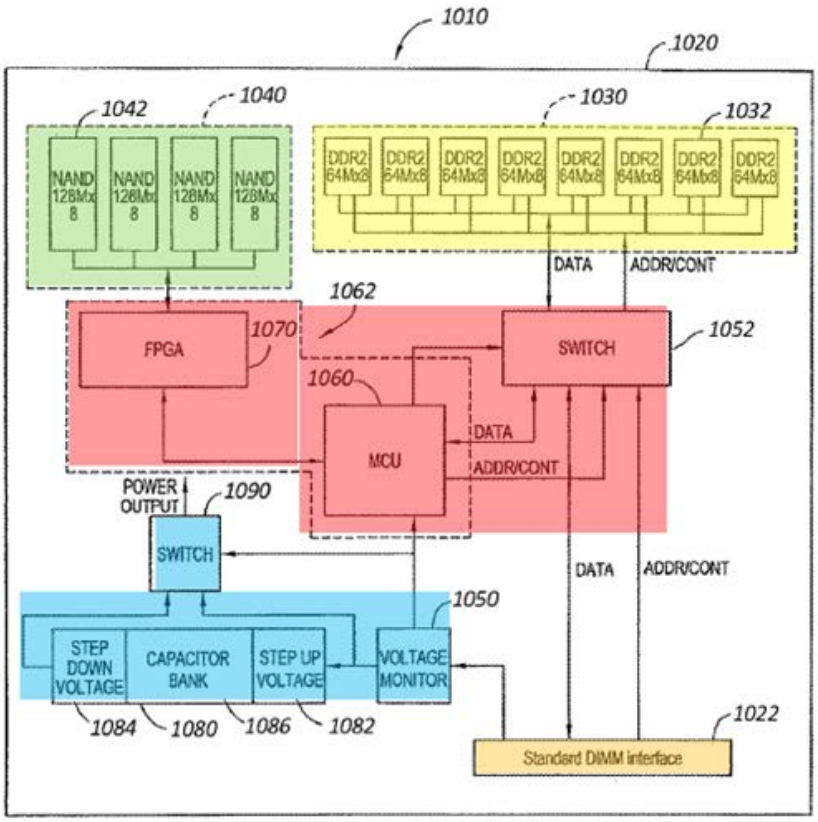


FIG. 12

In the event of a power failure detected by voltage monitor 1050, "[t]he controller [red] backs up the volatile memory [yellow] using the non-volatile memory [green]." EX1001, 20:21-24, 25:8-27.

[1] Unless stated otherwise, all emphasis in quotes and color annotations in figures have been added.

Figure 16 (below) illustrates a power module 1100 for the memory system above where "sub-block 1122 [below, right] comprises a buck converter, sub-block 1124 comprises a dual buck converter, and sub-block 1126 comprises a buck-boost converter" which output four different voltages (1102=1.8V, 1104=2.5V, 1105=1.2V, 1107=3.3V) to the components of the memory system. EX1001, 27:59-29:64.

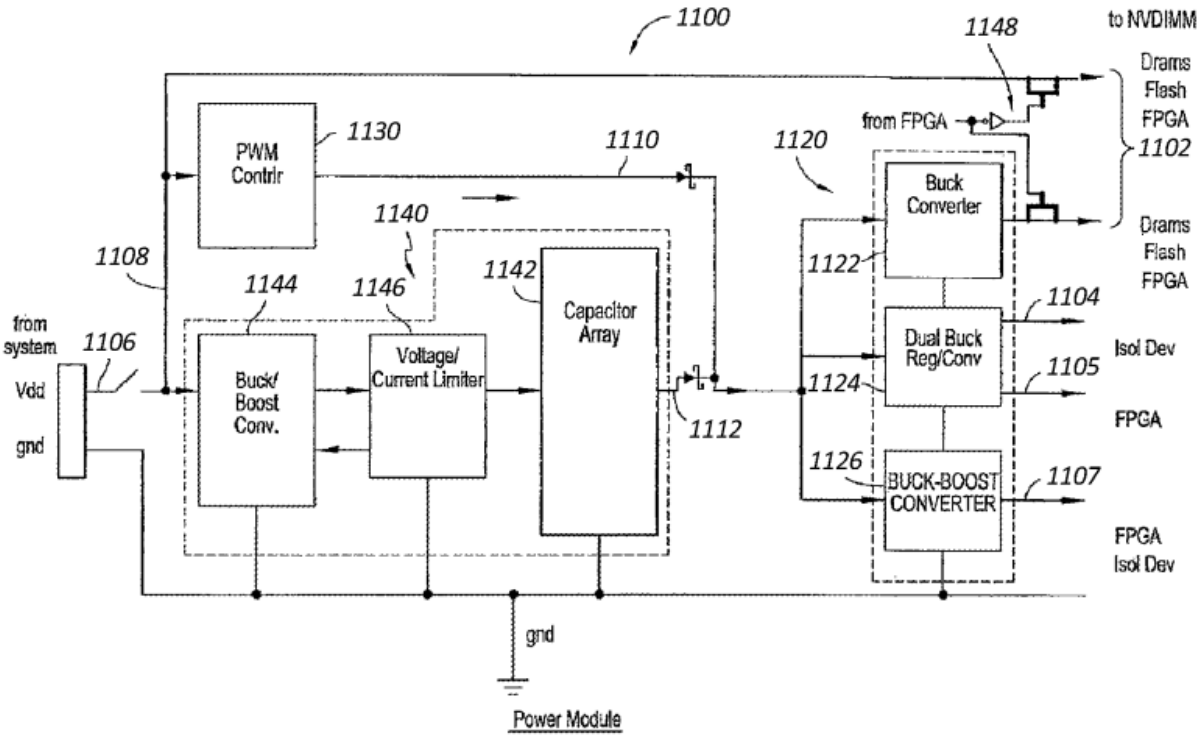


FIG. 16

2. Prosecution History and §325(d)

The 054 Patent was allowed after only one substantive office action, which included a double-patenting rejection based on the parent 918 patent. EX1002,

pp.359-69, 446-58, 471-78; EX1003, ¶¶122-127. The 054 Patent followed several earlier applications, including two resulting in patents that were later the subject of IPRs: the 833 and 831 patents. EX1003, ¶¶76-121. The claims of the 833 patent are directed to a different invention requiring "different frequencies depending on the mode of operation," as confirmed by an election during prosecution in response to a restriction requirement. EX1007, pp.120-33; EX1003, ¶¶81-83. The IPR against the 831 patent resulted in a Final Written Decision cancelling all claims. EX1020-21; EX1003, ¶¶93-97.

Advanced Bionics and §325(d) do not support discretionary denial given that the combinations cited by Petitioner were not presented to the Office, and no similar references were evaluated during prosecution. While two of the references relied on by Petitioner here (Spiers and JESD205) were marked "considered," both were buried in an IDS dumping over 100 references into the record, and neither was ever discussed. EX1002, pp.408, 428. Denial under §325(d) is thus unwarranted. *E.g., Thorne Research, Inc. v. Trustees of Dartmouth College*, IPR2021-00491, Paper 18 at 8-9 (PTAB Aug. 12, 2021).

C. Person of Ordinary Skill in the Art ("POSITA")

A POSITA in the field of the 054 Patent in 2008 would have had an advanced degree in electrical or computer engineering, or a related field, and two years working or studying in the field of design or development of memory

systems, or a bachelor's degree in such engineering disciplines and at least three years working in the field. EX1003, ¶61. Additional training can substitute for educational or research experience, and vice versa. Such a hypothetical person would have been familiar with the JEDEC industry standards, and knowledgeable about the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller and other parts of a computer system, including standard communication busses and protocols, such as PCI and SMBus busses and protocols. Such a hypothetical person would also have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs, FPGAs, and CPLDs, and more low-level circuits such as tri-state buffers. Such a hypothetical person would further have been familiar with voltage supply requirements of such structures (e.g., memory modules, memory devices, memory controller, and associated access and control circuitry), including voltage conversion and voltage regulation circuitry. *Id.*

D. Construction of Terms Used in the Claims

In related litigation, Patent Owner (Netlist) has interpreted some claim terms broadly for purposes of infringement, EX1071, pp.39-46; EX1073, pp.55-62, even though a narrower interpretation may be more reasonable, but Petitioner contends that no express constructions are needed for this proceeding because the claims are

obvious under either interpretation. EX1003, ¶128. It is likewise not necessary to determine whether any terms are governed by §112,¶6, given that for each claim at least one of the prior-art combinations matches the disclosure of the 054 Patent, as discussed below.

V. OVERVIEW OF THE PRIOR ART

A. Harris (EX1023)

U.S. Patent Publication No. 2006/0174140 ("Harris") was published August 3, 2006, and is prior art under §102(a). EX1023. Harris discloses an on-board voltage regulator (102) to convert an externally supplied voltage (104) to appropriate local voltage levels, such as "0.5V to 3.5V," for a wide variety of memory modules (100A), including "fully buffered DIMMs (FBDs)" standardized by JEDEC, comprising "known and heretofore unknown" types of DRAM memory devices (110-1 to 110-N), including those compatible with the DDR2, DDR3, and DDR4 JEDEC standards. *Id.*, Abstract, ¶¶[0009-13], Fig.1A (below); EX1003, ¶¶129-130.

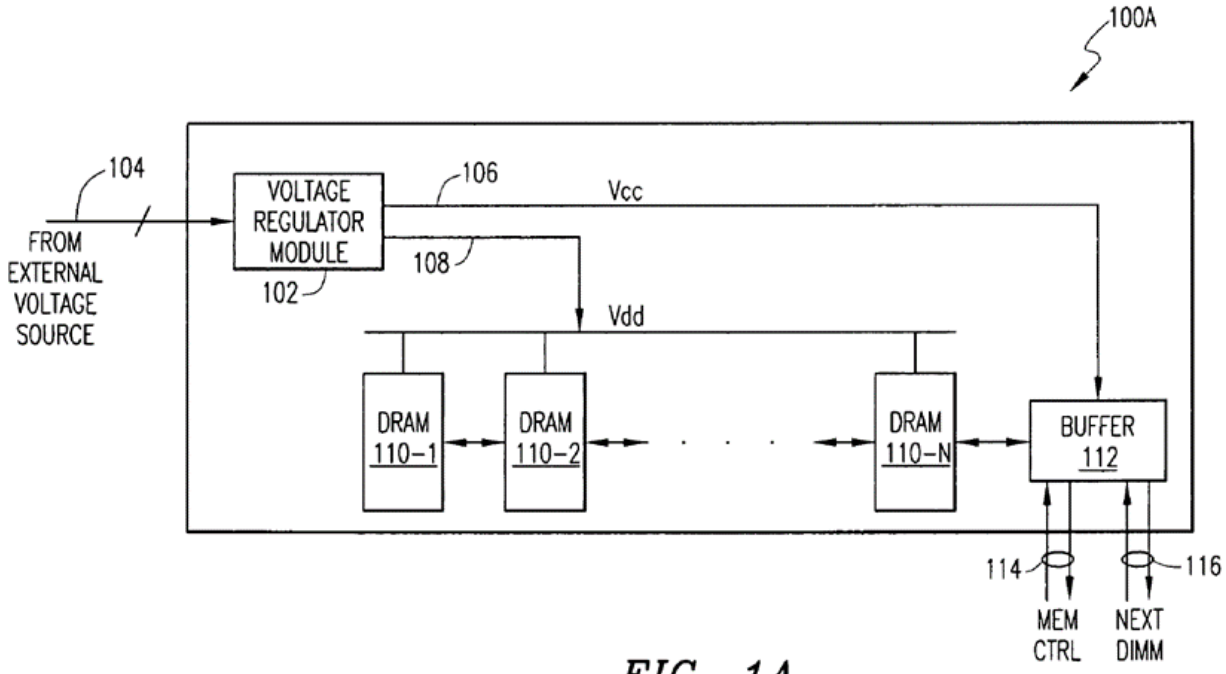


FIG. 1A

B. FBDIMM Standards (EX1027-28)

In March 2007, JEDEC published standards for Fully Buffered DIMM (FBDIMM) memory modules (compatible with Harris, above), including the "JESD82-20" (EX1027) and "JESD205" (EX1028) standards (collectively, "FBDIMM Standards"). *See* EX1029; EX1003, ¶¶134-137. The FBDIMM Standards are prior art under §102(a).

The FBDIMM Standards specify voltages for components on the memory module, including:

Supply voltages (nominal)	min	typ	max	
	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

EX1028, p.9. With respect to the "AMB buffer" on the memory module, the specified voltages include:

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

EX1027, p.83.

C. Amidi (EX1024)

U.S. Patent No. 7,724,604 ("Amidi"), filed October 25, 2006, is prior art under at least §102(e). EX1024. Amidi teaches monitoring the input voltage to a memory module so that in the event of a power fault, a battery can be used to supply the needed voltages to ensure "a stable power supply even in the face of disruptions." *Id.*, 4:14-22, 8:23-36, Fig.5 (below), Fig.14; EX1003, ¶¶131-132.

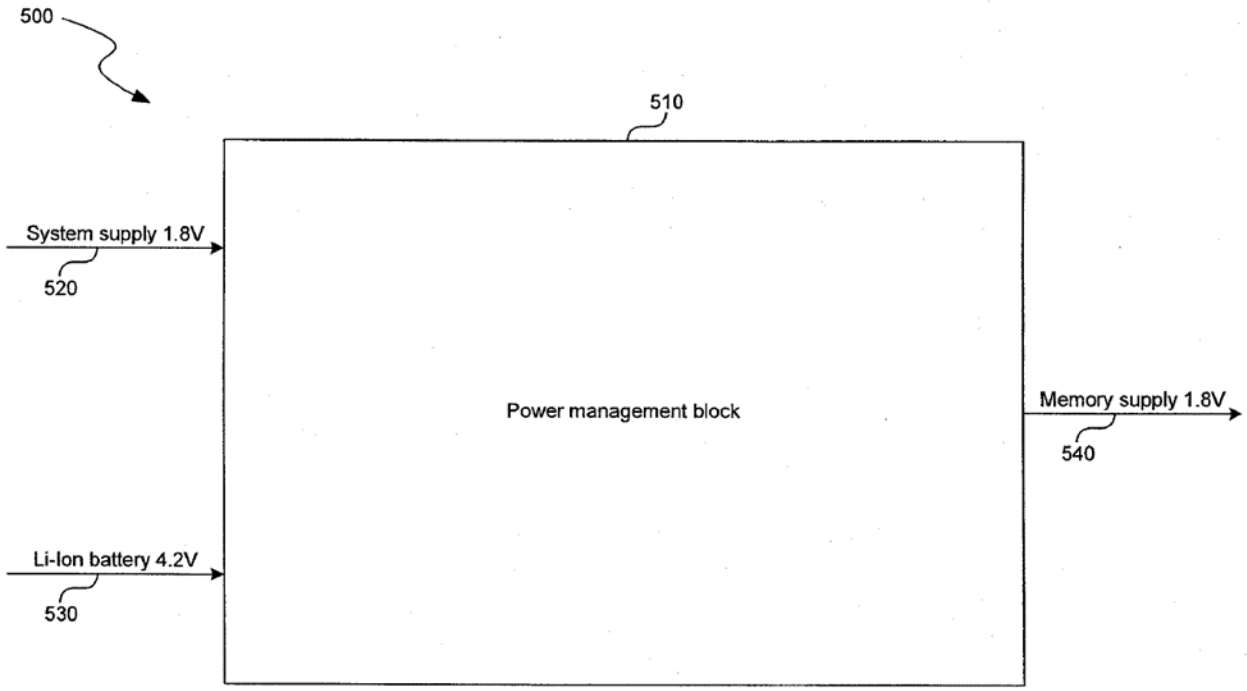


FIG. 5

D. Hajeck (EX1038)

U.S. Patent No. 6,856,556 ("Hajeck"), issued February 15, 2005, is prior art under §102(b). EX1038. Hajeck teaches a voltage detection circuit (48, red) to detect "anomalies" by monitoring the power input to a memory subsystem, including those with volatile and non-volatile memory. *Id.*, Abstract, 3:30-:39, 4:62-65, Fig.1 (below). Such anomalies include undervoltage, *see id.*, 3:34-37, and overvoltage, *see id.*, 3:37-39. EX1003, ¶138.

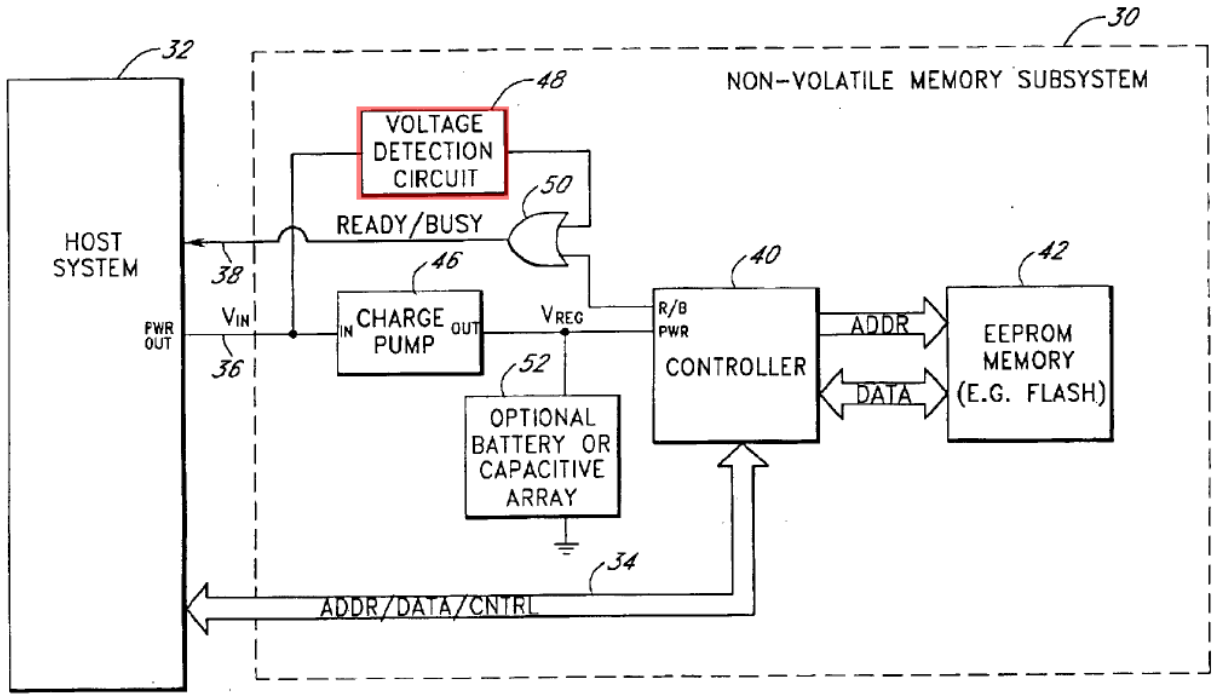
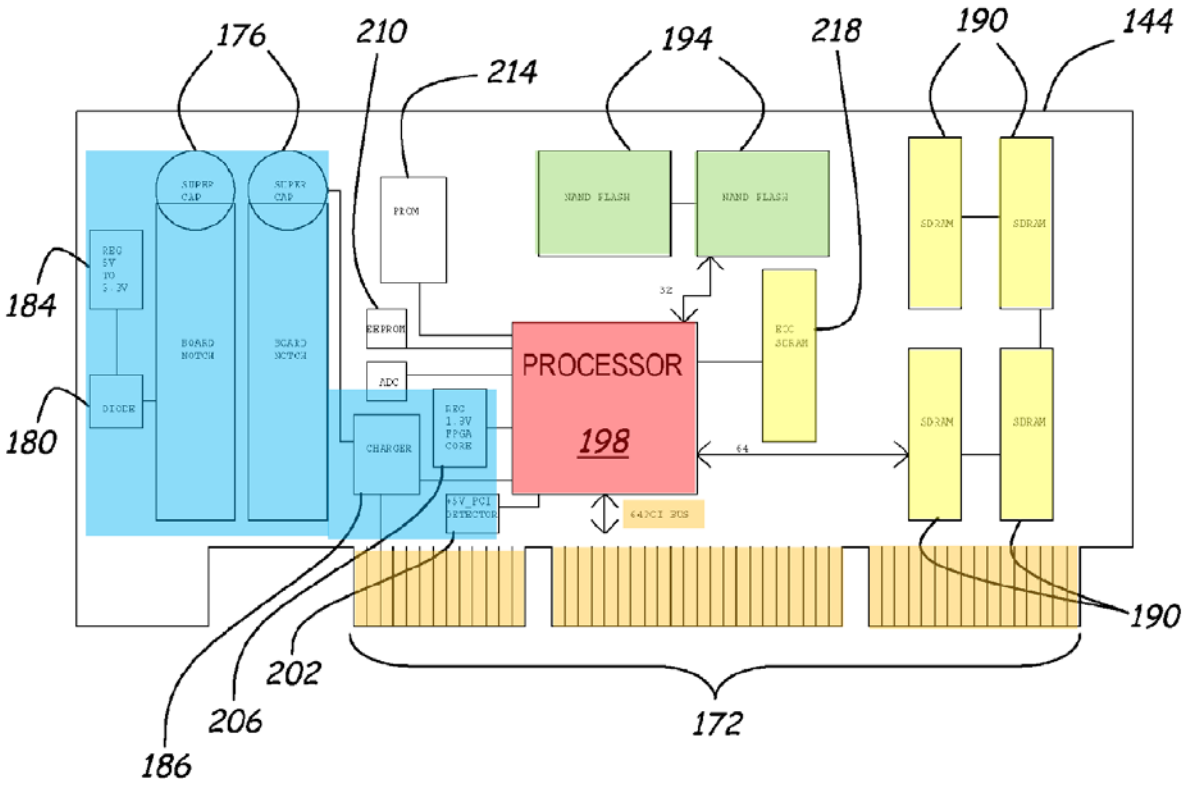


FIG. 1

E. Spiers (EX1025)

U.S. Patent Publication No. 2006/0080515 ("Spiers"), published April 13, 2006, is prior art under §102(b). EX1025. Spiers discloses a memory module (backup device 144) with both volatile (SDRAM) memory (190 and 218, yellow) and non-volatile (NAND flash) memory (194, green), as well as a temporary backup power supply (including capacitors 176, blue) and a processor (198, red) for "moving data from the volatile memory to the non-volatile memory" in the event of a power failure. *Id.*, ¶¶[0037-38], Fig.5 (below); EX1003, ¶133.



VI. ARGUMENT

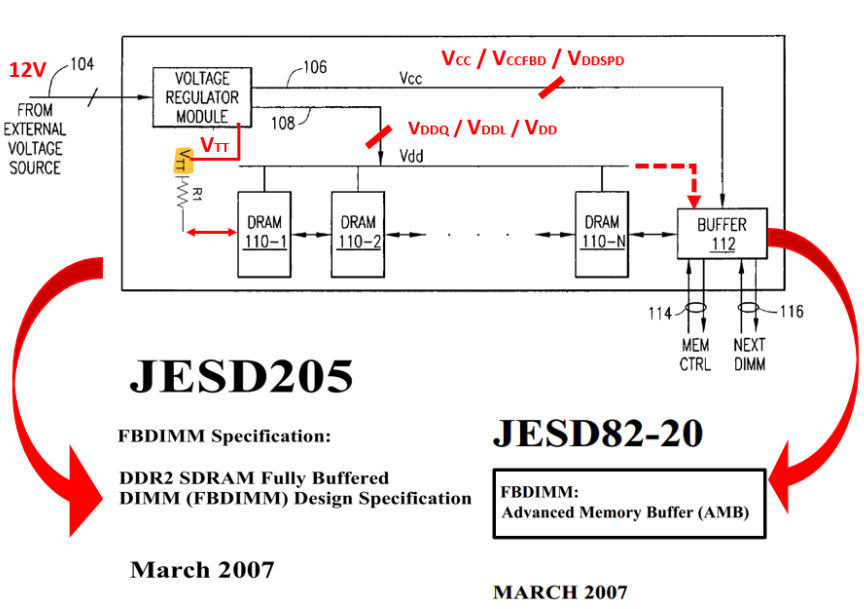
A. Ground 1

Ground 1 renders obvious claims 1-3 and 15.

1. Ground 1 combination: Harris (EX1023) + FBDIMM Standards (EX1027-28)

Ground 1 combines Harris with the FBDIMM Standards as follows:

Ground 1: Harris with JEDEC's FBDIMM Standards



JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

EX1003, ¶¶158-170. As explained below, the FBDIMM Standards specify particular voltages, and an embodiment of Harris's Voltage Regulator Module (upper left) can supply those voltages to various components on the memory module.

Harris recognized that "[a]s the performance of the DRAM technology goes up, and timing margins shrink, it is becoming increasingly more difficult for the ***system board*** [power] sources to provide tightly regulated power for the DRAM cores as well as input/output (I/O) interface buffers. Furthermore, each generation of DIMM/DRAM technology requires a different power supply which keeps getting lower (e.g., 3.3V, 2.5V, 1.8V, 1.5V and beyond), thereby making it difficult to mix memory technologies on a system board...." EX1023, ¶[0002].

Thus, Harris proposes "an ***on-board*** voltage regulator module to generate appropriate local voltage levels." *Id.*, ¶[0003].

A POSITA would have been motivated to combine Harris with the FBDIMM Standards, and had a reasonable expectation of success in doing so, because Harris expressly states that Figure 1A (above) is a "fully buffered DIMM" (i.e., FBDIMM or FBD), EX1023, ¶¶[0009-13], which a POSITA would have known refers to a particular type of memory module standardized by JEDEC's FBDIMM Standards, *id.*, ¶[0013]; EX1003, ¶¶158-166. Thus a POSITA would naturally look to the FBDIMM Standards for more details about the "fully buffered DIMM" that Harris describes as compatible with his "at least one on-board voltage regulator module (VRM)." *Id.*; EX1023, ¶[0010].

As summarized in the annotated figure above, the FBDIMM Standards specify particular voltages for various components on an FBDIMM, including those below, and thus a POSITA would have been motivated to implement Harris's Voltage Regulator Module (above left) to supply all the voltages below. EX1003, ¶¶167-170.

- 1.5V for V_{CC} and V_{CCFBD} to the "AMB" Buffer (112 above).
- 3.3V for V_{DDSPD} to the Buffer and the SPD ("Serial Presence Detect," EX1028, p.105) (not shown above).
- 1.8V for V_{DDQ}/V_{DD} to the Buffer.

- 1.8V for **V_{DDQ}**, **V_{DDL}**, and **V_{DD}** to the "DDR2" DRAM (110-1 to 110-N above).
- 0.9V for **V_{TT}** to the resistors, DRAM, and Buffer.

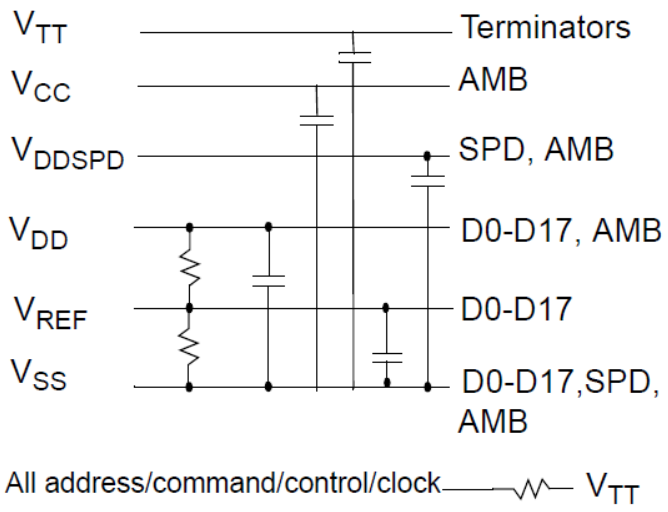
See EX1023, ¶¶[0002-3, 9-10, 17], Figs.1A, 3; EX1028, p.9 (below); *id.*, pp.11-16, 17-20 (V_{DDL}), 30-33, 68; EX1026, pp.6-7 (V_{DDL}, V_{DD}).

	min	typ	max	
Supply voltages (nominal)	1.7	1.8	1.9	(DRAM V_{DD}/V_{DDQ}, AMB V_{DDQ})
	1.455[1]	1.5	1.575[1]	(AMB V_{CC}/V_{CCFBD})
	0.453*V_{DD}	0.5*V_{DD}	0.547*V_{DD}	(DRAM Interface V_{TT}) This supply should track as 0.5 * 1.8 volt supply
	3.0	3.3	3.6	(V_{DDSPD})

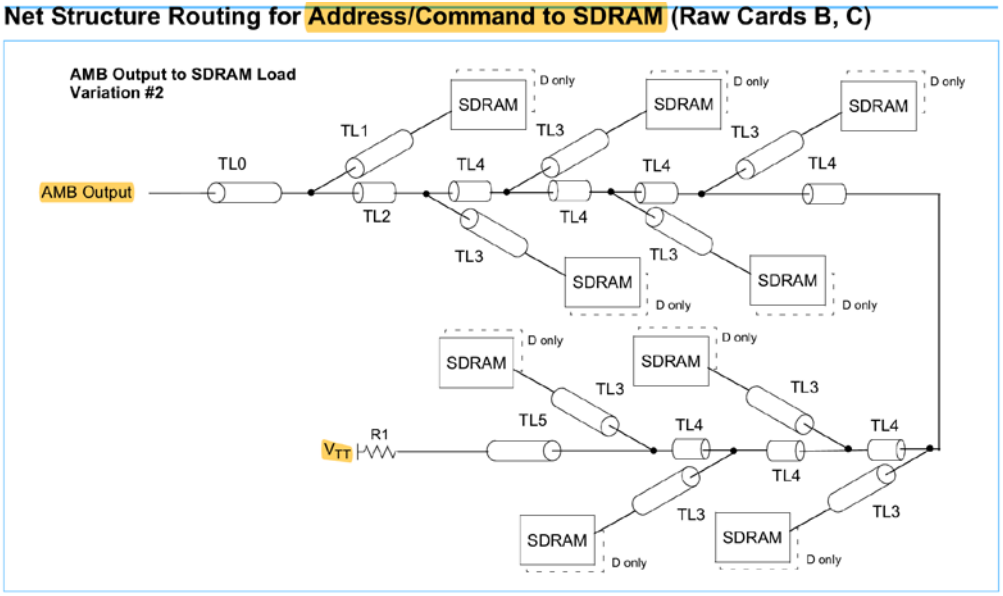
See also EX1027, p.83 (below, for the AMB Buffer); *id.* pp.31-32, 44, 78, 82-83; EX1023, ¶[0017], Fig.3 (V_{DDSPD}).

Power Supplies		
VCC (24 pins)	A	1.5V nominal supply for core IO
VCCFBD (8 pins)	A	1.5V nominal supply for FBD high speed IO
VDD (24 pins)	A	1.8V nominal supply for DDR IO
VSS (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes

See also, e.g., EX1028, p.15:



Id., p.68:



In the annotated figure for Ground 1 above (p.15), Voltage Mappings "A" to "C" (on the right) are simply different ways to apply the arbitrary labels "1st" through "3rd" to the voltages shown in red in the annotated figure. EX1003, ¶¶167-170.

Below, Ground 1A refers to Ground 1 above with Voltage Mapping "A," while Grounds 1B and 1C refer to Ground 1 above with Voltage Mappings "B" and "C," respectively. *Id.*

2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Grounds 1A-1C teach "*[a] memory module* [e.g., Harris's "memory module 100A" in Fig.1A, and 306 (below)] *comprising.*" EX1023, ¶¶[0009, 17, 20], Figs.1A, 3; EX1003, ¶¶217-223.

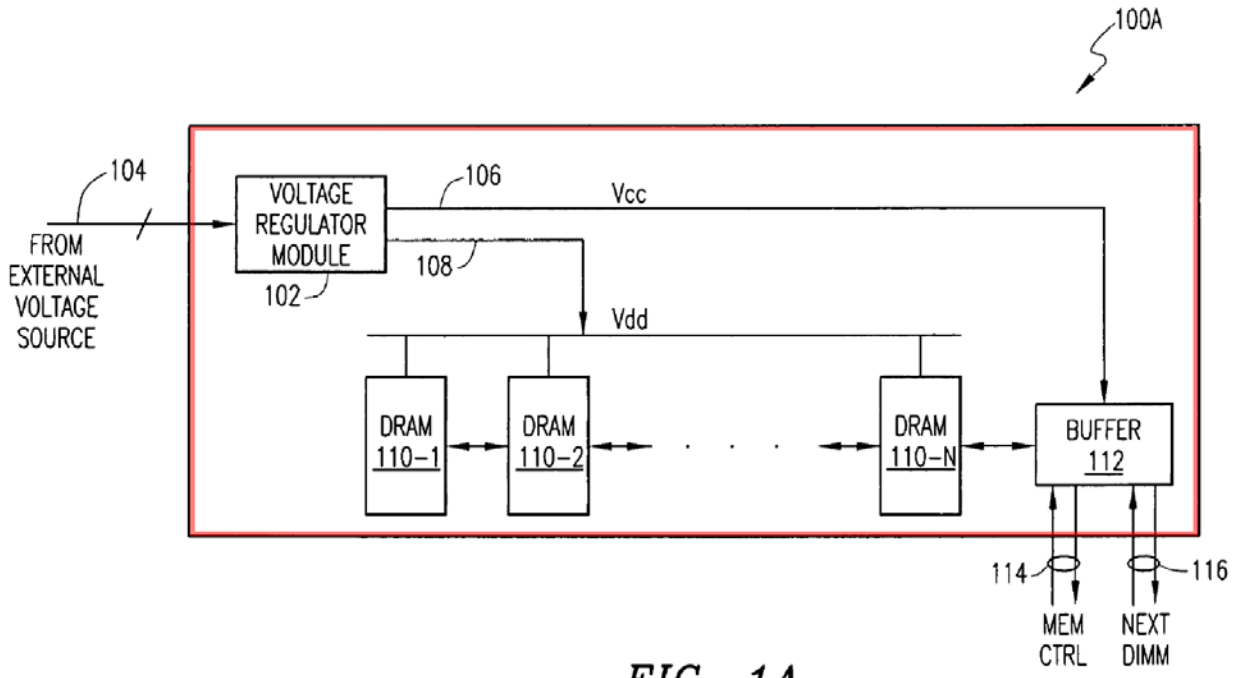


FIG. 1A

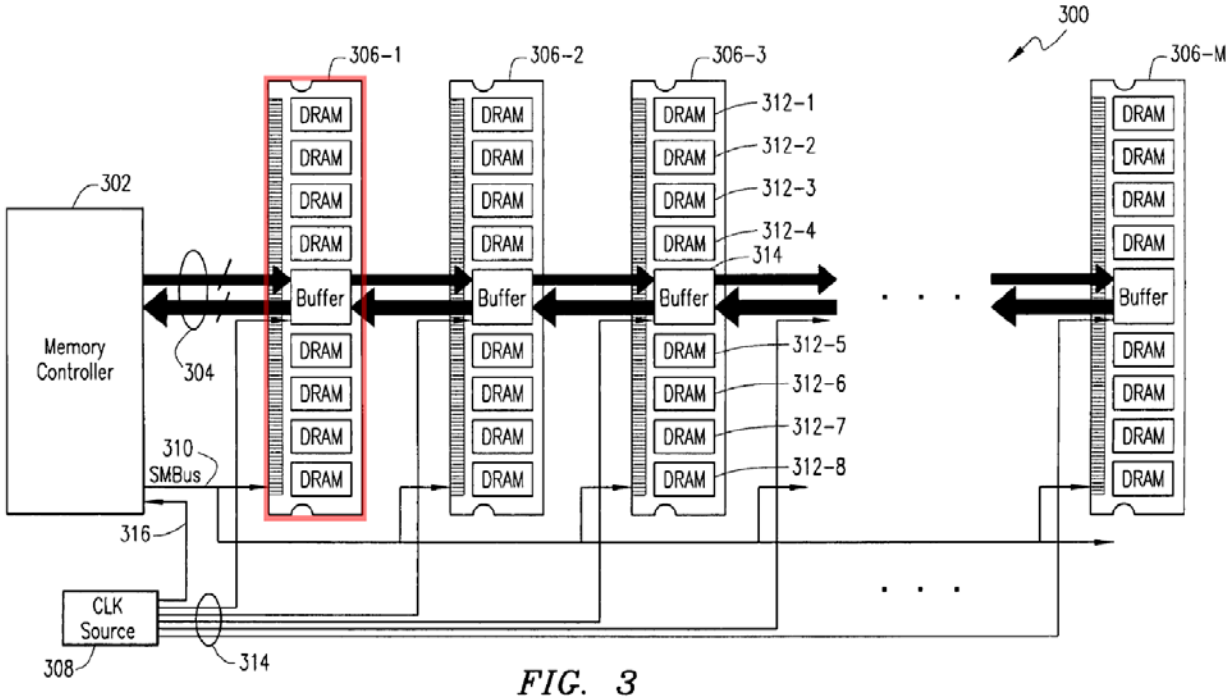
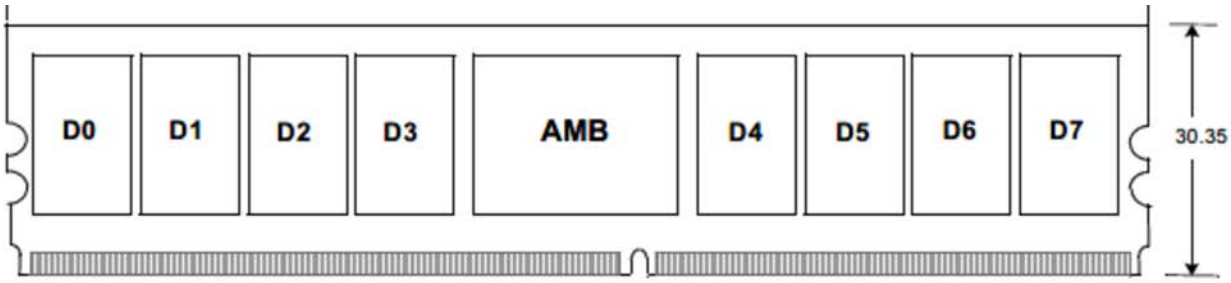


FIG. 3

A POSITA would have recognized the FBDIMM "*memory module[s]*" disclosed by Harris (above) are similar to the "*memory module[s]*" disclosed in JEDEC's FBDIMM Standards (e.g., below):



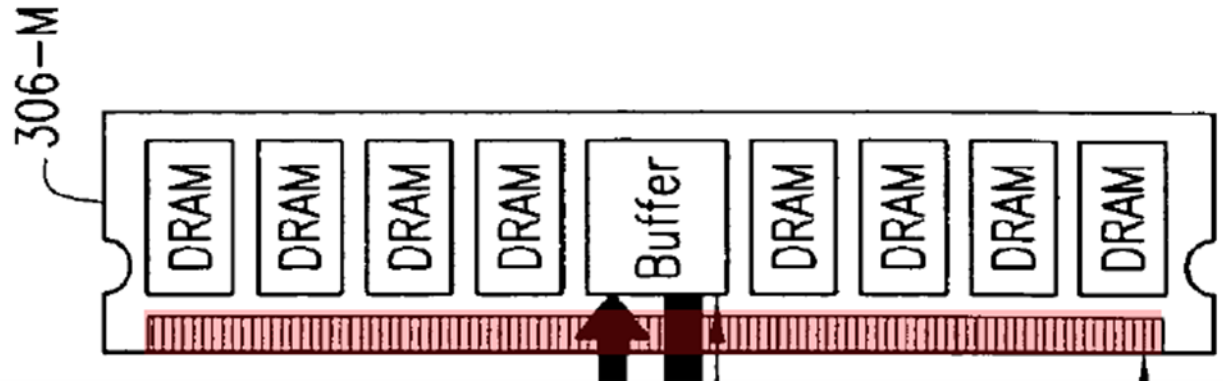
EX1028, p.38; EX1003, ¶222.

b) [1.b] Printed Circuit Board (PCB)

Grounds 1A-1C teach "*a printed circuit board (PCB),*" as shown above for [1.a]. *See also* EX1023, ¶[0013] ("printed circuit board"), ¶[0009] ("memory

board"), Figs.1A, 3; EX1028, pp.10 ("PCBs are called … 'raw cards'"), 38, 84; EX1003, ¶¶224-226.

Grounds 1A-1C teach the PCB "*having an interface configured to fit into a corresponding slot connector of a host system, the interface including a plurality of edge connections*" (sometimes called "pins") as shown above for [1.a] and reprinted below from Harris's Figure 3. EX1023, ¶¶[0002, 12-13, 19], Figs. 3-4; EX1028, pp.38, 84; EX1003, ¶¶227-228.



Grounds 1A-1C teach the edge connections in Harris, consistent with JEDEC's FBDIMM Standards, are "*configured to couple power, data, address and control signals between the memory module and the host system*":

- "*power*": EX1023, ¶[0012] ("power"/"+12V" "pins"); *id.*, ¶¶[0010, 19] & Fig.1A (104, below).

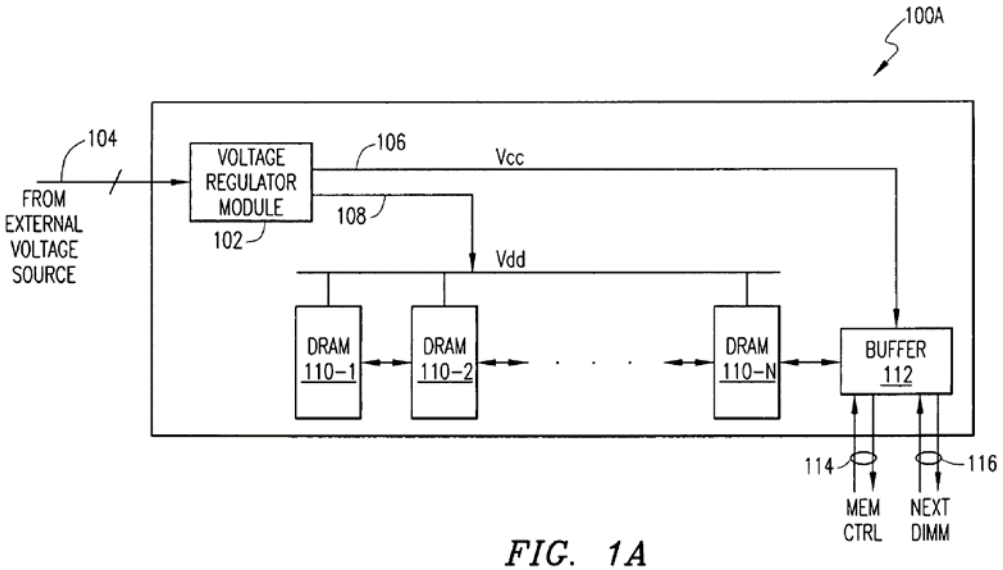
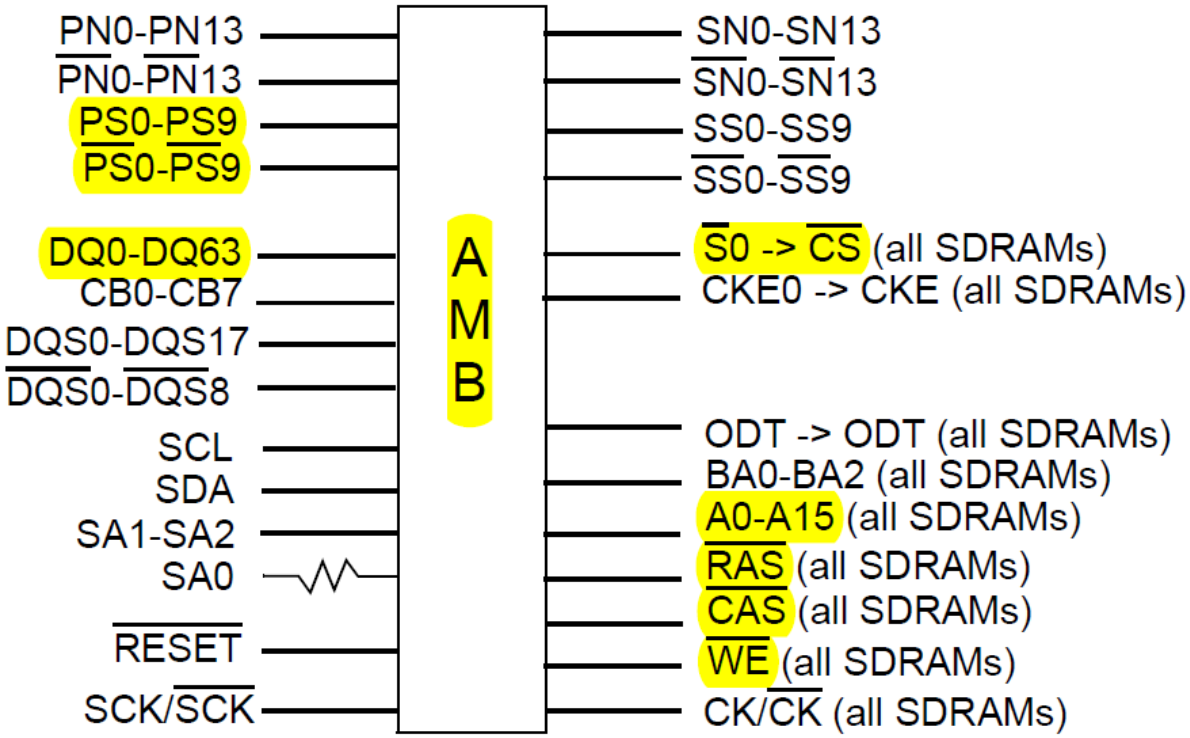


FIG. 1A

Furthermore, as shown in Figure 1A above, Buffer 112 (called "AMB" in the FBDIMM Standards) receives via 114 and transmits to DRAMs 110-1 to 110-N the following signals (as shown below and consistent with JEDEC standards):

- "*data*": e.g., DQ0-DQ63 (below); EX1023, ¶[0009] ("buffer/logic component 112 is provided for buffering command/***address*** (C/A) space as well as ***data*** space at least for a portion of the memory devices 110-1 through 110-N")
- "*address*": e.g., A0-A15 (below); *id.* ("***address***")
- "*control*": e.g., RAS, CAS, WE, CS (below); *id.* & Fig.1A (114, "CTRL"). These "*control*" signals together can form a "command." *See, e.g.*, EX1028, p.29 ("Part of command"); EX1026, pp.6 ("define the command"), 46-47, 52.

See also EX1023, ¶¶[0009-12, 17, 19], Figs.1A, 3; EX1028, pp.11, 13 (below), 29; EX1027, pp.1 (AMB "[a]cts as DRAM memory buffer for all read, write, and configuration accesses addressed to the DIMM"), 3-4 (below), 7, 81-82; EX1026, pp.6, 46-47, 52; EX1003, ¶¶229-232.



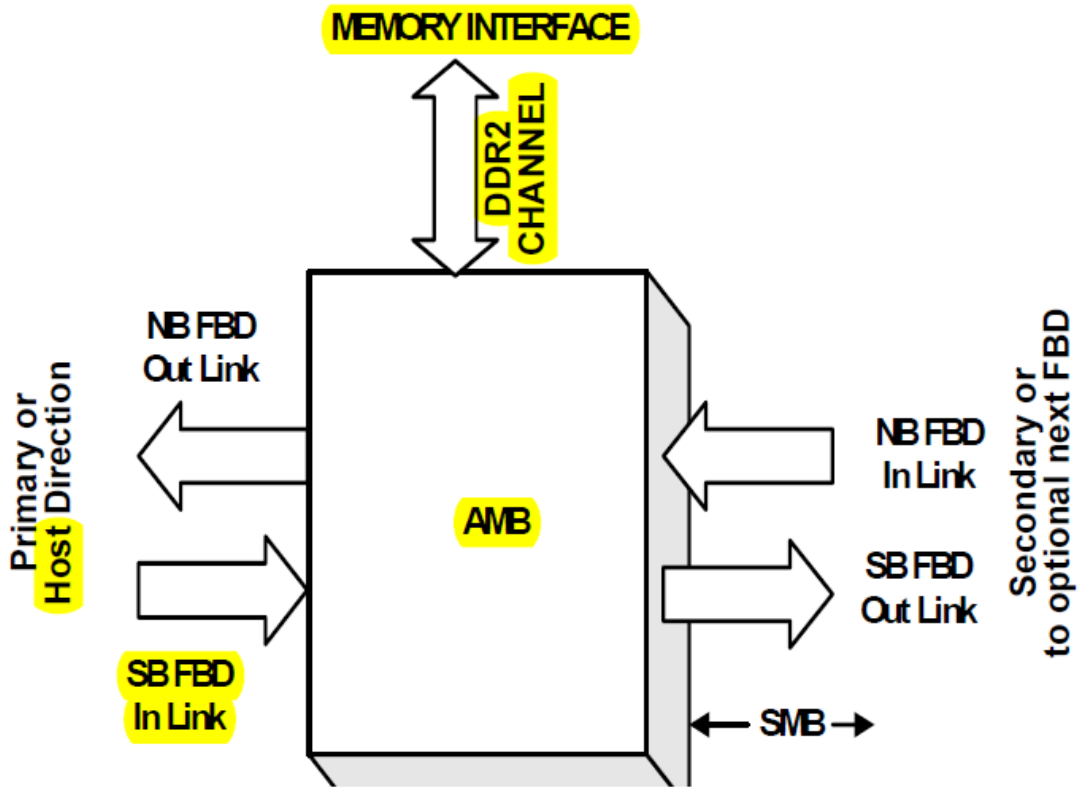


Figure 1.2 — Advanced Memory Buffer Interfaces

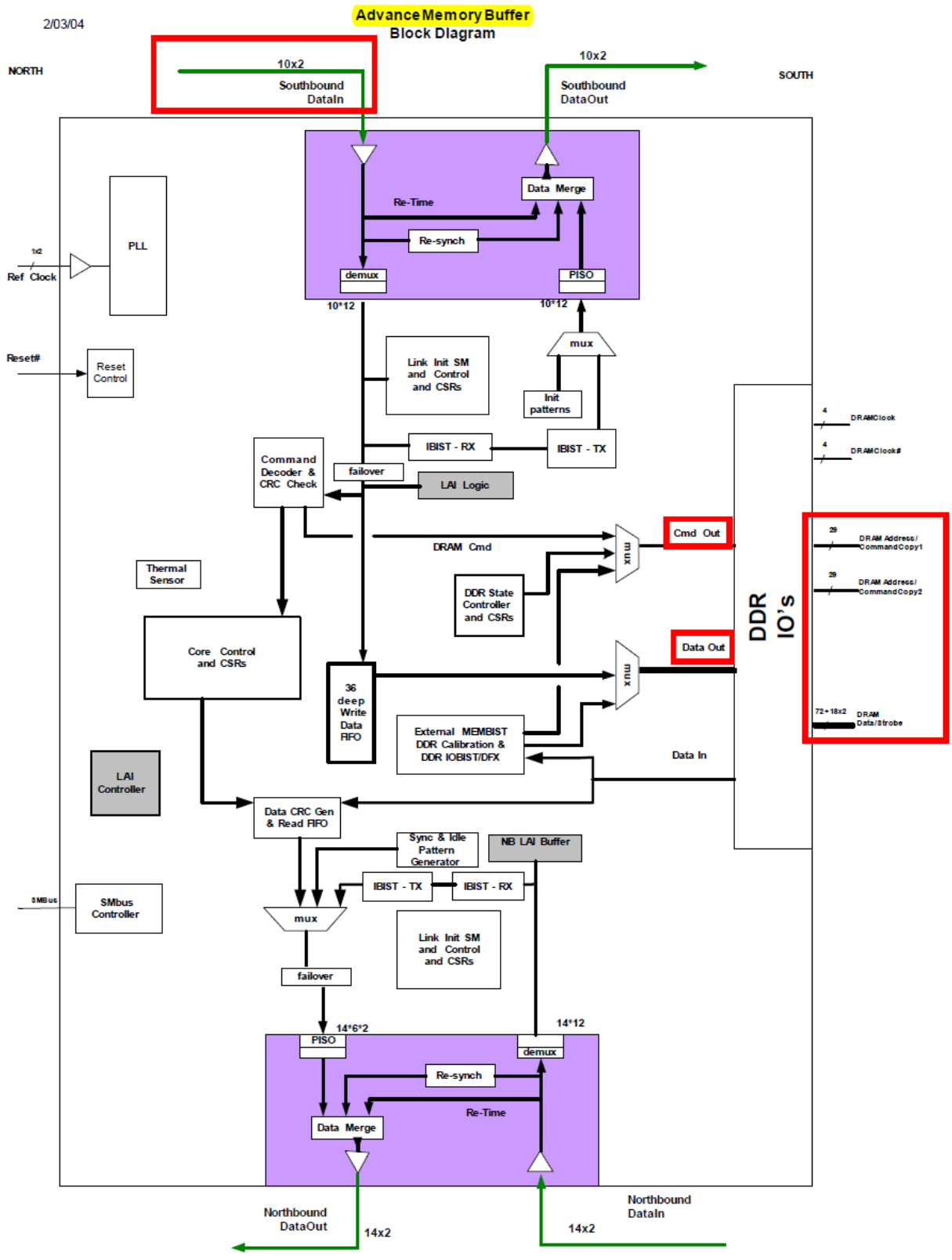
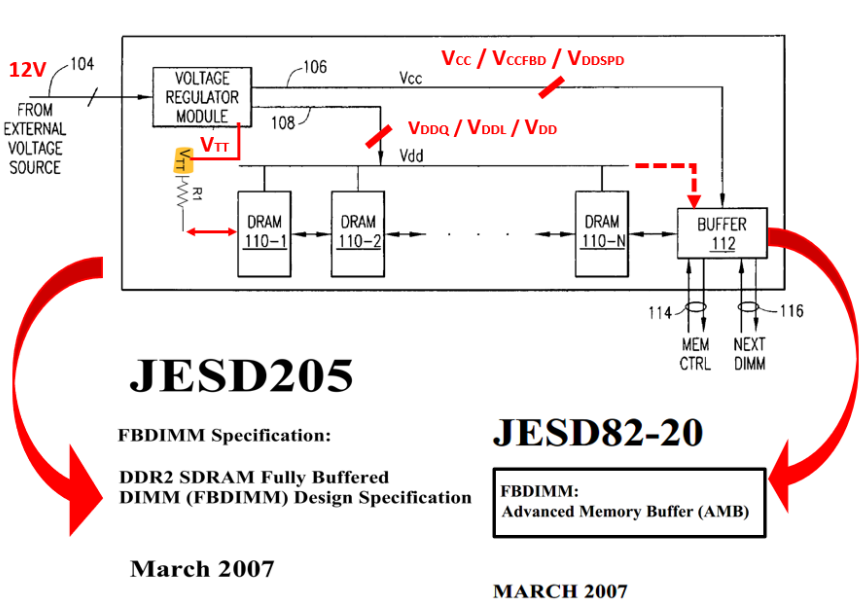


Figure 1.1 — Advanced Memory Buffer Block Diagram

c) [1.c] A Voltage Conversion Circuit

Grounds 1A-1C teach "*a voltage conversion circuit* [e.g., Voltage Regulator Module 102, EX1023, ¶[0010], Fig.1A] *coupled to the PCB* [see *id.*] *and configured to provide at least three regulated voltages* ["1st"/"*first*"; "2nd"/"*second*"; "3rd"/"*third*" below], *wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*":

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{DDL} = 1.8V

Voltage Mapping (B)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} = 1.5V
3rd : V_{CCFBD} = 1.5V

Voltage Mapping (C)
1st : V_{DD} / V_{DDQ} = 1.8V
2nd : V_{CC} / V_{CCFBD} = 1.5V
3rd : V_{TT} = 0.9V

See supra pp.14-19; EX1003, ¶¶233-260.

	Voltage Mappings (Grounds 1-3)		
	A	B	C
"*first*":	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V	V_{DD} or V_{DDQ} = 1.8V
"*second*":	V_{CC} or V_{CCFBD} = 1.5V	V_{CC}=1.5V	V_{CC} or V_{CCFBD} = 1.5V
"*third*":	V_{DDL}=1.8V	V_{CCFBD}=1.5V	V_{TT}=0.9V

Id.

As shown above, Grounds 1A-1B have two voltage amplitudes that are the same, consistent with Netlist's broad interpretation, EX1073, pp.59-61, while Ground 1C does not, consistent with a narrower interpretation.

Furthermore, Harris also discloses a range of voltages — "from about 0.5V to 3.5V or more," EX1023, ¶[0009] — as do the FBDIMM Standards, and thus any combination of "*first*" to "*third*" voltages in that range would have been obvious: "Where a prior art patent discloses a range of values, showing a claimed value falls within that range meets a party's burden of establishing the narrower claim would have been obvious where there is no reason to think the result would be unpredictable." *Gen. Hosp. Corp. v. Sienna Biopharms., Inc.*, 888 F.3d 1368, 1373 (Fed. Cir. 2018); *see also, e.g.*, *Iron Grip Barbell Co. v. USA Sports, Inc.*, 392 F.3d 1317, 1320-23 (Fed. Cir. 2004) (claim to three grips obvious in light of prior art teaching one, two, and four grips).

Harris teaches that the voltages above would be "*regulated*": Harris identifies "tightly ***regulated*** power" on the memory module as a problem to be solved, and proposes "at least one ***on-board*** voltage ***regulator***" that is "capable of generating ***tightly-controlled*** voltage levels" as the solution. EX1023, ¶¶[0002-3, 0009-11]; EX1003, ¶236.

Harris also teaches using "*buck converters*" to provide the three regulated voltages above. EX1003, ¶¶238-241. Harris discloses using "+12V pins (from an external voltage source)" and "a ***high-frequency switching voltage converter*** capable of generating tightly-controlled voltage levels" to provide each needed on-board regulated voltage. EX1023, ¶¶[0012, 0010]. A "buck converter" was a conventional device for implementing such a "***voltage-reducing switching converter***." EX1030, 2:41-43. Furthermore, it would have been obvious to a POSITA to use a "*buck converter*" to convert the higher input voltage (e.g., 12V) to the lower output voltage (e.g., 3.5V or less), and there would have been a reasonable expectation of success, given that buck converters were well-known "switching" devices commonly used to step down the voltage between its input and output, as had long been taught in textbooks. EX1003, ¶¶147-150, 239-241; EX1058 (Lenk textbook from 1995), pp.3 ("Figure 1-3 shows three typical MOSFET ***switching-regulator (or -converter)*** circuits, representing the three basic configurations: ***buck***, *boost*, and *buck-boost*…. The ***buck*** circuit is used when the

input voltage is always greater than the desired output voltage (and is also known as a *step-down* converter)."), 5 ("1.3 Switching-Regulator Theory"), 12-16 ("1.5.4 Buck or Step-Down"); EX1032 (Mohan textbook from 1995), pp.161 (identifying "Step-down ***(buck) converter***" as a "basic converter topolog[y]."), 164 ("step-down converter"); EX1030, 2:32-43, 5:39-44; EX1024 (Amidi) Fig.6 (showing "DC/DC ***buck***" converter 640 to step down a higher voltage to a lower one); EX1050, 1:21 (identifying buck converters as one of "the most basic building blocks in power electronics").

Further, "buck converters" were well-known as a ***highly-efficient*** way to step down voltages without generating excess heat or requiring large cooling devices, providing a further motivation (beyond Harris's express disclosure above) to implement Harris's voltage regulator using "*[buck] converter[s]*." EX1003, ¶240; EX1059, 5:23-30 ("***Switch mode buck converters*** … are ***more efficient*** … ***with lower power dissipation***…."); EX1058, p.5 (explaining the "***high efficiency*** of switching regulators"); *see also, e.g.*, EX1040, pp.1 ("high efficiency"), 23-24 (Figs.22-25); EX1041, pp. 1, 13 ("high efficiency"); EX1048, p.3; EX1062, p.11; EX1064, ¶[0101].

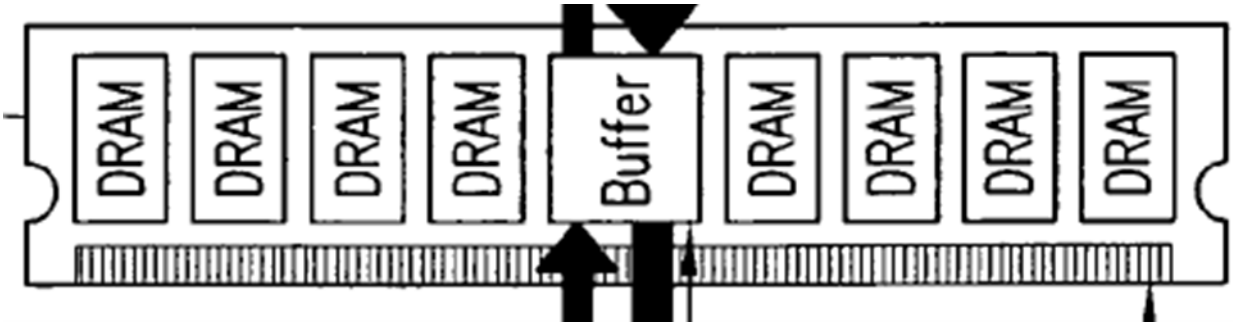
It would have been obvious to use at least ***three*** converters in Harris given the need for at least ***three*** different voltages in the FBDIMM Standards (e.g., 0.9V, 1.5V, 1.8V), as discussed above (pp.14-19) and as shown in Voltage Mapping C.

Furthermore, with respect to Voltage Mappings A and B (where two of the voltages are the same amplitude, either 1.5V or 1.8V), it also would have been obvious to use ***three*** converters because the two voltages with the same amplitude are ***separate*** voltages in the FBDIMM Standards as discussed above (pp.14-19). In particular, although V_{DD} and V_{DDQ} and V_{DDL} are all 1.8V, they are expressly identified as separate voltages with separate pins, *see, e.g.*, EX1028, pp.17-20, and JEDEC states that in one implementation they can be turned on and off separately, EX1026, p.9, and that V_{DDL} should use an isolated voltage source, *id.*, pp.2-3, providing a motivation to use separate converters for those voltages so that they can be controlled separately. EX1003, ¶¶248-249; *see also*, *e.g.*, EX1062, p.13 ("[A] particular standard voltage level may have to be ***independently*** furnished in numerous places …. to improve efficiency … or to meet sequencing requirements…."). Similarly, although V_{CC} and V_{CCFBD} are both 1.5V, they are expressly identified as separate voltages with separate pins, *see, e.g.*, EX1028, pp.30-32, which a POSITA would have understood provides independence for these power supplies to allow improved stability for each supply and flexibility for power management, providing a motivation to use separate converters for those voltages so that they can be controlled separately. EX1003, ¶255.

d) [1.d] A Plurality of Components Coupled to the PCB

(1) [1.d.1] Plurality of components each coupled to at least one regulated voltage

Grounds 1A-1C teach "*a plurality of components coupled to the PCB* [e.g., a Buffer and DRAMs (as shown in Harris's Figure 3, below) and an SPD and resistors, as discussed above, pp.14-19], *each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages* [as shown above, pp.14-19]." EX1003, ¶¶261-266.



(2) [1.d.2] Plurality of components includes SDRAM devices

Grounds 1A-1C teach that "*the plurality of components includ[es] a plurality of synchronous dynamic random access memory (SDRAM) devices* [e.g., Harris's "Double Data Rate (DDR) dynamic random access memory (DRAM) device[s]" 110-1 to 110-N, *see* EX1023, ¶¶[0009, 11], Figs.1A, 3]." EX1003, ¶¶267-271. A POSITA would know that according to the JEDEC standards, "DDR" memory devices are "*synchronous*" DRAM (i.e., SDRAM). *Id.*; EX1028, p.9 ("Double Data Rate ***Synchronous*** DRAM … ***S***DRAM"); EX1045, p.Cover

("(DDR) **S**DRAM"); EX1026, p.Cover-1 ("DDR2 **S**DRAM"); EX1046, p.Cover ("DDR3 **S**DRAM").

(3) [1.d.3] A first circuit coupled to the SDRAM devices and first set of edge connections

Grounds 1A-1C teach "*a first circuit* [e.g., Harris's "Buffer," red below, which is coupled to receive data, address, and control signals via 114 across the edge connections, and transmits them to DRAMs 110-1 to 110-N, as discussed in [1.b] above (pp.20-25)] *that is coupled to the plurality of SDRAM devices* [see [1.d.2] directly above] *and to a first set of edge connections of the plurality of edge connections* [see [1.b] (pp.20-25)]." EX1003, ¶¶272-277.

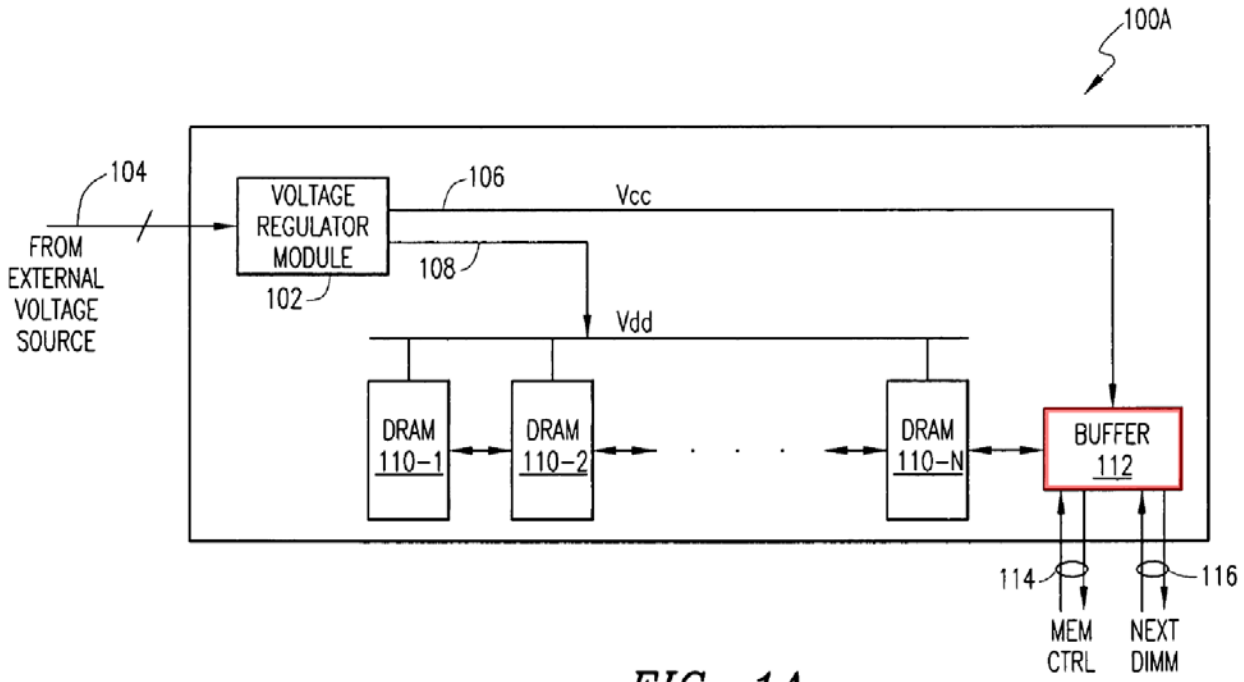


FIG. 1A

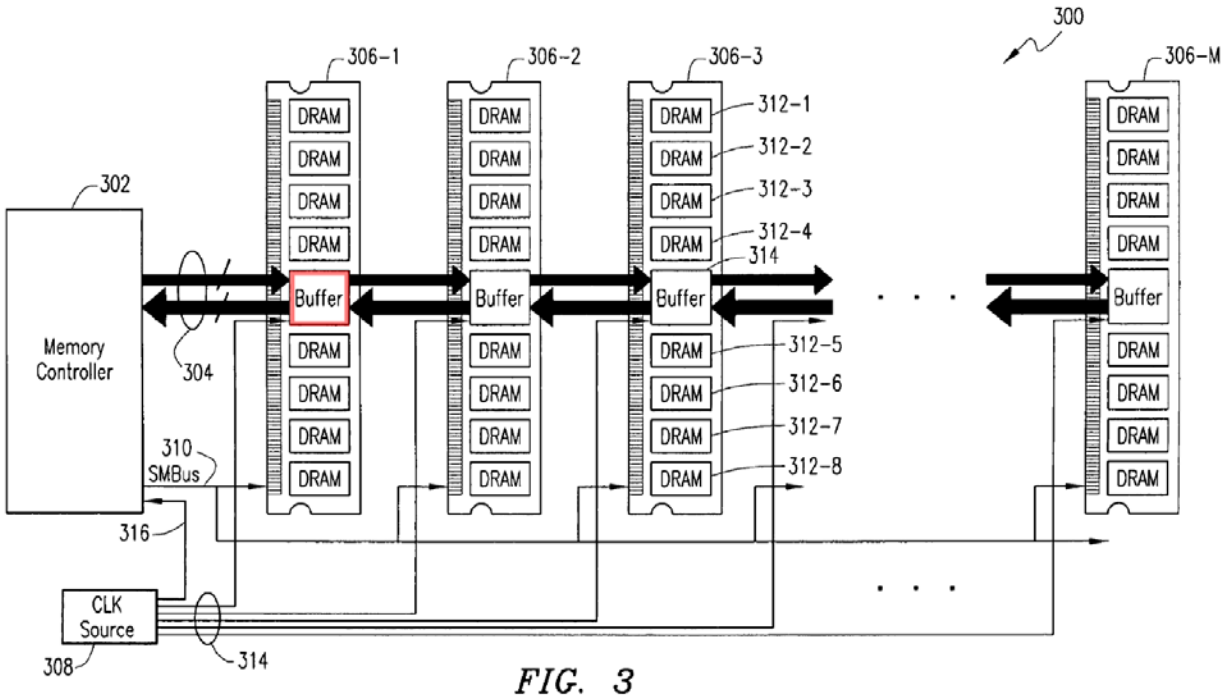
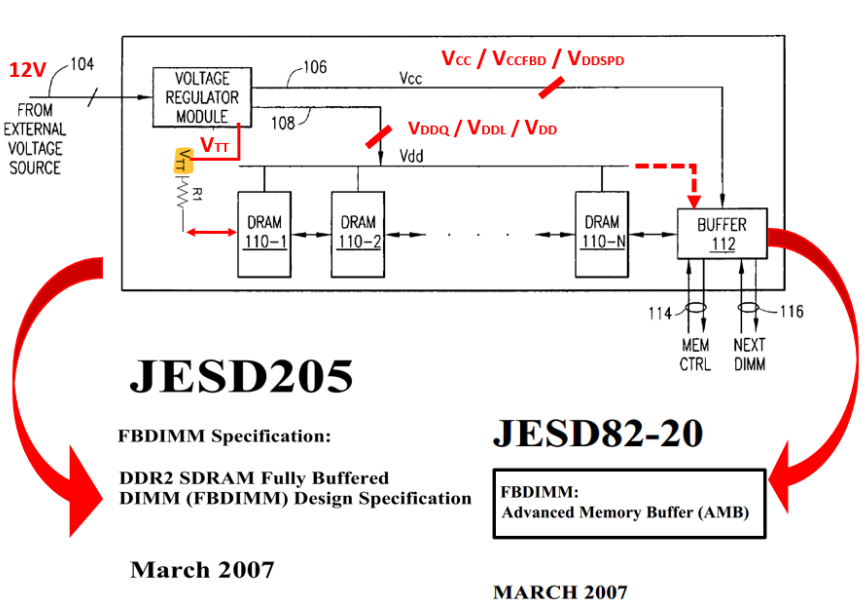


FIG. 3

(4) [1.d.4] Wherein the first circuit is coupled to first and second regulated voltages

Grounds 1A-1C teach "*the first circuit* [e.g., Harris's "Buffer"] *is coupled to first* [e.g., V_{DD} or V_{DDQ} = 1.8V] *and second* [e.g., V_{CC} or V_{CCFBD} = 1.5V] *regulated voltages of the at least three regulated voltages*," as shown below and discussed above (pp.14-19, 27). EX1003, ¶¶278-284.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

JESD205

FBDIMM Specification:

DDR2 SDRAM Fully Buffered DIMM (FBDIMM) Design Specification

March 2007

JESD82-20

FBDIMM: Advanced Memory Buffer (AMB)

MARCH 2007

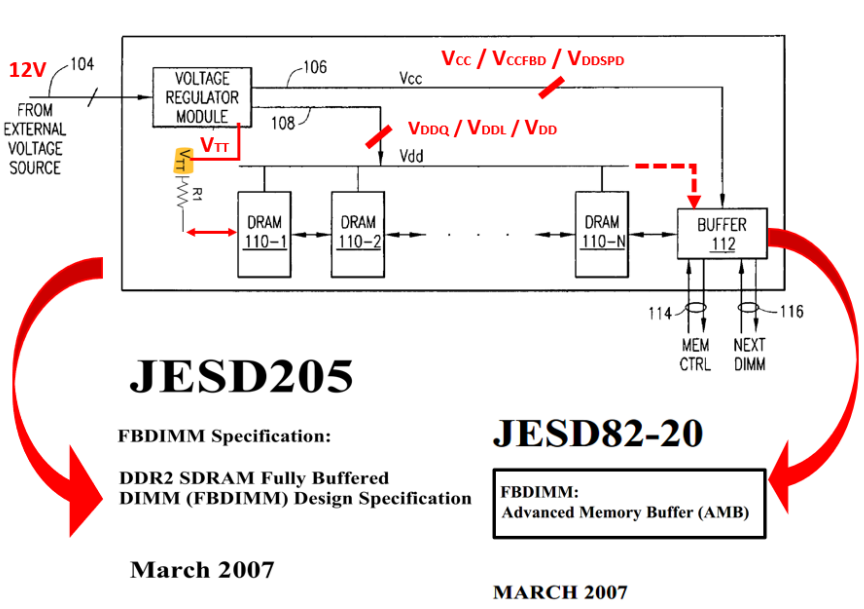
(5) [1.d.5] Wherein the SDRAM devices are coupled to the first regulated voltage

Grounds 1A-1C teach "*wherein the plurality of SDRAM devices* [from [1.d.2]] *are coupled to the first regulated voltage* [e.g., V_{DD} or V_{DDQ} = 1.8V] *of the at least three regulated voltages*," as shown above (pp.14-19, 27). EX1003, ¶¶285-287.

3. Claim 2

Grounds 1A-1C teach "*claim 1, wherein the first regulated voltage has a first voltage amplitude* [e.g., 1.8V], *and the second regulated voltage has a second voltage amplitude* [e.g., 1.5V] *wherein a first one of the first and second voltage amplitudes* [e.g., "2nd"/"*second*"=1.5V] *is less than a second one of the first and second voltage amplitudes* [e.g., "1st"/"*first*"=1.8V]," as shown below and discussed above (pp.14-19, 27). EX1003, ¶¶288-296.

Ground 1: Harris with JEDEC's FBDIMM Standards



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

4. Claim 3

Ground 1A teaches "*claim 1, wherein a third regulated voltage* [e.g., V_{DDL}] *of the at least three regulated voltages has a voltage amplitude of 1.8 volts*," as shown above (pp.14-19, 27). EX1003, ¶¶297-301.

5. Claim 15

Grounds 1A-1C teach "*claim 1, wherein two of the at least three buck converters are configured to operate as a dual-buck converter.*" EX1003, ¶¶431-448. The 054 Patent illustrates a "*dual buck converter*" as simply having ***two***

outputted voltages:

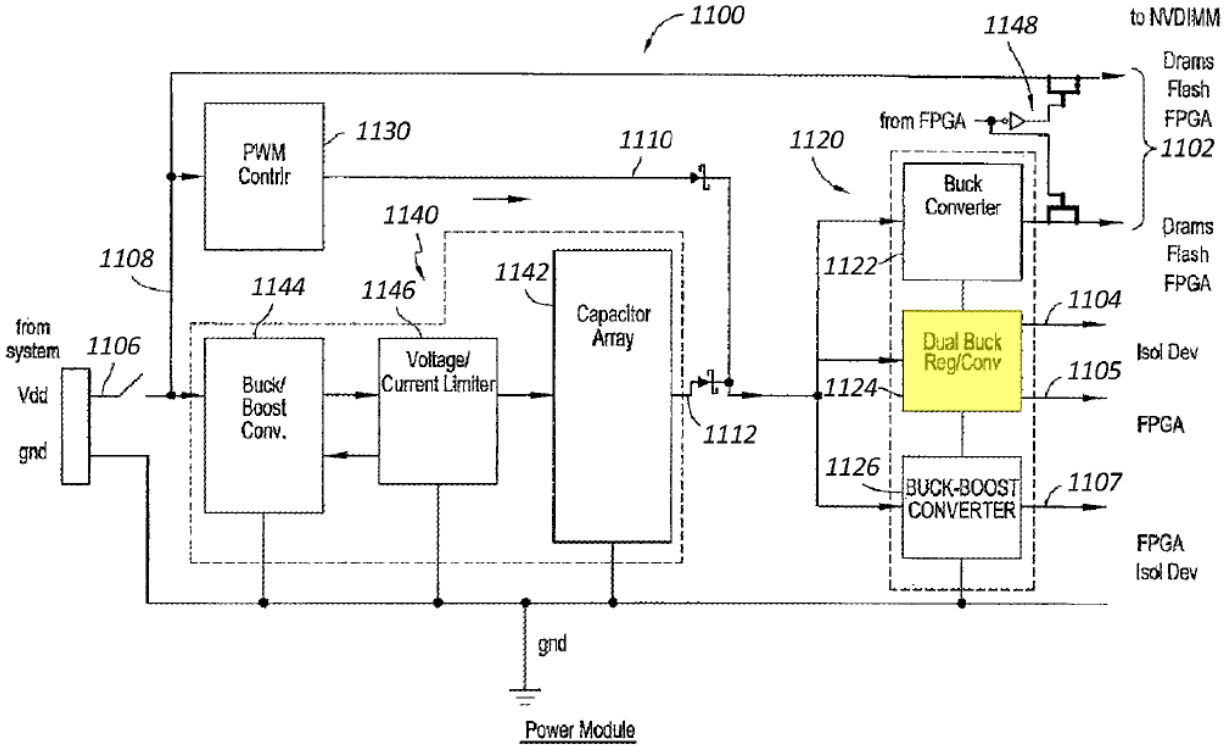
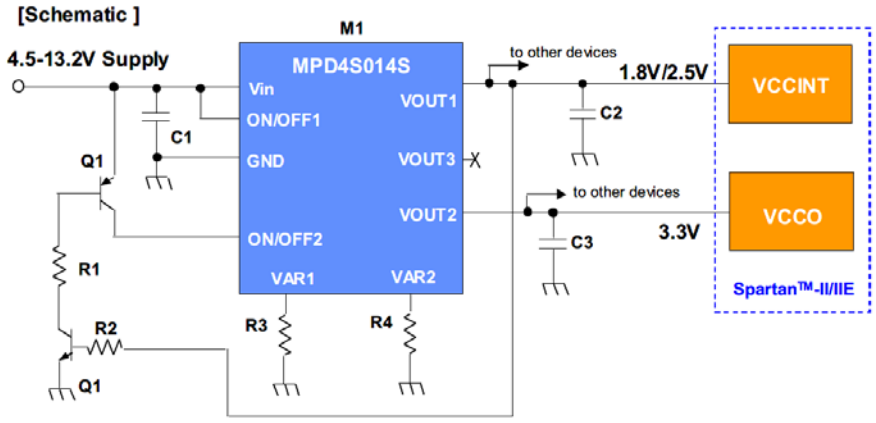


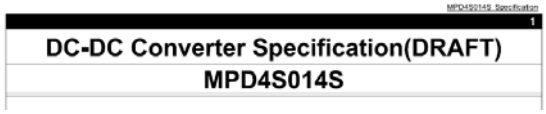
FIG. 16

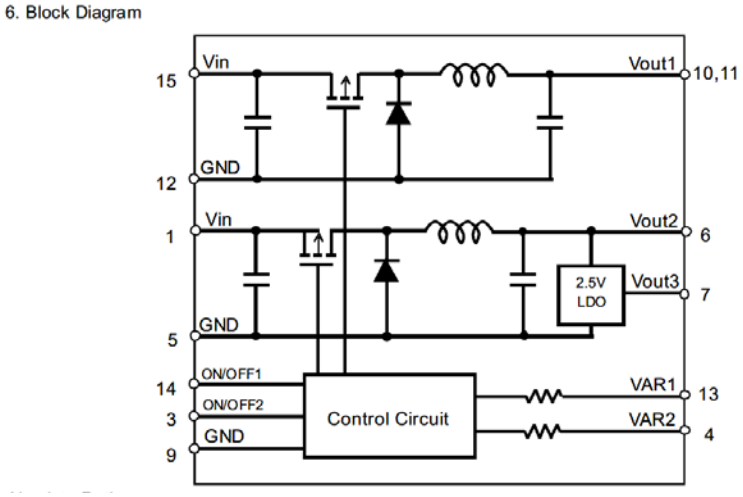
EX1001, 29:28-29, Fig.16 (1124).

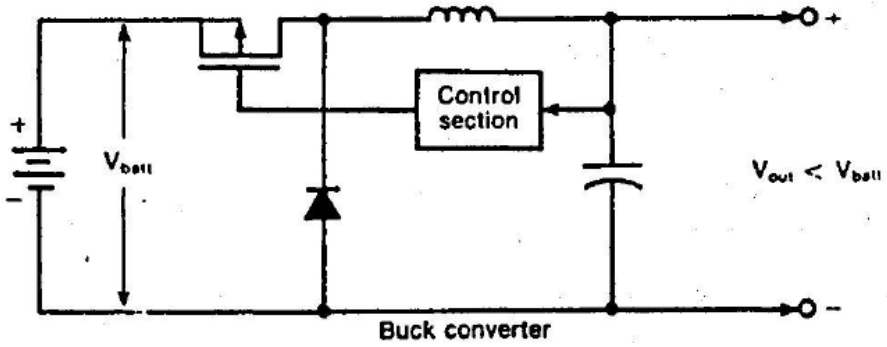
At the time, there were many commercially available products that could output two (or more) regulated voltages using buck converters, and thus in Grounds 1A-1C it would be obvious to implement any two of the regulated voltages as a "*dual buck converter*" to reduce the number of integrated circuits, pins, and interconnections on the module, therefore simplifying the design. EX1003, ¶439. *See, e.g.*, *Intel Corp. v. Qualcomm Inc.*, 21 F.4th 784, 797-99 (Fed. Cir. 2021).

For example, Murata offered a MPD4S014S dual buck converter with two different output voltages (e.g.,1.8V and 3.3V):







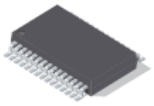


EX1042, p.16; EX1048, pp.1-2; EX1058, p.5.

As another example, Texas Instruments offered a TPS51020 "***Dual***" buck converter, e.g., for V_{DDQ} and V_{TT} voltages for DDR or DDR2 memory devices (similar to Ground 1C):

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- **Notebook Computers System Bus and I/O**
- **DDR I or DDR II Termination**

EX1040, pp.1, 11 ("TPS51020 gives a complete function set required for the DDR termination supply such as V_{DDQ}/2 tracking V_{TT}").

As another example, Fairchild offered a FAN5026 "***Dual-Output*** PWM Controller" with two different outputs (each anywhere from 0.9V to 5.5V), such as 2.5V and 1.8V, or V_{DDQ} and V_{TT} like Ground 1C:

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

■ DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

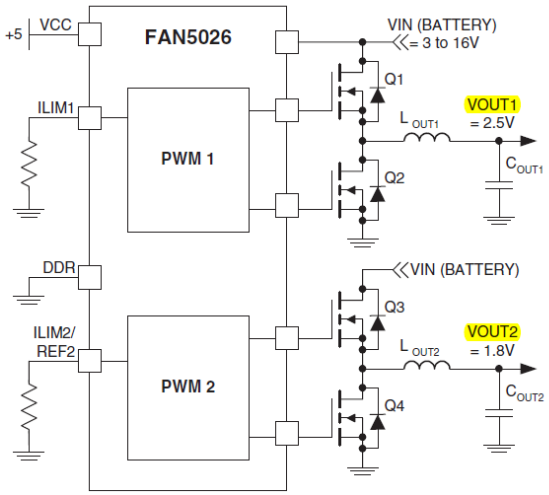


Figure 1. Dual Output Regulator

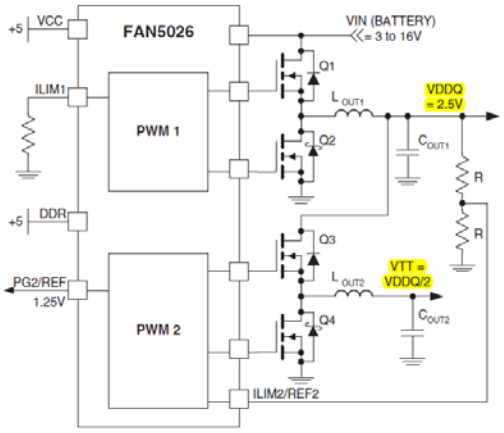


Figure 2. Typical Application

EX1041, pp.1-2, 9; *see also, id.*, pp.7-8 (similar).

In short, "*dual buck converters*" were an obvious design choice to simplify the number of parts needed to supply multiple regulated voltage. EX1003, ¶439. An additional motivation to use dual buck converters, like those above, was that the ***phases*** of the two voltages could be adjusted relative to each other, thus

reducing any input "ripple" and improving performance. EX1003, ¶¶443-444; EX1041, p.9; EX1040, p.10; *see also* EX1047, 3:49-50, 4:7-10, 4:37-56, 5:4-13, 5:46-59 & Fig.2 (illustrating dual buck converter with $V_{out1}=V_{DDQ}$ and $V_{out2}=V_{TT}$ and phase shifting).

Thus, Grounds 1A-1C teach claim 15.

In litigation, Netlist has pointed to a ***dual-phase*** buck converter (with a ***single*** voltage output) as a "*dual buck converter*." EX1073, pp.49-50, 58. This interpretation is not disclosed in the 054 Patent. EX1003, ¶446. In any event, a ***dual-phase*** buck converter would have been obvious given that Harris specifically teaches using "***multi-phase*** synchronous Pulse-Width Modulated (PWM) controllers." EX1023, ¶[0010]; *see also* EX1032, pp.161-64 (describing use of PWM controllers for buck converters). Such "multiphase buck converter" circuits were known to provide several advantages, including "lower ripple," "higher current capability," and "smaller size." EX1050, 3:36-37, 2:19-20. In light of Harris's express teaching, it would have been obvious to use a ***dual-phase*** buck converter (e.g., for V_{DD}) to reduce ripples and decrease the size of the circuit, thus satisfying Netlist's apparent interpretation for "*dual buck converter*." EX1003, ¶447.

B. Ground 2

Ground 2 renders obvious claims 1-30.

1. Ground 2 combination: Ground 1 + Amidi (EX1024)

Ground 2 combines Ground 1 (Harris with the FBDIMM Standards) with Amidi (shown in blue below) as follows:

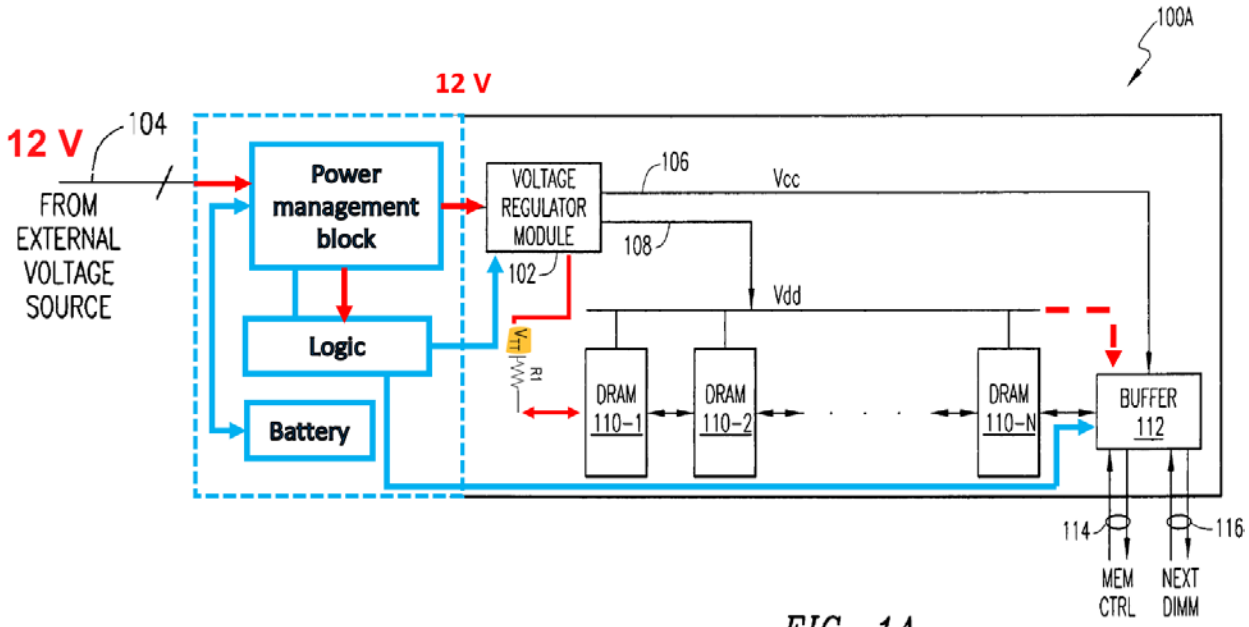


FIG. 1A

EX1003, ¶¶171-180. As explained below, Amidi teaches battery backup to provide power to Harris's memory module during a power disruption. The "Logic" of Amidi (blue above) can detect power disruptions, switch to battery power, and preserve data in the DRAMs by sending "self-refresh" commands.

A POSITA would have been motivated to combine Ground 1 with Amidi, and had a reasonable expectation of success in doing so, because Harris recognizes concerns with power reliability and proposes a "redundant" power source, EX1023, ¶¶[0012-14, 16], Figs.1B, 2, while Amidi teaches a redundant power source (e.g., a battery on the memory module) for maintaining data during a power

disruption, EX1024, Abstract, 1:28-35, 2:6-26, 4:14-60, Figs.5-6; EX1003, ¶¶171-177. The "power management block" of Amidi (above left, in blue) could be modified easily to work with the FBDIMM memory module of Harris, as shown in the annotated version of Figure 5 of Amidi below:

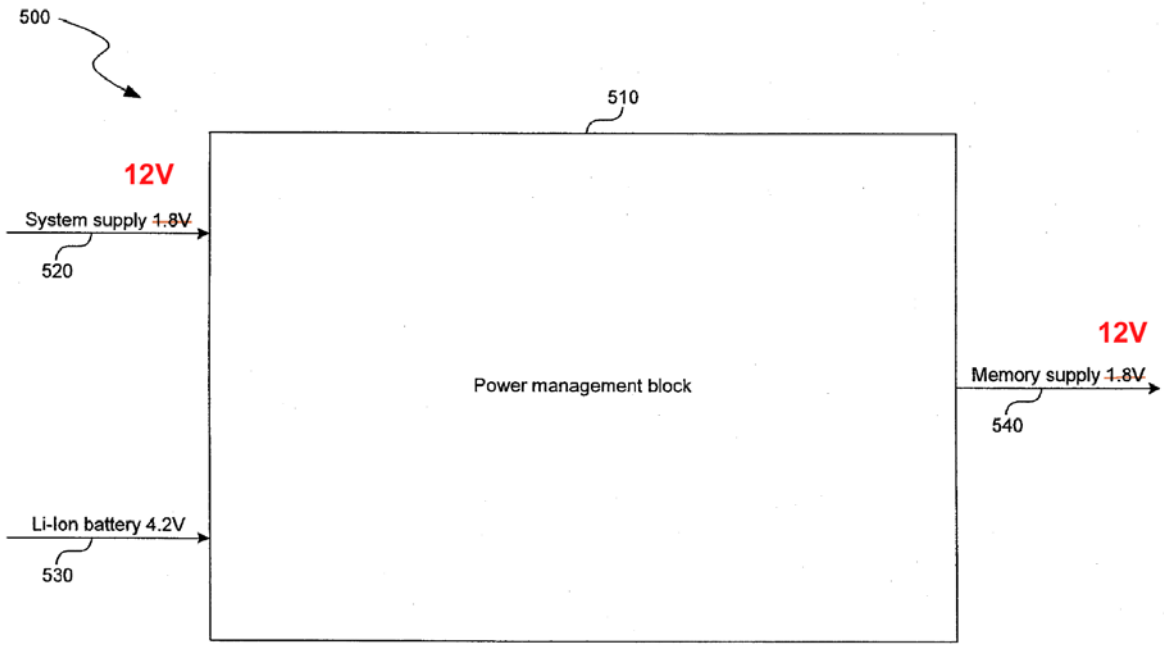


FIG. 5

EX1024, Fig.5 (annotated with teachings of Harris); EX1003, ¶¶173-174. Harris teaches using a 12V external supply, EX1023, ¶[0012], so in the Ground 2 combination, it would have been obvious to a POSITA that the 12-volt external supply (above left) is stepped-down with a buck converter to a 5-volt supply for Amidi's lithium-ion battery charger (EX1024, Fig.6 (620), not shown above), and Amidi's battery voltage (e.g., 4.2 volts, above left) is stepped-up with a boost converter to the 12-volt level used by Harris's memory module (above right).

EX1003, ¶¶173-174. Indeed, Amidi expressly discloses that his "power management block" (Fig.5 above) uses "buck" converters to step-down voltages as needed, *see, e.g.*, EX1024, 4:38-40 & Fig.6 (640 "buck"), and "boost" converters to step-up voltages as needed, *id.*, 4:27-32 & Fig.6 (610 "boost"), as had long been taught in textbooks, *see, e.g.*, EX1058, p.3 ("buck," "boost"); EX1032, p.161 (same).

Furthermore, Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module, where both modes put the DRAMs in a self-refresh state to preserve data while conserving power, providing another motivation to combine Ground 1 with Amidi. In particular, Amidi discloses that "one may provide a process which operates to … maintain memory (through refresh, for example)." EX1024, 2:16-19, Fig.11. Similarly, in "S3 sleep mode" on an FBDIMM like Harris, "the DIMMs are put into a very lower power state, with the DRAMs in self refresh mode." EX1027, p.39; EX1003, ¶¶175, 330. In particular, "in S3 power mode, all command/address outputs, including CKE, ODT, CLK, and all other command/address pins, will be driven low [i.e., they are not used]…. 1.8V supply is on [i.e., for V_{DD} to the DRAMs, *see* pp.14-19, 27]. 1.5V [i.e., for V_{CC}/V_{CCFBD} to the I/O of the Buffer, *see* pp.14-19, 27], Vtt, and 3.3V are off. DRAMs are in self refresh [i.e., still powered on with V_{DD}=1.8V], and the CKE signals must be driven low." EX1027, p.21. Thus, a POSITA would have

been motivated to use the teachings of S3 mode in Ground 1 when implementing Amidi's backup power supply and logic functionality. EX1003, ¶175. Indeed, the S3 mode was described in the FBDIMM Standards for the very purpose of saving power in all types of computers, including servers and workstations. EX1027, p.39 ("very lower power state"); EX1028, p.9 ("FB-DIMMs are intended for use as main memory when installed in systems such as servers and workstations.").

Thus, a POSITA would have been motivated to implement Harris's FBDIMM memory module with the functionality of Amidi's power management and logic blocks for detecting power disruptions and switching over to battery backup when needed. EX1003, ¶¶171-176. This straightforward modification of Harris's memory module in view of Amidi and the knowledge of a POSITA simply uses a known technique (e.g., Amidi's battery backup techniques) to improve a similar device (e.g., Harris's memory module) in the same way (e.g., to provide a backup power supply using a battery). *Id.*, ¶177. In addition, the modification merely applies a known technique (e.g., providing a backup power supply) to a known device (e.g., a memory module) that is ready for improvement to yield predictable results (e.g., redundancy when the system supply or clock fails). *Id.*

As summarized in the annotated figure below for Ground 2, Amidi's "power management block" (blue, below left) supplies the voltages for Amidi's logic and

for Harris's Voltage Regulator Module, which in turn supplies the voltages for various components on an FBDIMM memory module as specified by the FBDIMM Standards, including those listed below on the right. EX1003, ¶¶176-180.

Ground 2: Ground 1 and Battery Backup of Amidi

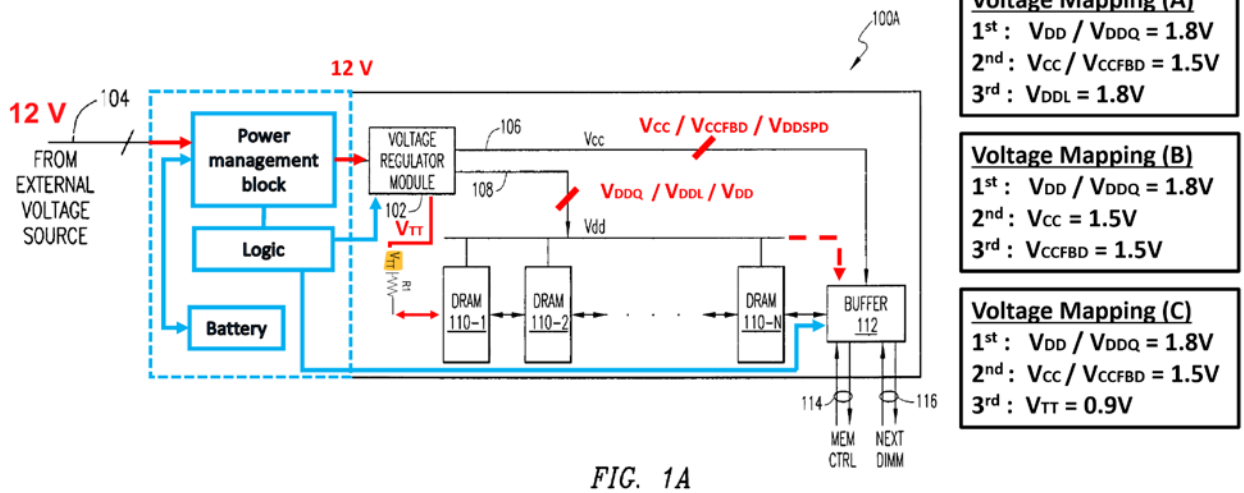


FIG. 1A

Voltage Mappings "A" to "C" (on the right, referred to as Grounds 2A-2C) are simply different ways to apply the arbitrary labels "1st" through "3rd" to the voltages shown in red in the annotated figure. EX1003, ¶¶175-180. Grounds 2A-2C involve the same voltage mappings as Grounds 1A-1C. *Supra* pp.14-19, 27.

2. Claims 1-3, 15

For claims 1-3 and 15, Grounds 2A-2C have the same voltage mappings as Grounds 1A-1C, and the addition of Amidi in Grounds 2A-2C does not negate any of the arguments in Grounds 1A-1C for those claims, and thus Grounds 2A-2C

invalidate those claims for at least the same reasons provided above for Grounds 1A-1C. EX1003, ¶¶216-301, 431-448.

3. Claim 4

a) [4.a] Preamble and [4.b] Voltage Monitor Circuit

Grounds 2A-2C teach "*claim 1, further comprising: a voltage monitor circuit* [e.g., including Amidi's power supervisory module/block 480/665/800 implemented in the blue "Power management" and "Logic" boxes in the combination of Ground 2, below] *coupled to the PCB and to a second set of edge connections of the plurality of edge connections* [e.g., Harris's edge connections for power, see [1.b] (pp.20-25)], *the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connection* [e.g., monitor the external system power supply 605/825 in Amidi, which is 12V in the combination of Ground 2], *the voltage monitor circuit configured to produce a trigger signal* [e.g., Amidi's signal 670/858/868] *in response to the input voltage having a voltage amplitude below a predetermined threshold voltage* [e.g., Amidi's reference voltage 675/820, which as shown below may be 5% or 10% below the nominal voltage, which is 12V in the combination of Ground 2, see pp.41-45, EX1023, ¶¶[0012-13]]." EX1003, ¶¶303-314.

Ground 2: Ground 1 and Battery Backup of Amidi

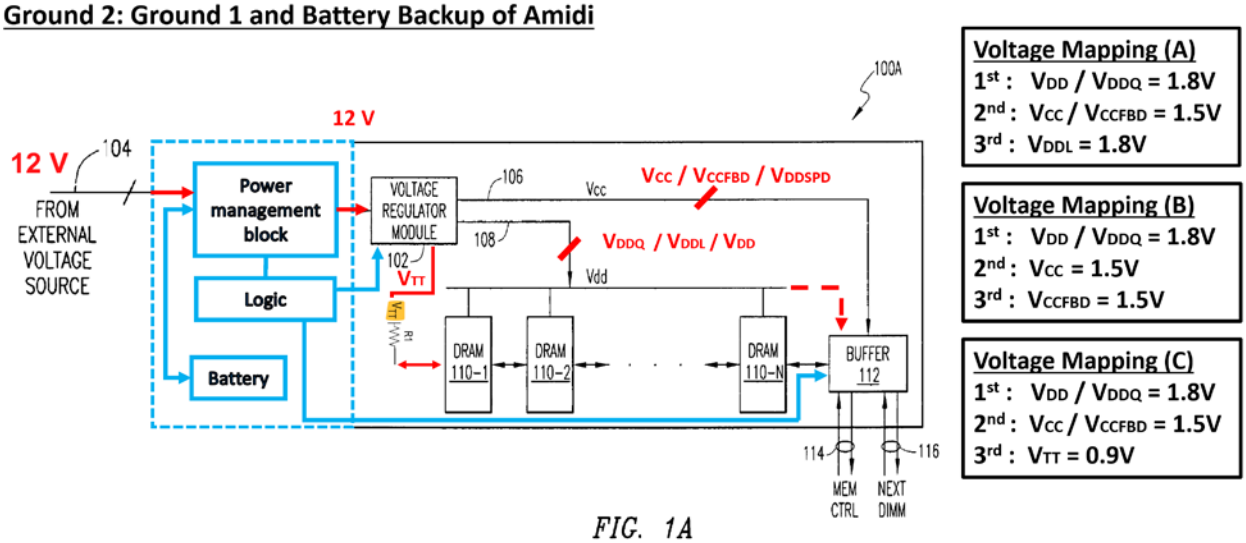


FIG. 1A

Amidi's "power supervisory" module 480 (red, below) is included in the "*voltage monitor circuit*" (blue above) and "*coupled to the PCB*" having an edge connector (orange, below). EX1024, 4:8-11, Fig. 4 (below).

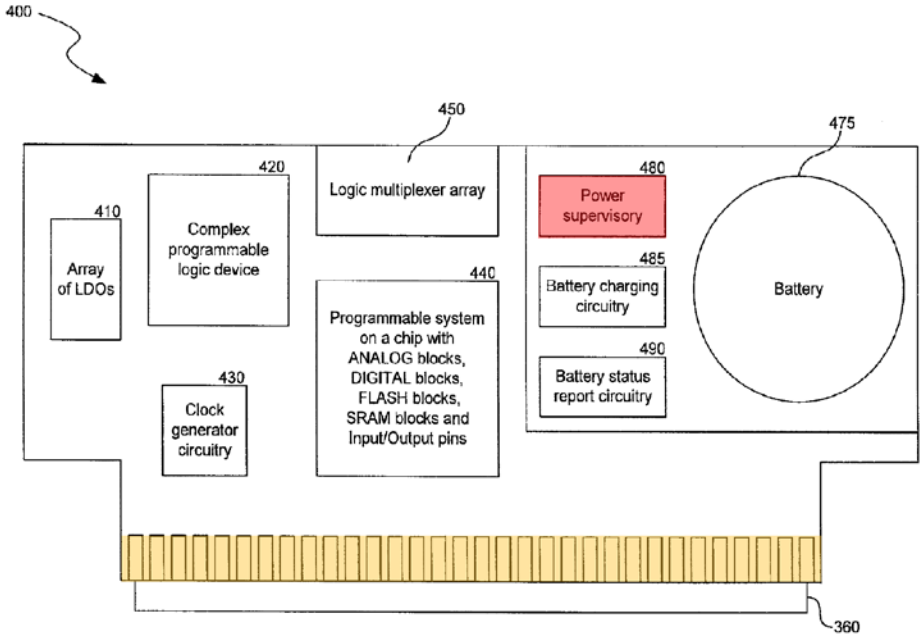
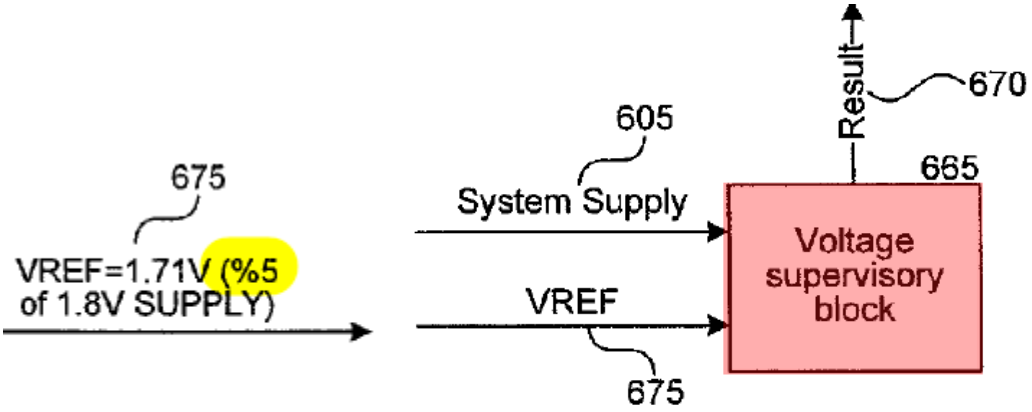


FIG. 4

Amidi's voltage supervisory functionality (e.g., 665 in red, below) (part of the "*voltage monitor circuit*") monitors the "System Supply" 605 ("*input voltage*," which is 12V in Ground 2) to determine if there is a power disruption and generates a signal 670 ("*trigger signal*") if the system supply has a voltage amplitude below a specified reference voltage (e.g., VREF 675). EX1024, 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs. 5, 6 (excerpted below), 14 (below), 15.



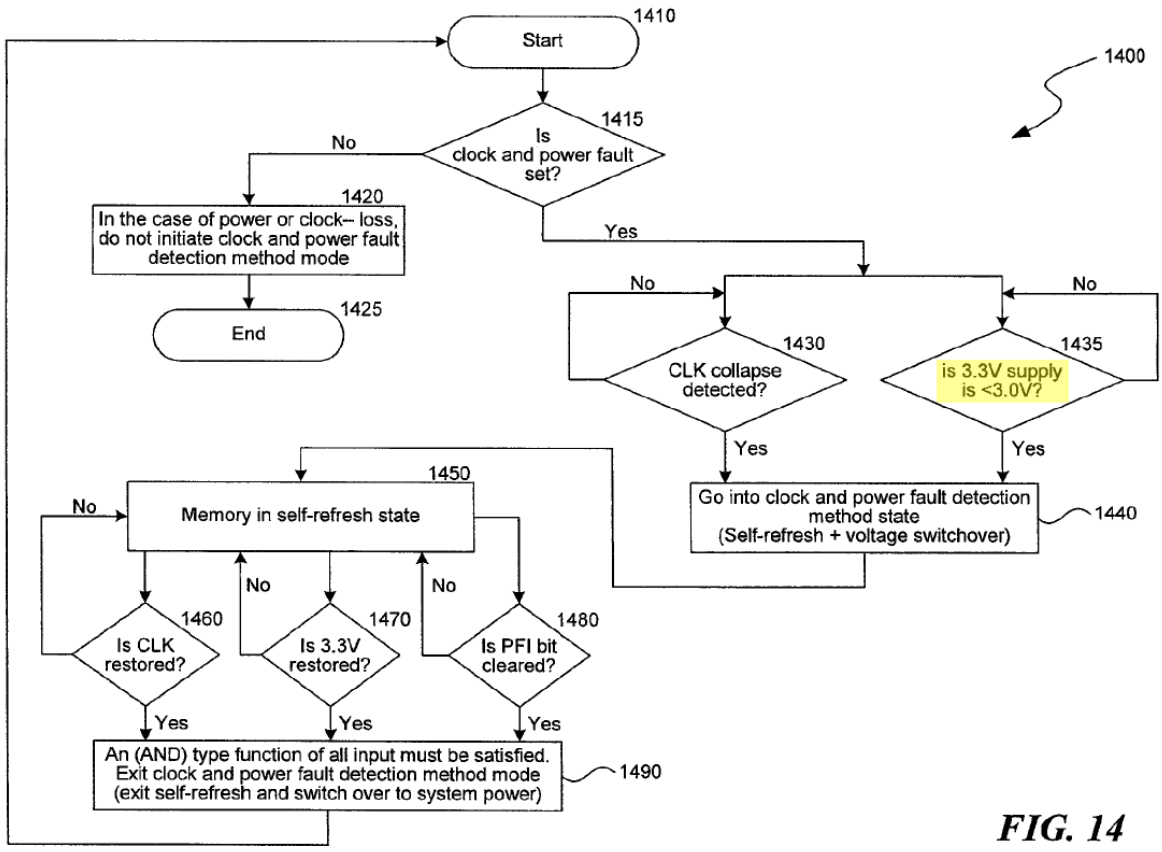


FIG. 14

See also EX1024, 5:31-62, 8:30-62, Figs. 7-8, 14 (describing Amidi's voltage supervisory block 800 and detecting a host request); EX1003, ¶¶311-312.

b) [4.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

Grounds 2A-2C teach that "*the memory module transitions from a first operable state* [e.g., normal operations using an external voltage when its amplitude is within a normal range] *to a second operable state* [e.g., self-refresh operations using battery backup when the external voltage amplitude is outside the normal range] *in response to the trigger signal* [e.g., Amidi's trigger signal 670/858/868 discussed immediately above]." EX1003, ¶¶315-321. Amidi

discloses that upon detecting a power fault (1520 and 1530, below), the memory module switches to battery backup (1540, below) and initiates memory self-refresh operations to preserve the data in the SDRAMs (1550, below). EX1024, 4:44-52, 9:8-22, Figs. 6-8, 15 (below); EX1003, ¶¶317-319.

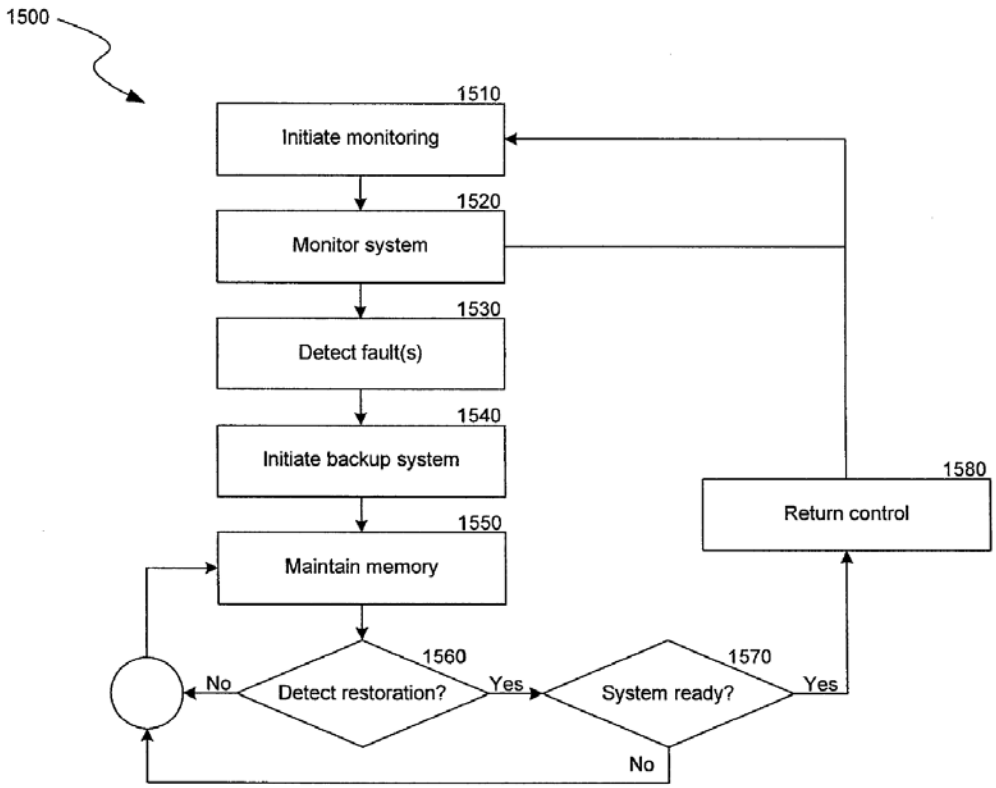


FIG. 15

See also EX1024, 8:30-62, Fig. 14; EX1003, ¶320.

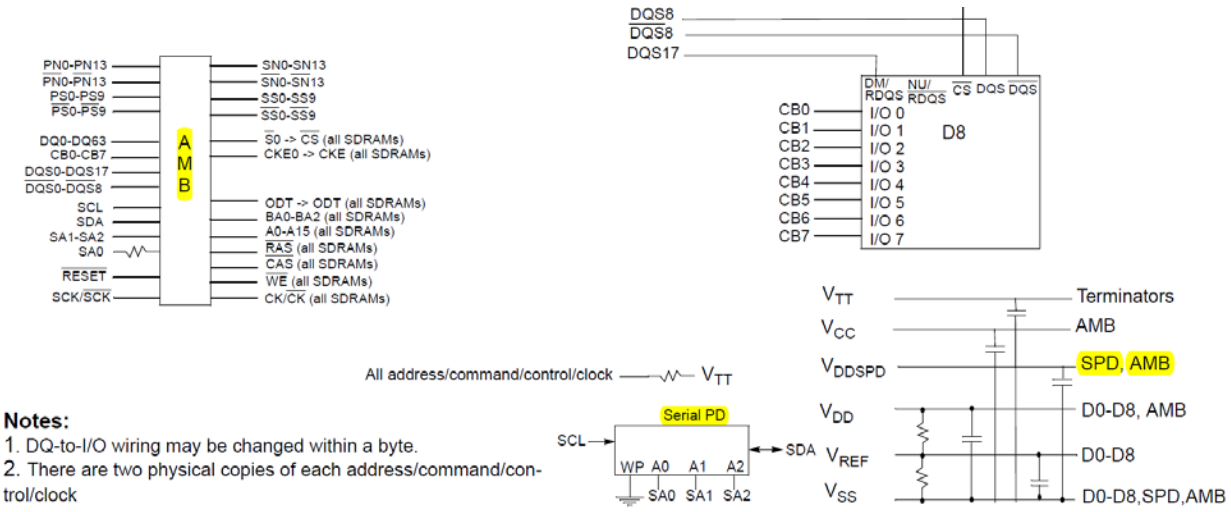
4. Claim 5

Grounds 2A-2C teach, at least under Netlist's apparent interpretation, EX1073, p.62, "*claim 4, further comprising: a controller* [e.g., logic for controlling S3 sleep mode, discussed above (pp.43-44)] *coupled to the voltage*

monitor circuit [e.g., Amidi's voltage supervisory block, from [4.b]]; *wherein, in response to the trigger signal* [from [4.b], indicating a power disruption], *the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory* [e.g., S3 configuration information is stored in non-volatile memory before entering S3 sleep mode]." EX1003, ¶¶322-340.

As discussed above (pp.43-44), Amidi's battery backup mode is similar to the S3 power-saving mode of Harris's FBDIMM memory module, because both modes put the SDRAMs in a self-refresh state to preserve data while conserving power. Thus, in the event of a power disruption causing Amidi's "*voltage monitor circuit*" to produce a "*trigger signal*" (see [4.b]), a POSITA would have been motivated to use the S3 sleep mode discussed above (pp.43-44) to conserve power when using Amidi's battery backup. EX1003, ¶¶322-333.

Before entering into S3 sleep mode, the controller will perform "*a write operation to transfer data* [e.g., S3 configuration information] *to non-volatile memory*." *See* EX1027, pp.25 ("The following CSRs [Control and Status Registers] should be stored in non-volatile memory before entering S3 mode and restored before normal DRAM transactions begin…."), 95-96, 141 ("S3RESTORE" registers). EX1003, ¶337. The "*non-volatile memory*" can be implemented in the SPD device on the module:



Notes:
1. DQ-to-I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/control/clock

EX1028, p.13; *see also* EX1027, p.117 ("SPD EEPROM" for storing settings); EX1066, 26:64-27:4 (storing configuration information in SPD). In the alternative, given that V_{DDSPD} is also supplied to the AMB Buffer (as shown above right), it also would be obvious to a POSITA that the claimed "*non-volatile memory*" could be contained in the Buffer, thus decreasing the number of components, interfaces, and interconnections on the memory module, resulting in a cheaper, faster, and more secure solution. EX1003, ¶338; EX1066, 26:64-27:4 (storing configuration information "on the buffer or controller device"); EX1067, pp.1-2 (FGPA logic integrating non-volatile memory); EX1023, ¶[0019] (benefits of pin-count reduction).

5. Claim 6

a) [6.a] Preamble and [6.b] Voltage Monitor Circuit

Claim 6 is similar to claim 4, except it concerns overvoltage detection rather than undervoltage detection (as in [4.b]). Thus, for the reasons provided above for

claim 1 (pp.19-34) and [4.b] (pp.46-49), and in light of Harris's teaching to detect both undervoltage and overvoltage conditions, *see* EX1023, ¶[0013] ("+/−15%"), Grounds 2A-2C teach "*claim 1, further comprising: a voltage monitor circuit* [e.g., including Amidi's power supervisory module/block 480/665/800 implemented in the blue "Power management" and "Logic" boxes in the combination of Ground 2, *see* [4.b] (pp.46-49)] *coupled to the PCB and to a second set of edge connections of the plurality of edge connections* [e.g., Harris's edge connections for power, see [1.b] (pp.20-25)], *the voltage monitor circuit configured to monitor an input voltage received from the second set of edge connections* [e.g., monitor the external system power supply 605/825 in Amidi, which is 12V in the combination of Ground 2], *the voltage monitor circuit configured to produce a trigger signal* [e.g., Amidi's signal 670/858/868, *see* [4.b] (pp.46-49)] *in response to the input voltage having a voltage amplitude above a predetermined threshold voltage* [e.g., 15% above a nominal value, such as 13.8V is 15% above 12V, as Harris teaches, EX1023, ¶[0013] ("+/−15%")]." EX1003, ¶¶341-355.

Harris teaches ***both*** overvoltage ***and*** undervoltage detection of "+/- 15%." EX1023, ¶[0013]. Thus, in the combination of Ground 2, a POSITA would have been motivated by Harris to include overvoltage detection in Amidi's "*voltage monitor circuit*," with a reasonable expectation of success. EX1003, ¶¶347-348.

Indeed, such circuitry for ***both*** overvoltage ***and*** undervoltage detection was well known and commercially available:

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PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar); EX1003, ¶¶349-352.

b) [6.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

As explained above for [4.c] (pp.49-50), Grounds 2A-2C further teach "*wherein the memory module transitions from a first operable state* [e.g., normal operations using an external voltage when its amplitude is within a normal range] *to a second operable state* [e.g., self-refresh operations using battery backup when

the external voltage amplitude is outside the normal range] *in response to the trigger signal* [from [6.b] directly above]." EX1003, ¶¶356-359.

6. Claim 8

a) [8.a] Preamble and [8.b] A Controller, Including a Voltage Monitor Circuit, Coupled to the PCB

Claim 8 is similar to claims 4 to 6 above (pp.46-55). Thus, Grounds 2A-2C teach "*claim 1, further comprising a controller* [see [5.b], e.g., for controlling S3 sleep mode, discussed above (pp.43-44)] *coupled to the PCB, the controller including a voltage monitor circuit* [see [4.b], e.g., Amidi's power supervisory module/block 480/665/800, below (red), implemented in the blue "Power management" and "Logic" boxes in the combination of Ground 2, second below] *configured to monitor an input voltage* [e.g., monitor the external system power supply 605/825 in Amidi, which is 12V in the combination of Ground 2] *received from a second set of edge connections of the plurality of edge connections* [e.g., Harris's edge connections for power, see [1.b] (pp.20-25)]." EX1003, ¶¶373-379.

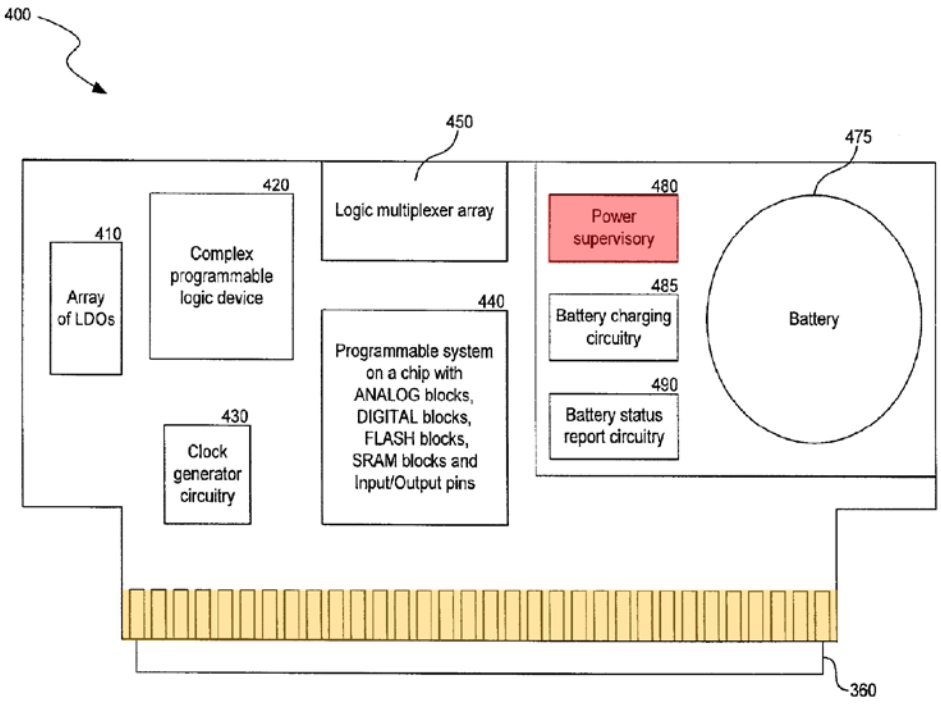


FIG. 4

Ground 2: Ground 1 and Battery Backup of Amidi

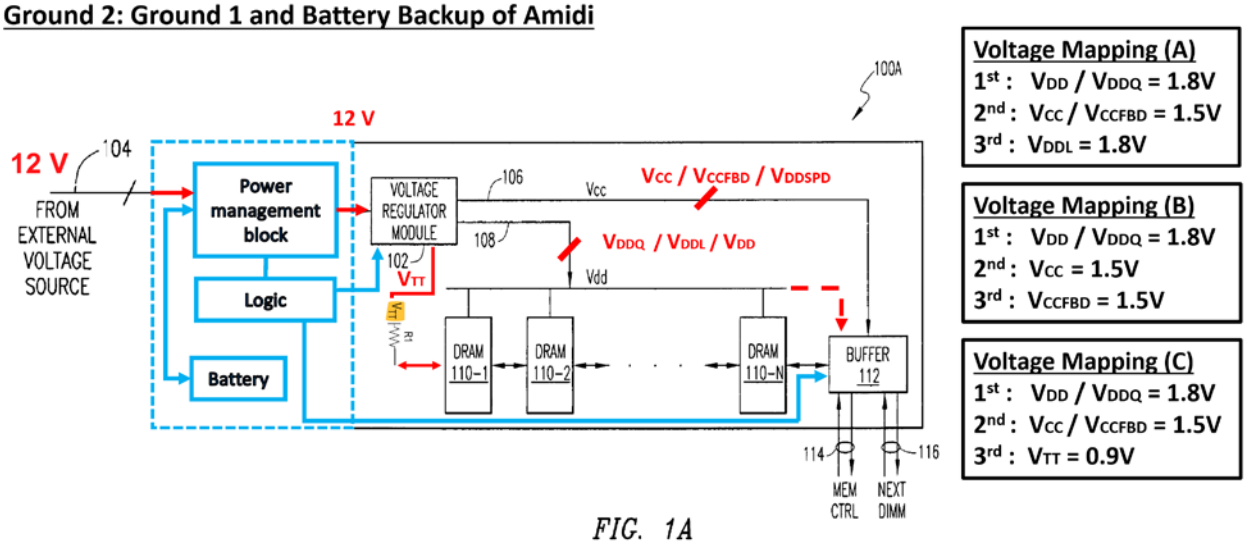


FIG. 1A

b) [8.c] Wherein the Voltage Monitor Circuit Transmits a Signal to Portion(s) of the Controller

Grounds 2A-2C further teach "*wherein, in response to the voltage monitor circuit detecting a power threshold condition* [e.g., the "*input voltage*" is either too

low, see [4.b] (pp.46-49), or too high, see [6.b] (pp.52-54)], *the voltage monitor circuit transmits a signal* [e.g., Amidi's signal 670/858/868, indicating a power disruption, see [4.b] (pp.46-49)] *to one or more portions of the controller* [e.g., to switch to battery backup and initiate S3 sleep mode to preserve data in the SDRAMs while conserving power, see [4.c] (pp.49-50) and [5.c] (pp.50-52)]." EX1003, ¶¶380-385.

7. Claims 7, 9, 11, 13, 16-17

Grounds 2A-2C teach claims 7, 9, 11, 13, and 16-17 for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[7.a]	[6.a]	¶¶361-363 (¶¶342-344)
[7.b]	[5.b]	¶¶364-367 (¶¶326-333)
[7.c]	[5.c]	¶¶368-371 (¶¶334-340)
[9.a]	[6.b]	¶¶387-390 (¶¶345-355)
[9.b]	[6.b][2]	¶¶391-394 (¶¶345-355)
[11.a]	[4.b], [8.c]	¶¶404-406 (¶¶306-314, 380-385)

[2] The "*specified operating voltage*" is Harris's 12V nominal external voltage as shown above (pp.41-45). EX1023, ¶¶[0012-13].

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[11.b]	[4.b][3]	¶¶407-410 (¶¶306-314)
[11.c]	[4.c]	¶¶411-414 (¶¶315-321)
[13]	[4.b]	¶¶419-423 (¶¶306-314)
[16.a]	[1.a]	¶¶450-452 (¶¶217-223)
[16.b]	[1.b]	¶¶453-455 (¶¶224-232)
[16.c]	[1.c]	¶¶456-458 (¶¶233-260)
[16.d.1]	[1.d.1]	¶¶459-461 (¶¶261-266)
[16.d.2]	[1.d.2]	¶¶462-464 (¶¶267-271)
[16.d.3]	[1.d.5]	¶¶465-467 (¶¶285-287)
[16.e.1]	[8.b], [1.b], [9.a][4]	¶¶468-471 (¶¶376-379, 224-232, 387-390)
[16.e.2]	[4.c]	¶¶472-474 (¶¶315-321)
[17]	[4.b], [6.b]	¶¶475-478 (¶¶306-314, 345-355)

[3] See note 2 directly above.

[4] Amidi's voltage supervisory block (e.g., 665) (part of the "*voltage monitor circuit*") is "*configured to detect an amplitude change in the input voltage*," for example, when the external system supply changes by crossing the reference voltage. EX1003, ¶471.

8. Claim 10

Grounds 2A-2C teach "*claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage* [e.g., 12V, see pp.41-45; EX1023, ¶¶[0012-13]]." EX1003, ¶¶395-402.

The claimed threshold of "*ten percent*" is within the range of thresholds disclosed in the prior art, and thus "*ten percent*" is obvious under Federal Circuit precedent discussed above (p.27). In particular, Harris teaches a threshold of "+/-15%," EX1023, ¶[0013], so under Federal Circuit precedent, any threshold in the range of 15% under to 15% over would have been obvious.

A POSITA would have understood that a tolerance around 10% provided a reasonable compromise between the risk of losing data, or damaging devices, from too high a tolerance, and of unnecessary interruptions from too low a tolerance. EX1003, ¶400. Indeed, thresholds around 10% for undervoltage and/or overvoltage were known, as shown by Amidi, the FBDIMM Standards, and commercially available products:

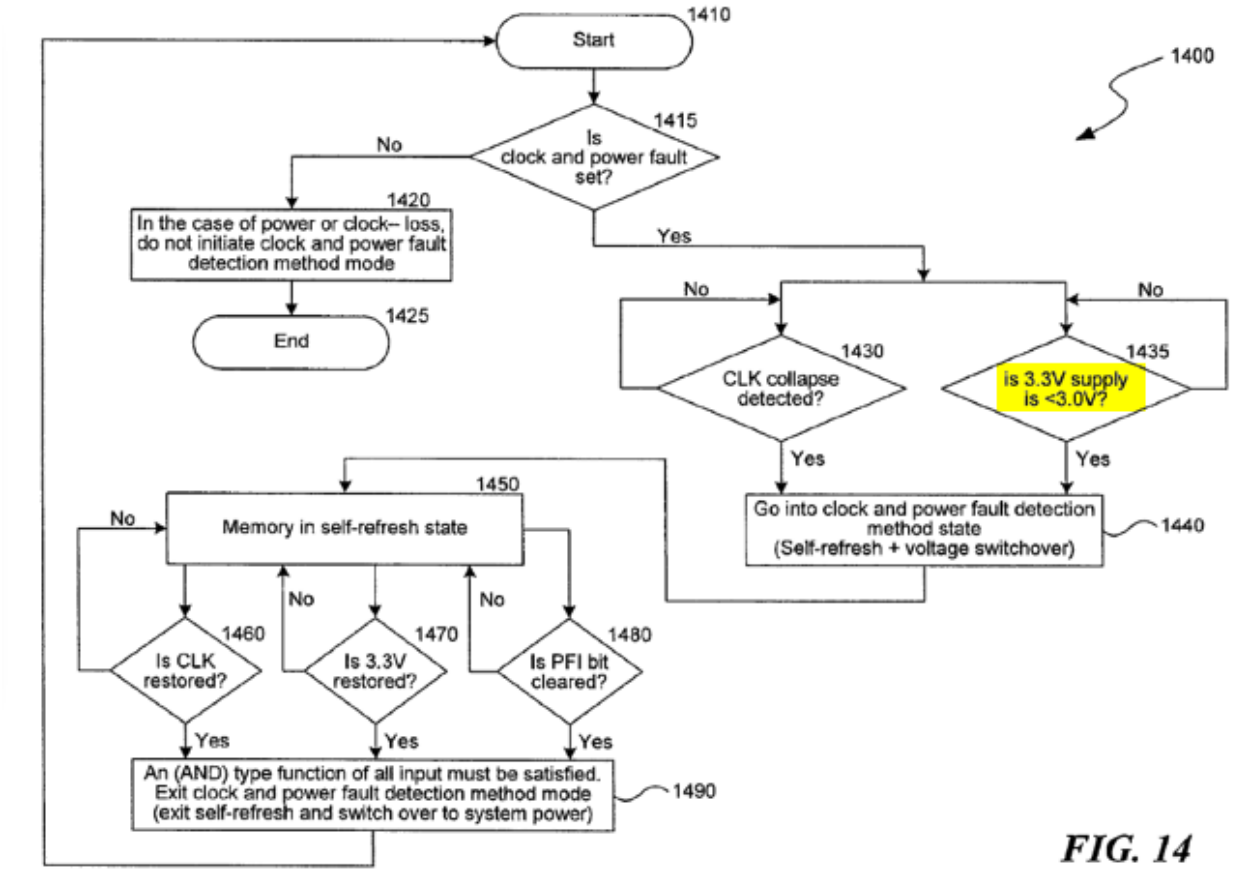


FIG. 14

EX1024, 8:23-36, Fig.14.

Table 4.2 — Advanced Memory Buffer Normal Mode DC Electrical Parameters

Parameter		Units	Min	Typ	Max
V_{CC} link / core	0kHz - 30kHz	Volts	1.455	1.5	1.575
V_{DD}		Volts	1.7	1.8	1.9
V_{DDSPD}		Volts	3.0	3.3	3.6

EX1027, p.32.

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DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (programmable under- and over-voltage protection over a range, including 10%).

9. Claim 12

For the same reasons discussed directly above for claim 10, Grounds 2A-2C teach "*claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*." EX1003, ¶¶415-418.

10. Claim 14

Grounds 2A-2C teach "*claim 8, wherein the voltage monitor circuit detecting a power threshold condition* [from [8.c] (pp.55-57), e.g., a power disruption detected by Amidi's voltage supervisory block, causing the system to switch to battery backup] *includes the voltage monitor circuit detecting a request by the host system* [e.g., Amidi's voltage supervisory block 800 detects a request

by the host system to return control to the host, below]." EX1003, ¶¶424-430. Amidi discloses that, if the power is restored after a failure, the voltage supervisory block detects whether the host has cleared the backup-mode bit ("*detecting a request by the host system*"), and subsequently, if so, returns the control of the module to the host, including handling of the power signal. EX1003, ¶¶311, 429; EX1024, 5:31-62, 9:11-39, Figs. 8, 15 (steps 1530, 1540, 1570, 1580, below); *see also id.*, 8:30-62, Fig.14 (1460-1490); EX1003, ¶312.

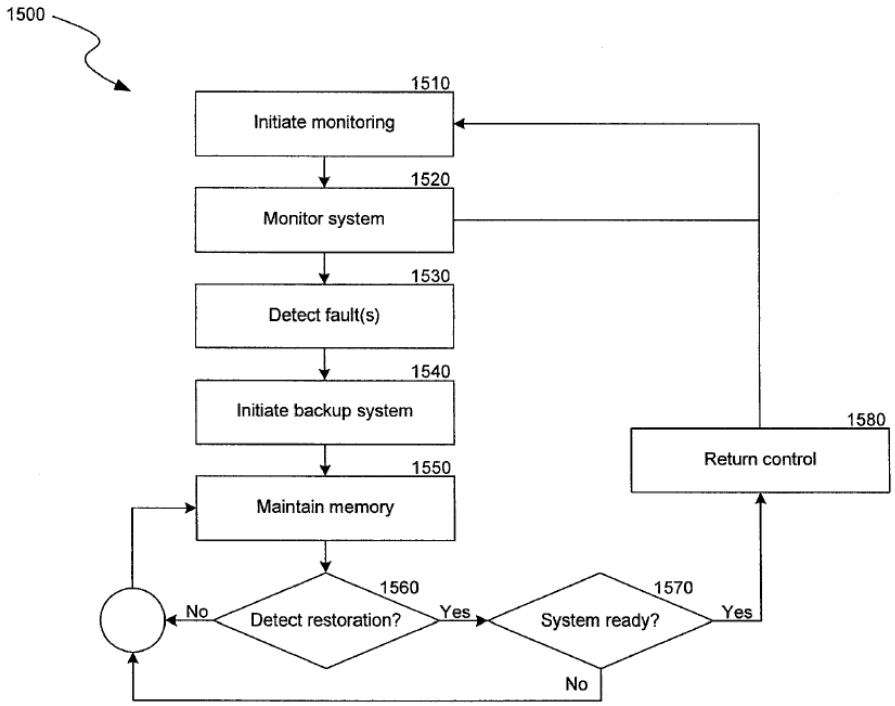


FIG. 15

11. Claim 18

a) [18.a] Using First Pre-Regulated Voltage

Grounds 2A-2C teach "*claim 16, wherein, in the first operable state* [e.g., normal operations using an external voltage when its amplitude is within a normal range, see [4.c] (pp.49-50)]*, the voltage conversion circuit provides the first regulated voltage* [V_{DD}/V_{DDQ}=1.8V (see pp.45, 14-19, 27)] *to the plurality of SDRAM devices* [see [1.d.2] (pp.31-32)] *using a first pre-regulated voltage* [below]." EX1003, ¶¶480-487.

To the extent a "*pre-regulated voltage*" can be satisfied by the "*input voltage*" of [16.e.2] being within pre-determined limits, as suggested by Netlist, EX1073, pp.49-50, Harris teaches that by disclosing a 12V external supply voltage within "+/- 15%" and by stating that it can be "regulated." EX1023, ¶¶[0013-14]; EX1003, ¶484.

To the extent the "*pre-regulated voltage*" must be a voltage pre-regulated on the memory board itself, EX1001, 28:53-58, Amidi (in the combination for Ground 2) teaches a boost converter in the "power management block" that converts (and thus pre-regulates) the battery voltage to an output of 12 volts, as shown in the annotated figures below and as discussed above (pp.41-43). EX1003, ¶¶485-486; EX1032, p.161 (explaining that switch-mode converters, including buck converters and boost converters, "convert the ***unregulated*** dc input into a ***controlled*** dc output

at a desired voltage level"). Furthermore, it would have been obvious to include a power regulator in the "power management block" that ensures a pre-regulated output voltage of 12V given Harris's teaching that the external "system supply" may be "unregulated," EX1023, ¶[0014], and to allow compatibility with input voltages other than 12V, EX1023, ¶[0020]; EX1032, p.161; EX1003, ¶486.

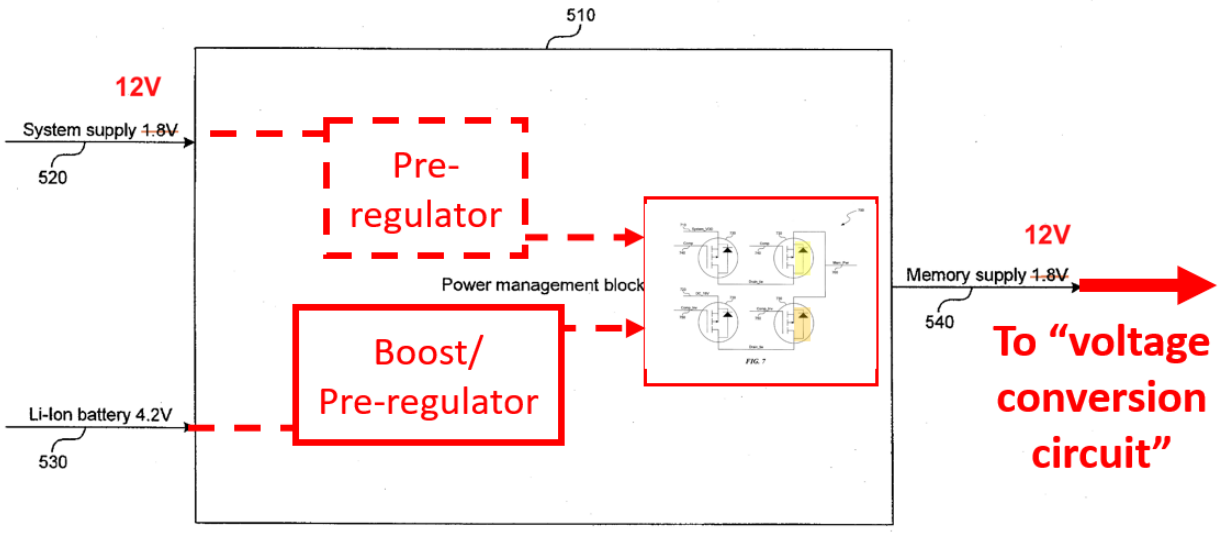


FIG. 5

Ground 2: Ground 1 and Battery Backup of Amidi

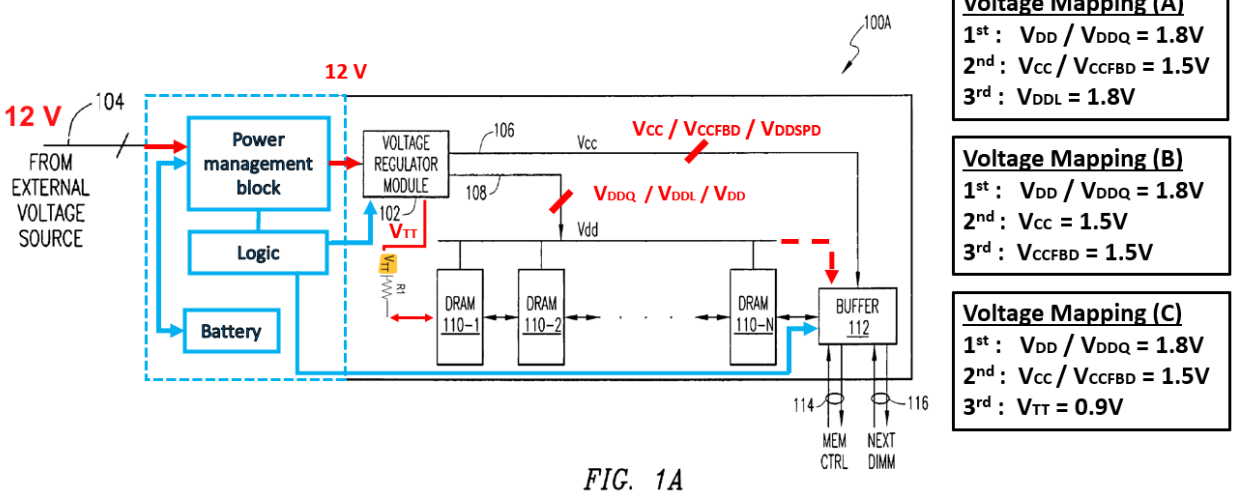


FIG. 1A

b) [18.b] Using Second Pre-Regulated Voltage

Grounds 2A-2C teach "*wherein, in the second operable state* [e.g., self-refresh operations using battery backup when the external voltage amplitude is outside the normal range, see [4.c] (pp.49-50)], *the voltage conversion circuit provides the first regulated voltage* [from [18.a]] *to the plurality of SDRAM devices* [from [18.a]] *using a second pre-regulated voltage* [e.g., from a boost converter in the "power management block" (blue, above) that converts (and thus pre-regulates) the 4.2V battery voltage to a regulated output voltage of 12V, as shown in the annotated figures above and as discussed immediately above and at pp.41-43]." EX1003, ¶¶488-492.

12. Claim 19

Grounds 2A-2C teach "*claim 18, wherein, in the first operable state* [from [18.a], e.g., when using an external voltage source], *the first pre-regulated voltage*

[from [18.a]] *is supplied to the voltage conversion circuit* [e.g., the Voltage Regulator Module, shown further below, see [1.c] (p.26)] *via a circuit* [e.g., the power switch multiplexer "*circuit*" shown in Amidi's Figure 7, below, inside the "Power management block" (blue, further below), where "System_VDD" (710) from the upper left—which in the combination of Ground 2 is pre-regulated as discussed for [18.a]—is supplied to the "*voltage conversion circuit*" to the right], *and wherein, in the second operable state* [from [18.b], e.g., when using battery backup], *the second pre-regulated voltage* [from [18.b]] *is supplied to the voltage conversion circuit via the circuit* [e.g., where "DC_18V" (720) from the lower left—which in the combination of Ground 2 is the battery supply boosted to 12 volts and thus pre-regulated as discussed for [18.b]—is supplied to the "*voltage conversion circuit*" to the right]." EX1003, ¶¶493-500; EX1024, 4:23-29, 4:56-5:24, Figs.5-7.

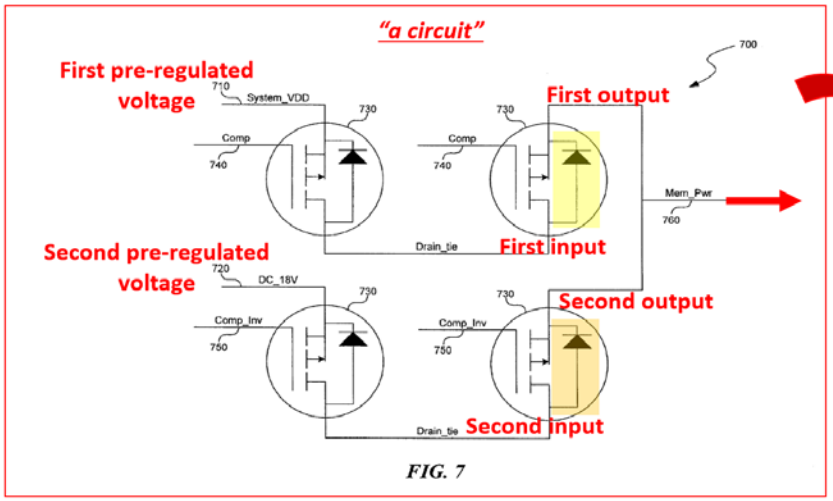


FIG. 7

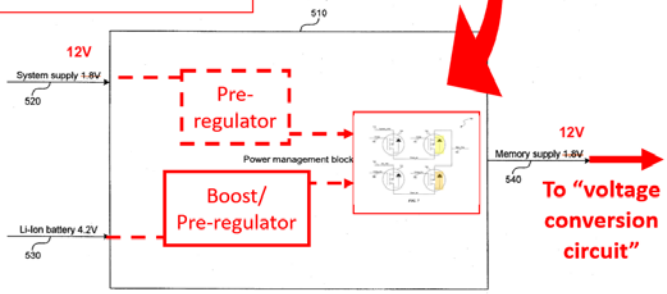
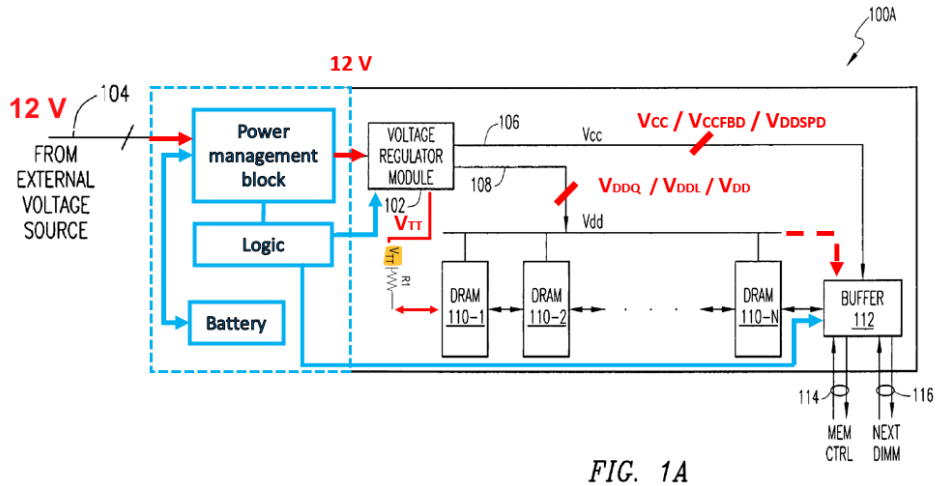


FIG. 5

Ground 2: Ground 1 and Battery Backup of Amidi



Voltage Mapping (A)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VDDL = 1.8V

Voltage Mapping (B)
1st : VDD / VDDQ = 1.8V
2nd : VCC = 1.5V
3rd : VCCFBD = 1.5V

Voltage Mapping (C)
1st : VDD / VDDQ = 1.8V
2nd : VCC / VCCFBD = 1.5V
3rd : VTT = 0.9V

FIG. 1A

13. Claim 20

Grounds 2A-2C teach "*claim 19, wherein the circuit* [from [19.a], e.g., the power switch multiplexer in Amidi's Figure 7, above (p.67), inside the "Power

management block" (blue, above)] *includes a first diode* [yellow, above (p.67), EX1024, 5:3] *having a first input and a first output, the first input is coupled to the first pre-regulated voltage* [from [18.a] and [19.a], upper left] *and the first output* [e.g., "Mem_Pwr" output (760), above (p.67)] *is coupled to the voltage conversion circuit, and wherein the circuit includes a second diode* [orange, above (p.67), EX1024, 5:17] *having a second input and a second output, the second input is coupled to the second pre-regulated voltage* [from [18.b] and [19.b], lower left] *and the second output is coupled to the first output* [e.g., "Mem_Pwr" output (760), above (p.67)] *and to the voltage conversion circuit* [as shown above (p.67)]." EX1003, ¶¶501-511; EX1024, 4:64-5:24, Fig.7.

14. Claim 21-30

Grounds 2A-2C teach claims 21-30 for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.a]	[16.a]	¶¶513-514 (¶¶450-452)
[21.b]	[20.a], [20.b]	¶¶515-517 (¶¶502-506, 507-511)
[21.c]	[18.a], [18.b]	¶¶518-520 (¶¶480-487, 488-492)
[21.d]	[19.a]	¶¶521-523 (¶¶494-497)

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.e]	[19.b]	¶¶524-526 (¶¶498-500)
[22]	[20.a], [20.b]	¶¶527-530 (¶¶502-506, 507-511)
[23.a]	[4.b], [6.b][5]	¶¶532-534 (¶¶306-314, 345-355)
[23.b]	[5.c]	¶¶535-537 (¶¶334-340)
[24.a]	[1.a]	¶¶539-541 (¶¶217-223)
[24.b]	[1.b]	¶¶542-544 (¶¶224-232)
[24.c]	[1.c]	¶¶545-547 (¶¶233-260)
[24.d.1]	[1.d.1]	¶¶548-550 (¶¶261-266)
[24.d.2]	[1.d.2]	¶¶551-553 (¶¶267-271)
[24.d.3]	[1.d.5]	¶¶554-556 (¶¶285-287)
[24.e.1]	[16.e.1][6]	¶¶557-559 (¶¶468-471)
[24.e.2]	[23.a], [23.b]	¶¶560-562 (¶¶532-537)
[24.e.3]	[23.b]	¶¶563-565 (¶¶535-537)

[5] See note 4 on p.58.

[6] Because the PCB has the claimed "*interface*" as shown above (pp.20-25), receiving an input voltage "from the host system ***via the interface***" for [16.e.1] also discloses receiving the input voltage "from the host system ***via the interface <u>of the PCB</u>***" for [24.e.1]. EX1003, ¶559.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[25]	[16.e.2]	¶¶566-569 (¶¶472-474)
[26.a]	[18.a]	¶¶571-573 (¶¶480-487)
[26.b]	[18.b]	¶¶574-576 (¶¶488-492)
[27]	[20.a]	¶¶577-580 (¶¶502-506)
[28]	[20.b]	¶¶581-584 (¶¶507-511)
[29]	[17]	¶¶585-588 (¶¶475-478)
[30]	[9.b], [11.b]	¶¶589-592 (¶¶391-394, 407-410)

C. Ground 3

Ground 3 renders obvious claims 1-30.

1. Ground 3 combination: Ground 2 + Hajeck (EX1038)

Ground 3 combines Ground 2 with the teachings of Hajeck, which discloses a "voltage detection circuit 48" for detecting both undervoltage and overvoltage anomalies in memory subsystems. EX1038, 3:30-40, Fig.1; EX1003, ¶¶181-188. Hajeck is analogous art to Harris and Amidi in Ground 2 as all relate to memory subsystems in general and protecting against power disruptions in particular. EX1003, ¶183. A POSITA would have been motivated to combine Ground 2 with Hajeck, and had a reasonable expectation of success in doing so, because Amidi discloses providing battery backup upon detecting undervoltage anomalies, EX1024, 4:44-53, and Harris teaches the need to detect both undervoltage and

overvoltage anomalies beyond a "15%" threshold, EX1023, ¶[0013], and Hajeck teaches how to detect both undervoltage and overvoltage anomalies to avoid data loss, EX1038, 1:10-31, 3:30-40, 4:62-65, consistent with techniques that were already well-known, *see, e.g.*, EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5; EX1063, pp.1-2; EX1061, p.15; EX1062, p.15. Thus, a POSITA would have looked to Hajeck's teachings related to overvoltage anomalies when implementing Amidi's voltage supervisory block in Ground 2 so that it detects both undervoltage and overvoltage anomalies. EX1003, ¶¶186-188.

The teachings of Hajeck do not affect any of the voltage mappings in Ground 2, and thus the voltage mappings for Grounds 3A-3C are the same as those for Grounds 2A-2C above (pp.27, 41-45).

2. Claims 1-30

Ground 3 renders obvious claims 1-30 for at least the same reasons provided above for Ground 2 (pp. 45-70). To the extent one were to argue that Ground 2 fails to teach overvoltage detection as required by [6.b] ("*the input voltage having a voltage amplitude above a predetermined threshold voltage*") and as discussed above (pp.52-54) — and required by claims 7, 9-12, 17, and 29-30 — such overvoltage detection was obvious in light of Hajeck in the combination for Ground 3. EX1003, ¶¶354-355. As explained above for the combination of Ground 3 (pp.70-71), a POSITA would have looked to Hajeck's teachings about

overvoltage anomalies when implementing Amidi's voltage supervisory block to detect both undervoltage and overvoltage anomalies. EX1003, ¶¶186-188. In particular, in the combination for Ground 3, Amidi's voltage supervisory block would be modified to detect voltage anomalies and switch to the backup power not only "[i]f system supply 605 has a magnitude lower than reference voltage 675" as disclosed by Amidi (EX1024, 4:44-52), but also "when the voltage exceeds a certain level" as taught by Hajeck (EX1038, 3:30-43; *see also id.* Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, Fig. 1). Thus, Ground 3 further teaches both overvoltage and undervoltage detection and protection, further rendering obvious claims 6, 9, 17, 29, and their dependents (7, 10-12, and 30). EX1003, ¶¶354-355, 389, 478, 588.

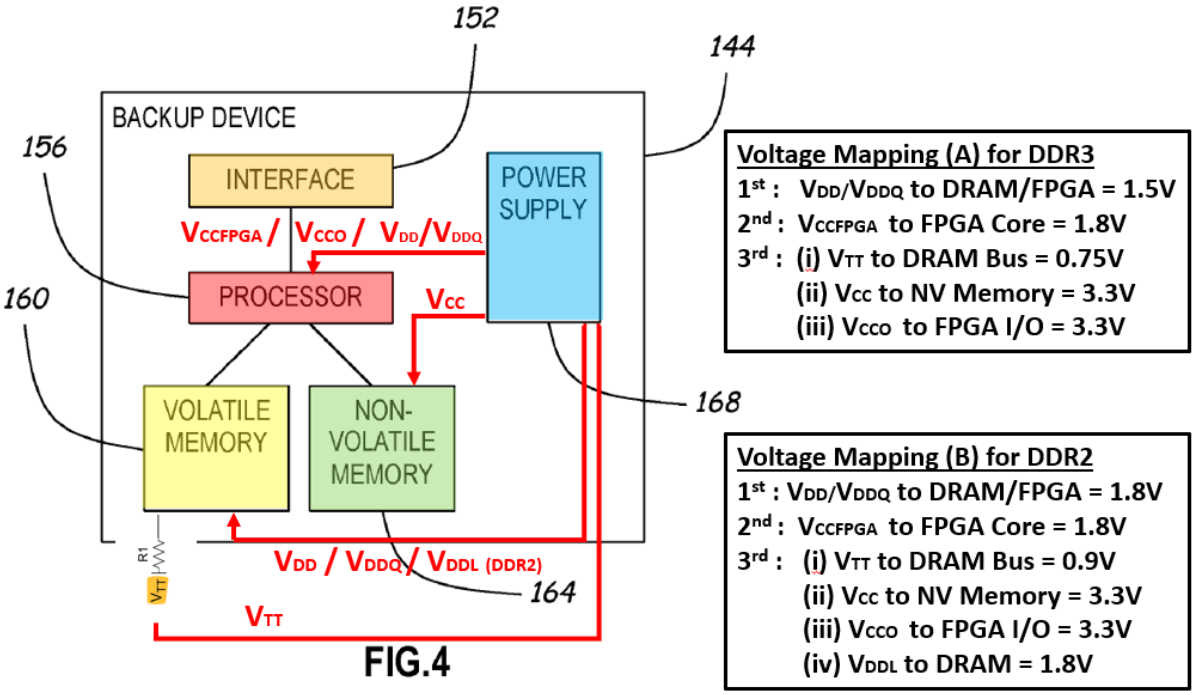
D. Ground 4

Ground 4 renders obvious claims 1-30.

1. Ground 4 combination: Spiers (EX1025) + Amidi (EX1024)

Ground 4 is based on Spiers in view of Amidi, implemented with DDR2 or DDR3 SDRAMs as follows:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



EX1003, ¶¶189-207; EX1025, Fig.4.

Spiers is remarkably similar to the 054 Patent: in the event of a power disruption, both teach transferring data from the volatile (SDRAM) memory (yellow) to the non-volatile (NAND flash) memory (green), as discussed previously (pp.4-6, 13-14). Amidi is analogous art that is similarly directed to providing backup capabilities to memory modules in the event of power disruptions, as discussed above (pp.11-12). A POSITA would have been motivated to consult Amidi's disclosure when implementing Spiers to learn specific implementation details, such as specific type of SDRAM devices and voltage regulators. EX1003, ¶¶197-201.

For example, Spiers teaches using volatile SDRAM devices in general, EX1025, ¶[0010], Fig.5 (190), while Amidi specifically discloses DDR SDRAM devices, EX1024, claims 4-5. A POSITA would have been familiar with the JEDEC standards for DDR2 (EX1026) and DDR3 (EX1046) SDRAMs, which specify particular voltages required for those memory devices. EX1003, ¶¶199-201. Indeed, DDR SDRAM (like NAND flash) was "off-the-shelf…commercially available." EX1064, ¶¶[0032, 29, 36-37]. Thus, a POSITA would have been motivated to implement Spiers with DDR2 or DDR3 SDRAMs powered according to the relevant standards, and had a reasonable expectation of success when using such well-known, standardized technology. EX1003, ¶¶199-201.

Ground 4, as summarized in the annotated figure above (p.73), includes DDR2 or DDR3 SDRAMs with the standard voltages below, and thus a POSITA would have been motivated to implement Spiers's Power Supply (168 above, blue) to supply these voltages. EX1003, ¶¶201-207.

- DDR3:

- 1.5V for **V_{DD}/V_{DDQ}** to DDR3 SDRAM (160, yellow) and the Processor (156, red, which could be implemented using an FPGA according to Spiers, EX1025, ¶[0037]).[7] EX1046, p.10:

V_{DDQ}	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply: 1.5 V +/- 0.075 V
V_{SS}	Supply	Ground
V_{REFDQ}	Supply	Reference voltage for DQ
V_{REFCA}	Supply	Reference voltage

- 0.75V for **V_{TT}** to resistors and DDR3 SDRAM. *Id.*, p.109 ("$V_{TT}=V_{DDQ}/2$").

- DDR2:

[7] The Processor would also receive V_{DD}/V_{DDQ} to be able to interface with the SDRAMs. EX1003, ¶204; EX1025, Fig.5 (showing 64-bit bus between the processor 198 and the SDRAMs 190). Spiers teaches the Processor may be implemented using an FPGA, EX1025, ¶[0037], which were designed to receive a separate voltage to interface with devices (such as SDRAMs). EX1003, ¶204; EX1067, p.2-23 (showing separate voltages V_{CCIO0}-V_{CCIO7}, one for each interface of the FPGA); 2-24 to 2-25 (tables listing different communication standards supported by the FPGA).

- 1.8V for **V_{DD}/V_{DDQ}** to DDR2 SDRAM (160, yellow) and the Processor (156, red).[8] EX1026, pp.6-7.
- 1.8V for **V_{DDL}** to DDR2 SDRAM (160, yellow). *Id.*:

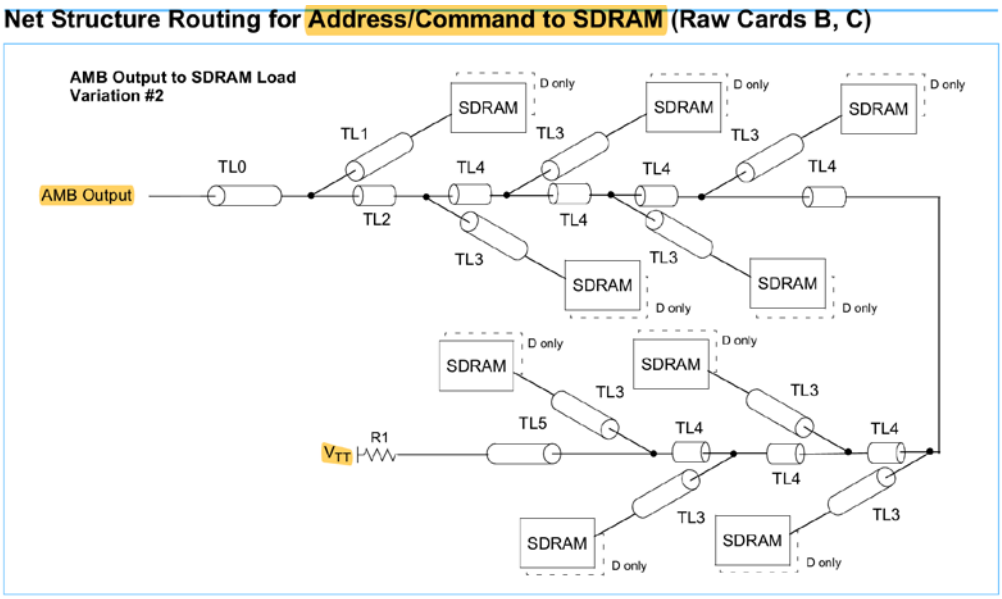
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

- 0.9V for **V_{TT}** to resistors and DDR2 SDRAM. *Id.*, p.71 ("V_{TT}=V_{DDQ}/2").

- 3.3V for **V_{CC}** to non-volatile memory (164, green). EX1025, ¶[0037], Fig.5 (184, "3.3V"); EX1049, p.38.
- 3.3V for **V_{CCO}** to input/output of the Processor (156, red), which could be implemented using an FPGA according to Spiers. *Id.*; EX1042, pp.2, 16.
- 1.8V for **V_{CCFPGA}** to the core of the Processor (156, red). EX1025, ¶[0037], Fig.5 (206, "1.8V"); EX1042, pp.2, 16 (labeled V_{CCINT}).

See also EX1028, p.68:

[8] See note 7 directly above.



In the annotated figure for Ground 4 above (p.73), Voltage Mappings "A" and "B" (on the right) are simply different ways to apply the arbitrary labels "1st" through "3rd" to the voltages shown in red in the annotated figure. EX1003, ¶¶202-207.

Below, Ground 4A refers to Ground 4 above with Voltage Mapping "A," while Ground 4B refers to Ground 4 above with Voltage Mappings "B." *Id.*

2. Independent Claim 1

a) [1.a] Preamble

To the extent the preamble is limiting, Grounds 4A-4B teach "*[a] memory module* [e.g., Spiers's backup device 144 (below) implemented in a PCI card including volatile memory (SDRAMs 190, yellow) and non-volatile memory (NAND Flash 194, green), and configured to store data in a memory system] *comprising.*" EX1003, ¶¶597-600; EX1025, ¶¶[0034, 37], Figs. 3, 5.

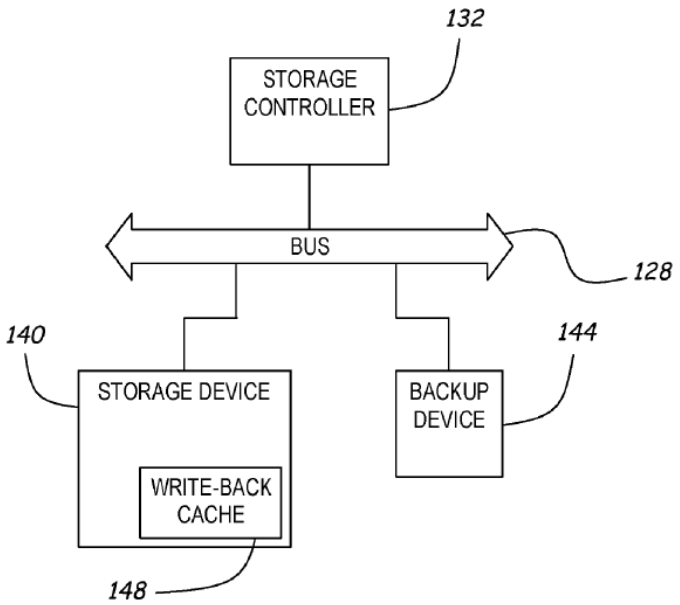
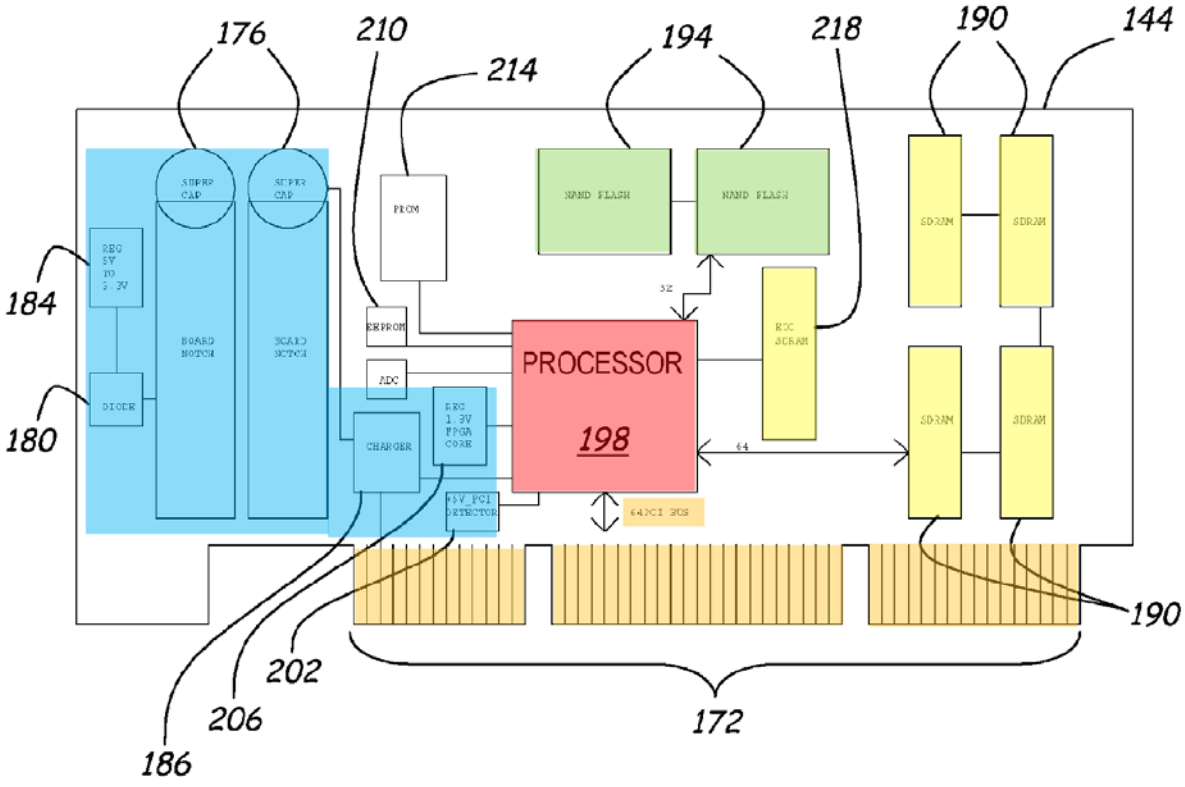

132
STORAGE CONTROLLER
BUS
128
140
144
STORAGE DEVICE
WRITE-BACK CACHE
BACKUP DEVICE
148

FIG.3


176
210
214
194
218
190
144
184
180
PROCESSOR
198
NAND FLASH
NAND FLASH
SDRAM
SDRAM
SDRAM
SDRAM
PROM
EEPROM
ADC
CHARGER
DIODE
64
64
190
202
206
186
172

b) [1.b] Printed Circuit Board Having an Interface

Grounds 4A-4B teach "*a printed circuit board (PCB)* [PCI card of backup device 144, above] *having an interface* [64-bit PCI card connector 172, orange above] *configured to fit into a corresponding slot connector of a host system* [e.g., "5 volt" PCI Board Connector, below], *the interface including a plurality of edge connections* [orange above]…." EX1003, ¶¶601-608; EX1025, Fig.5 (above); EX1031 (PCI standard), pp.114 (below), 152, 298.

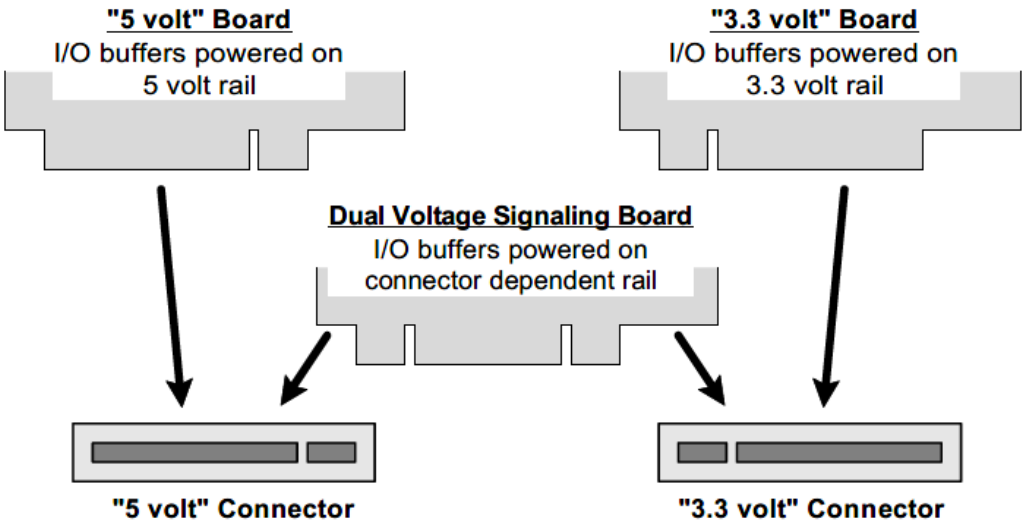


Figure 4-1: PCI Board Connectors

Grounds 4A-4B also teach that the "*edge connections*" are "*configured to couple power, data, address and control signals between the memory module and the host system*": The PCI connector 172 has "*edge connections configured to couple power*," including a +5V power supply monitored by +5V PCI detector 202. EX1003, ¶605; EX1025, ¶¶[0037, 54]; EX1031, pp.146-50. The "64-bit PCI

bus" "*edge connections*" of connector 172 also couple "*data, address and control signals*" with read or write commands from the host. EX1003, ¶¶606-608; EX1025, ¶¶[0037, 39], Figs. 9-11; EX1031, pp.1, 7 (Fig. 2-1, below), 10, 21-25 (below).

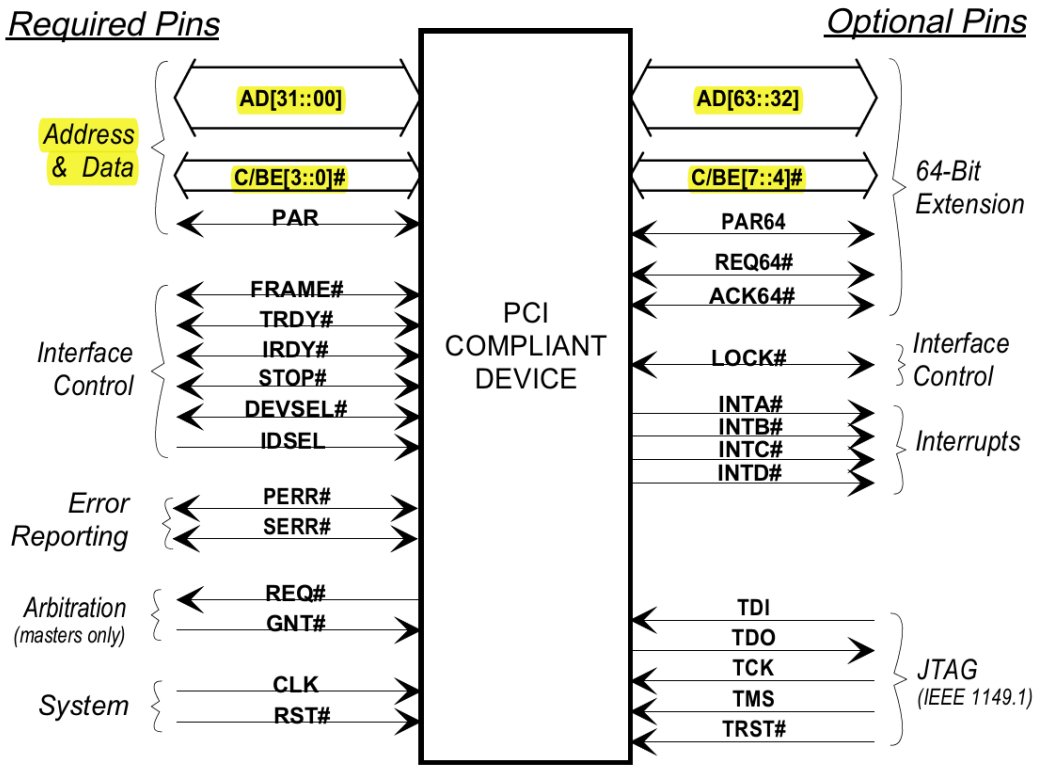


Figure 2-1: PCI Pin List

3.1.1. Command Definition

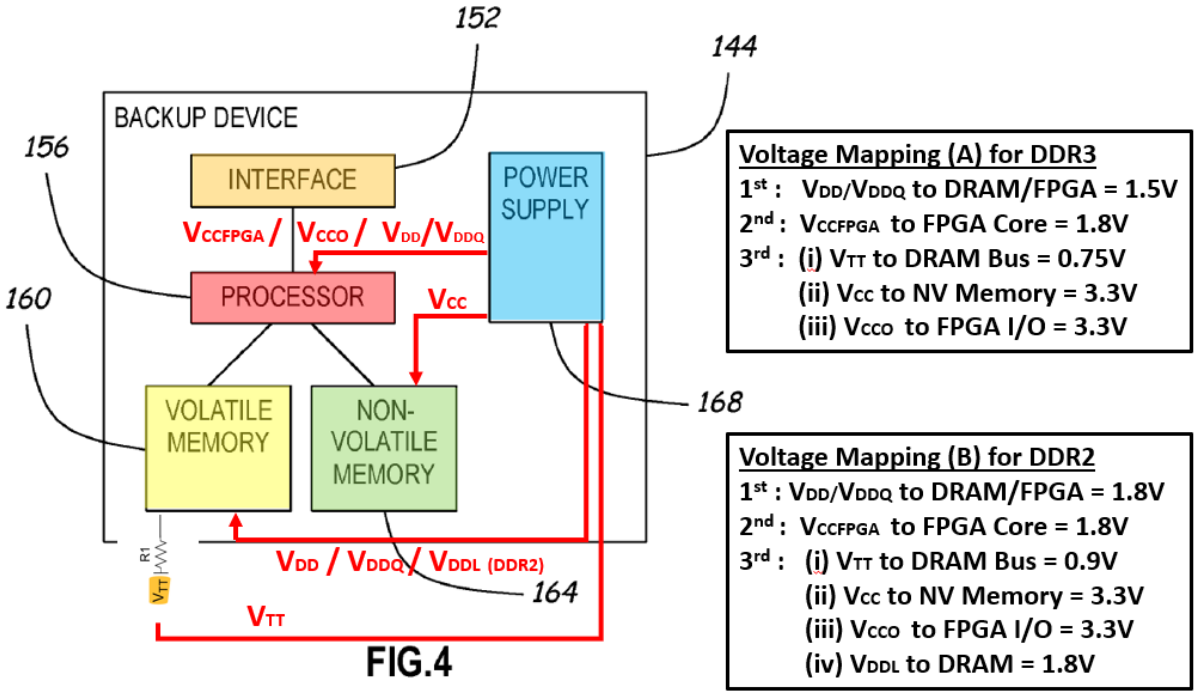
PCI bus command encodings and types are listed below, followed by a brief description of each. Note: The command encodings are as viewed on the bus where a "1" indicates a high voltage and "0" is a low voltage. Byte enables are asserted when "0".

C/BE[3::0]#	Command Type
0000	Interrupt Acknowledge
0001	Special Cycle
0010	I/O Read
0011	I/O Write
0100	Reserved
0101	Reserved
0110	Memory Read
0111	Memory Write
1000	Reserved
1001	Reserved
1010	Configuration Read
1011	Configuration Write
1100	Memory Read Multiple
1101	Dual Address Cycle
1110	Memory Read Line
1111	Memory Write and Invalidate

c) [1.c] A Voltage Conversion Circuit

Grounds 4A-4B teach "*a voltage conversion circuit coupled to the PCB* [e.g., Power Supply 168, blue below] *and configured to provide at least three regulated voltages* ["1st"/"*first*"; "2nd"/"*second*"; "3rd"/"*third*" below], *wherein the voltage conversion circuit includes at least three buck converters each of which is configured to produce a regulated voltage of the at least three regulated voltages*," when backup device 144 is implemented with DDR3 or DDR2 DRAMs as shown in Voltage Mappings A and B, respectively, below:

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



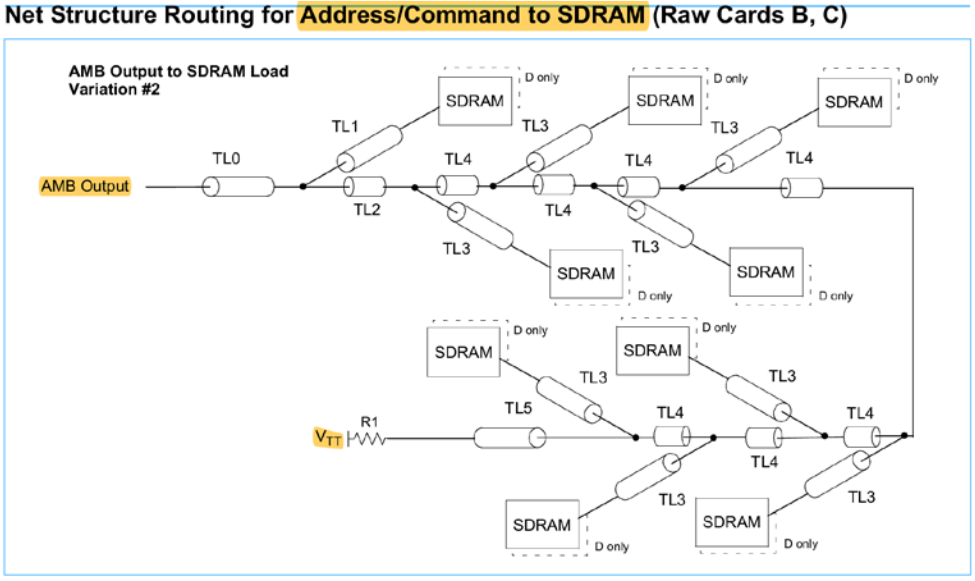
See supra pp.72-77; EX1003, ¶¶609-660.

	Voltage Mappings (Grounds 4-5)	
	A	B
"*first*":	V_{DD}/V_{DDQ}=1.5V	V_{DD}/V_{DDQ}=1.8V
"*second*":	V_{CCFPGA}=1.8V	V_{CCFPGA}=1.8V
"*third*":	(i) V_{TT}=0.75V (ii) V_{CC}=3.3V (iii) V_{CCO}=3.3V	(i) V_{TT}=0.9V (ii) V_{CC}=3.3V (iii) V_{CCO}=3.3V (iv) V_{DDL}=1.8V

Id. Ground 4B has "*voltage amplitude[s]*" that are the same, consistent with Netlist's apparent broad interpretation, EX1073, pp.59-61, while Ground 4A does not, consistent with a narrower interpretation. Furthermore, given that Grounds

4A-4B disclose a range of voltages, any specific voltage combinations within that range are obvious under Federal Circuit precedent discussed above (p.27).

Spiers discloses that the PCI card monitors and uses the "+5 volt" power supply of the PCI bus to power components of the card, including the SDRAM devices (190, 218) requiring power supply voltages, such as V_{DD} and V_{DDQ} ("*first regulated voltage*") and V_{DDL} ("*third regulated voltage*" (iv) in Mapping B), with amplitudes depending on the specific SDRAM type (DDR2, DDR3, etc.) as discussed above (pp.74-77). EX1003, ¶¶614-619, 634-635, 701; EX1025, ¶¶[0037, 54], Figs. 5, 14. A POSITA would have also recognized that a V_{TT} termination voltage ("*third regulated voltage*" (i) in Mappings A-B), whose amplitude is half of V_{DD}/V_{DDQ} as discussed above (pp.74-77), is also required for communicating with the DRAM devices, just like in an FBDIMM design. EX1003, ¶¶627-631; EX1025 Fig. 9, ¶¶[0037, 46]; EX1028, p.68 (below).



Spiers further discloses a voltage regulator 206 which provides V_{CCFPGA}=1.8V regulated power to the FPGA core ("*second regulated voltage*"). EX1003, ¶¶621-622; EX1025, ¶[0037], Fig. 5 (below, left). A POSITA would have also understood that different FPGAs had different voltage requirements for the FPGA core. EX1042, p.2 (labeled V_{CCINT} below, right).



	Spartan™-3/3E/3L	Spartan™-IIE	Spartan™-II	Virtex™-5	Virtex™-4	Virtex-II Pro™	Virtex™-II
V_{CCINT}	1.2V @0.2A-5A	1.8V @0.2A-1.5A	2.5V @0.2A-1A	1.0V @0.2A-15A	1.2V @0.2A-20A	1.5V @0.2A-20A	1.5V @0.2A-20A
V_{CCO}	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-0.5A	1.5V-3.3V @50mA-0.5A	1.2V-3.3V @50mA-5A	1.2V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A	1.5V-3.3V @50mA-3A
V_{CCAUX}	2.5V @50mA-0.3A	–	–	2.5V @50mA-0.7A	2.5V @50mA-0.7A	2.5V @50mA-0.3A	3.3V @50mA-0.3A

Spiers also discloses a voltage regulator 184 configured to step down a 5V backup voltage to a 3.3V output voltage which is used to transfer the data from the volatile to the non-volatile memories 194. EX1003, ¶¶632-633, 638-640; EX1025, Fig. 5 (below, left). A POSITA would have understood that 3.3V can be used as V_{CC} power to the non-volatile memories ("*third regulated voltage*" (ii) in Mappings A-B). *Id*., EX1049, p.38 (below, right).

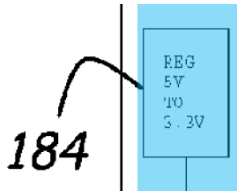
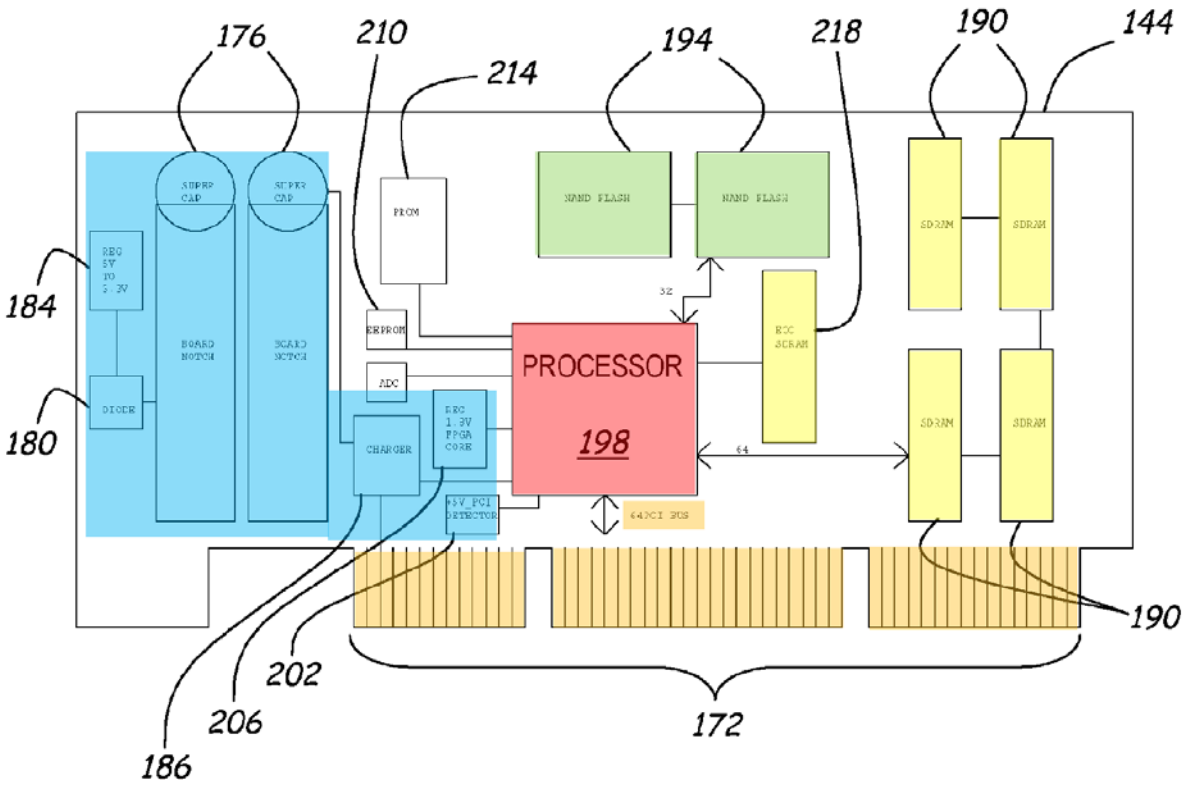


Table 12: Recommended Operating Conditions

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	^{t}A	0	–	+70	°C
	Extended	^{t}A	–40	–	+85	°C
Vcc supply voltage		Vcc	2.7	3.3	3.6	V
Supply voltage		Vss	0	0	0	V

A POSITA would have also understood that a converter circuit, such as voltage regulator 184 or another, similar voltage converter, is configured to provide a regulated voltage V_{CCO} of 3.3V ("*third regulated voltage*" (iii) in

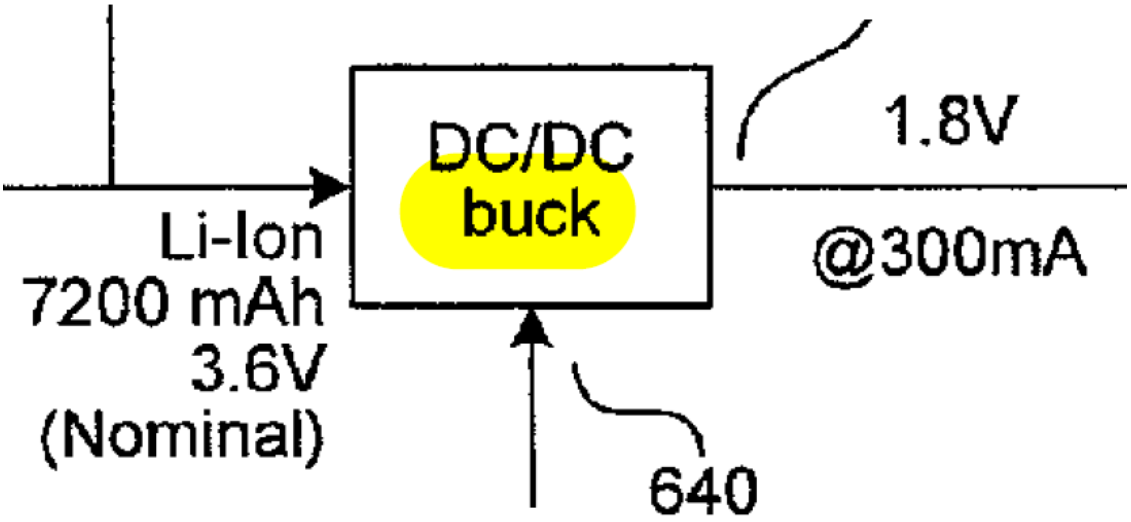
Mappings A-B) to an interface of the processor 198 (red) to transfer data to and from the non-volatile memories 194 (green). EX1003, ¶¶632-640; EX1042, pp.2, 16 (V_{CCO}).



Furthermore, it would have been obvious to a POSITA to use "*buck converters*," as taught by Amidi (below), to provide each of these regulated voltages from the +5V power supply, in order to achieve high efficiency, reliability, and flexible power conversion, as discussed previously (pp.29-30). EX1003, ¶¶649-659. Indeed, any loss at the power conversion creates heat that needs to be removed by additional cooling and takes away time from Spiers's backup operation, risking its successful completion. *Id.*; EX1025, Fig. 14 (step

752); EX1062, p.11 ("lower dissipation … saves the cost (and space) of cooling apparatus").

Buck converters powering SDRAM and FPGA devices from higher voltage sources were well known and commercially available at the time, as disclosed by Amidi (below, part of the combination in Ground 4) and others. EX1003, ¶¶651-653-655.



EX1024 (Amidi), Fig. 6 (640), 4:38-41; *see also* EX1047, 1:28-32, 2:47-55, 5:56-59, 7:6-14; EX1041, pp.1-2, 9 (first below); EX1042, p.16 (second below); EX1048, pp.1-2 (third below); EX1058, p.5 (fourth below).

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

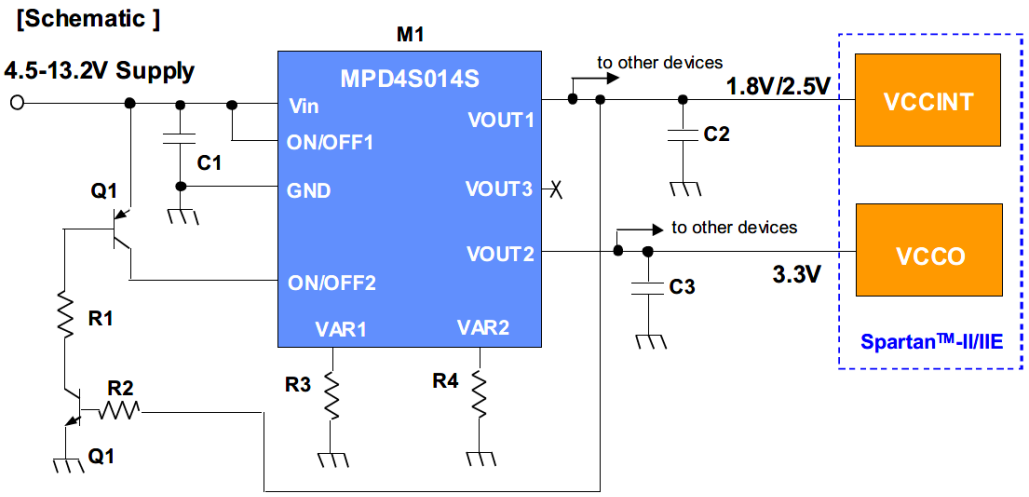
Applications

- DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

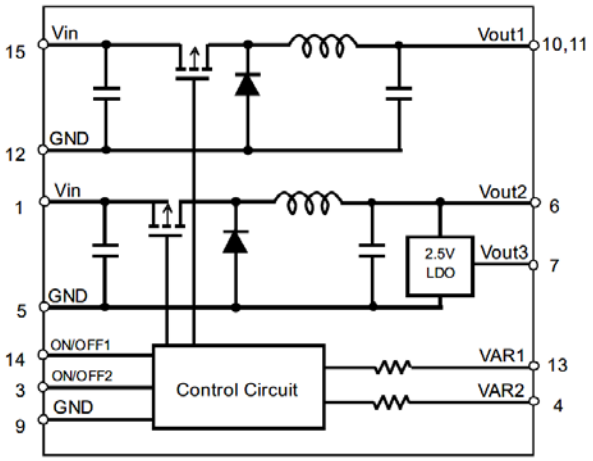
The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

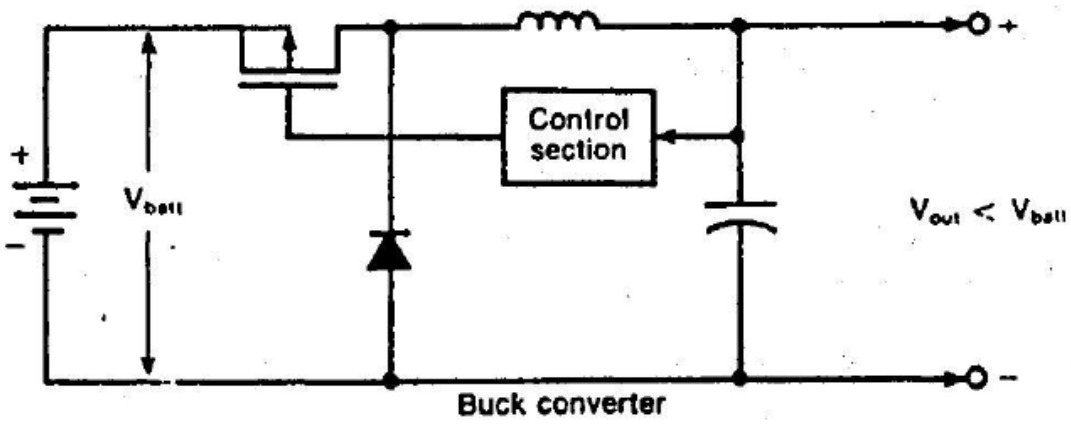


MPD4S014S_Specification
1

DC-DC Converter Specification(DRAFT)
MPD4S014S

6. Block Diagram





d) [1.d] A Plurality of Components Coupled to the PCB

(1) [1.d.1] Plurality of components each coupled to at least one regulated voltage

Grounds 4A-4B teach "*a plurality of components* [e.g., DRAM, FPGA/Processor, termination resistors, and non-volatile memory, as discussed above (pp.72-77) and shown below] *coupled to the PCB, each component of the plurality of components coupled to at least one regulated voltage of the at least three regulated voltages* [as discussed above (pp.72-77) and shown below]." EX1003, ¶¶661-664.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

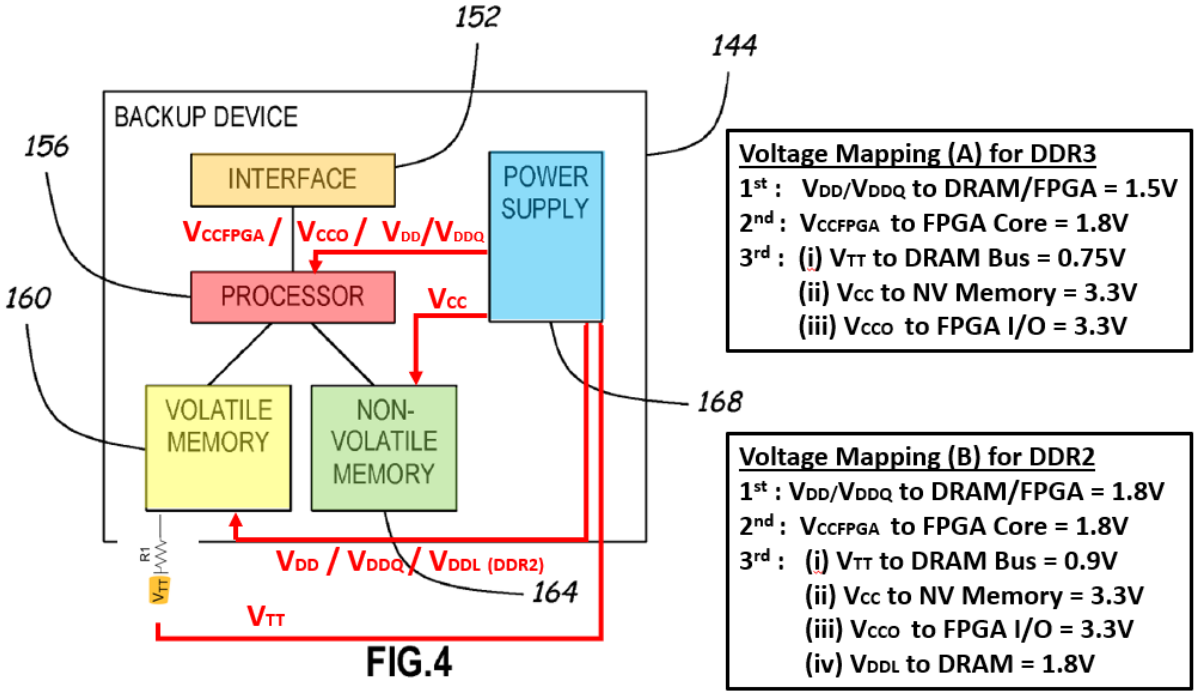


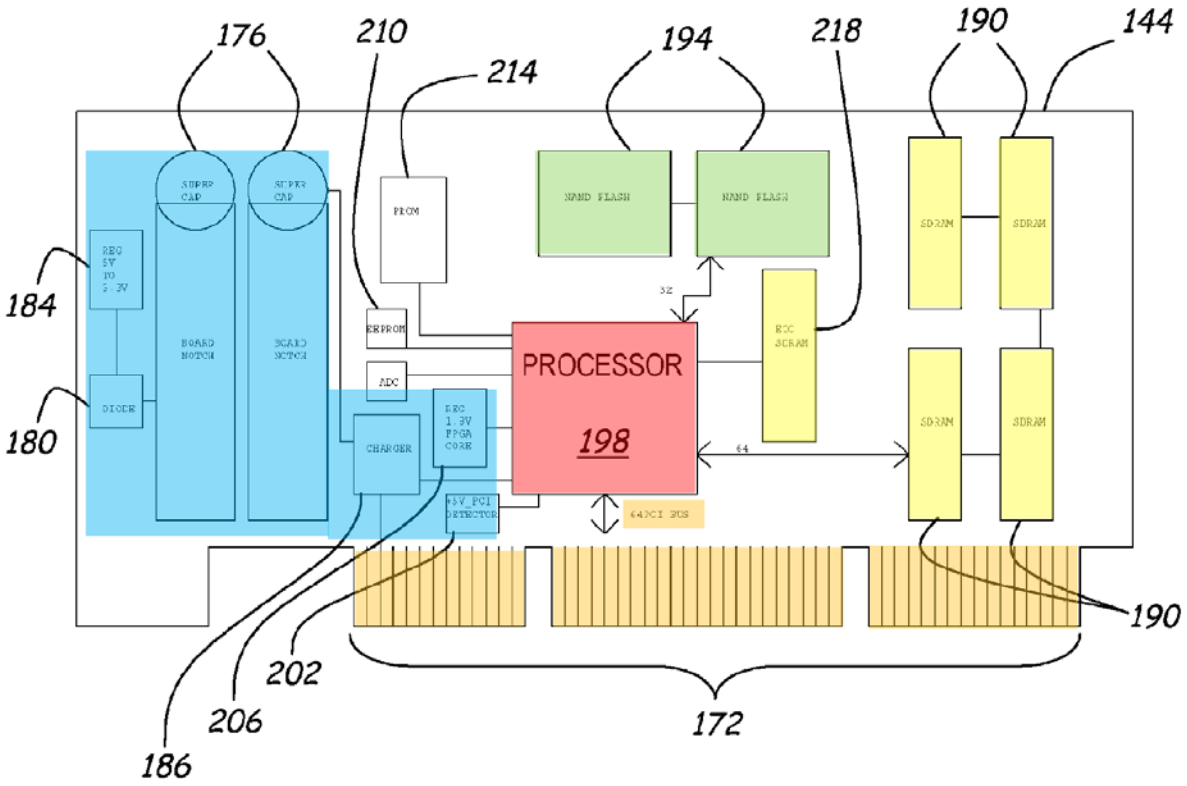
FIG.4

(2) [1.d.2] Plurality of components includes SDRAM devices

Grounds 4A-4B teach "*the plurality of components including a plurality of synchronous dynamic random access memory (SDRAM) devices*" [e.g., 190, yellow below, implemented as DDR2 or DDR3]" as discussed above (pp.72-77, 31). EX1003, ¶¶665-668.

(3) [1.d.3] A first circuit coupled to the SDRAM devices and first set of edge connections

Grounds 4A-4B teach "*a first circuit* [FPGA processor 198 (red)] *coupled to the plurality of SDRAM devices* [190, 218 (yellow)] *and to a first set of edge connections of the plurality of edge connections* [e.g., PCI interface 172 (orange) for data, address, and control signals from [1.b]]." EX1003, ¶¶671-672; EX1025, Fig. 5 (below), ¶[0037].



(4) [1.d.4] Wherein the first circuit is coupled to first and second regulated voltages

Grounds 4A-4B teach "*the first circuit* [FPGA processor (red)] *coupled to both the first* [e.g., V_{DD}/V_{DDQ} = 1.5V or 1.8V] *and second* [e.g., V_{CCFPGA}=1.8V] *regulated voltages*" as shown below and discussed above (pp.72-77, 82) and for [1.c]. EX1003, ¶¶674-683.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

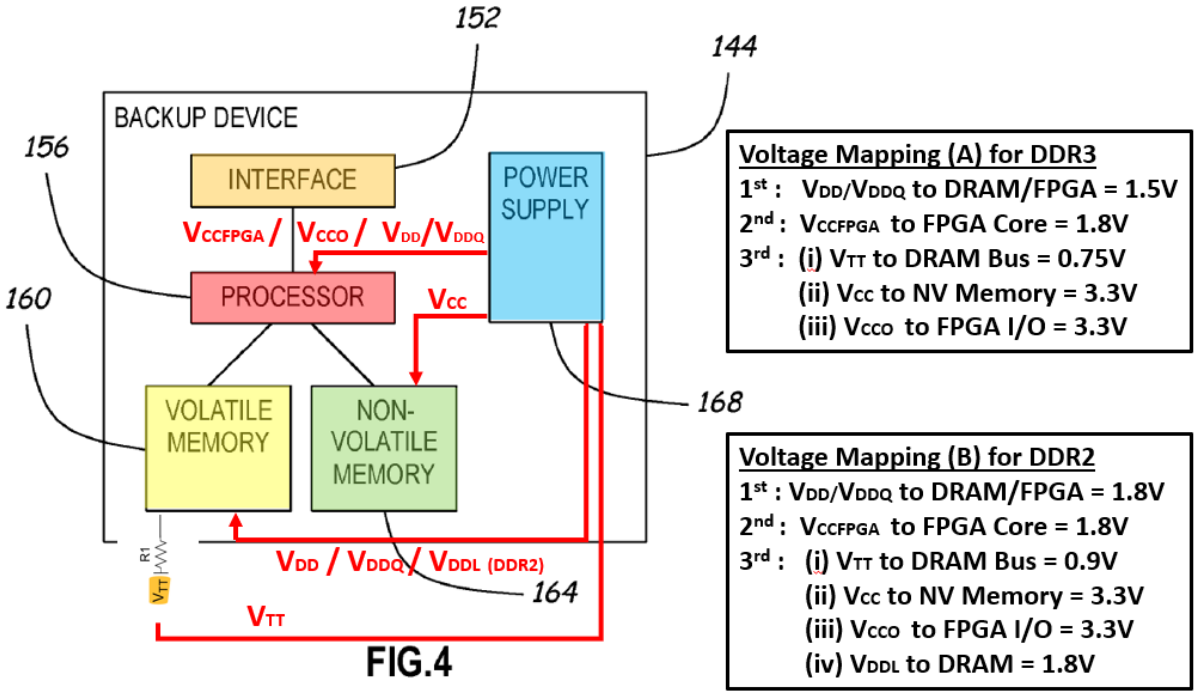


FIG.4

(5) [1.d.5] Wherein the SDRAM devices are coupled to the first regulated voltage

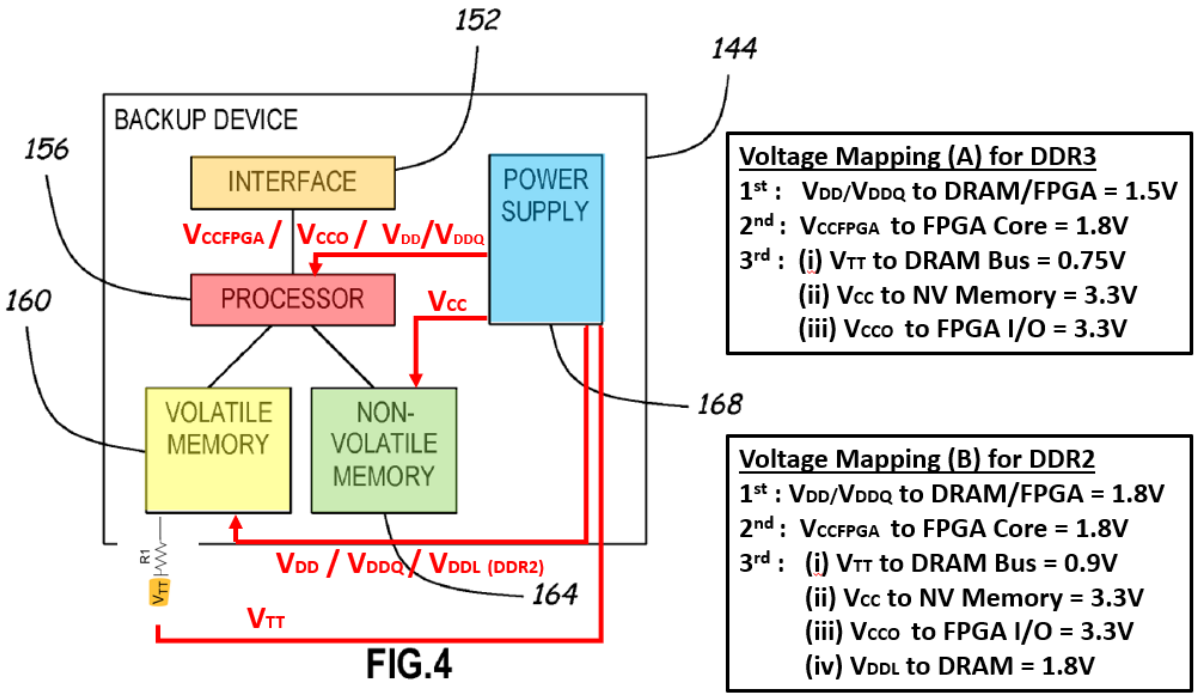
Grounds 4A-4B teach "*wherein the plurality of SDRAM devices* [e.g., Spiers's SDRAM from [1.d.1]-[1.d.2]] *are coupled to the first regulated voltage* [e.g., V_{DD}/V_{DDQ} = 1.5V or 1.8V] *of the at least three regulated voltages*," as shown above (pp.72-77, 82). EX1003, ¶¶684-687.

3. Claim 2

Ground 4A teaches "*claim 1, wherein the first regulated voltage has a first voltage amplitude* [e.g., V_{DD}/V_{DD}=1.5V], *and the second regulated voltage has a second voltage amplitude* [e.g., V_{CCFPGA}=1.8V], *wherein a first one of the first and second voltage amplitudes* [e.g., "1st"/"*first*"=1.5V] *is less than a second one of*

the first and second voltage amplitudes [e.g., "2nd"/"*second*"=1.8V]," as shown below and discussed above (pp.72-77, 82). EX1003, ¶¶688-697.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs



4. Claim 3

Ground 4B teaches "*claim 1, wherein a third regulated voltage of the at least three regulated voltages* [e.g., V_{DDL}=1.8V provided to the DDR2 SDRAMs as a separate voltage source from V_{DD} and V_{DDQ}] *has a voltage amplitude of 1.8 volts*" as shown below and discussed above (pp.72-77, 82) and for [1.c]. EX1003, ¶¶698-704.

Ground 4: Spiers in view of Amidi, with DDR2 or DDR3 DRAMs

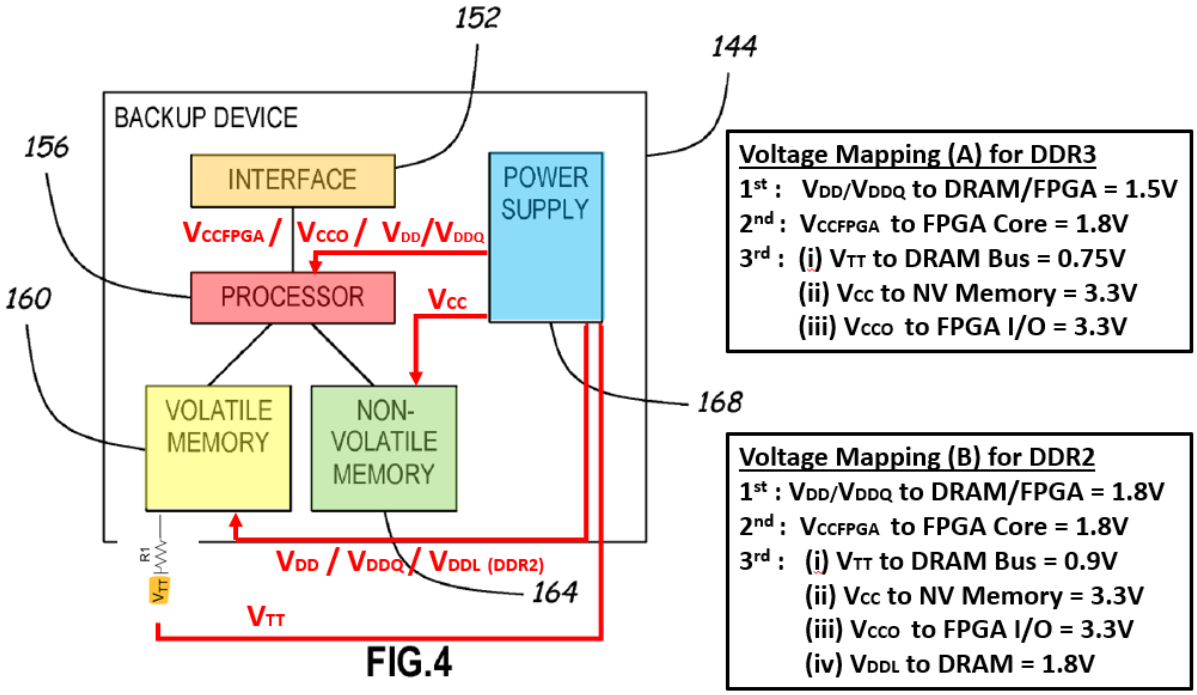


FIG.4

See also EX1026 (JESD79-2B), pp.2 (NOTE 5), 6-7 (annotated below), 9 (annotated below, showing order for applying V_{DDL} ***separately*** from V_{DD} and V_{DDQ}).

NOTE 5 VDDL and VSSDL are power and ground for the DLL. It is recommended that they be isolated on the device from VDD, VDDQ, VSS, and VSSQ

NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	**DQ Power Supply:** 1.8V +/- 0.1V
V_{SSQ}	Supply	**DQ Ground**
V_{DDL}	Supply	**DLL Power Supply:** 1.8V +/- 0.1V
V_{SSDL}	Supply	**DLL Ground**

Symbol	Type	Function
V_{DD}	Supply	**Power Supply:** 1.8V +/- 0.1V
V_{SS}	Supply	**Ground**
V_{REF}	Supply	**Reference voltage**

a) Apply power and attempt to maintain CKE below 0.2*VDDQ and ODT[*1] at a low state (all other inputs may be undefined.) The power voltage ramp time must be no greater than 20mS; and during the ramp, VDD>VDDL>VDDQ and VDD-VDDQ<0.3 volts.

- VDD, VDDL and VDDQ are driven from a single power converter output, AND
- VTT is limited to 0.95 V max, AND
- Vref tracks VDDQ/2.

or

- Apply VDD without any slope reversal before or at the same time as VDDL.
- Apply VDDL without any slope reversal before or at the same time as VDDQ.
- Apply VDDQ without any slope reversal before or at the same time as VTT & Vref.

at least one of these two sets of conditions must be met.

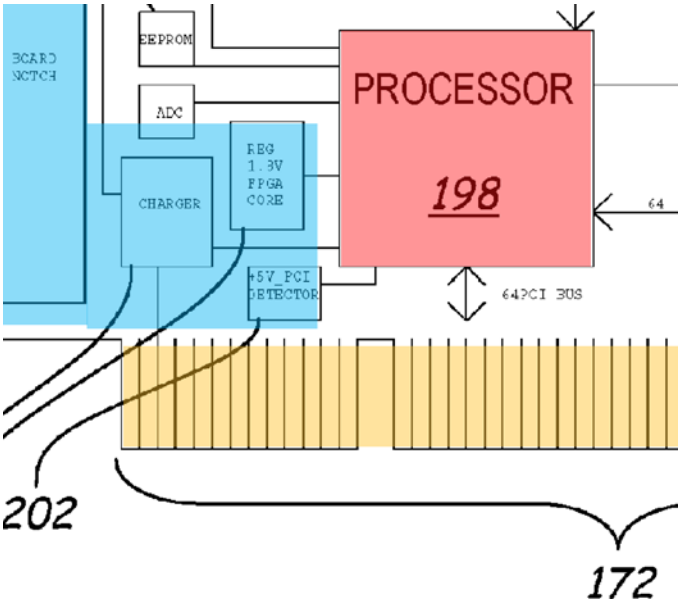
Insofar as the "*third regulated voltage*" must have a different amplitude than the "*first*" and "*second*" regulated voltages, Voltage Mapping A (where the "*first regulated voltage*" is V_{DD}/V_{DDQ}=1.5V) can be modified by swapping V_{CCFPGA}=1.8V as the "*third regulated voltage*" and V_{CCO}=3.3V as the "*second regulated voltage.*" Since V_{CCO} is coupled to the processor (156/198) to interface with the non-volatile memory (164/194) as discussed above (pp.72-77), claim limitations [1.d.4]-[1.d.5] (pp.91-92) are still satisfied after this modification, rendering claim 3 obvious. EX1003, ¶702.

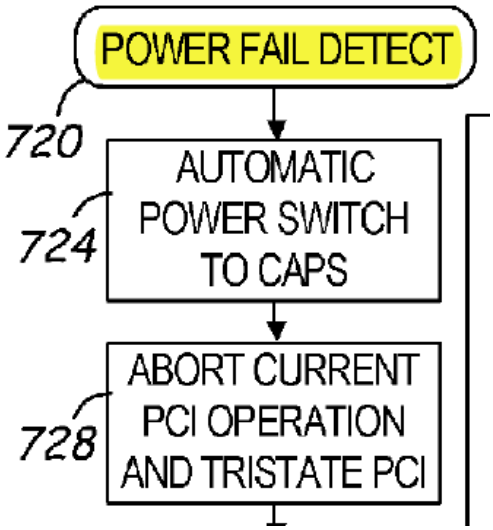
5. Claim 4

a) [4.a] Preamble and [4.b] Voltage Monitor Circuit

Grounds 4A-4B teach "*claim 1, further comprising: a voltage monitor circuit* [e.g., Spiers's +5V PCI detector 202 (blue, below)] *coupled to the PCB* [e.g., the PCB of Spiers's PCI card, see [1.b] (pp.79-81)] *and to a second set of edge connections of the plurality of edge connections* [from [1.b] (pp.79-81)], *the voltage monitor circuit configured to monitor an input voltage received from the*

second set of edge connections [e.g., monitors the +5V PCI supply voltage received at a +5V pin of the PCI connector 172 (orange, below)], *the voltage monitor circuit configured to produce a trigger signal* [e.g., Spiers's signal from detector 202 to processor 198 (red) at step 720 (Fig.14)] *in response to the input voltage having a voltage amplitude below a predetermined threshold voltage* [e.g., if the supply voltage is below a specified reference voltage, as Amidi teaches]." EX1003, ¶¶706-723; EX1025, ¶¶[0036-37, 54], Figs. (below, left), 14 (below, right).





See also EX1031, p.149 (showing PCI card pins for +5V supply ("*second set of edge connections*"), below).

Table 4-14: Pin Summary - 32-bit Expansion Board

Pin Type	5V Board	Universal Board	3.3V Board
Ground	22	18 (Note)	22 (Note)
+5 V	13	8	8
+3.3 V	12	12	17
I/O pwr	0	5	0
Reserv'd	4	4	4

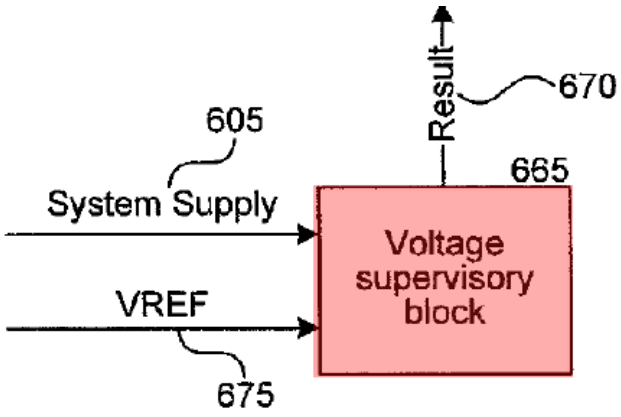
NOTE:

If the **M66EN** pin is implemented, the number of ground pins for a Universal board is 17 and the number of ground pins for a 3.3V board is 21.

Table 4-15: Pin Summary - 64-bit Board (incremental pins)

Pin Type	5V Board	Universal Board	3.3V Board
Ground	16	16	16
+5 V	6	0	0
+3.3 V	0	0	6
I/O pwr	0	6	0
Reserv'd	5	5	5

Amidi discloses details for power failure detection, and in the combination for Ground 4 it would have been obvious to implement Spiers's detector 202, as Amidi teaches, to generate a "*trigger signal*" (e.g., 670, below) "*in response to*" the system supply voltage (e.g., 605) ("*an input voltage having an amplitude*") being below a reference voltage (e.g., 675) ("*a predetermined threshold voltage*"). *See* EX1024, 4:44-52, 5:35-43, 8:23-29, 9:8-12, Figs. 5, 6 (excerpted, annotated below), 8, 14 (reproduced below), 15.



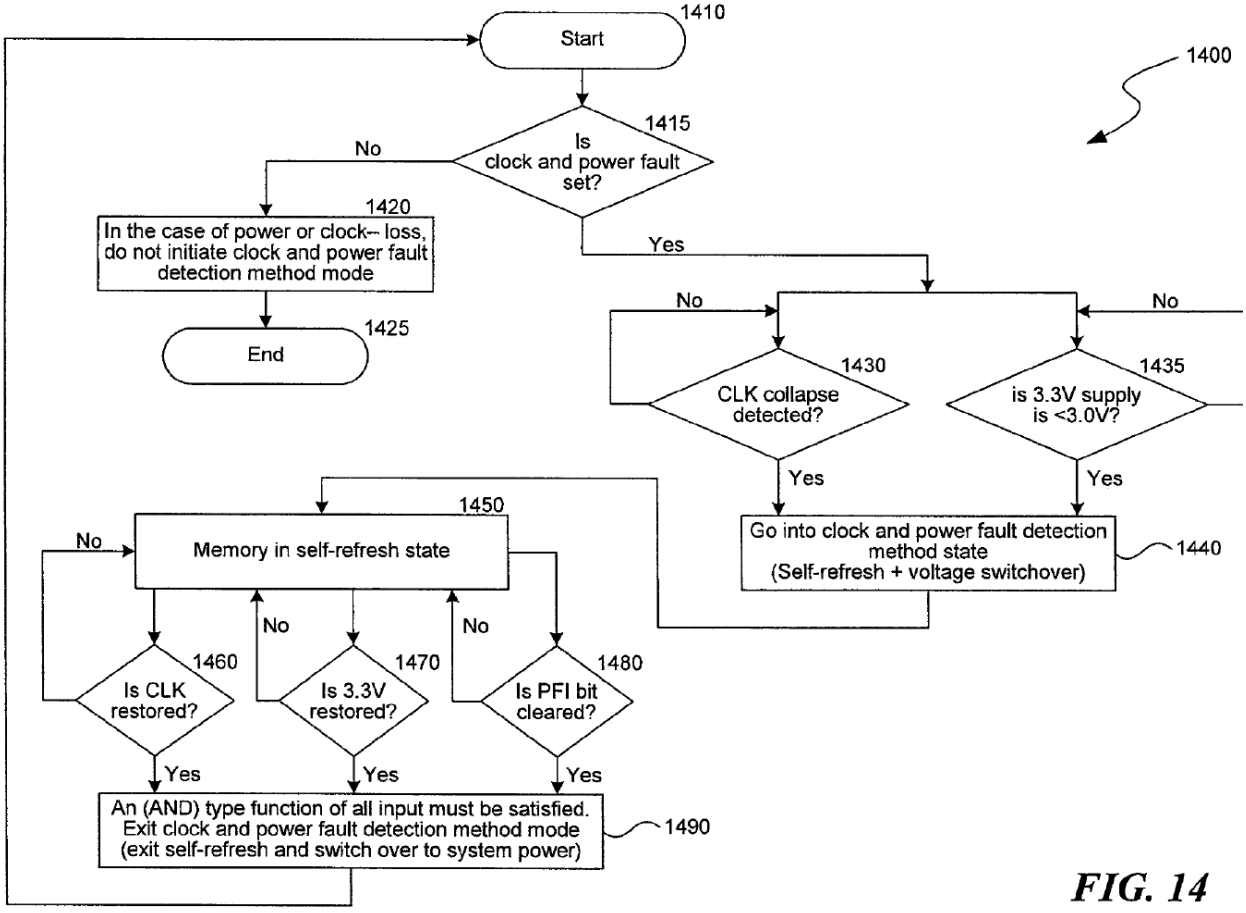


FIG. 14

Furthermore, Spiers's invention is not limited to detecting undervoltage conditions, EX1025, ¶[0041] ("power failure, power interruption, or other failure"), and thus it would have been obvious to implement Spiers's detector 202

to detect both undervoltage and overvoltage conditions, to avoid losing data or damaging the circuits. EX1003, ¶¶717-722; EX1023, ¶[0013] ("tolerance (e.g., around +/−15%) can be accommodated."). Detecting both undervoltage and overvoltage conditions was common practice and included in commercially-available products, including specifically for PCI products like Spiers. EX1063, pp.1-2 (below); EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

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PCI Local Bus Power Supervisor

DC Electrical Characteristics

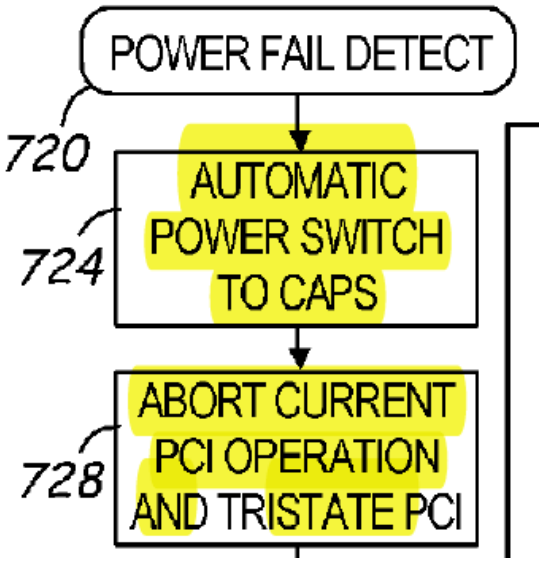
Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

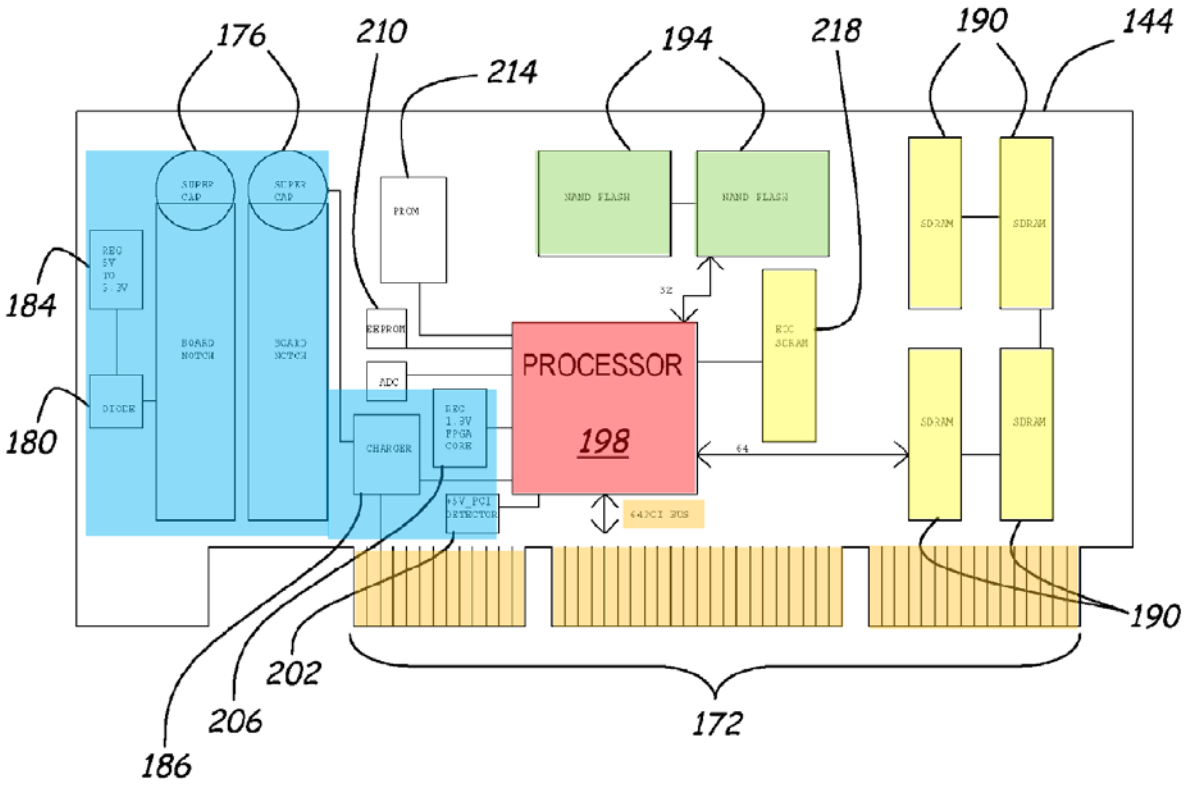
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

b) [4.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

Grounds 4A-4B teach "*wherein the memory module transitions from a first operable state* [e.g., normal operation with the PCI +5V power] *to a second*

operable state [e.g., backup operations with capacitor power and the PCI bus disconnected] *in response to the trigger signal*." EX1003, ¶¶724-730. Spiers discloses that, if a power failure is detected (step 720), the backup device processor switches power from the PCI bus to capacitors (step 724) and disconnects the PCI bus (step 728). EX1025, ¶[0054], Figs. 5, 14 (reproduced below in part, annotated).





Spiers teaches that backup capacitor power is provided to the volatile SDRAM (e.g., 190, yellow above), non-volatile NAND flash (e.g., 194, green above), and EEPROM (e.g., 210, white above) while data transfers from the SDRAM to the NAND and corresponding information is stored in the EEPROM. EX1003, ¶728; EX1025, ¶¶[0034, 36-37, 54-56], Figs.5 (above), 14 (below, red for power failure detection, yellow for examples of storing information to non-volatile memory, and orange for data transfer from SDRAM to NAND flash).

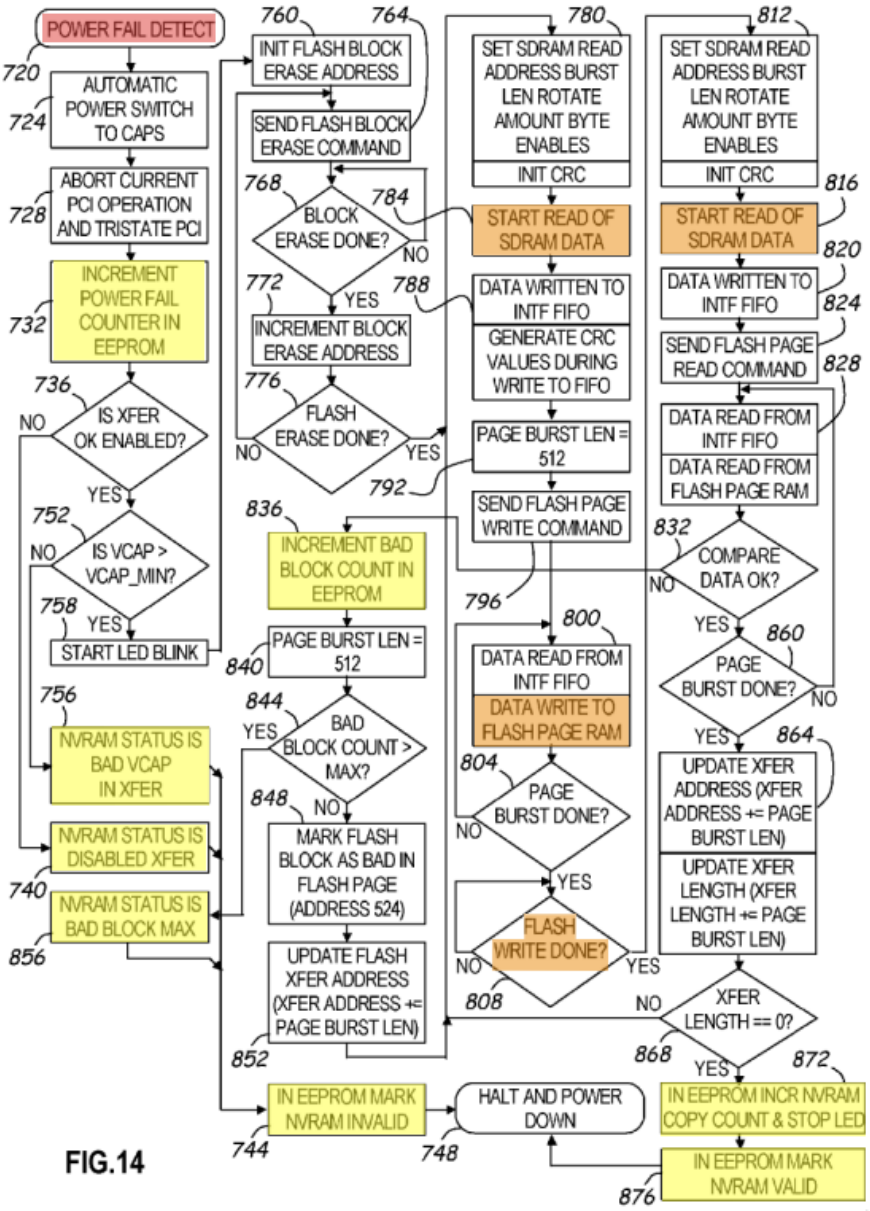


FIG.14

6. Claim 5

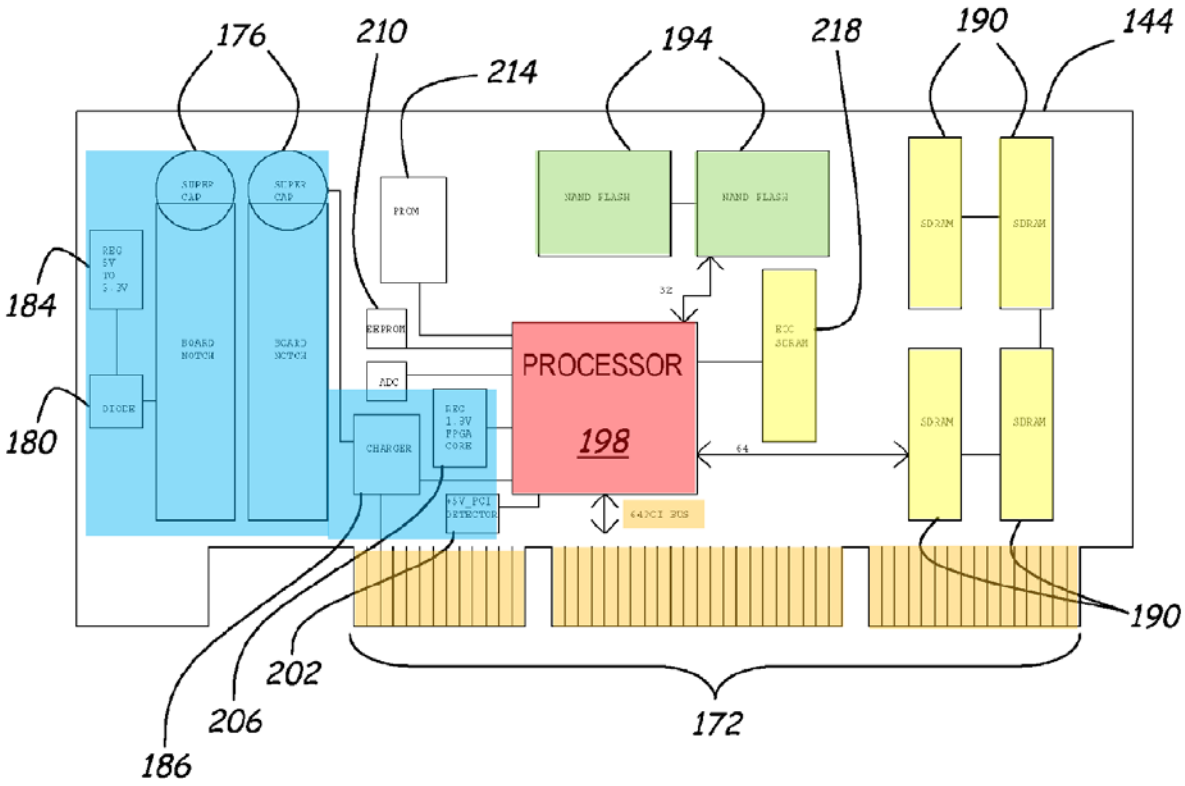
a) [5.a] Preamble and [5.b] Controller Coupled to the Voltage Monitor Circuit

Grounds 4A-4B teach "*claim 4, further comprising a controller* [e.g., including logic implemented in Spiers's processor 198] *coupled to the voltage monitor circuit* [e.g., Spiers's +5V PCI detector 202]." EX1003, ¶¶731-738. As

discussed above for [4.c] (pp.99-102), Spiers discloses logic implemented in its processor that is coupled to the +5V PCI detector 202 (*the voltage monitor circuit*") and that performs operations in response to a power failure detection.

b) [5.c] Wherein the Controller is Configured to Perform One or More Operations

Grounds 4A-4B teach "*wherein, in response to the trigger signal* [from [4.b], e.g., an indication of a power failure by Spiers's detector 202], *the controller is configured to perform one or more operations including a write operation to transfer data to non-volatile memory* [e.g., the logic in processor 198 performs operations in response to the power failure indication, including transferring and writing data from volatile SDRAMs (yellow, below) to non-volatile NAND flash (green, below)]" as discussed above for [4.c] (pp.99-102). EX1003, ¶¶739-744; EX1025, Abstract, ¶[0055], Fig.5 (below), 14 (illustrating data transfer process, below).


176
210
214
194
218
190
144
184
180
186
206
202
172
190
PROCESSOR
198
NAND FLASH
NAND FLASH
SDRAM
SDRAM
SDRAM
SDRAM
PROM
EEPROM
ADC
CHARGER
DIODE
SUPER CAP
SUPER CAP
BOARD NOTCH
BOARD NOTCH
32
64
64PCI BUS

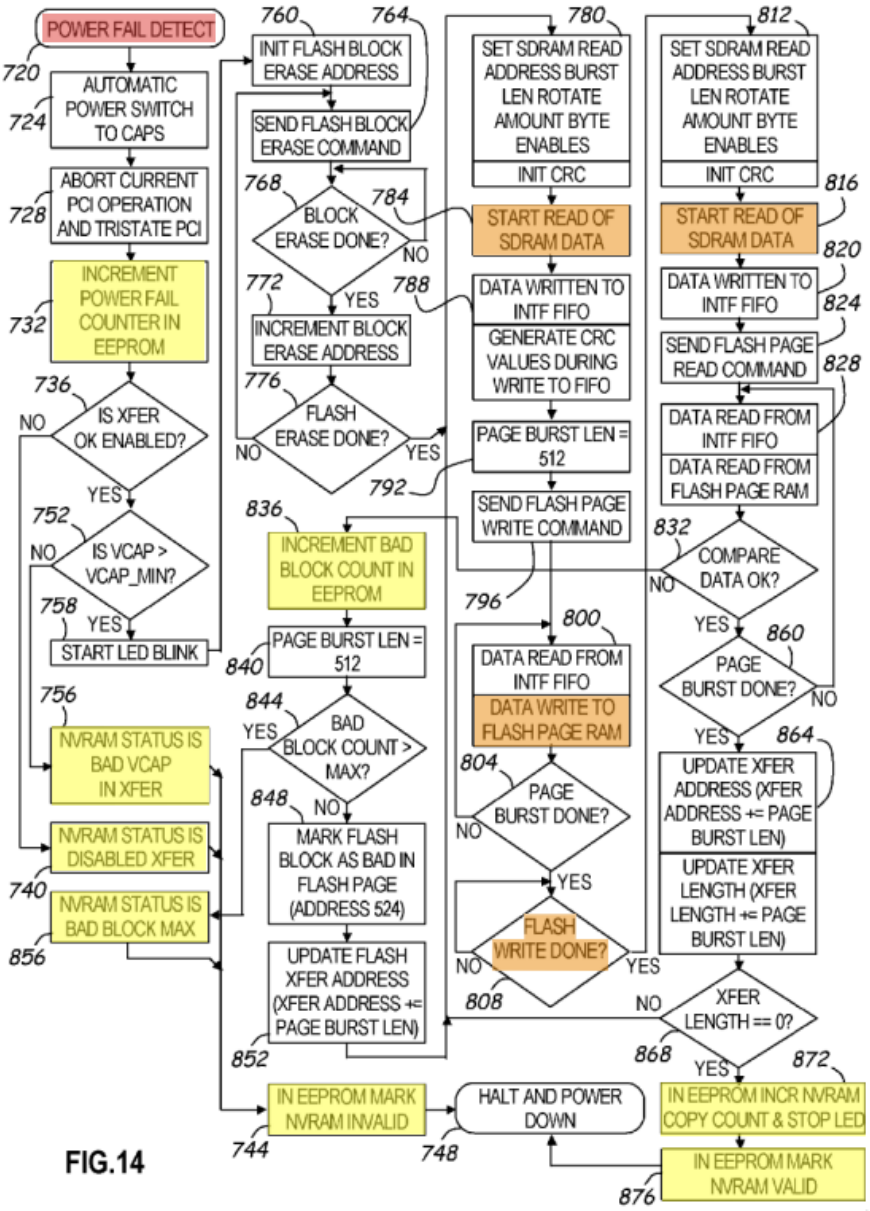


FIG.14

Spiers teaches that the logic in the processor 198 performs write operations of user data to the NAND flash 194, because Spiers's module receives address and data with corresponding read or write commands to store and retrieve user data, EX1025, ¶[0037]; EX1031, pp.1, 7 (Fig. 2-1, below), 21-25, and because Spiers teaches that its backup device includes both volatile and non-volatile memory "into

which data is moved in the event of a power failure," EX1025, ¶[0034, 39], Figs.9-11 (illustrating steps associated with receiving commands and transferring data between the host memory and the SDRAMs). EX1003, ¶¶742-743.

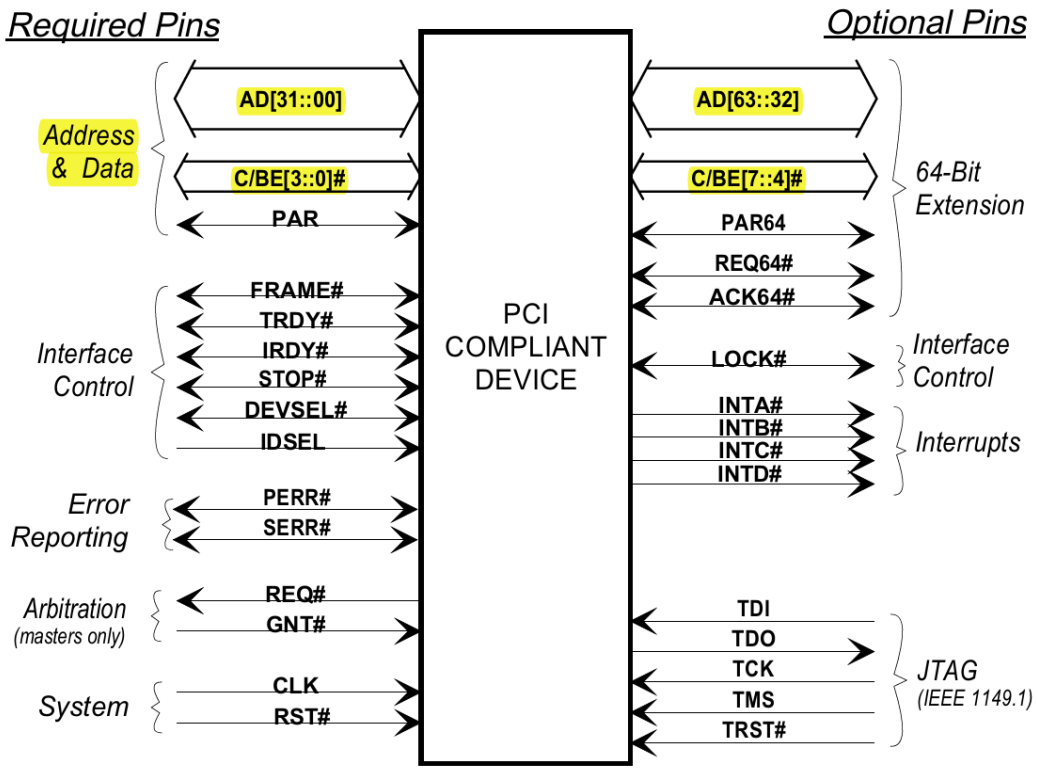


Figure 2-1: PCI Pin List

7. Claim 6

a) [6.a] Preamble and [6.b] Voltage Monitor Circuit

Claim 6 is similar to claim 4, except it concerns overvoltage detection rather than undervoltage detection as in [4.b] (pp.95-99): "*claim 1, further comprising: a voltage monitor circuit coupled to the PCB* [similar to [4.b]] *and to a second set of edge connections of the plurality of edge connections* [similar to [4.b]], *the voltage monitor circuit configured to monitor an input voltage received from the second*

set of edge connections [similar to [4.b]], *the voltage monitor circuit configured to produce a trigger signal* [similar to [4.b]] *in response to the input voltage having a voltage amplitude above a predetermined threshold voltage* [discussed below]." EX1003, ¶¶746-758.

Grounds 4A-4B teach claim 6, including overvoltage protection, for the reasons provided above in the discussion of [4.b] (pp.95-99). Spiers's invention is not limited to detecting undervoltage conditions, EX1025, ¶[0041] ("power failure, power interruption, or other failure"), and a POSITA would have been motivated to implement Spiers's detector 202 to detect both undervoltage and overvoltage conditions to avoid losing data or damaging the circuits. EX1003, ¶¶709-723; EX1023, ¶[0013] ("tolerance (e.g., around +/−15%) can be accommodated."). Detecting both undervoltage and overvoltage conditions was common practice and included in commercially available products, including specifically for PCI products like Spiers. EX1063, pp.1-2 (below); EX1061, p.15 (Analog Device circuit for "undervoltage" and "overvoltage" detection); EX1062, p.15 (same); EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5 (similar).

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DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

b) [6.c] Wherein the Memory Module Transitions from a First Operable State to a Second Operable State

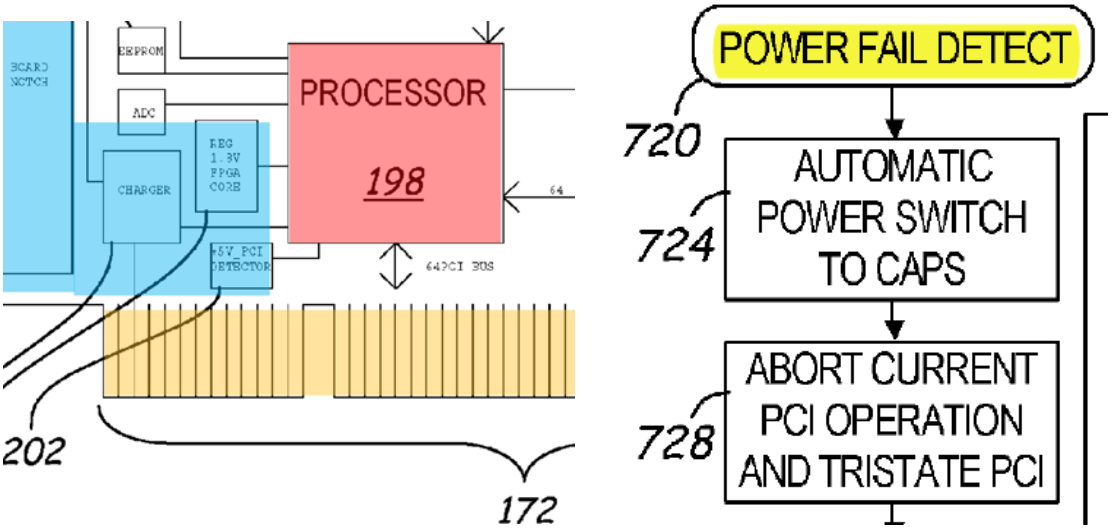
Grounds 4A-4B teach "*wherein the memory module transitions from a first operable state* [e.g., normal operation with the PCI +5V power] *to a second operable state* [e.g., backup operations with capacitor power and the PCI bus disconnected] *in response to the trigger signal*" for the same reasons discussed for [4.c] above (pp.99-102). EX1003, ¶¶759-762.

8. <u>Claim 8</u>

a) [8.a] Preamble and [8.b] A Controller, Including a Voltage Monitor Circuit, Coupled to the PCB

Claim 8 is similar to claims 4 to 6 above (pp.95-108). Thus, Grounds 4A-4B teach "*claim 1, further comprising a controller* [see [5.b], e.g., including logic in <u>Spiers</u>'s processor 198 (red, below)] *coupled to the PCB* [see [1.b], e.g., the PCI

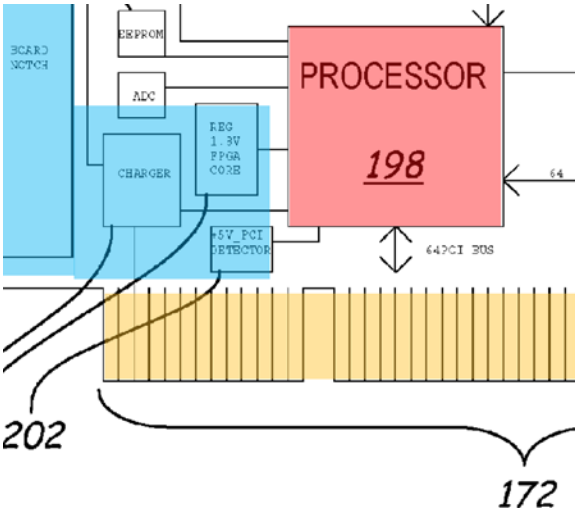
card], *the controller including a voltage monitor circuit* [see [4.b], e.g., Spiers's +5V PCI detector 202] *configured to monitor an input voltage received from a second set of edge connections of the plurality of edge connections* [e.g., for power failures, see [4.b] (pp.95-99) and [6.b] (pp.106-108)]." EX1003, ¶¶774-782; EX1025, ¶¶[0034, 36-37, 54-56], Figs. 5, 14 (reproduced below in part, annotated).



b) [8.c] Wherein the Voltage Monitor Circuit Transmits a Signal to Portion(s) of the Controller

Grounds 4A-4B teach "*wherein, in response to the voltage monitor circuit detecting a power threshold condition* [e.g., the "*input voltage*" is either too low, see [4.b] (pp.95-99), or too high, see [6.b] (pp.106-108)], *the voltage monitor circuit transmits a signal to one or more portions of the controller* [e.g., Spiers's detector 202 transmits a signal to logic in processor 198 when a power failure is detected, see [4.b] (pp.95-99) and [6.b] (pp.106-108)]." EX1003, ¶¶783-786;

EX1025, ¶[0054], Figs. 5 (reproduced below in part, annotated, showing the connection between the +5V PCI detector 202 and processor 198), 14.



9. Claims 7, 9, 11, 13, 16-17

Grounds 4A-4B teach claims 7, 9, 11, 13, and 16-17 for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[7.a]	[6.a]	¶¶764-766 (¶¶746-748)
[7.b]	[5.b]	¶¶767-770 (¶¶734-738)
[7.c]	[5.c]	¶¶771-773 (¶¶739-744)
[9.a]	[6.b]	¶¶788-792 (¶¶749-758)

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[9.b]	[6.b][9]	¶¶793-796 (¶¶749-758)
[11.a]	[4.b]	¶¶809-812 (¶¶709-723)
[11.b]	[4.b][10]	¶¶813-816 (¶¶709-723)
[11.c]	[4.c]	¶¶817-820 (¶¶724-730)
[13]	[4.b]	¶¶826-830 (¶¶709-723)
[16.a]	[1.a]	¶¶848-851 (¶¶595-599)
[16.b]	[1.b]	¶¶852-855 (¶¶601-608)
[16.c]	[1.c]	¶¶856-858 (¶¶609-660)
[16.d.1]	[1.d.1]	¶¶859-861 (¶¶661-664)
[16.d.2]	[1.d.2]	¶¶862-864 (¶¶665-668)
[16.d.3]	[1.d.5]	¶¶865-867 (¶¶684-687)

[9] Spiers discloses a +5V PCI detector 202 as discussed above (pp.79-81), and thus a POSITA would have understood that +5V represents a "*specified operating voltage*" for the input voltage used by the backup device 144. EX1003, ¶795; EX1025, ¶[0037], Figs.5, 14.

[10] See note 9 directly above.

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[16.e.1]	[8.b], [1.b], [9.a][11]	¶¶868-871 (¶¶778-782, 601-608, 788-792)
[16.e.2]	[4.c]	¶¶872-874 (¶¶724-730)
[17]	[4.b], [6.b]	¶¶875-878 (¶¶709-723, 749-758)

10. Claim 10

Grounds 4A-4B teach "*claim 9, wherein the first predetermined threshold voltage is ten percent above the specified operating voltage* [e.g., +5V, EX1025, ¶[0037]]." EX1003, ¶¶797-807.

The claimed threshold of "*ten percent*" is within the range of thresholds disclosed in the prior art, and thus "*ten percent*" is obvious under Federal Circuit precedent discussed above (p.27). In particular, thresholds around 10% for undervoltage and/or overvoltage were common in commercially available products, including specifically for PCI products like Spiers:

[11] Spiers's +5V PCI detector 202 (part of the "*voltage monitor circuit*") is "*configured to detect an amplitude change in the input voltage,*" for example, when the input voltage changes by crossing the reference voltage. EX1003, ¶871.

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DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 μF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
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V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1061, p.15 (programmable under- and over-voltage protection over a range, including 10%); EX1023, ¶[0013] ("+/- 15%"); EX1027, p.32 (VDDSPD is 3.3V +/-10%); EX1024 (Amidi), 8:23-36, Fig. 14 (below, showing 10% threshold).

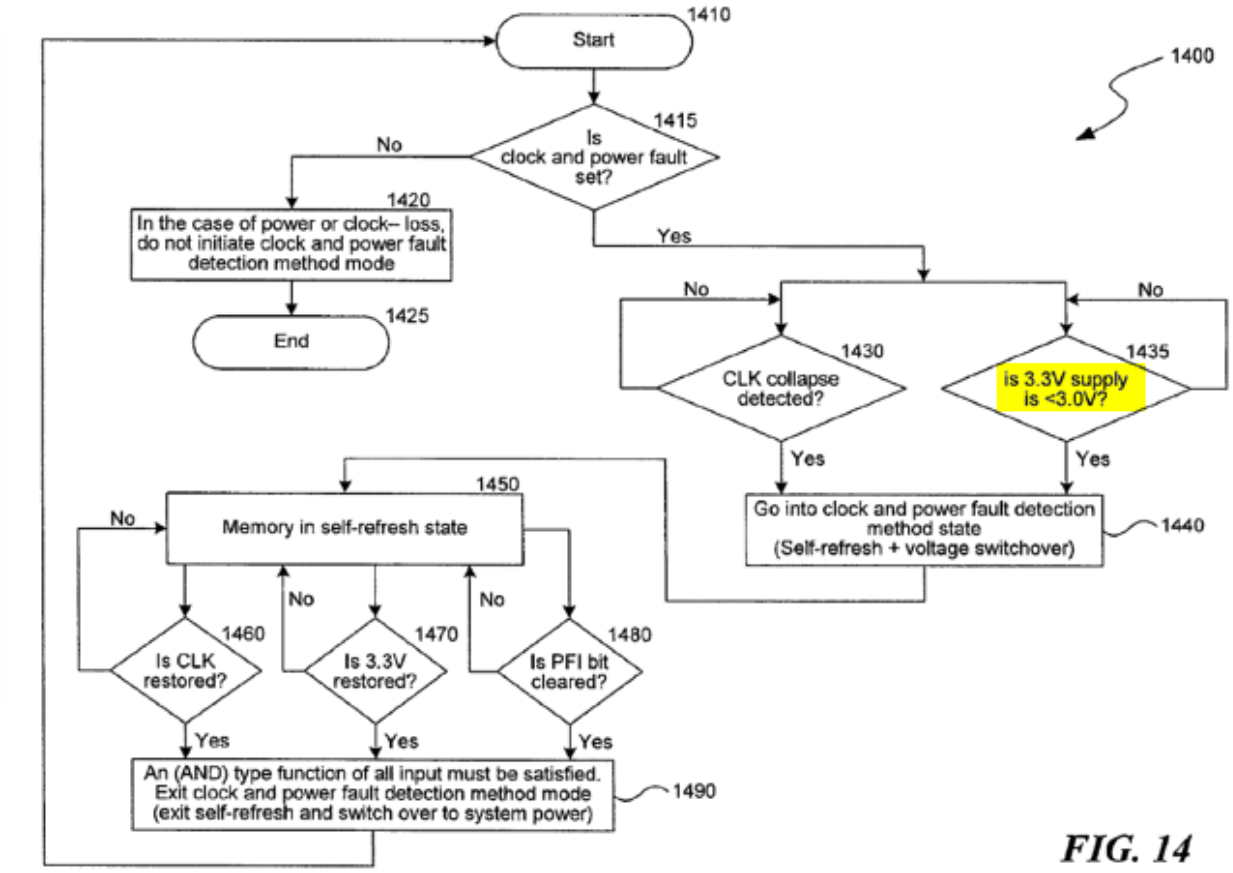


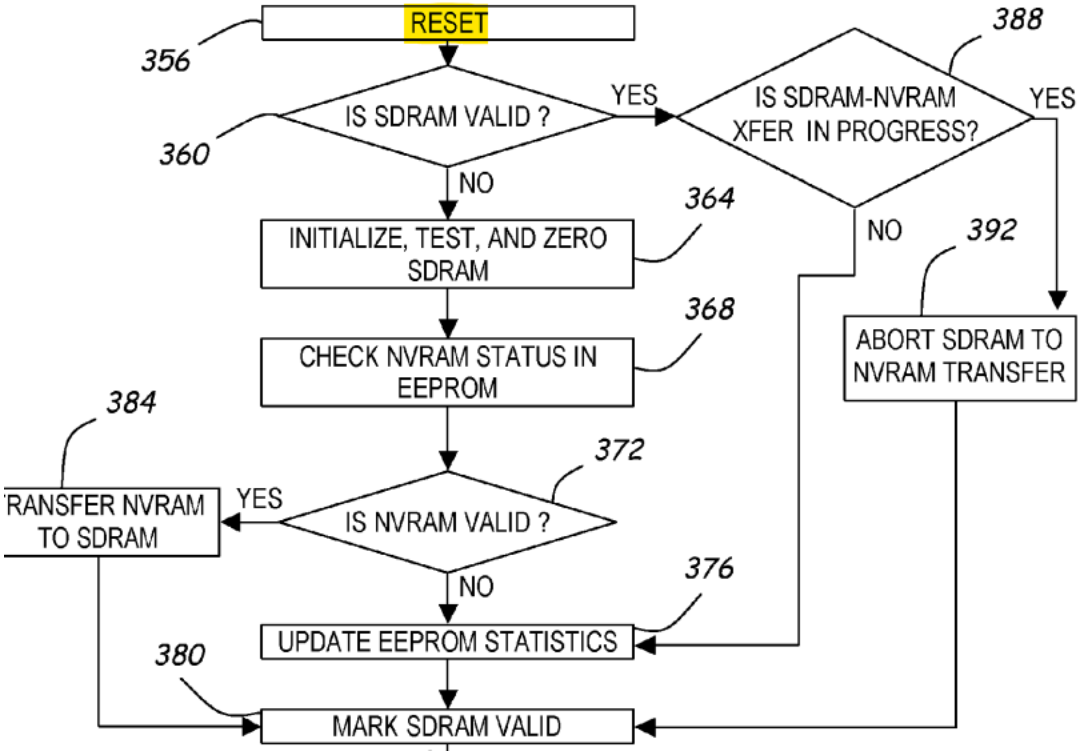
FIG. 14

11. Claim 12

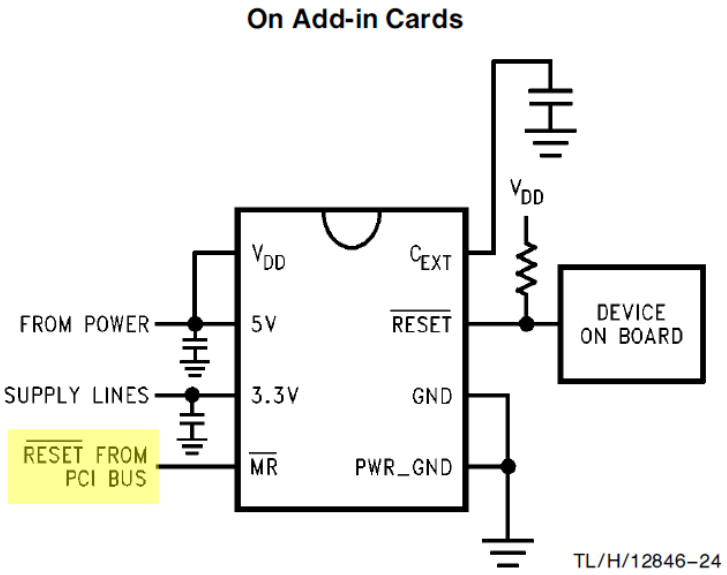
For the same reasons discussed directly above for claim 10, Grounds 4A-4B teach "*claim 11, wherein the second predetermined threshold voltage is ten percent below the specified operating voltage*." EX1003, ¶¶821-825.

12. Claim 14

Grounds 4A-4B teach "*claim 8, wherein the voltage monitor circuit detecting a power threshold condition includes the voltage monitor circuit detecting a request by the host system* [e.g., a reset host request]." EX1003, ¶¶831-838; EX1025, Fig.8 (reproduced below in part).



As shown above, Spiers teaches detecting a reset request by the host system when transferring data from volatile (e.g., SDRAM) to non-volatile (e.g., NAND flash) memory in response to a power failure. EX1025, Abstract, ¶[0043], Fig. 8. A POSITA would have understood from this disclosure that the host would request a reset of Spiers's detector, which in light of the PCI standard would have included a reset functionality like the one shown below, to properly reset parts of the module and ensure proper operation. EX1003, ¶¶836-837; EX1063, 1 (reproduced below in part, showing RESET from PCI Bus); *see also* EX1031, p.133 (PCI standard requiring, "The system must assert RST# [Reset] … in the event of a power failure.").

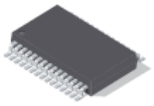


13. Claim 15

Grounds 4A-4B teach "*claim 1*, *wherein two of the at least three* [e.g., for V_{DD}/V_{DDQ} ("*first*"), V_{CCFPGA} ("*second*"), and V_{TT} ("*third*") (pp.72-77, 82)] *buck converters are configured to operate as a dual-buck converter* [for at least the same reasons discussed above (pp.35-40), e.g., to use fewer integrated circuits, pins, and interconnections on the module, consistent with commercially available dual buck converters such as EX1040, p.1 (below) and EX1041, pp.1-2 (below), 9 (showing two converters with different phases can reduce ripples), and to have V_{TT} follow the fluctuations of V_{DD}/V_{DDQ}, EX1040 p.11]." EX1003, ¶¶839-846.

TEXAS INSTRUMENTS

TPS51020



SLUS564B – JULY 2003 – REVISED DECEMBER 2003

DUAL, VOLTAGE MODE, DDR SELECTABLE, SYNCHRONOUS, STEP-DOWN CONTROLLER FOR NOTEBOOK SYSTEM POWER

APPLICATIONS

- Notebook Computers System Bus and I/O
- DDR I or DDR II Termination

FAIRCHILD SEMICONDUCTOR®

October 2005

FAN5026
Dual DDR/Dual-Output PWM Controller

Applications

- DDR V_{DDQ} and V_{TT} voltage generation

Circuit Description

Overview

The FAN5026 is a multi-mode, dual channel PWM controller intended for graphic chipset, SDRAM, DDR DRAM or other low output voltage power applications in PC's, VGA Cards and set top boxes. The IC integrates a control circuitry for two synchronous buck converters. The output voltage of each controller can be set in the range of 0.9V to 5.5V by an external resistor divider.

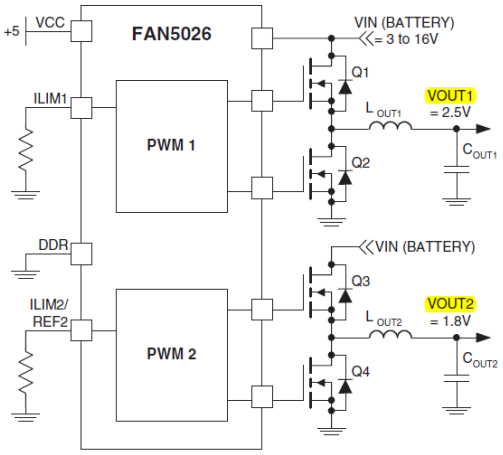


Figure 1. Dual Output Regulator

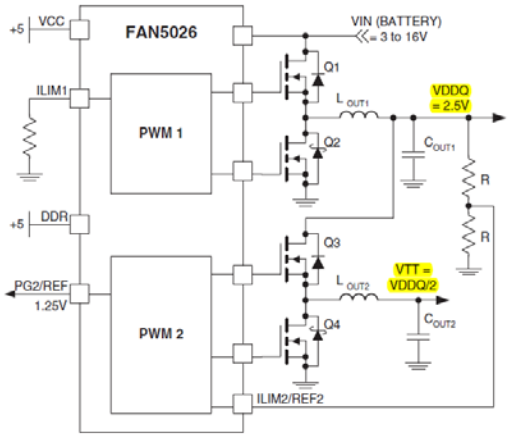


Figure 2. Typical Application

14. Claim 18

a) [18.a] Using First Pre-Regulated Voltage

Grounds 4A-4B teach "*claim 16, wherein, in the first operable state* [e.g., operation with the PCI +5V power, see [4.c] (pp.99-102)], *the voltage conversion circuit provides the first regulated voltage* [e.g., V_{DD}/V_{DDQ} =1.5V or 1.8V (see pp.82, 72-77)] *to the plurality of SDRAM devices* [see [1.d.2] (p.90)] *using a first pre-regulated voltage* [below]." EX1003, ¶¶879-890.

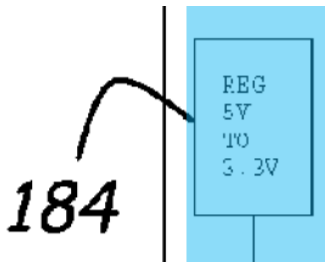
To the extent a "*pre-regulated voltage*" can be satisfied by the "*input voltage*" of [16.e.2] being within pre-determined limits, as suggested by Netlist, EX1073, pp.49-50, Spiers teaches that because the external supply voltage (e.g., PCI +5V) would be within a +/-5% tolerance according to the PCI standard. EX1003, ¶884; EX1025, ¶[0037]; EX1031, p.117 (allowing +/-0.25 V tolerance, below in part).

Table 4-1 summarizes the DC specifications for 5V signaling.

Table 4-1: DC Specifications for 5V Signaling

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{CC}	Supply Voltage		4.75	5.25	V	

To the extent the "*pre-regulated voltage*" must be a voltage pre-regulated on the memory board itself, EX1001, 28:53-58, it would have been obvious to a POSITA to convert the +5V PCI input voltage into a 3.3V "pre-regulated" voltage, in light of the teaching of Spiers. EX1003, ¶¶886-888. Spiers teaches that voltage regulator 184 converts the 5V voltage from the capacitors into a 3.3V regulated voltage:

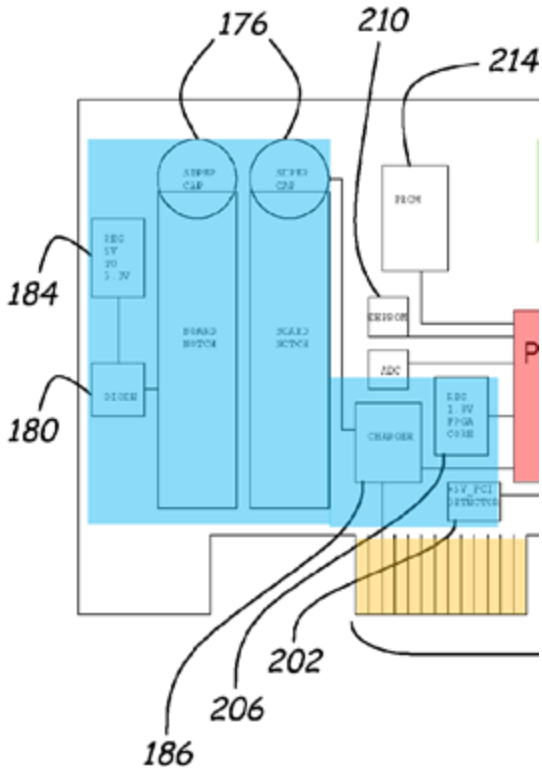


EX1025, ¶[0037], Fig.5; EX1003, ¶887. A POSITA would have been motivated, for similar reasons, to convert the +5V PCI input voltage into a 3.3V regulated voltage, so that the buck converters in Spiers always receive a pre-regulated voltage of 3.3V both during normal operation and when powered from the capacitors, thus avoiding large transients when changing from +5V PCI power to the capacitors. EX1003, ¶888. Such a 5V to 3.3V pre-regulator would also ensure the input to Spiers's voltage converters remains within a tolerated interval, even if

the external supply voltage becomes "unregulated," EX1023, ¶[0014], and would also allow Spiers's module to work with systems with an input voltage other than 5V without replacing other parts of the module, *id.*, ¶[0020]. A POSITA would understand that converting a 5V voltage to a 3.3V voltage results in the 3.3V voltage being regulated. EX1032, p.161 (explaining that switch-mode converters, including buck converters and boost converters, "convert the ***unregulated*** dc input into a ***controlled*** dc output at a desired voltage level"); EX1003, ¶888.

b) [18.b] Using Second Pre-Regulated Voltage

Grounds 4A-4B teach "*wherein, in the second operable state* [e.g., backup operations with capacitor power, see [4.c] (pp.99-102)], *the voltage conversion circuit provides the first regulated voltage* [from [18.a]] *to the plurality of SDRAM devices* [from [18.a]] *using a second pre-regulated voltage* [e.g., 3.3V, converted from the 5V capacitor voltage by "voltage ***regulator*** 184" (below)]." EX1003, ¶¶891-895; EX1025, ¶[0037] (describing the arrangement of capacitors 176, voltage regulator 184, and charger 186 in the power supply, and their function in case of power failure), Fig.5 (below in part).



15. Claim 19

Grounds 4A-4B teach "*claim 18, wherein, in the first operable state* [from [18.a], e.g., when using the PCI +5V power], *the first pre-regulated voltage* [from [18.a]] *is supplied to the voltage conversion circuit* [see [1.c] (p.81)] *via a circuit* [e.g., the power switch multiplexer "*circuit*" shown in Amidi's Figure 7, below, where "System_VDD" (710) from the upper left—which in the combination of Ground 4 is pre-regulated at 3.3V as discussed for [18.a]—is supplied to the "*voltage conversion circuit*" to the right], *and wherein, in the second operable state* [from [18.b], e.g., when using capacitor power], *the second pre-regulated voltage* [from [18.b]] *is supplied to the voltage conversion circuit via the circuit*

[e.g., where "DC_18V" (720) from the lower left—which in the combination of Ground 4 is pre-regulated at 3.3V as discussed for [18.b]—is supplied to the "*voltage conversion circuit*" to the right]." EX1003, ¶¶896-908; EX1024, 4:23-29, 4:56-5:24, Fig.5-6 (showing details in Power management block), 7 (below).

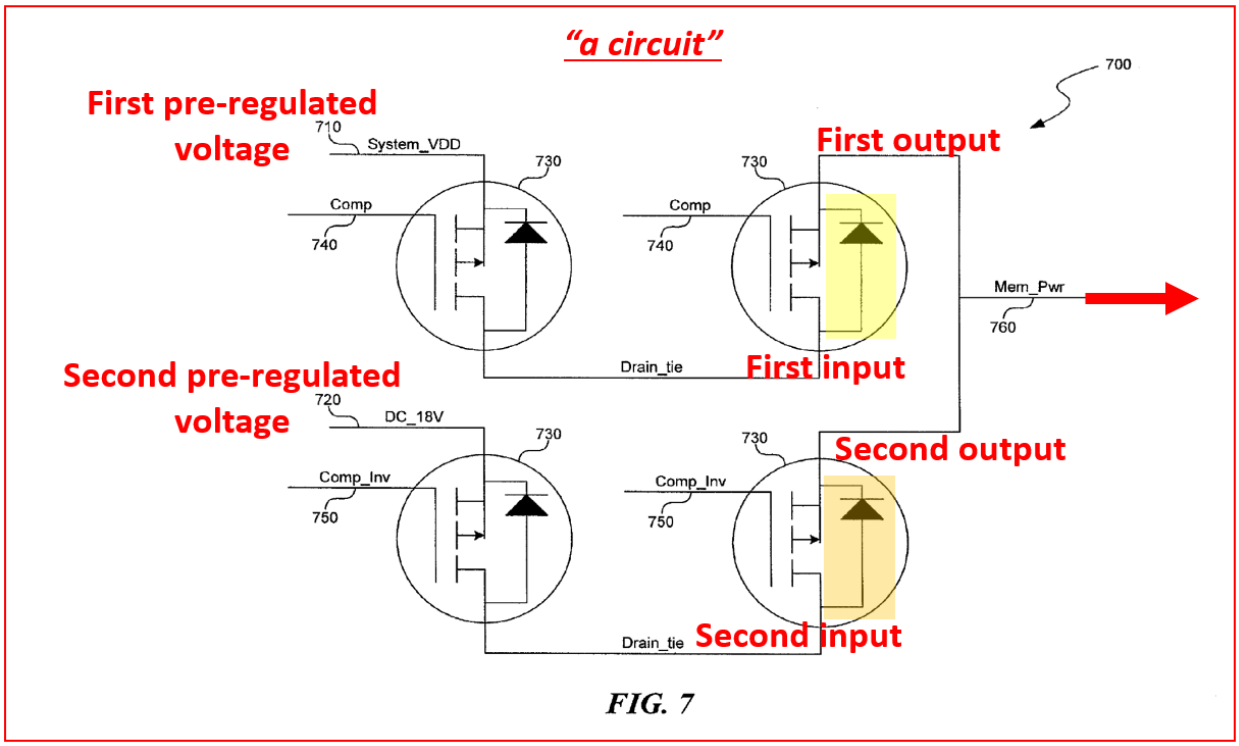


FIG. 7

Spiers discloses that upon detecting "a power failure," power is switched from the external power supply "to the capacitors." EX1025, ¶[0054], Fig.14. In the combination of Ground 4, Amidi's "power switch multiplexer" shown in Figure 7 (above) provides the details for implementing such a power switch, and a POSITA would have been motivated to use the structure of Amidi's Figure 7 (above) to reduce parasitic currents thus saving power. EX1003, ¶¶901-902; EX1024, 4:56-5:24, Fig.7.

16. Claim 20

Grounds 4A-4B teach "*claim 19, wherein the circuit* [from [19.a], e.g., the power switch multiplexer in Amidi's Figure 7, above] *includes a first diode* [yellow, above, EX1024, 5:3] *having a first input and a first output, the first input is coupled to the first pre-regulated voltage* [from [18.a] and [19.a], upper left] *and the first output* [e.g., "Mem_Pwr" output (760), above] *is coupled to the voltage conversion circuit* [to the right of the red arrow above], *and wherein the circuit includes a second diode* [orange, above, EX1024, 5:17] *having a second input and a second output, the second input is coupled to the second pre-regulated voltage* [from [18.b] and [19.b], lower left] *and the second output is coupled to the first output* [e.g., "Mem_Pwr" output (760), above] *and to the voltage conversion circuit* [to the right of the red arrow above]." EX1003, ¶¶910-917; EX1024, 4:64-5:24, Fig.7.

17. Claim 21-30

Ground 4A-4B teach claims 21-30 for at least the same reasons discussed above, because these claims have limitations substantially identical to earlier limitations, as shown in the following table:

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.a]	[16.a]	¶¶919-921 (¶¶848-851)

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[21.b]	[20.a]-[20.b]	¶¶922-925 (¶¶910-917)
[21.c]	[18.a]-[18.b]	¶¶926-929 (¶¶880-895)
[21.d]	[19.a]	¶¶930-933 (¶¶897-903)
[21.e]	[19.b]	¶¶934-937 (¶¶904-908)
[22]	[20.a]-[20.b]	¶¶938-942 (¶¶910-917)
[23.a]	[4.b], [6.b][12]	¶¶944-947 (¶¶709-723, 749-758)
[23.b]	[5.c]	¶¶948-951 (¶¶739-744)
[24.a]	[1.a]	¶¶953-956 (¶¶595-600)
[24.b]	[1.b]	¶¶957-960 (¶¶601-608)
[24.c]	[1.c]	¶¶961-964 (¶¶609-660)
[24.d.1]	[1.d.1]	¶¶965-968 (¶¶661-664)
[24.d.2]	[1.d.2]	¶¶969-972 (¶¶665-668)
[24.d.3]	[1.d.5]	¶¶973-976 (¶¶684-687)
[24.e.1]	[16.e.1][13]	¶¶977-980 (¶¶868-871)

[12] See note 11 on p.112.

[13] Because the PCB has the claimed "*interface*" as shown above (pp.79-81), receiving an input voltage "from the host system ***via the interface***" for [16.e.1]

This limitation…	…is substantially similar to this limitation…	…and thus obvious for at least the same reasons above and as discussed in EX1003:
[24.e.2]	[23.a], [23.b]	¶¶981-984 (¶¶944-951)
[24.e.3]	[23.b]	¶¶985-988 (¶¶948-951)
[25]	[16.e.2]	¶¶989-993 (¶¶872-874)
[26.a]	[18.a]	¶¶995-998 (¶¶880-890)
[26.b]	[18.b]	¶¶999-1002 (¶¶891-895)
[27]	[20.a]	¶¶1003-1007 (¶¶910-913)
[28]	[20.b]	¶¶1008-1012 (¶¶914-917)
[29]	[17]	¶¶1013-1017 (¶¶875-878)
[30]	[9.b], [11.b]	¶¶1018-1022 (¶¶793-796, 813-816)

E. Ground 5

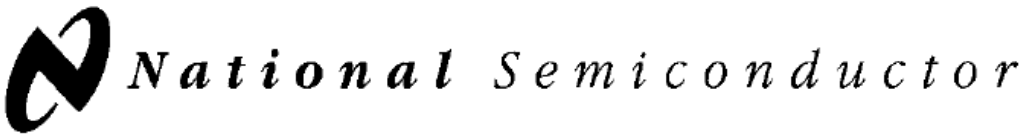
1. Ground 5 combination: Ground 4 + Hajeck (EX1038)

Ground 5 combines Ground 4 with the teachings of Hajeck, which discloses a "voltage detection circuit 48" for detecting both undervoltage and overvoltage anomalies in memory subsystems. EX1038, 3:30-40; EX1003, ¶¶211-212. Hajeck is analogous art to Spiers and Amidi in Ground 4 as all relate to memory modules in general and protecting against power disruptions in particular. EX1003, ¶209.

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also discloses receiving the input voltage "from the host system ***via the interface of the PCB***" for [24.e.1]. EX1003, ¶980.

A POSITA would have been motivated to combine Ground 4 with Hajeck, and had a reasonable expectation of success in doing so, because Spiers discloses a +5V PCI detector 202 to detect voltage anomalies and to switch to backup power, EX1025, ¶¶[0002, 37, 54], similar to Amidi, EX1024, 4:44-52, 5:25-43, 8:23-29, 9:8-12, Figs.5-6, 14-15, and Hajeck teaches the importance of detecting both undervoltage and overvoltage conditions to avoid data loss, EX1038, 1:10-31, 3:30-40, 4:62-65, consistent with voltage detection circuits for PCI cards (like Spiers) that were readily available at the time:



LMC6953
PCI Local Bus Power Supervisor

DC Electrical Characteristics

Unless otherwise specified, all **boldface** limits guaranteed for T_J = 0°C to 70°C, V_{DD} = 5V, $R_{PULL-UP}$ = 4.7 kΩ and C_{EXT} = 0.01 µF. Typical numbers are room temperature (25°C) performance.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{H5}	V_{DD} Over-Voltage Threshold	(Note 4)	**5.45**	5.6	**5.75**	V
V_{L5}	V_{DD} Under-Voltage Threshold	(Note 4)	**4.25**	4.4	**4.55**	V
$V_{H3.3}$	3.3V Over-Voltage Threshold	(Note 5)	**3.8**	3.95	**4.1**	V
$V_{L3.3}$	3.3V Under-Voltage Threshold	(Note 5)	**2.5**	2.65	**2.8**	V

EX1063, pp.1-2; *see also* EX1065, Abstract, ¶¶[0014, 18-19], Figs.1, 5; EX1061, p.15; EX1062, p.15.

The teachings of Hajeck do not affect any of the voltage mappings in Ground 4, and thus the voltage mappings for Grounds 5A-5B are the same as those for Grounds 4A-4B above (pp.82, 72-77).

2. Claims 1-30

Ground 5 renders obvious claims 1-30 for at least the same reasons provided above for Ground 4 (pp.77-125). To the extent one were to argue that Ground 4 fails to teach overvoltage detection as required by [6.b] ("*the input voltage having a voltage amplitude above a predetermined threshold voltage*") and as discussed above (pp.106-108) — and required by claims 7, 9-12, 17, and 29-30 — such overvoltage detection was obvious in light of Hajeck in the combination of Ground 5 discussed above (pp.125-127). EX1003, ¶¶756-758. In particular, in the combination of Ground 5, Spiers's "+5V PCI detector 202" would be implemented to detect voltage anomalies and switch to the backup power not only for undervoltage conditions as taught by Spiers and Amidi, EX1025, ¶¶[0002, 36-37], Fig.14; EX1024, 4:44-53, but also "when the voltage exceeds a certain level" as taught by Hajeck, EX1038, 3:30-43; *see also id.* Abstract, 1:10-18, 1:28-31, 1:62-2:7, 3:30-4:9, 4:62-65, FIG. 1. Thus, Ground 5 further teaches both overvoltage and undervoltage detection and protection, further rendering obvious claims 6, 9, 17, 29 and their dependents (7, 10-12, and 30). EX1003, ¶¶756-757, 791, 877, 1016.

VII. *FINTIV*

The *Fintiv* factors favor institution. There are two cases currently pending between the parties that involve (or could involve) the 054 Patent: a declaratory judgment action filed by Petitioner (EX1068-69), and an infringement action filed by Netlist (EX1073). Both of these cases are in their infancy: Netlist recently moved to dismiss Petitioner's action, EX1070, and Netlist recently served an amended complaint in its action, EX1073. There currently is no trial date in either case, nor have any discovery requests been served. This petition was filed quickly, less than one month after Petitioner was served with Netlist's amended complaint asserting the 054 Patent. *Id.* Thus the *Fintiv* factors favor institution.

VIII. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-30 be canceled as unpatentable.

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CERTIFICATE OF COMPLIANCE

I hereby certify that this petition complies with the type-volume limitations of 37 C.F.R. § 42.24 because it contains 13,803 words (as determined by the Microsoft Word word-processing system used to prepare the petition), excluding the parts of the petition exempted by 37 C.F.R. § 42.24.

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CERTIFICATE OF SERVICE

I hereby certify that on this 17th day of May, 2022, a copy of this Petition, including all exhibits, has been served in its entirety by FedEx Express on the following counsel of record for Patent Owner:

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