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Paper 29
Entered: June 27, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and
SK HYNIX MEMORY SOLUTIONS INC.,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2018-00362[1]
Patent 9,606,907 B2

Before BRYAN F. MOORE, JON M. JURGOVAN, and KAMRAN JIVANI, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge.*

FINAL WRITTEN DECISION
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

[1] IPR2018-00363 has been consolidated with the instant proceeding.

I. INTRODUCTION

On December 22, 2017, SK Hynix Inc., SK Hynix America Inc., and SK Hynix Memory Solutions Inc. ("Petitioner") sought *inter partes* review of claims 1–29 and 58–65 of U.S. Patent No. 9,606,907 B2 (Ex. 1001, the "'907 patent") owned by NETLIST, INC. ("Patent Owner"). IPR2018-00362 ("362 IPR"), Paper 1 ("362 Petition" or "362 Pet."). On the same date, Petitioner also sought *inter partes* review of claims 30–57 of the '907 patent. IPR2018-00363 ("363 IPR"), Paper 1 ("363 Petition" or "363 Pet."). Patent Owner filed Preliminary Responses on April 10, 2018. 362 IPR, Paper 6; 363 IPR, Paper 6. We consolidated the proceedings pursuant to 35 U.S.C. § 315(d) under IPR2018-00362, and instituted trial of claims 1–65 of the '907 patent ("the Challenged Claims") on all grounds under 37 C.F.R. § 42.108. 362 Pet., Paper 7.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that, except for claims 40 and 41, the Challenged Claims are unpatentable.

II. BACKGROUND

A. Procedural History

During the trial, Patent Owner filed a Patent Owner Response (Paper 14, "PO Resp."), and Petitioner filed a Reply thereto (Paper 18, "Reply"). Thereafter, Petitioner filed a Corrected Petitioner's Reply. (362 IPR, Paper 23, "Corr. Reply"). By Order of March 1, 2019 (362 IPR, Paper 24), we

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granted Patent Owner authorization to file a Sur-Reply to the Corrected Petitioner's Reply (362 IPR, Paper 26), which was filed on March 8, 2019.

Petitioner and Patent Owner filed requests for Oral Argument (362 IPR, Papers 19 and 20), and we held the hearing on March 26, 2019 in the Dallas Regional Office. At the hearing, the parties were represented by counsel of record. Tr. 4–5. Patent Owner objected to certain slides of Petitioner's demonstratives because they allegedly presented a different visual impression than the Petitions. Tr. 5–13. As demonstratives are not part of the evidentiary record, and the same substance presented in the briefings with different appearance in the slides would not affect our findings in this proceeding, we declined to strike Patent Owner's slides. Tr. 11–13. Thereafter, we heard the parties' arguments, allowing use of their demonstratives. Tr. 13–93.

Patent Owner filed Objections to Petition Evidence (362 IPR, Paper 9), Objections to Reply Evidence (362 IPR, Paper 21), and a Motion to Exclude (362 IPR, Paper 22). Petitioner filed an Opposition to Patent Owner's Motion to Exclude (362 IPR, Paper 25) in response to which Patent Owner filed a Reply to Petitioner's Opposition to Motion to Exclude (362 IPR, Paper 27).

B. Related Proceedings

Patent Owner asserted the '907 patent against Petitioner in *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) and *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:17-cv-01030 (C.D. Cal. filed June 14, 2017). 362 Pet. (iv).

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The ’907 patent is a continuation of U.S. Patent 8,516,185 B2 (“the ’185 patent”). The ’185 patent is involved in the following proceedings: *SanDisk Corp. v. Netlist, Inc.*, Case No. IPR2014-01029 (institution denied); *SMART Modular v. Netlist, Inc.*, Case No. IPR2014-01369 (institution denied); *SK hynix, Inc. v. Netlist, Inc.*, Case No. IPR2017-00577 (instituted July 7, 2017 as to claims 1–3, 7, 8, and 10–12 of the ’185 patent as obvious under 35 U.S.C. § 103 over Halbert and Amidi); *In the matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016); and *Netlist, Inc. v. SK hynix Inc., SK hynix America Inc., and SK hynix memory solutions Inc.*, Case No. 8:16-cv-01605 (C.D. Cal. filed Aug. 31, 2016). 362 Pet. (iv).

The ’907 patent also is involved in IPR2018-00364 (against claims 1–29 and 58–65 under 35 U.S.C. § 103 based primarily on Halbert); and IPR2018-00365 (against claims 30–57 under 35 U.S.C. § 103 based primarily on Halbert). 362 Pet. (v).

C. The ’907 Patent

The ’907 patent is directed to memory module 402, as shown in Fig. 3A below. Ex. 1001, 8:49–52.[2] Memory module 402 comprises memory devices 412 (*id.* at 9:18–20), data transmission circuits 416 (*id.* at 10:62–65), and module control circuit 430 (*id.* at 10:8–12). These components are mounted on printed circuit board (PCB) 410, as shown in Fig. 3A below. *Id.* at 8:7–14, 10:45–49.

[2] The exhibits filed in the 362 IPR appear to be identical to the exhibits filed in the 363 IPR. We, therefore, refer only to the exhibit number.

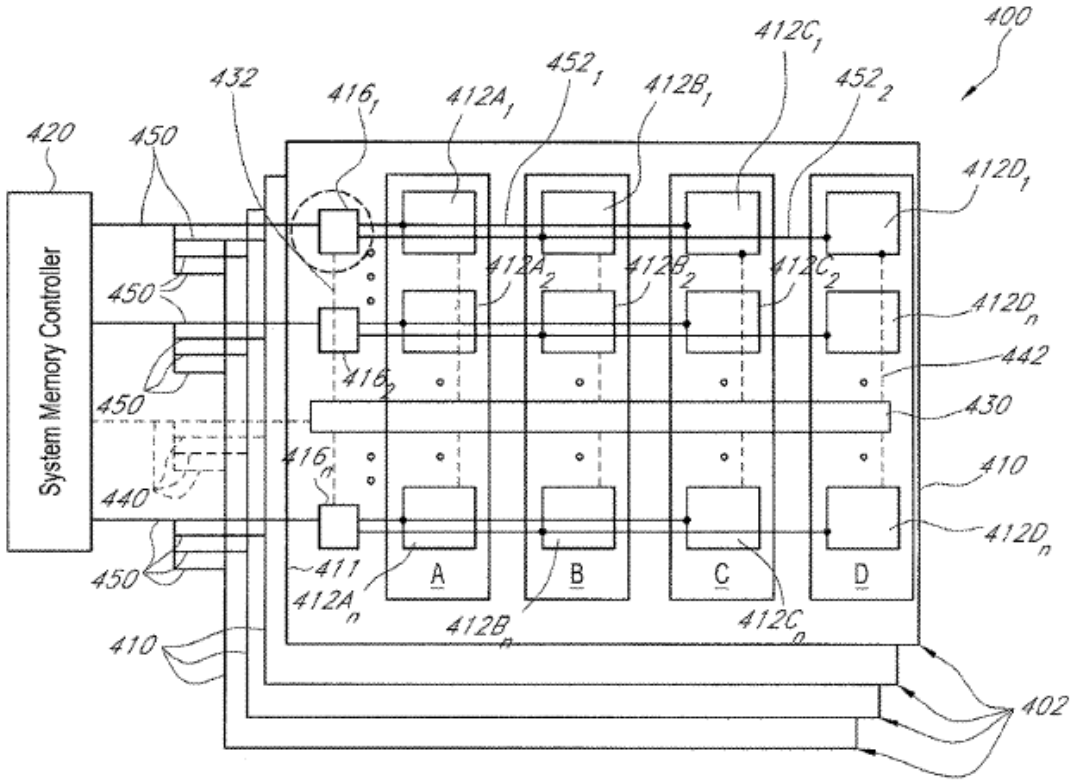


FIG. 3A

Fig. 3A depicts a schematic representation of an example memory subsystem.

Figure 3A of the ’907 patent shows memory subsystem 400, including memory modules 402 comprising memory devices 412, data transmission circuits 416, and module control circuits 430. Ex. 1001, Fig. 3A. Memory modules 402 are connected to system memory controller 420 via address and control lines 440 and data lines 450. *Id.* at 7:46–53.

Module control circuit 430 is connected to receive address and control signals from system memory controller 420 via control lines 440. *Id.* at 8:14–17, 10:24–29. In response to these signals, module control circuit 430 generates module control signals to address and control memory devices 412 on control lines 442. *Id.* at 8:14–17, 10:8–12. In addition, module control

circuit 430 generates module control signals for data transmission circuits 416 on control lines 432. *Id.* at 10:34–37. In response to these module control signals, memory devices 412 and data transmission circuits 416 output data to, or receive data from, system memory controller 420 via data lines 450, 452. *Id.* at 8:32–38.

Data transmission circuits 416 operate to reduce the load experienced by system memory controller 420 to speed performance of a read or write operation involving memory module 402. *Id.* at 10:55–62. Data transmission circuits 416 accomplish this by connecting the selected memory device 412 to memory controller 420 while isolating other memory devices. *Id.* at 11:27–54, 14:50–62. Specifically, data transmission circuits 416 comprise tri-state buffers to selectively connect memory devices 412 to data lines while isolating others. *Id.* at 13:22–23, 16:4–16.

D. Illustrative Claim

Of the challenged claims, claims 1, 16, 30, 43, 53, and 58 are independent. Claim 1 is illustrative:

> 1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=Mxn, comprising:
>
> a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;
>
> a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in

response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding

> to the respective one or more of the first memory devices and the respective one or more of the second memory devices.

Ex. 1001, 19:2–58.

E. Prior Art Relied Upon

Petitioner relies upon the following prior art references:

Ellsberry	US 2006/0277355 A1	Dec. 7, 2006	Ex. 1005[3]
Halbert	US 7,024,518 B2	Apr. 4, 2006	Ex. 1006[4]
Ruckerbauer	US 7,334,150 B2	Feb. 19, 2008	Ex. 1038[5]
JEDEC Standard No. 21–C, PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, Rev. 1.3., Jan. 2002.			Ex. 1010[6]
Stone, Harold S., Microcomputer Interfacing, Reading, MA; Addison Wesley, 1982			Ex. 1035[7]

[3] Ellsberry was published on December 7, 2006 and is thus prior art to the 907 patent under 35 U.S.C. §§ 102(a) and (b).
[4] Halbert issued as a patent on April 4, 2006 and is thus prior art to the 907 patent under 35 U.S.C. §§ 102(a) and (b).
[5] Ruckerbauer issued as a patent on February 19, 2008 and is thus prior art under 35 U.S.C. §§ 102(a) and (b).
[6] JEDEC Standard No. 21–C was published in January 2002 and is thus prior art to the 907 patent under 35 U.S.C. §§ 102(a) and (b).
[7] Stone published in 1982 and is thus prior art to the 907 patent under 35 U.S.C. §§ 102(a) and (b).

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F. Instituted Grounds of Unpatentability

Petitioner asserts the following grounds of unpatentability:

Case	Challenged Claim(s)	Basis	Reference(s)
362 IPR	1–29 and 58–65	§ 103(a)[8]	Ellsberry
	1–29 and 58–65	§ 103(a)	Ellsberry and JESD21-C
	7, 19 and 24	§ 103(a)	Ellsberry and Halbert
	9 and 28	§ 103(a)	Ellsberry and Ruckerbauer
	4, 17–23 and 60–65	§ 103(a)	Ellsberry and Stone
363 IPR	30–57	§ 103(a)	Ellsberry
	30–57	§ 103(a)	Ellsberry and JESD21-C
	36	§ 103(a)	Ellsberry and Ruckerbauer
	39–42 and 45–57	§ 103(a)	Ellsberry and Stone

G. Testimony

Petitioner supports its challenges with a declaration of Dr. Harold Stone, filed contemporaneously with the Petition. Ex. 1003. Dr. Stone testified further by deposition on October 5, 2018, and a transcript of his testimony has been entered into evidence. Ex. 2003.

[8] Because the claims at issue have an effective filing date prior to March 16, 2013, the effective date of the applicable provisions of the Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) ("AIA"), we apply the pre-AIA versions of 35 U.S.C. §§ 102 and 103 in this Decision.

Patent Owner rebuts Petitioner's challenges with a declaration of Dr. Jacob Baker, filed contemporaneously with the Patent Owner Response. Ex. 2002. Dr. Baker testified further by deposition on January 26, 2019, and a transcript has been entered into evidence. Ex. 1044.

III. ANALYSIS OF THE PETITIONER'S CHALLENGES

A. Principles of Law

Petitioner bears the burden of proving unpatentability of the challenged claims, and the burden of persuasion never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015). To prevail in its challenges to the Challenged Claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d).

A claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time of the invention to a person having ordinary skill in the art. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of non-obviousness, i.e., secondary considerations such as commercial success, long felt but unsolved needs, and failure of others. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). The obviousness inquiry further requires an analysis of "whether there was an apparent reason to combine the known

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elements in the fashion claimed by the patent at issue." *KSR*, 550 U.S. at 418 (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006) (requiring "articulated reasoning with some rational underpinning to support the legal conclusion of obviousness")).

B. The Level of Ordinary Skill in the Art

Petitioner's declarant states a person of ordinary skill in the art at the relevant time "would have an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years in the field." *See, e.g.*, 362 Pet. 4–5; Ex. 1003 ¶ 47. According to Petitioner's declarant, this person "would have been familiar with the JEDEC industry standards . . . and the design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with a memory controller of a computer system." *Id.* (citing Ex. 1041). Petitioner states this person would "have been familiar with the structure and operation of circuitry used to access and control computer memories, including sophisticated circuits such as ASICs [Application Specific Integrated Circuits] and CPLDs [Complex Programmable Logic Devices], and more low level circuits such as tri-state buffers." 362 Pet. 4–5; Ex. 1035. Patent Owner does not dispute this characterization of the level of ordinary skill in the art. *See generally* PO Resp.

In light of the complete trial record, we adopt Petitioner's articulation of the level of skill, above, and acknowledge that, commensurate with that articulation of the level of skill, the level of ordinary skill in the art is also reflected by the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350,

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1355 (Fed. Cir. 2001); *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978).

C. Claim Construction

Accordingly to the rules applicable to the present Petition, we interpret claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b) (2017)[9]; *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2144–46 (2016) (upholding the use of the broadest reasonable interpretation standard). Under the broadest reasonable interpretation standard, and absent any special definitions, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech. Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Any special definitions for claim terms or phrases must be set forth with reasonable clarity, deliberateness, and precision. *In re Paulsen*, 30 F.3d 1475, 1480 (Fed. Cir. 1994). In the absence of such a definition, limitations are not to be read from the specification into the claims. *See In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Petitioner initially proposed constructions for "isolate memory device load," "the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command," and "fork-in-

[9] A recent amendment to this rule does not apply here because the Petition was filed before November 13, 2018. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340 (Oct. 11, 2018) (amending 37 C.F.R. § 42.100(b) effective November 13, 2018).

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the-road" versus "straight-line." 362 Pet. 12–15. Patent Owner contends these constructions are unnecessary because the Petitions are deficient for reasons that do not turn on claim construction. PO Resp. 4–9. Petitioner contends it stands by its proposed constructions but agrees "there is no need for the Board to construe any claim terms, as none of Patent Owner's arguments turn on claim construction." Corr. Reply 4 n. 4.

We agree that the issues in this case do not turn on claim construction. Furthermore, the parties do not present any arguments related to claim construction at trial. *See* Corr. Reply 4 n. 4; PO Resp. 4–9. Accordingly, we did not construe any claim terms in reaching our decision. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc*., 200 F.3d 795, 803 (Fed. Cir. 1999) (explaining that only claim terms in controversy need to be construed, and only to the extent necessary to resolve the controversy); *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co*., 868 F.3d 1013, 1017 (Fed. Cir. 2017) (applying *Vivid Techs.* in the context of an *inter partes* review).

D. Challenge #1: Obviousness of Claims 1–65 Based on Ellsberry

Petitioner contends Ellsberry renders claims 1–65 unpatentable as obvious under 35 U.S.C. § 103(a). 362 Pet. 23–78; 363 Pet. 23–75. Ellsberry (Ex. 1005).

1. Ellsberry (Ex. 1005)

Ellsberry relates to "a device, system, and method for expanding the memory capacity of a memory module." Ex. 1005, Abstract. "A control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* "By selectively

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routing data to and from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry, shown below, "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." Ex. 1005 ¶ 28.

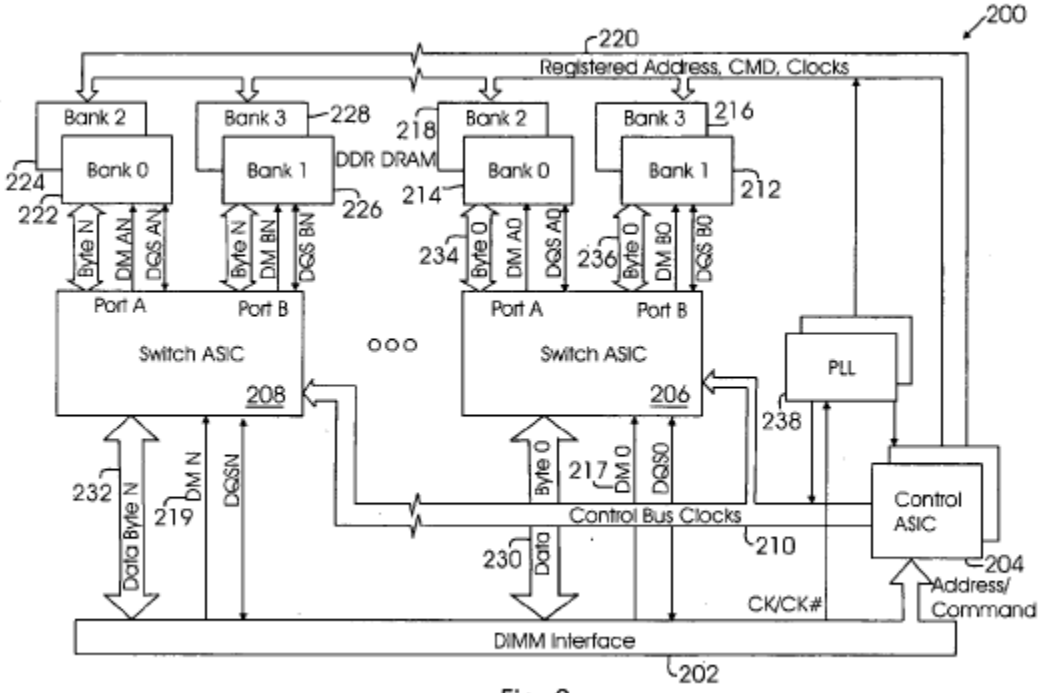


Fig. 2

Figure 2 illustrates a block diagram of a capacity-expanding memory device.

In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206, 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202

and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29.

Specifically, control unit 204 receives memory addresses and commands from DIMM interface 202 and controls switches 206 and 208 via control bus 210 to indicate how data from DIMM interface 202 should be received from and/or stored in memory banks 212–228. *Id.* ¶¶ 29–30, Fig. 2. The control unit 204 also generates address and command information on address bus 220 to access memory banks 212–228. *Id.* The switches 206 and 208 receive data from, or provide data to, the DIMM interface 202 via data buses 230 and 232. *Id.*

In one embodiment, switches 206, 208 each have two ports (Port A and Port B) connected to respective memory banks 212–228. *Id.* Control unit 204 determines which memory bank a received address corresponds to, and controls the appropriate switch by activating the port connected to the addressed memory bank and disabling the other port. *Id.* ¶¶ 30–31, 40. Thus, for example, "if the control unit 204 determines that a particular address is associated with, or mapped to, Bank 1212 coupled to memory bank switch 206, then it causes Port B to be activated and Port A to be disabled so that the data is written to the correct memory bank 212." *Id.* ¶ 31. Also,

> each memory bank switch 206 and 208 includes signal drivers to drive data signals to and from the memory banks and to and from the DIMM interface 202. This reduces resistive and/or capacitive loading of the data bus coupled to DIMM interface [202] and . . . bus 110 while emulating a standard device interface.

Id.

In another embodiment, control unit 204 enables both Port A and Port B at the same time, but sends an intended instruction to a selected memory bank of one port and a no-op (no operation) instruction to the memory bank(s) of the other port. *Id.* ¶ 41. In this way, data is read or written from only one memory bank at a time.

2. Mapping of Claim 1

Petitioner relies on Ellsberry to disclose all features of claim 1 with support from Dr. Stone's testimony. 362 Pet. 25–49 (citing Ex. 1003 ¶¶ 186–260, 271–279; Ex. 1005, Abstract, ¶¶ 2, 3, 10, 11, 26–33, 36, 40, 41, 45, 47; Figs. 1, 2, 5, 8A, 8B). Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of claim 1. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 1 as follows.

Referring to Ellsberry's Figure 2, Petitioner maps the claimed "memory module" to Ellsberry's capacity-expanding memory system 200, the claimed "module control circuit" to Ellsberry's control ASIC 204, the claimed "memory devices" to Ellsberry's memory banks 212–228, and the claimed "M buffer circuits" to buffers within Ellsberry's Switch ASICs 206, 208. *Id.* Petitioner further maps the claimed "first module control signals" to the signals on Ellsberry's bus 220, and the claimed "second module control signals" to signals on Ellsberry's bus 210. *Id.* Petitioner maps the "printed circuit board" to Ellsberry's Figure 5. Further details of Petitioner's mapping for claim 1 were provided in our decision to institute *inter partes* review. Paper 7. We provide the detailed mapping below, which Patent

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Owner does not dispute (*see generally* PO Resp.) and we adopt it as our own.

"A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:"

Petitioner contends Ellsberry discloses the stated claim limitation. 362 Pet. 24–27 (citing Ex. 1003 ¶¶ 186–196). Ellsberry discloses a processing unit 102 connected to memory module 106 through communication path 110. 362 Pet. 25; Ex. 1005 ¶ 27, Fig. 1. Thus, Ellsberry discloses the claimed "*memory module . . . configured to communicate with a memory controller*" (processing unit 102).

Petitioner contends Ellsberry describes DIMM interface 202 of memory module 200 "coupled to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." 362 Pet. 26; Ex. 1005 ¶ 28. We conclude that Ellsberry discloses the processing unit 102 and memory module 106/200 communicate "*via . . . control signal lines and . . . data lines*," as claimed.

Petitioner states that Ellsberry discloses "*M sets of data lines*" in the DIMM interface 202 having "two sets of data bits" on data buses 230, 232. 362 Pet. 27; Ex. 1005 ¶¶ 29, 30, Fig. 2; Ex. 1003 ¶ 195. "Each of the data buses 230 and 232 includes respective data lines to transmit an entire data byte (Data Byte 0; Data Byte N)," which is eight bits. 362 Pet. 27. We agree with Petitioner Ellsberry "discloses that each group of data bits is carried on a '*set of n data lines*' where '*n*' is eight." *Id.* Thus, on the full record before us, we are persuaded that Ellsberry discloses "*M sets of n data lines, where M is greater than one and N=Mxn*" as claimed. *Id.*

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"a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce first module control signals and second module control signals in response to the set of input address and control signals;"

Petitioner contends this limitation is disclosed by Ellsberry. 362 Pet. 27–33 (citing Ex. 1003 ¶¶ 197–211). According to Petitioner, the claimed *"module control circuit"* is taught by Ellsberry's control unit 204 of Figure 2. 362 Pet. 28; Ex. 1003 ¶ 198; Ex. 1005 ¶ 29, Fig. 2. "The control unit 204 receives memory addresses and commands over the DIMM interface 202." 362 Pet. 29; Ex. 1005, Abstract, ¶ 29; *see also id.* ¶¶ 36, 45, Fig. 2, Fig. 8A; Ex. 1003 ¶¶ 199–205. Ellsberry discloses the commands may be Read/Write commands. 362 Pet. 29–30; Ex. 1005 ¶ 10; *see also id.* ¶¶ 3, 11 Figs. 8A, 8B; Ex. 1003 ¶¶ 202, 203. On the full record before us, we are persuaded that Ellsberry discloses that its control unit 204 is "*configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines*."

Petitioner further relies upon Ellsberry's disclosure that "[t]he four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3) 212, 214, 216, and 218 are also communicatively coupled to an address bus 220 through which they receive address and command information from the control unit 204." 362 Pet. 35–36; Ex. 1005 ¶ 30. Ellsberry also discloses "[t]he control unit 204 is communicatively coupled to the dual memory bank switches 206 & 208 via a control bus 210 and indicates to the memory bank switches 206 & 208 how data from the DIMM interface 202 should be received and/or stored." Ex. 1005 ¶ 29. Thus, on the full record before us, we are persuaded

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that Ellsberry discloses *"to produce first module control signals and second module control signals in response to the set of input address and control signals"* as claimed.

"a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;"

Petitioner contends Ellsberry discloses this claim limitation. 362 Pet. 33–36 (citing Ex. 1003 ¶¶ 212–224). According to Petitioner, Ellsberry discloses its "memory module includes banks of *'memory devices',* such as DRAM and SDRAM devices, mounted on the circuit board of the memory module." *Id.* (emphasis added); Ex. 1005 ¶¶ 3, 26, 32 Fig. 2. Petitioner relies upon Ellsberry's disclosure that "[t]he four memory banks (i.e., Bank 0, Bank 1, Bank 2, and Bank 3) 212, 214, 216, and 218 are also communicatively coupled to an address bus 220 through which they receive address and command information from the control unit 204." Ex. 1005 ¶ 30; *see* Pet. 33. On the full record before us, we are persuaded that Ellsberry discloses *"a plurality of memory devices coupled to the module control circuit."*

Petitioner also relies upon Ellsberry's teaching that "[i]n one embodiment of the invention, the control unit 204 decodes a memory address received over the DIMM interface 202, determines to which memory bank the received address corresponds, and causes the memory bank switch 206 and 208 to activate the correct memory bank." Ex. 1005 ¶ 31; *see* Pet. 33. Ellsberry further states "[f]or example, if the control unit

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204 determines that a particular address is associated with, or mapped to, Bank 1212 coupled to memory bank switch 206, then it causes Port B to be activated and Port A to be disabled so that data is written to the correct memory bank 212." Ex. 1005 ¶ 31. Similarly, Ellsberry recites

> In one embodiment of the invention, the control unit 204 maps one logical memory bank to two physical memory banks. This is accomplished by selectively enabling or activating one of the two physical memory banks (e.g., either Port A or Port B) while disabling or deactivating the other. In this manner, only one of the two physical memory banks is written to or read from.

Ex. 1005 ¶ 40. Thus, Ellsberry discloses a "one-port-disabled" embodiment that activates one port while disabling the other. Ellsberry also discloses a "no-port-disabled" embodiment that activates both ports as follows:

> For example, in one implementation of the invention, the control unit 204 (FIG. 2) operates to send commands or instructions to two or more memory banks (e.g., Ports A & B) concurrently. That is, the control unit 204 sends the intended instruction to the selected memory bank and sends a no-op (no operation) instruction to the other memory bank(s).

Ex. 1005 ¶ 41; *see also id.* ¶¶ 11, 33; Ex. 1003 ¶ 208; Pet. 32. On the full record before us, we are persuaded that Ellsberry discloses

> *the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the first module control signals, the first memory devices output or receive each . . . data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command.*

According to Petitioner, "Ellsberry also discloses that each of the multiple (M) 'Data Group 0 through Data Group N' outputs or receives one byte (n=8 bits) simultaneously to provide the full bit width (M×n) of the

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module." 362 Pet. 35 (citing Ex. 1005 ¶¶ 29, 30, Fig. 2; Ex. 1003 ¶ 219). On the full record before us, we are persuaded that Ellsberry discloses "*N-bit wide*" data signals.

"M buffer circuits each configured to receive the second module control signals from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller;"

Petitioner contends that Ellsberry discloses the stated claim limitations. 362 Pet. 36–43 (citing Ex. 1003 ¶¶ 225–250). Specifically, Petitioner contends that Ellsberry's memory bank switches 206 and 208 teach the recited *"M buffer circuits each configured to receive the second module control signals from the module control circuit." Id.*; Ex. 1005, Fig. 2. Ellsberry also states "[t]he control unit 204 is communicatively coupled to the dual memory bank switches 206 & 208 via a control bus 210 and indicates to the memory bank switches 206 & 208 how data from the DIMM interface 202 should be received and/or stored." Ex. 1005 ¶ 29, Fig. 2; *see also* 362 Pet. 38; Ex. 1003 ¶ 227. Ellsberry further discloses bidirectional signal drivers 402 and 404, which are the claimed "buffer circuits" according to Petitioner's declarant. 362 Pet. 41; Ex. 1003 ¶ 242; Ex. 1005

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¶ 45. On the full record before us, we are persuaded that Ellsberry teaches the recited *"M buffer circuits."*

> Petitioner contends Ellsberry discloses
>
> *each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines*.

362 Pet. 36 (citing Ex. 1003 ¶¶ 225–239). As shown in Figure 2 of Ellsberry, *supra*, *M* switch ASICs 206, 208 (M=N=2 in this case) are connected to byte-sized (n=8) data buses 230, 232. 362 Pet. 36; Ex. 1005 ¶ 30. Petitioner contends Ellsberry discloses byte-sized data buses (234, 236) connected to respective memory banks "1" and "3" (212, 216) (*"second memory devices"*) and memory banks "0" and "2" (214, 218) (*"first memory devices"*). *Id.* On the full record before us, we are persuaded that Ellsberry teaches buffer circuits being coupled as recited.

> Petitioner contends Ellsberry discloses
>
> *the each respective buffer circuit including logic that responds to the second module control signals by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines*.

362 Pet. 40–43(citing Ex. 1003 ¶¶ 240–246). Ellsberry discloses that "[d]ata is transmitted from the DIMM interface 202 via the data bus 230 to bidirectional signal drivers 402, 404 that transmit and receive data over separate data busses 234 and 236 to the different sets of memory banks." Ex. 1005 ¶ 45; *see also* 362 Pet. 41. Petitioner's declarant testifies that

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> data bus 230 carries an [eight-bit] . . . section of the full bit width of the module (*"a respective n-bit section of the each N-bit wide data signal"*) which is communicated through the DIMM interface including the data bus 230 (*"the respective set of the M sets of n data lines"*) between the system "memory controller" and the targeted memory devices (*"respective one or more of the first memory devices"*).

Ex. 1003 ¶ 242. On the full record before us, we are persuaded that Ellsberry teaches each buffer circuit includes logic as recited.

Petitioner contends Ellsberry discloses *"wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller."* 362 Pet. 43 (citing Ex. 1003 ¶¶ 247–250). Ellsberry discloses that its memory module "presents a single load to the bus . . . not the load of the individual memory devices coupled thereto." Ex. 1005 ¶ 27; *see also* 362 Pet. 43; Ex. 1003 ¶ 248. According to Petitioner's declarant, Ellsberry's memory device load "is not 'presented' to the system bus because that load is electrically separated from the system bus" by "bidirectional drivers." Ex. 1003 ¶¶ 248, 249; *see also* Ex. 1005 ¶¶ 31, 45. On the full record before us, we are persuaded that Ellsberry teaches *"buffer circuits"* are configured as recited.

"a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB, the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of control signal lines, and between the M buffer circuits and the M sets of n data lines, wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at

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corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices."

Petitioner contends Ellsberry discloses *"a printed circuit board (PCB) having an edge connector positioned on an edge of the PCB."* 362 Pet. 44–45(citing Ex. 1003 ¶¶ 252–255). Specifically, "Ellsberry discloses a module on a PCB with an edge interface 506 (*'edge connector'*) in Figure 5 which corresponds to the module of Figure 2. *Id.*; Ex. 1005 ¶ 47; Ex. 1003 ¶¶ 252–253. Petitioner states, and we agree for purposes of this decision, that the memory module depicted in Ellsberry Figure 5 is a "printed circuit board (PCB)" because various circuits are mounted on it in a manner that is typical for PCBs, and because Figure 5 depicts the typical shape of a PCB in a SIMM[10] or DIMM[11] configuration, including an edge connector 506 "that serves to communicatively couple the memory module 500 to a memory slot or to a communication bus (e.g., memory bus, etc.)." 362 Pet. 45; Ex. 1005 ¶¶ 2, 47; Ex. 1010, 29, 66. According to Petitioner's declarant, the "edge interface" 506 is thus "*an edge connector positioned on an edge of the PCB.*" *Id.*; Ex. 1003 ¶¶ 254–255. On the full record before us, we are persuaded that Ellsberry discloses the recited *"PCB"*.

Petitioner contends Ellsberry discloses *"the edge connector comprising a plurality of electrical contacts configured to be releasably coupled to corresponding contacts of a computer system socket to provide electrical conductivity between the module control circuit and the set of*

[10] Single in-line memory module. 362 IPR Ex. 1001 8:61–67.

[11] Dual in-line memory module. 362 IPR Ex. 1001 8:61–67.

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control signal lines, and between the M buffer circuits and the M sets of n data lines." 362 Pet. 45–46 (citing Ex. 1003 ¶¶ 256–260). Petitioner and its declarant note Ellsberry states that the "edge interface 506 'serves to communicatively couple the memory module 500 to a memory slot' through electrical signals thereby disclosing that [such] interface is '*releasably coupled to corresponding contacts of a computer system socket*' and has '*electrical contacts configured . . . to provide electrical conductivity*.'" *Id.*; Ex. 1003 ¶¶ 256–257; Ex. 1005 ¶ 47. Petitioner notes Ellsberry discloses "[t]he DIMM interface 202 may be coupled to a memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted" and thus Ellsberry discloses *"control signal lines"* and *"data lines"* as claimed. Ex. 1005 ¶ 28 (emphasis added). Petitioner contends Ellsberry discloses *"M buffer circuits and M sets of n data lines."* On the full record before us, we are persuaded that Ellsberry discloses this limitation.

> Petitioner further asserts Ellsberry discloses
>
> *wherein the M buffer circuits are mounted on the PCB between the plurality of memory devices and the edge connector and are distributed along the edge connector at corresponding positions separate from each other, and wherein the each respective buffer circuit is disposed on the PCB in a position corresponding to the respective one or more of the first memory devices and the respective one or more of the second memory devices.*

362 Pet. 48 (citing Ex. 1003 ¶¶ 271–279). As shown below, the module of Figure 5 of Ellsberry "has nine bank switches 508 (*'M buffer circuits'* . . .) mounted on a PCB [502] between the memory devices of memory banks 504 and 512," and the edge interface 506. As Petitioner notes, in Figure 5 of Ellsberry, "[t]he bank switches 508 are distributed along the edge interface

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horizontally at uniformly spaced positions separate from one another, directly below the corresponding memory devices." 362 Pet. 48; Ex. 1003 ¶ 272; Ex. 1005 Fig. 5.

Figure 5 of Ellsberry is reproduced below.

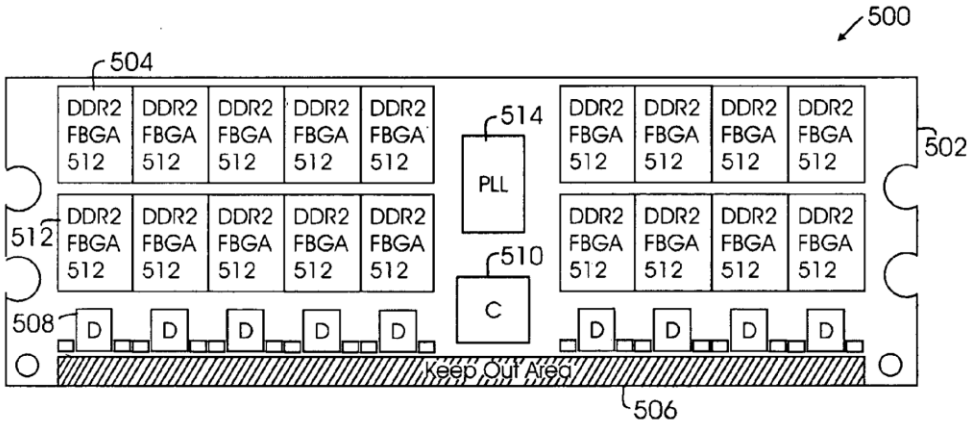


Fig. 5

Figure 5 of Ellsberry illustrates a memory module.

As shown in Figure 5, memory module 500 comprises substrate 502, memory devices 504, 512, edge interface 506, and memory controller 510. Ex. 1005 ¶ 47.

On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 1.[12] We are also persuaded that a person of ordinary skill in the art would have had reason to combine the cited disclosures of Ellsberry to obtain the claimed invention, and that such person

[12] Although Petitioner asserts an obviousness ground not an anticipation ground, Petitioner has not asserted any modification to Ellsberry would be necessary to meet the claim language. "[I]t is well settled that 'a disclosure that anticipates under § 102 also renders the claim invalid under § 103, for anticipation is the epitome of obviousness.'" Realtime Data, LLC v. Iancu, 912 F.3d 1368, 1373 (Fed. Cir. 2019) (quoting Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 1548 (Fed. Cir. 1983)).

would have had a reasonable expectation of success to arrive at the claimed memory module.

3. Mapping of Claim 16

Petitioner's mapping of claim 16 is identical to claim 1 for the preamble, "*control circuit*," and "*memory devices*." 362 Pet. 65–66. Claim 16 also recites "a plurality of buffer circuits," which we find are disclosed by Ellsberry. Ex. 1005 ¶¶ 11, 28, 30, 31, 45, Fig. 4; Ex. 1003 ¶¶ 186–196, 237, 247–250, 240–246, 403–410. Claim 16 further recites "*a printed circuit board (PCB) having an edge connector*," which we find is disclosed by Ellsberry. 362 Pet. 69–70 (citing Ex. 1003 ¶¶ 247–279, 409–414). Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of claim 16. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 16. On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 16, that a person of ordinary skill in the art would have had reason to combine the cited disclosures of Ellsberry, and would have had a reasonable expectation of success in arriving at the claimed memory module.

4. Mapping of Claim 30

Petitioner maps the preamble of claim 30 to Ellsberry. 363 Pet. 24–27 (citing Ex. 1005 ¶¶ 11, 26–30, 34, Figs. 1, 2; Ex. 1003 ¶¶ 186–196, 446–447; Ex. 1010, 6). Petitioner also maps the "*module control circuit*" to Ellsberry. 363 Pet. 27–31 (citing Ex. 1005 ¶¶ Abstract, 10, 29, 31, 36, 39, 45, 47, Figs. 1–4, 8A, 8B, 9; Ex. 1003 ¶¶ 126–134, 198, 199, 202–210, 327–342, 450, 452–458; Ex. 1011, 10, 22; Ex. 1009, 8–10.) Petitioner further

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maps the "*memory devices*" to Ellsberry. 363 Pet. 31–33 (citing Ex. 1005 ¶¶ 3, 11, 26, 29–33, Fig. 2, 3, 10–13; Ex. 1003 ¶¶ 138–152, 212–223, 448–458). Petitioner maps the "*plurality of buffer circuits*" to Ellsberry. 363 Pet. 33–41 (citing Ex. 1005 ¶¶ 28–31, 45, 47–56, Figs. 2, 4, 5, 6, 10–13; Ex. 1003 ¶¶ 210, 225–246, 403–408, 452–458, 462–463, 465–471). Petitioner maps the "*printed circuit board (PCB) having an edge connector*" to Ellsberry. 363 Pet. 41–46 (citing Ex. 1005 ¶¶ 2, 47, 48, 50, Figs. 2, 5; Ex. 1003 ¶¶ 194, 195, 230, 251–279, 473–476; Ex. 1010, 6, 29, 66, 73; Ex. 1006, 2:3–14, Figs. 1, 8). Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of claim 30. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 30. On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 30. We are also persuaded that a person of ordinary skill in the art would have had reason to combine the cited disclosures of Ellsberry to obtain the claimed invention, and that such person would have had a reasonable expectation of success to arrive at the claimed memory module.

5. Mapping of Claim 43

Petitioner contends the preamble of claim 43 is disclosed by Ellsberry. 363 Pet. 61 (citing Ex. 1003 ¶¶ 186–196, 515, 516). Petitioner also contends Ellsberry discloses the "*memory devices*" limitation. 363 Pet. 61 (citing Ex. 1003 ¶¶ 210, 212–224, 517, 518). Petitioner further contends Ellsberry discloses the "*module control circuit*" limitation. 363 Pet. 61–64 (citing Ex. 1005 ¶¶ 11, 28–33, Fig. 2; Ex. 1003 ¶¶ 206–211, 215–223, 452–458, 521–

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524; Ex. 1009 at 14). Petitioner contends Ellsberry discloses the "*plurality of buffer circuits*" limitation. 363 Pet. 64–66 (citing Ex. 1003 ¶¶ 225–239, 247–250, 403–408, 526–531). Petitioner contends Ellsberry discloses the "*printed circuit board (PCB) having an edge connector*" limitation. 363 Pet. 66 (citing ¶¶ 251–279, 532–535). Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of claim 43. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 43. On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 43. We are also persuaded that a person of ordinary skill in the art would have had reason to combine the cited disclosures of Ellsberry to obtain the claimed invention, and that such person would have had a reasonable expectation of success to arrive at the claimed memory module.

6. Mapping of Claim 53

Petitioner maps the preamble of claim 53 to Ellsberry. 363 Pet. 70–71 (citing Ex. 1003 ¶¶ 186–196, 562, 563). Petitioner also maps the "*module control circuit*" limitation to Ellsberry. 363 Pet. 71–72 (citing Ex. 1003 ¶¶ 198–201, 346–349, 452–458, 565–567). Petitioner further maps the "*memory devices*" limitation to Ellsberry. 363 Pet. 72–73 (citing Ex. 1003 ¶¶ 212–224, 346–349, 569–571). Petitioner maps the "*plurality of buffer circuits*" limitation to Ellsberry. 363 Pet. 73–75 (Ex. 1005 Fig. 4; Ex. 1003 ¶¶ 225–239, 403–408, 415–423, 573–578). Petitioner maps the "*printed circuit board (PCB)*" limitation to Ellsberry. 363 Pet. 75 (citing Ex. 1003 ¶¶ 251–279, 581–584). Patent Owner does not contend that Ellsberry, as

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mapped in the Petitions, fails to disclose any feature of claim 53. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 53. On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 53. We are also persuaded that a person of ordinary skill in the art would have had reason to combine the cited disclosures of Ellsberry to obtain the claimed invention, and that such person would have had a reasonable expectation of success to arrive at the claimed memory module.

7. Mapping of Claim 58

Petitioner maps the preamble of claim 58 to Ellsberry. 362 Pet. 70–71 (citing Ex. 1003 ¶¶ 186–196, 212–224, 593–596). Petitioner also maps the "*module control circuit*" limitation to Ellsberry. 362 Pet. 71–74 (citing Ex. 1005 ¶¶ 29, 31, 39, Figs. 8A, 8B, 9; Ex. 1003 ¶¶ 198–201, 212–224, 327–336, 338–341, 452–458, 598, 600–602; Ex. 1011, 10). Petitioner further maps the "*plurality of buffer circuits*" limitation to Ellsberry. 362 Pet. 74–77 (citing Ex. 1005 ¶ 45, Fig. 4; Ex. 1003 ¶¶ 240–250, 403–408, 452–458, 465–470, 608, 609). Petitioner likewise maps the "*printed circuit board (PCB)*" limitation to Ellsberry. 362 Pet. 77–78 (citing Ex. 1003 ¶¶ 251–279, 610–613). Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of claim 58. *See generally* PO Resp. Having reviewed the cited portions of Ellsberry and accompanying testimony, we adopt Petitioner's mapping of claim 58. On the full record before us, we are persuaded that Ellsberry discloses all of the limitations of claim 58. We are also persuaded that a person of ordinary

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skill in the art would have had reason to combine the cited disclosures of Ellsberry to obtain the claimed invention, and that such person would have had a reasonable expectation of success to arrive at the claimed memory module.

8. Patent Owner's Argument Alleging Petitioner Combines Mutually Exclusive Embodiments of Ellsberry

Patent Owner does not contend that Ellsberry, as mapped in the Petitions, fails to disclose any feature of the claims. *See generally* PO Resp. Instead, Patent Owner's main contention against the challenges to all claims is that the Petitions mix mutually exclusive portions of Ellsberry in arriving at the claimed invention. PO Resp. 9–61. Specifically, Patent Owner contends that Petitioner maps the claimed "first module control signals" to Ellsberry's "no-port-disabled scheme," and the claimed "second module control signals" to Ellsberry's "one-port disabled scheme." PO Resp. 9–11 (citing Ex. 1005 ¶¶ 40, 41, Fig. 2; Ex. 2002 ¶¶ 47–50). Patent Owner contends these two "disparate port schemes" are mutually exclusive embodiments that one of ordinary skill in the art would not have combined in an effort to obtain the claimed invention. *Id.* at 41–44.

Petitioner replies that it relies solely on what Patent Owner refers to as Ellsberry's "one-port-disabled functionality," and does not at all rely on the "no-port-disabled functionality" in its mapping to the claims. Corr. Reply 12–13; Tr. 24–25, 72. Petitioner's declarant, Dr. Stone, similarly testifies that the mapping of the claims to Ellsberry relies only on what Patent Owner refers to as the "one-port-disabled functionality." PO Resp. 15–16 (citing Ex. 2003, 93:22–94:1, 94:8–10, 94:21–22, 95:6–8, 96:7–18, 97:5–8, 97:16–98:14, 98:24–99:1, 99:16–23, 109:24–110:2). Thus, the main issue in this

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case centers on whether Petitioner's mappings to the claimed invention encompass mutually exclusive teachings of Ellsberry.

As Petitioner notes, the terms "no-port-disabled scheme" and "one-port-disabled scheme" are not mentioned anywhere in Ellsberry. Corr. Reply 4. Nevertheless, Patent Owner contends the substance of Ellsberry's paragraphs 40 and 41 disclose two mutually exclusive port schemes. PO Resp. 9–10. Ellsberry's paragraph 40 mentions "selectively enabling or activating one of the two physical memory banks (e.g., either Port A or Port B) while disabling or deactivating the other." Ex. 1005 ¶ 40. Patent Owner refers to this as the "one-port-disabled scheme." PO Resp. 9. In contrast, Ellsberry's paragraph 41 discloses "a novel scheme for performing operations in a first memory bank (i.e., Port A [of Switch ASIC 206 or 208] in Fig. 2) without disabling or deactivating a second memory bank (i.e., Port B [of Switch ASIC 206 or 208] in Fig. 2)." Ex. 1005 ¶ 41. Paragraph 41 further states "control unit 204 sends the intended instruction to the selected memory bank and sends a [NOP] (no operation) instruction to the other memory bank(s)." *Id.* This is what Patent Owner refers to as "no-ports-disabled scheme" in which both Port A and Port B of Switch ASIC 206 or 208 are activated at the same time and a write instruction is transmitted to a targeted memory bank while the other memory banks are disabled with NOPs. PO Resp. 10; Ex. 1005 ¶ 41.

Patent Owner's argument hinges critically on the assumption that only the "no-ports-disabled" embodiment (and not the "one-port-disabled" embodiment) uses commands and NOPs to perform memory bank selection. We do not agree a person of ordinary skill in the art would have read Ellsberry so restrictively. Ellsberry's paragraph 31 discloses bank switches

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206, 208 activate one and deactivate the other of ports A and B to select a bank for a memory read or write operation. Ex. 1005 ¶ 31. We agree with Dr. Stone that a person of ordinary skill in the art would have understood that Ellsberry teaches that when multiple banks are connected to each of ports A and B, row selection in addition to bank selection is needed to select a particular memory device for an operation. *See*, *e.g.*, Ex. 1003 ¶ 138. Ellsberry's paragraph 33 states: "Alternatively, when **row/bank mode addressing** is used, read and write commands are sent only to the targeted memory device. A NOP (no-operation) command is sent to the non-targeted memory device." Ex. 1005 ¶ 33 (Emphasis added.) We agree with Petitioner that a person of ordinary skill in the art would have understood these two Ellsberry paragraphs to suggest the possibility of using bank addressing through port selection via switches 206, 208 in addition to row addressing by sending a command to a targeted memory devices of a memory bank and NOPs to other memory devices connected to the same switch port. *See*, *e.g.*, 362 Pet. 32–33.

Additional evidence supporting the combination of row addressing through commands and NOPs and bank addressing using ports A and B of switches 206, 208 can be gleaned from Ellsberry's paragraph 28, which states the "capacity-expanding feature . . . is accomplished by **a combination of a control unit 204 and one or more memory bank switches 206 & 208**." Ex. 1005 ¶ 28 (emphasis added). This statement implies that selection of a particular memory device for a read or write operation is accomplished by the control unit and switches working in tandem. Ellsberry also states the bank switches serve the purpose of "reduc[ing] resistive and/or capacitive loading of the data bus coupled to the

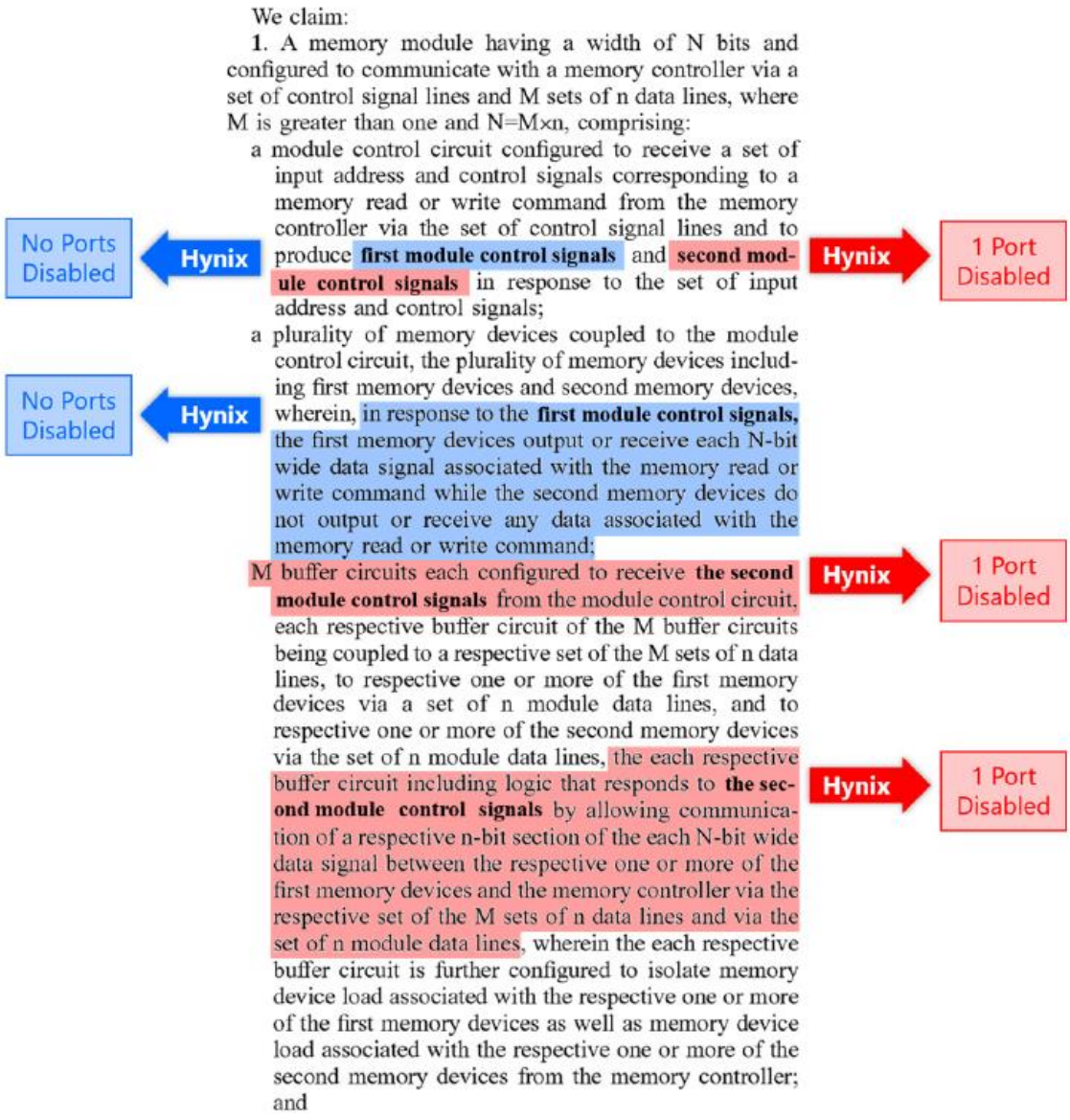
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DIMM interface and the bus 110 while emulating a standard memory device interface." *Id.* ¶ 31. Ellsberry also explains why it uses commands and NOPs for bank selection: "the control unit and switch architecture can control data to and from the memory banks without the delays caused by otherwise disabling the banks." *Id.* ¶ 42. We agree with Dr. Stone that a person of ordinary skill in the art reading Ellsberry would have understood that both advantages could be achieved by combining bank addressing using switches 206, 208 and row addressing through commands and NOPs using control unit 204. *See, e.g.*, Ex. 1003 ¶ 138.

We agree with Patent Owner that what Patent Owner identifies as "disparate port schemes" could not be used simultaneously because that would require the impossibility of activating and deactivating one of Ports A and B of the switches 206, 208 at the same time. *See, e.g.*, PO Resp. 9. Nonetheless, both alleged port schemes use signals on Ellsberry's bus 220 that can be considered "*first module control signals*" and signals on Ellsberry's bus 210 that can be regarded as "*second module control signals*." *See, e.g.*, Ex. 1005, Fig. 1 [210], [220]. Specifically, in what Patent Owner refers to as the "no-ports-disabled" embodiment (Ellsberry ¶ 40), bus 220 carries the memory address, instructions and NOP signals, while bus 210 carries a control signal to activate both Ports A and B of Switch ASIC 206 or 208. In what Patent Owner refers to as the "one-port disabled" embodiment (Ellsberry ¶ 41), bus 220 carries the memory address, instructions, and NOP signals, and bus 210 carries a control signal to disable one and activate the other of Ports A and B of Switch ASIC 206 or 208. Accordingly, we do not agree with Patent Owner's argument that "*first module control signals*" always correspond to the "no-ports-disabled" embodiment and the "*second*

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module control signals" always correspond to the "one-port disabled" embodiment, as Patent Owner's argument seems to suggest. *See* diagram at PO Resp. 12, reproduced below.



We claim:

1. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a module control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce **first module control signals** and **second module control signals** in response to the set of input address and control signals;

a plurality of memory devices coupled to the module control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to the **first module control signals,** the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

M buffer circuits each configured to receive **the second module control signals** from the module control circuit, each respective buffer circuit of the M buffer circuits being coupled to a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including logic that responds to **the second module control signals** by allowing communication of a respective n-bit section of the each N-bit wide data signal between the respective one or more of the first memory devices and the memory controller via the respective set of the M sets of n data lines and via the set of n module data lines, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and

In the diagram above, Patent Owner's arguments for claim 1 are shown graphically with language highlighted in blue and red. Patent Owner refers to the limitations depicted in blue as "telltale signs" of the "no-ports-

disabled" embodiment, and limitations in red as "telltale signs" of the "one-port disabled" embodiment. PO Resp. 27–34.

From the diagram above, it can be seen that what Patent Owner refers to as the "no-ports-disabled" embodiment maps to the following claim language of claim 1:

> in response to the first module control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command.

As noted above, however, what Patent Owner refers to as Ellsberry's "one-port-disabled" scheme uses memory address, command, and NOP signals on bus 220 to target particular memory banks, which output the addressed data in response thereto. *See* Ex. 1005 ¶¶ 33, 40. Thus, the alleged "one-port-disabled" scheme of Ellsberry discloses this claim limitation, and we are not persuaded by Patent Owner's contention that this claim language is restricted to the "no-ports-disabled" embodiment.

The Petition cites to Ellsberry's paragraph 41 in the mapping of the claimed "*module control circuit*," which is the same paragraph Patent Owner asserts discloses the "no-ports-disabled" embodiment. 362 Pet. 32; PO Resp. 10. However, the apparent reason Petitioner mentions paragraph 41 is for its discussion of memory bank selection using instructions (commands) and no-operations (NOPs), not for the operation of ports A and B of the Switch ASICs. 362 Pet. 32. In other words, paragraph 41's use of instructions and NOPs to select memory banks is applicable to both the "no-ports-disabled" and "one-port-disabled" embodiments though the technique is described in paragraph 41 in connection with Patent Owner's "no-ports-

Samsung Ex. 1117, p. 36
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disabled" embodiment. In addition to paragraph 41, Petitioner relies on paragraphs 11 and 33 to disclose the "module control circuit" of claim 1, and these paragraphs also mention the use of commands and NOPs to address memory banks or the memory devices thereof in read or write operations, similarly to paragraph 41. *Id.* Thus, Petitioner's reliance on paragraph 41 is not limited to a particular port scheme.

We also do not agree with Patent Owner's argument that the alleged "no-ports-disabled" embodiment of Ellsberry uses only the "column addressing mode" while the alleged "one-port-disabled" embodiment of Ellsberry uses only the "row/bank addressing mode." Prelim. Resp. 6–9; PO Resp. 19–25. This assertion is not borne out by Ellsberry, and Patent Owner identifies insufficient evidentiary support to establish this assertion as fact.

In summary, for the stated reasons, we conclude that Petitioner has shown that Ellsberry discloses all elements of claim 1. Specifically, in Patent Owner's terminology, Petitioner has shown that the "one-port disabled" embodiment with row/bank addressing discloses all elements of claim 1. Patent Owner has not established that Petitioner combined disparate or mutually exclusive port schemes in showing that claim 1 would have been obvious over Ellsberry. Consequently, on the full record before us, we conclude that Petitioner has shown by a preponderance of the evidence that claim 1 is obvious over Ellsberry.

We do not reach the issue of whether what Patent Owner refers to as the "no-port-disabled" embodiment of Ellsberry also would have rendered claim 1 obvious. Consequently, Patent Owner's arguments concerning the Board's so-called "either-or" view (PO Resp. 11–36) are moot.

As with claim 1 above, Patent Owner does not contend Ellsberry fails

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to disclose any element of independent claims 16, 30, 43, 53, and 58. *See generally* PO Resp. Instead, Patent Owner presents similar arguments as for claim 1, namely, that one of ordinary skill in the art would not have combined Ellsberry's alleged "no-ports-disabled" embodiment with Ellsberry's alleged "one-port-disabled" embodiment in an effort to obtain the claimed invention.

Patent Owner's arguments for these claims are shown graphically in Patent Owner's diagrams below. Again, Patent Owner refers to the limitations depicted in blue as "telltale signs" of the "no-ports-disabled" embodiment, and limitations in red as "telltale signs" of the "one-port disabled" embodiment. PO Resp. 27–34.

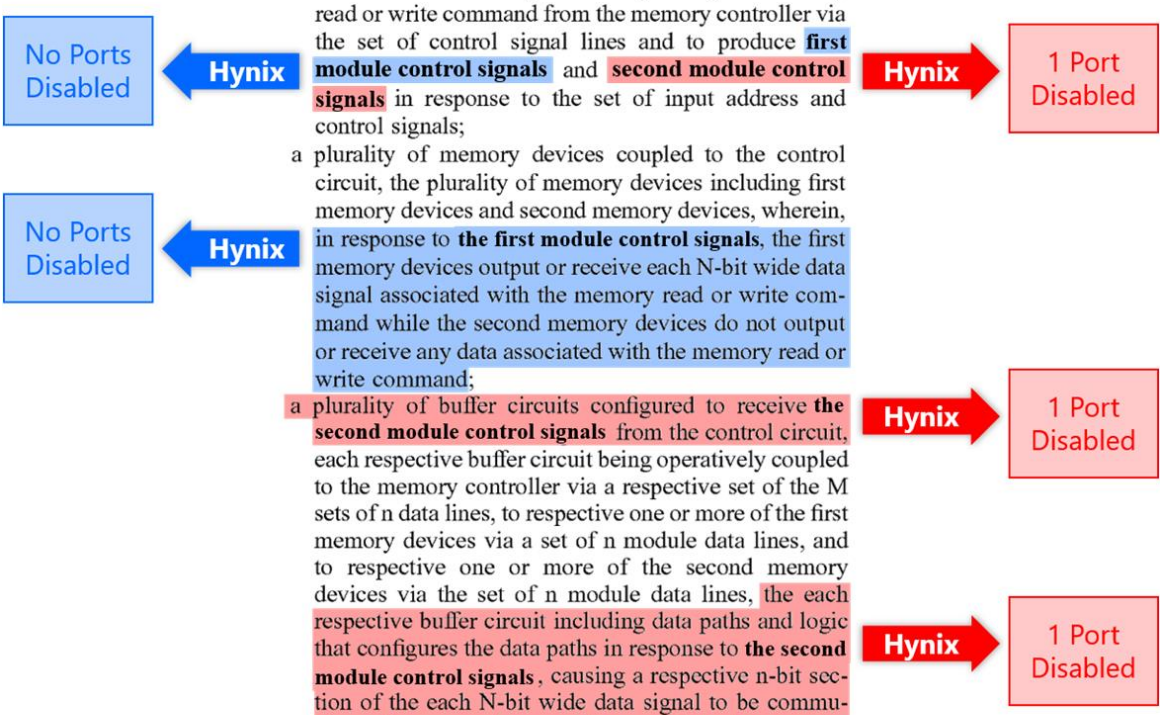
Samsung Ex. 1117, p. 38
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16. A memory module having a width of N bits and configured to communicate with a memory controller via a set of control signal lines and M sets of n data lines, where M is greater than one and N=M×n, comprising:

a control circuit configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce **first module control signals** and **second module control signals** in response to the set of input address and control signals;

a plurality of memory devices coupled to the control circuit, the plurality of memory devices including first memory devices and second memory devices, wherein, in response to **the first module control signals**, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits configured to receive **the second module control signals** from the control circuit, each respective buffer circuit being operatively coupled to the memory controller via a respective set of the M sets of n data lines, to respective one or more of the first memory devices via a set of n module data lines, and to respective one or more of the second memory devices via the set of n module data lines, the each respective buffer circuit including data paths and logic that configures the data paths in response to **the second module control signals**, causing a respective n-bit section of the each N-bit wide data signal to be communicated between the respective set of the M sets of n data lines and the set of n module data lines through the respective buffer circuits, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices as well as memory device load associated with the respective one or more of the second memory devices from the memory controller; and



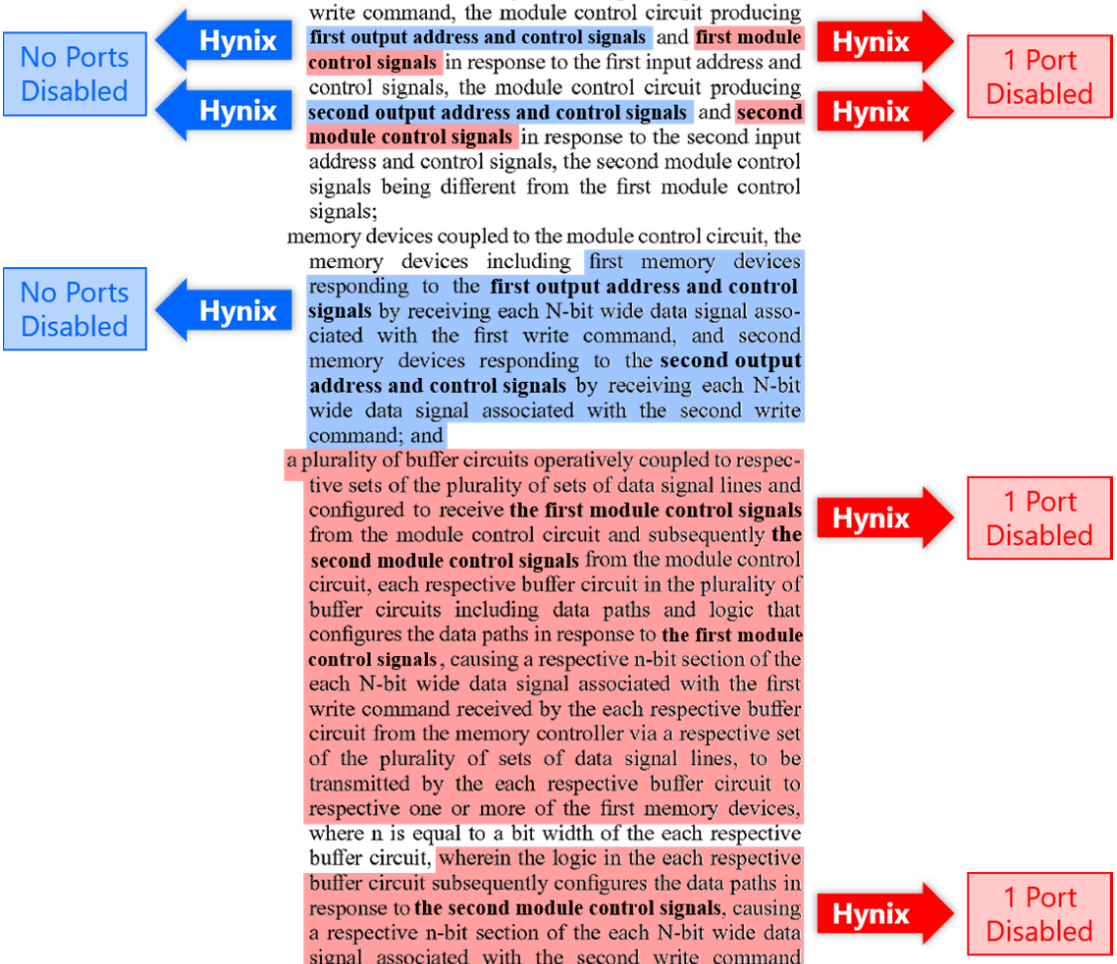
PO Resp. 53.

30. A memory module having a data width of N bits and configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

a module control circuit configured to receive from the memory controller via the set of control signal lines first input address and control signals corresponding to a first write command and subsequently second input address and control signals corresponding to a second write command, the module control circuit producing **first output address and control signals** and **first module control signals** in response to the first input address and control signals, the module control circuit producing **second output address and control signals** and **second module control signals** in response to the second input address and control signals, the second module control signals being different from the first module control signals;

memory devices coupled to the module control circuit, the memory devices including first memory devices responding to the **first output address and control signals** by receiving each N-bit wide data signal associated with the first write command, and second memory devices responding to the **second output address and control signals** by receiving each N-bit wide data signal associated with the second write command; and

a plurality of buffer circuits operatively coupled to respective sets of the plurality of sets of data signal lines and configured to receive **the first module control signals** from the module control circuit and subsequently **the second module control signals** from the module control circuit, each respective buffer circuit in the plurality of buffer circuits including data paths and logic that configures the data paths in response to **the first module control signals**, causing a respective n-bit section of the each N-bit wide data signal associated with the first write command received by the each respective buffer circuit from the memory controller via a respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the first memory devices, where n is equal to a bit width of the each respective buffer circuit, wherein the logic in the each respective buffer circuit subsequently configures the data paths in response to **the second module control signals**, causing a respective n-bit section of the each N-bit wide data signal associated with the second write command received by the each respective buffer circuit from the memory controller via the respective set of the plurality of sets of data signal lines, to be transmitted by the each respective buffer circuit to respective one or more of the second memory devices, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein each of the respective one or more of the first memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein each of the respective one or more of the second memory devices receives at least a portion of the respective n-bit section of the each N-bit wide data signal associated with the second write command; and



PO Resp. 58.

43. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices;

a module control circuit coupled to the set of control signal lines and configured to receive from the memory controller a set of input address and control signals corresponding to a memory read or write command via the set of control signal lines, and to produce **output address and control signals** in response to the set of input address and control signals, wherein the module control circuit is further configured to evaluate the set of input address and control signals to determine a subset of the memory devices to output or receive data associated with the memory read or write command, and to produce **a set of module control signals** dependent on which of the memory devices are determined to be the subset of the memory devices, and wherein, in response to **the output address and control signals**, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices not in the subset of the memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits each configured to receive **the set of module control signals** from the module control circuit, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective module data lines that are coupled to respective one or more memory devices in the subset of the memory devices and to one or more of the other memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to **the set of module control signals** to allow a respective portion of the data associated with the memory read or write command to be communicated between the memory controller and the respective one or more memory devices in the subset of the memory devices through the each respective buffer circuit, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more memory devices in the subset of the memory devices and memory device load associated with the one or more of the other memory devices from the memory controller; and

No Ports Disabled — Hynix

No Ports Disabled — Hynix

Hynix — 1 Port Disabled

Hynix — 1 Port Disabled

Hynix — 1 Port Disabled

PO Resp. 59.

53. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data signal lines, comprising:

a module control circuit coupled to the set of control signal lines and configured to receive a set of input address and control signals corresponding to a memory read or write command from the memory controller via the set of control signal lines and to produce **output address and control signals** and **a set of module control signals** in response to the input address and control signals, the module control circuit having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections;

memory devices including first memory devices and second memory devices, the first memory devices including a first number of memory devices coupled to the first input/output connections and a second number of memory devices coupled to the second input/output connections, the second memory devices including a third number of memory devices coupled to the third input/output connections and a fourth number of memory devices coupled to the fourth input/output connections, wherein, in response to **the output address and control signals**, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command;

a plurality of buffer circuits each configured to receive **the set of module control signals** from the module control circuit, wherein each respective buffer circuit is coupled between respective one or more of the first memory devices and a respective set of the plurality of sets of data lines, and between respective one or more of the second memory devices and the respective set of the plurality of sets of data lines, the each respective buffer circuit including data paths and logic that configures the data paths in response to the **set of module control signals** to allow a respective section of the each N-bit wide data signal to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the data paths include write data paths and read data paths, the write data paths including tristate buffers controlled by the logic and the read data paths including tristate buffers controlled by the logic, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and the respective one or more of the second memory devices from the memory controller; and

No Ports Disabled ← Hynix

Hynix → 1 Port Disabled

No Ports Disabled ← Hynix

Hynix → 1 Port Disabled

Hynix → 1 Port Disabled

PO Resp. 60.

58. A memory module configured to communicate with a memory controller via a set of control signal lines and a plurality of sets of data lines, comprising:

memory devices including first memory devices and second memory devices;

a module control circuit coupled to the set of address and control signal lines and configured to receive from the memory controller via the set of control signal lines a first set of input address and control signals corresponding to a first memory read or write command and subsequently a second set of input address and control signals corresponding to a second memory read or write command, and to produce **first output address and control signals** in response to the first set of input address and control signals and **second output address and control signals** in response to the second set of input address and control signals, wherein, in response to **the first output address and control signals**, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to **the second output address and control signals**, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second memory read or write command, and wherein the module control circuit is further configured to produce **a first set of module control signals** in response to the first set of input address and control signals and **a second set of module control signals** in response to the second set of input address and control signals, the second set of module control signals being different from the first set of module control signals;

a plurality of buffer circuits each configured to receive from the module control circuit **the first set of module control signals** and subsequently **the second set of module control signals**, wherein each respective buffer circuit of the plurality of buffer circuits is coupled between a respective set of the plurality of sets of data lines and respective one or more of the first memory devices, and between the respective set of the plurality of sets of data lines and respective one or more of the second memory devices, the each respective buffer circuit including data paths and logic that configures the data paths in response to **the first set of module control signals** to allow a respective portion of the data associated with the first memory read or write command to be communicated between the memory controller and the respective one or more of the first memory devices through the each respective buffer circuit, wherein the logic subsequently configures the data paths in response to **the second set of module control signals** to allow a respective portion of the data associated with the second memory read or write command to be communicated between the memory controller and the respective one or more of the second memory devices through the each respective buffer circuit, the data paths being configured differently when the logic is responding to the second module control signals from when the logic is responding to the first module control signals, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the one or more of the second memory devices from the memory controller; and

No Ports Disabled — Hynix
Hynix
No Ports Disabled — Hynix
Hynix — 1 Port Disabled
Hynix — 1 Port Disabled
Hynix — 1 Port Disabled
Hynix — 1 Port Disabled

PO Resp. 54.

For claim 16, the language of the claim argued as demonstrating what Patent Owner refers to as the "no-ports-disabled" embodiment is identical to claim 1. Thus, for similar reasons as stated with respect to claim 1, we are not persuaded by Patent Owner's arguments. Specifically, as discussed with respect to claim 1, the language highlighted in blue above is not unique to the alleged "no-ports-disabled" embodiment of Ellsberry, but is disclosed by the alleged "one-port-disabled" embodiment of Ellsberry as well. Accordingly, we find that Petitioner has shown by a preponderance of the evidence that claim 16 is obvious over Ellsberry for the reasons explained with respect to claim 1.

According to Patent Owner, claim 30 recites the "telltale signs" of "*first input address and control signals*," "*second input address and control signals*," and

> *the memory devices including first memory devices responding to the first output address and control signals by receiving each N-bit wide data signal associated with the first write command, and second memory devices responding to the second output address and control signals by receiving each N-bit wide data signal associated with the second write command*.

PO Resp. 12. Claim 30 recites that the "*second input address and control signals*" are generated by the module control circuit subsequently to the "*first input address and control signals*" and thus claim 30 covers operation of the claimed memory module over multiple reading or writing cycles. *See* Ex. 1003 ¶¶ 448, 450. Petitioner contends the claimed "*first memory devices*" may be mapped to Bank 1 in Ellsberry's Figure 2, and the "*second memory devices*" may be mapped to either Bank 3, as Patent Owner seems to contend (using "column addressing mode"), or as Bank 0 or Bank 2, which Petitioner contends is the proper construction (using "row/bank

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addressing mode"). 363 Pet. 33 (citing Ex. 1005 ¶¶ 30, 31, Figs. 2, 13; Ex. 1003 ¶¶ 138–152, 222, 448–458). We agree with Petitioner that the claimed language is not restricted to Ellsberry's "no-ports-disabled" embodiment, as Patent Owner contends. Instead, the claim limitation is disclosed by Ellsberry's alleged "one-port-disabled" embodiment using the "row/bank addressing mode" with read and write commands transmitted to the targeted memory device and NOPs transmitted to the non-targeted memory devices. Ex. 1005 ¶¶ 30, 31, 33, 42, Fig. 8A. Specifically, as Petitioner notes, the claimed "*first memory devices*" are disclosed by Banks 1 (212, 226) and the claimed "*second memory devices*" are disclosed by Banks 0 (214, 222) or Banks 2 (218, 224), as shown in Ellsberry's Figure 2. In what Patent Owner refers to as the "one-port-disabled" embodiment, the "*first input address and control signals*" are disclosed by Ellsberry's read or write commands to the targeted Banks 1 and NOPs to the other Banks, and the "*second input address and control signals*" are disclosed by read or write commands to the targeted Banks 0 or Banks 2 and NOPs sent to the other banks in a subsequent reading or writing cycle. Accordingly, we do not agree with Patent Owner's contention that Petitioner mixes mutually exclusive embodiments of Ellsberry. Instead, we find that Petitioner shows by a preponderance of the evidence that claim 30 is unpatentable as obvious over Ellsberry.

According to Patent Owner, claim 43 recites "tell-tales" of the "no-ports-disabled" embodiment, namely, the claimed "*output address and control signals*" and the claim limitation that recites

> *in response to the output address and control signals, the subset of the memory devices output or receive the data associated with the memory read or write command while other memory devices*

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> *not in the subset of the memory devices do not output or receive any data associated with the memory read or write command*.

PO Resp. 59. Petitioner contends these limitations are disclosed by what Patent Owner refers to as Ellsberry's "one-port-disabled" embodiment. 363 Pet. 63–64 (citing Ex. 1005 ¶¶ 11, 31, 33, Fig. 2; Ex. 1003 ¶¶ 215–223, 524); Corr. Reply 40. Specifically, as Petitioner notes, the "output address and controls signals" in the "row/bank addressing mode" are memory addresses, commands and NOPs transmitted to Banks 0–3 on bus 220 in Ellsberry's Figure 2. Ex. 1005 ¶¶ 11, 31, 33, Fig. 8A. In response to these signals, one subset of the memory devices (Banks 1) outputs or receives the data associated with the memory read or write command while other memory devices not in the subset (Banks 0, 2, or 3) do not output or receive any data associated with the memory read or write command. Consequently, the claim limitation Patent Owner contends is a "telltale sign" of the "no-ports-disabled" embodiment is actually "row/bank addressing mode." Thus, we are not persuaded by Patent Owner's argument. Petitioner demonstrates the claimed feature is not unique to Patent Owner's alleged "no-ports-disabled" embodiment but is included in the "one-port-disabled" embodiment.

According to Patent Owner, claim 53 recites "telltale signs" of the "no-port-disabled" embodiment, namely, the claimed "*output address and control signals*" and the claim limitation that recites "*in response to the output address and control signals, the first memory devices output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices do not output or receive any data associated with the memory read or write command*." PO Resp.

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60. Petitioner contends these limitations are disclosed by what Patent Owner refers to as Ellsberry's "one-port-disabled" embodiment. 363 Pet. 71–72 (citing Ex. 1003 ¶¶ 212–224, 346–349, 569–571). Specifically, as Petitioner notes, the "*output address and controls signals*" in the "row/bank addressing mode" are memory addresses, commands and NOPs transmitted to Banks 0–3 on bus 220 in Ellsberry's Figure 2. 363 Pet. 29, 32, 64, 71–72; Ex. 1005 ¶¶ 11, 31, 33, Fig. 8A. In response to these signals, first memory devices (Banks 1) output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices (Banks 0, 2, or 3) do not output or receive any data associated with the memory read or write command. Thus, the claim limitation that Patent Owner contends is a "telltale sign" of the "no-ports-disabled" embodiment is actually "row/bank addressing mode" via signals on bus 220 in Ellsberry's Figure 2. Accordingly, we are not persuaded by Patent Owner's argument. Petitioner demonstrates the claimed feature is not unique to the "no-ports-disabled" embodiment but instead encompasses the so-called "one-port-disabled" embodiment of Ellsberry.

Patent Owner contends claim 58 recites "telltale signs" of the "no-ports-disabled" embodiment, namely, the claimed "*first output address and control signals*," "*second output address and control signals*," and

> *in response to the first output address and control signals, the first memory devices output or receive data associated with the first memory read or write command while the second memory devices do not output or receive any data associated with the first memory read or write command, wherein, in response to the second output address and control signals, the second memory devices output or receive data associated with the second memory read or write command while the first memory devices do not output or receive any data associated with the second*

memory read or write command.

PO Resp. 54. Petitioner contends these limitations are disclosed by what Patent Owner refers to as Ellsberry's "one-port-disabled" embodiment. 362 Pet. 71–74 (citing Ex. 1005 ¶¶ 29, 31, 39, Figs. 8A, 8B, 9; Ex. 1003 ¶¶ 198–201, 212–224, 327–336, 338–341, 346–349, 452–458, 569–571, 598, 600–602; Ex. 1011, 10). Specifically, as Petitioner notes, the claimed "*first output address and control signals*" and "*second output address and control signals*" in the "row/bank addressing mode" are memory addresses, commands and NOPs transmitted to Banks 0–3 on bus 220 in Ellsberry's Figure 2. Ex. 1005 ¶¶ 11, 31, 33, Fig. 8A. In response to the first output address and control signals, first memory devices (Banks 1) output or receive each N-bit wide data signal associated with the memory read or write command while the second memory devices (Banks 0, 2, or 3) do not output or receive any data associated with the memory read or write command. Conversely, in response to the second output address and control signals, the second memory devices (Banks 0, 2, or 3) output or receive each N-bit wide data signal associated with the memory read or write command while the first memory devices (Banks 1) do not output or receive any data associated with the second memory read or write command. Thus, the claim limitation that Patent Owner contends is a "telltale sign" of the "no-ports-disabled" embodiment encompasses "row/bank addressing mode" via signals on bus 220 in Ellsberry's Figure 2. Accordingly, we are not persuaded by Patent Owner's argument that these claim limitations are "telltale signs" unique to the so-called "no-ports-disabled" embodiment because the claim language encompasses the so-called "one-port-disabled" embodiment of Ellsberry.

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For the foregoing reasons, we determine that Petitioner does not mix mutually exclusive embodiments of Ellsberry in showing claims 16, 30, 43, 53, and 58 are unpatentable as obvious. As Petitioner shows all limitations of the claims are disclosed in Ellsberry, we conclude Petitioner has shown by a preponderance of the evidence that independent claims 16, 30, 43, 53, and 58 are unpatentable as obvious over Ellsberry.

9. Claims 2, 4, 10, 21, 22 – Chip-Select Signal

Claim 2 recites

> *The memory module of claim 1, wherein the set of input address and control signals include at least one first chip-select signal, wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals, the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal*.

Claim 22 recites the same limitations. Petitioner contends the limitations of claims 2 and 22 are disclosed by Ellsberry. 362 Pet. 50–52 (citing Ex. 1005 ¶¶ 11, 28–33, 35–39, 42, 47, 52, 56, Figs. 2, 5, 8B, 11, 13; Ex. 1003 ¶¶ 222, 281–290, 299–301, 370, 379, 428–429; Ex. 1011, 6; Ex. 1007, Fig. 5). Patent Owner does not contend that Ellsberry fails to disclose the claimed limitations, only that Petitioner combines mutually exclusive embodiments, an argument we find unpersuasive for the reasons stated with respect to claims 1 and 16 discussed above.

We agree with Petitioner the claimed "chip-select signal" is disclosed in Ellsberry. Ellsberry's Figure 13 is shown below:

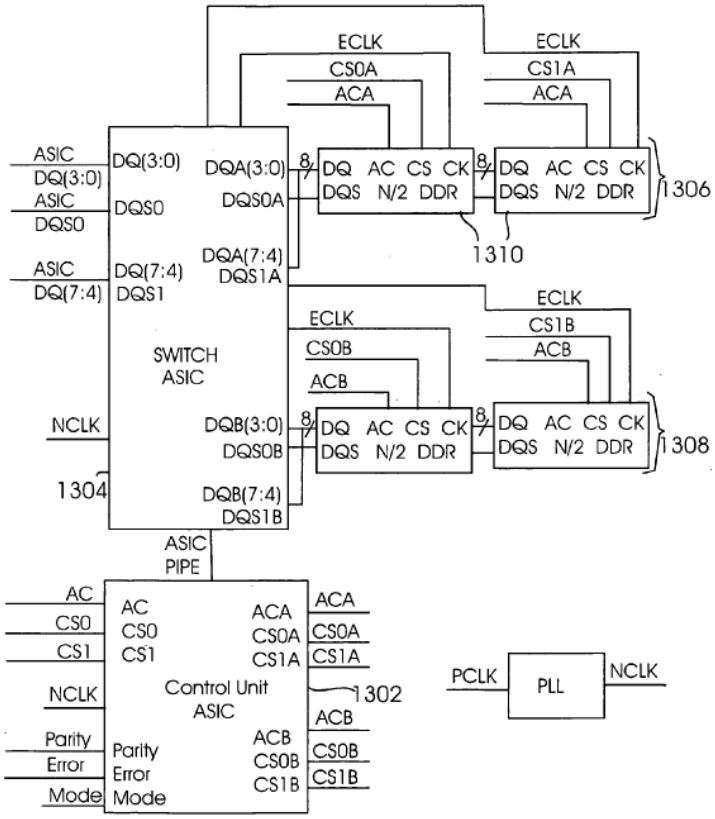


Fig. 13

Figure 13 shows part of a memory module with memory banks having eight-bit memory devices

In Ellsberry's Figure 13, above, input signals are input to control unit ASIC 1302 from the left, including chip select signals CS0, CS1. *See also* Ex. 1005 ¶ 56. These chip select signals disclose the claimed "*wherein the set of input address and control signals include at least one first chip-select signal*."

Using signals CS0, CS1, control unit ASIC 1302 generates chip select signals CS0A, CS1A, CS0B, CS1B to selectively enable memory devices 1310 of memory banks 1306 and 1308 each comprised of two memory devices. Ex. 1005 ¶ 56, Fig. 13; Ex. 1003 ¶ 140. We find these chip select signals correspond to the "*second chip-select signals*" in the claimed

"*wherein the first module control signals include second chip-select signals, and wherein the module control circuit is configured to generate the second chip-select signals based on the set of input address and control signals*."

Further, in Ellsberry's Figure 13, control unit ASIC 1302 receives two chip select signals CS0, CS1 and from them generates four chip select signals CS0A, CS1A, CS0B, CS1B, thus disclosing that "*the second chip-select signals having a larger number of chip select signals than the at least one first chip-select signal*."

Accordingly, Petitioner has shown that the limitations of claims 2 and 22 are disclosed by Ellsberry. We conclude that Petitioner has shown by a preponderance of the evidence that claims 2 and 22 are unpatentable as obvious over Ellsberry.

Claim 4 recites "*The memory module of claim 3, wherein the first module control signals include chip select signals, wherein the first memory devices and the second memory devices receive different chip select signals from the module control circuit*." Claims 10 and 21 recite similar limitations. Petitioner contends these features are disclosed by Ellsberry. 362 Pet. 52 (citing Ex. 1005 ¶¶ 31, Figs. 2, 5, 13; Ex. 1003 ¶¶ 222, 299–301, 370, 428–429). Referring again to Ellsberry's Figure 13, we find the "*first module control signals include chip select signals*" correspond to Ellsberry's chip select signals CS0A, CS1A, CS0B, CS1B. Duplicating Figure 13's architecture, as shown in Figure 2, Ellsberry discloses two sets of memory banks 1306, 1308 each receiving respective chip select signals CS0A, CS1A, CS0B, CS1B so that "*the first memory devices and second memory devices receive different chip select signals from the module control circuit*." We agree Ellsberry discloses the limitations recited in claims 4, 10, and 21.

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Accordingly, Petitioner has shown by a preponderance of the evidence that claim 10 is unpatentable as obvious over Ellsberry. Claim 4 depends from claim 3 and then claim 1. As we conclude subsequently in this decision that claim 3 is unpatentable as obvious, and we find that the limitation of claim 4 is disclosed by Ellsberry, we also conclude Petitioner has shown by a preponderance of the evidence that claim 4 is unpatentable as obvious.

Claim 21 depends from claim 17 and 18 and then from claim 16. We conclude subsequently in this decision that claims 17 and 18 are unpatentable as obvious subsequently in this decision, and we concluded previously that claim 16 is unpatentable as obvious over Ellsberry. As we conclude Ellsberry discloses the limitations of claim 21, we also conclude Petitioner has shown by a preponderance of the evidence that claim 21 is unpatentable as obvious over Ellsberry.

10. Claims 3, 5, 32, 33, 34, 47, 54 and 61 – Loading and Isolation

Claim 3 recites, "*The memory module of claim 1, wherein the each respective buffer circuit is configured to present one memory device load on each of the respective set of the M sets of n data lines to the memory controller*." Claim 61 is similar and recites, "*The memory module of claim 60, wherein the each respective buffer circuit is configured to present one memory device load on each data line of the respective set of the plurality of sets of data lines*." Petitioner contends the limitations recited in claims 3 and 61 are disclosed by Ellsberry. 362 Pet. 52–53 (citing Ex. 1005 ¶¶ 10, 27, 31, 46; Ex. 1003 ¶¶ 293–297; Ex. 1011, 65). Patent Owner does not contest Petitioner's assertion that Ellsberry discloses the subject matter of

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claims 3 and 61, but instead argues that Petitioner combines mutually exclusive embodiments of Ellsberry to arrive at the claimed invention. We conclude this argument is unpersuasive for the reasons stated above regarding independent claims 1 and 58 from which respective claims 3 and 61 depend.

Ellsberry states "the resistive and/or capacitive load on the bus 110 is not increased because the memory module 106 presents a single load to the bus 110, not the load of the individual memory devices coupled thereto." Ex. 1005 ¶ 27. This statement from Ellsberry discloses the limitations of claims 3 and 61. Thus, Petitioner has shown by a preponderance of the evidence that claim 3 is unpatentable as obvious over Ellsberry. Claim 61 depends from claims 59 and 60, which we subsequently determine to be unpatentable as obvious over Ellsberry, as well as independent claim 58, which we determined in a previous section to be obvious over Ellsberry. Thus, we conclude claim 61 is unpatentable as obvious over Ellsberry.

Claim 5 recites, "*The memory module of claim 1, wherein the each respective buffer circuit is configured to present a load to the respective one or more of the first memory devices that is the same as a load the memory controller would present*." Petitioner contends the limitations of claim 5 are disclosed by Ellsberry. 362 Pet. 53–54 (citing Ex. 1005 ¶¶ 44, 45, Figs.4, 9; Ex. 1003 ¶¶ 302–310; Ex. 1011, 14–15). Patent Owner does not dispute that Ellsberry discloses the limitations of claim 5, but instead argues Petitioner combines mutually exclusive embodiments, an argument we found unpersuasive above with respect to claim 1.

The parts of Ellsberry cited by Petitioner suggest the capability of the switches 206, 208 to modify the load experienced by the memory controller

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devices. Ex. 1005 ¶¶ 44, 45. We recognize that disclosing the capability alone is not sufficient; Petitioner must also show a person of ordinary skill in the art not only could have made the modification, but would have done so considering the reference. *In re Nuvasive*, 842 F.3d 1376, 1382 (Fed. Cir. 2016); *Metalcraft of Maryville, Inc. v. The Toro Co.*, 848 F.3d 1358, 1366 (Fed. Cir. 2017); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015); *KSR*, 550 U.S. at 418. Dr. Stone testifies

> the Skilled Artisan would be motivated to set the load of the bidirectional drivers 402 and 404 presented to the memory devices to be the same as the load an external memory controller would present in order to ensure that the electrical signals driven by the memory devices would behave similar to that when the memory is coupled to a memory controller and would not be distorted by a different load.

Ex. 1003 ¶ 305. We agree with Dr. Stone that a person of ordinary skill in the art would have recognized the desirability of having the switch impedance match what would be presented by the memory controller to avoid adverse signal behavior and distortion. Based on this uncontroverted evidence, we conclude claim 5 is unpatentable as obvious over Ellsberry.

Claim 32 recites

> *32. The memory module of claim 30, wherein the each respective buffer circuit is further configured to isolate memory device load associated with the respective one or more of the first memory devices and memory device load associated with the respective one or more of the second memory devices from the memory controller*.

Petitioner contends Ellsberry discloses the limitations of claim 32. 363 Pet. 48 (citing Ex. 1005 ¶¶ 12, 27, 31, 45; Ex. 1003 ¶¶ 247–250, 481–482; Ex. 1035, 68, 74, 75, 133, Figs. 2.28, 4.7). Patent Owner does not dispute

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that Ellsberry discloses the limitations of claim 32, but instead argues Petitioner combines mutually exclusive embodiments of Ellsberry, an argument we rejected above with respect to independent claim 30. We agree that Petitioner has shown by a preponderance of the evidence, for the reasons noted, that claim 32 is unpatentable as obvious over Ellsberry.

Claim 33 recites, "*The memory module of claim 32, wherein the each respective buffer circuit is configured to present to the memory controller one memory device load on each data signal line of the respective set of the plurality of sets of data signal lines*." Claims 47 and 54 recite similar limitations. Petitioner contends Ellsberry discloses the limitations of claims 33, 47, and 54. 363 Pet. 49–50 (citing Ex. 1005 ¶¶ 10, 27, 31, 46; Ex. 1003 ¶¶ 293–297, 484, 547–548, 585–586; Ex. 1011, 65). Patent Owner does not dispute that Ellsberry discloses the limitations of claims 33, 47, and 54, but argues one of ordinary skill in the art would not have combined mutually exclusive embodiments, an argument we found unpersuasive with respect to independent claims 30, 43, and 53, from which these claims depend. We agree Ellsberry discloses the limitations of claims 33, 47, and 54. Ex. 1005 ¶ 27. Thus, on the full record before us, we determine Petitioner has shown by a preponderance of the evidence that claims 33, 47, and 54 are unpatentable as obvious over Ellsberry.

Claim 34 recites

> *34. The memory module of claim 32, wherein the each respective buffer circuit is configured to present a load that is the same as a load the memory controller would present to the respective one or more of the first memory devices and subsequently to the respective one or more of the second memory devices*.

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Petitioner contends Ellsberry discloses the subject matter of claim 34. 363 Pet. 50–51 (citing Ex. 1005 ¶¶ 44, 45, Figs. 2, 9; Ex. 1003 ¶¶ 302–310, 485, 486; Ex. 1011, 14–15). Patent Owner does not dispute that Ellsberry discloses the subject matter of claim 34, but contends Petitioner combines mutually exclusive embodiments, an argument we found unpersuasive with respect to claim 30, from which claim 34 depends.

Specifically, Ellsberry states that the "squelch function allows the memory devices to be configured to operate in conjunction with the controller/switch devices and host system, rather than be directly programmed by the host system." Ex. 1005 ¶ 44. Dr. Stone testifies that a person of ordinary skill in the art would have been motivated to set the load of the bidirectional drivers 402 and 404 of Ellsberry's Figure 4 to be the same as presented by the external memory controller to avoid adverse signal behavior and distortion. Ex. 1003 ¶ 305. Based on this uncontroverted evidence, we determine Petitioner has demonstrated by a preponderance of the evidence that claim 34 is unpatentable as obvious over Ellsberry.

11. Claims 6, 15, 29, 35, 37, 42, 50, 51, 55, 56 and 63 – n or Eight Bits Wide

Claim 6 recites, "*The memory module of claim 1, wherein the each respective buffer circuit has a first data width of n bits, and wherein each of the plurality of memory devices has a second data width different from the first data width*." Petitioner contends Ellsberry discloses the subject matter of claim 6. 362 Pet. 54–55 (citing Ex. 1005 ¶¶ 30, 39, 52, Figs. 2, 11; Ex. 1003 ¶¶ 226, 230, 232–235, 312–315; Ex. 1010, 12, 15). Patent Owner does not contend Ellsberry fails to disclose the subject matter of claim 6, but instead argues Petitioner combines mutually exclusive embodiments, an

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argument we rejected with respect to claims 1, 16, and 58, from which respective claims 6, 15, 29, and 63 depend. PO Resp. 9–61. Patent Owner also argues that Petitioner failed to provide the requisite particularity for the Ellsberry embodiment mapped to the claims in the 362 and 363 Petitions. PO Resp. 61–82.

Ellsberry's Figure 11 is shown below:

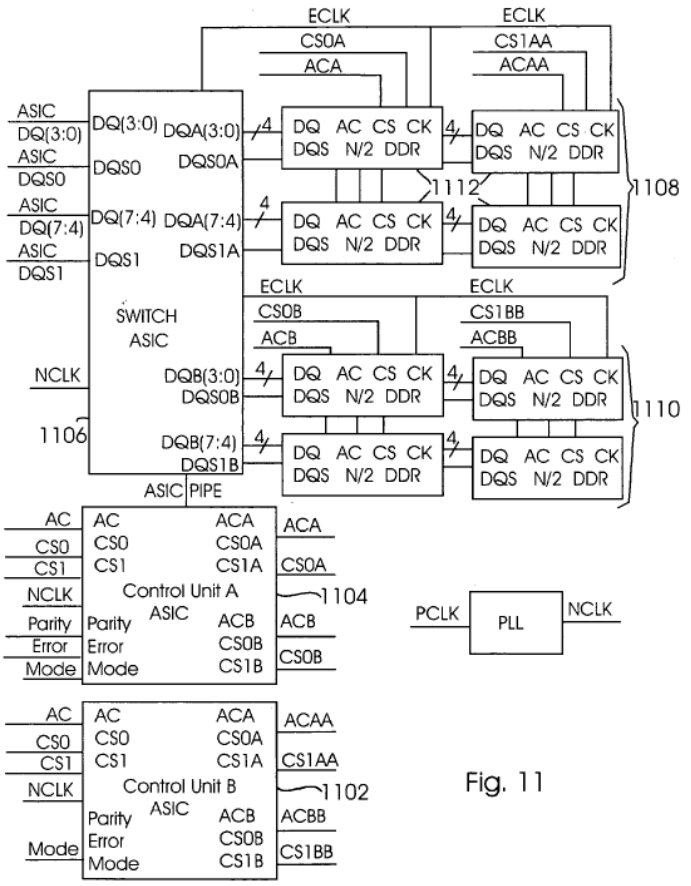


Fig. 11

Figure 11 shows part of a memory module with memory banks having four-bit memory devices

Ellsberry's Figure 11, above, shows that each port of switch 1106 receives two four-bit lines from pairs of four-bit memory devices of memory banks 1108 and 1110. Ex. 1005 ¶ 54, Fig. 11; Ex. 1003 ¶¶ 313–314. Thus, the switch 1106 discloses "*buffer circuit has a first data width of n bits*" where n

equals eight bits, and the memory devices have "*a second data width different from the first data width*," namely, a width of four bits. Accordingly, on the full record before us, we determine that Petitioner has shown by a preponderance of the evidence that claim 6 is unpatentable as obvious over Ellsberry.

Claim 15 recites, "*The memory module of claim 1, wherein the M buffer circuits are byte-wise buffer circuits, and wherein each set of the M sets of n data signal lines is eight bits wide*." Claims 29 and 63 recite the same limitations. Petitioner contends Ellsberry discloses the limitations of claims 15, 29, and 63 for the reasons given for claim 6, and also because Ellsberry discloses each bank switch transfers one byte at a time and thus discloses "*byte-wise buffer circuits*" and "*each set of . . . data signal lines is eight bits wide*" as claimed. 362 Pet. 55–56 (citing Ex. 1005, Fig. 2; Ex. 1003 ¶¶ 391–392, 444–445, 622–623. We agree with Petitioner that Ellsberry discloses the limitations of claims 15 and 29, rendering them obvious over Ellsberry. Claim 63 depends from claims 58–60 and 62. As we concluded previously that claim 58 is unpatentable as obvious over Ellsberry, and we conclude in a subsequent section of this decision that claims 59, 60, and 62 are unpatentable as obvious over Ellsberry, considering these claims as a whole, we likewise conclude claim 63 is unpatentable as obvious over Ellsberry.

Claim 35 recites, "*The memory module of claim 30, wherein the plurality of buffer circuits are byte-wise buffer circuits, and wherein each set of the plurality of sets of data signal lines is eight bits wide*." Claims 42, 50, and 55 recite the same limitation. Petitioner contends that Ellsberry discloses the limitations of claims 35, 42, 50, and 55. 363 Pet. 51 (citing Ex.

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1005 ¶¶ 29, 30, Fig. 2; Ex. 1003 ¶¶ 226, 230, 232–235, 312, 392, 487, 488, 513, 514, 556, 557, 587, 588). Patent Owner does not contest that Ellsberry discloses the limitations of claims 35, 42, 50, and 55. Ellsberry's Figure 2 shows that each of the data buses 230, 232 has a one-byte width, as do the buffers of switches 206, 208 that transfer data from the DIMM interface 202 to the memory banks 212–228, and vice versa. Accordingly, Petitioner has shown by a preponderance of the evidence that claims 35, 42, 50, and 55 are unpatentable as obvious over Ellsberry.

Claim 37 recites

> *37. The memory module of claim 30, wherein each of the memory devices is n-bit wide, wherein the respective one or more of the first memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a single memory device receiving the respective n-bit section of the each N-bit wide data signal associated with the second write command.*

Claim 51 recites

> *51. The memory module of claim 50, wherein each of the memory devices is eight bits wide, wherein the one or more memory devices in the subset of the memory devices include a single memory device outputting or receiving the respective portion of the data associated with the memory read or write command*.

Claim 56 recites

> *56. The memory module of claim 55, wherein each of the memory devices is eight bits wide, wherein the one or more of the first memory devices include a single memory device outputting or receiving the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command*.

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Petitioner contends that the limitations of claims 37, 51, and 56 are disclosed by Ellsberry. 363 Pet. 55–56 (citing Ex. 1005 Figs. 2, 5, 13; Ex. 1003 ¶¶ 241–245, 280–291, 373). Patent Owner does not dispute that Ellsberry discloses the limitations of claims 37, 51, and 56, but contends that Petitioner mixes mutually exclusive embodiments (PO Resp. 9–61), an argument we rejected with respect to independent claims 30, 43, and 53.

Regarding claim 37, Ellsberry's Figure 13, discussed *supra*, shows 8-bit memory devices connected in banks to Port A and Port B of switch 1304. Control unit 1302 may control the switch to write one 8-bit data into one of the memory devices at Port A and another 8-bit data to another of the memory devices at Port B of switch 1302. Ex. 1003 ¶¶ 372–374. Thus, Petitioner demonstrates that the limitation of claim 37 is disclosed by Ellsberry.

Regarding claim 51, Ellsberry's Figure 13, when incorporated into Ellsberry's Figure 2, shows that each of the memory devices is eight bits wide, and together with other memory devices outputs or receives an 8 x N bit wide data signal associated with a read or write command. We agree this discloses the limitation of claim 51. For the same reasons, we also agree Ellsberry discloses the limitation of claim 56.

Accordingly, Petitioner shows by a preponderance of the evidence that claims 37, 51, and 56 are unpatentable as obvious over Ellsberry.

12. Claims 7, 19, and 24 – Data Flow Direction

Claim 7 of the '907 patent recites, "*The memory module of claim 1, wherein the second module control signals indicate a direction of data flow through the buffer circuits*." Claims 19 and 24 recite the same limitation but

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depend directly or indirectly from claim 16. Petitioner contends Ellsberry discloses the limitations of claims 7, 19, and 24. 362 Pet. 56–58 (citing Ex. 1005 ¶¶ 39, 45, 47, Figs. 3, 4; Ex. 1003 ¶¶ 318–320; Ex. 1035, Fig. 4.7; Ex. 1006, 5:23–39, Fig. 4). Ellsberry's Figure 4 is shown below:

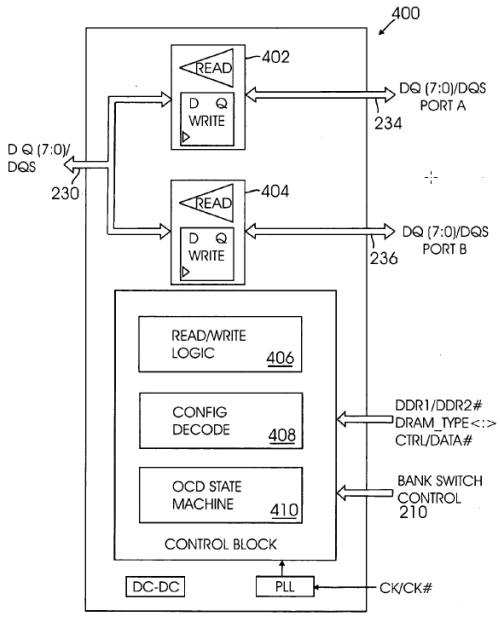


Fig. 4

Figure 4 shows data processing system 400 with bidirectional signal drivers 402, 404 that transmit and receive data over buses 230, 234, 236.

Specifically, Ellsberry states "address and command processing system 300 may be implemented as part of the control unit 204." Ex. 1005 ¶ 39. Ellsberry also states "command processing system 300 controls physical bank selected and bank switching direction." *Id.* Thus, Ellsberry discloses "*the second module control signals indicate a direction of data flow*" as recited in claims 7, 19, and 24. Further, Petitioner contends that Ellsberry's read/write logic unit 406, which is part of memory bank switch 206, determines whether data is read from or written to the memory devices, and thus discloses the "*direction of data flow through the buffer circuits*." Ex.

1005 ¶¶ 45, 47, Fig. 4. Thus, Petitioner has shown by a preponderance of the evidence that the limitations of claims 7 and 24 are disclosed by Ellsberry. We conclude elsewhere in this decision that the claims from which claims 7, 19, and 24 depend are unpatentable as obvious over Ellsberry. We likewise conclude Petitioner has shown by a preponderance of the evidence that dependent claims 7, 19, and 24 are unpatentable as obvious over Ellsberry.

13. Claims 8, 20, 25, and 31

Claim 8 recites, "*The memory module of claim 1, wherein the module control circuit is further configured to control the timing of each N-bit wide data signal associated with the memory read or write command using the second module control signals in accordance with a latency parameter*." Claims 20 and 25 recite similar limitations. Petitioner contends the limitations of these claims are disclosed by Ellsberry. 362 Pet. 58–59 (citing Ex. 1005 ¶¶ 10, 29, 31, 42, 44, 46, 50, Figs. 3, 4, 8A, 9; Ex. 1003 ¶¶ 327–342, 426, 427, 436, 437; Ex. 1009, 8–10; Ex. 1011, 12, 22, 23).

The term "latency" is nowhere mentioned in Ellsberry. Dr. Stone testifies that the "Posted CAS_n" parameter in Ellsberry's Figure 9 is an '"[a]dditive latency" parameter, which is used for timing read and write operations." Ex. 1003 ¶ 330. Dr. Stone further testifies that EMRS (Extended Mode Register Set) may include a latency parameter as defined under the JEDEC standard (Ex. 1011). Ex. 1003 ¶¶ 329, 333, 334, 336. Although Petitioner's challenge does not combine the JEDEC standard with Ellsberry, we note that one reference may be used to explain how a person of ordinary skill in the art would have understood terminology used in another

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reference relied upon to disclose the claim elements in an obviousness challenge. *Realtime Data, LLC v. Iancu*, 912 F.3d 1368, 1373 (Fed. Cir. 2019). Considering Ellsberry in light of Dr. Stone's testimony and the JEDEC standard (Ex. 1011), we determine that Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would have considered claims 8, 20, and 25 obvious over Ellsberry.

Claim 31 recites, "*The memory module of claim 30, wherein the data paths in the each respective buffer circuit are configured in accordance with a latency parameter when the logic is responding to the first module control signals and when the logic is responding to the second module control signals*." Petitioner contends the limitations of this claim are disclosed by Ellsberry. 363 Pet. 46–47 (citing Ex. 1005 ¶¶ 29, 42, 44, 46, 50, Figs. 8A, 9; Ex. 1003 ¶¶ 327–336, 403–408, 478–479; Ex. 1011, 12, 22, 23). For the same reasons as stated above with respect to claims 8, 20, and 25, Petitioner has shown that Ellsberry discloses the limitation of claim 31 when considered in light of Dr. Stone's testimony and the JEDEC standard (Ex. 1011). Accordingly, Petitioner has shown by a preponderance of the evidence that claim 31 is unpatentable as obvious over Ellsberry.

14. Claims 9, 13, 23, 28, 36, and 59

Claims 9, 28, and 36 recite that the

> *[module] control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices*

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> *coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections*.

Claims 13, 23 and 59 recite "*module signal lines . . . coupling respective input/output connections on the module control circuit to corresponding input/output connections on respective subsets . . . of memory devices*." Petitioner contends Ellsberry discloses the limitations of claims 9, 13, 23, 28, 36, and 59. 362 Pet. 59–62 (citing Ex. 1003 ¶¶ 215–223, 344–369, 380–381, 432–443, 614–615; Ex. 1005 ¶¶ 3, 23, 30–36, 39, 42–44, 46–50, Figs. 2, 3, 5, 8A–8B; Ex. 1037, 4:34–38; Ex. 1011, 1, 6, 46; Ex. 1010, 6, 19; Ex. 1042, 3–5, 72); 363 Pet. 52–54 (citing Ex. 1005 ¶¶ 3, 23, 30–36, 39, 42–44, 46–50, Figs. 2, 3, 5, 8A, 8B, Ex. 1003 ¶¶ 215–223, 344–353, 365–368, 489, 490; Ex. 1037, 4:34–38; Ex. 1011, 1, 6, 46; Ex. 1010, 6, 19; Ex. 1042, 3–5, 72) . Patent Owner does not contest that Ellsberry discloses the claimed limitations. *See generally* PO Resp.

Ellsberry's Figure 13, *supra*, shows connections for various signals from control unit ASIC 1302 to memory devices 1310. These connections include those for addresses ACA, ACB, chip select signals CS0A, CS1A, CS0B, CS1B, and these connections can be grouped into the claimed first through fourth connections between the control unit and memory devices, as recited in claims 9 and 28. Ex. 1005 ¶¶ 52, 56, Fig. 13; Ex. 1003 ¶ 140. These connections also constitute "*module signal lines*" in claims 13, 23, and 59. We agree Ellsberry discloses the subject matter of claims 9, 13, 23, and 56. Thus, Petitioner has shown by a preponderance of the evidence that claims 9, 13, 23, and 59 are unpatentable as obvious over Ellsberry. Claim 23 depends on claims 17 and 18, which we conclude in a later section of this decision are unpatentable as obvious over Ellsberry, as well as claim 16,

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which we previously determined to be unpatentable as obvious. Accordingly, we likewise determine on the full record before us that Petitioner has shown by a preponderance of the evidence that claim 23 is unpatentable as obvious over Ellsberry.

15. Claims 11, 26, and 64

Claim 11 recites, "*The memory module of claim 1, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command*." Claim 26 is identical to claim 11. Claim 64 recites

> *64. The memory module of claim 63, wherein each of the memory devices is eight bits wide, wherein the respective one or more of the first memory devices include a single memory device outputting or receiving the respective portion of the data associated with the first memory read or write command*.

Petitioner contends the limitations of claims 11, 26, and 64 would have been obvious over Ellsberry. 362 Pet. 63 (citing Ex. 1005 Fig. 2, 5, 13; Ex. 1003 ¶¶ 244, 280–291, 372–374, 438–439, 624–625).

Petitioner contends when Ellsberry's Figure 13, *supra*, is used in the module of Figures 2 and 5, any one of the memory devices, when activated, outputs or receives eight bits of data (one byte) which is an "*n-bit section of the each N-bit wide data signal*." 362 Pet. 63. We agree with Petitioner's contention. Petitioner has shown by a preponderance of the evidence that claims 11, 26, and 64 are disclosed by Ellsberry. We conclude elsewhere in this decision that the claims from which claims 11, 26, and 64 depend are unpatentable as obvious over Ellsberry. We likewise conclude Petitioner has

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shown by a preponderance of the evidence that claims 11, 26, and 64 are unpatentable as obvious over Ellsberry.

16. Claims 12, 27, 38, 52, 57, and 65 – n/2 or Four-Bits Wide

Claim 12 recites, "*The memory module of claim 1, wherein the respective one or more of the first memory devices include a pair of memory devices each outputting or receiving half of the respective n-bit section of the each N-bit wide data signal associated with the memory read or write command*." Claims 27 and 65 recite similar limitations. Petitioner contends Ellsberry discloses the limitations of claims 12, 27, and 65. 362 Pet. 63–64 (Ex. 1005, Fig. 2, 6, 11; Ex. 1003 ¶¶ 375–379, 440–441, 626–627). Patent Owner argues Petitioner fails to provide the required degree of particularity to show claims 12, 27, and 65 are obvious. PO Resp. 61–82. We address Patent Owner's argument concerning particularity in a subsequent section of this decision.

Ellsberry's Figure 11, *supra*, when used in the module of Figures 2 and 6, shows pairs of memory devices with a data bit-width of four-bits, so the pair has a combined width of eight bits, equal to the bit width of the bank switch. Accordingly, Petitioner has shown by a preponderance of the evidence that Ellsberry discloses the limitations of claims 12, 27, and 65. We conclude elsewhere in this decision that Petitioner has shown by a preponderance of the evidence that the claims from which claims 12, 27, and 65 depend are unpatentable as obvious over Ellsberry. We likewise conclude Petitioner has shown by a preponderance of the evidence that claims 12, 27, and 65 are unpatentable as obvious over Ellsberry

Claim 38 recites

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> *38. The memory module of claim 30, wherein each of the memory devices is n/2-bit wide, wherein the respective one or more of the first memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the first write command, and wherein the respective one or more of the second memory devices include a pair of memory devices each receiving half of the respective n-bit section of the each N-bit wide data signal associated with the second write command*.

Claim 52 recites

> *52. The memory module of claim 50, wherein each of the memory devices is four bits wide, wherein the one or more memory devices in the subset of the memory devices include a pair of memory devices each outputting or receiving half of the respective portion of the data associated with the memory read or write command*.

Claim 57 recites

> *57. The memory module of claim 55, wherein each of the memory devices is four bits wide, wherein the one or more of the first memory devices include a pair of memory devices each outputting or receiving 4 bits of the respective 8-bit section of each N-bit wide data signal associated with the memory read or write command*.

Petitioner contends Ellsberry discloses the limitations of claims 38, 52, and 57. 363 Pet. 56–57 (citing Ex. 1005 Figs. 2, 6, 11; Ex. 1003 ¶¶ 138–152, 241–245, 375–379, 493, 494, 560, 561, 591, 592). Patent Owner argues Petitioner fails to provide the required degree of particularity to show claims 32, 52, and 57 are obvious, which we address in a subsequent section.

With respect to claim 38, Ellsberry's Figure 11, *supra*, shows that each of the memory devices is four bits (n/2) wide, and pairs of memory devices provide eight bits (n) wide, and a first pair of memory devices

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connected to Port A of the switch receives n-bit wide data associated with a first write command, and a second pair of memory devices connected to Port B of the switch receives n-bit wide data associated with a second write command. Ex. 1003 ¶¶ 375–379. Accordingly, on the full record before us, Petitioner has shown by a preponderance of the evidence that claim 38 is unpatentable as obvious over Ellsberry.

With respect to claim 52, Ellsberry's Figure 11, *supra*, shows memory devices that are four-bits wide arranged in pairs that are eight-bits wide, each outputting or receiving half of the data for a read or write command. Thus, Petitioner shows that Ellsberry discloses claim 52. Elsewhere in this decision, we determine Petitioner has shown by a preponderance of the evidence that the claims from which claim 52 depends are unpatentable as obvious over Ellsberry. We likewise conclude that Petitioner has shown by a preponderance of the evidence that claim 52 is unpatentable as obvious over Ellsberry.

With respect to claim 57, Ellsberry's Figure 11, *supra*, discloses pairs of memory devices four bits wide each receiving or outputting four-bit data for a combined eight-bit data associated with a read or write command. When Figure 11 is incorporated with Ellsberry's Figure 2, Ellsberry discloses outputting or receiving an "*N-bit wide data signal*" (Nx8 bits wide in Ellsberry's Figure 2). We determine elsewhere in this decision that Petitioner has shown by a preponderance of the evidence that the claims from which claim 57 depends are unpatentable as obvious over Ellsberry. Thus, on the full record before us, Petitioner has shown by a preponderance of the evidence that claim 57 is unpatentable as obvious over Ellsberry.

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17. Claims 14, 17, 18, 39, 40, 41, 45, 46, 48, 49, 60, and 62 – buffers

Claim 14 recites, "*The memory module of claim 1, wherein the first memory read or write command is a memory write command, and wherein the each respective buffer circuit includes tristate buffers controlled by the logic to transmit the respective n-bit section of the each N-bit wide data signal associated with the memory write command to the respective one or more of the first memory devices*." Petitioner contends Ellsberry discloses the limitations of claim 14. 362 Pet. 64–65 (citing Ex. 1005 ¶¶ 31, 45, Figs. 4, 8A; Ex. 1003 ¶¶ 240–246, 383–388; Ex. 1035, 117). Patent Owner does not dispute that Ellsberry discloses the limitations of claim 14, other than to contend Petitioner combines mutually exclusive embodiments of Ellsberry. PO Resp. 9–61. For reasons explained with respect to claims 1, 16, and 58, we do not agree with Patent Owner's argument.

Petitioner contends Ellsberry discloses a "*memory write command*" and transmitting an "*n-bit section of the each N-bit wide data signal*" to the "*memory devices*." 362 Pet. 64–65; Ex. 1005 ¶¶ 31, 45, Figs. 4, 8A. Petitioner asserts it would have been obvious to implement bidirectional memory bus drivers 402, 404 (Fig. 4) using "*tristate buffers*." 362 Pet. 64. Dr. Stone testifies that it would have been obvious to implement Ellsberry's bidirectional drivers 402, 404 using tri-state buffers, and he cites his textbook as support for this proposition. Ex. 1003 ¶ 385; Ex. 1035, 117. Figure 4.7 from Dr. Stone's textbook is provided below:

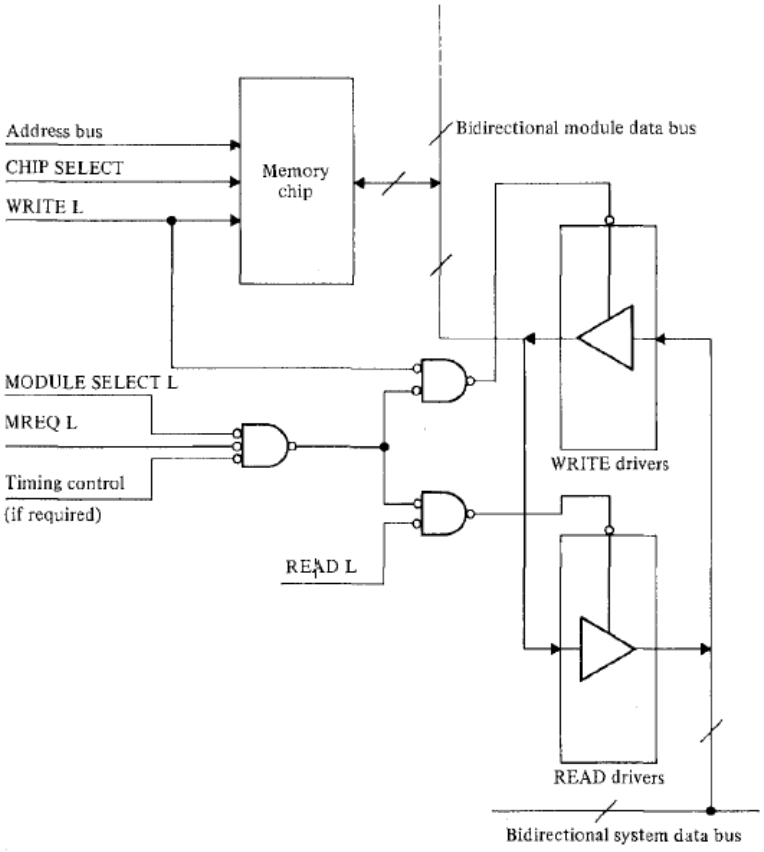


FIGURE 4.7 Tri-state driver control for interfacing memory chips to bidirectional data lines.

Stone's Figure 4.7 shows bidirectional drivers connected to a system data bus and memory chip.

The right side of Figure 4.7 shows "WRITE drivers" and "READ drivers" that together constitute bidirectional drivers. The WRITE drivers and READ drivers are depicted as tri-state buffers including input terminals, output terminals, and enable terminals used to enable or disable the tri-state buffer, causing it to enter a high-impedance state when disabled. Ex. 1003 ¶ 387.

Although Petitioner's challenge does not combine Dr. Stone's textbook with Ellsberry, we note that one reference may be used to explain how a person of ordinary skill in the art would have understood terminology used in another reference relied upon to disclose the claim elements in an

obviousness challenge. *See Realtime Data*, 912 F.3d at 1373. Here, Petitioner uses Dr. Stone's textbook to explain what specifically Ellsberry means, in the context of the '907 patent's reference to tri-state buffers, when it refers to bidirectional drivers. 362 Pet. 64–65; 363 Pet. 57–58. Thus, Petitioner has shown that Ellsberry's bidirectional drivers disclose the claimed tri-state buffers. On the full record before us, we determine that Petitioner demonstrates by a preponderance of the evidence that claim 14 is unpatentable as obvious over Ellsberry.

Claim 17 recites, "*The memory module of claim 16, wherein the data paths include write data paths, each write data path including at least one tristate buffer controlled by the logic*." Claim 60 recites the same limitation. Claim 18 recites, "*The memory module of claim 17, wherein the data paths further include read data paths, each read data path including a tristate buffer controlled by the logic*." Claim 62 recites the same limitation.

Petitioner contends Ellsberry discloses the limitations of claims 17, 18, 60, and 62. 362 Pet. 70 (citing Ex. 1005 Fig. 4; Ex. 1003 ¶¶ 403–408, 415–423). Petitioner refers back to arguments made with respect to claim 14 as support for its contention. For the reasons explained above, we agree with Petitioner that Ellsberry's bidirectional drivers disclose the claimed tri-state buffers. On the full record before us, Petitioner shows by a preponderance of the evidence that claims 17, 18, 60, and 62 would have been obvious to a person of ordinary skill in the art.

Claim 39 recites

> *39. The memory module of claim 30, wherein the each respective buffer circuit includes input buffers to receive the respective n-bit section of the each N-bit wide data signal associated with the first write command from the memory controller, wherein each*

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> *of the input buffers is comparable in loading to an input buffer on one of the memory devices*.

Petitioner contends Ellsberry discloses claim 39. 363 Pet. 57–58 (citing Ex. 1005 ¶¶ 10, 31, 45, 46; Ex. 1003 ¶¶ 242, 292–298, 386–388, 496, 497; Ex. 1011, 65; Ex. 1035, 117). Patent Owner does not dispute Ellsberry discloses the limitations of claim 39, but contends Petitioner combines mutually exclusive embodiments of Ellsberry, an argument we rejected with respect to claim 30 from which claim 39 depends.

Ellsberry's Figure 4 shows bidirectional signal drivers 402, 404 including D-flip-flops with inputs (the claimed "*input buffers*") associated with a write command that receive eight bits of the Nx8-bit wide data signal, as shown in Ellsberry's Figure 2. Ex. 1005 ¶ 45. Ellsberry further states the signal drivers "reduce[] resistive and/or capacitive loading of the data bus coupled to the DIMM interface and the bus 110 while emulating a standard memory device interface." Ex. 1005 ¶ 31. Also, Figure 4.7 of Dr. Stone's textbook shows bidirectional drivers including WRITE drivers that could be construed as the claimed "*input buffers*." Ex. 1035, 133. Thus, Petitioner shows by a preponderance of the evidence that claim 39 is unpatentable as obvious over Ellsberry.

Claim 40 recites

> *40. The memory module of claim 39, wherein the each respective buffer circuit further includes output buffers to drive the respective n-bit section of the each N-bit wide data signal associated with the first write command to the respective one or more of the first memory devices, wherein each of the output buffers is comparable in loading to an output buffer on the memory controller*.

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Petitioner contends Ellsberry discloses the limitations of claim 40. 363 Pet. 59 (Ex. 1003 ¶¶ 242, 302–310, 382–390, 502–505). Patent Owner does not dispute Ellsberry discloses the limitations of claim 40, but contends Petitioner combines mutually exclusive embodiments of Ellsberry, an argument we rejected with respect to claim 30 from which claim 40 depends.

Reviewing the evidence concerning claim 40, we determine Petitioner has not shown bidirectional signal drivers 402, 404 include both input buffers (as recited in claim 39 from which claim 40 depends) and output buffers (as recited in claim 40), that are both associated with a write command, as claimed. Specifically, Petitioner does not show where in Ellsberry's Figure 4 the bidirectional signal drivers 402, 404 or the D-flip-flops therein (which are identified in Figure 4 as associated with a write command) include both input and output buffers. Neither the '363 Petition nor Dr. Stone present evidence showing that Ellsberry discloses this feature. Accordingly, we conclude Petitioner has not shown by a preponderance of the evidence that claim 40 is unpatentable as obvious over Ellsberry.

Claim 41 recites

> *41. The memory module of claim 40, wherein the output buffers regenerate the respective n-bit section of the each N-bit wide data signal associated with the first write command to restore desired signal waveform shapes in the respective n-bit section of the each N-bit wide data signal associated with the first write command.*

Petitioner contends Ellsberry discloses the limitations of claim 41. 363 Pet. 60–61 (citing Ex. 1005 Fig. 4; Ex. 1003 ¶¶ 385–389, 507–512; Ex. 1035, 74, 96). Claim 41 depends from claim 40, and for similar reasons, we conclude Petitioner has not shown Ellsberry discloses the claimed feature of input buffers and output buffers both associated with a write command. Neither the '363 Petition nor Dr. Stone present evidence showing that the Ellsberry

discloses input buffers and output buffers that are associated with a write command. Accordingly, we conclude Petitioner has not shown by a preponderance of the evidence that claim 41 is unpatentable as obvious over Ellsberry.

Claim 45 recites, "*The memory module of claim 43, wherein the data paths include write data paths, and wherein the write data paths include tristate buffers controlled by the logic*." Claim 48 recites the same limitation. Petitioner contends the limitations of claims 45 and 48 are disclosed by Ellsberry. 363 Pet. 69 (Ex. 1005 Fig. 4; Ex. 1003 ¶¶ 382–390, 403–408, 415–423). Petitioner has shown that Ellsberry's bidirectional drivers include the claimed "*tristate buffers*." *See* Ex. 1035 Fig. 4.7, *supra*. Accordingly, we conclude Petitioner has shown by a preponderance of the evidence that claims 45 and 48 are unpatentable as obvious over Ellsberry.

Claim 46 recites

> *46. The memory module of claim 45, wherein the memory read or write command is a memory write command, and wherein the tn state buffers regenerate signals carrying the respective portion of the data associated with the memory read or write command received from the memory controller to restore signal waveform shapes, and transmit regenerated signals to the respective one or more of the subset of the memory devices*.

Claim 49 recites the same limitation. Petitioner contends Ellsberry discloses the limitations of claims 46 and 49. 363 Pet. 70 (citing Ex. 1005 ¶¶ 45; Ex. 1003 ¶¶ 544, 507–512, 542–546, 554). Claims 46 and 49 recite "*tn state buffers*" which we interpret to mean the "*tristate buffers*" referenced earlier in claim 45 from which claims 46 and 49 depend.[13] Petitioner demonstrates

[13] A district court may "correct an error in a patent by interpretation of the patent where no certificate of correction has been issued . . . only if (1) the correction is not subject to reasonable debate based on consideration of the

tristate buffers are disclosed by Ellsberry's bidirectional drivers in light of Dr. Stone's textbook. *See* Ex. 1035, Fig. 4.7, *supra*. Tristate buffers perform the function of regenerating and restoring data. Ex. 1003 ¶ 545. Accordingly, on the full record before us, we determine Petitioner has shown by a preponderance of the evidence that claims 46 and 49 are unpatentable as obvious over Ellsberry.

18. Claim 44

Claim 44 recites

> *44. The memory module of claim 43, wherein the set of module control signals are further dependent on whether the memory read or write command is a memory read command or a memory write command, and wherein the logic configures the data paths differently depending on whether the memory read or write command is a memory read command or a memory write command.*

Petitioner contends Ellsberry discloses the limitation of claim 44. 363 Pet. 67–69 (citing Ex. 1005 ¶¶ 39–45, 47, Figs. 3, 4; Ex. 1006 Fig. 4, 5:23–39; Ex. 1003 ¶¶ 318–320, 538; Ex. 1035 Fig. 4.7). Patent Owner does not argue that Ellsberry fails to disclose the limitation of claim 44, only that Petitioner improperly combines mutually exclusive embodiments of Ellsberry, an argument we rejected with respect to independent claim 43.

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claim language and the specification and (2) the prosecution history does not suggest a different interpretation of the claims." *Novo Indus., LP v. Micro Molds Corp*., 350 F.3d 1348, 1354 (Fed. Cir. 2003). We have applied this same standard in our proceedings. *E.g*., *Apple Inc. v. Achates Reference Publ'g, Inc.*, Case IPR2013-00080, slip op at 10–12 (PTAB June 3, 2013) (Paper 22).

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Ellsberry's Figure 4, *supra*, shows data buses (i.e., "paths") 230, 234, 236 connected to bidirectional signal drivers 402, 404. Ex. 1005 ¶ 45. Also, Ellsberry's Figure 4 shows a "control block" with read/write logic 406, which "determines whether data is being read from or written to the memory devices (e.g., 212)," and memory configuration information 408 obtained from the control unit (see control information "CTRL" entering the control block). *Id.* Dr. Stone testifies the "logic of the bank switches configures the data paths of the bidirectional drivers appropriately for either a read or write," and thus discloses the claimed "*wherein the logic configures the data paths differently depending on whether the memory read or write command is a memory read command or a memory write command*." Ex. 1003 ¶ 538. We determine Petitioner shows by a preponderance of the evidence on the full record before us that claim 44 is unpatentable as obvious over Ellsberry.

19. Patent Owner's Argument Concerning Particularity of the 362 and 363 Petitions with respect to the Four-Bit Patent Claims

Title 35 U.S.C. § 312(a)(3) provides that a petition must identify "in writing and ***with particularity***, each claim challenged, the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim." (Emphasis added). Further, as Patent Owner notes (PO Resp. 64), 37 C.F.R. § 42.104(b)(4) provides that "[t]he petition must specify where each element of the claim is found in the prior art patents or printed publications relied upon," and 37 C.F.R. § 42.104(b)(5) adds that the petition must "identify[] specific portions of the evidence that support the challenge." Also, 37 C.F.R. § 42.22(a)(2) provides that a petition "must include . . . [a] full statement of the reasons for the

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relief requested, including a detailed explanation of the significance of the evidence."

Patent Owner argues that Petitioner has failed to meet the requirements of 35 U.S.C. § 312(a)(3), 37 C.F.R. § 42.104(b), and 37 C.F.R. § 42.22(a). Specifically, Patent Owner argues Petitioner uses Ellsberry to manufacture a "first embodiment" using eight-bit memory devices (Figures 2, 5, and 13) and a "second embodiment" using four-bit memory devices (Figures 2, 6, and 11) to disclose the '907 patent's claims. PO Resp. 61–82. Patent Owner argues Petitioner fails to show how Petitioner's second embodiment discloses the limitations of the independent claims, and therefore alleges Petitioner's mappings fail for all claims reciting four-bit memory devices, which allegedly includes claims 6, 12, 15, 27, 29, 35, 38, 42, 50, 52, 55, 57, 63, and 65. *Id.*

Petitioner contends a person of ordinary skill in the art would have combined Ellsberry's Figures 2, 5, and 13 for the eight-bit memory device, or would have combined Ellsberry's Figures 2, 6, and 11 for the four-bit memory device, because of their inclusion in the same patent application, and because Ellsberry specifically relates them to each other. 362 Pet. 23–24; 363 Pet. 23–24; Corr. Reply 49–50. We agree with Petitioner's contention. For example, in reference to Figures 10, 11, 12, and 13, Ellsberry states "[t]hese configurations employ the control unit and bank switch previously described," thus relating these figures to the earlier-described control units and switches (including Figures 2, 5, and 6). Ex. 1005 ¶ 52. As another example, Ellsberry's Figures 5 and 6 are described together, and the description of Ellsberry's Figure 5 refers back to previously described operation of the memory controller and memory bank

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switch (i.e., the discussion of their operation with respect to Ellsberry's Figure 2). Ex. 1005 ¶¶ 47–49. Ellsberry also states "[t]he appearances of the phrase 'in one embodiment' or 'an embodiment' in various places in the specification are not necessarily all referring to the same embodiment." Ex. 1005 ¶ 22. Use of the phrase "not necessarily" suggests different mentions of the word "embodiment" may be referring to the same embodiment, a fact that Patent Owner does not acknowledge or address.

We do not agree with Patent Owner's argument that Petitioner was required to show the "second embodiment" with four-bit memory devices discloses the independent claims before Petitioner could show the "second embodiment" discloses any dependent claim reciting a four-bit embodiment. PO Resp. 65–66. Instead, what is required is to show the subject matter of a challenged claim is obvious over the prior art. *Ericsson Inc. v. Intellectual Ventures I LLC*, 890 F.3d 1336, 1338 (Fed. Cir. 2018). Patent Owner's argument also fails to consider that Ellsberry's Figure 2 and corresponding description are common to both the "first embodiment" and "second embodiment" and thus share disclosure used to demonstrate unpatentability of the independent claims which is not specific to the four-bit embodiment. Patent Owner's argument further fails to consider prior art embodiments may be properly combinable in the obviousness analysis as long as there is a reason that a person of ordinary skill in the art would have combined them, such as the case here where those embodiments are included in the same patent application and specifically refer to one another therein. *Boston Scientific Scimed, Inc. v. Cordis Corp.*, 554 F.3d 982, 991 (Fed. Cir. 2009) ("Combining two embodiments disclosed adjacent to each other in a prior art patent does not require a leap of inventiveness."). Furthermore, Patent

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Owner's argument effectively would require the four-bit dependent claim to be incorporated into its independent claim before reading the claim on the prior art. However, under the doctrine of claim differentiation, "the presence of a dependent claim that adds a particular limitation raises a presumption that the limitation in question is not found in the independent claim." *Liebel-Flarsheim Co. v. Medrad, Inc.*, 358 F.3d 898, 910 (Fed. Cir. 2004). Patent Owner has not rebutted that presumption. Accordingly, for all of the foregoing reasons, we do not find persuasive Patent Owner's argument that Petitioner was required to show the independent claims are unpatentable as obvious over the four-bit embodiment before demonstrating that the four-bit dependent claims are unpatentable as obvious over that embodiment.

With respect to claim 1, Patent Owner argues Petitioner's reliance on Ellsberry's Figure 5 and Figure 13, which show the eight-bit embodiment, renders the 362 and 363 Petitions fatally defective as to the four-bit embodiment. PO Resp. 69–70. We do not agree. Although Patent Owner correctly argues Petitioner relies on Ellsberry's Figure 13 to show "*second module control signals*" in claim 1 (PO Resp. 69), Patent Owner also relies on Ellsberry's Figure 2 and corresponding description, which similarly discloses "*second module control signals*," as well as Dr. Stone's testimony. 362 Pet. 31–33; Ex. 1003 ¶ 210. As noted, Petitioner uses Ellsberry's Figure 2 in both Ellsberry's "first embodiment" with eight-bit memory devices (Figures 2, 5, and 13) and Ellsberry's "second embodiment" with four-bit memory devices (Figures 2, 6, and 11). Thus, because Ellsberry's Figure 2 and corresponding description discloses the "second module control

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signals," Patent Owner's argument is unpersuasive to show Petitioner's four-bit embodiment is fatally defective.

As to the "*PCB having an edge connector*," Petitioner relies on Ellsberry's Figure 5, as Patent Owner contends. 362 Pet. 44. However, Petitioner also relies on Dr. Stone's testimony to disclose the "*PCB*" limitation. 362 Pet. 48 (citing Ex. 1003 ¶¶ 277–279). Dr. Stone's testimony maps Ellsberry's Figures 6 and 13 to the "PCB" limitation. Ex. 1003 ¶¶ 277–279. Dr. Stone's testimony also reproduces Ellsberry's Figures 6 and 13, which show "*electrical contacts configured . . . to provide electrical conductivity*" and "*electrical conductivity*" between the "*buffer circuits*" and the "*data lines*" recited in claim 1. We credit Dr. Stone's testimony. Thus, we do not find Patent Owner's argument persuasive to show that the 362 and 363 Petitions are fatally defective as to the four-bit embodiment.

With respect to claims 16, 30, 43, 53, and 58, Patent Owner makes similar arguments as for claim 1. PO Resp. 72–80. These arguments are unpersuasive for similar reasons as discussed for claim 1. For these other claims, the only additional elements Patent Owner indicates lack a mapping to the four-bit embodiment are "*output address and control signals*" and "*first*" and "*second memory devices*." PO Resp. 76, 79. However, the "*output address and control signals*" are shown as signals on bus 220 in Ellsberry's Figure 2, which Petitioner uses in both the four-bit and eight-bit embodiments, and the description of Ellsberry's Figure 2 indicates the memory banks shown may have one or more memory devices (e.g., DRAM). Ex. 1005 ¶ 30. Thus, we do not find Patent Owner's arguments persuasive.

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We also note that Petitioner and Dr. Stone present evidence that Ellsberry's Figure 11 circuit with four-bit memory devices is equivalent to Ellsberry's Figure 13 circuit with eight-bit memory devices. 362 Pet. 20–21; 363 Pet. 20–21; Ex. 1003 ¶ 160. Figures 11 and 13 are more detailed embodiments of parts of Ellsberry's Figure 2, and use similar terminology to describe their elements. *See, e.g.*, Ex. 1003 ¶¶ 138–148. As concerns the '907 patent's claim language, Ellsberry's Figures 5 and 6 are the same as far as showing printed circuit boards with edge connectors, and control units, memory devices, and buffers arranged thereon, and the corresponding description of these figures uses the same terminology as the description of Ellsberry's Figure 2. *See, e.g.*, Ex. 1003 ¶¶ 252–253. The differences between Ellsberry's Figures 5 and 6 that Patent Owner indicates (PO Resp. 67; Ex. 2002 ¶ 90) in terms of such things as chip packaging (fine pitch ball grid array vs. chip-scale package) are not recited in the '907 patent's claims. Thus, we do not agree with Patent Owner's position that the eight-bit and four-bit embodiments are so very different from one another, or that one of ordinary skill in the art would ignore the many similarities they share. Ex. 1003 ¶¶ 138–152. In this regard, it must be remembered that the obviousness inquiry is "an expansive and flexible approach," not a rigid one. *KSR*, 550 U.S. at 415.

Many of the claims Patent Owner asserts have insufficient particularity do not relate to Ellsberry's n/2-bit or four-bit embodiments, but to Ellsberry's n-bit or eight-bit embodiments. Particularly, claims 15, 29, 35, 42, 50, 55, and 63 pertain to n-bit or 8-bit embodiments, and not n/2-bit or four-bit embodiments. Thus, Patent Owner's arguments only have relevance, at most, to claims 6, 12, 27, 38, 52, 57, and 65.

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In summary, for this challenge, we conclude Petitioner has shown by a preponderance of the evidence that claims 1–39 and 42–65 are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry. We conclude Petitioner has not shown by a preponderance of the evidence that claims 40 and 41 are unpatentable as obvious over Ellsberry.

E. Challenge #2: Obviousness of Claims 1–65 based on Ellsberry and JESD21–C

Petitioner contends the combination of Ellsberry and JESD21–C renders claims 1–29 and 58–65 unpatentable as obvious under 35 U.S.C. § 103(a). 362 Pet. 78–80; 363 Pet. 75–76; Ex. 1005; Ex. 1010. Patent Owner contends Petitioner's obviousness analysis is cursory and that JEDC21-C does not cure the deficiencies of Ellsberry noted in the previous challenge with respect to the "*first module control signals*" and "*second module control signals*" of claims 1, 16, and 58 or the "*output address and control signals*" and "*module control signals*" of claims 30, 43, and 53. PO Resp. 82–84. Patent Owner also argues JESD21–C fails to overcome the alleged deficiencies of Petitioner's second embodiment with four-bit memory devices. *Id.*

1. JESD21–C (Ex. 1010)

JESD21–C is an industry standard for DDR SDRAM Dual In-Line Memory Modules (DIMMs). Ex. 1010, 5. JESD21–C discloses an edge connector that includes an address bus, memory data bus, and RAS, CAS,

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WE and chip select control signal lines to provide electrical conductivity for the corresponding signals. *Id.* at 6.

2. Reason to Combine

In the 362 Petition, Petitioner asserts Ellsberry and JESD21–C are analogous art because they are in the same field of endeavor "and are reasonably pertinent to the problem addressed by the '907 patent." 362 Pet. 79; 363 Pet. 76. Petitioner states "[t]he combination of Ellsberry and JESD21–C would have been simply the arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement in the context of DIMM modules." 362 Pet. 79 (citing Ex. 1005 ¶¶ 2, 23, 27, Figs. 5–6; Ex. 1003 ¶¶ 266–267). Petitioner further states a person of ordinary skill in the art

> would have been motivated to make the combination in order to use the standard PCB form factor at that time with the novel capacity-expanding technology of Ellsberry (*see* Ex. 1003 ¶ 268; Ex. 1005 ¶¶ [0026], [0027], [0050]), and to expand the possible market for any product embodying Ellsberry's technology (*see* Ex. 1003 ¶ 269), and to ensure the ability to incorporate JESD21-C compatible memory devices for a variety of design applications (*see* Ex. 1003 ¶ 270; Ex. 1036 at 1:65–2:3).

362 Pet. 79–80. Petitioner makes the same assertions in the 363 Petition. 363 Pet. 76–77. Patent Owner does not dispute Petitioner's assertion of analogous art or reasons to combine Ellsberry and JEDC21-C.

3. Obviousness Analysis

Like the previous challenge, this challenge is based on Ellsberry, but in combination with JEDC21–C. As we agreed with Petitioner that

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Ellsberry alone renders claims 1–39 and 42–65 unpatentable as obvious for the reasons discussed in the previous challenge, we also conclude the combination of Ellsberry with JEDC21–C renders the claims obvious for the same reasons, particularly in the absence of any evidence that JEDC21–C negates any evidence of obviousness with respect to Ellsberry. As to Patent Owner's argument Petitioner's showing is cursory, Patent Owner does not indicate what specific shortcomings the challenge has due to its brevity other than allegations Ellsberry is deficient with respect to the "*first module control signals*" and "*second module control signals*" of claims 1, 16, and 58 and the "*output address and control signals*" and "*module control signals*," contentions with which we disagree for the reasons stated with regard to the previous challenge. Likewise, we find Petitioner's second embodiment based on Ellsberry's Figures 2, 6, and 11 with four-bit memory devices used in the challenge against claims 6, 12, 27, 38, 52, 57, and 65 not to be deficient for the reasons we explained with respect to the first challenge. Accordingly, there are no deficiencies Petitioner needs JESD21–C to cover. Furthermore, Patent Owner does not dispute Petitioner's contention that the edge connector of JESD21–C discloses the limitation of claims 1, 16, and 58 reciting to "*provide electrical conductivity between the module control circuit and the set of control lines, and between the M buffer circuits and the M sets of n data lines.*" *See* 362 Pet. 78–79. Nor does Patent Owner dispute Petitioner's contention that the edge connector of JESD21–C discloses the limitation of claims 30, 43, and 53 reciting to "*provide electrical conductivity between the module control circuit and the set of control signal lines, and between the plurality of buffer circuits and the plurality of sets of data signal lines*." 363 Pet. 76. Thus, we conclude that Petitioner has

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shown by a preponderance of the evidence that claims 1–39 and 42–65 are unpatentable as obvious over Ellsberry and JESD21–C.

Petitioner does not rely on JESD21–C in this challenge to disclose the input buffers and output buffers associated with a write command in claims 40 and 41. Thus, for the reasons stated with regard to the previous challenge, we determine that Petitioner does not show by a preponderance of the evidence that claims 40 and 41 are unpatentable as obvious over the combination of Ellsberry and JESD21–C.

F. Challenge #3: Obviousness of Claims 7, 19, and 24 based on Ellsberry and Halbert

Claims 7, 19, and 24 recite that "*the second module control signals indicate a direction of data flow through the buffer circuits*." Petitioner contends the combination of Ellsberry and Halbert renders claims 7, 19, and 24 unpatentable as obvious under 35 U.S.C. § 103(a). 362 Pet. 80–81; Ex. 1005; Ex. 1006. Patent Owner asserts Petitioner's obviousness analysis is cursory and that Halbert does not cure the deficiencies of Ellsberry we noted in considering the previous challenge with respect to the "*first module control signals*" and "*second module control signals*" of claims 1 and 16. PO Resp. 82–84. Patent Owner further argues Halbert fails to overcome the deficiencies of Petitioner's second embodiment with four-bit memory devices. *Id.* at 83–84.

1. Halbert (Ex. 1006)

Halbert discloses a DIR (direction) signal that "specifies whether data flow is towards the memory array (TO) or away from the memory array (AWAY)." Ex. 1006, 5:25–28. "Module controller 110 determines the current value for DIR by snooping CMD signals as they pass through the

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controller." *Id.* at 5:28–30.

2. Reason to Combine

Petitioner contends Ellsberry and Halbert are analogous art to the '907 patent and use similar "snooping" techniques to determine the direction of data flow and control bidirectional drivers accordingly. 362 Pet. 80 (citing Ex. 1003 ¶¶ 323–325; Ex. 1005 ¶¶ 10, 12, 39; Ex. 1006, 3:58–4:8, 5:23–30, Fig. 4). Petitioner contends a person of ordinary skill in the art "would have readily understood that Ellsberry's command decoder 304 can be implemented to "snoop" read and write commands in order to generate a DIR signal and provide a predictable result (i.e., setting the direction of data flow)." 362 Pet. 80–81 (citing Ex. 1003 ¶ 325). Patent Owner does not dispute Petitioner's assertion that Ellsberry and Halbert are analogous art or Petitioner's reason to combine them.

3. Obviousness Analysis

This challenge is based on Ellsberry in addition to Halbert. Because we concluded in considering the first challenge that Petitioner has shown that Ellsberry alone renders claims 7, 19, and 24 unpatentable as obvious, we also conclude the combination of Ellsberry and Halbert renders the claims unpatentable as obvious absent any showing that Halbert in some way negates Petitioner's evidence with respect to Ellsberry. We do not agree with Patent Owner that Ellsberry fails to disclose the claimed "*first module controls signals*" or "*second module control signals*" as Patent Owner argues, for reasons we explained with respect to Petitioner's challenge based on Ellsberry alone. Patent Owner's contention regarding lack of particularity of the Ellsberry's embodiment with four-bit memory devices (based on Ellsberry's Figures 2, 6, and 11—see PO Resp. 62–63) has no

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bearing on these claims, which do not recite n/2 or four-bit memory devices. In addition, Patent Owner does not dispute that Halbert discloses a direction signal to control the direction of data flow through buffers as claimed. Ex. 1003 ¶ 320 (citing Ex. 1006 at 5:23–39, Fig. 4). Although Patent Owner alleges Petitioner's assertions and evidence are cursory, Patent Owner does not identify, nor do we find, anything missing from the evidence needed to support Petitioner's assertions. Accordingly, Petitioner has shown by a preponderance of the evidence that claims 7, 19, and 24 are unpatentable as obvious over Ellsberry and Halbert.

G. Challenge #4: Obviousness of Claim 9, 28, and 36 based on Ellsberry and Ruckerbauer

Claim 9 recites

> *9. The memory module of claim 1, wherein the module control circuit comprises one or more integrated circuits having first input/output connections, second input/output connections, third input/output connections, and fourth input/output connections, wherein the first memory devices include a subset of memory devices coupled to the first input/output connections and another subset of memory devices coupled to the second input/output connections, and wherein the second memory devices include a subset of memory devices coupled to the third input/output connections and another subset of memory devices coupled to the fourth input/output connections.*

Claims 28 and 36 recite similar limitations.

Petitioner contends the combination of Ellsberry and Ruckerbauer render claim 36 unpatentable as obvious under 35 U.S.C. § 103(a). 362 Pet. 81–82; 363 Pet. 77–78; Ex. 1005; Ex. 1038. Patent Owner argues Petitioner's challenge involves only cursory analysis, and fails to overcome the deficiencies of Petitioner's claim mapping of Ellsberry to the "*first*

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module control signals" and "*second module control signals*" in claims 1 and 16, or the "*output address and control signals*" and the "*module control signals*" in claim 30. PO Resp. 82–84.

1. Ruckerbauer (Ex. 1038)

Ruckerbauer discloses a register circuit mounted in the middle of a memory module and connections to the left and right of the register circuit. Ex. 1038, Abstract, 4:57–62, Figs. 1, 2.

2. Reason to Combine

Petitioner contends Ellsberry and Ruckerbauer are analogous art to the '907 patent because they are both directed to improving performance capacity of memory subsystems, including DIMMs. 362 Pet. 81; 363 Pet. 78. Petitioner contends a person of ordinary skill in the art "would have been motivated to implement Ellsberry's module with separate control lines to the left and right according to Ruckerbauer because it would simplify the connections and reduce the capacitive loading to reach the required signal speeds." 362 Pet. 81–82 (citing Ex. 1003 ¶¶ 358–362; Ex. 1005 ¶¶ 10, 27, Figs. 5 and 13; Ex. 1038 at 4:46–5:3); 363 Pet. 78 (citing same). Petitioner also contends implementation of separate control lines to the left and right "would have been well within the level of skill at the time, and would use well known, standardized techniques that would work as in the prior art provide predictable results." 362 Pet. 82 (citing Ex. 1003 ¶¶ 363–364; Ex. 1010 at 18; Ex. 1038 at 2:31–32, Fig. 1), 363 Pet. 78 (citing same). Patent Owner does not dispute that Ellsberry and Ruckerbauer are analogous art, or Petitioner's reason to combine them. *See generally* PO Resp.

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3. Obviousness Analysis

This challenge is based on Ellsberry in addition to Ruckerbauer. Because we concluded with respect to the first challenge that Ellsberry alone discloses and renders claims 9, 28, and 36 unpatentable as obvious, so too the combination of Ellsberry with Ruckerbauer renders the claims unpatentable as obvious absent any showing that Ruckerbauer in some way negates Ellsberry's disclosure, which has not been shown to be the case here. For reasons explained with respect to the first challenge, we do not agree with Patent Owner that Ellsberry fails to disclose the claimed "*first module controls signals*" or "*second module control signals*" as Patent Owner argues. Petitioner's contention regarding lack of particularity of the embodiment based on Ellsberry's Figures 2, 6, and 11 has no bearing on these claims, which do not recite n/2 or four-bit memory devices. In addition, Patent Owner does not dispute that Ruckerbauer discloses a register circuit mounted in the middle of a memory module and connections to the left and right, or that the combination of Ellsberry and Ruckerbauer discloses "mounting a control circuit in the middle of the circuit board such that some of the memory devices are mounted to the left of the control circuit and some of the memory devices are mounted to the right of the control circuit," with separate connections from the control circuit to the left and right memory devices according to Ruckerbauer. *See* 362 Pet. 81; 363 Pet. 77. Accordingly, we conclude that Petitioner has shown by a preponderance of the evidence that claims 9, 28, and 36 are unpatentable as obvious over Ellsberry and Ruckerbauer.

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H. Challenge #5: Obviousness of Claims 14, 17–23, and 60–65 based on Ellsberry and Stone

Petitioner contends Ellsberry and Stone render claims 14, 17–23, and 60–65 unpatentable as obvious under 35 U.S.C. § 103(a). 362 Pet. 82–84; Ex. 1005; Ex. 1035. These claims recite "*tristate buffers*" either directly or by dependency. Patent Owner contends Stone does not cure the alleged deficiencies of Ellsberry in relation to "*first module controls signals*" and "*second module control signals*" as recited in independent claims 1, 16, and 58. PO Resp. 82–84. In addition, Patent Owner contends Stone does not cure the alleged lack of particularity of the embodiment based on Ellsberry's Figures 2, 6, and 11 with four-bit memory devices. *Id.*

1. Stone (Ex. 1035)

Stone discloses tristate buffers suitable for driving multiple taps on a transmission line. Ex. 1035, 74. As depicted in Stone's Figure 4.7, *supra*, Stone also discloses separate write and read data paths. Stone further discloses that control signals control the tristate buffers. *Id.* at 133.

2. Reason to Combine

Petitioner contends "it would have been obvious to implement Ellsberry's bidirectional drivers using "tristate buffers" to drive data to and from the memory devices efficiently and reliably, as explained by Stone." 362 Pet. 82–83 (citing Ex. 1003 ¶¶ 385–388; Ex.1005, Figs.11, 13; Ex.1035, 68, 74 (Fig.2.28), 117). Petitioner contends that in Ellsberry's Figures 11 and 13, "each of the data buses on Ports A and B of the bank switch has multiple taps, one for each memory device." 362 Pet. 83 (citing Ex. 1003 ¶ 388). Petitioner further contends a person of ordinary skill in the art "would have been motivated to use 'tristate buffers' because Stone states

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that 'tri-state drivers . . . [are] ***suitable for driving several taps on a transmission line***." 362 Pet. 83 (citing Ex. 1035, 74; Ex. 1003 ¶ 388). Petitioner contends it would have been obvious to a person of ordinary skill in the art "to implement bidirectional drivers 402&404 in Ellsberry's multi-tap configuration using Stone's tristate buffers, such as those disclosed in Stone." 362 Pet. 83 (citing Ex. 1003 ¶¶ 388–389). Patent Owner does not dispute Petitioner's stated reasons to combine Ellsberry and Stone.

3. Obviousness Analysis

This challenge is based on Ellsberry in addition to Stone. Because we concluded with respect to the first challenge that Ellsberry alone disclosed claims 4, 17–23, and 60–65, we likewise conclude the combination of Ellsberry with Stone discloses the limitations of these claims and renders them unpatentable as obvious, particularly in the absence of any showing that Stone somehow negates Ellsberry's disclosure. For the reasons stated with respect to the first challenge, we are not persuaded Ellsberry was deficient in respect to the "*first module controls signals*" and "*second module control signals*." With respect to Patent Owner's contention that the 362 and 363 Petitions lacked particularity with respect to the showing for the claims reciting four-bit memory devices, of the claims involved in this challenge, only claim 65 recites four-bit memory devices. We find Petitioner's contention unpersuasive for reasons explained with respect to the challenge based on Ellsberry alone. Patent Owner does not dispute that Stone discloses tristate buffers suitable for driving multiple taps on a transmission line, separate write and read data paths, and control signals to control the tristate buffers. *See generally* PO Resp. Patent Owner also does not dispute Petitioner's reason to combine Ellsberry and Stone.

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Accordingly, for the foregoing reasons, we conclude Petitioner has shown by a preponderance of the evidence that claims 14, 17–23, and 60–65 are unpatentable as obvious over Ellsberry and Stone.

I. Motion to Exclude (362 IPR, Paper 22)

Patent Owner seeks to exclude Petitioner's Exhibits 1024 and 1043–1048 for various reasons. 362 IPR, Paper 22, 1–3. We did not rely on Exhibits 1024, 1043, and 1045–1048 in rendering our decision. These exhibits relate to a parallel ITC proceeding and were not helpful to us in rendering our decision in this case.

As to Dr. Baker's testimony, Exhibit 1044, we gave the evidence the due weight under the facts and circumstances, but did not find it necessary in rendering our decision to rely on any of the portions to which Patent Owner objects

IV. SUMMARY

Petitioner has shown by a preponderance of the evidence that:

(1) Claims 1–39 and 42–65 (but not claims 40 and 41) are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry;

(2) Claims 1–39 and 42–65 (but not claims 40 and 41) are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry and JESD21-C;

(3) Claims 7, 19, and 24 are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry and Halbert;

(4) Claims 9, 28, and 36 are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry and Ruckerbauer; and

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(5) Claims 14, 17–23, and 60–65 are unpatentable as obvious under 35 U.S.C. § 103(a) over Ellsberry and Stone.

V. ORDER

For the foregoing reasons, it is

ORDERED that claims 1–39 and 42–65 of the '907 patent are held unpatentable;

FURTHER ORDERED that claims 40 and 41 are not held unpatentable;

FURTHER ORDERED that Patent Owner's Motion to Exclude Petitioner's Evidence is *dismissed* as moot;

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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