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Paper 45
Entered: October 18, 2023

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., MICRON TECHNOLOGY, INC., MICRON SEMICONDUCTOR PRODUCTS, INC., and MICRON TECHNOLOGY TEXAS LLC,[1]
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00639
Patent 10,949,339 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and KARA L. SZPONDOWSKI, *Administrative Patent Judges.*

JURGOVAN, *Administrative Patent Judge*.

DECISION
Final Written Decision
Determining All Challenged Claims Unpatentable
Dismissing Petitioner's Motion to Exclude
35 U.S.C. § 318(a)

[1] Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC filed a motion for joinder and a petition in IPR2023-00204 and have been joined as petitioners in this proceeding. *See* Paper 33.

I. INTRODUCTION

A. Background and Summary

Samsung Electronics Co., Ltd. ("Samsung") filed a Petition (Paper 1, "Pet.") for *inter partes* review of claims 1–35 ("challenged claims") of U.S. Patent 10, 949,339 B2 (Ex. 1001, "the '339 patent"). Netlist, Inc. ("Patent Owner") filed a Preliminary Response (Paper 7, "Prelim. Resp.") to the Petition. Samsung filed an authorized Preliminary Reply (Paper 13) ("Reply"), and Patent Owner filed an authorized Preliminary Sur-Reply (Paper 14) ("Sur-Reply"). We instituted *inter partes* review under 35 U.S.C. § 314(a). Paper 15 ("Inst. Dec.").

During the trial, Patent Owner filed a Response (Paper 27, "Resp."), Petitioner filed a Reply (Paper 31), and Patent Owner filed a Sur-Reply (Paper 36). We joined Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC as petitioners in this proceeding, and we refer to Samsung and these entities collectively as "Petitioner." *See* Paper 33.

Petitioner and Patent Owner requested oral argument (Papers 34 and 35). A hearing was conducted on July 19, 2023. Paper 44 ("Tr.").

Petitioner objected to evidence (Papers 17, 28, 37) and filed a Motion to Exclude (Paper 38). Patent Owner filed an Opposition to Petitioner's Motion to Exclude (Paper 40), and Petitioner filed a Reply (Paper 41) in support of its Motion to Exclude.

We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a). Having reviewed the complete trial record, we determine that Petitioner has shown, by a preponderance of the evidence, that the challenged claims are unpatentable.

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B. Real Parties in Interest

Petitioner entities, Samsung Electronics Co., Ltd., Samsung Semiconductor, Inc., Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC identify themselves as real parties in interest. Pet. xxxii; IPR2023-00204, Paper 3, 1.

Patent Owner identifies itself as the sole real party in interest. Paper 3, 1.

C. Related Matters

The parties advise that the '339 patent is related to the following pending matters:

- *Samsung Electronics Co., Ltd. et al. v Netlist, Inc.,* No. 1:21-cv-01453 (D. Del. filed Oct. 15, 2021)
- *Netlist, Inc. v. Samsung Electronics Co., Ltd. et al.*, No. 2:21-cv-00463 (E.D. Tex. filed Dec. 20, 2021)
- U.S. Patent Application No. 17/202,021.

Petitioner contends that the '339 patent is related to the following matters, which are no longer pending:

- *In the Matter of Certain Memory Modules and Components Thereof*, Inv. No. 337-TA-1089 (USITC filed Oct. 31, 2017) (U.S. Patent No. 9,606,907)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (USITC filed Sept. 1, 2016) (U.S. Patent No. 8,516,185)
- U.S. Patent Application No. 16/841,552 (abandoned)
- IPR2018-00362 (U.S. Patent No. 9,606,907)
- IPR2018-00363 (U.S. Patent No. 9,606,907)

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- IPR2018-00364 (U.S. Patent No. 9,606,907)
- IPR2018-00365 (U.S. Patent No. 9,606,907)
- IPR2017-00577 (U.S. Patent No. 8,516,185)

Pet. xxxii–xxxiii; Paper 3, 1.

D. Overview of the '339 Patent (Ex. 1001)

The '339 patent is titled "Memory Module with Controlled Byte-Wise Buffers." Ex. 1001, code (54). The memory module communicates with a memory controller and comprises double data rate (DDR) dynamic random access memory (DRAM) devices arranged in multiple ranks each of the same width as the memory module. *Id.* at code (57). The module controller is configured to receive and register input control signals for a read or write operation from the memory controller and to output registered address and control signals to the DRAM devices. *Id.* The memory module further comprises byte-wise buffers controlled by a set of module control signals to actively drive respective byte-wise sections of each data signal associated with the read or write operation between the memory controller and the selected rank. *Id.*

Figure 3C of the '339 patent is shown below.

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Figure 3C:

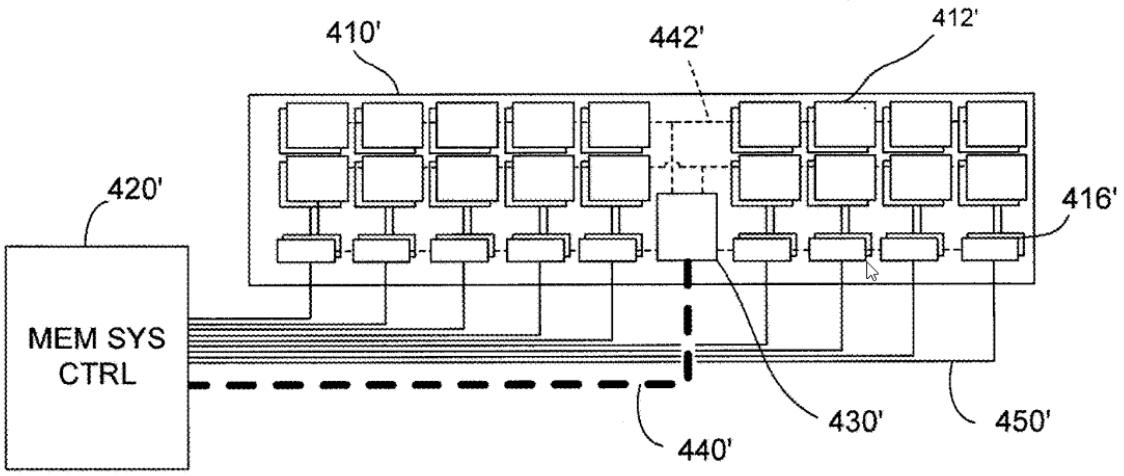


Figure 3C shows a layout of memory devices 412', data transmission circuits 416', and control circuit 430' on printed circuit board (PCB) 410' of memory module 402'. Ex. 1001, 3:57–60, 9:10–13. Memory devices 412' are arranged in ranks on PCB 410'. *Id.* at 9:27–31. Memory devices 412' are connected to data transmission circuits 416' arranged along the bottom edge of memory module 410'. *Id.* at 9:18–26. Data transmission circuits 416' are further connected to memory control system 420' via data lines 450'. *Id.* at 7:59–61. Memory system controller 420' connects to control circuit 430' via address and control lines 440'. *Id.* at 7:64–65. Control circuit 430' in turn connects with memory devices 412' via lines 442'. *Id.* at 10:17–21. Control circuit 430' receives commands and address signals from memory system controller 420' and generates appropriate control and address signals to select memory devices 412' and carry out the command (e.g., a read or write operation). *Id.* at 7:56–58, 8:23–26, 10:33–50.

Figure 5 of the '339 patent is shown below.

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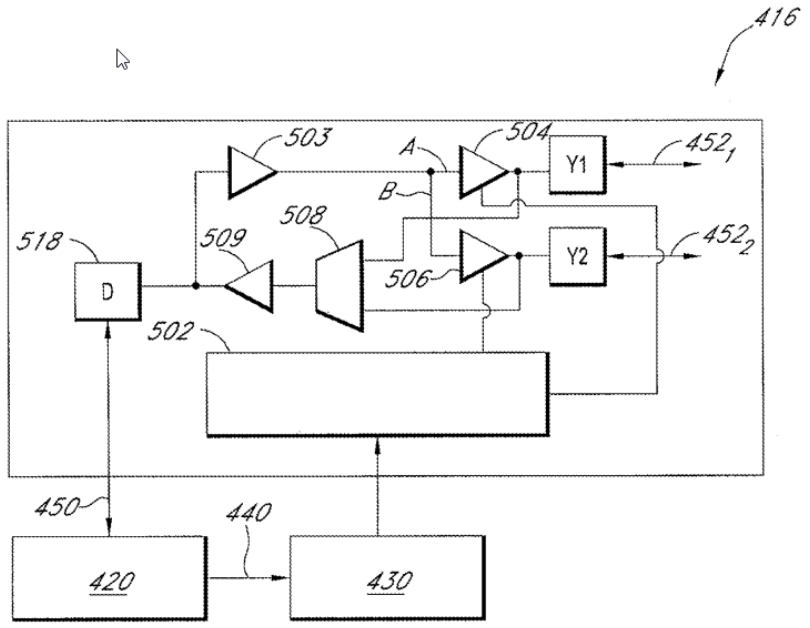


FIG. 5

Figure 5 shows a data transmission circuit 416. *Id.* at 4:4–6. Data transmission circuit 416 includes control logic circuitry 502 to control various components including buffers, switches, and multiplexers. *Id.* at 15:26–33. The embodiment of Figure 5 is 1-bit wide and switches a single data line 518 between the memory controller 420 and memory devices 412. *Id.* at 15:33–35. In a write operation, data entering data line 518 is driven onto two data paths, labeled path A and path B after passing through write buffer 503. *Id.* at 15:45–48. Ranks of memory devices 412 are divided into groups in ranks A and C associated with path A, and ranks B and D, associated with path B. *Id.* at 15:48–58. Control circuit 430 provides enable control signals to control logic circuitry 502 to select either path A or B to direct the data. *Id.* at 16:7–11. First tri-state buffer 504 in path A is enabled, and second tristate buffer in path B is disabled with its output in a high-impedance condition. *Id.* at 16:13–16. Data is directed along path A to

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terminal Y1 connected to the first group of memory devices 412, ranks A and C. *Id.* at 16:16–20. If an "enable B" signal is received, then first tristate buffer 504 opens path A and the second tristate buffer 504 closes path B, thus directing the data to second terminal Y2 that is connected to the second group of memory devices 412 in ranks B and D. *Id.* at 16:21–25.

E. Illustrative Claim

Claims 1, 11, 19, and 27 are independent claims and the rest are dependent. Claim 1, reproduced below with Petitioner's identifiers in brackets, is illustrative of the claimed invention:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:
>
> [1a] a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket;
>
> [1b] double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks;
>
> [1c1] a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals,

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[1c2] wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals; and

[1d1] a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals,

[1d2] wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side,

[1d3] wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines;

[1e] wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period; and

[1f] wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:9–67.

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F. Evidence[2]

Petitioner relies upon the following prior art references:

Reference		Date	Exhibit No.
Ellsberry[3]	US 2006/0277355 A1	Dec. 7, 2006	1005
Halbert[4]	US 7,024,518 B2	Apr. 4, 2006	1006

Pet. 1, 11–13.

G. Asserted Challenge to Patentability

Petitioner asserts the following ground of unpatentability:

Claims Challenged	35 U.S.C. §	Reference(s)/Basis
1–35	§ 103(a)	Ellsberry, Halbert

Pet. 1.

II. ANALYSIS

A. Principles of Law

In an *inter partes* review, a petitioner bears the burden of persuasion to prove "unpatentability by a preponderance of the evidence." *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015) (quoting 35 U.S.C. § 316(e)); *see* 37 C.F.R. § 42.1(d) (2021).

A claim is unpatentable under 35 U.S.C. § 103(a) if "the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

[2] Petitioner also relies upon the Declaration of Dr. Vivek Subramanian (Ex. 1003).
[3] Petitioner contends Ellsberry is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 11.
[4] Petitioner contends Halbert is prior art under pre-AIA 35 U.S.C. § 102(b). Pet. 12.

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invention was made to a person having ordinary skill in the art to which said subject matter pertains." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) objective evidence of nonobviousness, i.e., secondary considerations. *See Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

B. Level of Ordinary Skill in the Art

Factors pertinent to a determination of the level of ordinary skill in the art include "(1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Envtl. Designs, Ltd. v. Union Oil Co. of Cal.*, 713 F.2d 693, 696 (Fed. Cir. 1983) (citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381–82 (Fed. Cir. 1983)). "Not all such factors may be present in every case, and one or more of these or other factors may predominate in a particular case." *Id.* at 696–697.

Petitioner contends that a person of ordinary skill in the art in the field of the '339 patent in 2009 would have had an advanced degree in electrical or computer engineering and two years working in the field, or a bachelor's degree in such engineering disciplines and at least three years working in the field. Pet. 2 (citing Ex. 1003 ¶¶ 50–51). Petitioner contends such person would have been familiar with various standards of the day, including JEDEC industry standards, and would have been knowledgeable about the

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design and operation of standardized DRAM and SDRAM memory devices and memory modules and how they interacted with the memory controller of a computer system. *Id.* (citing Ex. 1003 ¶ 51; Ex. 1041).

Patent Owner indicates that it applies the skill level of a person of ordinary skill in the art proposed by Petitioner for this proceeding. Resp. 31.

On this record, we accept Petitioner's statement of the level of ordinary skill in the art except that we omit the qualifier "at least" before years of experience because it may encompass levels that are beyond ordinary and render the level ambiguous. Otherwise, we find Petitioner's statement of the level of ordinary skill in the art consistent with the '339 patent and the applied prior art references. *Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (the applied prior art may reflect an appropriate level of skill).

C. Claim Construction

We construe claim terms "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. 282(b)." 37 C.F.R. § 42.100(b) (2021). There is a presumption that claim terms are given their ordinary and customary meaning, as would be understood by a person of ordinary skill in the art in the context of the specification. *See In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007). Nonetheless, if the specification "reveal[s] a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess[,] . . . the inventor's lexicography governs." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1316 (Fed. Cir. 2005) (en banc) (citing *CCS Fitness, Inc. v. Brunswick Corp.*, 288 F.3d 1359, 1366 (Fed. Cir. 2002)). "In determining the meaning of the disputed claim limitation, we look

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principally to the intrinsic evidence of record, examining the claim language itself, the written description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing Phillips, 415 F.3d at 1312–17). Only disputed claim terms must be construed, and then only to the extent necessary to resolve the controversy. *See Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017).

1. "Rank" and "Rank Select Signal"

Petitioner discusses the terms "rank" and "rank select signal" in the claim construction section of its Petition. Pet. 8–10. Petitioner contends that a "rank select signal" is also known as a "chip-select signal" and alleges that the '339 patent uses the terms consistently with the JEDEC standards of the time. *Id.* at 8–9. Petitioner also contends that the term "bank" has been replaced over time with "rank." *Id.* at 9–10 (citing Ex. 1041, 318–20 (discussing DIMMs, ranks, banks, and arrays), 413 (Fig. 10.5)). Although Petitioner cites a definition of "rank" (*id.* at 9), Petitioner does not propose that this definition should be applied in this case. *See id.* at 8–10. Patent Owner does not dispute Petitioner's discussion of the terms "rank" and "rank select signal." *See* Resp. As there is no evidence of any dispute concerning these terms, we need not construe them. *See Nidec, supra*.

2. "Fork-in-the-Road" versus "Straight Line"

Petitioner contends that the '339 patent only discloses a "fork-in-the-road" configuration as opposed to a "straight line" configuration. Pet. 10–11. Petitioner alleges that Patent Owner "has tried (unsuccessfully) to construe similar claims to cover a 'straight line' layout where the claimed ranks are on the same data path without any 'fork in the road.'" *Id.* at 10

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(citing Ex. 1003 ¶¶ 170–171; Ex. 1034, 36; Ex. 1076, 30–35). Petitioner contends that "it is not necessary to resolve this potential claim construction dispute because the Ellsberry reference discussed below discloses the same layout found in the 339 Patent, thus rendering the claims obvious either way." *Id.* (citing Ex. 1062, 12–23, 44–45; Ex. 1003 ¶¶ 172, 297, 436). Petitioner does not propose construction of any claim term, particularly not one related to the "fork-in-the-road" or "straight line" configuration. *See id.* at 10–11.

Patent Owner argues that in the district court litigation, the "drive" terms (e.g., "actively drive" in claim 1 (e.g., limitation 1(e)) were construed as "enabling only one of the data paths while the other possible paths are disabled," which "takes into consideration [Petitioner's] argument that the '339 patent is about fork-in-the-road . . . while also accounting for the fact . . . that the claims do not require there necessarily be more than one possible path." Resp. 31 (citing Ex. 2016, 10; Ex. 2006, 57:21–60:19). Patent Owner argues this construction should be adopted here. *Id.* *See also* Sur-Reply 27–28.

Petitioner argues that its disagreement with Patent Owner concerning claim construction "is not relevant here." Reply 1. We agree as concerns the "fork-in-the-road" or "straight line" distinction.

Petitioner and Patent Owner have not identified any dispute concerning specific claim language that requires interpretation as "fork-in-the-road" or "straight line" configuration. Consequently, there is no dispute as to claim language before us that we need to resolve. *See Nidec*, *supra*.

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3. Means Plus Function

Petitioner contends "it is . . . not necessary to determine whether any terms of the 339 Patent are governed by § 112,¶6, given that Ellsberry alone or in view of Halbert matches the disclosure of the 339 Patent." Pet. at 10–11 (citing Pet. 11–38 (§§IV.E–G)). When claims do not mention the word "means," there is a rebuttable presumption that § 112, ¶ 6 does not apply. *Williamson v. Citrix Online, LLC*, 792 F.3d 1339, 1348 (Fed. Cir. 2015) (citing *Personalized Media Commc'ns, LLC v. Int'l Trade Comm'n*, 161 F.3d 696, 703–04 (Fed. Cir. 1998)). Neither Petitioner nor Patent Owner provide any evidence to rebut the presumption here that § 112, ¶ 6 does not apply to the '339 patent's claims in the absence of any mention of the word "means." Accordingly, we do not construe any limitation of the '339 patent's claims as "means plus function" under § 112, ¶ 6.

D. Obviousness Over the Combination of Ellsberry and Halbert

Petitioner contends that claims 1–35 of the '339 patent are unpatentable as obvious over the combination of Ellsberry and Halbert. Pet. 44–145. Patent Owner counters that claims 1–35 are patentable. Resp. 31–79. We address Ellsberry and Halbert and their combination in the following section and conclude that Petitioner has shown claims 1–35 unpatentable for the reasons that follow.

1. Ellsberry (Ex. 1005)

Ellsberry is titled "Capacity-Expanding Memory Device." Ex. 1005, code (54). Ellsberry describes that "[a] control unit and memory bank switch are mounted on a memory module to selectively control write and/or read operations to/from memory devices communicatively coupled to the memory bank switch." *Id.* at code (57). "By selectively routing data to and

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from the memory devices, a plurality of memory devices may appear as a single memory device to the operating system." *Id.*

Figure 2 of Ellsberry is shown below.

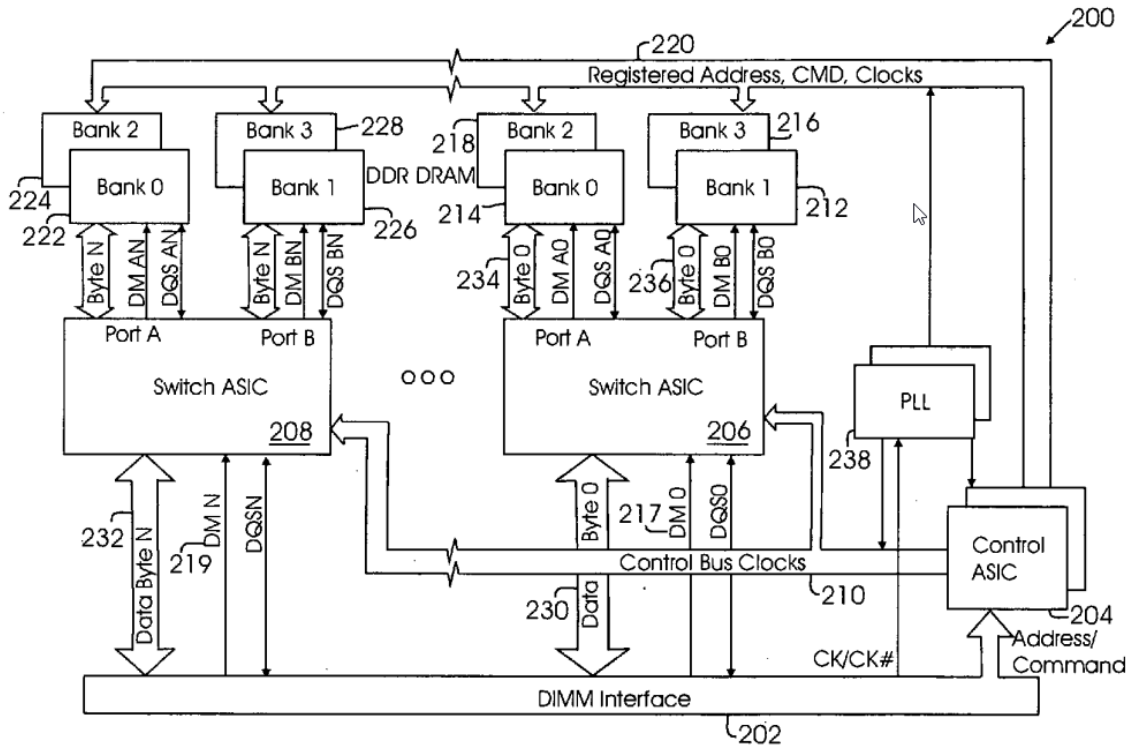


Fig. 2

Figure 2 "illustrates a block diagram of a capacity-expanding memory system 200 according to one embodiment." *Id.* ¶ 28. In Figure 2, system 200 has a DIMM interface 202 that couples to a "memory socket and communication bus over which data, memory addresses, commands, and control information are transmitted." *Id.* "The capacity-expanding feature of the invention is accomplished by a combination of control unit 204 and one or more memory bank switches 206 & 208." *Id.* Figure 2 of Ellsberry illustrates system 200 with control ASIC 204 that receives addresses and commands from DIMM interface 202 and generates corresponding control signals on bus 210 and addresses on bus 220 to selectively connect memory

banks 212–228 to DIMM interface 202 via switch ASICs 206, 208. *Id.* ¶¶ 28–29. Ellsberry also teaches that the command scheme for a control unit operating multiple banks includes a Posted CAS_n[5] parameter pertaining to latency. *Id.* ¶ 19, Fig. 8B, n.3, Fig. 9.

2. Halbert (Ex. 1006)

Halbert is titled "Dual-Port Buffer-to-Memory Interface" and discloses a memory module with selectable ranks of memory devices. Ex. 1006, codes (54), (57). Halbert's Figure 4 is shown below.

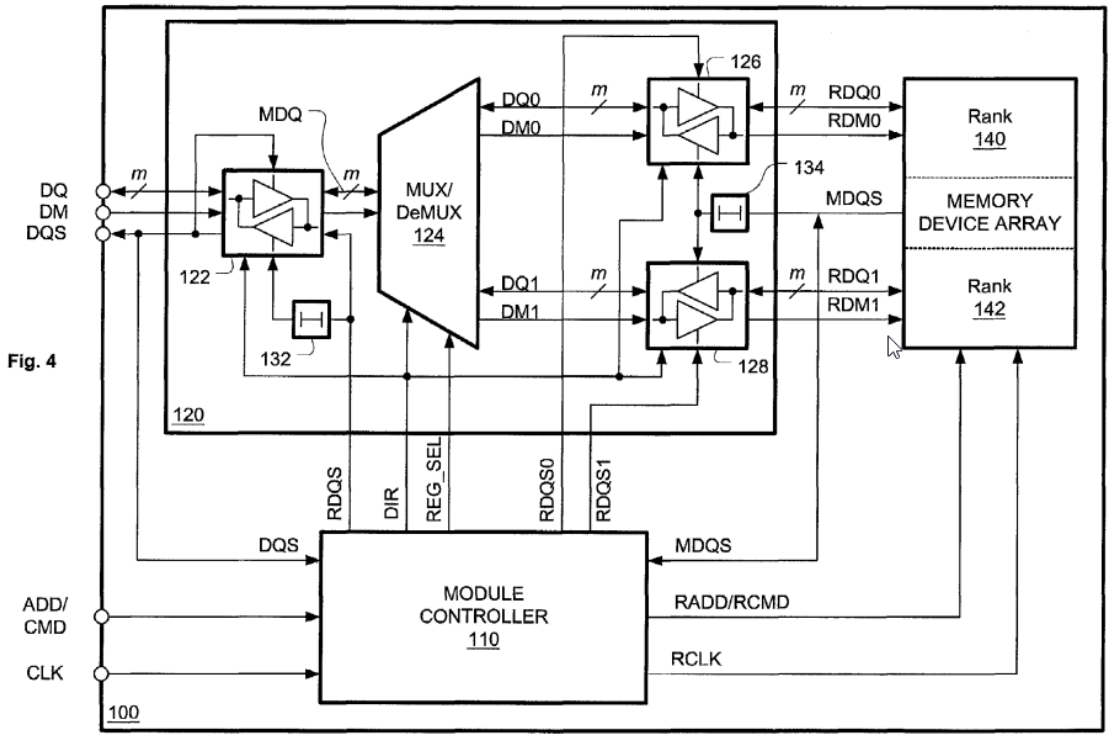


Fig. 4

In Figure 4, memory module 100 includes a module controller 110; data interface circuit 120; and a memory device array 140/142. *Id.* at 4:36–39. Module controller 110 synchronizes operation of module 100 with the attached memory system. *Id.* at 4:40–41. Module controller 110 also

[5] "CAS" stands for Column Address Strobe.

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provides timing and synchronization signals to data interface circuit 120. *Id.* at 4:45–47. Data interface circuit 120 provides for m-bit-wide data transfers between the memory module and the system memory data bus, and Rxm-bit-wide data transfers between the interface circuit and the memory device array. *Id.* at 4:49–53. In Figure 4, R is 2 because the memory device array comprises two ranks 140 and 142, each capable of performing m-bit-wide data transfers. *Id.* at 4:52–55.

Bidirectional buffer 122 is coupled to a bi-directional module data port that can be connected to a system memory data bus. *Id.* at 4:60–62. An m-bit wide path through buffer 122 receives and drives data signals DQ on the system memory data bus. *Id.* at 4:62–64. Two bi-directional data registers 126 and 128 connect, respectively, to memory device array ranks 140 and 142. *Id.* at 5:6–7. Each data register can drive an m-bit-wide word to that rank. *Id.* at 5:8–11.

Multiplexer/demultiplexer 124 multiplexes data signals DQ0 from register 126 and DQ1 from register DQ1 to buffer 122 when the module is reading from memory device array 140/142. *Id.* at 5:15–19. When the module is writing to the memory device array, data signals MDQ from buffer 122 can be channeled to either DQ0 or DQ1. *Id.* at 5:19–22.

Module controller 110 synchronizes operation of the data port buffer 122, MUX/deMUX 124, and data registers 126 and 128 via control signals. *Id.* at 5:23–25. Buffers 122, 126, and 128 are illustrated as bidirectional tristate buffers. *Id.* at Figs. 4, 9.

3. Motivation to Combine Ellsberry and Halbert

Petitioner contends that one of ordinary skill in the art would have been motivated to combine Ellsberry and Halbert. Pet. 44–47. Specifically,

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Petitioner annotates Ellsberry's Figure 4 as shown below to demonstrate its proposed combination of Ellsberry and Halbert:

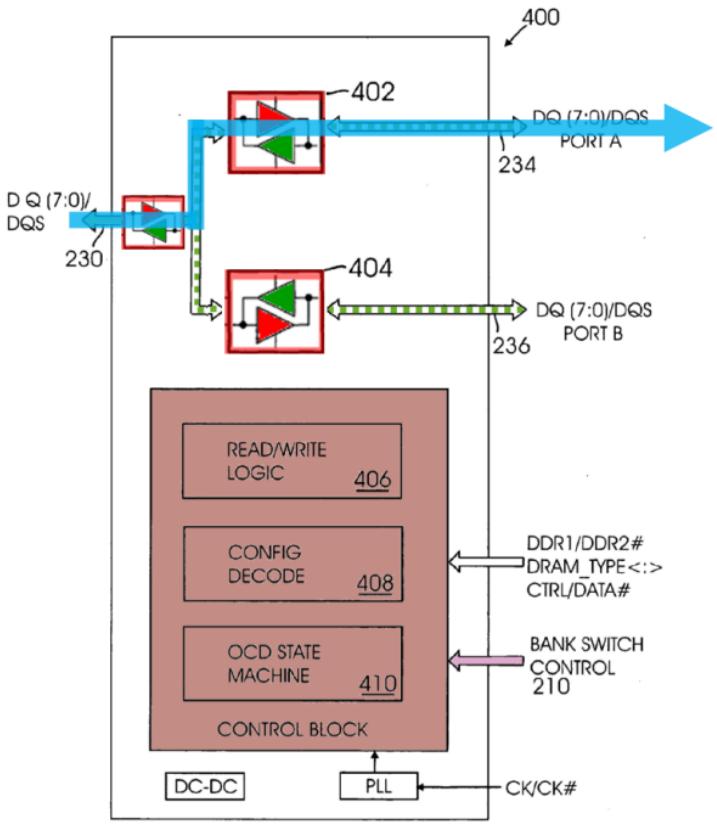


Fig. 4

Pet. 45 (citing Ex. 1003 ¶¶ 256–265). Petitioner's annotated Figure 4, above, proposes to replace Ellsberry's two bidirectional drivers 402, 404 with Halbert's tristate buffers 126, 128 to interface with memory buses 234, 236, and to add an additional Halbert tristate buffer 122 to interface with system controller bus 230. *Id.* at 46–47 (citing Ex. 1003 ¶¶ 257–264; Ex. 1005 ¶ 45, Fig. 4; Ex. 1006, 5:23–65, 9:27–35, Fig. 4; Ex. 1035, 133, Figs. 4, 7).

According to Petitioner, "[a]dding such a bidirectional buffer to interface the system memory bus and implementing Ellsberry's bidirectional drivers with tristate buffers would have been well within the level of skill at

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the time, since both Ellsberry and Halbert teach using bidirectional buffers interfacing with bidirectional busses, as taught in textbooks for decades." *Id.* at 46–47 (citing Ex. 1005 ¶ 45, Fig. 4; Ex. 1006, 5:23–65, 9:27–35, Fig. 4; Ex. 1035, 133, Fig. 4.7; Ex. 1003 ¶¶ 261–263). Petitioner contends that the combination of Ellsberry and Halbert "would have provided nothing more than expected at the time," namely, "providing an operational interface to bidirectional data busses 234 and 236." *Id.* at 47 (citing Ex. 1003 ¶ 264).

Petitioner's reasons to combine Ellsberry and Halbert, and Patent Owner's arguments against the combination, are addressed below.

a) Reducing Bus Conflicts

Petitioner contends that one of ordinary skill in the art would have considered it obvious to use Halbert's tristate buffers to interface with Ellsberry's bidirectional buses to eliminate bus conflicts in accordance with standard protocols. Pet. 46 (citing Ex. 1003 ¶¶ 257–264); *see also id.* at 78, 81.

We agree with Petitioner that one of ordinary skill in the art would have combined Ellsberry and Halbert to avoid bus conflicts. Pet. 46(citing Ex. 1003 ¶¶ 257–264). Ellsberry discloses embodiments which enable only one of its ports at a time by enabling or disabling bidirectional drivers 402, 404 as appropriate. Ex. 1005 ¶¶ 31, 40. A person of ordinary skill in the art would have understood that the drivers on a bidirectional bus need to be turned off to allow other devices to drive data on that bus without creating a conflict. Ex. 1003 ¶¶ 239–240, 260; Ex. 1035, 89–90. Hence, Ellsberry's drivers 402, 404 implementing Halbert's tristate buffers 126, 128, when selectively operated as high or low, or high-impedance, states, prevent data on buses 234 and 236 being output simultaneously onto the "fork in the

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road" during a read operation (in the opposite direction of the blue arrow in the previous figure). *Id.* at 45–46 (citing Ex. 1003 ¶¶ 257–264). The additional Halbert tristate buffer 122 which interfaces with the memory controller bus 230 prevents bus conflicts with other memory modules attached to the memory controller bus. Ex. 1006, Fig. 4 [122]; Ex. 1006, 7:54–61; Ex. 1003 ¶ 259. Accordingly, we agree with Petitioner that one of ordinary skill in the art would have seen the benefit of combining Ellsberry and Halbert to avoid bus conflicts.

Patent Owner and its expert argue that bus conflicts are not a concern for write operations, but only for read operations where data from different groups of memory ranks could collide on the data bus 230. Resp. 55–58, 66 (citing Pet. § VI.A.3(a); Ex. 2006, 188:17–189:2, 189:5–12, 189:13–17, 189:22–190:16; Ex. 2007, 68:16–20, 69:16–19, 70:20–23, 72:19–22, 114:9–22; Ex. 2005 ¶ 128); Sur-Reply 27. Since the claims are directed to write operations, Patent Owner argues that conflicts in read scenarios would not motivate the combination. Sur-Reply 27 (citing Resp. 55–58; Reply 31).

In cases where there is a known problem and the proposed combination is a predictable solution to it, a reason to combine has been shown. *See KSR*, 550 U.S. at 420 (placing a sensor on a nonmoving point was a predictable solution to known wire-chafing problem); *Intel v. Qualcomm Inc.*, 21 F.4th 784, 799 (Fed. Cir. 2021) (a reference's switch was a known solution to a feedthrough problem). Petitioner has demonstrated that the problem of bus conflicts was known in DIMMs, and that tristate buffers were a solution to it. Pet. 78 (citing Ex. 1035, 89–90); Ex. 1003 ¶¶ 239–240, 264, 366, 373. Using Halbert's tristate buffers in Ellsberry

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amounts to combining familiar elements according to known methods to yield predictable results. *KSR*, 550 U.S. at 416.

b) Reducing Load

Petitioner contends that one of ordinary skill in the art would have combined Halbert and Ellsberry, which each teach to reduce the load experienced by the memory controller to a single load rather than the loads of multiple ranks of memories. Pet. 45–46 (citing Ex. 1005 ¶¶ 6–9, 12, 45, Fig. 4; Ex. 1006, 3:67–4:5, 4:18–22, Fig. 4; Ex. 1001, 4:27–47, Fig. 5; Ex. 1003 ¶¶ 257–264).

Patent Owner contends that Ellsberry was already capable of tristate functionality in order to present a single load, and that a person of ordinary skill in the art would have considered it redundant to combine the disclosures of Ellsberry and Halbert. Resp. 68 (citing Ex. 2005 ¶ 121; *South-Tek Sys., LLC v. Engineered Corrosion Sols.*, LLC, 748 F.App'x 1003, 1007 (Fed. Cir. 2018)); Sur-Reply 29–30. Patent Owner contends that Petitioner has not met its burden to explain why a person of ordinary skill in the art would have included the tristate functionality in Ellsberry's bidirectional signal drivers 402, 404. Resp. 68.

We agree with Petitioner and its expert, Dr. Subramanian, that Ellsberry discloses that its memory bank switch includes signal drivers to present a single load to a bus coupled to the memory bank switch, but does not provide the details of how that is done, such that one of ordinary skill in the art would have looked to Halbert for details concerning implementing Ellsberry's bidirectional drivers with Halbert's tristate buffers to present a single load to the system memory controller. Pet. 46–47 (citing Ex. 1003

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¶¶ 257–264); Reply 31–32 (citing Ex. 2007, 104:25–106:8, 108:10–22, 109:17–113:4).

Although Patent Owner argues that Ellsberry and Halbert are redundant in teaching to provide a single load to the system memory controller, we do not think this would deter a person of ordinary skill in the art from combining the references. A person of ordinary skill in the art would be curious, naturally, how others solved this problem and would have been drawn to implement Ellsberry's bidirectional drivers with Halbert's tristate buffers. *Intel Corp. v. PACT XXP Schweiz AG*, 61 F.4th 1373, 1380 (Fed. Cir. 2023) (that the references address the same problem and one reference solves that problem through a different mechanism is a reason to combine under *KSR* and Federal Circuit precedent).

To the extent that Patent Owner argues that the memory-controller-side tristate buffer 122 interfacing with bus 230 is redundant to the memory-side tristate buffers 126, 128, we find a person of ordinary skill in the art would have understood that the tristate buffer 122, in the high-impedance state, prevents the bus 230, and hence the system memory controller, from experiencing the load imposed by the circuitry in the data buffer between tristate buffer 122 and tristate buffers 126, 128. Ex. 2007, 110:24–111:6. It would also enable more exact timing of enabling and disabling the tristate buffers 122, 126, 128 as data traverses the memory buffer, which would pass through buffer 122 and buffers 126, 128 at slightly different times. Ex. 1006, Figs. 4, 6 [e.g., compare timing of DQ, MDQ, DQ0/DQ1, RDQ0_IN, RDQ0_OUT, RDQ1], 6:66–7:30. In addition, it would prevent the system memory controller from experiencing the memory module's load when communicating with other memory modules on system bus 230. *See*

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Ex. 1003 ¶¶ 241, 259, 374, 399; Ex. 1006, Figs. 4, 6, 9, 6:66–7:6, 8:10–18 (memory module is activated by Active command). In addition, Halbert's Figure 4 teaches the person of ordinary skill that the tristate buffers should be arranged in this way. Ex. 1006, 4:60–62 (bidirectional buffer 122 is connected to the system memory data bus). Consequently, a person of ordinary skill in the art would have had reason to add Halbert's tristate buffer 122 to interface with Ellsberry's bus 230.

c) Saving Power by Disabling Write Drivers

Petitioner contends that a person of ordinary skill in the art "would have . . . understood that driving the data busses only for an interval as necessary for transmitting [a] burst of data according to the JEDEC protocol would . . . save power, thus further motivating her to follow those timing protocols in accordance with [Halbert's] disclosure." Pet. 81 (citing Ex. 1003 ¶ 366). Petitioner contends that the combination of Ellsberry and Halbert "would be well within the level of skill at the time, since the JEDEC standards were designed to be implemented by memory systems at the time." *Id.* (citing Ex. 1003 ¶ 367).

Patent Owner argues that Halbert does not mention power concerns and leaves the write path enabled between memory operations, and that Petitioner's expert, Dr. Subramanian, presents no analysis of the amount of power savings achieved to justify making the combination. Resp. 4 (citing Ex. 1006, Fig. 6; Ex. 2005 ¶¶ 104–108; Ex. 1003 ¶ 366), 47 (citing Ex. 2007, 72:5–8; Ex. 2005 ¶ 107), 58–59; Sur-Reply 28–29.

In Reply, Petitioner argues that it would have been obvious to use Halbert's tristate buffers (elements 122, 126, 128 in Figure 4) to enter the high impedance state whenever not actively sending data to save power.

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Reply 25 (citing Ex. 2007, 14:11–22, 17:21–19:12, 24:5–26:24, 37:9–24, 57:1–58:2; *see also* Ex. 1092, 123:16–125:11). Petitioner contends that Figures 3, 5, and 6 of Halbert disclose that "the data paths are actively driven only during the data bursts." *Id.* (emphasis omitted) (citing Ex. 1003 ¶ 362; Pet. 79–80). Petitioner further contends that the motivation to save power "need not be found in the references sought to be combined, but may be found in any number of sources, including common knowledge, the prior art as a whole, or the nature of the problem itself." Reply 26 (emphasis omitted) (citing *DyStar Textilfarben GmbH v. C.H. Patrick Co.*, 464 F.3d 1356, 1361 (Fed. Cir. 2006)). Petitioner contends that Patent Owner's expert concedes that power savings were a concern with devices such as laptop computers implementing DDR2 and DDR3 memory modules. *Id.* (citing Ex. 2013, 5; Ex. 1092, 123:16–23, 124:13–20, 125:2–11; Ex. 2010, 2). Petitioner argues that its expert, Dr. Subramanian, explained that buffers should be placed in a high-impedance state when not actively driving data because otherwise the total energy that will be lost would be significant. *Id.* at 26–27 (citing Ex. 2007, 59:7–60.8, 120:12–121:7, 121:19–122:11; Ex. 1003 ¶¶ 366, 422, 662). According to Petitioner, he quantified the total energy lost as "the capacitance of the line multiplied by the voltage to which it is charged, squared and multiplied by half, approximately." *Id.* at 26–27 (quoting Ex. 2007, 60:4–8).

In Sur-Reply, Patent Owner contends that "[n]o prior art references taught . . . enabling the data path only for [a] burst period would save a sufficient amount of power to be desirable." Sur-Reply 28. Patent Owner further asserts that "[t]he argument also does not address the lack of

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teaching, or reasonable expectation of success in timing the enablement of the data paths correctly." *Id.* (citing Ex. 2013, 5; Ex. 2021, 37, 43).

Petitioner's and Patent Owner's experts agree that at least in some applications (e.g., laptop computers), one of ordinary skill in the art would have considered power savings an important priority in the design of a memory module. Ex. 1003 ¶¶ 366, 422, 662; Ex. 2007, 18:8–18, 37:20–24, 57:1–10; Ex. 1092, 123:16–125:11; Ex. 2013, 5; Ex. 2010, 2. The record thus establishes that excessive power consumption was a known problem in the art. The record further establishes that Halbert's tristate buffers in the high-impedance state would have been effective in saving power when a memory module was not actively conducting a read or write operation. Ex. 1003 ¶ 366; Ex. 2007, 18:8–18, 27:21–25, 37:20–24, 57:1–10; Ex. 1092, 123:16–125:11.

We do not agree with Patent Owner's argument that the references must teach the problem of power consumption and describe a way of addressing it in order for one of ordinary skill in the art to combine the references. Resp. 4, 47; Sur-Reply 28. The case here is similar to *KSR* and *Qualcomm* where a predictable solution to a known problem was found obvious. *See KSR*, 550 U.S. at 420; *Qualcomm*, 21 F.4th at 799, *supra*.

As to Patent Owner's argument that Petitioner's expert did not show that the amount of power savings achieved would be significant enough to justify implementing Ellsberry's bidirectional drivers with Halbert's tristate buffers, we do not agree. Resp. 4, 47; Sur-Reply 28. Both Petitioner's and Patent Owner's experts agree that power savings would have been desired for memory modules by a person of ordinary skill in the art. Ex. 1003 ¶¶ 366, 422, 662; Ex. 2007, 18:8–18, 37:20–24, 57:1–10; Ex. 1092,

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123:16–125:11; Ex. 2013, 5; Ex. 2010, 2. The evidence shows that putting the tristate buffers in high impedance states and enabling only when necessary to drive data would have resulted in power savings, which would have been an improvement.

To the extent Patent Owner argues that Petitioner's expert's testimony is not supported by underlying facts and data as required (see 37 C.F.R. § 42.65(a)), we find that the record provides sufficient support. Resp. 4, 58–59. Petitioner's expert provided on the record the equation by which power consumption can be calculated. Ex. 2007, 60:4–8. In addition, the JEDEC standard indicates power savings are desirable by providing a "power-saving, power-down mode" in its DDR SDRAM specification. Ex. 1009, 1. We also note that a textbook in the record indicates that "excess power consumption means excess heat generation, higher operating cost, and perhaps the addition of a fan and air filter." Ex. 1035, 135. And Patent Owner's own expert agrees that power consumption is a problem that one of ordinary skill in the art would have recognized at the time of the '339 patent. Ex. 1092, 123:16–125:11. Petitioner shows that implementing Ellsberry's bidirectional drivers with Halbert's tristate buffers and adding an additional buffer similar to Halbert's tristate buffer 122 would have solved this problem. Ex. 2013, 5; Ex. 1092, 114:7–115:1, 123:16–23, 124:13–20, 125:2–11; Ex. 2010, 2. Accordingly, we do not agree with Patent Owner's argument.

We determine that the problem of saving power would have provided a reason for one of ordinary skill in the art to combine Halbert's tristate buffers with Ellsberry's bidirectional drivers with a reasonable expectation of success.

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d) Compatibility of Ellsberry and Halbert

Patent Owner argues that Ellsberry and Halbert have incompatible architectures. Resp. 60–64; Sur-Reply 30–31. According to Patent Owner, Halbert uses concurrent read/write operations in all memory ranks. Resp. 60 (citing Ex. 1006, 4:55–59). Patent Owner's expert contends that "Halbert's architecture is for a design in which all memory banks are enabled and no data paths are disabled." Ex. 2005 ¶ 134, *cited in* Resp. 61. In contrast, Patent Owner argues, "Petitioner's unpatentability theory requires Ellsberry to assume a configuration in which some data paths are disabled and only some memory banks can be accessed." Resp. 60–61 (citing Pet. 73–74, 102).

As we noted in our Institution Decision, Halbert teaches that "[*g*]*enerally*, multiple ranks will receive the same address and commands, and will perform memory operations with the interface circuit concurrently." Inst. Dec. 28–29 (citing Ex. 1006, 4:57–59). Halbert's use of the word "generally" means that it is not always the case that memory ranks perform memory operations concurrently. Inst. Dec. 28–29. Thus, as shown in Halbert's Figure 4, memory module 100 may receive data DQ of *m* bits from the memory controller and store them in either rank 140 or 142 in a write operation, or may transmit data DQ of *m* bits to the memory controller after reading them from rank 140 or 142 in a read operation. Ex. 1006, 4:49–57. We agree with Petitioner that Patent Owner's expert attempts to redefine the term "generally" in Halbert to mean "manufacturing variances," when the word clearly refers to multiple ranks receiving the same address and commands in the same sentence. Reply 33. Our opinion has not changed that replacing Ellsberry's bidirectional drivers with Halbert's tristate buffers

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is merely "combining familiar elements according to known methods to yield predictable results." Inst. Dec. 28 (citing *KSR*, 550 U.S. at 416).

e) Omission of Halbert's MUX/DeMUX from the Combination

Petitioner contends that a person of ordinary skill would have understood that Halbert's MUX would not be needed in Ellsberry. Pet. 46 (citing Ex. 1003 ¶ 262; Ex. 1005 ¶ 46, Fig. 7; Ex. 1006, 5:66–6:65, 7:7–13, Figs. 5–6). Petitioner's contention is supported by Dr. Subramanian, who states a person of ordinary skill in the art would have understood that the functionality of Halbert's MUX/DeMUX 124 is not necessary in Ellsberry. Ex. 1003 ¶ 262.

Patent Owner does not dispute Petitioner's contention that Halbert's MUX would not be needed in Ellsberry. *See* Resp.

In the absence of contrary evidence, we accept Petitioner's contention that one of ordinary skill in the art would have omitted Halbert's MUX/DeMUX in making the combination.

f) Latency Differences Between Memory Devices and Modules

Patent Owner argues that SDRAM device latency and module latency are different things, and that without the inventor of the '339 patent's teaching, one would not have known how to time the enablement or disablement of a data path in a data buffer. Resp. 49–50 (citing Ex. 2009, 27).

Petitioner contends that Patent Owner's argument relates to unloaded latency when the system is idle, and loaded latency when a memory module is saturated with memory requests. Reply 30 (citing Ex. 2009, 15; Ex. 1092, 246:19–247:5). Petitioner contends that those latencies are not the latency

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relevant here, which is the CAS latency (including CAS latency (CL) and Posted CAS latency or Additive latency (AL)) which is configured during initialization and does not change during normal operation. *Id.* We agree with Petitioner that the latencies Patent Owner mentions do not relate to the CAS latency at issue in this case. Patent Owner's argument does not undermine Petitioner's combination.

g) Predictability of Latency through Data Buffer

Patent Owner argues that latency through a data buffer varies in a complex and unknown manner such that one of ordinary skill in the art "would not have had a reasonable expectation of success to achieve the correct timing and synchronization for the data buffer data path needed for the modification." Resp. 3, 50–51; Sur-Reply 7–11 (citing Ex. 1085; Ex. 1092, 49–64; Ex. 2007, 227:1–20, 254:2–5; Ex. 2012, 2, 5–7; U.S. Patent No. 8,787,060, 18:31–37, Figs. 6A–6B; Ex. 2008, Figs. 5–6; Ex. 2009, 27; Ex. 2020, 1–2; Ex. 1006, 7:37–41, Fig. 7; Ex. 2005 ¶¶ 92–94); *see also* Sur-Reply 25–26.

Petitioner disagrees and argues that U.S. Patent No. 7,532,537 ("'537 patent") teaches that if there is a data buffer on the module, then including "one additional clock cycle" in the CAS latency can provide sufficient time budget for the data buffer to perform its functions while still complying the timing requirements shown in the JEDEC standards. Reply 9–10 (Ex. 1014, 21:28–52; Ex. 1092, 174:8–175:21, 179:14–181:6).

Petitioner further argues that Ellsberry teaches to include one additional clock cycle in the CAS latency for the data buffer to perform its functions while still complying with JEDEC's timing requirements. Reply 10 (citing Ex. 1005, Fig. 8B, n.1; Ex. 2007, 181:9–182:22, 204:11–205:24,

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230:25–234:16; Pet. 36–37, 75–78).

Petitioner contends Halbert is even more detailed and provides precise timing diagrams for the data buffer while teaching compliance with JEDEC's timing requirements for a DIMM without a data buffer (such as a Registered DIMM ("RDIMM")). *Id.* at 10–11 (citing Pet. 78–81; Ex. 1003 ¶¶ 196–198; Ex. 1006, 3:42–57, 6:1–4, Figs. 5–6; Ex. 1092, 279:15–280:6).

Although Patent Owner argues that it was learned after the '339 patent that shorter stubs and traces would reduce latency (Sur-Reply 9), Patent Owner does not dispute that adding an additional clock cycle, as taught by the '537 patent, Ellsberry, and Halbert, would be sufficient to address latency through a data buffer, as Petitioner proposes. *See* Reply 6–11. Consequently, Patent Owner's argument fails to show that a person of ordinary skill in the art would not have had a reasonable expectation of success in arriving at the '339 patent's claims.

h) Conclusion on Motivation to Combine

Petitioner has shown that one of ordinary skill in the art would have reasons to combine Ellsberry and Halbert. Specifically, one of ordinary skill in the art would have looked to Halbert for details on how Ellsberry's bidirectional drivers would be implemented using Halbert's tristate buffers. In addition, one of ordinary skill in the art would have been led to add a buffer to Ellsberry similar to Halbert's buffer 122 to receive and drive signals on the interface with the system memory controller. One of ordinary skill in the art would have appreciated that the Ellsberry-Halbert combination would have reduced or eliminated bus conflicts, presented a single load to the system memory controller, and would have saved power

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by not expending it unless actively executing a read or write operation, notwithstanding Patent Owner's arguments to the contrary.

Accordingly, Petitioner has shown by a preponderance of the evidence that one of ordinary skill in the art would have combined Ellsberry and Halbert with a reasonable expectation of success.

4. Claim 1

Petitioner contends that claim 1 of the '339 patent is unpatentable over the combination of Ellsberry and Halbert. Pet. 47–86. We consider Petitioner's contentions for each limitation of claim 1 shown below.

a) Preamble 1pre

The preamble of claim 1 recites:

> [1pre] A N-bit-wide memory module mountable in a memory socket of a computer system and configurable to communicate with a memory controller of the computer system via address and control signal lines and N-bit wide data signal lines, the N-bit wide data signal lines including a plurality of sets of data signal lines, each set of data signal lines is a byte wide, the memory module comprising:

Ex. 1001, 19:9–15. Petitioner contends that Ellsberry teaches an N-bit wide memory module 106 mountable via DIMM interface 202 in a memory socket of computer system 100, which is configured to communicate address and control signals with processing unit 102 via communication path 110. Pet. 47–48 (citing Ex. 1005, Figs. 1–3, 5, 6). Petitioner contends that Ellsberry teaches that the N-bit with data signal lines include sets of data signal lines (9 sets) with each set a byte wide (8 bits). *Id.* at 48–49 (citing Ex. 1005 ¶¶ 2, 3, 11, 14, 23, 26–30, 34, Figs. 1, 2 (data buses 230, 232), 5, 6; Ex. 1003 ¶¶ 267–278).

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Patent Owner does not dispute that Ellsberry teaches the preamble of claim 1. *See* Resp.

Petitioner shows that Ellsberry teaches the preamble of claim 1. Accordingly, we need not address whether the preamble is limiting. *See, e.g.*, *Catalina Marketing Int'l, Inc. v. Coolsavings.com, Inc.*, 289 F.3d 801 (Fed. Cir. 2002).

b) Limitation 1a

Limitation 1a of claim 1 of the '339 patent recites "a printed circuit board (PCB) having an edge connector comprising a plurality of electrical contacts which are positioned on an edge of the PCB and configured to be releasably coupled to corresponding contacts of the memory socket." Ex. 1001, 19:16–20. Petitioner contends that Ellsberry alone or combined with Halbert teaches the claimed PCB. Pet. 49–51 (citing Ex. 1003 ¶¶ 279–295). Specifically, Petitioner contends that Ellsberry teaches a substrate 502/602 with an edge interface 506. *Id.* at 49–50 (citing Ex. 1005 ¶¶ 2, 21, 27, 28, 47, 50, claim 10, Figs. 5, 6). Petitioner also contends that Halbert teaches that its DIMM is a circuit board with an edge connector with contacts releasably connecting to corresponding contacts of a memory socket. *Id.* at 50–51 (citing Ex. 1006, 2:3–14, Figs. 1, 8; Ex. 1003 ¶¶ 288–295).

Patent Owner does not dispute Petitioner's contention that Ellsberry alone or combined with Halbert teaches limitation 1a of claim 1. *See* Resp.

Petitioner shows that Ellsberry alone and combined with Halbert teach limitation 1a of claim 1.

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c) Limitation 1b

Limitation 1b of claim 1 of the '339 patent recites "double data rate dynamic random access memory (DDR DRAM) devices coupled to the PCB and arranged in multiple N-bit-wide ranks." Ex. 1001, 19:21–23. Petitioner contends that Ellsberry discloses DDR DRAM devices 512 coupled to substrate 502/602 that are arranged in nine 8-bit memory devices, or nine pairs of 4-bit memory devices. Pet. 51–54 (citing Ex. 1005 ¶¶ 3, 26, 30–32, 40, 46, 47, Figs. 2, 5, 6, 11, 13; Ex. 1003 ¶¶ 296–305).

Patent Owner does not dispute Petitioner's contention that Ellsberry teaches limitation 1b of claim 1. *See* Resp.

Petitioner shows that Ellsberry teaches limitation 1b of claim 1.

d) Limitation 1c1

Limitation 1c1 of claim 1 of the '339 patent recites

> a module controller coupled to the PCB and operatively coupled to the DDR DRAM devices, wherein the module controller is configurable to receive from the memory controller via the address and control signal lines input address and control signals for a memory write operation to write N-bit-wide write data from the memory controller into a first N-bit-wide rank of the multiple N-bit-wide ranks, and to output registered address and control signals in response to receiving the input address and control signals.

Ex. 1001, 19:24–33. Petitioner contends Ellsberry teaches controllers (e.g., ASIC 204 and controllers 300, 510, 604, 1102, 1104, 1302) connected to PCB 502, 602 and operatively connected to DDR DRAM memory devices 512. Pet. 55–61. Petitioner further contends the controllers receive address and control signals System Address/CMD from processing unit 102. *Id.* at 56. Petitioner further contends the input and address signals are for a write operation to write N-bit-wide write data from the processing unit 102 into

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one of the multiple N-bit-wide ranks and to output registered address and command signals on bus 220 in response to the received input address and control signals from the processing unit. *Id.* (citing Ex. 1005 ¶¶ 3, 10, 11, 29, 20, 36, 39, 40, 42, 45, 47, Figs. 2, 3, 5, 6, 8, 11, 13; Ex. 1003 ¶¶ 306–318).

Patent Owner does not dispute Petitioner's contentions with respect to limitation 1c1 of claim 1. *See* Resp.

Petitioner shows that Elsberry teaches limitation 1c1 of claim 1 of the '339 patent.

e) Limitation 1c2

Limitation 1c2 of claim 1 of the '339 patent recites "wherein the registered address and control signals cause the first N-bit-wide rank to perform the memory write operation by receiving the N-bit-wide write data, wherein the module controller is further configurable to output module control signals in response to at least some of the input address and control signals." Ex. 1001, 19:33–39. Petitioner contends that Ellsberry teaches that the registered address and control signals on bus 220 cause bank 1 to perform a memory write operation under control of control ASIC 204. Pet. 61–65. Specifically, the control ASIC 204 outputs control signals on bus 210 in response to the input address and control signals from processing unit 102 to cause N-bit-wide write data to be written to Bank 1. Pet. 61 (citing Ex. 1005 ¶¶ 29–31, 39, 42, 52, Figs. 2–4, 8A, 11, 13; Ex. 1003 ¶¶ 319–326).

Patent Owner does not dispute Petitioner's showing with respect to limitation 1c2 of claim 1. *See* Resp.

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Petitioner shows that Ellsberry teaches limitation 1c2 of claim 1 of the '339 patent.

f) Limitation 1d1

Limitation 1d1 of claim 1 of the '339 patent recites "a plurality of byte-wise buffers coupled to the PCB and configured to receive the module control signals." Ex. 1001, 19:53–55. Petitioner contends that in Ellsberry switch ASICs 206 and 208, device 400 and bank switches 1106 and 1304 are byte-wise buffers coupled to PCB 502, 602 and are configured to receive module control signals from the control ASIC on control bus 210. Pet. 65–67 (citing Ex. 1005 ¶¶ 29, 30, 45, 47, Figs. 2–6, 11, 13; Ex. 1003 ¶¶ 327–333).

Patent Owner does not dispute Petitioner's showing that Ellsberry teaches limitation 1d1 of claim 1. *See* Resp.

Petitioner shows that Ellsberry teaches limitation 1d1 of claim 1 of the '339 patent.

g) Limitation 1d2

Limitation 1d2 of claim 1 of the '339 patent recites

> wherein each respective byte-wise buffer of the plurality of byte-wise buffers has a first side configured to be operatively coupled to a respective set of data signal lines, a second side that is operatively coupled to at least one respective DDR DRAM device in each of the multiple N-bit-wide ranks via respective module data lines, and a byte-wise data path between the first side and the second side.

Ex. 1001, 19:40–49. Petitioner contends that Ellsberry teaches that the byte-wise buffer is the switch ASIC 206, 208 which is connected on a first side to the data buses 230, 232 coupled to DIMM interface 202, 230, DQ(3:0), DQ(7:4) and a second side that is operatively coupled to at least one DDR

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DRAM device in each of the multiple N-bit wide banks via data bus 234, 236 (Figs. 2, 4), and "/4" (Fig. 11) and "/8" (Fig. 13). Pet. 68–71. Petitioner further contends Ellsberry teaches a byte-wise data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) (Figs. 2, 4) or the 8-bit data path between DQ(3:0)/DQ(7:4) (Figs. 11, 13). *Id.* at 68–71 (citing Ex. 1005 ¶¶ 29, 47, 50, Figs. 2, 5, 6, 11–13; Ex. 1003 ¶¶ 343–347).

Patent Owner does not dispute Petitioner's showing with respect to limitation 1d2 of claim 1. *See* Resp.

Petitioner shows that Ellsberry teaches limitation 1d2 of claim 1 of the '339 patent.

h) Limitation 1d3

Limitation 1d3 of claim 1 of the '339 patent recites

> wherein the each respective byte-wise buffer is disposed on the PCB at a respective position corresponding to the respective set of the plurality of sets of data signal lines.

Ex. 1001, 19:49–52. Petitioner contends that Ellsberry discloses limitation 1d3. Pet. 71–73 (citing Ex. 1003 ¶¶ 343–347). Specifically, Petitioner contends that "wherein the each respective byte-wise buffer is disposed on the PCB" is disclosed by Ellsberry's switch ASIC 206, 208 in Fig. 2, memory bank switch 508 in Figures 5 and 6, and bank switch 1106 in Figure 11, and substrates 502 and 602 in Figures 5 and 6. *Id.* at 71. Petitioner contends that "at a respective position corresponding to the respective set of the plurality of sets of data signal lines" is disclosed by Ellsberry's data buses 230, 232 in Figure 2. *Id.* at 71–73 (citing Ex. 1003 ¶ 343–347; Ex. 1005 ¶¶ 29, 47, 50, Figs. 2, 5, 6, 11–13; Ex. 1010, 8–9 (showing edge pin assignment to data line sets pins); Ex. 1062, 25–26)).

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Patent Owner does not dispute Petitioner's showing with respect to limitation 1d3 of claim 1. *See* Resp.

Petitioner shows that Ellsberry teaches limitation 1d3 of claim 1 of the '339 patent.

i) Limitation 1e

Limitation 1e of claim 1 of the '339 patent recites

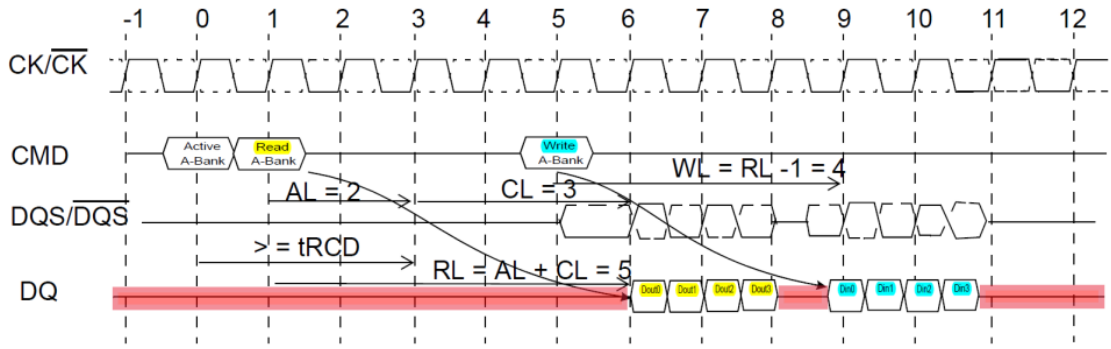
> wherein the each respective byte-wise buffer further includes logic configurable to control the byte-wise data path in response to the module control signals, wherein the byte-wise data path is enabled for a first time period in accordance with a latency parameter to actively drive a respective byte-wise section of the N-bit wide write data associated with the memory operation from the first side to the second side during the first time period.

Ex. 1001, 19:53–61. Petitioner contends that Ellsberry alone or combined with Halbert teaches limitation 1e of claim 1. Pet. 73–81. Specifically, Petitioner contends that Ellsberry discloses that switch ASIC 206, 208, 400 includes a control block including read/write logic 406 ("logic") to control the 8-bit data path between data bus 230 and either data bus 234 (Port A) or data bus 236 (Port B) in response to module control signals on bus 210. *Id.* at 73. Petitioner contends that the byte-wise data path is enabled through Port B and disabled through Port A, or vice versa, for a "first time period" in accordance with a "latency parameter," Posted CAS_n (Fig. 9), to actively drive through the combination's bidirectional drivers (tristate buffers) a respective byte-wise section of the N-bit wide write data from the first side (data bus 230) to the second side (data bus 234 or 236). Pet. 73–75 (citing Ex. 1005 ¶¶ 11, 29, 31, 39, 40, 44–46, 50, Figs. 2, 4, 9; Ex. 1003 ¶¶ 348–368).

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Petitioner contends the "first time period" relates to a data burst under the JEDEC standards which starts in accordance with the latency parameters (AL and CL) and has a duration in accordance with a burst length parameter (BL). Pet. 74 (citing Ex. 1003 ¶¶ 348–368). Petitioner contends that the latency parameters include the Posted CAS latency (AL) and CAS latency (CL). *Id.* at 77 (citing Ex. 1003 ¶¶ 352, 363).

Petitioner presents the following timing diagram, Figure 21, from the JEDEC standard, annotated by Petitioner, to explain these latencies.



[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Figure 21 — Example 1: Read followed by a write to the same bank, where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4

Reply 8 (citing Ex. 1011, 22; Ex. 1092, 43:21–44:2, 91:7–92:16, 93:4–14); *see also* Pet. 76–78. As shown in the annotated Figure 21 above, the JEDEC standard provides a delay between assertion of the command CMD and the strobing of data DQ of RL=AL+CL= 5 clock cycles for a read operation, and WL=RL–1=4 clock cycles for a write operation.

Petitioner contends that Ellsberry teaches including one additional clock cycle in the CAS latency for the data buffer to perform its functions while still complying with JEDEC's timing requirements. Reply 10 (citing Ex. 1005, Fig. 8B, n.1; Ex. 2007, 181:9–182:22, 204:11–205:24, 230:25–234:16; Pet. 36–37, 75–78).

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Petitioner contends that, to the extent Ellsberry alone does not teach limitation 1e, it would have been obvious in view of Halbert. The combination of Ellsberry and Halbert was shown and discussed above in Section II.D.3. Petitioner contends that Halbert teaches using preset latency parameters for timing data transfer bursts and that the data paths are driven only during the data bursts. Pet. 79 (citing Ex. 1006, 1:51, 2:46–60, 6:66–67, 9:55–65, Figs. 3–6; Ex. 1003 ¶ 362). Petitioner contends that Halbert further provides precise timing diagrams for the data buffer while teaching compliance with JEDEC's timing requirements. Reply 10–11 (citing Ex. 1003 ¶¶196–98; Ex. 1006, 3:42–3:57, 6:1–4; Ex. 1092, 279:15–280:6). Petitioner contends that, in the combination "communication failures can be avoided on the shared bidirectional data busses by following the JEDEC timing protocol and driving the bidirectional memory data busses for the duration of the data burst when forwarding the write data from the system memory controller to the memory device." Pet. 80.

(1) Enabling and Disabling Data Paths through the Data Buffer

Patent Owner argues that all of Ellsberry's embodiments keep the data paths enabled at all times, and thus do not enable any data paths in accordance with a latency parameter. Resp. 33–42; Sur-Reply 11–15. We agree with Patent Owner that Ellsberry discloses embodiments that use data masking or NOP commands that could function with data paths always enabled. However, we disagree with Patent Owner that Ellsberry is limited to embodiments with always-enabled data paths. As Petitioner contends, Ellsberry discloses "one port disabled" embodiments that use switch ASICs

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206, 208, 400 to enable or disable data paths to respective banks of memory devices. Pet. 73–74 (citing Ex. 1005 ¶¶ 30–31, 40, Figs. 2, 4).

Ellsberry is very clear that in certain embodiments, the control unit controls the bank switch (switch ASIC) to enable or disable Port A or Port B as appropriate for the memory address received by the control unit. Ex. 1005 ¶¶ 30–31, 40, Figs. 2, 4; Ex. 1003 ¶¶ 231, 358. The parties refer to this configuration as the "one-port disabled" embodiment. *See, e.g.*, Pet. 149; Resp. 13. Ellsberry's Figure 2 and related description shows that the Ports A and B are selectively enabled or disabled to output respective data bytes (Byte 0) and data strobe signals (DQS A0, DQS B0) on data buses 234, 236. *See* Ex. 1005 ¶ 31 ("[I]f the control unit 204 determines that a particular address is associated with, or mapped to, Bank 1212 coupled to memory bank switch 206, then it causes Port B to be activated and Port A to be disabled so that the data is written to the correct memory bank 212.").

Thus, we do not agree with Patent Owner's argument that Ellsberry is limited to always-enabled data paths.

(2) Using Bidirectional Drivers to Enable or Disable Data Paths

Patent Owner argues that Ellsberry does not disclose that Ellsberry's bidirectional drivers 402/404 enable or disable data paths. Resp. 40–43; Sur-Reply 17–21. However, as just explained, Ellsberry teaches "one port disabled" embodiments which selectively enable or disable Ports A and B of switch ASICs 206, 208, 400. Ex. 1005 ¶ 31. Ellsberry's Figure 4 shows that the only elements within the data processing unit 400 (part of the switch ASIC) that the data paths pass through are the bidirectional drivers 402, 404. *Id.* ¶ 45. This would suggest to one of ordinary skill in the art that the

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bidirectional drivers 402, 404 are what enables or disables data paths. Ex. 1003 ¶¶ 235, 355, 358; *see KSR*, 550 U.S. at 418 ("a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ"), 421 ("[a] person of ordinary skill is also a person of ordinary creativity, not an automaton"). Review of Halbert's Figure 4 and its bidirectional drivers 122, 126, 128 confirms that these tristate buffers would be used to enable or disable data paths between the system data bus and the buses connected to the respective ranks of memory devices. Ex. 1006, 4:60–64, 5:6–11, 5:51–65, Figs. 3, 5, 6.

Patent Owner argues that Ellsberry does not disclose enabling or disabling the data path by enabling or disabling drivers 402 and 404. Resp. 40–42. Patent Owner contends that Dr. Wolfe, Petitioner's expert in another case involving a different combination of prior art, stated that the bidirectional drivers 402 and 404 did not enable or disable data paths, but instead that pin drivers performed these functions. *Id.* at 41–42 (citing Ex. 2007, 225:12–25, 227:14–228:9, 228:11–25, 229:17–231:3); *see also* Ex. 2005 ¶ 47.

Ellsberry is clear that its memory bank switches 206 and 208 enable one data path to one of Ports A and B, and disable the other. Ex. 1005 ¶ 31. Although Patent Owner alleges that Dr. Wolfe states that pin drivers are what enable and disable data paths (Ex. 2007, 225:12–25), elsewhere, Dr. Wolfe is unequivocal that the bidirectional drivers 402 and 404 are what enable and disable data paths (Ex. 2007, 181:10–12 (Question: "And by 'switch,' which switch are you referring to?" Answer: "[bidirectional drivers] 402 and 404 act as a switch in Ellsberry.")). Petitioner's expert in this case, Dr. Subramanian, also states unequivocally that the bidirectional

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drivers 402 and 404 are what enables and disables data paths through the memory bank switches. Ex. 1003 ¶¶ 159, 239–240. Since Dr. Subramanian is testifying in this case, and Dr. Wolfe is not, we credit Dr. Subramanian's testimony over Dr. Wolfe's. In any case, there is no dispute between the parties that Halbert's tristate buffers would provide the capability to enable or disable data paths. Thus, we agree with Petitioner that Ellsberry's bidirectional drivers enable or disable the data paths through the data buffer. Reply 21 (citing Pet. 79–80; Ex. 1003 ¶ 362). To the extent there is any doubt as to what in Ellsberry's memory bank switch performs these functions, there is no dispute that Halbert's bidirectional buffer 122 and bidirectional data registers 126 and 128 have the capability to enable and disable data paths because they are illustrated in Figure 4 as symbols recognized in the art as tristate buffers. Ex. 1006, Fig. 4; Ex. 2007, 17:21–18:6. Halbert's Figure 6 shows a write operation with "don't care" states, which Patent Owner alleges to mean that the tristate buffers of Halbert's bidirectional buffer 122 and bidirectional data registers 126 and 128 are enabled during these times. However, Petitioner relies on the general knowledge of a person of ordinary skill of the art which includes the JEDEC standards, which show that the data DQ are disabled until the data DQ are output to the memory devices during a write operation. Ex. 1011, 6, 22. We agree with Petitioner that Ellsberry alone or in combination with Halbert, when viewed with the general knowledge of a person of ordinary skill in the art, teaches enabling and disabling data paths through the data buffer.

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(3) Use of Posted CAS Latency (AL) Parameter in Ellsberry's Switches

Patent Owner argues that Petitioner has not shown enablement of the data path is done for a first time period in accordance with a latency parameter to drive a byte-wise section of write data from the host side to the memory side of the data buffer. Resp. 33. Specifically, Patent Owner argues that Ellsberry does not use Posted CAS latency (AL) bits to control timing of the enablement of the data path across its switch ASIC. Resp. 34–36 (citing Ex. 1005 ¶ 44; Ex. 2005 ¶¶ 80–81; Ex. 2007, 122:16–126:24, 130:1–133:6, 238:9–244:3); Sur-Reply 27 (citing Ex. 1092, 263:3–15, 211:18–214:24). Patent Owner also argues that Ellsberry does not mention passing CAS latency (CL) bits to switch ASICs 206/208. Resp. 36–40 (citing Ex. 2007, 130:20–131:16, 134:20–135:21, 220:4–25, 229:4–230:11, 259:6–260:6; Ex. 1005 ¶¶ 29, 39, 44–45, Figs. 3, 8A; Ex. 2005 ¶¶ 86–90; Pet. 61–64, 74, 76, 98). We do not agree with Patent Owner's arguments.

Petitioner contends that Patent Owner's expert admitted that "CAS latency" is an example of a "latency parameter" within the meaning of limitation 1e. Reply 7 (citing Ex. 1092, 166:8–13). Petitioner contends that the JEDEC standards required setting CAS (CL) latency, Posted CAS (AL) latency, and burst length (BL) during initialization using respective mode register set (MRS) and extended MRS (EMRS) commands. *Id.* (citing Ex. 1011, 10–11; Ex. 1092, 69:6–70:10, 70:20–74:2, 74:7–76:1, 78:7–79:6, 80:8–24, 86:4–10, 86:25–87:18). Petitioner contends that once these latencies and burst length are set during initialization, they do not need to be changed during normal operation. *Id.* (citing Ex. 1092, 88:22–89:7, 90:3–91:6; Ex. 1041, 342). Accordingly, Petitioner argues that every read

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and write operation is performed "in accordance with" those "latency" parameters. *Id.* at 8.

Ellsberry teaches that instead of passing EMRS commands directly to the memory devices (SDRAMs), the memory module's control unit passes the commands to the memory bank switch where the values are stored. Ex. 1005 ¶ 44, Fig. 9, *cited in* Pet. 74. As shown in Ellsberry's Figure 9, the command and its parameters are squelched but the Posted CAS_n latency parameter is sent through to the memory bank switch. Ex. 1005 ¶ 44, Fig. 9. Ellsberry states that the squelch function allows the memory devices to be configured to operate in conjunction with the controller/switch devices and host system, rather than be directly programmed by the host system. *Id.* ¶ 44. Patent Owner seems to argue that the memory bank switch merely passes the Posted CAS_n latency parameter (AL) to the memory devices along with the burst length (BL) and CAS latency parameter (CL). Resp. 34 (citing Ex. 1005 ¶ 44; Ex. 2005 ¶¶ 80–81). But in paragraph 44, Ellsberry mentions the Posted CAS_n latency parameter (AL), not the burst length (BL) and CAS latency (CL). *Id.* ¶ 44. And Patent Owner does not explain why the memory bank switch would store the Posted CAS_n latency parameter if it did not use it. *Id.* We find that the memory bank switch is using the Posted CAS_n parameter for some purpose, as discussed below.

Petitioner contends that Ellsberry and the '339 patent disclose that their memory modules are compatible with JEDEC standards. Pet. 36–37 (citing Ex. 1005 ¶¶ 27, 44, 50, Fig. 9 ("Posted CAS_n"); Ex. 1001, 1:63–2:4, 3:35–41, 4:48–53, 5:4–8, 5:44–55, 9:31–36, 15:61–66 ("(CAS) latency"); EX1003 ¶¶ 247–250). In addition to the JEDEC standards, Petitioner relies on the '537 patent as providing general knowledge that a person of ordinary

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skill in the art would have known at the time of the '339 patent. Pet. viii; Reply 9–10; *see Koninklijke Philips N.V. v. Google LLC*, 948 F.3d 1330, 1337 (Fed. Cir. 2020) ("[T]he inquiry into whether any 'differences' between the invention and the prior art would have rendered the invention obvious to a skilled artisan necessarily depends on such artisan's knowledge."). The '537 patent is incorporated by reference in the '339 patent. Ex. 1001, 10:48–53; Ex. 1003 ¶ 46.

As shown in Figure 21 from the JEDEC standard, an annotated version of which is reproduced above in Section II.D.4.i, the JEDEC standards provide a read latency RL from when a read command is received by a memory module to when read data DQ is strobed by DQS, as well as a write latency WL from when a write command is issued to when write data DQ is strobed by DQS. Ex. 1011, 22. These latencies RL and WL depend upon the CAS latency CL and the Posted CAS latency (or additive latency) AL (RL=AL+CL; WL=AL+CL–1). Ex. 1011, 10–11; Ex. 1003 ¶ 352.

Petitioner contends that the Posted CAS latency (or additive latency) (AL) is in accordance with the claimed "latency parameter" which is set to account for the time needed for data to traverse the data buffer, which Petitioner contends is one clock cycle. Reply 10 (citing Ex. 1005, Fig. 8B, n.1; Ex. 2007, 181:9–182:22, 204:11–205:24, 230:25–234:16; Pet. 36–37, 75–78).

As correctly asserted by Petitioner (Reply 9–10), the '537 patent teaches that if there is a data buffer on the module, then one additional clock cycle in the overall CAS latency can provide sufficient time budget for the data buffer to perform its functions while still complying with the timing requirements for a registered DIMM, which has no data buffer. Ex. 1014

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(the '537 patent), 10:50–53, 21:28–53; Ex. 1092, 174:8–175:21, 179:14–181:6. Patent Owner contends that Ellsberry and the '537 patent are incompatible because Ellsberry allegedly subtracts—not adds as in the '537 patent—one clock cycle to comply with JEDEC timing requirements. Sur-Reply 13 (citing Ex. 2007, 182:4–183:24, 231:21–234:13; Ex. 1005, Fig. 8B; Reply 10). Specifically, the end of Ellsberry's Figure 8B indicates "NOTES" including "1. if cl_mode = subtract; cl= cl-1 to DDRs." Ex. 1005, Fig. 8B, n.1. According to Dr. Subramanian, Ellsberry's note means that

> the latency specified to the DDRs is reduced by 1 to account for the fact that there is one-cycle clock delay that's been added in. So the net result is, as far as system is concerned, it's showing the same effective latency.

Ex. 2007, 182:16–22.

We agree with Petitioner that the '537 patent teaches to add one clock cycle to account for propagation delay through a data buffer. Ex. 1014, 21:28–53. Primed with this teaching, a person of ordinary skill in the art would have implemented Ellsberry to budget one clock cycle to account for delay through the data buffer. Also, Dr. Subramanian states that Ellsberry's note should be understood as meaning that one cycle has been added to account for propagation delay through the data buffer so one cycle should be subtracted from the overall latency so that the system memory controller encounters the same delay it would have in the absence of the data buffer. Ex. 2007, 182:16–22.

Thus, considering the knowledge of a person of ordinary skill in the art, as evidenced by the teachings of the '537 patent, we find that a person of ordinary skill in the art would have understood that Ellsberry's Posted CAS latency parameter (Fig. 9) would have been useful to account for

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propagation delay through data buffers by adding a clock cycle to the latency period from receiving a write command to strobing the write data into a memory device. Ex. 1003 ¶ 363; Ex. 1014, 21:28–53; Ex. 2007, 182:16–22; Ex. 1092, 174:8–175:21, 179:14–181:6.

Thus, we do not agree with Patent Owner's arguments. As discussed above, Petitioner has established that Ellsberry's switch ASICs use Posted CAS latency (AL) bits to control timing of the enablement of the data path across its switch ASICs 206, 208, 400.

(4) FET Switches and Pin Drivers

Patent Owner contends that Ellsberry disclosed that FET switches and pin drivers were too slow to perform high-speed switching, so Ellsberry must leave the data paths enabled at all times. Resp. 12, 43 (citing Ex. 1005 ¶¶ 7–9, 57). As Petitioner notes, Ellsberry does not purport to use FET switches or pin drivers, but rather an integrated ASIC to perform switching at DDR and DDR2 speeds. Reply 19 (citing Ex. 1005 ¶ 57; Ex. 2007, 150:7–153:25, 224:7–226:13, 244:23–245:10, 247:11–249:3 (discussing Ex. 1084)). We agree with Petitioner that Ellsberry achieves high-speed switching because its switch is integrated in an ASIC, and that it does not use FET switches or pin drivers. *See* Ex. 1005 ¶ 57 (noting that FET "based switches are too slow for the required high-speed switching as their switching speed is too imprecise"). Patent Owner's argument does not undermine Petitioner's showing with respect to Ellsberry.

(5) Actively Driving Only During Data Bursts: Halbert's "Don't Care" States and JEDEC's High-Impedance States

Patent Owner next argues that Halbert does not disclose limitation 1e. Resp. 43–47; Sur-Reply 21–26. Specifically, Patent Owner argues that

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Halbert does not disclose the use of latency parameters for enabling write data paths. Resp. 44 (citing Ex. 2005 ¶ 114). Patent Owner contends that Halbert's write path is on by default and is only turned off when the module controller detects a read command and switches the direction signal to direct data to the memory devices. *Id.* at 45. Patent Owner contends that Halbert puts the data lines DQ in a high-impedance state only when a read operation is underway, but puts the data lines DQ in a "don't care" state which could be either high or low, but not high-impedance, before and after a write operation. *Id.* Patent Owner's expert, Dr. Brogioli, states that "Halbert's write path is enabled even when there are no memory operations." *Id.* at 45 (citing Ex. 2001 ¶ 104). Patent Owner also contends that an IBM application note (Ex. 2010) concerning DRAM operation and a datasheet (Ex. 2011) for a Texas Instruments JEDEC-compliant memory controller show similar "don't care" states associated with write operations. *Id.* at 46.

Petitioner contends that Halbert's Figures 3, 5, and 6 disclose that "the data paths are actively driven only during the data bursts" consistent with JEDEC timing for read and write operations that use latency parameters. Reply 21 (emphasis omitted) (citing Ex. 1003 ¶ 362; Pet. 79–80; Ex. 1092, 279:15–280:6, 281:10–20, 282:7–18). Petitioner argues that the shaded areas of Halbert's Figure 6 can be high-impedance states. *Id.* at 23. Petitioner further contends that the IBM application note that Patent Owner cites later explains that at the time when there is not a "write operation" or a "read operation," the "DQs are in a high impedance state . . . [which] prevents DQ contention [i.e., a collision] when two or more devices share the data bus." *Id.* at 23–24 (citing Ex. 2010, 2; Ex. 1092, 116:5–8, 117:10–19, 294:18–296:20, 297:10–21). Petitioner further contends that the

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JEDEC standard teaches that "[u]pon completion of a burst [of write data], assuming no other commands have been initiated, the DQs will remain High-Z." *Id.* at 24 (emphasis omitted) (citing Ex. 1009, 26; Ex. 1092, 119:2–18; Ex. 1009, 17; Ex. 1092, 119:22–120:10). Petitioner further contends that Figure 21 of the JEDEC standard shows the DQ data lines are put in a High-Z state—meaning the data path is disabled—except for times when there is a burst of data. *Id.* (citing Ex. 1011, 22; Ex. 1003 ¶ 352).

Although we agree with Patent Owner that Halbert's Figure 6 shows that DQ and MDQ are in "don't care" states at some points of a write operation, as Petitioner indicates, this does not preclude their being in a high-impedance state during those times. Reply 23. Both Ellsberry and Halbert indicate that at least some of their embodiments are compliant with the JEDEC standards. Ex. 1005 ¶ 50; Ex. 1006, 9:55–65. Figure 21 from the JEDEC standard, an annotated version of which is reproduced above in Section II.D.4.i, shows the JEDEC standard for write timing with flat lines highlighted in red before and after a write operation, which signify high-impedance states. Ex. 1011, 22; *see* Ex. 1009 (JEDEC DDR SDRAM Specification), 17 (noting that, for reads, "[u]pon completion of a burst, assuming no other commands have been initiated, the DQs will go High–Z"), 26 (noting that, for writes, "[u]pon completion of a burst, assuming no other commands have been initiated, the DQs will remain High–Z and any additional input data will be ignored").

There are only two options for the states of the data lines when a read or write operation is not underway: "don't care" per Halbert's Figure 6, or high impedance per Halbert's Figure 5 or the JEDEC timing diagram (Ex. 1011, 22). The Supreme Court has stated

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> When there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense.

KSR, 550 U.S. at 421. As Petitioner has shown, a person of ordinary skill in the art would have recognized that the high-impedance state would be useful in solving problems known in the art, e.g., avoiding bus conflicts, reducing load, and saving power. *See* Sects. II.D.3a–c.

Thus, considering all of the evidence, we determine that Patent Owner's arguments with respect to Halbert's "don't care" states do not undermine Petitioner's combination.

Therefore, Petitioner shows that Ellsberry alone or in combination with Halbert teaches limitation 1e of claim 1 of the '339 patent.

j) Limitation 1f

Limitation 1f of claim 1 of the '339 patent recites

> wherein the byte-wise data path includes first tristate buffers, and the logic in response to the module control signals is configured to enable the first tristate buffers to drive the respective byte-wise section of the N-bit wide write data to the respective module data lines during the first time period.

Ex. 1001, 19:62–67. Petitioner contends that Ellsberry alone or combined with Halbert teaches limitation 1f of the '339 patent. Pet. 81–86. Specifically, Petitioner contends Ellsberry alone or combined with Halbert teaches that the data path through Port A or Port B within bidirectional drivers 402, 404 (Ellsberry Fig. 4) and the control block (Ellsberry Fig. 4) in response to module control signals on bus 210 are configured to enable tristate buffers (Halbert Fig. 4) to drive the byte-wise section of the N-bit

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wide write data to the respective module lines 234 or 236 (Ellsberry Figures 2, 4) during a first time period corresponding to burst and latency parameters. *Id.* at 81–82 (citing Ex. 1005 ¶¶ 31, 45, Figs. 2, 4, 8A; Ex. 1003 ¶¶ 369–377). Petitioner contends that given the data buses are bidirectional, it would have been obvious to implement Ellsberry's bidirectional drivers 402, 404 (Fig. 4) using tristate buffers. *Id.* at 83 (citing Ex. 1003 ¶¶ 372–373).

To the extent Ellsberry does not sufficiently teach limitation 1f, Petitioner contends that it would have been obvious to implement bidirectional drivers 402, 404 using a similar arrangement with Halbert's tristate buffers. Pet. 84–85 (citing Ex. 1005, Fig. 4 (Ellsberry and Halbert combined); Ex. 1006, Fig. 4). Petitioner contends that, to drive the write data onto module data lines 236 on Port B, the control block must enable the tristate buffer in bidirectional driver 404 in the write direction during the first time period. *Id.* at 86 (citing Ex. 1003 ¶ 376).

(1) Enablement of Tristate Buffers by Logic in Response to Module Control Signal

Patent Owner argues that the combination of Ellsberry and Halbert does not disclose or suggest limitation 1f of claim 1 of the '339 patent. Resp. 65–69; Sur-Reply 31. Specifically, Patent Owner argues that Petitioner has not shown that enablement of tristate buffers was by the logic in response to a module control signal, or "what signals in particular" enable the tristate buffers in Ellsberry's switch ASIC. *Id.* at 65–66.

As Petitioner indicates, Ellsberry's Figure 2 includes a bus 210 (called the "ASIC PIPE" in Figures 11 and 13), which provides signals from the control ASIC 204 that control logic inside of switch ASIC 206 to enable and

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disable the tristate buffers in the switch ASIC. Reply 33–34 (citing *id.* at 2, 14–20; Ex. 1062, 21–23, 69–71). Although Ellsberry's Figure 4 does not show control signals from the control block to the bidirectional drivers 402, 404, one of ordinary skill in the art would have understood, as shown in Ellsberry's Figure 2, that the clock signals to drive the D-flip-flops of bidirectional drivers 402, 404 are coming from control ASIC 204 on control bus 210. Ex. 1005 ¶ 29 ("The control unit 204 is communicatively coupled to the dual memory bank switches 206 & 208 via control bus 210 and indicates to the memory bank switches 206 & 208 how data from the DIMM interface 202 should be received and/or stored."); Ex. 1003 ¶¶ 357–358, 376.

Thus, Patent Owner's argument does not undermine Petitioner's showing.

(2) Modifying Ellsberry's Bidirectional Drivers 402/404 to Include Tristate Buffers

Patent Owner argues that Petitioner has not shown why a person of ordinary skill in the art would have modified Ellsberry's bidirectional drivers 402, 404 to include tristate buffers. Resp. 66–68. We addressed this argument previously and do not find it undermines Petitioner's showing. *See* Sect. II.D.3.a–c.

Patent Owner further argues that there is no evidence that signal drivers 402/404 are enabled only during data bursts. Resp. 68–69. We addressed this argument previously and do not find that it undermines Petitioner's showing. *See* Sect. II.D.4.i.5.

(3) Enabling Bidirectional Drivers 402/404 Only During Data Bursts

Patent Owner contends, as argued for claim limitation 1e, "nothing in Ellsberry or prior art suggests that the signal driver 402/404 on the path

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between bus 230 and bus 234/236 is enabled for driving data only during the data burst period." Resp. 68–69. We addressed this argument previously and find that it does not undermine Petitioner's showing for claim limitation 1f. *See* Sect. II.D.4.i.5.

Therefore, Petitioner shows that Ellsberry alone or in combination with Halbert teaches limitation 1f of claim 1 of the '339 patent.

k) Summary/Conclusion for Claim 1

Petitioner has shown by a preponderance of the evidence that each and every limitation of claim 1 of the '339 patent is taught or suggested by Ellsberry alone or in combination with Halbert. In addition, Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would have modified or combined Ellsberry with Halbert with a reasonable expectation of success in arriving at the claimed invention. Accordingly, we determine that claim 1 is unpatentable as obvious over Ellsberry alone or in combination with Halbert.

5. Claims 11 and 27

Petitioner contends Ellsberry alone or with Halbert teaches all limitations of claim 11 and 27. Pet. 108–115 (claim 11), 134–139 (claim 27). Petitioner contends claim 11 is similar to claim 1 and recites a pair of 4-bit memory devices, as in claim 2. Pet. 108–115 (citing Ex. 1005, Figs. 2, 6, 11; Ex. 1003 ¶¶ 450–490). Petitioner contends claim 27 is like claims 1 and 10, and requires a write operation and a read operation. *Id.* (citing Ex. 1003 ¶¶ 609–659).

Patent Owner argues that claims 11 and 27 are patentable for reasons stated above for claim 1. Resp. 69. For the reasons stated above, we disagree. *See* Sect. II.D.4.a-k; Reply 37.

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Claim 27 includes limitation 27d5 that recites "the logic in response to the second module control signals is configured to enable the second set of tristate buffers for a second time period corresponding to the memory read operation to drive the respective n-bit section of the read data." Ex. 1001, 26:21–27. In relation to limitation 27d5, and in reference to Halbert's Figure 5, Patent Owner argues

> under Dr. Subramanian's/Petitioner's theory as to when the period starts, the second set of tristate buffers would be enabled for a time period shorter than that corresponding to a read operation. This is because according to Dr. Subramanian, the second tristate buffers would only be driving when there is data on DQ0 and DQ1 lines (see 44:10-46:25), but that period ends halfway between T9n and T10. But the data is driven until T10 when the read operation is completed (*id.*, 42:18-43:2), that is, after the period identified by Dr. Subramanian as the time that the second set of tristate buffers are enabled.

Resp. 69; Sur-Reply 32.

We do not agree with Patent Owner's argument. Each component of the memory module, including Halbert's bidirectional buffer 122 and bidirectional registers 126, 128, must remain enabled for the entire burst length (BL), i.e., second time period, during a read operation; otherwise, the data under transfer would be cut off. In this regard, Dr. Subramanian states the following:

> Halbert . . . discloses that the data paths are actively driven only during the data bursts. Ex.1006 at Figs 3, 5, and 6. For example, Halbert's Fig. 6 shows that a burst of four bits, a1, a2, b1, and b2 is received on DQ from the system and is actively driven in the internal busses of the data buffer, including busses MDQ and DQ0/DQ1 only for the duration of that data burst. *Id.* at Fig. 6 (reproduced below, annotated). I further note that, although Halbert changes the data rate on the data busses RDQ0 and RDQ1 coupled to the memory devices, those busses are still driven only for the duration of the respective data.

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Ex. 1003 ¶ 362.

In addition, Dr. Subramanian states

> A Skilled Artisan would have understood that these timing protocols for actively driving the data for a time period in accordance with latency parameters and the burst length are consistent with the industry standards at the time, including the JEDEC standards.

Id. ¶ 363. Thus, in making its argument, Patent Owner is conflating the time periods needed for data to pass through different components rather than considering that each component along the data path must be enabled for the "second time period" during a read operation.

Patent Owner's argument does not undermine Petitioner's showing with respect to claims 11 and 27.

6. Claims 3 and 14

Claim 3 depends from claim 2 and recites

> wherein the byte-wise data path further includes a set of write buffers configurable to receive the respective byte-wise section of the N-bit wide write data from the respective set of data signal lines before the first tristate buffers regenerate and drive the respective byte-wise section of the N-bit wide data to the second side of the each respective byte-wise buffer.

Ex. 1001, 20:19–25. Thus, claim 3 recites write buffers arranged in the byte-wise data path before tristate buffers. *Id.* Petitioner contends that Ellsberry alone or combined with Halbert teaches this feature. Pet. 89–93 (citing Ex. 1005 ¶¶ 12, 27, 45, 50, claim 2, Figs. 2, 4, 11; Ex. 1003 ¶¶ 395–407). Petitioner argues that claim 14, reciting a similar limitation as claim 3, is unpatentable for the same reasons. Pet. 115 (citing Ex. 1003 ¶¶ 497–502).

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> With respect to claims 3 and 14, Patent Owner argues
>
> if tristate functionality is inserted into signal driver 402 (and 404) and the driver is placed into Hi-Z, then that configuration would already present a single load without the need for the driver at bus 230. EX2007, 106:21-108:16. This would render the added write buffers redundant in functionality.

Resp. 70–71; *see also* Sur-Reply 32. Patent Owner argues that Petitioner is using improper hindsight instead of considering how one of ordinary skill in the art would have implemented the design. *Id.* at 71.

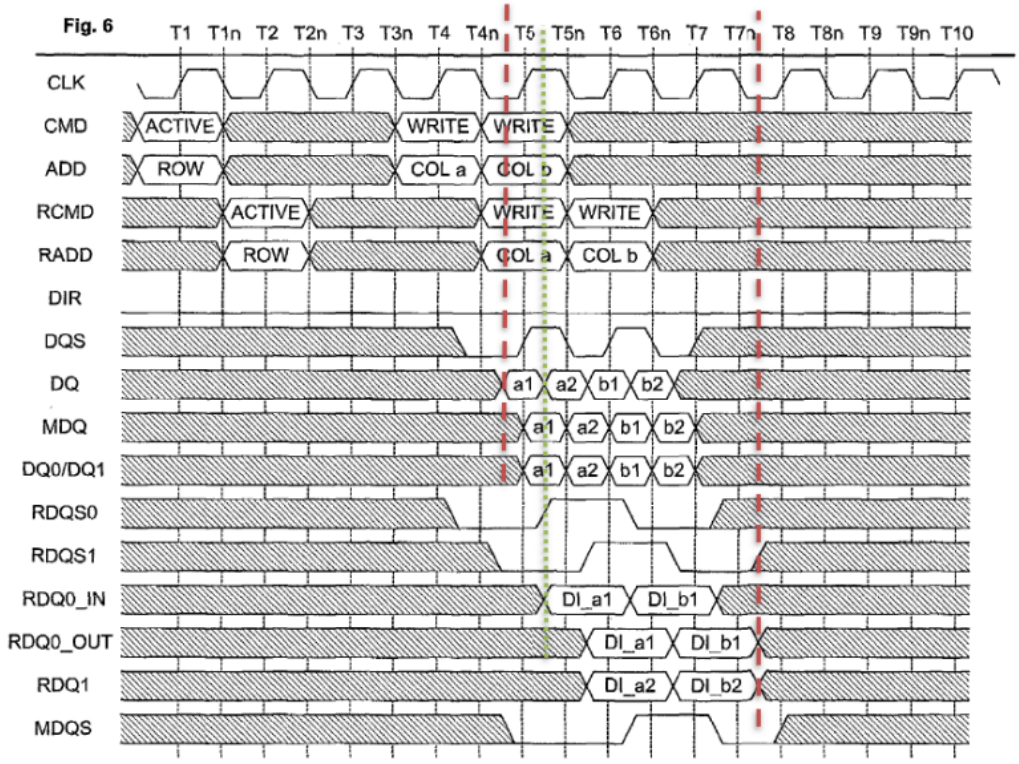
We do not agree with Patent Owner's argument, which is very similar to the one we previously addressed concerning the write operation. *See* Sect. II.D.3.b. Halbert's Figure 4 clearly teaches that the tristate buffers should interface with the system bus and memory buses, and one of ordinary skill in the art would have carried this teaching over to Ellsberry's memory module. Ex. 1003 ¶¶ 256–265.

7. *Claim 6*

Claim 6 depends from claim 1 and recites "wherein the logic is configurable to enable the first tristate buffers at a beginning of the first time period and to disable the first tristate buffers at an end of first time period." Ex. 1001, 20:36–39. Petitioner contends that Ellsberry alone or combined with Halbert teaches claim 6. Pet. 97 (citing Ex. 1005; Fig. 4; Ex. 1003 ¶¶ 421–423).

To explain its argument, Patent Owner presents Halbert's Figure 6 annotated by Patent Owner, as shown below.

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Resp. 72. Figure 6 of Halbert, above, depicts a timing diagram for two consecutive write operations for the memory module in Halbert's Figure 4. Ex. 1006, 3:9–10. In reference to annotated Figure 6, Patent Owner contends that Dr. Subramanian stated that the claimed "first time period" starts between T4n and T5 (depicted as a red dotted line) and ends between T7n and T8 (also depicted as a red dotted line) in Halbert's Figure 6. Resp. 71–72. Patent Owner further argues that Dr. Subramanian stated that the first tristate buffer is enabled after T5 (depicted as a green dotted line) and thus the "first time period" would be enabled after the beginning of the first time period, contrary to claim 6. *Id.* at 73–74.

As previously explained in Section II.D.5, each component along the data path must be enabled for the entire burst length (BL) or the data will be cutoff. Petitioner's contention is that the time it takes for the data to pass

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through each tristate buffer accords with the burst length (BL). Pet. 74; Reply 36. Dr. Subramanian's testimony is consistent with Petitioner's contention:

> The DQ is driven specifically approximately halfway between T4n and T5. And it is complete -- in this specific case where we are talking about a burst length of 4, it is complete halfway between T6n and T7. Of course, because there are propagation delays in the system, it continues to shift a little in time while the duration is maintained to account for the propagation delays.

Ex. 2007, 86:8–16. Thus, Patent Owner's argument overlooks that data passes through different components along a data path at different times. Resp. 72–74; Sur-Reply 32. Petitioner is correct that Ellsberry alone or combined with Halbert teaches that the first tristate buffers are enabled at the start of the first time period, which follows the additive latency (AL), and disabled afterward, the duration of which accords with the burst length (BL).

Patent Owner's argument does not undermine Petitioner's showing with respect to claim 6.

8. Claims 7, 16, and 21

Claim 7 depends from claim 1 and recites "wherein the module controller is configured to use the module control signals to control timing of the first time period in accordance with the latency parameter." Ex. 1001, 20:40–43. Claim 16 is similar. *Id.* at 22:55–58. Claim 21 is also similar but is directed to control timing for first and second memory operations using the latency parameter. *Id.* at 24:41–46.

Petitioner contends Ellsberry alone or combined with Halbert teaches claim 7. Pet. 98–99 (citing Ex. 1005, Fig. 4 (modified by Petitioner); Ex. 1003 ¶¶ 424–426). Petitioner contends that Ellsberry alone or with

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Halbert also teach claims 16 and 21 for the same reasons as claim 7. Pet. 116 (citing Ex. 1003 ¶¶ 506–508); Pet. 122 (citing Ex. 1005 ¶ 46; Ex. 1003 ¶¶ 563–565).

Patent Owner argues that Petitioner has not shown that Ellsberry includes a latency parameter as part of the signals sent to the memory bank switch via control bus 210. Resp. 74–75. Patent Owner also argues that there is no evidence that the CAS latency (CL) or additive latency (AL) are ever used to control operation of the switch ASICs. *Id.* at 75.

We disagree with these contentions because Petitioner has shown that Ellsberry teaches that the Posted CAS_n (AL) latency parameter is sent to and stored in the switch ASICs using an EMRS command, the JEDEC standard teaches that the AL latency parameter is sent using an EMRS command, and the '537 patent teaches to add a clock cycle to the latency parameter to account for propagation delay through a data buffer. *See* Sects. II.D.4.i.3, II.D.4.i.5; Ex. 1005 ¶ 44.

9. Claim 19

Petitioner contends that "[c]laim 19 is similar to claim 1 except that it requires a read operation rather than a write operation, and a second read operation similar to claim 10." Pet. 116. Petitioner contends that Ellsberry alone or combined with Halbert renders claim 19 obvious for similar reasons as claim 1. Pet. 116–120 (citing Ex. 1003 ¶¶ 515–550; Ex. 1005, code (57), ¶¶ 10, 12, 30, 32, 40, 45–47, 50, Fig. 8A; Ex. 1011, 6, 21–38, 46; Ex. 1051, 6, 24–41, 49).

Patent Owner argues that Ellsberry does not involve data path enablement or disablement. Resp. 75. As explained, we disagree. Ellsberry

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teaches "one-port-disabled" embodiments that enable or disable data paths using switch ASICs. *See* Sect. II.D.4.i.1.

Patent Owner also argues that Halbert does not disclose data paths enabled after the first period and before the second time period between memory operations. Resp. 75–76. As explained, although Halbert's Figure 6 shows data paths in a "don't care" state, as Petitioner contends, this does not preclude that they would be in the high-impedance state, and the JEDEC standards show that data paths are disabled between memory operations. *See* Sect. II.D.4.h.5; Ex. 1011, 22.

Patent Owner's arguments do not undermine Petitioner's showing with respect to claim 19.

10. Claim 28

Claim 28 depends from claim 27 and recites "wherein the logic is configurable to keep the first set of tristate buffers and the second set of tristate buffers disabled when the memory module is not targeted by the memory controller for any memory operations." Ex. 1001, 26:33–37.

Petitioner contends that Ellsberry alone or combined with Halbert teaches claim 28 for the same reasons stated for claims 6 and 19. Pet. 139–140 (citing Ex. 1003 ¶¶ 660–662). Petitioner contends the person of ordinary skill in the art would have understood that the system memory data bus can be shared by multiple modules. *Id.* at 139 (citing Ex. 1006, Fig. 8). Halbert's Figure 8 is reproduced below:

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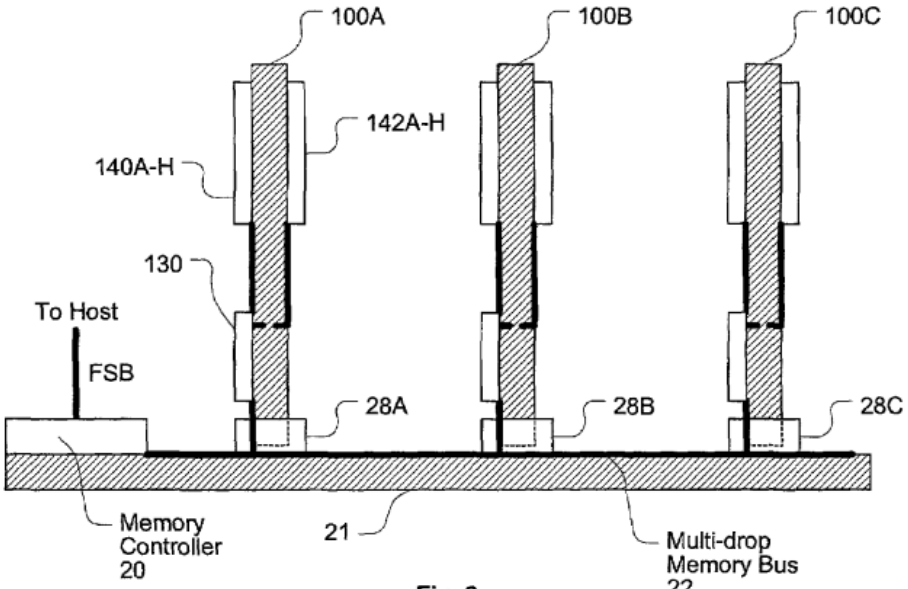


Fig. 8

Ex. 1006, Fig. 8. Halbert's Figure 8 shows that memory controller 20 is connected to memory modules 100A, 100B, 100C on a multi-drop memory bus 22. *Id.* at 7:54–61.

Petitioner contends that a person of ordinary skill in the art would have been motivated to disable the first and second sets of tristate buffers when the claimed memory module is not targeted by the memory controller for any memory operations to follow JEDEC timing protocols, save power, and avoid bus conflicts on the multi-drop memory bus, among other reasons. Pet. 140 (citing Ex. 1005 ¶ 46; Ex. 1035, 89–90, 132–133).

Patent Owner repeats arguments we have considered and rejected, including that Ellsberry is silent as to when its write drivers are enabled or disabled; and that Halbert's write drivers are enabled even when there are no memory operations. Resp. 77–78. As discussed, Ellsberry discloses "one-port-disabled" embodiments that selectively enable or disable write drivers associated with Ports A and B to write data to one bank or the other. *See* Sect. II.D.4.i.1. Although Halbert's Figure 6 shows write drivers enabled

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when no memory operations are under way, there is no statement in Halbert prohibiting disabling the write drivers may occur when there are no memory operations, and the JEDEC standard teaches that they should be disabled at that time. *See* Sect. II.D.4.i.5.

11. Claim 34

Claim 34 depends from claim 27 and recites "wherein the first set of tristate buffers are enabled for the first time period in accordance with a latency parameter." Ex. 1001, 28:23–25.

Petitioner contends that Ellsberry alone or with Halbert discloses claim 34 for the same reasons stated for limitation 1f of claim 1 and claim 7. Pet. 144 (citing Ex. 1003 ¶¶ 705–707).

Patent Owner again argues that Ellsberry is silent with respect to enabling or disabling drivers. Resp. 78. As discussed, Ellsberry discloses "one-port-disabled" embodiments which enable and disable data paths and thus we do not agree with Patent Owner's argument. *See* Sect. II.D.4.i.1.

Patent Owner also argues that Halbert's drivers are in a "don't care" state, and thus are always enabled, and could not be enabled in accordance with a latency parameter. Resp. 78–79. As explained, Halbert's Figure 6 does not preclude high-impedance states for data paths, and JEDEC teaches to disable the data paths when not performing a memory operation. *See* Sect. II.D.4.h.5; Ex. 1006, Fig. 6; Ex. 1011, 22.

12. Claims 2, 4, 5, 8–10, 12, 13, 15, 17, 18, 20, 22–26, 29–33, and 35

Petitioner contends that claims 2, 4, 5, 8–10, 12, 13, 15, 17, 18, 20, 22–26, 29–33, and 35 are unpatentable as obvious over Ellsberry alone or with Halbert. Pet. 86–89, 93–96, 99–108, 115–116, 120–134, 140–145.

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Patent Owner presents no additional arguments specific to these claims except for claims 10 and 18. *See* Resp. For claims 10 and 18, Patent Owner argues that these claims involve both read and write, and that the data paths for both are disabled when there are no read or write operations. Sur-Reply 32. Patent Owner argues the prior art does not teach independent control of read/write data paths. *Id.*

"A sur-reply may only respond to arguments raised in the corresponding reply and may not be accompanied by new evidence other than deposition transcripts of the cross-examination of any reply witness." 37 C.F.R. § 42.23(b). Patent Owner's argument concerning disablement of both data paths when there are no read or write operations, and independent control of the read and write data paths, amounts to new argument. This new argument further is not supported by corresponding language in the claims. To the extent this argument is not new, we have addressed it with respect to claim 27. *See* Sect. II.D.5.

We have carefully reviewed Petitioner's contentions in relation to these claims. Petitioner has shown by a preponderance of the evidence that the combination of Ellsberry and Halbert, when considered with the general knowledge of a person of ordinary skill in the art at the time of the '339 patent, discloses all of the limitations of claims 2, 4, 5, 8–10, 12, 13, 15, 17, 18, 20, 22–26, 29–33, and 35.

13. Conclusion

Petitioner has shown by a preponderance of the evidence that a person of ordinary skill in the art would have combined Ellsberry and Halbert with a reasonable expectation of success for the reasons Petitioner contends. We further determine that the Ellsberry alone or in combination with Halbert,

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when considered in conjunction with the general knowledge that a person of ordinary skill in the art would have had, as represented, for example, by the JEDEC standards and the '537 patent, teaches and suggests each and every limitation of claims 1–35. Accordingly, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–35 are unpatentable as obvious over the combination of Ellsberry and Halbert.

E. Collateral Estoppel

Petitioner raises collateral estoppel as precluding Patent Owner from re-litigating the patentability of the claims in the '339 patent. Pet. 41–44; Reply 1–2. As we have decided this case on the merits, we need not, and do not, reach Petitioner's collateral estoppel arguments.

F. Motion to Exclude

Petitioner seeks to exclude Exhibits 2006, 2009, 2012, and 2020–2024. Paper 38. Because we do not rely on any of these Exhibits in a manner adverse to Petitioner, we dismiss the Motion to Exclude as moot.

III. CONCLUSION

For the foregoing reasons, we determine that Petitioner establishes by a preponderance of the evidence that claims 1–35 of the '339 patent are unpatentable.

IV. ORDER

Accordingly, it is:

ORDERED that claims 1–35 of the '339 patent have been shown to be unpatentable;

FURTHER ORDERED that Petitioner's Motion to Exclude is moot;

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FURTHER ORDERED that any party seeking judicial review must comply with the notice and service requirements of 37 C.F.R. § 90.2.[6]

In summary:

Claim(s)	35 U.S.C. §	Reference(s)/Basis	Claim(s) Shown Unpatentable	Claim(s) Not shown Unpatentable
1–35	103	Ellsberry, Halbert	1–35	

[6] Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner's attention to the April 2019 Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding. *See* 84 Fed. Reg. 16,654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. *See* 37 C.F.R. § 42.8(a)(3), (b)(2).

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