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Impact of Line Voltage Sag on Switch Mode Power Supply Operation

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ABSTRACT

Switch-mode power supplies (SMPS) provide lowvoltage dc power to almost every type of computer, control and instrumentation equipment. As such, the performance of this equipment operating in unprotected ac supply systems reflects the behavior of the SMPS to the voltage surges and sags that are endemic to power systems not protected by UPS. One purpose for this paper is to analyze the operation of SMPS during line voltage sags over and above merely observing the discharge of the dc link capacitor. A further purpose is to show that the tolerance of an SMPS to line-voltage sags can be improved by: (1) using a larger dc capacitor; (2) operating at less than the power rating; and (3) using power factor correction. Inrush current control circuits must be designed to operate effectively for line voltage sags of all predictable depths and time durations. Moreover, voltage disturbance plots of events do not indicate SMPS failures for each event outside the ITI limits. A percentage of SMPS will be operating at part load and not fail.

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***Abstract* - Switch-mode power supplies (SMPS) provide low-voltage dc power to almost every type of computer, control and instrumentation equipment. As such, the performance of this equipment operating in unprotected ac supply systems reflects the behavior of the SMPS to the voltage surges and sags that are endemic to power systems not protected by UPS.**

One purpose for this paper is to analyze the operation of SMPS during line voltage sags over and above merely observing the discharge of the dc link capacitor. A further purpose is to show that the tolerance of an SMPS to line-voltage sags can be improved by: (1) using a larger dc capacitor; (2) operating at less than the power rating; and (3) using power factor correction. Inrush current control circuits must be designed to operate effectively for line voltage sags of all predictable depths and time durations. Moreover, voltage disturbance plots of events do not indicate SMPS failures for each event outside the ITI limits. A percentage of SMPS will be operating at part load and not fail.

***Index Terms*: Line voltage sag, SMPS, inrush current control.**

I. Introduction

Commercial facilities, automated factories, transportation systems and residences are replete with computers, PLCs, sensors, robots, CNC controlled machines, and other electronic systems [1]. A common characteristic is that all incorporate SMPS to provide dc power. Line voltage sags shut down and/or damage SMPS with consequent shut down of the host equipment. Quoting Bendre et. al., "The impact of voltage sags on equipment has not been studied in detail, and the interactions are poorly understood." [2].

This paper addresses the failure of SMPS to provide the required dc power output during and following line-voltage sags. Obviously, not all degrees of sag nor types of SMPS can be covered. We will address the cause of failure on, (1) depth and duration of voltage sag; (2) design and loading of representative SMPS.

II. Types of SMPS to be Considered

Practically all SMPS utilize the basic rectifier design of Fig. 1. The circuit consists of an input rectifier, dc capacitor, and a dc-dc converter. The converter consists of a switcher, high-frequency transformer and output rectifier. As examples, three types of SMPS, defined by the line voltage-to-rectified dc power circuit, will be considered as follows:

1. Diode-bridge rectifier with filter
2. Diode-bridge rectifier with current inrush control
3. Rectifier with input power-factor control

These rectifier input circuits are selected by designers to meet the requirements of dc power, harmonic standards, ac line voltage range, and, of course, cost [3].

III. Diode Bridge Rectifier

Fig. 1 shows an input circuit for an SMPS that utilizes an inductor between the rectifier and the capacitor. The capacitor provides filtering and the energy during a line-voltage sag that may prevent a dip in the SMPS output voltage. The LC circuit is designed to reduce line-current harmonics to the levels set by conducted and radiated emissions standards. This circuit will serve as the initial model for the analyses in this paper.

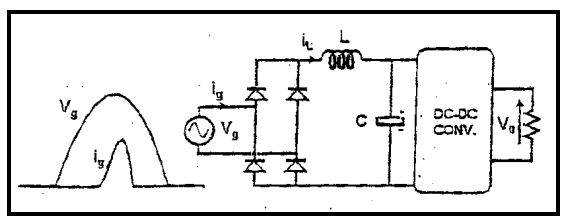

Fig. 1. Diode-Rectifier Input Circuit [3].

For example, assume that the circuit must operate under the following conditions:

Vline = 85-to-130 Vrms, 115 Vrms nom.
P = 100 W to the dc-dc converter

During a line voltage sag, as the capacitor discharges, the dc-dc converter will deliver rated dc output voltage until the

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capacitor voltage reaches a minimum value V min, set by the design of the input circuit to the converter. Assume that this voltage is 1/3 of the maximum line voltage, or 1/3 x 130 = 43.3 Vrms, or 61.3 Vpk [4]. The time to reach this voltage at rated load is defined as the hold up time t_h. If the SMPS operates during an extended sag of 43.3 V at rated power, the line current is increased by 115/43.3 =2.66 times rated current until the line voltage is restored. The value of the capacitor C can be calculated under the assumption that the capacitor charges to the peak of the rectified ac voltage and the energy transfer to the dc-dc converter is lossless by the equation [3]

$$C = \frac{2 \times P \times t_h}{(V^2nom - V^2min)}$$

where Vnom and Vmin are the peak values.

The tolerance curves for line voltage vs. time per ITIC and SEMI F47 standards shown in Fig. 2 will be used to demonstrate the selection of capacitor C for the SMPS to tolerate a line-voltage sag [4]. To tolerate a worst-case sag within the ITIC limits a sag to point "a" in Fig.2, a voltage sag from nominal line voltage of 115 V, 162.6 Vpk, to zero with rated output voltage, and power, the capacitor must discharge to Vmin, or 61.3 Vpk to maintain the operation of the dc-dc converter. The capacitor must have a value at least,

$$C = \frac{2 \times 100 \times 0.02}{(162.6)^2 - (61.3)^2} = 176\ \mu F$$

Figs. 5 to 8 show the capacitor voltage as a function of time.

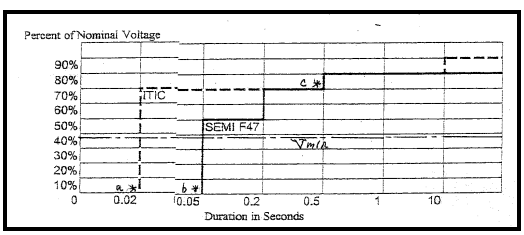


Fig. 2. Voltage Tolerance Curve [4].

It is obvious that the capacitor can be selected to meet the requirement for voltage sags to zero voltage for the ITIC curve, 0.02s, or the SEMI F47 curve, 0.05 s, in Fig. 2. A line voltage sag of 0.05 s, or 3 cycles of 60 cycles, is considered as typical for utility events, such as line recloser operations, line fuse blowing, and switching. To meet the requirements for the SEMI F47 curve to point "b" in Fig. 2, the capacitor value must be multiplied by 0.05/0.02 = 2.5, or 440 µF. The line voltage sag to point "c" in Fig. 2, 0.5 s, to 70% of nominal voltage, is higher than Vmin, 37.6%, so that the dc-dc converter will process the rectified voltage without relying on the capacitor energy. When larger capacitors are utilized to tolerate longer-duration voltage sag, the inrush line current increases and the power supply becomes bulkier.

Obviously the SMPS will be more tolerant of the duration of line-voltage sags as the load power is reduced for the same capacitor size. This is shown by the voltage tolerance limits in Fig. 3 as load is reduced from 100% to 25%; allowable sag to zero line voltage, time increases from 0.02 s to 0.08 s. For longer time sags, the minimum line voltage is set by the dc-dc converter. Fig. 4 presents a voltage disturbance scatter plot of events recorded at an industrial facility over a period of one year. For this plant there were a total of 77 recorded short duration voltage sags [2]. Of these, approximately 16 were outside the ITI curve indicating that even if the plant equipment met the ITI requirements, there could be up to 16 process interruptions in a year.

Fig. 3 also shows that in the real world an SMPS might not be fully loaded at the time the voltage sag is outside the ITI limits, as shown in Fig 2, and survive. A plot, such as Fig. 4, does not show that every connected SMPS will fail to produce rated dc output voltage. Each event outside the ITI limits on the plot for an individual facility may affect 100 SMPS, for example, of which only 10 may be operating at rated load and be affected. In summary the ability of the SMPS to tolerate line voltage sags can be controlled by the capacitor size, the percent load, and the minimum voltage for the converter to operate.

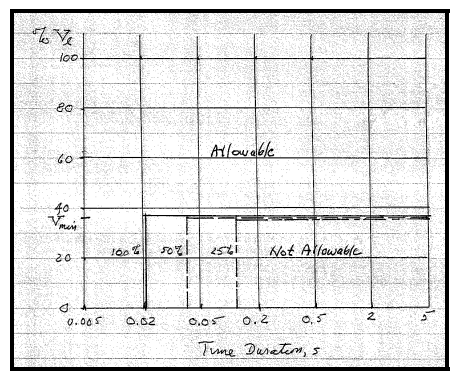


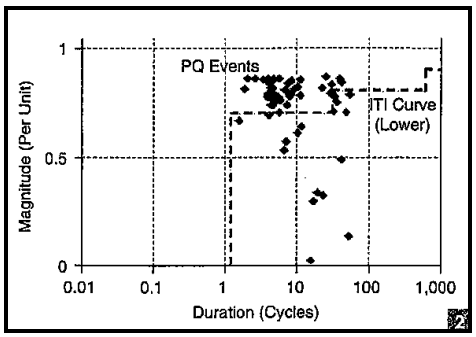
Fig. 3. Voltage tolerance to zero line voltage as a function of loading.

IV. SMPS WITH CURRENT INRUSH CONTROL

The dc capacitor bank typically uses filter capacitors that have a low equivalent series resistance (ESR) and a low equivalent series inductance (ESL), with associated high short circuit current capacity [5]. Depending on the application, the total filter capacitance may be of a relatively large value, ranging from a few hundred µF to thousands of µF depending upon the rated power. At start-up, due to the low source line impedance and due to the low impedance of the dc capacitor,

the peak charging current can be extremely high, typically of the order of hundreds to thousands of amps. This high inrush current can have a degrading effect on the input components including the dc capacitor, the diode bridge and copper traces on the printed circuit board. Additionally, this high inrush current may result in the generation of high EMI with the possibility of interference to neighboring electronic devices.

Typically, a pre-charging circuit is used to charge the capacitor using an inrush current limiter. In low power applications, this current limiting is provided by a negative temperature coefficient (NTC) resistor. The NTC has a high resistance when cold but a relatively low resistance when hot. Thus, the current is limited at startup by the NTC, and under normal operation, the relatively low resistance results in a small voltage drop. For high power applications, a pre-charging resistor is used to charge the dc capacitor bank. When the capacitor bank is almost fully charged, the pre-charging resistor is bypassed by a power contactor.



Fig, 4. Voltage disturbance at a major U.S Industrial Facility over a 12-month period [2].

A. *Analysis of Inrush Current*

During short duration voltage sags, the capacitor may discharge for several cycles, without re-setting the soft-start circuit. For the NTC (thermal time constant of several tens of seconds), a sag of a few cycles is insufficient to allow the NTC to cool. Similarly, a sag of a few cycles may be insufficient for the bypass contactor circuit to reset [2]. Thus, when ac power is re-applied, the inrush current pulse may be dramatically different from normal operation with the pre-charge circuit limiting the inrush current. In such instances, the inrush current may be substantially higher. The amplitude of the high peak current is dependant on the source impedance of the incoming line. Ref [2] also presents a simplified analysis with the voltage sag assumed to begin and end at the peak of the line voltage. The capacitor voltage decay and the resultant initial current pulse are given by:

$$\Delta V = I_o T_{60} / 2 C_{dc} \qquad (1)$$

$$I_p = (2N - ½) \Delta V / (L_s/C_{dc})^{½} \qquad (2)$$

where

ΔV is the capacitor voltage decay
I_o is the load current; T_{60} is the 60-cycle period
C_{dc} is the filter capacitor; I_p is the initial current
N is the number of cycles of sag
L_s is the lumped input line inductance

Under normal operating conditions, the capacitor is essentially charged to close to the peak of the ac line voltage (V_p) plus $\Delta V/2$ [2]. This assumes that the depth of the voltage sag is greater than ΔV. Calculations indicate that for a filter capacitor of 7,500 µF, and a load current of 20 A, ΔV= 22.2 Vdc. Thus for a 120 Vac system, with the above conditions, the peak capacitor voltage is approximately 180.8 V, and exceeds the peak line voltage of 169.7 V.

B. *PSpice Computer Simulation*

Fig. 5-8 present PSpice computer simulation waveforms for a simplified 120 Vac single phase bridge rectifier circuit with a 7,500 µF filter capacitor. The input line inductance is represented by a lumped value of 10 µH. The simulated voltage sag is for 3 cycles (0.05 s). Two test conditions were simulated for the condition that the precharge circuit does not reset:

1. Voltage sag to begin and end at approximately the peak of the line voltage (Fig. 5 and 7). Equations of this simplified analysis are presented in [2].

2. Voltage sag to begin and end at approximately the zero crossing of the line voltage (Fig. 6 and 8). No equations are presented in [2] for this condition.

Fig. 7 presents the PSpice voltage and current waveforms for the 7,500-µF filter capacitor for a 20 A load for test condition 1 with the voltage sag to begin and end at approximately the peak of the line voltage. Under steady-state conditions, the peak capacitor voltage is approximately 177.5 V which agrees within 2 % of the above calculated value of 180.8 V to verify the model. This voltage exceeds the peak line voltage of 169.7 V.

Fig. 7 also presents the PSpice waveforms with an expanded time scale for the 7,500 µF filter capacitor at the end of the 3 cycle sag. Using the simplified analysis of [2], the calculated peak voltage is approximately 292 V. The PSpice simulation voltage of approximately 274 V is within 6.5% of the calculated value. From Fig. 7, it is observed that the capacitor voltage has a fast rise time of the order of 300 V/ms and a high peak current of approximately 3,250 A. Solving (2) results in a peak current of approximately 3,350 A which is within approximately 3 % of the simulated value.

The PSpice simulation also indicates that the filter capacitor is subjected to a high di/dt of the order of 4.5 A/µs. These high peak currents and voltages and the high rate of rise may be damaging to the diodes, fuses, capacitors and other components. As stated in [2], component I^2t rating may also be exceeded, hence overstressing the components and resulting in a premature failure.

Fig. 6 and 8 present the PSpice voltage and current waveforms for the 7,500 µF filter capacitor with the sag voltage beginning and ending at approximately the zero crossing of the line voltage. The simulated voltage and peak currents are lower than in the previous test condition. Moreover, it is observed that there are two adjacent charging current pulses to the filter capacitor. Furthermore the simulation shows that the capacitor voltage ratchets up to its final value without the overshoot of the previous condition.

In summary, we see that a precharge circuit might not act at the end of a voltage sag to prevent a damaging peak current to charge the capacitor.

V. Rectifier with Input Power Factor Control

In power factor corrected front-ends of SMPSs, the line current is shaped to improve the power factor and thus conform to standards on input line current harmonics. In Europe, power supplies drawing between 75 and 600 W must comply with EN-61000-3-2 Class D which specifies limits on the amplitude of odd line harmonic content up to the 39th harmonic [6]. The limits depend on the rating of the power supply; for a 100 W switching power supply the harmonic limits are 0.34 A for the 3rd, 0.19 A for the 5th, 0.1 A for the 7th, and so on as shown in Table 1. Currently in the USA, there is no standard for the magnitude of the input line current harmonics for computer switching power supplies. However, manufacturers who want to sell world-wide are designing to the EN-61000-3-2 standard.

Issues related with offline rectifiers with and without power factor correction will next be investigated with a 180W converter case study.

A. *Offline Diode Rectifier*

Fig 9[1] shows the line voltage and line current for a typical 120 Vac, 60 Hz front-end rectifier. The line current consists of narrow spikes, corresponding to the charging time of the bus capacitor. The output power is 174 W (Vo = 166 V with 8 Vpp ripple), with a poor power factor of ~ 36%. The spectrum of the line current is rich in harmonics, well in excess of EN-61000 limits. A further disadvantage is the tradeoff between rectifier filter time constant and line harmonics; if the value of the filter capacitor is increased to improve voltage sag mitigation, the line current harmonics get worse.

TABLE 1

EN-61000-3-2 Line Current Harmonic Limits for Class D (Computer Equipment)

Harmonic order N	Permissible harmonic current (mA/Watt)
3	3.4
5	1.9
7	1.0
9	0.5
11	0.35
13	0.296
15 < N < 39	3.85/N

B. *Passive Power Factor Correction (PFC)*

The waveforms of Fig. 10 show the effect of adding an input line reactor, 1 mH. Though the output power decreases to 170 W, the power factor improves significantly to 60%.

C. *Active PFC using a Boost Converter*

Fig. 11 shows the waveforms for a boost dc-dc converter with front-end signal processing to achieve a power factor approaching 100%. In this 100 kHz converter (boost L=1 mH and boost C=200 µF), the line current I_{in} is shaped by a variation in the duty cycle of the MOSFET switch. The output power is 183 W (output voltage Vo=428 V into a 1 kΩ load). The line current is in phase with the line voltage, and has very little harmonic content resulting in a power factor of 98.5%, and harmonics that pass the EN61000-3-2 limits shown in Table 2. Voltage sag mitigation is good since the duty cycle of the converter will adjust to maintain constant power. The converter can also ride-through an outage of several cycles, with the output voltage droop set by the time constant of the 200 µF, 1 kΩ load. If a longer time constant is needed, the capacitor can be increased with little effect on power factor.

The non-PFC and PFC input circuits operate differently during a line-voltage sag. Consider two cases for an SMPS with a capacitor sized to carry rated load for a 0.05 s sag:

1. <u>Line voltage sags to Vmin for 0.05 s:</u> For the non-PFC, the capacitor voltage reverse biases the rectifier as it discharges to Vmin. The line current is zero. A line-current spike occurs when line voltage is restored. For the PFC, the boost converter continues to take energy from the line during the line voltage sag. The line current increases to 1/Vmin (pu), or ~ 2.7 pu at constant power.

[1] Simulations performed using Powersim, Inc.'s PSIM simulator. demo version 7.1. The 160 Ω load models the load current of the DC/DC converter.

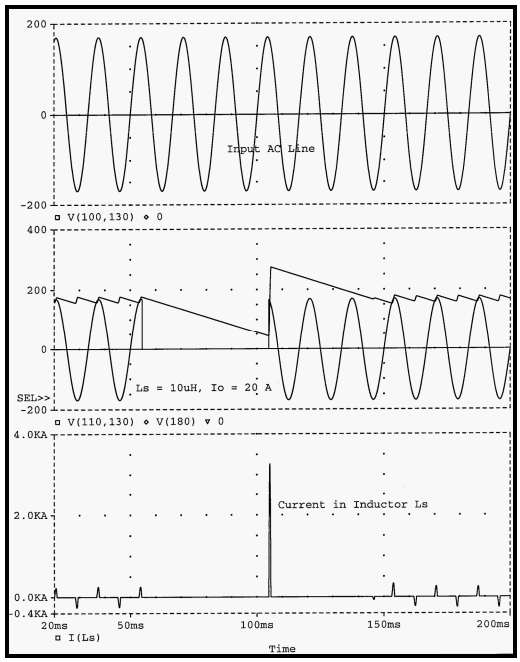


Fig. 5. Top waveform: Input AC Voltage
Middle waveform: Capacitor voltage, Sag voltage
Bottom waveform: Input line current

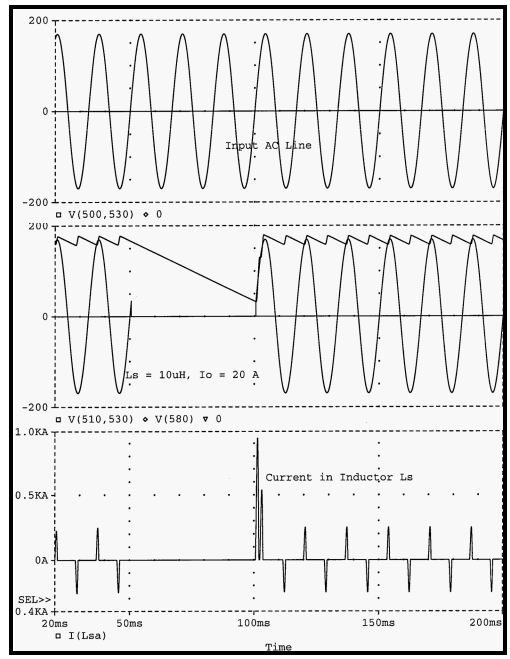


Fig. 6. Top waveform: Input AC Voltage
Middle waveform: Capacitor voltage, Sag voltage
Bottom waveform: Input line current

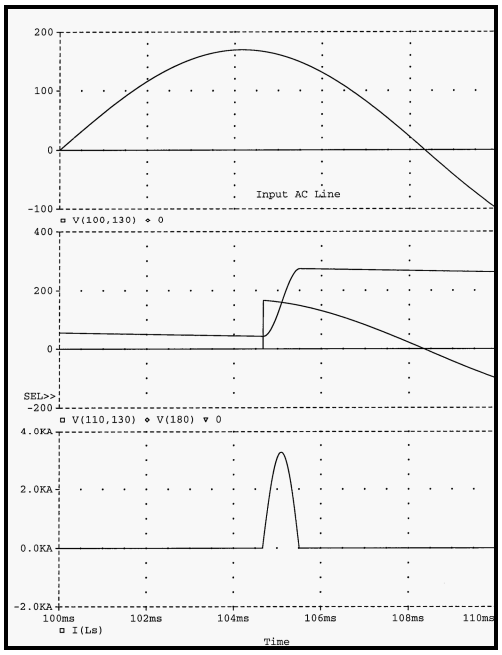


Fig. 7. Expanded Time Scale
Top waveform: Input AC Voltage
Middle waveform: Capacitor voltage, Sag voltage
Bottom waveform: Input line current

Test Condition: Voltage sag begins and ends at approximately the peak of the line voltage.

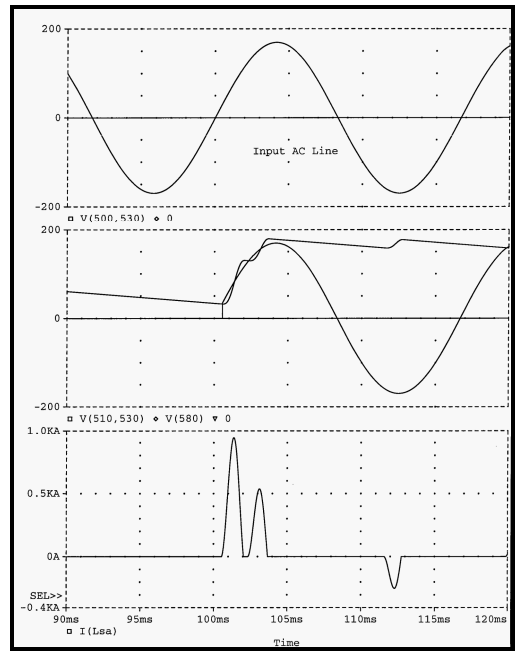


Fig. 8. Expanded Time Scale
Top waveform: Input AC Voltage
Middle waveform: Capacitor voltage, Sag voltage
Bottom waveform: Input line current

Test Condition: Voltage sag begins and ends at approximately the zero crossing of the line voltage.

2. Line voltage sags to zero for 0.05 s: Both the non-PFC and the PFC take energy from the capacitor, as it discharges to Vmin. The line current is zero. When line voltage is restored, for the non-PFC, the line current appears as a spike; for the PFC, the line current is controlled.

Table 2.
EN-61000-3-2 SIMULATED VS. LIMITS FOR 183 W BOOST CONVERTER

Harmonic order N	Permissible harmonic current (A)	Simulated harmonic current (A)
3	0.62	0.1
5	0.35	< 0.1
7	0.18	< 0.1
9	0.09	<< 0.1

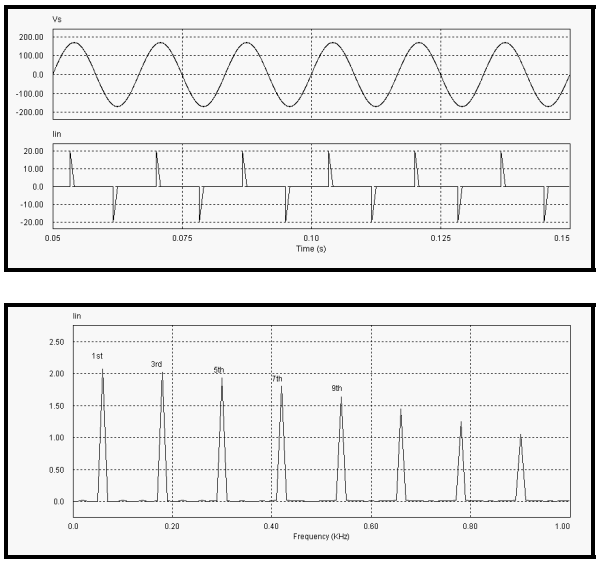


Fig. 9. Top: Waveforms showing line voltage (top trace) and line current (bottom trace) for a full-wave rectifier front end for a SMPS. Bottom: Spectrum of line current.

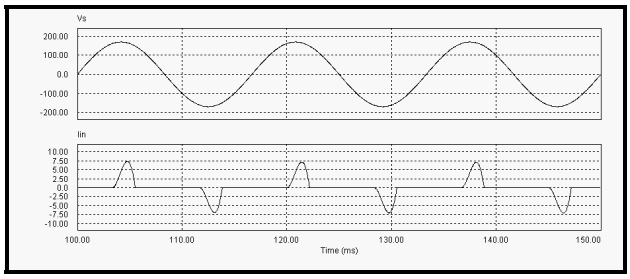


Fig. 10. Waveforms, showing line voltage (top trace) and line current (bottom trace) for a full-wave rectifier front end for a SMPS with line reactor.

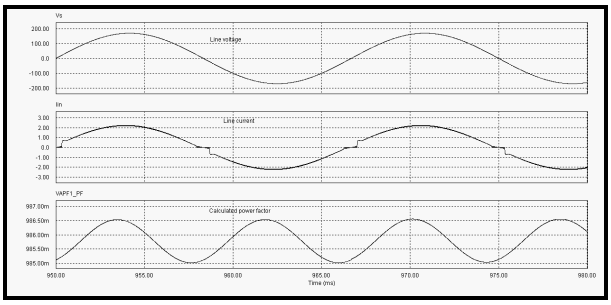


Fig. 11. Waveforms, showing line voltage (top trace), line current (middle trace) and calculated power factor (bottom trace) for a boost PFC rectifier for a SMPS.

VI. CONCLUSIONS

1. The tolerance of an SMPS to line-voltage sags can be improved by: (1) using a larger dc capacitor; (2) operating at less than the rated power; (3) reducing the minimum voltage for the dc-dc converter; (4) employing a front end power-factor control circuit.

2. Inrush current control circuits must be designed to operate effectively for line voltage sags of all predictable depths and time durations.

3. Voltage disturbance plots of events do not indicate SMPS failures for each event outside the ITI limits. Statistically, a percentage of SMPS will be operating at part load and will not fail.

4. During a line-voltage sag, the minimum capacitor voltage is set by the design of the dc-dc converter. For a power-factor corrected SMPS, the minimum line voltage is set by the allowable line current at constant input and output power.

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